Chapter 4

Hardware Functional Overview

4.1 Overview

The FIC A360 consist of several major functions and subsystems including:

- System Processor – implemented on the motherboard using the Intel Pentium-III or Celeron with FC-PGA packaging at 100/133MHz system bus speed.
- System North Bridge Core Logic – implemented on the motherboard using the VIA Twister chipset.
  - SMA (Share Memory Architecture)
  - Savage IX AGP 3D Graphics Accelerator
- System South Bridge Core Logic – implemented on the motherboard using the VIA VT82C686B PCI-to-ISA chipset.
  - Enhanced IDE Interface for HDD, CD-ROM, and IDE Device Bay
  - SoundBlaster/DirectSound AC97 Digital Audio Controller
  - USB Interface for the external USB port
  - Super I/O
- Clock Frequency Generator – implemented on the motherboard using the IMI 9806I clock generator chip.
- Cache Memory Subsystem – implemented on-die on the Intel CPU.
- Video Subsystem – integrated on the motherboard using S3 Savage IX VGA chip and on the LCD Panel for supporting the LCD and CRT.
- PCMCIA Subsystem – implemented on the motherboard using the O2Micro OZ6933 PCI-CARDBUS BRIDGE controller chip.
- Audio Subsystem – implement included on the VT82C686B.
- Keyboard and Pointing Device Subsystem – implemented on the AIO board, the Keyboard assembly, and the Glidepad assembly.
- I/O Subsystem – implement included on the VT82C686B.
- Modem Feature Card – implemented on the motherboard via the mini-PCI bus module socket.
- Power Subsystem – implemented on the battery board, LCD Inverter Board, Battery Pack, and AC adapter.
- Micro-P Subsystem – implemented on the motherboard using Mitsubishi PMU07.

4.2 System Hardware Block Diagram

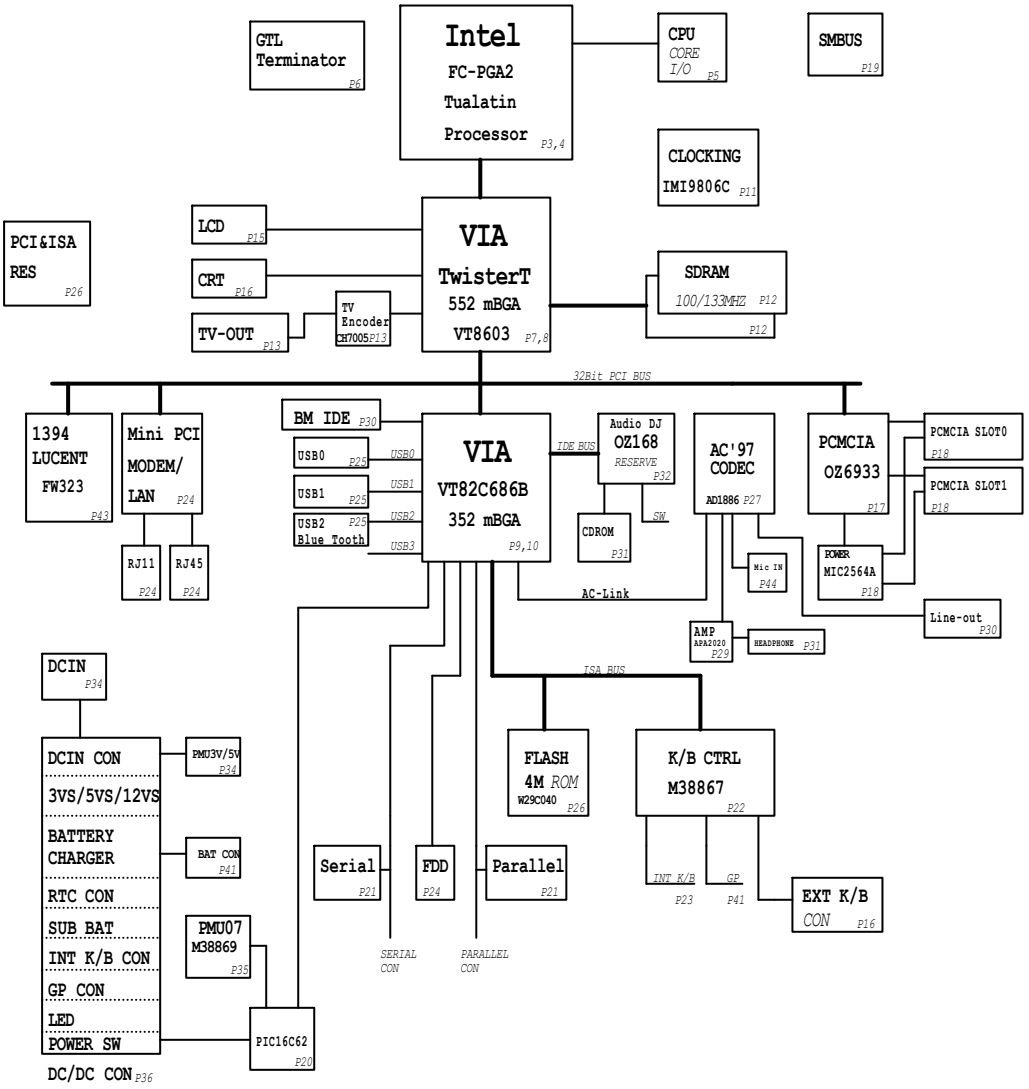

Figure 1-1 A360 Block Diagram

4.3 Chipset Summary

The notebook consists of following major chipsets:

Controller Chip	Vendor	Description
Processor	Intel	FC-PGA Pentium III 933 / 1G / 1.3GMHz FC-PGA Celeron 766 / 800MHz
Core Logic	VIA	Twister + VT82C686B
Video Controller	S3	Savage IX
PCMCIA Controller	O2Micro	OZ6933
Supper I/O Controller	VIA	Integrated in South Bridge (VIA VT82C686B).
Audio Chip	VIA	Integrated in South Bridge (VIA VT82C686B)
Audio Amplifier	APEC	APA2020
Keyboard Controller	Mitsubishi	M38867
PMU Controller	Mitsubishi	PMU07, Mitsubishi M38867M(E)SA-xxxHP
Gas Gauge IC		Included in PMU07
ROM BIOS	SST	28SF040-12
Clock Generator	IMI	IMI 9806I
Temperature Sensor	NS	MAXIM-1617
USB Hub		Integrated in South Bridge (VIA VT82C686B)
Modem (Type 3B)	ASKEY	1456VQL19R-4 Mini-PCI Solution (Type-3B)
IEEE1394	Agere	FW-323

4.4 System Processor (CPU)

The FIC A360 runs on Intel Pentium-III based on FC-PGA packaging. It supports CPU with up to 1GHz clock speed rating. The processor operates in conjunction with the RAM and ROM memory and the system control logic (e.g. VIA Twister) to process software instructions (BIOS, Windows, and Applications).

4.4.1 Intel Pentium-III Features

Using Intel' s advanced 0.18 micron process technology, the Intel mobile Pentium III processor is offered at speeds of 700MHz to 1GHz while still offering lower power for long battery life. Other performance advancements include the addition of new Internet Streaming SIMD instructions, the advanced transfer cache architecture, and a processor system bus speed of 100MHz.

Intel Mobile Pentium III processor featuring Intel SpeedStep technology is the next dramatic step towards achieving near desktop performance. This exciting new processor has two performance modes and allows real-time dynamic switching of the voltage and frequency between the modes. This occurs by switching the bus ratios, core operating voltage, and core processor speeds without resetting the system.

There are two performance modes offered, Maximum Performance and Conserved Performance. Maximum Performance mode provides near desktop performance and runs at 700, 750, 800 and 850 MHz. Conserved Performance mode provides the best balance between performance and battery life and operates at a lower frequency of 550, 600, 650, 700 MHz. You can check the table of two performance modes as following.

The integrated L2 cache is designed to help improve performance, and it complements the system bus by providing critical data faster and reducing total system power consumption. The Pentium III processor's 64-bit wide Gunning Transceiver Logic (GTL+) system bus provides a glue-less, point-to-point interface for an I/O bridge/memory controller.
Features summary of the Pentium-III CPU:

- Processor core/bus speeds
  - Featuring Intel SpeedStep technology: Maximum Performance Mode at 1.60V and Conserved Performance Mode at 1.35V
- Supports the Intel Architecture with Dynamic Execution
- On-die primary (L1) 16-Kbyte instruction cache and 16-Kbyte write-back data cache
- On-die second level L2 cache (256-Kbyte)
- Integrated GTL+ termination
  64-bit data bus, 100-MHz operation
- Integrated math co-processor
- Intel Processor Serial Number
- Fully compatible with previous Intel microprocessors
  - Binary compatible with all applications
  - Support for MMX technology
  - Support for Streaming SIMD Extensions enhances floating point, video, sound, and 3-D application performance
- Power Management Features
  - Quick Start for low power, low exit latency clock "throttling"
  - Deep Sleep mode provide low power dissipation
- On-die thermal diode

4.4.2 Intel Celeron Features

The Intel Celeron processor is designed for uni-processor based Value PC and is binary compatible with previous generation Intel architecture processors. The Intel Celeron processor provides good performance for applications running on advanced operating systems such as Windows 98 / Me, Windows NT / 2000, and UNIX. This is achieved by integrating the best attributes of Intel processors – the dynamic execution performance of the P6 micro-architecture plus the capabilities of MMX technology – bringing a balanced level of performance to the Value PC market segment.

Features summary of the Celeron CPU:

- Available up to 700 MHz core frequencies
- Integrated primary (L1) 16-Kbyte instruction cache and 16-Kbyte write back data cache
- Integrated second level (L2) cache 128-Kbyte ECC protected cache data array
- Intel's latest Celeron processors in the FC-PGA package are manufactured using the advanced 0.18 micron technology.
- Binary compatible with applications running on previous members of the Intel microprocessor line.
- Supports the Intel Architecture with Dynamic Execution
- Specifically designed for uni-processor based Value PC systems, with the capabilities of MMX technology.
- Power Management Features. Quick Start for low power, low exit latency clock "throttling" and Deep Sleep mode for extremely low power dissipation.
- Optimized for 32-bit applications running on advanced 32-bit operating systems.

- UPGA-2 packaging technology for thin form factor notebook designs. Exposed die enables more efficient heat dissipation.
- Low-Power GTL+ processor system bus interface. 64-bit data bus, 100-MHz operation.
- Integrated Intel Floating-Point Unit compatible with the IEEE Std 754
- Integrated thermal diode measuring processor temperature.

4.5 System Core Logic

The system core logic function of the notebook is implemented on the CPU module and motherboard using the VIA S3 Savage IX AGPset. The VIA S3 Savage IX AGPset is intended for the Pentium III processor platform and emerging 3D graphics/multimedia applications. The VIA S3 Savage IX AGPset brings 100/133-MHz FSB (front-side bus), ATA/33/66/100 HDD support in UDMA mode 2 & 4 and PC100/133 SDRAM performance to entry-level Performance PCs.

4.5.1 VIA TWISTER Features

The VIA TWISTER Host Bridge provides a Host-to-PCI bridge, optimized DRAM controller and data path, and an Accelerated Graphics Port (AGP) interface. AGP is a high performance, component-level interconnect targeted at 3D graphics applications and is based on a set of performance enhancements to PCI.

The VIA TWISTER functions and capabilities include:

Define Integrated Solutions for Value PC Mobile Designs

- Integrated VIA Apollo Pro133 and S3®Savaged IX in a single chip
- 64-bit Advanced Memory controller supporting PC100/PC133 SDRAM and VCM
- Combines with VIA VT82C686B PCI-LPC South Bridge for state-of-the-art power management

High Performance CPU Interface

- Socket 370 support for Intel Pentium III, Celeron™processors
- 66/100/133 MHz CPU Front Side Bus (FSB)
- Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
- Five outstanding transactions (four In-Order Queue IOQ) plus one output latch)
- Dynamic deferred transaction support

Advanced High Performance DRAM Controller

- DRAM interface runs synchronous (66/66, 100/100, 133/133) mode or pseudo-synchronous (66/100, 100/66, 100/133, 133/100) mode with FSB
- Concurrent CPU, AGP, and PCI access
- Supports SDRAM and VCM SDRAM memory types
- Support 3 DIMMs or 6 banks for up to 1.5 GB of DRAM (256Mb DRAM technology)
- 64-bit data width
- Supports maximum 8-bank interleave (8 pages open simultaneously); banks are allocated based on LRU
- SDRAM X-1-1-1-1-1-1-1 back-to-back accesses

Integrated Savage4 2D/3D/Video Accelerator
- Optimized Shared Memory Architecture (SMA)
- 8 to 32 MB frame buffer using system memory
- Floating point triangle setup engine
- Single cycle 128-bit 3D architecture
- 8M triangles/second setup engine
- 140M pixels/second trilinear fill rate
- Full internal AGP4X performance
- S3 DX7 texture compression (S3TC™)
- Next generation, 128-bit 2D graphics engine
- High quality DVD video playback
- Flat panel monitor support
- 2D/3D resolutions up to 1920x1440

3D Rendering Features
- Single pass multiple textures
- 8-bit stencil buffer
- 32-bit true color rendering
- Specular lighting and diffuse shading
- Alpha blending modes
- Massive 2K x 2K textures
- MPEG-2 video textures
- Vertex and table fog
- 16 or 24-bit Z-buffering
- Sprite anti-aliasing, reflection mapping, texture morphing, shadows, procedural textures and atmospheric effects

Motion Video Architecture
- High quality up/down scalar
- Planar to packed format conversion
- Motion compensation for full speed DVD playback
- Hardware subpicture blending and highlights
- Multiple video windows for video conferencing
- Contrast, hue, saturation, brightness and gamma controls
- Digital port for NTSC/PAL TV encoders

Advanced System Power Management Support
- Dynamic power down of SDRAM
- Independent clock stop controls for CPU/SDRAM, AGP and PCI bus
- Low-leakage I/O pads

Full Software Support
- Drivers for major operating systems and APIs
- North Bridge/Chipset and Video BIOS support

4.5.2 VT82C686B Features

The VT82C686B PSIPC (PCI Super-I/O Integrated Peripheral Controller) is a high-integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to PCI bus bridge functionality to make a complete Microsoft PC99-compliant PCI/ISA system.

The VT82C686B functions and capabilities include:

Inter-operable with VIA and other Host-to-PCI Bridges

- Combine with TWISTER for a complete 66 / 100 / 133 MHz Socket 370 or Slot-1 system with integrated 2D / 3D graphics (S3 Savage 4)
- Inter-operable with Intel or other Host-to-PCI bridges for a complete PC99 compliant PCI / AGP / ISA system

PCI to ISA Bridge

- Integrated ISA Bus Controller with integrated DMA, timer, and interrupt controller
- Integrated Keyboard Controller with PS2 mouse support
- Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
- Integrated USB Controller with root hub and four function ports
- Integrated UltraDMA-33/66 master mode EIDE controller with enhanced PCI bus commands
- PCI-2.2 compliant with delay transaction and remote power management
- Distributed DMA support for ISA legacy DMA across the PCI bus
- Fast reset and Gate A20 operation
- Flash EPROM, 4Mb EPROM and combined BIOS support
- Supports positive and subtractive decoding

UltraDMA-33 / 66 / 100 Master Mode PCI EIDE Controller

- Dual channel master mode PCI supporting four Enhanced IDE devices
- Transfer rate up to 33MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-33 interface
- Support ATAPI compliant devices including DVD devices
- Support PC native and ATA compatibility modes
- Complete software driver support

Integrated Super IO Controller

- Supports 2 serial ports, IR port, parallel port, and floppy disk controller functions
- Two UARTs for Complete Serial Ports
- Infrared-IrDA (HPSIR) and ASK (Amplitude Shift Keyed) IR port multiplexed on COM2
- Multi-mode parallel port
- Floppy Disk Controller

SoundBlaster Pro Hardware and Direct Sound Ready AC97 Digital Audio Controller

- Dual full-duplex Direct Sound channels between system memory and AC97 link

- PCI master interface with scatter / gather and bursting capability
- 32 byte FIFO of each direct sound channel
- Standard v1.0 or v2.0 AC97 Codec interface for single or cascaded AC97 Codec's from multiple vendors
- Loopback capability for re-directing mixed audio streams into USB and 1394 speakers
- Hardware SoundBlaster Pro for Windows DOS box and real-mode DOS legacy compatibility
- Hardware assisted FM synthesis for legacy compatibility
- Direct two game ports and one MIDI port interface
- Complete software driver support for Windows-95/98/2000 and Windows NT
- Voltage, Temperature, Fan Speed Monitor and Controller
- Five positive voltage (one internal), three temperature (one internal) and two fan-speed monitoring
- Programmable control, status, monitor and alarm for flexible desktop management
- Automatic clock throttling with integrated temperature sensing
- Internal core VCC voltage sensing
- Flexible external voltage sensing arrangement (any positive supply and battery)

Universal Serial Bus Controller

- USB v1.1 and Intel Universal HCI v1.1 compatible
- Eighteen level (doublewords) data FIFO with full scatter and gather capability
- Root hub and four function ports
- Integrated physical layer transceivers with optional over-current detection status on USB inputs
- Legacy keyboard and PS/2 mouse support

System Management Bus Interface

- Host interface for processor communications
- Slave interface for external SMBus masters

Sophisticated PC99-Compatible Mobile Power Management

- Supports both ACPI and legacy APM power management
- ACPI v1.0 Compliant
- APM v1.2 Compliant
- CPU clock throttling and clock stop control for complete ACPI C0 to C3 state support
- PCI bus clock run, Power Management Enabled (PME) control, and PCI/CPU clock generator stop control
- Supports multiple system suspend types
- Multiple suspend power plane controls and suspend status indicators
- Normal, doze, sleep, suspend and conserve modes
- Global and local device power control
- System event monitoring with two event classes
- Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up
- Up to 12 general purpose input ports and 23 output ports
- One programmable chip select and one microcontroller chip select

- Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
- Thermal alarm on either external or any combination of three internal temperature sensing circuits
- Hot docking support
- I/O pad leakage control

Plug and Play Controller

- PCI interrupts steerable to any interrupt channel
- Steerable interrupts for integrated peripheral controllers: USB, floppy, serial, parallel, audio, soundblaster, MIDI
- Steerable DMA channels for integrated floppy, parallel, and soundblaster pro controllers
- One additional steerable interrupt channel for on-board plug and play devices
- Microsoft Windows 98, Windows NT, Windows 95 and plug and play BIOS compliant
- Integrated I/O APIC (Advanced Peripheral Interrupt Controller) (CG Silicon)
- Built-in NAND-tree pin scan test capability 35um, 3.3V, low power CMOS process
- Single chip 27x27 mm, 352 pin BGA

4.6 Clock Frequency Generator

The notebook utilizes the IMI 9896I chip to supply the system clock needed to run the computer. The following are the available clock frequencies:

System clock:

Clock generator IMI 9806I support:

- 66/100 MHz for Pentium III Mobile CPU
- 30/33 MHz for PCI device bus clock use
- 48 MHz for PIIX4M
- 14.318 MHz for PIIX4M refresh use

- 14.318 MHz XTAL for Clock Generator use
- 32.768 KHz XTAL for RTC real time clock
- 8.0 MHz XTAL for K/B controller use
- 14.318 MHz OSC for sound blaster use

4.7 Cache Memory

The primary (L1) and secondary (L2) level cache are integrated on the CPU. By incorporating the cache on-die (meaning it is combined with the CPU into one component), Intel eliminates the need for separate components. The 256KB on-die L2 cache provides three (3X) times faster processor access, resulting in significant improvements in performance. Likewise, an integrated cache means a reduction of connections resulting in increased reliability.

4.8 System Memory

The memory subsystem, implemented on the motherboard, includes System and Video memory. The VIA Twister System Controller chip provides primary control for the system memory.

4.8.1 System Memory

The notebook offers two 64-bit SODIMM (Small Outline Dual Inline Memory Module) sockets for main memory configuration. The memory sockets accept any standard 144-pin SODIMM modules at 16MB, 32MB, 64MB, 128MB and 256MB sizes. Memory modules are 3.3V SDRAM type.

4.8.2 Video Memory

The video memory of the notebook is embedded inside the VGA controller chip (S3 Savage 4) with 8,16 and 32MB SMA video memory that can support display resolutions of up to 1024 x 768 at 32-bit 16M color (TFT LCD).

4.9 System BIOS

The notebook utilizes the Phoenix BIOS 4.0 Release 6.0 (Basic I/O System) that contains both the main system BIOS and the VGA BIOS with Shadow BIOS capability. It utilizes Flash EPROM BIOS that allows instant erasing and programming without replacing the EPROM chip.

The BIOS is stored in a 32-pin PLCC package FLASH ROM SST 28SF040A-90/120 or Winbond W29C040P-90 with 4Mbit size and is mounted into the motherboard. While posting the system, the Shadow RAM will be enabled and the ROM will be disabled.

4.10 Video Subsystem

The video subsystem, integrated inside the North Bridge chip and the LCD panel, controls the display output to both the LCD Panel screen and to the external VGA port.

4.10.1 Video Chip Controller

S3 Savage 4 also includes 8, 16 and 32MB of shared architecture memory (SMA) with all of the above in a single BGA package.

Feature Summary of the S3 Savage 4:

- S3 Savage 4 Chip set
- 32/64-Bit 8/16/32MB SMA video buffer
- Designed for AGP 4X/2X with side-band addressing and execute modes
- 128 bit engine with dual rendering pipelines
- Floating point triangle setup engine Single cycle 3D architecture and trilinear filtering
- True color rendering
- 140MHz pixels/sectrilinear fill rate
- 8M triangle/sec setup engine Full speed DVD video play back
- VESA-DPMS 2.0 and DDC2
- Support Industry standard S3 Texture Compression

- Support major 3D standards: DierctX, OpenGL
- Support Pentium III SEE Command and AMD K6-2 / 3 , K7 3Dnow! Technology.Resolution up to 1920x1440

	Frame Buffer Size	
Resolutions Supported	8MB	16/32MB
640x480x8/16/32 bit	Yes	Yes
800x600x8/16/32 bit	Yes	Yes
1024x768x8/16/32 bit	Yes	Yes
1280x1024x8/16 bit	Yes	Yes
1280x1024x32 bit	Yes	Yes
1600x1200x8/16 bit	Yes	Yes
1600x1200x32 bit	Yes	Yes
1920x1440x8 bit	Yes	Yes
1920x1440x16 bit	Yes	Yes
1920x1440x32 bit		Yes

4.10.2 Video Clock

VIA VT82C686B provides input to generate VGA internal slate machine, MCLK, and DCLK. Also provides 32.768 KHz O/P for video RAM refresh.

4.11 PCMCIA Controller

The PCMCIA controller of the notebook is implemented on the motherboard using the O2Micro OZ6933 CardBus Controller. The notebook supports two PCMCIA slots for insertion of two Type I/II cards at the same time.

CARDBUS CONTROLLERS

The OZ6933 is an ACPI and PC98/99 logo certified high performance, dual slot PC Card controller with a synchronous 32-bit bus master/target PCI interface. This PC Card to PCI bridge host controller is compliant with the 2000 PC Card Standard. This standard incorporates the new 32-bit CardBus while retaining the 16-bit PC Card specification as defined by PCMCIA release 2.1. CardBus is intended to support "temporal" add-in functions on PC Cards, such as Memory cards, Network interfaces, FAX/Modems and other wireless communication cards, etc. The high performance and capability of the CardBus interface will enable the new development of many new functions and applications.

The OZ6933 CardBus controller is compliant with the latest ACPI-PCI Bus Power Management interface Specification. It supports all four power states and the PME# function for maximum power savings and ACPI compliance. Additional compliance to On Now Power Management includes D3 cold state support, paving the way for low sleep state power consumption and minimized resume times. To allow host software to reduce power consumption further, the OZ6933 provides a power-down mode in which internal clock distribution and the PC Card socket clocks are stopped. An advanced CMOS process is also used to minimize system power consumption.

The OZ6933 dual PCMCIA socket supports two 3.3V/5V 8/16-bit PC Card R2 cards or 32-bit CardBus R3 cards. The R2 card support is compatible with the Intel 82365SL PCIC controller,

and the R3 card support is fully compliant with the 2000 PC Card Standard CardBus specification. The OZ6933 is an additional buffer chip for the PC Card socket interface. In Addition, the OZ6933 supports dynamic PC Card hot insertion and removal, with auto configuration capabilities.

The OZ6933 is fully complains with the 33Mhz PCI Bus specification, v2.2. It supports a master device with internal CardBus direct data transfer. The OZ6933 implements FIFO data buffer architecture between the PCI bus and CardBus socket interface to enhance data transfers to CardBus Devices. The bi-directional FIFO buffer permits the OZ6933 to accept data from a target bus (PCI or CardBus interface) while simultaneously transferring data. This architecture not only speeds up data transfers but also prevents system deadlocks.

The OZ6933 is a PCMCIA R2/CardBus controller, providing the most advanced design flexibility for PC Cards that interface with advanced notebook designs.

FEATURES - Dual Slot Solution OZ6933

- Supports 2 PCMCIA 2.1 and JEIDA 4.2 R2 cards or 2 CardBus cards
- ACPI-PCI Bus Power Management Interface Specification Rev 1.1 Compliant
- Supports OnNow LAN wakeup, OnNow Ring Indicate, PCI CLKRUN#, PME#, and CardBus CCLKRUN#
- Compliant with the 33Mhz PCI Specification V2.2, 2000 PC Card Standard 7.1 for OZ6933
- Yenta™PCI to PCMCIA CardBus Bridge register compatible
- ExCA (Exchangeable Card Architecture) compatible registers map-able in memory and I/O space
- Intel™82365SL PCIC Register Compatible
- Supports PCMCIA_ATA Specification
- Supports 5V/3.3V PC and 3.3V Cardbus cards
- Supports two PC Card or CardBus slots with hot insertion and removal
- Supports multiple FIFOs for PCI/CardBus data transfer
- Supports Direct Memory Access for PC/PCI and PCI/Way on PC Card socket
- Programmable interrupt protocol: PCI, PCI+ISA, PCI/Way, or PC/PCI interrupt signaling modes
- Win'98 IRQ and PC-98/99 compliant
- Parallel or Serial interface for socket power control devices including Micrel and TI
- Integrated PC 98/99 -Subsystem Vendor ID support, with auto lock bit
- LED Activity Pins

- OZ6933 supports D3cold state PME# wakeup; 3.3Vaux Power; and Zoomed video buffer enable pins
- OZ6860: "Built-in" live video, high throughput, multimedia ZV ports support without additional buffers; 3V card protection during host system suspend with Auto Card VS# resensing; dedicated ZV output port to LCD controller

SmartCardBus™(OZ711E1/OZ711E2) combines a Smart Card reader and CardBus controller in a single IC. In addition to meeting PC Card standards, SmartCardBus is compliant to Microsoft PC/SC, ISO 7816-1, -2, -3 electrical specifications, standard protocols including T = 0, T = 1, and synchronous and asynchronous formats. SmartCardBus lowers the cost of ownership of e-commerce and corporate security Smart Card applications.

4.12 Audio Subsystem

The audio subsystem is integrated inside the South Bridge chip on the motherboard. Refer to the System Core Logic section of this chapter.

An internal two-way mini speaker and microphone provide the notebook with mobile sound generation and recording capabilities. In addition, a set of 3.5mm bayonet socket (1/8" minijack) connectors allow for external microphone, line inputs, and headphone outputs.

4.13 Keyboard and Pointing Device

The Keyboard Subsystem of the notebook is implemented on the Motherboard and Keyboard Assembly using the Mitsubishi 38867M8 keyboard controller chip and the Phoenix MultiKey/M3886L keyboard controller firmware. This chip controls the internal built-in keyboard, the built-in touchpad pointing device, as well as the external PS/2 keyboard and mouse port. The keyboard controller allows simultaneous use of both the internal and external keyboard and PS/2 mouse.

The A360 membrane keyboard is an 86-key IBM 101-key enhanced compatible keyboard with standard characters and 12 function keys including an embedded numeric keypad. See Chapter 1 for more information.

The pointing device subsystem consists of the built-in Synaptics touch pad pointing device module on the system top cover assembly and a pre-programmed Mitsubishi 38867M8 micro-controller that interfaces the mouse device to the Motherboard. The touch pad module is connected to battery board through a 6-pin FPC cable. An external PS/2 port also supports the use of an external PS/2 compatible mouse where the system automatically detects on system power up and runs both internal and external mouse simultaneously.

The Synatics touch pad, a pointing device for personal computers, detects the position of a finger over a touch-sensitive area. To move the cursor, the user lightly slides a finger over the smooth sensor area. To ' click' , the user gently taps on the surface.

The ultra-thin module is the thinnest PCB based touchpad available today. It is a capacitive sensor - the finger is detected by measuring its effect on an array of capacitive lines integrated into the PC board. The pad senses both the finger' s position and its contact area (X, Y, and Z). The area of contact is a measure of applied pressure. One side of the module PC board is the

sensor surface; electronic components are mounted on the other side. The sensitive area is protected by a layer of smooth and durable mylar.

The Synatics touch pad communicates with the host via a standard PS/2 mouse or trackball interface. It is fully compatible with the standard Microsoft mouse driver. The module connector includes the PS/2 signal pins, power supply pins and two connections for external button switches.

The Synatics touch pad includes a special "edge-motion" feature that allows the user to extend a drag operation when the finger reaches the edge of the sensor pad. The cursor continues to coast in the indicated direction when the finger is held against the edge.

4.14 Disk Drives Subsystem

The disk drives subsystem, implemented on the Motherboard and on the associated internal hard disk drive assembly and device bay, provides disk storage for all system software and user files.

The notebook is equipped with high capacity hard disk drive using Enhanced IDE controller with LBA (Logical Block Addressing) and Ultra DMA mode support.

The VT82C686B controller chip provides the Primary IDE controller for the internal hard disk, and the Secondary Master for the CD-ROM.

The floppy disk drive supports standard 3.5-inch 720KB and 1.44MB mini-diskettes while adding support for 1.2MB (3 Mode) mini-diskettes for Japanese market.

The notebook uses the 24X-speed IDE CD-ROM Drive that reads digital data stored on CD-ROM at 24 times faster rotational speed. The CD-ROM drive supports CD-DA transfer over ATAPI function that the host system can read CD audio data. The drive also supports Photo-CD Multi-session disc compatibility and Multimedia PC-3 specification compatibility. The notebook also could use the 8X+ speed IDE DVD-ROM Drive that reads DVD digital data stored on DVD-ROM at 8 times faster rotational speed.

4.15 Power Subsystem

The Power Subsystem consists of the following major sections:

4.15.1 AC Power Adapter

The computer is equipped with a 60W universal AC power adapter that converts AC voltage (100 to 240VAC, 50 to 60Hz) into DC voltage used to operate the notebook and charge the batteries.

4.15.2 Internal Battery Pack

The computer utilizes Nickel Metal Hydride (NiMH) or Lithium-Ion (Li-Ion) that provides DC power for the notebook and real time clock battery on the motherboard when the AC Adapter is not connected to the computer.

The normal charging time for the battery is around 2.5 hours when computer is turn off while it should take around 8 hours when the computer is running. Running time of battery is around 2 to 2.5 hours.

4.15.3 DC-DC Module of Motherboard

The DC-DC module receives approximately 12VDC from the battery pack and uses this input voltage to generate multiple regulated output voltages to provide power for all internal notebook board assemblies.

4.15.4 LCD Inverter Board Assembly

The LCD Inverter Board Assembly is located in the LCD Panel Assembly. It converts the +12VDC input directly from the Battery Pack into a high voltage AC output used to light the CCFT (Cold-Cathode Fluorescent Tube).

4.16 Micro-P Subsystem (PMU-07)

The micro controller Mitsubishi PMU07 acts as a supplement for the power management control. It supports many functions via the SMBus interface.

The system communicates with the PMU07 via the SMBus interface. The SMBus host (M38867) should be first initialized before starting the transaction. The following is the procedure for system communication with PMU07:

1. Enable SMBus interface by writing 01h to SmbHstCfg register.
2. Get SMBus I/O port base address by reading from SmbBA register.
3. Clear SMBus status by writing 1Eh to SmbHstSts register.
4. Write the PMU07 slave address to SmbHstAdd register.
   - Send command to PMU07 -- Slave address is 04h.
   - Read data from PMU07 -- Slave address is 05h.
5. Write the desired command to SmbHstCmd register.
6. Write the desired parameters to SmbHstDat0(High byte) and SmbHstDat1(Low byte) registers if the system wants to send command to PMU07.
7. Wait for SMBus interrupt occurred by monitoring SmbHstSts register INTR bit.
8. Get the desired data by reading from SmbHstDat0(High byte) and SmbHstDat1(Low byte) registers if the system wants to read data from PMU07.

Features Summary of the Micro-P:

- 5 channels 8-bit analog to digital converter
- Timer0: 8-bit tuner/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter. TMR1 can be incremented during sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Capture, Compare, PWM module
- Synchronous Serial port (SSP) with SPI and I^2C
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)
- Brown-out detection circuitry for Brown-out Reset (BOR)
- 2K bytes program memory
- 128 bytes data memory
- 22 I/O pin
- 8 interrupt sources