Chapter 3

Software Functional Overview

3.1 Overview

The A360 is an IBM PC/AT compatible Notebook PC which support the Intel' s FC-PGA processors family. The following are the major features that A360 supports:

- Microsoft PC99 logo and WinME Logo approval.
- Offer 800x600 SVGA display with 12.1" LCD panel
- Offer 1024x768 XGA display with 13.3" LCD panel
- Offer 1024x768 XGA display with 14.1" LCD panel
- Support ACPI 1.0B (or above)
- Support PCI 2.1 (or above)
- Support AGP 2.0.
- Support SMBIOS 2.3
- Support PC-100/133 SDRAM
- Support 100/133 MHz CPU front side bus.
- Support a proprietary Port Replicator

3.2 Summary of the BIOS Specification

Below is the summary of the BIOS software specification:

Controller Chip	Description
BIOS Feature	▪ Microsoft PC99 logo and WinME Logo approval. ▪ Support Boot Block / Crisis Rescue ▪ Support ACPI 1.0B (or above) ▪ Support PCI 2.1 (or above) Spec ▪ Support SMBIOS 2.3 ▪ Support AGP 2.0. ▪ Support Windows 98 SE, Windows 2000 and Windows ME. ▪ Support flash function including both DOS and Windows interface for new BIOS update. ▪ Support 3 Mode FDD. ▪ Support 4 different keyboards on same BIOS ▪ Support boot from FDD, HDD,CDROM and LAN Drive ▪ Support Quick Boot (10 Seconds)
CPU	Auto detect the CPU type and speed for Intel Pentium III based system
DRAM	Auto sizing and detection. Support PC-100/133 SDRAM.
Cache	▪ Level 2 SRAM auto sizing and detection ▪ Always enable CPU L1 and L2 cache
Shadow	Always enable VGA and System BIOS shadow
Display	▪ System auto detects LCD or CRT presence on boot and lid closed

	▪ Support Panning while LCD in a display resolution greater than supported ▪ Support Microsoft Direct 3D ▪ Support AGP4X Bus

Controller Chip	Description
Hard Disk	▪ Enhanced IDE spec ▪ Support auto IDE detection ▪ Support LBA mode for larger capacity HDD ▪ Support Ultra DMA 33 ▪ Support Fast PIO mode 1-4 transfer ▪ Support 32-bit PIO transfer ▪ Support Multi-Sector transfer ▪ Support SMART monitoring.
Multi Boot	Allow the user to select boot from FDD, HDD and CD-ROM and LAN devices.
Plug and Play	Support PnP Run Time Service and conflict-free allocation of resource during POST
Smart Battery	Support BIOS interface to pass battery information to the application via SMBus
Keyboard Controller	Support Fn hot keys, two Win98 hot keys, built-in Glide Pad and external PS/2 mouse/keyboard
PCMCIA	Compliant with PCMCIA 2.1 specification
Audio DJ	With DVD resume system
Port Replicator	I/O port replicator duplicates the following ports ▪ Video Port ▪ Printer Port ▪ COM1 Port ▪ PS/2 Mouse & Standard Keyboard Port ▪ USB Port ▪ DC In Jack
Power Management Support (ACPI Mode)	The power management is compliant with ACPI 1.0B specification and supports the following power state: ▪ S0 (Full-On) Mode ▪ S1 (Doze) Mode ▪ S4 (STD) Mode ▪ S5 (Soft-Off) Mode

3.3 Subsystem Software Functions

This section provides introduction on the software functions of the notebook subsystems and BIOS related function.

3.3.1 Key Chipset Summary

Following are the main chipsets used in the notebook:

Controller Chip	Vendor	Description
Processor	Intel	FC-PGA 370 Socket Pentium III 933 / 1G / 1.13G MHz Celeron 766/ 800 MHz
Core Logic	VIA	Twister VT8603 (North Bridge) VT82C686B (South Bridge)
Video Controller	S3	Savage4 with AGP 4X SMA
PCMCIA Controller	O2Micro	OZ6933
Super I/O Controller	VIA	VT82C686B embed super I/O
Audio Chip	VIA	South Bridge Integrated
Audio Codec	ADI	AD1886
Keyboard Controller	Mitsubishi	M38869
PMU Controller	Mitsubishi	PMU07
Gas Gauge IC	Include PMU07	
ROM BIOS	Winbond	W29C040P, Boot Block Structure
Clock Generator	IMI	C9896B
Temperature Sensor	NS	MAX1617A
LAN	INTEL	82559
Modem	Lucent	MARS III
IEEE 1394	Lucent	FW323

3.3.2 System Memory

The system memory consists of SDRAM memory on 64-bit bus and the module size options are 64/128/256MB upward. The BIOS will automatically detect the amount of memory in the system and configure CMOS accordingly during the POST (Power-On Self Test) process. This must be done in a way that requires no user interaction.

Base SO-DIMM DRAM slot (Bank 0 & 1)	Expansion SO-DIMM DRAM slot (Bank 2 & 3)	Total Size
64MB	NIL	64MB
64MB	64MB	128MB
64MB	128MB	192MB
64MB	256MB	320MB
128MB	NIL	128MB
128MB	64MB	192MB
128MB	128MB	256MB
128MB	256MB	384MB

256MB	NIL	256MB
256MB	64MB	320MB
256MB	128MB	384MB
256MB	256MB	512MB
NIL	64MB	64MB
NIL	128MB	128MB
NIL	256MB	256MB

3.3.3 Video

The Video subsystem used share memory of Video memory. The system will support the true ZV port, the Microsoft Direct 3D assist, simultaneous display, monitor sense for auto display on boot and VESA Super VGA function call.

Supported Video Mode

The following is the display modes supported by the S3 Savega4 in LCD only, CRT only, and simultaneous mode. The VGA BIOS will allow mode sets of resolutions greater than the panel size but only show as much mode display as will fit on the panel.

Panel Type Initialization

The VGA BIOS will issue INT 15h function call during POST. This function call allows the system BIOS to specify the panel type to the VGA BIOS. The system BIOS should get the panel type from GPI pins before the VGA chip initialized, and pass this information to VGA BIOS through INT 15 Function 5F01h.

Supported standard VGA modes:

The VGA BIOS supports the IBM VGA Standard 7-bit VGA modes numbers.

Mode	Pixel Resolution	Colors	Memory
00h/01h	40*25	16	Text
02h/03h	80*25	16	Text
04h/05h	320*200	4	2-bit Planar
06h	640*200	2	1-bit Planar
07h	80*25	Mono	Text
0Dh	320*200	16	4-bit Planar
0Eh	640*200	16	4-bit Planar
0Fh	640*350	Mono	1-bit Planar
10h	640*350	16	4-bit Planar
11h	640*480	2	2-bit Planar
12h	640*480	16	4-bit Planar
13h	320*200	256	8-bit Planar

Note: All Standard VGA Modes are limited to the standard VGA refresh rates.

Supported extended video modes:

CRT device will support all listed VESA mode; and other devices such as PANEL & TV may be limited to the mode support due to their characteristics.

VESA Mode	Pixel Resolution	Memory Model	Refresh Rates In (Hz)	Minimum Memory
100h	640 x 400	8-bit Packed	70	2MB
101h	640 x 480	8-bit Packed	60, 72, 75, 85	2MB
102h	800 x 600	4-bit Planar	60, 72, 75, 85, 100	2MB
103h	800 x 600	8-bit Packed	60, 72, 75, 85, 100	2MB
104h	1024 x 768	4-bit Planar	43(I), 60, 70, 75, 85, 100	2MB
105h	1024 x 768	8-bit Packed	43(I), 60, 70, 75, 85, 100	2MB
106h	1280 x 1024	4-bit Planar	43(I), 60, 75, 85	2MB
107h	1280 x 1024	8-bit Packed	43(I), 60, 75, 85	2MB
10Eh	320 x 200	16-bit Packed	70	2MB
10Fh	320 x 200	32-bit Unpacked	70	2MB
111h	640 x 480	16-bit Packed	60, 72, 75, 85	2MB
112h	640 x 480	32-bit Unpacked	60, 72, 75, 85	2MB
114h	800 x 600	16-bit Packed	60, 72, 75, 85, 100	2MB
115h	800 x 600	32-bit Unpacked	60, 72, 75, 85, 100	2MB
117h	1024 x 768	16-bit Packed	43(I), 60, 70, 75, 85, 100	2MB
118h	1028 x 768	32-bit Unpacked	43(I), 60, 70, 75, 85, 100	4MB
11Ah	1280 x 1024	16-bit Packed	43(I), 60, 75, 85	4MB
11Bh	1280 x 1024	32-bit Unpacked	43(I), 60, 75, 85	8MB
11Dh	640 x 400	16-bit Packed	70	2MB
11Eh	640 x 400	32-bit Packed	70	2MB
120h	1600 x 1200	8-bit Packed	48(I), 60, 75, 85	2MB
122h	1600 x 1200	16-bit Packed	48(I), 60, 75, 85	4MB
124h	1600 x 1200	32-bit Unpacked	48(I), 60, 75, 85	8MB
12Ah	640 x 480	24-bit Packed	60, 72, 75, 85	2MB
12Bh	800 x 600	24-bit Packed	60, 72, 75, 85, 100	2MB
12Ch	1024 x 768	24-bit Packed	43(I), 60, 70, 75, 85, 100	4MB
12Dh	1280 x 1024	24-bit Packed	43(I), 60, 75, 85	4MB
12Eh	320 x 200	8-bit Packed	70	2MB
131h	320 x 200	8-bit Packed	72	2MB
133h	320 x 200	16-bit Packed	72	2MB
134h	320 x 200	32-bit Packed	72	2MB
13Bh*	1400 x 1050	8-bit Packed	60, 75	2MB
13Ch*	1400 x 1050	16-bit Packed	60, 75	4MB
13Eh*	1400 x 1050	32-bitUnpacked	60, 75	8MB

141h	400 x 300	8-bit Packed	72	2MB
143h	400 x 300	16-bit Packed	72	2MB
144h	400 x 300	32-bitUnpacked	72	2MB
151h	512 x 384	8-bit Packed	70	2MB
153h	512 x 384	16-bit Packed	70	2MB
154h	512 x 384	32-bitUnpacked	70	2MB
171h	720 x 480	8-bit Packed	75	2MB
173h	720 x 480	16-bit Packed	75	2MB
174h	720 x 480	24-bit Packed	75	2MB
175h	720 x 480	32-bitUnpacked	75	2MB
176h	720 x 576	8-bit Packed	75	2MB
178h	720 x 576	16-bit Packed	75	2MB
179h	720 x 576	24-bit Packed	75	2MB
17Ah	720 x 576	32-bitUnpacked	75	2MB

Note: "*" The modes may not be available. Their availability should be determined by VESA function calls.

Panel Type Initialization

The VGA BIOS will issue INT 15h function call during POST. This function call allows the system BIOS to specify the panel type to the VGA BIOS. The system BIOS should get the panel type from GPIO pins before the VGA chip initialized, and pass this information to VGA BIOS through INT 15 Function 5F01h.

LCD Panel ID pin Definition:

VT82C686B GPI Pins				Panel Type
GPI [23]	GPI [17]	GPI [11]	GPI [10]	
0	0	0	0	ADI 12.1" SVGA TFT AA121SJ23
0	0	0	1	Hannstar HSD121PS11
0	0	1	0	
0	0	1	1	
0	1	0	0	ADT L133X3-1
0	1	0	1	Unipac UB133X3-1
0	1	1	0	
0	1	1	1	
1	0	0	0	CPT CLAA141XC01
1	0	0	1	Hyundai HT14X13-101
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	

1	1	1	0	
1	1	1	1	

3.3.4 Enhanced IDE

The system BIOS must be ready to support 4 IDE devices on two controllers. The BIOS support Ultra DMA 33 and also supports automatic configuration of drives using both the LBA and CHS large drive remapping method. In addition to supporting standard drives through an auto-configuration process that does NOT require user involvement or confirmation. The system should automatically do this at POST time in a way that is transparent to the user. If a drive is connected to the bus, the drive should be automatically recognized, configured and available for use under MS-DOS 6.2x.

Ultra DMA

Ultra DMA 33 is a physical protocol used to transfer data between an Ultra DMA/33 capable IDE controller and one or more Ultra DMA/33 capable IDE devices. It utilizes the standard Bus Master IDE functionality and interface to initiate and control the transfer. Ultra DMA/33 utilizes a "source-synchronous" signaling protocol to transfer data at rates up to 33 Mbytes/sec.

3.3.5 Audio

The audio subsystem will support the requirements identified by the AC' 97 specification. Both software and hardware will control the volume level for the internal audio subsystem. In addition to the volume control, the user will be able to mute the sound to completely cut off the volume using both software and hardware.

3.3.6 Super I/O

This controller contains 16550A or FIFO Enabled UART, ECP/EPP/Uni-directional Parallel Port meeting the 1284 specification, and an Infrared port.

3.3.7 PCMCIA

The PCMCIA controller chip of the notebook provides the following features:

- Individually accessed, dual-buffer implementation
- Support for 2 separate CardBus slots (one type III or two type II stacked)
- Support for 3.3v, 5v and 12v (flash programming) cards

3.3.8 LED Indicator

The table below lists down the functions of the Status LED indicator:

Indicator	Function Description
IDE accessing LED❶	This LED will turn on while accessing the IDE Device.
FDD accessing LED❶	This LED will turn on while accessing the FDD Device.
Battery Charging LED	Turn on (Amber) – Battery is under charging mode Turn off – Battery full charged or no battery
Caps Lock LED❶	This LED will turn on when the function of Caps Lock is active.
Scroll Lock LED❶	This LED will turn on when the function of Scroll Lock is active.
Num Lock LED❶	This LED will turn on when the function of Num Lock is active.
Power Status LED	Green – System is powered on. Green Blinking- System is entered suspend mode. Amber – Battery Low.
Mail LED❶	This LED will turn on while Mail was arrived.

❶ - There LEDs will be turned off during Suspend mode.

3.3.9 Hot Keys Definition

All Hot keys must be active at all times under all operation systems.

Hot Key	Function	Handler
Fn + F3	Toggle Display (LCD/CRT/TV/LCD&CRT)	BIOS Handler
Fn + F5	Display Stretch	BIOS Handler
Fn + F6	System Speakers On/Off	BIOS Handler
Fn + F8	Brightness Increase	Controlled by PMU07
Fn + F9	Brightness Decrease	Controlled by PMU07
Internet Button	Internet Function Key	Controlled by Driver
Mail Button	Internet Function Key	Controlled by Driver

The system will issue a beep to inform user while the following hot keys are pressed.

1) Fn + F3 (Toggle Display) -- LCD => CRT=> LCD+CRT
2) Fn + F5 (Display Stretching)
3) Fn + F6 (System Speakers On/Off)
4) Fn + F8 (Brightness Up)
5) Fn + F9 (Brightness Down)

3.3.9-1 Port Replicator

The Port Bar duplicates the following ports from the Notebook:

- CRT Port
- Serial Port
- Printer Port
- PS/2 Port For Keyboard
- PS/2 Port For Mouse
- One USB Ports
- DC in Jack

The Port replicator can just support the cold insertion but not hot insertion. While hot insertion, the system is not guaranteed that functionality.

3.3.10 Plug & Play

The BIOS supports the Plug and Play Specification 1.0A. (Include ESCD)
This section describes the device management. The system board devices and its resources are as follows:

Device	Connect Type	Resources			
		I/O	IRQ	DMA	Memory
DMA Controller	Static	00~0F, 81~8F	-	DMA4	-
Interrupt Controller	Static	20~21, A0~A1	IRQ2	-	-
System Timer	Static	40~43	IRQ0	-	-
RTC	Static	70~71	IRQ 8	-	-
ISA Bus	Static	-	-	-	-
System Speaker	Static	61	-	-	-
System Board	Static	-	-	-	E0000~FFFFF
PnP Mother Board	Static	80	-	-	-
Keyboard Controller	Static	60, 64	IRQ 1	-	-
PMU07	Static	68, 6C			
Math Coprocessor	Static	F0~FF	IRQ 13	-	-
PS/2 Mouse	Enable / Disable	-	IRQ 12	-	-
Video Controller	Static	3B0~3BB, 3C0~3DF	IRQ 5	-	A0000~BFFFF, C0000~CFFFF
Serial Port	Static	3F8~3FF	IRQ 4	-	-
ECP, Parallel port	Static	378~37F, 778~77F	IRQ 7	DMA 1	-
FDC	Static	3F0~3F5, 3F7	IRQ 6	DMA 2	-
Dual IDE Controller	Static	170~177, 1F0~1F7, 3F6	IRQ 14, 15	-	-
CardBus Controller	Dynamic	3E0~3E1	IRQ 10	-	
Audio chip	Dynamic	220~22F, 300~301, 388~38B	IRQ 5	DMA 3	
Modem	Dynamic	3E8~3EF	IRQ 10	-	
LAN	Dynamic	1080~10FF	IRQ 10		
IR	Enable/ Disable	158~15F, 2F8-2EF	IRQ 3		-
USB Host Controller	Dynamic	EF80~EF9F	IRQ 9	-	-

3.3.11 PCI Device

The table below summarizes the PCI IDSEL Pin Allocation:

IDSEL Pin	PCI Device		
	Device Number	Function Number	Device Name
AD11	Device 00	Function 0	VT8603 – Host to PCI bridge.
AD12	Device 01	Function 0	VT8603 – PCI to AGP bridge.
AD15	Device 04	Function 0	ESS 1988 Audio Accelerator
AD16	Device 05	Function 0	ASKEY Combo card
AD17	Device 06	Function 0	LAN / MODEM
AD18	Device 07	Function 0	VT82C686B – PCI to ISA bridge
		Function 1	VT82C686B – IDE interface
		Function 2	VT82C686B – USB Port 0-1interface
		Function 3	VT82C686B – USB Port 2-3interface
		Function 4	VT82C686B – PMU and SMBus interface
		Function 5	VT82C686B – AC97 Audio Interface
AD23	Device 0C	Function 0	OZ6933 – Card Bus Socket A
		Function 1	OZ6933 – Card Bus Socket B
AD24	Device 0D	Function 0	IEEE 1394

The table below summarizes the INT Pin Allocation:

INT Pin	PCI Device
INTA	CardBus / LAN / Modem / IEEE1394
INTB	CardBus / LAN / Modem
INTC	VGA / Audio
INTD	USB

The table below summarizes the PCI bus master Allocation:

REQ# Pin	PCI Device
REQ 0	VGA / Audio
REQ 1	CardBus
REQ 2	LAN / Modem
REQ 3	IEEE1394

3.3.12 SMBus Devices

The SMBus is a two-wire interface through which the system can communicate with power-related chips. The BIOS should initialize the SMBus devices during POST.

3.3.12 VT82C686B SMBus Connection Devices

SMBus Device	Master/Slave	Address	BIOS Need to Initialization
VT82C686B – Core Logic	Both Host and Slave	02h	Enable SMBus interface and SMBus interrupt
SO-DIMM	Slave	A0h	Not Need
PMU07	Master	10h	Enable PS01 decode interface
MAXIM1617 – Temperature Sensor	Slave	9Ch	Program the desired temperature range.
OZ168	Slave	34h	Audio DJ
Battery	Slave	A8h	No Need
Clock Synthesizer	Slave	D2h	Program the desired clock frequency (Pin23 output 24MHz, Pin22 output 48MHz)

3.3.13 Resource Allocation

This section summarizes the resource allocation of the notebook computer.

I/O Map

Hex Address	Device
000 - 01F	8237-1
020 - 021	8259-1
022	VIA VT82C686B
040 - 05F	8254
060 - 064	Keyboard Controller
068 – 06C	PMU07 Controller
070 - 07F	RTC & NMI Mask
080 - 08F	DMA Page Registers
092	System Control Port
0A0 - 0A1	8259-2
0B2	Advanced Power Management Control Port
0B3	Advanced Power Management Status Port
0C0 – 0DF	8237-2
0F0 – 0FF	Math Coprocessor
170 - 177	IDE Secondary Command Block
1F0 - 1F7	IDE Primary Command Block
200 - 20F	Game Port
220 - 22F	Sound Blaster
279	ISA PnP Address

330 - 333	MIDI
376	IDE Secondary Control Block
378 – 37F	Parallel Port
388 - 38B	FM Synthesizer
398 - 399	Super I/O Chip
3B0 - 3DF	Video Controller
3E0 - 3E1	PCMCIA Controller
3E8 - 3EF	Fax/Modem
3F0 - 3F5, 3F7	Floppy Disk Controller
3F6	IDE Primary Control Block
3F8 - 3FF	Serial Port 1
778 – 77F	ECP port
A79	ISA PnP Address
CF8 – CFF	PCI BUS configuration Register

ISA DMA Map

DMA Channel	Device
DMA 0	Unused
DMA 1	ECP
DMA 2	Floppy Disk
DMA 3	Audio
DMA 4	[Cascade]
DMA 5	Unused
DMA 6	Unused
DMA 7	Unused

Memory Map

Address Range	Length	Description
00000 - 9F7FFh	638 KB	Base Memory
9F800 - 9FFFFh	2 KB	Extended BIOS Data Area
A0000 – BFFFFh	128 KB	Video Memory
C0000 – CBFFFh	48 KB	Video ROM
CC000 – CFFFFh	16 KB	Unused
D0000 – DFFFFh	64 KB	Unused
E0000 – E0FFFh	4 KB	DMI information
E1000 – FFFFFh	124 KB	System ROM BIOS

IRQ Map

IRQ#	Description
IRQ 0	System Timer
IRQ 1	Keyboard
IRQ 2	[Cascade]
IRQ 3	Serial Infrared Port

IRQ 4	Serial Port
IRQ 5	Audio / USB
IRQ 6	Floppy Disk Drive
IRQ 7	Parallel Port
IRQ 8	RTC Alarm
IRQ 9	ACPI
IRQ10	LAN / Modem / CardBus/ VGA
IRQ11	Reserved for PCMCIA Card
IRQ12	PS/2 Mouse
IRQ13	FPU
IRQ14	Hard Disk Drive
IRQ15	CD-ROM or DVD-ROM

3.3.14 GPIO Pin Assignment

The GPI and GPO pins connected to system devices. The BIOS can get device's status and control the device via the GPI and GPO pins.

VT82C686B GPI pin assignment

Pin Name	Function Name	Connected Device	Description
GPI[0]	Pull High		
GPI[1]	ECSCI#	PMU07	Low = SCI request from PMU07
GPI[2]	BATLOW#	PMU07	Low = Battery Low Activated
GPI[3]	MEDIA_DET	OZ168	Wake Up system for Audio DJ. (Program to LID function)
GPI[4]	IRQ6		Assign to IRQ6
GPI[5]	PME#	CardBus, LAN, Modem, IEEE1394	Low = PME Request
GPI[6]	SENSE#	PHS connector	Low = PHS Connected
GPI[7]	WAKECOM#	PMU07	Low = Ring signal from PMU07
GPI[8]	GPO[8]		Refer GPO[8].
GPI[9]	GPO[9]		Refer GPO[9]
GPI[10]	PANELID0	LCD FPC	LCD Panel Type Select
GPI[11]	PANELID1	LCD FPC	LCD Panel Type Select
GPI[16]	N.C.		
GPI[17]	PANELID2	LCD FPC	LCD Panel Type Select
GPI[18]	MB_ID0	DIP Switch	Mother board revision ID data 0
GPI[19]	MB_ID1	DIP Switch	Mother board revision ID data 1
GPI[20]	INTE_LATCH	M38869	Internet key status
GPI[21]	MAIL_LATCH	M38869	Mail key status
GPI[22]	AGP_BUSY#	VT8603	
GPI[23]	PANELID3	LCD FPC	LCD Panel Type Select

3.3.15 VT82C686B GPO pin assignment

Pin Name	Function Name	Connected Device	Description
GPO[0]	N.C.		
GPO[1]	SUSA#	VT8603, PMU07, Clock Generator	This pin will output Low to power down devices during Standby, STR, STD and SOFF
GPO[2]	SUSB#		Low = Suspend to RAM
GPO[3]	SUS_STA1#	VT8603	Low = Suspend Status 1.
GPO[4]	CPU_STP#	Clock Generator, SpeedStep Controller	Low = CPU clock Stop.
GPO[5]	PCI_STP#	Colck Generator	Low = PCI clock Stop.
GPO[7]	SLP#	VT8603	This pin will output Low to power down devices during Standby, STR, STD and SOFF
GPO[8]	GCLSMENA#	PCA9559	Low = Disable PCA 9559 Write Protect feature
GPO[9]	BIOSWEN#	BIOS ROM	Low = Enable Write BIOS ROM
GPO[10]	GPI[10]		Refer GPI[10]
GPO[11]	GPI[11]		Refer GPI[11]
GPO[12]	PMUCS1# (PCS0#)	PMU07	Low = Select PMU07 Chip
GPO[13]	PMUCS0# (MCCS#)	PMU07	Low = Select PMU07 Chip
GPO[14]	IRTX#	SIR	Infrared Transmit.
GPO[15]	IRRX#	SIR	Infrared Receive.
GPO[16]	FAN_HI/LO	FAN	High = FAN work on high speed Low = FAN work on low speed
GPO[17]	FANON#	FAN	Low = Turn on FAN
GPO[18]	PCMUTE#	Speaker	Low = PC sound off
GPO[19]	PCI_SERIRQ	CardBus Controller	Serial Interrupt Request
GPO[20]	FETON	PHS Connector	Enable PHS power
GPO[21]	BLEN	LCD Panel	Low = Turn off LCD Backlight
GPO[22]	DRAMENA		Select SMBus Device 00:DRAM Slot1 01:DRAM Slot2 10:NC 11:Clock Generator
GPO[23]	DRAMENB		
GPO[24]	USBOC1#	USB Connector 1	Low = USB Port 1 Over Current Detect
GPO[25]	USBOC0#	USB Connector 0	Low = USB Port 0 Over Current Detect

3.3.16 PMU07 GPIO pin assignment

PIN Name	Function Name	I/O	Connected Device	Description
GPIOA0	LID#	I	LID Switch	Low = LCD Close.
GPIOA1	N.C.	X		
GPIOA2	MailLED#	O	Mail LED	Low = Mail Arrival
GPIOA3	QGSMI#	I	M38869	Low = Keyboard SMI
GPIOA4	N.C.	X		
GPIOA5	PSTMSK#	O		Low = PCI Reset Mask
GPIOA6	PCMRI#	I	OZ6933	Low = Ring Signal from PCMCIA
GPIOA7	RI1#	I	Serial Port	Low = Ring Signal from Serial Port
GPIOB0	N.C.	X		
GPIOB1	N.C.	X		
GPIOB2	LEDSEL	O	Mail LED	Low = Disable Mail LED during POST. High = Enable Mail LED after POST.
GPIOB3	SHDN#	O	MAX3243	Low = Power down RS232
GPIOB4	N.C.	X		
GPIOB5	N.C.	X		
GPIOB6	SUSA#	I	VT82C686B	Low = Suspend Status 1
GPIOB7	WakeCOM#	O	VT82C686B	Low = Wake Up Event
GPIOC0	PMU5V	I	Pull High	
GPIOC1	N.C.	X		
GPIOC2	CHGLED	O	Charge LED	High = Turn ON Charge LED
GPIOC3	STSCLR	O		High = Clear Internet/Mail keys Status

3.3.17 M38867 GPIO pin assignment

Pin Name	Function Name	Connected Device	Description
P40	GSMI#	VT82C686B	Keyboard SMI#
P41	.		
P46	ECSCI_686B	VT82C686B	SCI
P54	ECSCI_PMU07	VT82C686B	ECSCI in
P55	N.C.		
P56	N.C.		
P57	N.C.		
P60	KBSEL1	DIP Switch	
P61	KBSEL2	DIP Switch	
P62	PASS#	DIP Switch	Low = Need to Clear

			Password during POST
P63	LOGOSEL	DIP Switch	
P64	N.C.		
P65	Pull High		
P66	N.C.		
P67	Pull High		
P76 (SDA)	Pull High		
P77 (SCL)	Pull High		

3.4 Power Management

This section provides the Power Management software function of the notebook.

3.4.1 General Requirements

The BIOS meet the following general Power Management requirements:

- Compliant with ACPI 1.0B Specification
- Support for Suspend-to-RAM (S1 state) and Suspend-to-Disk mode
- Support for Resume on Modem Ring while in S1 / S4 Mode.
- Power Management must not substantially affect or degrade system performance.
- Power Management must be OS independent
- Support resume on Time/Date

3.4.2 System Power Plane

The system components are grouped as the following parties to let the system to control the On/Off of power under different power management modes.
The power plane is divided as following:

Power Group	Power Control Pin	Controlled Devices
+B	Nil	IMM, (9V~20V)
+3VA	Nil	PIC16C62A, VT82C686B (RTC I/F), Internal Modem, PMU07
+12V	PWRON	PCMCIA Card, AC97 Codec
+5V	PWRON	PCMCIA Slot 5V
+3V	PWRON	VGA, PCMCIA, PCMCIA Slot 3V, DRAM, Twister(DRAM I/F), M38867, MAX3243
+5VS	SUSB#	FLASH ROM, HDD, CD-ROM, USB, Internal K/B, Glide Pad, External P/S2 Mouse, FDD, Audio AMP, Fan
+3VS	SUSB#	VT82C686B (ISA I/F Power), Clock Generator & Buffer (W137)
+RTCVCCS	Nil	VT82C686B (RTC)

3.5 ACPI

This section provides the ACPI software function of the notebook.

3.5.1 General Requirements

The BIOS must meet the following general Power Management requirements:

- Refers to the portion of the firmware that is compatible with the ACPI 1.0 specifications.
- Support for Suspend-to-RAM (S1 state) and Suspend-to-Disk mode (S4 state).
- Support the Wake up event from Modem Ring in S1~S4 state.
- Support the Wake up event from RTC Time/Date alarm in S1 state. This is enabled by a CMOS Setup option.
- Power Management must not substantially affect or degrade system performance.

Global System State Definitions

Global system states (Gx states) apply to the entire system and are visible to the user. Following is a list of the system states:

G0/S0 - Working:

A computer state where the system dispatches user mode (application) threads and they execute. In this state, devices (peripherals) are dynamically having their power state changed. The user will be able to select (through some user interface) various performance/power characteristics of the system to have the software optimize for performance or battery life. The system responds to external events in real time. It is not safe to disassemble the machine in this state.

G1 - Sleeping:

A computer state where the computer consumes a small amount of power, user mode threads are not being executed, and the system "appears" to be off (from an end user's perspective, the display is off, etc.). Latency for returning to the Working state varies on the wakeup environment selected prior to entry of this state (for example, should the system answer phone calls, etc.). Work can be resumed without rebooting the OS because large elements of system context are saved by the hardware and the rest by system software. It is not safe to disassemble the machine in this state.

G2/S5 - Soft Off:

A computer state where the computer consumes a minimal amount of power. No user mode or system mode code is run. This state requires a large latency in order to return to the Working state. The system's context will not be preserved by the hardware. The system must be restarted to return to the Working state. It is not safe to disassemble the machine.

G3 – Mechanical Off:

A computer state that is entered and left by a mechanical means. It is implied by the entry of this off state through a mechanical means that the no electrical current is running through the circuitry and it can be worked on without damaging the hardware or endangering the service personnel. The OS must be restarted to return to the Working state. No hardware context is retained. Except for the real time clock, power consumption is zero.

Sleeping State Definitions

Sleeping states (Sx states) are types of sleeping states within the global sleeping state, G1. The Sx states are briefly defined below. For a detailed definition of the system behavior within each Sx state, refer to ACPI specification section 7.5.2. For a detailed definition of the transitions between each of the Sx states, refer to ACPI specification section 9.1.

S1 Sleeping State:

The S1 sleeping state is a low wake-up latency sleeping state. In this state, no system context is lost (CPU or chip set) and hardware maintains all system context.

S2 Sleeping State:

The S2 sleeping state is a low wake-up latency sleeping state. This state is similar to the S1 sleeping state except the CPU and system cache context is lost (the OS is responsible for maintaining the caches and CPU context). Control starts from the processor's reset vector after the wake-up event.

S3 Sleeping State:

The S3 sleeping state is a low wake-up latency sleeping state where all system context is lost except system memory. CPU, cache, and chip set context are lost in this state. Hardware maintains memory context and restores some CPU and L2 configuration context. Control starts from the processor's reset vector after the wake-up event.

S4 Sleeping State:

The S4 sleeping state is the lowest power, longest wake-up latency sleeping state supported by ACPI. In order to reduce power to a minimum, it is assumed that the hardware platform has powered off all devices. Platform context is saved in disk.

S5 Soft Off State:

The S5 state is similar to the S4 state except the OS does not save any context nor enable any devices to wake the system. The system is in the "SOFT" off state and requires a complete boot when awakened. Software uses a different state value to distinguish between the S5 state and the S4 state to allow for initial boot operations within the BIOS to distinguish whether or not the boot is going to wake from a saved memory image.

3.5.2 System Power Plane

The system components are grouped as the following parties to let the system to control the On/Off of power under different power management modes.

The power plane is divided as following:

Power Group	Power Control Pin	Controlled Devices
B+	Nil	IMM, (9V~12V)
+3VA	Nil	PIC16C62A, VT82C686B(RTC I/F), Internal Modem, PMU07
+12V	PWRON	PCMCIA card , AC97 codec
+5V	PWRON	PCMCIA Slot 5V
+3V	PWRON	VGA, PCMCIA, PCMCIA Slot 3V, DRAM, Twister(DRAM I/F), M38867, MAX3243
+5VS	SUSB#	Flash ROM, HDD, CD-ROM, USB, Internal K/B, Glide Pad, External PS/2 Mouse, Audio AMP, Fan

+3VS	SUSB#	VT82C686B (ISA I/F Power), Clock Generator & Buffer (W137)
+RTCVCCS	Nil	VT82C686B (RTC)

3.5.3 Global System State Definitions

Global system states (Gx states) apply to the entire system and are visible to the user.

Following is a list of the system states:

G0/S0 – Working

A computer state where the system dispatches user mode (application) threads and they execute. In this state, devices (peripherals) are dynamically having their power state changed. The user will be able to select (through some user interface) various performance/power characteristics of the system to have the software optimize for performance or battery life. The system responds to external events in real time. It is not safe to disassemble the machine in this state.

G1 - Sleeping

A computer state where the computer consumes a small amount of power, user mode threads are not being executed, and the system "appears" to be off(from an end user's perspective, the display is off, etc). Latency for returning to the Working state varies on the wakeup environment selected prior to entry of this state (for example, should the system context are saved by the hardware and the rest by system software. It is not safe to disassemble the machine in this state.

G2/S5 – Soft Off

A computer state where the computer consumes a minimal amount of power. No user mode or system mode code is running. This state requires a large latency in order to return to the Working state. The system's context will not be preserved by the hardware. The system must be restarted to return to the Working state. It is not safe to disassemble the machine.

G3 – Mechanical Off

A computer state that is entered and left by a mechanical means. It is implied by the entry of this off state through a mechanical means that the no electrical current is running through the circuitry and it can be worked on without damaging the hardware or endangering the service personnel. The OS must be restarted to return to the Working state. No hardware context is retained. Except for the real time clock, power consumption is zero.

3.5.4 Device Power State Definitions

Device # CPU K+

C0 Power State	-CPU executes instruction
C1 Power State	-CPU is in Auto Halt State
C2 Power State	-CPU is in Stop Clock mode
C3 Power State	-CPU is in Stop Clock mode

Device # HDD

D0 Power State	-HDD is accessing or idle
D1 Power State	-HDD is in standby mode -D1 is resumed by any access
D2 Power State	-HDD is in sleep mode -D2 is resumed by reset
D3 Power State	-Same with D2

Device # CD-ROM

D0 Power State	-CD-ROM is accessing or idle (motor on)
D1 Power State	-CD-ROM is in standby mode -D1 is resumed by any access
D2 Power State	-CD-ROM is in sleep mode -D2 is resumed by reset
D3 Power State	-Same with D2

Device # VGA

D0 Power State	-VGA is accessing or idle
D1 Power State	-VGA is in standby mode -D1 is resumed by any access
D2 Power State	-VGA is in suspend mode -D2 is resumed by access
D3 Power State	-Same with D2

Device # Modem

D0 Power State	-Modem is accessing or idle
D1 Power State	-Modem is in standby mode -D1 is resumed by any access
D2 Power State	-Same with D1
D3 Power State	-Same with D1

Device # PCMCIA

D0 Power State	-PCMCIA is accessing or idle
D1 Power State	-PCMCIA is in RUN# mode
D2 Power State	-PCMCIA is in suspend mode
D3 Power State	-Same with D2

Device # NIC

D0 Power State	-NIC is accessing or idle
D1 Power State	-Snooze is in CLKRUN is asserted
D2 Power State	-Sleep mode, PCI chip in suspend mode
D3 Power State	-Power down mode, both PCI and phyter in sleep mode.

3.5.5 Sleeping State Definitions

Sleeping states (Sx states) are types of sleeping states within the global sleeping state, G1. The Sx states are briefly defined below. For a detailed definition of the system behavior within each Sx state and transition, refer to the ACPI specification.

S1 Sleeping State

The S1 sleeping state is a low wake-up latency sleeping state. In this state, no system context is lost (CPU or chip set) and hardware maintains all system context.

S2 Sleeping State

The S2 sleeping state is a low wake-up latency sleeping state. This state is similar to the S1 sleeping state except the CPU and system cache context is lost (the OS is responsible for maintaining the caches and CPU context). Control starts from the processor's reset vector after the wake-up event.

S3 Sleeping State (STR mode)

The S3 sleeping state is a low wake-up latency sleeping state where all system context is lost except system memory. CPU, cache, and chip set context are lost in this state. Hardware maintains memory context and restores some CPU and L2 configuration context. Control starts from the processor's reset vector after the wake-up event.

S4 Sleeping State (STD mode)

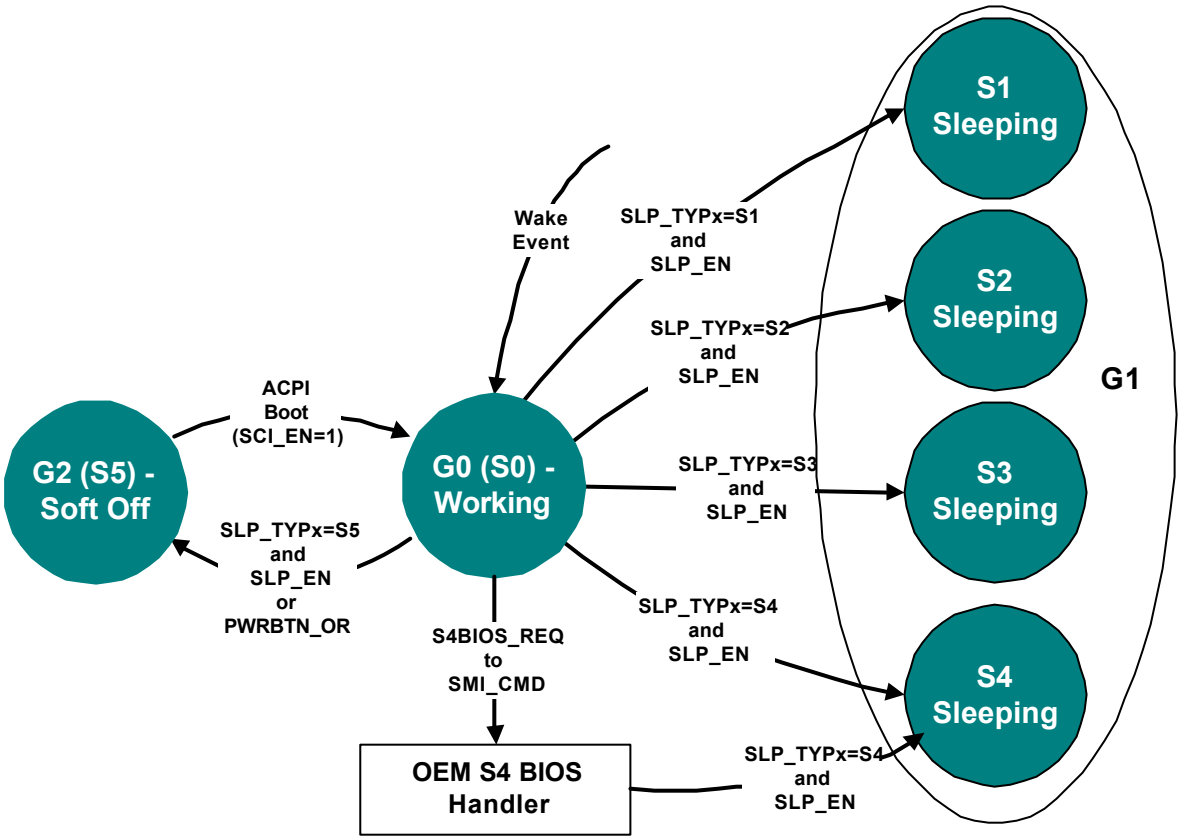
The S4 sleeping state is the lowest power, longest wake-up latency sleeping state supported by ACPI. In order to reduce power to a minimum, it is assumed that the hardware platform has powered off all devices. Platform context is saved in disk.

S5 Soft Off State

The S5 state is similar to the S4 state except the OS does not save any context nor enable any devices to wake the system. The system is in the "SOFF" off state and requires a complete boot when awakened. Software uses a different state value to distinguish between the S5 state and the S4 state. This is to allow for initial boot operations within the BIOS to distinguish whether or not the boot is going to wake from a saved memory image.

3.5.6 Power Management Mode Transition Flow Chart

From a user-visible level, the system can be thought of as being one of the states in the following diagram:



3.5.7 Power States transition event

The following table summarizes the entry events and wake-up events of each power:

Power State	Entry Event	Wake up Event
S1	OSPM control, Sleep Button, Lid Close	Sleep button Ring Indicator PME Event LAN Wake Up Lid Open Schedule Alarm
S4	OSPM control, Power Button Lid Close Battery Low - Low	Power Button Schedule Alarm
S5	Power Button Execute Windows shutdown command	Power Button

OSPM: OS-directed Power Management

3.5.8 Lid Switch

Display mode	Power States	Lid Close	Lid Open
LCD	G0	S3	G0
	S3~S5	No active	No active
CRT	G0	No active	No active
	S3~S5	No active	No active
SIMUL	G0	CRT	No active
	S3~S5	No active	No active

ⓘ If dual view enable lid close always suspend.

3.5.9 Power Button and Internet / Mail Button

Button	State			
	G0	S1	S4	S5
Power	Power off	Power off	No active	G0

ⓘ *Press power and suspend button reset PIC

3.5.10 Device Power Control Methodology

This section illustrates the power control status of each key device/component of the system under each power management mode.

PowerState Component	Doze	STR	STD/SOff
CPU	Stop Grant	Stop Clock	Power Off
L2 CACHE	ON	Power Down	Power Off
VT8603	ON	Stop Clock	Power Off
VT82C686B	ON	ON	Power Off (except SUSVcc, RTCVcc)
DRAM	ON	Self Refresh	Power Off
Clock Synthesizer	ON	Low Power	Power Off
CDROM	ON	Power Down	Power Off
HDD	ON	Power Down	Power Off
FDD	ON	Power Down	Power Off
KBC	ON	ON	Power Off
PIC16C62A	ON	ON	Power Down
PMU07	ON	ON	Power Down
VGA/VRAM	ON	Power Down	Power Off
PCMCIA	ON	Power Down	Power Off
Super I/O	ON	Power Down	Power Off

AUDIO	ON	Power Down	Power Off
Audio AMP	ON	Power Down	Power Off
LCD Backlight	ON	Power Off	Power Off
Serial Port	ON	Power Down	Power Off
IR Module	ON	Power Down	Power Off
LAN	ON	Power Down	Power Down
Internal Modem	ON	Power Down	Power Down

Device Power control Methodology During S2 Mode

This section illustrates the control methodology of each device/component and its details under Stand by mode.

Device	Power Down Controlled by	Description
CPU	Hardware	Controlled by SUS_STAT1# pin
L2 CACHE	Hardware	Controlled by BIOS
VT8603	Hardware	Controlled by SUS_STAT1# pin
VT82C686B	Working	
DRAM	Hardware	Self Refresh
Clock Synthesizer	Hardware	Controlled by SUSA# pin
CDROM	Software	CDROM support power down command
HDD	Software	HDD support power down command
FDD	Software	FDD support power down command
KBC	Working	
PIC16C62A	Working	
VGA/VRAM	Software	Controlled by VT8603
PCMCIA	Software	Controlled by Driver enter Dx status
Super I/O	Software	Controlled by VT82C686B
AUDIO	Software	Controlled by VT82C686B
Audio AMP	Software	Controlled by BIOS
LCD Backlight	Hardware	Controlled by VGA chip
Serial Port	Software	Controlled by PMU07 GPIO[B3] pin
IR Module	Software	IR module support power down command
LAN	Software	LAN support power down

		command
Internal Modem	Software	Modem support power down command

Device Power Control Methodology During S1 Mode

This section illustrates the control methodology of each device/component and its details under Suspend to RAM mode.

Device	Power Down Controlled by	Description
CPU	Hardware	Controlled by SUSB# pin
L2 CACHE	Hardware	Power off
VT8603	Hardware	Controlled by SUSB# pin
VT82C686B	Hardware	Controlled by SUSB# pin
DRAM	Software	Self Refresh
Clock Synthesizer	Hardware	Controlled by SUSB# pin
CDROM	Hardware	Power off
HDD	Hardware	Power off
FDD	Hardware	Power off
KBC	Software	Controlled by M38867 power down command
PIC16C62A	Software	Controlled by PIC16C62A power down command
PMU07	Sofeware	Controlled by PMU07 power down command
VGA/VRAM	Software	Controlled by VT8603
PCMCIA	Software	Controlled by SUSB# pin
Super I/O	Hardware	Controlled by VT82C686B
AUDIO	Hardware	Controlled by VT82C686B
Audio AMP	Hardware	Controlled by BIOS
LCD Backlight	Hardware	Power off
Serial Port	Software	Controlled by PMU07 GPIO[B3] pin
IR Module	Hardware	Controlled by SUSB# pin
LAN	Hardware	Controlled by Driver enter Dx status
Internal Modem	Hardware	Controlled by Driver enter Dx ststus

3.5.11 Expanding Event Through the Embedded Controller

The following figure shows the relationships between the devices that are wired to the embedded controller, the embedded controller queries, and ACPI general

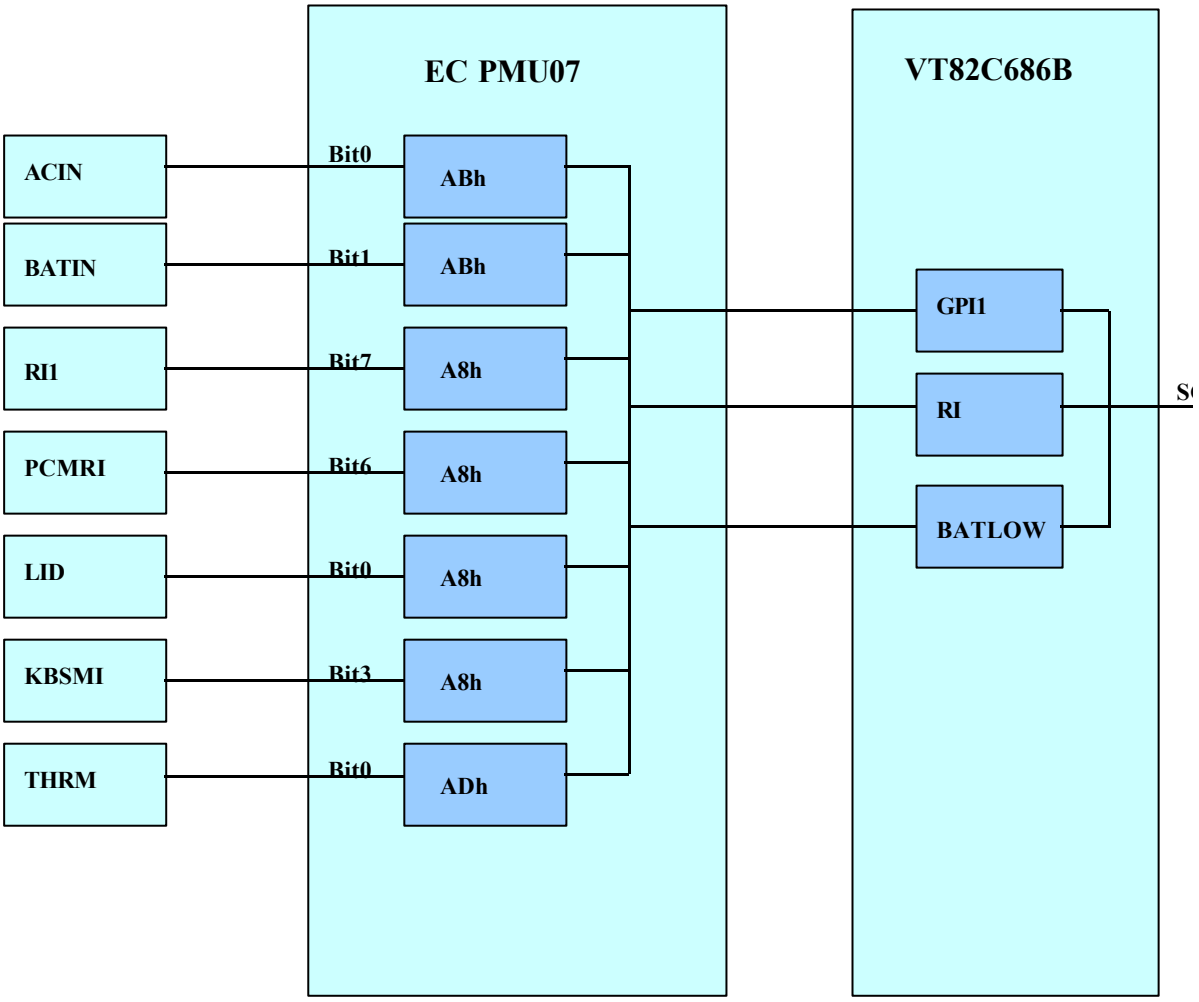


Figure 3-2 The Relationships between ACPI, Controller, and Device

SCI Source and GPE Event from PMU07

PMU07	Input Event	GPE Event	Handler
ADPIN0	AC Plug In / Out	GPI1	AML Handler
BAT00	Battery Plug In / Out	GPI1	AML Handler
GPIOA0	LID Event	RI	AML Handler

GPIOA3	KB SMI event	RI	AML Handler
GPIOA6	PCMCIA Ring In	RI	AML Handler
GPIOA7	COM Port Ring In	RI	AML Handler
THRM	Thermal Event	GPI1	AML Handler

The system will issue a beep to inform user while the following SCI alerted:

- AC (AC status change) update battery information.
- Battery A (Power status change) update battery information.
- Lid (Lid close /open event) update Lid position status.
- RI10 COM Port Ring Event
- PCMRI10 PCMCIA Ring Event
- PME (Modem SCI) update system power status.

Control Method Battery Subsystem

EC should support all the battery information to ACPI-OS

- Designed Battery capacity
- Designed Voltage
- Designed Low battery capacity
- Designed Low – Low battery capacity
- Latest Full charged capacity
- Present Remaining capacity
- Present drain rate
- Present voltage
- Present Battery Status

ACPI BIOS should support an independent device object in the name space, and implement the following methods.

3.5.12 Thermal Control

ACPI allows the OS to be proactive in its system cooling policies. With the OS in control of the operating environment, cooling decisions can be made based on application load on the CPU and the thermal heuristics of the system. Graceful shutdown of the OS at critical heat levels becomes possible as well. The following sections describe the thermal objects available to the OS to control platform temperature. ACPI expects all temperatures to be given in tenths of Kelvin.

The ACPI thermal design is based around regions called *thermal zones.* Generally, the entire PC is one large thermal zone, but an OEM can partition the system into several thermal zones if necessary.

Active, Passive, and Critical Policies

There are three primary cooling policies that the OS uses to control the thermal state of the hardware. The policies are *Active, Passive* and *Critical:*

- **Passive cooling:** The OS reduces the power consumption of the system to reduce the thermal output of the machine by slowing the processor clock. The _PSV control method is used to declare the temperature to start passive cooling.
- **Active cooling:** The OS takes a direct action such as turning on a fan. The _AC*x* control methods declare the temperatures to start different active cooling levels.
- **Critical trip point:** This is the threshold temperature at which the OS performs an orderly, but critical, shut down of the system. The _CRT object declares the critical temperature at which the OS must perform a critical shutdown.

When a thermal zone appears, the OS runs control methods to retrieve the three temperature points at which it executes the cooling policy. When the OS receives a thermal SCI it will run the _TMP control method, which returns the current temperature of the thermal zone. The OS checks the current temperature against the thermal event temperatures. If _TMP is greater than or equal to _AC*x* then the OS will turn on the associated active cooling device(s). If _TMP is greater than or equal to _PSV then the OS will perform CPU throttling. Finally if _TMP is greater than or equal to _CRT then the OS will shutdown the system.

An optimally designed system that uses several SCI events can notify the OS of thermal increase or decrease by raising an interrupt every several degrees. This enables the OS to anticipate _AC*x*, PSV, or _CRT events and incorporate heuristics to better manage the systems temperature.The operating system can request that the hardware change the priority of active cooling vs passive cooling.

Dynamically Changing Cooling Temperatures

An OEM can reset _ACx and _PSV and notify the OS to reevaluate the control methods to retrieve the new temperature settings. The following three causes are the primary uses for this thermal notification:

- When a user changes from one cooling mode to the other.
- When a swappable bay device is inserted or removed. A swappable bay is a slot that can accommodate several different devices that have identical form factors, such as a CD-ROM drive, disk drive, and so on. Many mobile PCs have this concept already in place.
- When the temperature reaches an _AC*x* or the _PSV policy settings

In each situation, the OEM-provided AML code must execute a **Notify** (*thermal_zone*, 0x80) statement to request the OS to re-evaluate each policy temperature by running the _PSV and _AC*x* control methods.

- **Resetting Cooling Temperatures from the User Interface**

  When the user employs the UI to change from one cooling mode to the other, the following occurs:

1. The OS notifies the hardware of the new cooling mode by running the Set Cooling Policy (_SCP) control method.
2. When the hardware receives the notification, it can set a new temperature for both cooling policies and notify the OS that the thermal zone policy temperatures have changed.
3. The OS re-evaluates _PSV and _ACx.

- **Resetting Cooling Temperatures to Adjust to Bay Device Insertion or Removal**

The hardware can adjust the thermal zone temperature to accommodate the maximum operating temperature of a bay device as necessary. For example,

1. Hardware detects that a device was inserted into or removed from the bay and resets the _PSV and/or _AC*x* and then notifies the OS of the thermal and device insertion events.
2. The OS reenumerates the devices and reevaluates _PSV and _ACx.

- **Resetting Cooling Temperatures to Implement Hysteresis**

An OEM can build hysteresis into platform thermal design by dynamically resetting cooling temperatures. For example,

1. When the heat increases to the temperature designated by _AC*x*, the OS will turn on the associated active cooling device and the hardware will reset the AC*x* value to a lower temperature.
2. The hardware will then run the Notify command and the OS will reevaluate the new temperatures. Because of the lower _AC*x* value now, the fan will be turned off at a lower temperature than when turned on.
3. When the temperature hits the lower _AC*x* value, the OS will turn off the fan and reevaluate the control methods when notified.

3.5.13 Hardware Thermal Events

An ACPI-compatible OS expects the hardware to generate a thermal event notification through the use of the SCI. When the OS receives the SCI event, it will run the _TMP control method to evaluate the current temperature. Then the OS will compare the value to the cooling policy temperatures. If the temperature has crossed over one of the three policy thresholds, then the OS will actively or passively cool (or stop cooling) the system, or shutdown the system entirely.

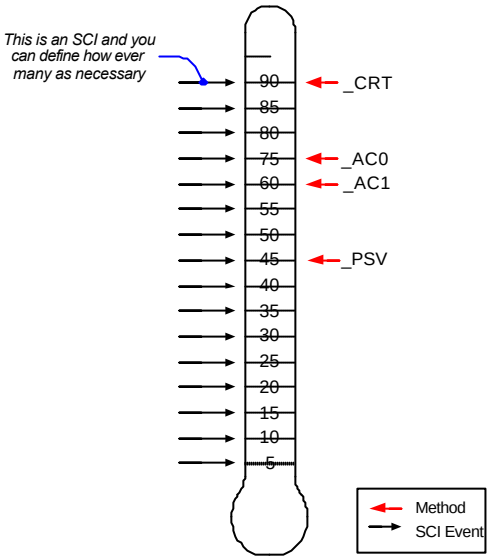


Figure 3-3 SCI Events

Both the number of SCI events to be implemented and the granularity of the temperature separation between each SCI event is OEM-specific. However, it is important to note that since the OS can use heuristic knowledge to help cool the system, the more events the OS receives the better understanding it will have of the system thermal characteristic.

3.5.14 Active Cooling Strength

The Active cooling methods (_Ac*x*) in conjunction with active cooling lists (_AL*x*), allows an OEM to use a device that offers varying degrees of cooling capability or multiple cooling devices. The _AC*x* method designates the temperature at which the Active cooling is enabled or disabled (depending upon the direction in which the temperature is changing). The _AL*x* method evaluates to a list of devices that actively cool the zone. For example:

- If a standard single-speed fan is the Active cooling device, then the policy is represented by the temperature to which _AC0 evaluates, and the fan is listed in _AL0.
- If the zone uses two independently-controlled single-speed fans to regulate the temperature, then _AC0 will evaluate to the maximum cooling temperature using two fans, and _AC1 will evaluate to the standard cooling temperature using one fan.
- If a zone has a single fan with a low speed and a high speed, the _AC0 will evaluate to the temperature associated with running the fan at high-speed, and _AC1 will evaluate to the temperature associated with running the fan at low speed. _AL0 and _AL1 will both point to different device objects associated with the same physical fan, but control the fan at different speeds.

3.5.15 Passive Cooling Equation

Unlike the case for _AC*x*, during passive cooling the OS takes the initiative to actively monitor the temperature in order to cool the platform. On an ACPI-compatible platform that properly implements CPU throttling, the temperature transitions will be similar to the following figure.

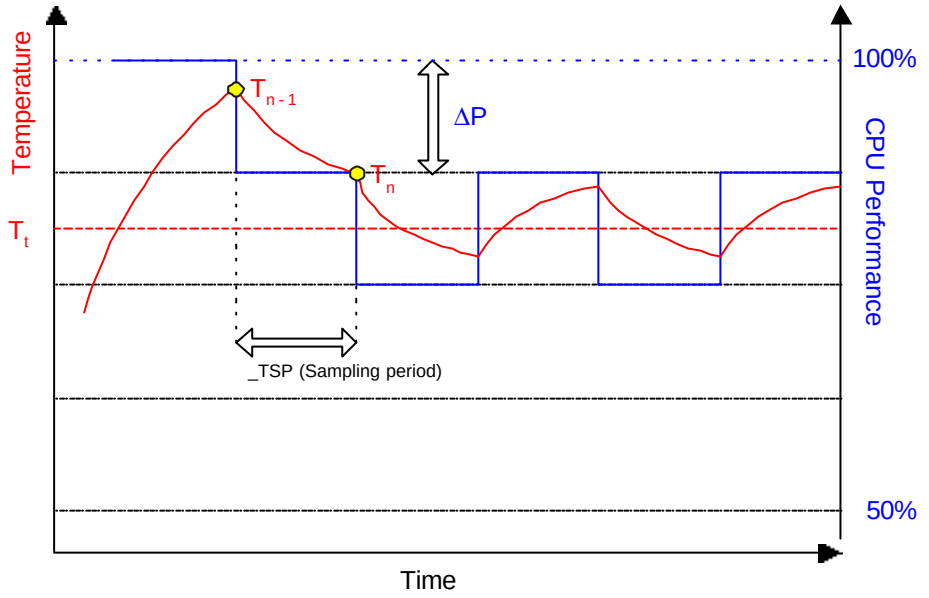


Figure 3-4 Temperature and CPU Performance Versus Time

For the OS to assess the optimum CPU performance change required to bring the temperature down, the following equation must be incorporated into the OS.

$$\Delta P\ [\%] = \_TC1 * (Tn - Tn\text{-}1) + \_TC2 * (Tn - Tt)$$

where

Tn = current temperature
Tt = target temperature (_PSV)

The two coefficients _TC1 and _TC2 and the sampling period _TSP are hardware-dependent constants the OEM must supply to the OS (for more information, see section 12.3). The object _TSP contains a time interval that the OS uses to poll the hardware to sample the temperature. Whenever _TSP time has elapsed, the OS will run _TMP to sample the current temperature (shown as Tn in the above equation). Then the OS will use the sampled temperature and _PSV (which is the target temperature Tt) to evaluate the equation for ΔP. The granularity of ΔP is determined by the CPU duty width of the system. A detailed explanation of this thermal feedback equation is beyond the scope of this specification.

3.5.16 Critical Shutdown

When the heat reaches the temperature indicated by _CRT, the OS must immediately shutdown the system. The system must disable the power either after the temperature reaches some hardware-determined level above _CRT or after a predetermined time has passed.

Before disabling power, platform designers should incorporate some time that allows the OS to run its critical shutdown operation. There is no requirement for a minimum shutdown operation window that commences immediately after the temperature reaches _CRT. This is because

- Heat might rise rapidly in some systems and slower on others, depending on casing design and environmental factors.
- Shutdown can take several minutes on a server and only a few short seconds on a hand-held device.

Because of this indistinct discrepancy and the fact that a critical heat situation is a remarkably rare occurrence, ACPI does not specify a target window for a safe shutdown. It is entirely up to the OEM to build in a safe buffer that it sees fit for the target platform.

3.5.17 Other Implementation Of Thermal Controllable Devices

The ACPI thermal event model is flexible enough to accommodate control of almost any system device capable of controlling heat. For example, if a mobile PC requires the battery charger to reduce the charging rate in order to reduce heat it can be seamlessly implemented as an ACPI cooling device. Associating the charger as an active cooling device and reporting to the OS target temperatures that will enable or disable the power resource to the device do this. Figure as following illustrates the implementation. Because the example does not create noise, this will be an implementation of *silence* mode.

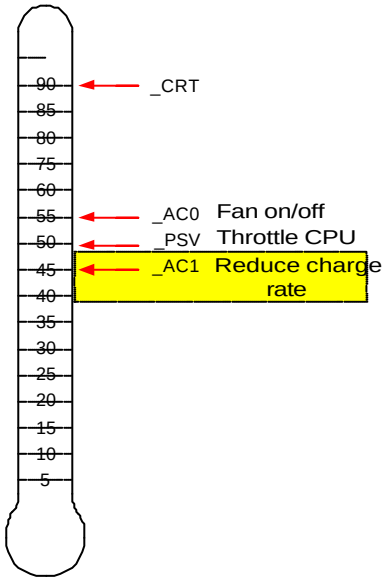


Figure 3-5 Other Thermal Control

3.5.18 Thermal Control Methods

Control methods and objects related to thermal management are listed in the table below.

Object	Description
_AC*x*	Returns Active trip point in tenths Kelvin
_AL*x*	List of pointers to active cooling device objects
_CRT	Returns critical trip point in tenths Kelvin
_PSL	List of pointers to passive cooling device objects
_PSV	Returns Passive trip point in tenths Kelvin
_SCP	Sets user cooling policy (Active or Passive)
_TC1	Thermal constant for Passive cooling
_TC2	Thermal constant for Passive cooling
_TMP	Returns current temperature in tenths Kelvin
_TSP	Thermal sampling period for Passive cooling in tenths of seconds

_AC*x*

This control method returns the temperature at which the OS must start or stop Active cooling, where *x* is a value between 0 and 9 that designates multiple active cooling levels of the thermal zone. If the Active cooling device has one cooling level (that is, n") then that cooling level is named _AC0. If the cooling device has two levels of capability, such as a high fan speed and a low fan speed, then they are named _AC0 and _AC1 respectively. The smaller the value of *x*, the greater the cooling strength _AC*x* represents. In the above example, _AC0 represents the greater level of cooling (the faster fan speed) and _AC1 represents the lesser level of cooling (the slower fan speed). For every AC*x* method, there must be a matching AL*x* method.

Arguments: None.

Result Code: Temperature in tenths Kelvin

The result code is an integer value that describes up to 0.1 precisions in Kelvin. For example, 300.0K are represented by the integer 3000.

_AL*x*

This object evaluates to a list of Active cooling devices to be turned on when the associated _ACx trip point is exceeded. For example, these devices could be fans.

_CRT

This control method returns the critical temperature at which the OS must shutdown the system.

Arguments: None.

Result Code: Temperature in tenths Kelvin

The result is an integer value that describes up to 0.1 precisions in Kelvin. For example, 300.0K are represented by the integer 3000.

_PSL

This object evaluates to a list of processor objects to be used for Passive cooling.

_PSV

This control method returns the temperature at which the OS must activate CPU throttling.

Arguments: None.

Result Code: Temperature in tenths Kelvin.

The result code is an integer value that describes up to 0.1 precision in Kelvin. For example, 300.0 Kelvin is represented by 3000.

_SCP

This control method notifies the hardware of the current user cooling mode setting. The hardware can use this as a trigger to reassign _AC*x* and _PSV temperatures. The operating system will automatically evaluate _ACx and _PSV objects after executing _SCP.

Arguments: 0 - Active; 1 - Passive

Result Code: None.

_TC1

This is a thermal object that evaluates to the constant _ TC1 for use in the Passive cooling formula:

ΔPerformance [%]= _TC2 * (Tn - Tn-1) + _TC1 * (Tn. - Tt)

_TC2

This is a thermal object that evaluates to the constant _TC2 for use in the Passive cooling formula:

ΔPerformance [%]= _TC2 * (Tn - Tn-1) + _TC1 *.(Tn. - Tt)

_TMP

This control method returns the thermal zone current operating temperature in Kelvin.

Argument: None.

Result Code: Temperature in tenths Kelvin.

The result is an integer value that describes up to 0.1 precision in Kelvin. For example, 300.0K is represented by the integer 3000.

_TSP

This is an object that evaluates to a thermal sampling period used by the OS to implement the Passive cooling equation. This value, along with _TC1 and _TC2, will enable the OS to provide the proper hysteresis required by the system to accomplish an effective passive cooling policy. The granularity of the sampling period is 0.1second. For example, if the sampling period is 30.0 seconds, then _TSP needs to report 300; if the sampling period is 0.5 seconds, then it will report 5. The OS can normalize the sampling over a longer period if necessary.

3.5.19 AC Adapters and Power Source Objects

The Power Source objects describe the power source used to run the system.

Object	Description
_PSR	Returns present power source device
_PCL	List of pointers to powered devices.

_PSR

Returns the current power source devices. Used for the AC adapter and is located under the AC adapter object in name space. Used to determine if system is running off the AC adapter.
Arguments: None
Results code : **0x00000000** = Off-line; **0x00000001** = On-line

_PCL

This object evaluates to a list of pointers, each pointing to a device or a bus powered by the power source device. Pointing a bus means that all devices under the bus is powered by it power source device.

3.6 Battery Management

The A360 supports both Li-Ion and Ni-MH Battery Pack. There is only one battery pack activating at one time. The special designed Bridge Battery module can backup the system under Suspend To RAM mode for a short period of time.

3.6.1 Battery Sub-system

- The charger will stop charge the battery when the following condition is detected.
  - The temperature of the system is too high
  - The remaining capacity is 95% and more.
- Battery Life → 2.5 to 3 Hours.
- Battery reading methodology is through PMU07 SMBus.

Note that the battery life is dependent on different configuration running. E.g. with CD-ROM battery life is shorter, document keyin only battery life is longer, PMU disable battery life is short, PMU enable battery life is longer.

3.6.2 Battery Low Warning

When the battery capacity remains 8%, the PMU07 will generate a battery warning SMI. The system will do the following action.

- The Power LED Indicator will continually blinking with 1 Hz.
- The system issues a warning beep (3 beeps at once).

3.6.3 Battery Low

When the battery capacity remains 3%, the system will generate a battery low SMI. The system will do the following action.

- The system will enter Suspend To Disk mode even the power management is disabled.

– The function of power-on or Resume will be inhibited until the battery low condition is removed.

3.6.4 AC Adapter

When plug in the AC adapter, the system will do the following action:

– The charger will charge the Main Battery, if it is possible.
– The Battery Charging Indicator will turn on if the battery is in changing mode.
– The power management function will be disabled, if the Setup item of "Power Management" is set to "Battery Only".

3.7 PMU07

The Embedded controller PMU07 acts as a supplement for power management control. It supports a lot of functions via SMBus interface.

3.7.1 The System EC RAM with PMU07

Embedded Controller Command Set
The EC I/F command set allows the OS to communicate with the PMU07.
For detail information refer to ACPI 1.0B specification.

EC I/F Command	Command Byte Encoding	Byte	Register	R / W	Description	Interrupt
Read Embedded Controller (RD_EC)	0x80	#1	EC_SC	W	Command byte Header	Interrupt on IBF=0
		#2	EC_DATA	W	Address byte to read	No Interrupt
		#3	EC_DATA	R	Read data to host	Interrupt on OBF=1
Write Embedded Controller (WR_EC)	0x81	#1	EC_SC	W	Command byte Header	Interrupt on IBF=0
		#2	EC_DATA	W	Address byte to write	Interrupt on IBF=0
		#3	EC_DATA	W	Data to write	Interrupt on IBF=0
Burst Enable Embedded Controller (BE_EC)	0x82	#1	EC_SC	W	Command byte Header	No Interrupt
		#2	EC_DATA	R	Burst acknowledge byte	Interrupt on OBF=1
Burst Disable Embedded Controller (BD_EC)	0x83	#1	EC_SC	W	Command byte Header	Interrupt on IBF=0
Query Embedded Controller (QR_EC)	0x84	#1	EC_SC	W	Command byte Header	No Interrupt
		#2	EC_DATA	R	Query value to host	Interrupt on OBF=1

3.7.2 PMU07 EC RAM List

The micro controller PMU07 acts as a supplement for power management control. It supports the following functions via SMBus Command **(0x80 , 0xC0)**

Function	Address	Register Name	R/W	Bit Number 7	6	5	4	3	2	1	0	Logic	Default	Description
1st Battery [_BIF]	00h *3	Power unit	R(/W)	DATA[15:0] *1								-	0xffff	0x0000: mWh [Fixed value] 0xffff: Unknown
	02h *3	Design capacity	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xfffe(mWh) 0xffff: Unknown
	04h *3	Last Full Charge Capacity	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xfffe(mWh) 0xffff: Unknown
	06h *3	Battery Technology	R(/W)	DATA[15:0] *1								-	0xffff	0x0000 : Primary 0x0001: Secondary [Fixed value] 0xffff: Unknown.
	08h *3	Design Voltage	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xfffe(mV) 0xffff: Unknown
	0Ah *3	Design capacity of Warning	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xfffe(mWh) 0xffff: Unknown
	0Ch *3	Design capacity of Low	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xfffe(mWh) 0xffff: Unknown
	0Eh *3	Battery capacity Granularity 1	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xfffe(mWh) 0xffff: Unknown
	10h *3	Battery capacity Granularity 2	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xfffe(mWh) 0xffff: Unknown
	12h *3	Model number	R(/W)	DATA[15:0] *1								-	0xffff	0x0000 [Not support]
	14h *3	Serial Number	R(/W)	DATA[15:0] *1								-	0xffff	0x0000 [Not support]
	16h *3	Battery type	R(/W)	DATA[15:8] *1 All bits are 0								-	0xffff	CELL_TYPE [3:0] This code depends on battery data format. In the future, this code may be added. 0x00: NiMH 0x01: Li-ion 0x10: Non-rechargeable battery (Reserved)
	18h *3	OEM Information	R(/W)	DATA [15:8] *1 All bits are 0								-	0xffff	Vender [7:0] This code depends on battery data format. And the following name should be described in the ASL with the same character code. In the future, these codes will be added. 0: "MoliEnergy" 1: "Panasonic" 2: "" (SANYO does not agree) 3: "TBCL" (Toshiba) 4: "Sony"

CELL_TYPE [7:0]
Vender[7:0]

*1: The register type is word.

*3: This register is not cleared if the system is in S4-S5 state.

R(/W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

Function	Address	Register Name	R/W	Bit Number 7	6	5	4	3	2	1	0	Logic	Default	Description
1st Battery [_BST]	1Ah *3	Battery State	R(/W)	DATA[15:3] *1 All bits are 0					CRIT	CHG	DCHG	-	-	DCHG=1: The battery is discharged CHG =1 : The battery is charged CRIT =1 : The battery is critical (Empty)
	1Ch *3	Battery Present rate	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xfffe(mW) 0xffff: Unknown
	1Eh *3	Battery Remaining Capacity	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xfffe(mWh) 0xffff: Unknown
	20h *3	Battery present Voltage	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xfffe(mV) 0xffff: Unknown
1st Battery [_BTP]	22h	Battery Trip Point	R/W	DATA[15:0] *1								-	0x0000	0x0000 :Clear the trip point 0x0001-0xffff(mWh)
2nd Battery [_BIF]	24h to 3Ch *3	*2	*2	*2								*2	*2	*2
2nd Battery [_BST]	3Eh to 44h *3	*2	*2	*2								*2	*2	*2
2nd Battery [_BTP]	46h	*2	*2	*2								*2	*2	*2
-	48h	Battery data Size	R(/W)	DATA[7:0]								-	-	0x01 : DATA size is 3byte.(PMU06A) 0x00 :DATA size is 2 byte. (PMU06) *8
1st Battery [_BIF]	49h	Design capacity	R(/W)	DATA[23:16] *1 *7								-	0xff	PMU06A use this data with 02/03h. *7 *8
	4Ah	Last Full Charge Capacity	R(/W)	DATA[23:16] *1 *7								-	0xff	PMU06A use this data with 04/05h. *7 *8
1st Battery [_BST]	4Bh	Battery Remaining Capacity	R(/W)	DATA[23:16] *1 *7								-	0xff	PMU06A use this data with 1E/1Fh. *7 *8
1st Battery [_BTP]	4Ch	Battery Trip Point	R(/W)	DATA[23:16] *1 *7								-	0x00	PMU06A use this data with 22/23h. *7 *8
2nd Battery [_BIF]	4Dh	Design capacity	R(/W)	DATA[23:16] *1 *7								-	0xff	PMU06A use this data with 26/27h. *7 *8
	4Eh	Last Full Charge Capacity	R/(/W)	DATA[23:16] *1 *7								-	0xff	PMU06A use this data with 28/29h. *7 *8
2nd Battery [_BST]	4Fh	Battery Remaing Capacity	R(/W)	DATA[23:16] *1 *7								-	0xff	PMU06A use this data with 42/43h. *7 *8
2nd Battery [_BTP]	50h	Battery Trip Point	R(/W)	DATA[23:16] *1 *7									0x00	PMU06A use this data with 46/47h. *7 *8
	51h to 6Bh *3	Reserved	R/W	Don' t care								-	-	

*1: The register type is word.
*2: Same as 1st Battery CMBatt Data.
*3: This register is not cleared if the system is in S4-S5 state.
R(/W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

Function	Address	Register Name	R/W	Bit Number 7	6	5	4	3	2	1	0	Logic	Default	Description
PMU Access	6Ch	PMU_LOW_ADR	R/W	DATA [7:0]								-	-	These registers are available when PMU slave mode or charger mode is selected. For detail information, refer to PMU slave communication section in this document
	6Dh	PMU_HIG_ADR	R/W	DATA [15:8]								-	-	
	6Eh	CHECK_SUM	R/W	DATA [7:0]								-	-	
	6Fh	PMU_DATA	R/W	DATA [7:0]								-	-	
SMBus	70h *7	SMB_PTCL	R/W	PROTOCOL[7:0]								-	-	For detail information, refer to ACPI 1.0 specification [13.9 SMBus Host controller Interface via Embedded controller] These registers are not available when PMU slave mode or charger mode is selected. The PMU06 has access protect function for the EEPROM in the battery, to cancel the protection, set the access protect cancel bit. For detail, refer to SMBus section
	71h *7	SMB_STS	R/W	DONE	ALRM	RES	STATUS [4:0]					-	-	
	72h	SMB_ADDR	R/W	ADDRESS [6:0]							RES	-	-	
	73h	SMB_CMD	R/W	COMMAND								-	-	
	74h to 93h	SMB_DATA [0-31]	R/W	DATA								-	-	
	94h	SMB_BCNT	R/W	RES[7:5]			BCNT[4:0]					-	-	
	95h	SMB_ALARM_ADDR	R(/W)	ADDRESS[6:0]							RES	-	-	
	96h to 97h	AMB_ALARM_DATA[0-1]	R(/W)	DATA								-	-	
	98h	SMB_CNRL	R/W	RES[7:1]							PRT		0x00	PRT =1 : The SMBus address (A8-AE) protection is cancelled.
Reserve	99h to 9Fh	Reserved	R/W	Don't care								-	-	

*7: When polling checks this register, the interval time is necessary more than 500usec.

R(/W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

Function	Address	Register Name	R/W	Bit Number 7	6	5	4	3	2	1	0	Logic	Default	Description
Status	A0h *3	ADP_STS	R(/W)	RES[7:1]							CON	-	-	CON = 1 : AC adapter is connected
	A1h *3	BAT1_STS (1st Battery)	R(/W)	BTP	EMP	LOW	WAR	ERR	DCHG	CHG	CON	-	-	BTP =1: Battery trip point is detected. EMP =1: Battery is empty. LOW =1: Battery is Low battery state. WAR=1: Battery is Warning state. ERR =1: Battery is Error state. DCHG=1: Battery is discharged. CHG=1: Battery is charged. CON=1: Battery is connected.
	A2h *3	BAT2_STS (2nd Battery)	R(/W)	BTP	EMP	LOW	WAR	ERR	DCHG	CHG	CON	-	-	
	A3h *3	Reserved	R/W	Don't care								-	-	
	A4h *3	BAT1_CAP	R(/W)	BCAP								-	-	0x00-0x64 = 0-100(%) 0x7F = Unknown 0x80 = Not installed
	A5h *3	BAT2_CAP	R(/W)	BCAP								-	-	
	A6h *3	Reserved	R/W	Don't care								-	-	
	A7h	SMB_Alert_ ADDR	R/W	ADDRESS[6:0]							RES	-	0x00	SMBAlert output device address The alert response function is available when this register is cleared (0x00) only. When the several devices assert the alert signal at the same time, the least address is stored to this register. And when this register is cleared , next alert address is stored to this register.
	A8h *5	GPIO-A_ EVT_STS	R/W	STS_A [7:0]								Read 0:No event 1:EVT detection Write 0:Clear event 1:Ignore	0x00	To clear the notified event flag without unexpected event loss, clear the corresponding bit flag only. For this operation, this register has special writing manner as follows. **STS_X ← (STS_X) AND (Written data)**
	A9h *5	GPIO-B_ EVT_STS	R/W	0	STS_B [6:0]								0x00	
	AAh *5	GPIO-C_ EVT_STS	R/W	0	0	0	0	0	0	STS_C [1:0]			0x00	
	ABh *5	RUN_ EVT_STS	R/W	BTP2	SMB	ALRT	GPIO	RES	BAT2	BAT1	ADP	Read 0:No event 1:EVT detection Write 0:Clear event 1:Ignore	0x00	BTP2 =1: BTP2 event is detected SMB =1 : SMBus event is detected. ALRT=1 : SMBAlert is detected. GPIO =1 : GPIO event is detected. BATn=1 : Battery event is detected. ADP =1 : Battery event is detected. TH =1 : Thermal event is detected HIGH=1 : High alarm point is detected. LOW =1 : Low alarm point is detected. ERR =1 : Polling communication failure with retry.
	ACh *5	WAKE_ EVT_STS	R/W										0x00	
	ADh *5	RUN_ EVT_STS_2	R/W	Reserved [7:1]							TH		0x00	To clear the notified event flag without unexpected event loss, clear the corresponding bit flag only. For this operation, this register has special writing manner as follows. **STS_X ← (STS_X) AND (Written data)**
	AEh *5	WAKE EVT_STS_2	R/W	Reserved [7:1]							TH		0x00	
	AFh *5	THERMAL_ EVT_STS	R/W	Reserved [7:3]					ERR	LOW	HIGH		0x00	

*3: This register is not cleared if the system is in S4-S5 state.
*5: After writing to this register, Set the "00h" to the BURST_FLG_CLR register.
R(/W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

Function	Address	Register Name	R/W	Bit Number 7	6	5	4	3	2	1	0	Logic	Default	Description
Event/ GPIO Control	B0h	EC_RUN_ ENB	R/W	BTP2	SMB	ALRT	RES[4:1]				ADP	0: Disable 1: Enable	0x00	BTP2: BTP2 event SMB : SMBus event. ALRT: SMBAlert event. ADP: Adapter event.
	B1h	EC_WAKE_ ENB	R/W									0: Disable 1: Enable	0x00	
	B2h	BATT_RUN _ ENB	R/W	BTP	EMP	LOW	WAR	ERR	CAP	C/D	CON	0: Disable 1: Enable	0x00	BTP: Battery trip point EMP: Empty. LOW: Low battery WAR: Warning ERR: Error CAP: Capacity learning C/D: Charge/Discharge CON: Battery presence
	B3h	BATT_WAK E _ENB	R/W									0: Disable 1: Enable	0x00	
	B4h	GPIO-A_ IO_CONF	R/W	CONF_A [7:0]								0: Input 1: Output	0x00	For detail information, refer to GPIO section in this document.
	B5h	GPIO-A_ DATA	R/W	DATA_A [7:0]									-	
	B6h	GPIO-A_ RUN_ENB	R/W	RUN_ENB_A [7:0]								0: Disable 1: Enable	0x00	
	B7h	GPIO-A_ EVT_POL	R/W	POL_A [7:0]								0: Falling edge 1: Rising edge	0x00	
	B8h	GPIO-A_ WAKE_ENB	R/W	WAKE_ENB_A [7:0]								0: Disable 1: Enable	0x00	
	B9h	GPIO-B_ IO_CONF	R/W	1	CONF_B [6:0]							0: Input 1: Output	0x80	
	BAh	GPIO-B_ DATA	R/W	0	DATA_B [6:0]								-	
	BBh	GPIO-B_ RUN_ENB	R/W	0	RUN_ENB_B [6:0]							0: Disable 1: Enable	0x00	
	BCh	GPIO-B_ EVT_POL	R/W	0	POL_B [6:0]							0: Falling edge 1: Rising edge	0x00	
	BDh	GPIO-B_ WAKE_ENB	R/W	0	WAKE_ENB_B [6:0]							0: Disable 1: Enable	0x00	
	Beh	GPIO-C_ DATA	R/W	RES [7 :4] *4				DATA_C [3:0]					-	
	BFh	GPIO-C_ RUN_ENB	R/W	0	0	0	0	0	0	RUN _ENB _C [1:0]		0: Disable 1: Enable	0x00	

*4: Should be 0.

*6: This register' s response time is 150usec max.

Function	Address	Register Name	R/W	Bit Number 7	6	5	4	3	2	1	0	Logic	Default	Description	
Event/ GPIO Control	C0h	GPIO-C_ EVT_POL	R/W	0	0	0	0	0	0	POL _C [1:0]		0: Falling edge 1: Rising edge	0x00		
	C1h	GPIO-C_ WAKE_ENB	R/W	0	0	0	0	0	0	WAK E_ ENB _C [1:0]		0: Disable 1: Enable	0x00		
	C2h	EVT_CONT	R/W	RES [7:6]		WAKE	SCI	RES *4	Q_RUN	WAKE_OUT	SUS_X		0x00	WAKE SCI Q_Run WAKE_OUT Sus_X	=0: Wake# output is "Level". =1: Wake# output is "Pulse". =0: SCI is always output by event detection and SCI_EVT shows the query data is stored. And next SCI is not output until SCI_EVT is cleared. =1: SCI is output when the command set is not executed and OBF=0. SCI_EVT shows the output SCI is for event notification. =0: Runtime event status is reflected to RUN_EVT_STS register. =1: Runtime event status is reflected to Query data. =0: Wake event output is always enable.(in S0-S3) =1: Wake event output is enable when SUS_X=L. =0: Runtime and Wakeup is selected by SUS_B. (GPIO B6 is enable) =1: Runtime and Wakeup is selected by SUS_A. (GPIO B6 is used as SUS_A input.)
	C3h	EC_RUN_ ENB_2	R/W	Reserved [7:1]							TH	0: Disable 1: Enable	0x00	TH: Thermal event	
	C4h	EC_WAKE_ ENB_2	R/W									0: Disable 1: Enable	0x00		
	C5h To C7h	Reserved	R/W	Don't care								-	-		
	C8h *6	GPI_AD0	R	AD0_DATA [7:0]								-	-	For detail information, refer to GPIO section in this document.	
	C9h *6	GPI_AD1	R	AD1_DATA [7:0]								-	-		
	Cah *6	Reserved	R/W	Don't care								-	-		
	CBh	D/A_CONT	R/W	DATA [7:0]								-	0xff	0x00-0xfe: D/A converter output data 0xff : Battery capacity(%) output	
	CCh	WAKE_DIS	R/W	DATA [7:0]								-	0x00	0x00 : WAKE# output enable 0x01 : WAKE# output disable	

*4: Should be 0.
*6: This register's response time is 150usec max.

Function	Address	Register Name	R/W	Bit Number 7	6	5	4	3	2	1	0	Logic	Default	Description
Battery control	D0h	BAT_CHG_CONT	R/W	RES[7:5]			CHG_RDY#	RES[3:2]		CHG2	CHG1	-	-	CHG_RDY# =0 : Charge ready CHGn =1 : The nth battery is charged
	D1h	BAT_DCH_PRI	R/W	RES[7:3]					PAT [2:0]			-	0x00	Battery discharge priority 0 : 2 1 1 : 1 2 2 : 2 1 3 : 2 1 4 : 1 2 5 : 1 2 6 : Same as 0 7 : Simultaneously discharge (Read only :This data can be set using PMU register)
	D2h	BAT_DCH_CONT	R/W	RES[7:2]						DCHG2	DCHG1	0: Not discharge 1: Discharge	-	The discharge battery can be selected one of the batteries can be discharged.
	D3h	BAT_WAR_ABS	R/W	DATA[15:0] *1								-	0x0000	Absolute capacity battery Warning detection point 0x0000-0xffff (mWh)
	D5h	BAT_LOW_ABS	R/W	DATA[15:0] *1								-	0x0000	Absolute capacity battery Low detection point 0x0000-0xffff (mWh)
	D7h	BAT_WAR_REL	R/W	DATA [7:0]								-	0x10	Relative capacity battery Warning detection point 00-C8h (0-100% step 0.5%)
	D8h	BAT_LOW_REL	R/W	DATA [7:0]								-	0x06	Relative capacity battery Low detection point 00-C8h (0-100% step 0.5%)
	D9h *3	FULL_DATA	R/W	DATA [7:0]								-	0xbe	Full charge cancel point 00-C8h (0-100% step 0.5%)
	Dah	CC_CUR_DATA	R	DATA [7:0]								-	0x00	Battery charging current setting 0x01-0xff (0.02-5.10A step 0.02A) 0x00 Depends on the battery This register is “ read only” , to change the value, use the register in PMU registers area.
	DBh To DCh	BTP2	R/W	DATA [15:0]								-	0x0000	0x0000: Clear the trip point 0x0001-0xffff : (mWh) When all of the battery’ s capacities lesser than this setting value, the BTP2 is detected if event is enabled.
	DDh To DFh	Reserved	R/W	Don't care								-	-	

*3: This register is not cleared if the system is in S4-S5 state.

R(/W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

Function	Address	Register Name	R/W	Bit Number 7	6	5	4	3	2	1	0	Logic	Default	Description
PMU control	E0h	PMU_CONT	R/W	RES[7:3]					EC_REG	BAY_LED	POW_LED	-	0x00	EC_REG =1: PMU does not initialize EC register when system power is off. BAY_LED =1: PMU indicates the Battery discharge status to the LED_BAY#n, POW_LED =1: when the battery is installed. The Power LED blink
	E1h	ACPI_ACC_ENB	R/W	RES [7:1]							OS_STS	-	0x00	OS_STS = 1: ACPI mode = 0: Legacy mode
	E2h	OFF_TIME	R/W	DATA [7:0]								-	0x64	Power switch over ride function timer 01h-FFh (0.1-25.5esc step 0.1sec) 00h : Reserved
Thermal Sensor Polling	E3h	POLLING_ADDRESS	R/W	Slave Address [6:0]							RES		0x00	Address: 0x00-0x7F The polling slave address setting If this address is 00, the Polling is disabled.
	E4h	HIGH_ALARM	R/W	DATA [7:0]								Signed value	0x00	If the received data GE this value, the event will be detected.
	E5h	LOW_ALARM	R/W	DATA [7:0]								Signed value	0x00	If the received data LE this value, the event will be detected.
	E6h	POLLING_INTERVAL	R/W	DATA [7:0]									0x00	0x00 :Polling disable 0x01 – 0xFF [x 250ms] (250ms to 63.75sec)
	E7h	POLLING_DATA	R(/W)	DATA [7:0]								Signed value	0x00	This register shows data at latest polling.
	E8h	HARDWARE_SHUT_DOWN	R/W	DATA [7:0]								Signed value	0x7D	If the thermal sensor read value GE this value, the PMU automatically off the power.
	E9h	POLLING_COMMAND	R/W	DATA [7:0]									0x00	Polling command (data register) address.
	EAh	RETRY_COUNT	R/W	DATA [7:0]									0x10	0x00 - 0xFF: Retry count value (0-255)
	Ebh To EFh	Reserved	R/W	Don't care										
PMU control	F0h	BURST_FLG_CLR	R/W	DATA [7:0]								-	-	After writing to the register addressed A8h-AFh, Set the 00h to this register.
	F1h To FFh	Reserved	R/W	Don't care										

R(/W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

3.8 Miscellaneous

3.8.1 Security

The user may enter up to eight standard text characters for a password. The password includes two levels. The higher priority is the Supervisor Password. The lower priority is the User Password. The Supervisor Password can access all the system resource, while the User Password may not access the floppy disk when it is protected by Supervisor Password. Also, the User Password may not access the floppy disk when the Supervisor Password protects it.

When the security function is enabled, the system will request the user to enter password during the following situation:

- Power On → The system will prompt the user to enter the password before booting the OS. If the user key in the wrong password for 3 times, then the system will halt.

- Resume → The system will prompt the user to enter password while resuming from STR or STD mode. If the user keys in the wrong password for 3 times, the system will not resume and should return to Suspend mode.

- Entering CMOS Setup → The system will prompt the user to enter the password before entering the CMOS Setup. If the user keys in the wrong password for 3 times, then the system will halt.

3.9 CMOS Setup Utility

The Setup utility is used to configure the system. The Setup contains the information regarding the hardware for boot purpose. The changed settings will take effect after the system rebooted. Refer to Chapter 1 on running BIOS Setup Program for more detailed information.