TUCANA Block Diagram

PROJECT CODE : 91.4KK01.001
PCB P/N : 48.4KK01.0SB
REVISION : S0201-SB

Clock Generator
ICS9LVS3197BKLFT 3

Thermal Sensor
GMT G787 37

DDRIII 800 Slot 0 21 — DDRIII Channel A
DDRIII 800 Slot 1 22 — DDRIII Channel B

Intel CPU
SFF
4,5,..,10,11

FDIx8 / DMIx4

INTEL
PCH
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
6 SATA ports
8 PCIE ports
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
12,13,...,19,20

Int MIC
Line Out
MIC In
SPKR 1.5W
Codec Realtek ALC269 31~33 — AZALIA

LVDS — LCD 23
RGB — CRT 24
PCIe — HDMI 25

USB
9 — CAMERA 23
0,1,4 — USB Port x 3 28
12 — Blue Tooth 27
2 — Cardreader Realtek RTS5186 34 — MS Pro Duo /SD(SDHC) 34
8 — Mini 1 Card WLAN/ WIMAX 35

PCIe
1 — Giga LAN Atheros AR8131M 29 — TXFM 30 — RJ45 30

HDD 26 — 0 — SATA
Flash ROM 4MB 39 — SPI

LPC
KBC Winbond NPCE781L 38 — SPI — Flash ROM 128KB 39
LPC DEBUG CONN. 39
Touch Pad 40
INT. KB 38

PCB STACKUP

TOP		L1
VCC		L2
S		L3
S		L4
GND		L5
BOTTOM		L6

SMbus ADDRESS

DIMM 1	1010 000x b
DIMM 2	1010 001x b
CLK GEN	1110 001x b
Thermal Sensor	0101 110x b
CHARGER	0001 001x b
BATTERY	0001 110x b

SYSTEM DC/DC RT8223 47

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5

RT8209 49

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(20A)

RT8209 48

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(9.4A)

RT9026 51

INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 1.2A

CHARGER BQ24751 52

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ADP3211 46

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 27A

GFX Core ADP3211 50

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 11A

DVT 1ST

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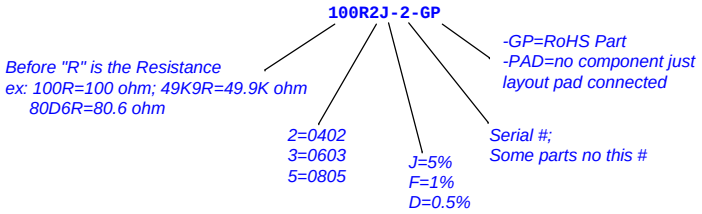
PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

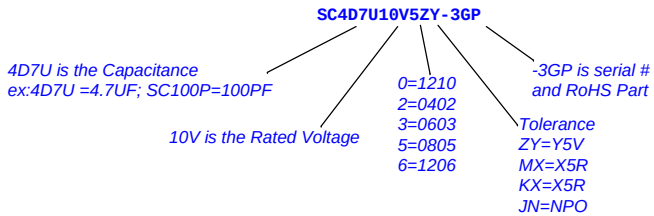
Processor Strapping

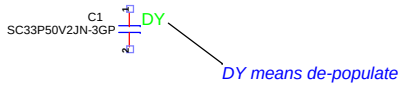
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

Resistor



Capacitor





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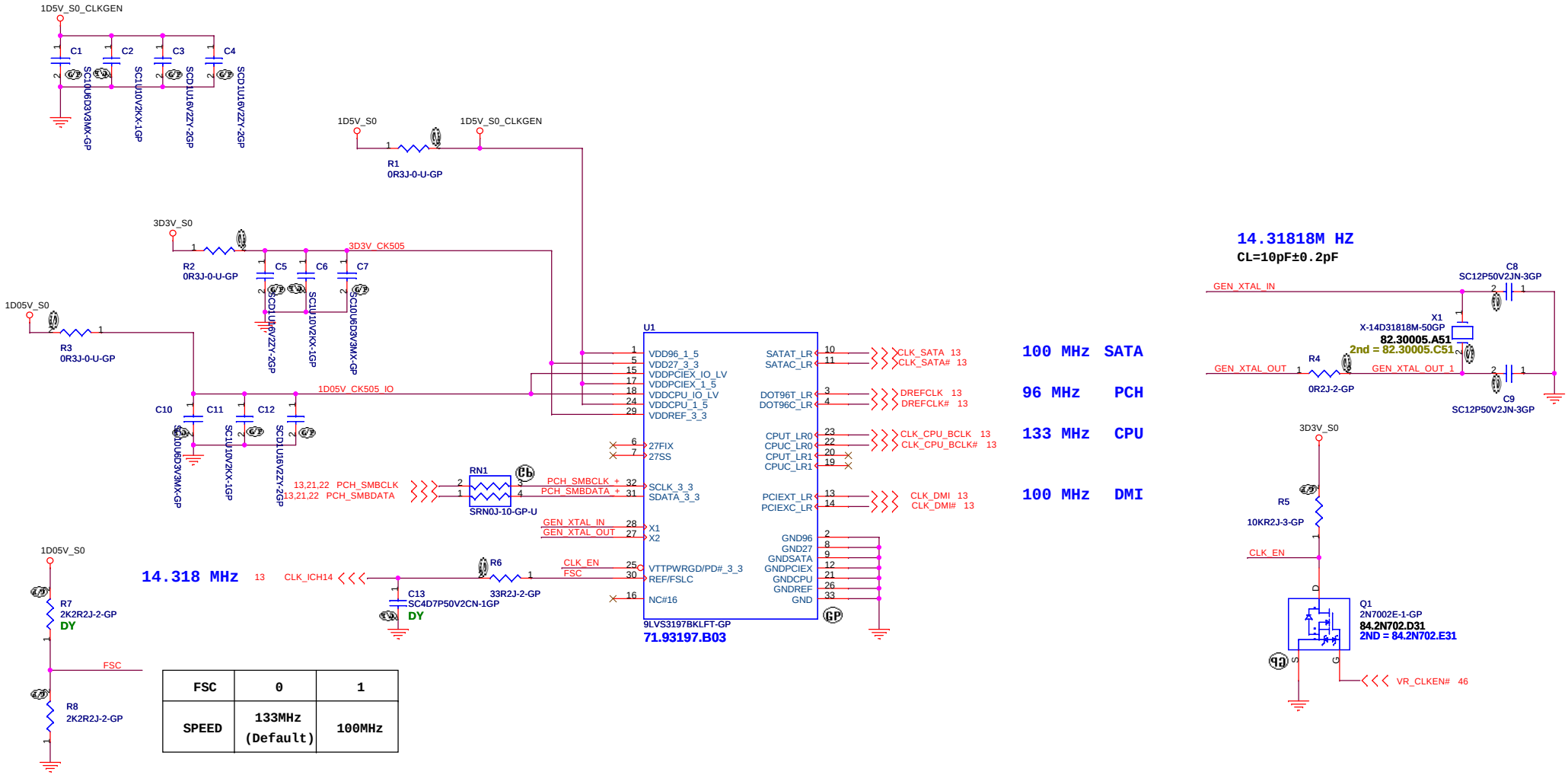
Title: Reference	
Size: A3	Document Number: TUCANA — Rev: SB
Date: Wednesday, July 07, 2010	Sheet 2 of 56



FSC	0	1
SPEED	133MHz (Default)	100MHz

<Core Design>

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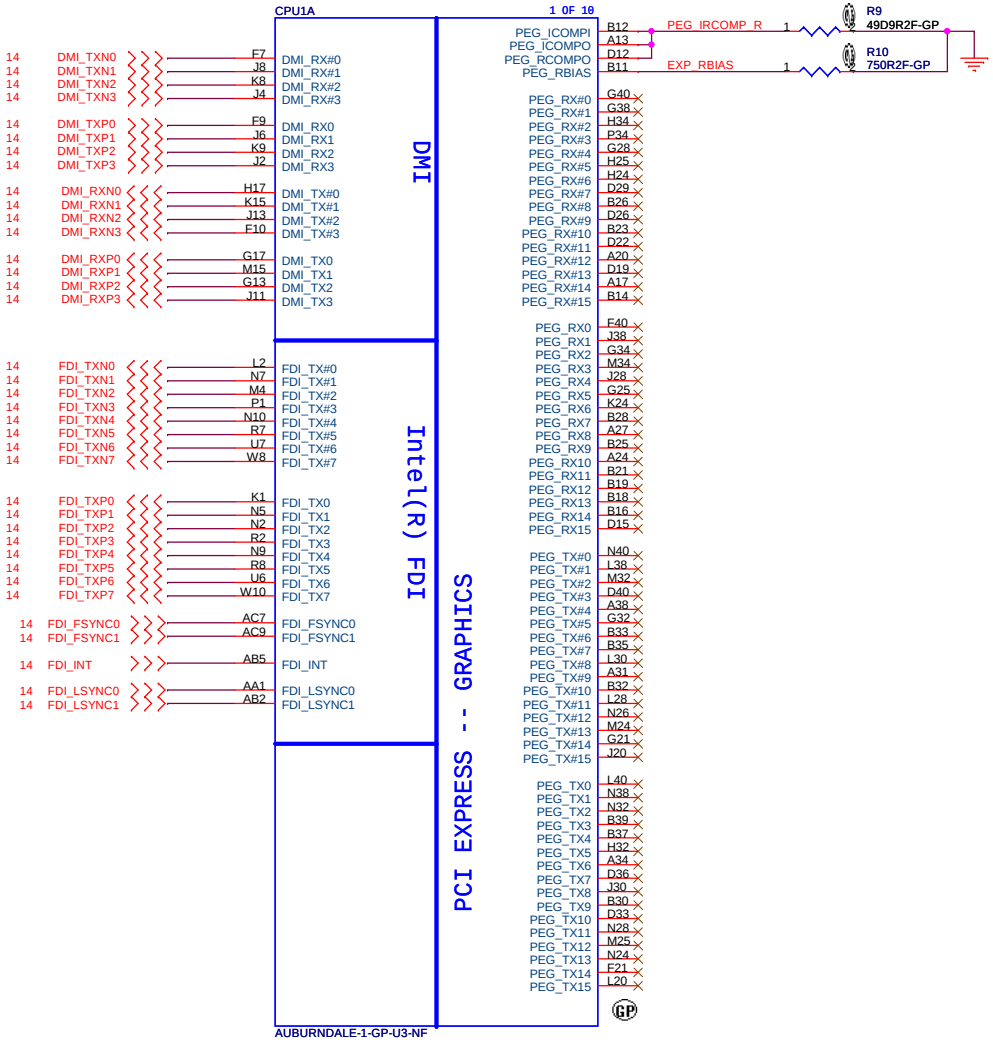
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator

Size	Document Number	Rev
A3	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 3 of 56



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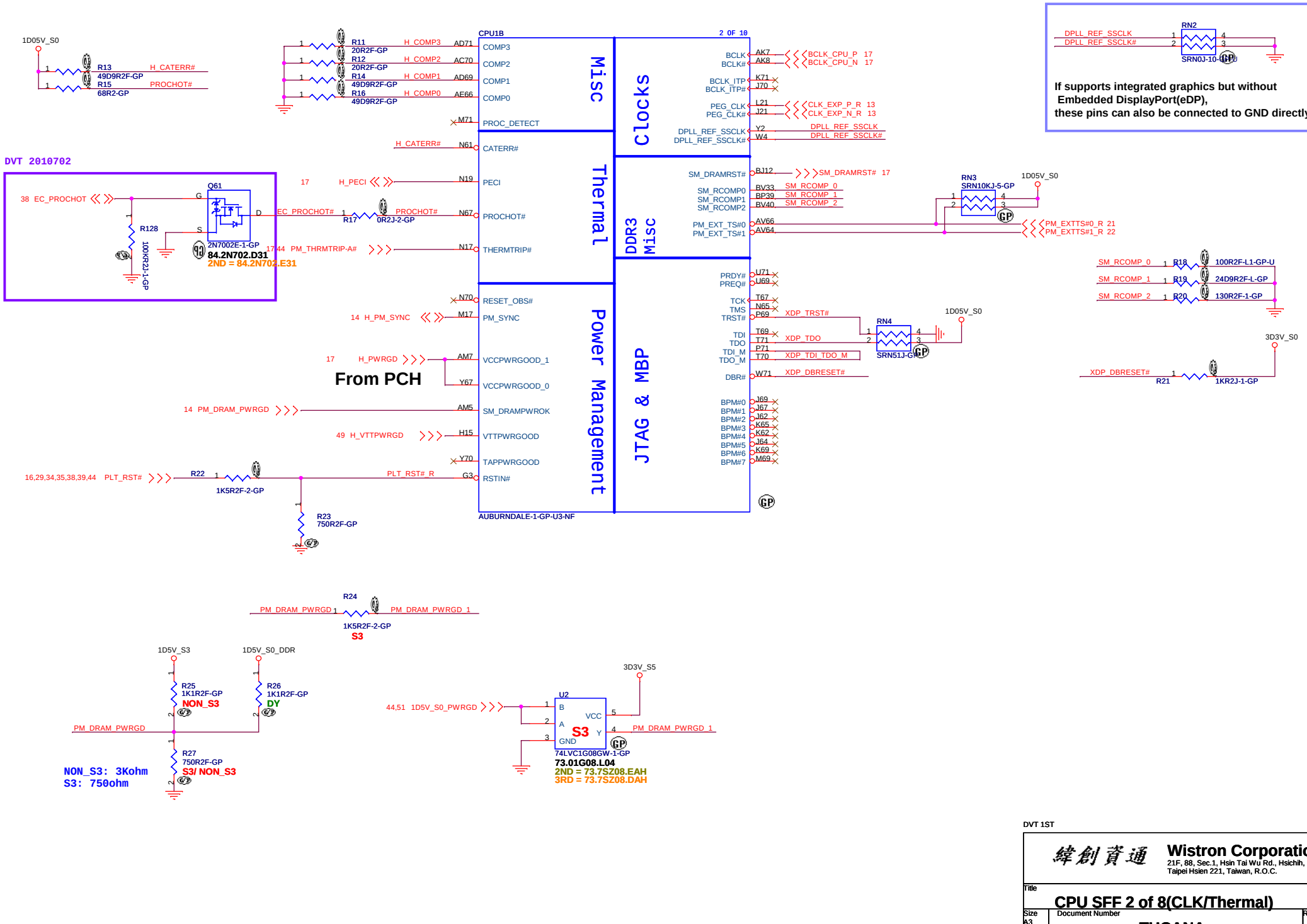
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU SFF 1 of 8(DMI/FDI/PEG)**

Size	Document Number	Rev
A3	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 4 of 56



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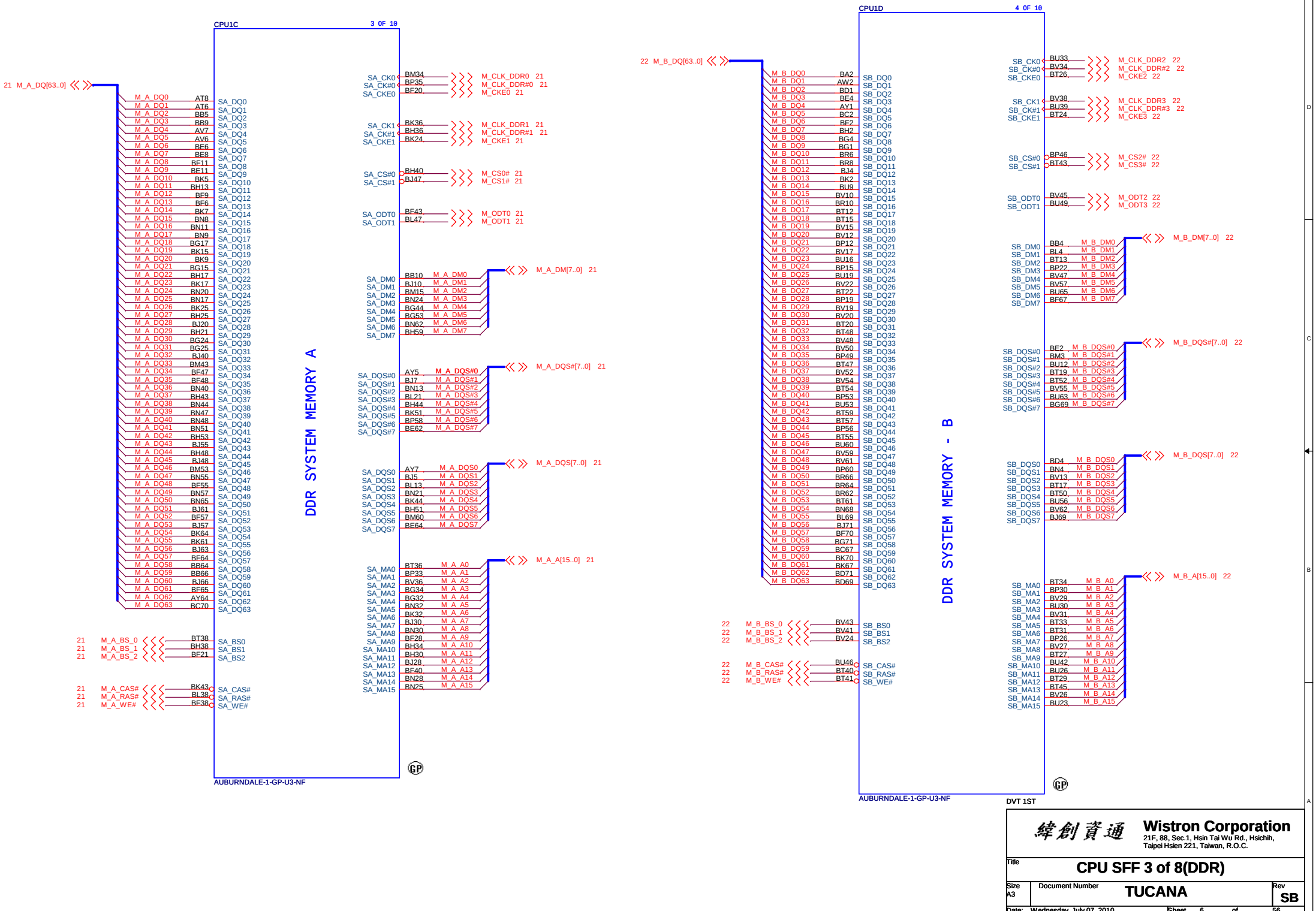
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU SFF 2 of 8(CLK/Thermal)

Size: A3 | Document Number: TUCANA | Rev: SB

Date: Wednesday, July 07, 2010 | Sheet 5 of 56


CPU1C
3 OF 10
DDR SYSTEM MEMORY A
AUBURNDALE-1-GP-U3-NF
21 M_A_DQ[63..0]
M_A_DQ0 AT8 SA_DQ0
M_A_DQ1 AT6 SA_DQ1
M_A_DQ2 BB5 SA_DQ2
M_A_DQ3 BB9 SA_DQ3
M_A_DQ4 AV7 SA_DQ4
M_A_DQ5 AV6 SA_DQ5
M_A_DQ6 BE6 SA_DQ6
M_A_DQ7 BE8 SA_DQ7
M_A_DQ8 BF11 SA_DQ8
M_A_DQ9 BE11 SA_DQ9
M_A_DQ10 BK5 SA_DQ10
M_A_DQ11 BH13 SA_DQ11
M_A_DQ12 BF9 SA_DQ12
M_A_DQ13 BF6 SA_DQ13
M_A_DQ14 BK7 SA_DQ14
M_A_DQ15 BN8 SA_DQ15
M_A_DQ16 BN11 SA_DQ16
M_A_DQ17 BN9 SA_DQ17
M_A_DQ18 BG17 SA_DQ18
M_A_DQ19 BK15 SA_DQ19
M_A_DQ20 BK9 SA_DQ20
M_A_DQ21 BG15 SA_DQ21
M_A_DQ22 BH17 SA_DQ22
M_A_DQ23 BK17 SA_DQ23
M_A_DQ24 BN20 SA_DQ24
M_A_DQ25 BN17 SA_DQ25
M_A_DQ26 BK25 SA_DQ26
M_A_DQ27 BH25 SA_DQ27
M_A_DQ28 BJ20 SA_DQ28
M_A_DQ29 BH21 SA_DQ29
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M_A_DQ62 AY64 SA_DQ62
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21 M_A_BS_0 BT38 SA_BS0
21 M_A_BS_1 BH38 SA_BS1
21 M_A_BS_2 BF21 SA_BS2
21 M_A_CAS# BK43 SA_CAS#
21 M_A_RAS# BL38 SA_RAS#
21 M_A_WE# BF38 SA_WE#
SA_CK0 BM34 M_CLK_DDR0 21
SA_CK#0 BP35 M_CLK_DDR#0 21
SA_CKE0 BF20 M_CKE0 21
SA_CK1 BK36 M_CLK_DDR1 21
SA_CK#1 BH36 M_CLK_DDR#1 21
SA_CKE1 BK24 M_CKE1 21
SA_CS#0 BH40 M_CS0# 21
SA_CS#1 BJ47 M_CS1# 21
SA_ODT0 BF43 M_ODT0 21
SA_ODT1 BL47 M_ODT1 21
SA_DM0 BB10 M_A_DM0
SA_DM1 BJ10 M_A_DM1
SA_DM2 BM15 M_A_DM2
SA_DM3 BN24 M_A_DM3
SA_DM4 BG44 M_A_DM4
SA_DM5 BG53 M_A_DM5
SA_DM6 BN62 M_A_DM6
SA_DM7 BH59 M_A_DM7
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SA_MA8 BN30 M_A_A8
SA_MA9 BF28 M_A_A9
SA_MA10 BH34 M_A_A10
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SA_MA12 BJ28 M_A_A12
SA_MA13 BF40 M_A_A13
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SA_MA15 BN25 M_A_A15
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CPU1D
4 OF 10
DDR SYSTEM MEMORY - B
AUBURNDALE-1-GP-U3-NF
22 M_B_DQ[63..0]
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M_B_DQ1 AW2 SB_DQ1
M_B_DQ2 BD1 SB_DQ2
M_B_DQ3 BE4 SB_DQ3
M_B_DQ4 AY1 SB_DQ4
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M_B_DQ6 BF2 SB_DQ6
M_B_DQ7 BH2 SB_DQ7
M_B_DQ8 BG4 SB_DQ8
M_B_DQ9 BG1 SB_DQ9
M_B_DQ10 BR6 SB_DQ10
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SB_CK#0 BV34 M_CLK_DDR#2 22
SB_CKE0 BT26 M_CKE2 22
SB_CK1 BV38 M_CLK_DDR3 22
SB_CK#1 BU39 M_CLK_DDR#3 22
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SB_CS#1 BT43 M_CS3# 22
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SB_ODT1 BU49 M_ODT3 22
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SB_DQS3 BT17 M_B_DQS3
SB_DQS4 BT50 M_B_DQS4
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SB_MA2 BV29 M_B_A2
SB_MA3 BU30 M_B_A3
SB_MA4 BV31 M_B_A4
SB_MA5 BT33 M_B_A5
SB_MA6 BT31 M_B_A6
SB_MA7 BP26 M_B_A7
SB_MA8 BV27 M_B_A8
SB_MA9 BT27 M_B_A9
SB_MA10 BU42 M_B_A10
SB_MA11 BU26 M_B_A11
SB_MA12 BT29 M_B_A12
SB_MA13 BT45 M_B_A13
SB_MA14 BV26 M_B_A14
SB_MA15 BU23 M_B_A15
M_B_A[15..0] 22
DVT 1ST
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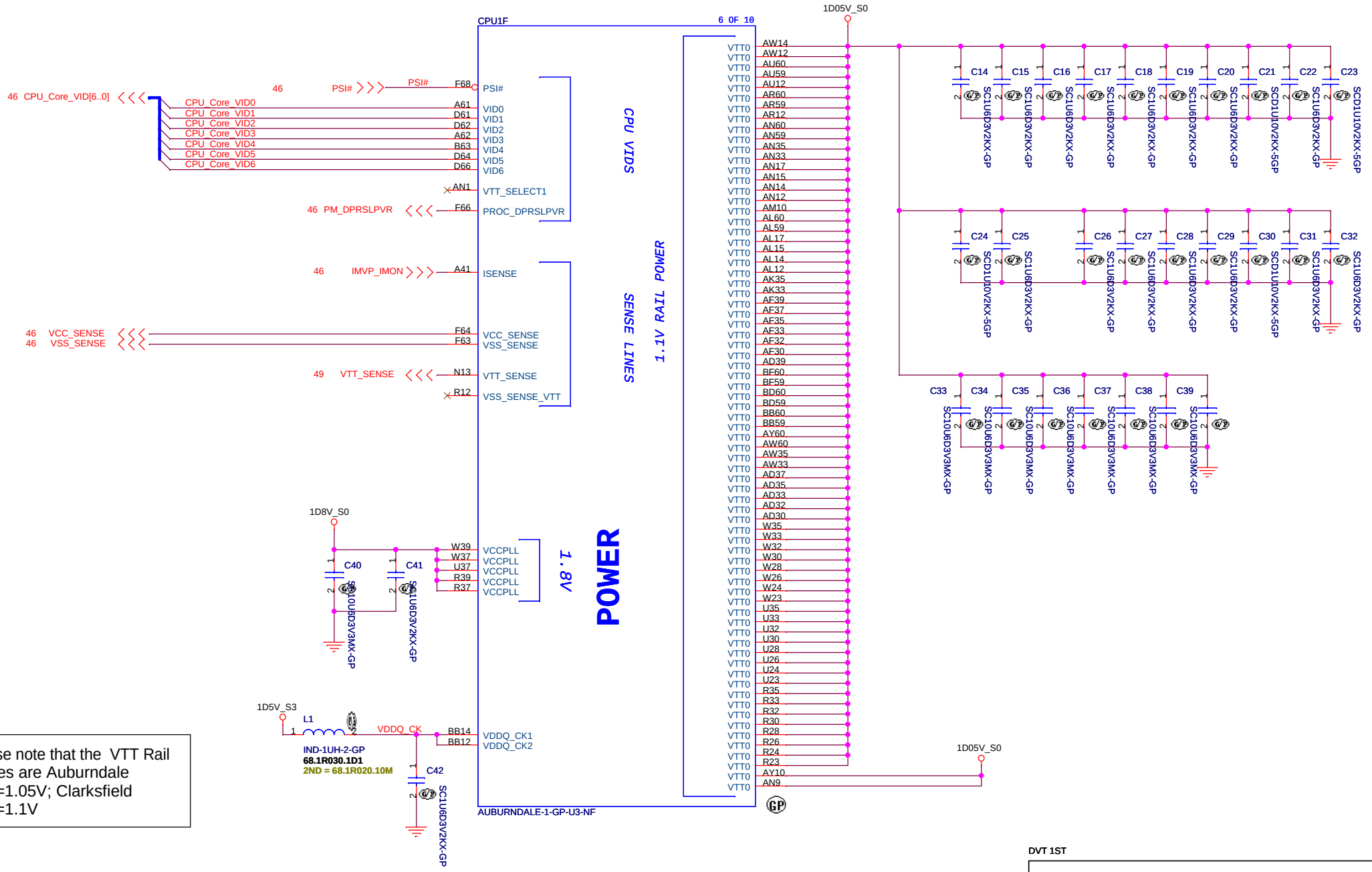
Title
CPU SFF 3 of 8(DDR)
Size A3
Document Number
TUCANA
Rev SB
Date: Wednesday, July 07, 2010
Sheet 6 of 56



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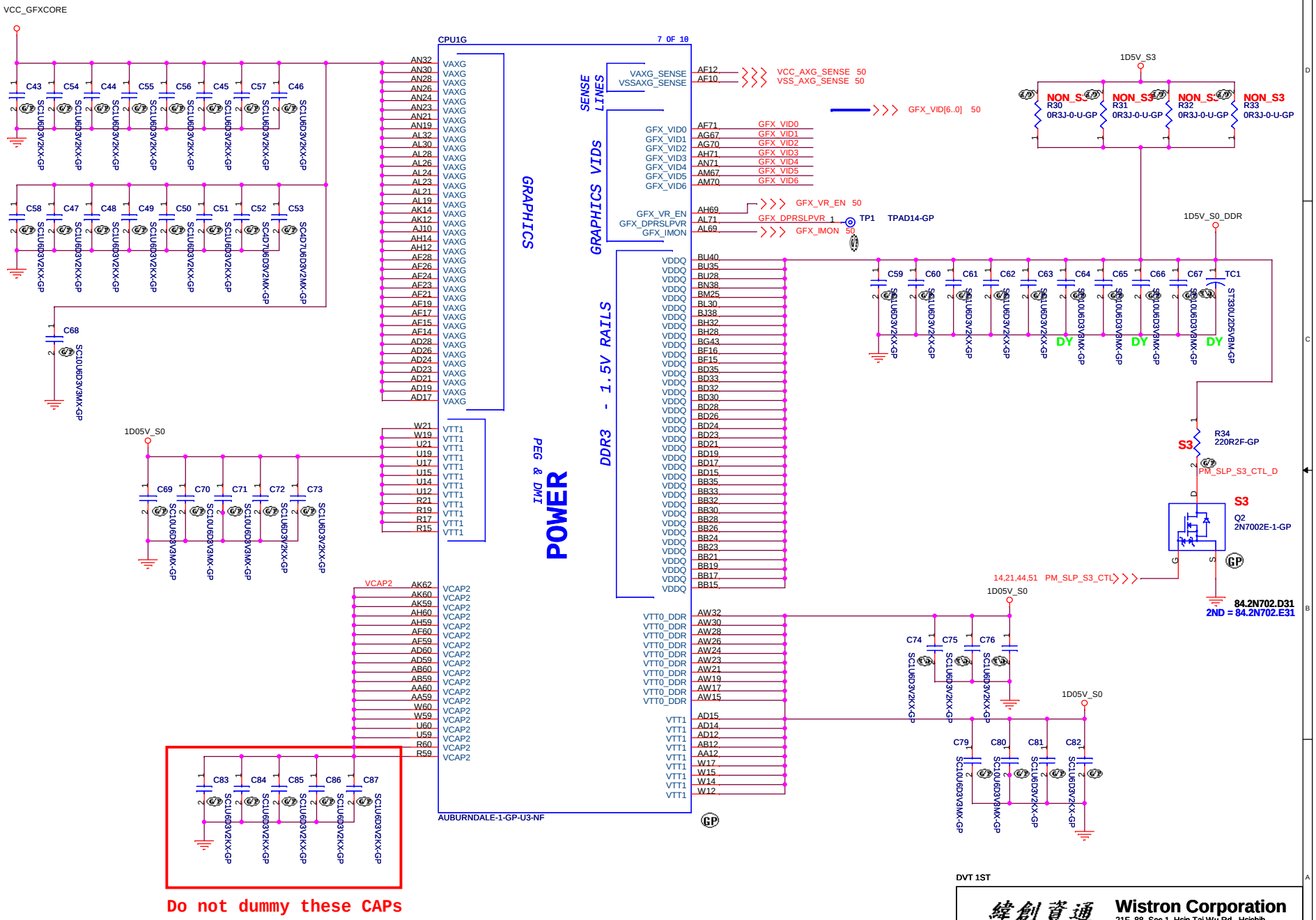
Title	CPU SFF 4 of 8(POWER/VTT)	
Size: Custom	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 7 of 56	


VCC_GFXCORE
CPU1G
7 OF 10
GRAPHICS
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
PEG & DMI
POWER
VAXG_SENSE
VSSAXG_SENSE
VCC_AXG_SENSE 50
VSS_AXG_SENSE 50
GFX_VID[6..0] 50
GFX_VR_EN 50
GFX_IMON 50
GFX_DPRSLPVR
TP1 TPAD14-GP
1D5V_S3
1D5V_S0_DDR
1D05V_S0
NON_S3
R30 0R3J-0-U-GP
R31 0R3J-0-U-GP
R32 0R3J-0-U-GP
R33 0R3J-0-U-GP
R34 220R2F-GP
PM_SLP_S3_CTL_D
14,21,44,51 PM_SLP_S3_CTL
Q2 2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
AUBURNDALE-1-GP-U3-NF
Do not dummy these CAPs
DVT 1ST
Wistron Corporation
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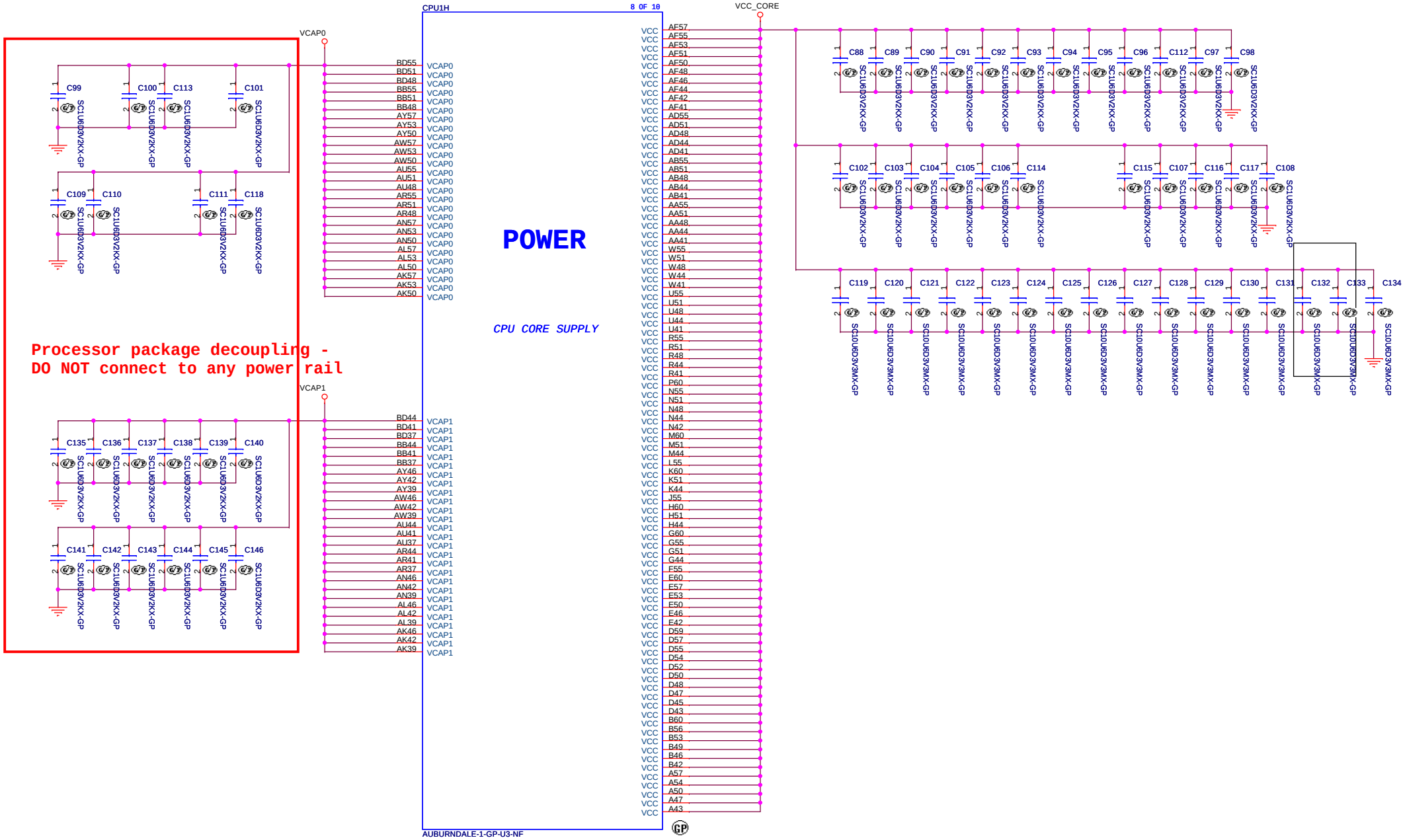
Taipei Hsien 221, Taiwan, R.O.C.
CPU SFF 5 of 8(PWR/DDR/GFX/)
TUCANA
SB
Wednesday, July 07, 2010
8
56



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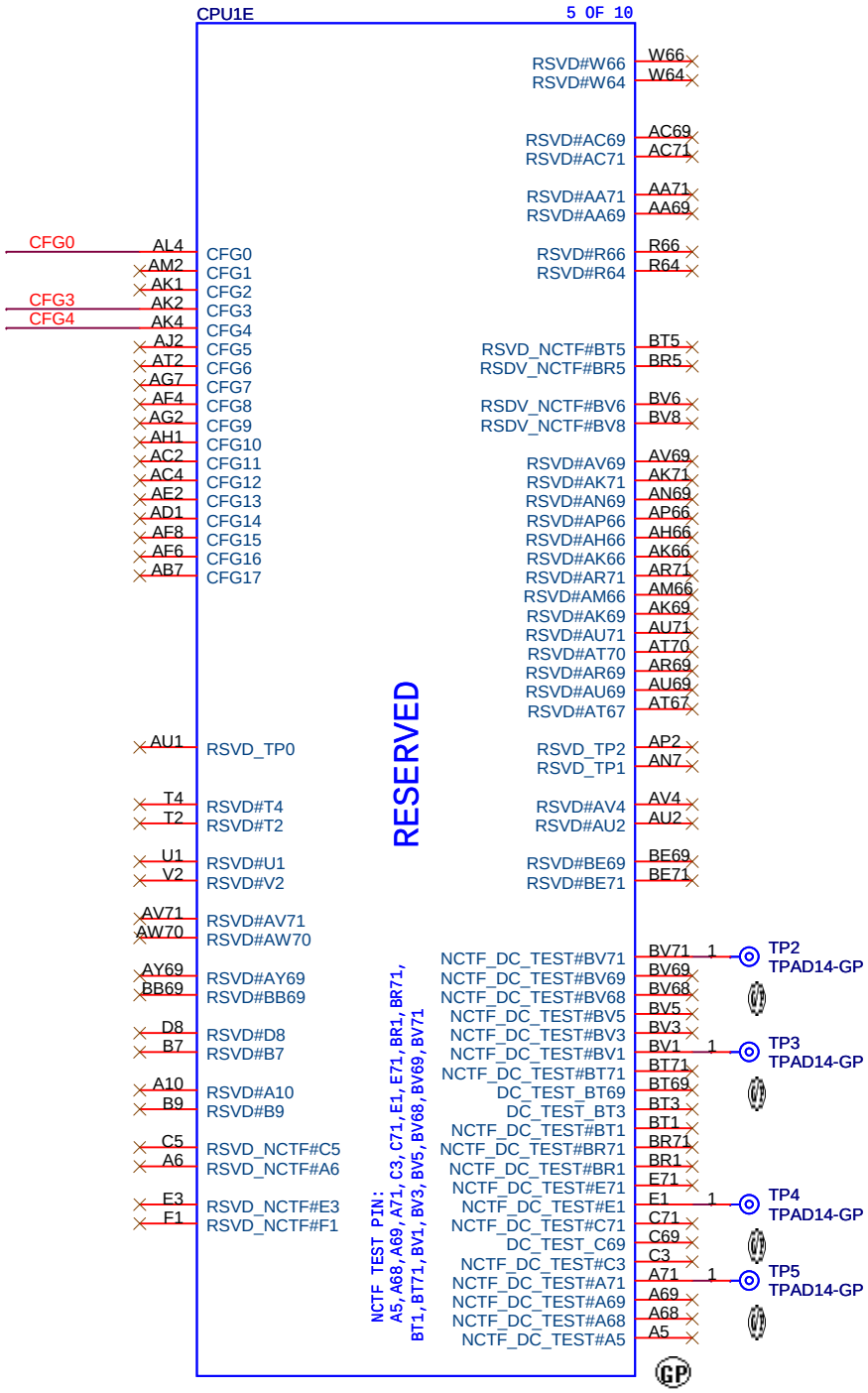
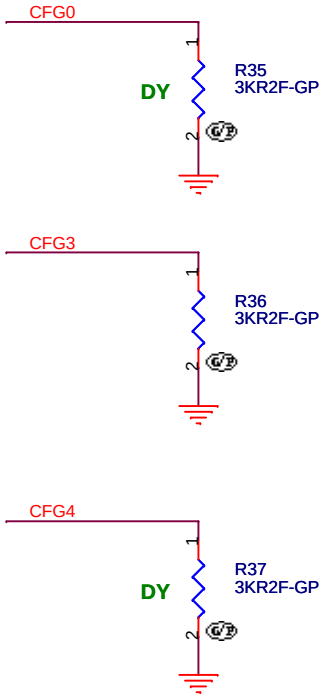
Title	CPU SFF 6 of 8(CPUCORE)	
Size A3	Document Number TUCANA	Rev SB
Date: Wednesday, July 07, 2010	Sheet 9 of 56	





PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

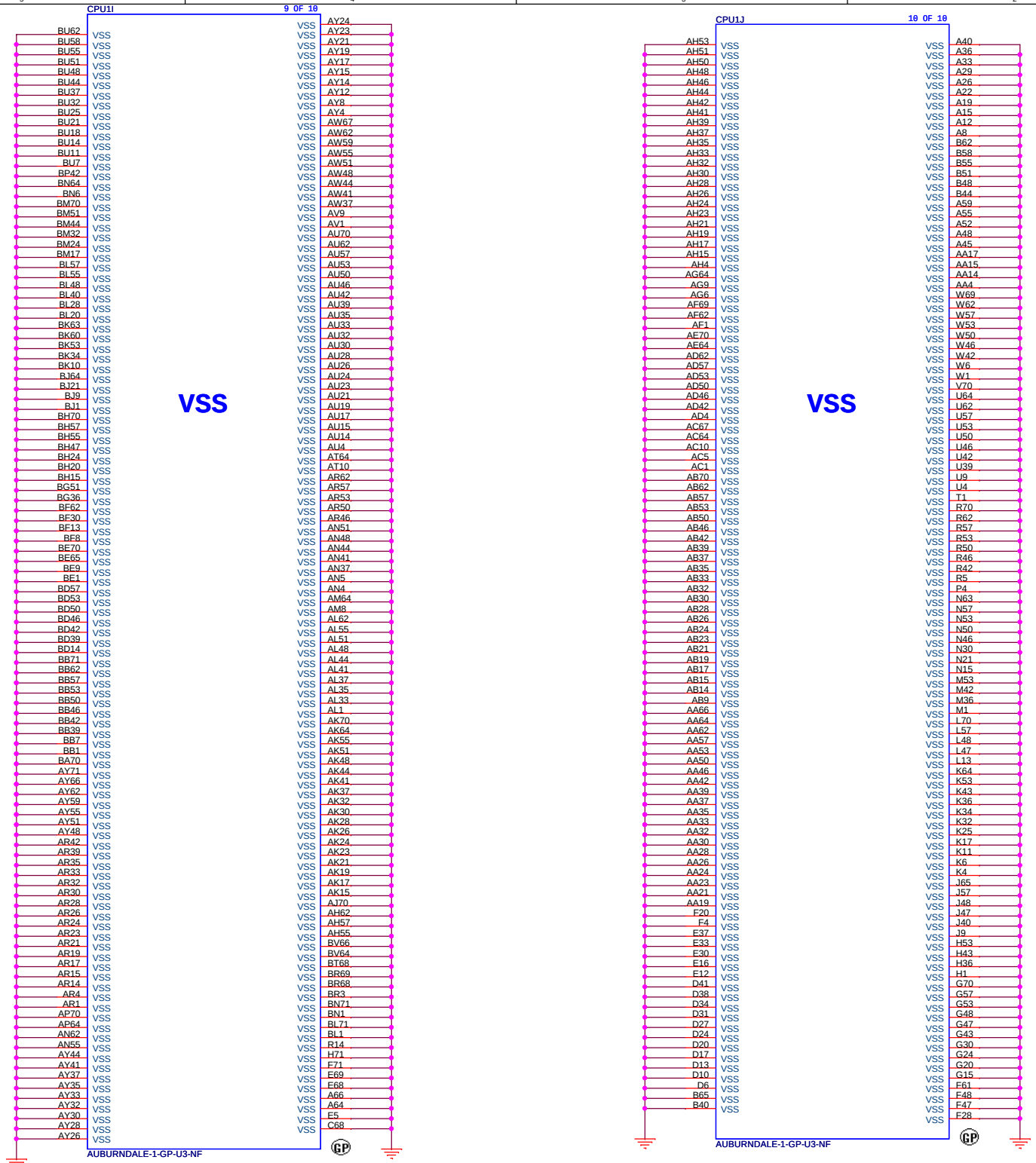
DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU SFF 7 of 8(RESERVED)**

Size	Document Number	Rev
A4	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 10 of 56

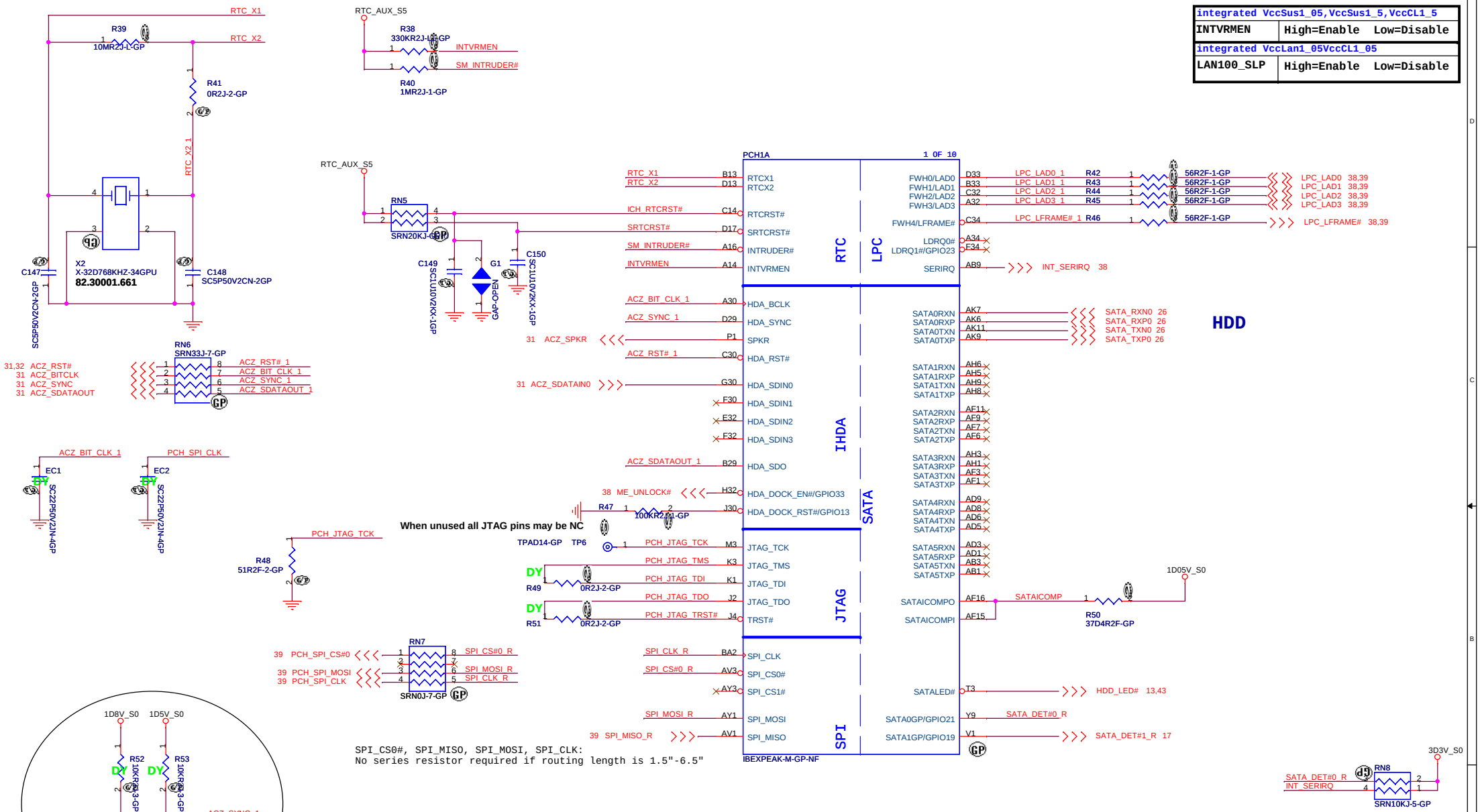


DVT 1ST

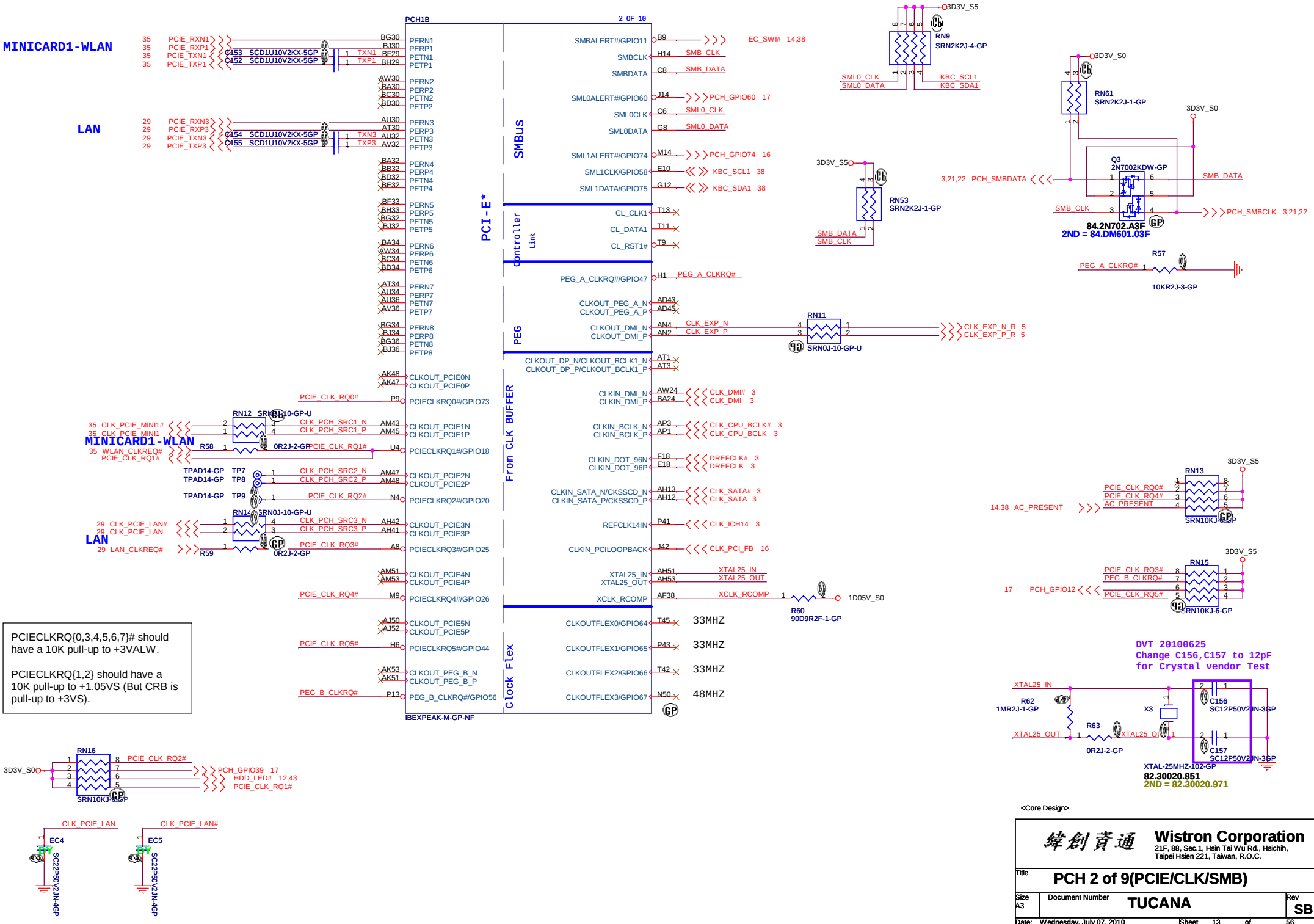
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

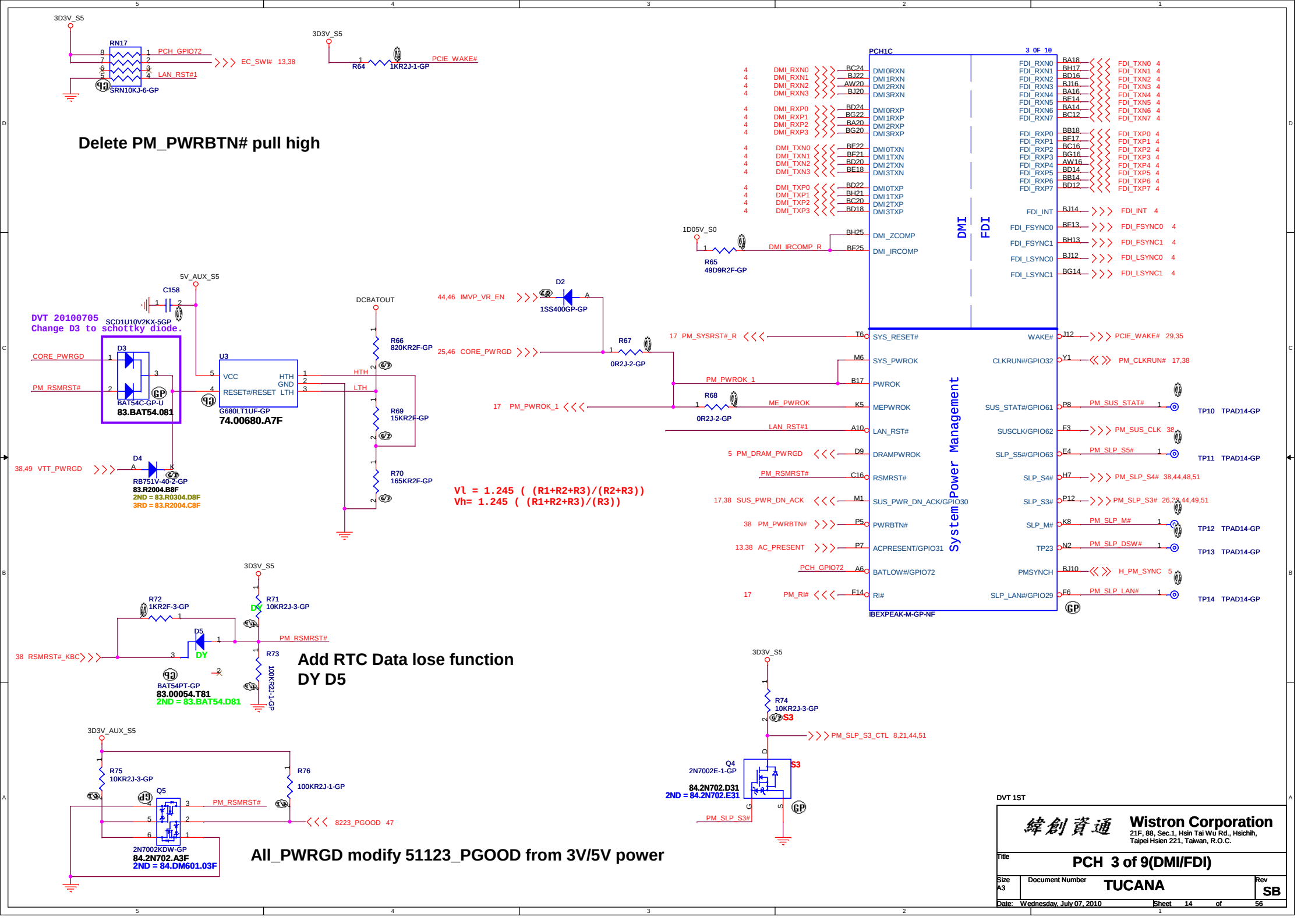
Title	CPU SFF 8 of 8(VSS)	
Size A3	Document Number TUCANA	Rev SB
Date: Wednesday, July 07, 2010	Sheet 11 of 56	

integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

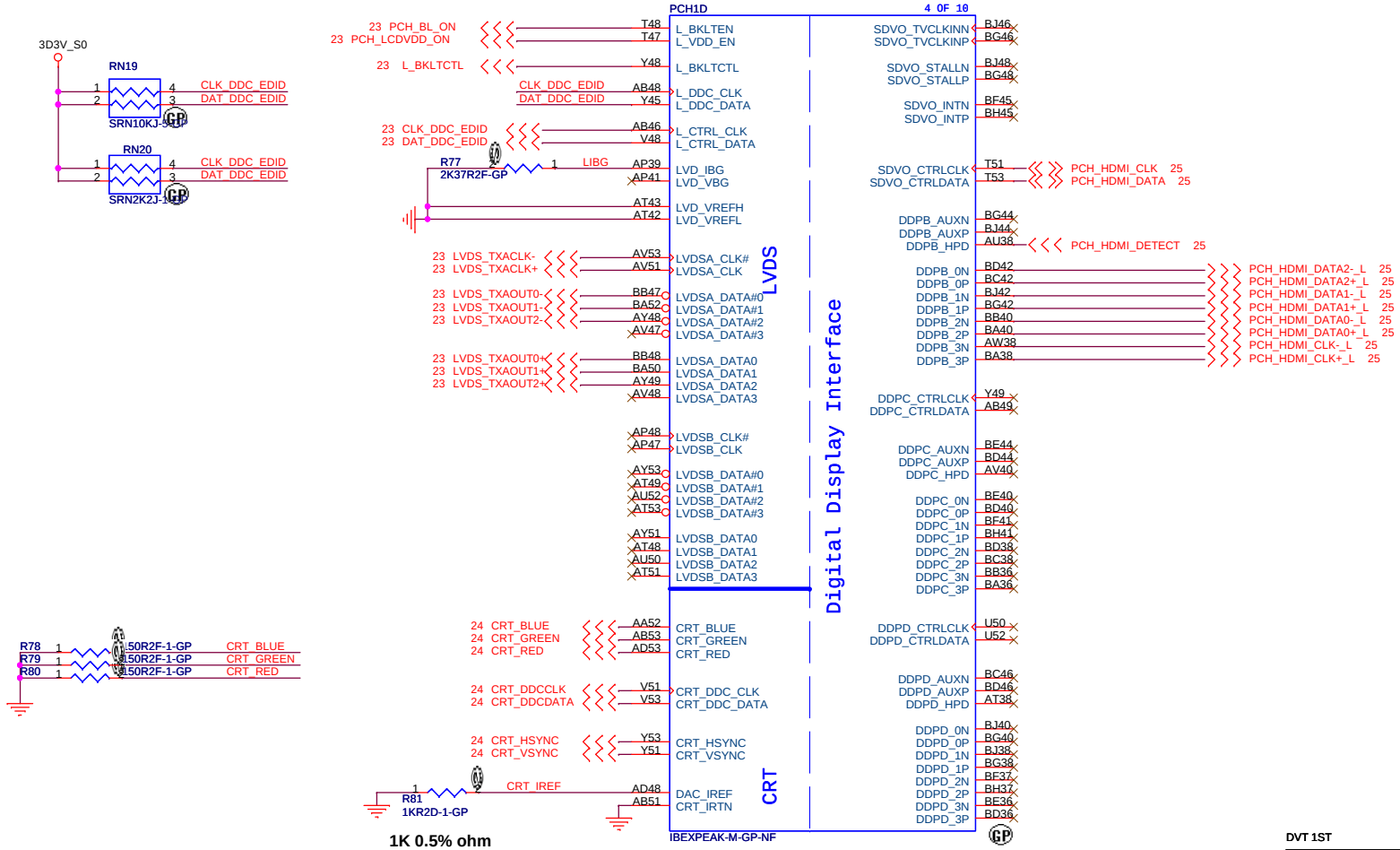


DVT 1ST	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PCH 1 of 9(SATA/RTC/HDA)
Size A3	Document Number TUCANA Rev SB
Date: Wednesday, July 07, 2010	Sheet 12 of 56


MINICARD1-WLAN
LAN
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
DVT 20100625
Change C156,C157 to 12pF
for Crystal vendor Test
84.2N702.A3F
2ND = 84.DM601.03F
82.30020.851
2ND = 82.30020.971
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH 2 of 9(PCIE/CLK/SMB)
Size A3
Document Number
TUCANA
Rev SB
Date: Wednesday, July 07, 2010
Sheet 13 of 56


3D3V_S5
RN17
PCH_GPIO72
EC_SW# 13,38
LAN_RST#1
SRN10KJ-6-GP
3D3V_S5
R64
1KR2J-1-GP
PCIE_WAKE#
Delete PM_PWRBTN# pull high
PCH1C
3 OF 10
DMI0RXN
DMI1RXN
DMI2RXN
DMI3RXN
DMI0RXP
DMI1RXP
DMI2RXP
DMI3RXP
DMI0TXN
DMI1TXN
DMI2TXN
DMI3TXN
DMI0TXP
DMI1TXP
DMI2TXP
DMI3TXP
DMI_ZCOMP
DMI_IRCOMP
DMI
FDI
FDI_RXN0
FDI_RXN1
FDI_RXN2
FDI_RXN3
FDI_RXN4
FDI_RXN5
FDI_RXN6
FDI_RXN7
FDI_RXP0
FDI_RXP1
FDI_RXP2
FDI_RXP3
FDI_RXP4
FDI_RXP5
FDI_RXP6
FDI_RXP7
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1
1D05V_S0
R65
49D9R2F-GP
DMI_IRCOMP_R
5V_AUX_S5
C158
SCD1U10V2KX-5GP
DVT 20100705
Change D3 to schottky diode.
D3
CORE_PWRGD
PM_RSMRST#
BAT54C-GP-U
83.BAT54.081
U3
VCC
RESET#/RESET
HTH
GND
LTH
G680LT1UF-GP
74.00680.A7F
DCBATOUT
R66
820KR2F-GP
R69
15KR2F-GP
R70
165KR2F-GP
HTH
LTH
D4
38,49 VTT_PWRGD
RB751V-40-2-GP
83.R2004.B8F
2ND = 83.R0304.D8F
3RD = 83.R2004.C8F
D2
44,46 IMVP_VR_EN
1SS400GP-GP
R67
0R2J-2-GP
25,46 CORE_PWRGD
R68
0R2J-2-GP
ME_PWROK
17 PM_SYSRST#_R
17 PM_PWROK_1
PM_PWROK_1
LAN_RST#1
5 PM_DRAM_PWRGD
PM_RSMRST#
17,38 SUS_PWR_DN_ACK
38 PM_PWRBTN#
13,38 AC_PRESENT
PCH_GPIO72
17 PM_RI#
SYS_RESET#
SYS_PWROK
PWROK
MEPWROK
LAN_RST#
DRAMPWROK
RSMRST#
SUS_PWR_DN_ACK/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
RI#
IBEXPEAK-M-GP-NF
System Power Management
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_M#
TP23
PMSYNCH
SLP_LAN#/GPIO29
PCIE_WAKE# 29,35
PM_CLKRUN# 17,38
PM_SUS_STAT#
PM_SUS_CLK 38
PM_SLP_S5#
PM_SLP_S4# 38,44,48,51
PM_SLP_S3# 26,38,44,49,51
PM_SLP_M#
PM_SLP_DSW#
H_PM_SYNC 5
PM_SLP_LAN#
TP10 TPAD14-GP
TP11 TPAD14-GP
TP12 TPAD14-GP
TP13 TPAD14-GP
TP14 TPAD14-GP
Vl = 1.245 ((R1+R2+R3)/(R2+R3))
Vh= 1.245 ((R1+R2+R3)/(R3))
3D3V_S5
R72
1KR2F-3-GP
R71
10KR2J-3-GP
DY
D5
38 RSMRST#_KBC
PM_RSMRST#
R73
100KR2J-1-GP
BAT54PT-GP
83.00054.T81
2ND = 83.BAT54.D81
Add RTC Data lose function
DY D5
3D3V_S5
R74
10KR2J-3-GP
S3
PM_SLP_S3_CTL 8,21,44,51
Q4
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
PM_SLP_S3#
3D3V_AUX_S5
R75
10KR2J-3-GP
R76
100KR2J-1-GP
Q5
PM_RSMRST#
8223_PGOOD 47
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
All_PWRGD modify 51123_PGOOD from 3V/5V power
DVT 1ST
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH 3 of 9(DMI/FDI)
Size
A3
Document Number
TUCANA
Rev
SB
Date: Wednesday, July 07, 2010
Sheet 14 of 56

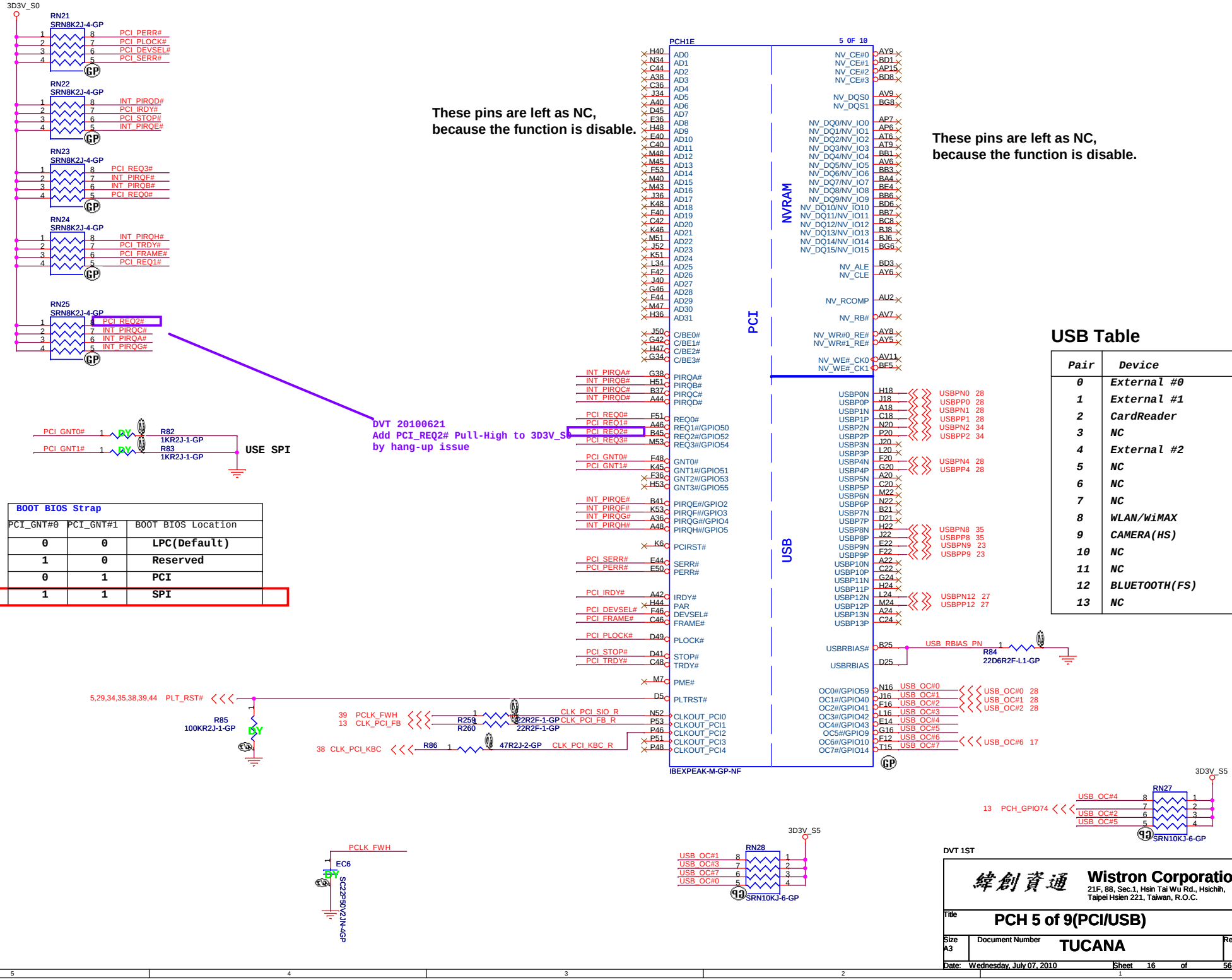
Panel backlight enable control for LVDS -
used to gate power into the backlight circuit



DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH 4 of 9(LVDS/CRT/DP)	
Size: Custom	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 15 of 56	



BOOT BIOS Strap

PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

USB Table

Pair	Device
0	External #0
1	External #1
2	CardReader
3	NC
4	External #2
5	NC
6	NC
7	NC
8	WLAN/WiMAX
9	CAMERA(HS)
10	NC
11	NC
12	BLUETOOTH(FS)
13	NC

DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH 5 of 9(PCI/USB)**

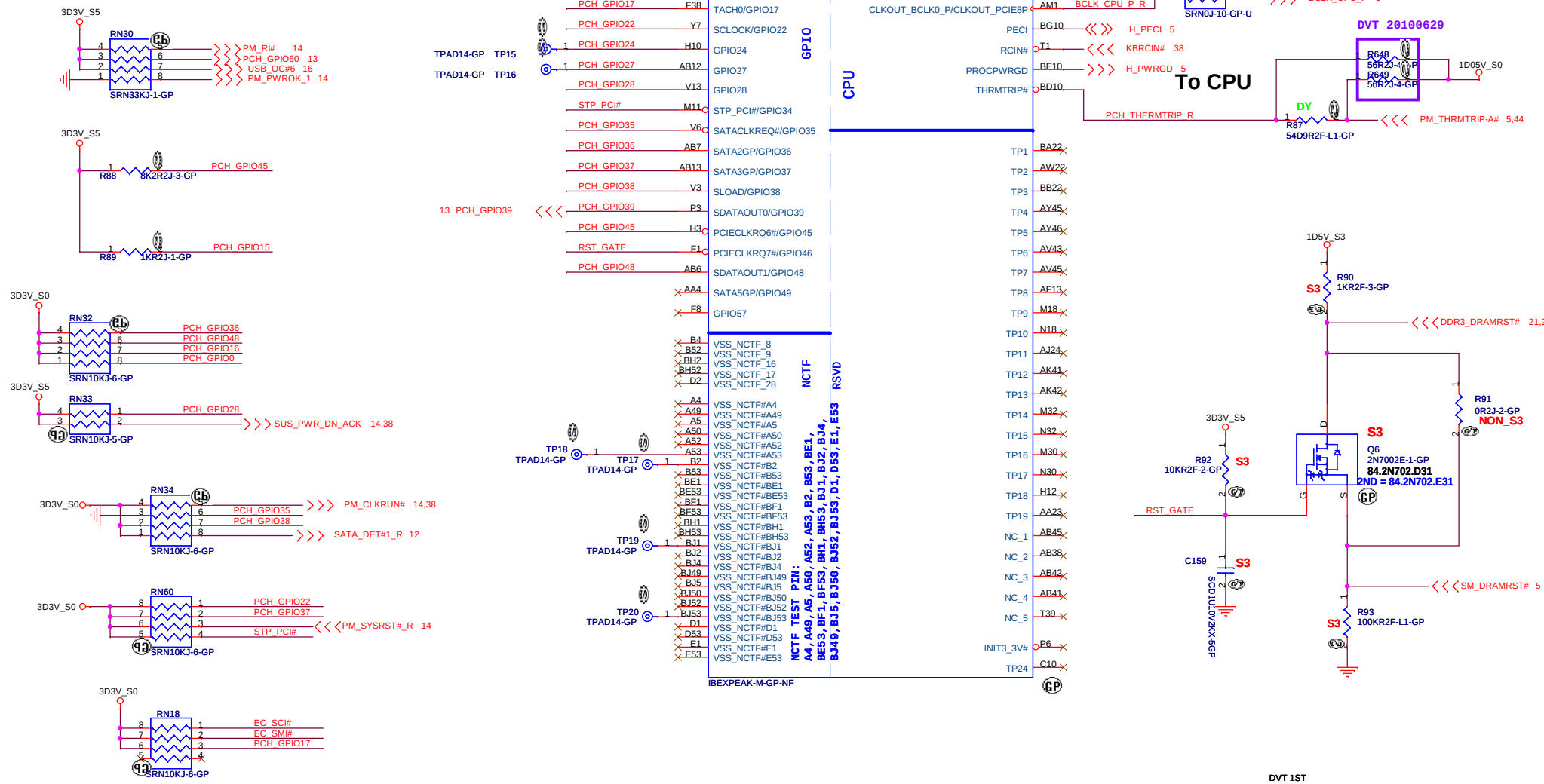
Size	Document Number	Rev
A3	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 16 of 56

GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

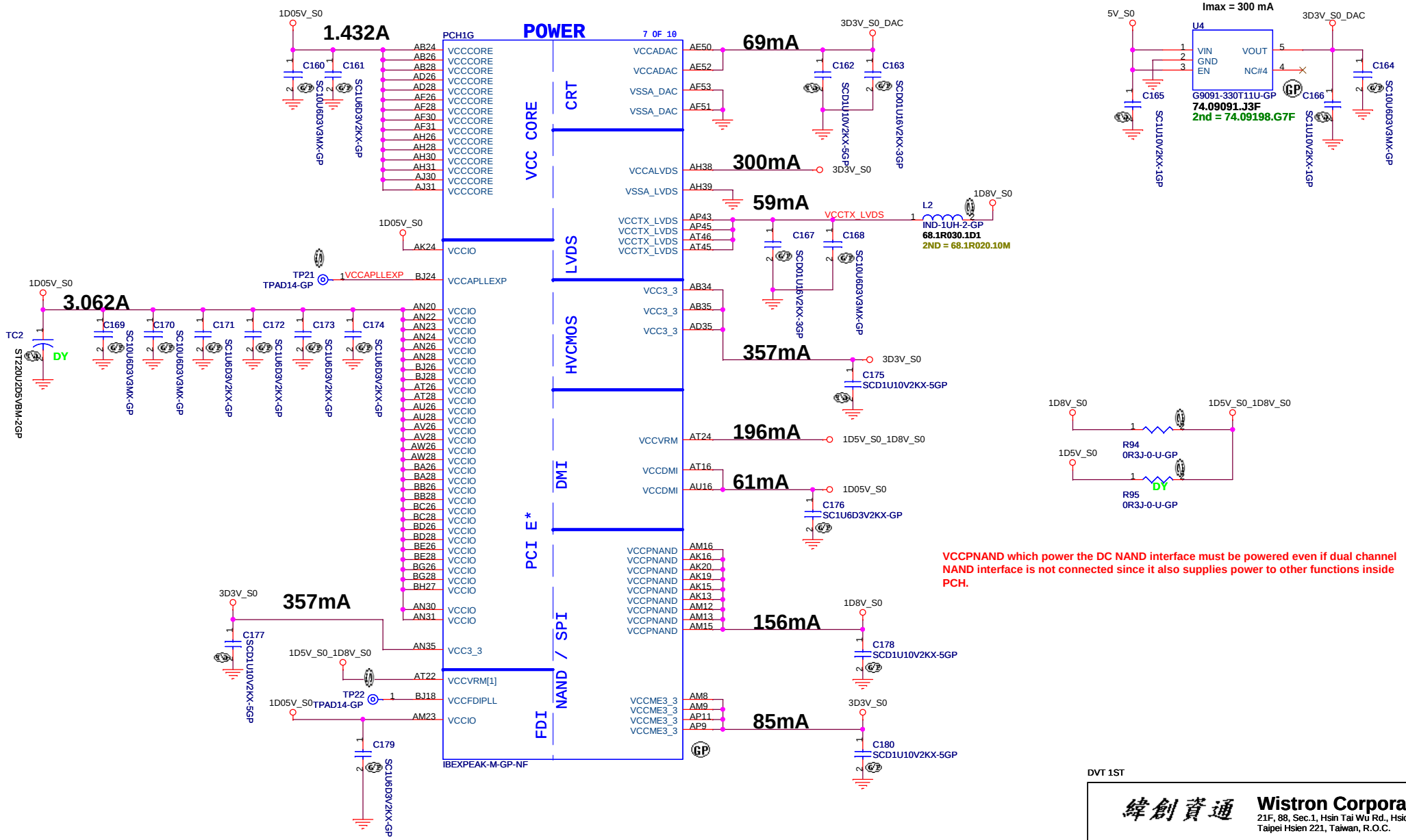
GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

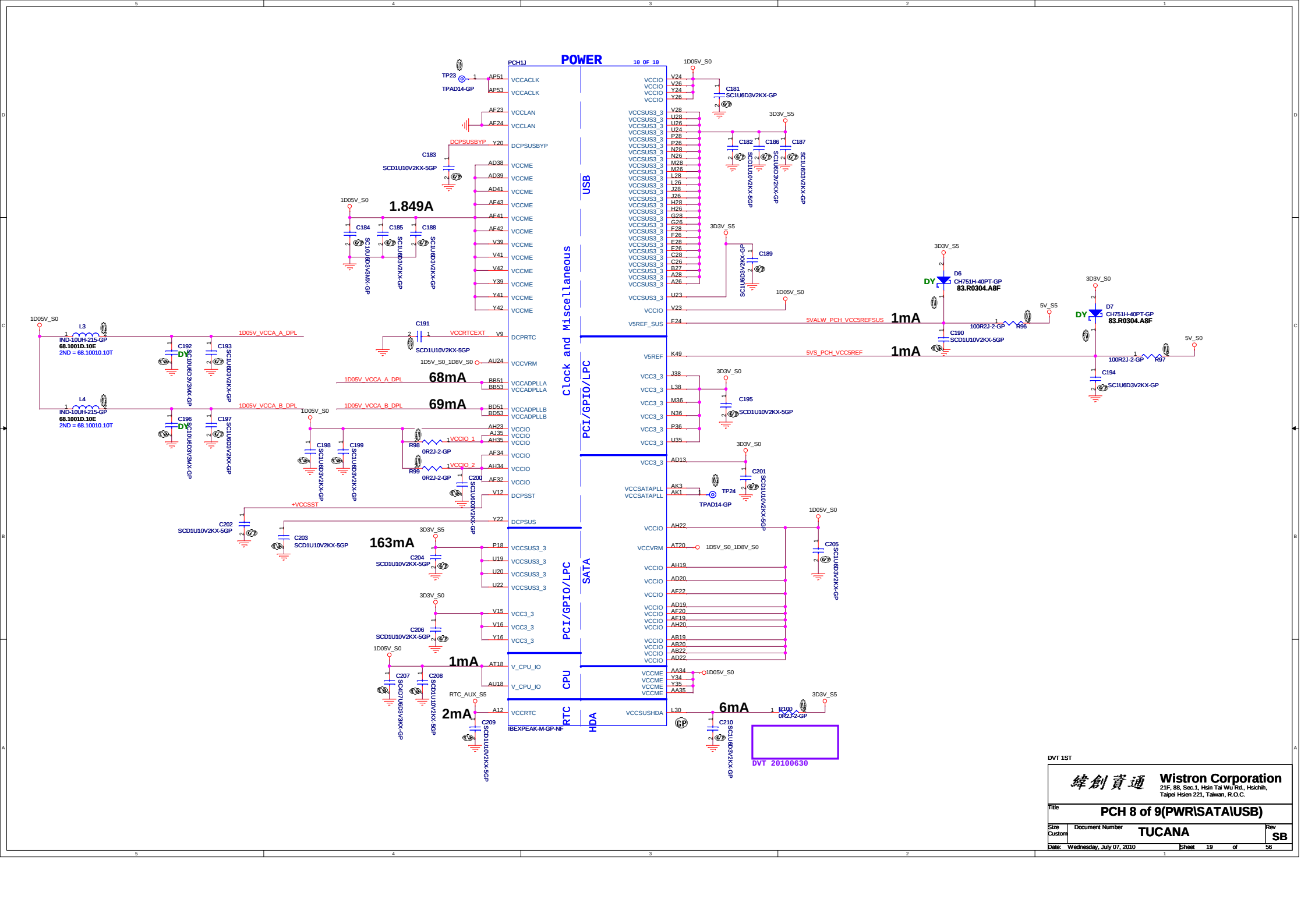
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

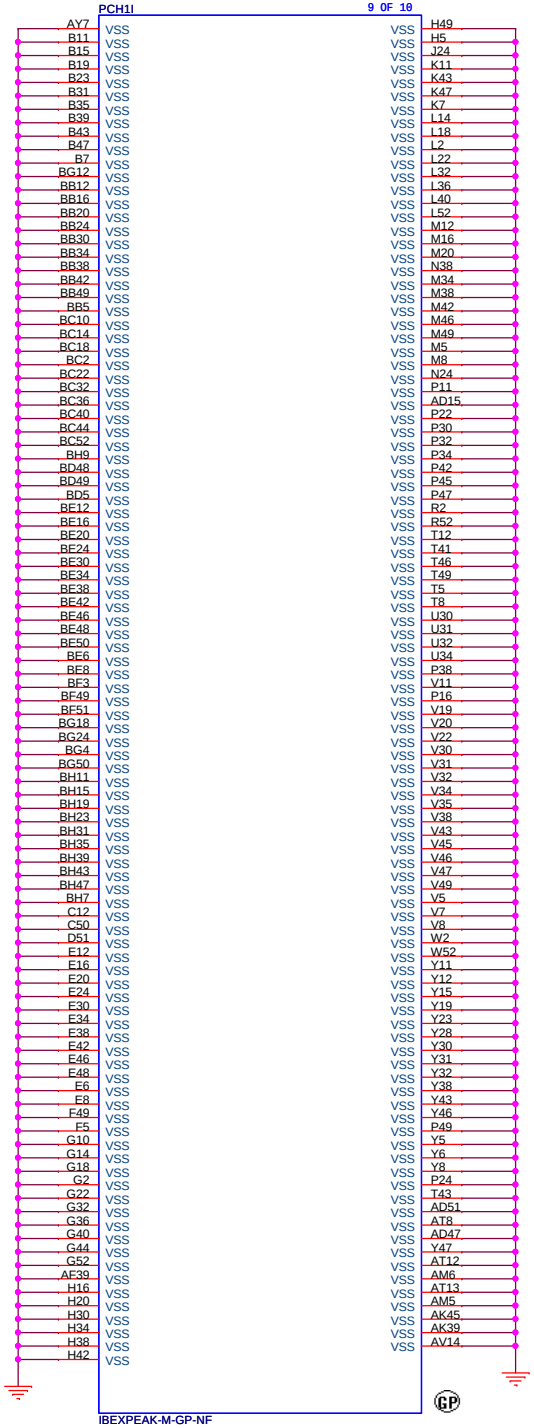


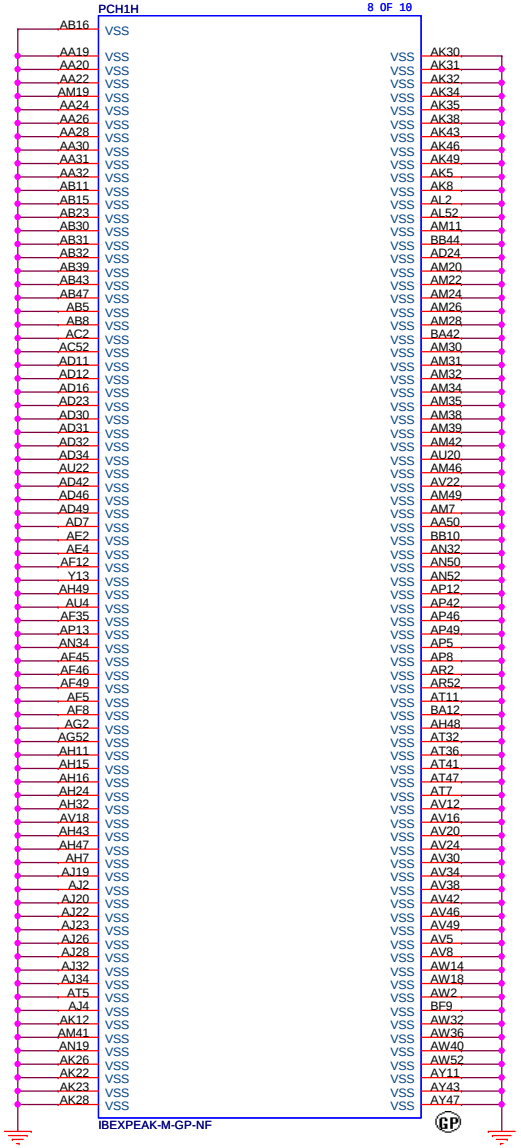
DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH 6 of 9(GPIO/RSVD)		
Size: A3	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 17 of 56	


POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.432A
3.062A
357mA
69mA
300mA
59mA
357mA
196mA
61mA
156mA
85mA
1D05V_S0
3D3V_S0
3D3V_S0_DAC
1D8V_S0
1D05V_S0_1D8V_S0
5V_S0
VCCADAC
VSSA_DAC
VCCALVDS
VSSA_LVDS
VCCTX_LVDS
VCC3_3
VCCVRM
VCCDMI
VCCPNAND
VCCME3_3
VCCIO
VCCAPLLEXP
VCCFDIPLL
VCCVRM[1]
IBEXPEAK-M-GP-NF
Imax = 300 mA
G9091-330T11U-GP
74.09091.J3F
2nd = 74.09198.G7F
IND-1UH-2-GP
68.1R030.1D1
2ND = 68.1R020.10M
0R3J-0-U-GP
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
DVT 1ST
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH 7 of 9(PWR/VCORE/LVDS)
TUCANA
SB
Date: Wednesday, July 07, 2010
Sheet 18 of 56


POWER
PCH1J
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
1.849A
68mA
69mA
163mA
1mA
2mA
6mA
5VALW_PCH_VCC5REFSUS
5VS_PCH_VCC5REF
DVT 20100630
DVT 1ST
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH 8 of 9(PWR\SATA\USB)
TUCANA
SB
Wednesday, July 07, 2010
19
56



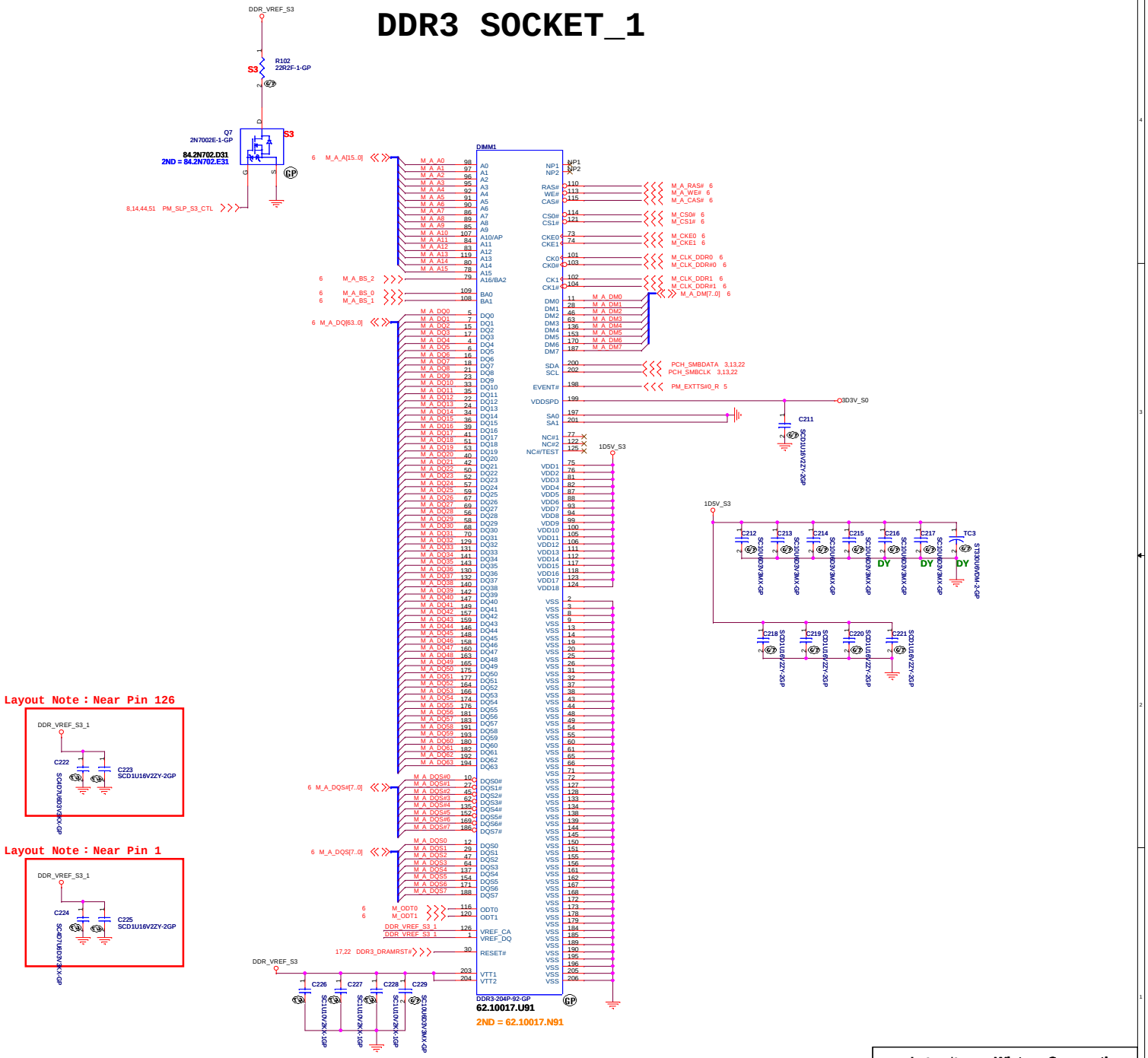


DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

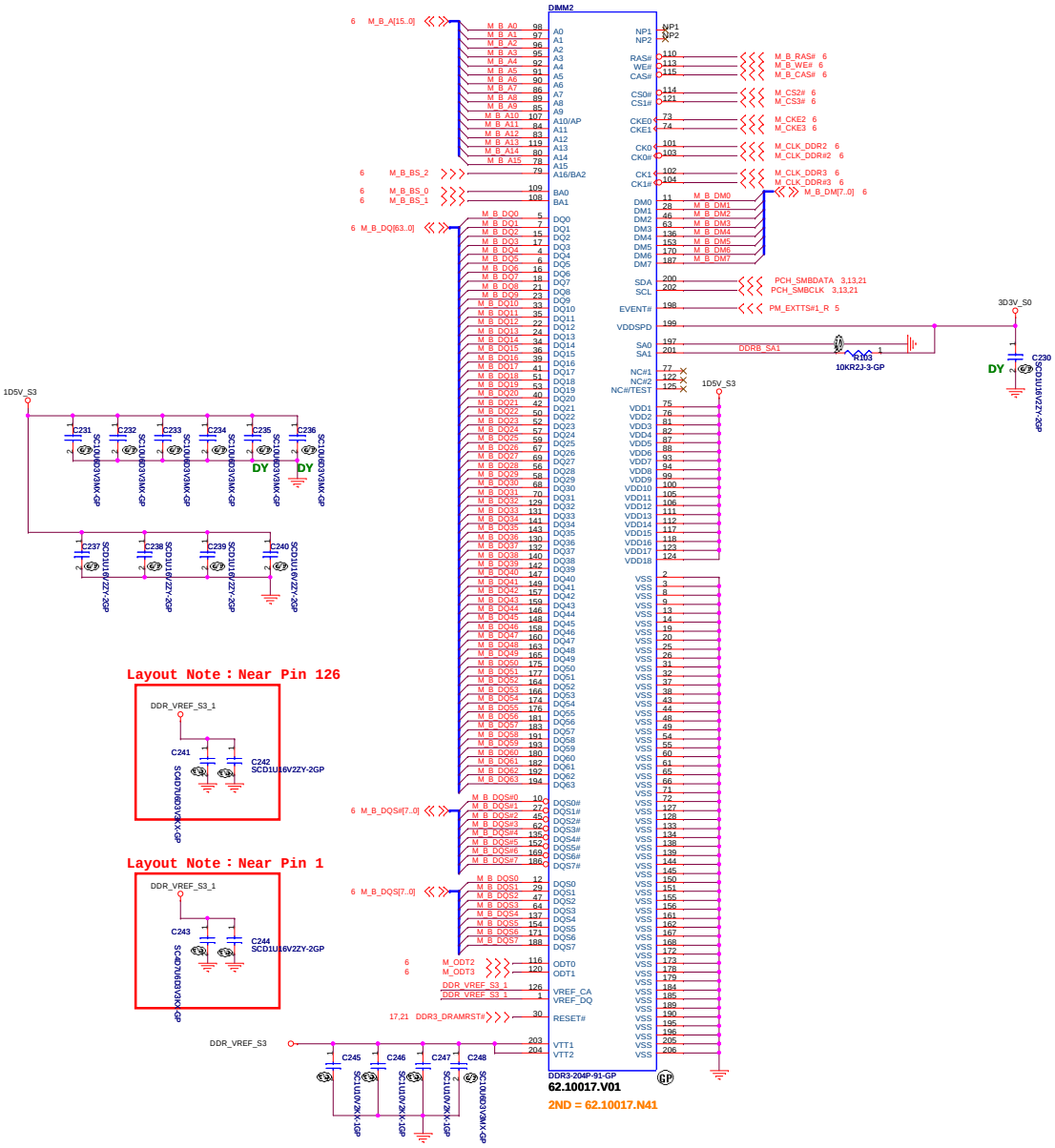
Title	PCH 9 of 9(VSS)	
Size A3	Document Number TUCANA	Rev SB
Date: Wednesday, July 07, 2010	Sheet 20 of 56	

DDR3 SOCKET_1



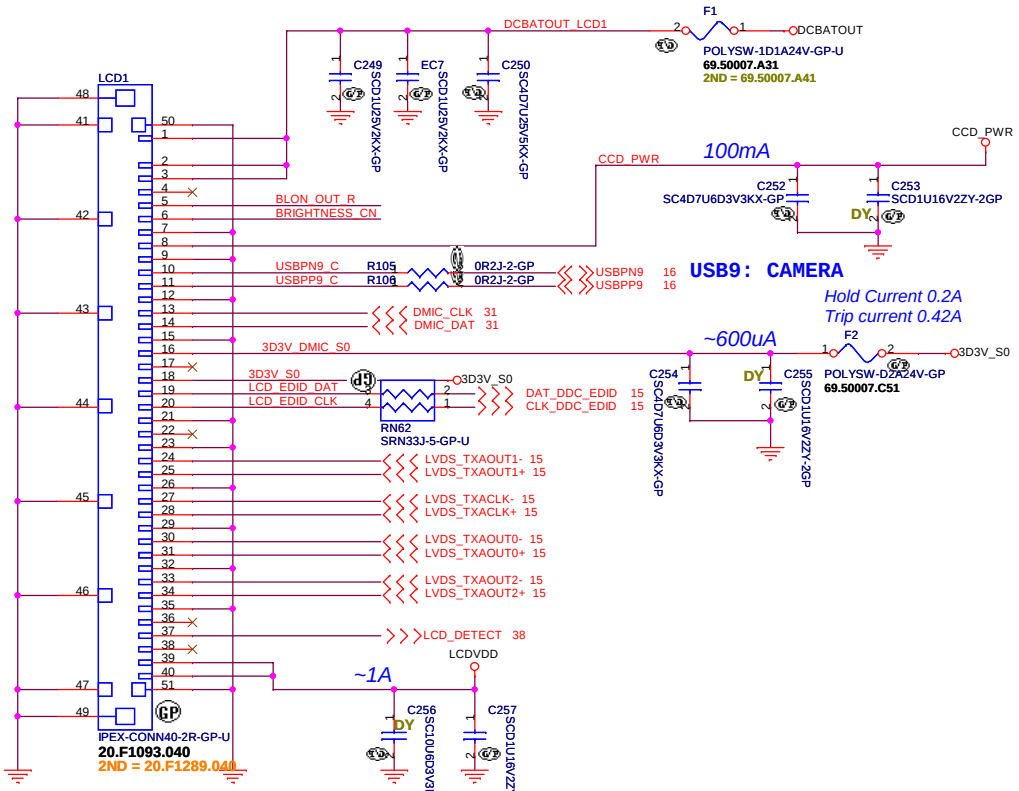
緯創資通 Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: DDR3 Socket1			
Size	Document Number: TUCANA	Rev: SB	
Date: Wednesday, July 07, 2010	Sheet 21 of 56		

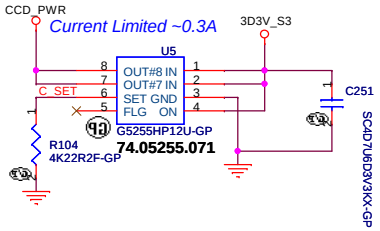
DDR3 SOCKET_2

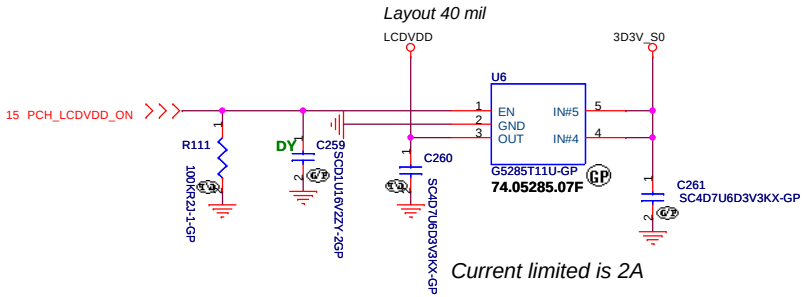


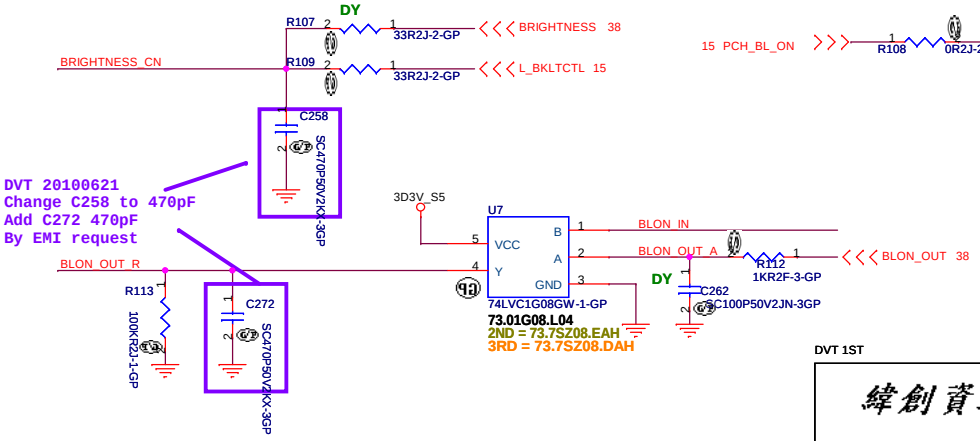
緯創資通 Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: DDR3 Socket2			
Size	Document Number: TUCANA	Rev: SB	
Date: Wednesday, July 07, 2010	Sheet 22 of 56		

LCD/CCD CONN









DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD CONN		
Size	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 23 of 56	

Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 40 ohm@100MHz

15 CRT_RED
15 CRT_GREEN
15 CRT_BLUE

CRT_RED
CRT_GREEN
CRT_BLUE

L5 SBK160808T-4[DY]-N-GP
L6 SBK160808T-4[DY]-N-GP
L7 SBK160808T-4[DY]-N-GP
68.00119.241
2ND = 68.00909.151

CRT_R
CRT_G
CRT_B

R116 150R2F-1-GP
R117 150R2F-1-GP
R118 150R2F-1-GP

C264 C265 C266 C267 C268 C269
SC5P50V2CN-2GP

3D3V_S0
5V_S0

C263 SCD1U16V2ZY-2GP

U8
CM2009-02QR-GP
83.02009.BA0

VCC_SYNC
VCC_VIDEO
VCC_DDC
VIDEO_1
VIDEO_2
VIDEO_3
BYP
DDC_IN1
DDC_IN2
DDC_OUT1
DDC_OUT2
SYNC_IN1
SYNC_IN2
SYNC_OUT1
SYNC_OUT2
GND

C270 SCD22U10V2KX-1GP

R114 R115 2K7R2J-GP

CLK_DDC1_5
DAT_DDC1_5

CRT_DDCCLK 15
CRT_DDCDATA 15
CRT_HSYNC 15
CRT_VSYNC 15

CRT_HSYNC1_R
CRT_VSYNC1_R
CRT_HSYNC1
CRT_VSYNC1

RN35 SRN33J-5-GP-U

DVT 20100621
Change R114,R115,R119,R120 to 2.7K ohm for CRT VEVS report

CRT_DDCCLK
CRT_DDCDATA
R119 2K7R2J-GP
R120 2K7R2J-GP

EC122 EC123 SCD01U50V2KX-1GP

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR

6 1 7 2 8 3 9 4 10 5

5V_CRT_S0

EC8 EC9 SCD1U16V2ZY-2GP

CRT1
D-SUB-15-76-GP
20.20891.015
2ND = 20.20886.015

NC#4
NC#11
VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
GND
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC

DAT_DDC1_5
CLK_DDC1_5
CRT_R
CRT_G
CRT_B
CRT_VSYNC1
CRT_HSYNC1

C273 SCD01U50V2KX-1GP

~300mA

D8 CH551H-30PT-GP
83.R5003.C8F
2ND = 83.5R003.08F
3RD = 83.R5003.H8H

F6 POLYSW-40A60V-GP
69.44002.001

5V_S0

DVT 20100601
Change F6 to 69.44002.001, for Cadiz use

C274 C275 C276 C277 DY
SC18P50V2JN-1-GP

DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT CONN**
Size | Document Number: **TUCANA** | Rev: **SB**
Date: Wednesday, July 07, 2010 | Sheet 24 of 56

DVT 20100611
Change C283,C364 to 1uF
Change C282,C285 to 1KpF
for EMI request

3D3V_S0

C284 SCD1U16V2ZY-2GP
C285 SC1KP50V2KX-1GP
C286 SCD1U16V2ZY-2GP
C364 SC1U6D3V2KX-GP
C280 SCD1U16V2ZY-2GP
C281 SCD1U16V2ZY-2GP
C282 SC1KP50V2KX-1GP
C283 SC1U6D3V2KX-GP

VCC x8, NC#35, NC#34

15 PCH_HDMI_DATA0-_L
15 PCH_HDMI_DATA0+_L
C290 SCD1U10V2KX-5GP
C291 SCD1U10V2KX-5GP
HDMI_DATA0- 38
HDMI_DATA0+ 39
IN_D1-
IN_D1+

15 PCH_HDMI_CLK-_L
15 PCH_HDMI_CLK+_L
C288 SCD1U10V2KX-5GP
C289 SCD1U10V2KX-5GP
HDMI_CLK- 41
HDMI_CLK+ 42
IN_D2-
IN_D2+

15 PCH_HDMI_DATA1-_L
15 PCH_HDMI_DATA1+_L
C292 SCD1U10V2KX-5GP
C293 SCD1U10V2KX-5GP
HDMI_DATA1- 44
HDMI_DATA1+ 45
IN_D3-
IN_D3+

15 PCH_HDMI_DATA2-_L
15 PCH_HDMI_DATA2+_L
C294 SCD1U10V2KX-5GP
C295 SCD1U10V2KX-5GP
HDMI_DATA2- 47
HDMI_DATA2+ 48
IN_D4-
IN_D4+

OUT_D1- 23 HDMI_TX0-
OUT_D1+ 22 HDMI_TX0+
OUT_D2- 20 HDMI_TXC-
OUT_D2+ 19 HDMI_TXC+
OUT_D3- 17 HDMI_TX1-
OUT_D3+ 16 HDMI_TX1+
OUT_D4- 14 HDMI_TX2-
OUT_D4+ 13 HDMI_TX2+

Recommended Equalization: [PC1,PC0]=01, 4dB
3D3V_S0
R122 DY 4K7R2J-2-GP
R121 5K1R2F-2-GP
PC0 3
PC1 4
PC0
PC1

R493 499R2F-2-GP
REXT_HDMI 6
RT_EN# 10
P8101_OE# 25
DDC_EN_PS8101 32
REXT
RT_EN#
OE#
DDC_EN

SDA 8
SCL 9
HPD 7
PCH_HDMI_DATA 15
PCH_HDMI_CLK 15
PCH_HDMI_DETECT 15
R123 100KR2J-1-GP

HPD_SINK 30 HDMI_HPD
SDA_SINK 29 TMDS_SDA
SCL_SINK 28 TMDS_SCL

GND x9

U73
PS8101-GP
71.P8101.003

HDMI in : Hi
HDMI out : Low

HDMI1
HDMI_TX2+_R 20
HDMI_TX2-_R 3
HDMI_TX1+_R 4
HDMI_TX1-_R 6
HDMI_TX0+_R 7
HDMI_TX0-_R 9
HDMI_TXC+_R 10
HDMI_TXC-_R 12
HDMI_A_CEC 13
TMDS_SCL 15
TMDS_SDA 16
HDMI_5V_S0_1_R 18
HDMI_HPD 19
NP1 1
NP2 21
23 22
SKT-HDMI25P-1-GP
22.10296.461

TP25 TPAD14-GP
3D3V_S0
R124 20KR2J-L2-GP
P8101_OE#
Q12 2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31

DVT 20100630
Change Q12 to 84.2N702.D31
(ESD Protected 1.0KV)

DVT 20100517
change 2nd source to 69.4R500.151

5V_S0
F4 FUSE-D5A6Y-2-GP
69.4R500.141
2ND = 69.4R500.151
HDMI_5V_S0_1
Q59 AO3413-GP
84.03413.A31
2ND = 84.02130.031
HDMI_5V_S0_1_R

R620 10KR2J-3-GP
R621 10KR2J-3-GP
C278 SCD1U10V2KX-4GP
C279 SC1KP50V2KX-1GP

Q60 2N7002E-1-GP
84.2N702.D31
2nd = 84.2N702.E31
14,46 CORE_PWRGD

HDMI_5V_S0_1_R
D9 CH551H-30PT-GP
83.R5003.C8F
2ND = 83.5R003.08F
3RD = 83.R5003.H8H
RN36 SRN2K2J-1-GP
TMDS_SCL
TMDS_SDA

3D3V_S0
RN51 SRN2K2J-1-GP
PCH_HDMI_DATA
PCH_HDMI_CLK

3D3V_S0
R127 4K7R2J-2-GP
PC0
R126 4K7R2J-2-GP
DDC_EN_PS8101
R125 4K7R2J-2-GP
RT_EN#

U9
HDMI_TX2-_R
HDMI_TX2+_R
R182 0R2J-2-GP
R215 0R2J-2-GP
HDMI_TX2-
HDMI_TX2+
FILTER-4P-14-GP
69.10118.051
2nd = 68.01210.20C
R614 200R2J-L1-GP

U11
HDMI_TX0-_R
HDMI_TX0+_R
R183 0R2J-2-GP
R222 0R2J-2-GP
HDMI_TX0-
HDMI_TX0+
FILTER-4P-14-GP
69.10118.051
2nd = 68.01210.20C
R615 200R2J-L1-GP

DVT 20100611
Change R614~R617 to 200R ohm
By EMI request

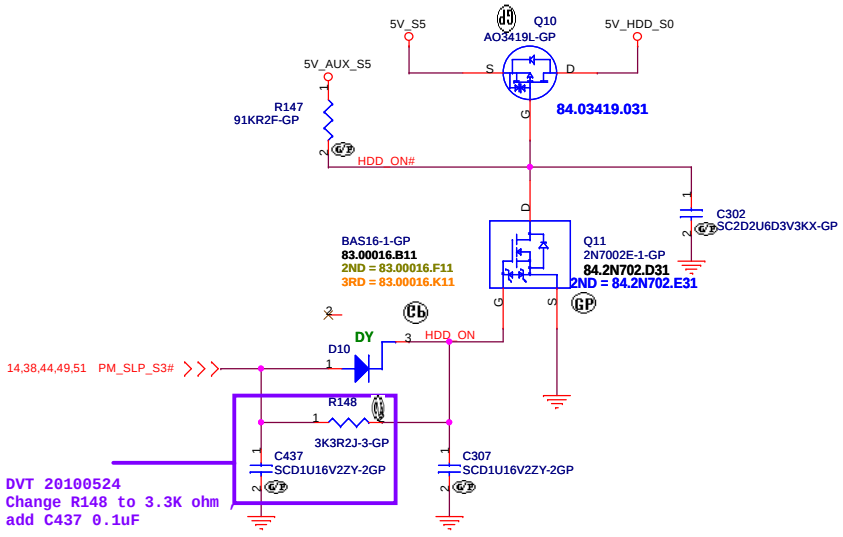
U10
HDMI_TX1-_R
HDMI_TX1+_R
R185 0R2J-2-GP
R223 0R2J-2-GP
HDMI_TX1-
HDMI_TX1+
FILTER-4P-14-GP
69.10118.051
2nd = 68.01210.20C
R616 200R2J-L1-GP

U12
HDMI_TXC-_R
HDMI_TXC+_R
R186 0R2J-2-GP
R241 0R2J-2-GP
HDMI_TXC-
HDMI_TXC+
FILTER-4P-14-GP
69.10118.051
2nd = 68.01210.20C
R617 200R2J-L1-GP

DVT 1ST

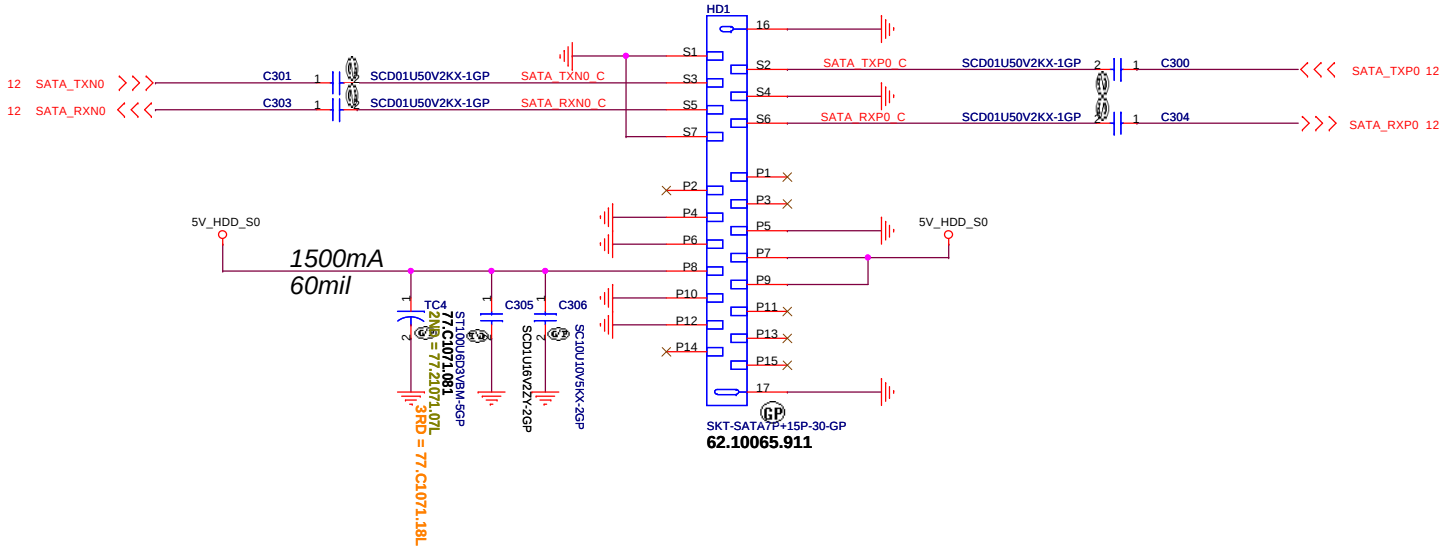
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI CONN
Size: | Document Number: TUCANA | Rev: SB
Date: Wednesday, July 07, 2010 Sheet 25 of 56



Delay HDD power off timing for 400ms after SATA controller shut down. Control the C307 and R148 to finally tune delay timing between 500ms and 400ms.

SSD SATA Connector



<Core Design>

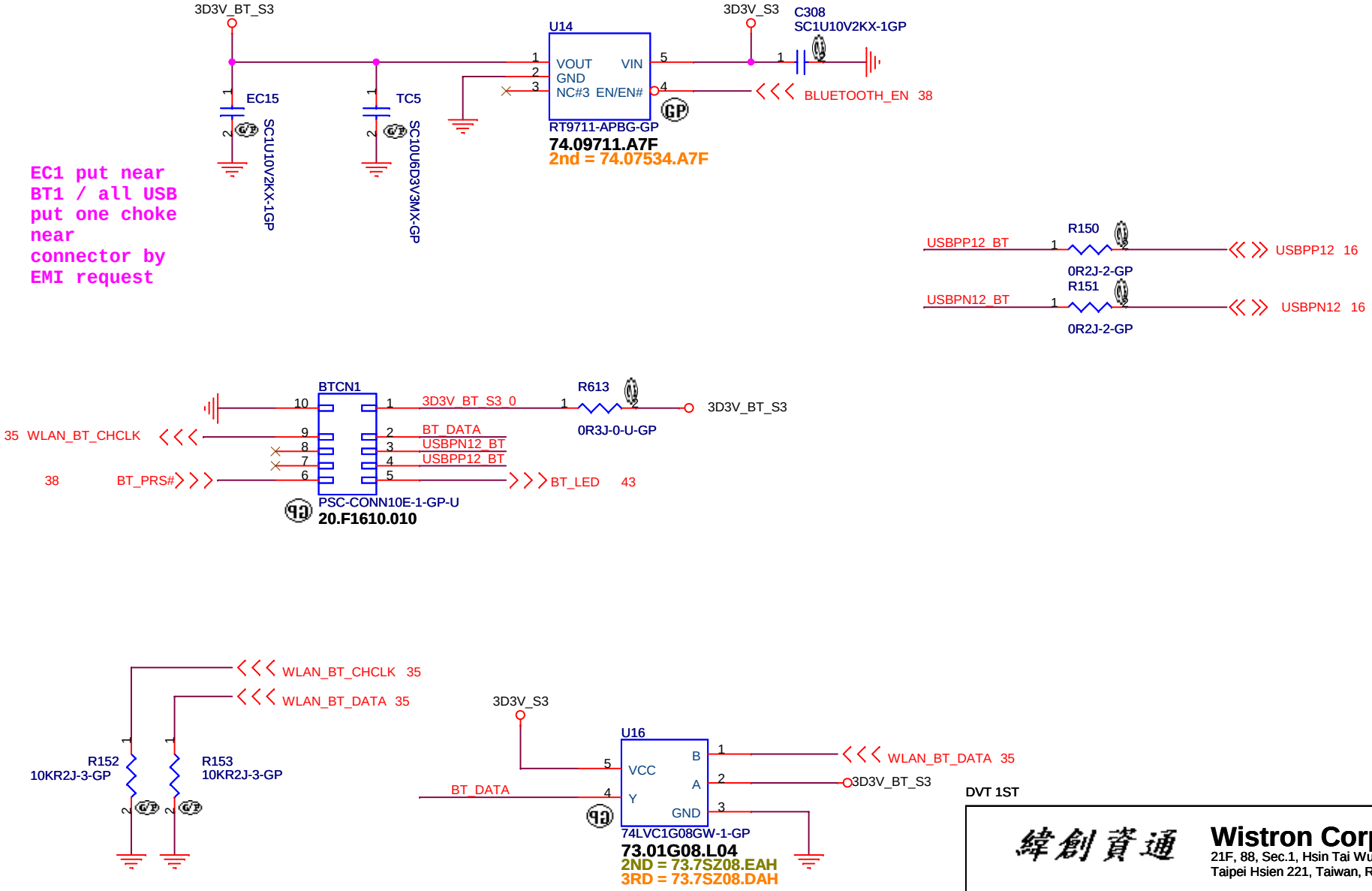
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD Connector

Size	Document Number	Rev
	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 26 of 56

Bluetooth



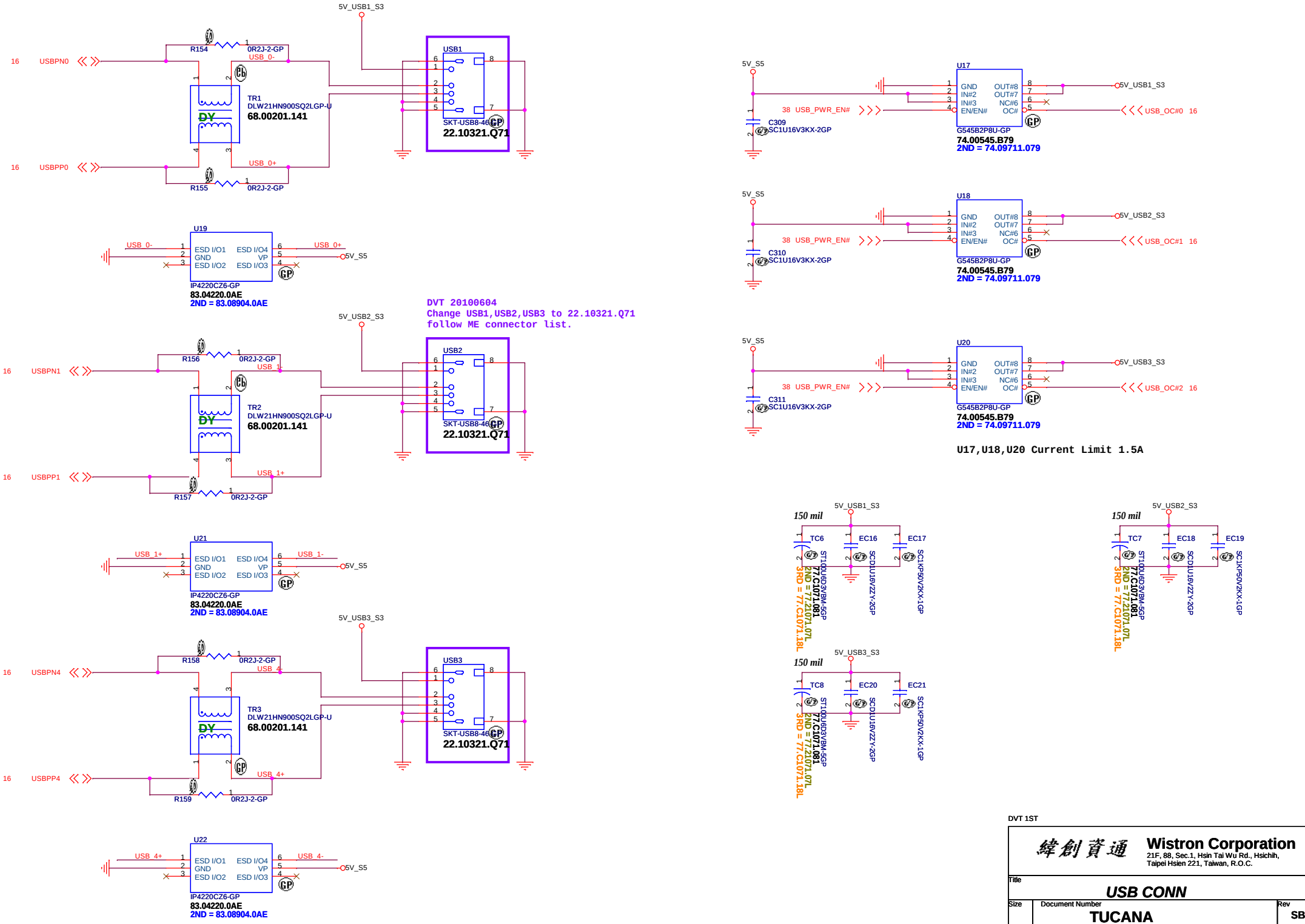
DVT 1ST

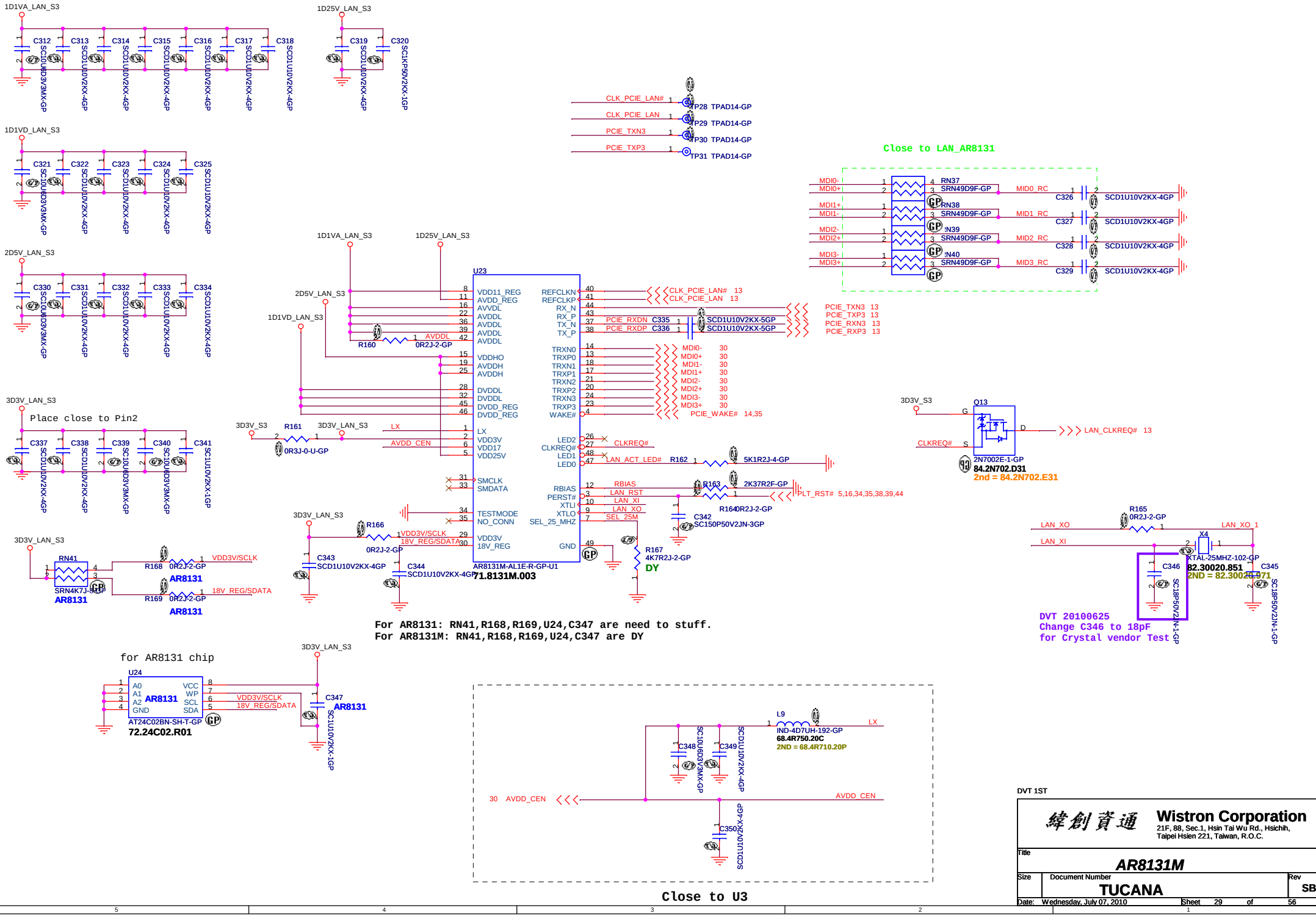
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 27 of 56


5V_USB1_S3
R154
0R2J-2-GP
USB_0-
16 USBPN0
TR1
DLW21HN900SQ2LGP-U
68.00201.141
DY
USB1
SKT-USB8-46
22.10321.Q71
16 USBPP0
USB_0+
R155
0R2J-2-GP
U19
USB_0-
ESD I/O1
GND
ESD I/O2
ESD I/O4
VP
ESD I/O3
USB_0+
5V_S5
IP4220CZ6-GP
83.04220.0AE
2ND = 83.08904.0AE
DVT 20100604
Change USB1,USB2,USB3 to 22.10321.Q71
follow ME connector list.
5V_USB2_S3
R156
0R2J-2-GP
USB_1-
16 USBPN1
TR2
DLW21HN900SQ2LGP-U
68.00201.141
DY
USB2
SKT-USB8-46
22.10321.Q71
16 USBPP1
USB_1+
R157
0R2J-2-GP
U21
USB_1+
ESD I/O1
GND
ESD I/O2
ESD I/O4
VP
ESD I/O3
USB_1-
5V_S5
IP4220CZ6-GP
83.04220.0AE
2ND = 83.08904.0AE
5V_USB3_S3
R158
0R2J-2-GP
USB_4-
16 USBPN4
TR3
DLW21HN900SQ2LGP-U
68.00201.141
DY
USB3
SKT-USB8-46
22.10321.Q71
16 USBPP4
USB_4+
R159
0R2J-2-GP
U22
USB_4+
ESD I/O1
GND
ESD I/O2
ESD I/O4
VP
ESD I/O3
USB_4-
5V_S5
IP4220CZ6-GP
83.04220.0AE
2ND = 83.08904.0AE
5V_S5
U17
38 USB_PWR_EN#
C309
SC1U16V3KX-2GP
GND
IN#2
IN#3
EN/EN#
OUT#8
OUT#7
NC#6
OC#
5V_USB1_S3
USB_OC#0 16
G545B2P8U-GP
74.00545.B79
2ND = 74.09711.079
5V_S5
U18
38 USB_PWR_EN#
C310
SC1U16V3KX-2GP
5V_USB2_S3
USB_OC#1 16
G545B2P8U-GP
74.00545.B79
2ND = 74.09711.079
5V_S5
U20
38 USB_PWR_EN#
C311
SC1U16V3KX-2GP
5V_USB3_S3
USB_OC#2 16
G545B2P8U-GP
74.00545.B79
2ND = 74.09711.079
U17,U18,U20 Current Limit 1.5A
5V_USB1_S3
150 mil
TC6
EC16
EC17
ST10U6D3VBM-5GP
77.C1071.081
2ND = 77.21071.07L
3RD = 77.C1071.18L
SCDU16V2ZY-2GP
SC1KF50V2KX-1GP
5V_USB2_S3
150 mil
TC7
EC18
EC19
ST10U6D3VBM-5GP
77.C1071.081
2ND = 77.21071.07L
3RD = 77.C1071.18L
SCDU16V2ZY-2GP
SC1KF50V2KX-1GP
5V_USB3_S3
150 mil
TC8
EC20
EC21
ST10U6D3VBM-5GP
77.C1071.081
2ND = 77.21071.07L
3RD = 77.C1071.18L
SCDU16V2ZY-2GP
SC1KF50V2KX-1GP
DVT 1ST
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
USB CONN
Size
Document Number
TUCANA
Rev
SB
Date: Wednesday, July 07, 2010
Sheet 28 of 56



DVT 1ST

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AR8131M

Size	Document Number	Rev
	TUCANA	SB

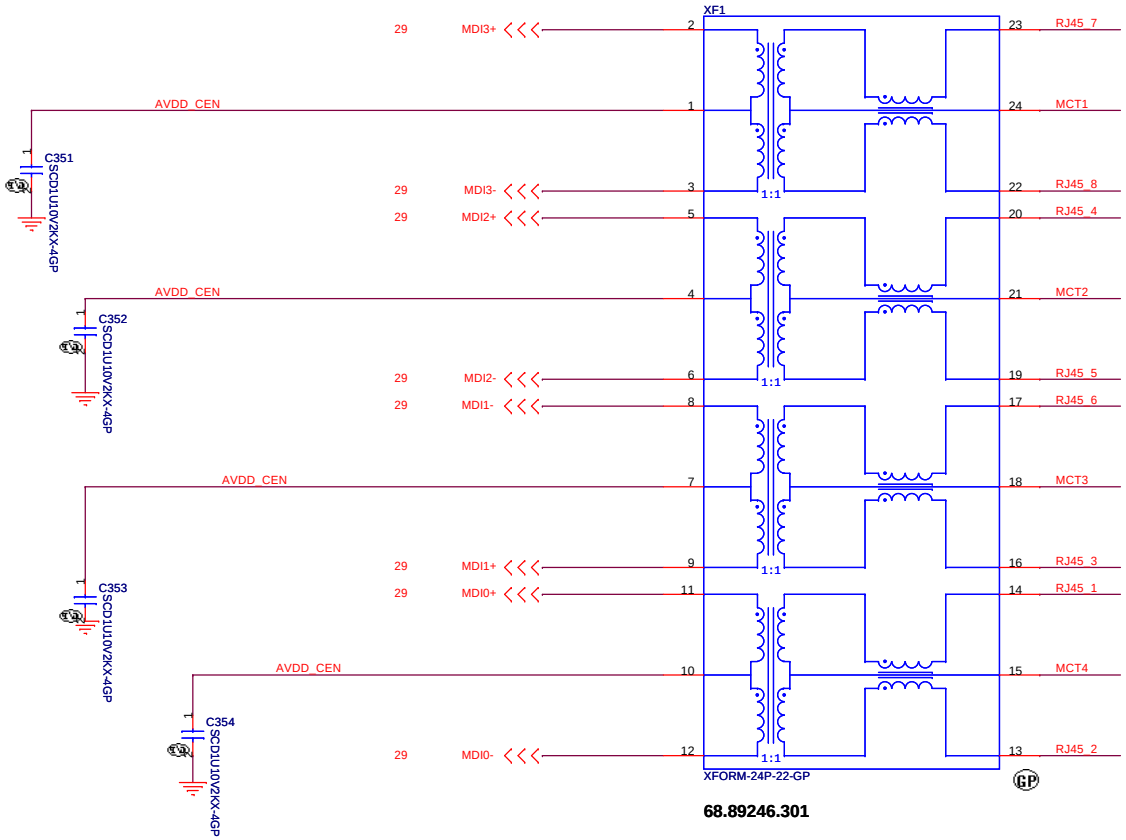
Date: Wednesday, July 07, 2010 Sheet 29 of 56

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

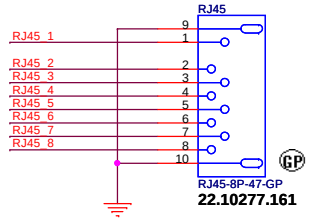
LAN Transformer

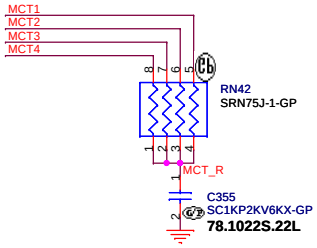
AVDD_CEN 29

GIGA Lan Transformer



LAN Connector

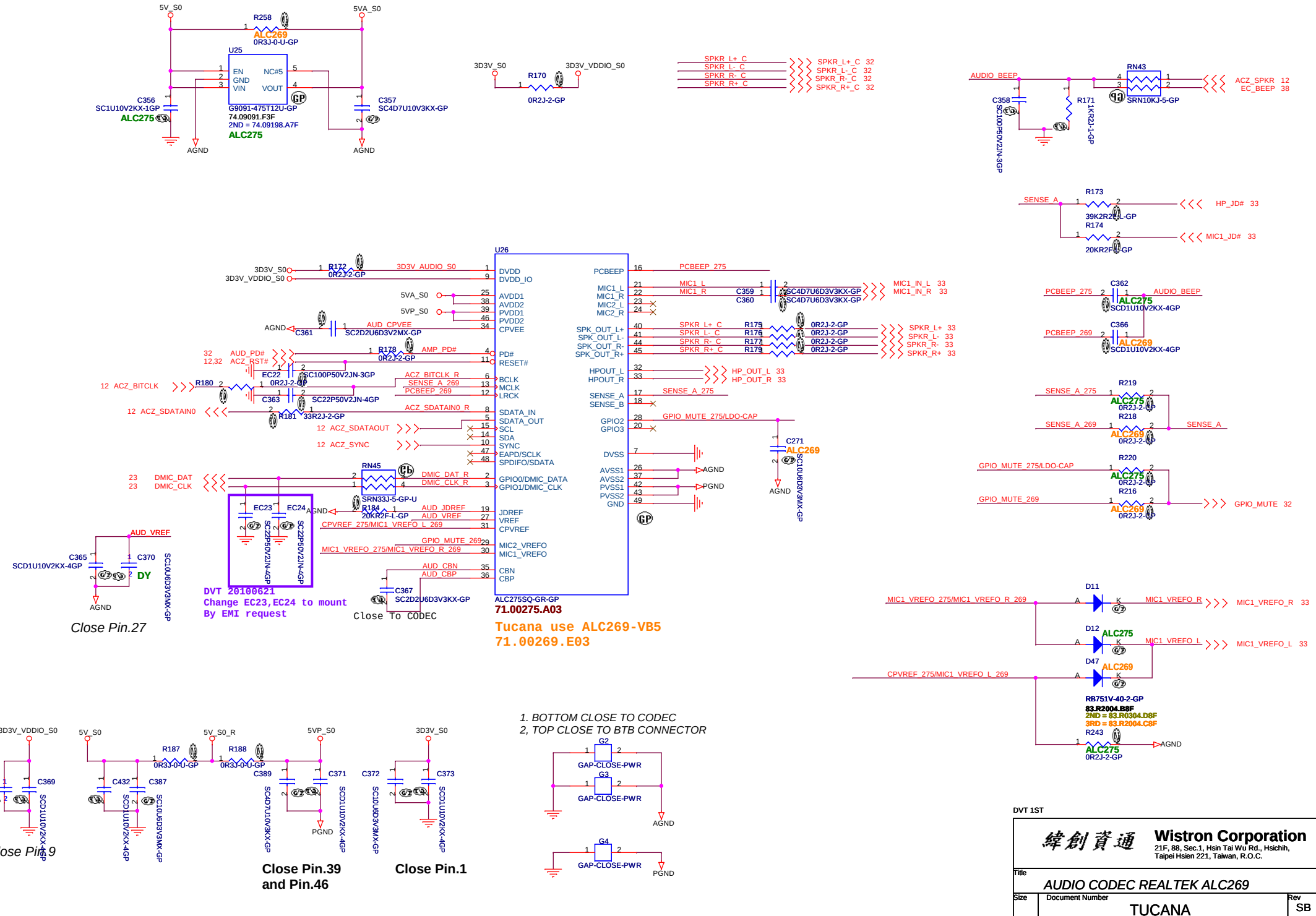




DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**		
Size	Document Number: **TUCANA**	Rev: **SB**
Date: Wednesday, July 07, 2010	Sheet 30 of 56	



DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO CODEC REALTEK ALC269*

Size	Document Number	Rev
	TUCANA	SB

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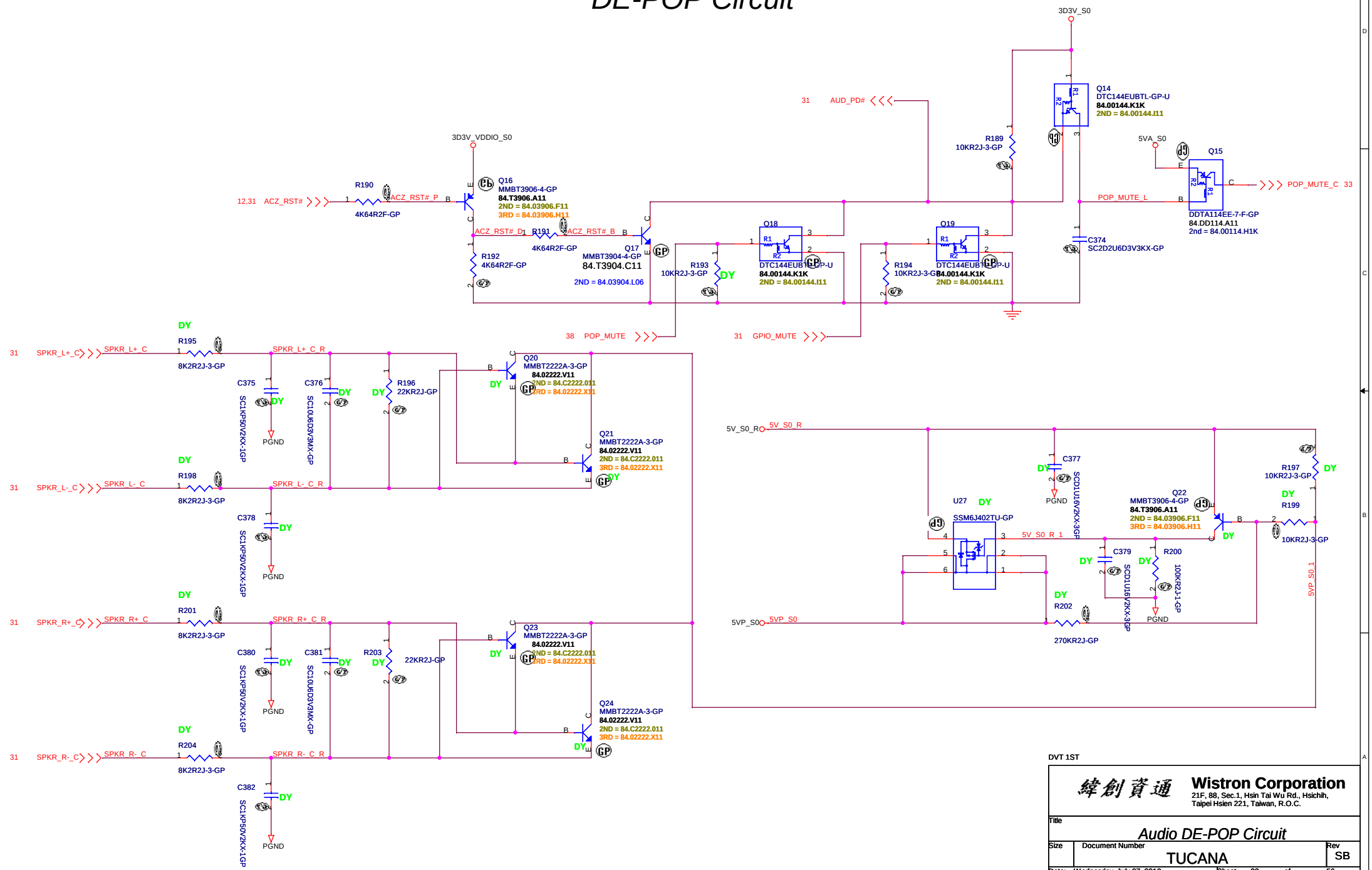
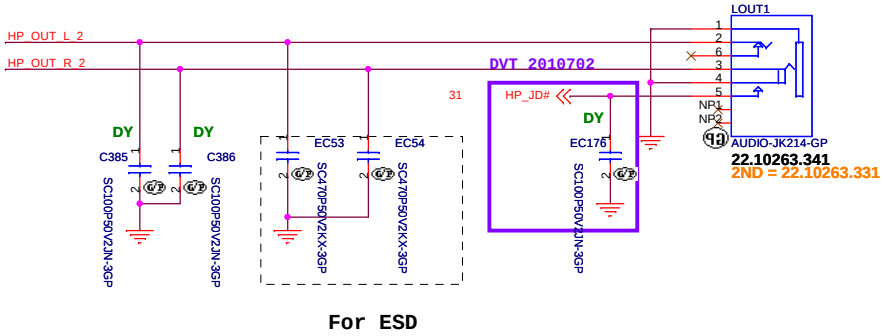
DE-POP Circuit



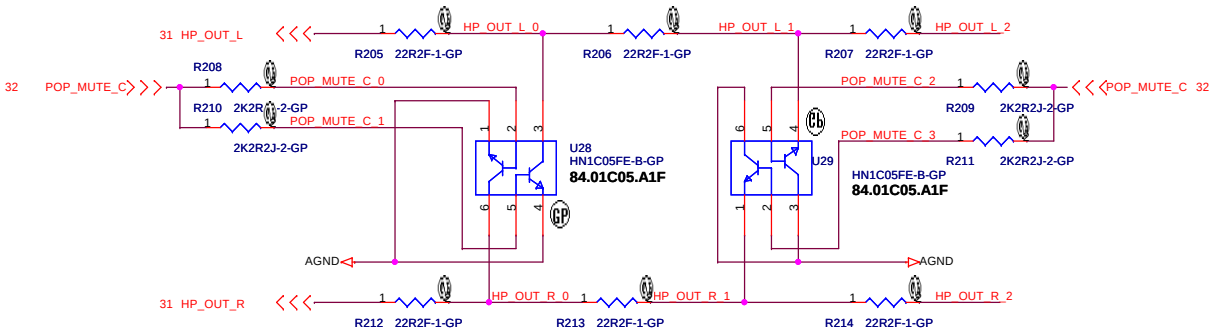
DVT 1ST

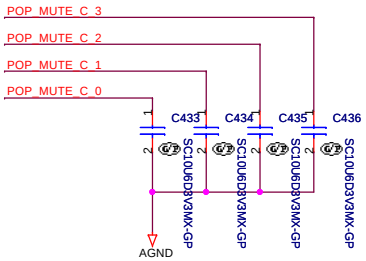
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*Audio DE-POP Circuit*	
Size	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 32 of 56	

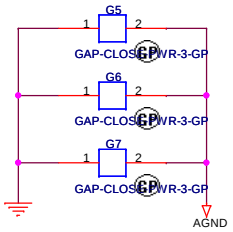
LINE OUT



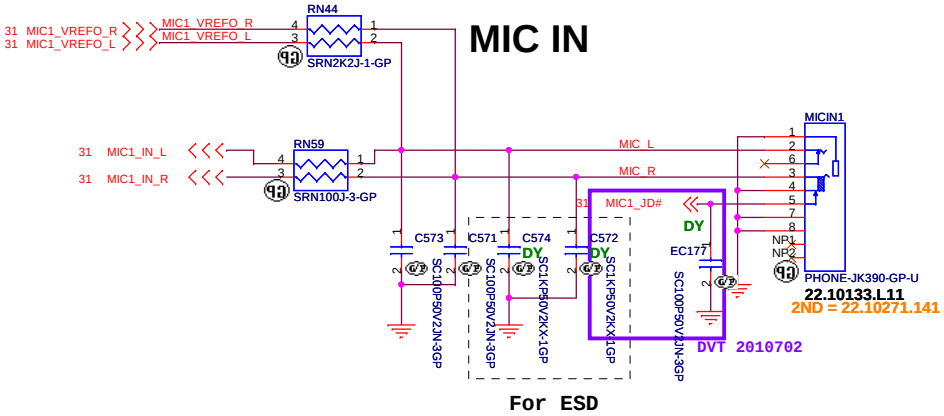
For ESD





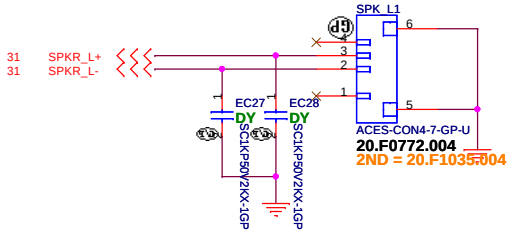


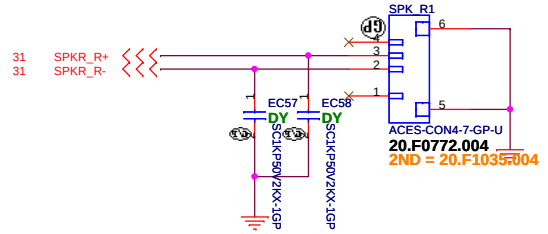
MIC IN



For ESD

Internal Speaker CONN





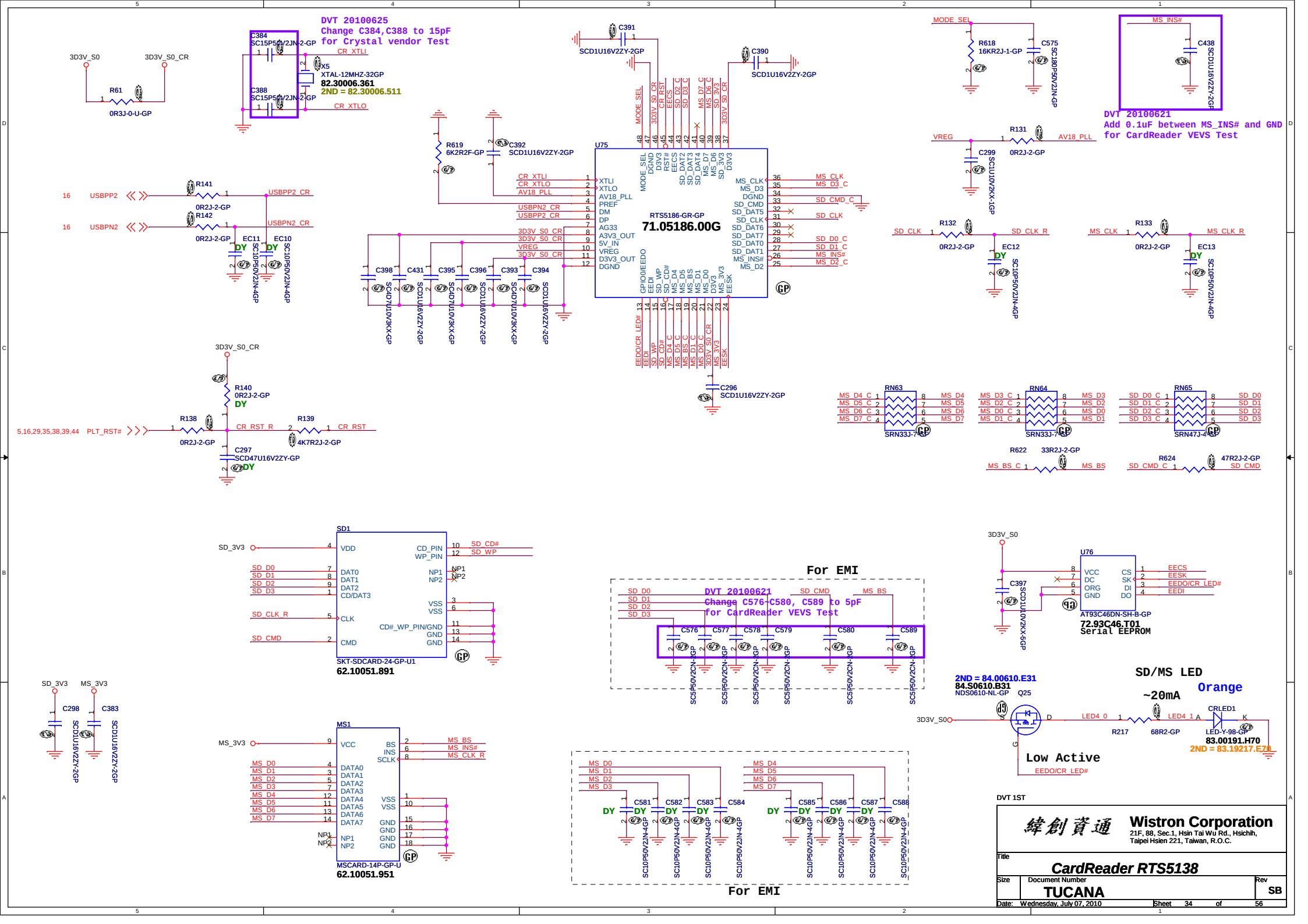
DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack & Speaker

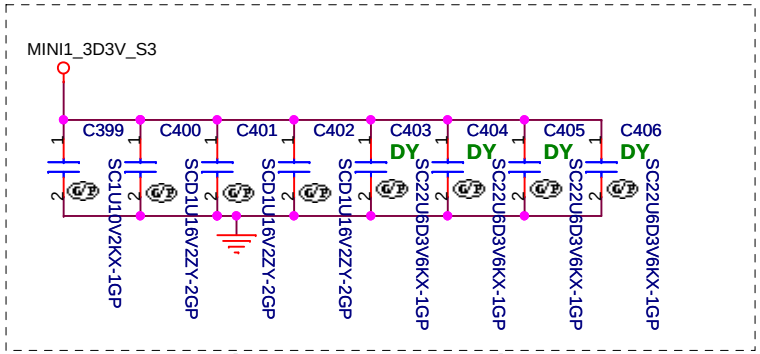
Size	Document Number	Rev
	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 33 of 56


DVT 20100625
Change C384,C388 to 15pF
for Crystal vendor Test
DVT 20100621
Add 0.1uF between MS_INS# and GND
for CardReader VEVS Test
RTS5186-GR-GP
71.05186.00G
U75
SKT-SDCARD-24-GP-U1
62.10051.891
MSCARD-14P-GP-U
62.10051.951
AT93C46DN-SH-B-GP
72.93C46.T01
Serial EEPROM
For EMI
DVT 20100621
Change C576~C580, C589 to 5pF
for CardReader VEVS Test
2ND = 84.00610.E31
84.S0610.B31
NDS0610-NL-GP Q25
SD/MS LED
Orange
~20mA
Low Active
LED-Y-98-GP
83.00191.H70
2ND = 83.19217.E70
DVT 1ST
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CardReader RTS5138
TUCANA
Rev SB
Date: Wednesday, July 07, 2010
Sheet 34 of 56

Mini Card Connector(WLAN)

WLAN_EN:
Low: disable the radio
High: enable the radio



C50,C68 bypass MINI1 pin2
C51,C69 bypass MINI1 pin39
C52,C70 bypass MINI1 pin41
C53,C71 bypass MINI1 pin52
Place near MINI1

MINI1
PTWO-CONN52A-8-GP
20.F1518.052
2ND = 62.10043.981

WAKE#
27 WLAN_BT_DATA
27 WLAN_BT_CHCLK
13 WLAN_CLKREQ#
13 CLK_PCIE_MINI1#
13 CLK_PCIE_MINI1
38 E51_RxD
38 E51_TxD
R611 0R2J-2-GP
R612 0R2J-2-GP
E51_RxD_1
E51_TxD_1
13 PCIE_RXN1
13 PCIE_RXP1
13 PCIE_TXN1
13 PCIE_TXP1
MINI1_3D3V_S3
5V_S5
R289 0R2J-2-GP
MINI_5V_S5
NP1
NP2

3D3V_S3
L62 0R3J-0-U-GP
MINI1_3D3V_S3
C569 SC100P50V2JN-3GP
DY
PLT_RST1#_MINI1
R489 0R2J-2-GP
WLAN_EN 38
PLT_RST# 5,16,29,34,38,39,44
USBPN8_MINI
USBPP8_MINI
R491 0R2J-2-GP
R492 0R2J-2-GP
USBPN8 16
USBPP8 16
WLAN_LED# 1
WLAN_LED# 43
Q27
2N7002EW-1-GP
84.2N702.C3K
2ND = 84.2N702.B3K

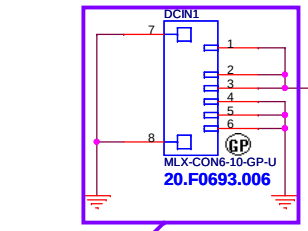
3D3V_S3
R221 10KR2J-3-GP
Q26
WAKE#
PCIE_WAKE# 14,29
2N7002EW-1-GP
84.2N702.C3K
2ND = 84.2N702.B3K

DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD CONN		
Size	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 35 of 56	

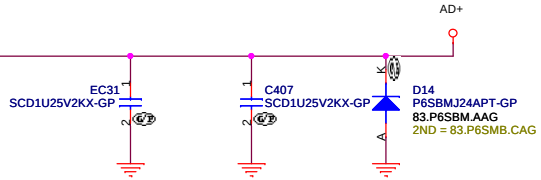
DC IN Connector

1 pin 1A



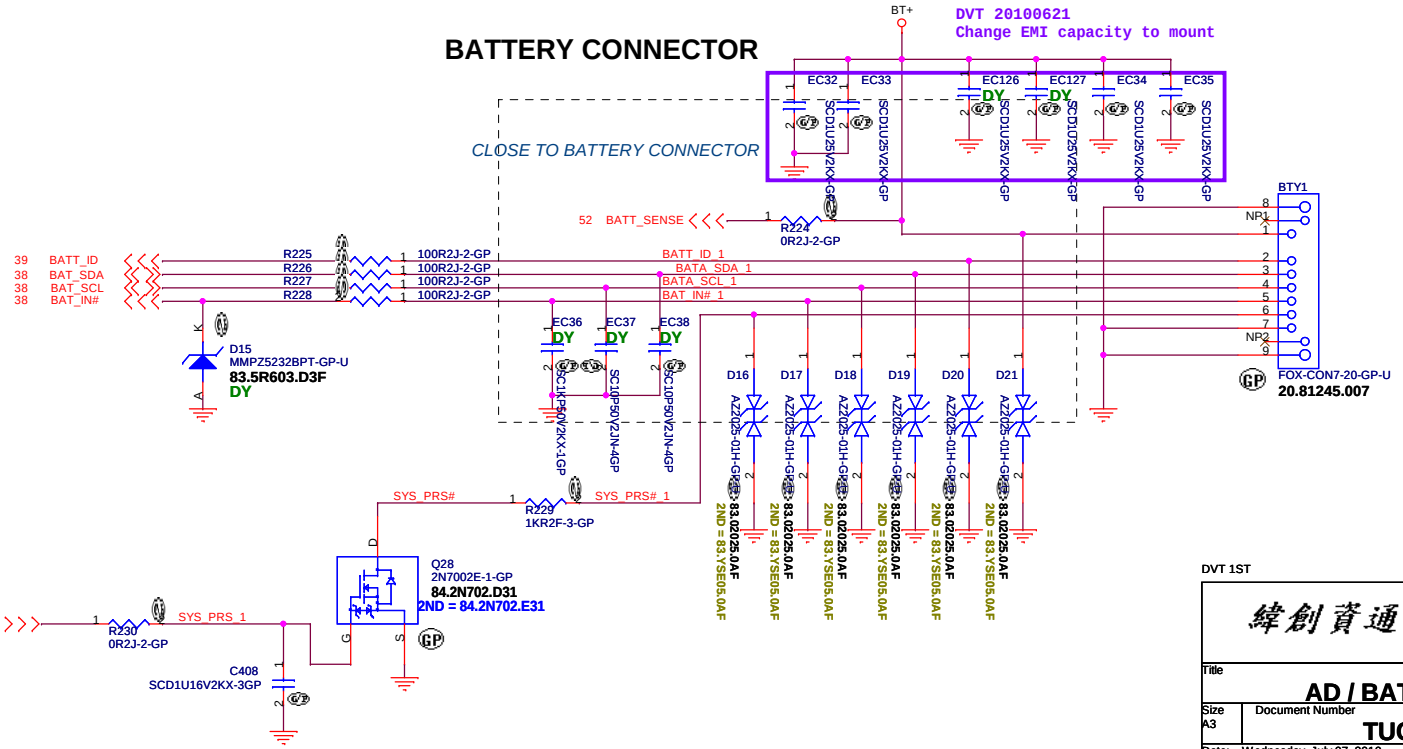
DVT 20100610
Change DCIN1 to 20.F0693.006
(follow connector list)

Adaptor in to generate DCBATOUT



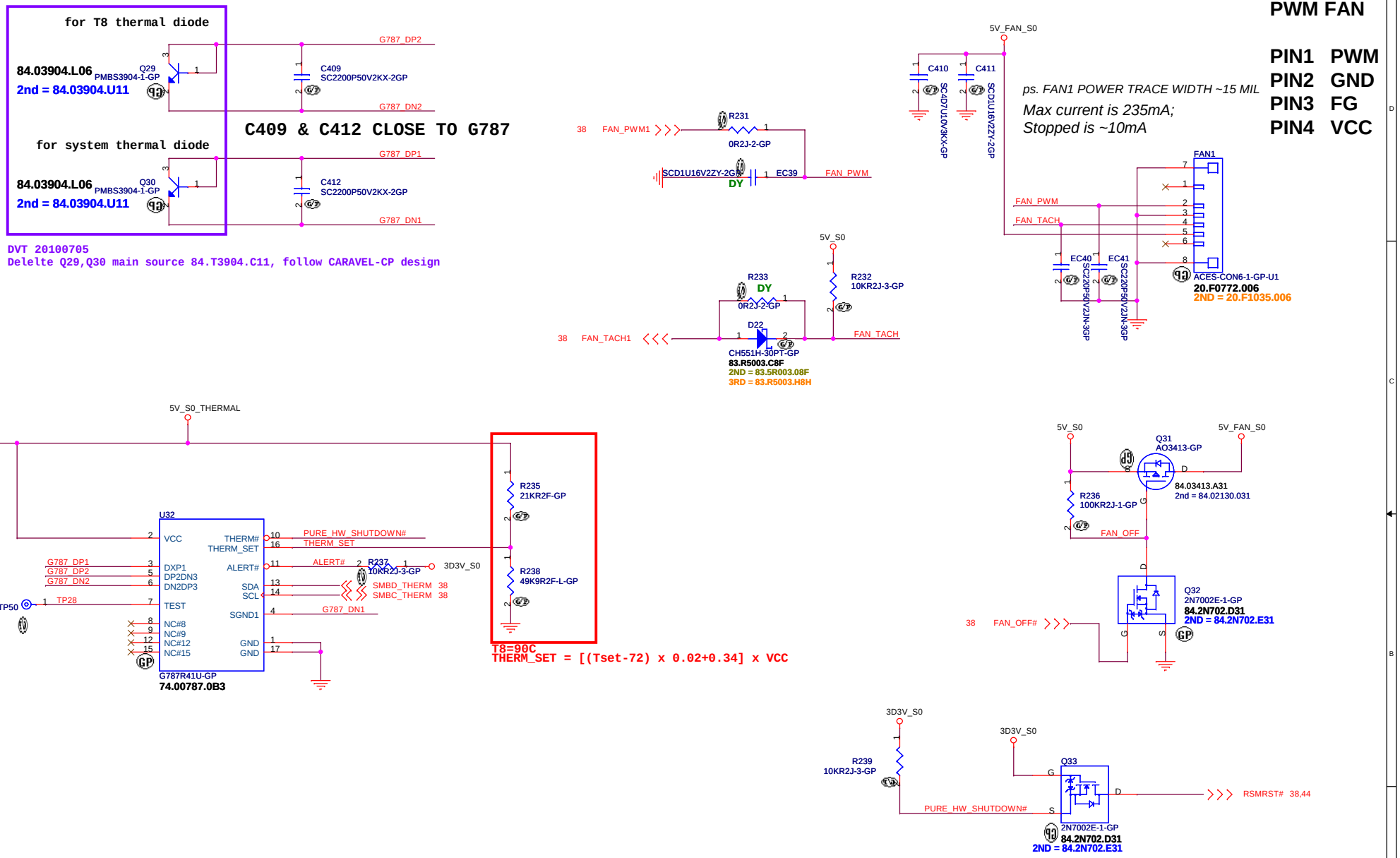
BATTERY CONNECTOR

DVT 20100621
Change EMI capacity to mount



DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AD / BATT CONN		
Size: A3	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 36 of 56	



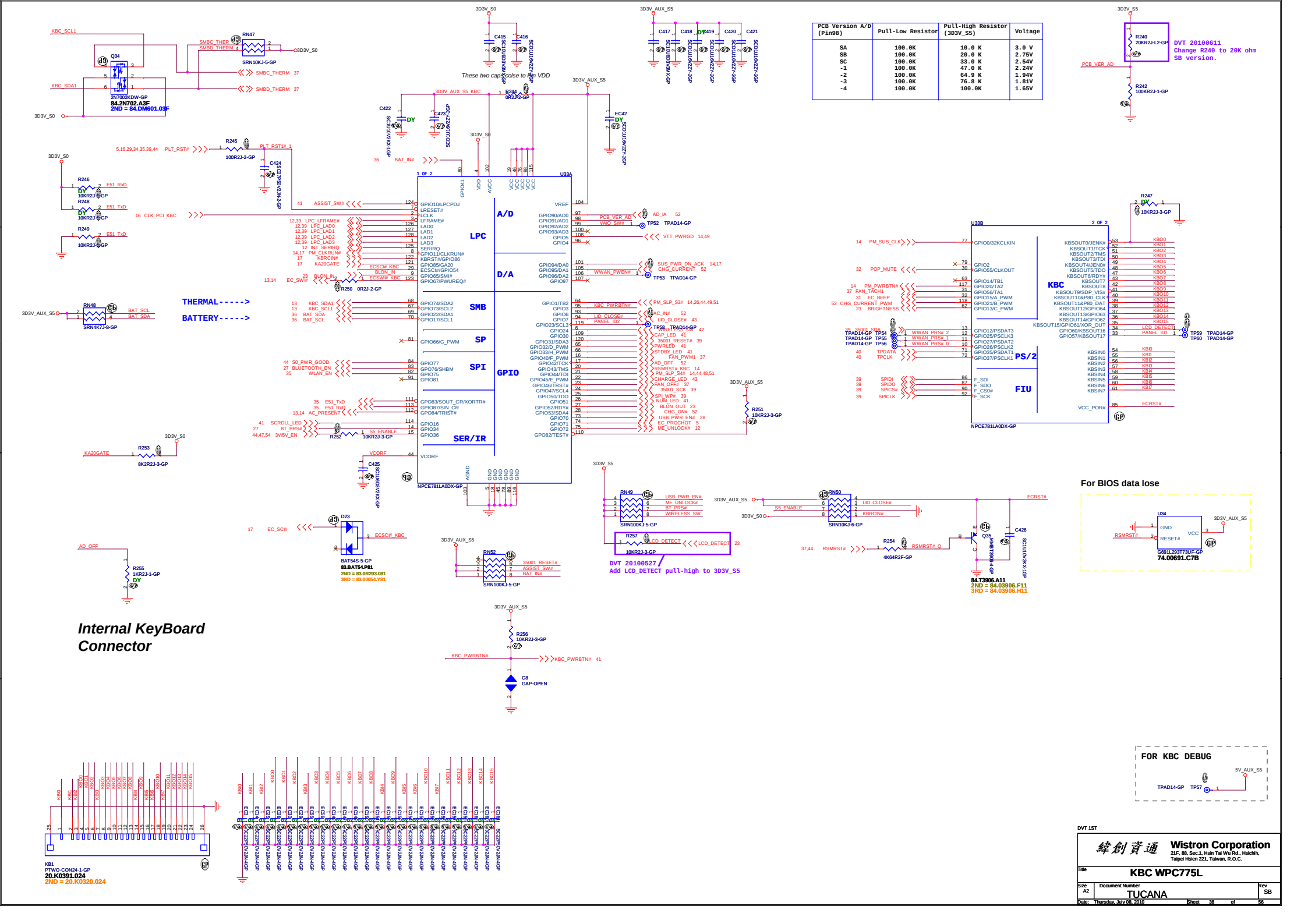
DVT 1ST

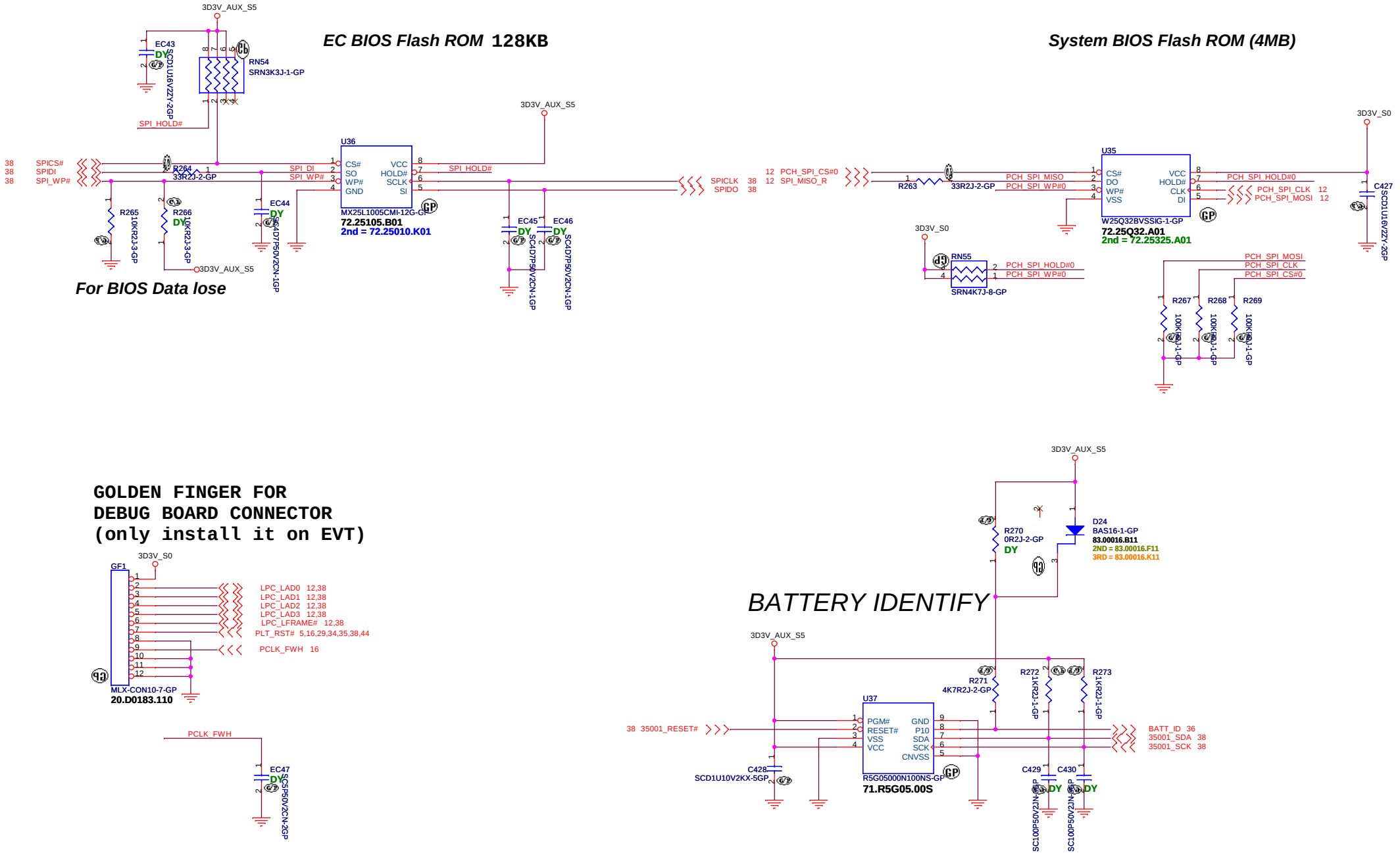
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor***

Size	Document Number	Rev
	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 37 of 56


PCB Version A/D (Pin98) | Pull-Low Resistor | Pull-High Resistor (3D3V_S5) | Voltage
SA | 100.0K | 10.0 K | 3.0 V
SB | 100.0K | 20.0 K | 2.75V
SC | 100.0K | 33.0 K | 2.54V
-1 | 100.0K | 47.0 K | 2.24V
-2 | 100.0K | 64.9 K | 1.94V
-3 | 100.0K | 76.8 K | 1.81V
-4 | 100.0K | 100.0K | 1.65V
These two caps close to Pin VDD
DVT 20100611
Change R240 to 20K ohm
SB version.
DVT 20100527
Add LCD_DETECT pull-high to 3D3V_S5
For BIOS data lose
THERMAL ----->
BATTERY ----->
A/D
D/A
SMB
SP
SPI
SER/IR
LPC
GPIO
KBC
PS/2
FIU
NPCE781LA0DX-GP
Internal KeyBoard Connector
FOR KBC DEBUG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775L
TUCANA
Thursday, July 08, 2010



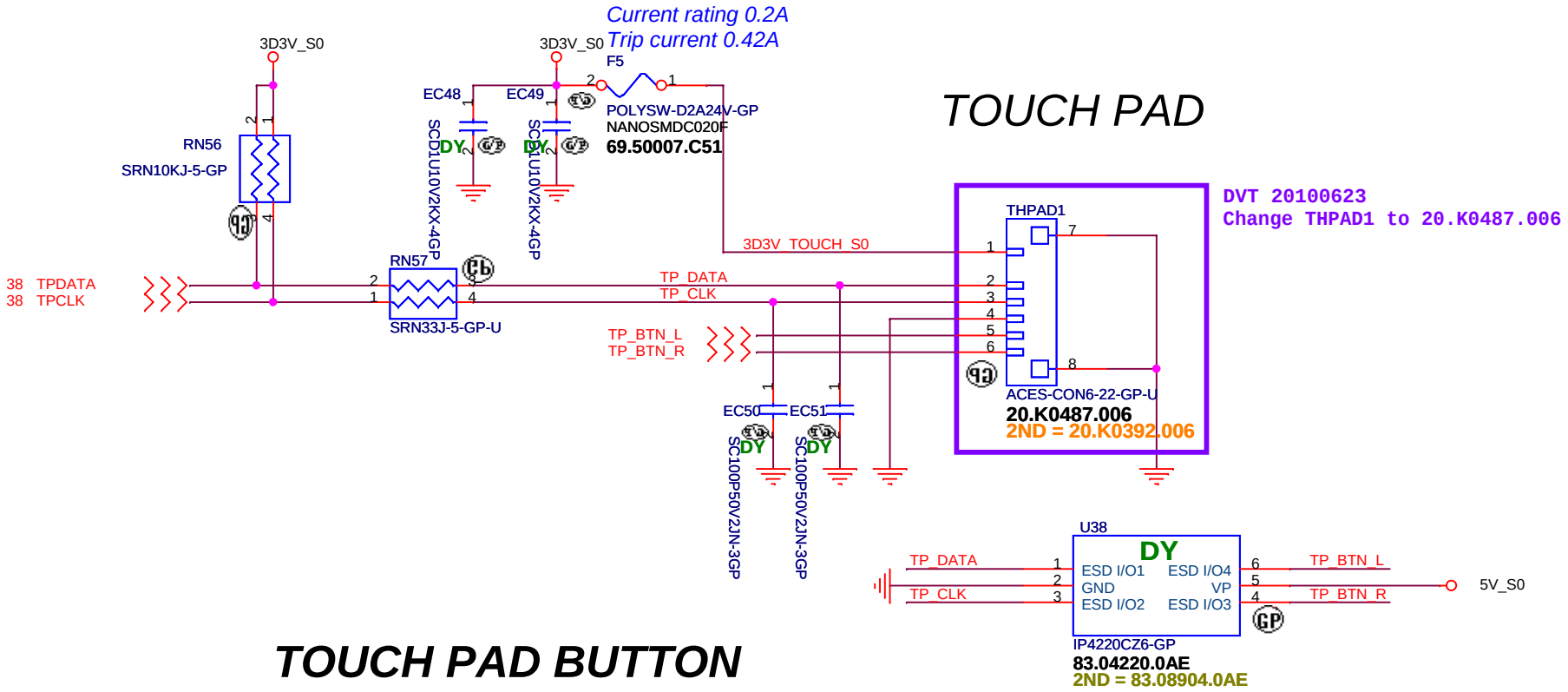
DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS & SW/C & BAT ID**

Size	Document Number	Rev
	TUCANA	SB

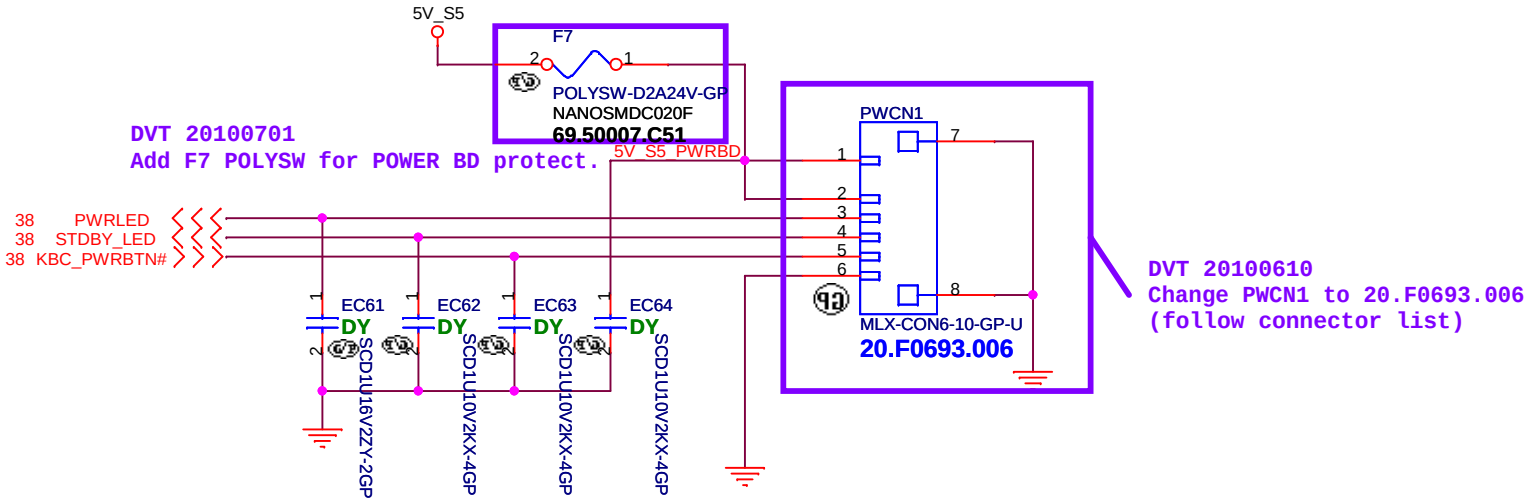
Date: Wednesday, July 07, 2010 Sheet 39 of 56



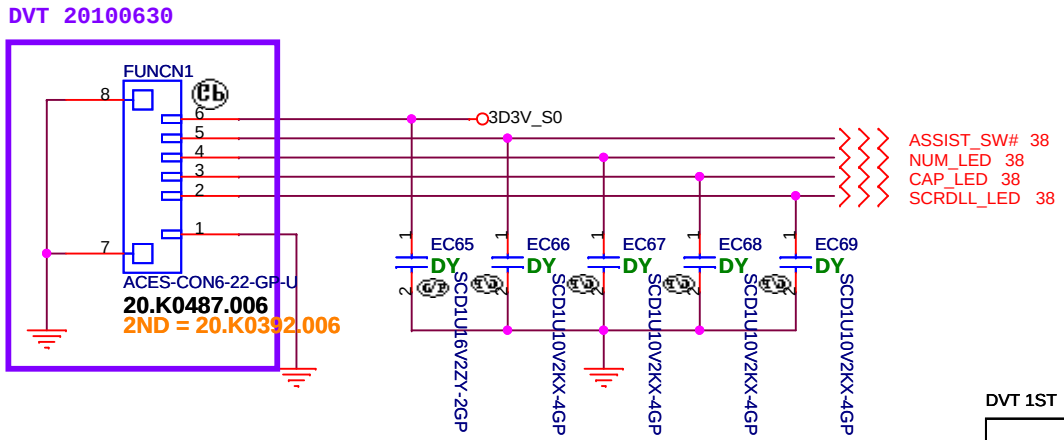
DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TouchPad		
Size: A4	Document Number: TUCANA	Rev: SB
Date: Wednesday, July 07, 2010	Sheet 40 of 56	

POWER BUTTON BD CONN



FUNCTION BD CONN

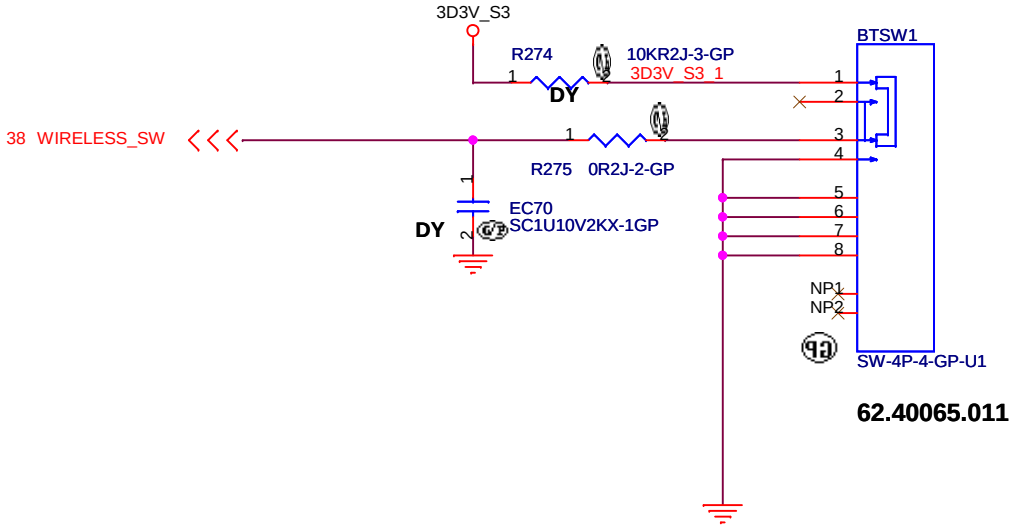


DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**FUNCTION BD & POWER BD**	
Size	Document Number: **TUCANA**	Rev: **SB**
Date: Wednesday, July 07, 2010	Sheet 41 of 56	

WLAN SWITCH



DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Switch*		
Size	Document Number: TUCANA	Rev: SB
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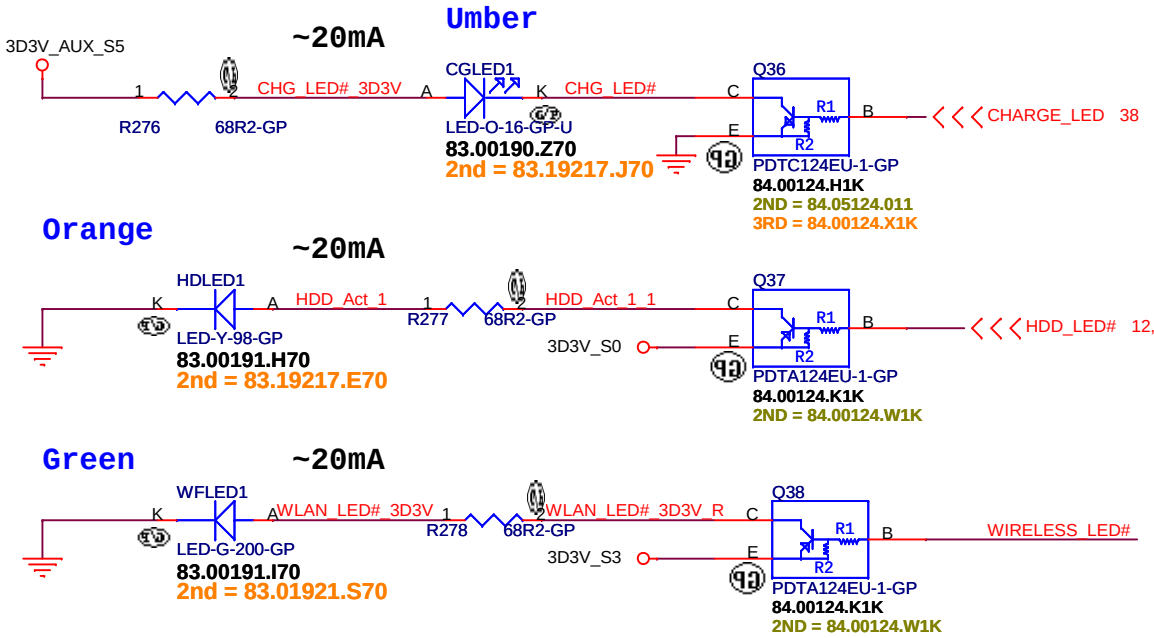
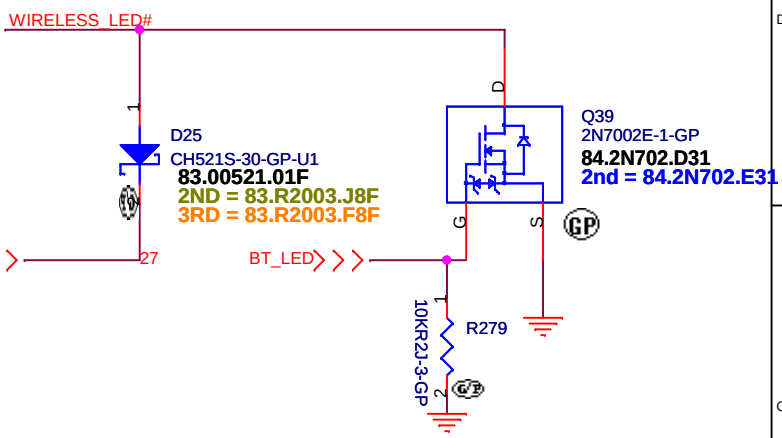
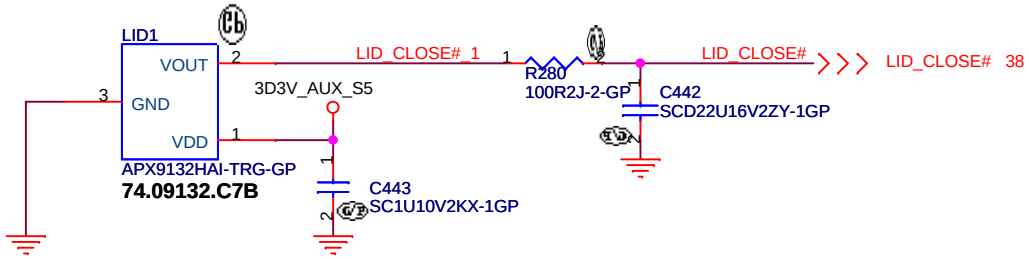
LED





active	High	Low
WWAN(W_DISABLE#)	ON	OFF
WLAN(WLAN_LED#)	OFF	ON
Bluetooth(BT_LED)	ON	OFF

Cover Up Switch



Common wireless SW(mechanical)	ON							
WLAN SW(software)	ON	OFF	ON	OFF	ON	OFF	ON	OFF
WWAN SW(software)	ON	ON	OFF	OFF	ON	ON	OFF	OFF
Bluetooth SW(software)	ON	ON	ON	ON	OFF	OFF	OFF	OFF
LED	TURN ON							OFF

DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Lid Switch & LED***

Size	Document Number	Rev
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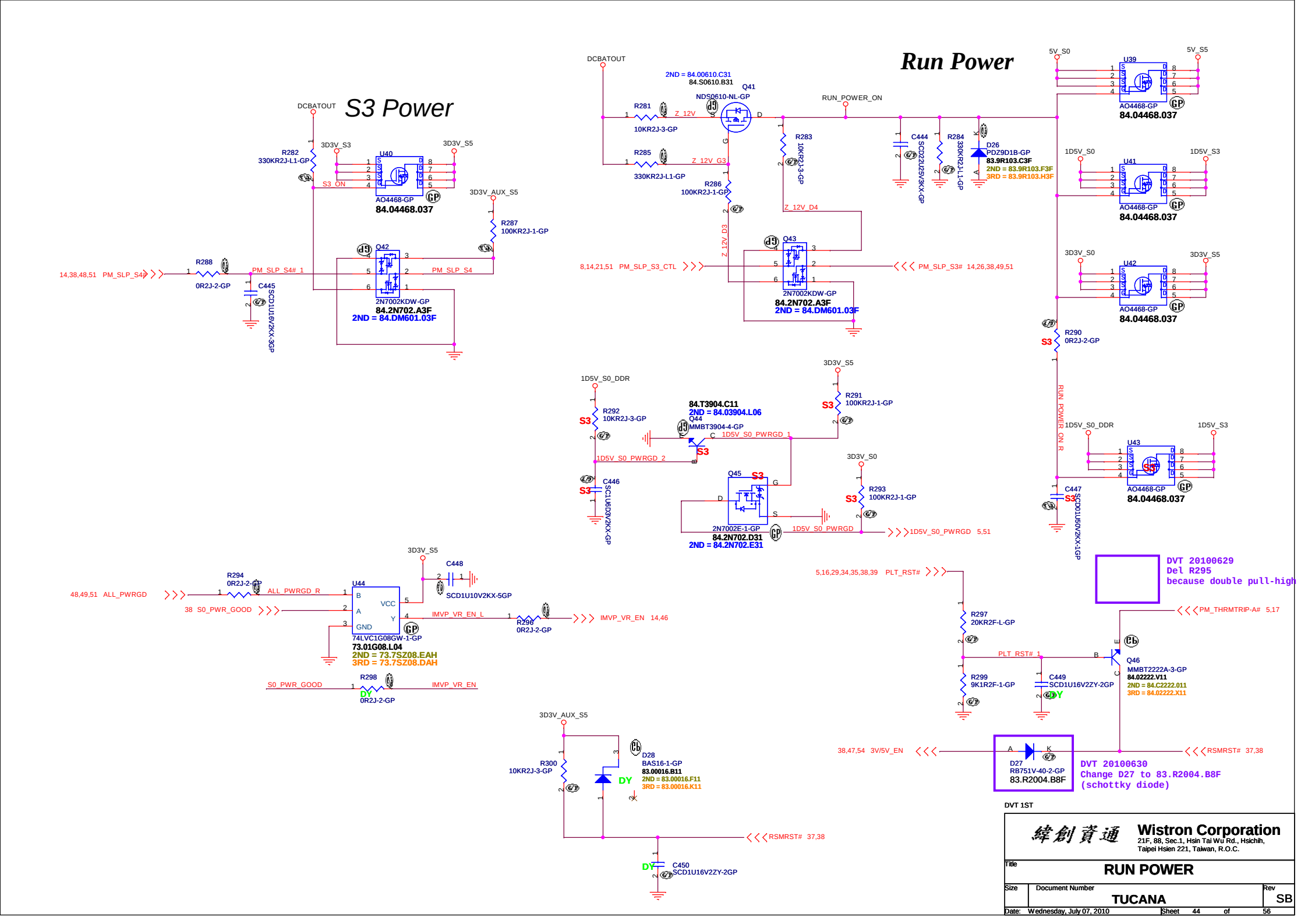
S3 Power
Run Power
DCBATOUT
R282
330KR2J-L1-GP
3D3V_S3
3D3V_S5
U40
S3_ON
AO4468-GP
84.04468.037
3D3V_AUX_S5
R287
100KR2J-1-GP
Q42
R288
0R2J-2-GP
14,38,48,51 PM_SLP_S4#
PM_SLP_S4# 1
PM_SLP_S4
C445
SCD1U16V2KX-3GP
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
2ND = 84.00610.C31
84.S0610.B31
Q41
NDS0610-NL-GP
R281
10KR2J-3-GP
Z_12V
R285
330KR2J-L1-GP
Z_12V_G3
R286
100KR2J-1-GP
Z_12V_D3
R283
10KR2J-3-GP
Z_12V_D4
RUN_POWER_ON
C444
SCD22U25V3KX-GP
R284
330KR2J-L1-GP
D26
PDZ9D1B-GP
83.9R103.C3F
2ND = 83.9R103.F3F
3RD = 83.9R103.H3F
Q43
8,14,21,51 PM_SLP_S3_CTL
PM_SLP_S3# 14,26,38,49,51
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
5V_S0
5V_S5
U39
AO4468-GP
84.04468.037
1D5V_S0
1D5V_S3
U41
AO4468-GP
84.04468.037
3D3V_S0
3D3V_S5
U42
AO4468-GP
84.04468.037
R290
0R2J-2-GP
S3
RUN_POWER_ON_R
1D5V_S0_DDR
1D5V_S3
U43
AO4468-GP
84.04468.037
C447
SCD01U50V2KX-1GP
1D5V_S0_DDR
R292
10KR2J-3-GP
84.T3904.C11
2ND = 84.03904.L06
Q44
MMBT3904-4-GP
1D5V_S0_PWRGD_1
1D5V_S0_PWRGD_2
C446
SC1U6D3V2KX-GP
3D3V_S5
R291
100KR2J-1-GP
Q45
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
3D3V_S0
R293
100KR2J-1-GP
1D5V_S0_PWRGD
1D5V_S0_PWRGD 5,51
48,49,51 ALL_PWRGD
R294
0R2J-2-GP
ALL_PWRGD_R
38 S0_PWR_GOOD
U44
74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.EAH
3RD = 73.7SZ08.DAH
3D3V_S5
C448
SCD1U10V2KX-5GP
IMVP_VR_EN_L
R296
0R2J-2-GP
IMVP_VR_EN 14,46
S0_PWR_GOOD
R298
DY
0R2J-2-GP
IMVP_VR_EN
5,16,29,34,35,38,39 PLT_RST#
R297
20KR2F-L-GP
PLT_RST# 1
R299
9K1R2F-1-GP
C449
SCD1U16V2ZY-2GP
Q46
MMBT2222A-3-GP
84.02222.V11
2ND = 84.C2222.011
3RD = 84.02222.X11
PM_THRMTRIP-A# 5,17
DVT 20100629
Del R295
because double pull-high
38,47,54 3V/5V_EN
D27
RB751V-40-2-GP
83.R2004.B8F
RSMRST# 37,38
DVT 20100630
Change D27 to 83.R2004.B8F
(schottky diode)
3D3V_AUX_S5
R300
10KR2J-3-GP
D28
BAS16-1-GP
83.00016.B11
2ND = 83.00016.F11
3RD = 83.00016.K11
RSMRST# 37,38
C450
SCD1U16V2ZY-2GP
DVT 1ST
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RUN POWER
Size
Document Number
TUCANA
Rev
SB
Date: Wednesday, July 07, 2010
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CPU_CORE
ADP3211

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6261A
5V_S0
3D3V_S0

- VID Setting
  - VID0(I / 3.3V)
  - VID1(I / 3.3V)
  - VID2(I / 3.3V)
  - VID3(I / 3.3V)
  - VID4(I / 3.3V)
  - VID5(I / 3.3V)
  - VID6(I / 3.3V)
- Input Signal
  - EN (I / 3.3V)
- Voltage Sense
  - VSEN(I / Vcore)
  - RGND(I / Vcore)
- Input Power
  - VCC(I)
  - VCC(I)
  - VCC(I)
- Output Signal
  - PGOOD
- Output Power
  - VCC_CORE_PWR(O)

VR_PWROK
VCC_CORE(Imax=27A)

RT8209 1D05V_S0

DCBATOUT_8202_1D05V
ALL_PWRGD

VIN
EN
1D5V(O)
PGOOD

1D05V_S0 (20A)
CPUCORE_ON

RT8209 1D5V_S3

DCBATOUT_8202_1D5V
PM_SLP_S4#

VIN
EN
1D5V(O)
PGOOD

1D5V_S3 (9.4A)
S3_PWRGD

GFX_CORE/ VGA_CORE
ADP3211

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT_3211

GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

- VID Setting
  - VID0(I / 3.3V)
  - VID1(I / 3.3V)
  - VID2(I / 3.3V)
  - VID3(I / 3.3V)
  - VID4(I / 3.3V)
- Input Power
  - VDD
  - VIN
- Input Signal
  - VR_ON
- Voltage Sense
  - VSEN(I / Vcore)
  - RGND(I / Vcore)
- Output Signal
  - PGOOD
- Output Power
  - VGFXCORE (O)

CPUCORE_ON
VCC_GFXCORE(11A)

RT9026 0D75V_S0

5V_S5
1D5V_S3
PM_SLP_S3#
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D75V_S3 (1.2A)
0D75V_S3_1

RT8015 1D8V_S0

3D3V_S5
PM_SLP_S3#

VDD
EN
VTT

1D8V_S0 (1.577A)

5V/3D3V
RT8223

DCBATOUT_51123
S5_ENABLE
ALW_PWRGD_3V_5V

- Input Power
  - VIN
- Input Signal
  - EN0
- Output Signal
  - PGOOD
- Output Power
  - 5V(O)
  - 3D3V(O)
  - 5V(O)
  - 3D3V(O)

5V_S5 (6A)
3D3V_S5 (5A)
5V_AUX_S5
3D3V_AUX_S5

Charger BQ24751

CHG_ON#
AD+

- Input Signal
  - CHGEN#
- Input Power
  - ACDET
- Output Signal
  - ACGOOD#
  - SRSET
  - BAT
- Output Power
  - VOUT (O)
  - VOUT (O)

AC_IN#
CHG_CURRENT
BATT_SENSE
BT+
DCBATOUT

Adapter

AD_OFF
AD_JK
5V_AUX_S5

- Input Signal
  - (I)
- Input Power
  - VCC(I)
  - VCC(I)
- Output Signal
  - (O)
- Output Power
  - VCC(O)

AD_IN#
AD+

DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence Logic

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DVT 20100701
Change OPEN-GAP to CLOSE-GAP

DVT 20100623

DVT 20100623

DVT 20100623

Id=24A
Qg=11nC
Rdson=9.6~13.4mohm

Id=50A
Qg=46nC
Rdson=2.3~3.6mohm

Mag. 0.36uH
DCR=1.05~1.2mohm
Idc=30A, Isat=60A

Iomax=27A
OCP>40.5A

Panasonic 330uF
2V, ESR=9mohm

64.64915.6DL

Intel support POC (power on current).

DVT 1ST			
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: ADP3211 CPU CORE			
Size	Document Number: TUCANA		Rev: SB
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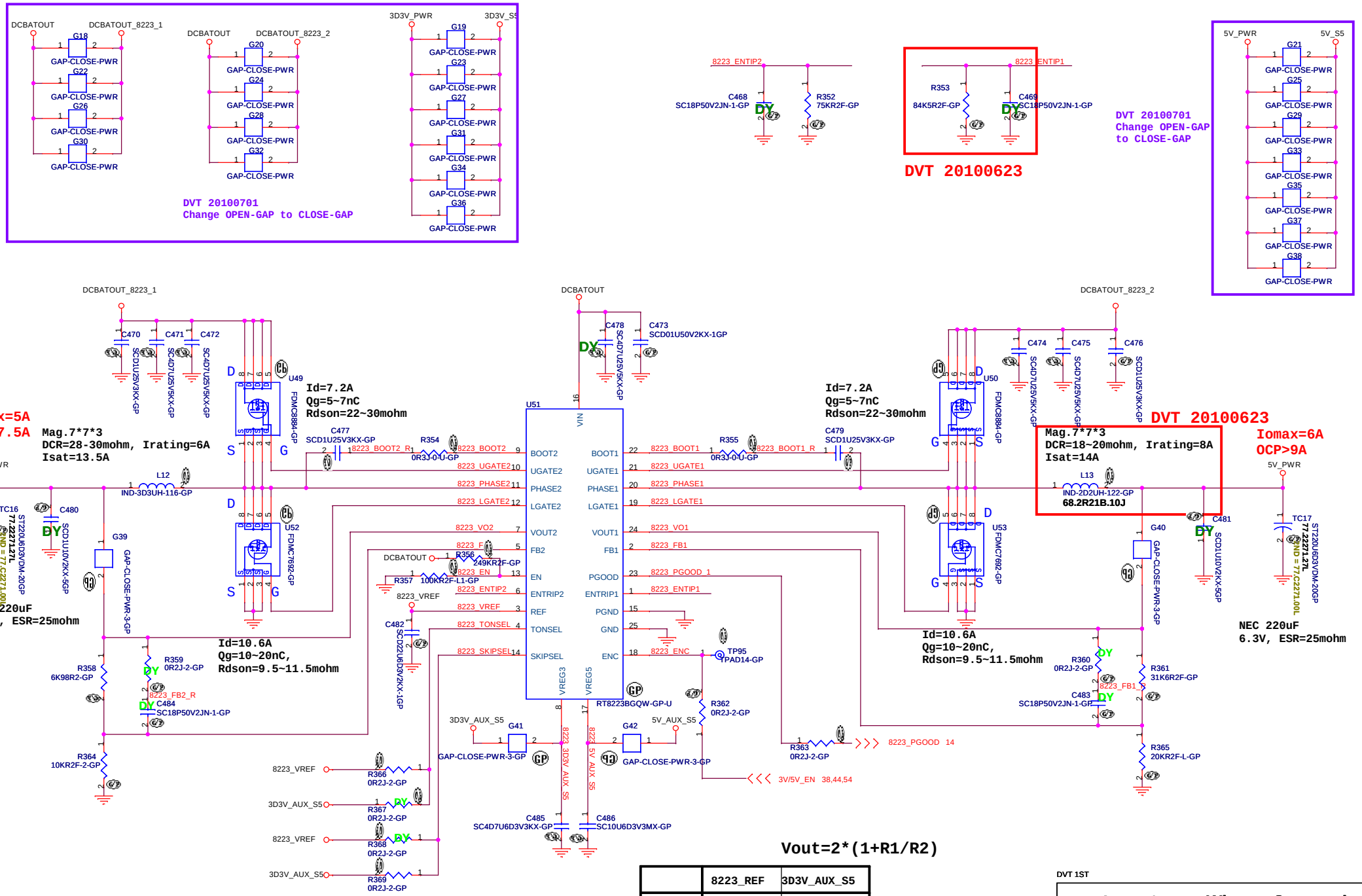
DCBATOUT
DCBATOUT_8223_1
DCBATOUT_8223_2
3D3V_PWR
3D3V_S5
5V_PWR
5V_S5
GAP-CLOSE-PWR
DVT 20100701
Change OPEN-GAP to CLOSE-GAP
8223_ENTIP2
8223_ENTIP1
C468
SC18P50V2JN-1-GP
R352
75KR2F-GP
R353
84K5R2F-GP
C469
DVT 20100623
U49
U50
U51
U52
U53
FDMC8884-GP
FDMC7692-GP
Id=7.2A
Qg=5~7nC
Rdson=22~30mohm
Iomax=5A
OCP>7.5A
Mag.7*7*3
DCR=28-30mohm, Irating=6A
Isat=13.5A
Iomax=6A
OCP>9A
Mag.7*7*3
DCR=18~20mohm, Irating=8A
Isat=14A
L12
IND-3D3UH-116-GP
L13
IND-2D2UH-122-GP
68.2R21B.10J
RT8223BGQW-GP-U
VIN
BOOT2
UGATE2
PHASE2
LGATE2
VOUT2
FB2
EN
ENTRIP2
REF
TONSEL
SKIPSEL
VREG3
BOOT1
UGATE1
PHASE1
LGATE1
VOUT1
FB1
PGOOD
ENTRIP1
PGND
GND
ENC
VREG5
8223_BOOT2
8223_UGATE2
8223_PHASE2
8223_LGATE2
8223_VO2
8223_FB2
8223_EN
8223_ENTIP2
8223_VREF
8223_TONSEL
8223_SKIPSEL
8223_BOOT1
8223_UGATE1
8223_PHASE1
8223_LGATE1
8223_VO1
8223_FB1
8223_PGOOD_1
8223_ENTIP1
8223_ENC
8223_PGOOD 14
3V/5V_EN 38,44,54
3D3V_AUX_S5
5V_AUX_S5
NEC 220uF
6.3V, ESR=25mohm
Id=10.6A
Qg=10~20nC,
Rdson=9.5~11.5mohm
Vout=2*(1+R1/R2)
8223_REF
3D3V_AUX_S5
SKIPSEL
PWM
00A AUTOSKIP
TONSEL
245k/CH1
305k/CH2
300k/CH1
375k/CH2
DVT 1ST
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
RT8223_5V/3D3V
TUCANA
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RT8209 for 1D5V

DVT 20100701
Change OPEN-GAP to
CLOSE-GAP

DCBATOUT
DCBATOUT_8209_1D5V
G47 GAP-CLOSE-PWR
G49 GAP-CLOSE-PWR
G51 GAP-CLOSE-PWR
G53 GAP-CLOSE-PWR
TC28 DY ST15U25VDM-1-GP
77.21561.00L
2ND = 77.C1561.03L

DVT 20100701
Change OPEN-GAP to
CLOSE-GAP

1D5V_PWR
1D5V_S3
G43 GAP-CLOSE-PWR
G44 GAP-CLOSE-PWR
G45 GAP-CLOSE-PWR
G46 GAP-CLOSE-PWR
G48 GAP-CLOSE-PWR
G50 GAP-CLOSE-PWR
G52 GAP-CLOSE-PWR
G54 GAP-CLOSE-PWR
G55 GAP-CLOSE-PWR
G56 GAP-CLOSE-PWR

5V_S5
C487 SC1U10V2KX-1GP
R370 2D2R3-1-U-GP
8209_1D5_V5FILT
C491 SC1U10V2KX-1GP
R371 0R3J-0-U-GP
8209_1D5_PHASE_1
C492 SCD1U25V3KX-GP
R372 0R3J-0-U-GP
8209_1D5_UGATE_R

U55
VDD
VDDP
FB
BOOT
UGATE
LGATE
PHASE
VOUT
PGOOD
GND
PGND
NC#15
EN/DEM
TON
CS
RT8209EGQW-GP

8209_1D5_UGATE
8209_1D5_LGATE
8209_1D5_PHASE
8209_1D5_PGOOD
8209_1D5_FB
8209_1D5_BOOT
8209_1D5_EN
8209_1D5_TON
8209_1D5_CS

1D5V_PWR
3D3V_S0
R378 10KR2F-2-GP
R379 0R2J-2-GP
ALL_PWRGD 44,49,51

14,38,44,51 PM_SLP_S4#
R374 0R2J-2-GP
R373 249KR2F-GP
R376 100KR2F-L1-GP
C495 DY SCD1U10V2KX-5GP
R377 7K5R2F-1-GP

DVT 20100623

DCBATOUT_8209_1D5V
U54 SI7686DP-T1-GE3-GP
84.07686.A37
C488 SC4D7U25V5KX-GP
C489 SC4D7U25V5KX-GP
C490 SCD1U25V3KX-GP

Id=14.3A
Qg=9.2~14nC
Rdson=11~14mohm

Mag. 1.0uH
DCR=2.9~3.3mohm
Idc=18A, Isat=36A

Iomax=9.4A
OCP>14.1A

L14 IND-1UH-93-GP
68.1R01B.10J
20100401

1D5V_PWR
C493 DY SC33P50V2JN-3GP
C494 SCD1U10V2KX-5GP
TC18 2ND = 77.23371.31L
80.3371V.A2L
ST330U2D5VBM-1-GP
Panasonic 220uF
2V, ESR=9mohm

U56 SIR460DP-T1-GE3-GP
84.00460.037
R375 31K6R2F-GP
R380 30KR2F-GP
8209_1D5_FB

20100331

Id=19.4A
Qg=16.8~25.5nC,
Rdson=4.9~6.1mohm

20100331

Vout=0.75*(1+R1/R2)

DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209_1D5V
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RT8209 1D05V

DCBATOUT
DCBATOUT_RT8209_1D05V
G57 GAP-CLOSE-PWR
G58 GAP-CLOSE-PWR
G60 GAP-CLOSE-PWR
G62 GAP-CLOSE-PWR
TC19 ST15U25VDM-1-GP
DY
77.21561.00L
2ND = 77.C1561.03L

DVT 20100701
Change OPEN-GAP to
CLOSE-GAP

DVT 20100701
Change OPEN-GAP to
CLOSE-GAP

1D05V_PWR
1D05V_S0
G59 GAP-CLOSE-PWR
G61 GAP-CLOSE-PWR
G63 GAP-CLOSE-PWR
G64 GAP-CLOSE-PWR
G65 GAP-CLOSE-PWR
G66 GAP-CLOSE-PWR
G67 GAP-CLOSE-PWR
G68 GAP-CLOSE-PWR
G69 GAP-CLOSE-PWR
G70 GAP-CLOSE-PWR
G71 GAP-CLOSE-PWR
G72 GAP-CLOSE-PWR
G73 GAP-CLOSE-PWR
G74 GAP-CLOSE-PWR
G75 GAP-CLOSE-PWR
G76 GAP-CLOSE-PWR
G77 GAP-CLOSE-PWR
G78 GAP-CLOSE-PWR
G79 GAP-CLOSE-PWR
G80 GAP-CLOSE-PWR

DCBATOUT_RT8209_1D05V
U57 SI7686DP-T1-GE3-GP
84.07686.A37
C496 SC4D7U25V5KX-GP
C497 SC4D7U25V5KX-GP
C498 SC4D7U25V5KX-GP
C499 SCD1U25V3KX-GP

Id=24A
Qg=11nC
Rdson=9.4~13.5mohm

DVT 20100622
Mag. 0.56uH
DCR=1.6~1.8mohm
Idc=25A, Isat=40A

Iomax=20A
OCP>30A

20100428

5V_S5
C500 SC1U10V2KX-1GP
C503 SC1U10V2KX-1GP
R382 2D2R3-1-U-GP
8209_1D05_V5FILT
R383 0R3J-0-U-GP
8209_1D05_BOOT
8209_1D05_BOOT_1
C501 SCD1U25V3KX-GP
R381 0R3J-0-U-GP
8209_1D05_UGATE_R
L15 IND-D56UH-27-GP
68.R5610.10P
1D05V_PWR
C502 SC18P50V2JN-1-GP
DY
TC21 ST330U2D5VBM-1-GP
80.337V1.A2L
2ND = 77.23371.31L
TC20 ST330U2D5VBM-1-GP
80.337V1.A2L
2ND = 77.23371.31L
R384 10KR2F-2-GP
R385 24KR2F-GP
8209_1D05_FB

U59
VDD
VDDP
FB
BOOT
EN/DEM
TON
CS
UGATE
LGATE
PHASE
VOUT
PGOOD
GND
PGND
NC#15
RT8209EGQW-GP
74.08209.B73

8209_1D05_UGATE
8209_1D05_LGATE
8209_1D05_PHASE
8209_1D05_FB
8209_1D05_EN
8209_1D05_TON
8209_1D05_CS
1D05V_PWR
VTT_PWRGD 14,38

44,48,51 ALL_PWRGD
R386 0R2J-2-GP
R387 200KR2F-L-GP
R388 100KR2F-L1-GP
R389 14K3R2F-GP
DVT 20100623

Id=50A
Qg=46nC,
Rdson=2.3~3.6mohm

U58 SIR164DP-T1-GE3-GP
84.00164.037

Vout=0.75*(1+R1/R2)

8209_1D05_FB
R390 0R2J-2-GP
DY
VTT_SENSE 7

The processor needs to be warned about the VTT rails shutdown at least 100 ns before the VTT rail falls to -5% of nominal value.

3D3V_S5
R391 10KR2J-3-GP
Q47 2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
VTT_PWRGD
H_VTTPWRGD_R
3D3V_S5
R392 100KR2J-1-GP
1D05V_S0
R394 1KR2J-1-GP
H_VTTPWRGD 5

3D3V_S5
R393 100KR2J-1-GP
DY
Q48 2N7002KDW-GP
H_VTTPWRGD
H_VTTPWRGD_1
PM_SLP_S3# 14,26,38,44,51
DY
84.2N702.A3F
2ND = 84.DM601.03F

DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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DVT 20100701
Change OPEN-GAP to
CLOSE-GAP

DCBATOUT
DCBATOUT_3211_GFX
G81 GAP-CLOSE-PWR
G82 GAP-CLOSE-PWR
G83 GAP-CLOSE-PWR
G84 GAP-CLOSE-PWR
G85 GAP-CLOSE-PWR
G86 GAP-CLOSE-PWR
TC22 ST15U25VDM-1-GP
DY
77.21561.00L
2ND = 77.C1561.03L

8 GFX_VID[6..0]
GFX_VID6 R395 0R2J-2-GP GFX_R_VID6
GFX_VID5 R396 0R2J-2-GP GFX_R_VID5
GFX_VID4 R397 0R2J-2-GP GFX_R_VID4
GFX_VID3 R398 0R2J-2-GP GFX_R_VID3
GFX_VID2 R399 0R2J-2-GP GFX_R_VID2
GFX_VID1 R401 0R2J-2-GP GFX_R_VID1
GFX_VID0 R402 0R2J-2-GP GFX_R_VID0
8 GFX_VR_EN R403 0R2J-2-GP GFX_IMVP_VR_EN
R405 470R2F-GP
3D3V_S5 R404 10KR2J-3-GP GFX_PWRGD
8 GFX_IMON R406 0R2J-2-GP
R407 8K66R2D-GP
C509 SCD056U16V2KX-GP

U61
ADP3211MNR2G-GP
74.03211.033
EN VID0 VID1 VID2 VID3 VID4 VID5 VID6
PWRGD IMON CLKEN# FBRTN FB COMP GPU ILIM
VCC BST DRVH SW PVCC DRVL PGND GND
IREF RPM RT RAMP LLINE CSREF CSRTN CSCOMP

GFX_PWRGD
GFX_FBRTN
GFX_FB
GFX_COMP
GFX_ILIM
GFX_CSCOMP
GFX_IREF
GFX_RPM
GFX_RT
GFX_RAMP
GFX_CSREF
GFX_CSRTN
GFX_CSCOMP

5V_S5 R409 6K65R2F-GP
C511 SC220P50V2JN-3GP
C512 SC1P5V2JN-3GP
R410 1KR2F-1-GP
C514 SC470P50V2KX-3GP
R411 20KR2F-1-GP
R412 80K6R2F-GP
R413 160KR2F-GP
R414 261KR2F-GP
GFX_AGND

DCBATOUT_3211_GFX
R415 1KR2F-3-GP
GFX_RAMP_1
R416 422KR2F-1-GP
C516 SC1KP50V2KX-1GP
C515 SC1KP50V2KX-1GP

R417 71K5R2F-1-GP
GFX_CSCOMP_1
R418 165KR2F-GP
R419 56K2R3F-GP
GFX_SW_L
R420 NTC-220K-5-GP
C517 SC82P50V2KX-1GP
C518 SC1KP50V2KX-1GP
C519 SC1KP50V2KX-1GP

R421 100R2F-L1-GP-U
VCC_GFXCORE
R422 0R2J-2-GP
VCC_AXG_SENSE 8
R423 0R2J-2-GP
VSS_AXG_SENSE 8
R424 100R2F-L1-GP-U

G89 GAP-CLOSE-PWR-3-GP

5V_S5
R400 10R3F-GP
C507 SC1U10V2KX-1GP
GFX_AGND

R408 1R3J-L1-GP
GFX_BST_1
C510 SCD22U16V3KX-2-GP
C513 SC3D3U10V5KX-2GP

DCBATOUT_3211_GFX
U60 SI7686DP-T1-GE3-GP
U62 SI7164DP-T1-GE3-GP
C508 SC4D7U25V5KX-GP
C504 SC4D7U25V5KX-GP
C505 SC4D7U25V5KX-GP
C506 SCD1U25V2KX-3GP

Id=14.3A
Qg=9.2~14nC
Rdson=11~14mohm
Mag. 0.56uH
DCR=1.6~1.8mohm
Idc=25A, Isat=40A
Iomax=12A
OCP>18A

Id=26.5A
Qg=40.6~61nC
Rdson=2.6~3.2mohm

L16 IND-D56UH-27-GP
VCC_GFXCORE
G87 GAP-CLOSE-PWR-3-GP
G88 GAP-CLOSE-PWR-3-GP
C23 ST330U2D5VBM-1-GP
C24 80.33371V.A2L
C26 ST330U2D5VBM-1-GP
Panasonic 330uF
2V, ESR=9mohm

DVT 20100623
DVT 20100623

DVT 1ST

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Title: ADP3211_GFX_CORE
Size: A2 | Document Number: TUCANA | Rev: SB
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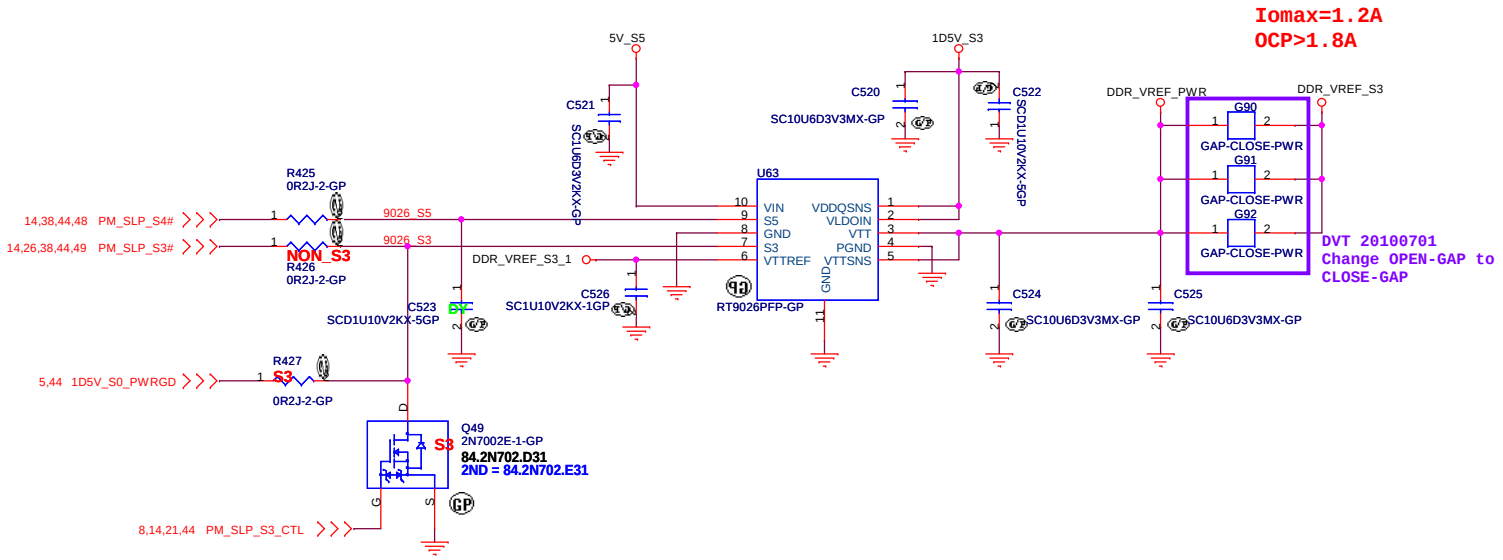
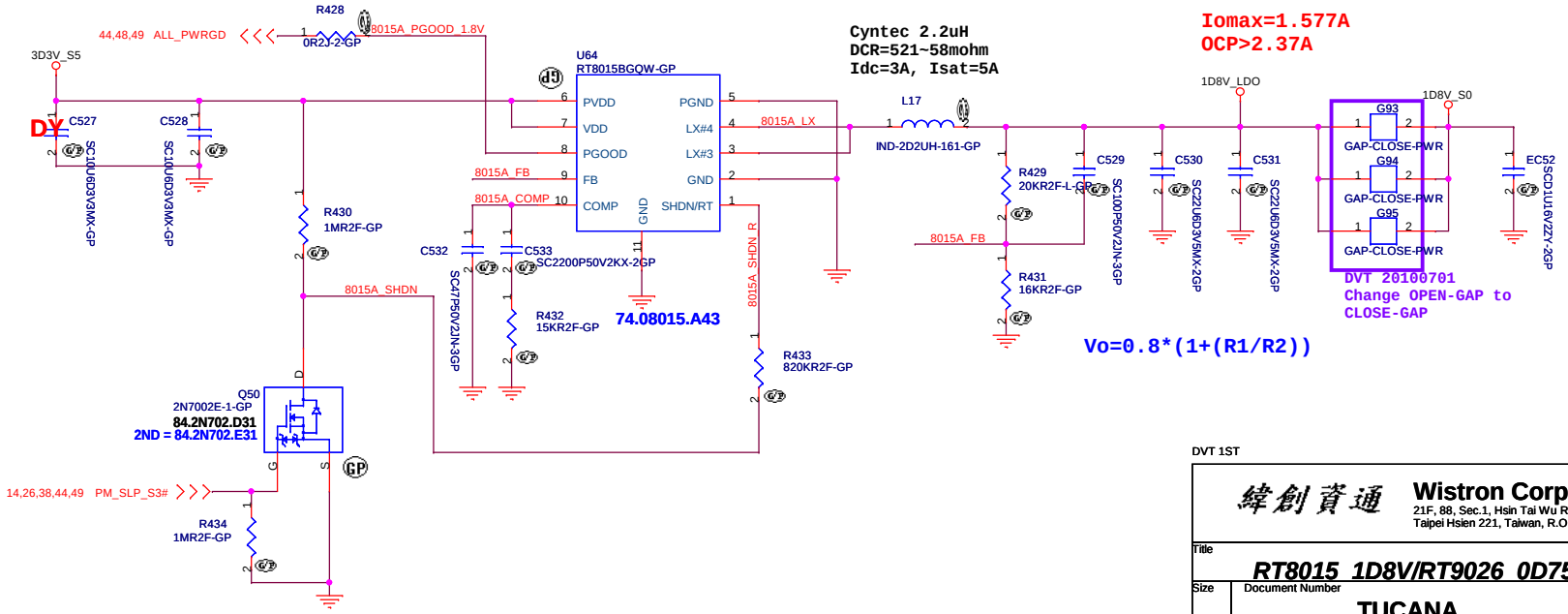
RT9026 for 0D75V_S3



RT8015 for 1D8V_S0



DVT 1ST

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***RT8015_1D8V/RT9026_0D75***	
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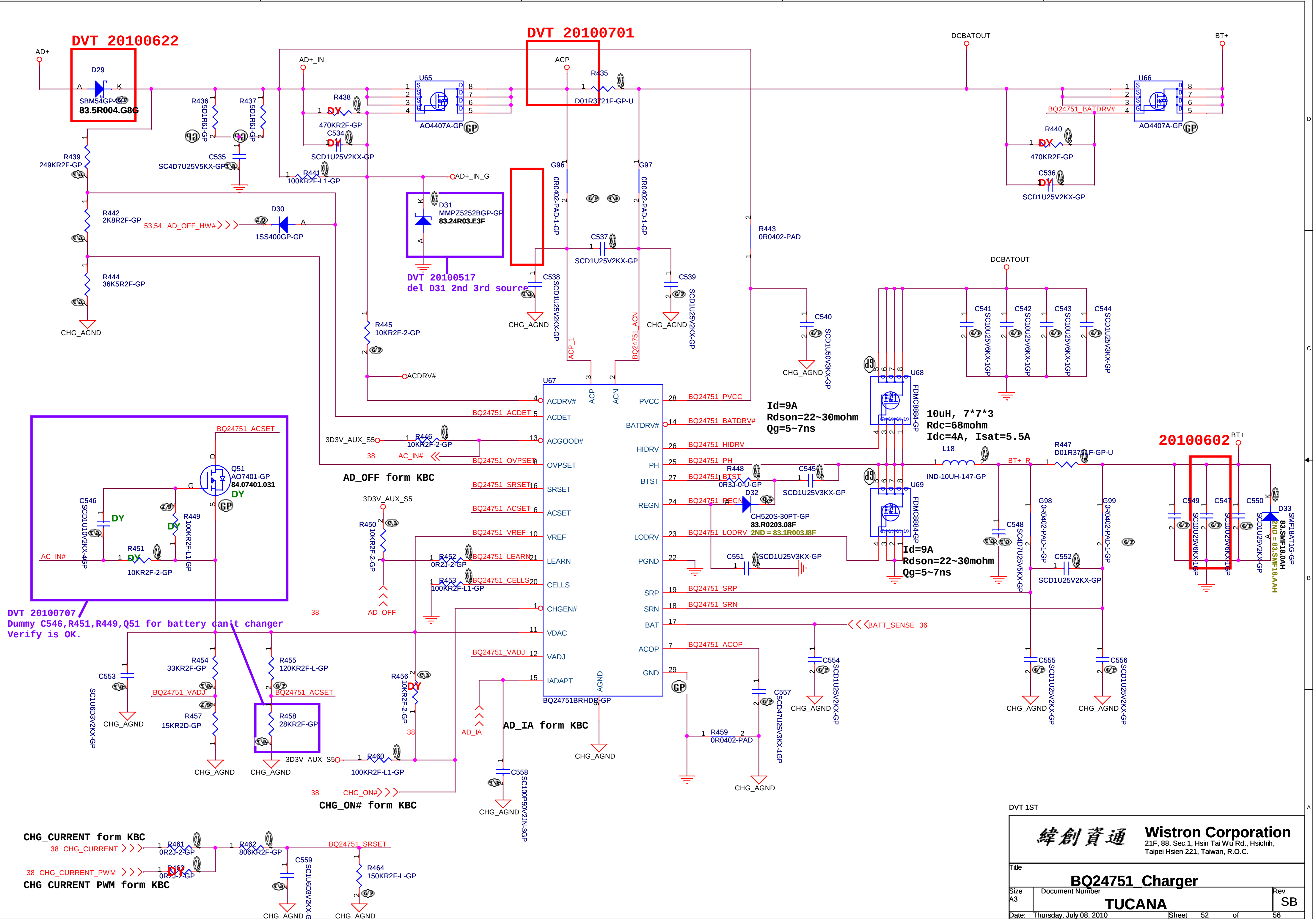


DVT 1ST

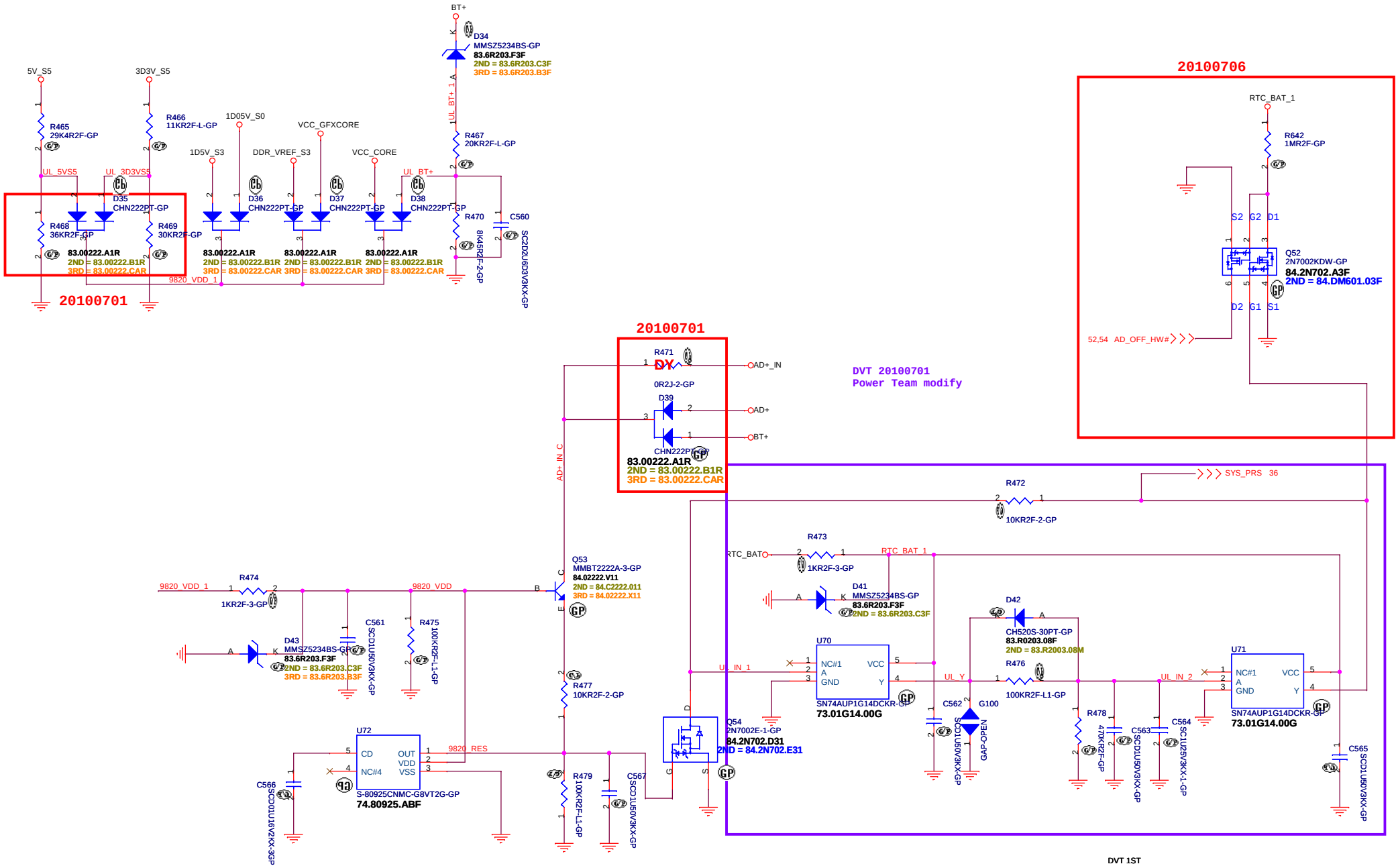
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: BQ24751_Charger

Size: A3 | Document Number: TUCANA | Rev: SB

Date: Thursday, July 08, 2010 | Sheet 52 of 56



DVT 1ST

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**UL circuit**
Size A3	Document Number **TUCANA** Rev SB
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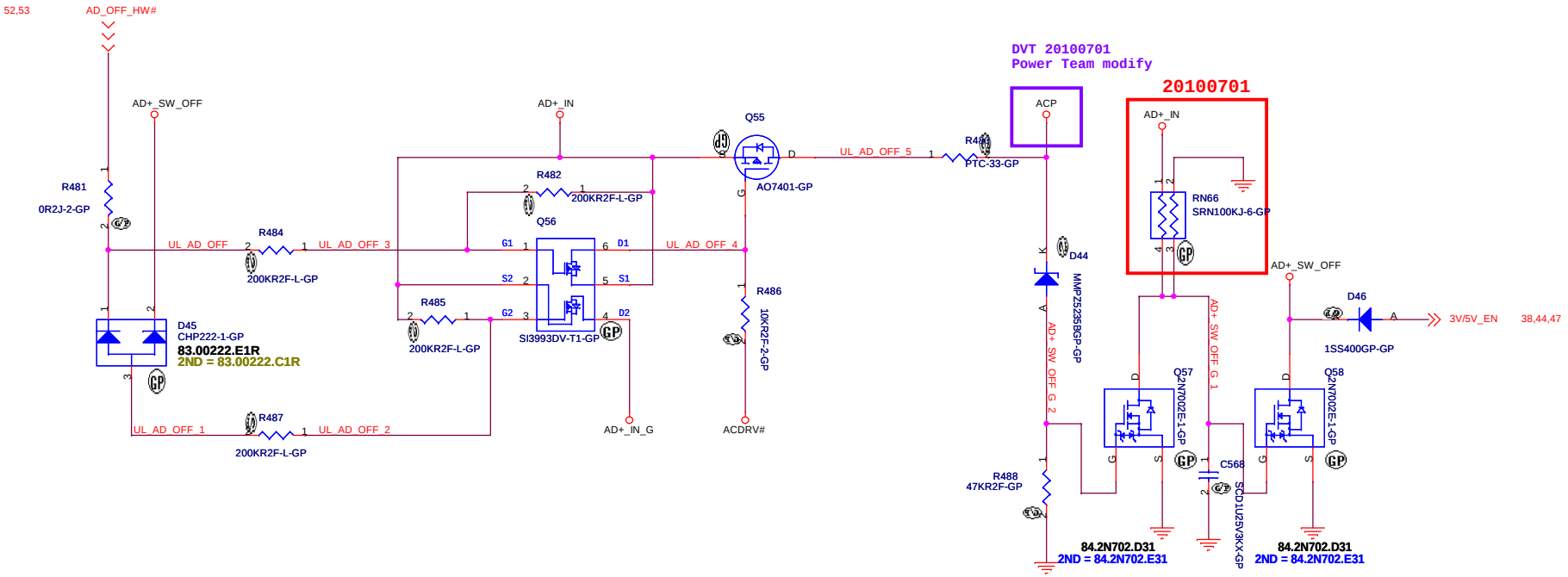

DVT 1ST

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Taipei Hsien 221, Taiwan, R.O.C.

Title: UVP Protect

Size: A3 | Document Number: TUCANA | Rev: SB

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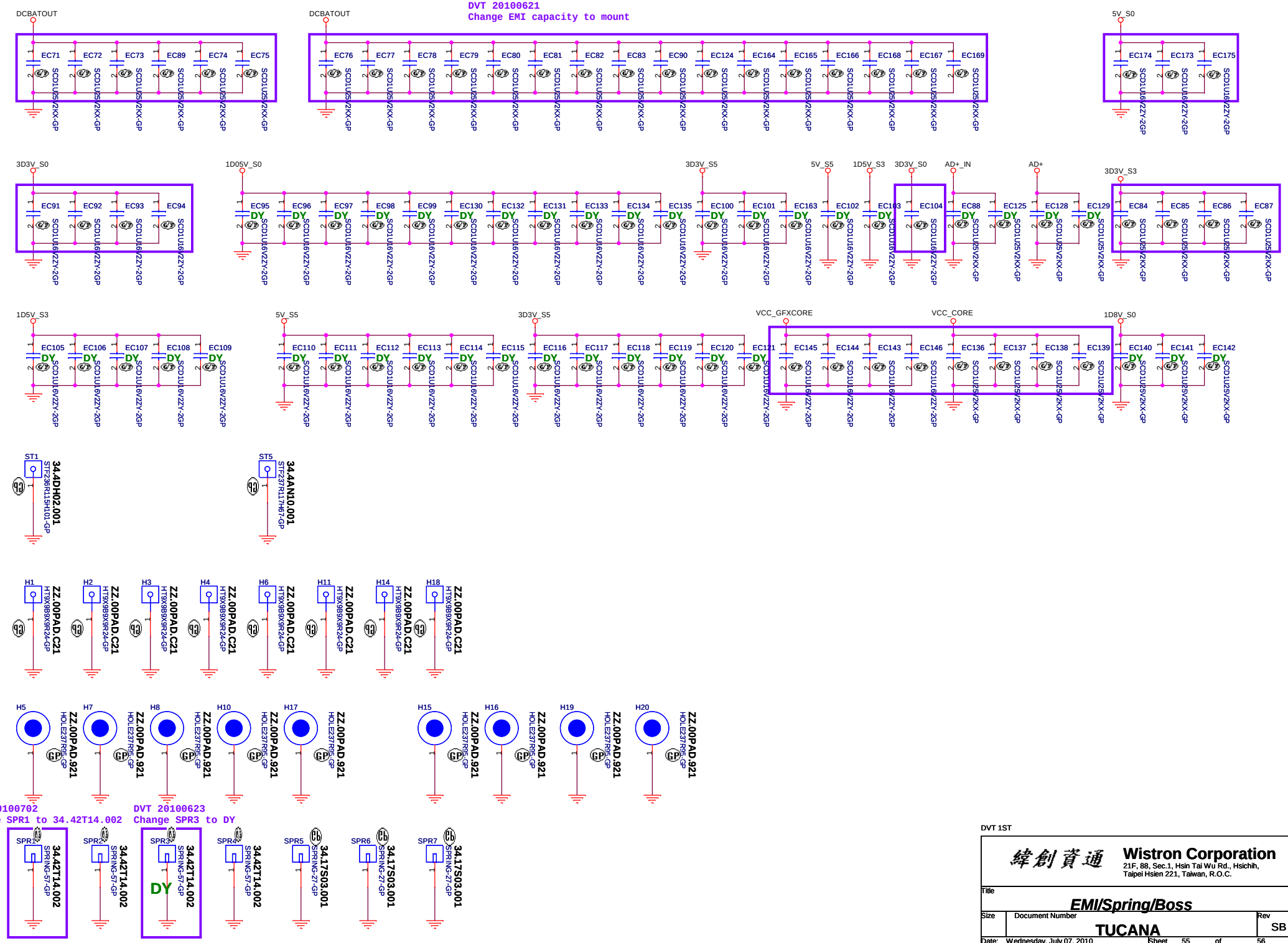
DVT 20100621
Change EMI capacity to mount
DCBATOUT
EC71 EC72 EC73 EC89 EC74 EC75
DCBATOUT
EC76 EC77 EC78 EC79 EC80 EC81 EC82 EC83 EC90 EC124 EC164 EC165 EC166 EC168 EC167 EC169
5V_S0
EC174 EC173 EC175
3D3V_S0
EC91 EC92 EC93 EC94
1D05V_S0
EC95 EC96 EC97 EC98 EC99 EC130 EC132 EC131 EC133 EC134 EC135
3D3V_S5
EC100 EC101 EC163
5V_S5
EC102
1D5V_S3
EC103
3D3V_S0
EC104
AD+_IN
EC88 EC125
AD+
EC128 EC129
3D3V_S3
EC84 EC85 EC86 EC87
1D5V_S3
EC105 EC106 EC107 EC108 EC109
5V_S5
EC110 EC111 EC112 EC113 EC114 EC115
3D3V_S5
EC116 EC117 EC118 EC119 EC120 EC121
VCC_GFXCORE
EC145 EC144 EC143 EC146
VCC_CORE
EC136 EC137 EC138 EC139
1D8V_S0
EC140 EC141 EC142
ST1
34.4DH02.001
ST5
34.4AN10.001
H1 H2 H3 H4 H6 H11 H14 H18
ZZ.00PAD.C21
H5 H7 H8 H10 H17 H15 H16 H19 H20
ZZ.00PAD.921
DVT 20100702
Change SPR1 to 34.42T14.002
DVT 20100623
Change SPR3 to DY
SPR1 SPR2 SPR3 SPR4
34.42T14.002
DY
SPR5 SPR6 SPR7
34.17S03.001
DVT 1ST
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
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EVT

2010/5/17	P.52[BQ24751_Charger]	Del D31 2nd 3rd source
2010/5/17	P.25[HDMI CONN_PS8101]	Change 2nd source to 69.4R500.151
2010/5/24	P.26[HDD Connector]	Change R148 to 3.3K ohm ,add C437 for PM_SLP_S3# Delay
2010/5/27	P.38[KBC_NPCE781L / KB]	Add LCD_DETECT pull-high to 3D3V_S5
2010/5/31	P.52[BQ24751_Charger]	Mount C546,R451,R449,Q51 for battery can't Changer
2010/6/1	P.24[CRT CONN]	Change F6 to 69.44002.001, for Cadiz use
2010/6/4	P.33[Audio Jack]	Change MICIN1 to 20.10133.L11 , follow connector list
	P.28[USB]	Change USB1,USB2,USB3 connector to 22.10321.Q71 [follow ME connector list]
2010/6/10	P.36[AD / BATT CONN]	Change DCIN1 to 20.F0693.006 (follow connector list)
	P.41[FUNCTION BD & POWER BD]	Change PWCN1 to 20.F0693.006 (follow connector list)
2010/6/11	P.41[FUNCTION BD & POWER BD]	Del FUNCN2 connector by ME request
	P.38[KBC_NPCE781L / KB]	Change R240 to 20K ohm SB version.
	P.25[HDMI CONN_PS8101]	Change R614~R617 to 200R2J , Set mount. [for EMI request]
	P.25[HDMI CONN_PS8101]	Change C283,C364 to 1uF [for EMI request]
	P.25[HDMI CONN_PS8101]	Change C282,C285 to 1KpF [for EMI request]
2010/6/21	P.16[PCH (5 of 9)-PCI/USB]	Add PCI_REQ2# Pull-High to 3D3V_S0 by hang-up issue
	P.31[Audio Codec ALC269]	Change EC23,EC24 to mount [for EMI request]
	P.55[EMI/Spring/Boss]	Change DCBATOUT capacity to mount (EC71~83,EC89,EC90,EC124,EC164~169) [for EMI request]
		Change 5V_S0 capacity to mount (EC173~EC175) [for EMI request]
		Change 3D3V_S0 capacity to mount (EC91~94,EC104) [for EMI request]
		Change 3D3V_S3 capacity to mount (EC84~87) [for EMI request]
		Change VCC_GFXCORE capacity to mount (EC142~146) [for EMI request]
		Change VCC_CORE capacity to mount (EC136~139) [for EMI request]
	P.36[AD / BATT CONN]	Change BT+ capacity to mount (EC32~35) [for EMI request]
	P.23[LCD CONN]	Change C258 to 470pF (BRIGHTNESS_CN) [for EMI request]
		Add C272 between BLON_OUT_R and Gnd [for EMI request]
	P.34[CardReader RTS5186]	Change C576~580,C589 to 5pF [CardReader VEVS test]
		Add 0.1uF between MS_INS# and GND [CardReader VEVS test]
	P.24[CRT CONN]	Change R114,R115,R119,R120 to 2.7K ohm [CRT VEVS report]
2010/6/22	P.53[UL CIRCUIT]	UL Circuit modify. [Prevent the RTC_BAT keep protecting.]
2010/6/23	P.40[TouchPad]	Change THPAD1 to 20.K0487.006 [Follow ME connector list]
	P.55[EMI/Spring/Boss]	Change SPR3 to DY [for EMI request]
	P.53[UL CIRCUIT]	Add D42(83.00400.D1F), D41(83.00400.D1F) components. [Reduce the RTC_BAT discharge]
		connect R467 pin1 to D41 and D42 pin k. [Reduce the RTC_BAT discharge]
		connect D42 pin A to AD+_in. [Reduce the RTC_BAT discharge]
		connect D41 pin A to ACP_UVP [Reduce the RTC_BAT discharge]
	P.46[ADP3211_CPU CORE]	Change U45 to 84.08030.037 [Improve High side Vgs induce voltage]
		Change U47 to 84.08028.037 [Improve High side Vgs induce voltage]
		Change U48 to 84.08028.037 [Improve High side Vgs induce voltage]
		add these statements. [follow Power Team design]
		Change R316 to 7.87K ohm (old use 7.32K ohm) [Tune CPU Imon value]
		Change C465 to 680pF (old use 560pF) [Tune CPU load line value]
	P.47[RT8223_5V/3D3V]	Change R353 to 84.5K ohm (old use 97.6K ohm) [Adjust OCP value]
		Change L13 to 2.2uH (old use 3.3uH) [IC needs highter sensing voltage to detect it.]
	P.48[RT8209_1D5V]	Change R377 to 7.5K ohm (old use 11.5K ohm) [Adjust OCP value]
	P.49[RT8209_1D05V]	Change R389 to 14.3K ohm (old use 10.2K ohm) [Adjust OCP value]
		Change L15 to 0.56uH (old use 0.45uH) [Reduce the output ripple voltage]
	P.50[ADP3211_GFX_CORE]	Change R419 to 56.2K ohm (old use 53.6K ohm) [Tune GFX load line value]
		Change TC26 to mount.(old Dummy) [Improve under-shoot voltage phenomenon]
2010/6/25	P.13[PCH (2 of 9)-PCIE/CLK/SMB]	Change C156,C157 to 12pF [for Crystal vendor Test]
	P.29[LAN AR8131M]	Change C346 to 18pF [for Crystal vendor Test]
	P.34[CardReader RTS5186]	Change C384,C388 to 15pF [for Crystal vendor Test]
2010/6/29	P.17[PCH (6 of 9)-GPIO/RSVD]	Change RN31 to R648,R649 (56 ohm) for pull-high 1.05V_S0
		Del R295 , because double pull-high
2010/6/30	P.41[FUNCTION BD & POWER BD]	Change pin define of the FUNCN1 connector [follow the way of FFC folder for ME]
	P.19[PCH (8 of 9)-PWR\SATA\USB]	Del R101 , only use 3D3V_S5
	P.12[PCH (1 of 9)-SATA/RTC/HDA]	Change D1 to 83.R2003.I81 (SCHOTTKY DIODE)
	P.25[HDMI CONN_PS8101]	Change Q12 to 84.2N702.D31 (ESD Protected 1.0KV)
	P.44[RUN POWER]	Change D27 to 83.R2004.B8F (schottky diode)
2010/7/1	P.46[ADP3211_CPU CORE]	Change OPEN-GAP to CLOSE-GAP (G9~14)
	P.47[RT8223_5V/3D3V]	Change OPEN-GAP to CLOSE-GAP (G18,G22,G26,G30,G20,G24,G28,G32)
		Change OPEN-GAP to CLOSE-GAP (G19,G23,G27,G31,G34,G36)
		Change OPEN-GAP to CLOSE-GAP (G21,G25,G29,G33,G35,G37,G38)
	P.48[RT8209_1D5V]	Change OPEN-GAP to CLOSE-GAP (G47,G49,G51,G53)
		Change OPEN-GAP to CLOSE-GAP (G43~46,G48,G50,G52,G54~56)
	P.49[RT8209_1D05V]	Change OPEN-GAP to CLOSE-GAP (G57,G58,G60,G62)
		Change OPEN-GAP to CLOSE-GAP (G59,G61,G63~80)
	P.50[ADP3211_GFX_CORE]	Change OPEN-GAP to CLOSE-GAP (G81~86)
	P.51[RT8015_1D8V/ RT9026_0D75]	Change OPEN-GAP to CLOSE-GAP (G90~95)
	P.41[FUNCTION BD & POWER BD]	Add F7 POLYSW for POWER BD 5V_S5 protect.
	P.54[UVP Protect]	Delete R483 and add RN66. (RN66 part number is 66.10436.04L)
		Connect AD+_IN to RN66 pin 1.
		Connect RN66 pin2 to GND.
		Connect RN66 pin3 and pin4 to AD+_SW_OFF_G_1
	P.53[UL CIRCUIT]	Change R468 part number to the 64.36025.6DL
		Change R469 to the part number 64.30025.6DL
		Cummy R471 and mount D39.
		Delete D40 and RN58.
		Add R642. (Part number is 64.10045.6DL)
		Connect R642 pin 1 to RTC_BAT.
		Connect R642 pin2 to Q52 pin 2 and pin3.
	P.52[BQ24751_Charger]	Connect ACP to R435 pin 1.
	P.27[Bluetooth]	UPDATE BTCN1 PCB LAYOUT (REMOVE THE NPTH)
2010/7/2	P.38[KBC_NPCE781L / KB]	Rename H_PROCHOT# to EC_PROCHOT
	P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add R128 for EC_PROCHOT pull-low to Gnd
	P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add Q61 for EC_PROCHOT to PROCHOT#
	P.33[Audio Jack]	Add EC176 for HP_JD# to GND , Set Dummy for ESD.
		Add EC177 for MIC1_JD# to GND , Set Dummy for ESD.
	P.55[EMI/Spring/Boss]	Change SPR1 to 34.42T14.002
2010/7/5	P.14[PCH (3 of 9)-DMI/FDI]	Change D3 to schottky diode.
	P.37[Thermal / Fan Controllor]	Delelte Q29,Q30 main source 84.T3904.C11, follow CARAVEL-CP design
2010/7/6	P.53[UL CIRCUIT]	Rename R642 Pin1 contact to RTC_BAT_1 (Old use RTC_BAT),follow CARAVEL-CP

<Core Design>

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