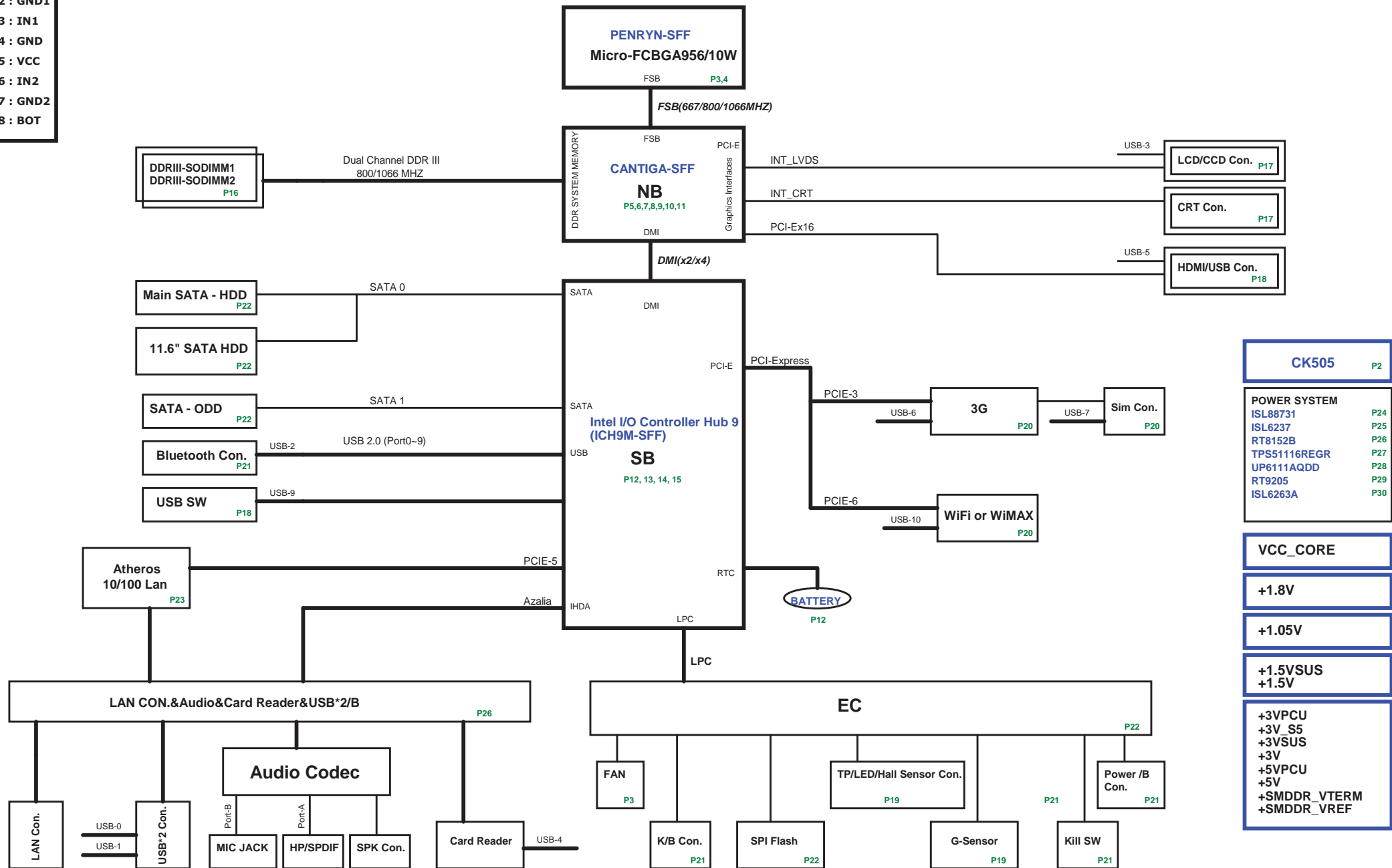


# PCB STACK UP

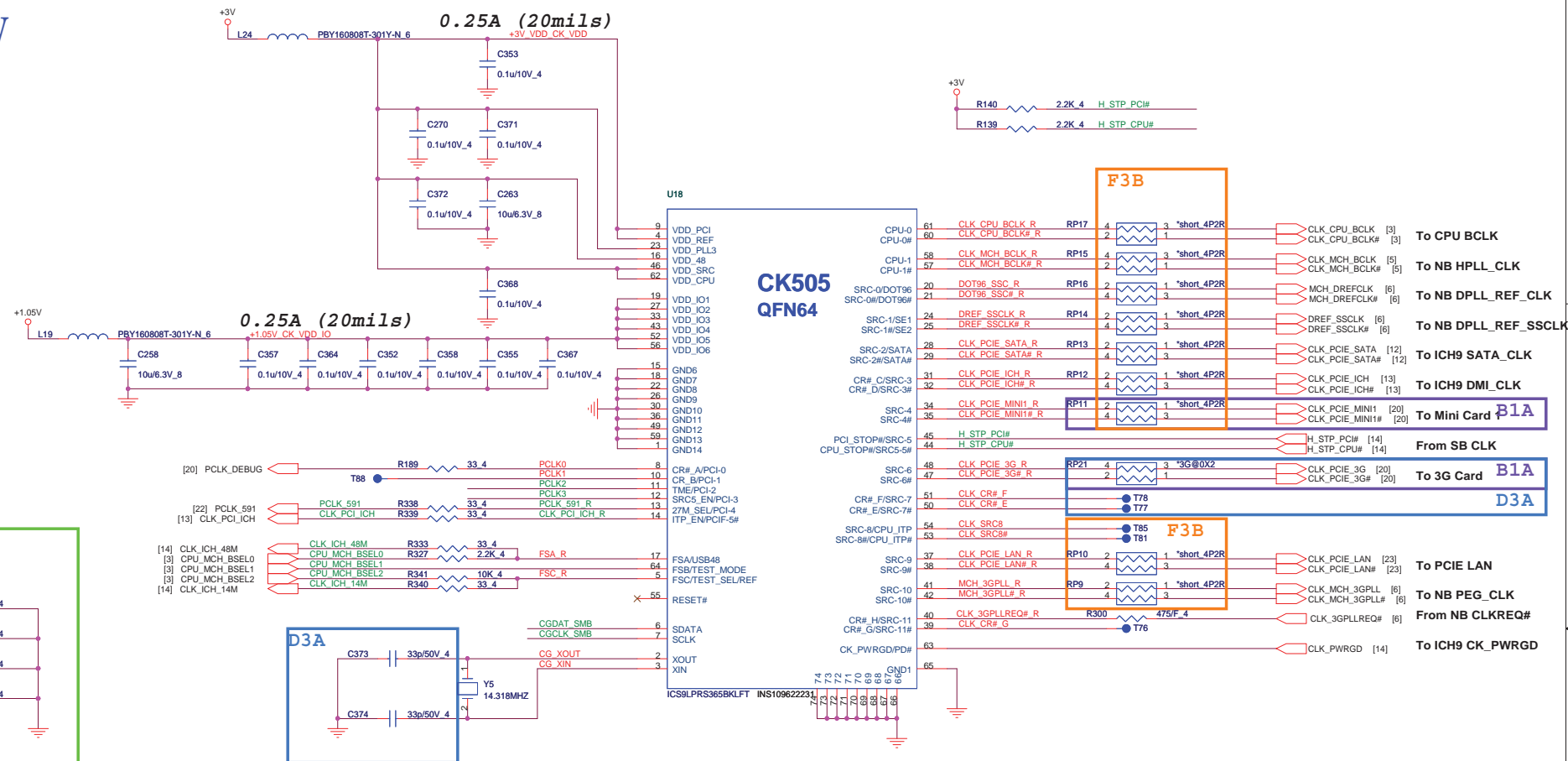
- LAYER 1 : TOP
- LAYER 2 : GND1
- LAYER 3 : IN1
- LAYER 4 : GND
- LAYER 5 : VCC
- LAYER 6 : IN2
- LAYER 7 : GND2
- LAYER 8 : BOT

# BU3 Block Diagram



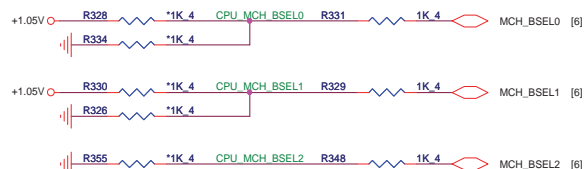


## CLOCK GEN



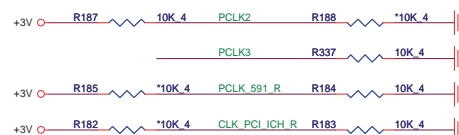
### BSEL Frequency Select Table

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

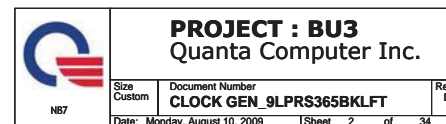
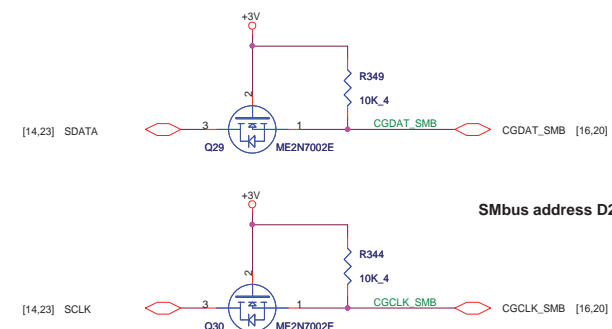


## Clock Gen Strap

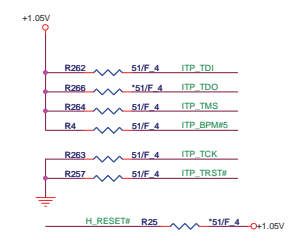
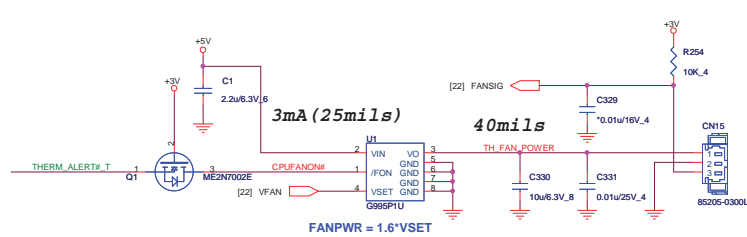
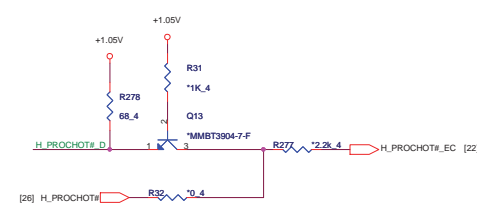
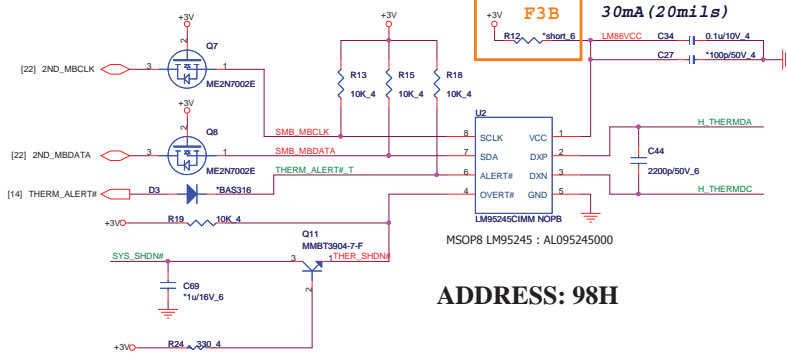
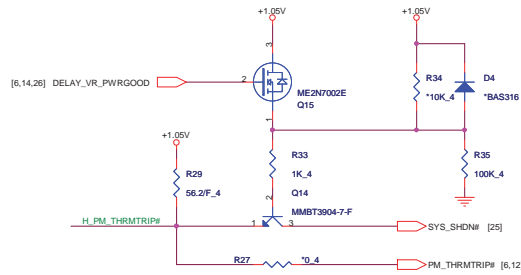
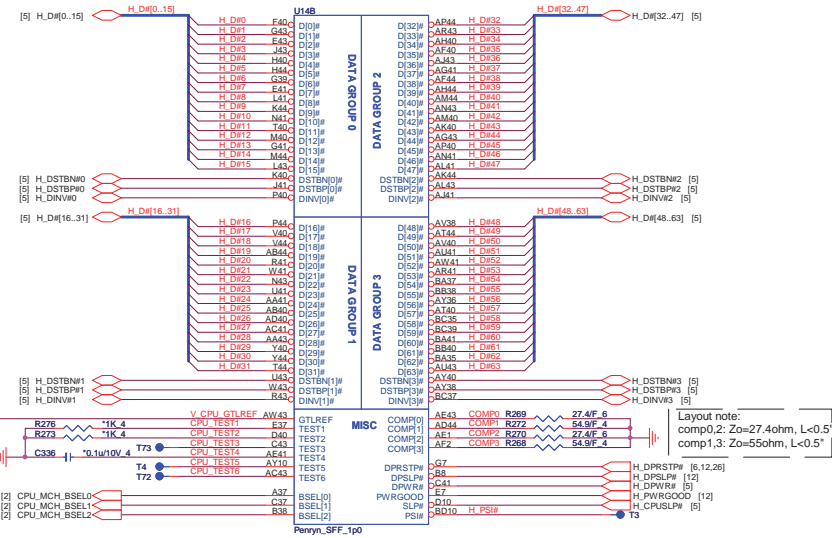
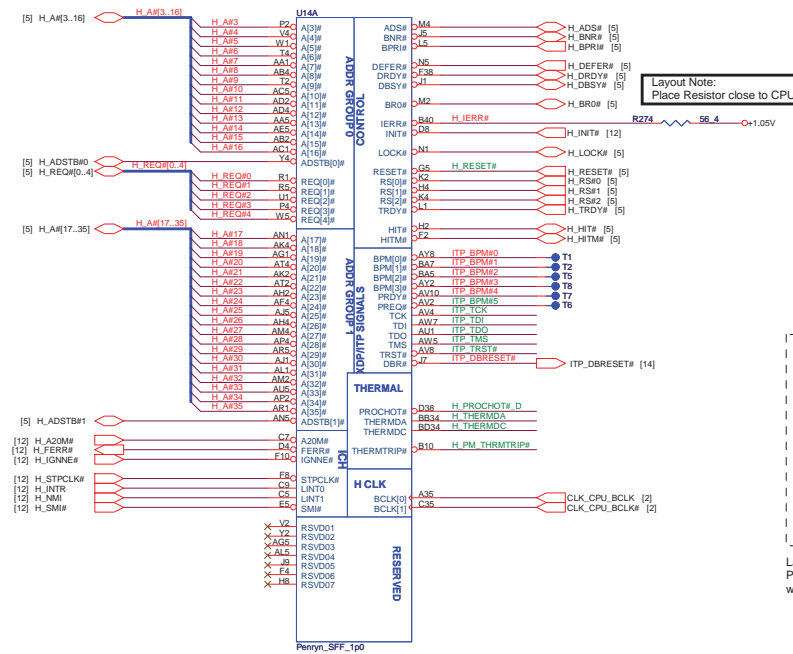
	SL88SP513	PULL HIGH	PULL DOWN
PIN11	PCI2/TWE	NO OVERCLOCKING (default)	NORMAL RUN
PIN12	PCI-3	PIN44/45 IS SRC5	PIN44/45 IS PCI_STOP/CPU_STOP (default)
PIN13	PCI-4/27M_SEL	PIN 24/25 IS 27MHz	PIN 21/20 IS SRC/DOT (default)
PIN14	PCIP-5/ITP_EN	PIN 53/54 IS CPUITP	PIN 53/54 IS SRC (default)



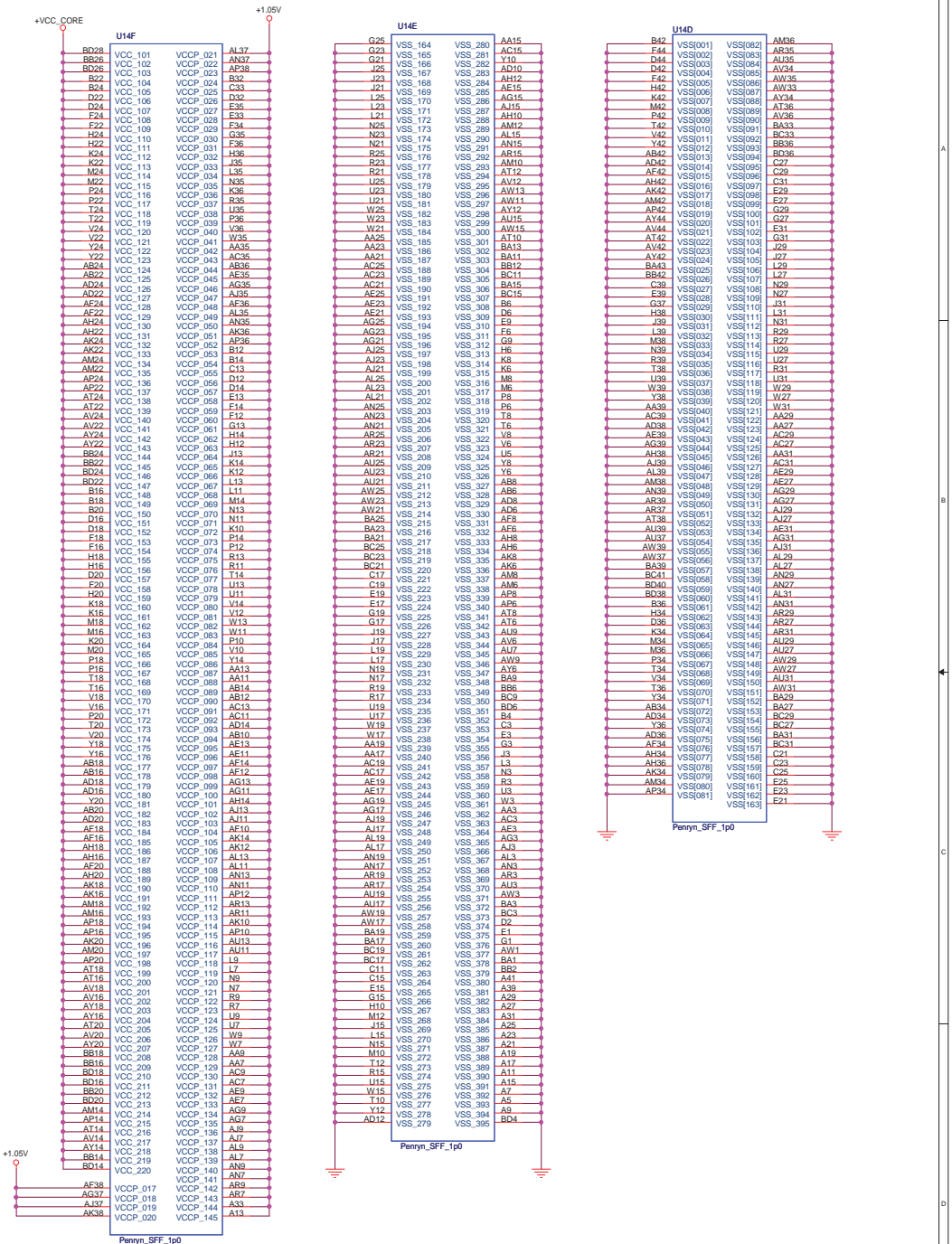
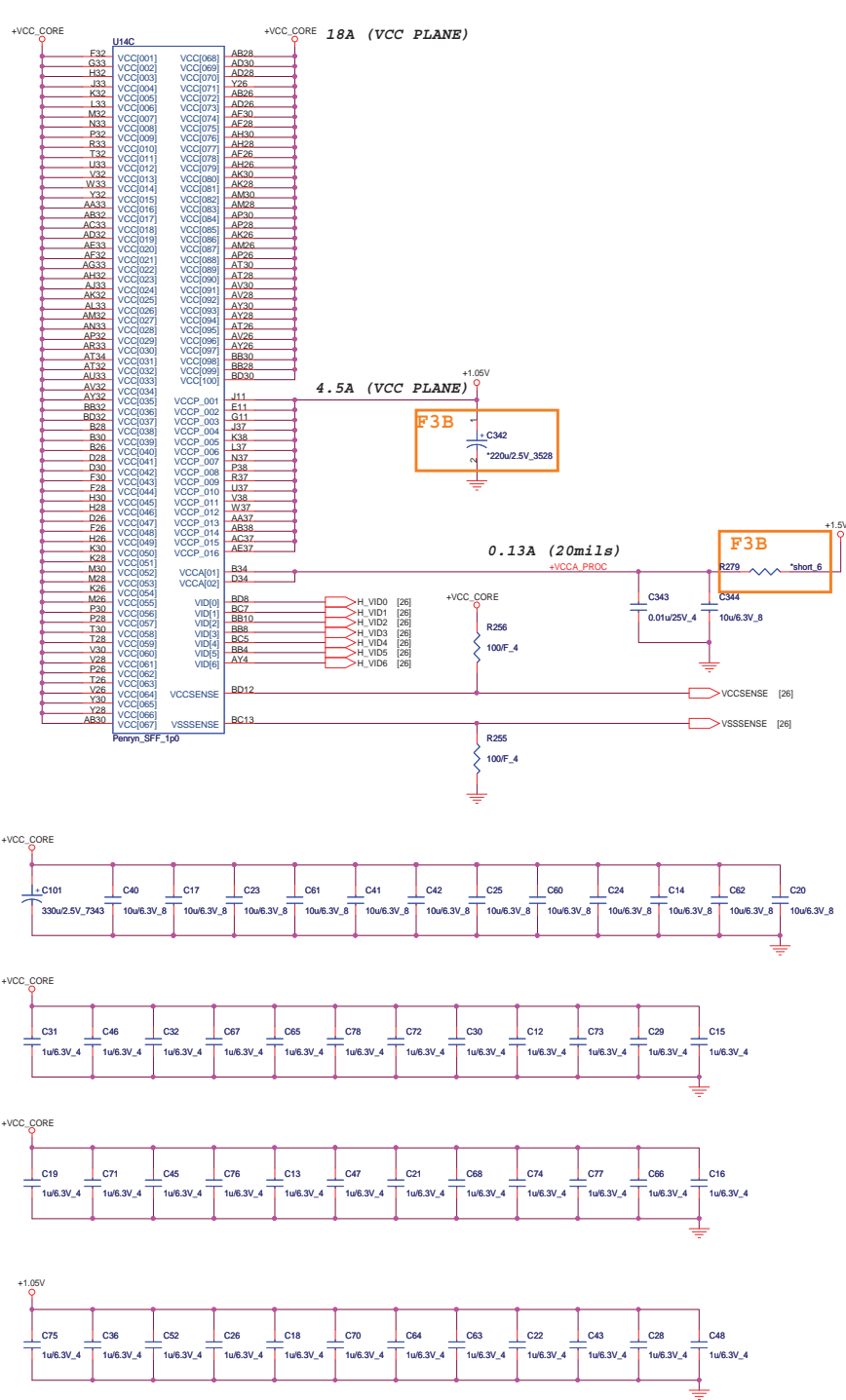
## Clock Gen I2C



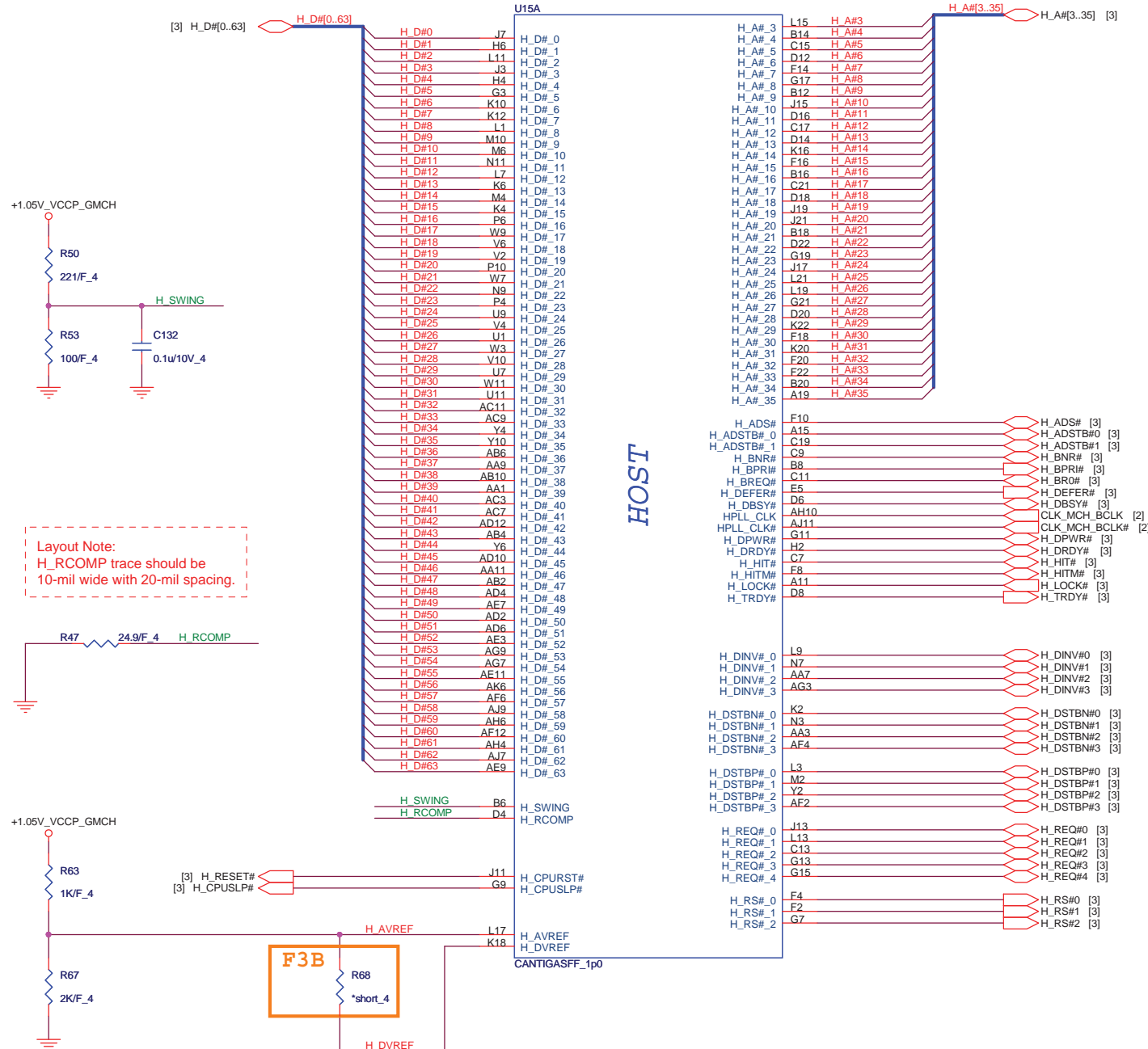




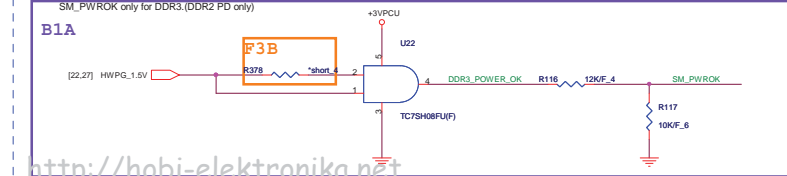
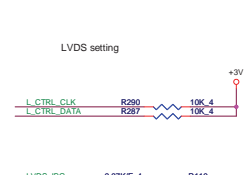
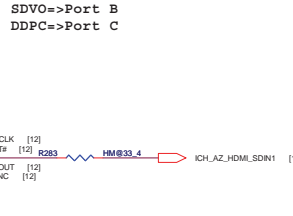




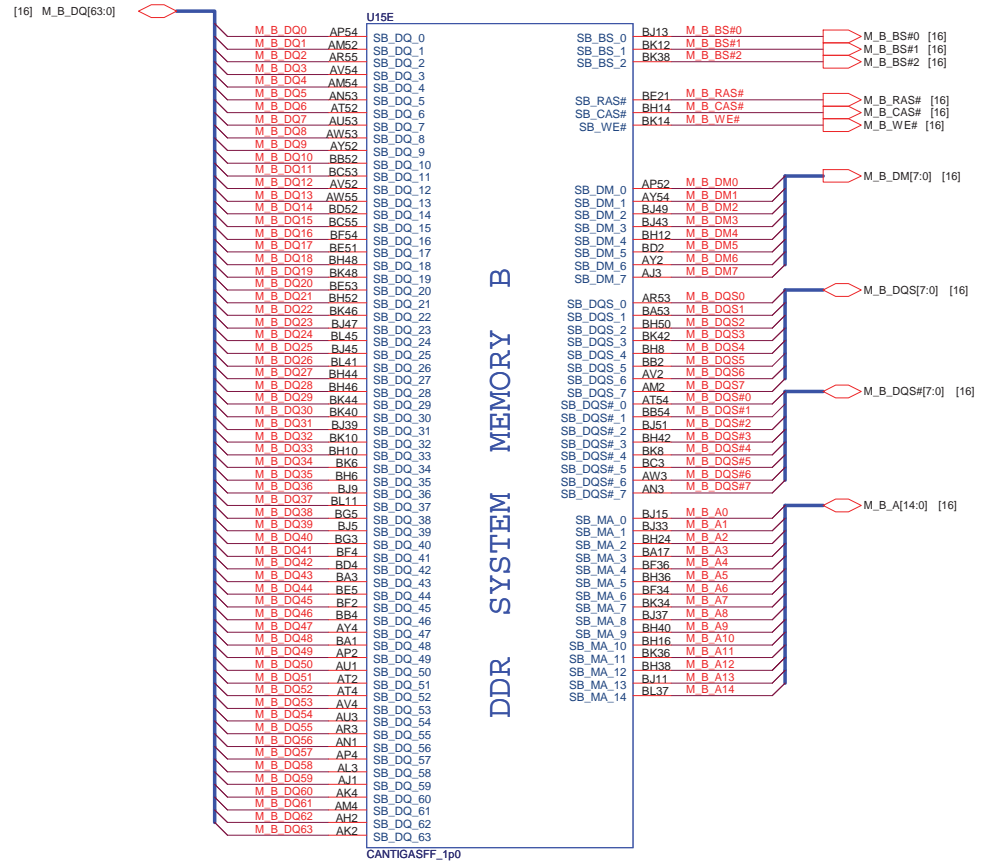
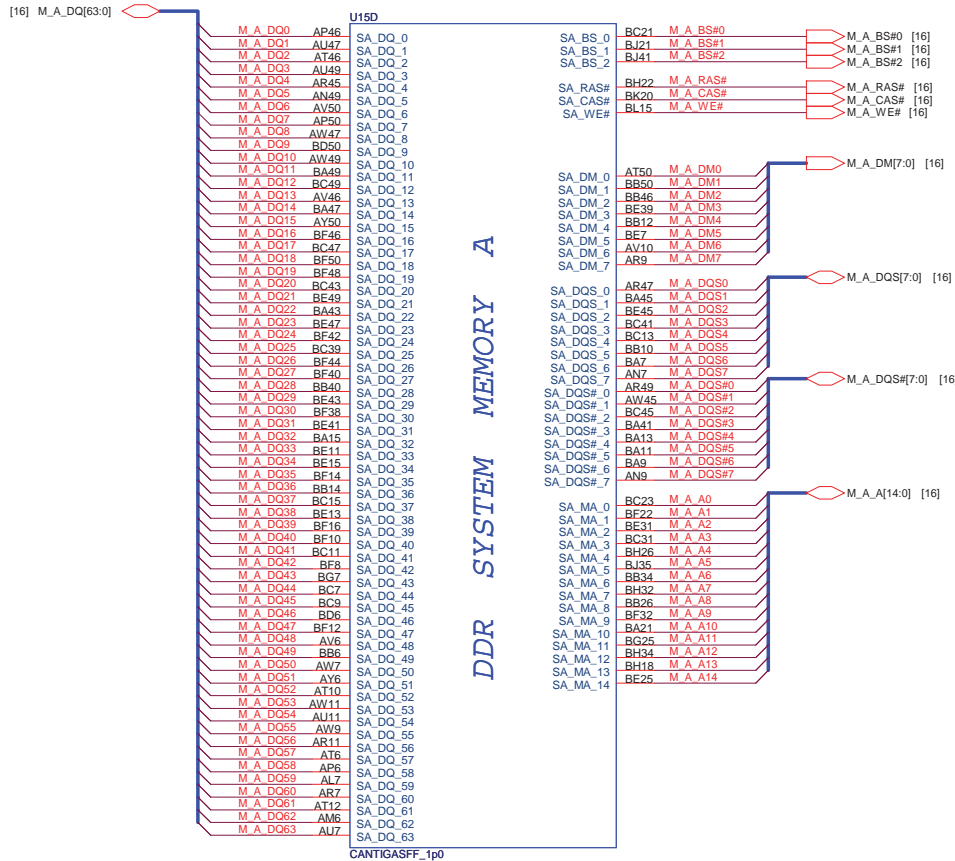






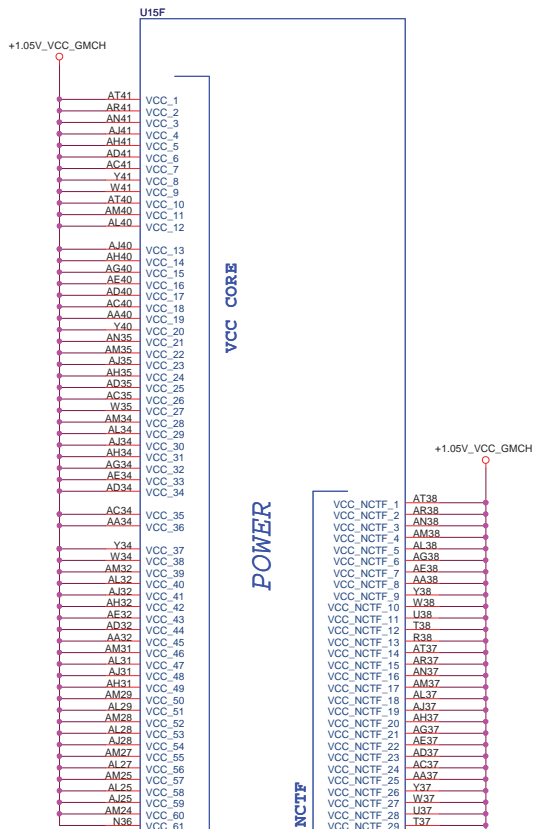






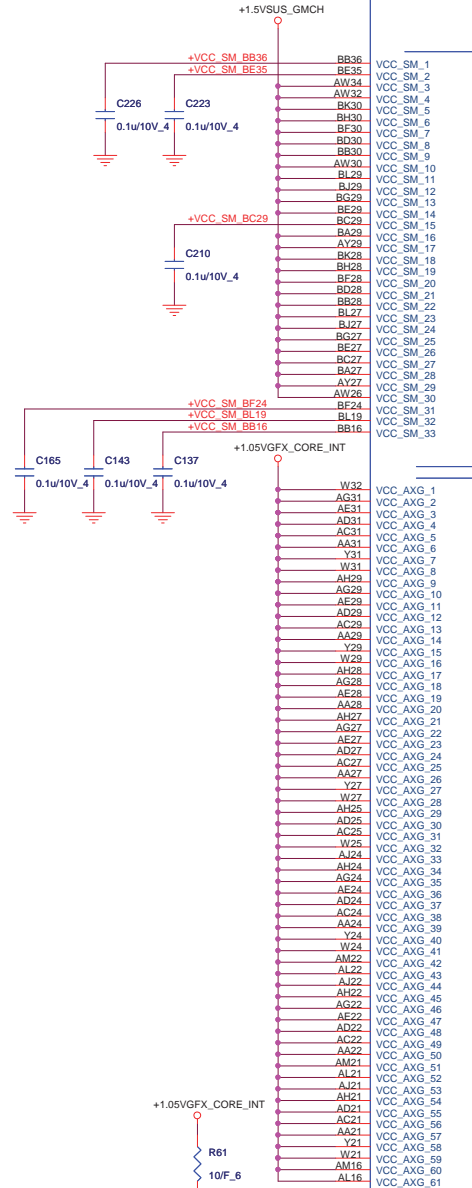


Ivcc internal VGA 2.2A  
(Shape or 120mils)



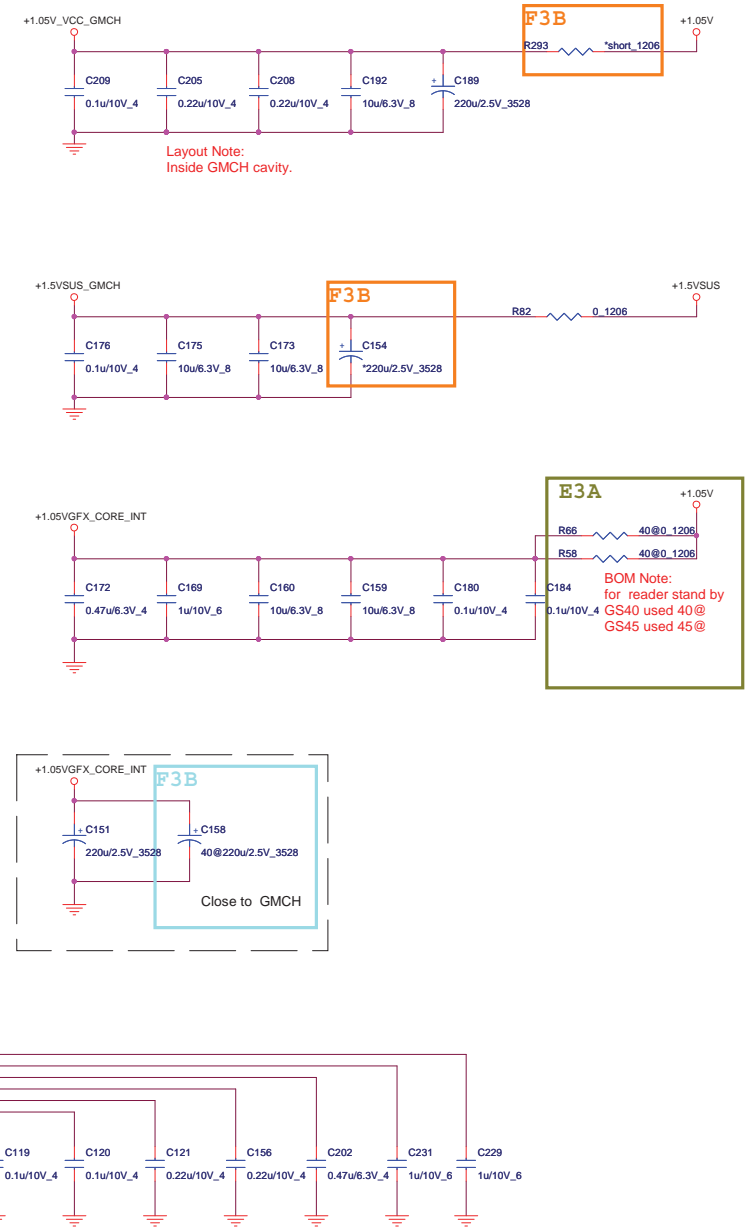
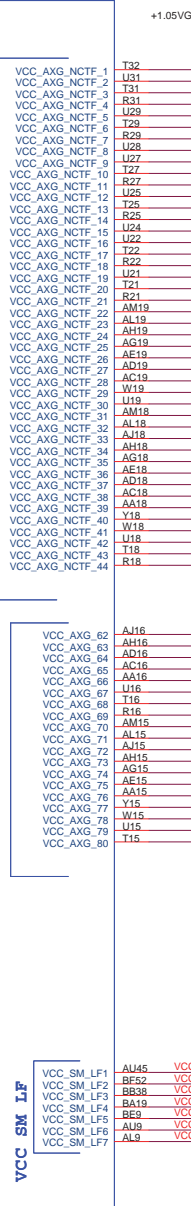
[30] VCC\_AXG\_SENSE  
[30] VSS\_AXG\_SENSE

DDR3-800 3.1625A  
DDR3-1066 4.14A  
(Shape or 200mils)



UMA: Places R721, R726 to 10 ohm.

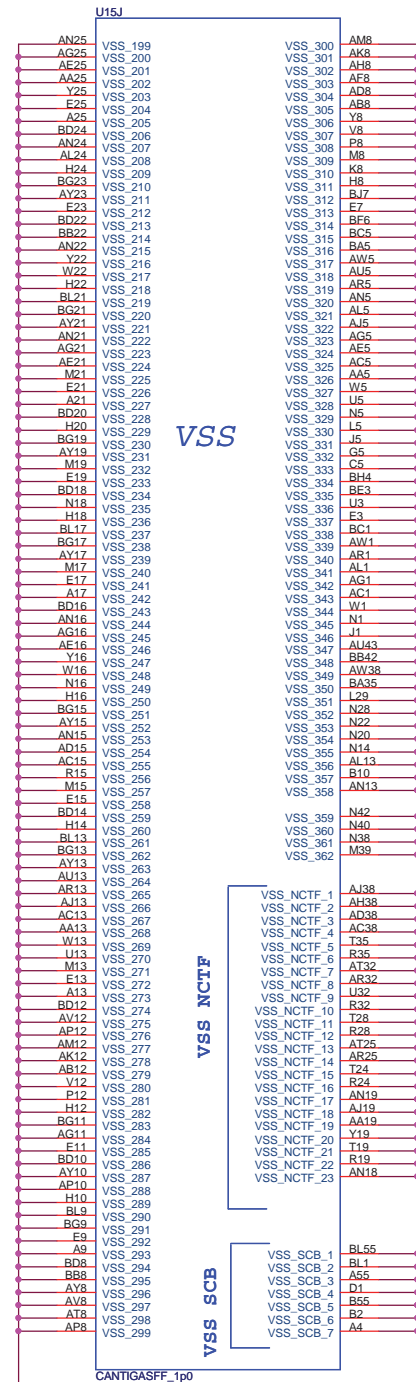
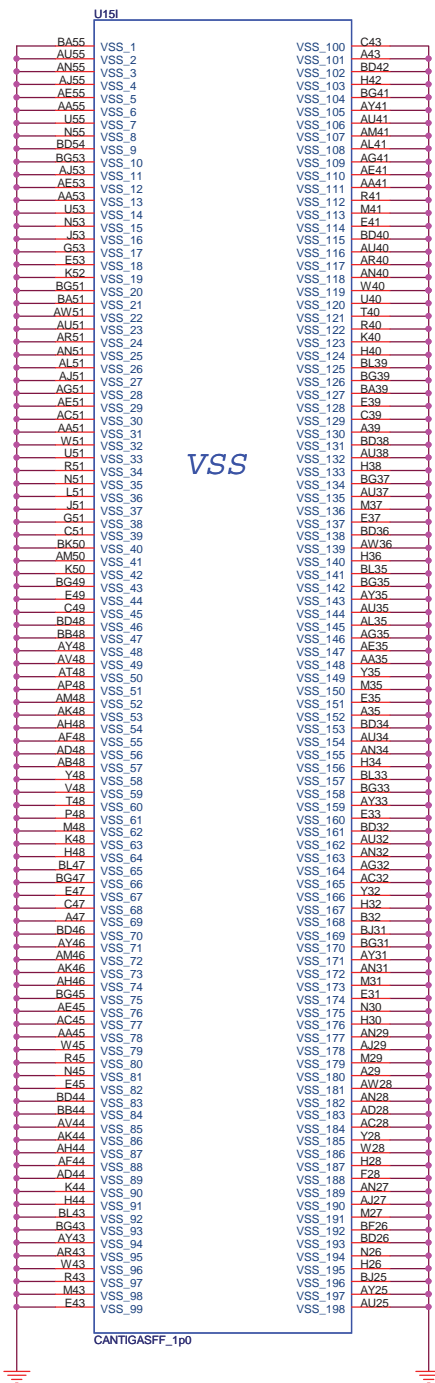
UMA 9.6A  
(Plane or shape)






















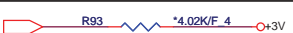


**PROJECT : BU3**  
Quanta Computer Inc.

Size Custom	Document Number <b>GANTIGA VSS(6/6)</b>	Rev D3B
Date: Monday, August 10, 2009	Sheet 10 of 34	



# North Bridge Strap Pin Configuration Table

(See DG 2.0 P306 Table 187)  
(See NB EDS 1.0 P187 Table 74)

Pin Name	Strap description	Configuration	PU<4.02K> PD <2.21K>	Note
<b>CFG[2:0]</b>	FSB Frequency Select	[000]= FSB 1066MHz [010] = FSB 800MHz [011] = FSB 667MHz	See Page 2 FSB selection table	
<b>CFG[4:3]</b>	Reserved			
<b>CFG5</b>	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)	[6] MCH_CFG5 	
<b>CFG6</b>	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)	[6] MCH_CFG6 	
<b>CFG7</b>	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)	[6] MCH_CFG7 	
<b>CFG8</b>	Reserved			
<b>CFG9</b>	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)	[6] MCH_CFG9 	
<b>CFG10</b>	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)	[6] MCH_CFG10 	
<b>CFG11</b>	Reserved			
<b>CFG12</b>	ALLZ	0 = ALLZ mode enable 1 = disable(Default)	[6] MCH_CFG12 	
<b>CFG13</b>	XOR	0 = XOR mode enable 1 = disable(Default)	[6] MCH_CFG13 	
<b>CFG[15:14]</b>	Reserved			
<b>CFG16</b>	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)	[6] MCH_CFG16 	
<b>CFG[18:17]</b>	Reserved			
<b>CFG19</b>	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed	[6] MCH_CFG19 	
<b>CFG20</b>	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port	[6] MCH_CFG20 	
<b>SDVO_CTRLDATA</b>	SDVO Present	0 = No SDVO/HDMI/DP Device Present(Default) 1 = SDVO/HDMI/DP Device present	<i>Strap on P18 SDVO_CTRLDATA</i>	
<b>L_DDC_DATA</b>	Local Flat Panel(LFP) Present	0 = LFP Disable(Default) 1 = LFP Card Present;PCIE disable	<i>Strap on P17 INT_LVDS_EDIDDATA</i>	
<b>DDPC_CTRLDATA</b>	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present	[6] DDPC_CTRLDATA 	

[6] DDPC\_CTRLCLK 

## Enable iTPM Table

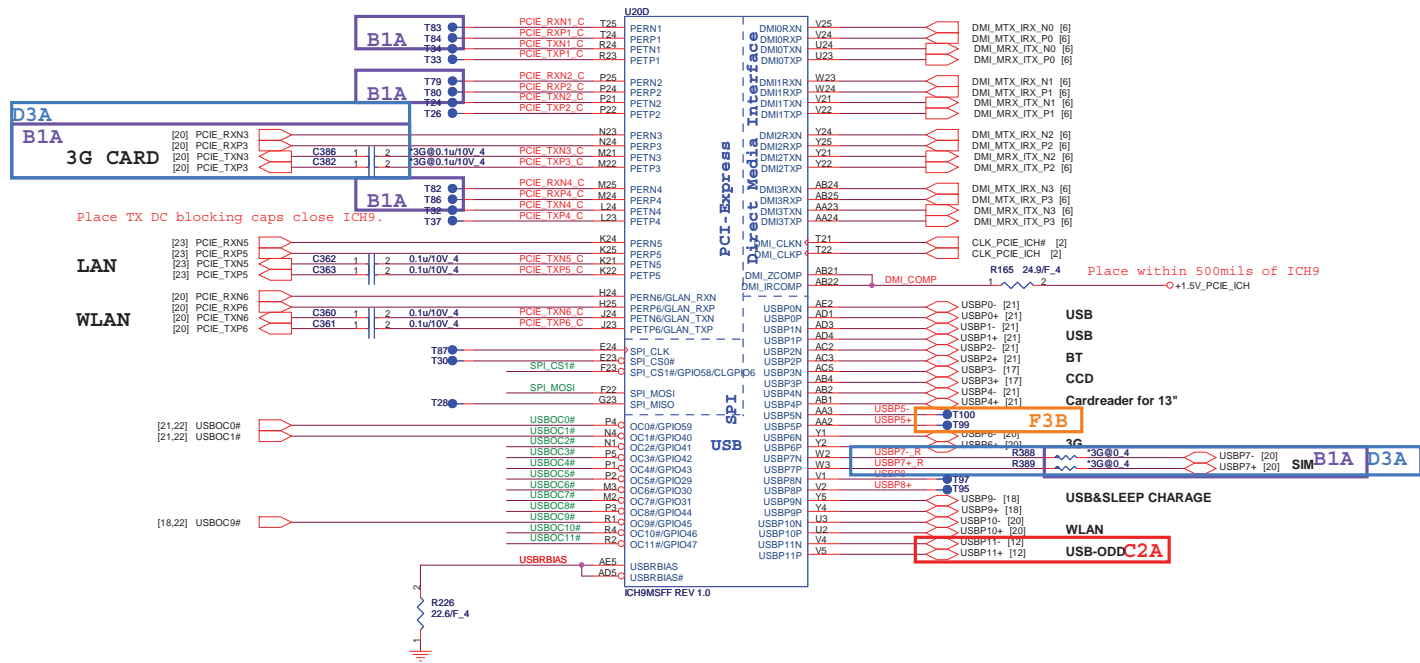
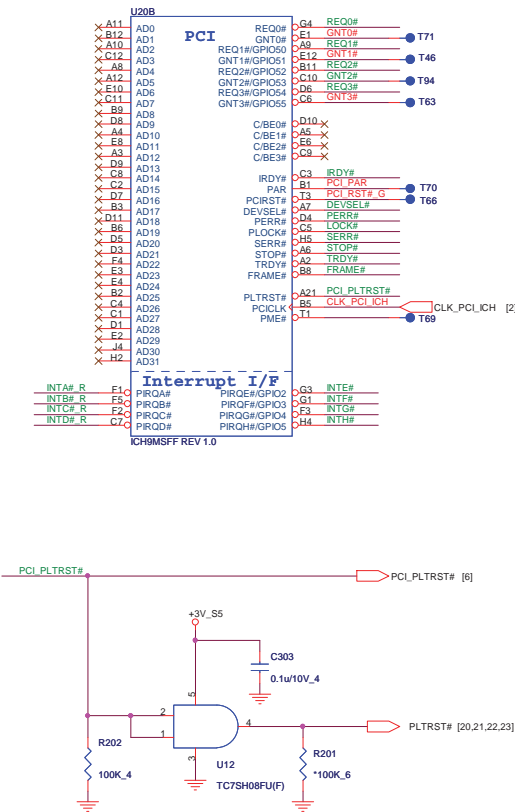
PAGE	Net Name	PU & PD	NOTE
11	MCH_CFG_6	PD 10K to GND	NB Strap pin
13	SPI_MOSI	PU 20K to +3V_S5	SB Strap pin
14	CLGPIO5	PU 10K to +3V_S5	SB Strap pin







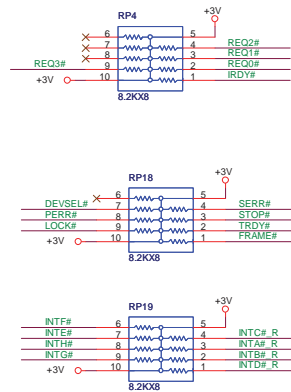
*ICH9*



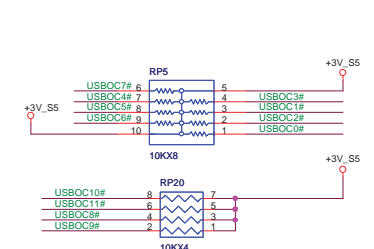
### South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD		
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	 +1.5V_HDA_IO_1CH R231 *1K_4 AC2_SYNC		
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	 GNT2# R370 *1K_4		
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	 GNT3# R218 *1K_4		
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	 SPI_MOSI R314 *20K_4		
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	 GNT0# R246 *1K_4
			0	1	SPI(Default)	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	 SPI_CS1# R164 *1K_4

## PCI PULL-UP



USBOC# PULL-UP

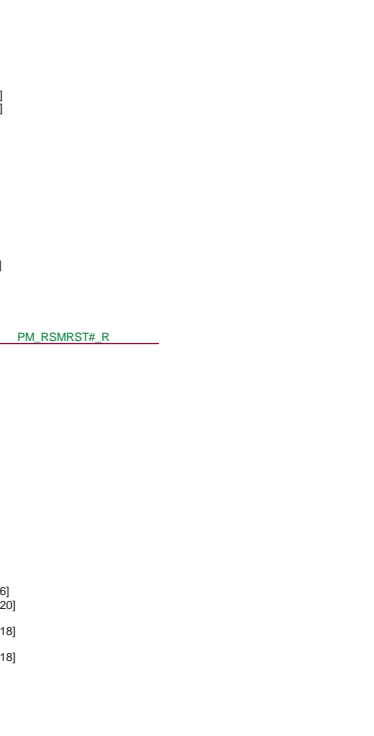
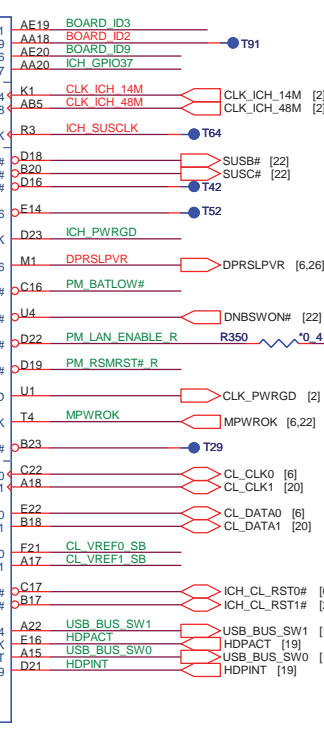
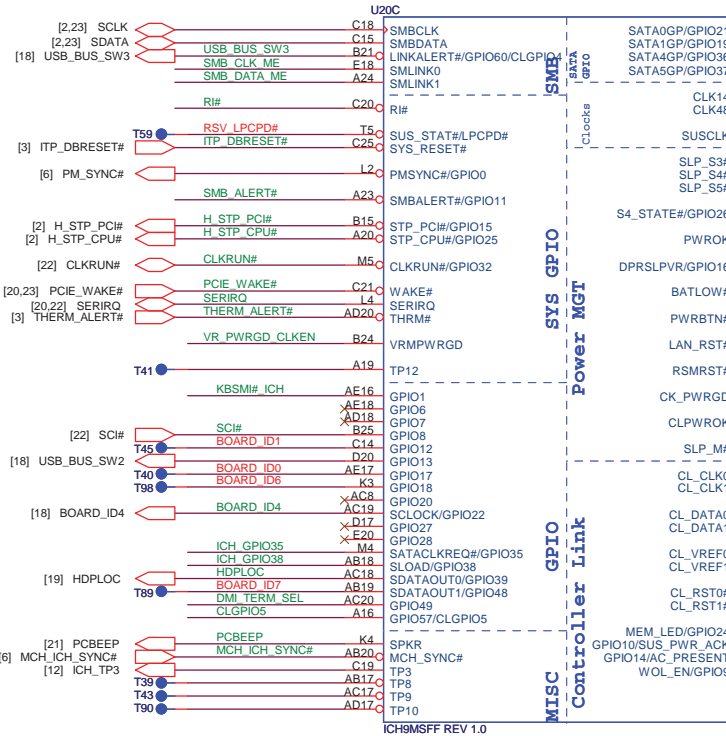
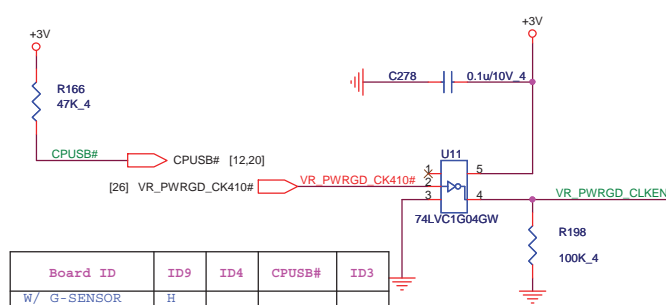
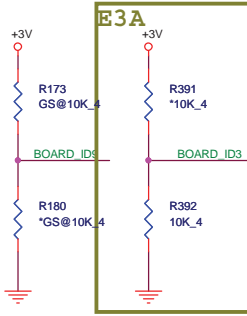
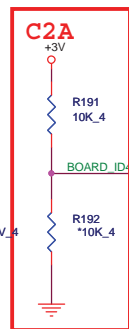
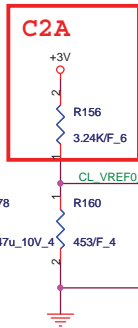
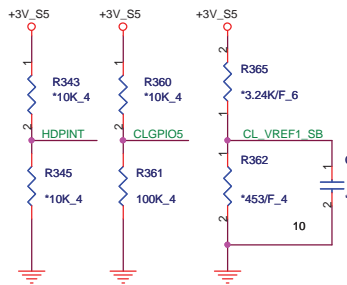
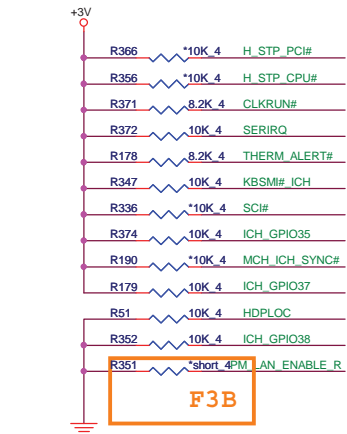
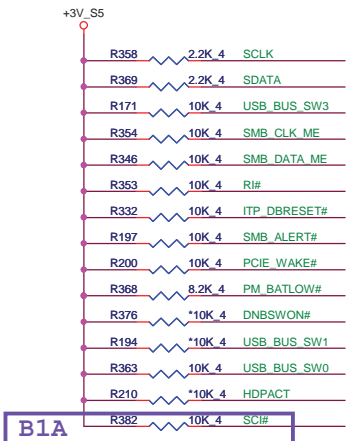


**PROJECT : BU3**  
Quanta Computer Inc.

Size Custom	Document Number <b>ICH9-M (USB/PCIE/DMI)</b>	Rev D3B
Date: Monday, August 10, 2009	Sheet 13 of 34	



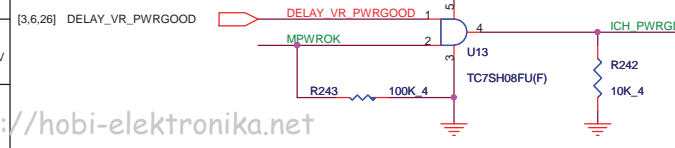
# ICH9



## South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
PCBEEP	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCBEEP R245 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R172 *1K_4

Board ID	ID9	ID4	CPUSB#	ID3
W/ G-SENSOR W/O G-SENSOR	H L			
W/ HDMI W/O HDMI		L H		
W/ 3G W/O 3G			H L	
FOR 1.1" FOR 1.3"				H L



**PROJECT : BU3**  
Quanta Computer Inc.

Size Custom

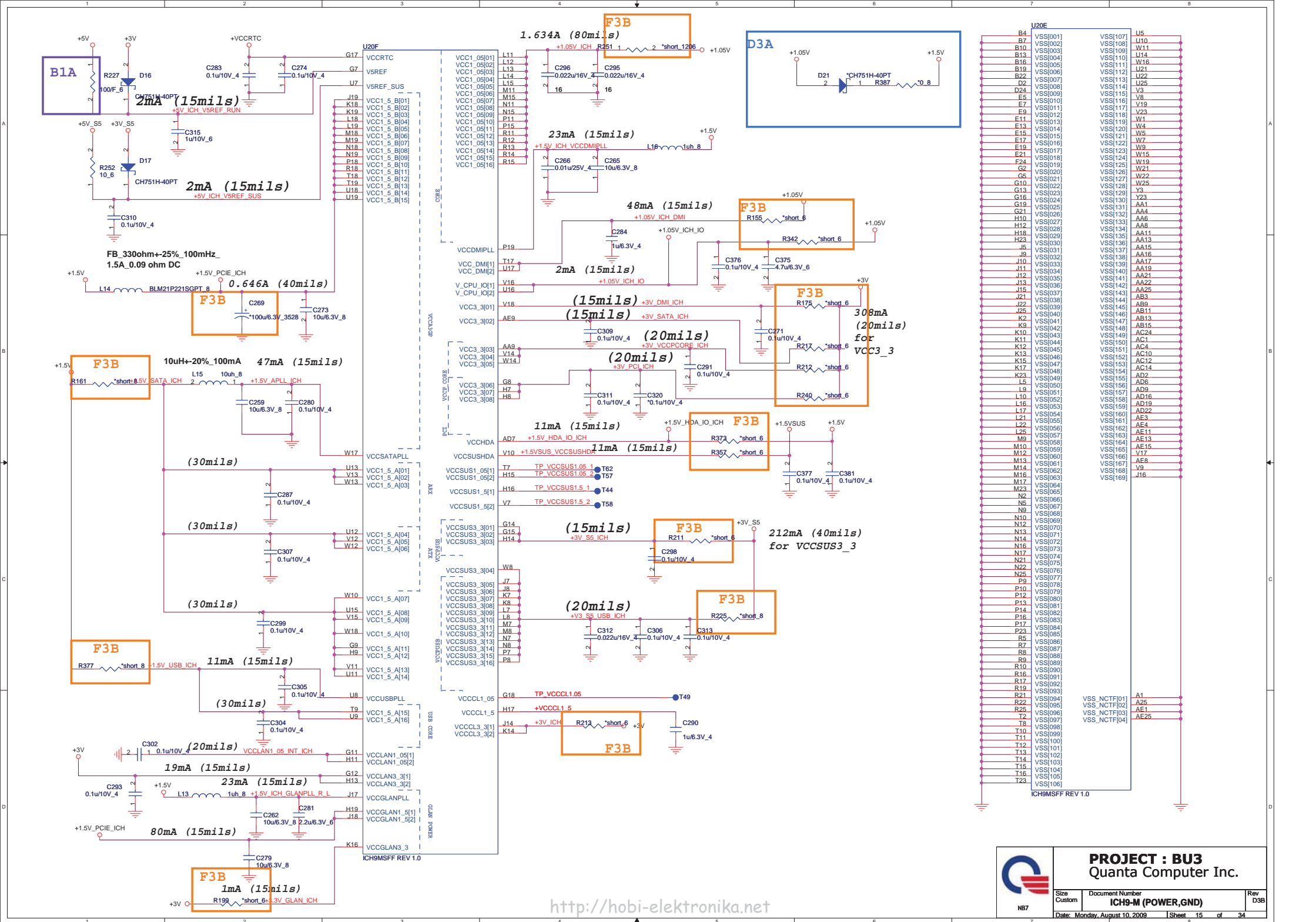
Document Number  
**ICH9-M (PM,GPIO,SMB)**

Date: Monday, August 10, 2009

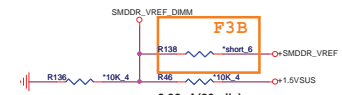
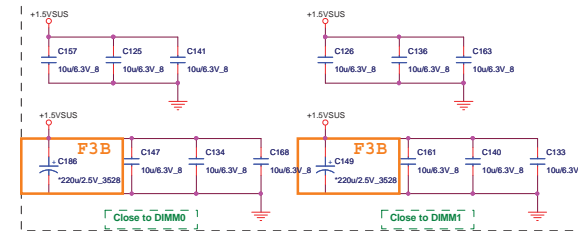
Rev D3B

Sheet 14 of 34







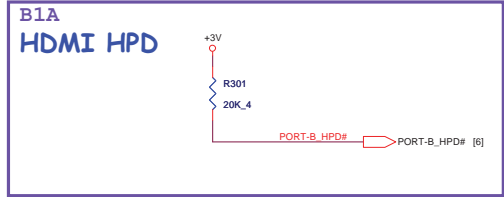
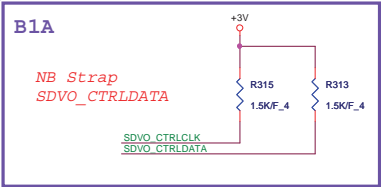




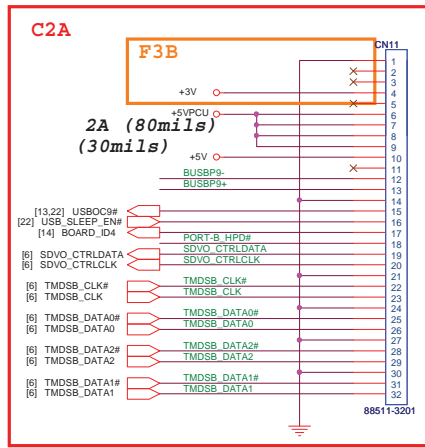




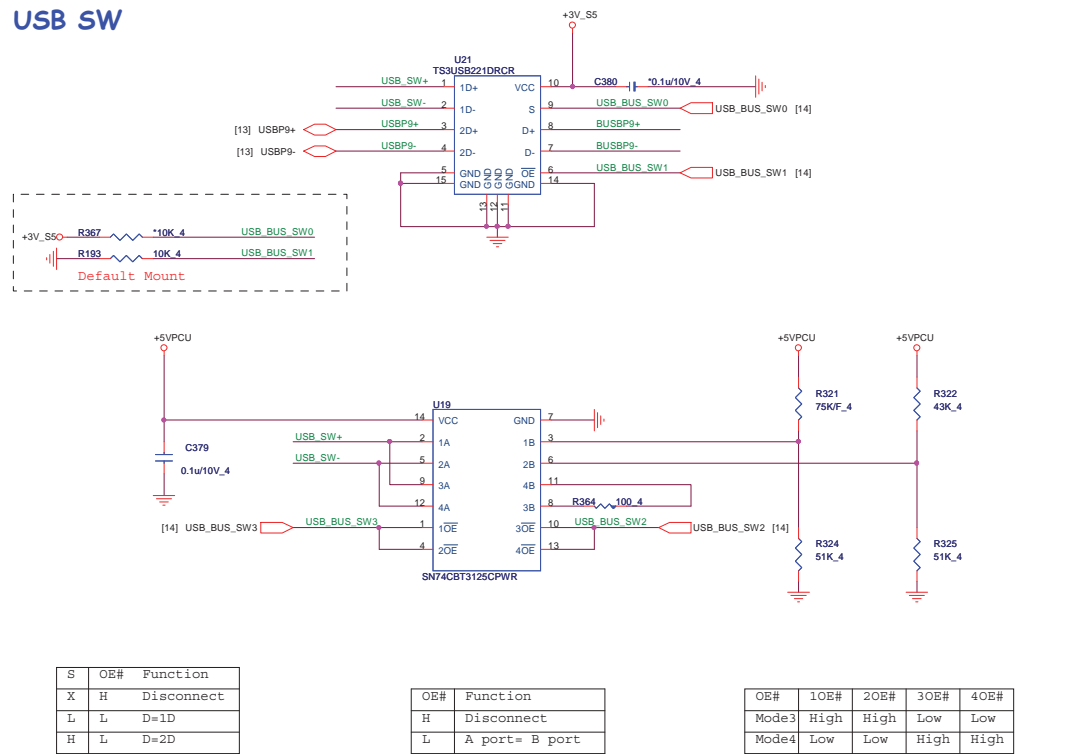
HDMI IC



HDMI CON.



USB SW



EMI



## C2A

[illegible]

**CN5**

Pin	Signal	Destination
1	GND	Ground
2	SATA_TXP0	SATA_TXP0 [12]
3	SATA_TXN0	SATA_TXN0 [12]
4	GND	Ground
5	SATA_RXN0	SATA_RXN0 [12]
6	SATA_RXP0	SATA_RXP0 [12]
7	GND	Ground
8	DP	DP
9	+5V	+5V_HDD1
10	+5V	+5V_HDD1

**0.94A (80mils)**

**+5V\_HDD1**

**\*11 @88513-1041**

---

The schematic diagram illustrates the power supply section of the MAX9814C evaluation board. It features a 5VPCU input connected to the VIN pin (pin 3) of the MAX9814C IC (U7). The IC's SHDN pin (pin 1) is connected to a +5VPCU source, and its VO pin (pin 4) is connected to a +3V\_HDP source. The GND pin (pin 2) is connected to ground. The SET pin (pin 5) is connected to a +3V\_HDP source. A capacitor C170 (GS@0.1uF/10V\_4) is connected between the VIN pin and ground. A capacitor C185 (GS@10uF,6.3V\_4) is connected between the VO pin and ground. The IC is also connected to a +3V\_HDP source. The diagram includes labels for the input signals, the IC, the capacitors, and the ground connections.

FS (Full Scale) selection

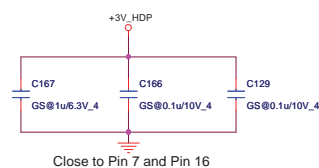
FS	0	1
	2g Full-Scale	6g Full-Scale

PD (Power Down) selection

	0	1
PD	Normal Mode	Power-down mode

### HDPPD selection

HDPPD	0	1
	Normal Mode	Power-down mode



Close to Pin 7 and Pin 16

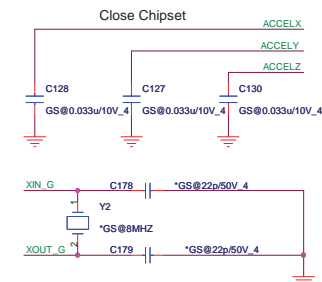
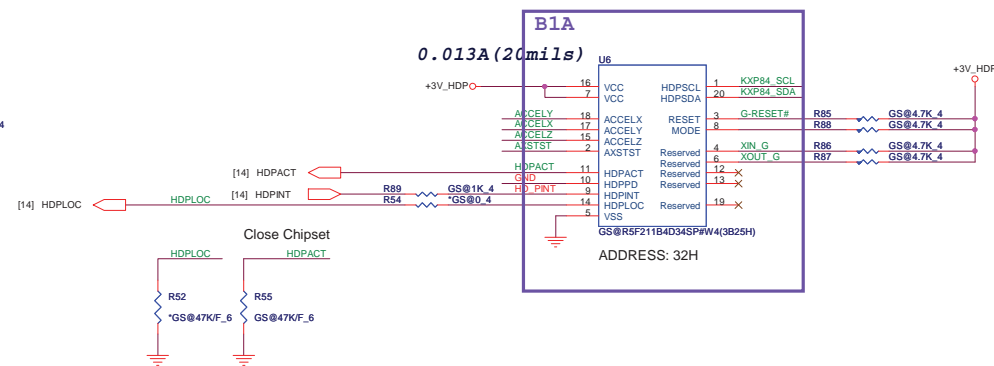
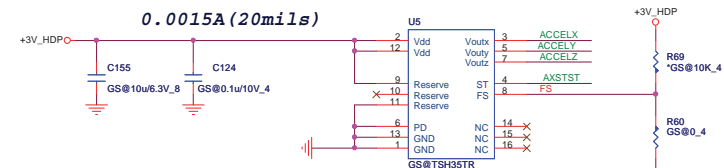
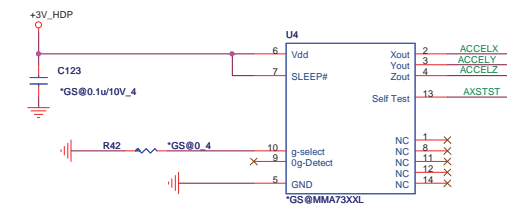
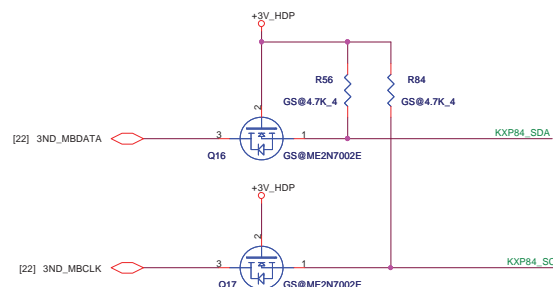
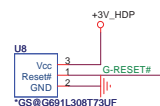
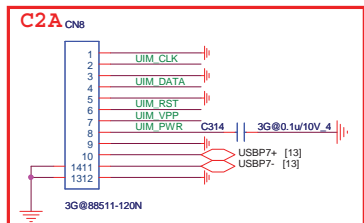
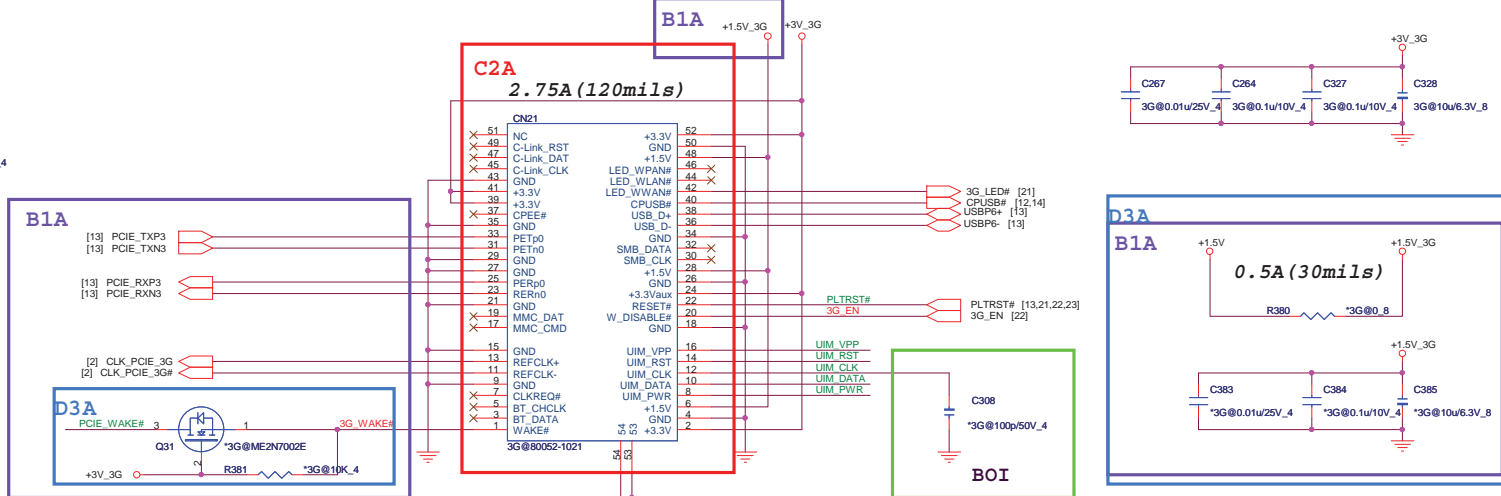
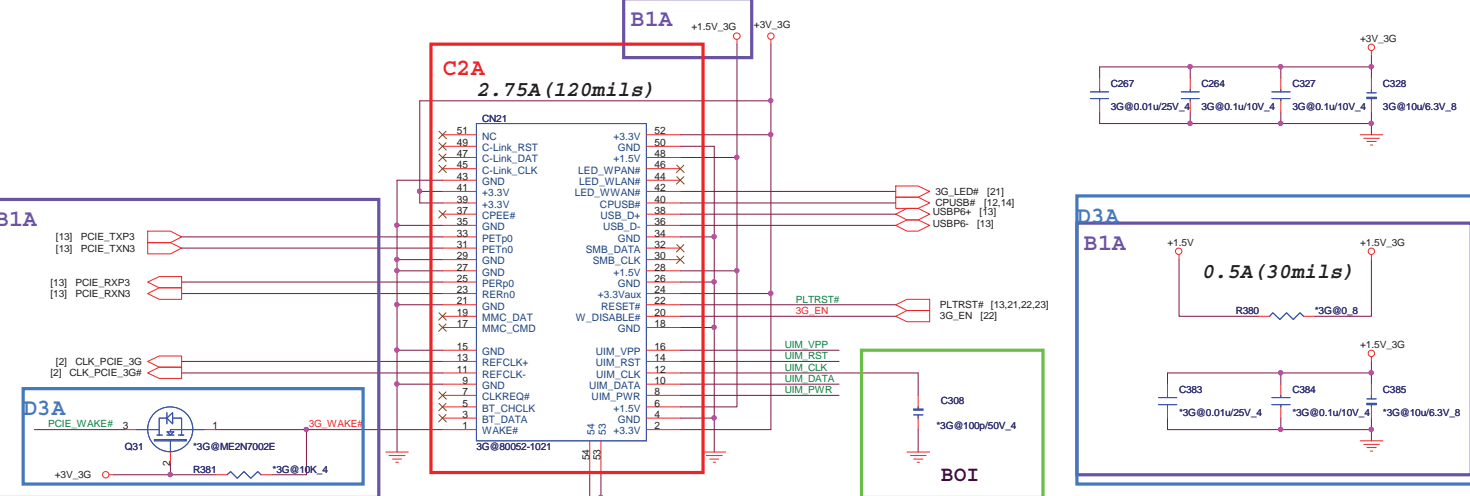




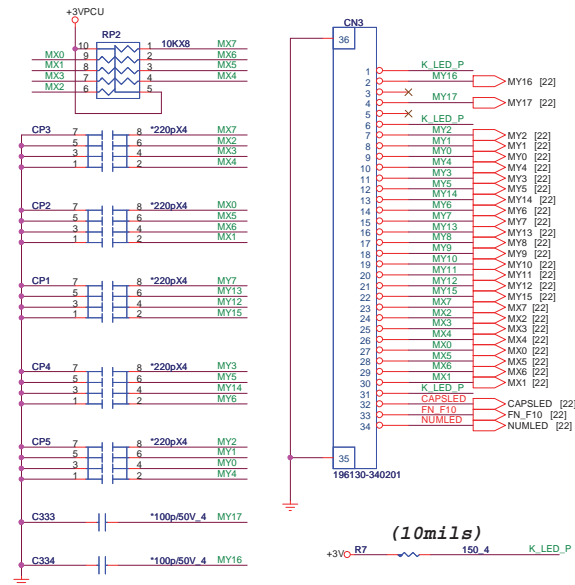
Diagram illustrating a bus connection:

- A green line labeled **PLTRST#** connects to a purple box labeled **B1A**.
- Inside the purple box, the label **D3A** is present.
- A red line labeled **R379** connects to a resistor symbol.
- The resistor symbol is connected to a label **\*100K 4**.

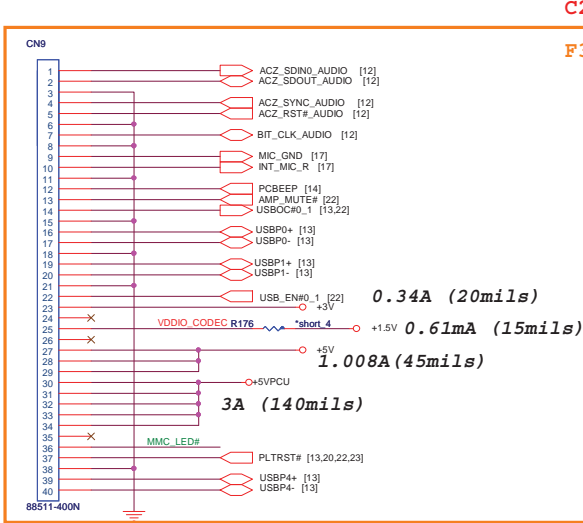




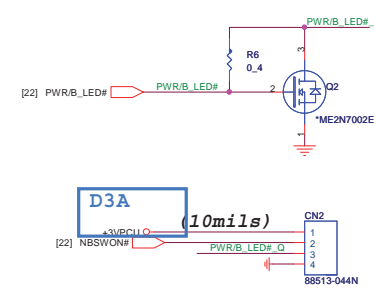
## INT Keyboard



## USB&FPC&CARDERAD CONNECTOR

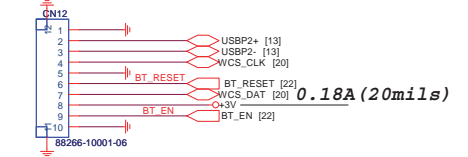


## Power board

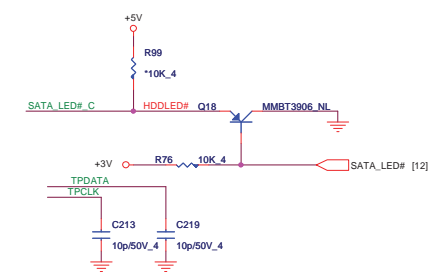
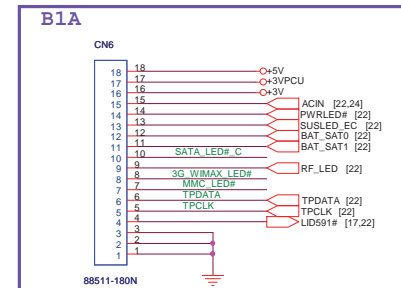


## B1A

## Bluetooth

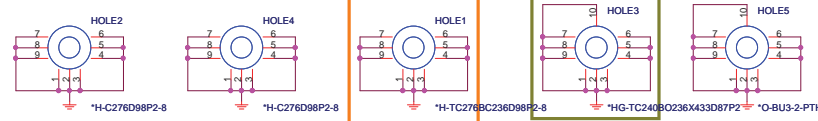
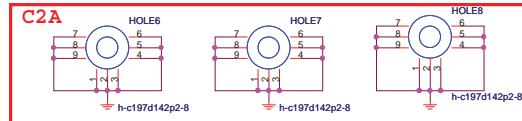


## LED/TP/Hall Sensor Con.

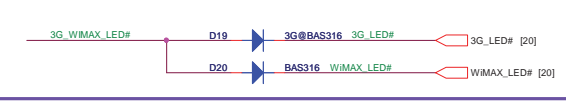


## HOLE

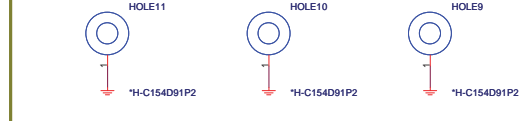
## CPU FAN



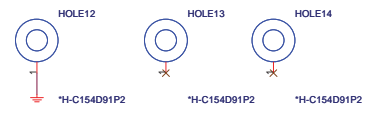
## B1A



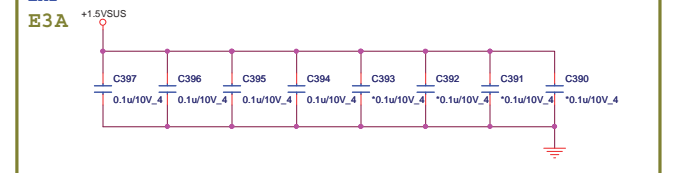
## E3A



## F3B



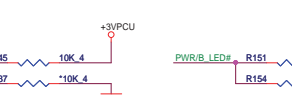
## EMI







Size	Document Number	Rev
	EC-WPCE775CA0DG	D3B
Date:	Monday, August 10, 2009	Sheet 22 of 24

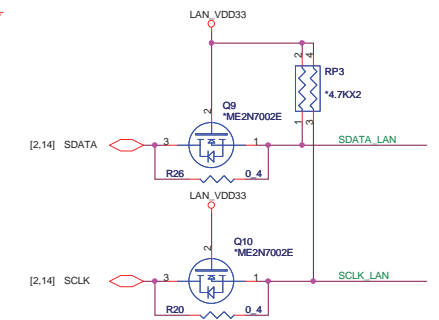


SMBUS	Devices	Address
1	Battery	
2	CPU Thermal Sensor1	98H
	EC EEPROM	A0H
3	3D Sensor	40H

<http://hobi-elektronika.net>



### Close to U3



(60mils)

### Close to U3

Pin5

VDD3V/CTRL12

C104  
0.1µF/10V\_4

Pin15

+2.5V\_LAN

R44 0.6

AVDD\_CEN  
TX1P  
TX1N  
TX0P  
TX0N

1  
2  
3  
4  
5  
6

88513-064N

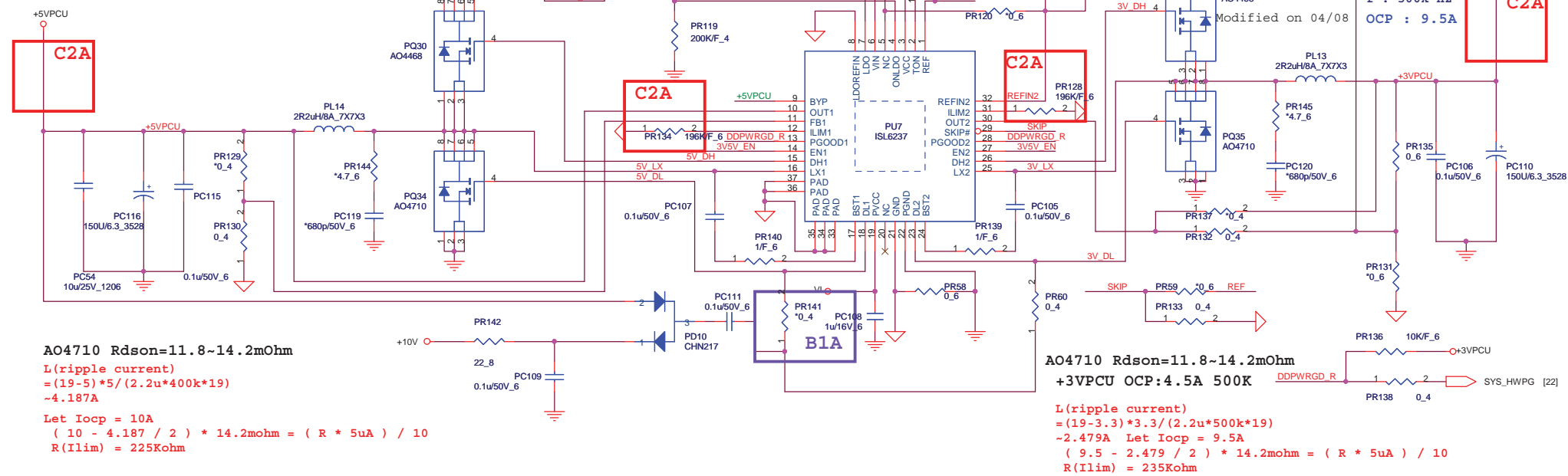
Size	Document Number	Rev
	Atheros Lan	D3B
Date:	Monday, August 10, 2009	Sheet 23 of 34





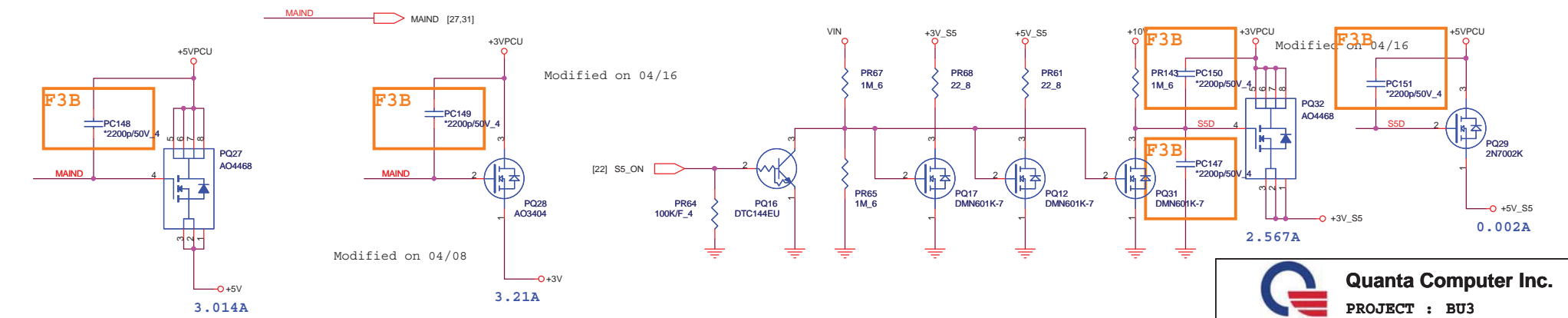


Peak 8.521A,AVG 6.391A  
Total capacitor : 160uF  
ESR : 25mΩ  
f : 400k Hz  
OCP: 10A



AO4710 Rdson=11.8~14.2mOhm  
L(ripple current)  
= (19-5) \* 5 / (2.2u \* 400k \* 19)  
~4.187A  
Let Iocp = 10A  
(10 - 4.187 / 2) \* 14.2mohm = (R \* 5uA) / 10  
R(Ilim) = 225Kohm

AO4710 Rdson=11.8~14.2mOhm  
+3VPCU OCP:4.5A 500K  
L(ripple current)  
= (19-3.3) \* 3.3 / (2.2u \* 500k \* 19)  
~2.479A Let Iocp = 9.5A  
(9.5 - 2.479 / 2) \* 14.2mohm = (R \* 5uA) / 10  
R(Ilim) = 235Kohm



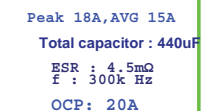
3.014A

3.21A

**Quanta Computer Inc.**  
PROJECT : BU3

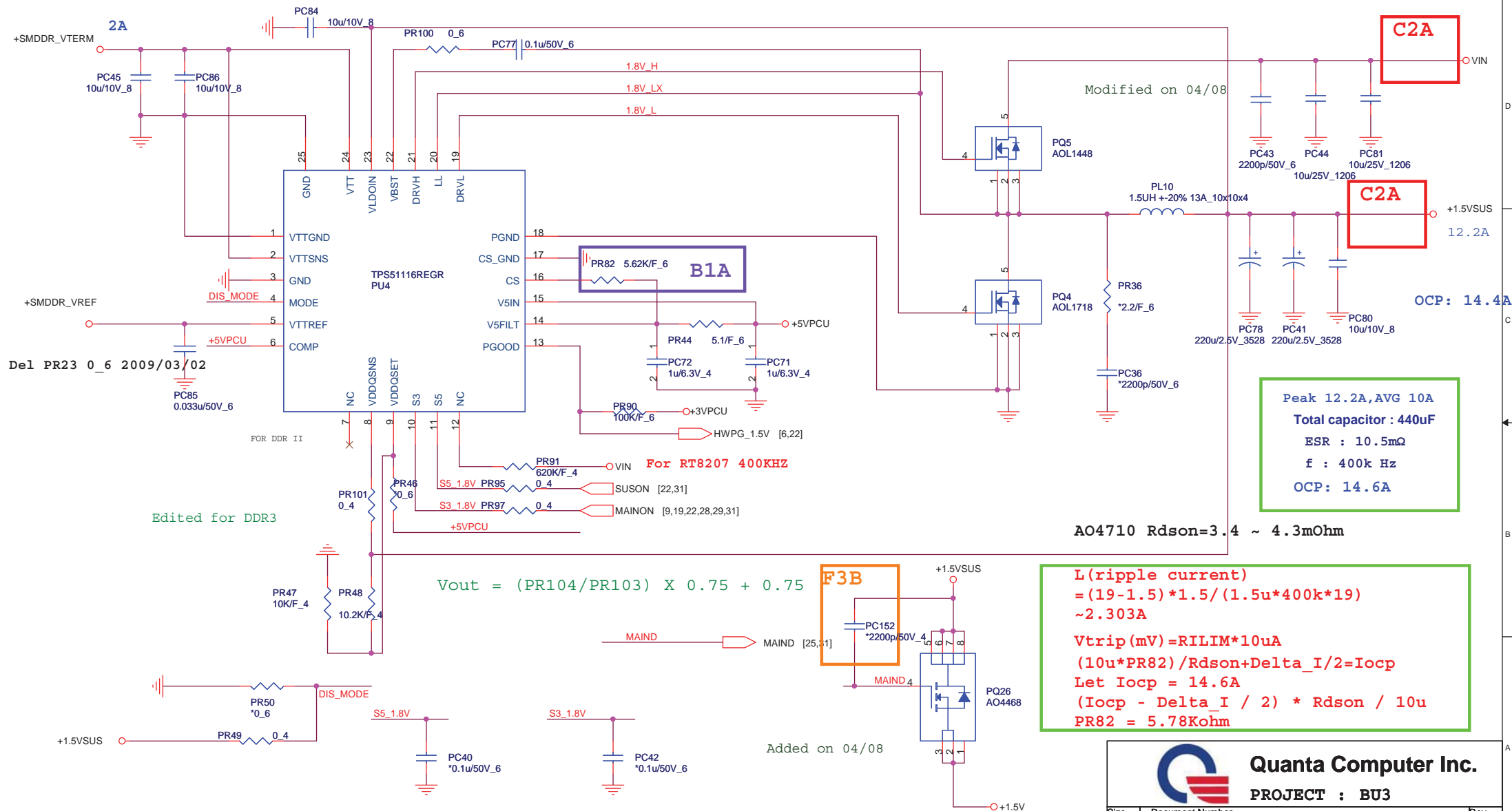
Size	Document Number	Rev
	SYSTEM 5V/3V (ISL6237)	D3B
Date:	Monday, August 10, 2009	Sheet 25 of 34



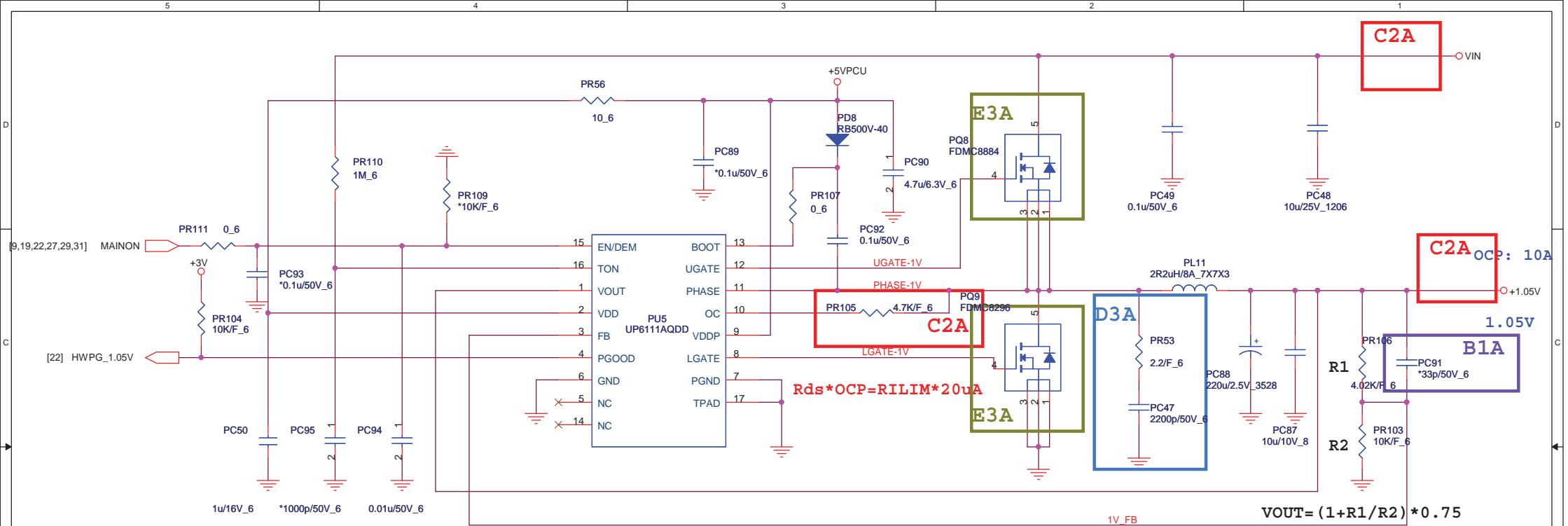


```
Rocset = ( Ioc * Rdroop) / 10uA
Rdroop = 4mV/A
Ioc = Rocset * 10uA / Rdroop = 20.15A
```









$TON = 3.85p \cdot RTON \cdot Vout / (Vin - 0.5)$   
 $TOFF = (Vin / Vout - 1) \cdot Ton$   
 $TON = 2.185 \cdot 10^{-7}$   
 $TOFF = 3.736 \cdot 10^{-6}$   
 $Frequency = 1 / (Ton + Toff) \sim 253K$

FDMC8296 Rdson = 8 mOhm

$L(\text{ripple current})$   
 $= (19 - 1.05) \cdot 1.05 / (2.2u \cdot 253k \cdot 19)$   
 $\sim 1.78A$

$Let Iocp = 10A$   
 $Iocp - Iripple / 2 = RILIM \cdot 20u / Rdson$   
 $10 - 1.78 / 2 = RILIM \cdot 20u / 8mohm$   
 $RILIM = 3.644Kohm$

(Peak 21.199A, AVG 8A)  
 Total capacitor : 230 uF  
 ESR : 21mΩ  
 f : 253k Hz  
 OCP : 10A



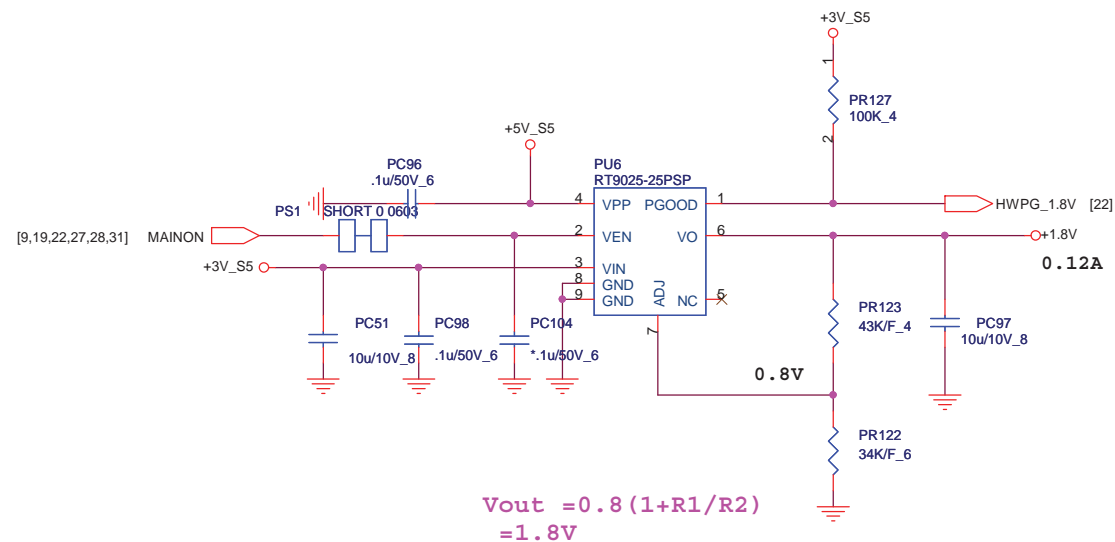
Quanta Computer Inc.

PROJECT : BU3

Size	Document Number	Rev
	VCCP 1.05V(UP6111AQDD)	D3B

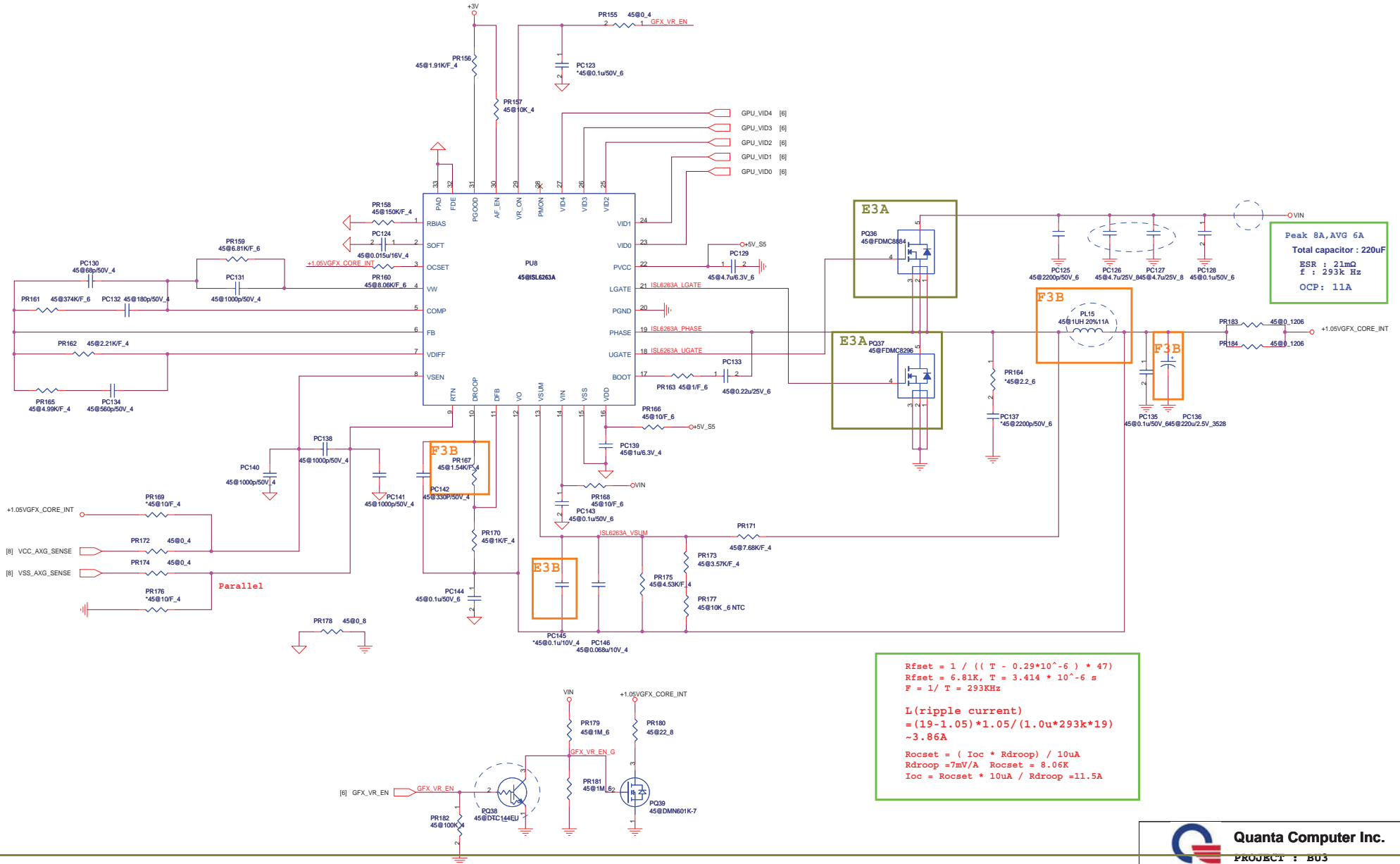
Date: Monday, August 10, 2009 Sheet 28 of 34



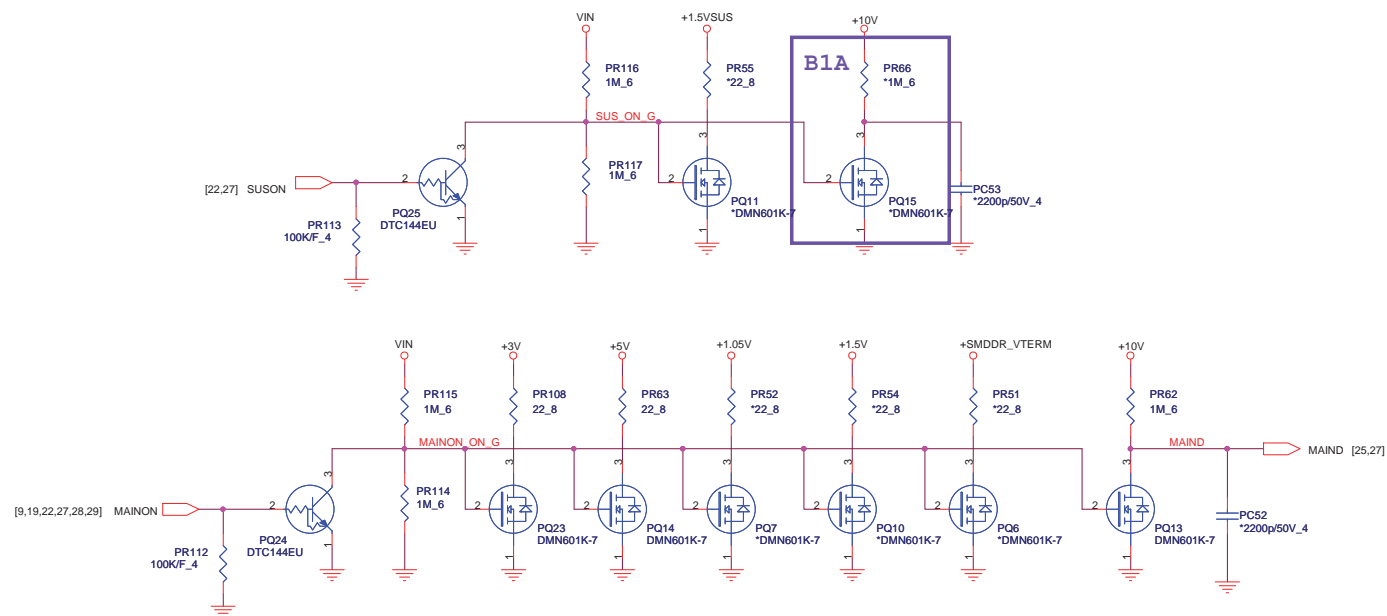




E3A










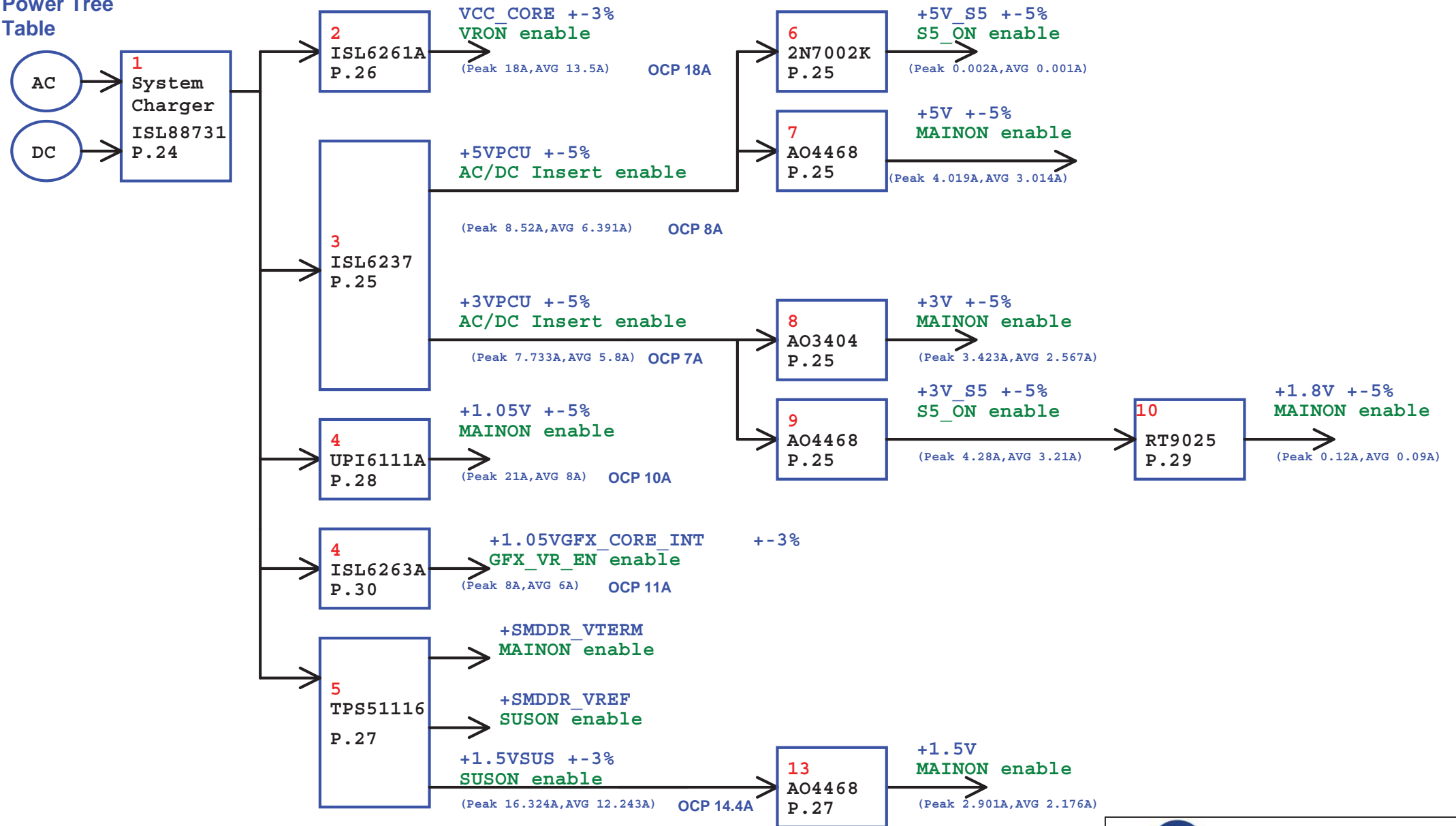




Model		REV	CHANGE LIST				MODEL			BU3		
							PAGE	FROM			To	
BU3 MB	D3A	PAGE 26: Add PR146,PR147,PR148 value 0_4 ,PR149 value 10K/F_4 for power suggest						1	1A			1B
		PAGE 22: Add D22 for ESD/EOS suggestion - Power pin EOS						2	1A			1B
		PAGE 22: C386,C382,RP21不上件						3	1A			1B
		PAGE 02: change C373,C374 value to 33p/50V_4 for XTAL report						4	1A			1B
		PAGE 20: reserve Q31,R381,R380,C383,C384,C385						5	1A			1B
	E3A	PAGE 17: reserve CRT FILTER R390,R393,R394,C398,C399,C400,C401,C402,C403 for EMI requirement.						6	1A			1B
		PAGE 21: add C390,C391,C392,C393,C394,C395,C396,C397 for EMI requirement .						7	1A			1B
		PAGE 30: add 1.05v GFX SCHEMATIC for reader stand by function (GS45 only)						8	1A			1B
		PAGE 28: change PQ8 and PQ9 value and footprint .						9	1A			1B
		PAGE 17: Add R3,R2 BOI-OPTION for GS40.						10	1A			1B
	F3A	PAGE 17: Add R392 ,R391 for Board ID3						11	1A			1B
		PAGE 21: Add HOLE 9,HOLE 11, HOLE 10.						12	1A			1B
		PAGE (12) :Change R244 to bead 120ohm, C324 to 22PF for EMI requirement.						13	1A			1B
		PAGE (24) : Add PR88, PR35 for Adapter Voltage monitor						14	1A			1B
		PAGE (17) : Reserve U25 for LVDS_VADJ option (support XP function key).						15	1A			1B
		PAGE (25) : Reserve PC147,PC148,PC149,PC150,PC151,PC152 for power soft start						16	1A			1B
		PAGE (21) : Change CN9 connector pin define to 40 pin						17	1A			1B
		PAGE (17) : Change D1 footprint						18	1A			1B
		PAGE (18) : Change HDMI CN11 connector PIN DEFINE						19	1A			1B
		PAGE (22) : R176,RP7,RP8,L2,R138,R161,R377,R199,R251,R351,R213,R225,R211,R373,R357,R240,R212,R217,R175,R342,R155,R48,R59,R112,R111,R130,R131,R288,R284,R62,R91,R41,R134 replace by short pad						20	1A			1B
		PAGE (22) : R378,R68,R279,R12,RP17,RP15,RP16,RP14,RP13,RP12,RP11,RP10,RP9,R293,R8 replace by short pad						21	1A			1B
		PAGE (22) : Change CN9 pin define. 40PINS						22	1A			1B
		PAGE (30) : Change PL15 from 2.2uH to 1uH , PC145 change to unmounted , PR167 change to 1.54K , PC136 should be mounted for 3D hang up issue.						23	1A			1B
		PAGE (09) : reserve C186,C149,C269,C247,C113,C342,C154,C135 for cost down						24	1A			1B
								25	1A			1B
								26	1A			1B
								27	1A			1B
								28	1A			1B
								29	1A			1B
								30	1A			1B
DOC NO. 204		PROJECT MODEL : BU3		APPROVED BY: Mosy Li		DATE: 2009/04/27		<div> Quanta Computer Inc.</div> <div>PROJECT : BU3</div> <div>Change list</div> <div>Date: Monday, August 10, 2009 Sheet 32 of 33</div>				
PART NUMBER: 31BU3MB0000		DRAWING BY: Mosy Li		REVISION: 1B								



# Power Tree Table



Quanta Computer Inc.

PROJECT : BU3

Size	Document Number	Rev
	Power Tree Table	D3B
Date:	Monday, August 10, 2009	Sheet 34 of 34