

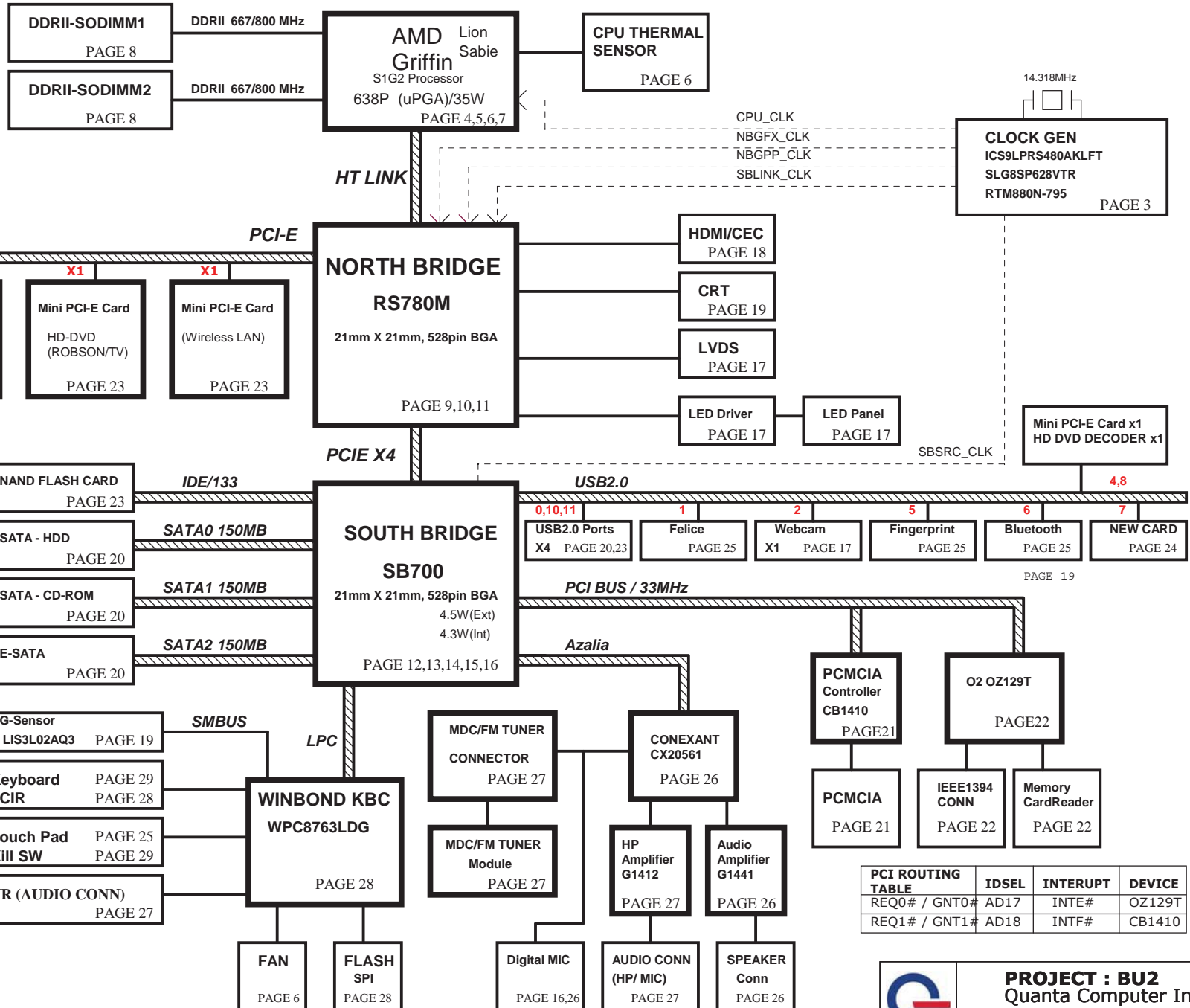
## PCB STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1  
LAYER 4 : SVCC  
LAYER 5 : IN2  
LAYER 6 : IN3  
LAYER 7 : SGND1  
LAYER 8 : BOT

# BU2 SYSTEM DIAGRAM



01



PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ0# / GNT0#	AD17	INTE#	OZ129T
REQ1# / GNT1#	AD18	INTF#	CB1410

**PROJECT : BU2**  
Quanta Computer Inc.

Size Custom

Document Number  
**BLOCK DIAGRAM**

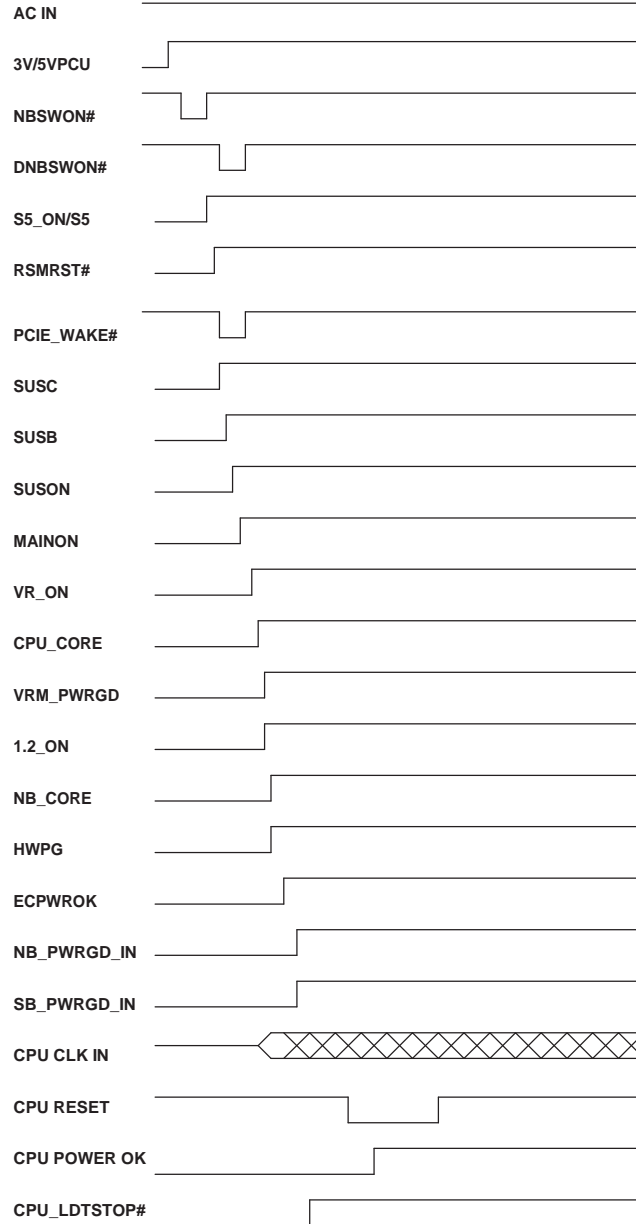
Date: Wednesday, January 30, 2008 | Sheet 1 of 35

Rev 1A

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2	SYSTEM INFORMATION	
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22	OZ129T(5IN1/1394)	
23	MINI CARD & NAND FLASH CARD	
24	NEW CARD & RJ45 BOARD/BEEP	
25	TP/FP/BT/PB/FELICA/MMB CONN	
26	CONEXANT(CX205601)/SPK/AMP	
27	JACK/VR/FM/MIC/MDC/AMPLIFIER	
28	EC(KBC)-WPCPC8763/WPC8769	
29	KEYBOARD/LED/KILL SW/HOLE	
30	CHARGER (ISL6251A)	
31	SYSTEM 5V/3V (ISL6237)	
32	AMD GRIFFIN (ISL6265)	
33	+NB_CORE (RT8202)	
34	DDR 1.8V(TPS51116)	
35	DISCHARGE (1.25V/1.5V)	

## Power Sequence



02

### SB700 SM BUS

SB700 SMBUS	SMBUS Function Define
SMBCLK0 SMBDAT0	DDR / DDR THER / CLOCK GEN (+3V)
SMBCLK1 SMBDAT1	Mini Card/New Card (+3VS5)
SMBCLK2 SMBDAT2	HDMI CEC (+3VS5)

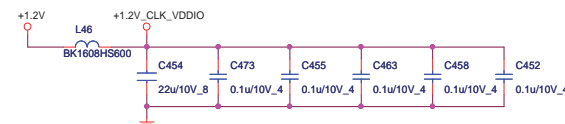
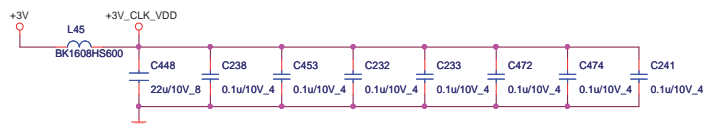
### KBC(EC) SM BUS

KBC SMBUS	SMBUS Function Define
MBCLK MBDAT	BATTERY (+3VPCU)
2ND_MBCLK 2ND_MBDATA	CPU THER / SENSOR/EC (+3V/PCU)
3ND_MBCLK 3ND_MBDATA	HDMI CEC / TOUCH SEN(+3VS5)



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Quanta Computer Inc.

Size Custom	Document Number <b>SYSTEM INFORMATION</b>	Rev 1A
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ICS9LPRS480

P/N :

SLG8SP628

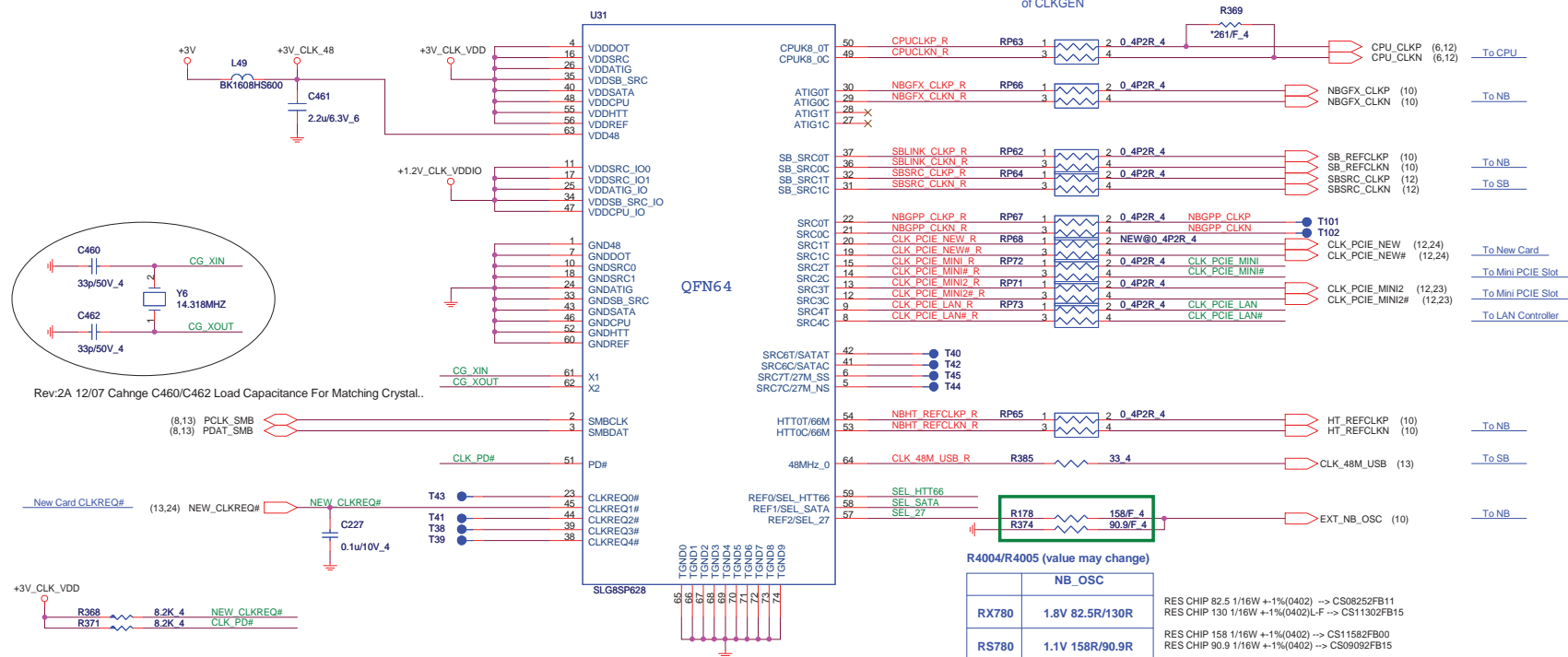
P/N : AL8SP628000

RTM880N-796

P/N : AL000880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN



## NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

## R4004/R4005 (value may change)

	NB_OSC
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

RES CHIP 82.5 1/16W +/-1%(0402) -> CS08252FB11  
 RES CHIP 130 1/16W +/-1%(0402)L-F -> CS11302FB15  
 RES CHIP 158 1/16W +/-1%(0402) -> CS11582FB00  
 RES CHIP 90.9 1/16W +/-1%(0402) -> CS09092FB15

## FOR EXTERNAL/INTERNAL CLOCK



Place Close to Drivers Side

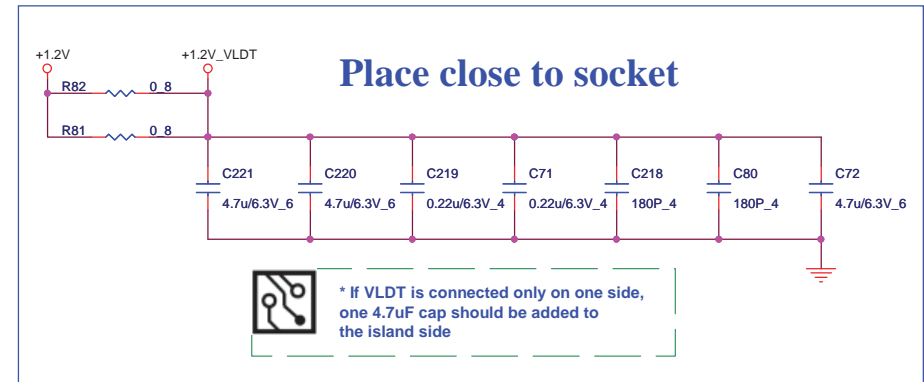
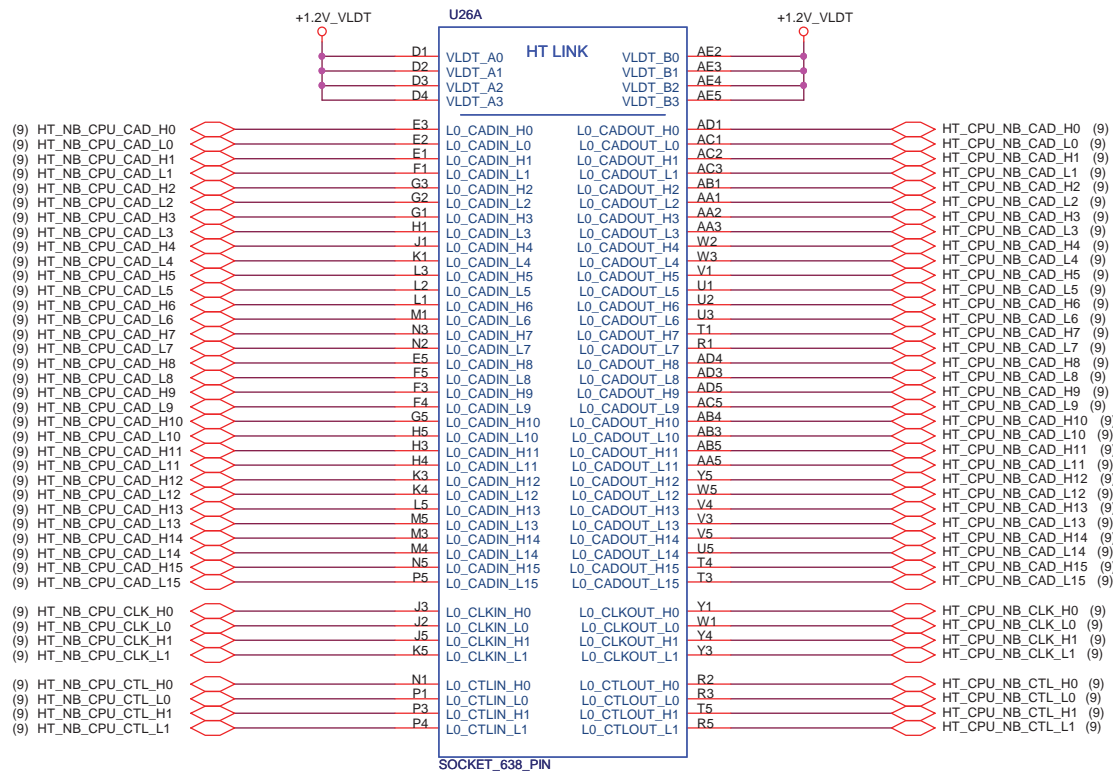
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

\* default

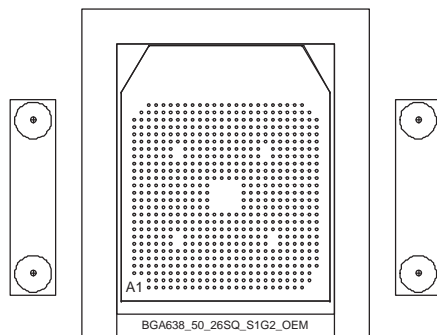


**PROJECT : BU2**  
**Quanta Computer Inc.**

Size Custom Document Number  
**CLK GENERATOR\_SLG8SP628** Rev 1A  
 Date: Thursday, July 24, 2008 Sheet 3 of 35



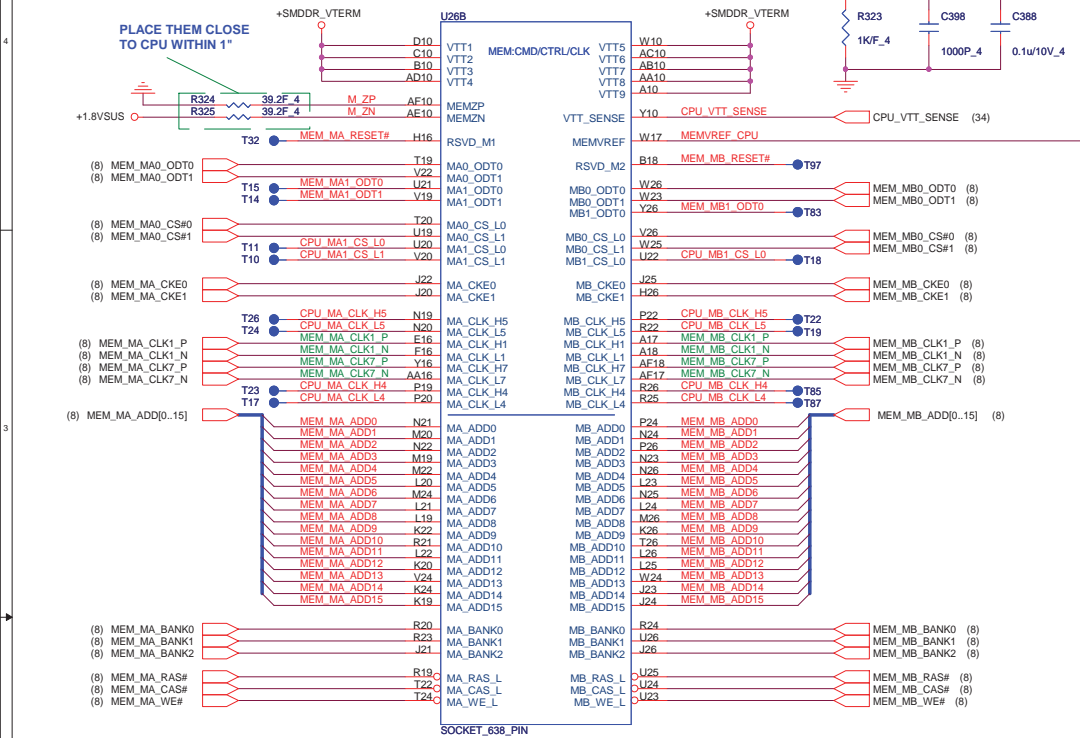
CPU



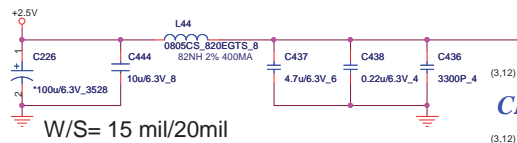
**PROJECT : BU2**  
Quanta Computer Inc.

Size	Document Number	Rev
B	S1G2 HT I/F 1/4	1A
Date: Thursday, July 24, 2008	Sheet 4 of 35	

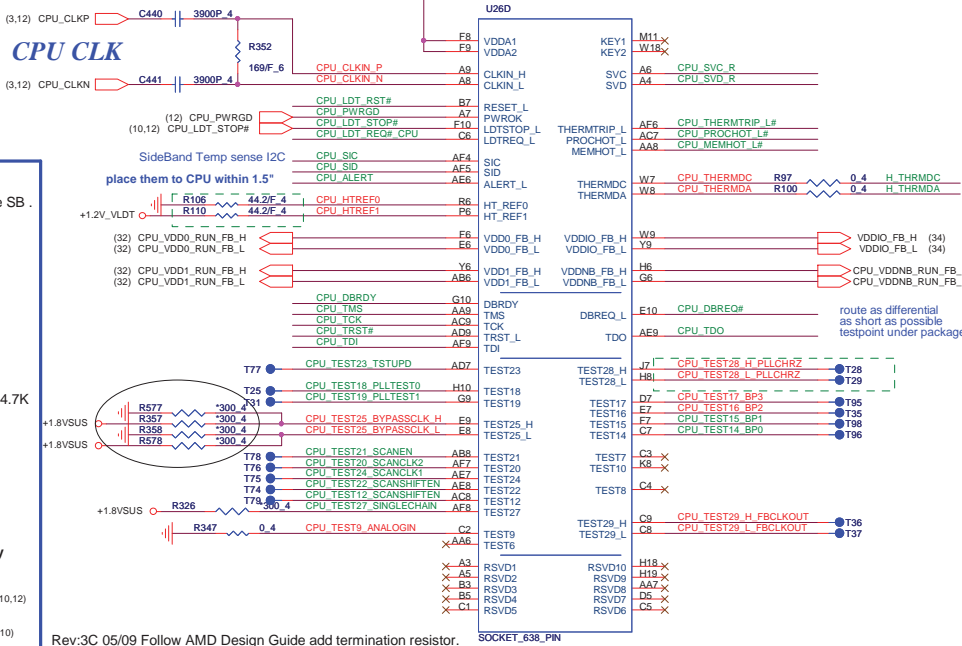
## Processor Memory Interface



*CPU*

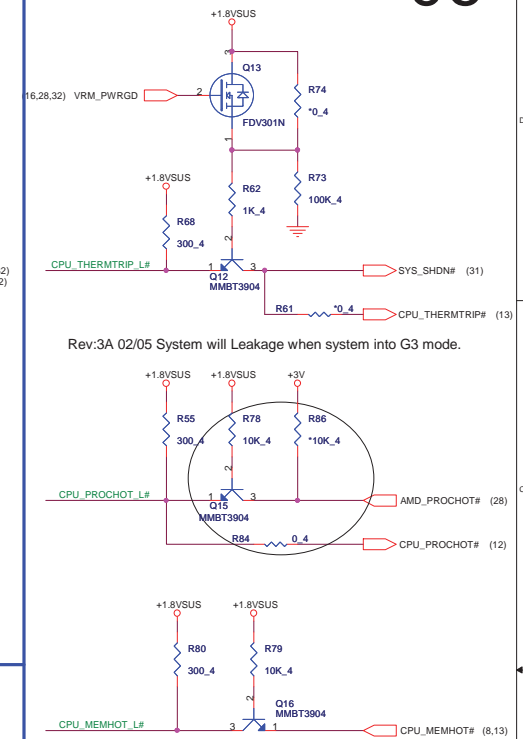


*CPU CLK*

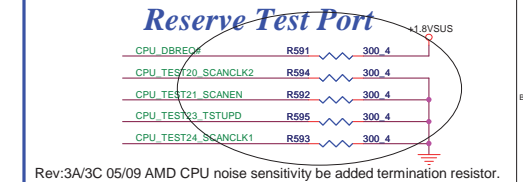


*CPU THERM*

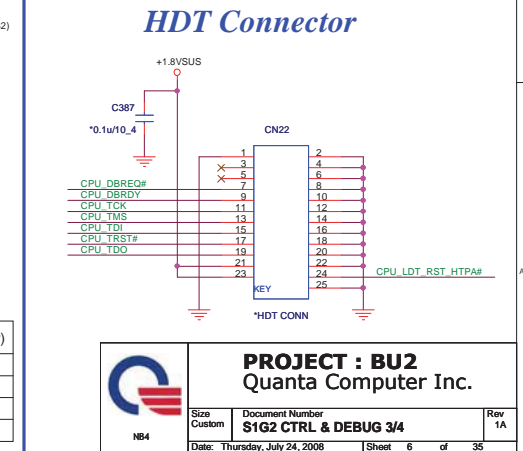
06



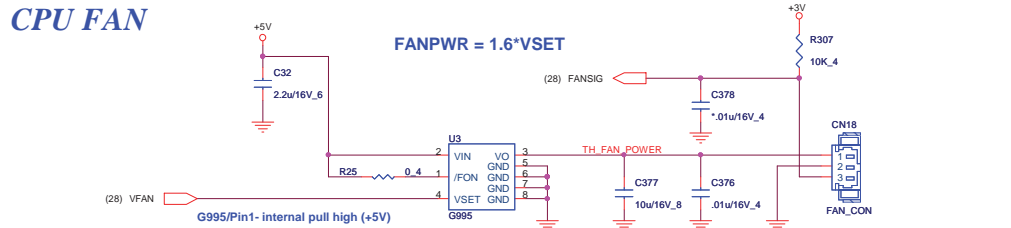
### Reserve Test Port



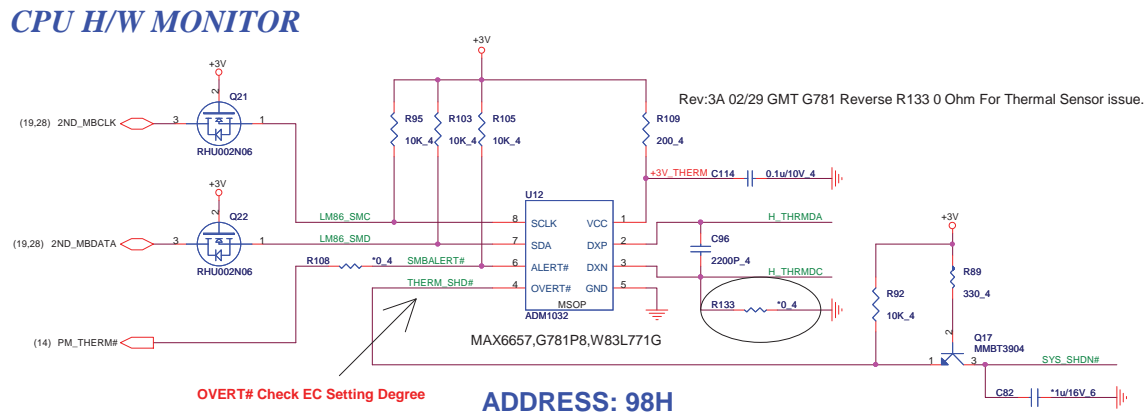
### *HDT Connector*



*CPU FAN*



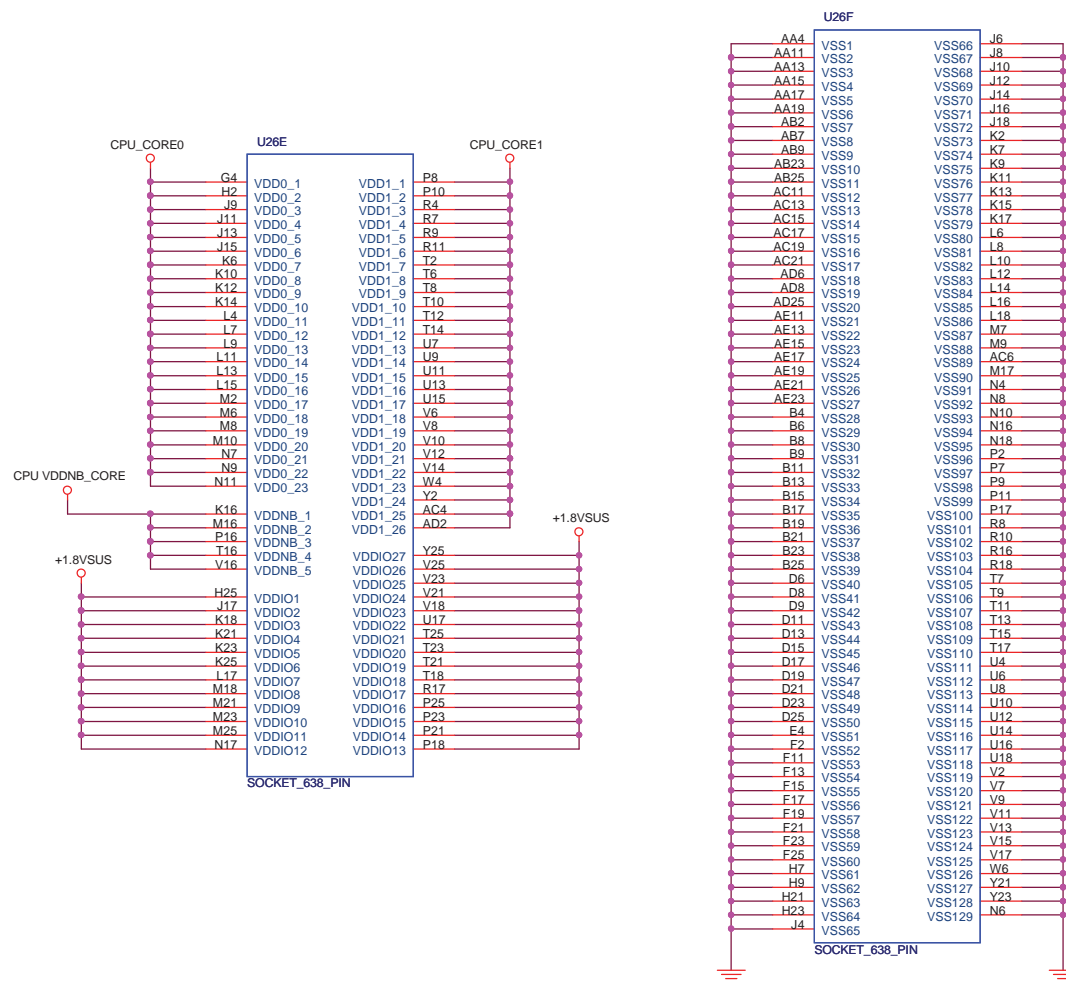
## CPU H/W MONITOR



## Serial VID

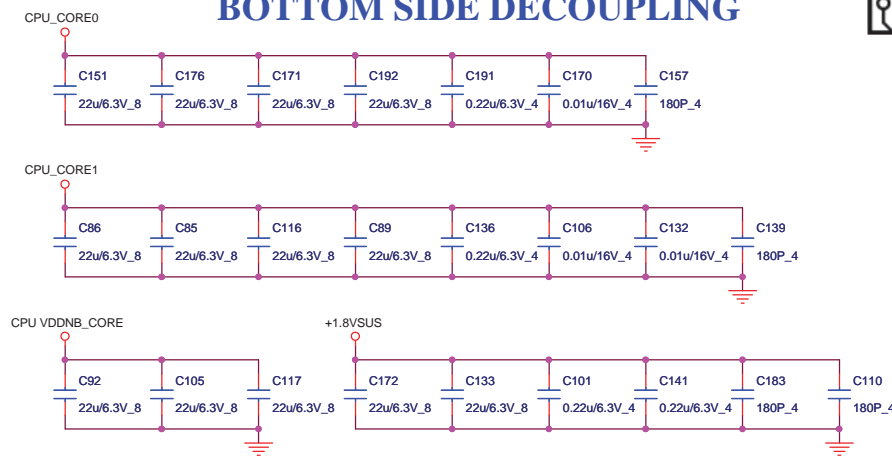
VFIX MODE		VID Override Circuit
SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V



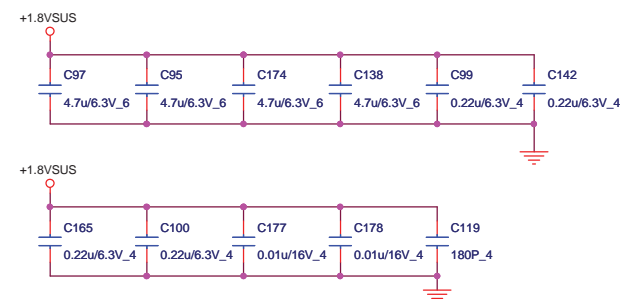


## PROCESSOR POWER AND GROUND

### BOTTOM SIDE DECOUPLING



### DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



[illegible]

Rev:2A 12/13 No-Sutff DDRII H/W Montor Circuit.

ADDRESS: 92H Close DDR2 socket

ADDRESS: 92H Close DDR2 socket

ADDRESS: 92H Close DDR2 socket

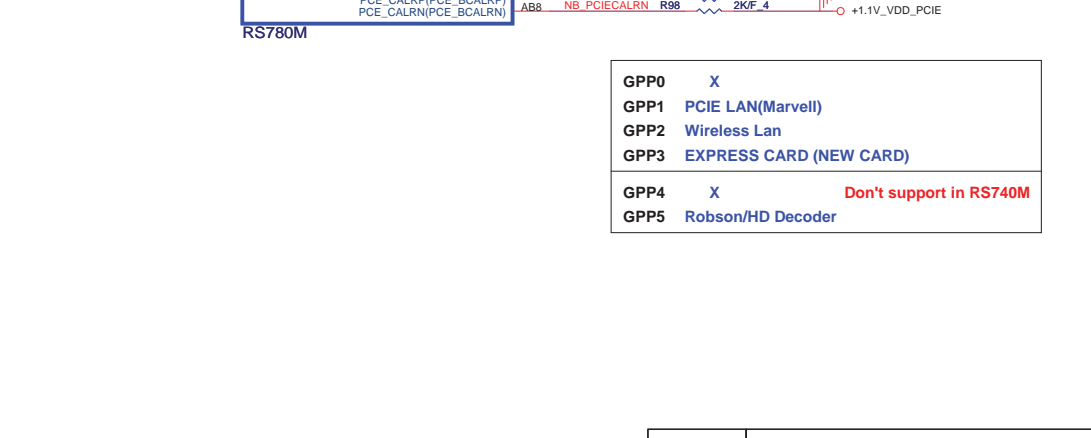
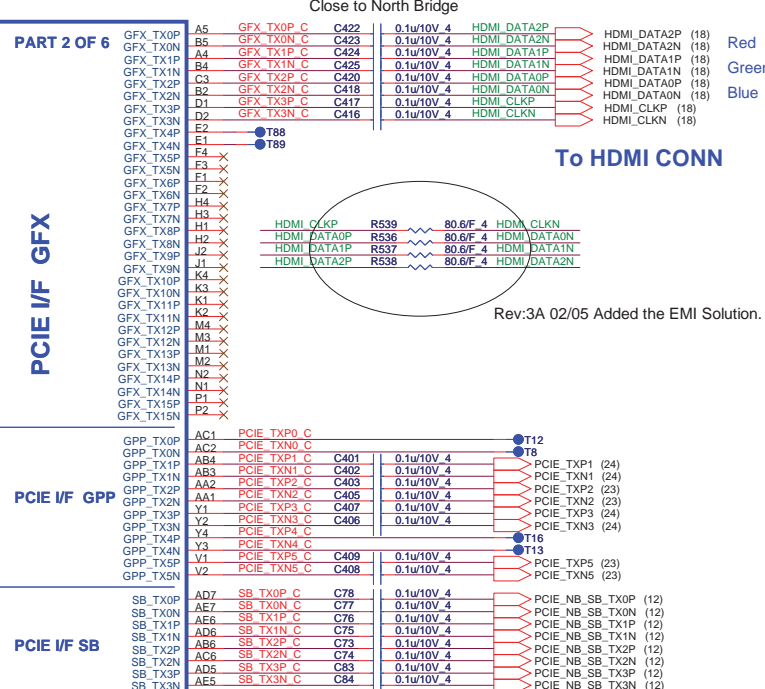
**PROJECT : BU2**  
Quanta Computer Inc.

Size Custom	Document Number <b>DDR2 SODIMMS: A/B CHANNEL</b>	Rev 1A
Date: Thursday, July 24, 2008	Sheet 8 of 35	



NB4

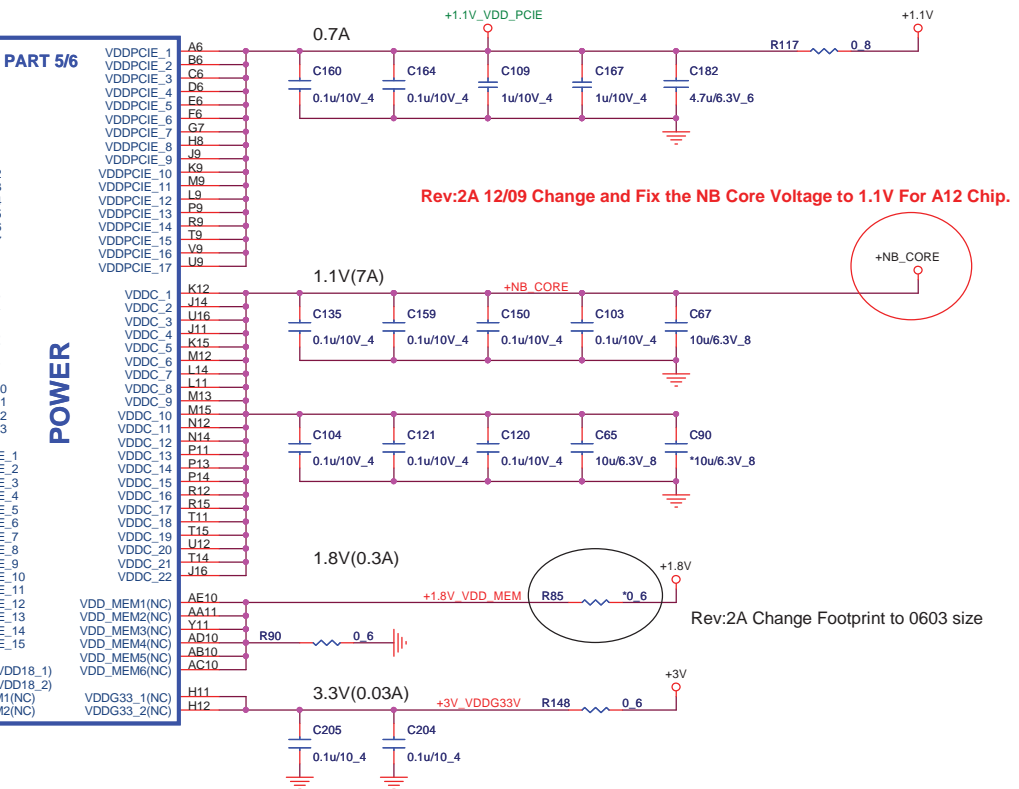
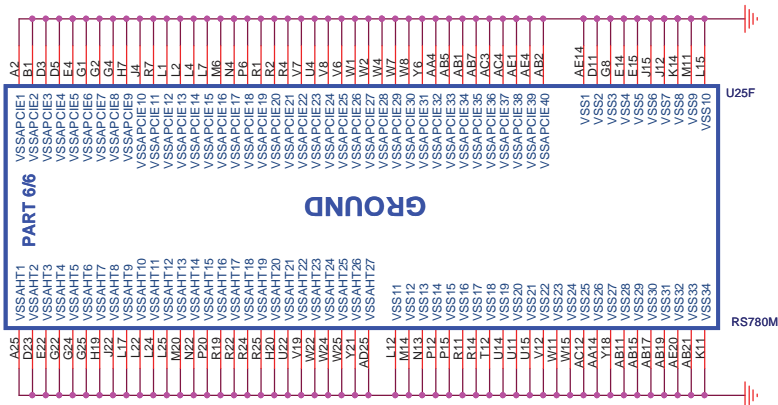






RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDDG18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDDG33	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDLTP33	+3.3V	NC	NC



A11 Chip Bug Errata  
use A12 Chip Can Remove

Rev:2A 12/09 Change VDDHTTX Voltage From 1.35V to 1.2V Rails For A12 Chip.

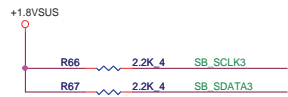
RS780



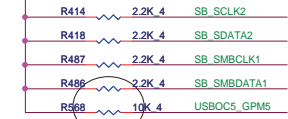
**PROJECT : BU2**  
Quanta Computer Inc.

Size Custom	Document Number <b>RS740/RS780-POWER5/5</b>	Rev 1A
Date: Thursday, April 10, 2008	Sheet 11 of 35	

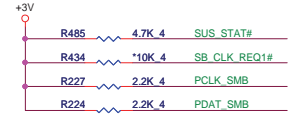




Rev:2A 12/06 Support the New Card Hot Plug Function.



Rev:3B 04/07 USB Overcurrent 5 Pull-up 10K For Open Drain.



Rev:2A 12/06 DEL G-Sensor SCI Event(GPIO).

Rev:3A 02/05 Move Board ID4 Pin Name From GPIO66 to GPIO3.



Rev:3B 04/07 Added the USB Overcurrent 3 to Support USB 2.0 Ports.

Rev:3A 02/05 Move Hot Plug Pin Name From GEVENT5# to GPM1#.

## HD Audio Interface

To Azalia



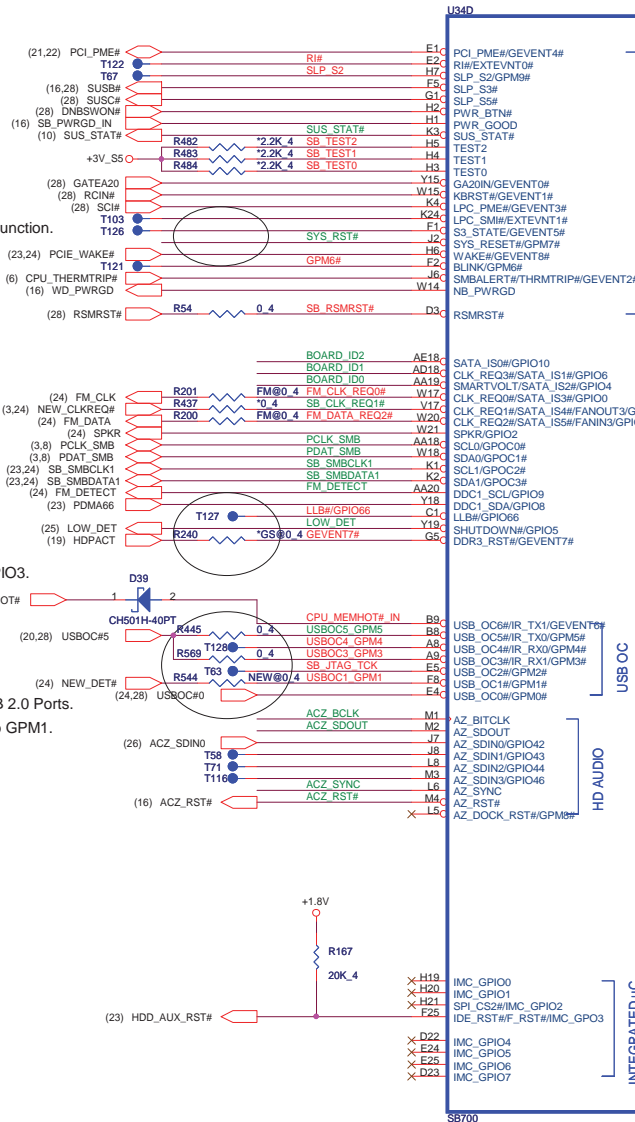
To Azalia



To Azalia



To Azalia



SB700

ACPI / WAKE UP EVENTS

GPIO

USB OC

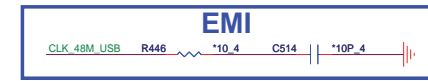
HD AUDIO

INTEGRATED IC

INTEGRATED IC

INTEGRATED IC

INTEGRATED IC



48MHz



Rev:3C 04/08 Reserve the 0hm to USB7 Controller.

Rev:3A 03/03 Swap USB CONN From USB11 to USB7 For Controller ESATA Certification.

Rev:2A 12/11 Swap the New Card From USB7 to USB3 For OHCI Controllers.

E-SATA and USB Connector

TV/HD DECODER Min-Card

USB Connector

BLUETOOTH

FINGERPRINT

Min-Card

NEW CARD

CAMERA USB

Felica

USB Connector(RJ45 USB BOARD)

SPI/LPC define

SPI/LPC define

SPI/LPC define

SPI/LPC define

SPI/LPC define

SPI/LPC define

SPI/LPC define

SPI/LPC define

SPI/LPC define

SPI/LPC define

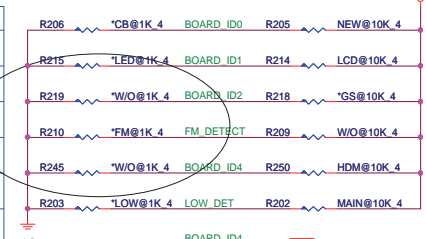
SPI/LPC define

SPI/LPC define

## MB ID Selection Table

BOARD_ID	BOARD_ID0	BOARD_ID1	BOARD_ID2	FM_DETECT	BOARD_ID4	LOW_DET
W/ New Crad W/ Crad Bus	H	L				
W/ CCFL Panel W/ LED Panel		H	L			
W/ G-Sensor W/O G-Sensor			H	L		
W/O FM W/FM				H	L	
W/ HDMI W/O HDMI					H	L
Main Stream Low Cost						H

## MB ID



Rev:3B 04/18 There is internal 8.2K of I/O Balls So Change Pull-Down Resistors From 10K to 1K.



**PROJECT : BU2**  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	SB700-ACPI/GPIO/USB 2/4	
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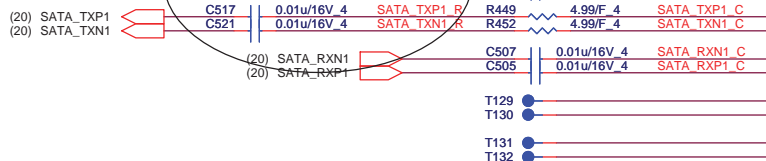
# SB700

PLACE SATA AC COUPLING CAPS CLOSE TO SB700

## SATA HDD

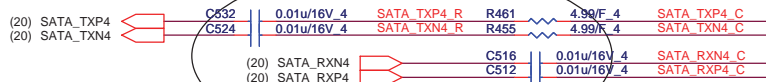


## E-SATA



Rev:3B 04/18 Change HDD Control From Channel/2 to Channel/0 For Spin Down Issue.

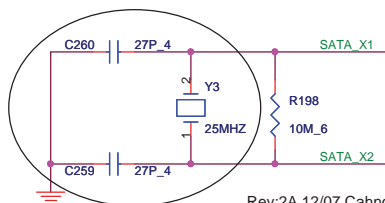
## SATA ODD



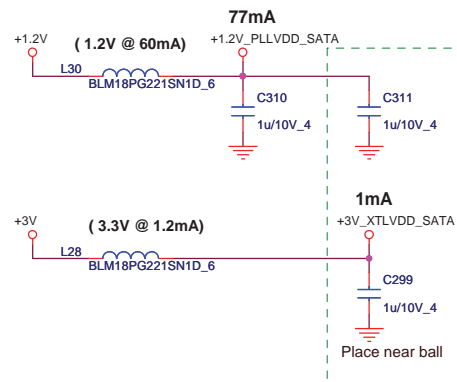
Rev:3A 02/22 Change Setting the SATA ODD to be IDE Legacy class Mode..

### NOTE:

R635 IS 1K 1% FOR 25MHZ XTAL, 4.99K 1% FOR 100MHZ INTERNAL CLOCK



Rev:2A 12/07 Change C259/C260 Load Capacitance For Matching Crystal.



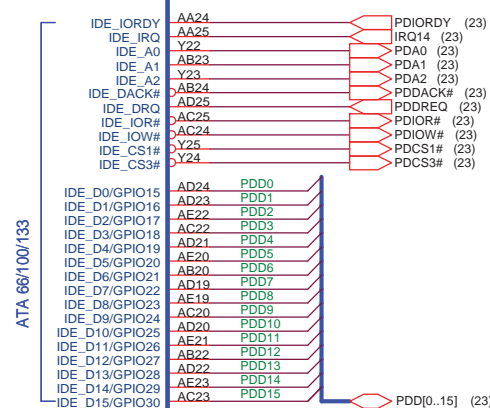
U34B

## SB700 Part 2 of 5

SERIAL ATA

SATA PWR

HW MONITOR



Rev:3C 04/08 Reserve the Board ID For USB Controller.  
Rev:3A 02/05 Added the Board ID4 to GPIO3..

Rev:3C 05/09 Remove Test Ports For Space Limiting.

Rev:3C 05/09 Remove Test Ports For Space Limiting.

Rev:2A 12/07 Change +3V Domain For System Leakage When System into S5 Mode.



**PROJECT : BU2**  
**Quanta Computer Inc.**

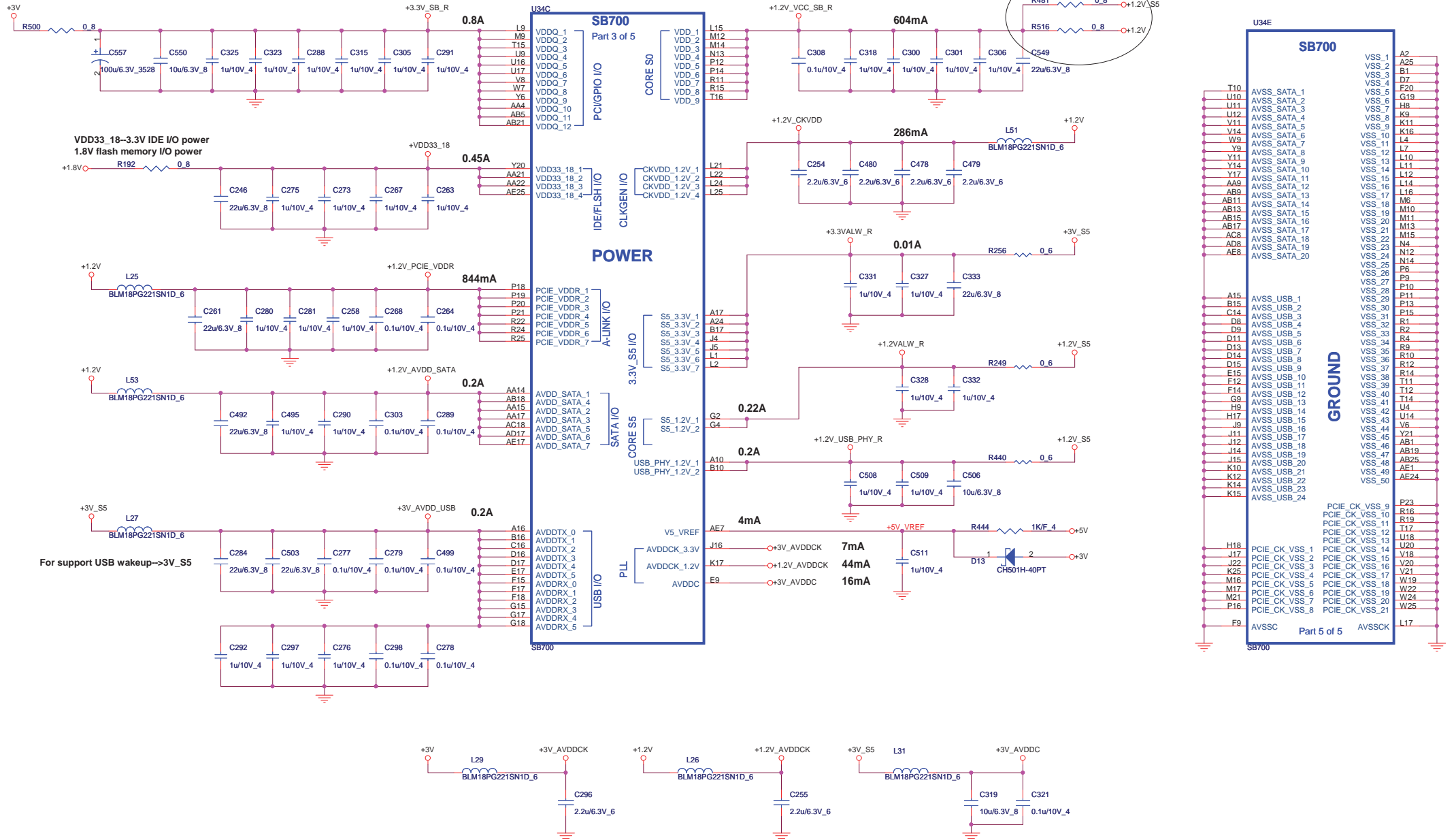
Size Custom	Document Number <b>SB700-ACPI/GPIO/USB 2/4</b>	Rev 1A
Date: Thursday, July 24, 2008	Sheet 14 of 35	

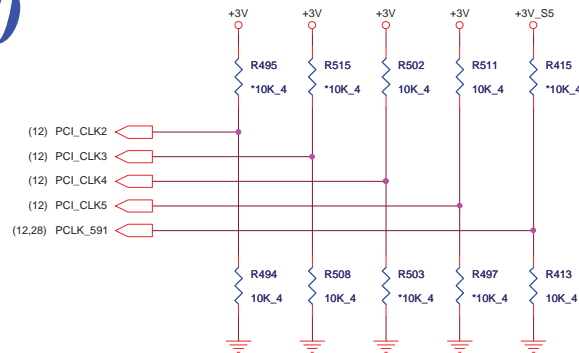


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

Rev:2A 12/10 The VDD Power Pin to be connected to S0\_1.2V Power For A12 Chip.

A11 Chip Bug  
use A12 Chip Can Remove

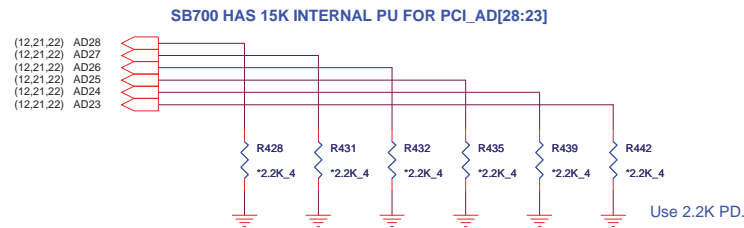




## REQUIRED STRAPS

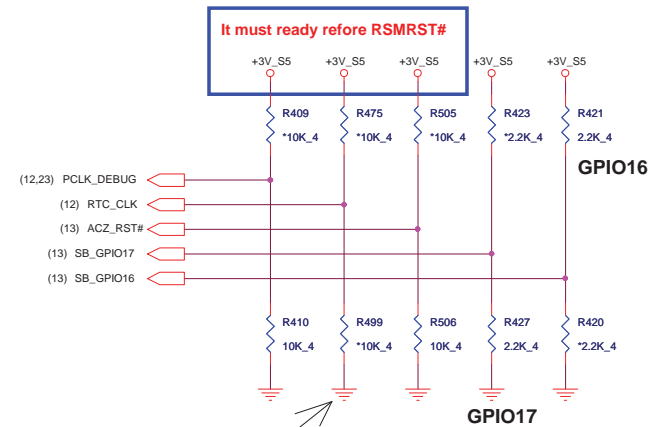
PULL	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0
	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED  DEFAULT	IGNORE DEBUG STRAPS  DEFAULT			DISABLE PCI MEM BOOT  DEFAULT

## DEBUG STRAPS



## REQUIRED STRAPS

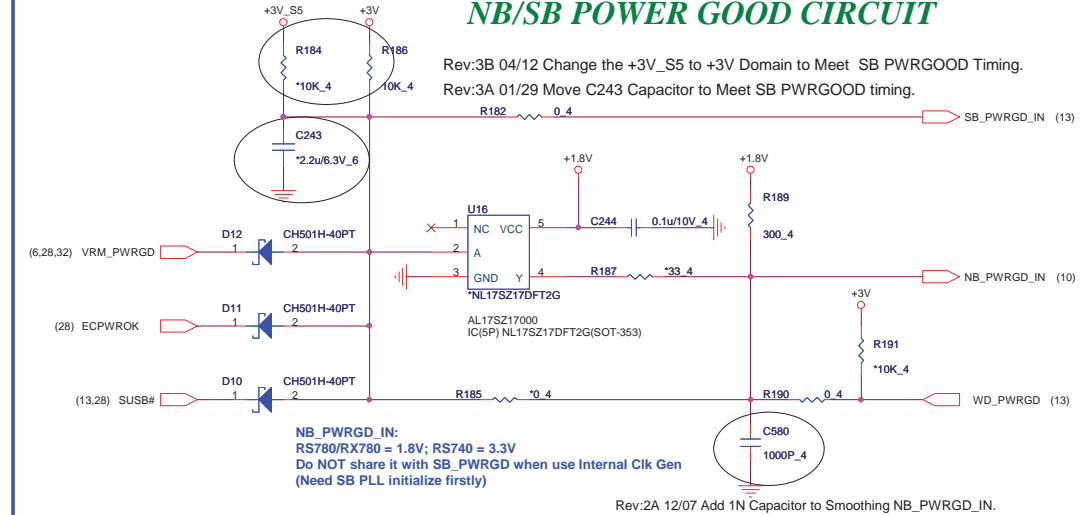
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

PULL	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17	GP16
	CLKGEN ENABLED	INTERNAL RTC  DEFAULT	EC ENABLED		ROM TYPE: H, H = Reserved  H, L = SPI ROM
PULL LOW	CLKGEN DISABLED  DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED  DEFAULT		L, H = LPC ROM L, L = FWH ROM  DEFAULT

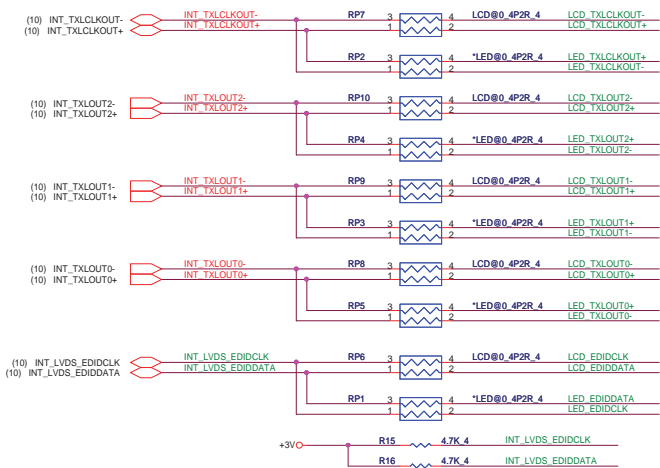
## NB/SB POWER GOOD CIRCUIT



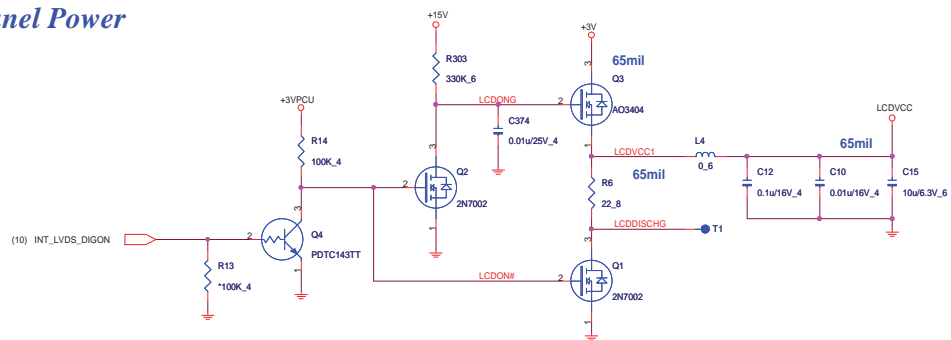
**PROJECT : BU2**  
Quanta Computer Inc.

Size Custom	Document Number <b>SB700-STRAPS &amp; PWRGD</b>	Rev 1A
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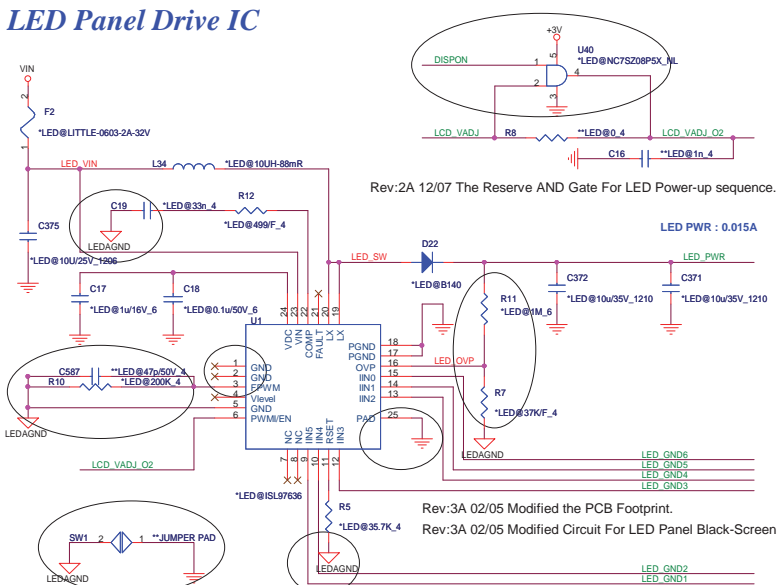
### Panel Source



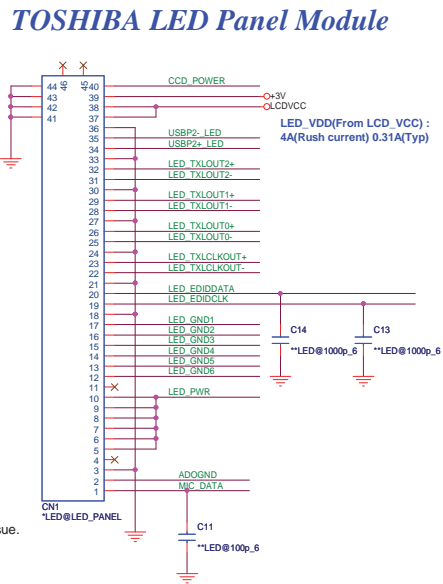
### *Panel Power*



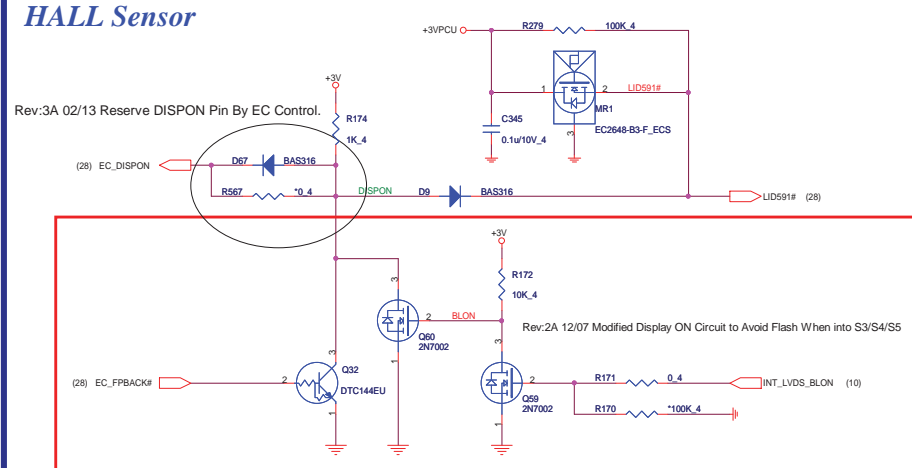
## LED Panel Drive IC



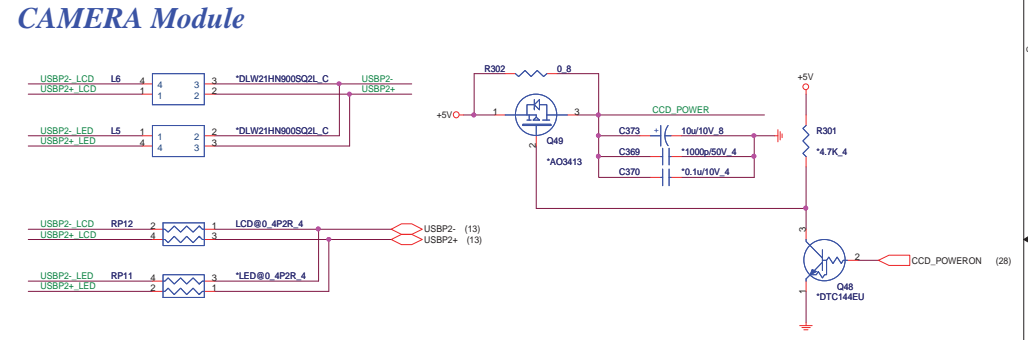
## *TOSHIBA LED Panel Module*



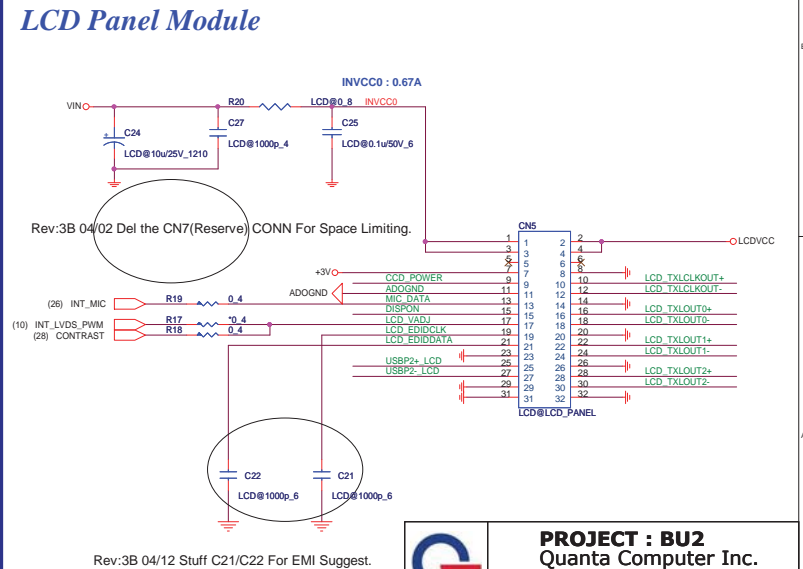
## HALL Sensor

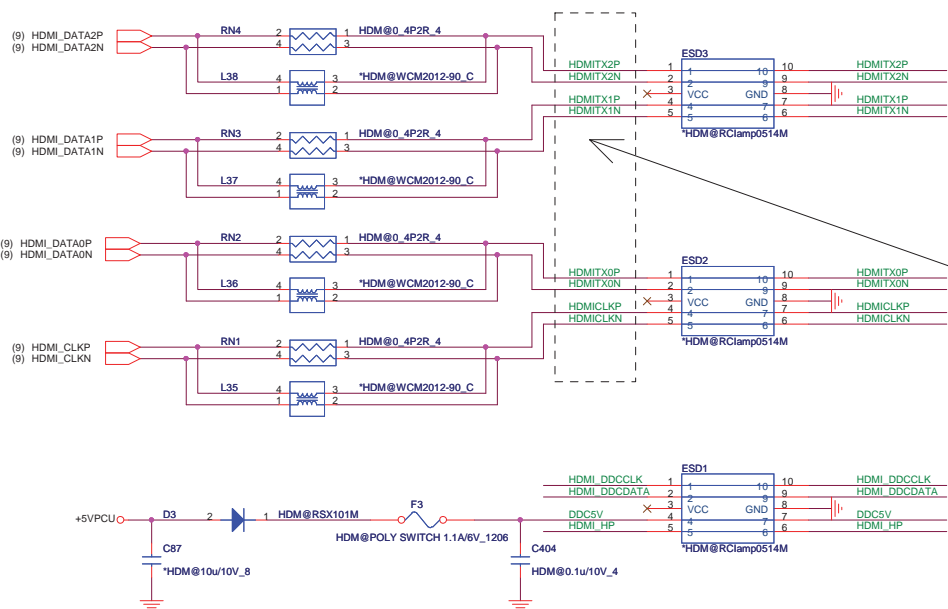


## CAMERA Module

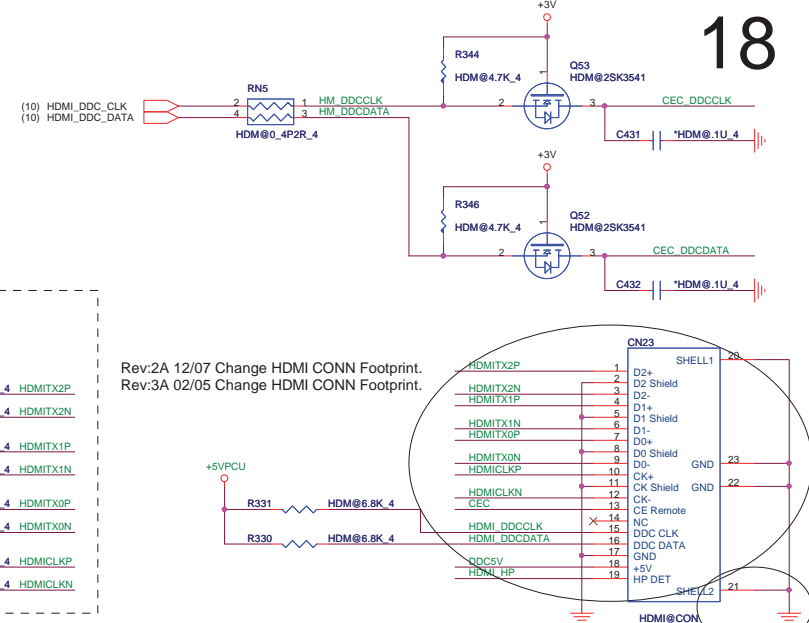
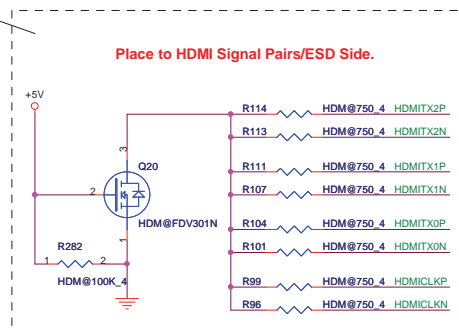


## LCD Panel Module



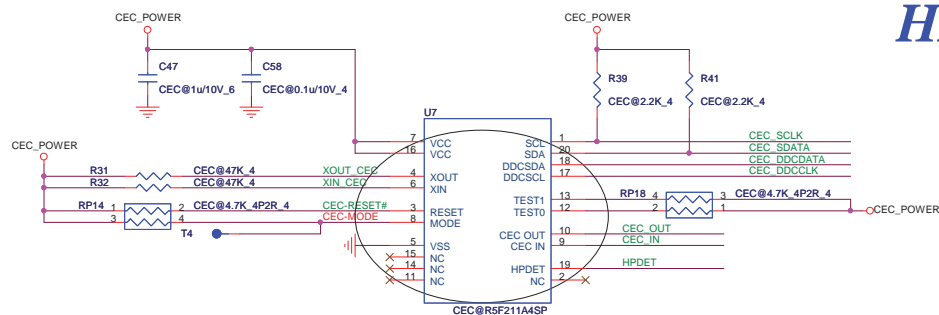


## HDMI

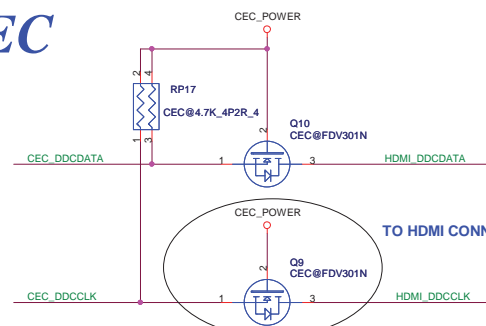


Rev:3A 02/05 Change PIN20/21/22/23 To Ground For ESD. EMI GROUND

## HDMI-CEC

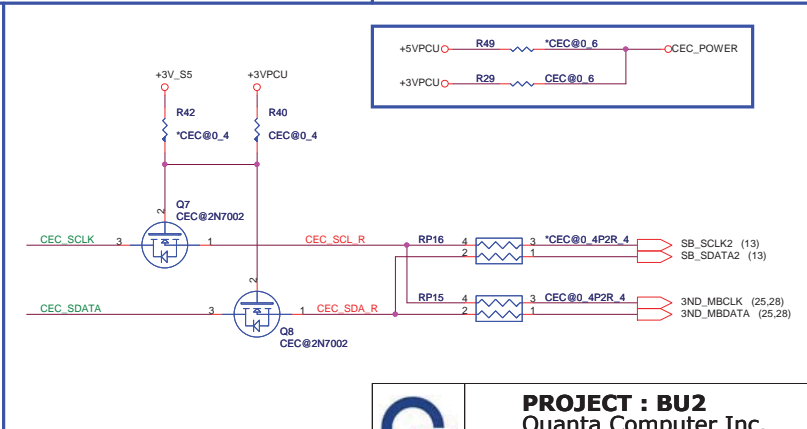
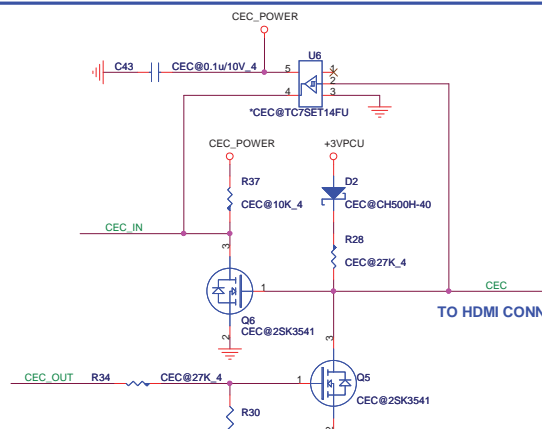
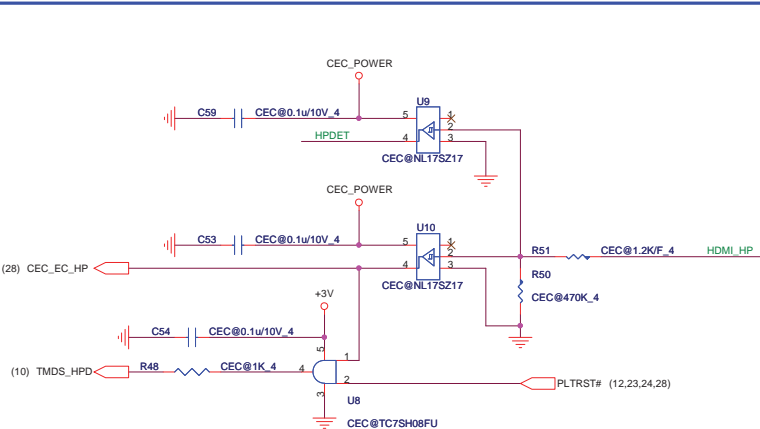
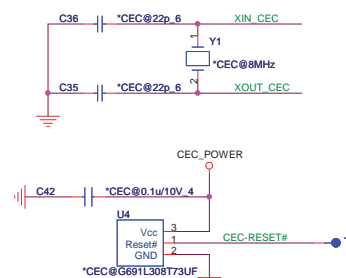


Rev:3A 03/03 Change the CECC V1.10 (P/N R5F211A4C22SP)

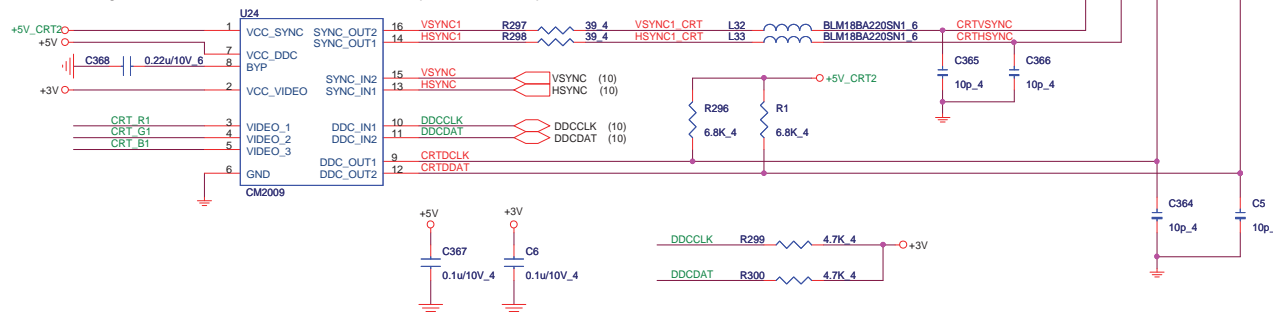
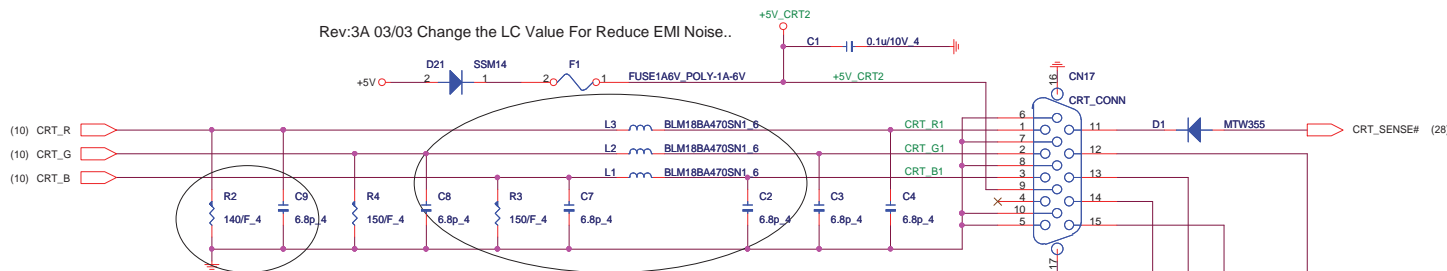


Rev:2A 12/07 Level Shift Circuit Wrong Change to Pull-up CEE\_POWER Domain.

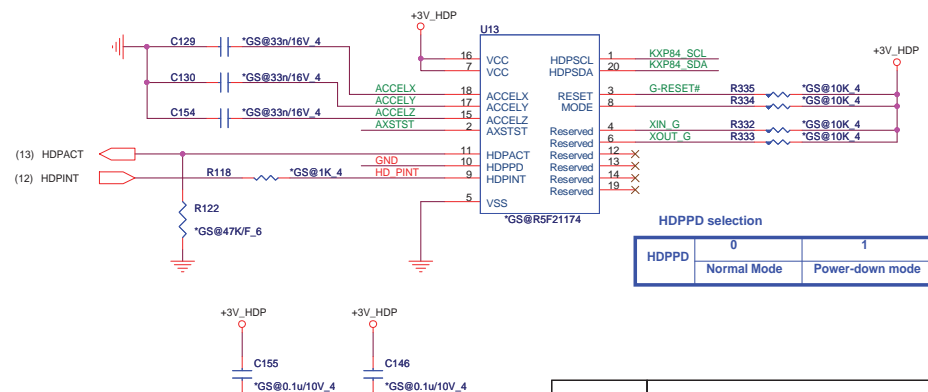
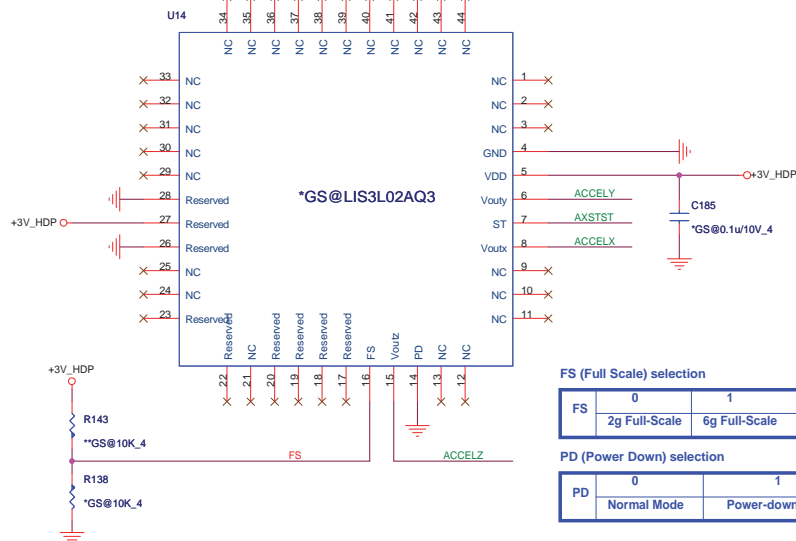
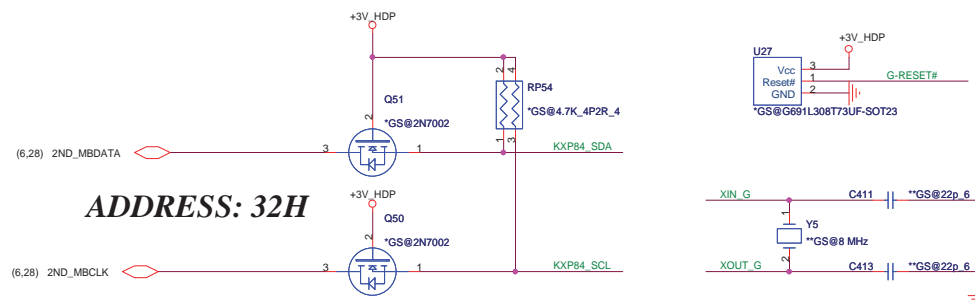
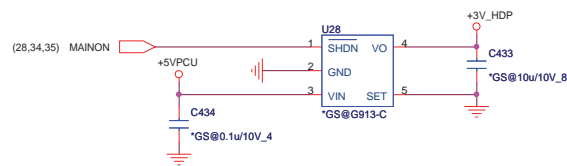
## Clock/Test Pad



Rev:3A 03/03 Change the LC Value For Reduce EMI Noise..



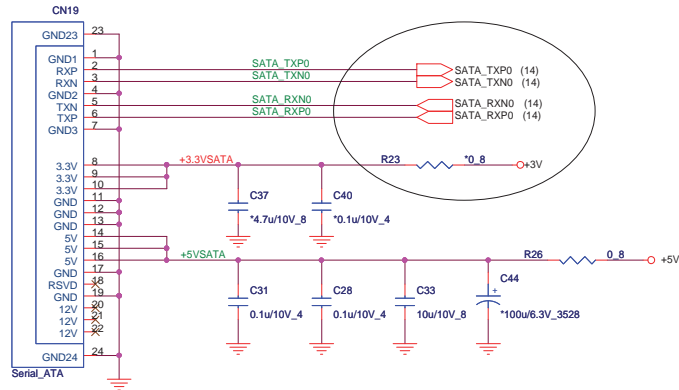
## G-SENSOR



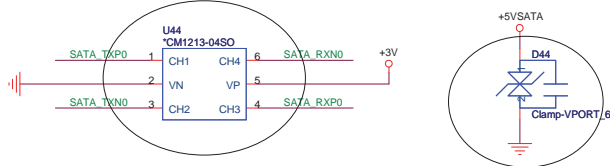
Close to Pin 7 and Pin 16

<http://hobi-elektronika.net>

# SATA HDD



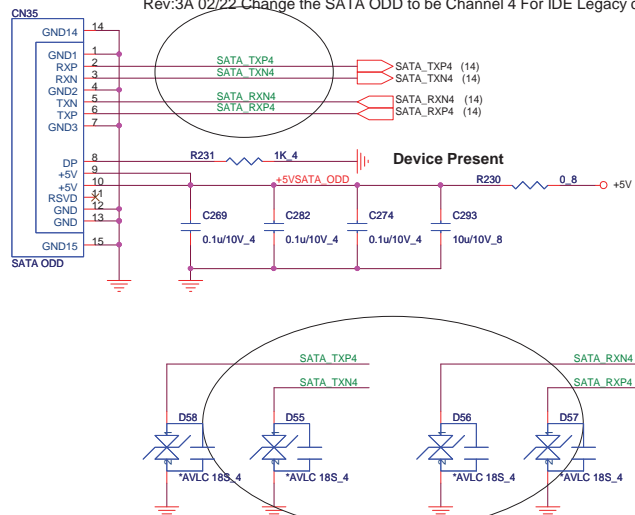
Rev:3B 04/18 Change HDD Control From Channel/2 to Channel/0 For Spin Down Issue.



Rev:3B 04/18 Remove D51/D52/D53/D54 Varistor And Change to U44 CM1213-04SO ESD Protection Arrays.

# SATA ODD

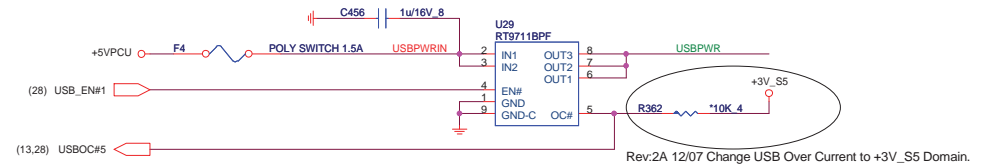
Rev:3A 02/22 Change the SATA ODD to be Channel 4 For IDE Legacy class Mode..



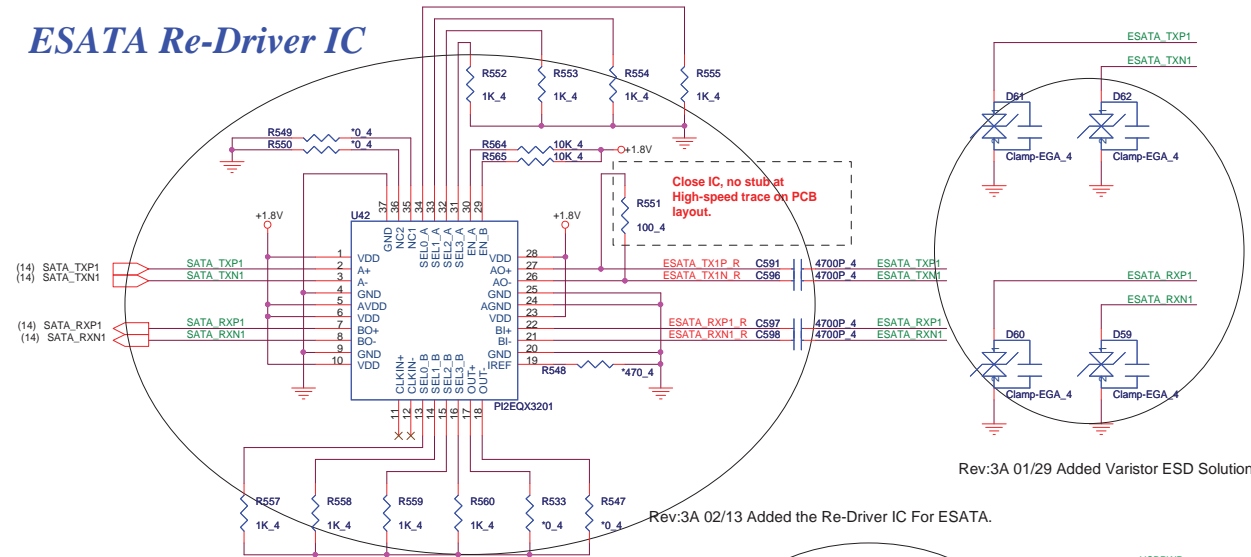
Rev:3A 01/29 Added Varistor ESD Solution.

# USB & ESATA

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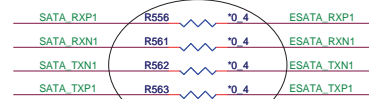
## ESATA Re-Driver IC



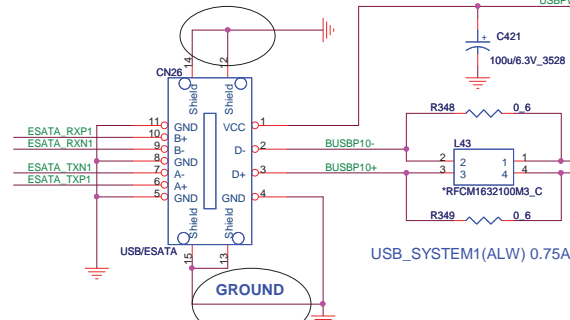
Rev:3A 01/29 Added Varistor ESD Solution.

Rev:3A 02/13 Added the Re-Driver IC For ESATA.

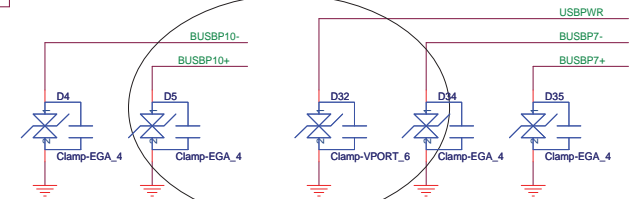
SEL0_X	SEL1_X	Eq	SEL2_X	Swing	SEL3_X	De-Emphasis
0	0	0dB	0	1.0X	0	0dB
0	1	2.5dB	1	1.2X	1	-3.5dB
1	0	4.5dB				
1	1	6.5dB				



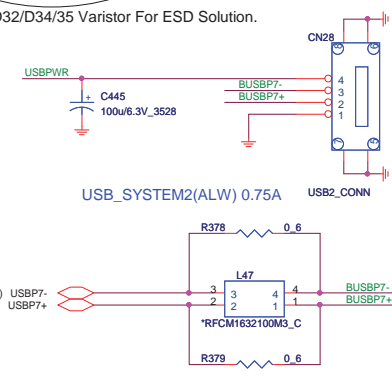
Rev:3A 02/05 Added PIN12/14 To Ground For ESD.



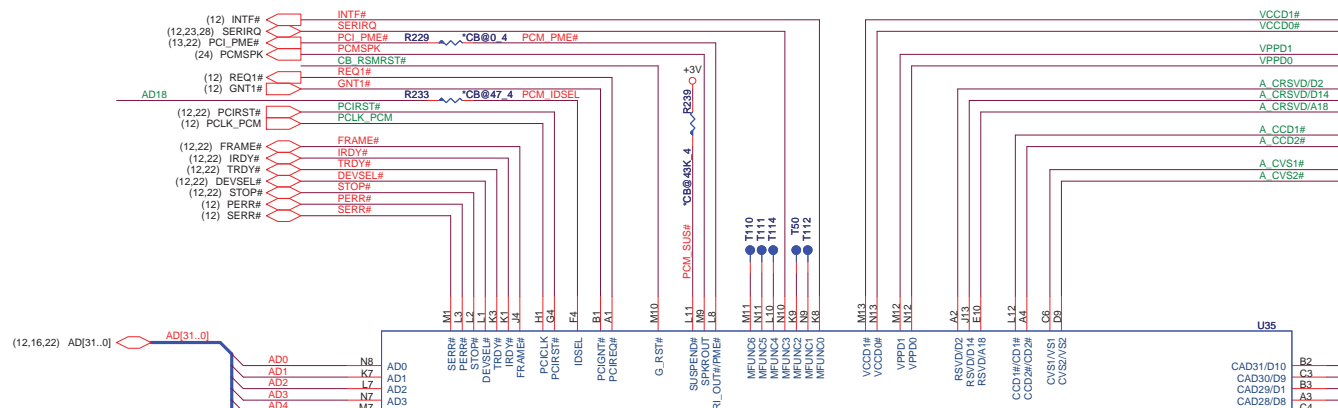
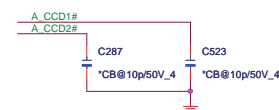
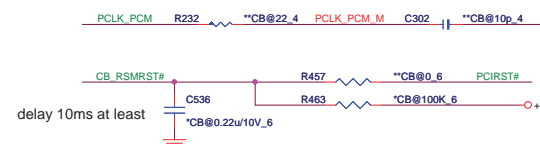
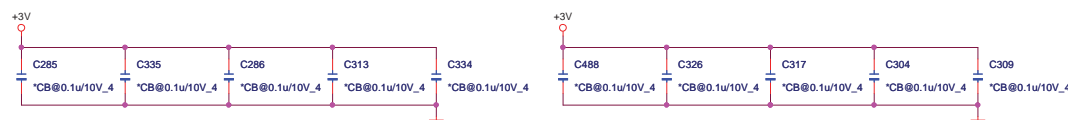
Rev:3A 01/29 Delete R133 For ESD Solution.



Rev:3A 03/03 Stuff the D4/D5/D32/D34/35 Varistor For ESD Solution.

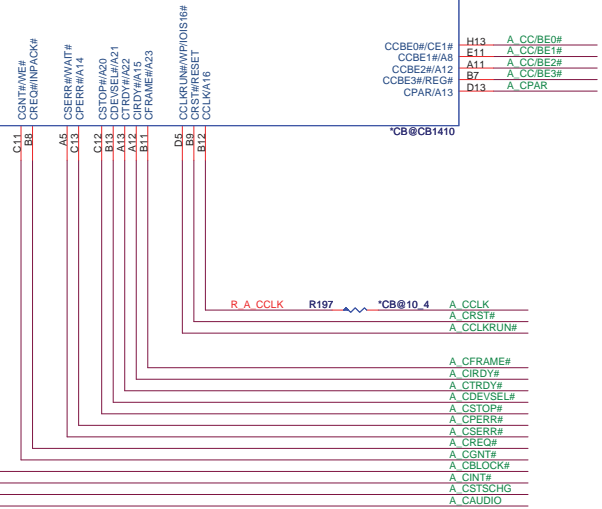
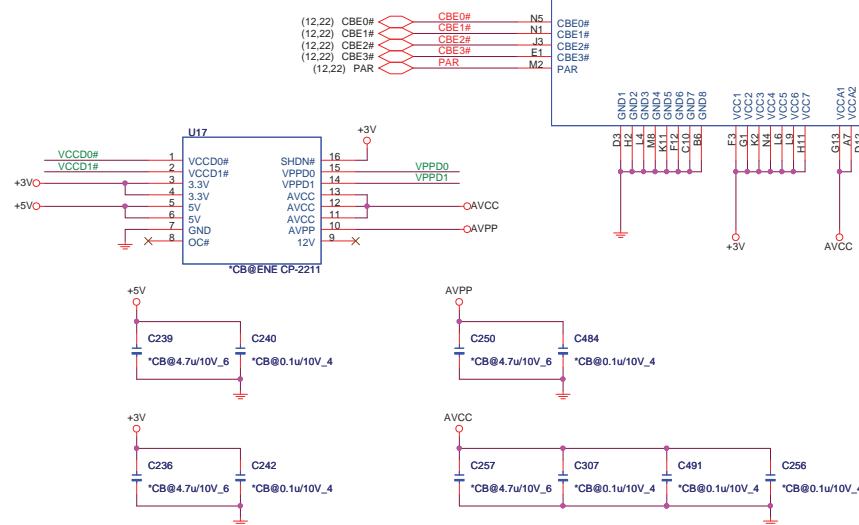
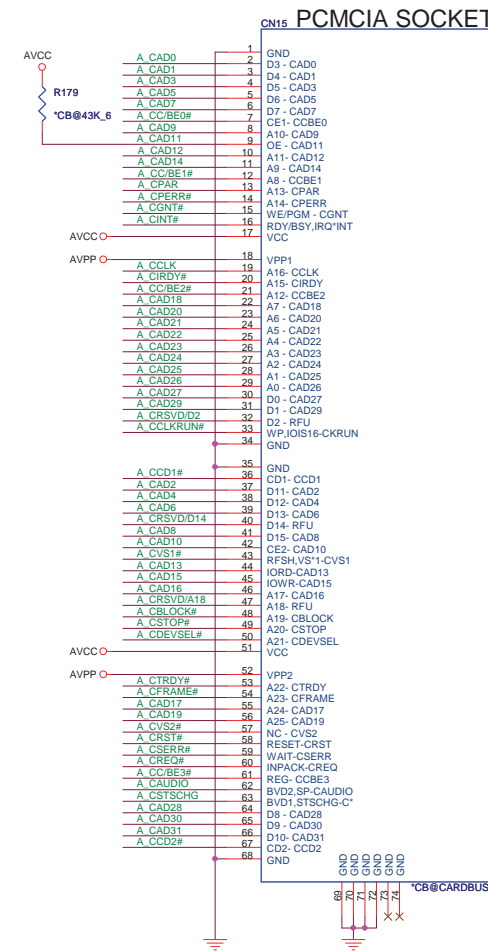






ENE1410	AJ014100T41
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ID Select	: AD18
Interrupt Pin	: INTF#
Request Indicate	: REQ1#
Grant Indicate	: GNT1#



**CARDBUS**

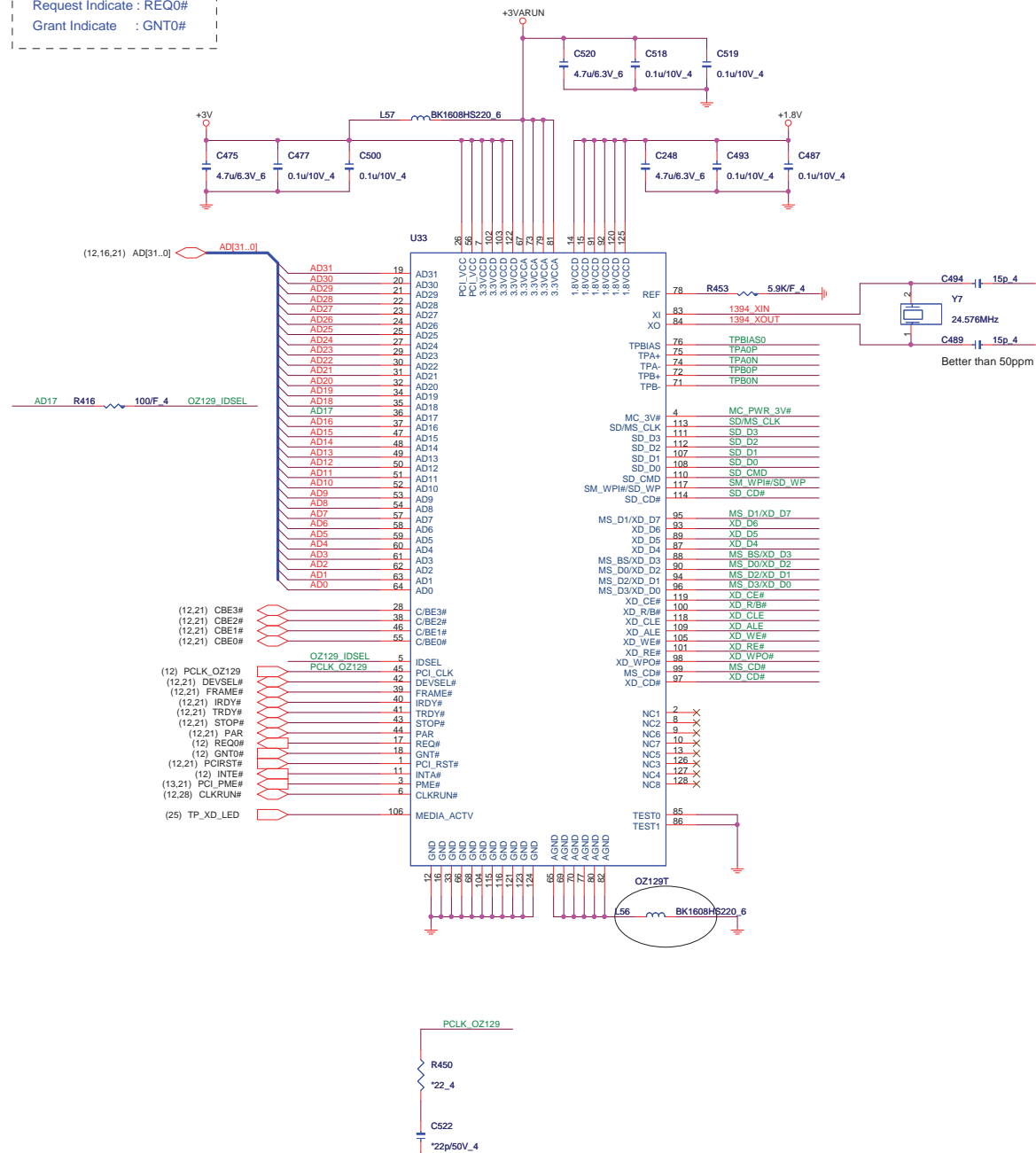


**PROJECT : BU2**  
Quanta Computer Inc.

Size Custom	Document Number <b>PCMCIA(CB1410) -OPTION</b>		
Date: Thursday, July 24, 2008	Sheet	21	of 35

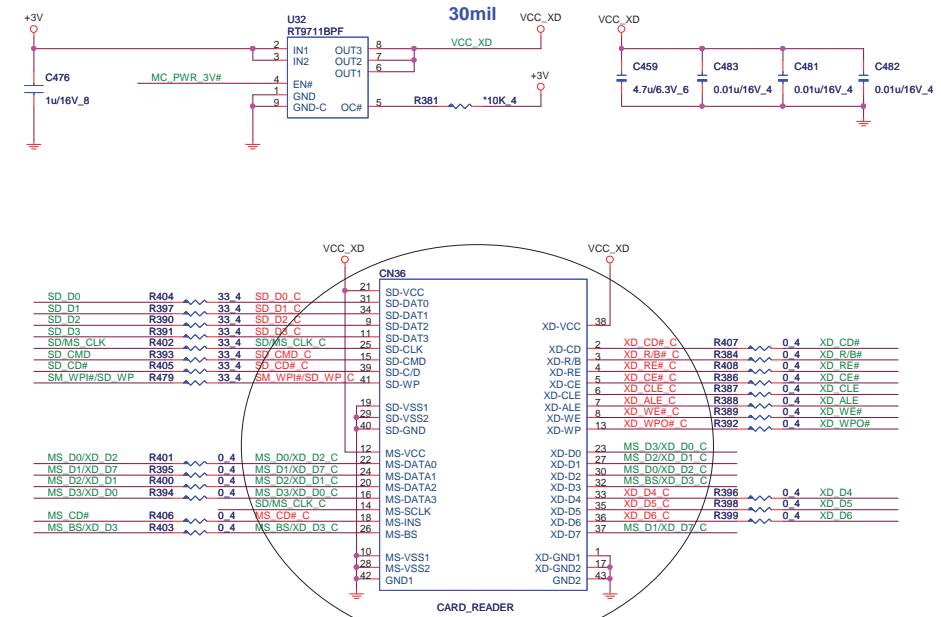
*OZ129 CardReader/1394*

ID Select : AD17  
Interrupt Pin : INTE#  
Request Indicate : REQ0#  
Grant Indicate : GNT0#



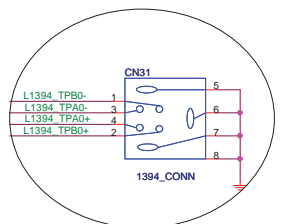
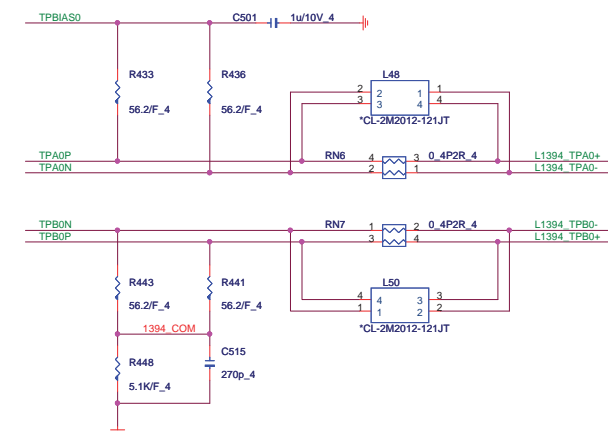
## 5 IN 1 Card Reader

22



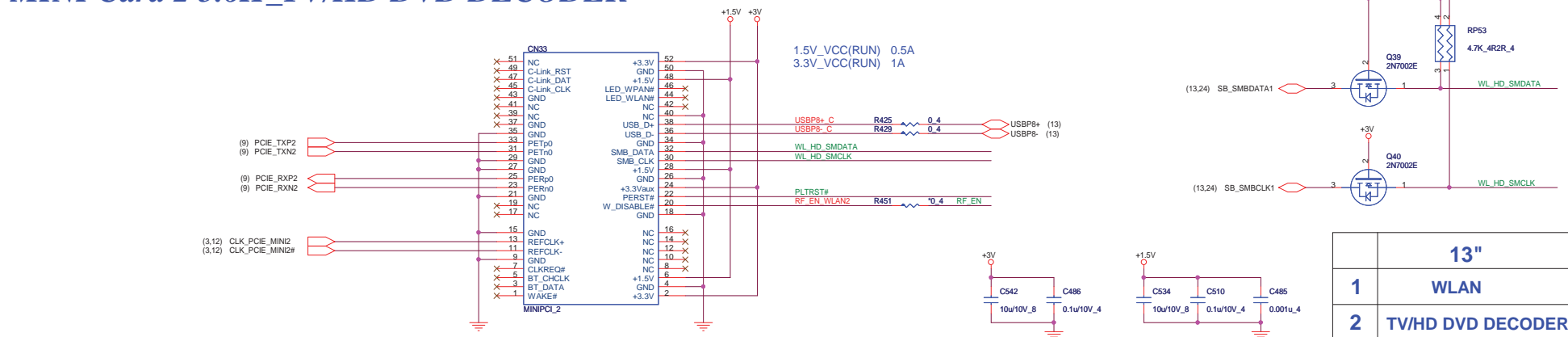
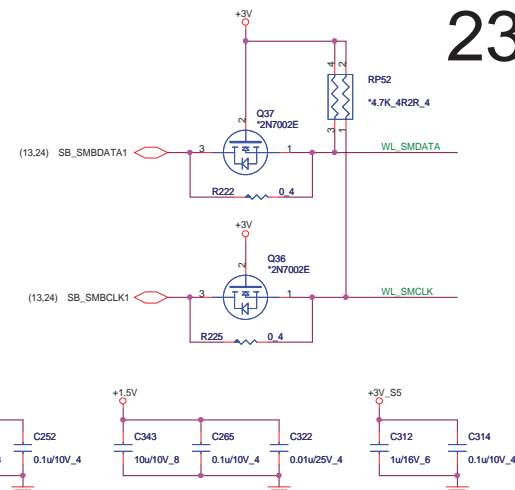
Rev:2A 12/07 Modified the CN36 Footprint For Open Issue.

## 1394

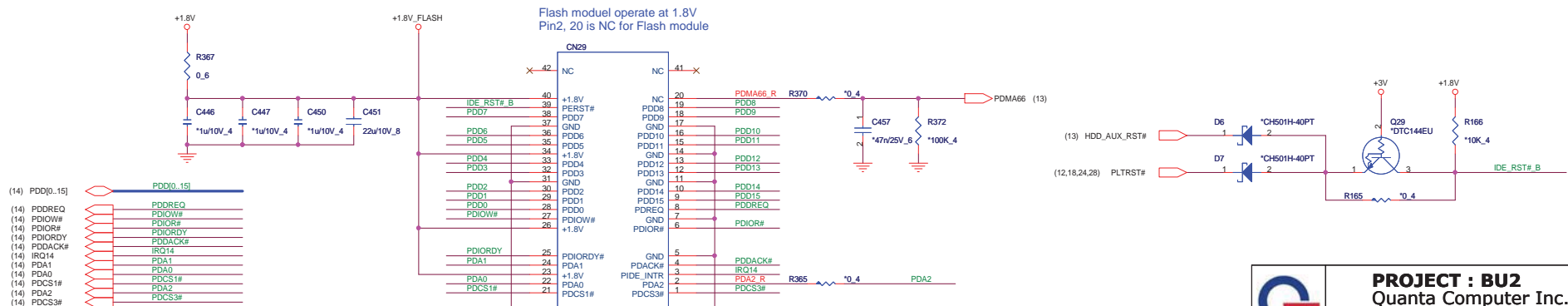


Rev:2A 12/07 Change New Part Number.

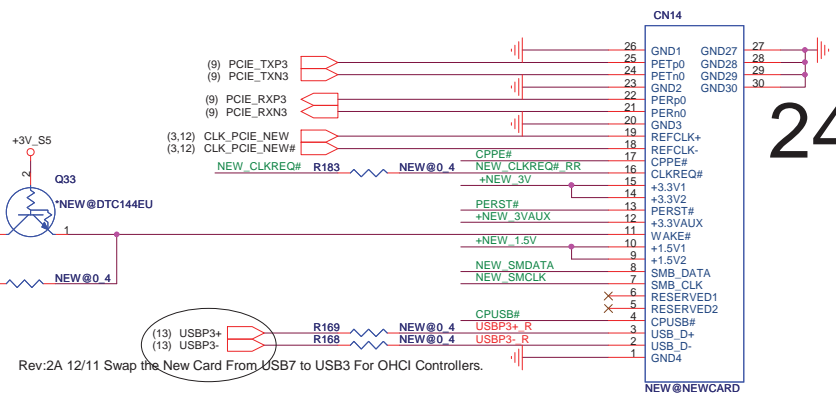
## 23



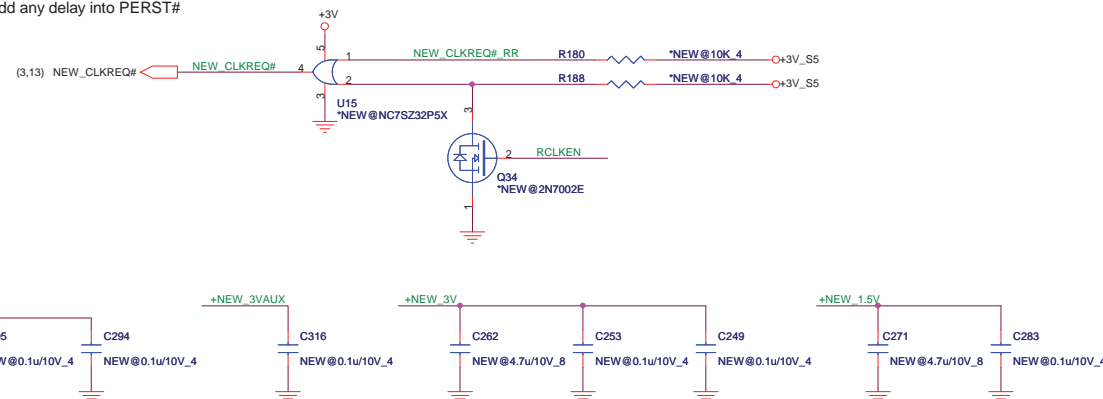
## DECODER



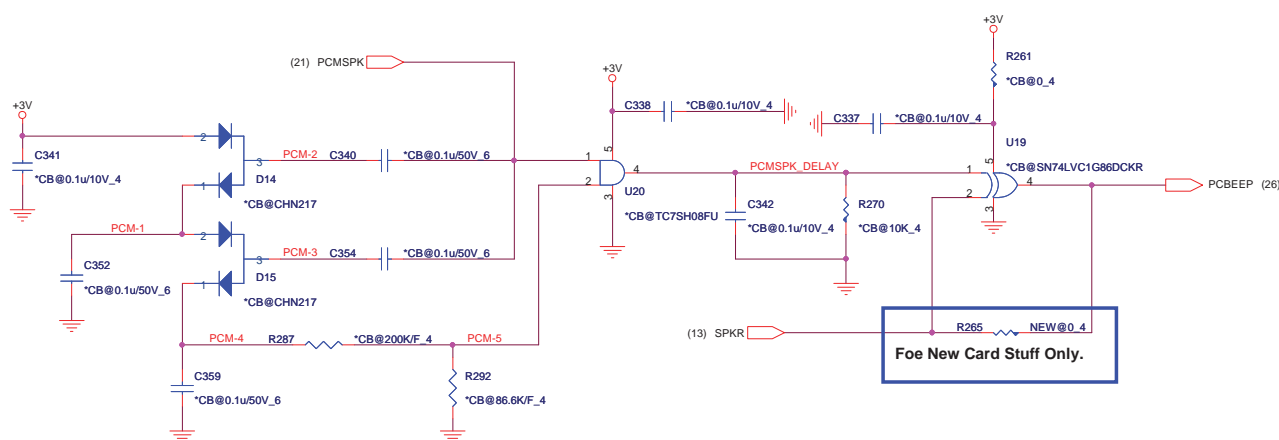
24



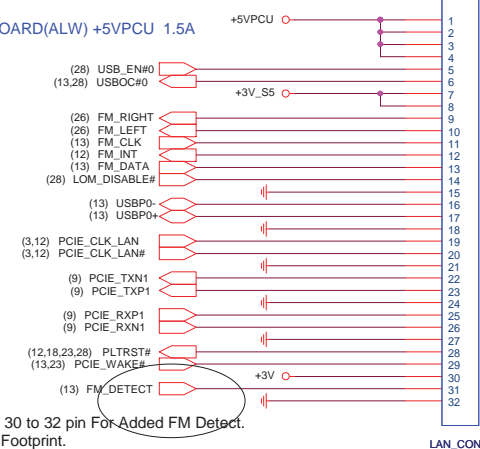
Rev:2A 12/11 Swap the New Card From USB7 to USB3 For OHCI Controllers



## RJ45/USB BOARD

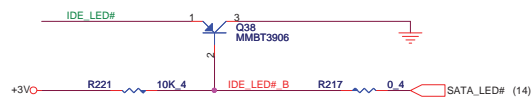
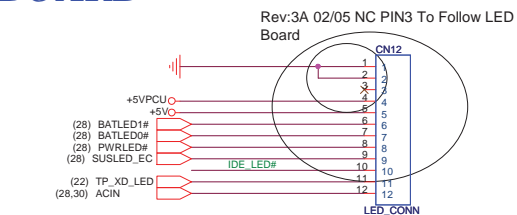


USB &amp; LAN BOARD(ALW) +5VPCU 1.5A

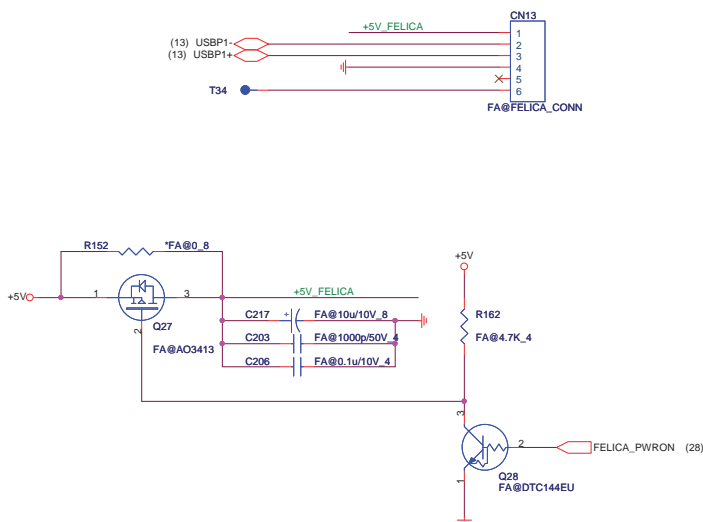


Rev:2A 12/07 Change Connector From 30 to 32 pin For Added FM Detect.  
Rev:3A 02/05 Change Connector PCB Footprint.

## LED BOARD

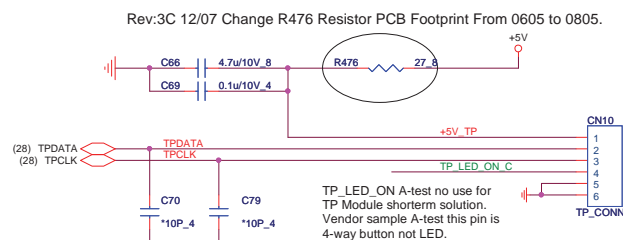


## Felica

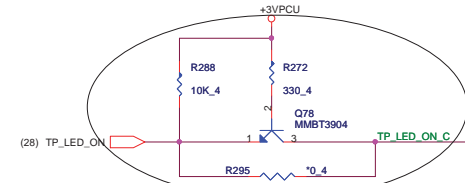


## TP BOARD

25

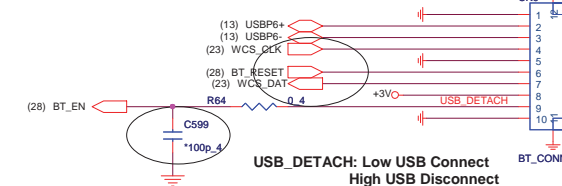


Rev:2A 12/07 Apply isolate TP\_LED\_ON From EC to Mainstream TP



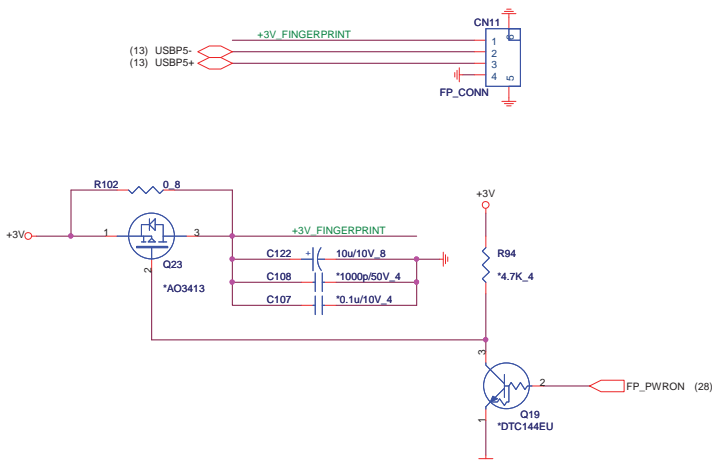
## Bluetooth Module

Rev:3D 07/23 Remove R59 and Added control BT Reset by EC GPIO77



Rev:3A 03/03 Reserve C599 Capacitors to Bluetooth Enable For EMI..

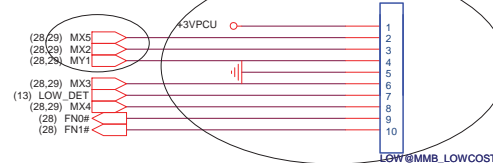
## FINGER-PRINT



## MMB

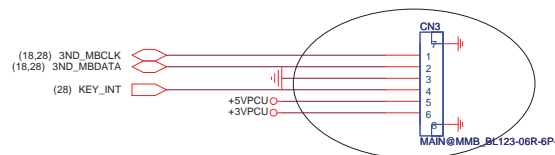
Rev:2A 12/07 Change Low cost pin1 From MX1 to MX5

Low cost

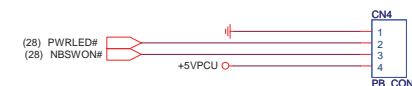


Rev:2A 12/07 Change CONN Footprint.

Main stream



## POWER BOARD

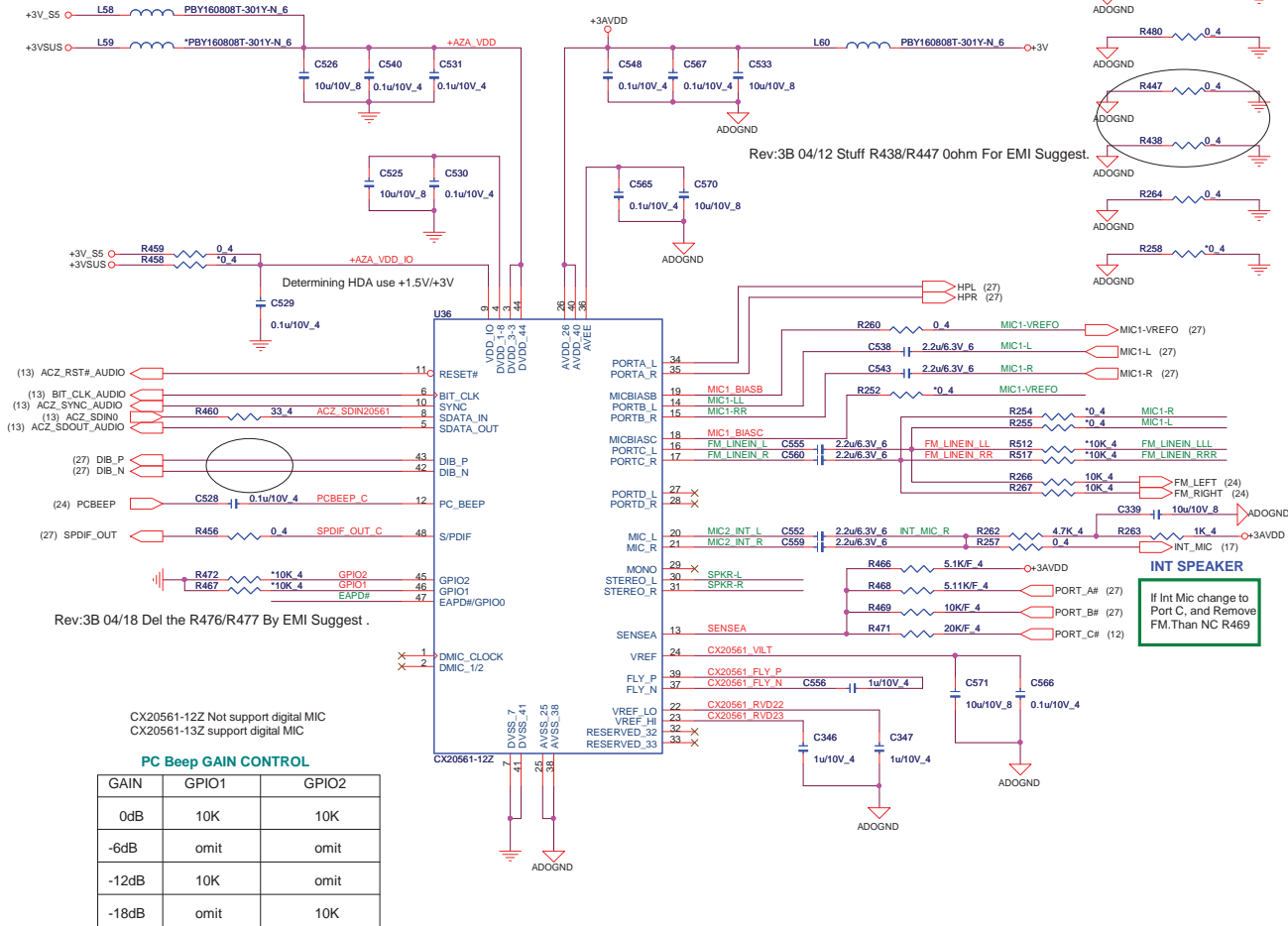


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Quanta Computer Inc.

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Custom	TP/FP/BT/PB/FELICA/MMB CONN	1A
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# CODEC(CX20561)

Rev:3A 02/05 Added the EMI Solution.



Rev:3B 04/12 Stuff R438/R447 0ohm For EMI Suggest.

Rev:3B 04/18 Del the R476/R477 By EMI Suggest.

CX20561-12Z Not support digital MIC  
CX20561-13Z support digital MIC

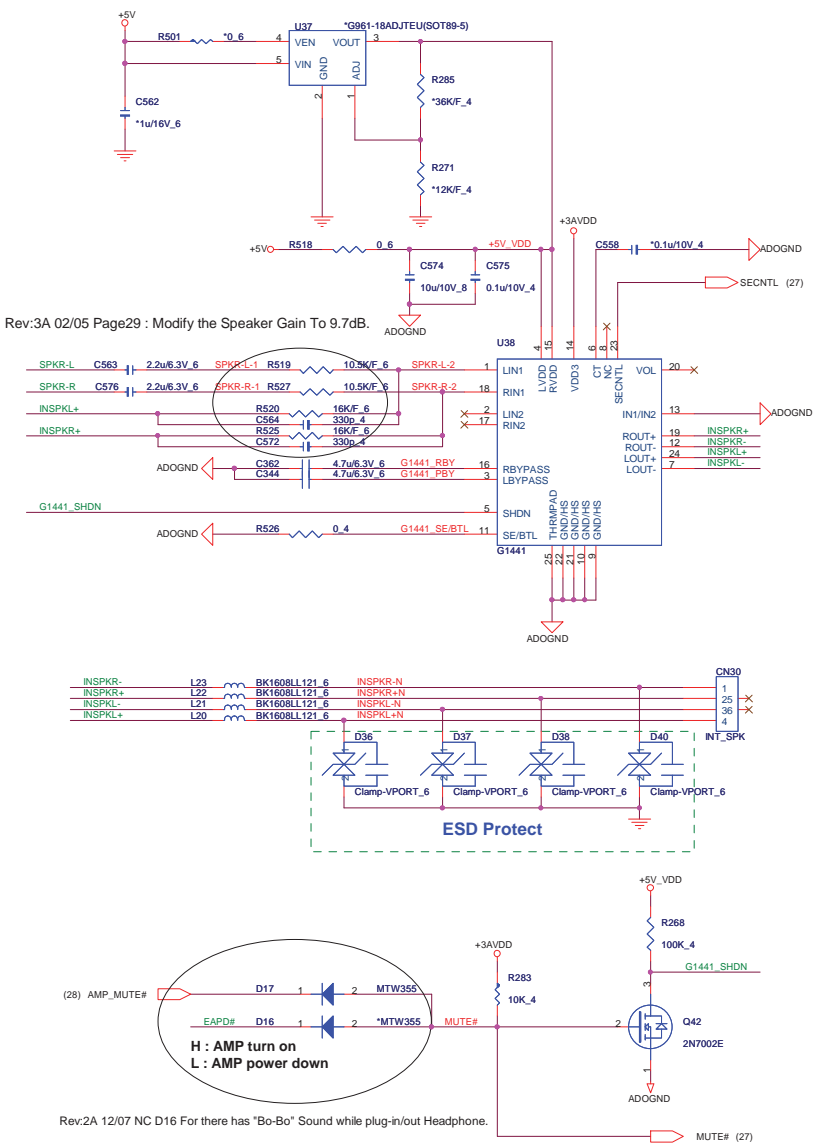
Rev:3A 02/05 Stuff C539/C544 For INT MIC Recording Noise.

INT SPEAKER

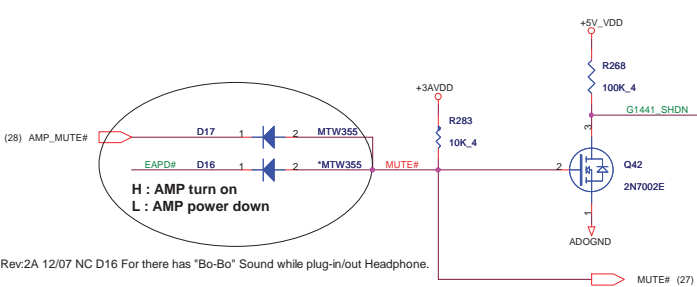
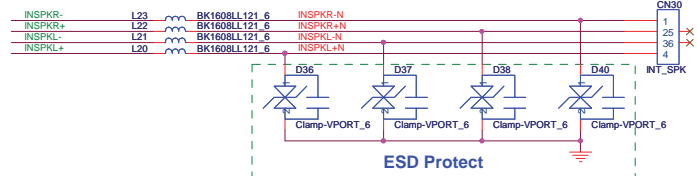
If Int Mic change to Port C, and Remove FM. Than NC R469

# INT SPK AMP

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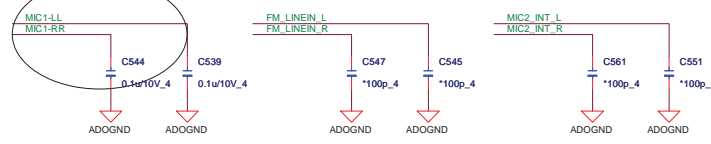
Rev:3A 02/05 Page29 : Modify the Speaker Gain To 9.7dB.



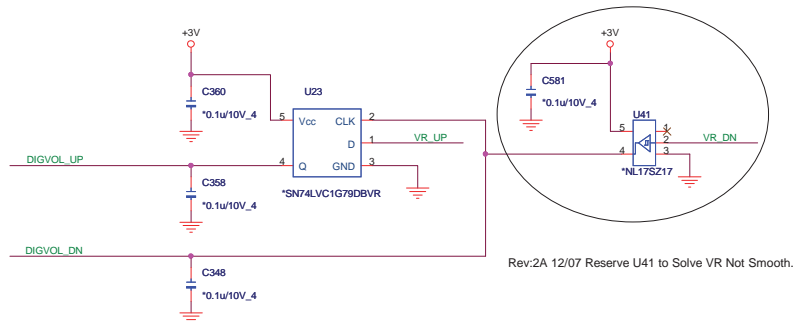
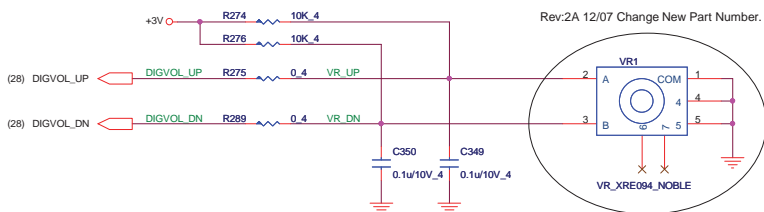
Rev:2A 12/07 NC D16 For there has "Bo-Bo" Sound while plug-in/out Headphone.

## Reserve INTMIC

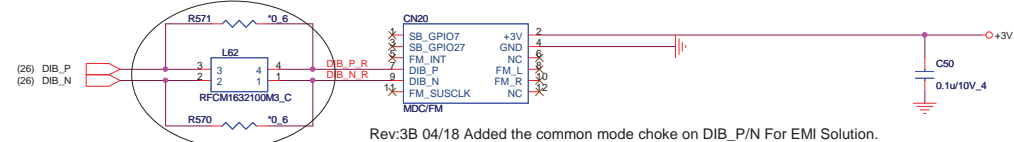
## Reserve FM



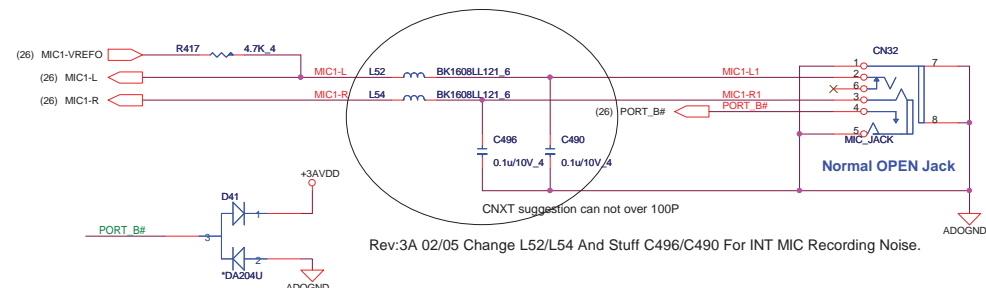




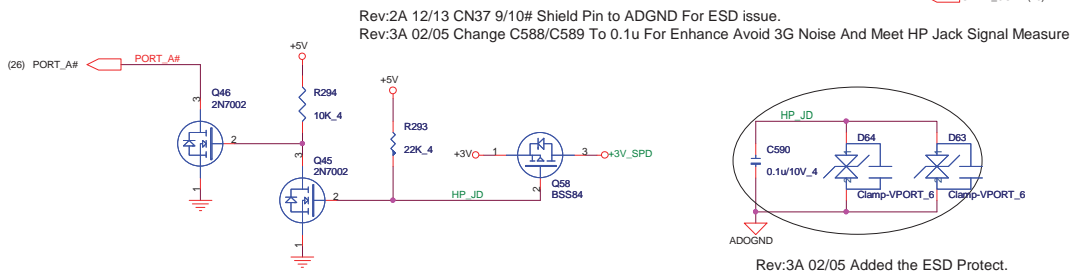
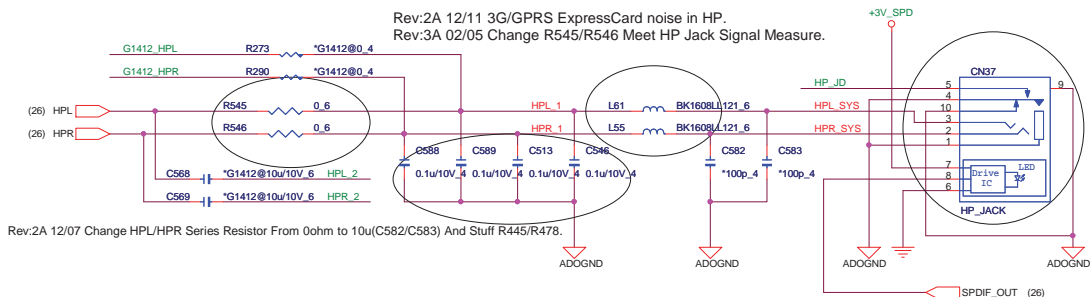
## FM TUNER &amp; MDC



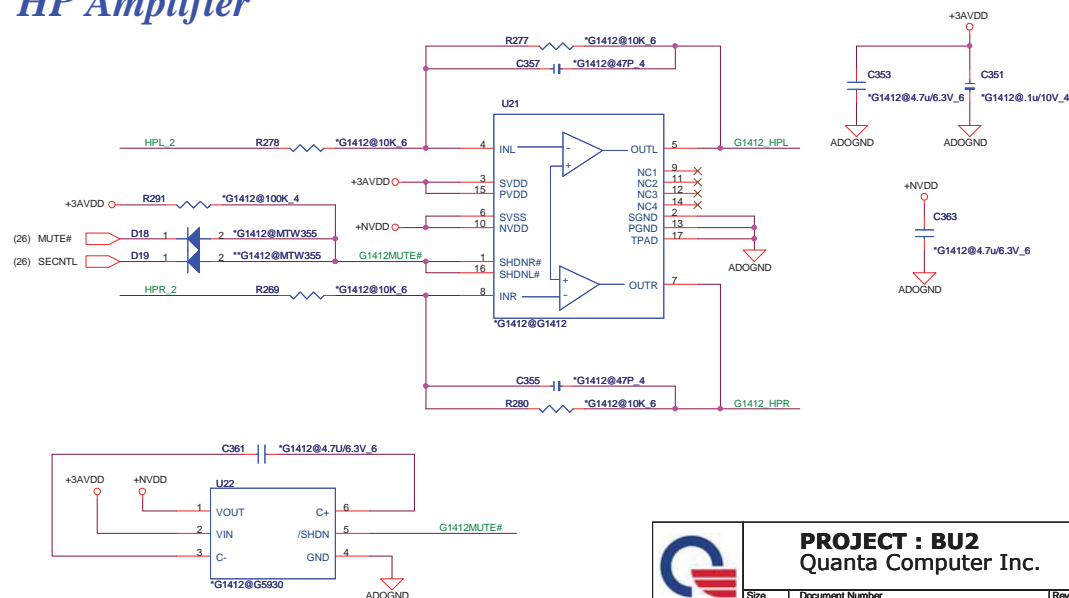
## SYSTEM MIC



## HP JACK



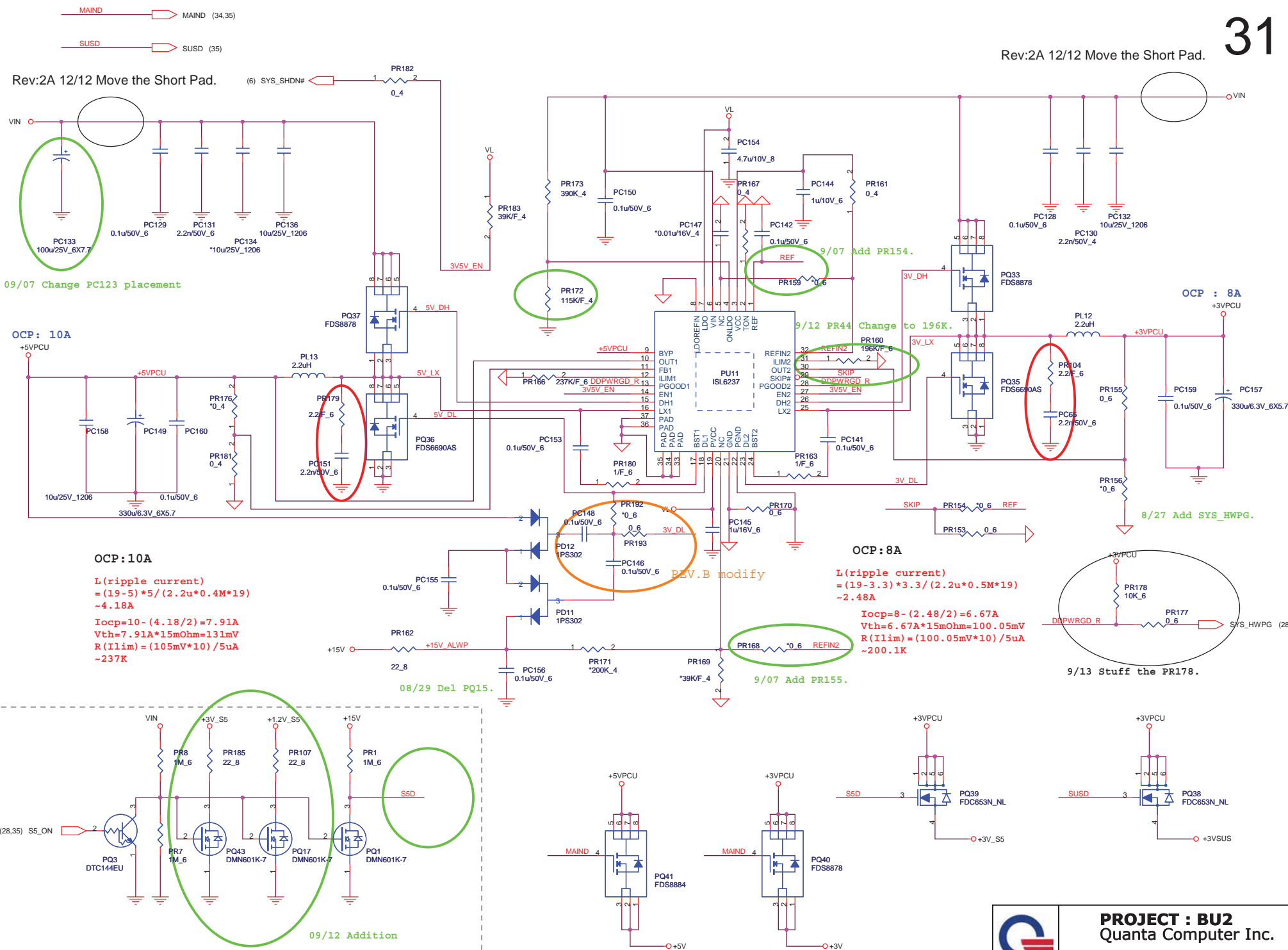
## HP Amplifier











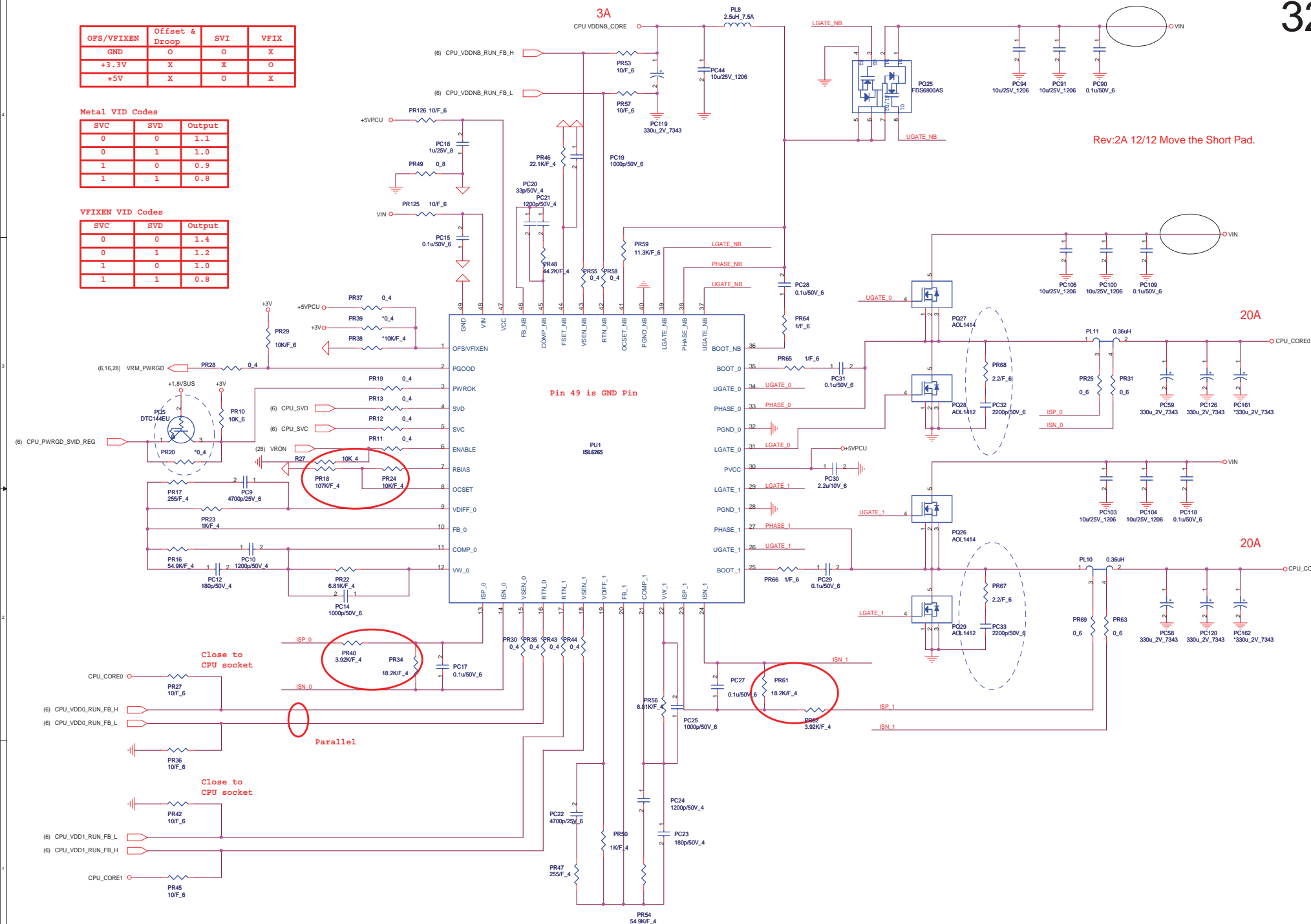
OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

### Metal VID Codes

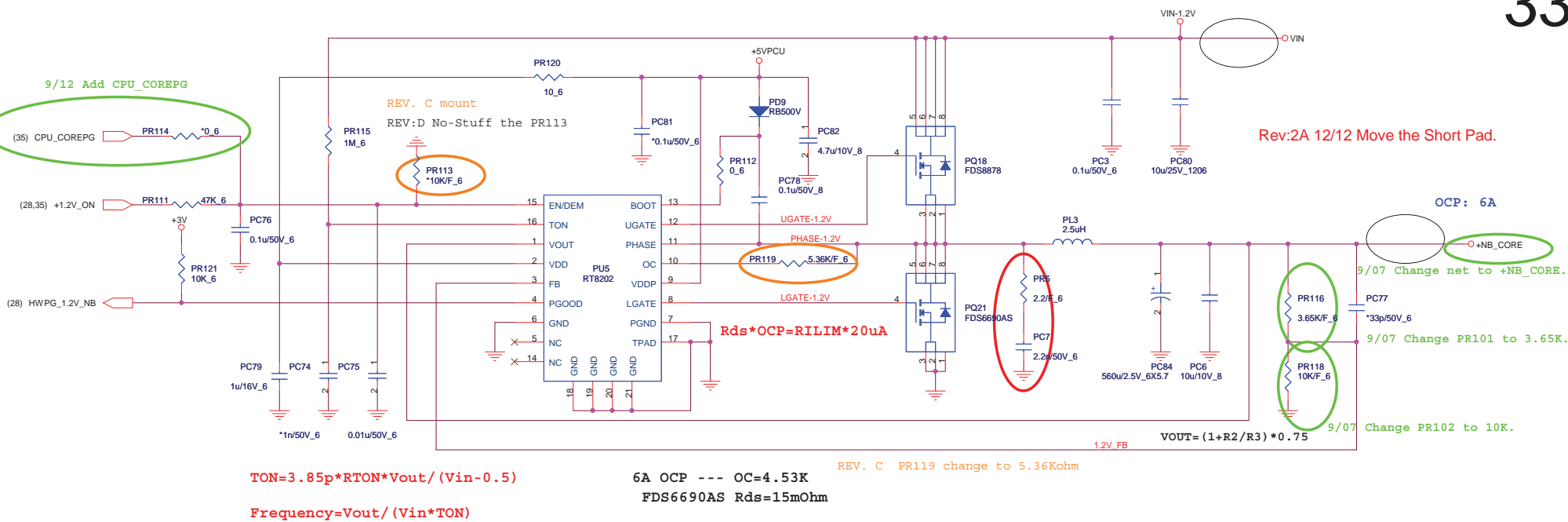
SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

### VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8







1/30 modify

