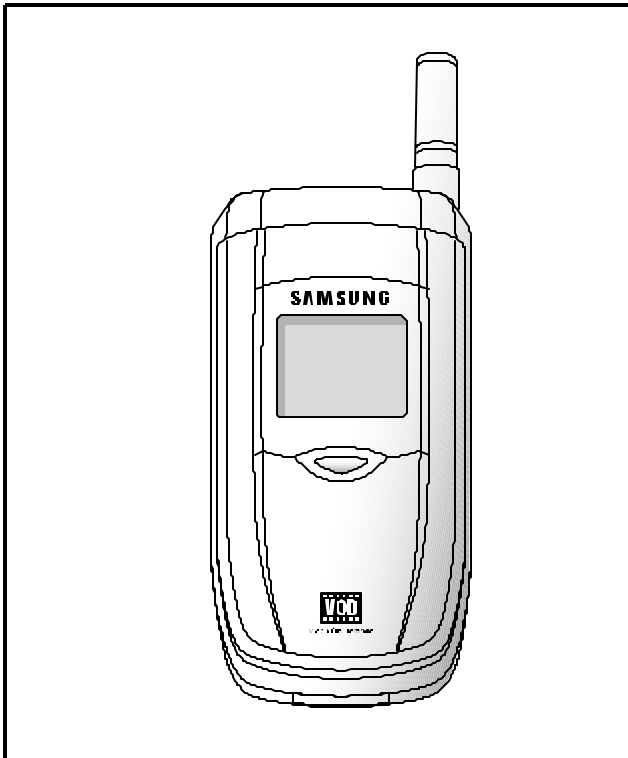


SAMSUNG

GSM TELEPHONE
SGH-V100

SERVICE *Manual*

GSM TELEPHONE



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1. SGH-V100 Specification

1. GSM General Specification

	GSM900 Phase 1	EGSM 900 Phase 2	DCS1800 Phase 1	PCS1900
Freq. Band[MHz] Uplink/Downlink	890~915 935~960	880~915 925~960	1710~1785 1805~1880	1850~1910 1930~1990
ARFCN range	1~124	0~124 & 975~1023	512~885	512~810
Tx/Rx spacing	45MHz	45MHz	95MHz	80MHz
Mod. Bit rate/ Bit Period	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us
Time Slot Period/Frame Period	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms
Modulation	0.3GMSK	0.3GMSK	0.3GMSK	0.3GMSK
MS Power	33dBm~13dBm	33dBm~5dBm	30dBm~0dBm	30dBm~0dBm
Power Class	5pcl ~ 15pcl	5pcl ~ 19pcl	0pcl ~ 15pcl	0pcl ~ 15pcl
Sensitivity	-102dBm	-102dBm	-100dBm	-100dBm
TDMA Mux	8	8	8	8
Cell Radius	35Km	35Km	2Km	-

2. GSM TX power class

TX Power control level	GSM900	TX Power control level	DCS1800	TX Power control level	PCS1900
5	33 ±2 dBm	0	30 ±3 dBm	0	30 ±3 dBm
6	31 ±2 dBm	1	28 ±3 dBm	1	28 ±3 dBm
7	29 ±2 dBm	2	26 ±3 dBm	2	26 ±3 dBm
8	27 ±2 dBm	3	24 ±3 dBm	3	24 ±3 dBm
9	25 ±2 dBm	4	22 ±3 dBm	4	22 ±3 dBm
10	23 ±2 dBm	5	20 ±3 dBm	5	20 ±3 dBm
11	21 ±2 dBm	6	18 ±3 dBm	6	18 ±3 dBm
12	19 ±2 dBm	7	16 ±3 dBm	7	16 ±3 dBm
13	17 ±2 dBm	8	14 ±3 dBm	8	14 ±3 dBm
14	15 ±2 dBm	9	12 ±4 dBm	9	12 ±4 dBm
15	13 ±2 dBm	10	10 ±4 dBm	10	10 ±4 dBm
16	11 ±3 dBm	11	8 ±4dBm	11	8 ±4dBm
17	9 ±3dBm	12	6 ±4 dBm	12	6 ±4 dBm
18	7 ±3 dBm	13	4 ±4 dBm	13	4 ±4 dBm
19	5 ±3 dBm	14	2 ±5 dBm	14	2 ±5 dBm
		15	0 ±5 dBm	15	0 ±5 dBm

2. SGH-V100 Circuit Description

1. SGH-V100 RF Circuit Description

1) RX PART

1. ASM(F950) Switching Tx, Rx path for GSM900, DCS1800 and PCS1900 by logic controlling.

2. ASM Control Logic (U701, U702, U703) Truth Table

	VC1	VC2	VC3
GSM Tx Mode	H	L	L
DCS / PCS Tx Mode	L	H	L
PCS Rx Mode	L	L	H
GSM / DCS Rx Mode	L	L	L

3. SAW FILTER

To convert Electro magnetic Field Wave to Acoustic Wave and then pass the specific frequency band.

- PCS SAW FILTER(F951)

==> For filtering the frequency band between 1930 and 1990MHz

4. TC-VCXO (U703)

To generate the 13MHz reference clock to drive the logic and RF.

After additional process, the reference clock applies to the U900 Rx IQ demodulator and Tx IQ modulator.

The oscillator for RX IQ demodulator and Tx modulator are controlled by serial data to select channel and use fast lock mode for GPRS high class operation.

5. Si 4200 (U901)

This chip integrates three differential-input LNAs.

The GSM input supports the E-GSM, DCS input supports the DCS1800, PCS input supports the PCS1900. The LNA inputs are matched to the 200 ohm differential output SAW filters through eternal LC matching network.

Image-reject mixer downconverts the RF signal to a 100 KHz intermediate frequency(IF) with the RFLO from SI4133T frequency synthesizer. The RFLO frequency is between 1737.8 ~ 1989.9 MHz.

The Mixer output is amplified with an analog programmable gain amplifier(PGA), which is controlled by AGAIN.

The quadrature IF signal is digitized with high resolution A/D converts (ADC).

6. Si 4201 (U900)

The SI4201 down-converts the ADC output to baseband with a digital 100 KHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interface signals.

After channel selection, the digital output is scaled with a digital PGA, which is controlled with the DGAIN. DACs drive a differential analog signal onto the RXIP, RXIN, RXQP, RXQN pins to interface to standard analog-input baseband IC.

2) TX PART

Baseband IQ signal fed into offset PLL, this function is included inside of U902 chip.

SI4200 chip generates modulator signal which power level is about 1.5dBm and fed into Power Amplifier(U951).

The PA output power and power ramping are well controlled by Auto

Power Control circuit. We use offset PLL below

Modulation Spectrum	200kHz offset 30 kHz bandwidth	GSM	-35dBc
		DCS	-35dBc
		PCS	-35dBc
	400kHz offset 30 kHz bandwidth	GSM	-66dBc
		DCS	-65dBc
		PCS	-66dBc
	600kHz ~ 1.8MHz offset 30 kHz bandwidth	GSM	-75dBc
		DCS	-68dBc
		PCS	-75dBc

2. Baseband Circuit description of SGH-V100

1. PSC2006

1.1. Power Management

Seven low-dropout regulators designed specifically for GSM applications power the terminal and help ensure optimal system performance and long battery life. A programmable boost converter provides support for 1.8V, 3.0V, and 5.0V SIMs, while a self-resetting, electronically fused switch supplies power to external accessories. Ancillary support functions, such as an LED driver and two call-alert drivers, aid in reducing both board area and system complexity.

A three-wire serial interface unit(SIU) provides access to control and configuration registers. This interface gives a microprocessor full control of the PSC2006 and enables system designers to maximize both standby and talk times.

Supervisory functions, including a reset generator, an input voltage monitor, and a thermal monitor, support reliable system design. These functions work together to ensure proper system behavior during start-up or in the event of a fault condition(low microprocessor voltage, insufficient battery energy, or excessive die temperature).

1.2. Battery Charge Management

A battery charge management block provides fast, efficient charging of a single-cell Li-ion battery. Used in conjunction with a current-limited voltage source and an external PMOS pass transistor, this block safely conditions near-dead cells and provides the option of having fast-charge and top-off controlled internally or by the system's microprocessor.

1.3. Backlight LED Driver

The backlight LED driver is a low-side, programmable current source designed to control the brightness of the keyboard and LCD illumination. The driver is enabled by EN_LED, and its current setting is determined by LED[0:2]. Provided EN_LED is ' 1 ', the driver can be programmed to sink from 12.5mA to 100mA in 12.5mA steps. LED_DRV is capable of sinking 100mA at a worst-case maximum output voltage of 0.6V. For efficient use, the LEDs is connected between the battery and the LED_DRV output.

1.4. Vibrator Motor Driver

The vibrator motor driver is a low-side, programmable voltage source designed to drive a small dc motor that silently alerts the user of an incoming call. The driver is enabled by EN_VIB, and its voltage setting is determined by VIB[0:2]. Provided EN_VIB is a logic 1, the driver can be programmed to maintain a motor voltage of 1.1V to 2.5V in 20mV steps and while sinking up to 100mA. For efficient use, the vibrator motor should be connected between the main battery and the VIB_DRV output.

2. Connector

2-1. LCD Connector

LCD is consisted of main LCD(color 65K STN LCD) and small LCD(4-gray LCD). Chip select signals of EMI part in the trident, CLCD_EN_FO and GLCD_EN_FO, can enable Each LCD. LED_EN_FO signal enables white LED of main LCD and EL_EN_FO signal enables EL of small LCD. These two signals are from IO part of the DSP in the trident. RST signal from 2006 initiates the initial process of the LCD.

16-bit data lines(D(0)_FO~D(15)_FO) transfers data and commands to LCD through emi_filter. Data and commands use A(2)_FO signal. If this signal is high, Inputs to LCD are commands. If it is low, Inputs to LCD are data. The signal which informs the input or output state to LCD, is required. But this system is not necessary this signal. So CP_WEN_FO signal is used to write data or commands to LCD. Power signals for LCD are V_bat and V_ccd. SPK1P and SPK1N from CSP1093 are used for audio speaker. And VIB_EN_FO from enables the motor.

2-2. JTAG Connector

Trident has two JTAG ports which are for ARM core and DSP core(DSP16000). So this system has two port connector for these ports. Pins ' initials for ARM core are ' CP_ ' and pins ' initials for DSP core are ' DSP_ '. CP_TDI and DSP_TDI signal are used for input of data. CP_TDO and DSP_TDO signals are used for the output of the data. CP_TCK and DSP_TCK signals are used for clock because JTAG communication is a synchronous. CP_TMS and DSP_TMS signals are test mode signals. The difference between these is the RESET_INT signal which is for ARM core RESET.

2-3. IRDA

This system uses IRDA module, HSDL_3201, HP ' s. This has signals, IRDA_EN(enable signal), IRDA_RX(input data) and IRDA_TX(output data). These signals are connected to PPI of trident. It uses two power signals. V_ccd is used for circuit and V_bat is used for LED.

2-4. Keypad connector

This is consisted of key interface pins among PPI in the trident, KEY_ROW[0~4] and KEY_COL[0~4]. These signals compose the matrix. Result of matrix informs the key status to key interface in the trident. Some pins are connected to varistor for ESD protection. And power on/off key is seperated from the matrix. So power on/off signal is connected with PSC2006 to enable PSC2006. SVC_GREEN, SVC_RED and SVC_BLUE are from OCTL of CSP1093. These signals decide the color of LED, service indicator. Eighteen key LED use the V_bat supply voltage. These are connected to BACKLIGHT signal in the PSC2006. This signal enables LEDs with current control. FLIP_SNS informs the status of folder (open or closed) to the trident. This uses the hall effect IC, A3210ELH. A magnet under main LCD enables A3210ELH which is on the key FPCB.

3. IF connector

It is 18-pin connector, and uses 18-pin at present. They are designed to use SDS, DEBUG, DLC-DETECT, JIG_ON, VEXT, VTEST, VF, CF, VBAT and GND. They connected to power supply IC, microprocessor and signal processor IC.

4. Audio

AOUTAP from CSP1093 is connected to the main speaker. AOUTAN is connected to the speaker via audio-amp. AOUTBN and AOUTBP are connected to the ear-mic speaker via ear-jack. MICIN and MICOUT are connected to the main MIC. And AUXIN and AUXOUT are connected to the Ear-mic.

YMU762MA3 is a LSI for portable telephone that is capable of playing high quality music by utilizing FM synthesizer and ADPCM decoder that are included in this device.

As a synthesis, YMU762MA3 is equipped 16 voices with different tones. Since the device is capable of simultaneously generating up to synchronous with the play of the FM synthesizer, various sampled voices can be used as sound effects. Since the play data of YMU762MA3 are interpreted at anytime through FIFO, the length of the data (playing period) is not limited, so the device can flexibly support application such as incoming call melody music distribution service. The hardware sequencer built in this device allows playing of the complex music without giving excessive load to the CPU of the portable telephones. Moreover, the registers of the FM synthesizer can be operated directly for real time sound generation, allowing, for example, utilization of various sound effects when using the game software installed in the portable telephone.

YMU759 includes a speaker amplifier with high ripple removal rate whose maximum output is 550mW (SPVDD=3.6V). The device is also equipped with conventional function including a vibrator and a circuit for controlling LEDs synchronous with music.

For the headphone, it is provided with a stereophonic output terminal.

For the purpose of enabling YMU762MA3 to demonstrate its full capabilities, Yamaha purpose to use "SMAF: Synthetic music Mobile Application Format" as a data distribution format that is compatible with multimedia. Since the SMAF takes a structure that sets importance on the synchronization between sound and images, various contents can be written into it including incoming call melody with words that can be used for training karaoke, and commercial channel that combines texts, images and sounds, and others. The hardware sequencer of YMU762MA3 directly interprets and plays blocks relevant to synthesis (playing music and reproducing ADPCM with FM synthesizer) that are included in data distributed in SMAF.

5. Memory

This system uses Intel's memory, 28F6408W30BH70. It is consisted of 64M bits flash memory and 8M bits SRAM. It has 16 bit data line, D[0~15] which is connected to trident, LCD or CSP1093. It has 22 bit address lines, A[1~22]. They are connected too. CP_CSROMEN and CO_CSROM2EN signals, chip select signals in the trident enable two memories. They use 3 volt supply voltage, V_{ccd} and 1.8 volt supply voltage, V_{cc_1.8a} in the PSC2006. During writing process, CP_WEN is low and it enables writing process to flash memory and SRAM. During reading process, CP_OEN is low and it output information which is located at the address from the trident in the flash memory or SRAM to data lines. Each chip select signals in the trident select memory among 2 flash memory and 2 SRAM. Reading or writing procedure is processed after CP_WEN or CP_OEN is enabled. Memories use FLASH_RESET, which is buffered signal of RESET from PSC2006, for ESD protection. A[0] signal enables lower byte of SRAM and UPPER_BYTE signal enables higher byte of SRAM.

6. Trident

Trident is consisted of ARM core and DSP core. It has 20K*16bits RAM 144K*16bits ROM in the DSP. It has 4K*32bits ROM and 2K*32bits RAM in the ARM core. DSP is consisted of timer, one bit input/output unit(BIO), JTAG, EMI and HDS(Hardware Development System). ARM core is consisted of EMI, PIC(Programmable Interrupt Controller), reset/power/clock unit, DMA controller, TIC(Test Interface Controller), peripheral bridge, PPI, SSI(Synchronous Serial Interface), ACC(Asynchronous communications controllers), timer, ADC, RTC(Real-Time Clock) and keyboard interface. DSP_AB[0~8], address lines of DSP core and DSP_DB[0~15], data lines of DSP core are connected to CSP1093. A[0~20], address lines of ARM core and D[0~15], data lines of ARM core are connected to memory, LCD and YMU759. ICP(Interprocessor Communication Port) controls the communication between ARM core and DSP core. CSROMEN, CSRAMEN and CS1N to CS4N in the ARM core are connected to each memory. WEN and OEN control the process of memory. External IRQ(Interrupt ReQuest) signals from each units, such as, YMU, Ear-jack, Ear-mic and CSP1093, need the compatible process.

Some PPI pins has many special functions. CP_KB[0~9] receive the status from key FPCB and are used for the communicatios using IRDA(IRDA_RX/TX/EN) and data link cable(DEBUG_DTR/RTS/TXD/RXD/CTS/DSR). And UP_CS/SCLK/SDI, control signals for PSC2006 are outputted through PPI pins. It has signal port for charging(CHG_DET, CHG_STAT0), SIM_RESET and FLIP_SNS with which we knows open.closed status of folder. It has JTAG control pins(TDI/TDO/TCK) for ARM core and DSP core. It recieves 13MHz clock in CKI pin from external TCXO and receives 32.768KHz clock from X1RTC. ADC(Analog to Digital Convector) part receives the status of temperature, battery type and battery voltage. And control signals(DSP_INT, DSP_IO and DSP_RWN) for DSP core are used. It enables main LCD and small LCD with DSP IP pins.

7. CSP1093

CSP1093 integrates the timing and control functions for GSM 2+ mobile application with the ADC and DAC functions. The CSP1093 interfaces to the trident, via a 16-bit parallel interface. It serves as the interface that connects a DSP to the RF circuitry in a GSM 2+ mobile telephone. DSP can load 148 bits of burst data into CSP1093 's internal register, and program CSP1093 's event timing and control register with the exact time to send the burst. When the timing portion of the event timing and control register matches the internal quarter-bit counter and internal frame counter, the 148 bits in the internal register are GMSK modulated according to GSM 2+ standards. The resulting phase information is translated into I and Q differential output voltages that can be connected directly to an RF modulator at the TXOP and TXON pins. The DSP is notified when the transmission is completed. For receiving baseband data, a DSP can program CSP1093 's event timing and control register with the exact time to start receiving I and Q samples through TXIP and TXIN pins. When that time is reached, the control portion of the event timing and control register will start the baseband receive section converting I and Q sample pairs. The samples are stored in a double-buffered register until the register contains 32 sample pairs. CSP1093 then notifies the DSP which has ample time to read the information out before the next 32 sample pairs are stored. The voice band ADC converter issues an interrupt to the DSP whenever it finishes converting a 16-bit PCM word. The DSP then reads the new input sample and simultaneously loads the voice band output DAC converter with a new PCM output word. The voice band output can be connected directly to a speaker via AOUTAN and AOUTAP pins and be connected to a Ear-mic speaker via AOUTBN and AOUTBP pins.

8. X-TAL(13MHz)

This system uses the 13MHz TCXO, TCO-9141B, Toyocom. AFC control signal form CSP1093 controls frequency from 13MHz x-tal. It generates the clock frequency. This clock is inverted through NOT gate, TC7S04FU and is connected to CSP1093. 13MHz clock for YMU759 uses a not-inverted clock. Clock for RF parts uses same type.

3. Video On demand description of SGH-V100

1) ECD(A3)

ECD(A3) is an application and multi-media processor targeted for the mobile market. This includes cell phone, PDAs and accessories. The chips can serve mobile applications regardless of the cellular technology itself. It is a full duplex A/V codec assembled with a large variety of application. Application is like this. Streaming is video and audio. Capturing is video and digital still. Playing is audio, video and still picture. The chip supports the following standard and recommendations. It is MPEG-4, H.263, MP3, G.7231, GSM-AMR and ACC, WMF RTFD 1.0, 3GPP Packet-Switched Streaming Service(26.234) Release 4.

The solution is based on the ARM platform as a high-performance, fully programmable core processor, with the addition of video capture and video encoding accelerator and display H/W blocks for enhancing performance and quality, and reducing power consumption of the total solution.

The major blocks in ECD(A3) are as follows:

- ARM920 MacroCell
- 256KB On-chip SRAM Data Memory
- 4 x 40KB Frame buffers
- Host Interface(HIF)
- External Bus Interface(EBI)
- Audio Interface(AIF)
- Video Capture Unit(VCU)
- Motion Estimation unit(MEU)
- Display Unit(DU)
- UART
- I2C
- 16 General Purpose Inputs/Outputs(GPIO)
- Real Time Clock(RTC)
- Interrupt Control Unit(ICU)
- Power Management unit

2) OSD

OSD(LC78715) is a system LSI to output movie from ECD(A3) with OSD to LCD panel. Output data consists of digital 65536 colors movie data and 256 color OSD.

OSD(LC78715) has RGB picture memory(for movie and picture 176 x 220 x 16 bit) and 2 OSD frame memories(176 x 220 x 8 bit).

-Features

- LCD I/F
driver LC13002 is available

-CPU(TRIDENT)I/F

Address has 17 bits width. Data has 16 bits width. When the Msbit of address is "1, CPU(TRIDENT) can access(write/read) registers. When the Msbit of address is "0", CPU can access frame memories. Data bis width is selectable 16bit or8bit.

-ECD(movie engine)I/F

-OSD block copy function

Rectangle OSD data in a frame memory can be copied to another place by OSD block copy function. This function is available both in inter frame copy and in intra frame copy.

-System clock

System clock is 27 MHz.

3) CODEC(STW5094)

CODEC(STW5094) is a low power Stereo Audio DAC device with Headphones Amplifiers for high quality MP3 and FM radio listening. The STW5094 includes also an high performance low power combined PCM CODEC/FILTER tailored to implement the audio front-end functions required by low voltage low power consumption digital cellular terminals with added MP3 and FM radio listening.

STW5094 offers a number of programmable functions accessed through an I2C-bus compatible interface. The STW5094 Stereo Audio DAC section is suited for MP3, or any other stereo source, listening. It supports all the MP3 rates from 8kHz to 48kHz. The audio data serial interface is I2s compatible and can be programmed to handle 16 to 24 bit word length input data. The internal D to A converters work with 18bit input resolution. The STW5094 Voice Codec section can be configured either as a 14-bit linear or as an 8-bit companded PCM coder. The Voice Codec can be either the standard 8kHz value or the extended 16kHz one. In addition to the Stereo Audio DAC and CODEC/FILTER function, STW5094 includes a Tone/Ring/DTMF generator that can be used both in Audio Listening mode and in Voice Codec mode, a sidetone control function tailored to handle an external on-hook off-hook button.

4) FLASH MEMORY(INTEL)

The 3-Volt Advanced+ Boot Block Flash Memory product line is a high performance memory utilize reliable. This FLASH memory feature 1.65V - 2.5V or 2.7V - 3.6V I/Os and a low Vcc/Vpp operating range of 2.7V - 3.6V for Read, Program, and Erase operations. Bus width of this memory is 16bit. A3 chip is multimedia processor, therefore A3 chip needs operation program. The program is stored this memory by Downloader PGM. A3 system uses Intel's this memory, GE28F160C3BC70. It is consisted of 16M bits flash memory. It has 16 bit data line, D[0~15] which is connected to A3 chip It has 20 bit address lines, A[1~20]. They are connected too. _XCSO, chip select signals in the A3 chip enable this memory. This uses 3 volt supply voltage. During writing process, _X_WR is low and it enables writing process to flash memory. During reading process, _X_RD is low and it output information which is located at the address from the A3 chip in the flash memory. Reading or writing procedure is processed after _X_WR or _X_RD is

5) NAND FLASH MEMORY(K9F5608U08-DIB0)

This memory offered in 32Mx8bit, the K9F5608U08-DIB0 is 256Mbit with *M bit capacity. The device is offered in 3 Volt Vcc. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation programs the 528-byte page in typical 200usec and an erase operation can be performed in typical 2msec on a 16K-byte block. Data in the page can be read out at 50nsec cycle time per word. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip writ control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. This memory is an optimum solution for large nonvolatile storage applications such solid state file storage and other portable applications requiring non-volatility. A3 system uses SAMSUNG Semiconductor's memory, K9F5608U08-DIB0. It is consisted of 256M bits NAND flash memory. Multimedia contents(MPEG and MP3) are stored this memory by downloader Program. It has 8bit I/O line, XD[0~7] which is connected to A3 chip These pins's function are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled. XA(0) is COMMAND LATCH ENABLE(CLE). The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports

on the rising edge of the WE signal.

XA(1) is ADDRESS LATCH ENABLE(ALE). input controls the activating path for address to the internal address.

Address are latched on the rising edge of WE with ALE high. `_XCS3` is chip enable and `_X_RD` is Read Enable and `_X_WE` is Write Enable. GPIO15 is READY/BUSY OUTPUT. The pin output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z when the chip deselected or when outputs are disabled

6) Audio Amplifier(LM4890)

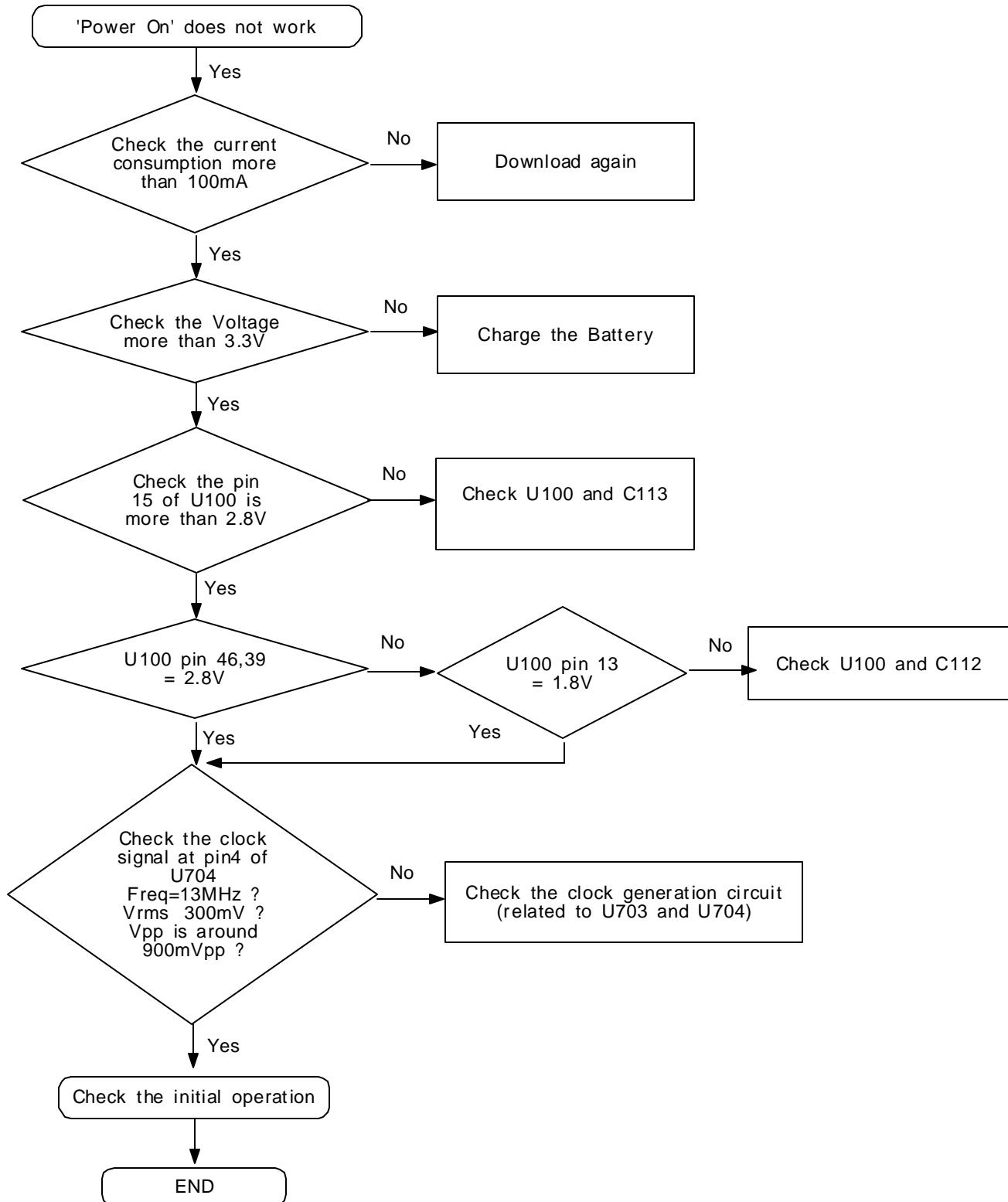
The LM4890 is a dual audio power amplifier capable of delivering 200mW of continuous average power into an 8 ohm load with 0.1% from a 5V power supply.

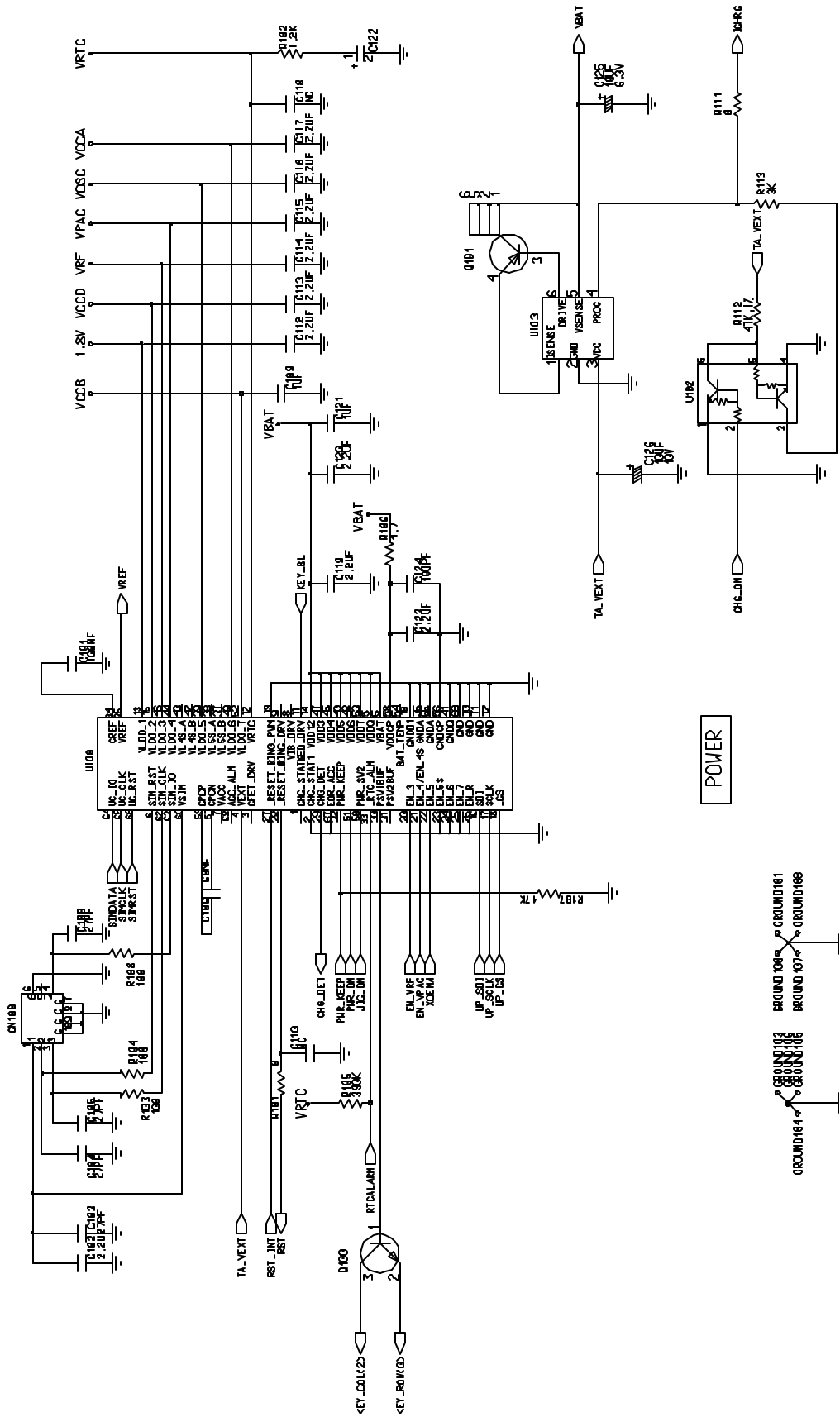
Boomer audio power amplifier was designed specifically to provide high quality output power with a minimal amount of external components using surface mount packing. Since the LM4890 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems. The LM4890 features an externally controlled, low power consumption shutdown mode which is virtually clickless and popless, as well as an internal thermal shutdown protection mechanism. The unity-gain stable LM4890 can be configured by external gain-setting resistors.

3. SGH-V100 Flow Chart of Troubleshooting

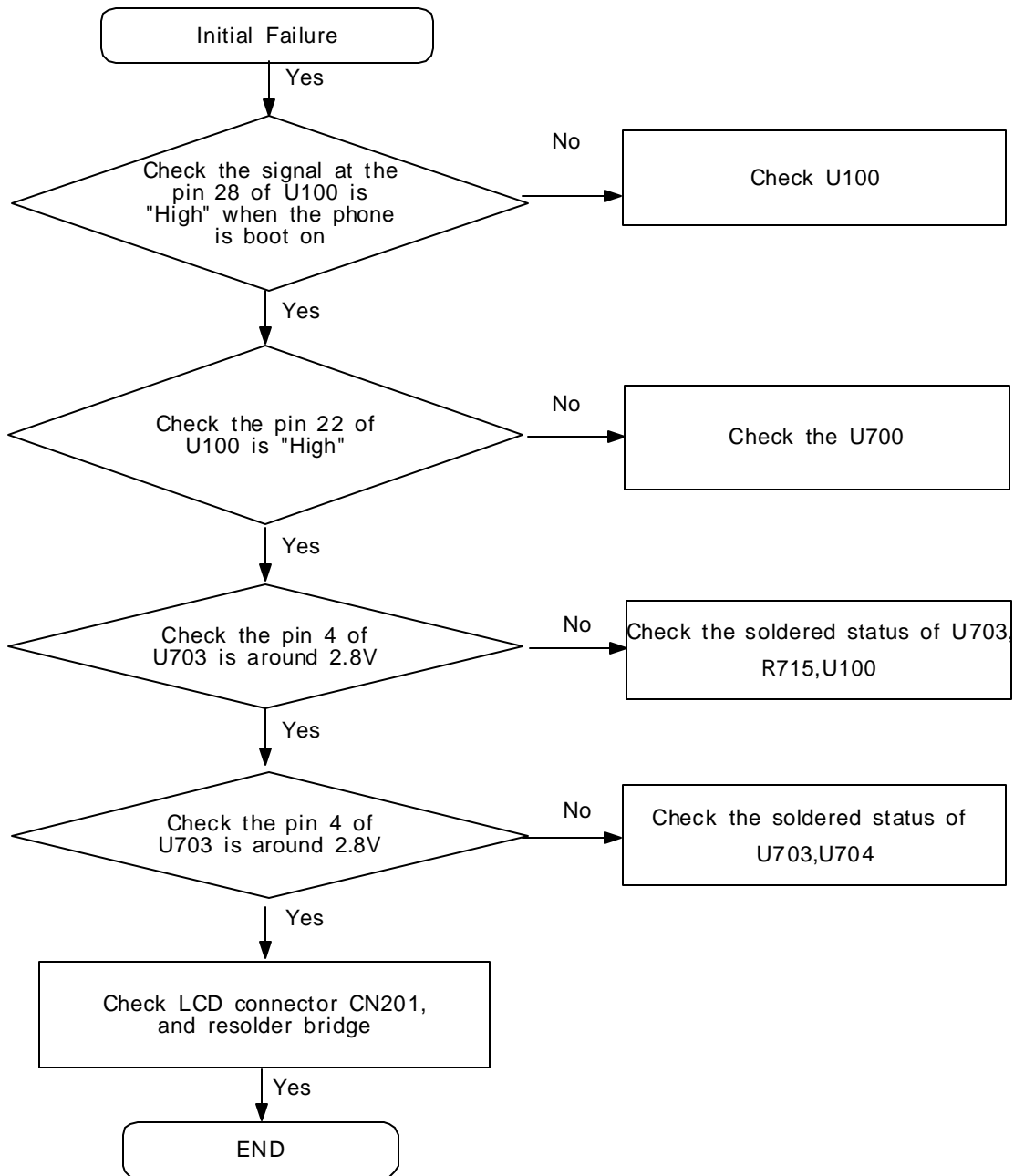
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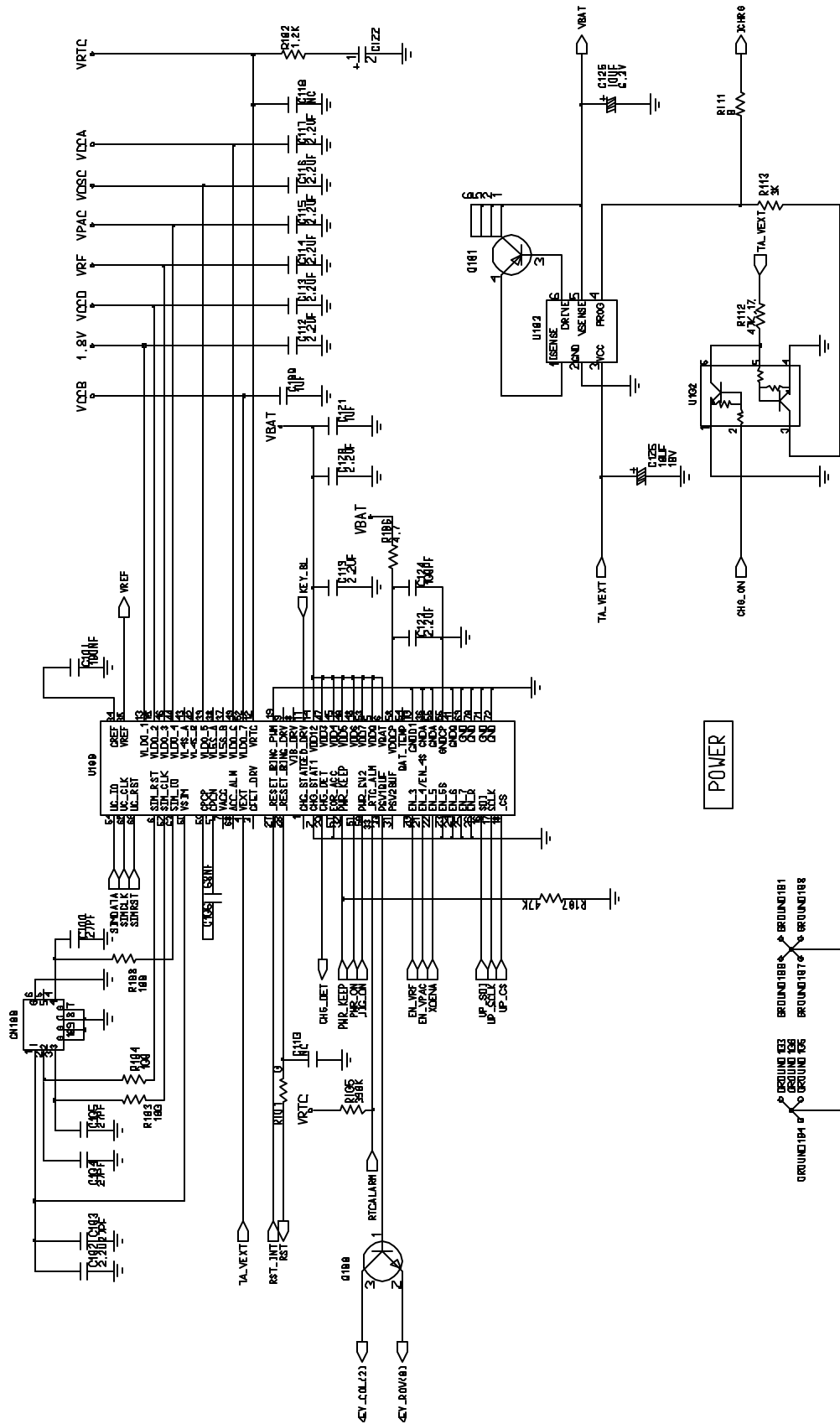
1. Power ON



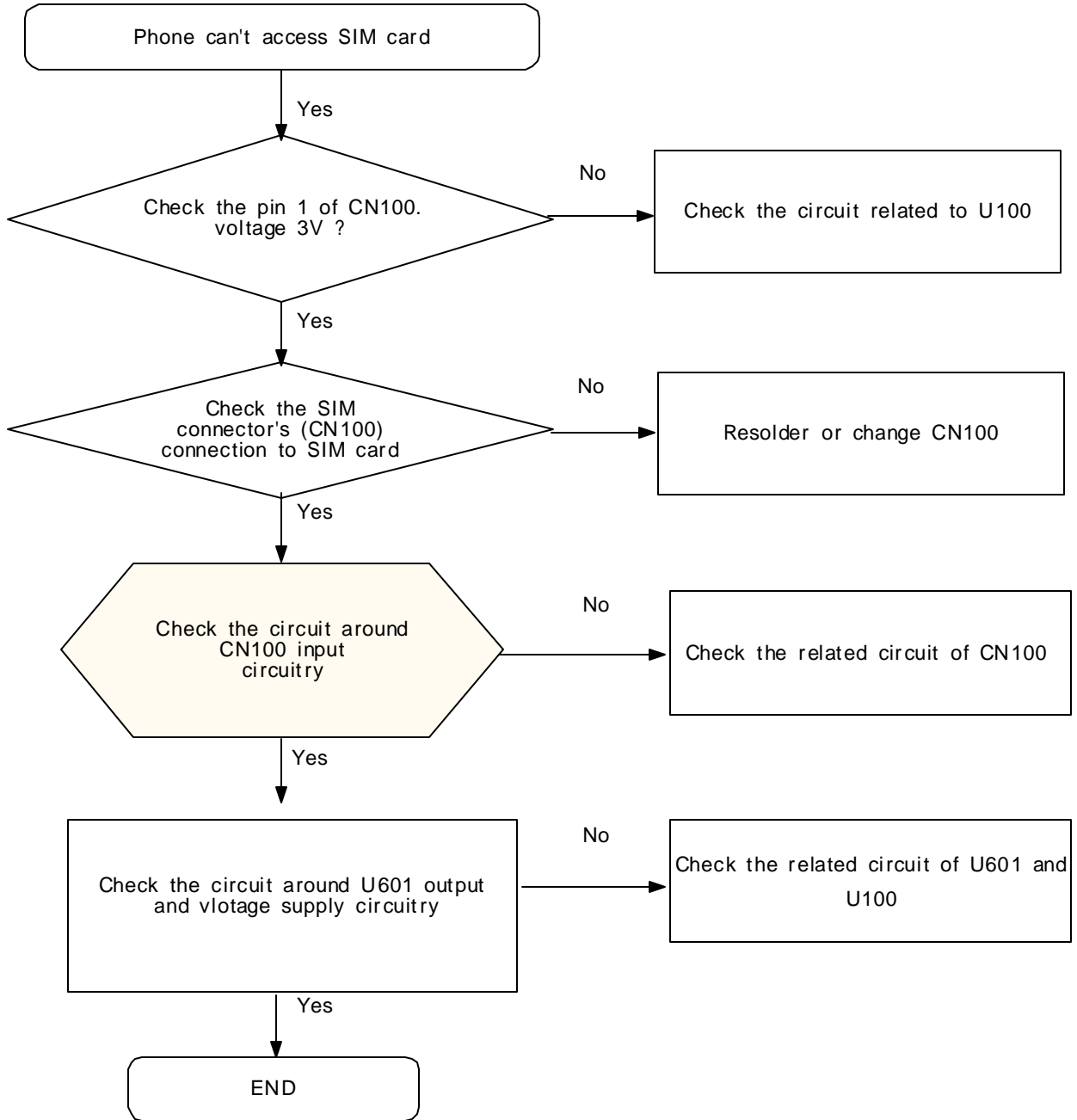


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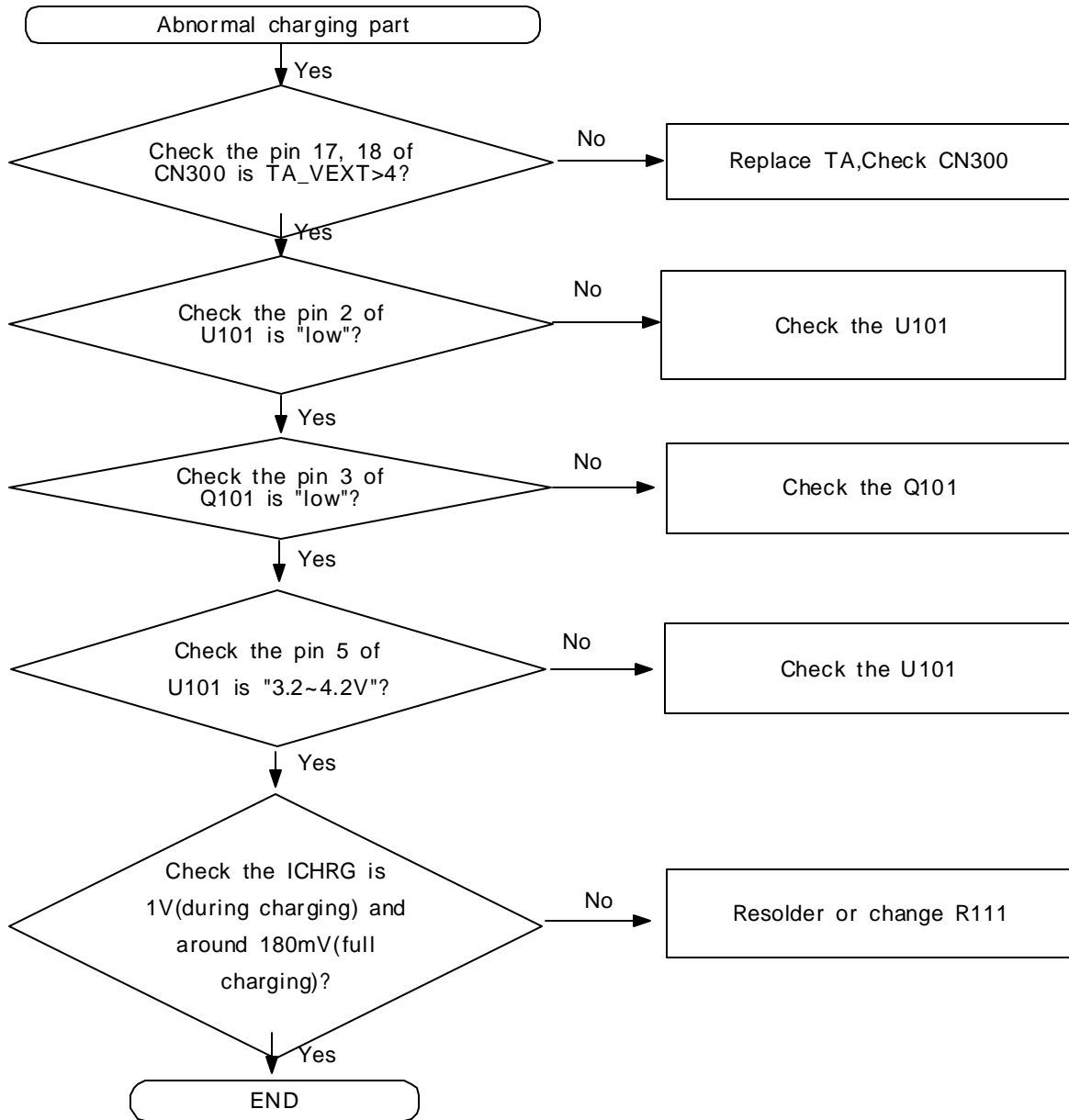




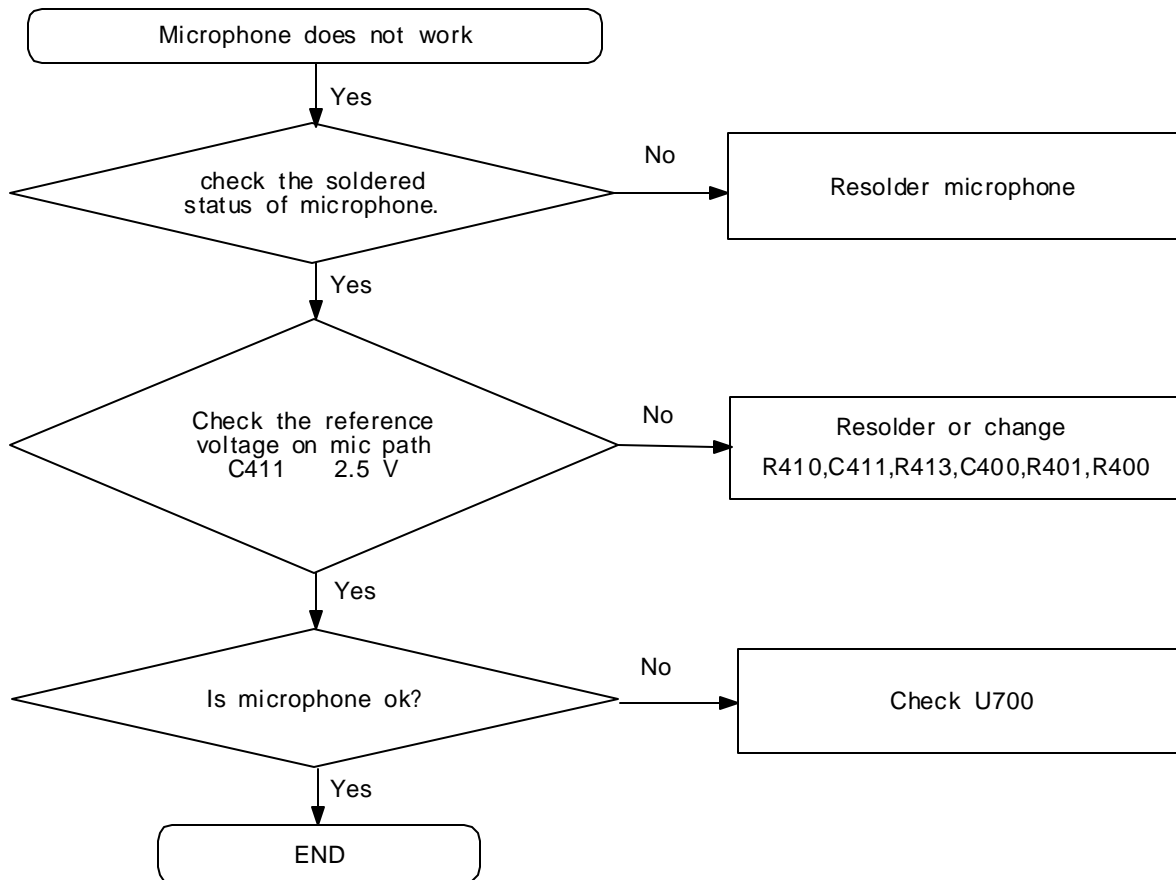
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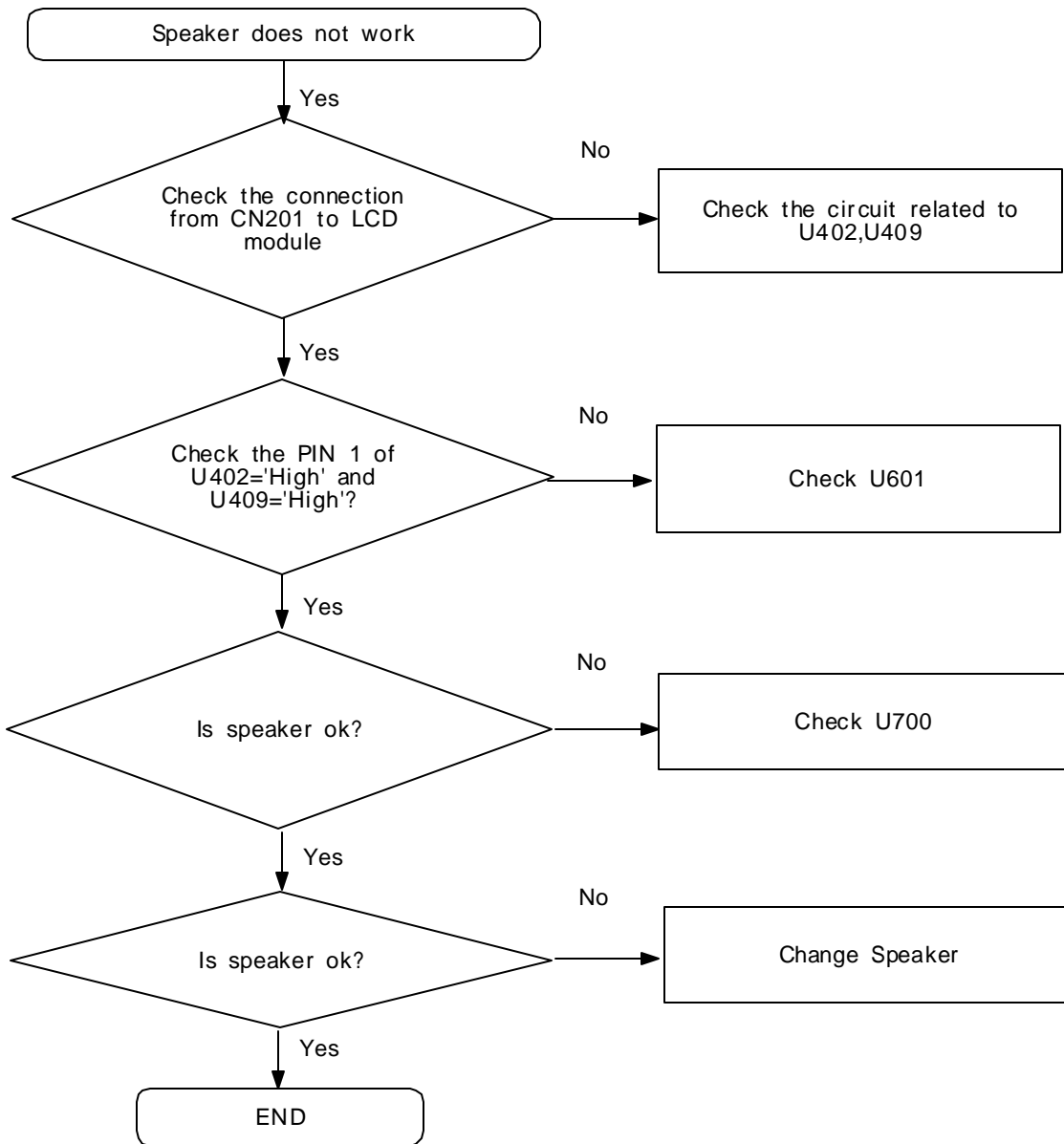
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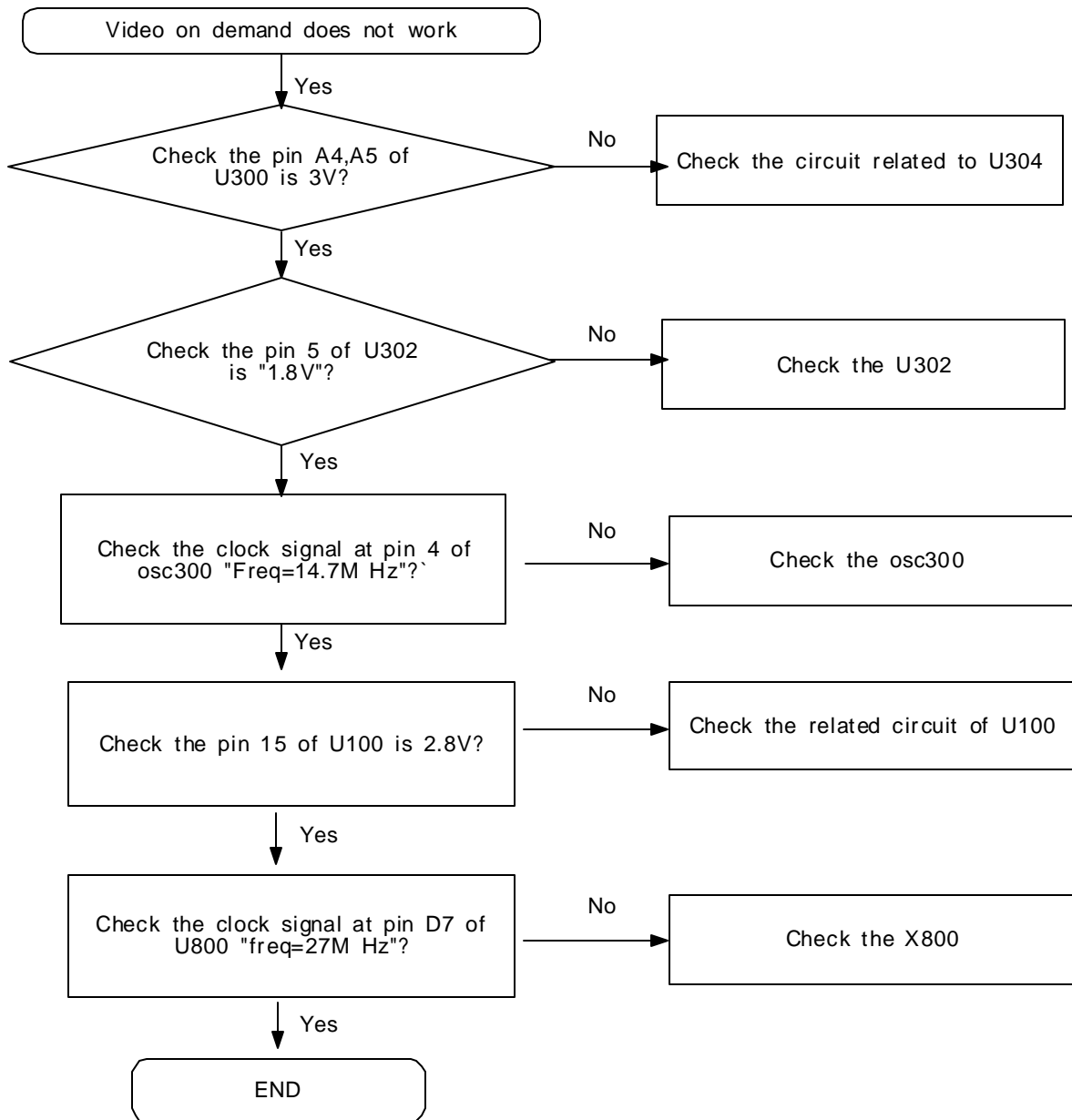
5. Microphone Part



6. Speaker Part

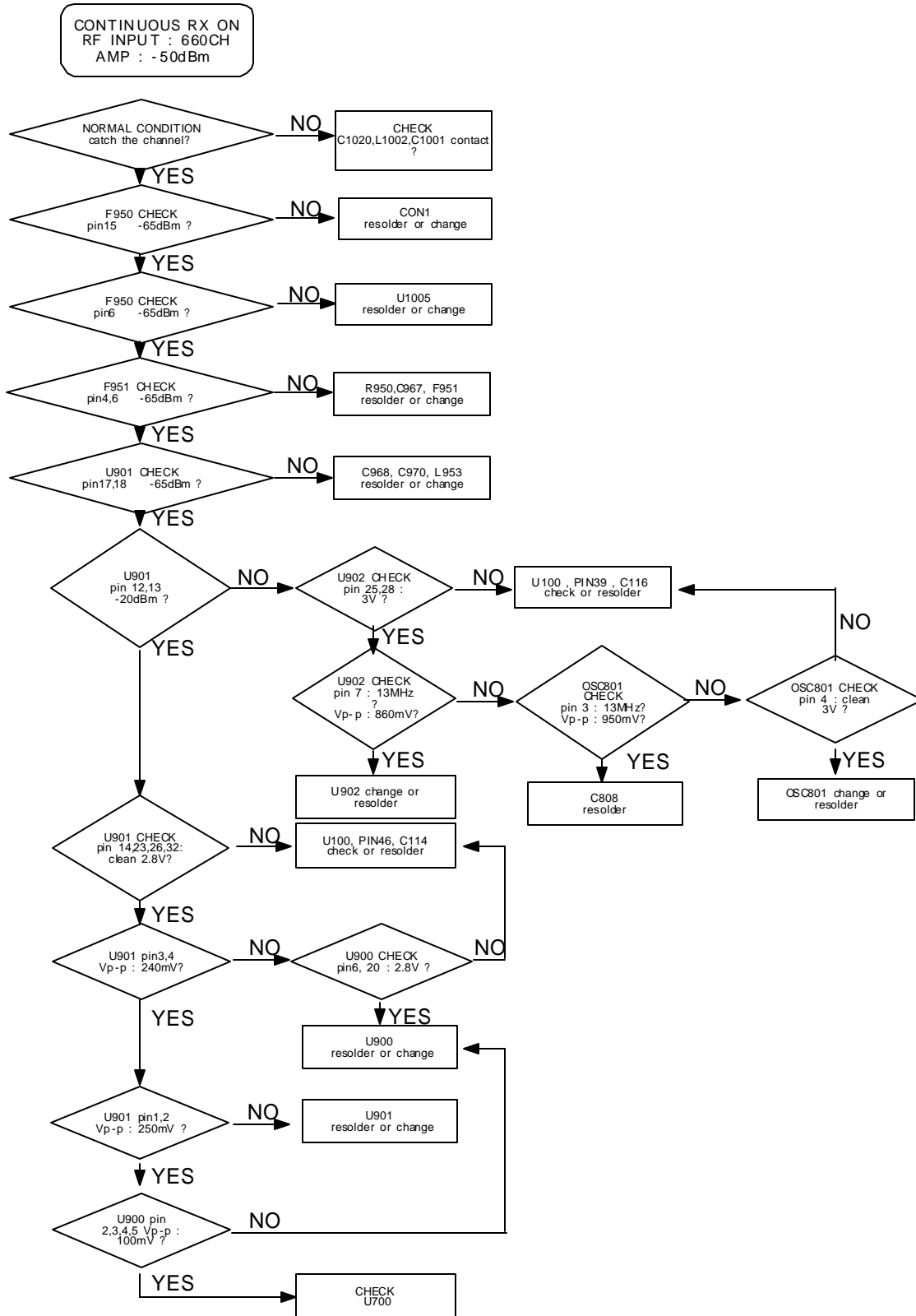


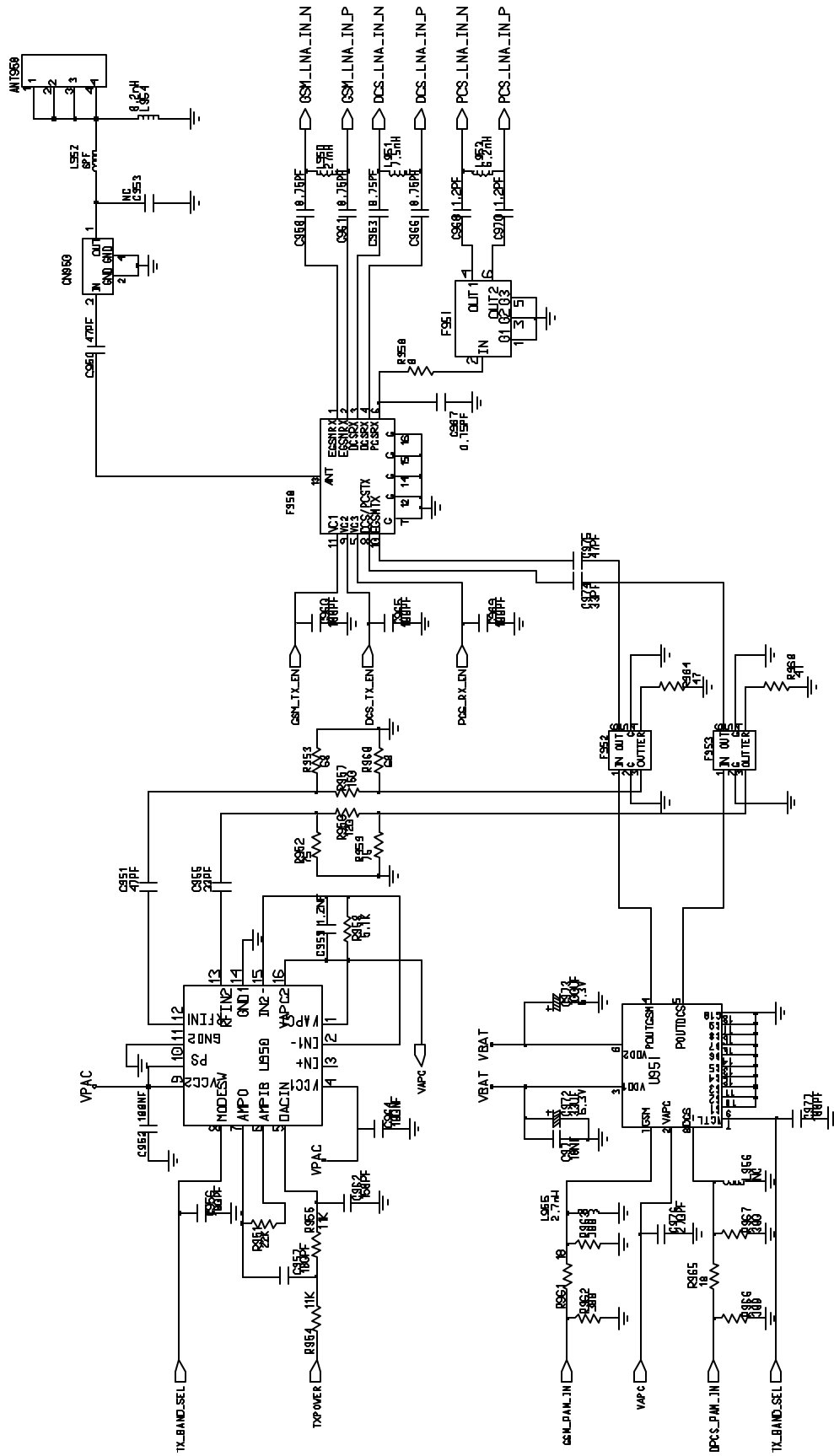
7. Vod Part



2.RF

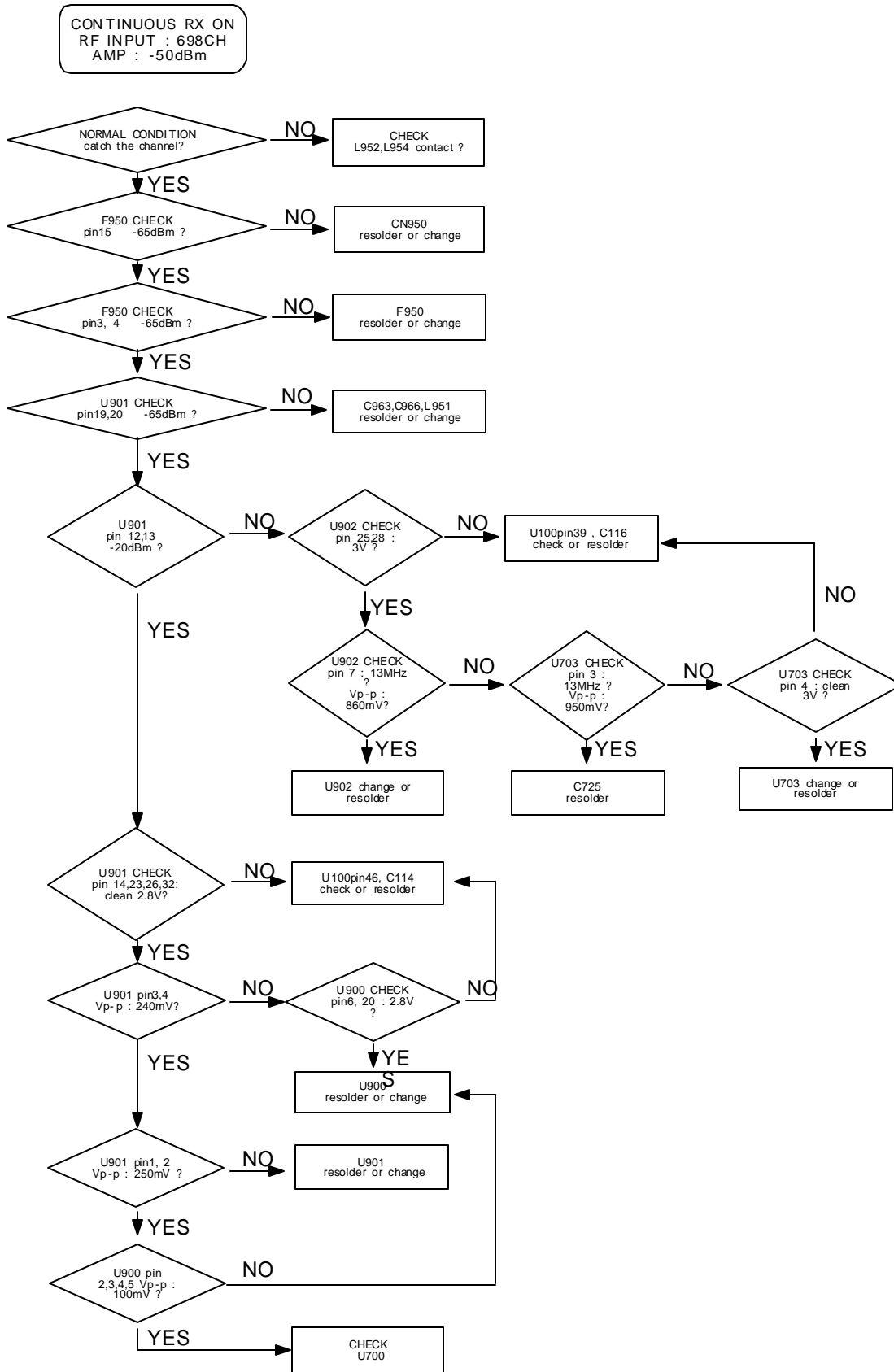
1. PCS Receiver



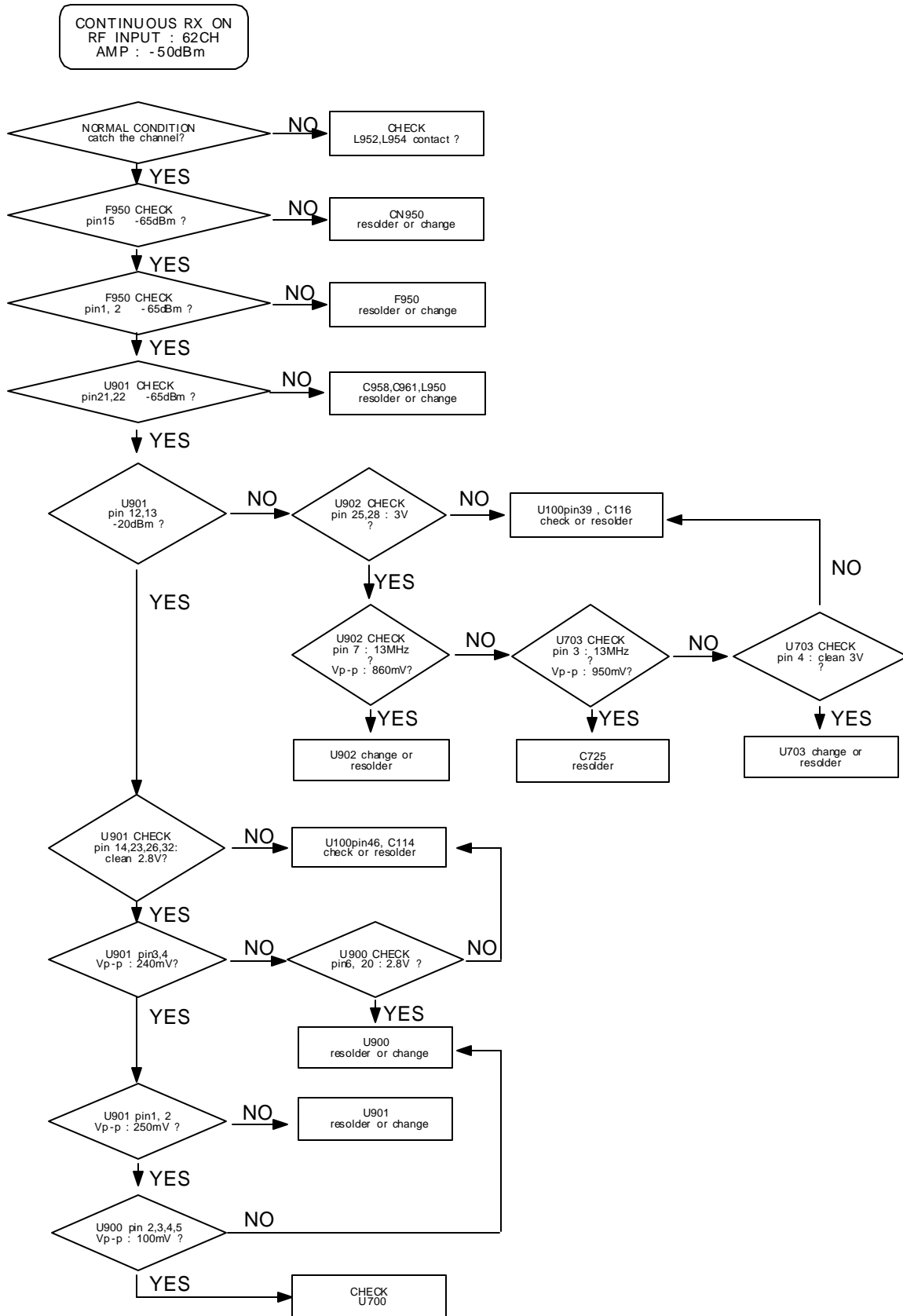


TRANSMITTER & RECEIVER

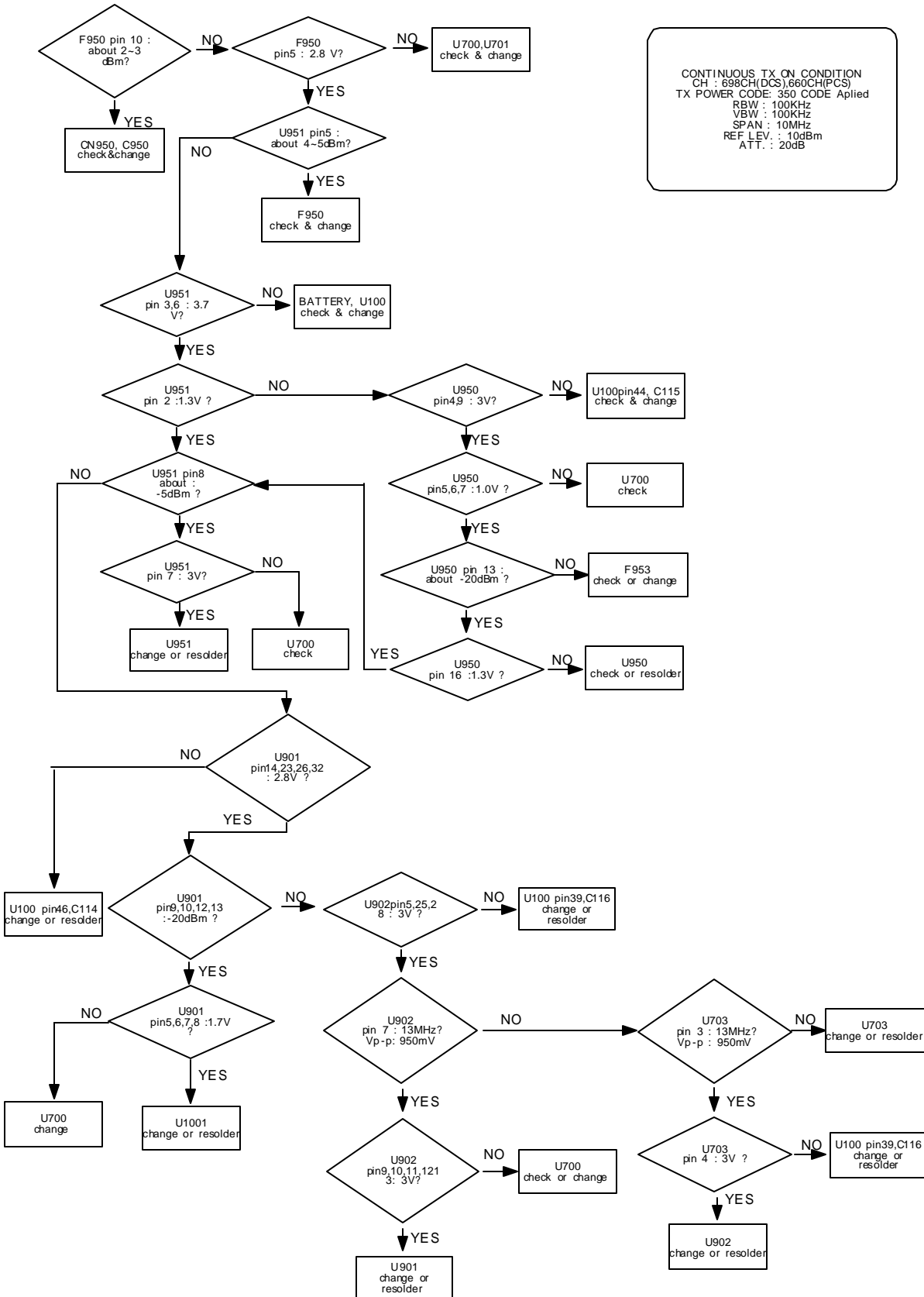
2. DCS Receiver



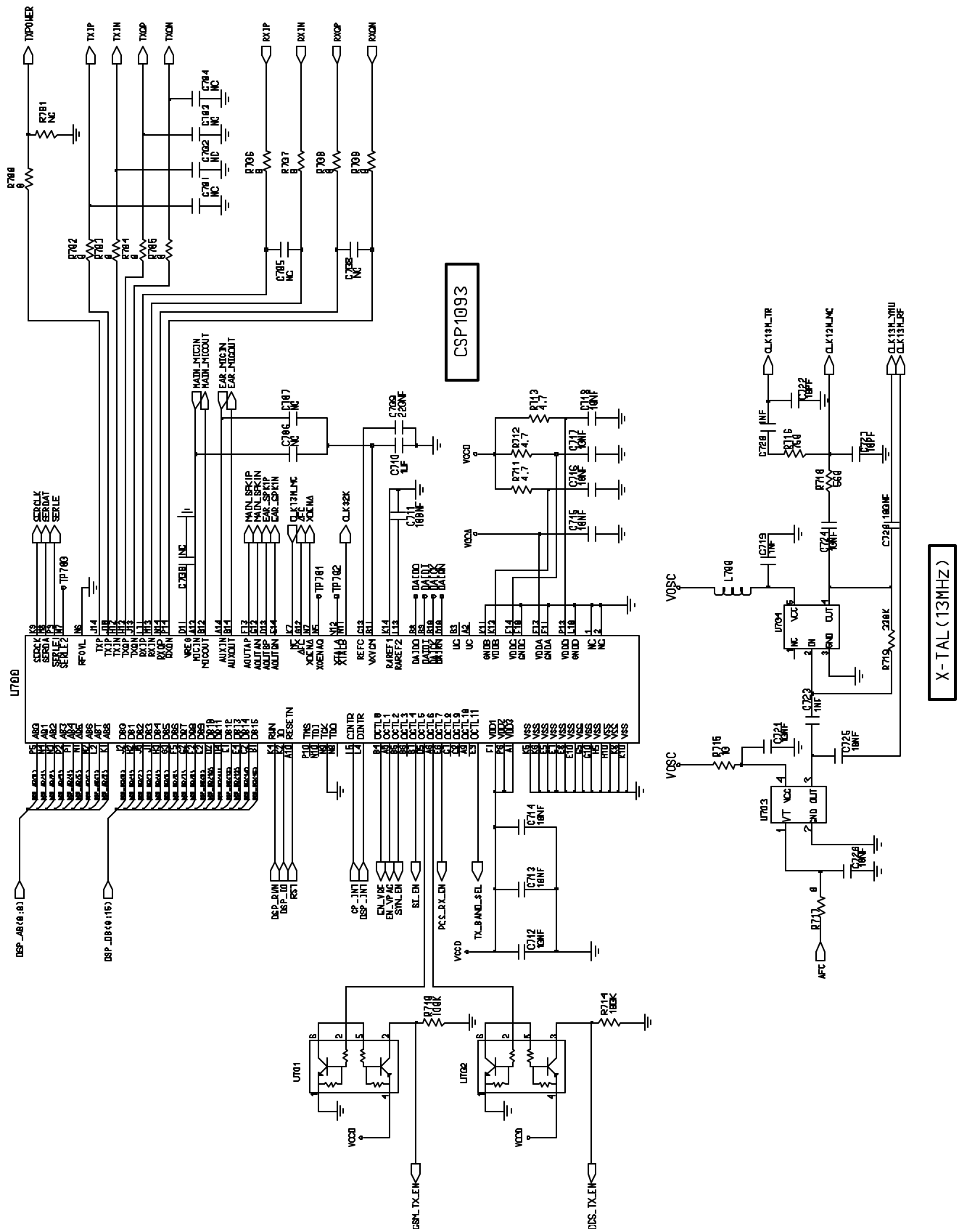
3. EGSM Receiver

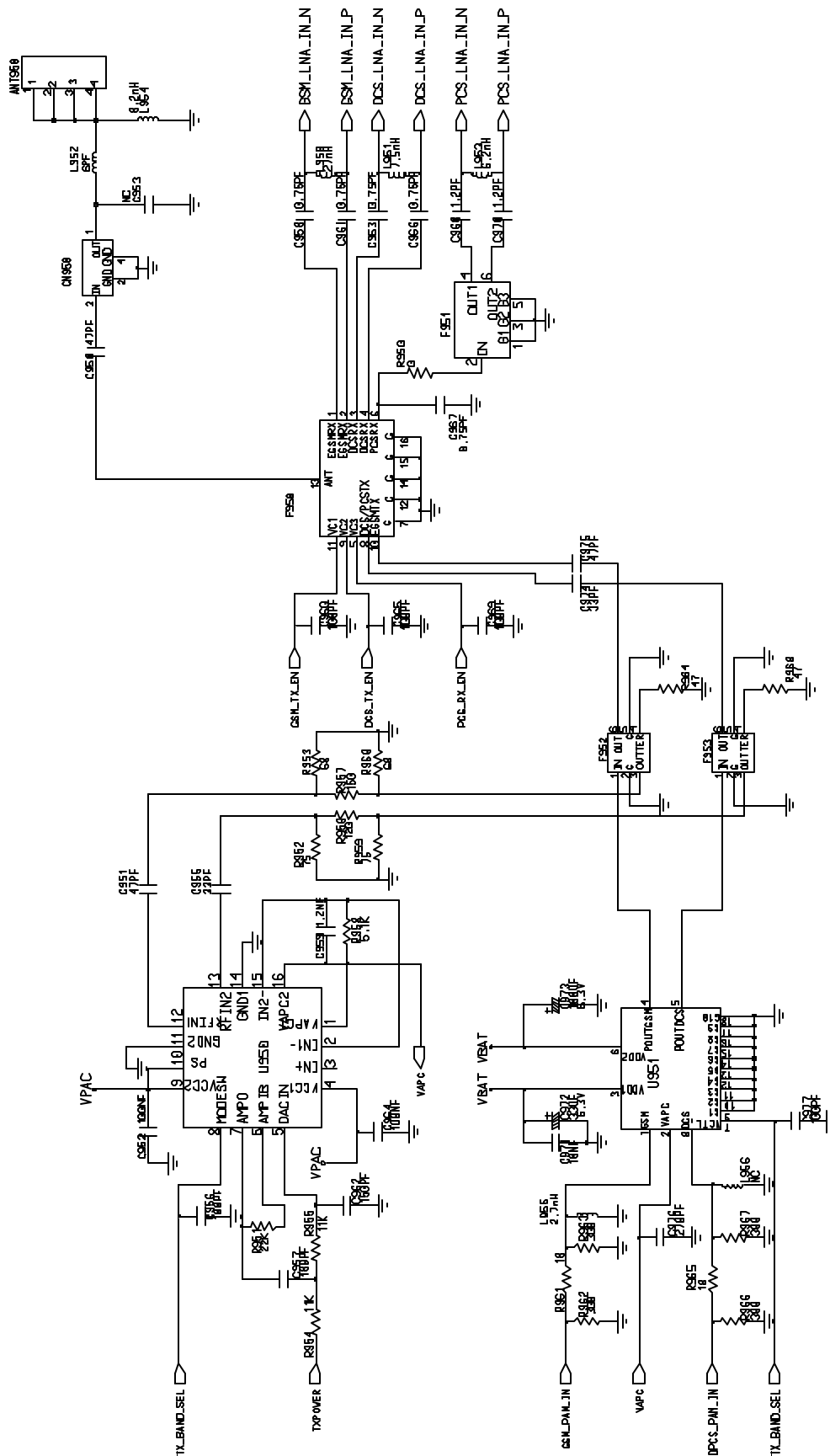


4. DPCS Transmitter



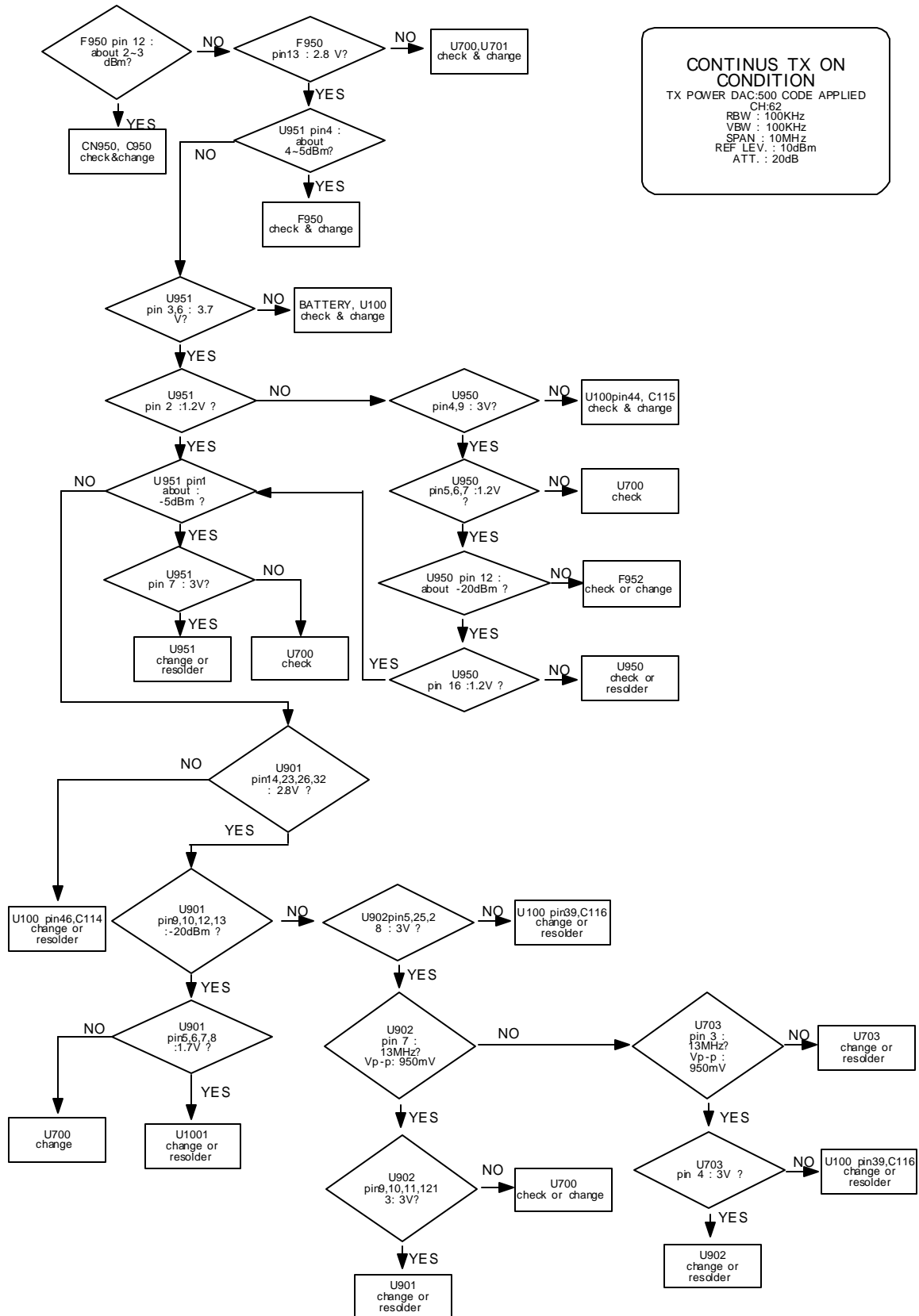
CONTINUOUS TX ON CONDITION
 CH : 698CH(DCS),660CH(PCS)
 TX POWER CODE: 350 CODE Applied
 RBW : 100KHz
 VBW : 100KHz
 SPAN : 10MHz
 REF LEV. : 10dBm
 ATT. : 20dB



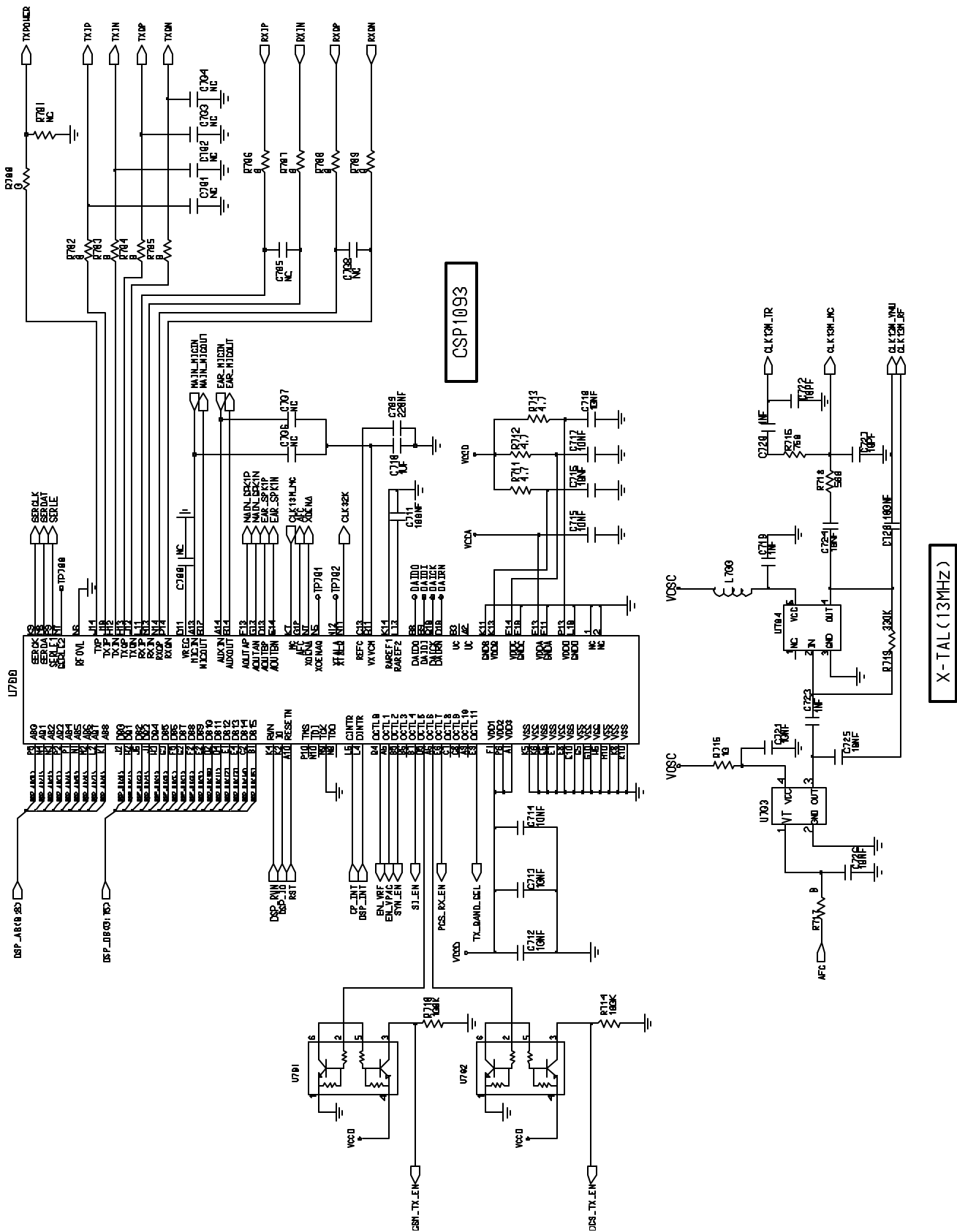


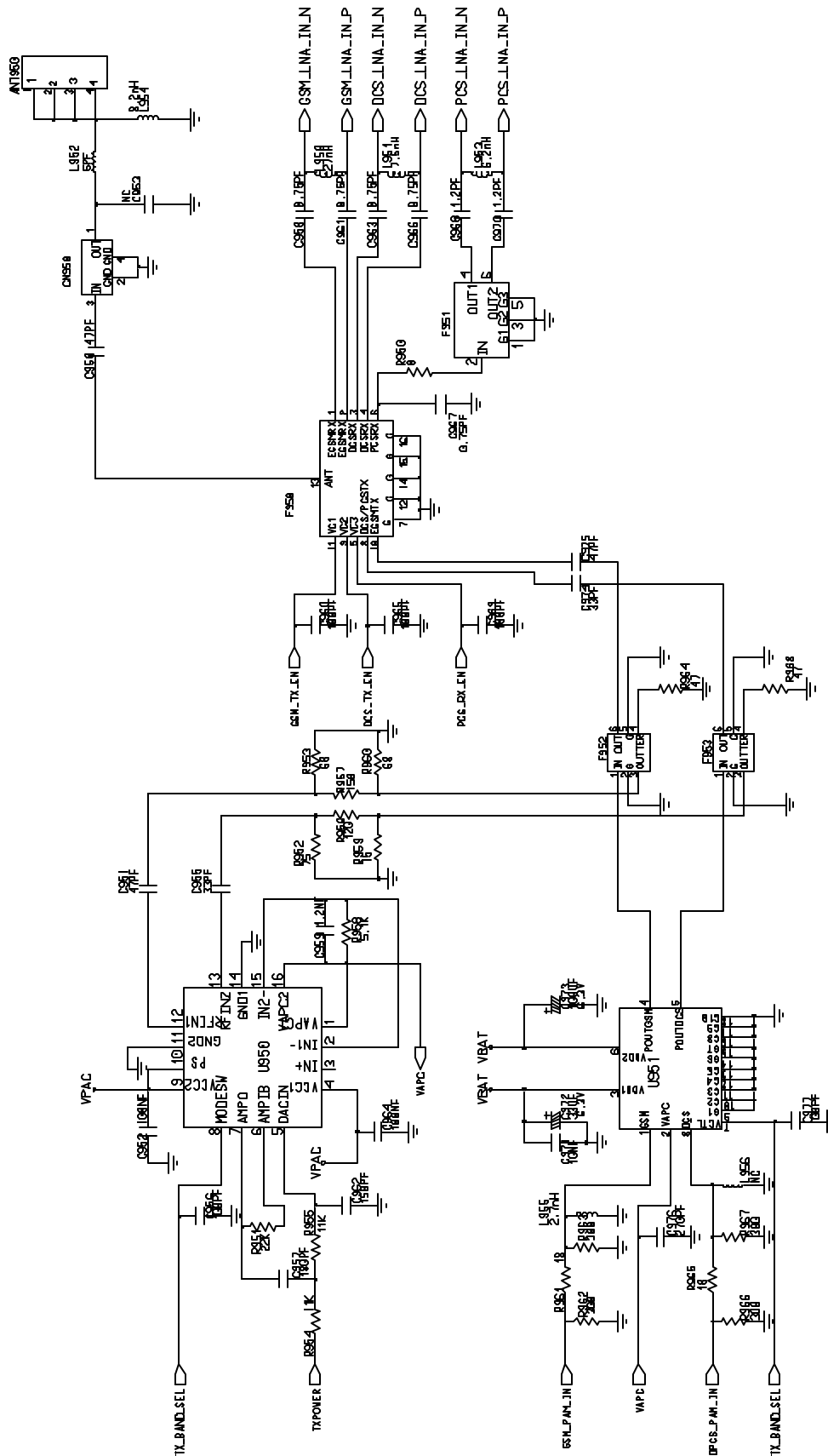
TRANSMITTER & RECEIVER

5. EGSM Transmitter



**CONTINUS TX ON
CONDITION**
 TX POWER DAC:500 CODE APPLIED
 CH:62
 RBW : 100KHz
 VBW : 100KHz
 SPAN : 10MHz
 REF. LEV. : 10dBm
 ATT. : 20dB

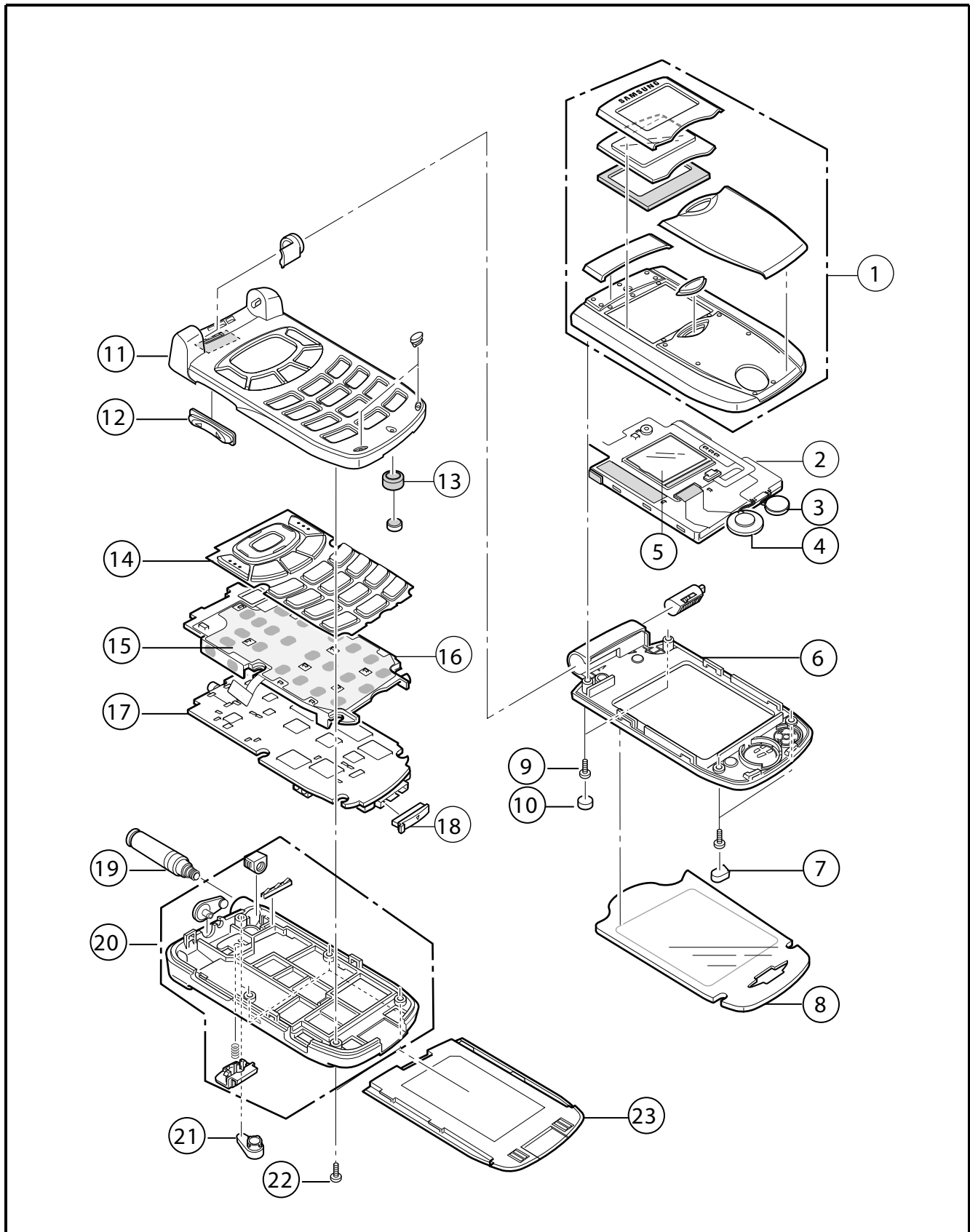




TRANSMITTER & RECEIVER

4. SGH-V100 Exploded View and its Parts list

1. Cellular phone Exploded View



2. Cellular phone Parts list

Location NO.	Description	SEC CODE	Remark
1	FOLDER UPPER	GH75-02536A	
2	MAIN LCD	GH07-00206A	
3	MOTOR	3101-001326	
4	SPEAKER	3001-001361	
5	DUAL LCD	GH07-00263A	
6	FOLDER LOWER	GH75-02537A	
7	FOL/SCREW COVER	GH73-01757A	
8	WINDOW LCD	GH72-06312A	
9	SCREW	6001-001479	
10	FOL/SCREW COVER	GH73-01756A	
11	FRONT COVER	GH75-02535A	
12	VOLMUE KEY	GH75-02540A	
13	MIC	GH59-00138A	
14	KEYPAD	GH75-02538A	
15	DOME SHEET	GH59-00550A	
16	SHIELD COVER	GH71-01281A	
17	MAIN PBA	GH92-01361A	
18	CONNECTOR COVER	GH73-01536A	
19	ANTENNA	GH42-00244A	
20	REAR COVER	GH75-02539A	
21	RF COVER	GH73-01630A	
22	SCREW	6001-001479	
23	BATTERY	GH43-00725A	900MAH
		GH43-00726A	780MAH

3. Test Jig (GH80-00865A)



3-1. RF Test Cable
(GH39-00090A)



3-2. Test Cable
(GH39-00127A)



3-3. Serial Cable



3-4. Power Supply Cable



3-5. DATA CABLE
(GH39-00159A)



3-6. TA
(GH44-00184A)



5. SGH-V100 MAIN Electrical Parts List

SEC Code	Design LOC
BSGH-V100	
GH92-01361A	
GH41-00349A	
GH96-01257A	
GH59-00550A	
GH71-01281A	
GH73-01790A	
GH74-04273A	
GH74-04274A	
GH71-00566A	ANT950
2203-000679	C100
2203-005061	C101
2203-001598	C102
2203-000679	C103
2203-000679	C104
2203-000679	C105
2203-005483	C106
2203-005065	C109
2203-001598	C112
2203-001598	C113
2203-001598	C114
2203-001598	C115
2203-001598	C116
2203-001598	C117
2203-001598	C119
2203-001598	C120
2203-005065	C121
4302-001119	C122
2203-001598	C123
2203-000233	C124
2404-001105	C125
2404-001268	C126
2203-001239	C200
2203-000812	C201
2203-005061	C202
2203-000679	C203
2203-000679	C204
2203-000679	C205
2203-000679	C206
2203-000679	C207
2203-000679	C208
2203-000679	C209

SEC Code	Design LOC
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2203-000679	C213
2203-000679	C214
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2203-000679	C228
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2203-005061	C246
2203-006053	C249
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2203-005061	C301
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2203-000233	C310
2203-005061	C311

SEC Code	Design LOC
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2203-005061	C316
2404-001105	C317
2203-005061	C318
2404-001105	C319
2203-000995	C320
2203-000995	C321
2203-005065	C400
2404-001105	C403
2203-005065	C404
2203-000812	C405
2203-005393	C406
2404-001151	C411
2203-005061	C412
2203-000359	C417
2203-000425	C418
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2203-000679	C623
2203-005496	C709
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2203-005061	C711
2203-000254	C712
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2203-000438	C720
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2203-000254	C725
2203-000254	C726
2203-000278	C727
2203-005061	C728
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2203-005061	C801
2203-000233	C802
2404-000335	C803
2404-001105	C804
2203-000233	C900
2203-000233	C901
2203-000233	C902
2203-001405	C903
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2203-000233	C917
2203-000233	C918
2203-000233	C919
2203-001405	C920
2203-000995	C950
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SEC Code	Design LOC
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2203-000812	C955
2203-000233	C956
2203-005503	C957
2203-002677	C958
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4709-001279	F952
4709-001278	F953
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2703-001513	L400
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2703-002165	L951
2203-001170	L952
2703-002532	L953
2703-001733	L954
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0604-001146	LED600
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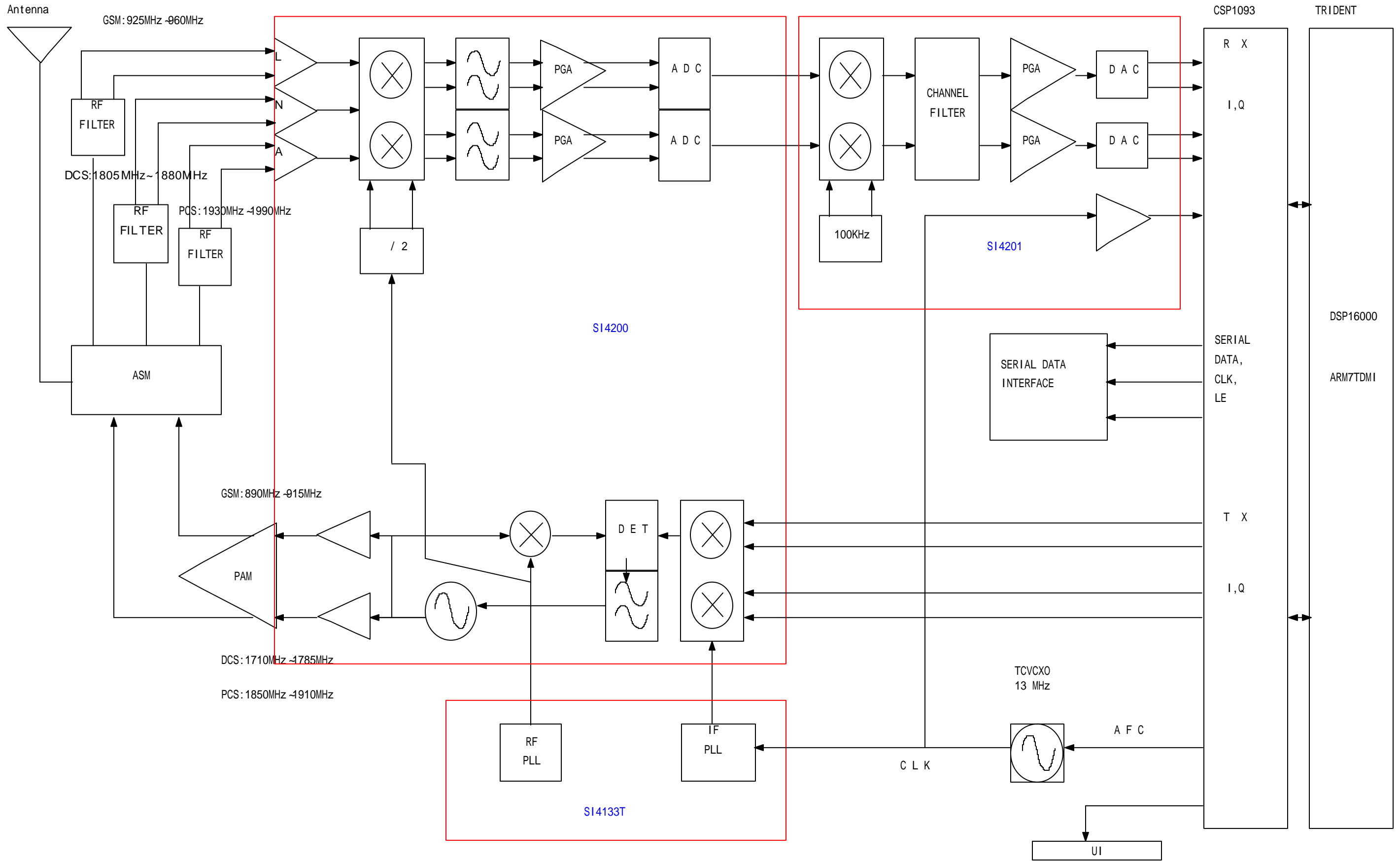
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SEC Code	Design LOC
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2007-001306	R957
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2007-001301	R960
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1205-002271	U301
1203-002690	U302
1107-001408	U303
1203-001285	U304
0801-002529	U305
0801-000794	U306
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1001-001152	U402
1205-002256	U403
1204-001960	U407
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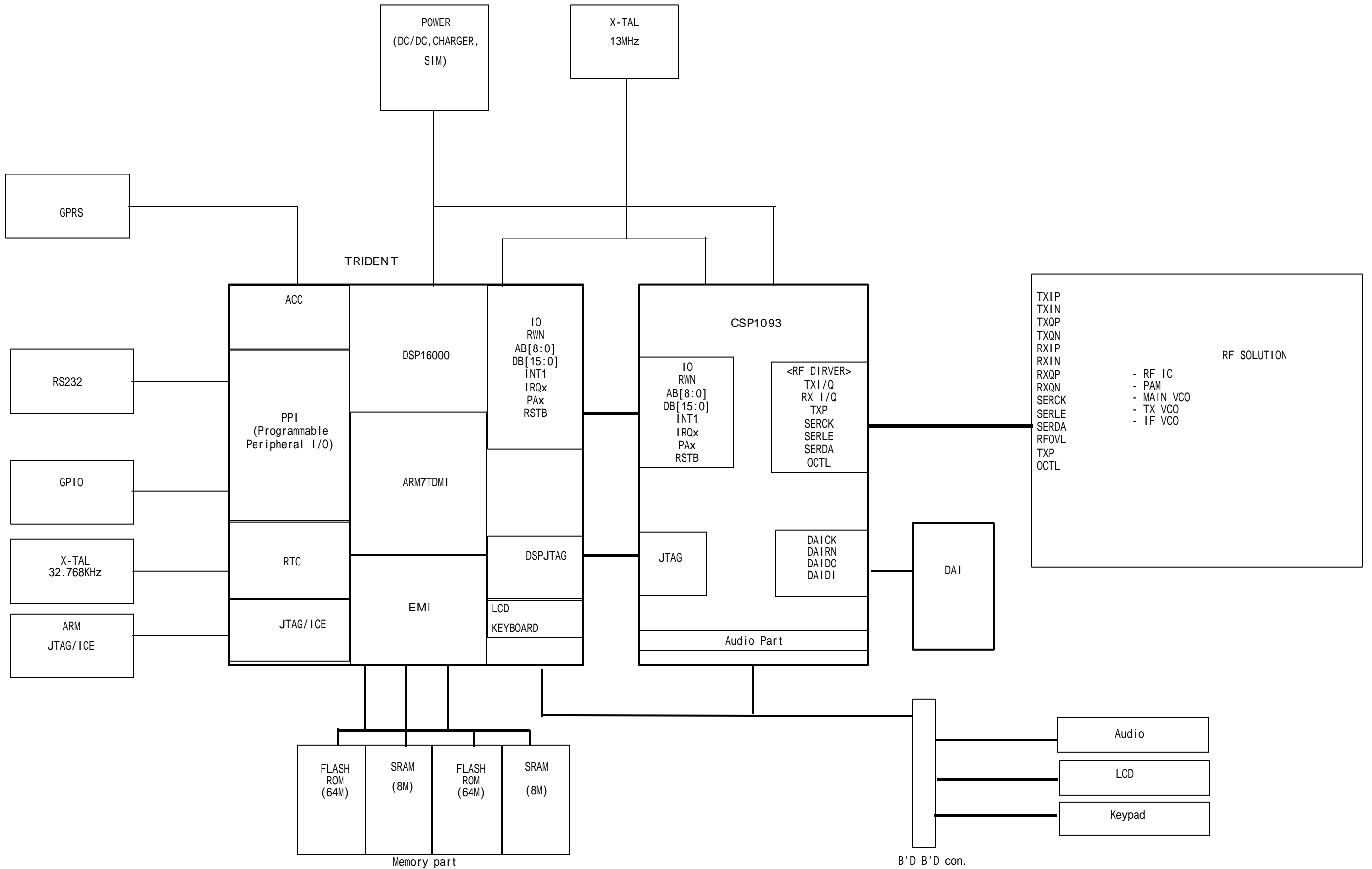
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0801-002540	U505
0801-002212	U506
GH09-00020A	U601
1209-001219	U602
GH09-00022A	U603
1204-001984	U700
0504-001042	U701
0504-001042	U702
2809-001260	U703
0801-002345	U704
GH13-00013A	U800
1203-002368	U801
1205-002185	U900
1205-002268	U901
1209-001434	U902
1209-001379	U950
1201-001982	U951
2203-000233	U952
2203-002443	U953
2203-002443	U954
2802-001104	X800
0406-001084	ZD200
0406-001084	ZD201
0406-001084	ZD202
0406-001084	ZD203
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0406-001150	ZD400
0404-001172	ZD800
0403-001047	ZD801

6. SGH-V100 Block Diagrams

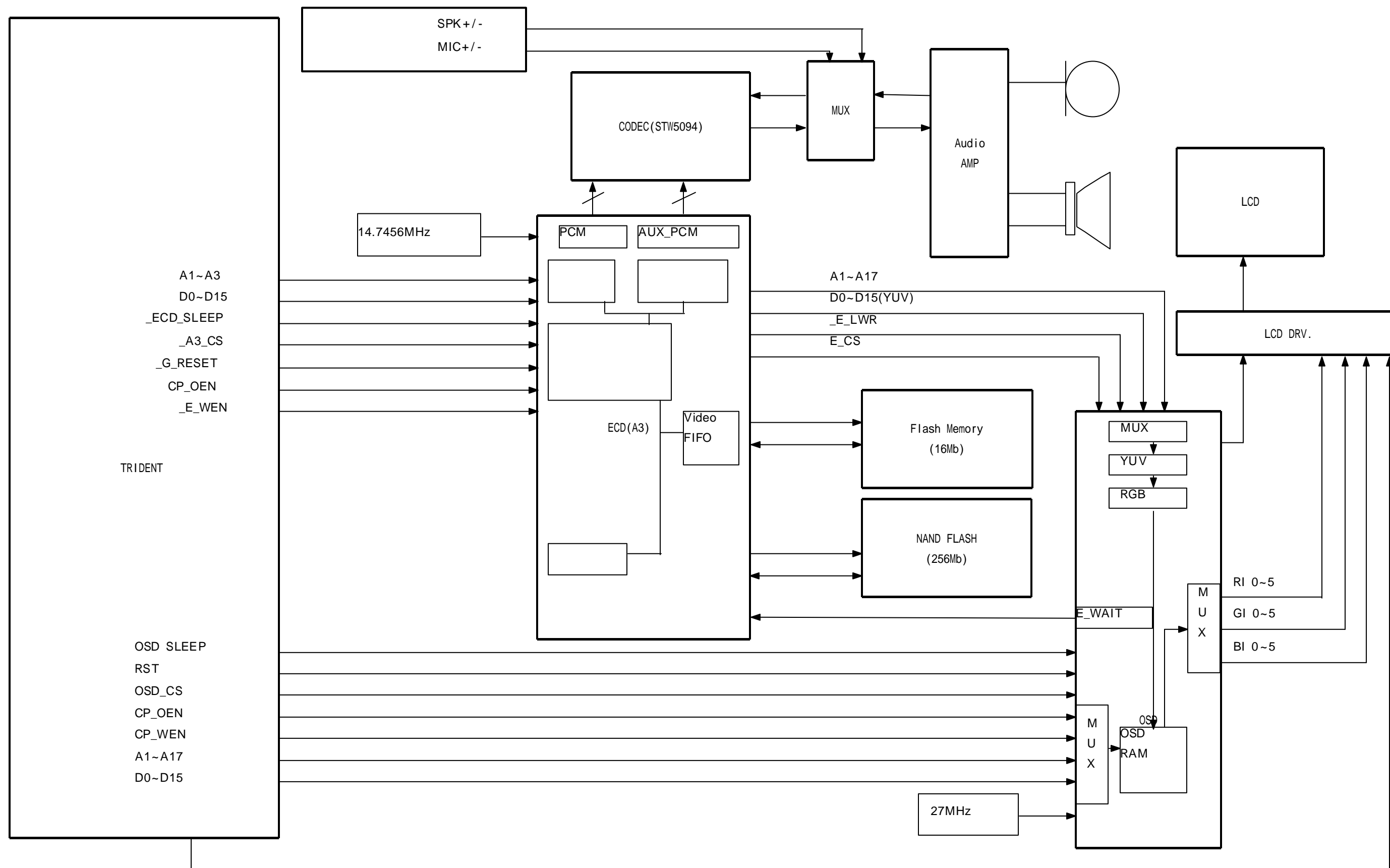
1. RF Solution Block Diagram



2. Base Band Solution Block Diagram

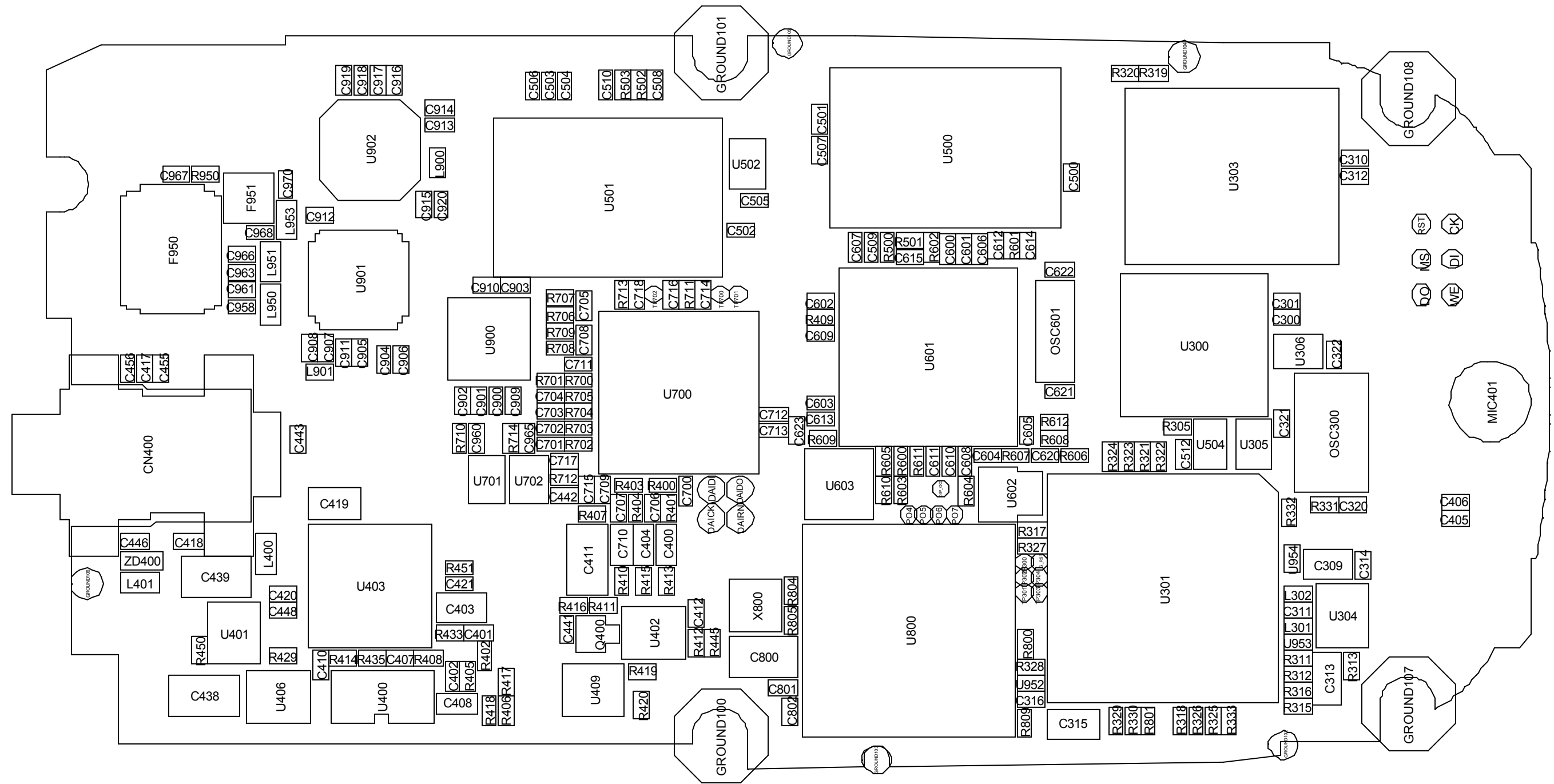


3. Video On Demand Block Diagram



7. SGH-V100 PCB Diagrams

1. Main PCB Top Diagram





ELECTRONICS

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BASIC.