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MACAO

CPU : STEALEY (A110)

Chip Set : 945GU + ICH7-U

Remarks : Ultra Mobile PC
WSVGA, HSDPA, DMB

Model Name : MACAO

PBA Name : BA41-00743A

Dev. Step : SR

Revision : 0.1

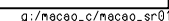
T.R. Date : 2007.03.15

DRAW	CHECK	APPROVAL
W.S. Ko	H.K. Park	J.S. Euh

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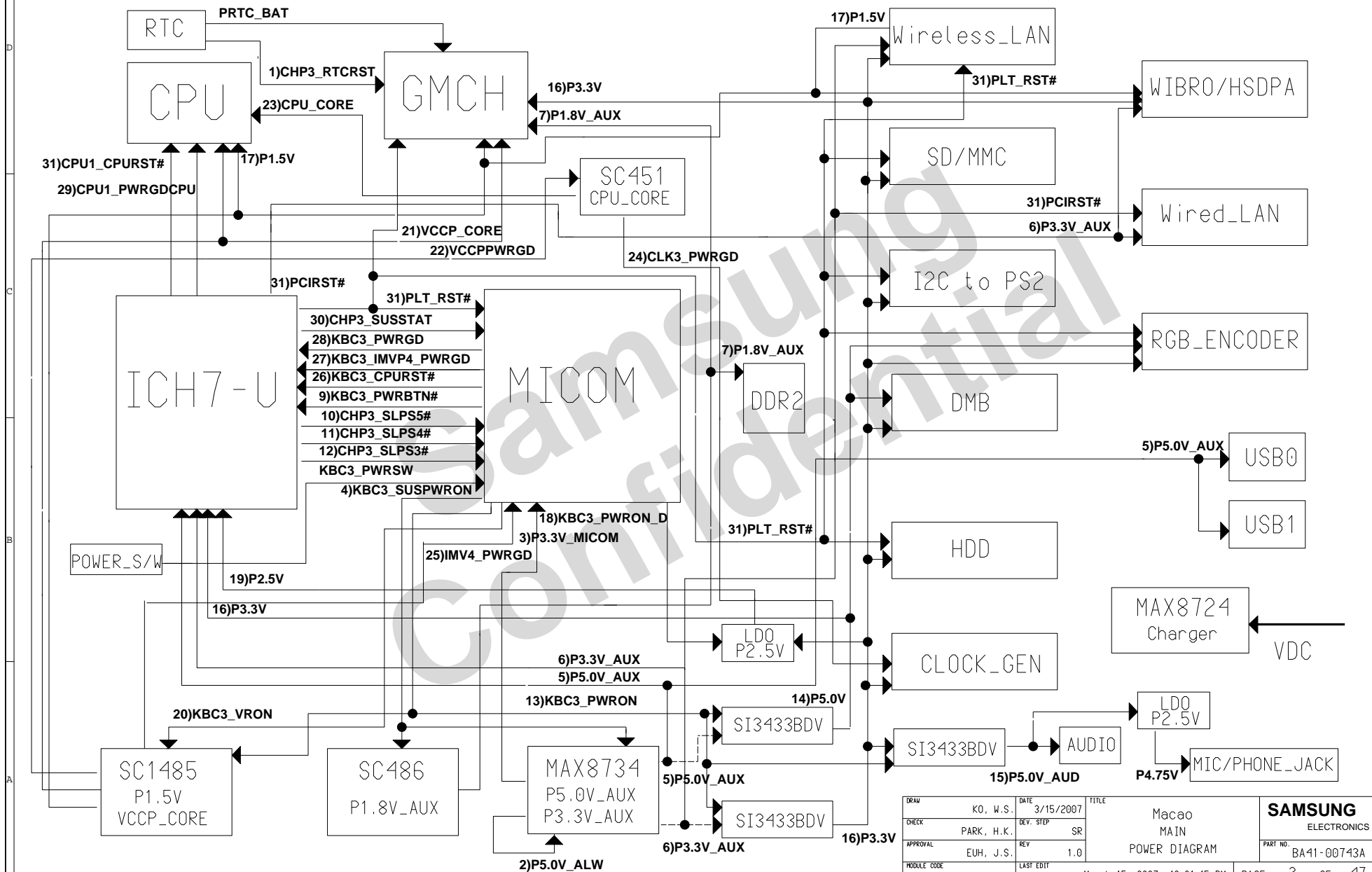
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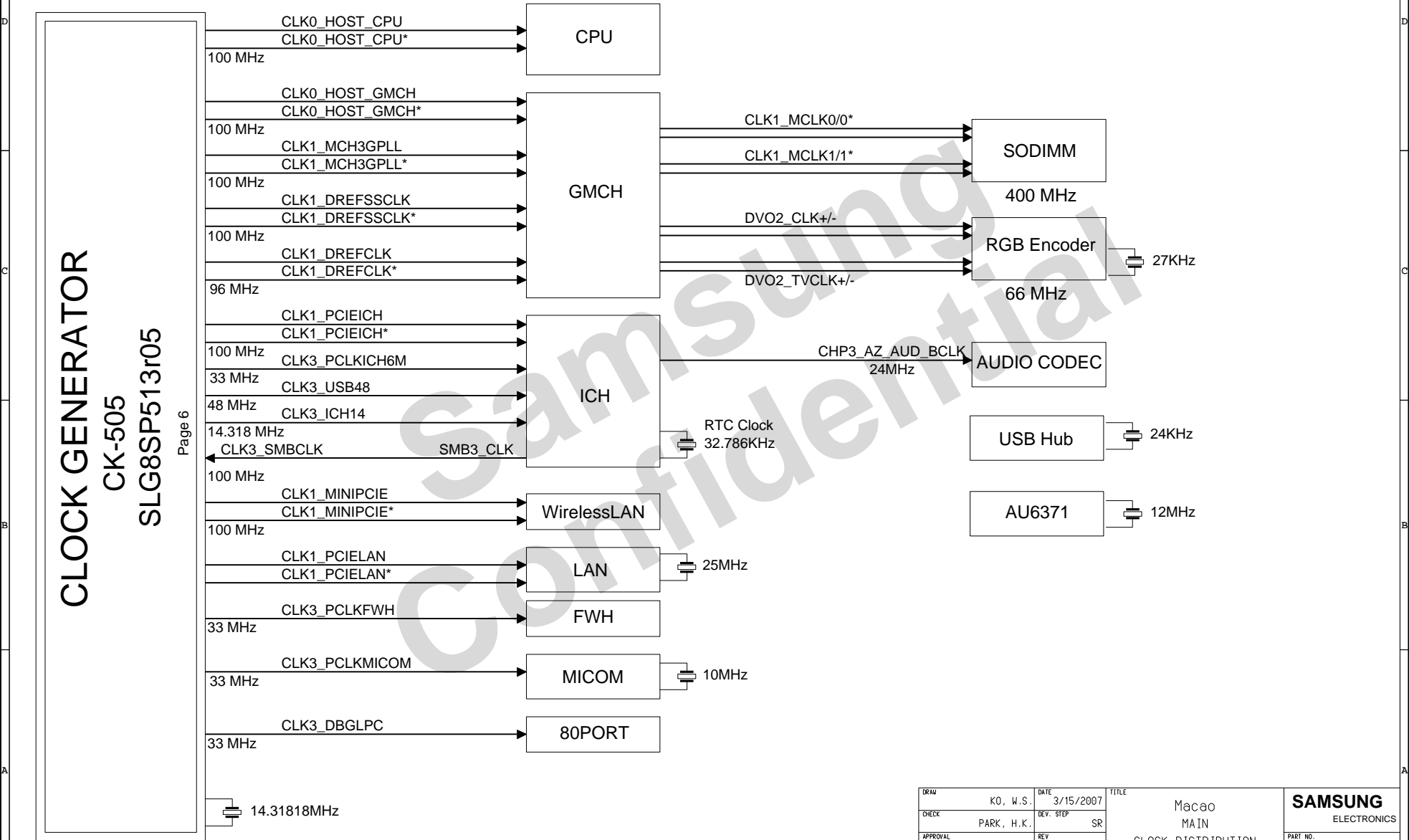
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Power Sequence Block Diagram



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CLOCK DISTRIBUTION



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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Wired LAN	AD21	3	G
USB Hub to PCI LPC Bridge/IDE/AC97/SMBUS	AD29(internal) AD30(internal) AD31(internal)	Programable	

I²C / SMB Address

Devices	Address	Hex	Bus
ICH6M	Master	-	SMBUS Master
CK-510M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
SODIMMO	1010 000X	A0h	-
USB Hub	1010 000X	A0h	-
MICOM	Master		
BATTERY	0001 011h	16h	
THERMAL MORNITOR	x111 1010	7Ah	
HALL MOUSE	x001 1100	1Ch	

USB PORT Assign

Port0	Right USB JACK
Port1	Left USB JACK
Port2	Touch Sensor Panel
Port3	SD/MMC Controller
Port4	Bluetooth
Port5	DMB
Port6	FingerPrint
Port7	USB Hub
	- 1. USIM Controller
	2. Camera
	3. Wibro / HSDPA

System Power States

Power Rail	Devices (Page Number)
P5V	FAN(10) 80PORT(20) MICOM(25) DMB(25) RGB_ENCODER(21) AUDIO AMP(32)
P3.3V	CLOCK(6) Thermal sensor(10) SODIMM(15) ICH7(17) 80PORT(20) HDD(24)WIBRO/HSDPA(29)SD/MMC(27) MICOM(26) DMB(25) I2CtoPS2(24)GMCH(11)Wireless_LAN(28)
P1.5V	CPU(7) GMCH(11) ICH7(16) WIBRO/HSDPA(29)SC1485(37)
P2.5V	GMCH(11)ICH7(16)RGB_ENCODER(21)
P5V_AUX	ICH7(16) USB0(25)USB1(45)MAX8734(36)
P3.3V_AUX	ICH7(16)Wired_LAN(30) WIBRO/HSDPA(29)MAX8734(36)
P1.8V_AUX	GMCH(11) SODIMM(15) SC486(35)
VCCP_CORE	CPU(7) GMCH(11) ICH7(16) SC1485(37)
VCC_CORE	CPU(7)SC451(39)

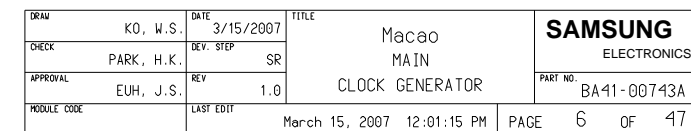
Voltage Rails

Power Rail	Descriptions
PRTC_BAT VDC	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well. Primary DC system power supply (6 to 19V)
P5V_AUX P3.3V_AUX P1.8V_AUX	5.0V power rail (off in S4-S5) 3.3V power rail (off in S4-S5) GMCH/DDR II Power Source(off in S4-S5)
P5V P3.3V P1.5V P2.5V VCCP_CORE CPU_CORE	5.0V switched power rail (off in S3-S5) 3.3V switched power rail (off in S3-S5) 1.5V switched power rail (off in S3-S5) 2.5V LDO power rail (off in S3-S5) 1.05V power rail, GMCH core, CPU/GMCH FSB Termination. Core voltage for Stealey CPU (0.74~1.30V)
P3.3V_MICOM P1.5V_DMI	3.3V always on power rail for MICOM 1.5V (Direct Media Interface Compensation)
LCD_VDD3V VCC_CRT	3.3V (LCD) 5V (CRT)
P4.75_AUD P5.0V_AMP	4.75V (ALC262) 5V (Audio AMP)

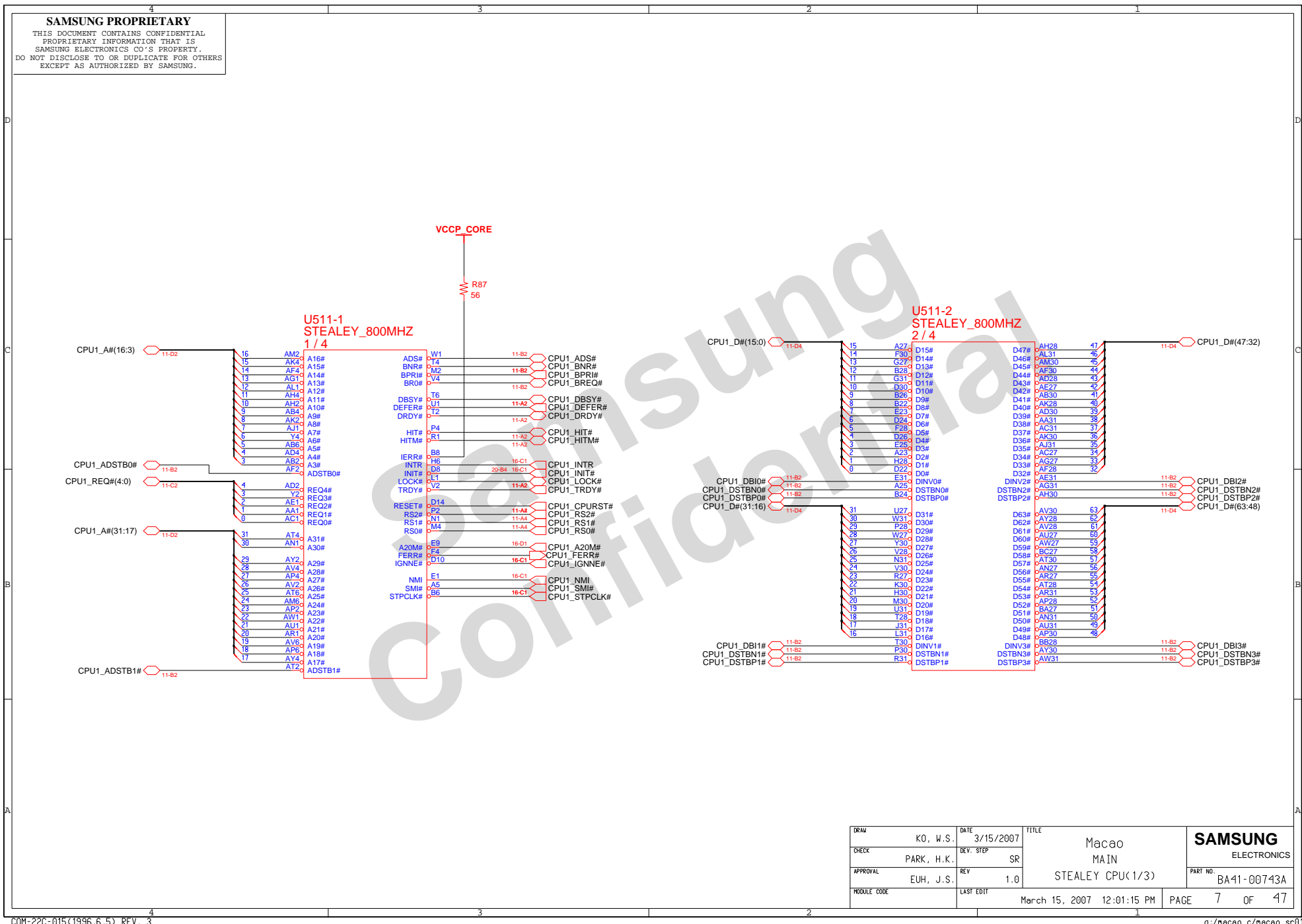
CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V	
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V	
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V	
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V	
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V	
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V	
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V	
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V	
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V	
0	0	1	0	0	1	1.564 V	1	0	1	0	1	0	1.052 V	
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V	
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V	
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V	
0	0	1	1	0	1	1.500 V	1	0	1	1	1	0	0.988 V	
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V	
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V	
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V	DOTHAN-ULV Base Stealey HIGH FREQUENCY MODE
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V	
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V	
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V	
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V	
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V	
0	1	0	1	1	0	1.356 V	1	1	0	1	1	0	0.844 V	
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V	
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V	DOTHAN-ULV Base Stealey LOW FREQUENCY MODE
0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V	
0	1	1	0	1	0	1.292 V	1	1	1	1	0	0	0.780 V	
0	1	1	0	1	1	1.276 V	1	1	1	1	1	0	0.764 V	
0	1	1	1	0	0	1.260 V	1	1	1	1	1	0	0.748 V	
0	1	1	1	0	1	1.244 V	1	1	1	1	1	0	0.732 V	
0	1	1	1	1	0	1.228 V	1	1	1	1	1	1	0.716 V	DOTHAN-ULV Base Stealey DEEPER SLEEP MODE
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V	Refer to page??

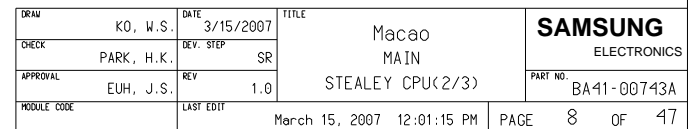
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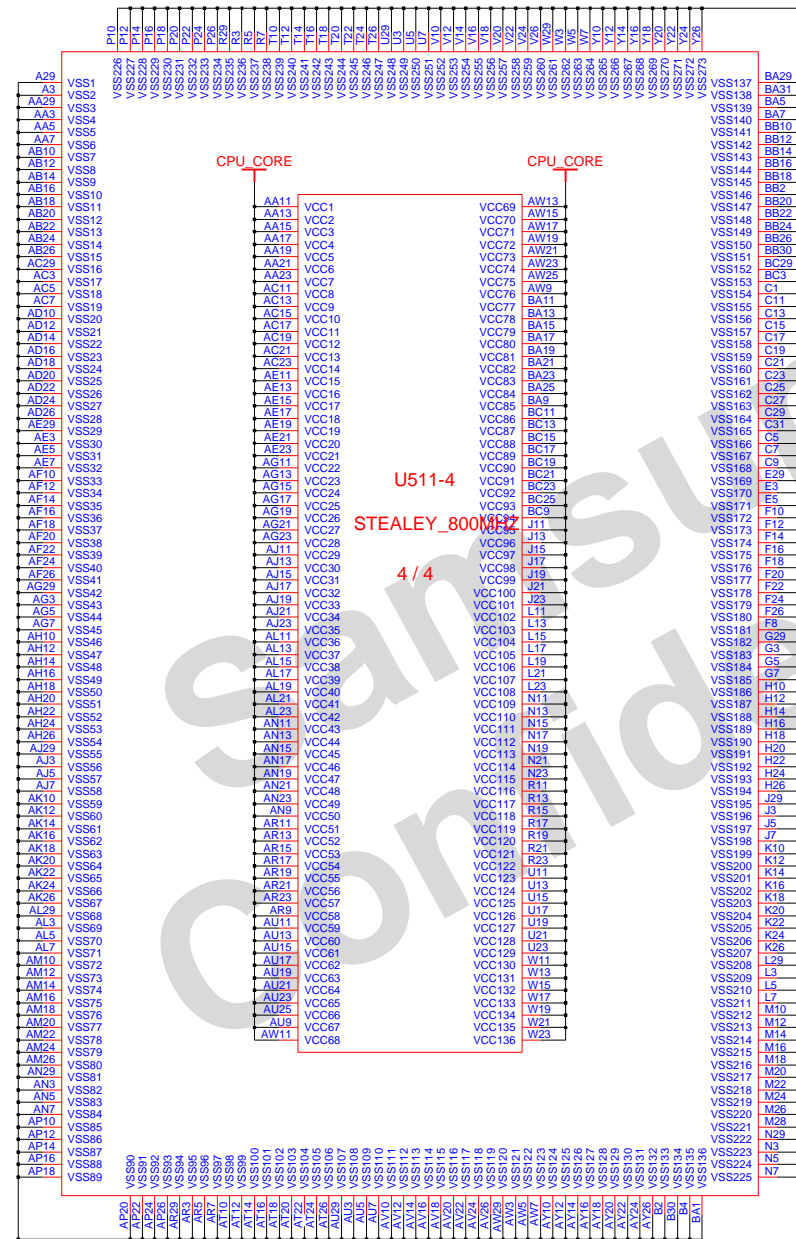


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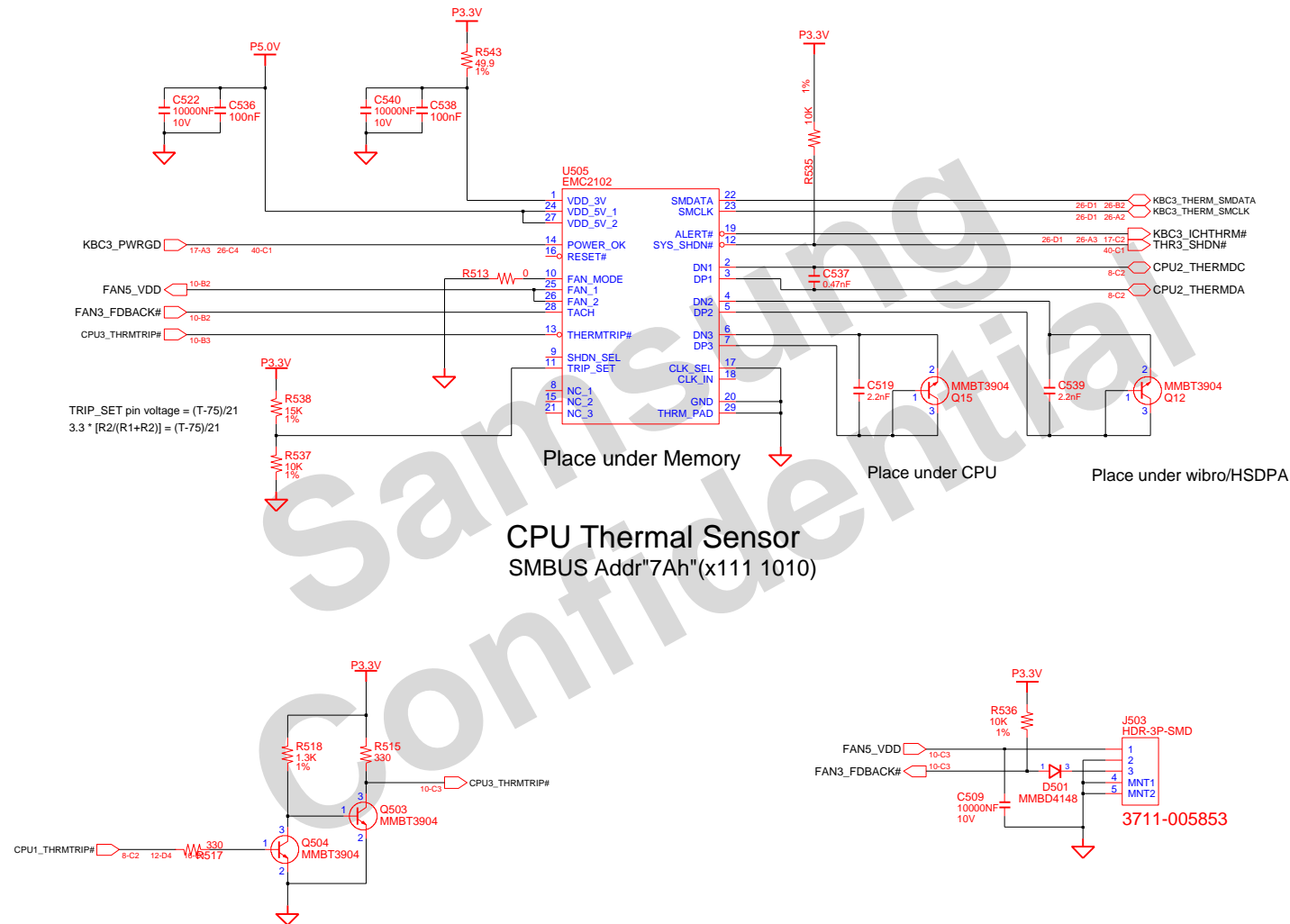
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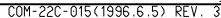
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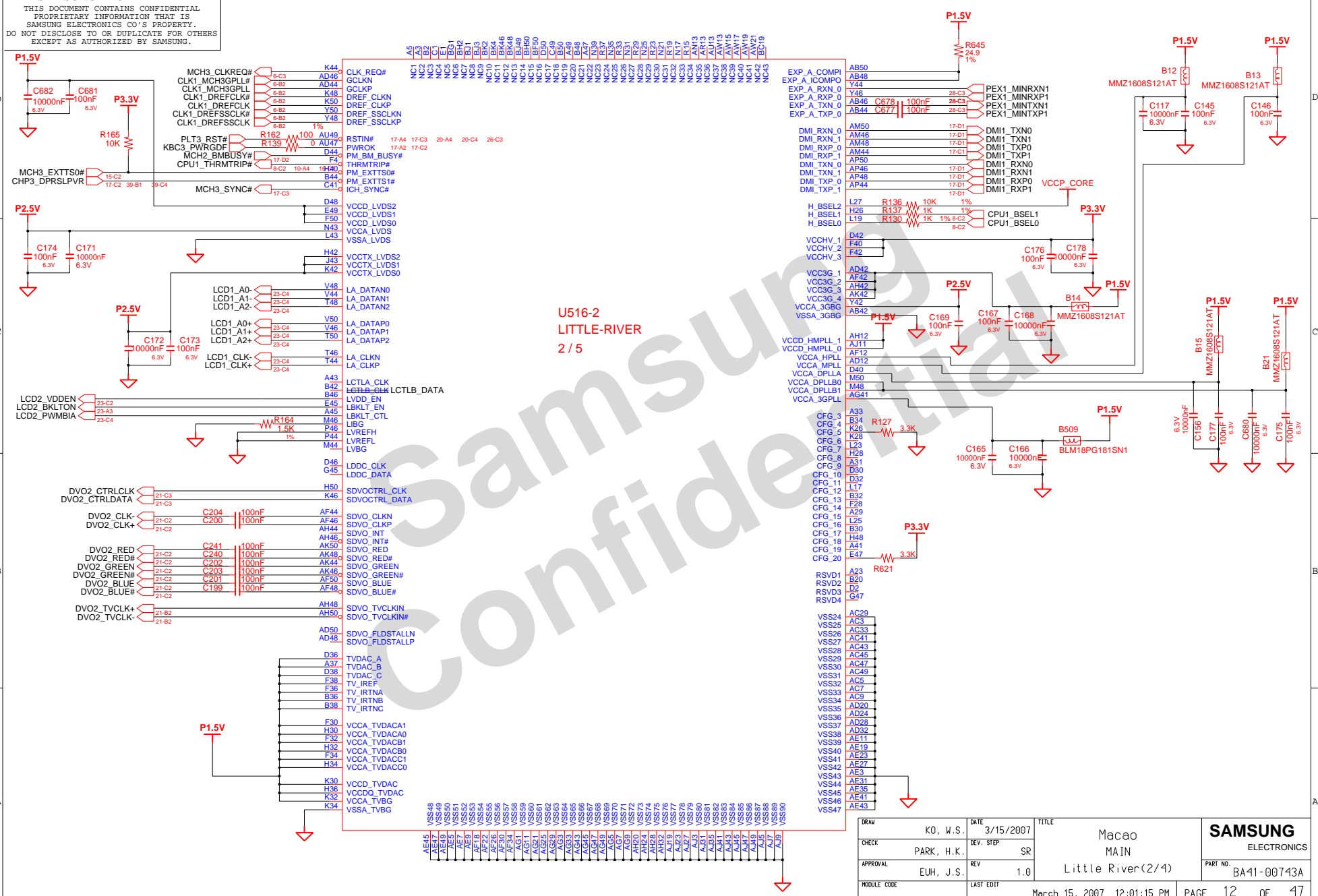
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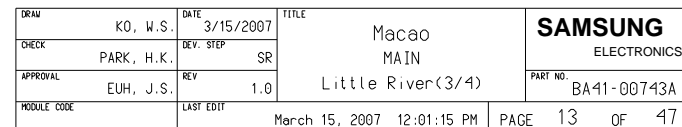


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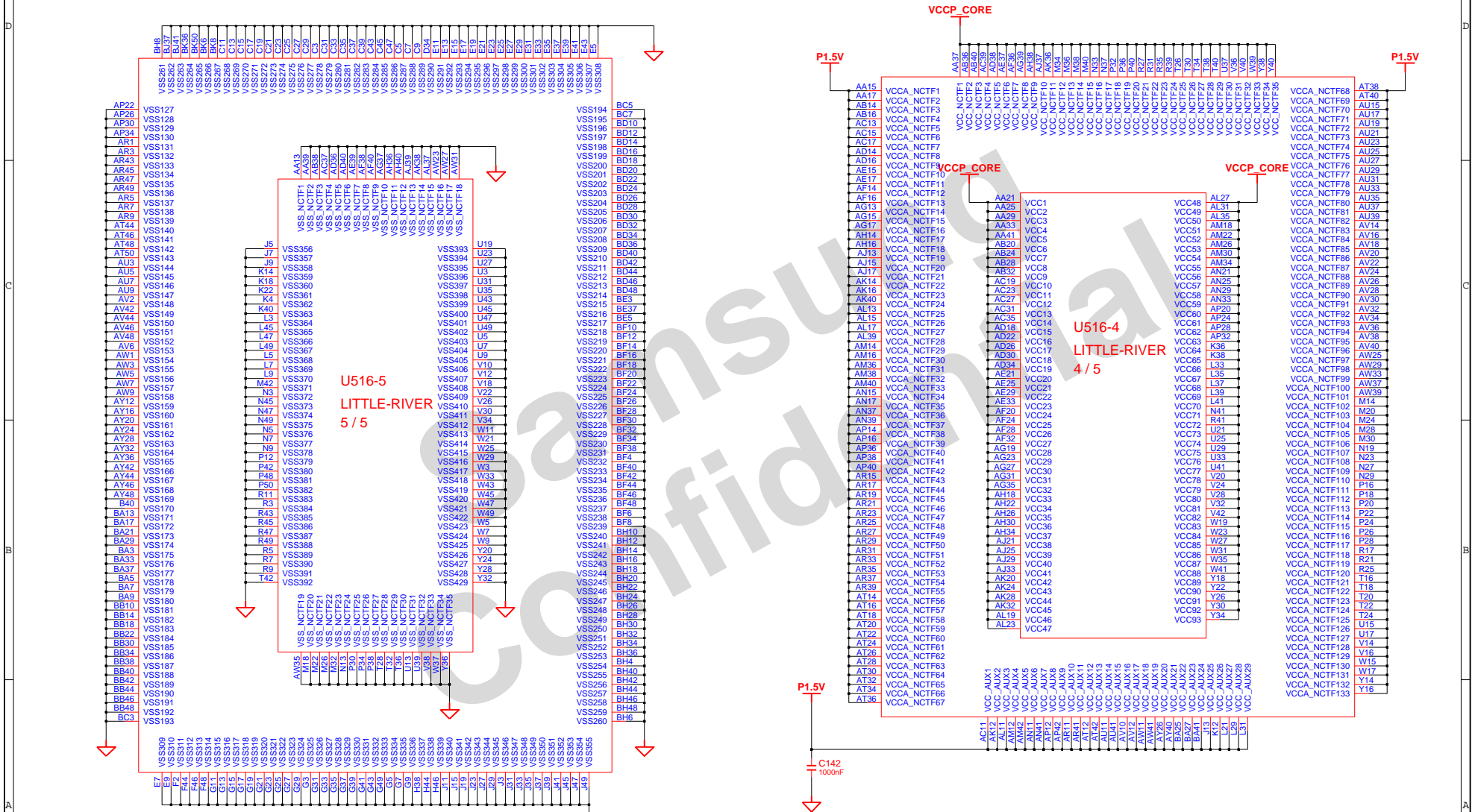
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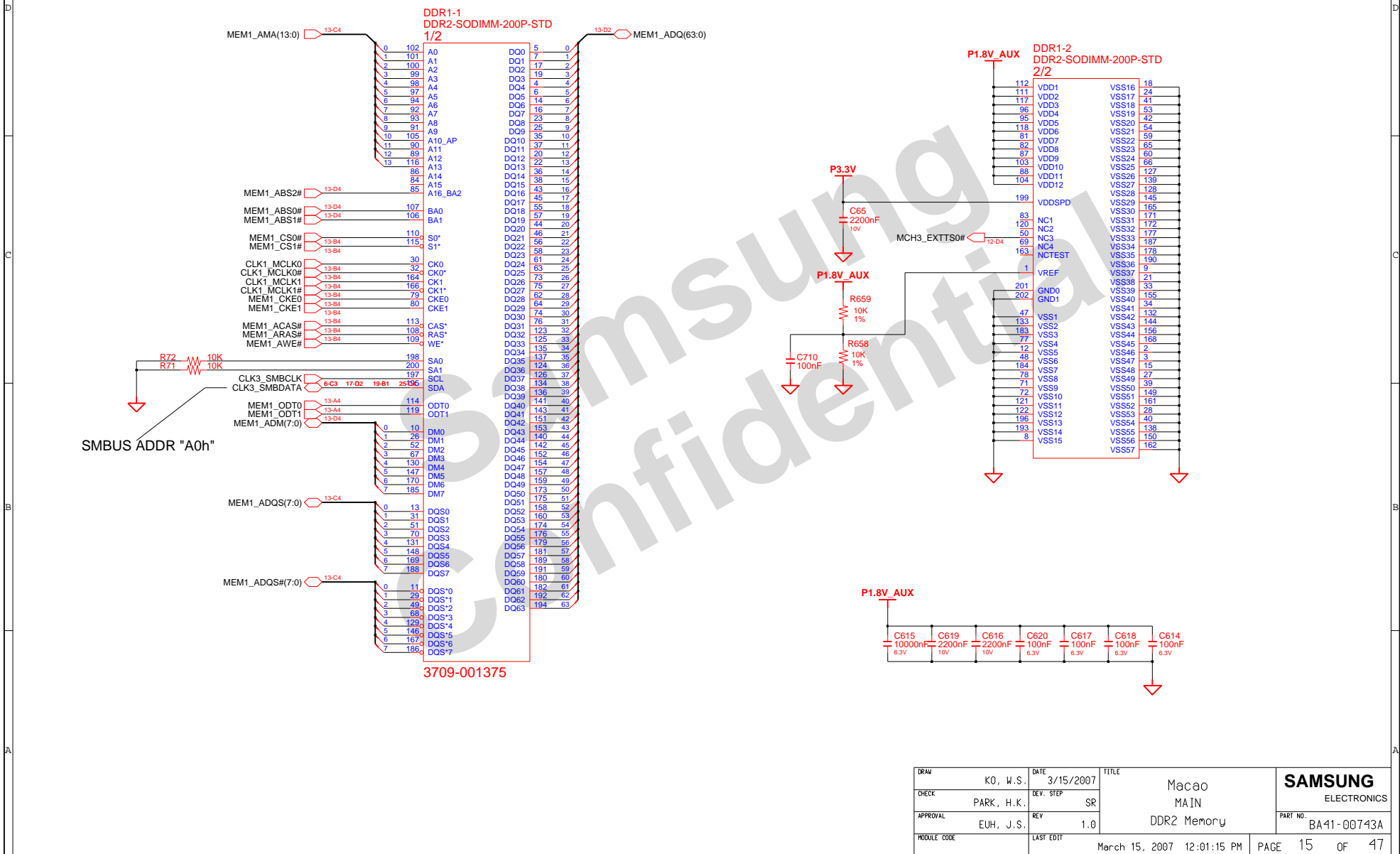


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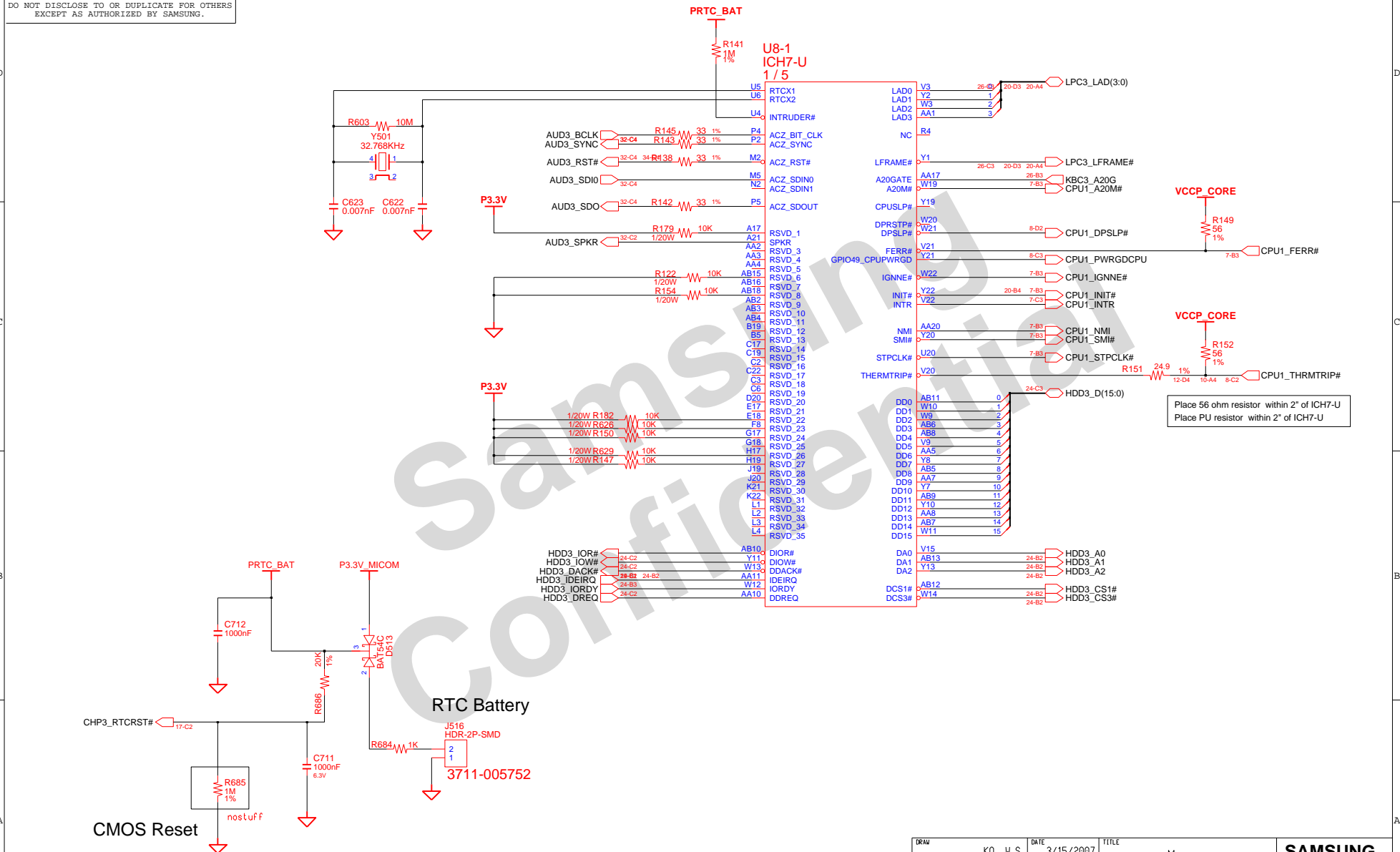


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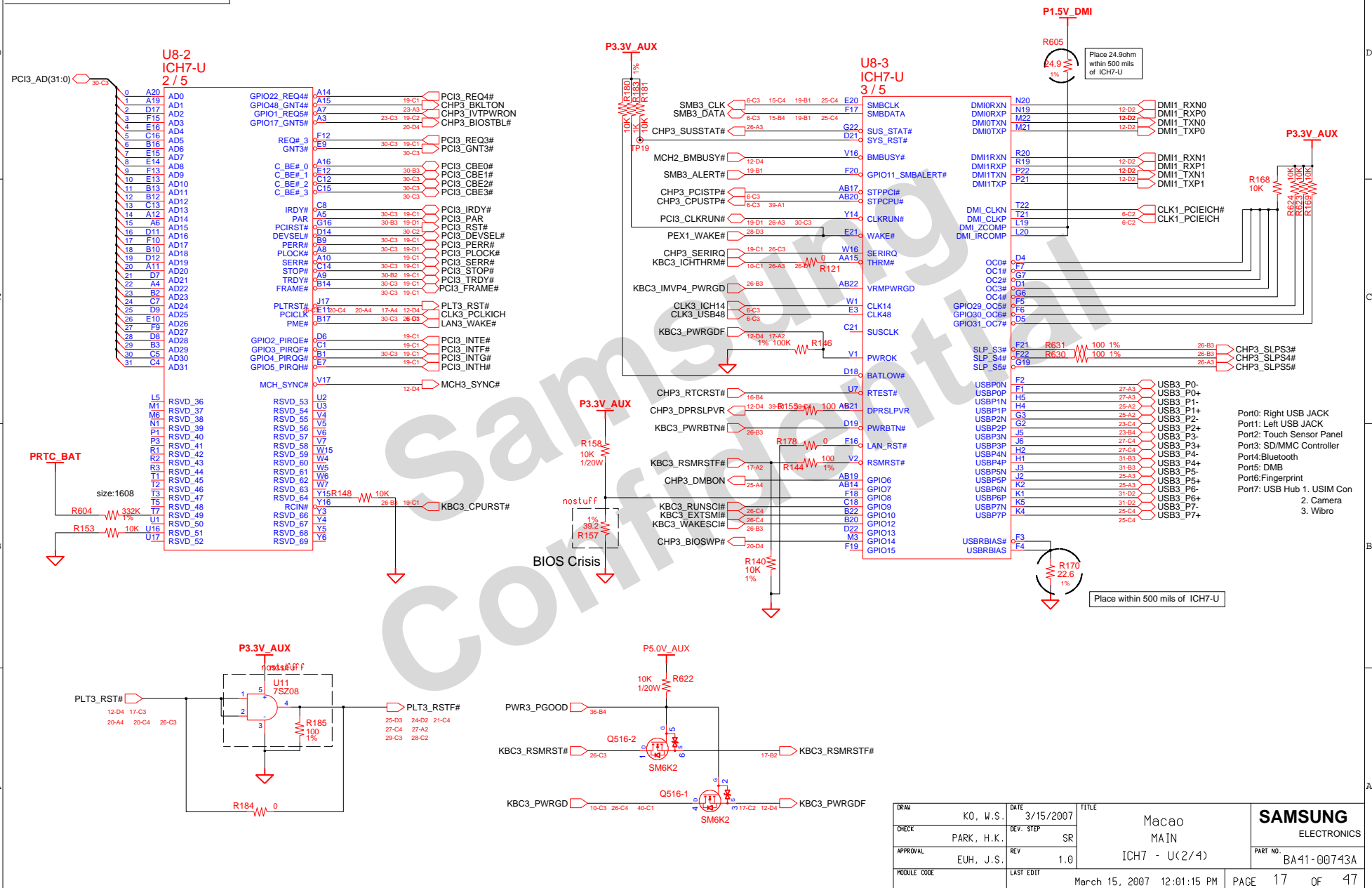
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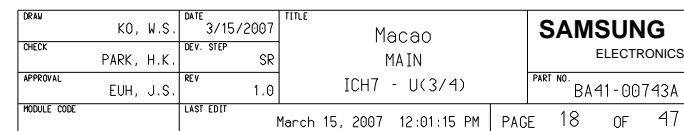


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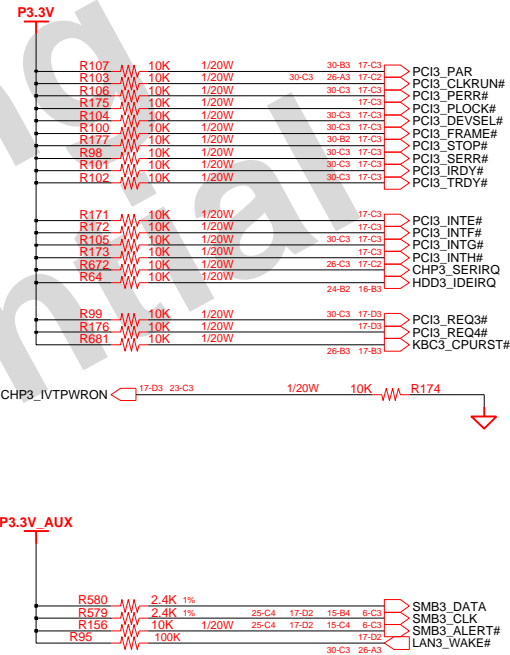
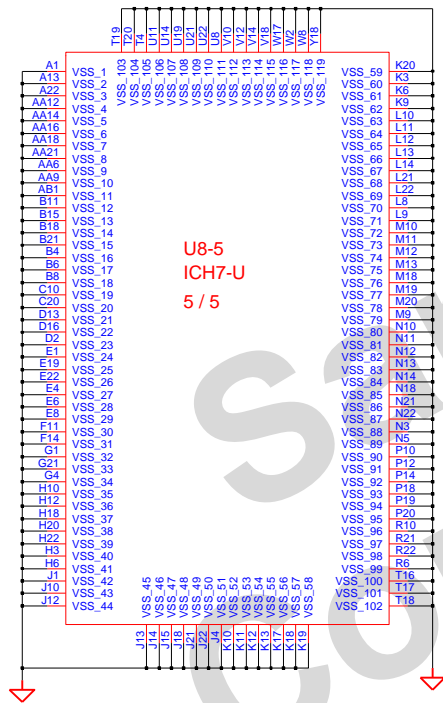
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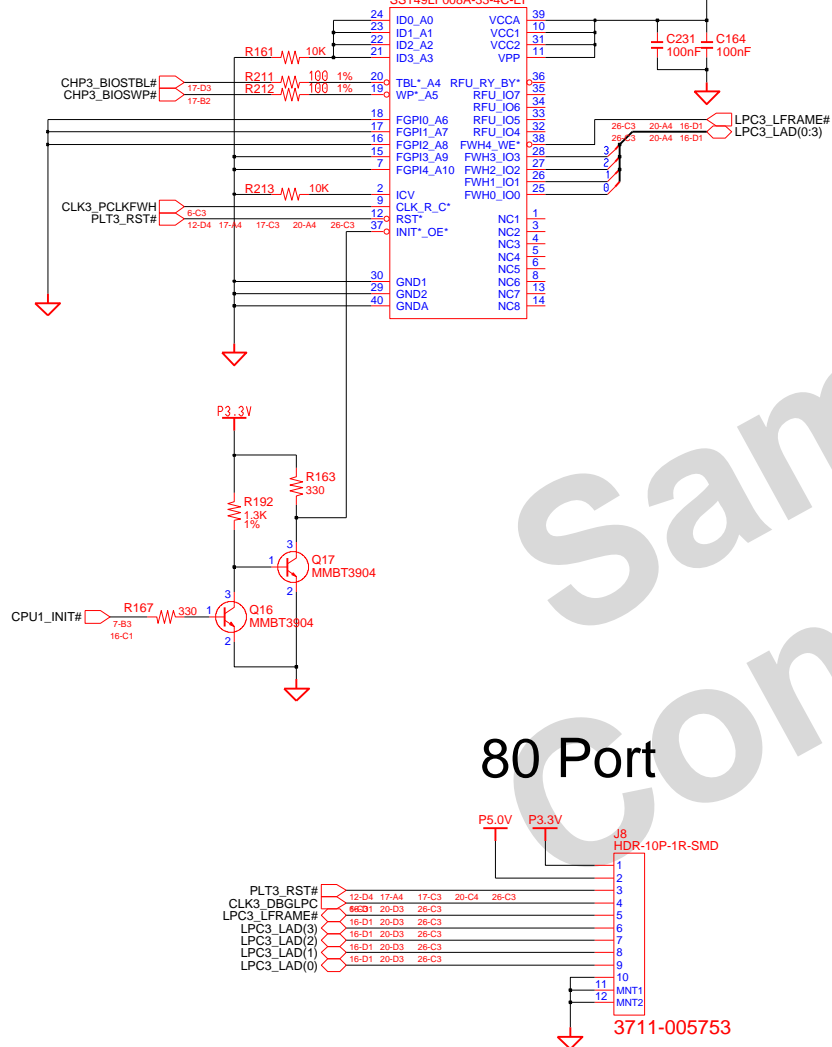
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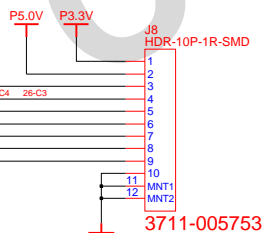
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VENDOR: SST, ATMEL

U14 SST49LF008A-33-4C-EI



80 Port



02 VERIFY REAL MODE
 03 DISABLE NMI
 04 GET CPU TYPE
 06 INIT. SYSTEM H/W
 08 INIT. CHIPSET REG.
 09 SET IN POST FLAG
 0A INIT CPU.REG
 0B CPU CACHE ON
 0C INIT.CACHE TO POST
 0E INIT. I/O VALUE
 0F ENABLE THE L-BUS IDE
 10 INIT. POWER MANAGER
 11 LOAD ALTERNATE REG.
 13 PCI BUS MASTER RESET
 WITH INITIAL POST VALUE
 14 INIT. KEYBOARD CONTROLLER
 16 CHECK CHECKSUM
 18 8254 TIMER INIT.
 1A 8237 DMA CONTROLLER INIT.
 1C RESET INTERRUPT CONTROLLER
 20 TEST DRAM REFRESH
 22 TEST 8742 KEYBOARD CONTROLLER
 24 SET ES SEGMENT REG. TO 4GB
 26 ENABLE A20
 28 AUTO SIZING DRAM
 32 COMPUTE THE CPU SPEED
 34 TESET CMOS RAM
 38 SHADOW SYSTEM BIOS ROM
 3A AUTO SIZING CACHE
 3C CONFIGURE ADVANCED CHIPSET REG.
 3D LOAD ALTER REG. WITH CMOS VALUE
 42 INIT. INTERRUPT VECTOR
 44 INIT. BIOS INTERRUPT
 46 CHECK ROM COPYRIGHT NOTICE
 47 INIT. I20 SUPPORT IF INSTALLED
 48 CHECK VIDEO CONFIGURE AGAINST CMOS
 49 INIT. PCI BUS AND DEVICE
 4A INIT. ALL VIDEO BIOS ROM
 4C SHADOW VIDEO BIOS ROM
 50 DISPLAY CPU TYPE AND SPEED
 52 TEST KEYBOARD
 54 SET KEYCLICK IF ENABLED
 56 ENABLE KEYBOARD
 58 TEST FOR UNEXPECTED INTERRUPTS
 5A DISPLAY " PRESS SETUP"
 5C TEST RAM BETWEEN 512K AND 640K
 60 TEST EXTENDED MEMORY
 62 TEST EXTENDED MEMORY ADDRESS LINE
 64 JUMP TO USER PATCH 1

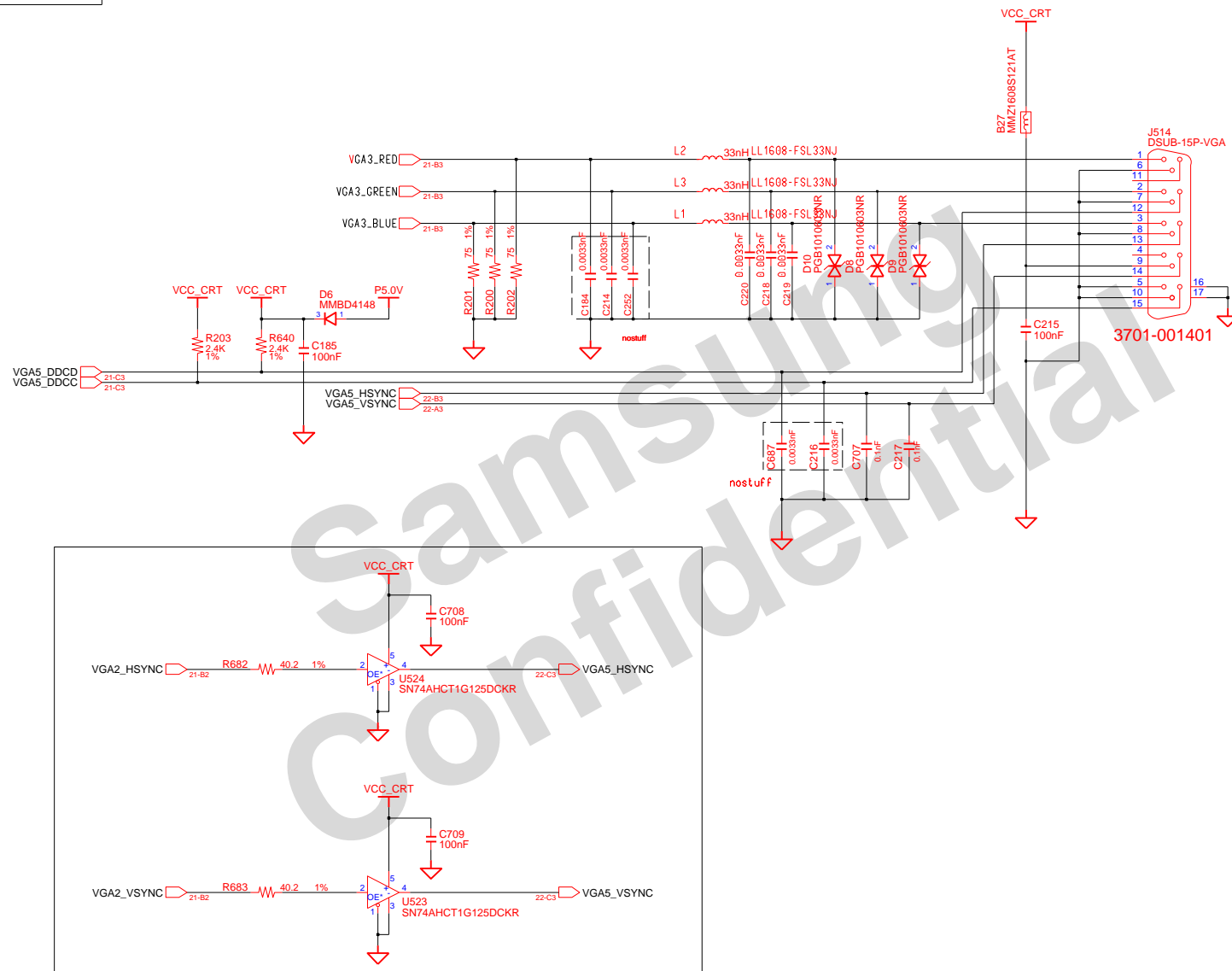
66 CONFIGURE ADVANCE CACHE REG.
 6A DISPLAY EXTERNAL CACHE SIZE
 6C DISPLAY SHADOW MESSAGE
 6E DISPLAY NON-DISPOSABLE SEGMENT
 70 DISPLAY ERROR MESSAGE
 72 CHECK FOR CONFIGURATION ERROR
 74 TEST REAL-TIME CLOCK
 76 CHECK FOR KEYBOARD ERROR
 7C SETUP HARDWARE INTERRUPT VECTOR
 7E TEST COPROCESSER IF PRESENT
 80 DISABLE ON-BOARD I/O PORT
 82 DETECT AND INSTALL EXT.RS232C
 84 DETECT AND INSTALL EXT.PARALLEL
 86 RE-INIT. ON-BOARD I/O PORT
 88 INIT. BIOS DATA ROM
 8A INIT.EXTENDED BIOS DATA AREA
 8C INIT. FDD CONTROLLER
 9A SHADOW OPTION ROMS
 9C SETUP POWER MANAGEMENT
 9E ENABLE H/W INTERRUPT
 A0 SET TIME OF DAY
 A4 INIT. TYPOMATIC RATE
 A8 ERASE F2 PROMPT
 AA SCAN FOR F2 KEY STROKE
 AC ENTER SETUP
 AE CLEAR IN POST FLAG
 B0 CHECK FOR ERRORS
 B2 POST DONE-PREPARE TO BOOT O/S
 B4 ONE BEEP
 B6 CHECK PASSWORD (OPTION)
 B7 ACPI INIT
 BA DMI INIT
 BE CLEAR SCREEN
 C0 TRY BOOT WITH INT19
 D0 INTERRUPT HANDLER ERROR
 D2 UNKNOWN INTERRUPT ERROR
 D4 PENDING INTERRUPT ERROR
 D6 SHUTDOWN 5
 D8 SHUTDOWN ERROR
 DA EXTENDED BLOCK MOVE
 DC SHUTDOWN 10
 89 ENABLE NMI
 90 INIT. HDD CONTROLLER
 91 INIT. LOCAL BUS HDD CONTROLLER
 92 JUMP TO USER PATCH 2
 94 DISABLE A20 ADDRESS LINE
 96 CLEAR HUGE ES SEGMENT REG.
 98 SEARCH FOR OPTION ROMS

DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG
CHECK	PARK, H.K.	DEV. STEP	SR		MAIN	ELECTRONICS
APPROVAL	EUH, J.S.	REV	1.0		FWH & 80port	PART NO. BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	20	OF 47

COM-22C-015(1996.6.5) REV. 3

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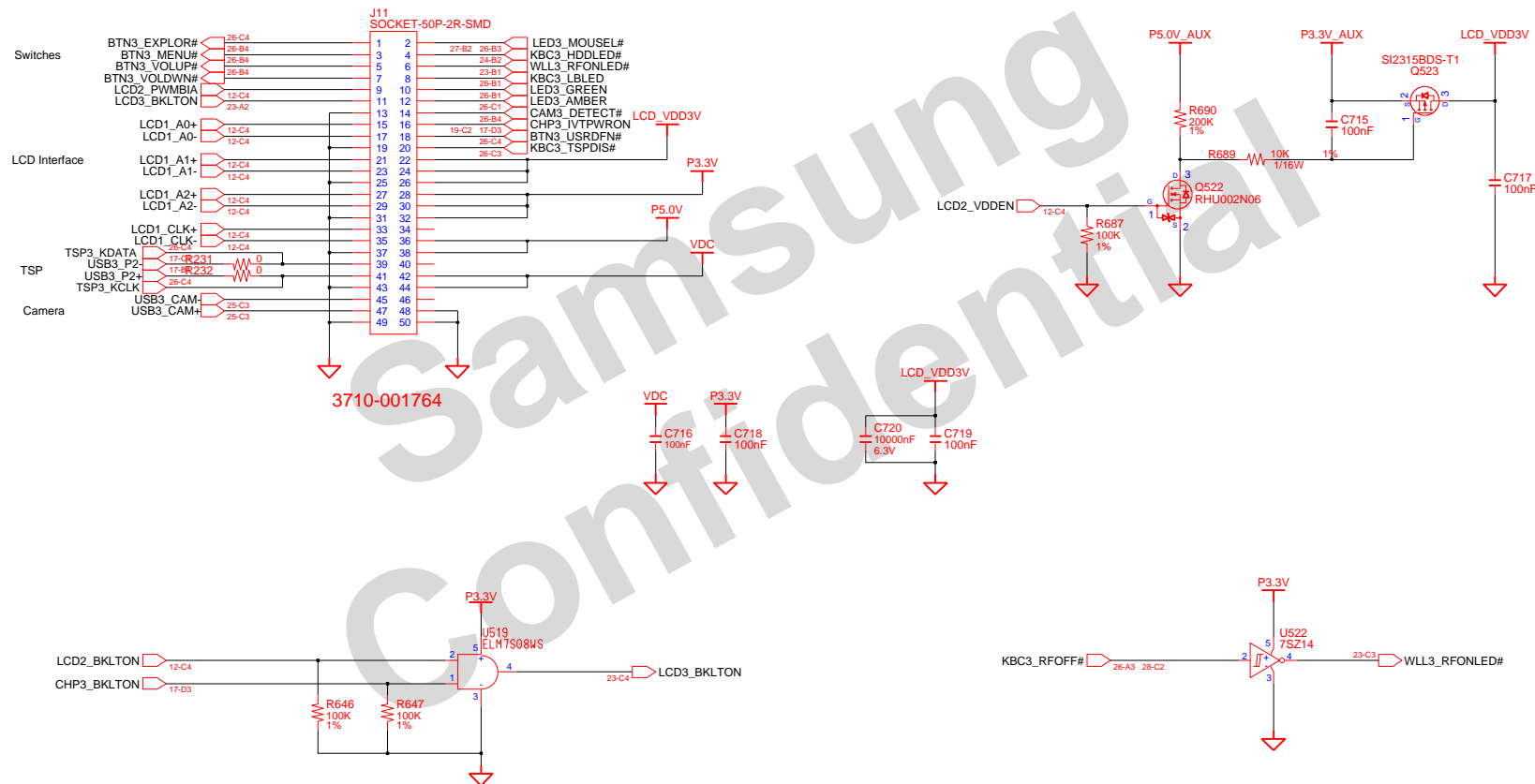
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DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao MAIN VGA Conn(CRT)	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR			PART NO. BA41-00743A
APPROVAL	EUH, J.S.	REV	1.0			
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	22	OF 47

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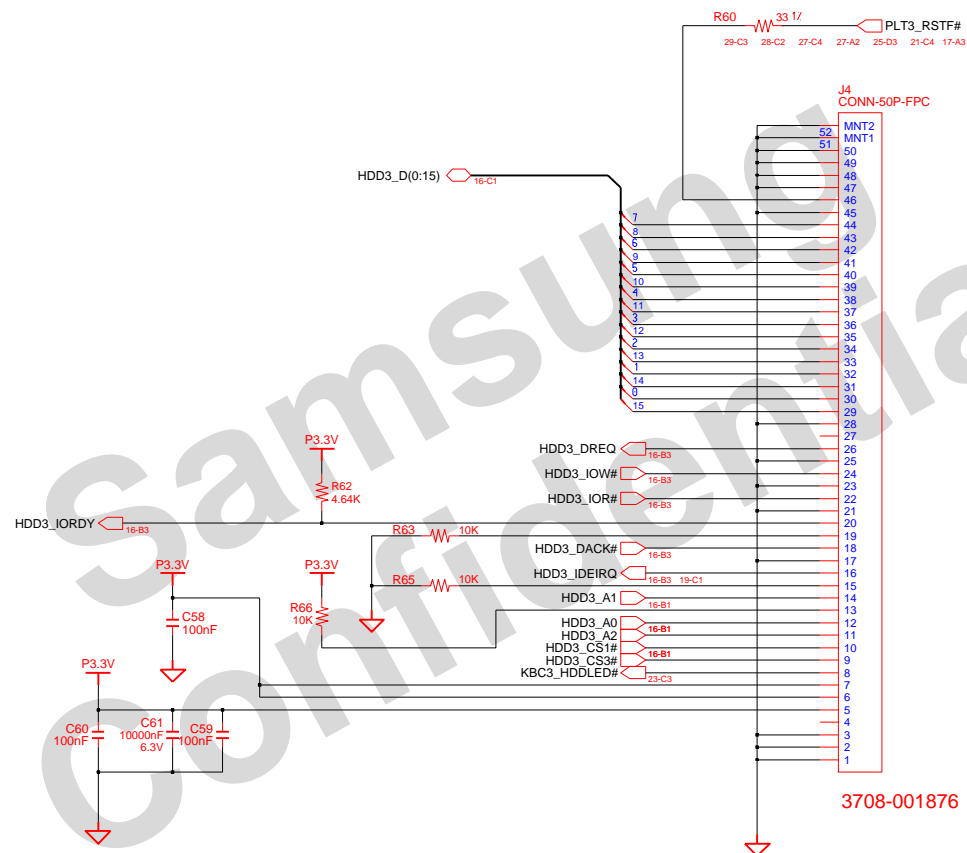
TCON Sub B'd



DRAW	K0, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	1.0	TCON Sub Conn	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	23	OF 47

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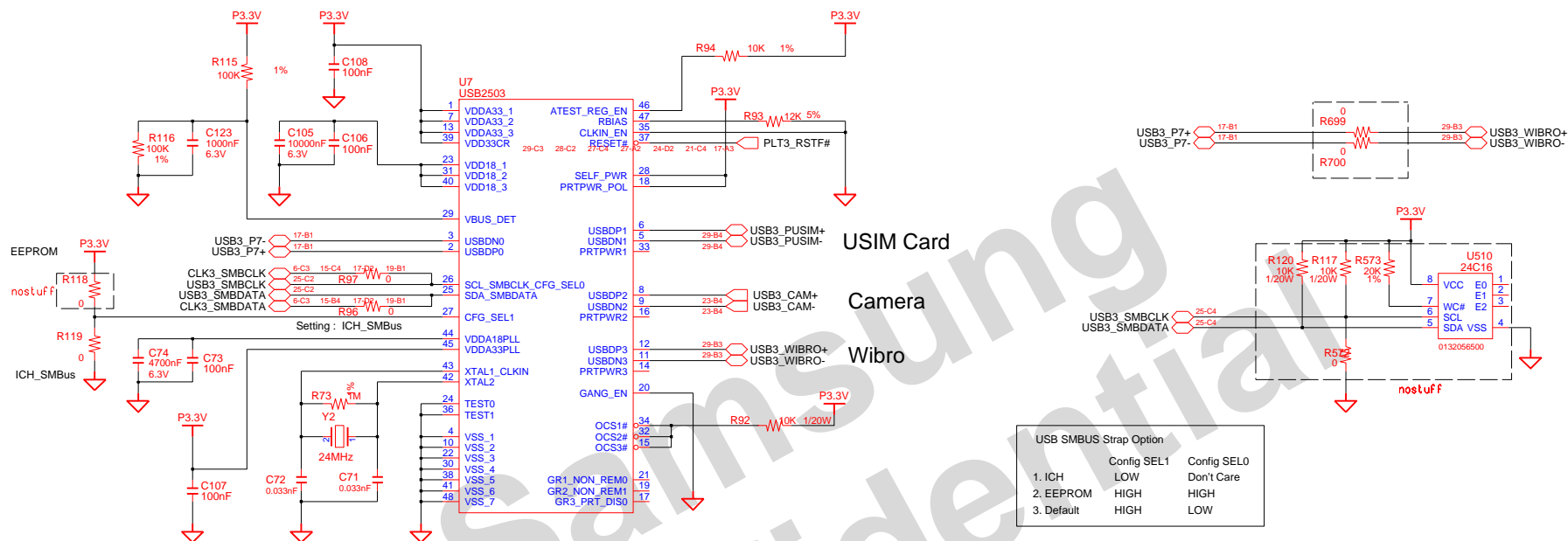
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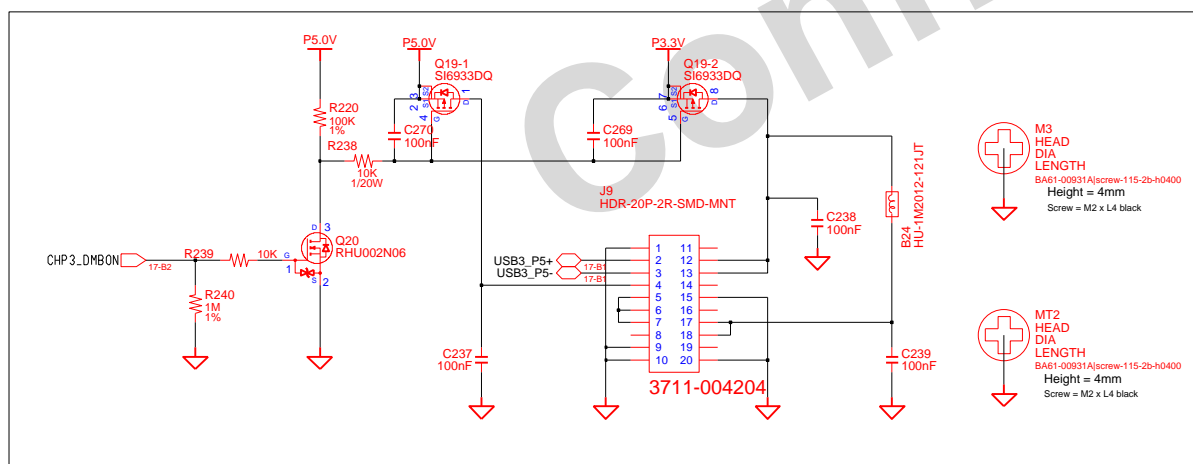
DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR		MAIN	
APPROVAL	EUH, J.S.	REV	1.0		HDD CONNECTOR	
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	24 OF 47	

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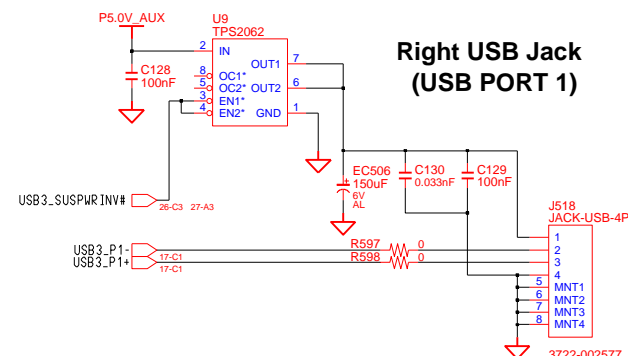
USB Hub 4 ports + EEPROM




DMB Connector & Pem(4mm Height)

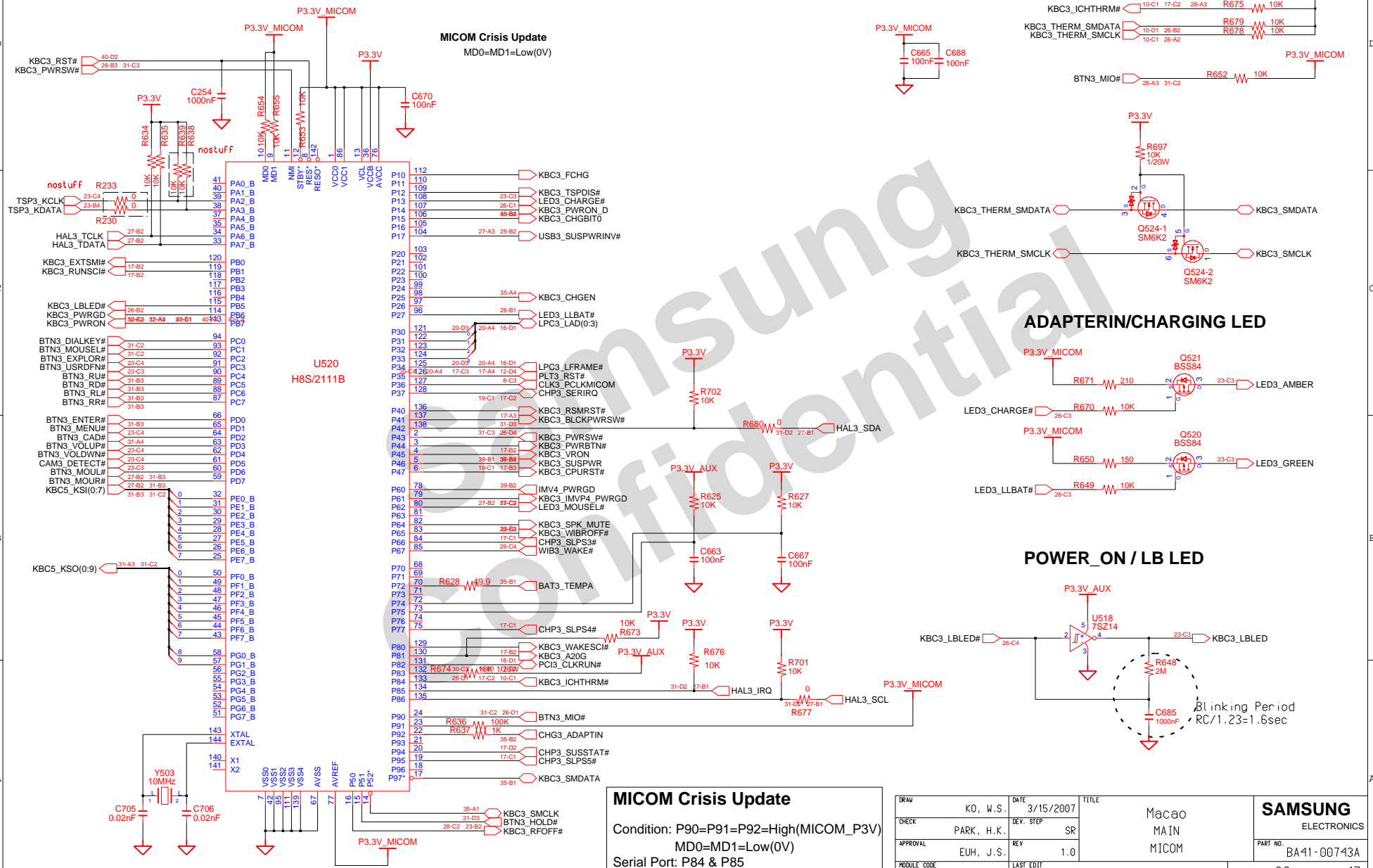


**Right USB Jack
(USB PORT 1)**



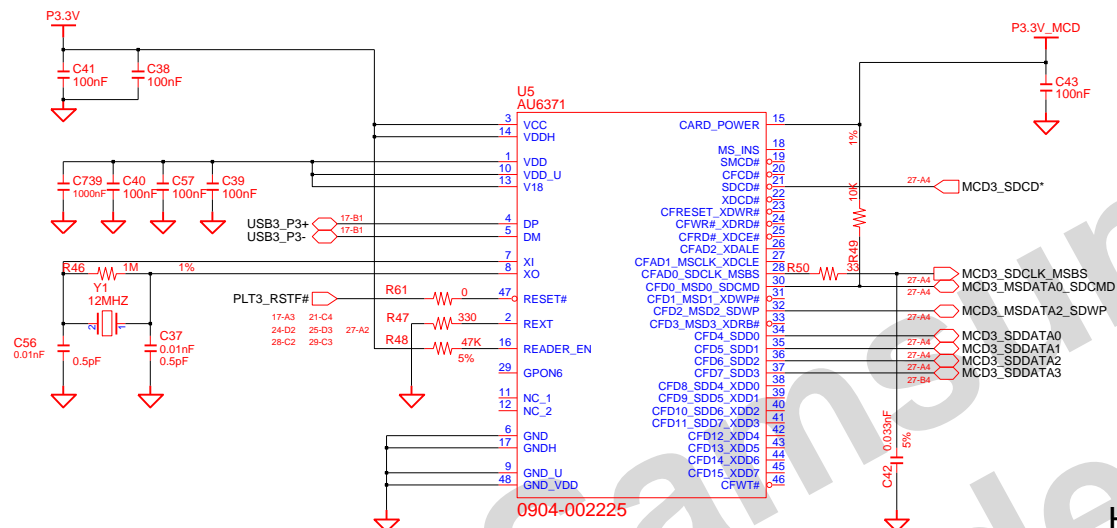
DRAM	K0, W.S.	DATE	3/15/2007	TITLE Macao MAIN USB & DMB	
CHECK	PARK, H.K.	DEV. STEP	SR		
APPROVAL	EUH, J.S.	REV	1.0		
MODULE CODE	LAST EDIT		March 15, 2007 12:01:15 PM		

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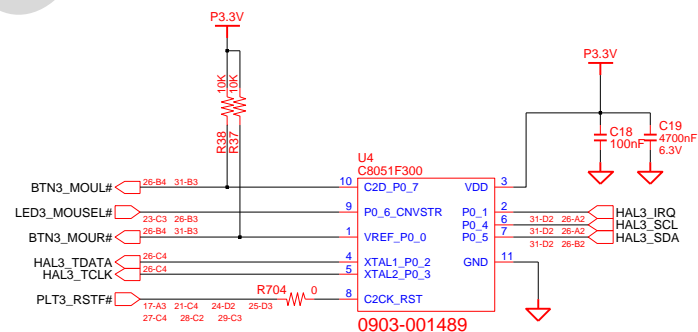
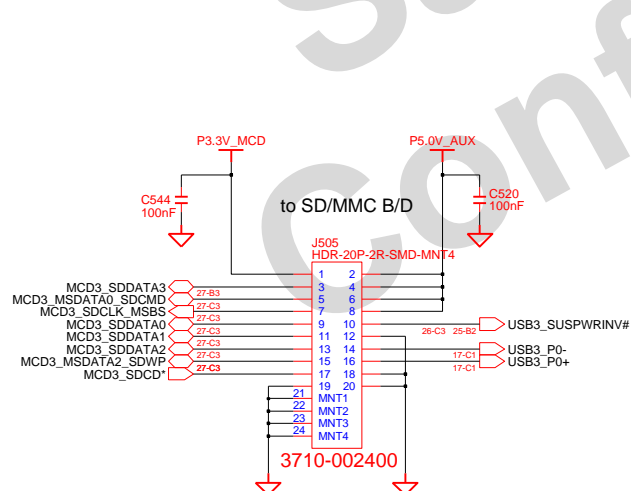


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Hall Mouse IC (I2C to PS2 Conversion IC)



DRAW	K0, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR		MAIN	
APPROVAL	EUH, J.S.	REV	1.0		SD/MMC Controller	
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM		PAGE 27 OF 47	

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Host Board Connections:

- P3.3V
- P1.5V
- P3.3V_AUX

Card Pin Connections:

- MPE3_CLKREQ# (6-C2)
- CLK1_MINIPCI#1 (6-C2)
- CLK1_MINIPCI#1 (6-C2)
- PEX1_MINRXN1 (12-D2)
- PEX1_MINRXP1 (12-D2)
- PEX1_MINTXN1 (12-D2)
- PEX1_MINTXP1 (12-D2)

Card Labels:

- 3709-001401
- 4mm Height

Mini PCI Express Card Dimensions:

- Width: 30.00 mm
- Height: 50.95 mm
- Pin 1 location: 50.95 mm from bottom edge

Card Orientation:

- Top
- Pin 1

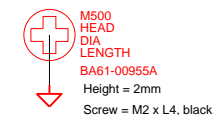
Card Pinout:

- 1: WAKE*
- 2: RSVD_1
- 3: RSVD_2
- 4: CLKREQ*
- 5: GND_2
- 6: REFCLK-
- 7: REFCLK+
- 8: GND_3
- 9: SIM_RSVD_C8
- 10: SIM_RSVD_C4
- 11: GND_5
- 12: PERNO
- 13: PERP0
- 14: GND_7
- 15: GND_8
- 16: PETN0
- 17: PETP0
- 18: GND_10
- 19: RSVD_11
- 20: RSVD_12
- 21: RSVD_13
- 22: RSVD_14
- 23: RSVD_15
- 24: RSVD_16
- 25: RSVD_17
- 26: RSVD_18
- 27: GND_11
- 28: LED_WWAN*
- 29: LED_WLAN*
- 30: LED_WPAN*
- 31: P1.5V_3
- 32: GND_12
- 33: P3.3V_2
- 34: MNT1
- 35: MNT2

Host Board Components:

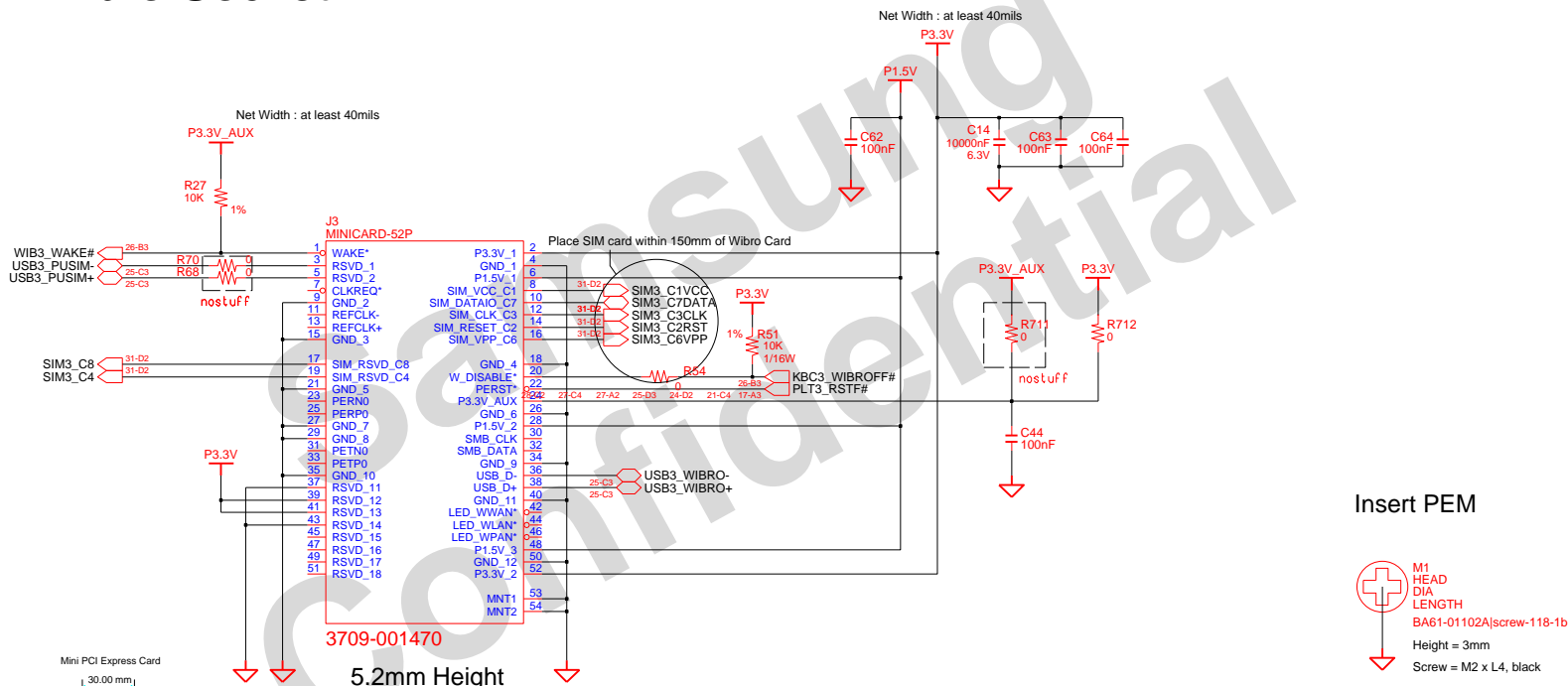
- R219: 10K 1/20W
- R691: 0-1
- R692: 0-1
- R693: 0-1
- R694: 0-1
- R695: 0-1
- R696: 0-1
- R697: 0-1
- R698: 0-1
- R699: 0-1
- R700: 100nF
- R701: 100nF
- R702: 100nF
- R703: 100nF
- R704: 100nF
- R705: 100nF
- R706: 100nF
- R707: 100nF
- R708: 100nF
- R709: 100nF
- R710: 100nF
- R711: 100nF
- R712: 100nF
- R713: 100nF
- R714: 100nF
- R715: 100nF
- R716: 100nF
- R717: 100nF
- R718: 100nF
- R719: 100nF
- R720: 100nF
- R721: 100nF
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- R739: 100nF
- R740: 100nF
- R741: 100nF
- R742: 100nF
- R743: 100nF
- R744: 100nF
- R745: 100nF
- R746: 100nF
- R747: 100nF
- R748: 100nF
- R749: 100nF
- R750: 100nF
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- R879: 100nF
- R880: 100nF
- R881: 100nF
- R882: 100nF
- R883: 100n

Insert PEM



DRAM	K0, W.S.	DATE	3/15/2007	TITLE Macao MAIN WirelessLAN	SAMSUNG ELECTRONICS PART NO. BA41-00743A
CHECK	PARK, H.K.	DEV. STEP	SR		
APPROVAL	EUH, J.S.	REV	1.0		
MODULE CODE	LAST EDIT		March 15, 2007 12:01:15 PM		

Wibro Socket



Mini Card (Socket Only)

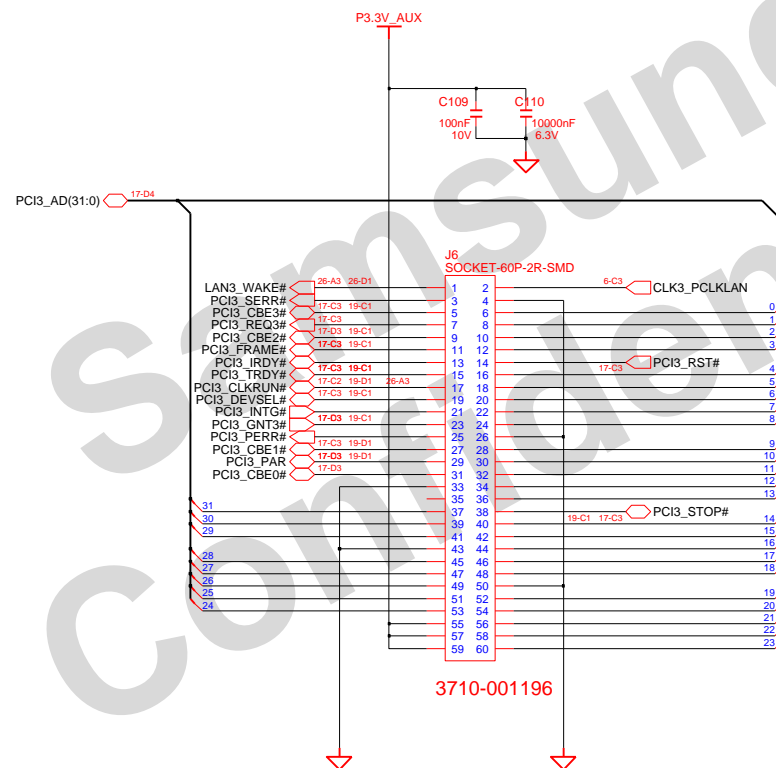
PCI Express Mini Card ElectroMechanical Spec. 1.0

DRAW	K.O. W.S.	DATE	3/15/2007	TITLE	Macao MAIN Wibro/HSDPA	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR			
APPROVAL	EUH, J.S.	REV	1.0			
MODULE CODE	LAST EDIT		March 15, 2007 12:01:15 PM			
				PART NO.	BA41-00743A	

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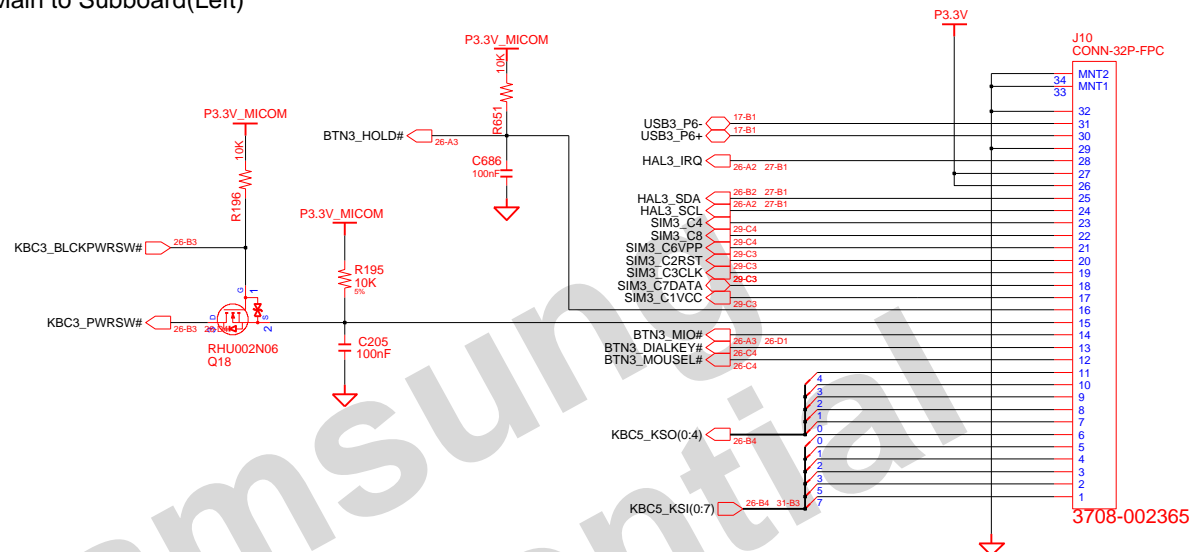
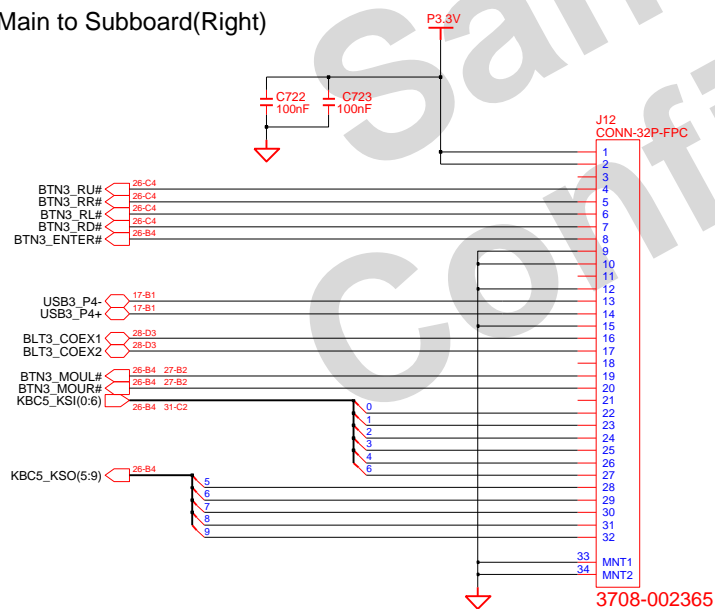
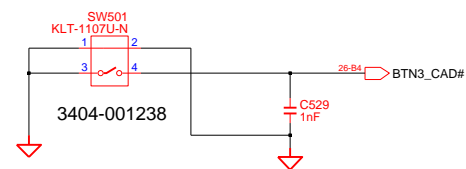
Wired LAN : 60p Conn



DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS PART NO. BA41-00743A
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	1.0	Wired LAN Conn		
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	30 OF 47	

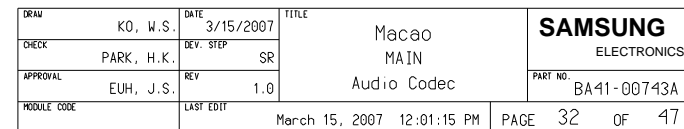
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Main to Subboard(Left)**Main to Subboard(Right)****Ctrl_Alt_Del Button**

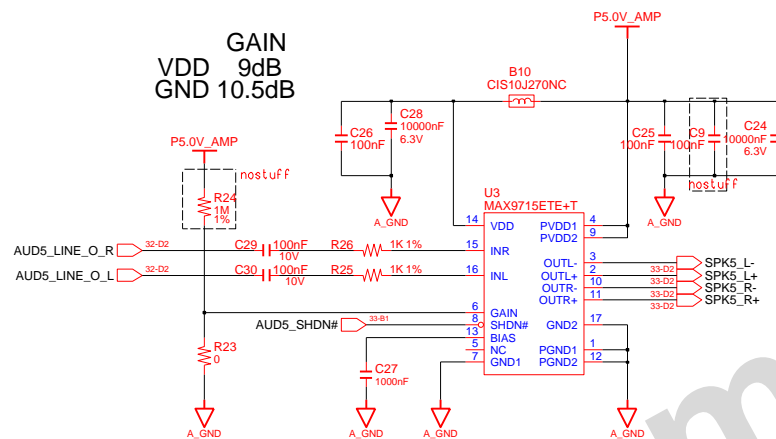
DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR		MAIN	
APPROVAL	EUH, J.S.	REV	1.0		SUB B'D Conn. & S/W	PART NO. BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	31	OF 47

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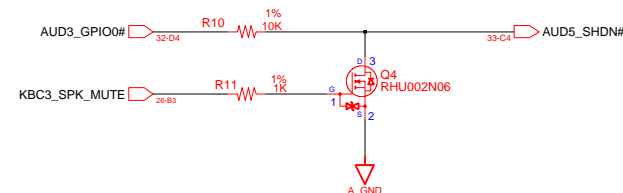
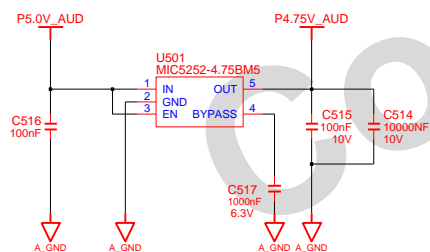
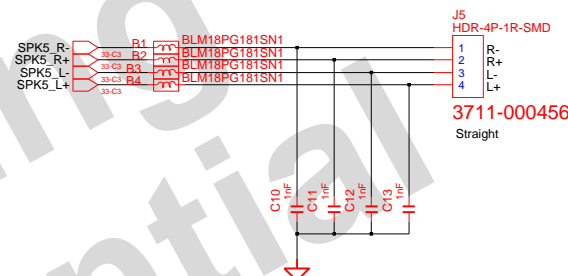


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INTERNAL STEREO SPEAKERS

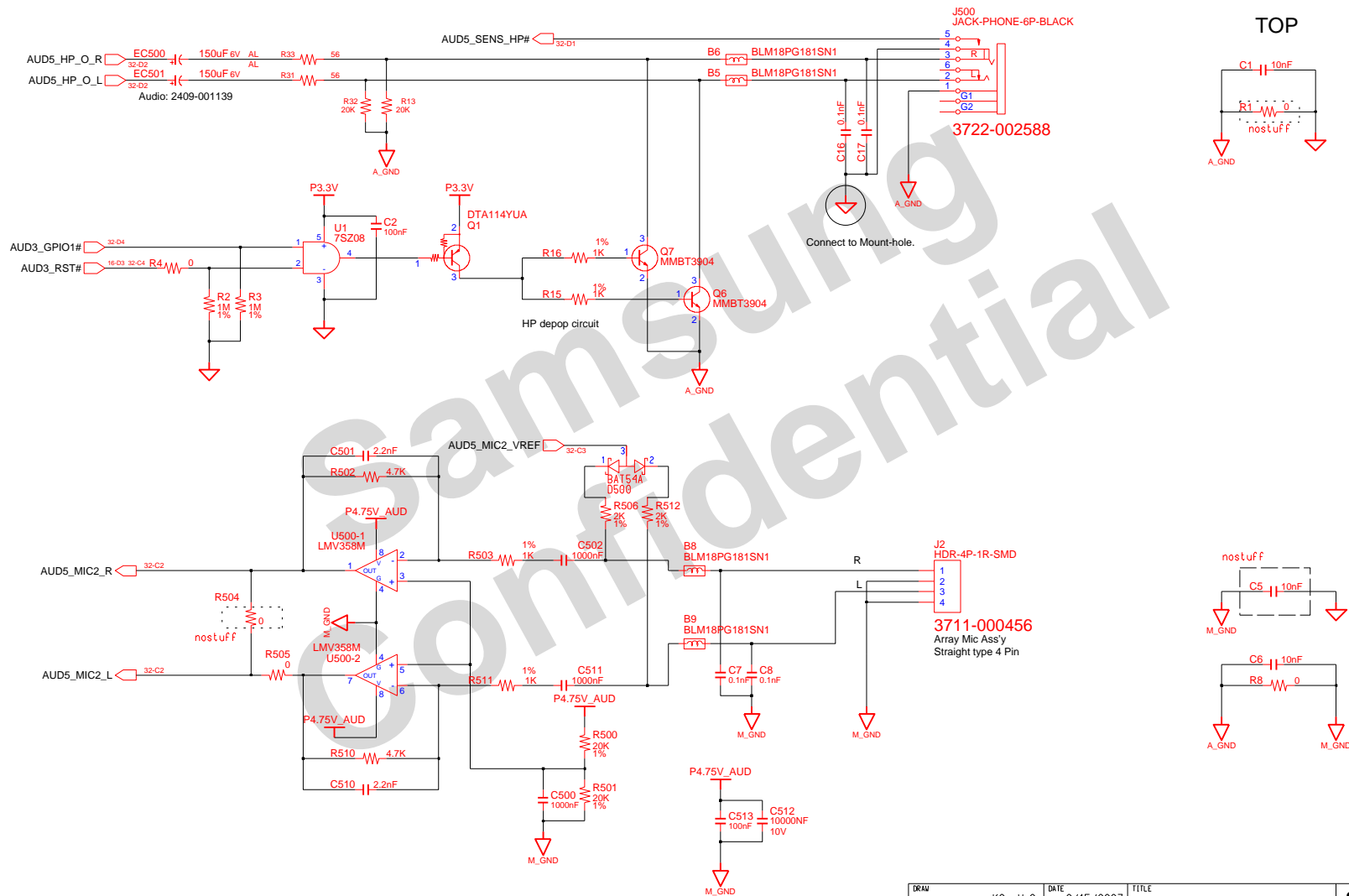


DRAW	K0, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR		MAIN	
APPROVAL	EUH, J.S.	REV	1.0		AMP & Spkr Conn	
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	33 OF 47	

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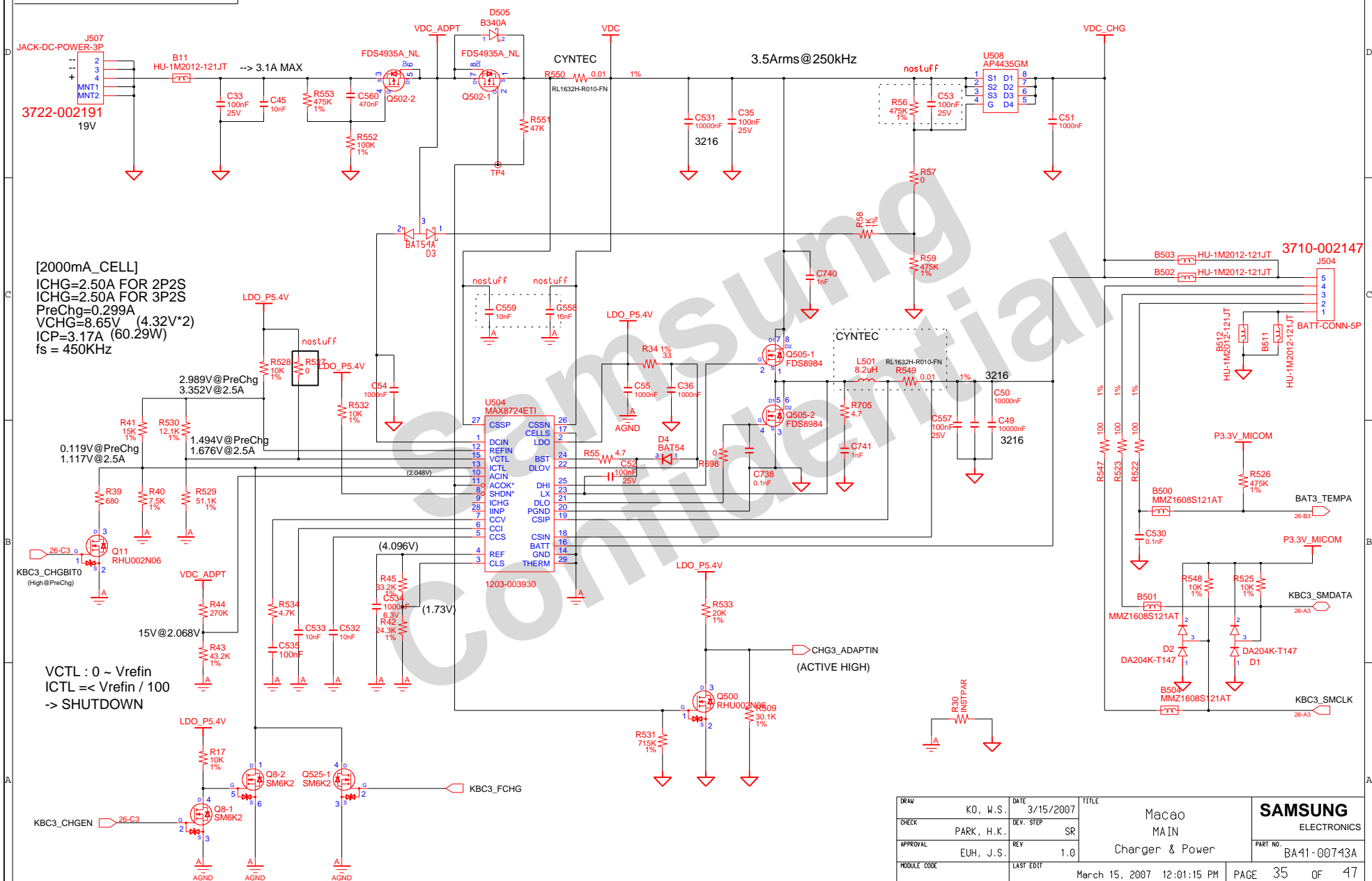
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HEADPHONE



DRAW	K0, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN	ELECTRONICS	
APPROVAL	EUH, J.S.	REV	1.0	Phone Jack & MIC	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	34	OF 47

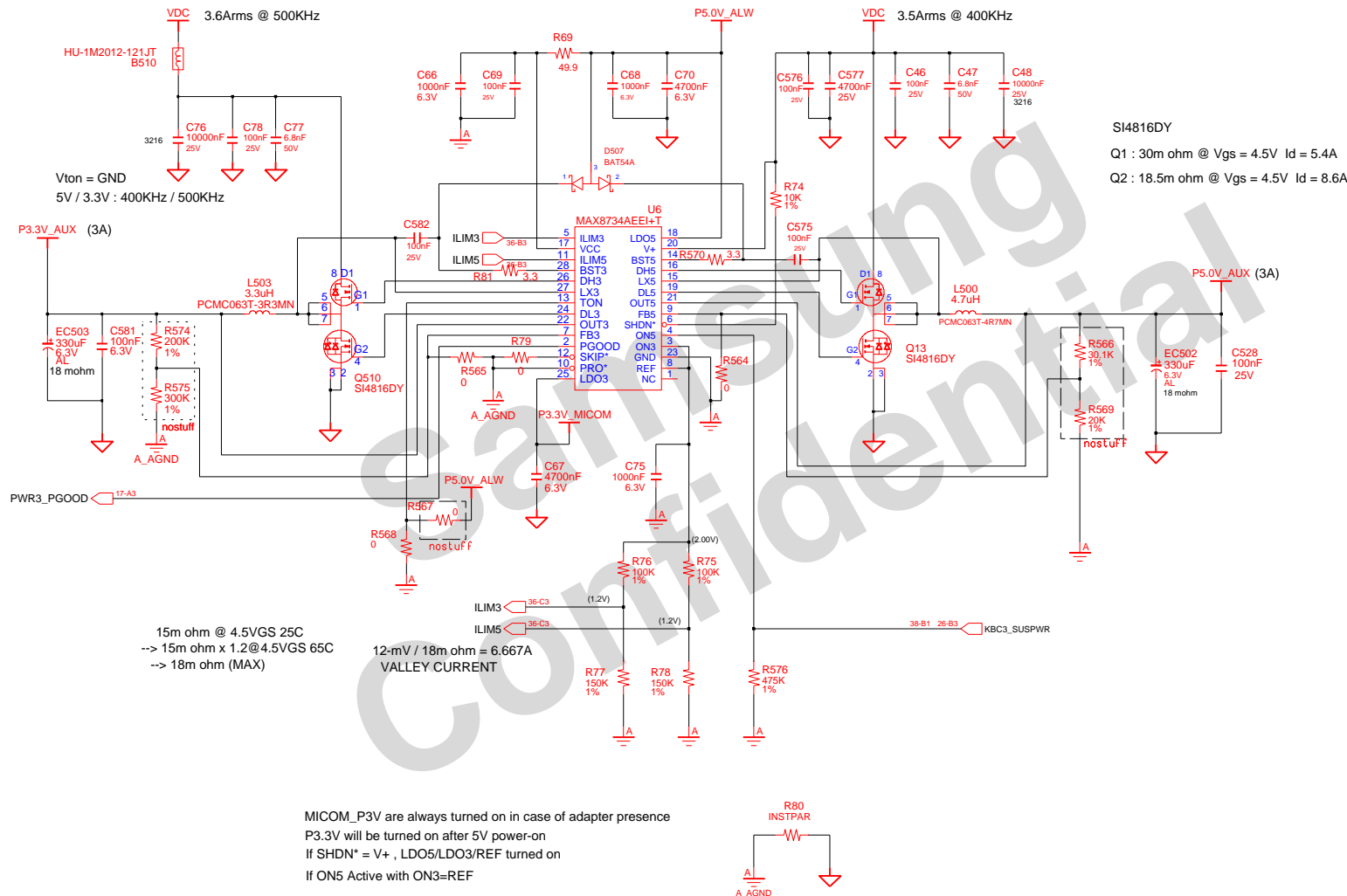
CHARGER & POWER MANAGEMENT



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P3.3V_AUX & P5V_AUX & P3.3V_MICOM



DRAW	K0, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR		MAIN	
APPROVAL	EUH, J.S.	REV	P3	P3V_AUX & P5V_AUX & MICOM_P3V	BA41-00743A	
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	36	OF 47


P1.5V & VCCP_CORE

COM-22C-015(1996.6.5) REV. 3

DDR2 POWER

g:/macao_c/macao_sr01

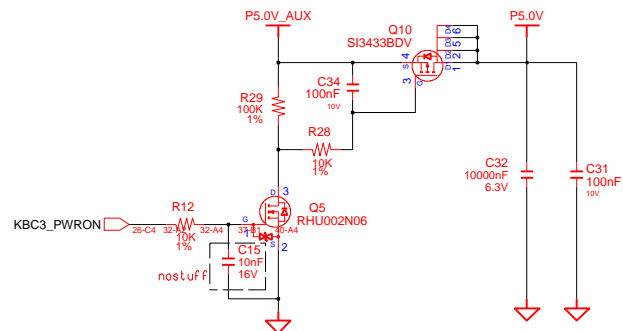
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DRAM	KO, W.S.	DATE	3/15/2007	TITLE	Macao MAIN CPU VRM	
CHECK	PARK, H.K.	DEV. STEP	SR			
APPROVAL	EUH, J.S.	REV	1.0			
MODULE CODE	LAST EDIT		March 15, 2007 12:01:15 PM			
				PART NO.	BA41-00743A	

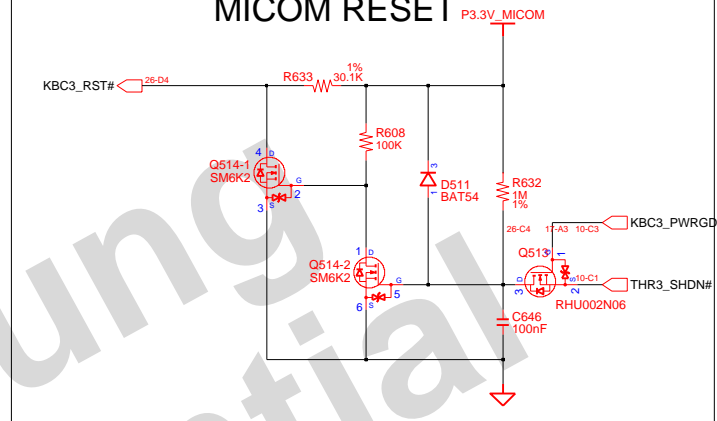
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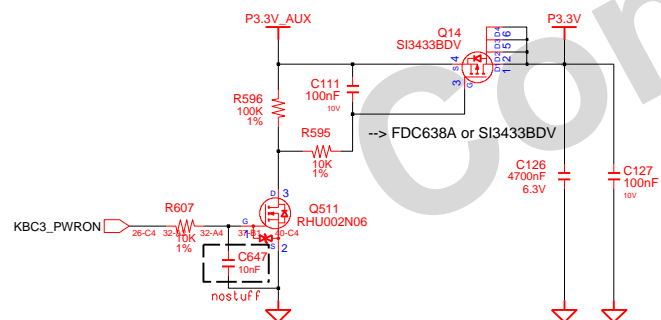
Load Switch Control(P5.0V)



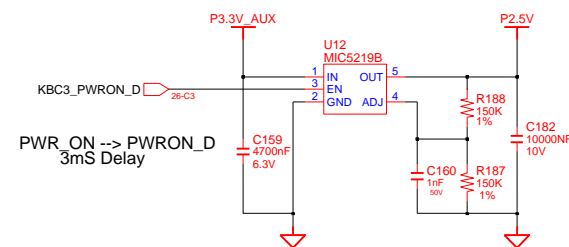
MICOM RESET



Load Switch Control(P3.3V)



LDO Power (P2.5V)



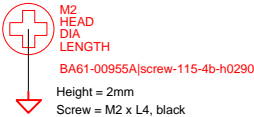
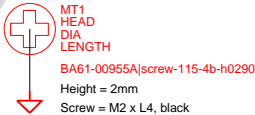
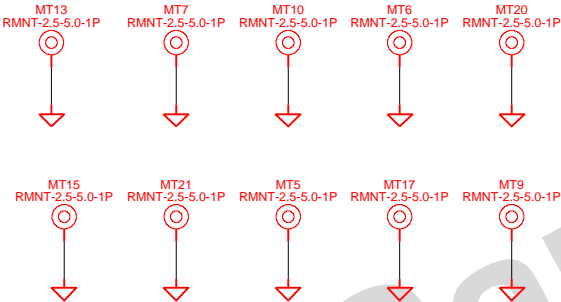
DRAW	K0, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR		MAIN	
APPROVAL	EUH, J.S.	REV	1.0		Switched Power	
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	40 OF 47	

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PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV1
1 O
2 O O3

Main Board Mount Hole



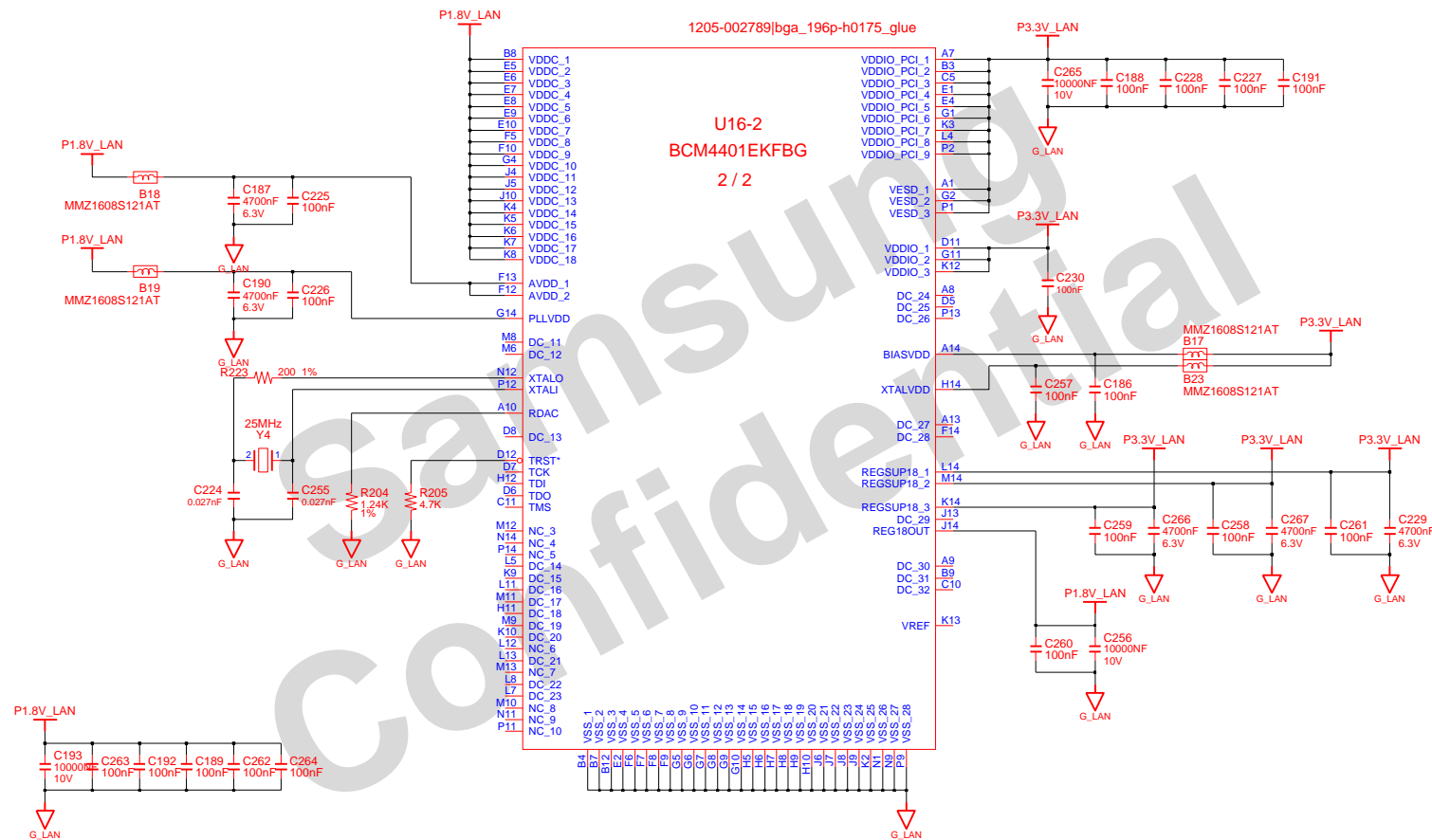
Mount Hole for LAN sub board

DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR	MAIN		
APPROVAL	EUH, J.S.	REV	1.0	Mount Hole		PART NO.
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM			BA41-00743A
				PAGE	41	OF 47

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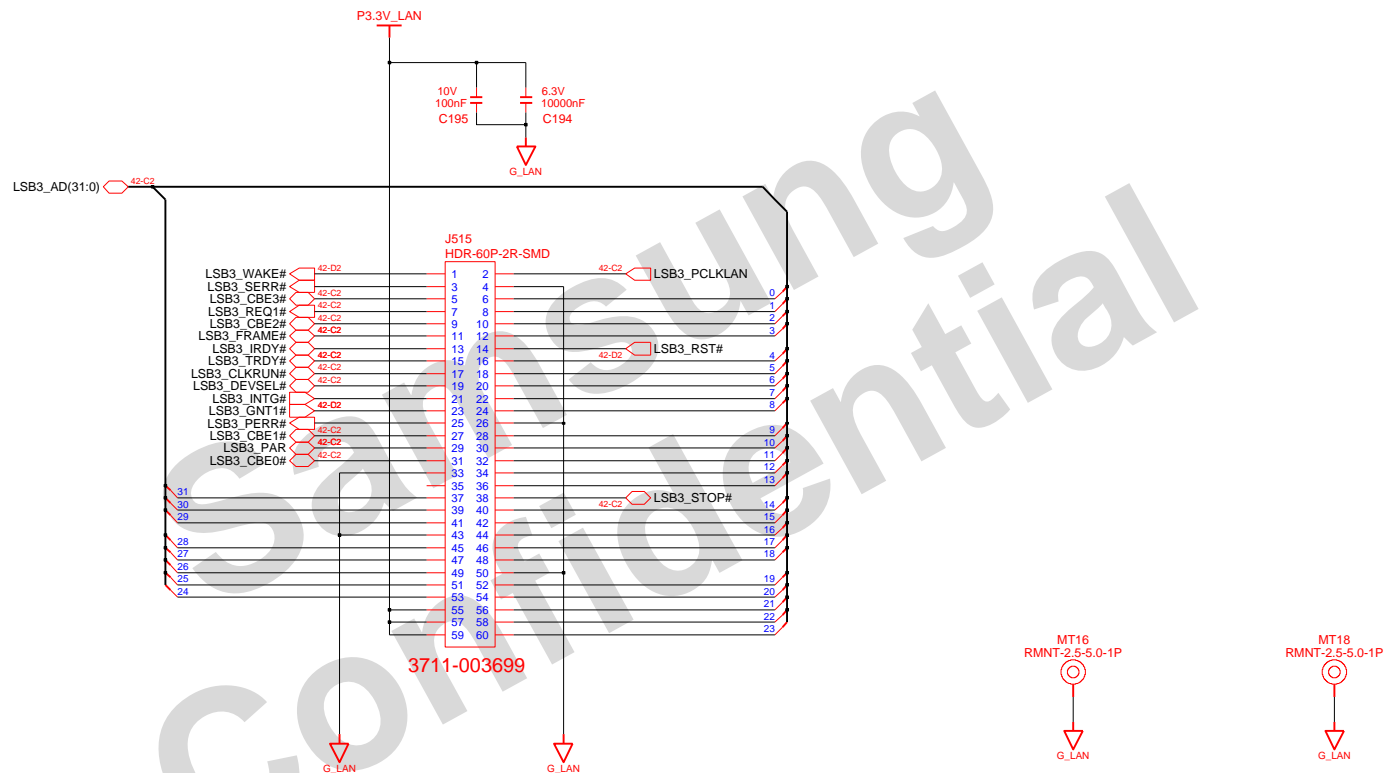
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LAN Controller (Only 10/100M)



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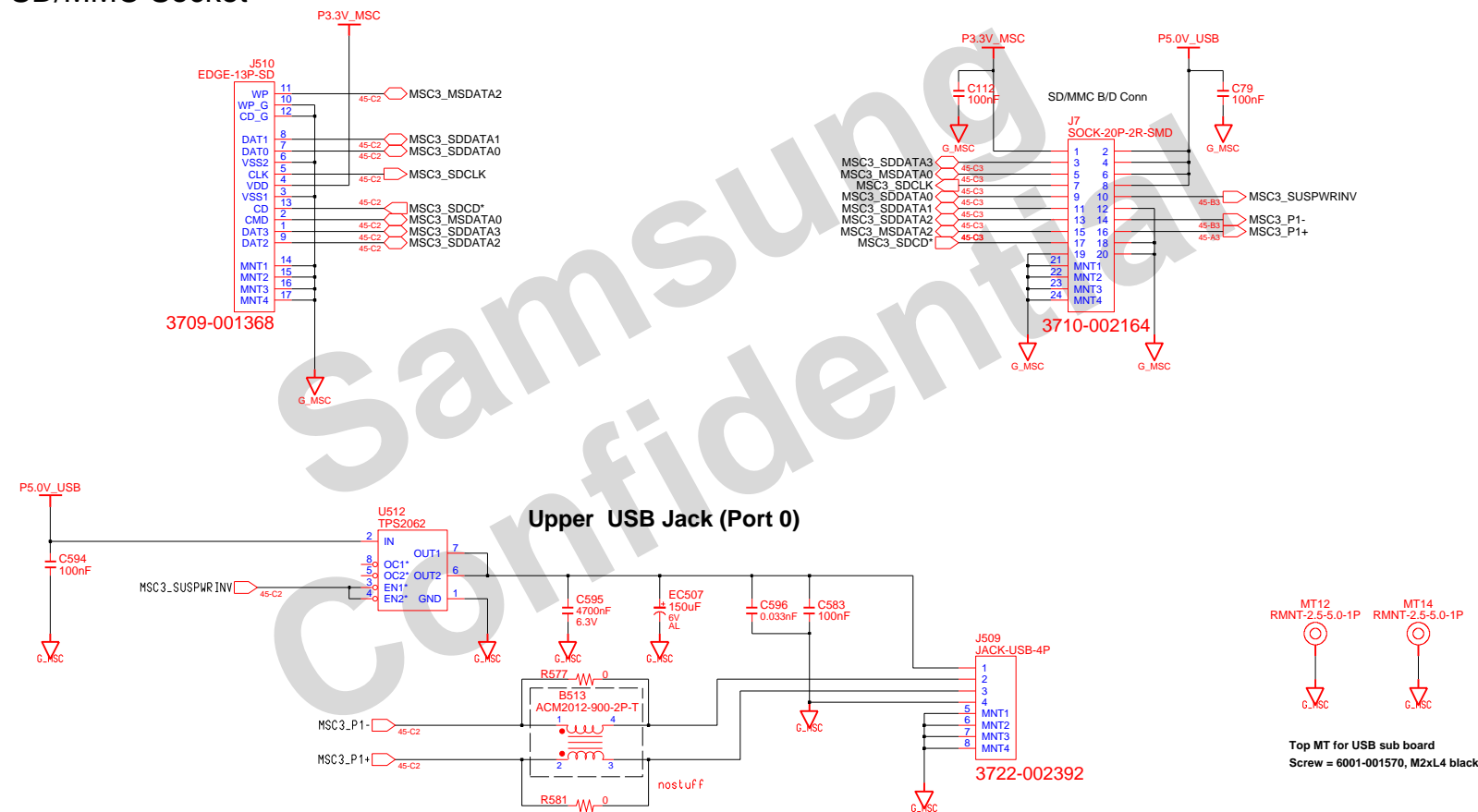
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Bottom MT for LAN sub board
Screw = 6001-001570, M2xL4 black

DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG ELECTRONICS
CHECK	PARK, H.K.	DEV. STEP	SR		LAN B'd	
APPROVAL	EUH, J.S.	REV	1.0		LAN(3/3)	
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	44 OF 47	

SD/MMC Socket



DRAM	KO, W. S.	DATE	3/15/2007	Macao SD/MMC Socket B'd SD/MMC Socket	SAMSUNG ELECTRONICS
CHECK	PARK, H. K.	DEV. STEP	SR		
APPROVAL	EUH, J. S.	REV	1.0		
MODULE CODE	LAST EDIT		March 15, 2007 12:01:15 PM		
				PART NO.	BA41-00743A

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Sub Board Left

Sub Left Board to Main board

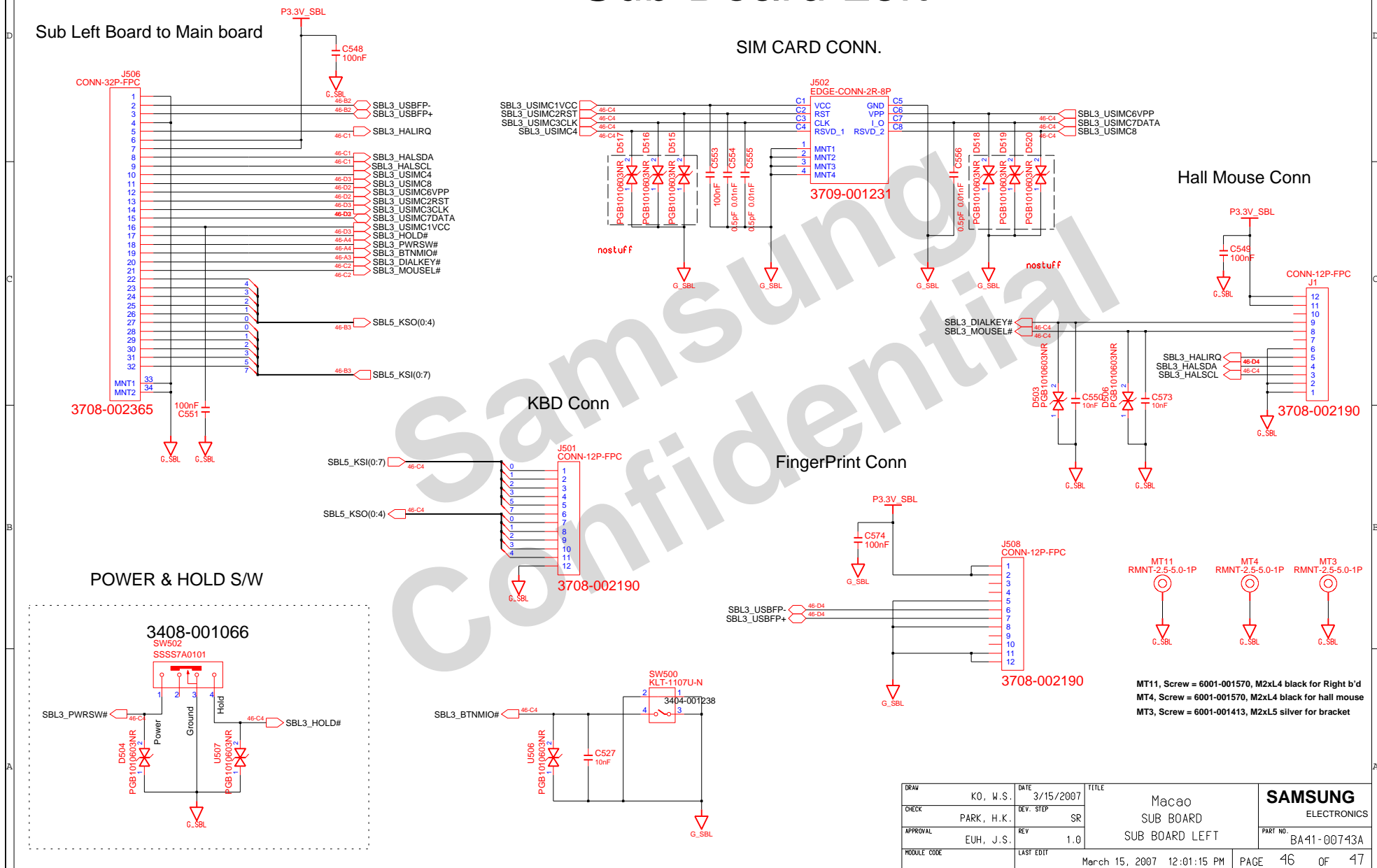
SIM CARD CONN.

Hall Mouse Conn

KBD Conn

FingerPrint Conn

POWER & HOLD S/W



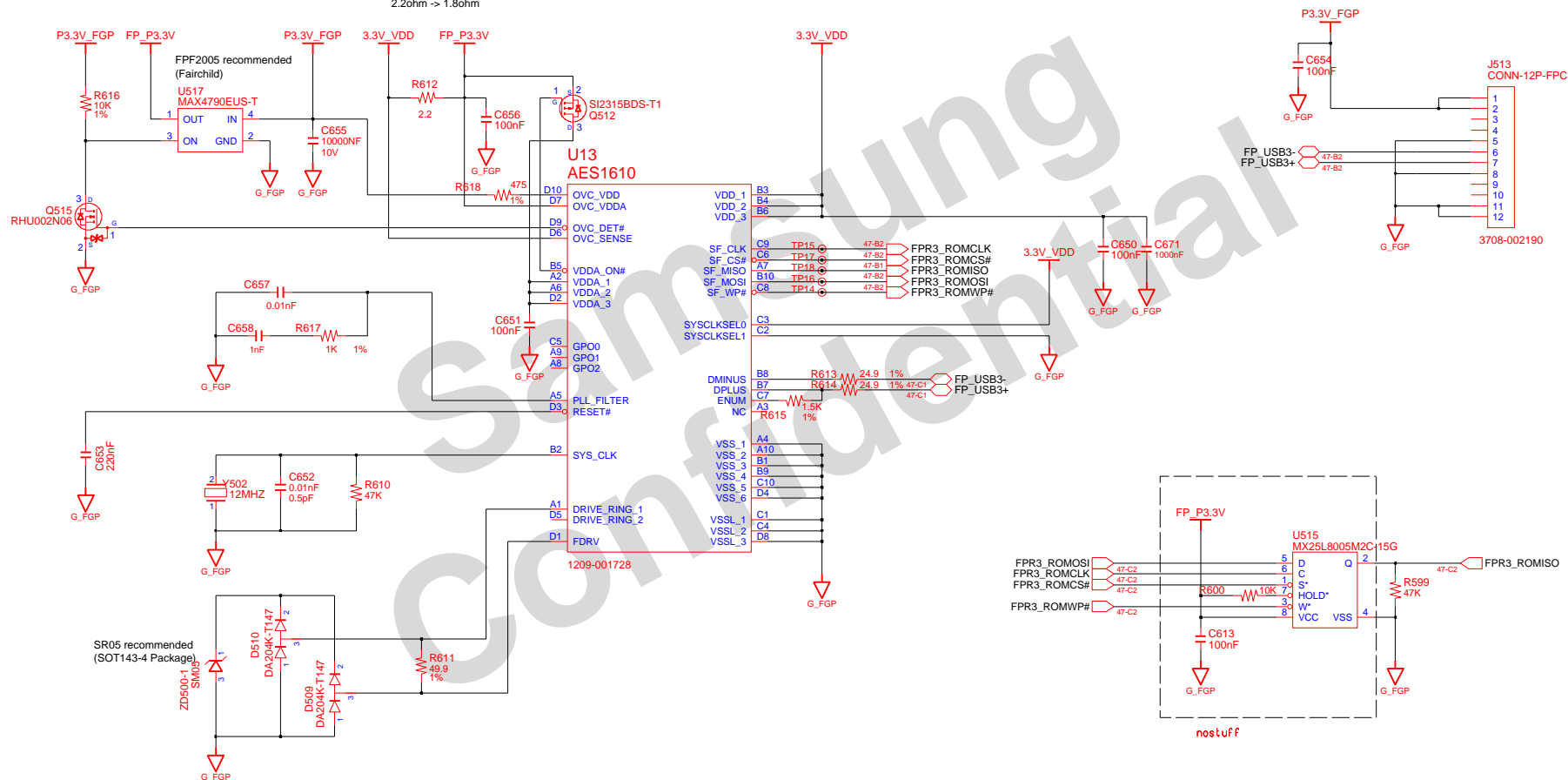
DRAW	KO, W.S.	DATE	3/15/2007	TITLE	Macao	SAMSUNG
CHECK	PARK, H.K.	DEV. STEP	SR	SUB BOARD		ELECTRONICS
APPROVAL	EUH, J.S.	REV	1.0	SUB BOARD LEFT	PART NO.	BA41-00743A
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	46	OF 47

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Finger Print Sub Board

Recommend value
2.2ohm -> 1.8ohm



DRAW	K0, W.S.	DATE	3/15/2007	TITLE	Macao SUB BOARD FINGERPRINT	SAMSUNG ELECTRONICS PART NO. BA41-00743A
CHECK	PARK, H.K.	DEV. STEP	SR			
APPROVAL	EUH, J.S.	REV	1.0			
MODULE CODE		LAST EDIT	March 15, 2007 12:01:15 PM	PAGE	47 OF 47	