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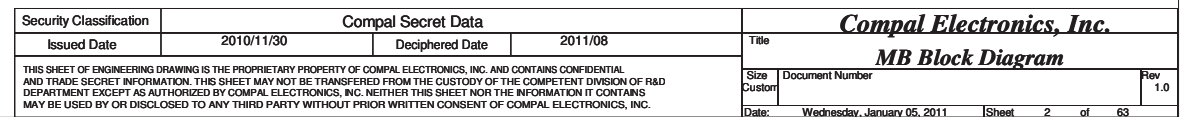
PIQY0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
nVIDIA N12P-GT

2010-12-30

REV: 1.0

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Voltage Rails

power plane	State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0		○	○	○	○
S3		○	○	○	✗
S5 S4/AC		○	○	✗	✗
S5 S4/ Battery only		○	✗	✗	✗
S5 S4/AC & Battery don't exist		✗	✗	✗	✗

SMBUS Control Table

	SOURCE	VGA	BATT	KB930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	✗	✓ +3VALW	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	✗	✗	✗	✗	✗	✗	✓ +3VS
SMBCLK SMBDATA	PCH +3VALW	✗	✗	✗	✓ +3VS	✓ +3VS	✗	✗
SML0CLK SML0DATA	PCH +3VALW	✗	✗	✗	✗	✗	✗	✗
SML1CLK SML1DATA	PCH +3VALW	✓ +3VS	✗	✓ +3VS	✗	✗	✓ +3VS	✗

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BOM Structure Table

BTO Item	BOM Structure
UMA	
UMA Only	UMA_ONLY@
Optimus	OPTI@
VRAM	X76@
HDMI	HDMI@
Blue Tooth	BT@
USB3.0	USB30@
ESATA	ESATA@
USB Charger	USB_CHG@
No USB Charger	NO_CHG@
Unpop	@
Codec ALC272	272@
Codec ALC5503	5503@
LAN 57781	57781@
LAN 57780	57780@
Ventura Feature	VENTURA@
Camera	CMOS@

VRAM BOM Config

X761G@: X7625738L01	Samsung 1GB
Sub: X7625738L02	Hynix 1GB
X762G@: X7625738L03	Samsung 2GB
Sub: X7625738L04	Hynix 2GB

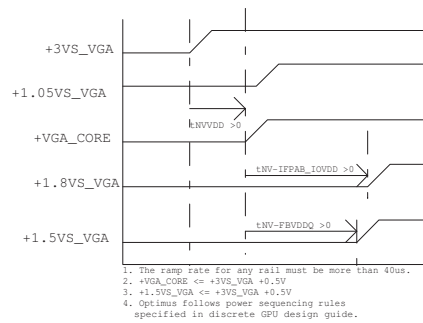
GPU BOM Config

N12P SKU:	OPTI@
GS SKU:	GS@
GT SKU:	GT@

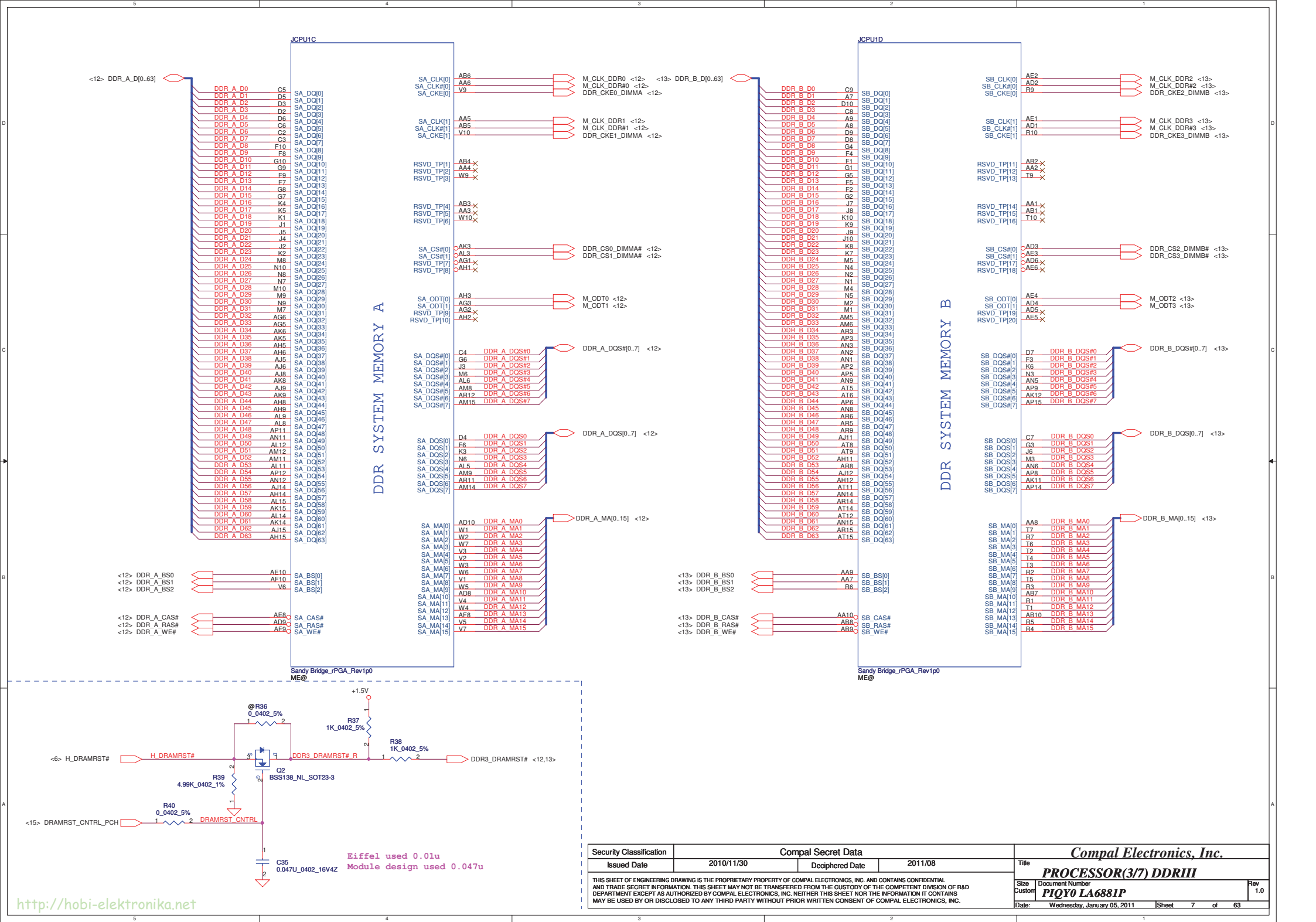
USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/Cable (Right Side)
		1	USB Port (Right Side COMBO)
	UHCI1	2	USB/B (Left Side)
		3	USB/B (Left Side)
	UHCI2	4	
		5	Camera
EHCI2	UHCI3	6	
		7	
	UHCI4	8	
		9	Mini Card(WLAN)
	UHCI5	10	
		11	
	UHCI6	12	
		13	Blue Tooth

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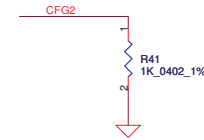
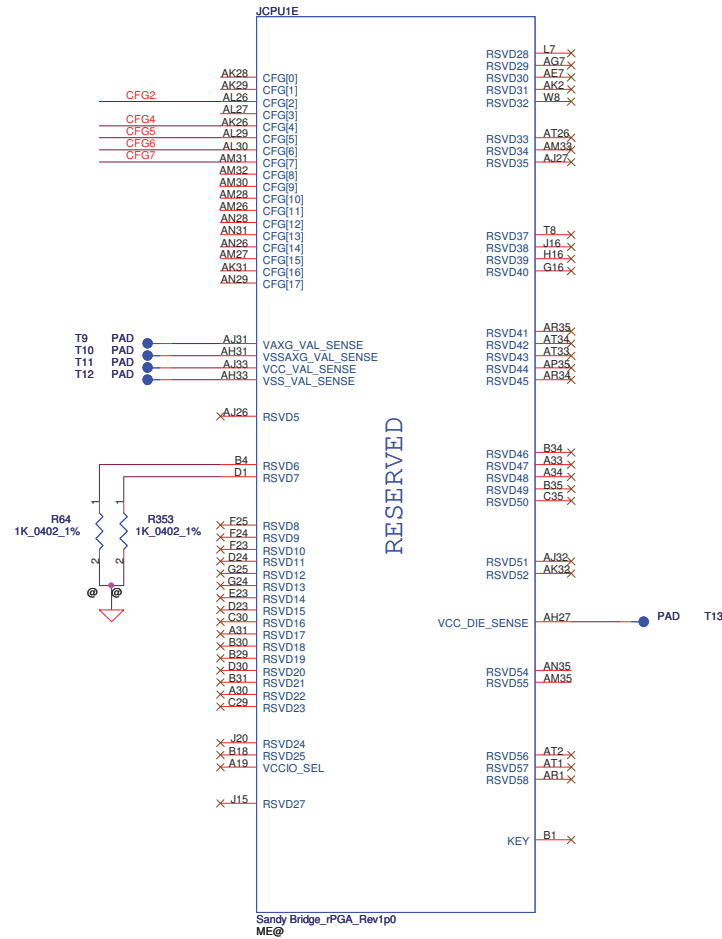
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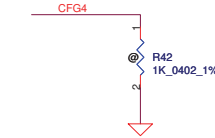
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								PROCESSOR(3/7) DDRIII			
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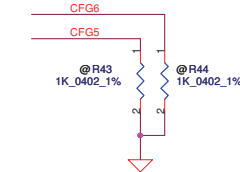
CFG Straps for Processor



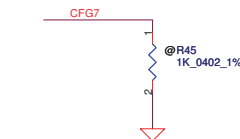
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

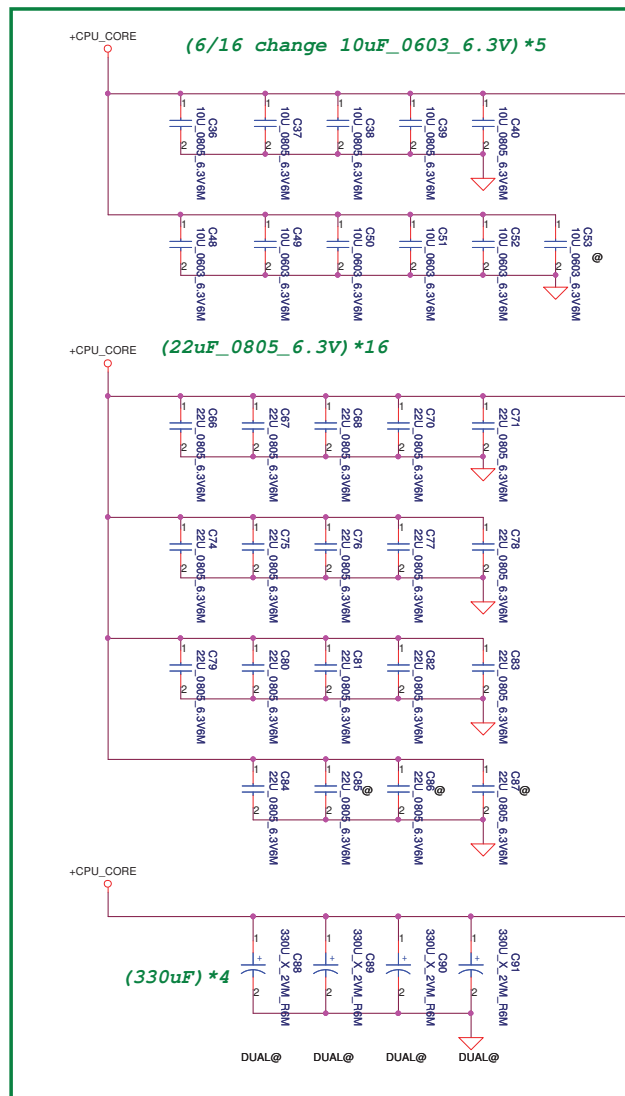


PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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POWER

JCPU1F



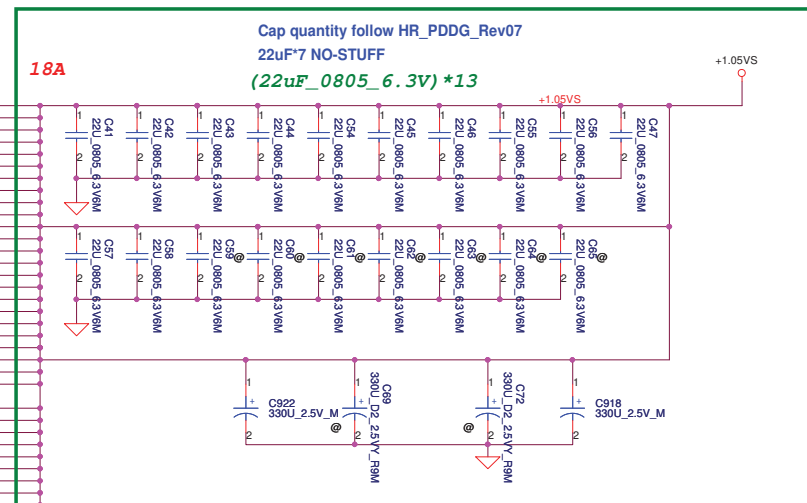
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DC=53A

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AD35 VCC20
AD34 VCC21
AD33 VCC22
AD32 VCC23
AD31 VCC24
AD30 VCC25
AD29 VCC26
AD28 VCC27
AD27 VCC28
AD26 VCC29
AC35 VCC30
AC34 VCC31
AC33 VCC32
AC32 VCC33
AC31 VCC34
AC30 VCC35
AC29 VCC36
AC28 VCC37
AC27 VCC38
AC26 VCC39
AA35 VCC40
AA34 VCC41
AA33 VCC42
AA32 VCC43
AA31 VCC44
AA30 VCC45
AA29 VCC46
AA28 VCC47
AA27 VCC48
Y35 VCC49
Y34 VCC50
Y33 VCC51
Y32 VCC52
Y31 VCC53
Y30 VCC54
Y29 VCC55
Y28 VCC56
Y27 VCC57
Y26 VCC58
Y25 VCC59
Y24 VCC60
Y23 VCC61
Y22 VCC62
Y21 VCC63
Y20 VCC64
Y19 VCC65
Y18 VCC66
Y17 VCC67
Y16 VCC68
Y15 VCC69
Y14 VCC70
Y13 VCC71
Y12 VCC72
Y11 VCC73
Y10 VCC74
Y09 VCC75
Y08 VCC76
Y07 VCC77
Y06 VCC78
Y05 VCC79
Y04 VCC80
Y03 VCC81
Y02 VCC82
Y01 VCC83
Y00 VCC84
Y00 VCC85
Y00 VCC86
Y00 VCC87
Y00 VCC88
Y00 VCC89
Y00 VCC90
Y00 VCC91
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Y00 VCC96
Y00 VCC97
Y00 VCC98
Y00 VCC99
Y00 VCC100

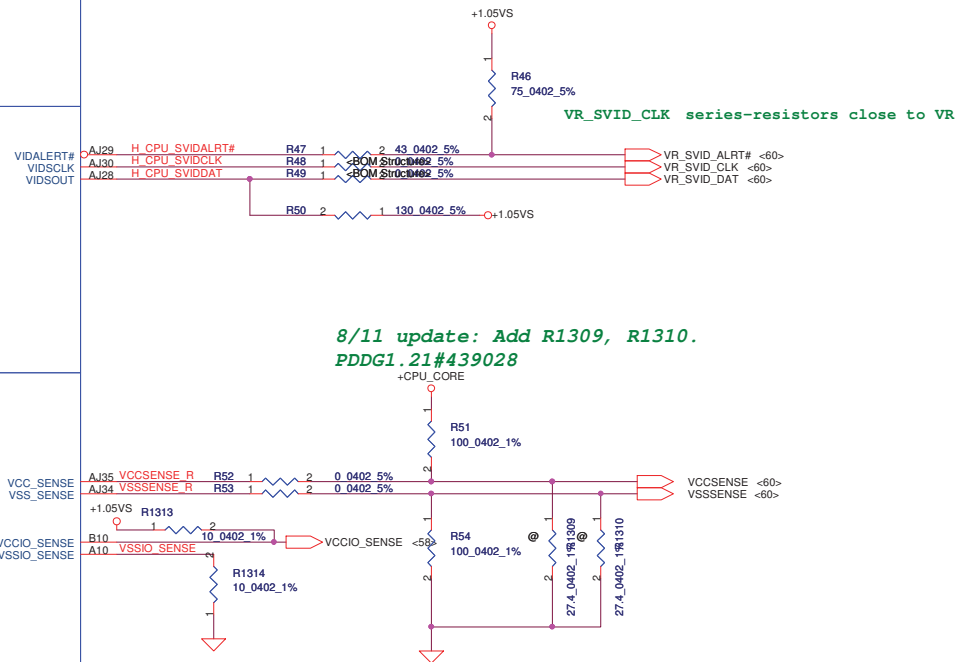
CORE SUPPLY

SVID

SENSE LINES



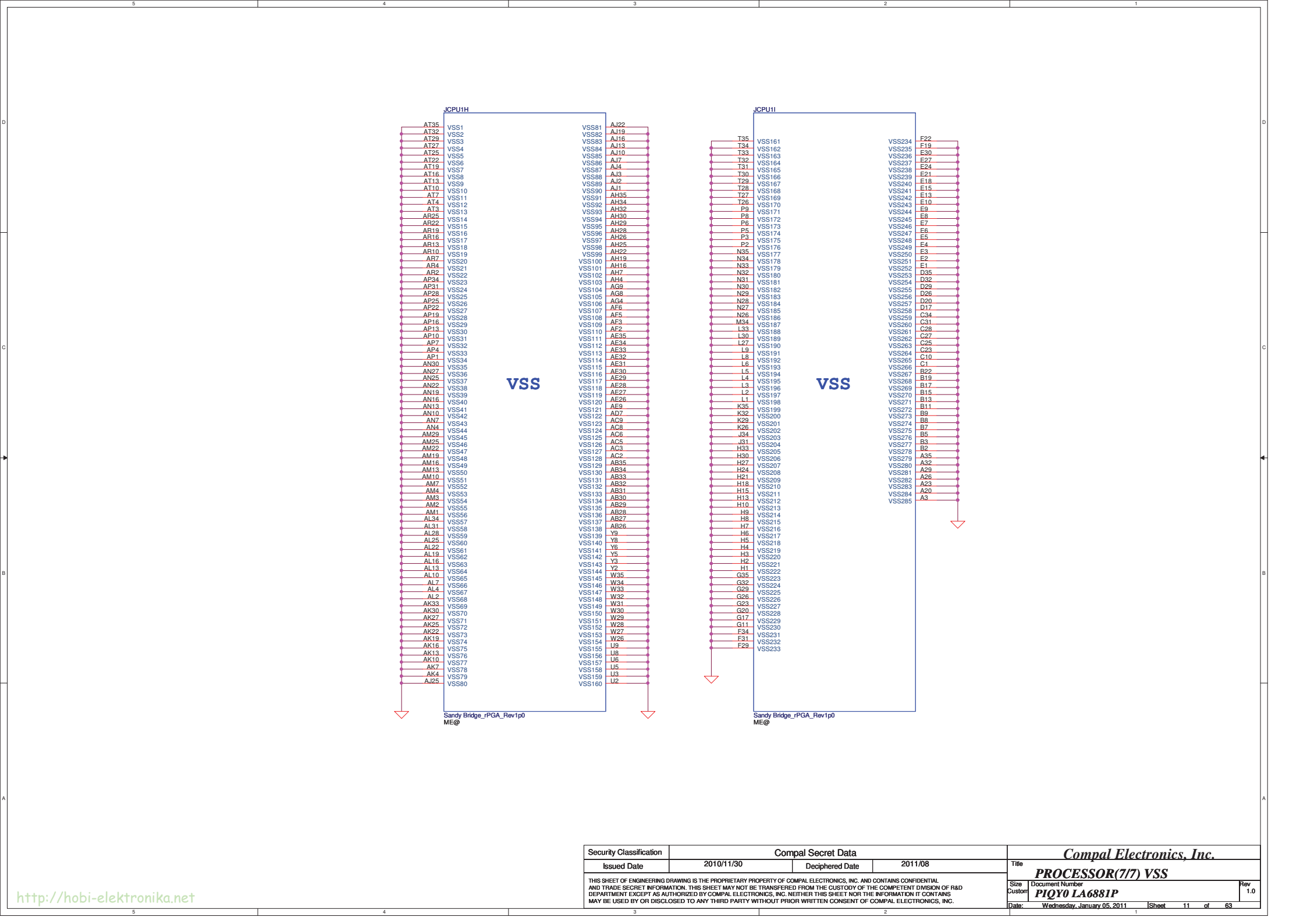
PEG AND DDR

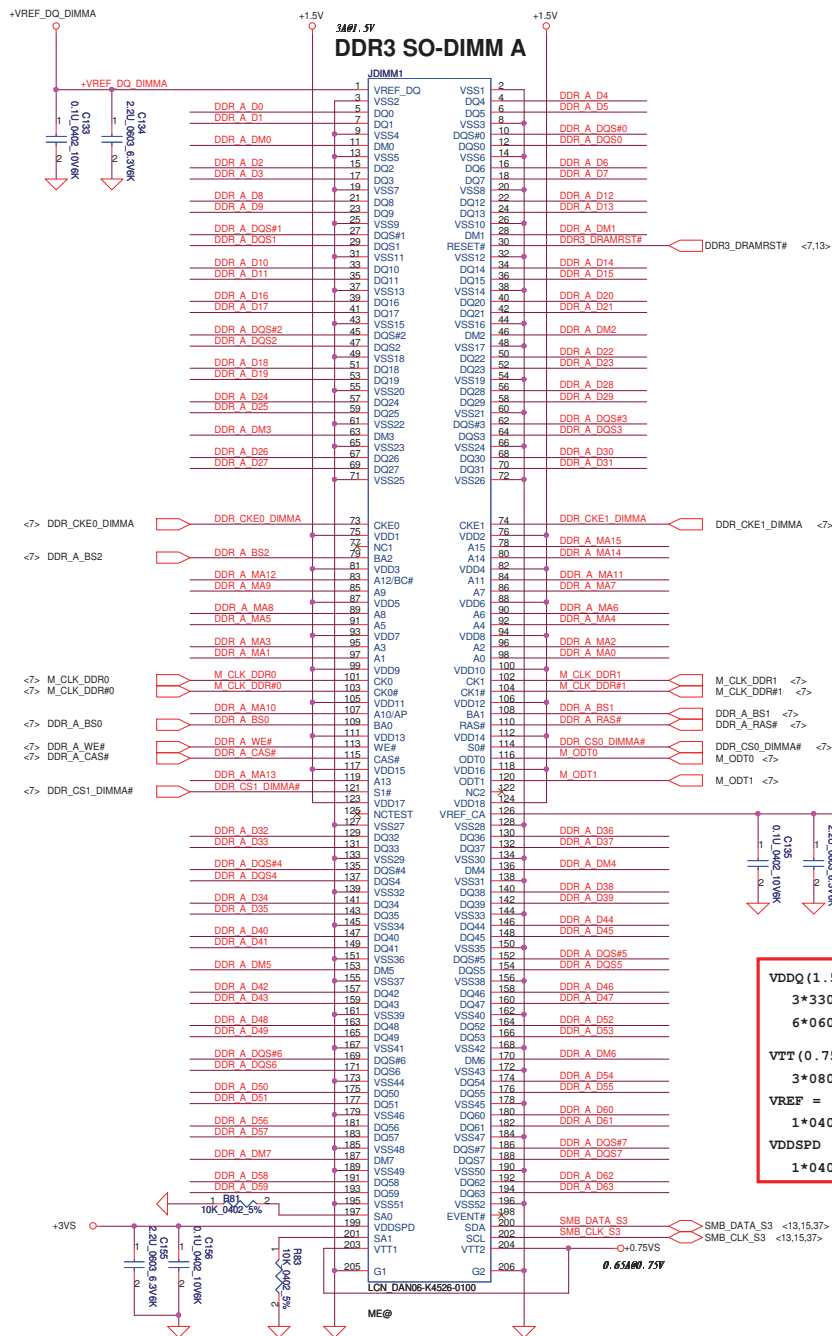


Sandy Bridge_rPGA Rev1.0
ME@

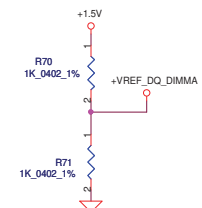
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PROCESSOR(5/7) PWR,BYPASS	
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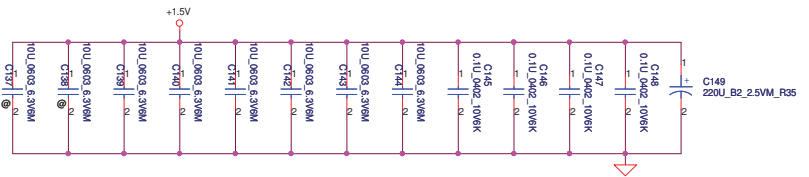


- <7> DDR_A_D[0..63]
- <7> DDR_A_DQS[0..7]
- <7> DDR_A_DQS[0..7]
- <7> DDR_A_MA[0..15]

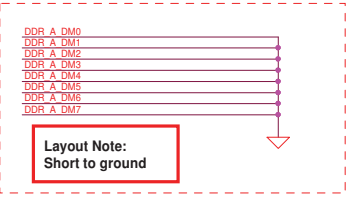
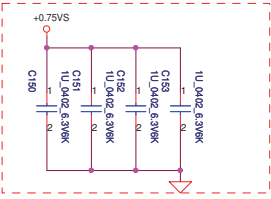


Layout Note:
Place near DIMM

(10uF_0603_6.3V) *8
(0.1uF_402_10V) *4



Layout Note:
Place near DIMM



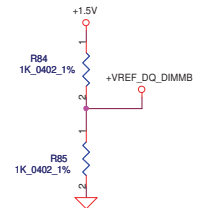
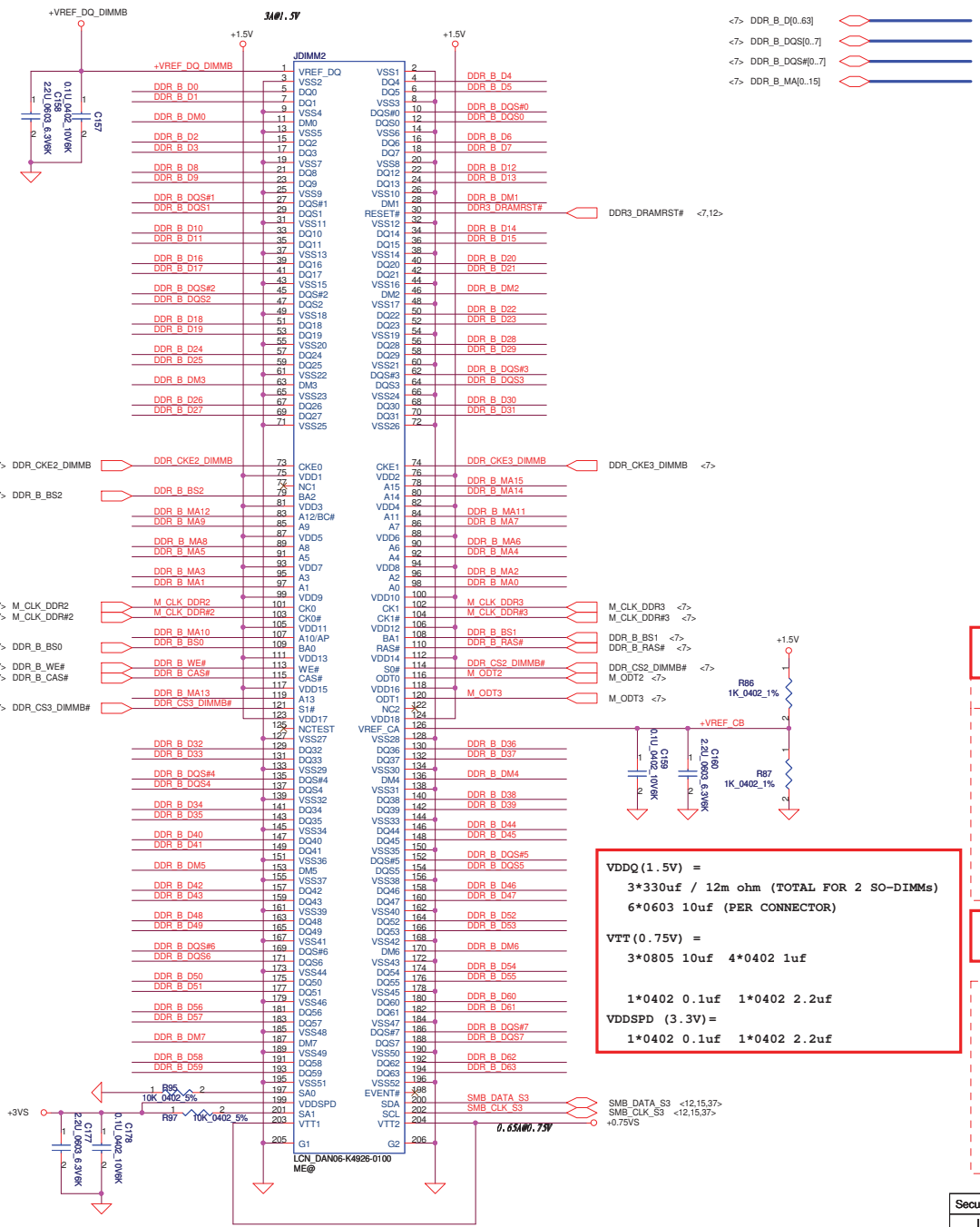
VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V) =
1*0402 0.1uf 1*0402 2.2uf

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For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.
07/17/2009

Layout Note:
Place near DIMM

(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note:
Place near DIMM

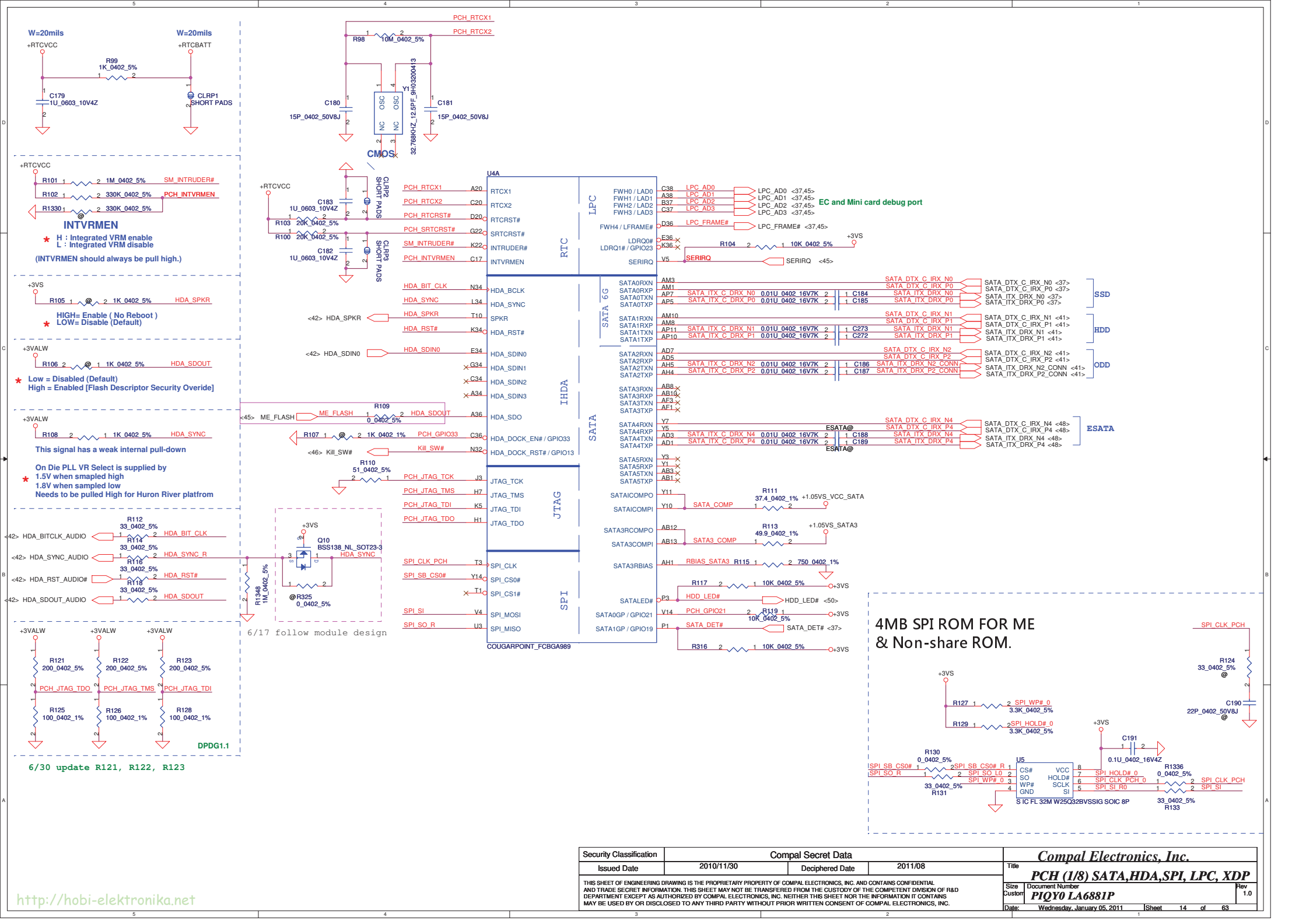
Layout Note:
Short to ground

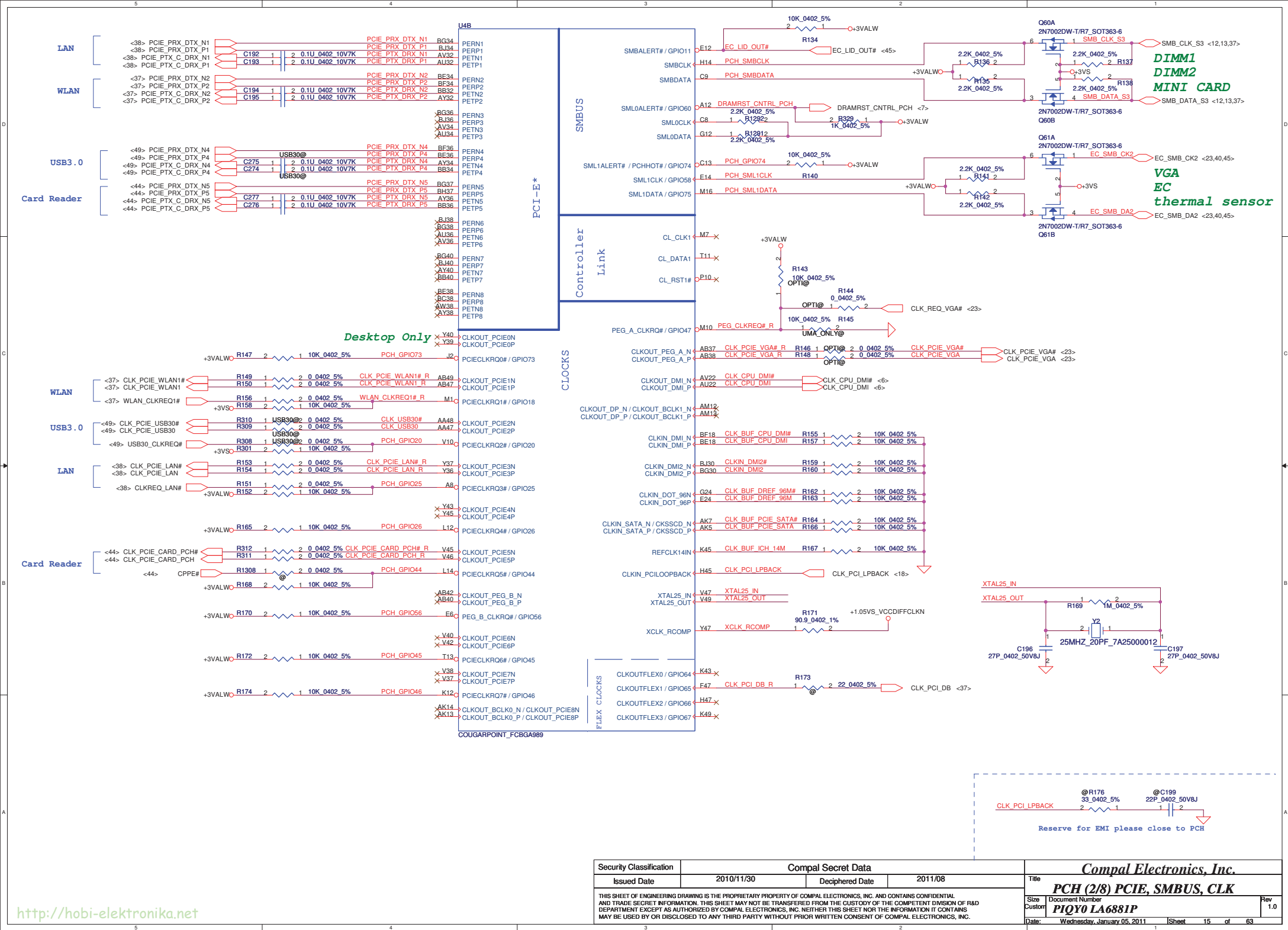
VDDQ (1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMS)
6*0603 10uf (PER CONNECTOR)

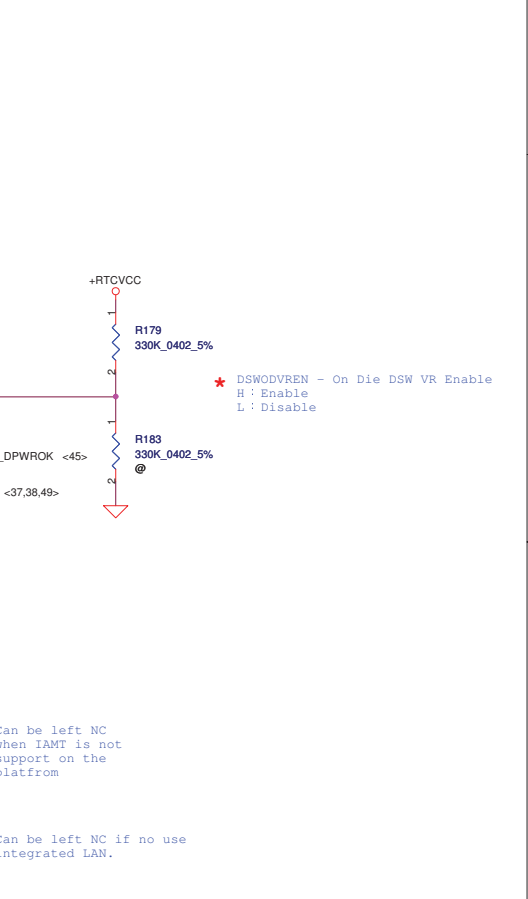
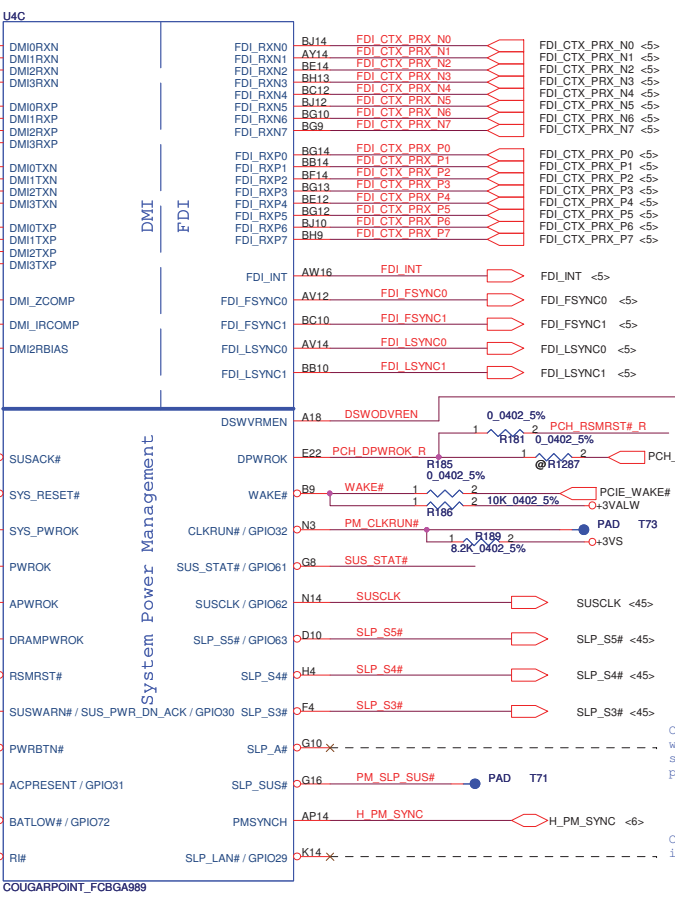
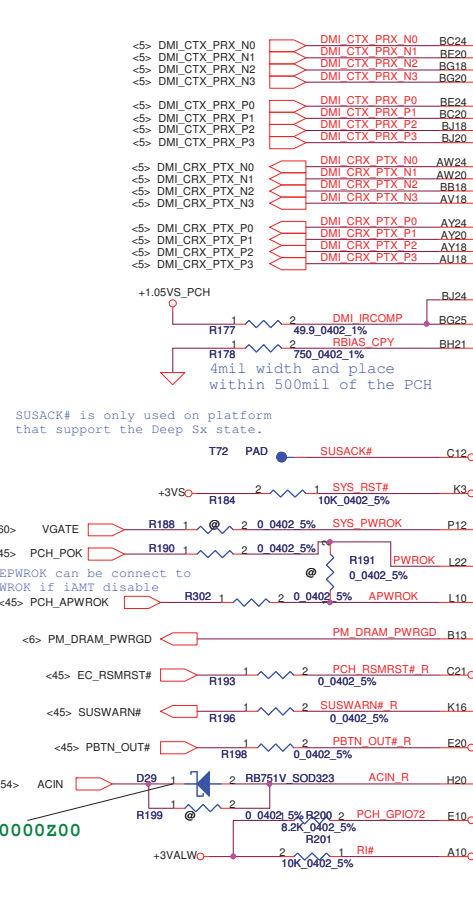
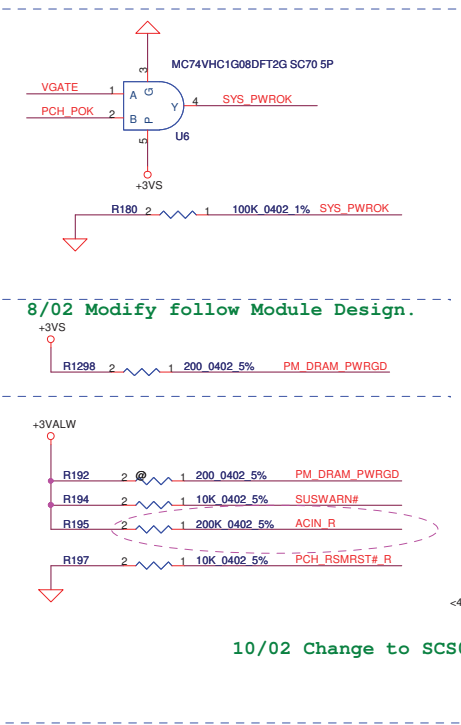
VTT (0.75V) =
3*0805 10uf 4*0402 1uf

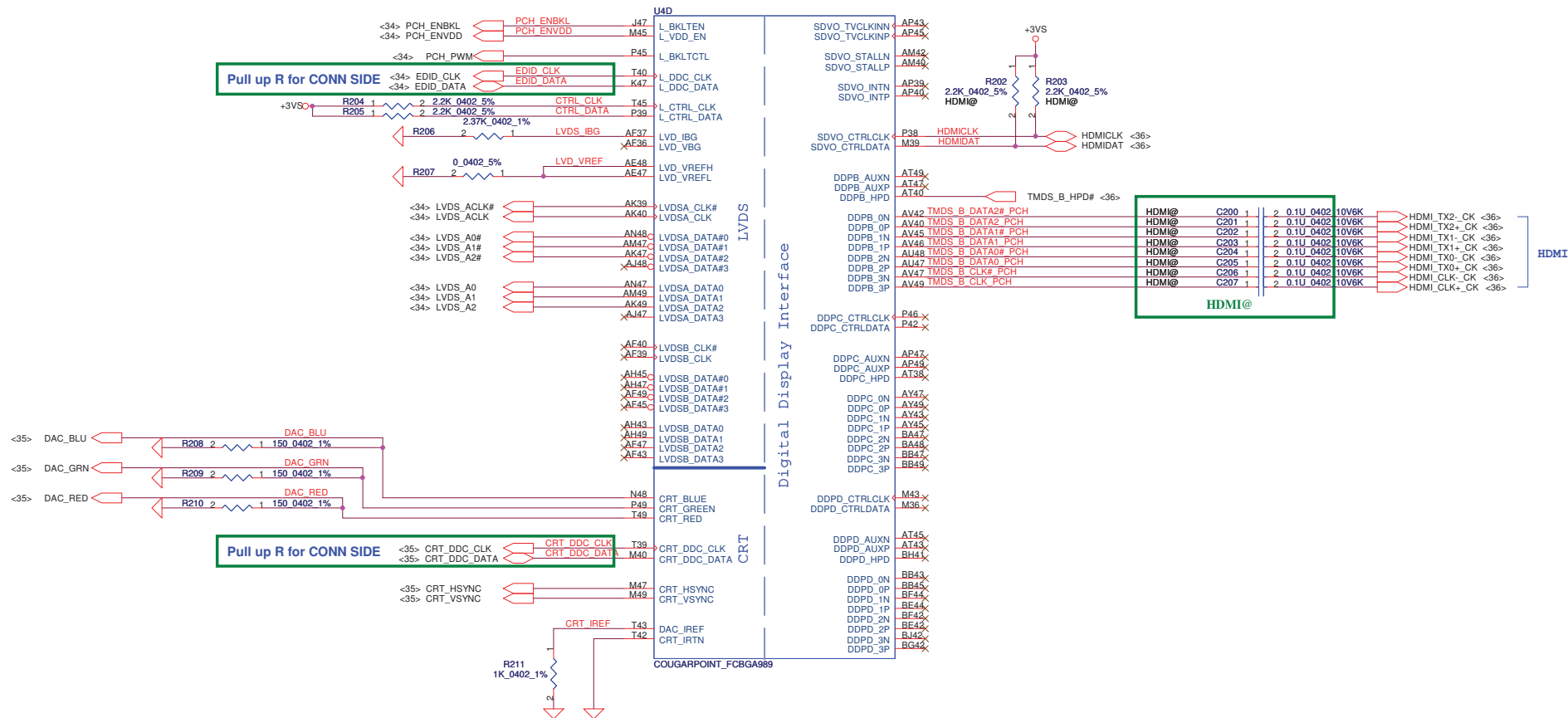
VDDSPD (3.3V) =
1*0402 0.1uf 1*0402 2.2uf
1*0402 0.1uf 1*0402 2.2uf

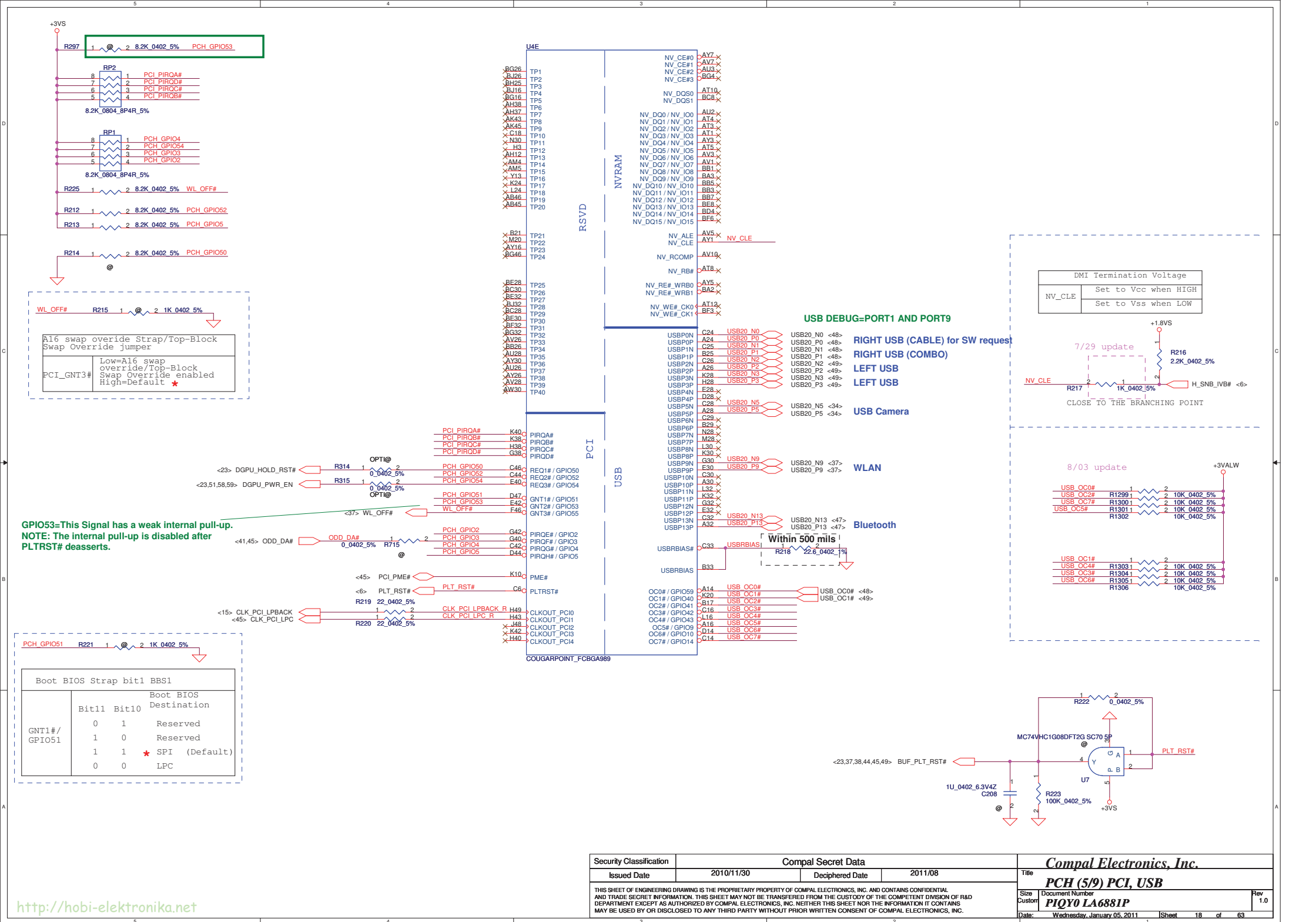
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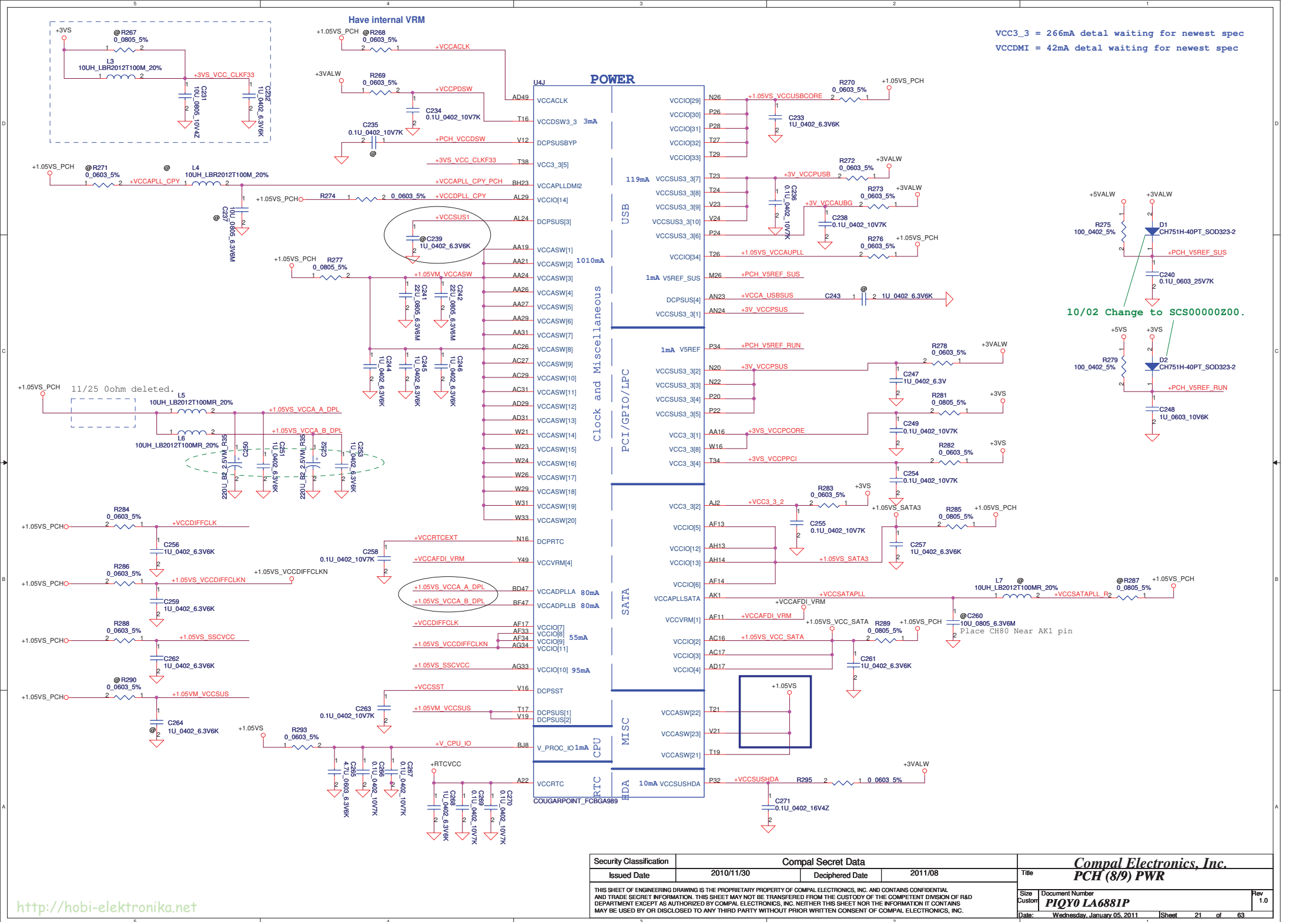


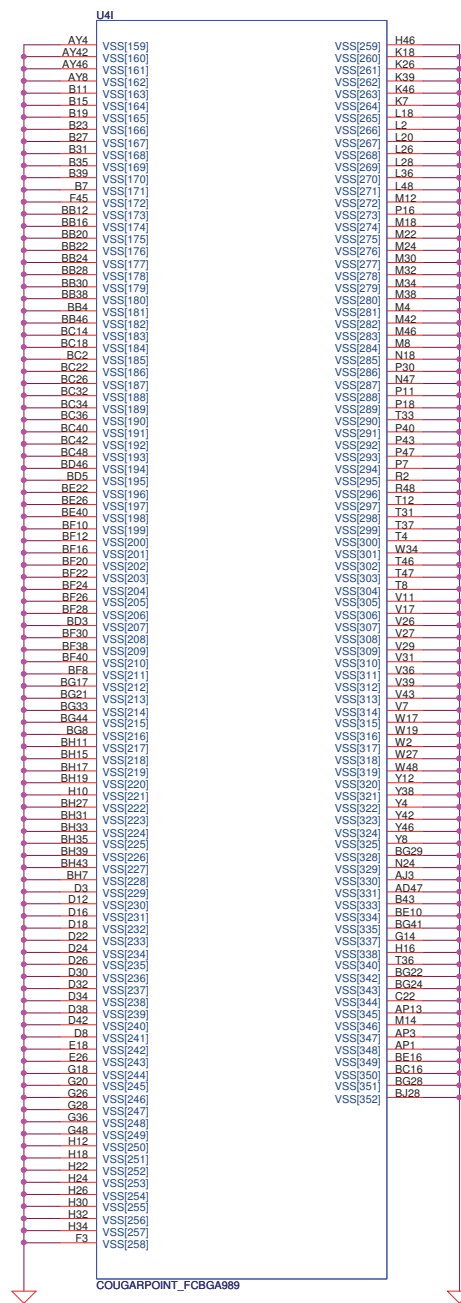
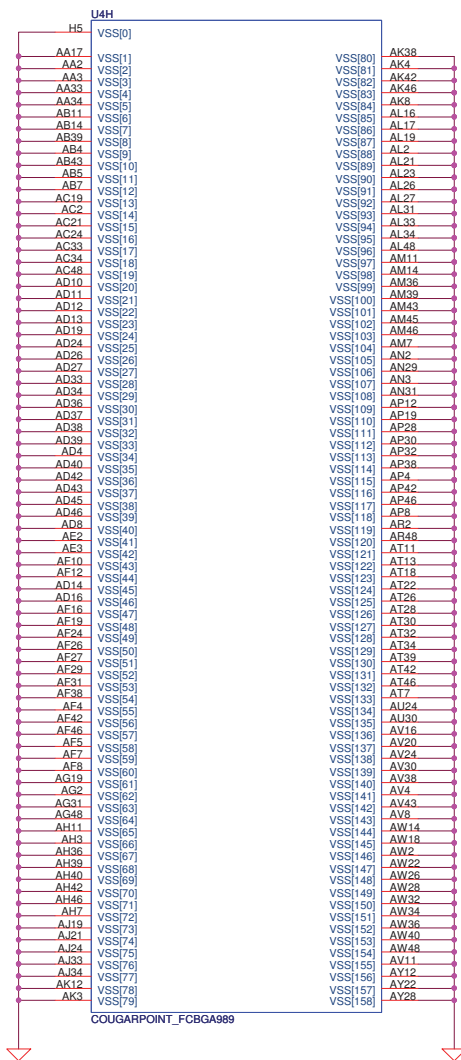




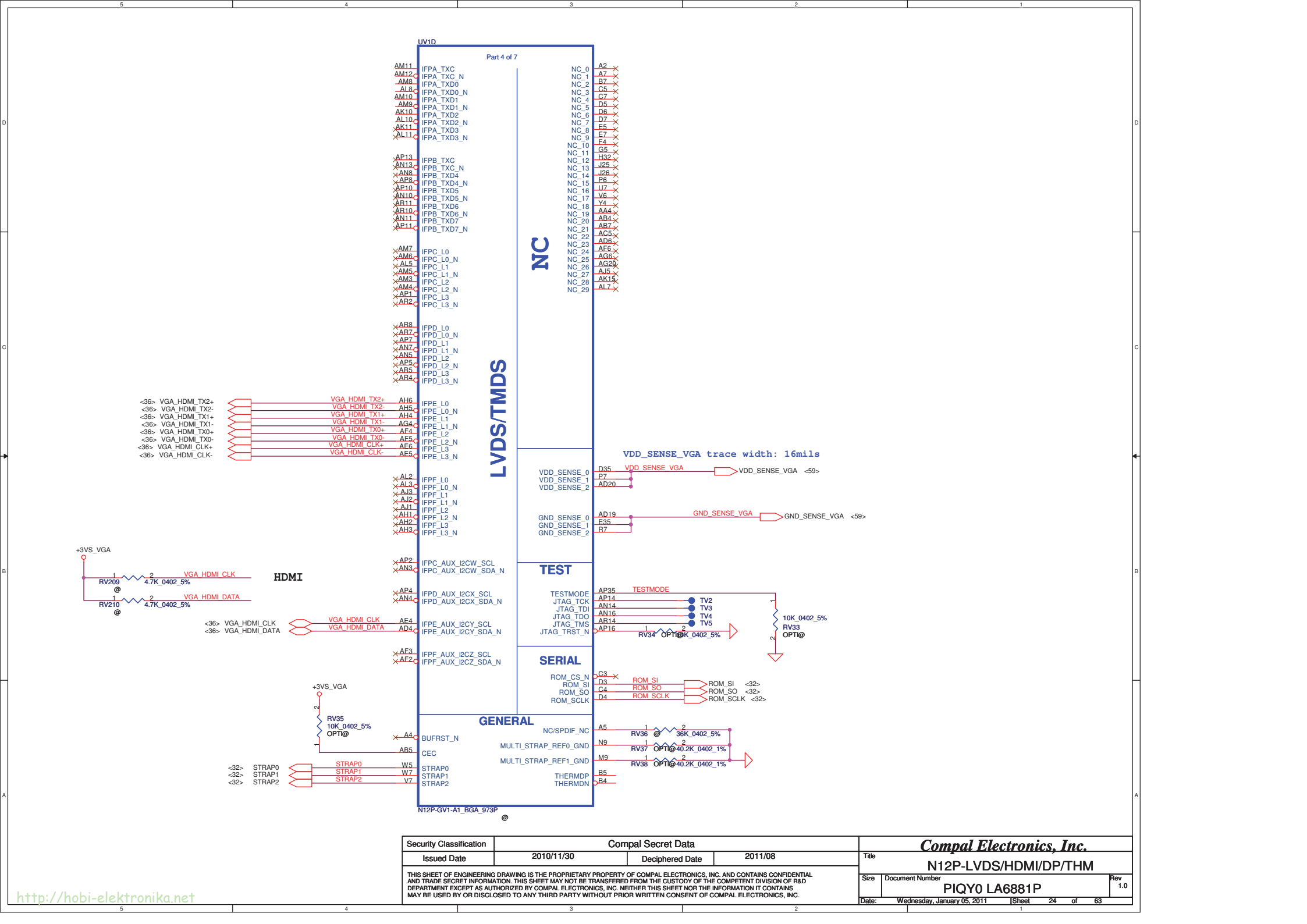


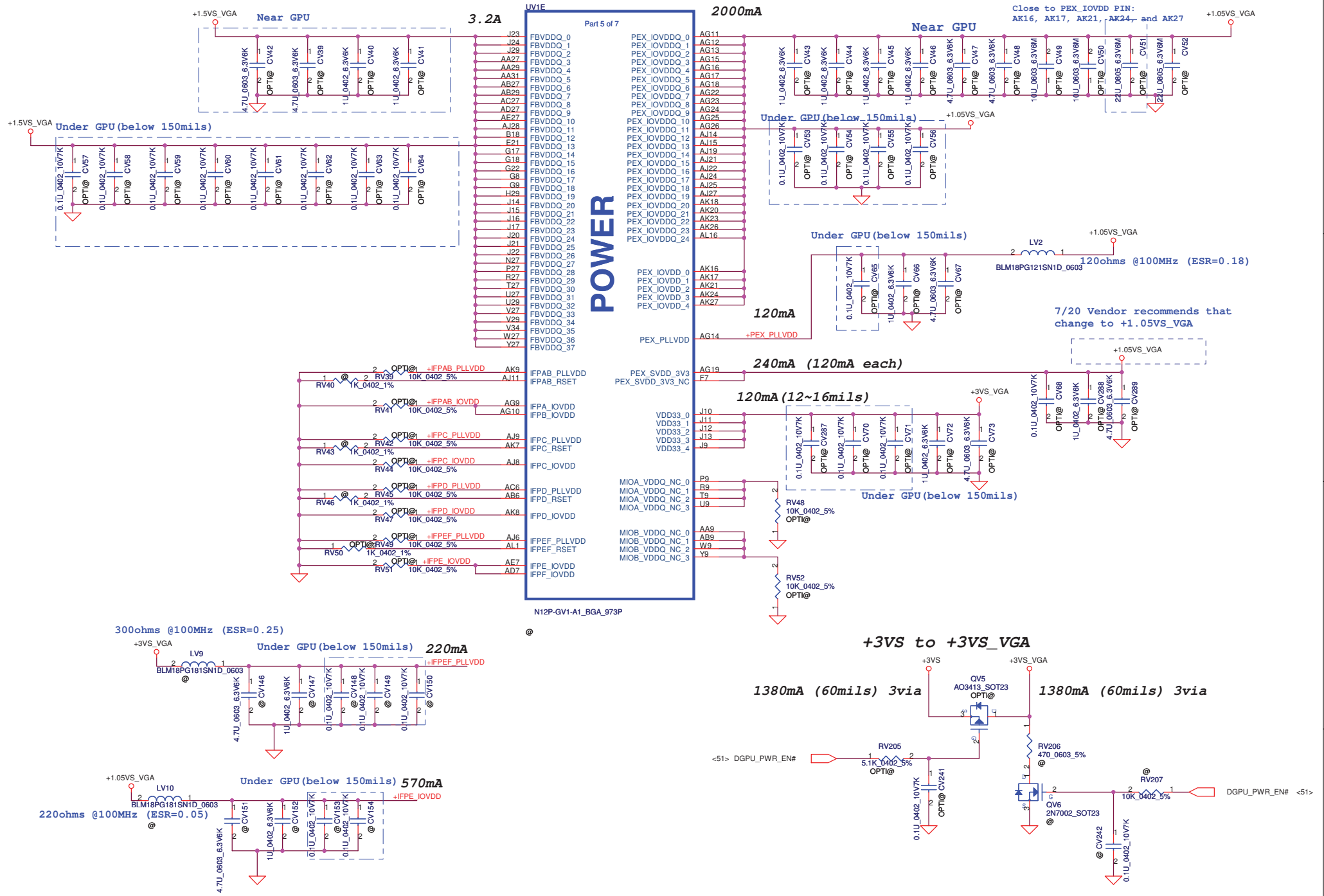






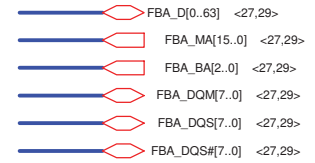
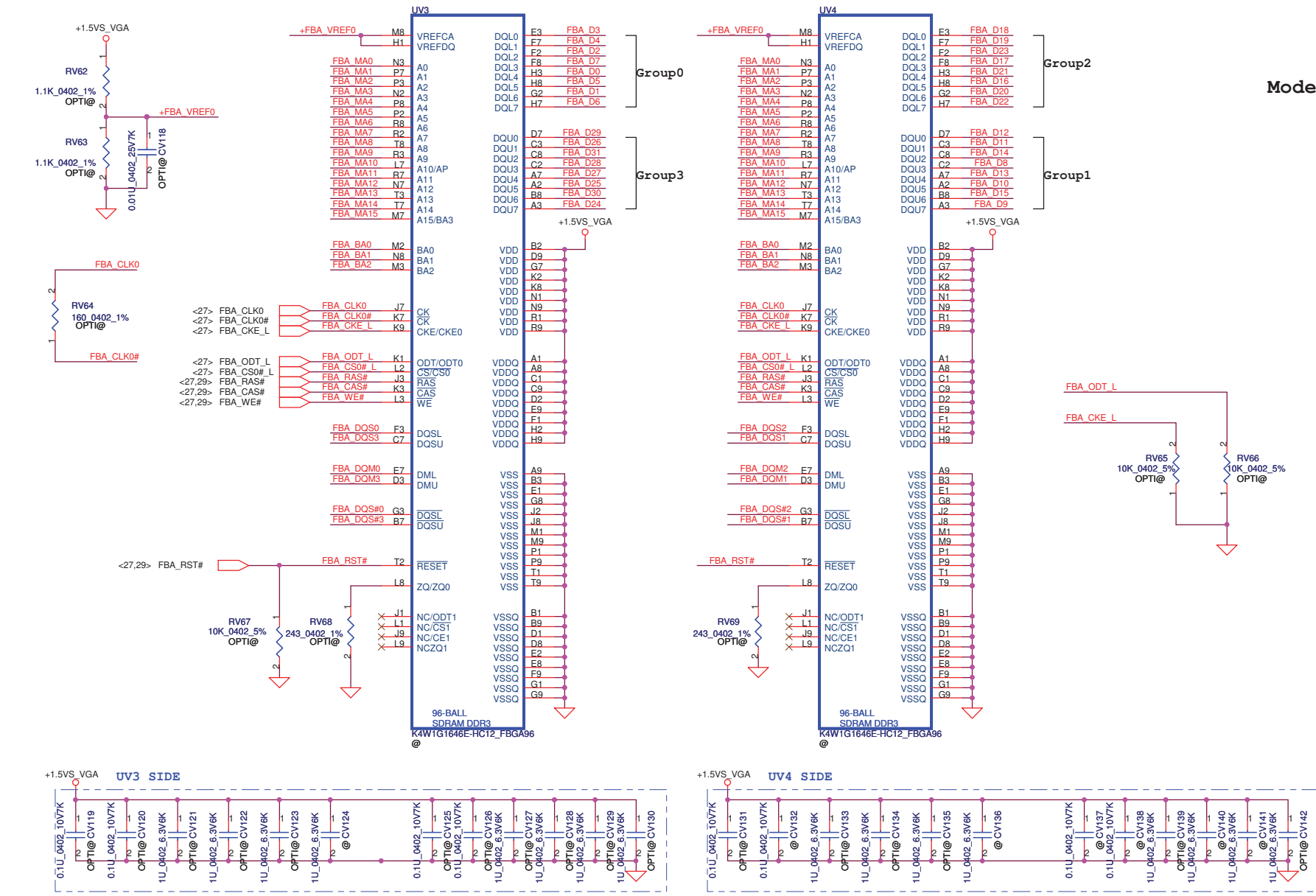
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				Rev 1.0

Memory Partition A - Lower 32 bits



Mode D - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification

Issued Date

2010/11/30

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Compal Electronics, Inc.

Title

N12P-VRAM A Lower

Size

Document Number

PIQY0 LA6881P

Rev

1.0

Date

Wednesday, January 05, 2011

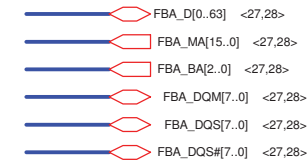
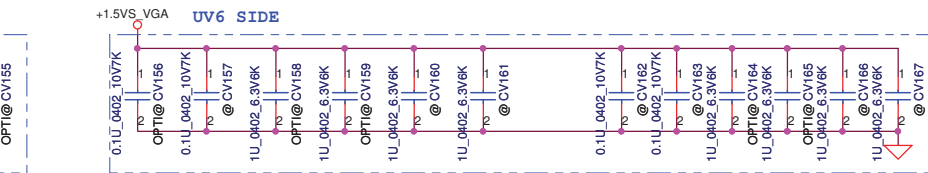
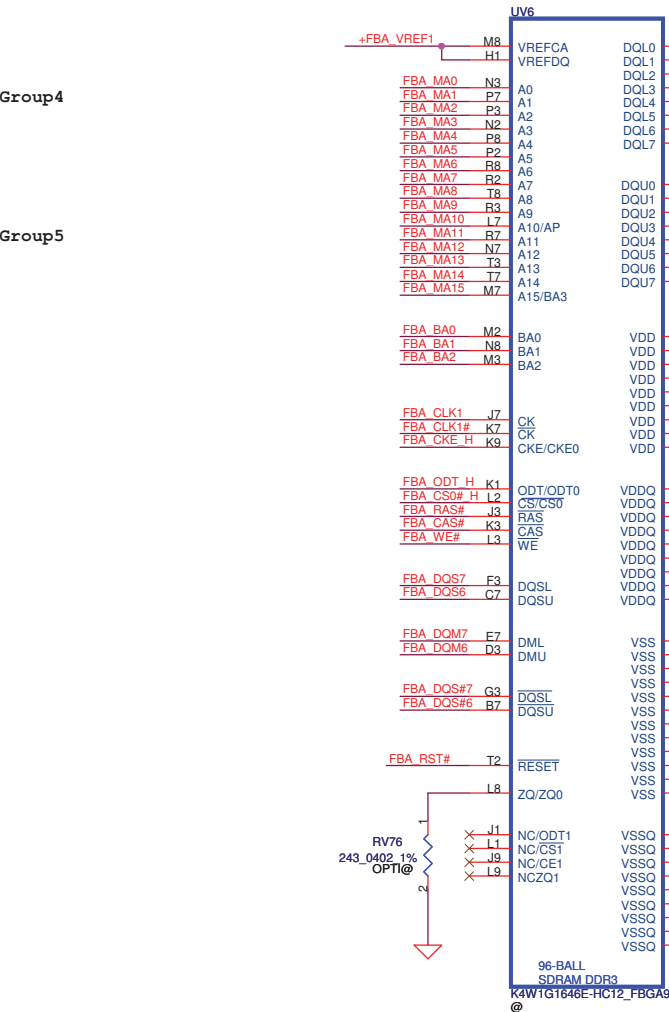
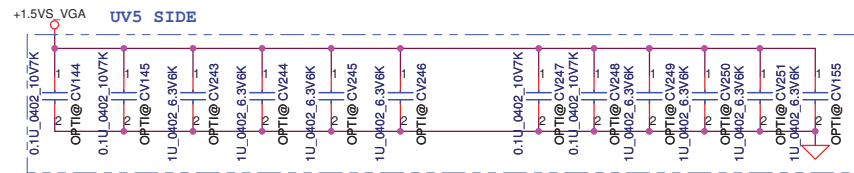
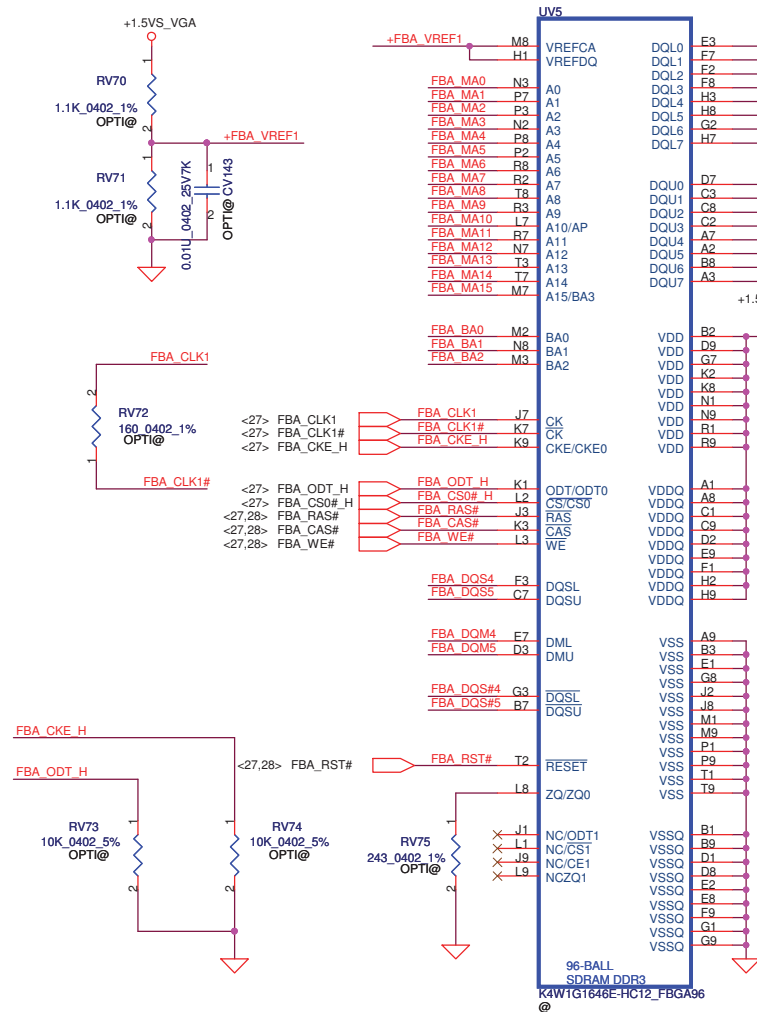
Sheet

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of

63

Memory Partition A - Upper 32 bits

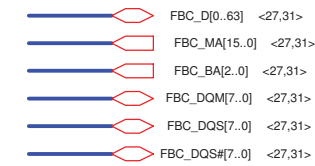
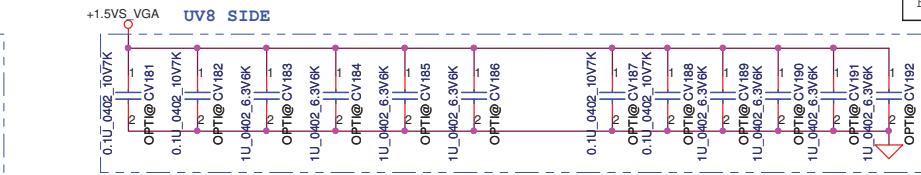
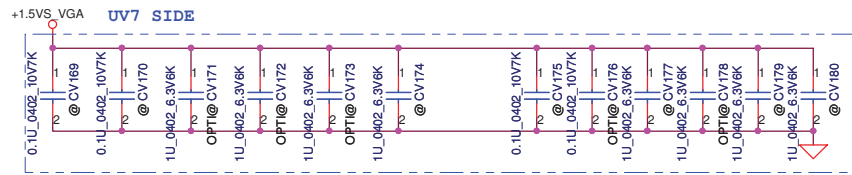


Mode D - Mirror Mode Mapping

Address	DATA Bus
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14
FBx_CMD5	RST
FBx_CMD6	A9
FBx_CMD7	A7
FBx_CMD8	A2
FBx_CMD9	A0
FBx_CMD10	A4
FBx_CMD11	A1
FBx_CMD12	BA0
FBx_CMD13	WE#
FBx_CMD14	A15
FBx_CMD15	CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13
FBx_CMD21	A8
FBx_CMD22	A6
FBx_CMD23	A11
FBx_CMD24	A5
FBx_CMD25	A3
FBx_CMD26	BA2
FBx_CMD27	BA1
FBx_CMD28	A12
FBx_CMD29	A10
FBx_CMD30	RAS#

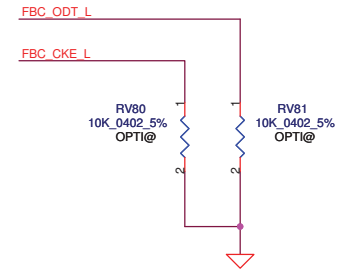
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Issued Date	2010/11/30	N12P-VRAM A Upper	
Deciphered Date	2011/08	PIQY0 LA6881P	
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		Date:	Wednesday, January 05, 2011
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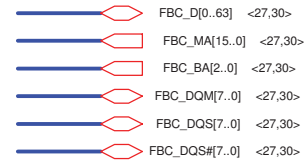
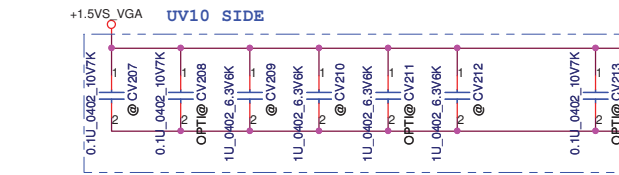
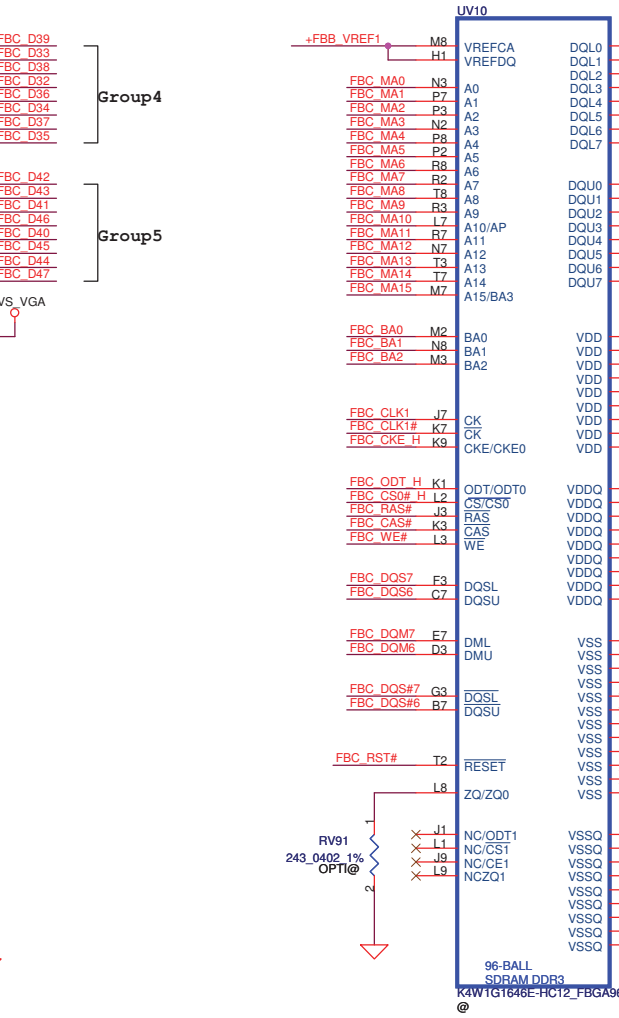
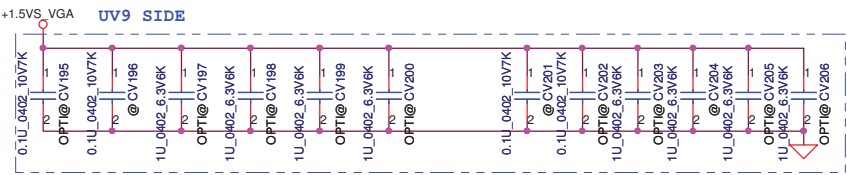
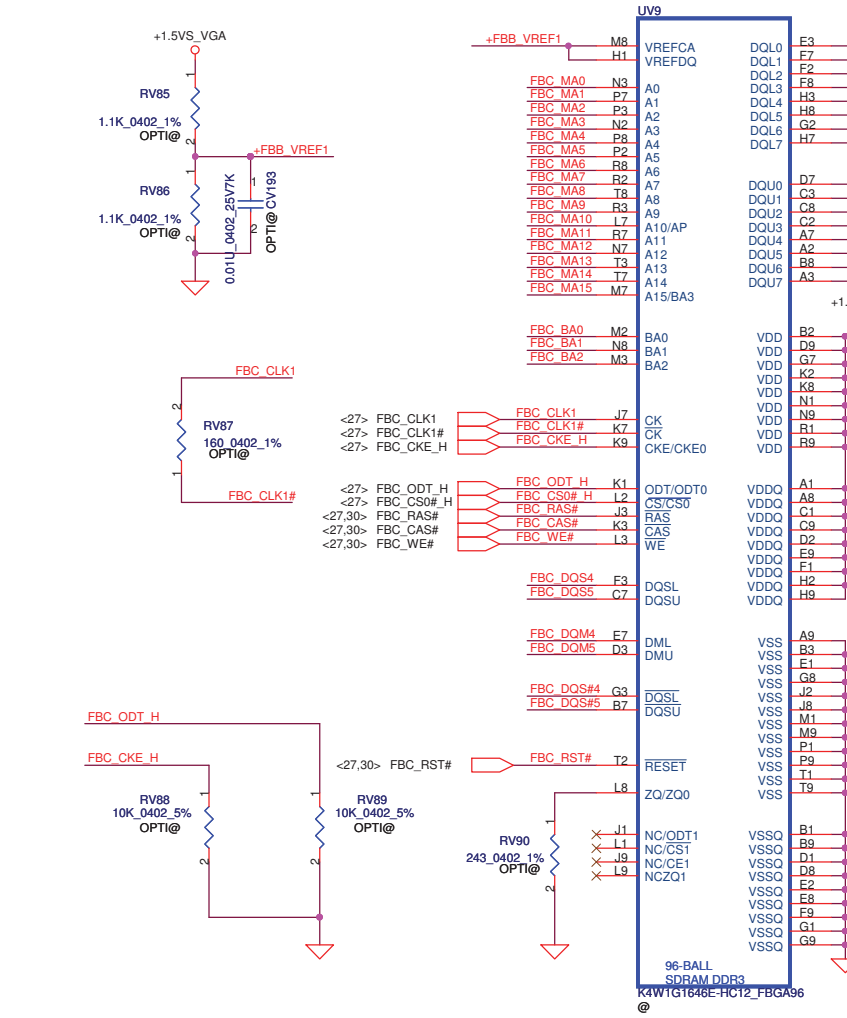
Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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Memory Partition C - Upper 32 bits



Mode D - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14
FBx_CMD5	RST
FBx_CMD6	A9
FBx_CMD7	A7
FBx_CMD8	A2
FBx_CMD9	A0
FBx_CMD10	A4
FBx_CMD11	A1
FBx_CMD12	BA0
FBx_CMD13	WE#
FBx_CMD14	A15
FBx_CMD15	CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13
FBx_CMD21	A8
FBx_CMD22	A6
FBx_CMD23	A11
FBx_CMD24	A5
FBx_CMD25	A3
FBx_CMD26	BA2
FBx_CMD27	BA1
FBx_CMD28	A12
FBx_CMD29	A10
FBx_CMD30	RAS#

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Size

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Date

Wednesday, January 05, 2011

Compal Electronics, Inc.

N12P-VRAM C Upper

PIQY0 LA6881P

Rev

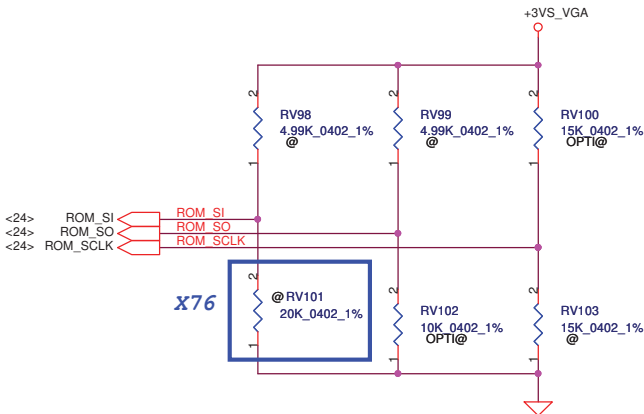
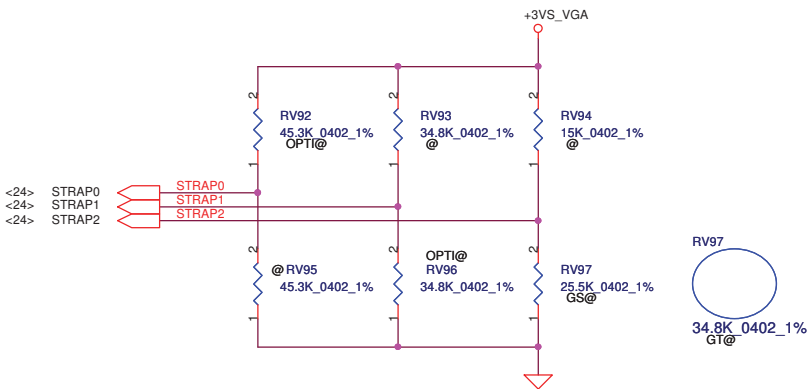
1.0

Sheet

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ROM_SO : PD-10K
 ROM_SCLK : PH-15K
 ROM_SI : PD20K (Samsung)
 Strap 2 : N12P-GS, PD-25K,
 N12P-GT, PD35K,
 Strap 1 : PD-35K
 Strap 0 : PH-45K

	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GT	0x0DF6	Pull up 15K	Pull down 35K

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_VGA	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

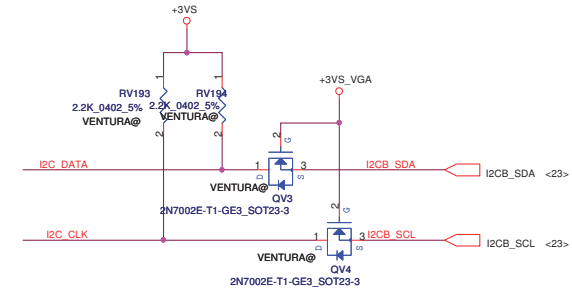
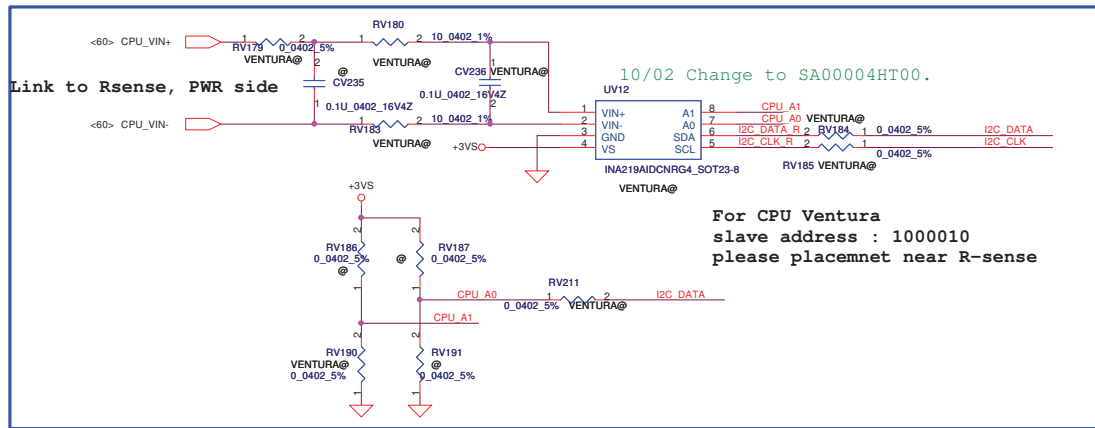
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

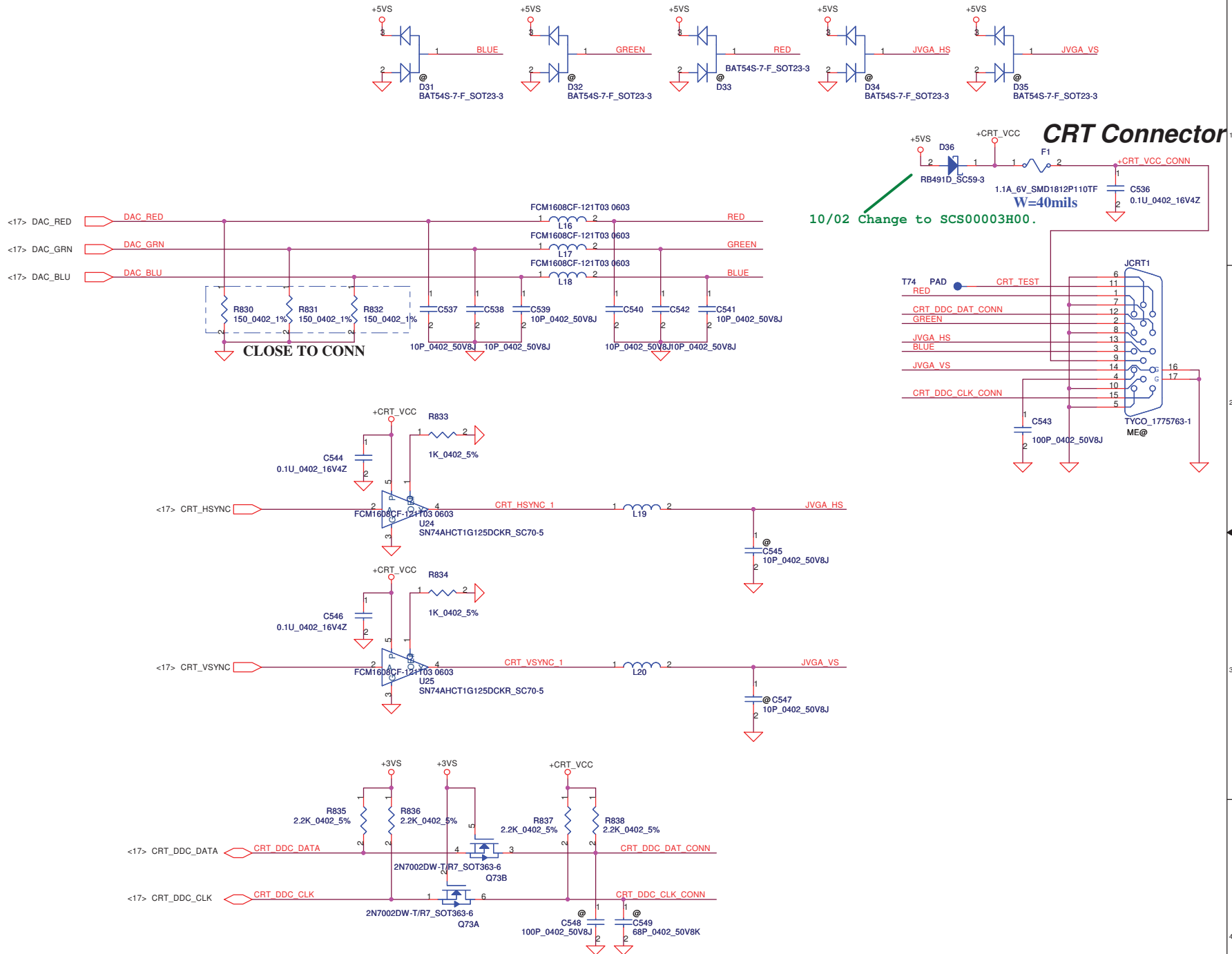
Hynix H5TQ1G63BFR-12C	64Mx16	0010	PD 15K	SA000041S30
	128Mx16	0110	PD 35K	SA00003Y000
Samsung K4W1G1646E-HC12	64Mx16	0011	PD 20K	SA000041T10
	128Mx16	0111	PD 45K	SA000047Q10

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				Size Custom	Document Number	Rev
				PIQY0 LA6881P		1.0
Date:		Wednesday, January 05, 2011		Sheet	32	of 63

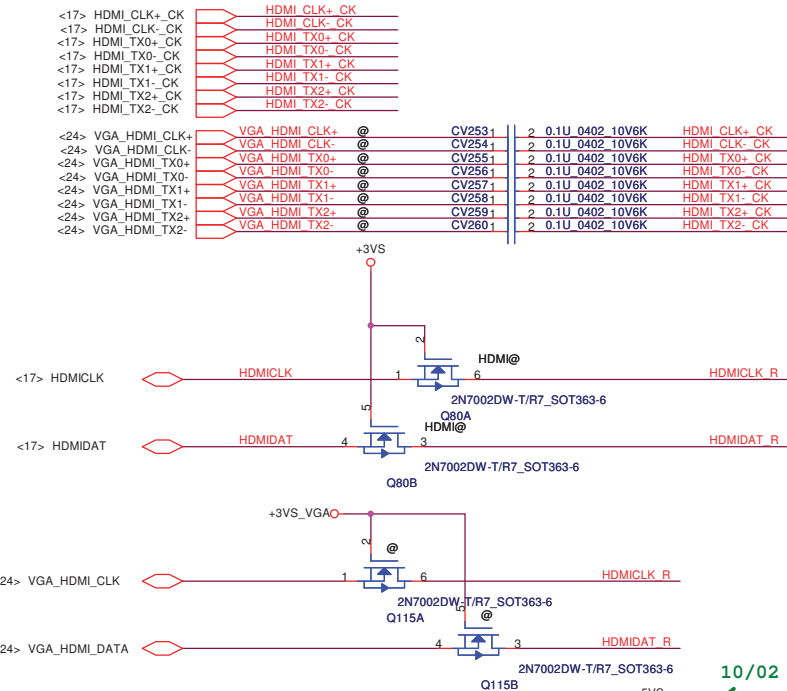
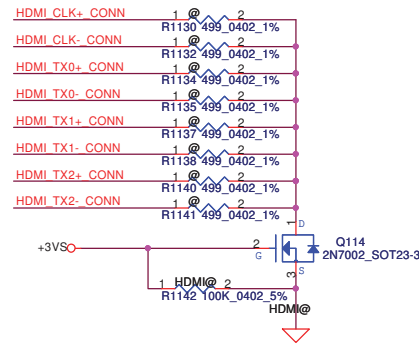
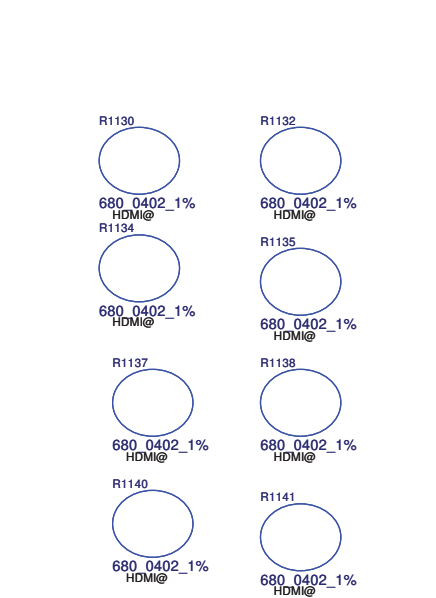
TOP side (under inductor)



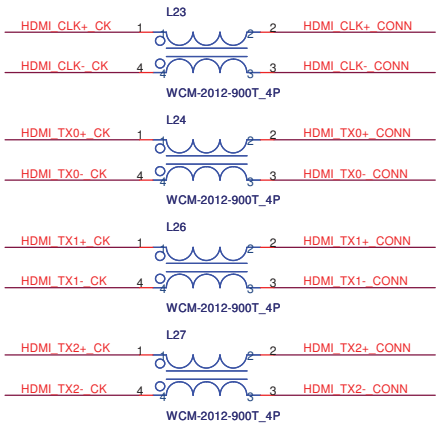
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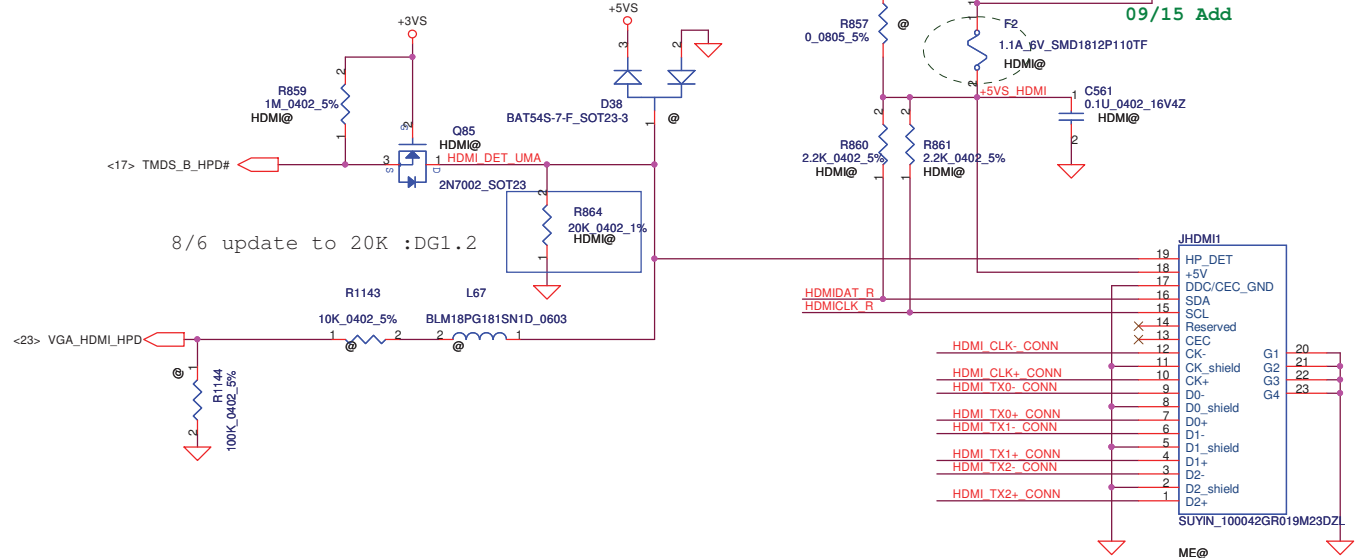
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DVT, Change to SM070000I00 for EMI request.



HDMI CLK+ CK	R855	1	2	0	0402_5%	HDMI CLK+ CONN
HDMI CLK- CK	R856	1	2	0	0402_5%	HDMI CLK- CONN
HDMI TX0+ CK	R867	1	2	0	0402_5%	HDMI TX0+ CONN
HDMI TX0- CK	R868	1	2	0	0402_5%	HDMI TX0- CONN
HDMI TX1+ CK	R869	1	2	0	0402_5%	HDMI TX1+ CONN
HDMI TX1- CK	R870	1	2	0	0402_5%	HDMI TX1- CONN
HDMI TX2+ CK	R871	1	2	0	0402_5%	HDMI TX2+ CONN
HDMI TX2- CK	R872	1	2	0	0402_5%	HDMI TX2- CONN



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				Deciphered Date				HDMI CONN			
				2011/08				Size			
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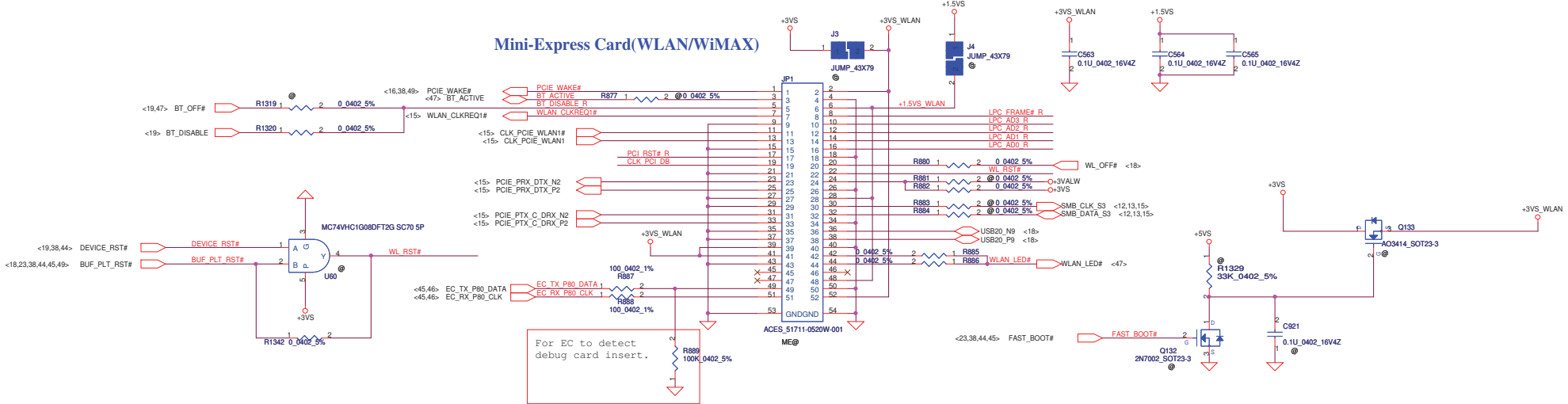
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Mini-Express Card for WLAN/WiMAX(Half) Mini-Express Card for SSD(Full)

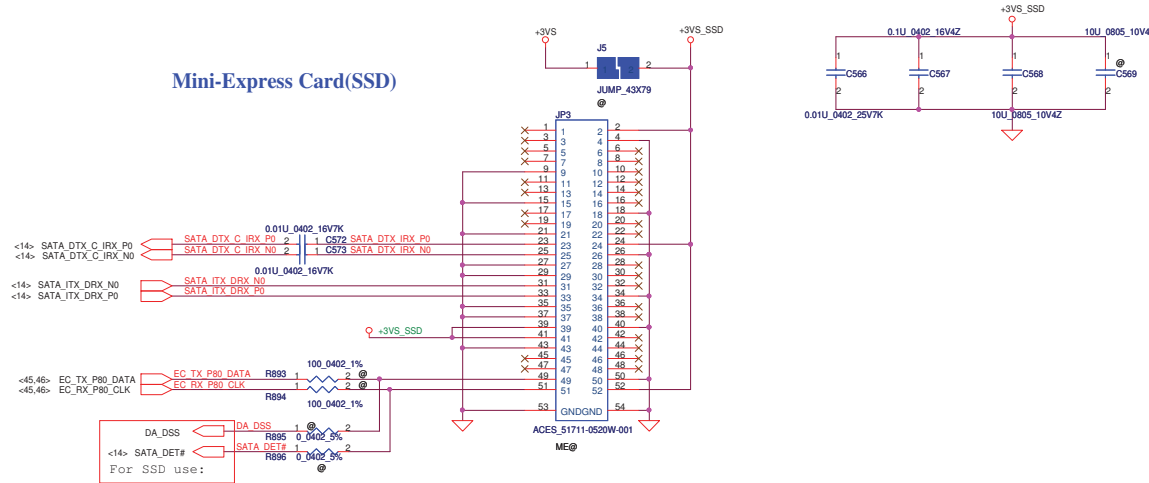
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R873	1	2	0.0402_5%	LPC_FRAME#	LPC_FRAME#	<14,45>
LPC_AD3 R	R874	1	2	0.0402_5%	LPC_AD3	LPC_AD3	<14,45>
LPC_AD2 R	R875	1	2	0.0402_5%	LPC_AD2	LPC_AD2	<14,45>
LPC_AD1 R	R876	1	2	0.0402_5%	LPC_AD1	LPC_AD1	<14,45>
LPC_AD0 R	R877	1	2	0.0402_5%	LPC_AD0	LPC_AD0	<14,45>
RST# R	R878	1	2	0.0402_5%	BUF_PLT_RST#	CLK_PCI_DB	<15>

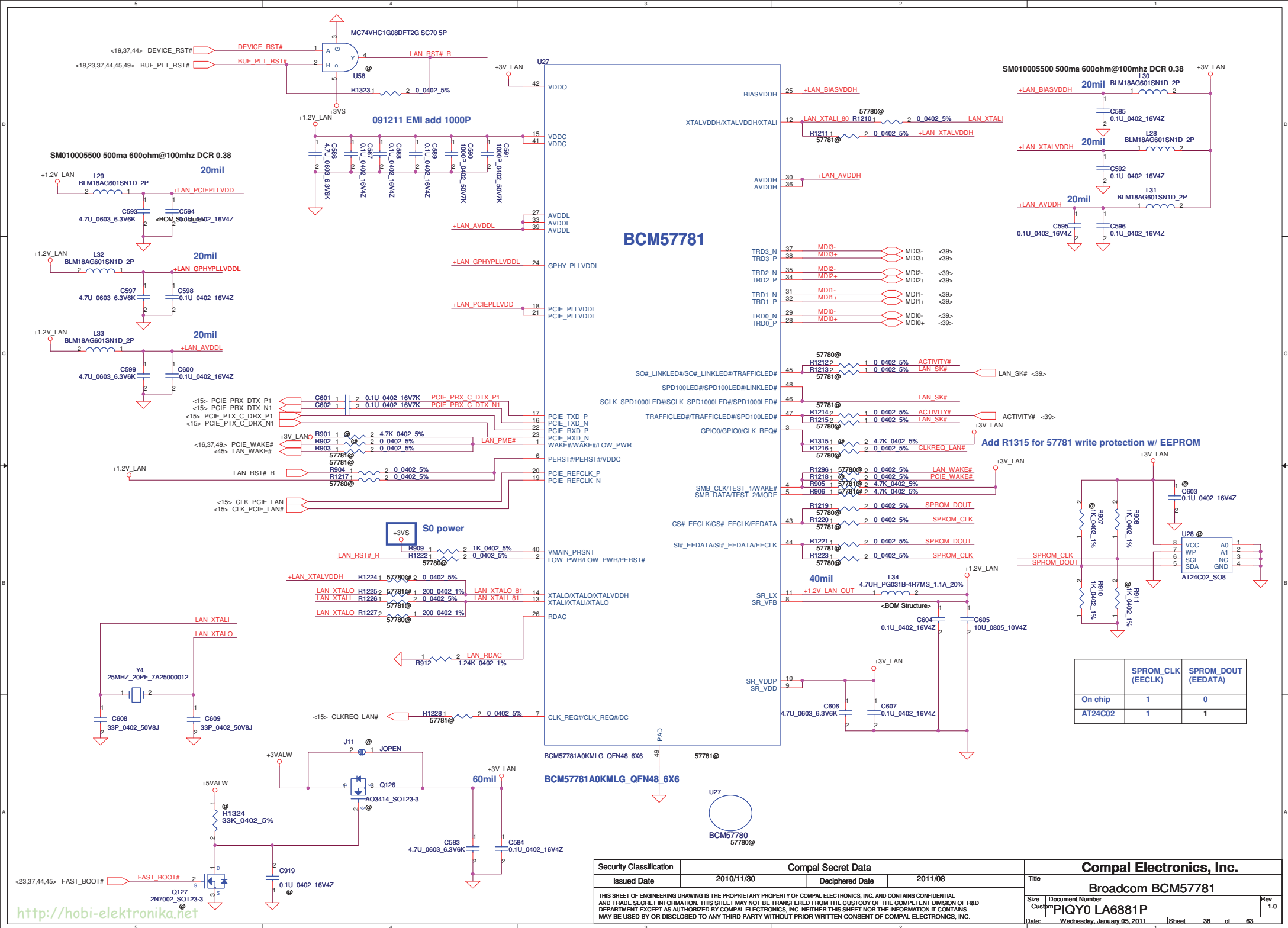


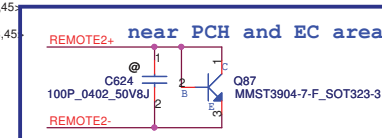
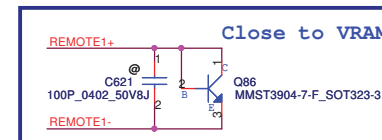
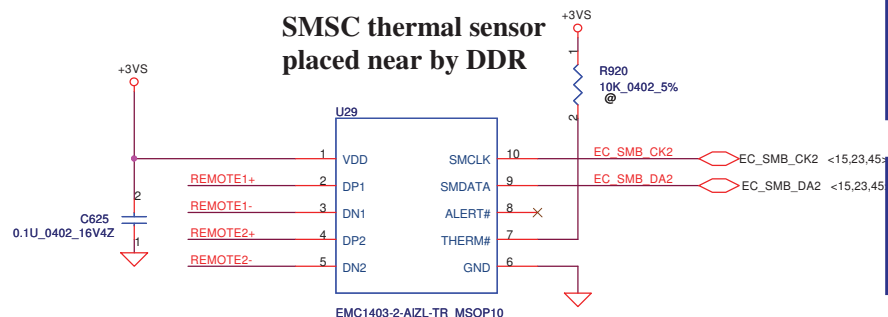
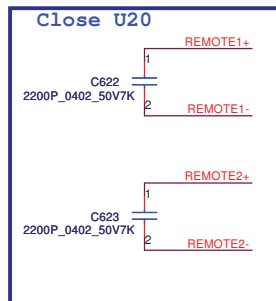
SSD Active:0.22W(0.06A)

Mini-Express Card(SSD)



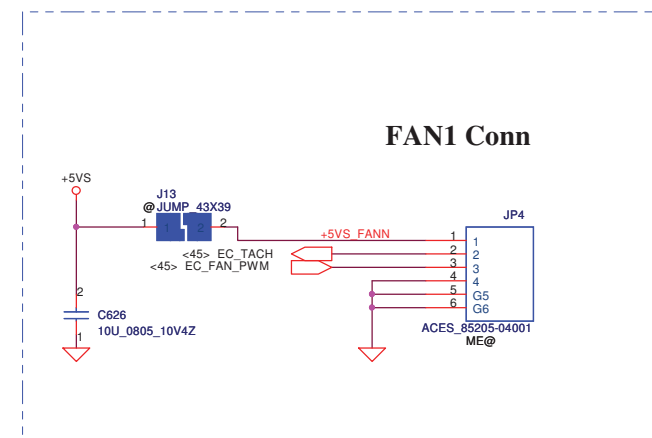
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REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Address 1001_101xb
8/02 Change PN to SA000046C00, Fintek.



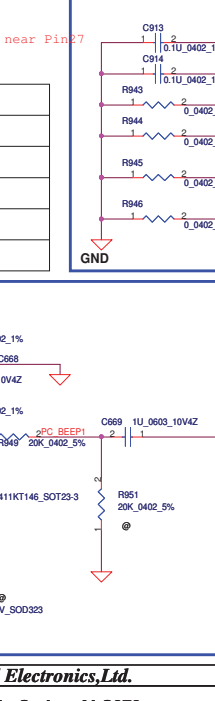
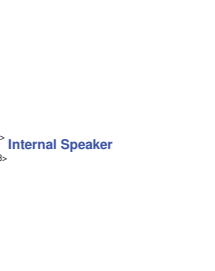
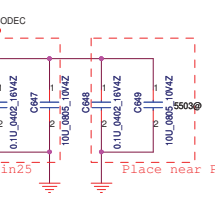
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				Sheet 40 of 63	Rev 1.0

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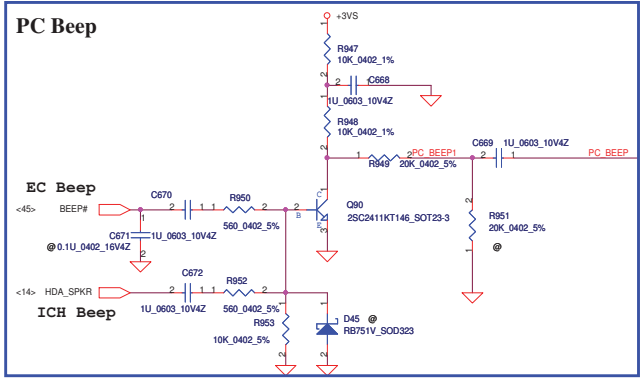
The schematic diagram illustrates the internal wiring of the SATA to SATA-Express adapter. It shows the connection between the SATA connector (left) and the SATA-Express connector (right). The SATA connector has pins for SATA_ITX_DRX_P2_CONN, SATA_ITX_DRX_N2_CONN, SATA_DTX_C_IRX_N2, and SATA_DTX_C_IRX_P2. The SATA-Express connector has pins for GND, A+, A-, B, B+, GND, DP, +5V, +5V, MD, GND, GND, and GND. The diagram includes components such as resistors R710, R711, R712, R713, R714, R715, R716, R717, R718, R719, R720, R721, R722, R723, R724, R725, R726, R727, R728, R729, R730, R731, R732, R733, R734, R735, R736, R737, R738, R739, R740, R741, R742, R743, R744, R745, R746, R747, R748, R749, R750, R751, R752, R753, R754, R755, R756, R757, R758, R759, R760, R761, R762, R763, R764, R765, R766, R767, R768, R769, R770, R771, R772, R773, R774, R775, R776, R777, R778, R779, R780, R781, R782, R783, R784, R785, R786, R787, R788, R789, R790, R791, R792, R793, R794, R795, R796, R797, R798, R799, R800, R801, R802, R803, R804, R805, R806, R807, R808, R809, R810, R811, R812, R813, R814, R815, R816, R817, R818, R819, R820, R821, R822, R823, R824, R825, R826, R827, R828, R829, R830, R831, R832, R833, R834, R835, R836, R837, R838, R839, R840, R841, R842, R843, R844, R845, R846, R847, R848, R849, R850, R851, R852, R853, R854, R855, R856, R857, R858, R859, R860, R861, R862, R863, R864, R865, R866, R867, R868, R869, R870, R871, R872, R873, R874, R875, R876, R877, R878, R879, R880, R881, R882, R883, R884, R885, R886, R887, R888, R889, R890, R891, R892, R893, R894, R895, R896, R897, R898, R899, R900, R901, R902, R903, R904, R905, R906, R907, R908, R909, R910, R911, R912, R913, R914, R915, R916, R917, R918, R919, R920, R921, R922, R923, R924, R925, R926, R927, R928, R929, R930, R931, R932, R933, R934, R935, R936, R937, R938, R939, R940, R941, R942, R943, R944, R945, R946, R947, R948, R949, R950, R951, R952, R953, R954, R955, R956, R957, R958, R959, R960, R961, R962, R963, R964, R965, R966, R967, R968, R969, R970, R971, R972, R973, R974, R975, R976, R977, R978, R979, R980, R981, R982, R983, R984, R985, R986, R987, R988, R989, R990, R991, R992, R993, R994, R995, R996, R997, R998, R999, R1000, R1001, R1002, R1003, R1004, R1005, R1006, R1007, R1008, R1009, R1010, R1011, R1012, R1013, R1014, R1015, R1016, R1017, R1018, R1019, R1020, R1021, R1022, R1023, R1024, R1025, R1026, R1027, R1028, R1029, R1030, R1031, R1032, R1033, R1034, R1035, R1036, R1037, R1038, R1039, R1040, R1041, R1042, R1043, R1044, R1045, R1046, R1047, R1048, R1049, R1050, R1051, R1052, R1053, R1054, R1055, R1056, R1057, R1058, R1059, R1060, R1061, R1062, R1063, R1064, R1065, R1066, R1067, R1068, R1069, R1070, R1071, R1072, R1073, R1074, R1075, R1076, R1077, R1078, R1079, R1080, R1081, R1082, R1083, R1084, R1085, R1086, R1087, R1088, R1089, R1090, R1091, R1092, R1093, R1094, R1095, R1096, R1097, R1098, R1099, R1100, R1101, R1102, R1103, R1104, R1105, R1106, R1107, R1108, R1109, R1110, R1111, R1112, R1113, R1114, R1115, R1116, R1117, R1118, R1119, R1120, R1121, R1122, R1123, R1124, R1125, R1126, R1127, R1128, R1129, R1130, R1131, R1132, R1133, R1134, R1135, R1136, R1137, R1138, R1139, R1140, R1141, R1142, R1143, R1144, R1145, R1146, R1147, R1148, R1149, R1150, R1151, R1152, R1153, R1154, R1155, R1156, R1157, R1158, R1159, R1160, R1161, R1162, R1163, R1164, R1165, R1166, R1167, R1168, R1169, R1170, R1171, R1172, R1173, R1174, R1175, R1176, R1177, R1178, R1179, R1180, R1181, R1182, R1183, R1184, R1185, R1186, R1187, R1188, R1189, R1190, R1191, R1192, R1193, R1194, R1195, R1196, R1197, R1198, R1199, R1200, R1201, R1202, R1203, R1204, R1205, R1206, R1207, R1208, R1209, R1210, R1211, R1212, R1213, R1214, R1215, R1216, R1217, R1218, R1219, R1220, R1221, R1222, R1223, R1224, R1225, R1226, R1227, R1228, R1229, R1230, R1231, R1232, R1233, R1234, R1235, R1236, R1237, R1238, R1239, R1240, R1241, R1242, R1243, R1244, R1245, R1246, R1247, R1248, R1249, R1250, R1251, R1252, R1253, R1254, R1255, R1256, R1257, R1258, R1259, R1260, R1261, R1262, R1263, R1264, R1265, R1266, R1267, R1268, R1269, R1270, R1271, R1272, R1273, R1274, R1275, R1276, R1277, R1278, R1279, R1280, R1281, R1282, R1283, R1284, R1285, R1286, R1287, R1288, R1289, R1290, R1291, R1292, R1293, R1294, R1295, R1296, R1297, R1298, R1299, R1300, R1301, R1302, R1303, R1304, R1305, R1306, R1307, R1308, R1309, R1310, R1311, R1312, R1313, R1314, R1315, R1316, R1317, R1318, R1319, R1320, R1321, R1322, R1323, R1324, R1325, R1326, R1327, R1328, R1329, R1330, R1331, R1332, R1333, R1334, R1335, R1336, R1337, R1338, R1339, R1340, R1341, R1342, R1343, R1344, R1345, R1346, R1347, R1348, R1349, R1350, R1351, R1352, R1353, R1354, R1355, R1356, R1357, R1358, R1359, R1360, R1361, R1362, R1363, R1364, R1365, R1366, R1367, R1368, R1369, R1370, R1371, R1372, R1373, R1374, R1375, R1376, R1377, R1378, R1379, R1380, R1381, R1382, R1383, R1384, R1385, R1386, R1387, R1388, R1389, R1390, R1391, R1392, R1393, R1394, R1395, R1396, R1397, R1398, R1399, R1400, R1401, R1402, R1403, R1404, R1405, R1406, R1407, R1408, R1409, R1410, R1411, R1412, R1413, R1414, R

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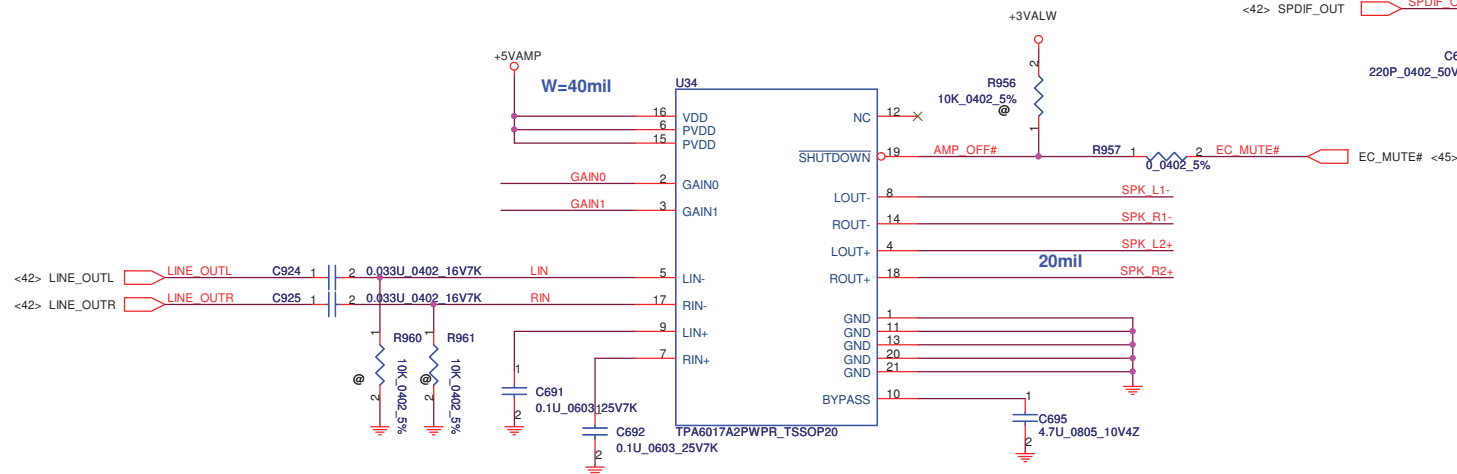
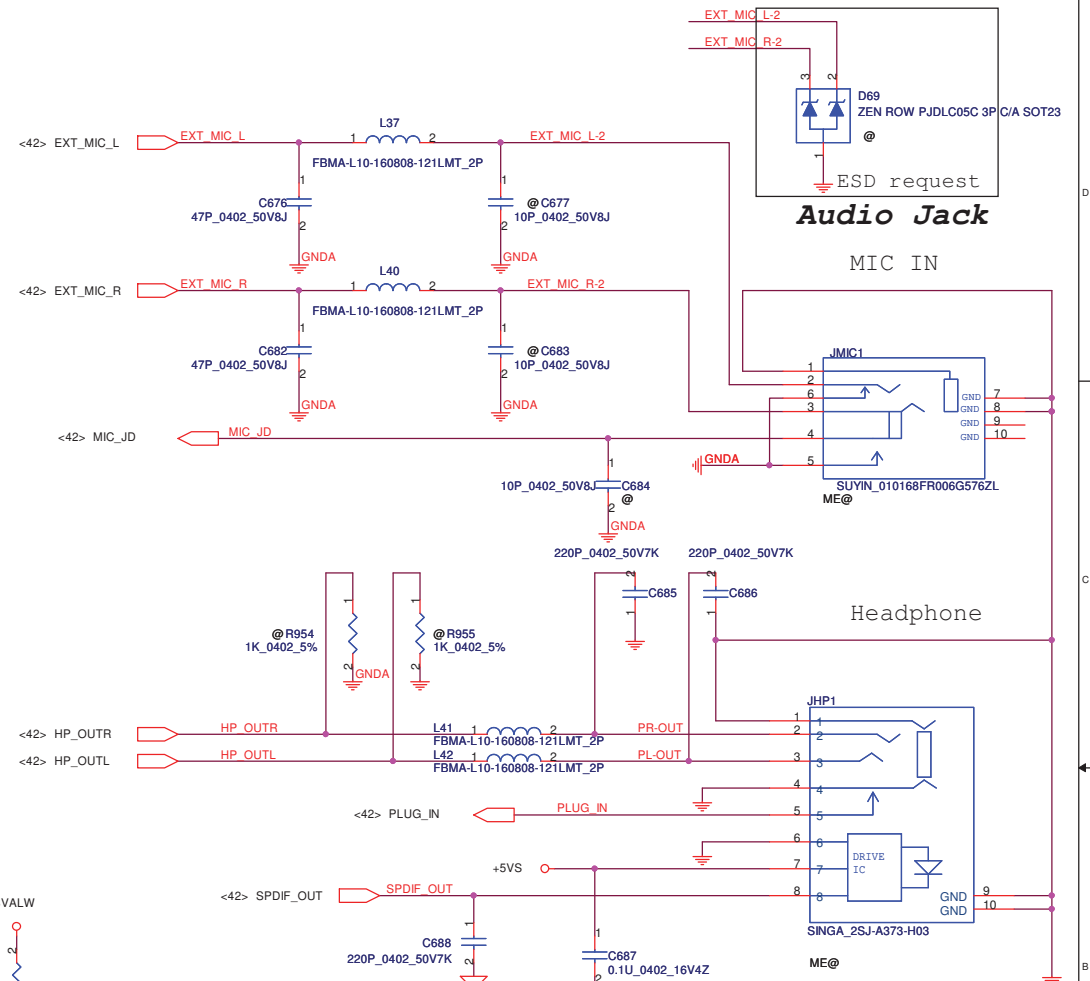
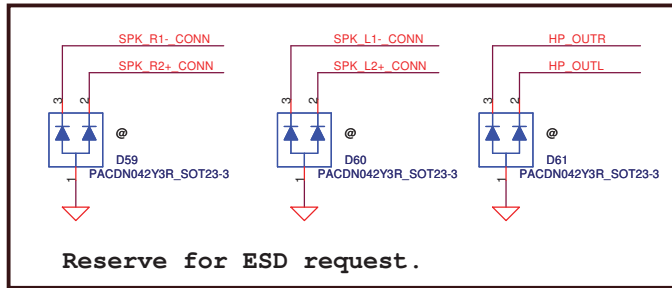
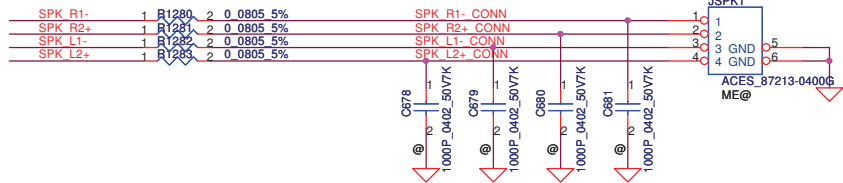
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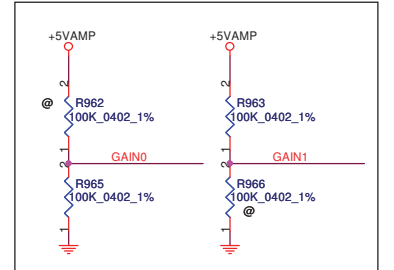
Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1 (Pin21/22)	External	Mic in
MIC2 (Pin16/17)	Internal	Internal Mic



wide 20MIL

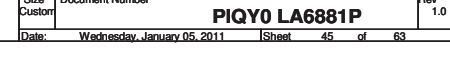
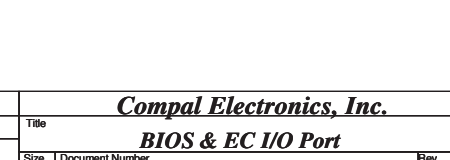
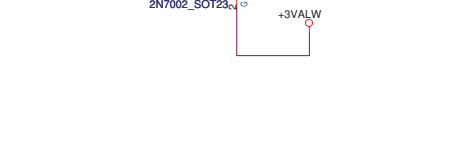
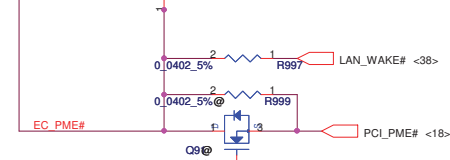
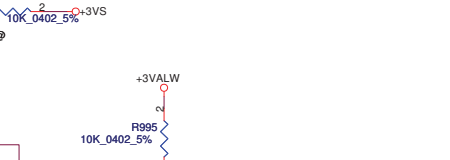
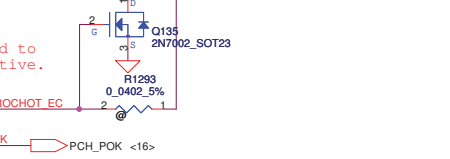
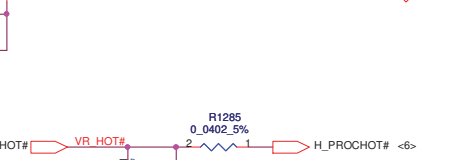
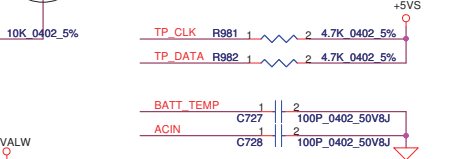
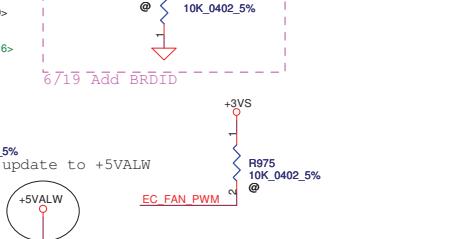
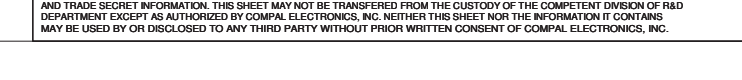
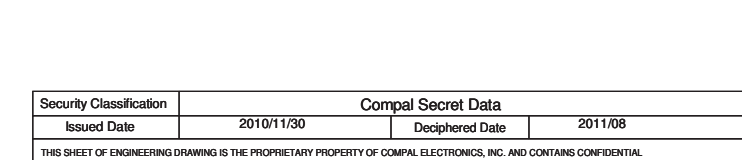
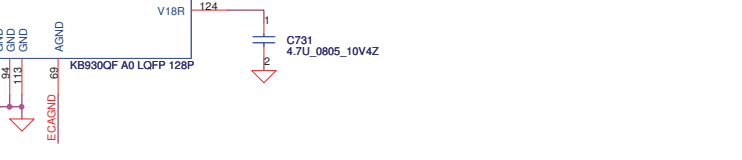
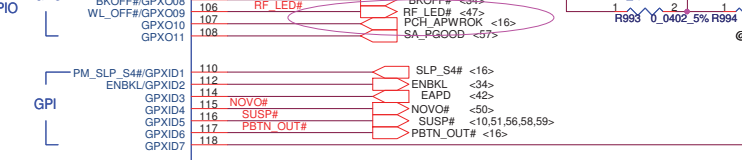
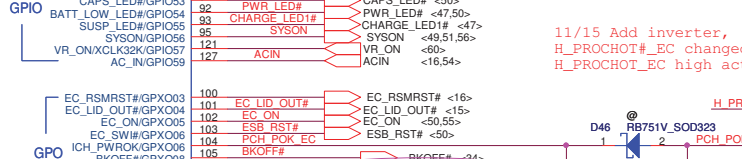
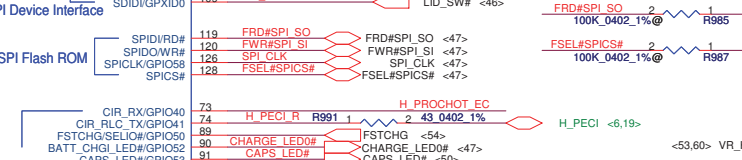
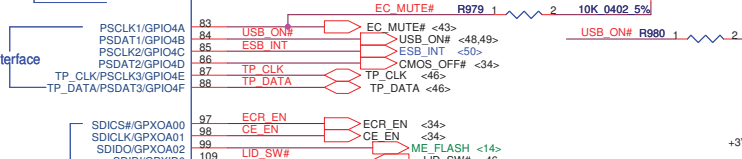
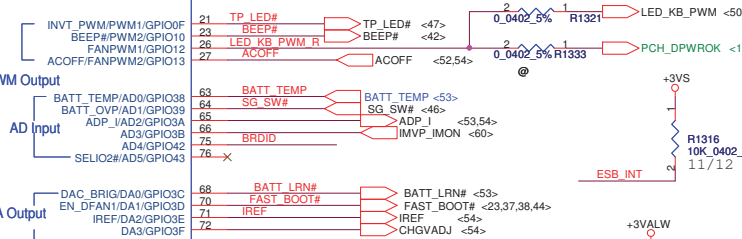
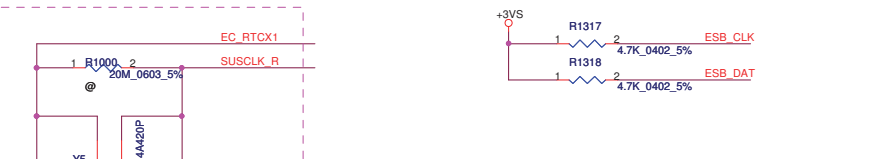
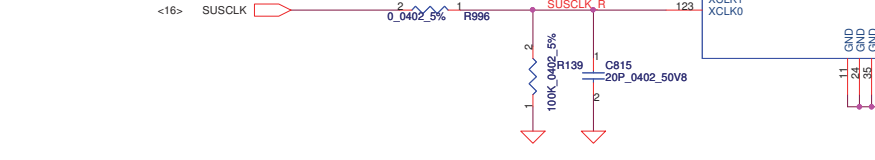
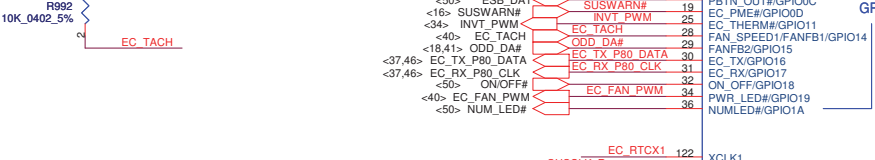
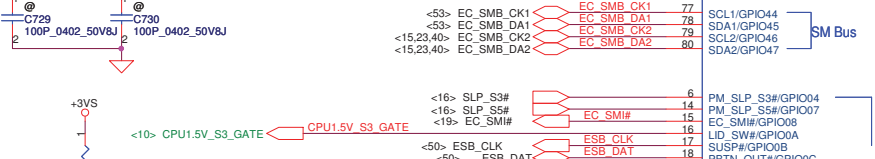
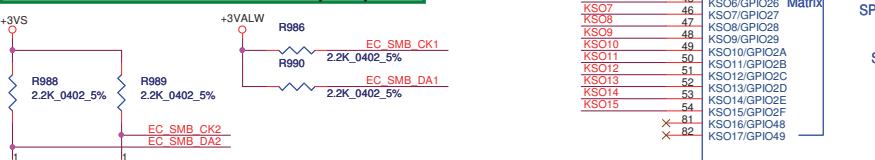
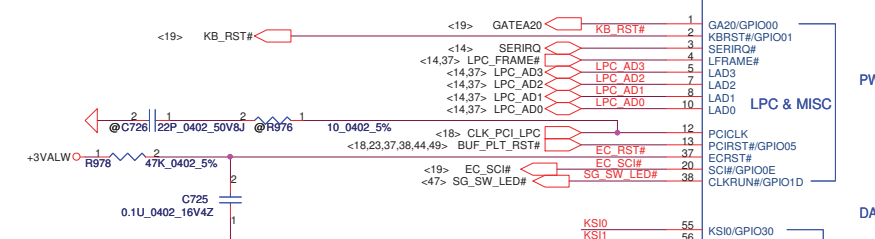


GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



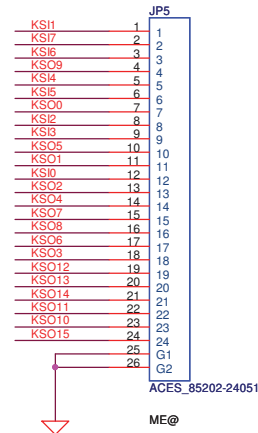
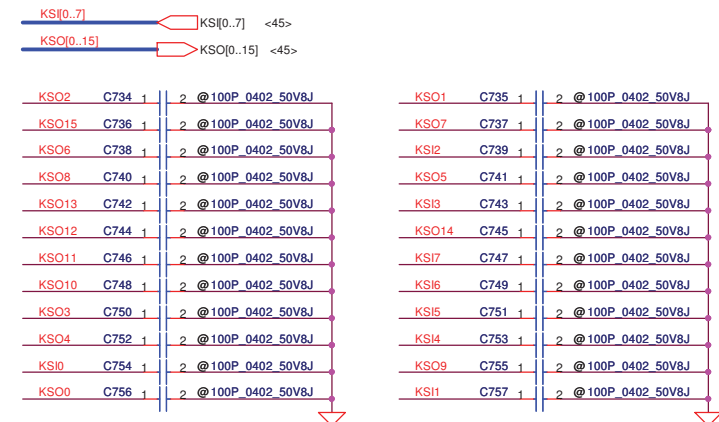
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The schematic diagram illustrates the power supply circuit for the 1000P_0402_50V7K. It features a +3V1W input connected to a network of components. Inductors L43 and L44 are connected in series with the input. Capacitor C721 (0.1U_0402_16V4Z) is connected in parallel to ground (ECAGND). Inductor L44 is connected to the input, and capacitor C722 (1000P_0402_50V7K) is connected in parallel to ground. The output is labeled +EC_AVCC. Other components include capacitors C723, C719, C718, C720, and C724, all connected in parallel to ground. A diode D402 is connected in series with the output. The ground connection is labeled ECAGND.

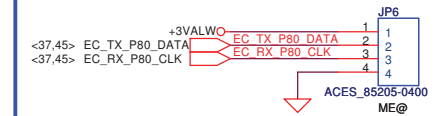


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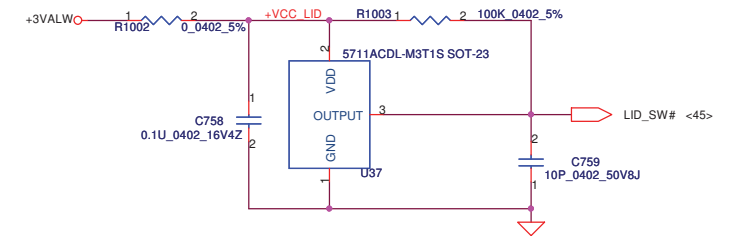
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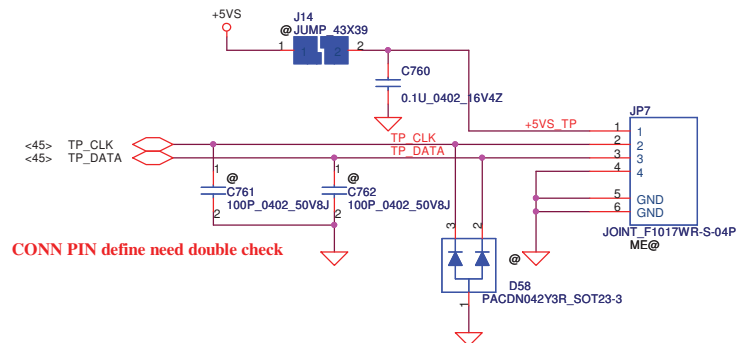
EC DEBUG PORT



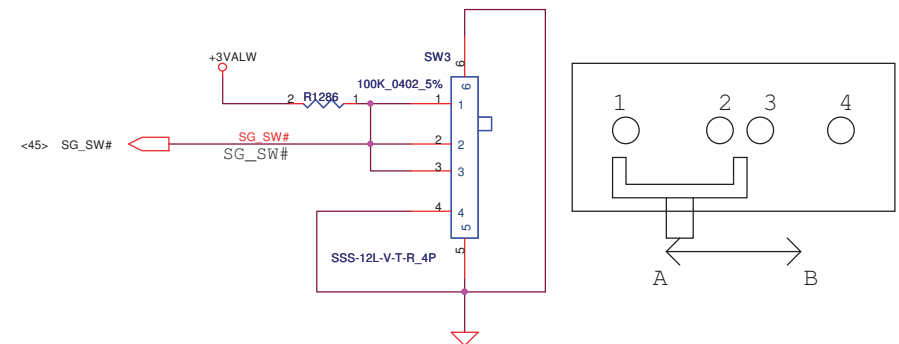
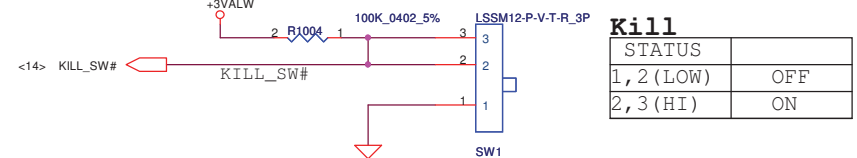
Lid Switch



To TP/B Conn.

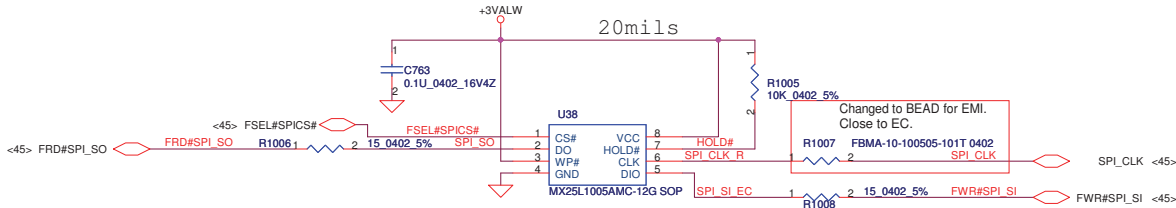


Kill Switch

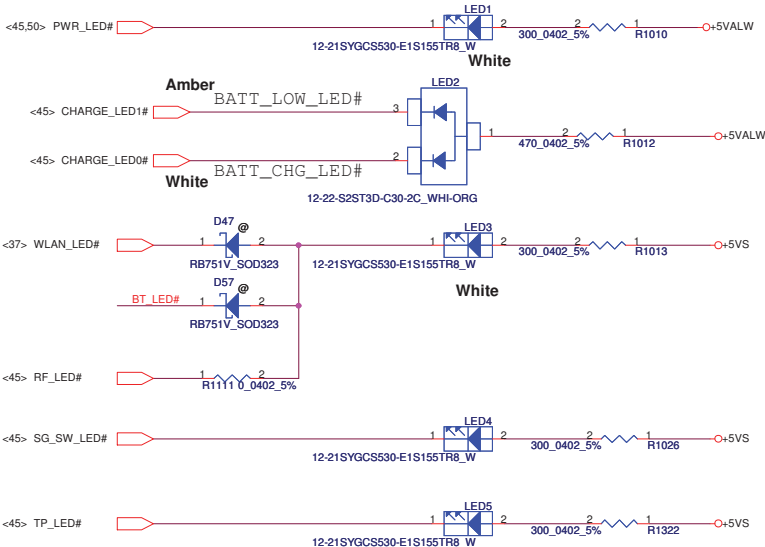


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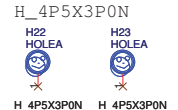
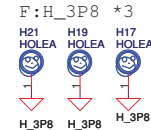
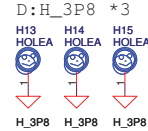
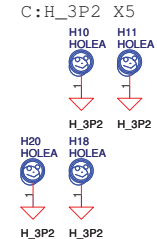
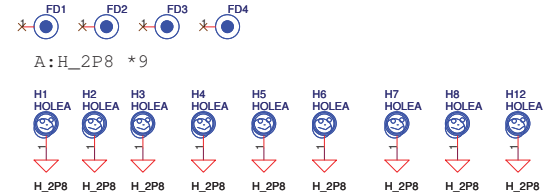
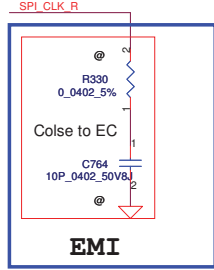
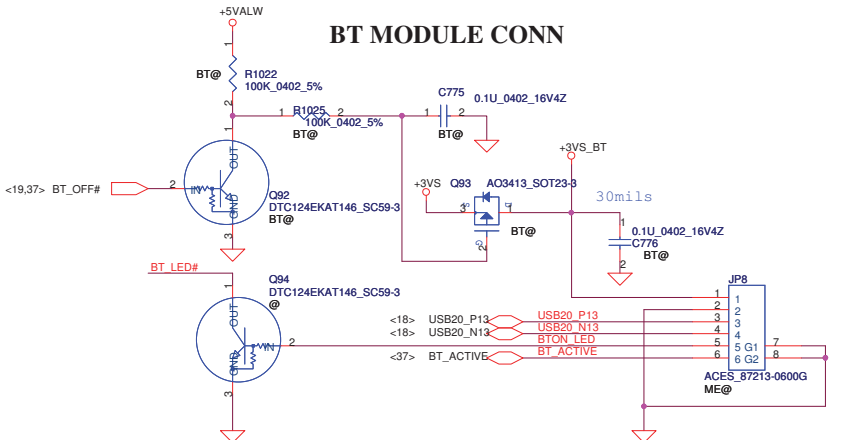
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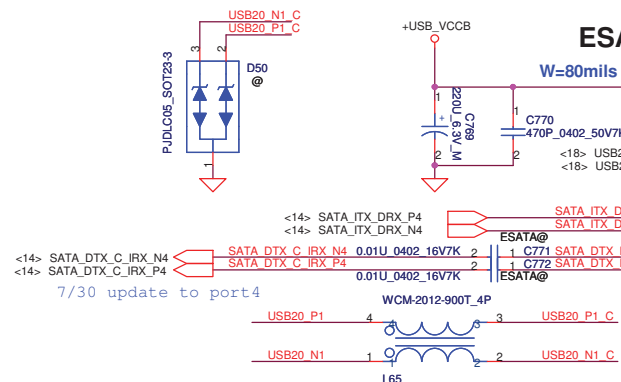
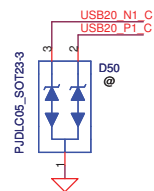
LED



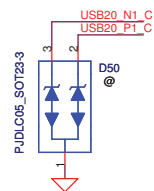
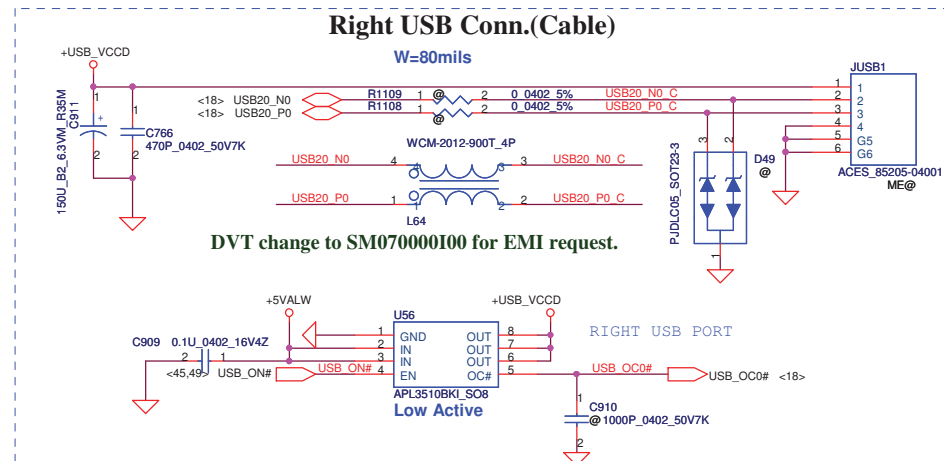
BT MODULE CONN



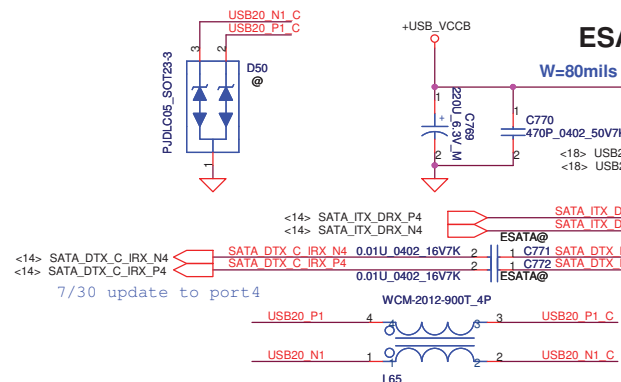
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/11/30	Deciphered Date	2011/08	Title		
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				Size B	Document Number	Rev 1.0
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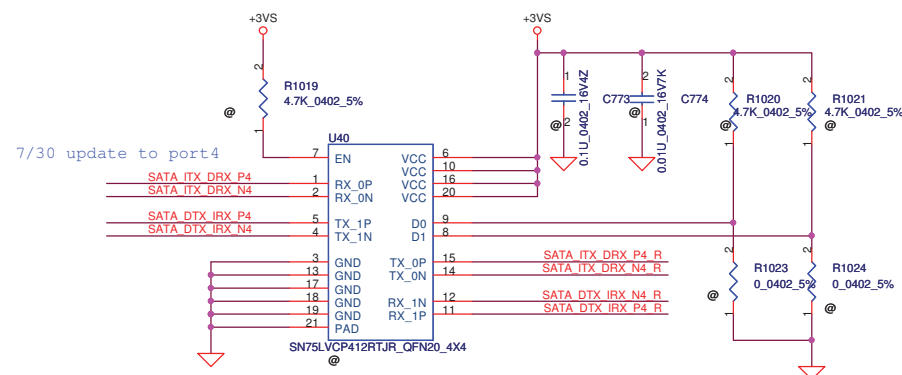
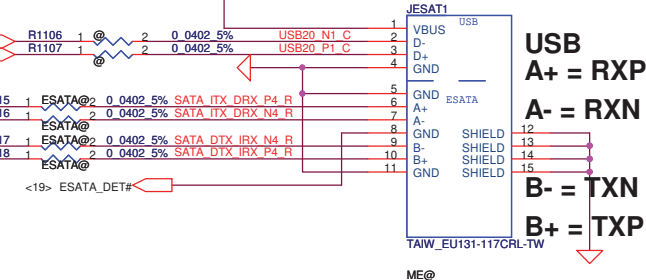
DVT change to SM070000I00 for EMI request.



ESATA and USB Conn.

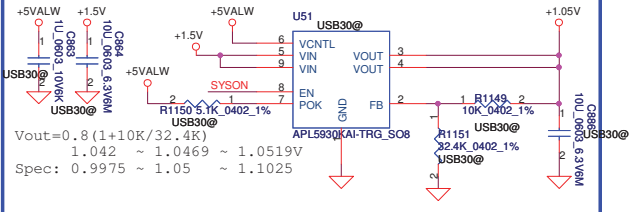


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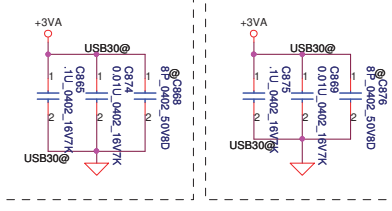
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Issued Date	2010/11/30	Deciphered Date	2011/08	Title USB ports/E-SATA			
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				Custom	PIQY0 LA6881P	1.0	
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+1.5V to +1.05V Transfer

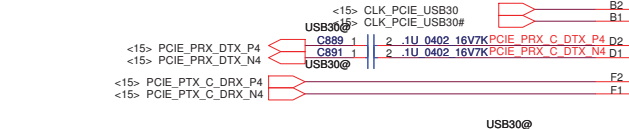
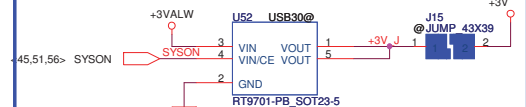


Close to U3.D7

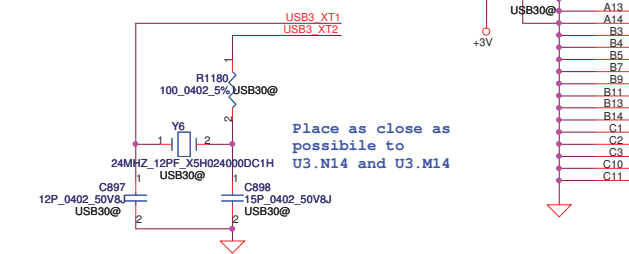
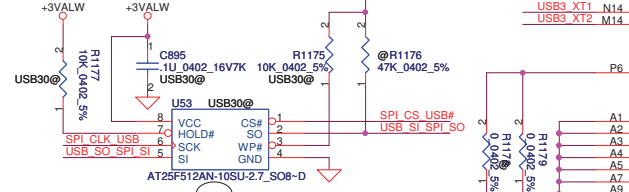
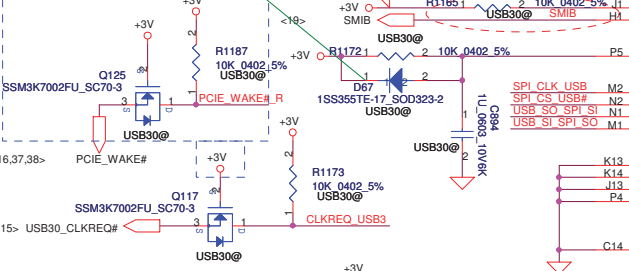
Close to U3.P13



+3VALW to +3V Transfer



10/02 Change to SC100001K00.
 7/30 update



Pin compare table for support USB remote wakeup or not

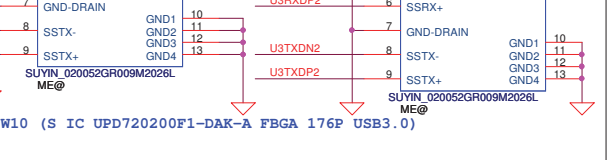
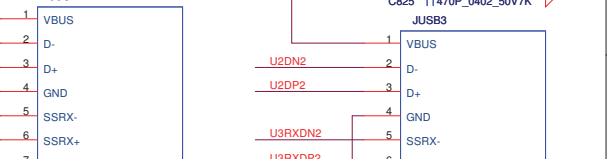
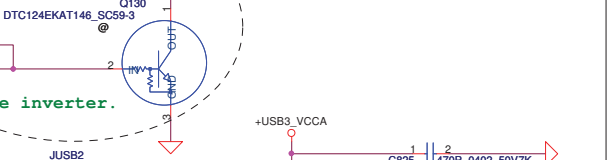
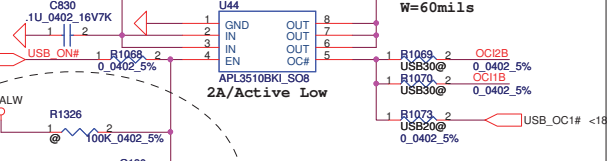
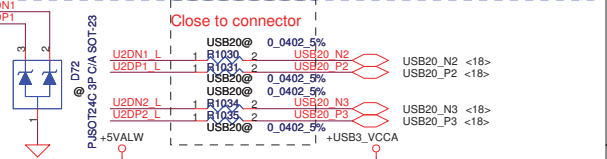
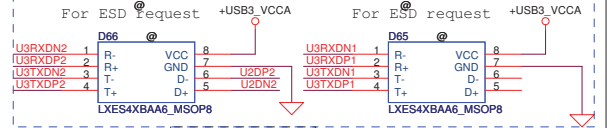
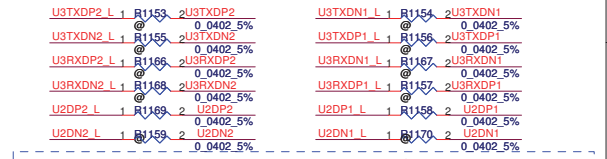
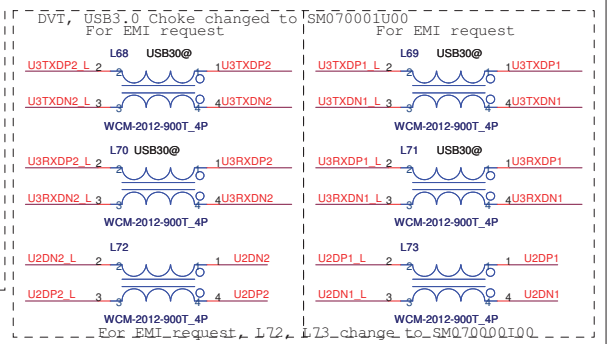
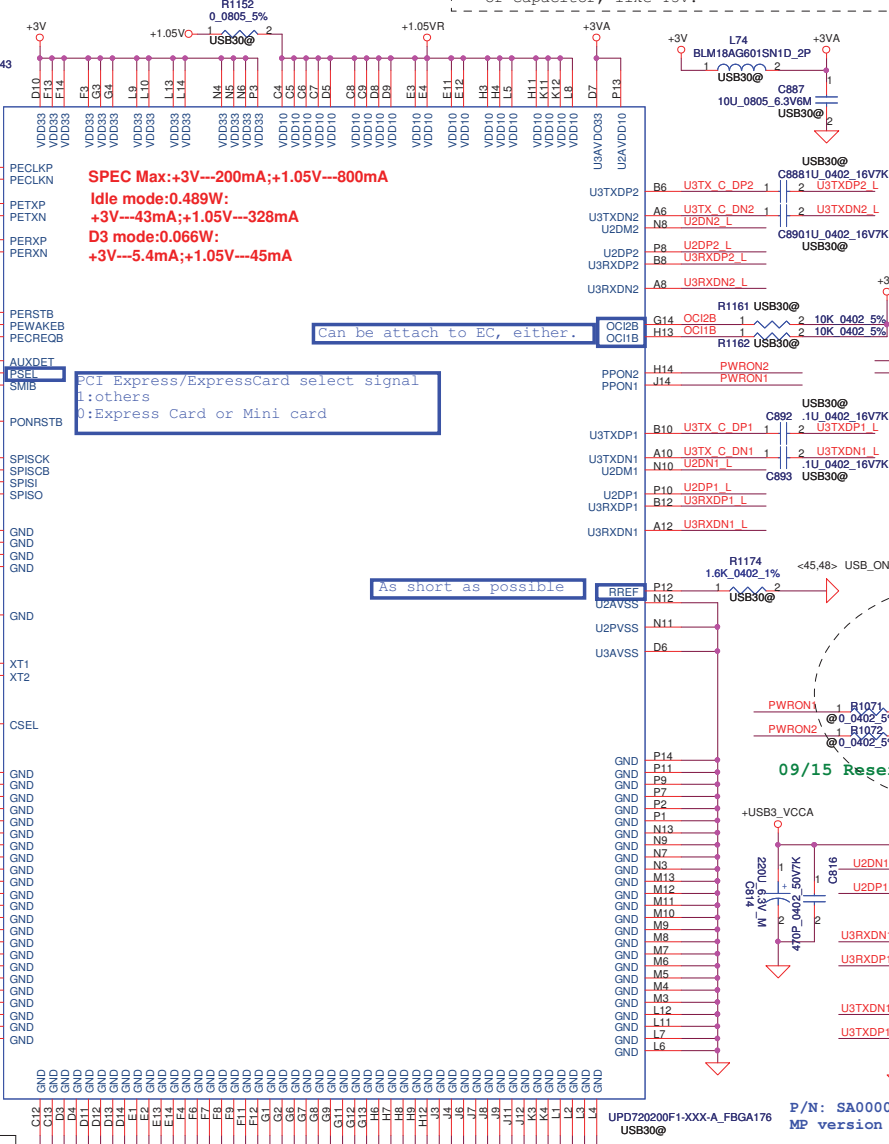
	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

SPEC Max: +3V---200mA; +1.05V---800mA
 Idle mode: 0.489W;
 +3V---43mA; +1.05V---328mA
 D3 mode: 0.066W;
 +3V---5.4mA; +1.05V---45mA

PCI Express/ExpressCard select signal
 1: others
 0: Express Card or Mini card

Can be attach to EC, either.

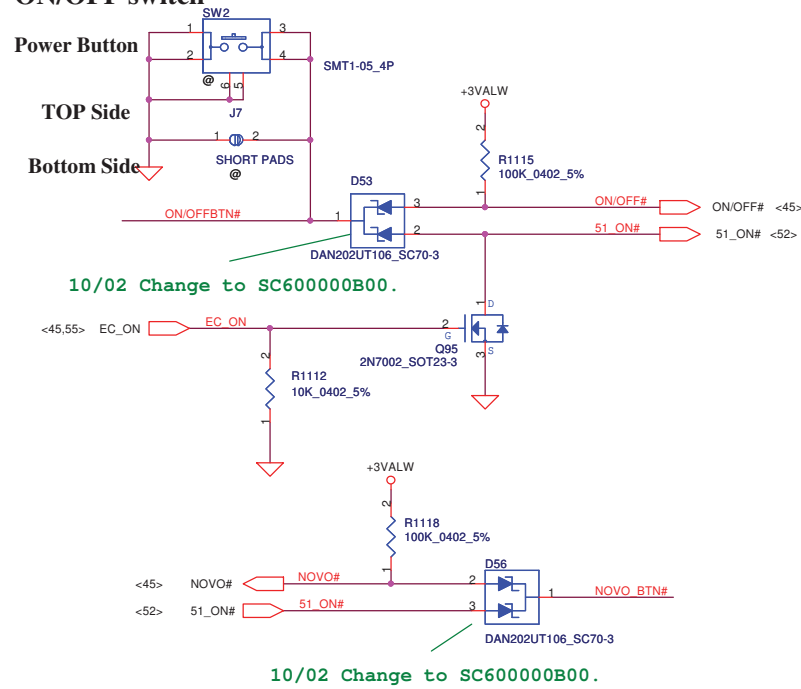
As short as possible



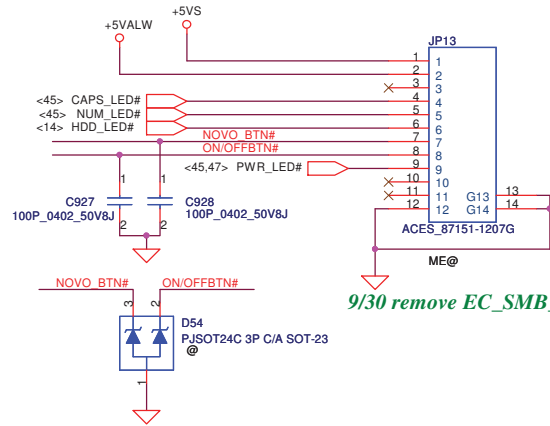
P/N: SA00033W10 (S IC UPD720200F1-DAK-A FBGA 176P USB3.0) MP version

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ON/OFF switch

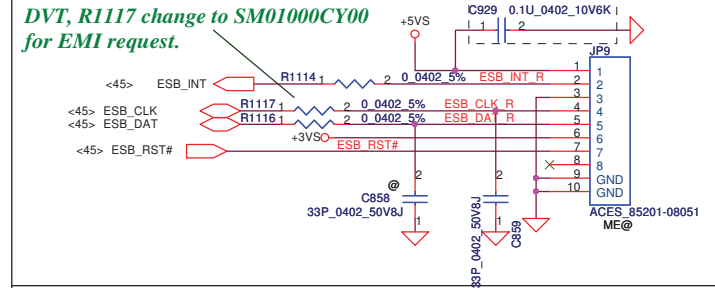


Power Bottom Board Conn. 10pin



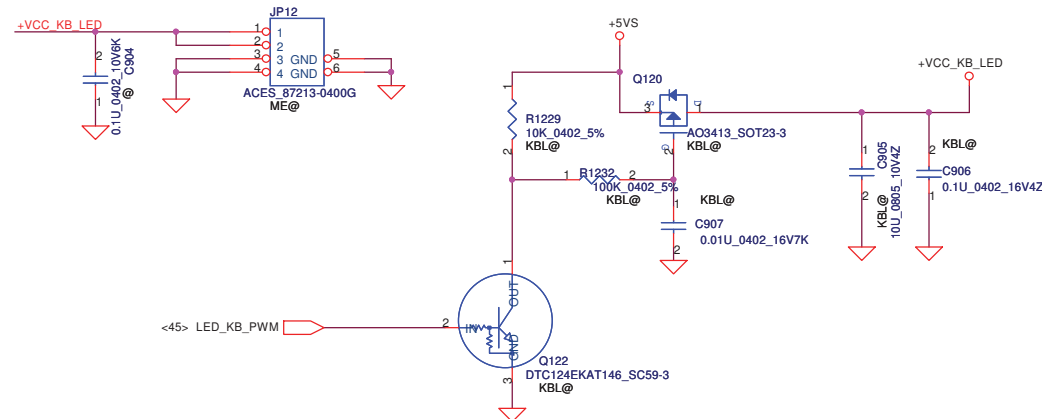
EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Silder Bar Board Mdule Conn. 6pin



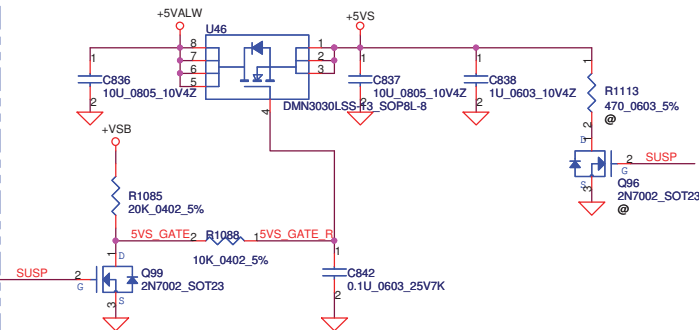
9/30 remove EC_SMB_CK2, EC_SMB_DA2

KB Lighting CONN.4pin

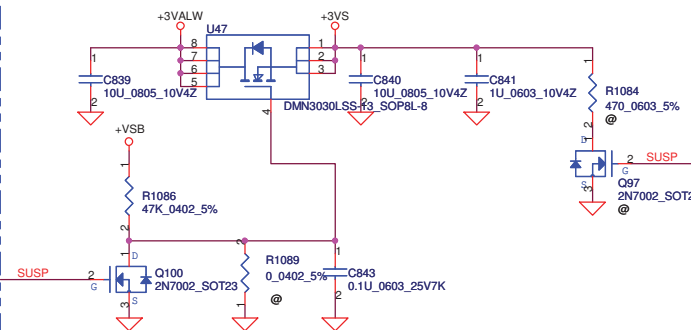


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Size Custom	Document Number	PIQY0 LA6881P		Rev 1.0
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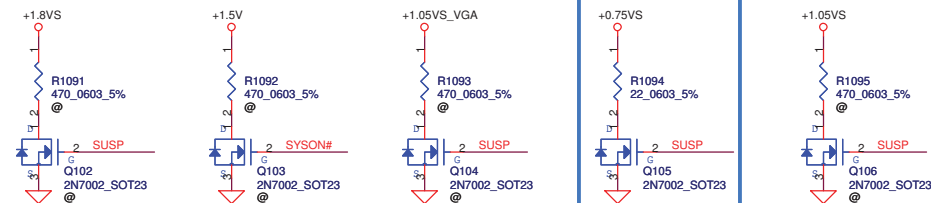
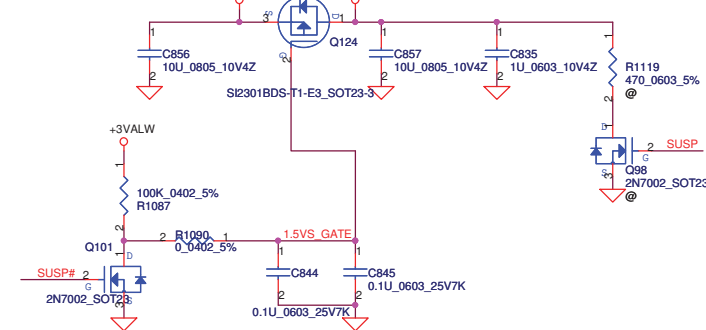
+5VALW TO +5VS



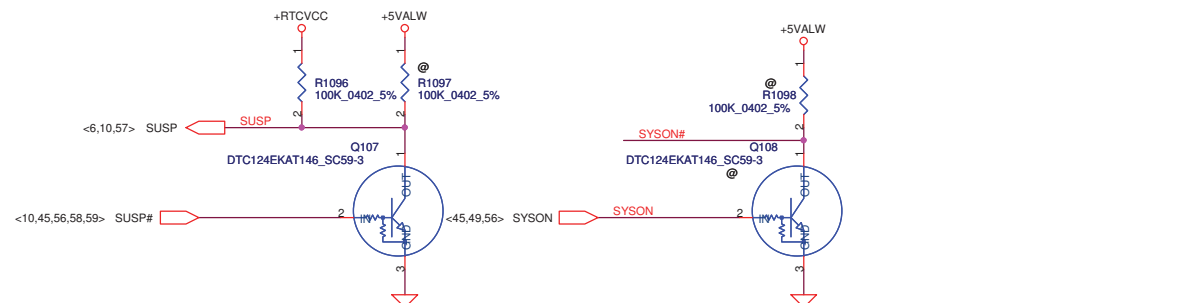
+3VALW TO +3VS



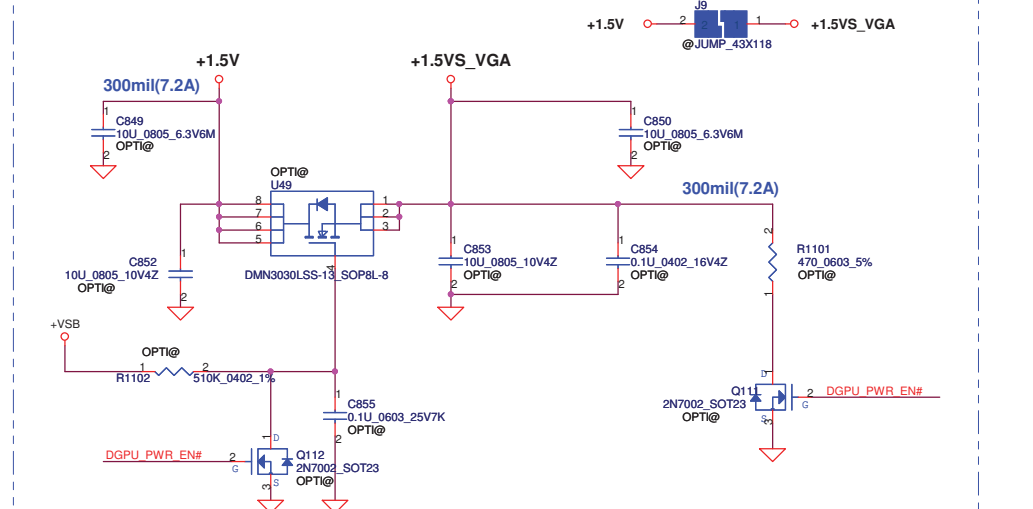
+1.5V to +1.5VS



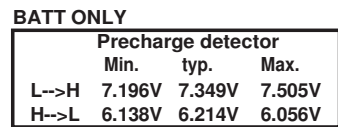
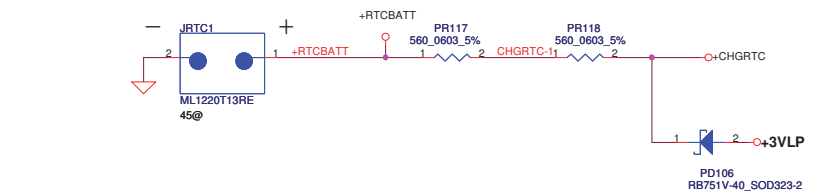
For Intel S3 Power Reduction.



+1.5V to +1.5VS_VGA Transfer

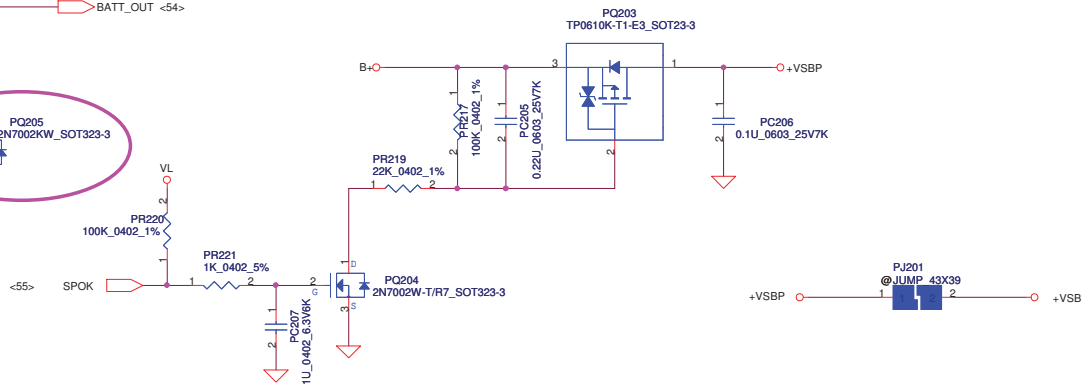
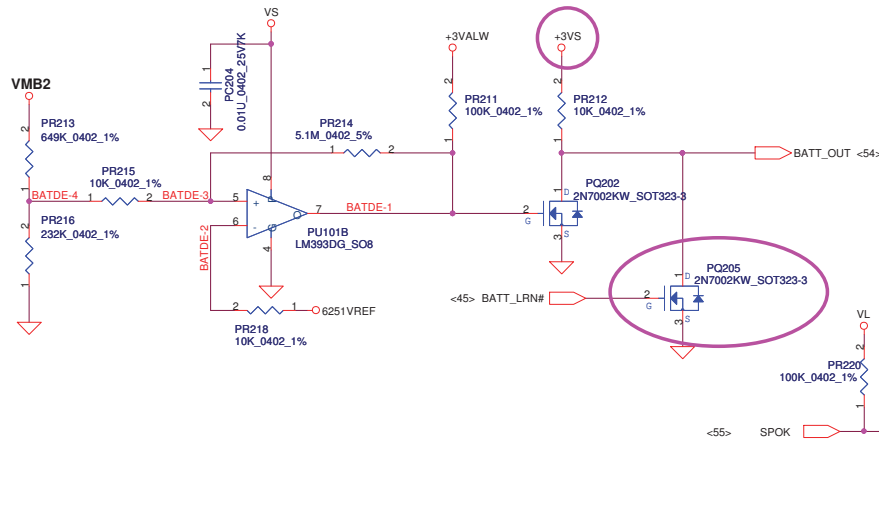
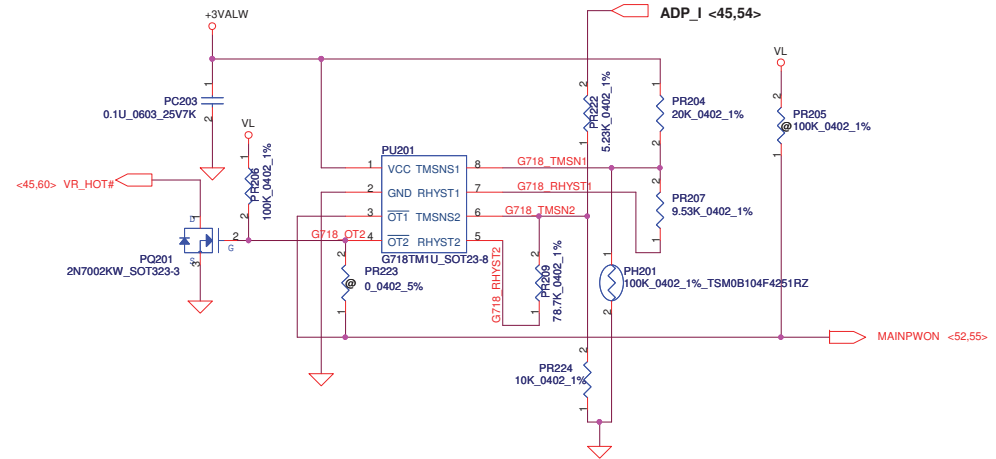
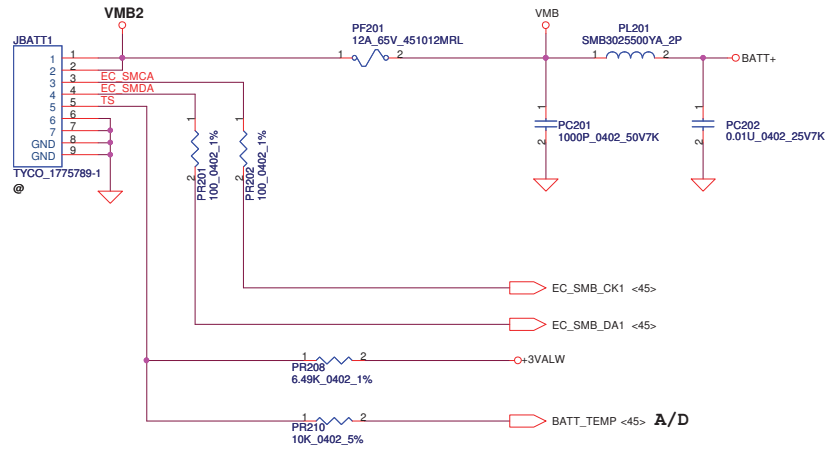


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Security Classification	Compal Secret Data			Compal Electronics, Inc. PWR DCIN / Vin Detector /Pre-charge		
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PWR DCIN / Vin Detector /Pre-charge	
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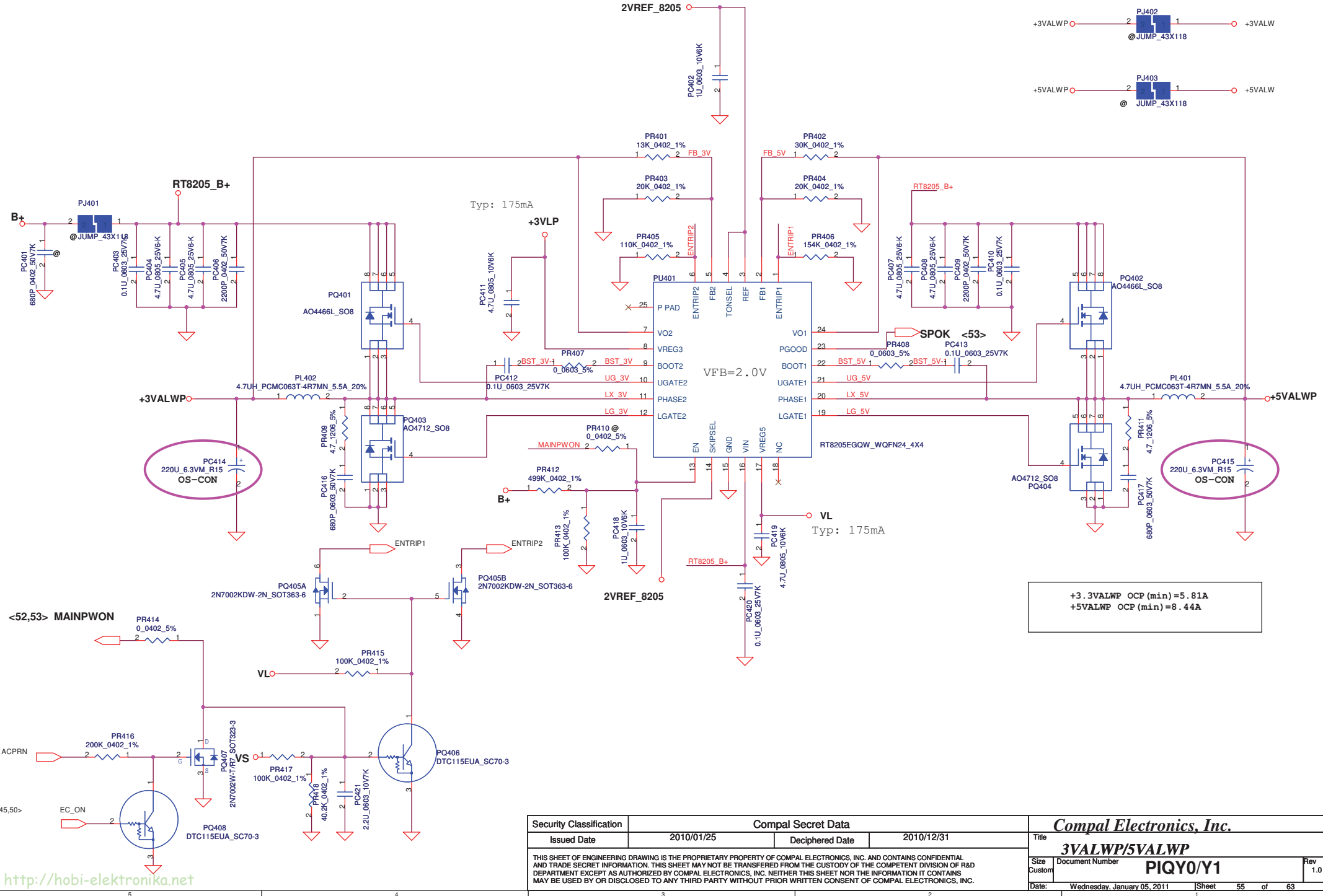
PH201 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C



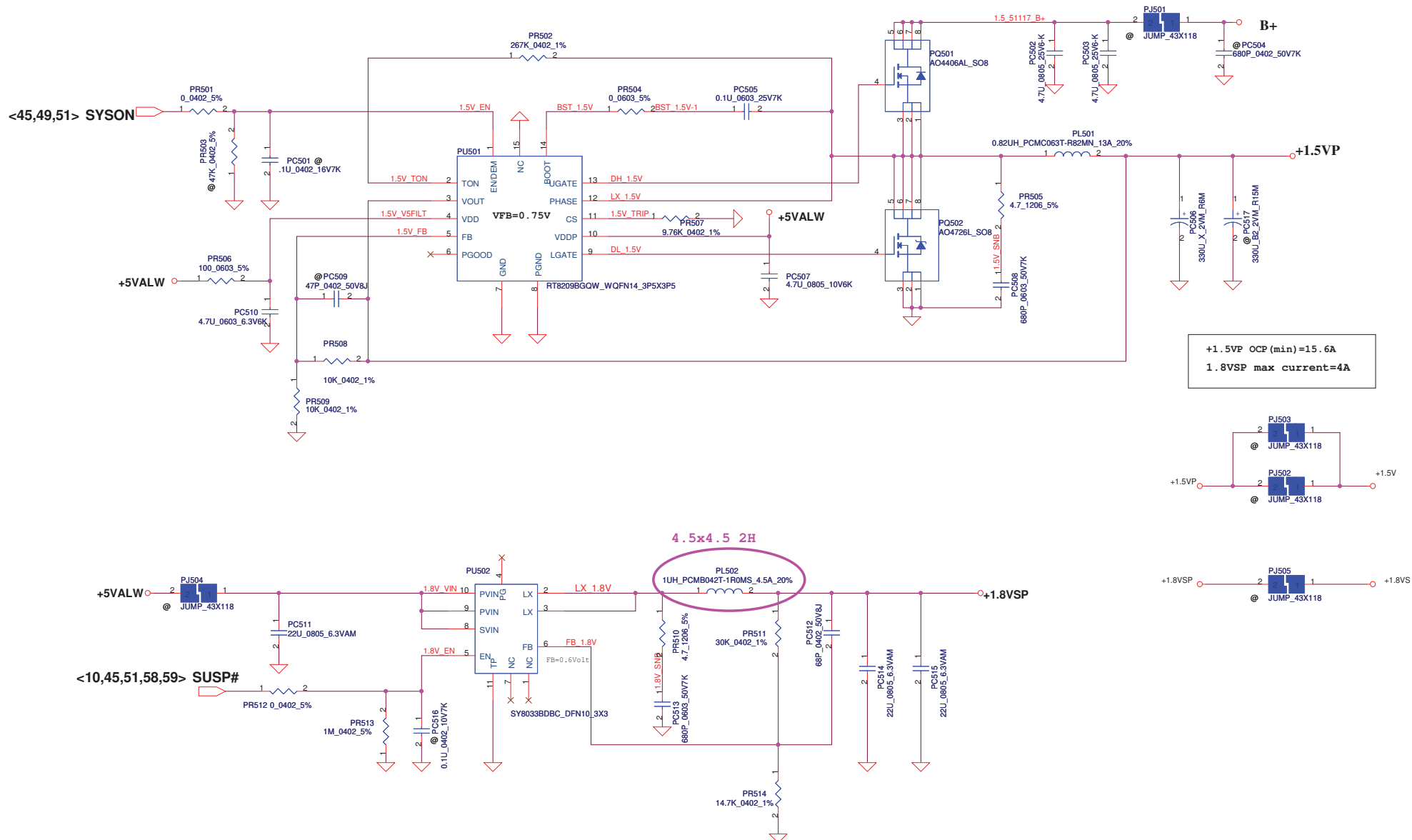
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	
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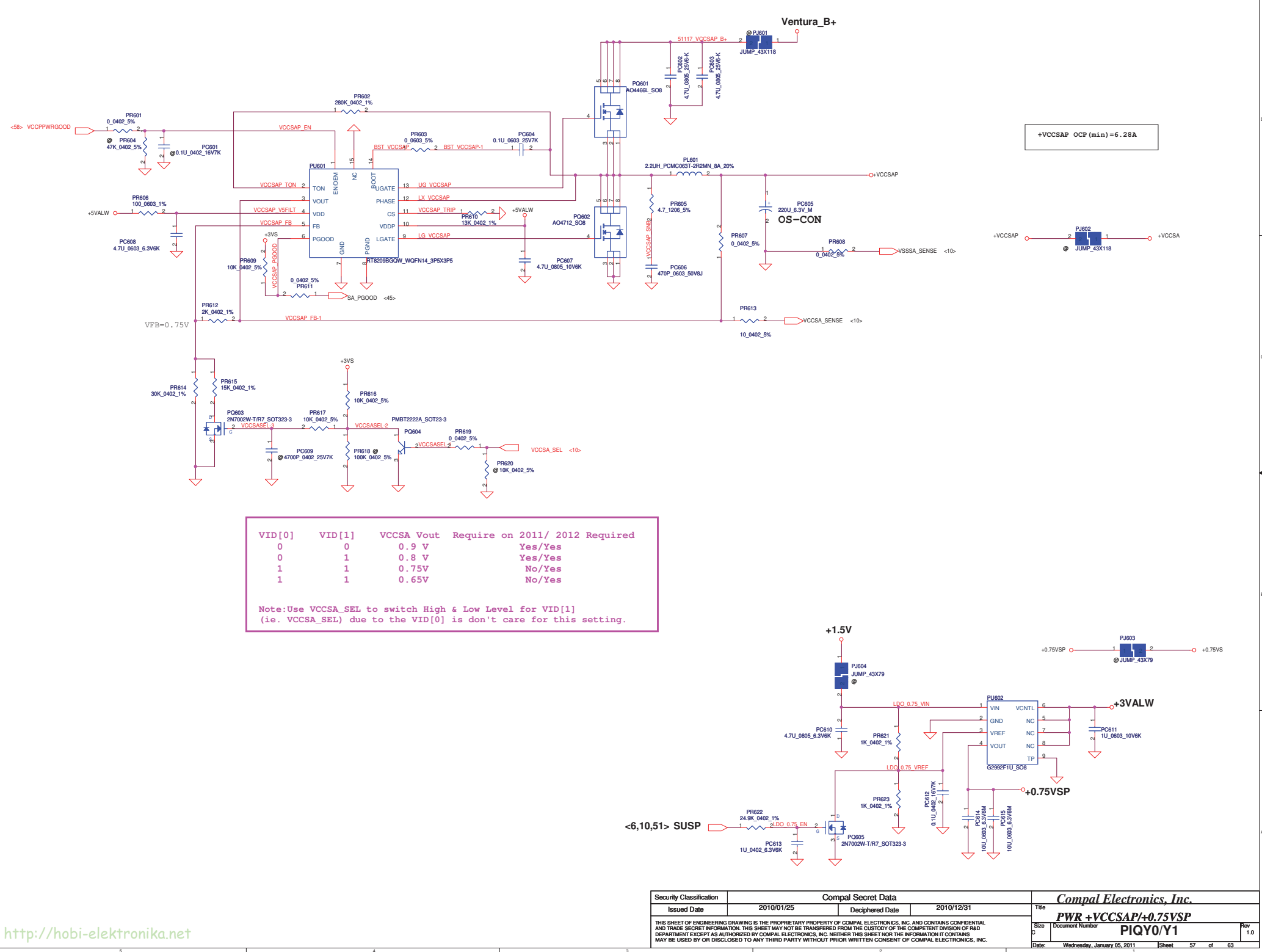
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

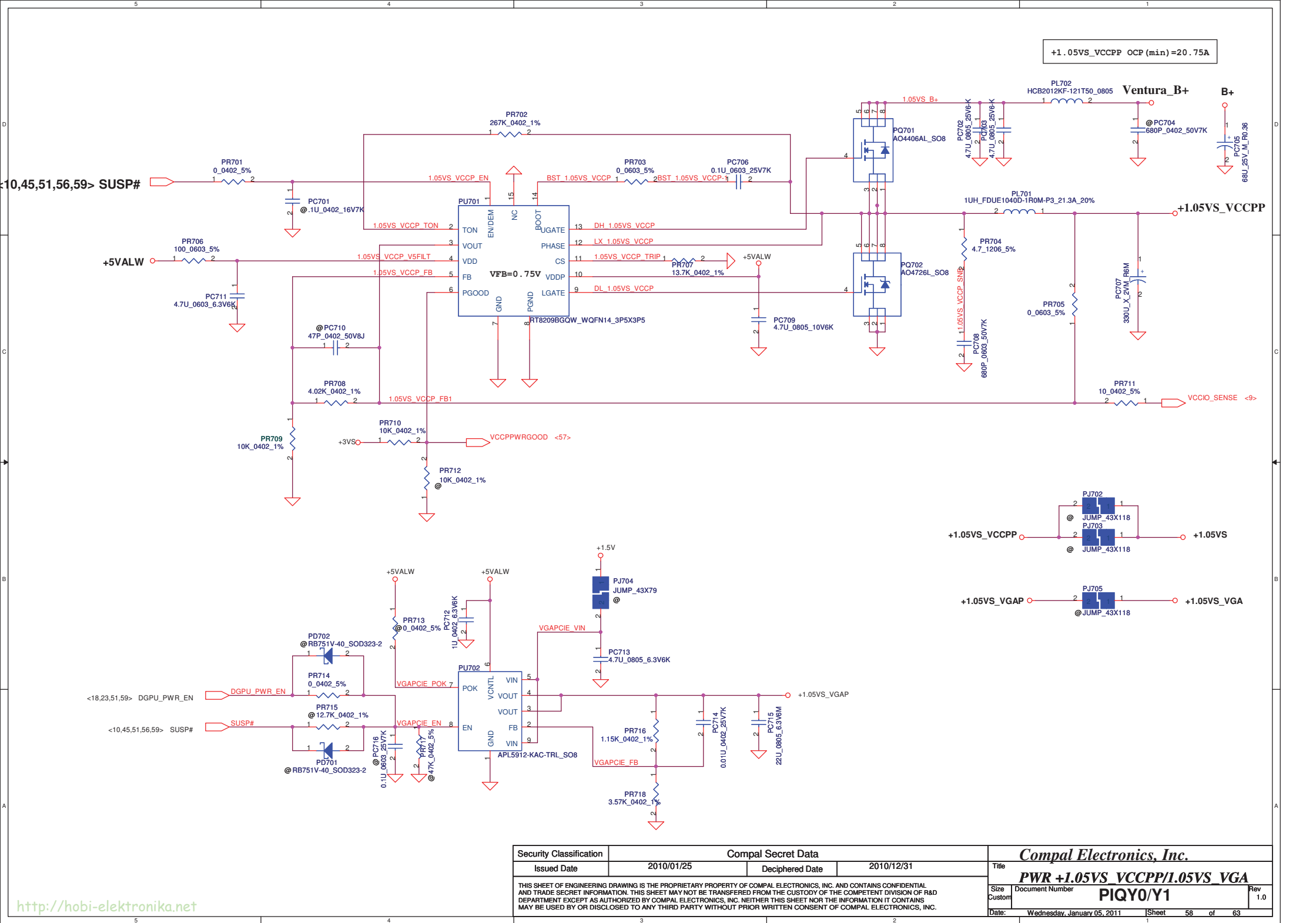


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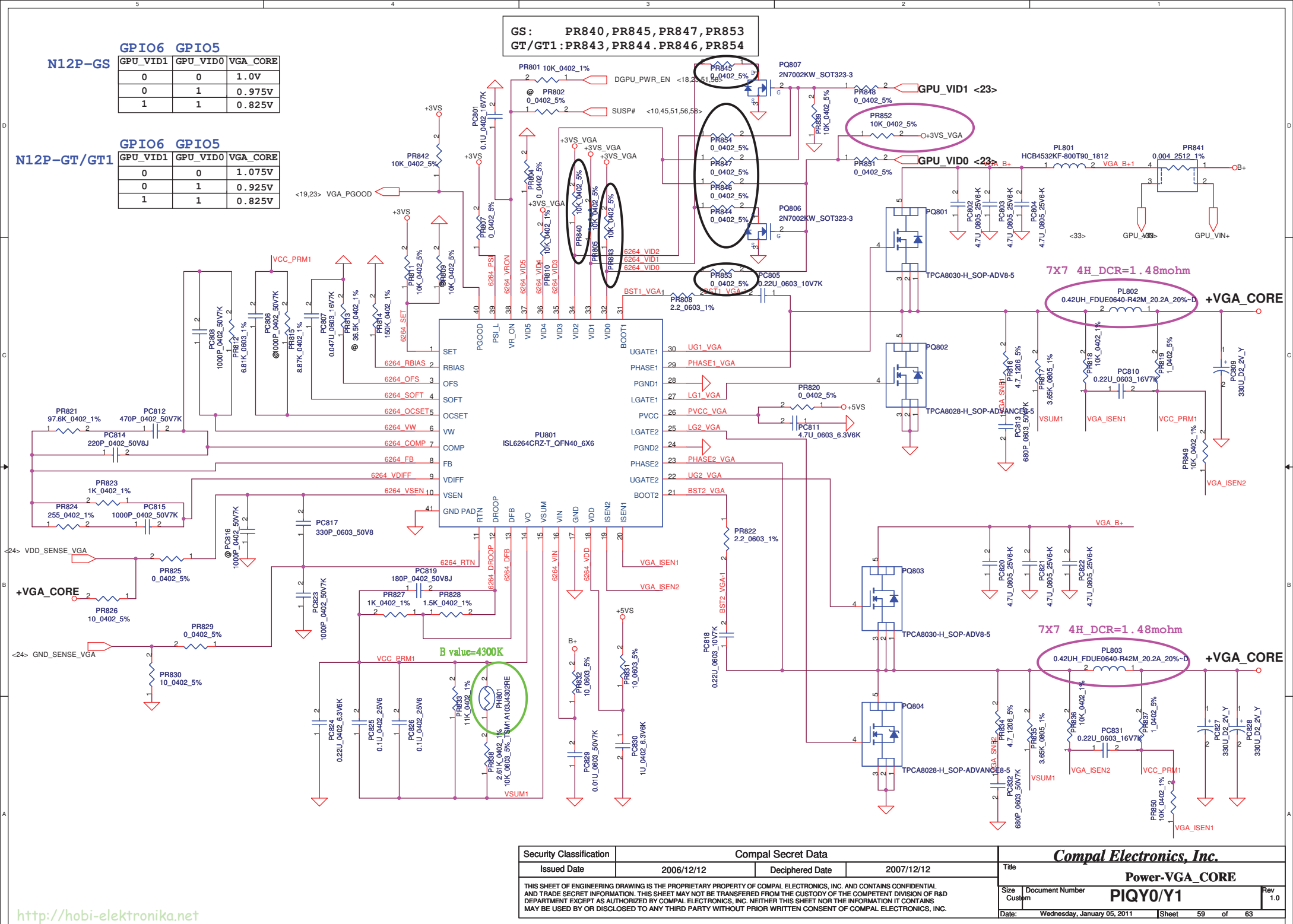
GS: PR840, PR845, PR847, PR853
GT/GT1: PR843, PR844, PR846, PR854

N12P-GS

GPIO6	GPIO5	VGA_CORE
GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.0V
0	1	0.975V
1	1	0.825V

N12P-GT/GT1

GPIO6	GPIO5	VGA_CORE
GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.075V
0	1	0.925V
1	1	0.825V



http://hobi-elektronika.net



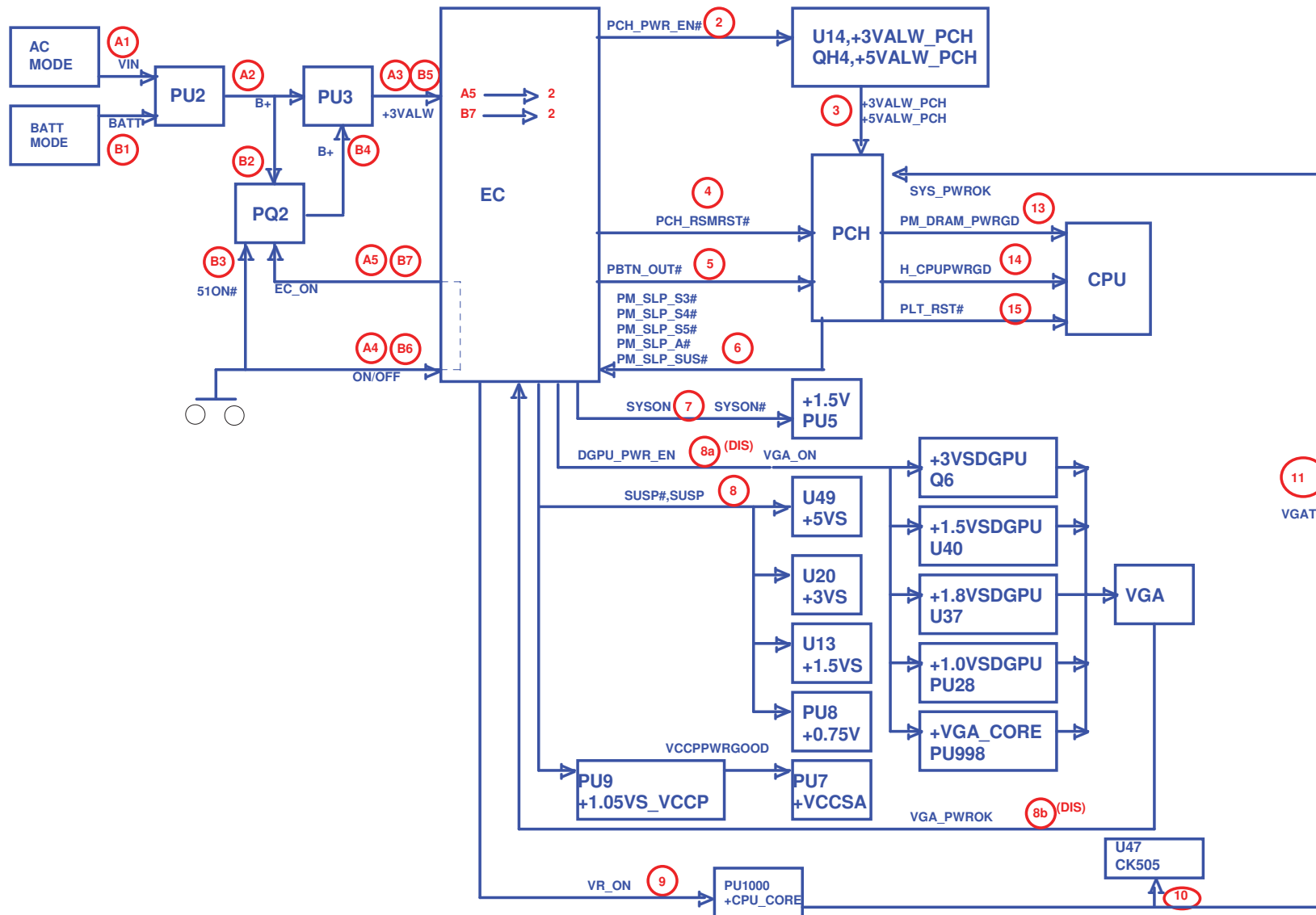
http://hobi-elektronika.net

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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				PIQY0/Y1	
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PIQY0 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
----- DVT TO DVT				
1		P18	Reserve R297	Reserve pull down for PCH GP1053.
2		P18	Exchange SATA port0 & port1	For fast boot function.
3		P50	Change KB light control circuit	Change KB light control from PWM to on/off.
			Delete U55, C908, R1233, R1235, R1236, 1238, R1230, R1231, Q121	
4		P36	Add F2 (poly-fuse)	For HDMI port diode protection.
5		P19	Stuff R303, unstuff R340	Change ESATA_DET# to GP101.
6		P49	Stuff R1068, reserve R1326, Q130	Reserve USB3.0 power swith control inverter circuit.
7		P48	Add R1327	For CHG_ON# pull down.
8		P45	Stuff R996, R139, C815, unstuff R1000, C732, C733, Y5	Change EC CLK from crystal to SUSCLK.
9		P37	Add U60, Q132, C921, R1329, Q133, R1328	Add WLAN power switch circuit
10		P34	Modify JLVDS1	Modify connector from 40pin to 30pin.
11		P09	Add C922	Add C922 to place at CPU sdie.
12		P21	Add R1330	Add for INTVREN control
13		P41	Modify C639	Modify type from 0805 to 0603
14		P45	Modify TP_LED#, PCH_DPWROK and LED_KB_PWM link	Change LED_KB_PWM to U36. pin26 GP1012.
15		P18	Delete EN_CARD_PW#, EN_WOL#	Add FAST_BOOT# to replace EN_CARD_PW# and EN_WOL#
16		P48		Remove USB charger function
17		P42	Change C660, C661 from 3300p to 0.1u	For 100Hz High Pass filter
18		P43	Replace R958, R959 to C924, C925 0.033u	For 100Hz High Pass filter
19		P14	Add one more SPI-ROM circuit	For dual BIOS function
20		P50	Remove EC_SMB_CK2, EC_SMB_DA2 link to JP13	Remove light sensor function
21		P14	Add Q134, R1345, R1346	Add for Fast boot SPI ROM selection by EC.
22		P34	Add R1341, C926	Added for EMI request
23		P37, P44	Add R1342, R1343	Added for WLAN and CARD reader Reset signal.
24		P19	Add R1344	Added for VENTURA detection.
----- DVT TO PVT				
1		P10	Add R1347, Change R56 to 20K,	Modify S3 1.5V reduction sequence.
2		P45	Add Q135	Modify PROCHOT control circuit.
			Modify R980 link to +5VALW	Change USB_ON PU power rail
----- PVT TO SVT				
1		P23, P45	FAST_BOOT#	Link FAST_BOOT# to VGA GP1012
2		P50	Add C929	EMI Request
2		P14	Add R1348	INTEL Design Guide update



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Size	Document Number	Rev			1.0
Customer	PIQY0 LA6881P				
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