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AC/100
ATA 66/100

ATA 66/100

AC97

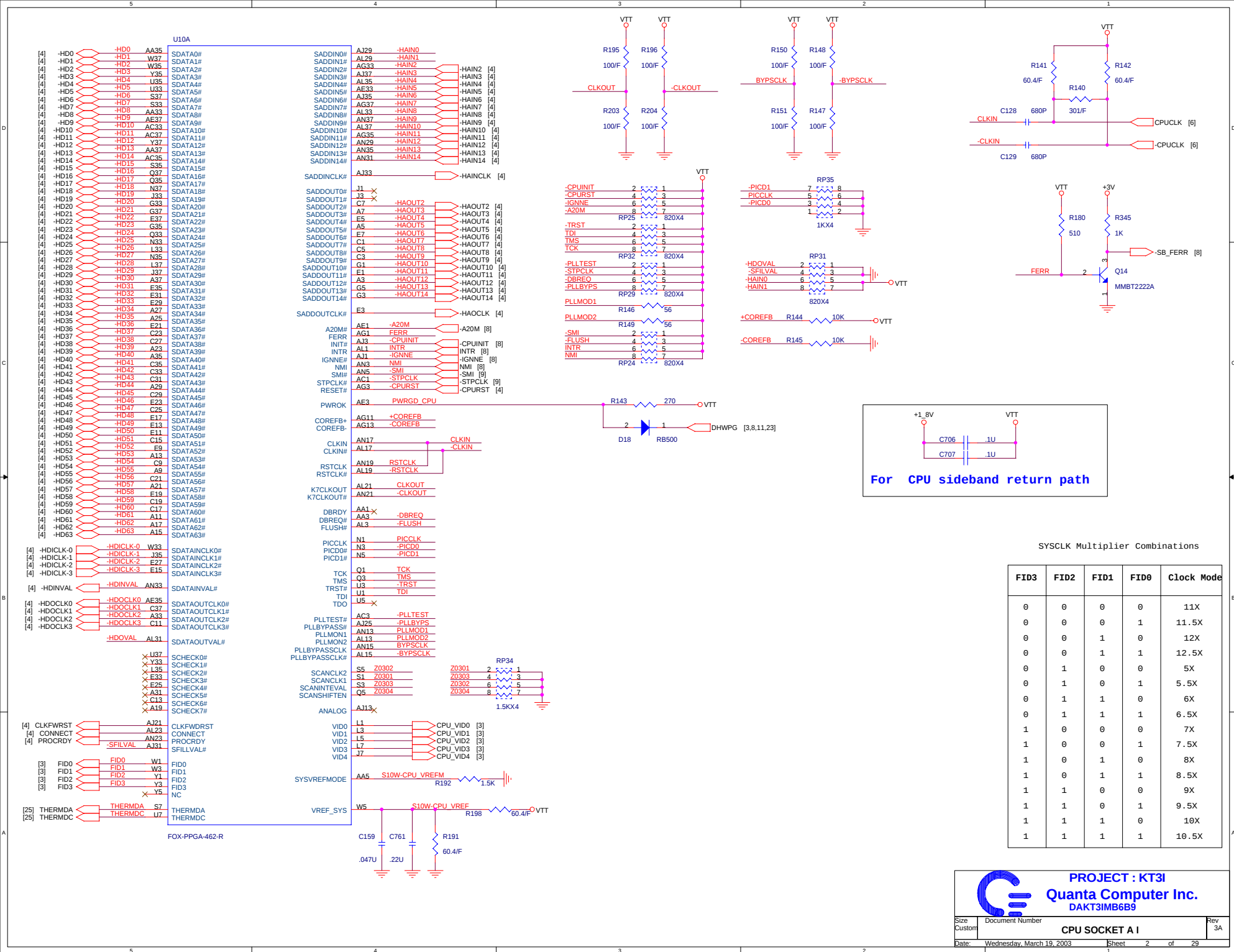
33MHZ, 3.3V PCI

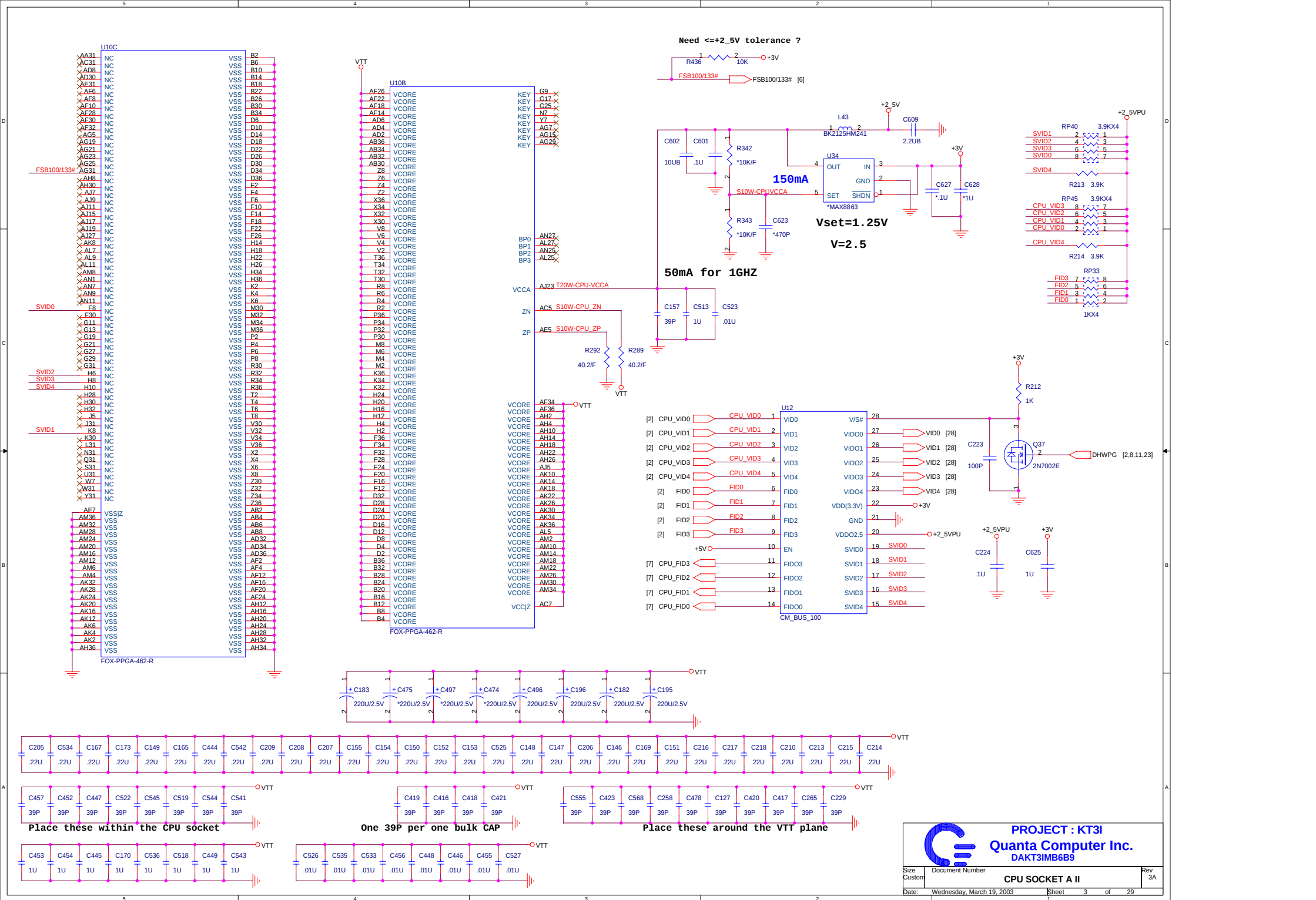
S2K-2X100/133MHZ

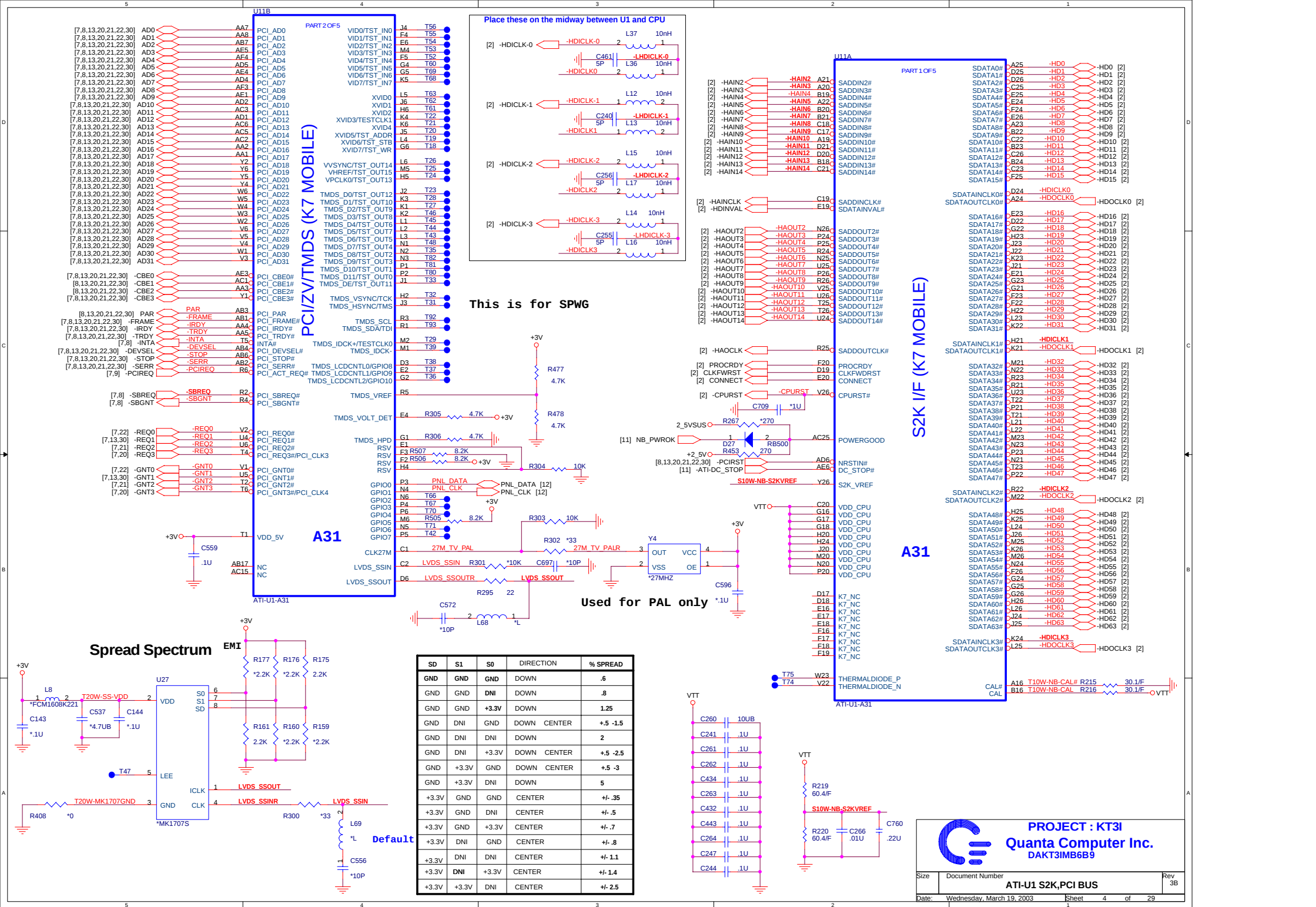
LVDS

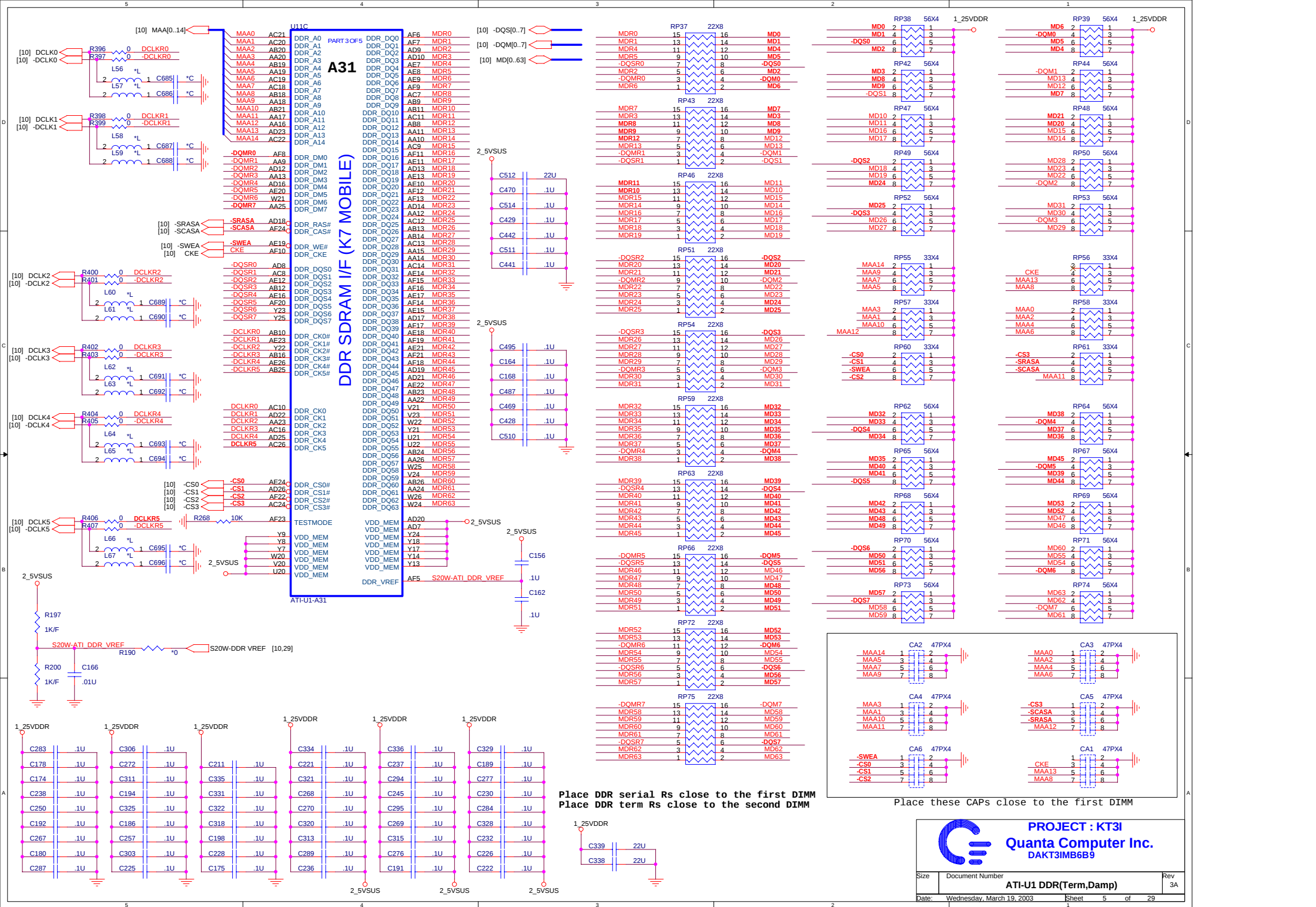
266MHZ DDR

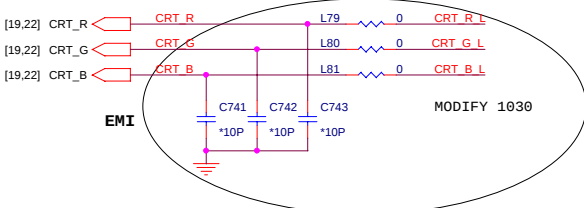
ISA BUS



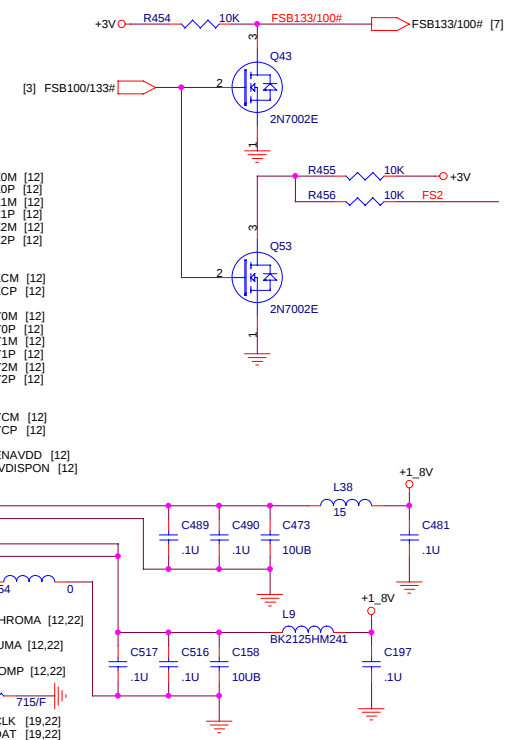
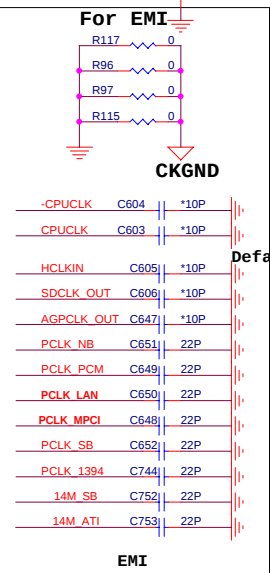
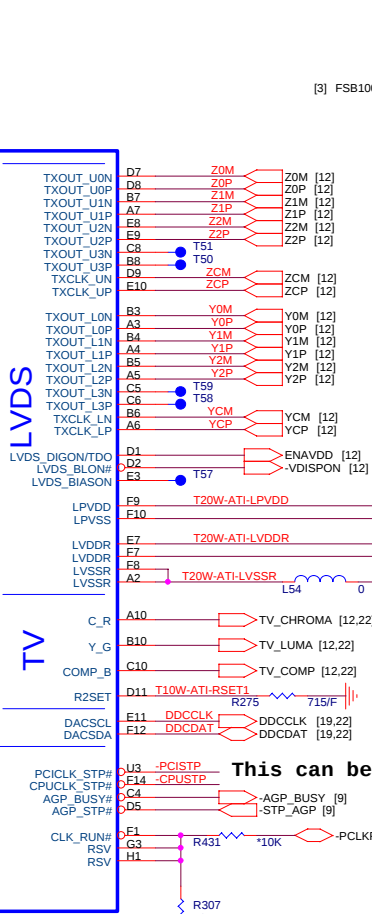
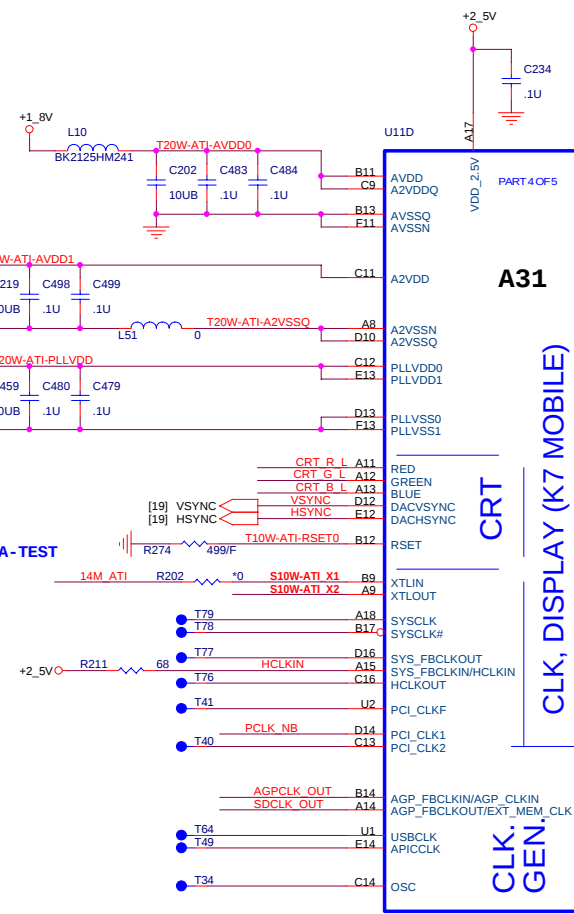
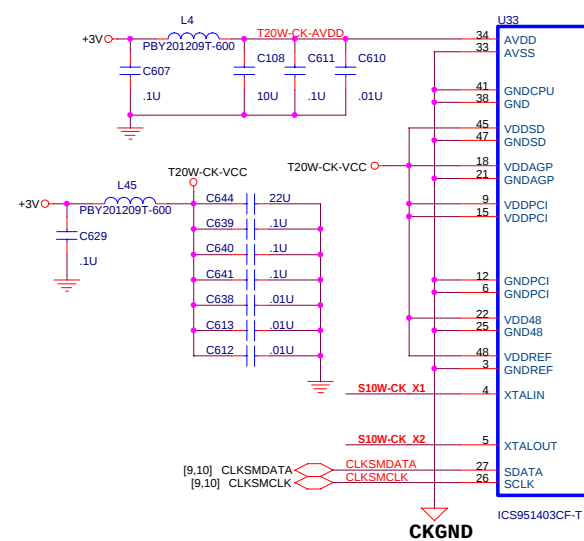
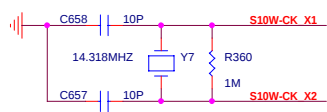
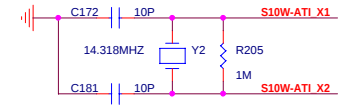




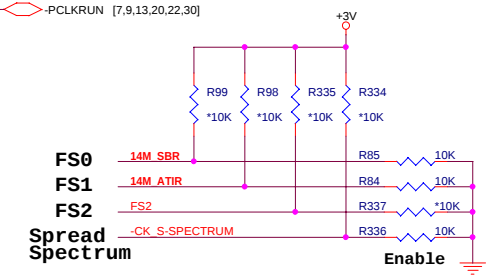




Try to save the 14.318Mhz crystal for ATI after A-TEST



This can be no connect ?



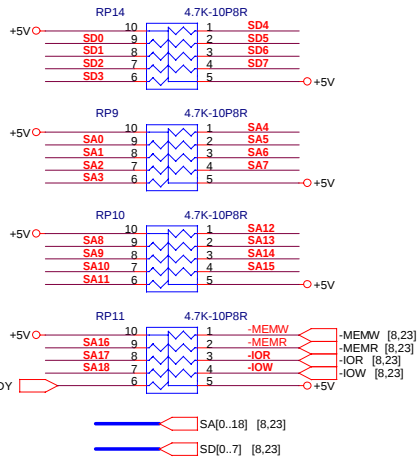
ICS951403 FREQUENCY SELECTION							
FS3	FS2	FS1	FS0	CPU	SDRAM	PCICLK	AGP SEL=0
0	0	0	0	100.00	100.00	33.33	66.67
0	0	0	1	100.00	133.33	33.33	66.67
0	0	1	0	100.00	150.00	30.00	60.00
0	0	1	1	100.00	66.67	33.33	66.67
0	1	0	0	133.33	133.33	33.33	66.67
0	1	0	1	125.00	100.00	31.25	62.50
0	1	1	0	124.00	124.00	31.00	62.00
0	1	1	1	133.00	100.00	33.33	66.67



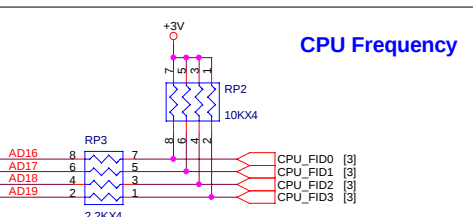
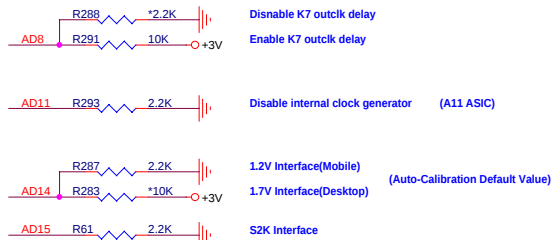
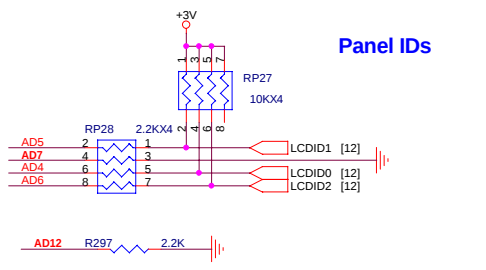
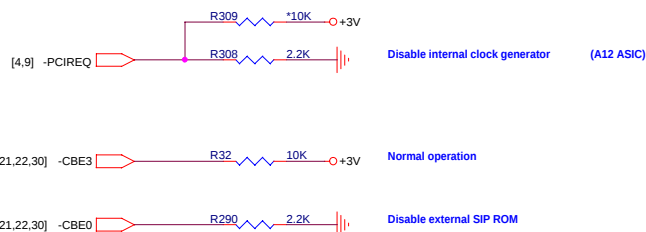
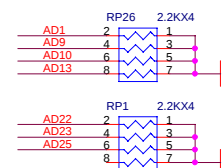
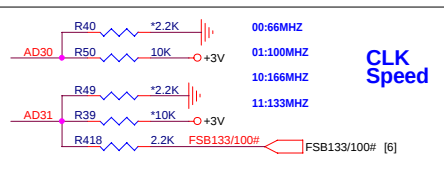
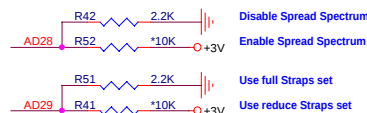
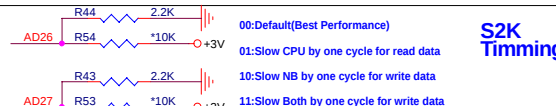
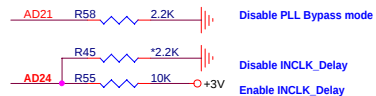
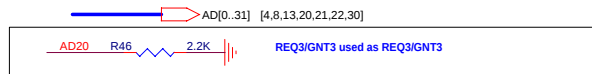
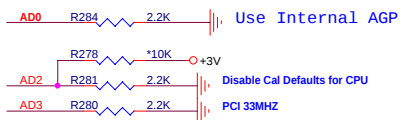
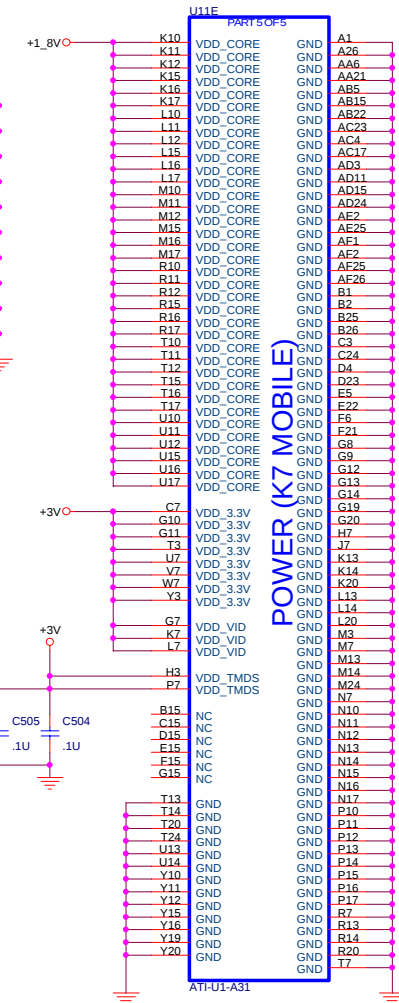
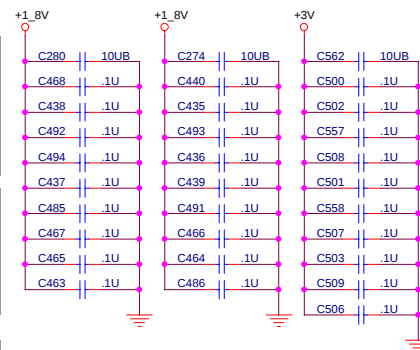
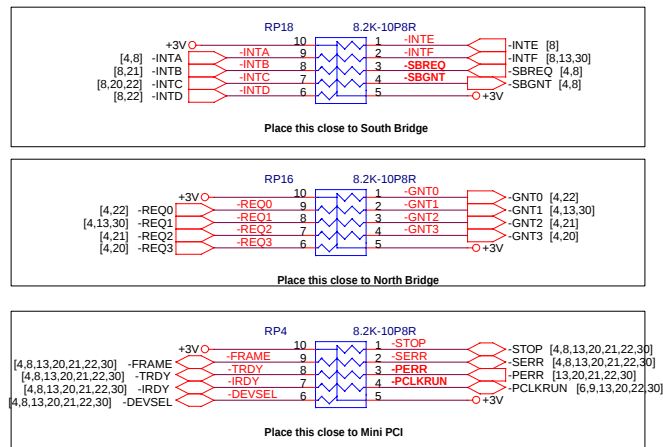
PROJECT : KT31
Quanta Computer Inc.
DAKT31MB6B9

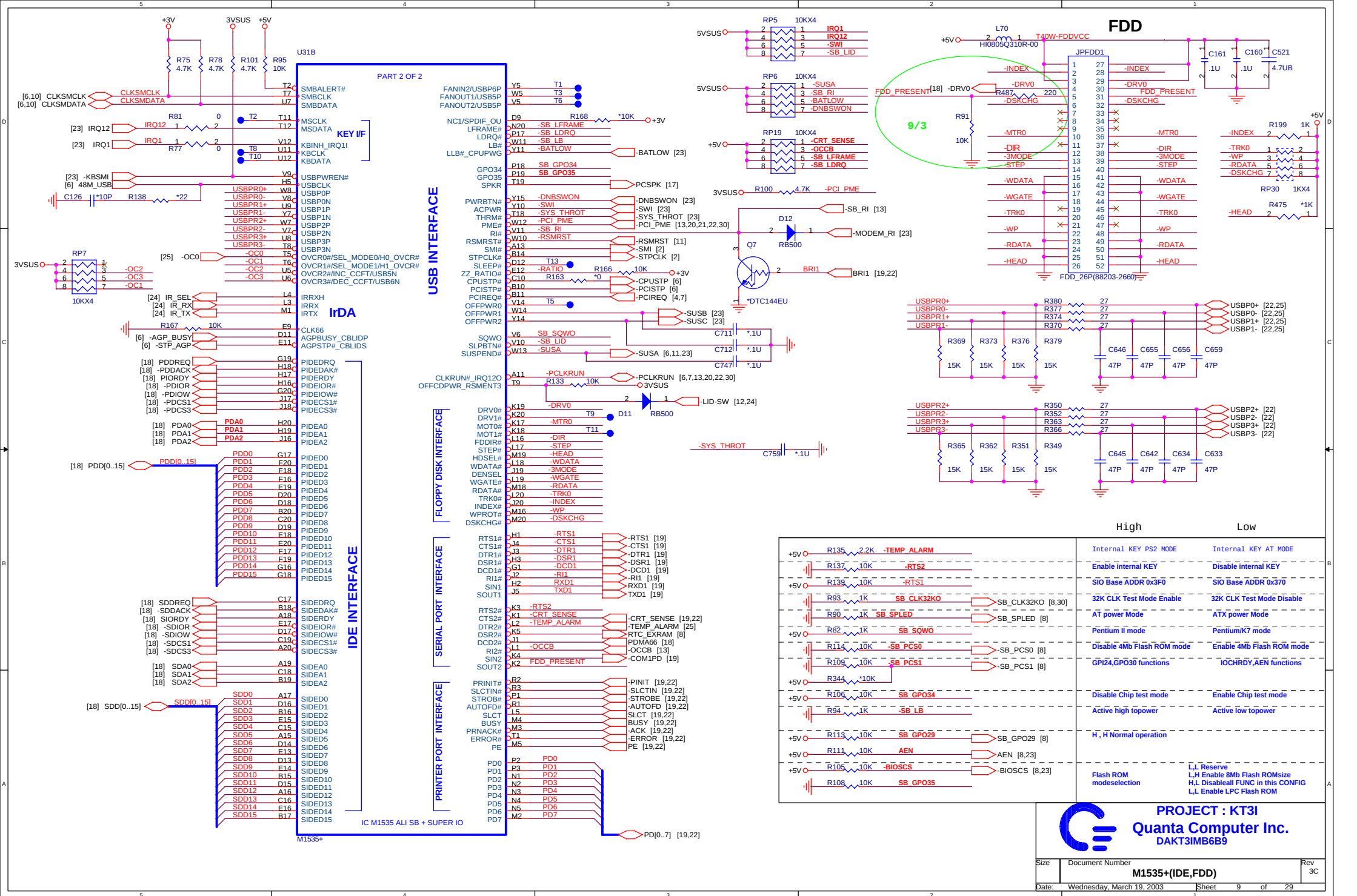
Size	Document Number	Rev
	ATI-U1 VID,CRT,TV&CKGEN	3A
Date:	Wednesday, March 19, 2003	Sheet 6 of 29

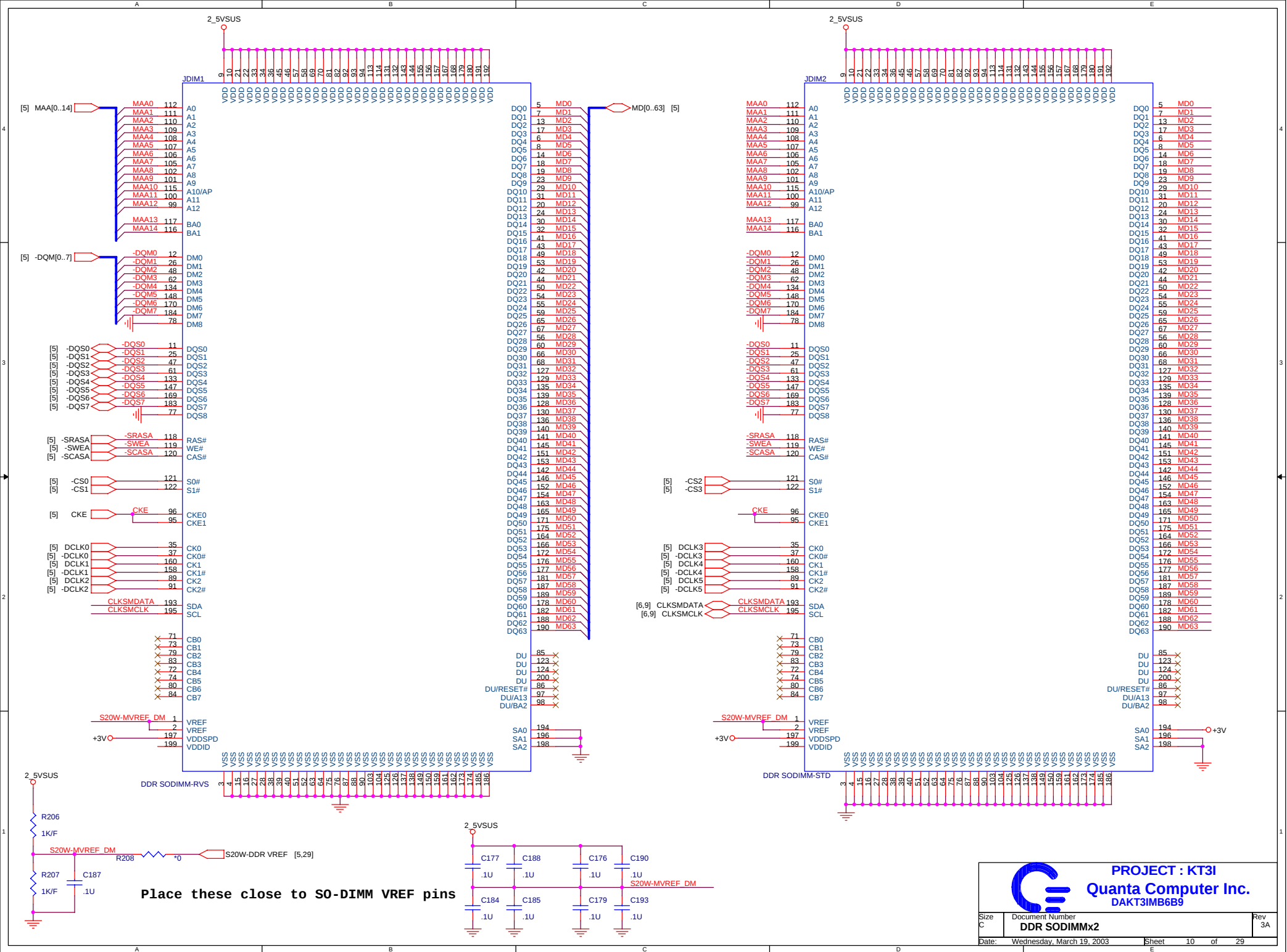
ISA PU



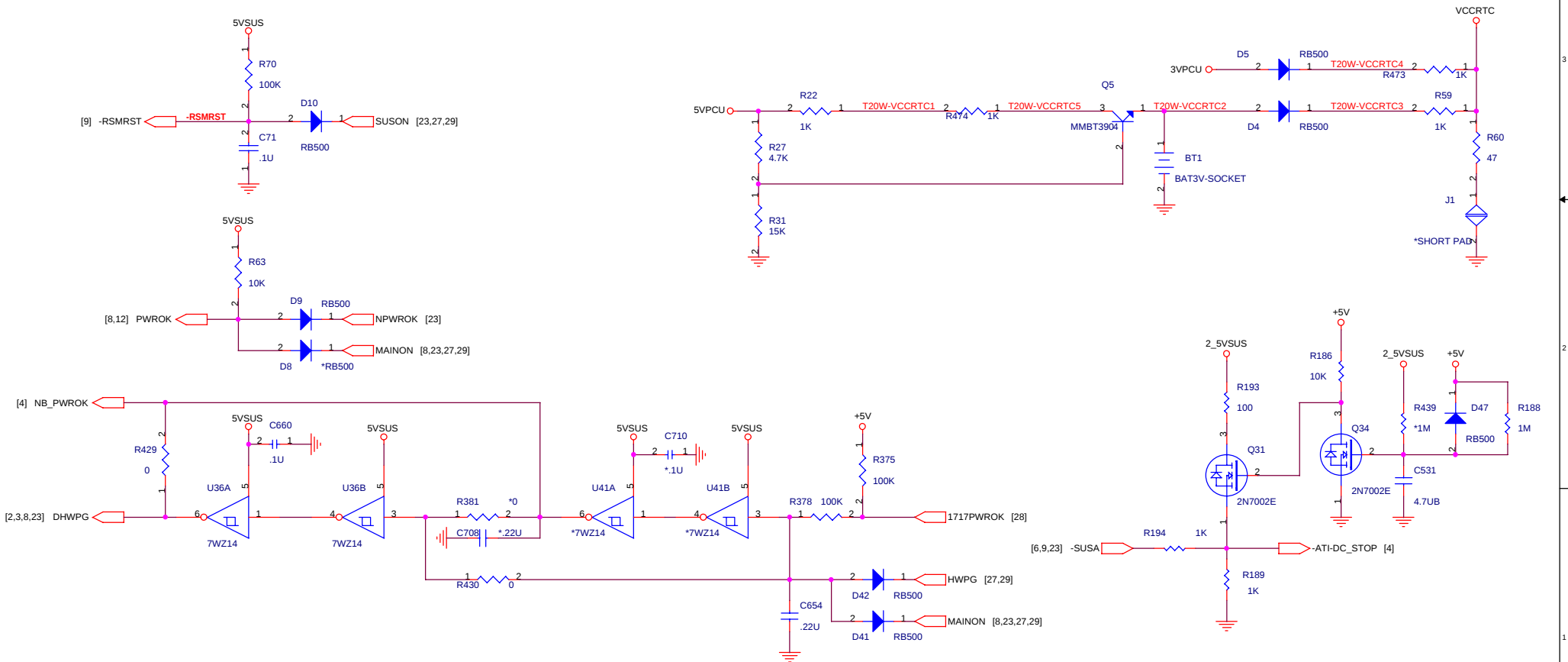
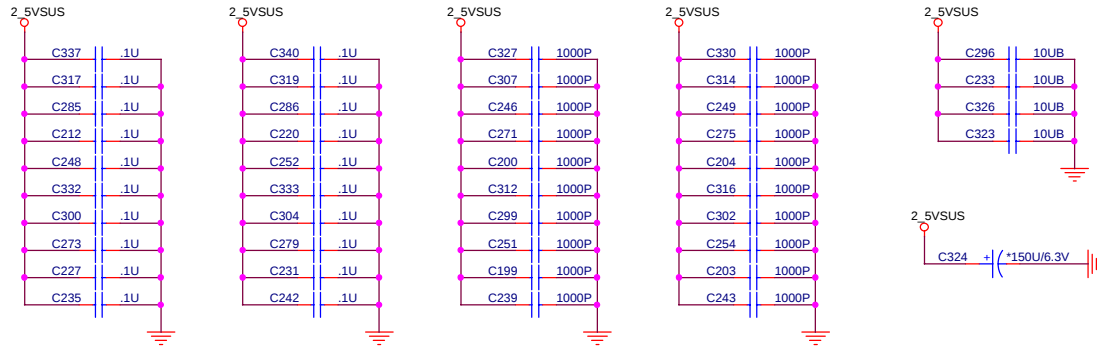
PCI PU

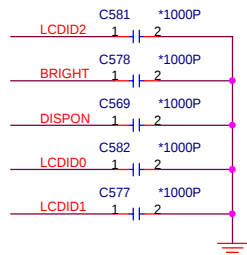
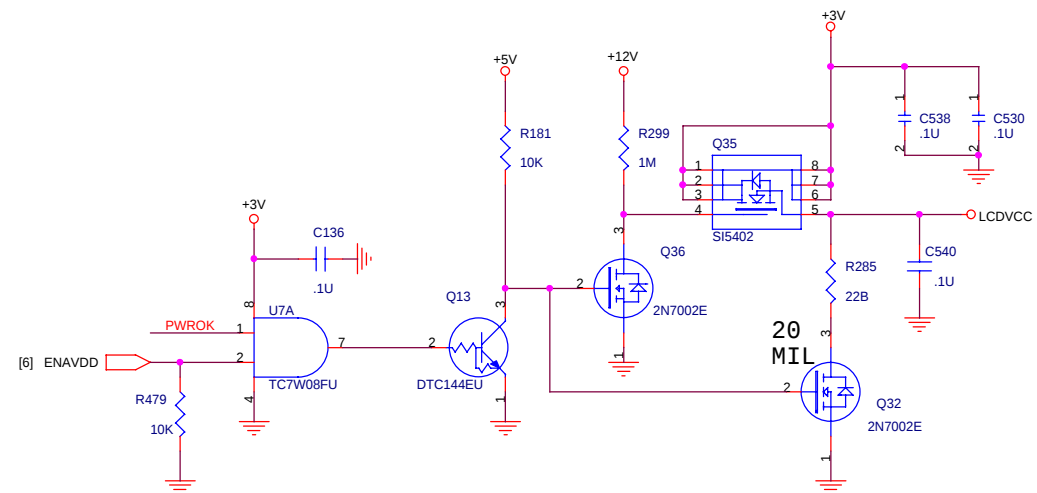
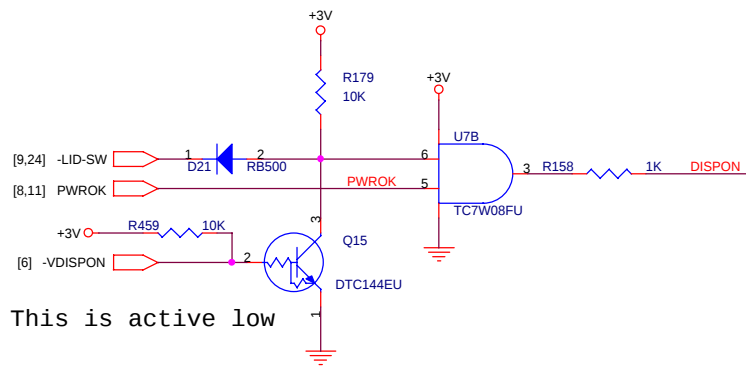




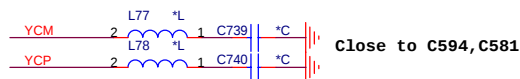


For S0-DIMM

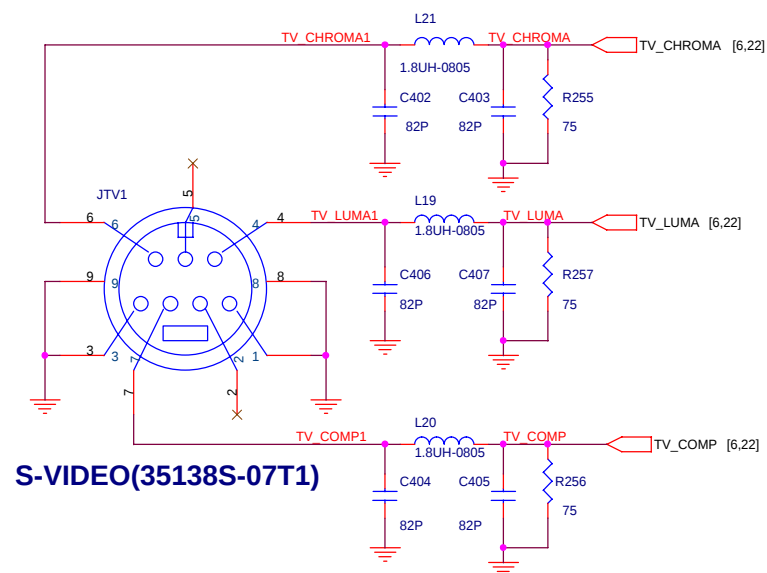
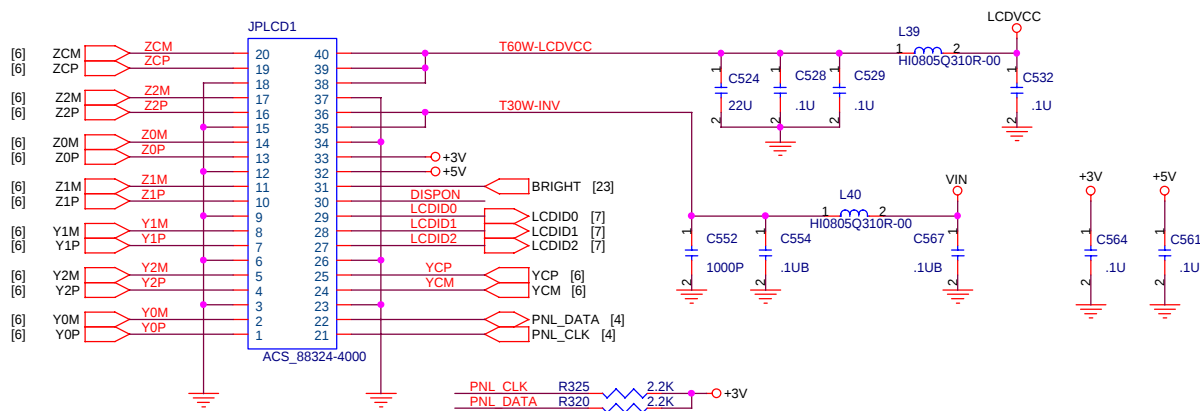




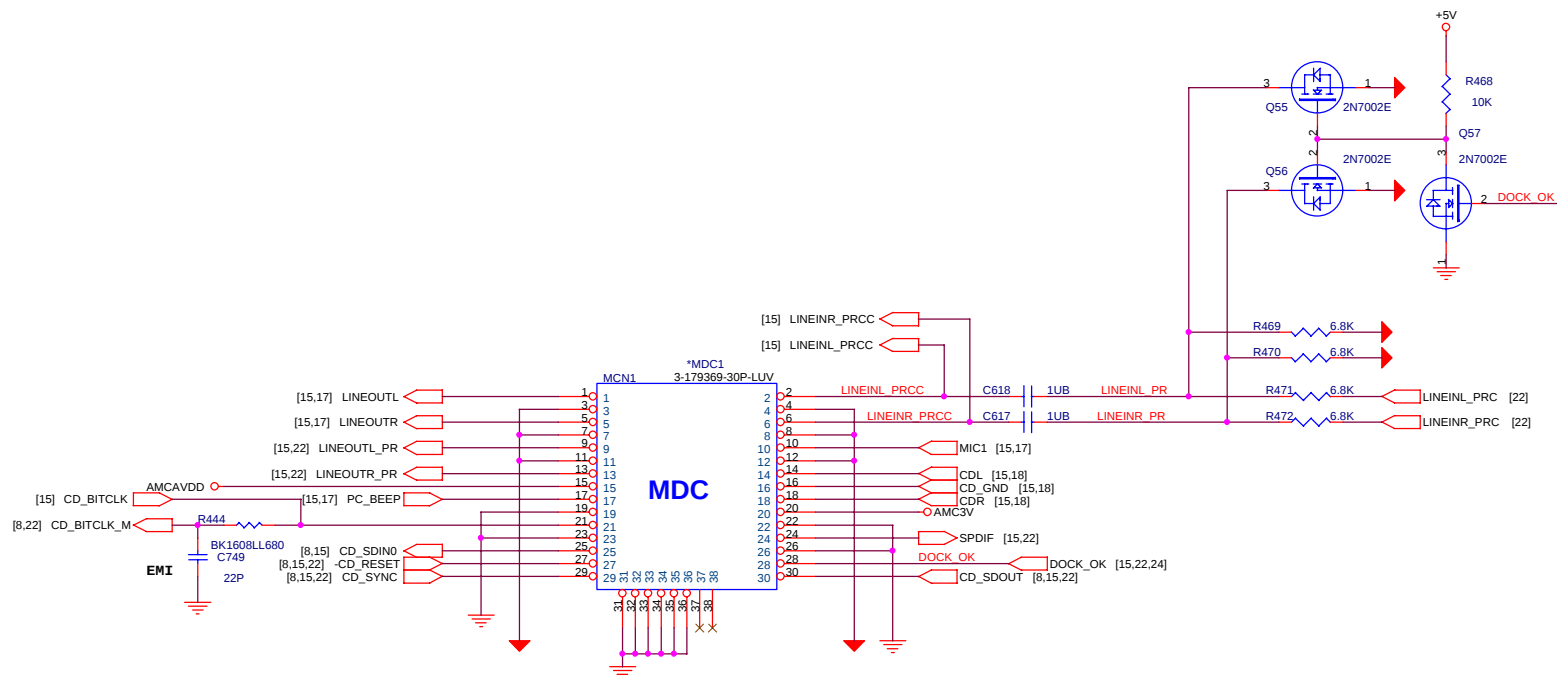
LCDID0	LCDID1	LCDID2	
1	1	1	Non SPWG XGA 1024*768 TFT
0	1	1	SXGA 1400*1050 TFT
1	0	1	SPWG XGA 1024*768 TFT



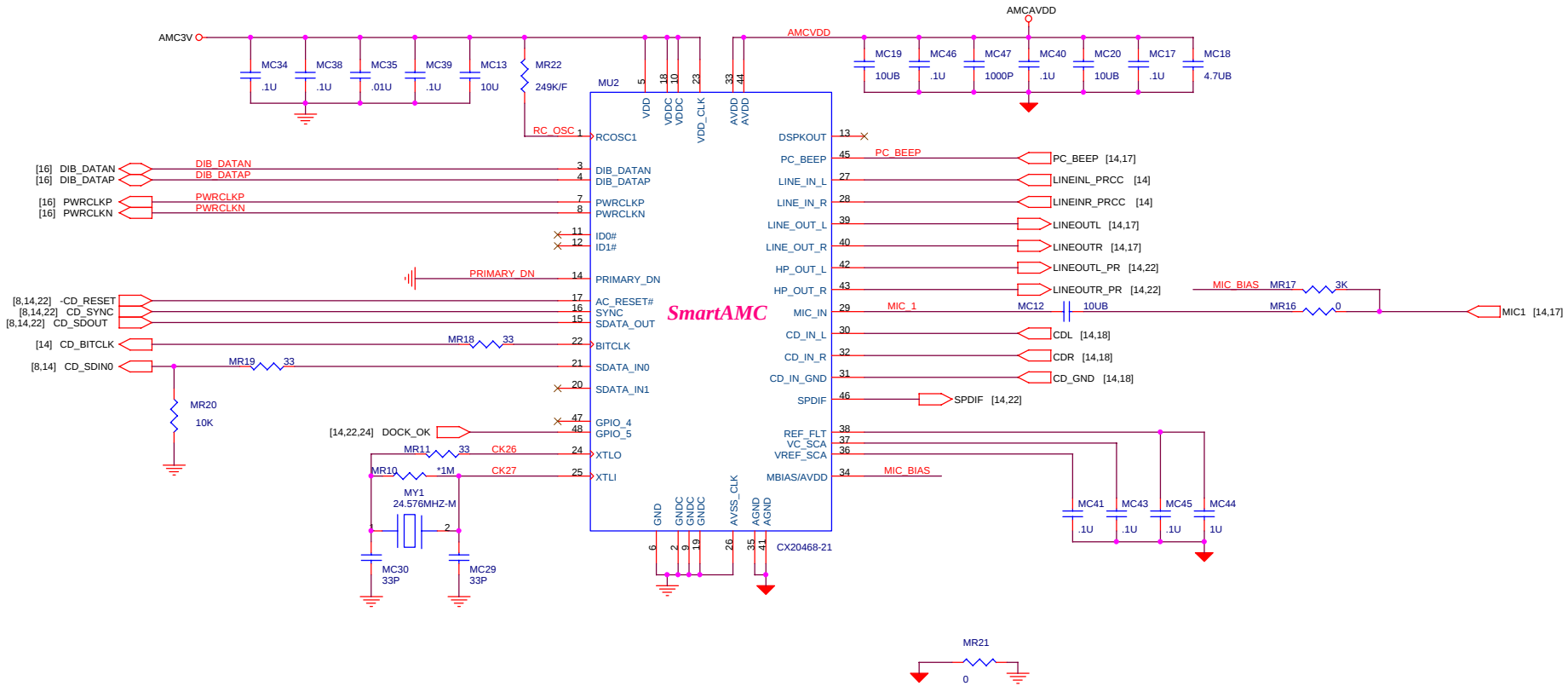
LCD INTERFACE



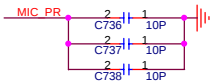
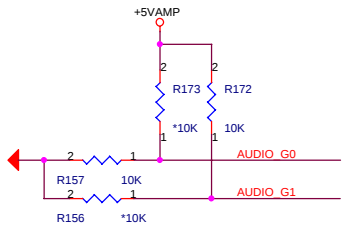
	DEFEATURE	FULL FUNCTION
R468	NO INSTALL	INSTALL
R469	0 OHM	6.8K
R470	0 OHM	6.8K
R471	NO INSTALL	INSTALL
R472	NO INSTALL	INSTALL
Q55	NO INSTALL	INSTALL
Q56	NO INSTALL	INSTALL
Q57	NO INSTALL	INSTALL



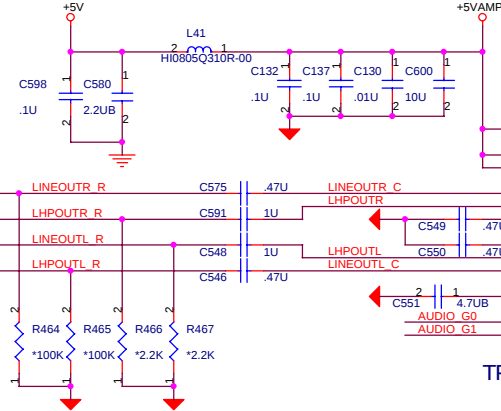
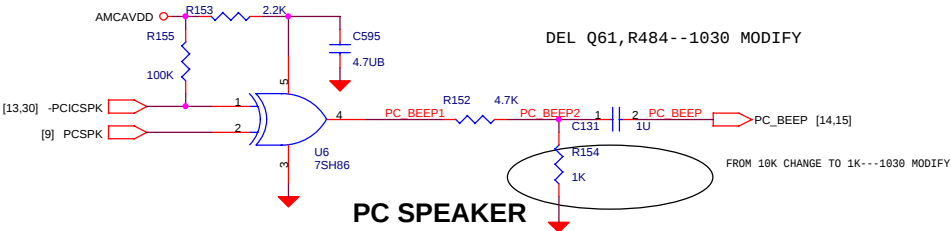
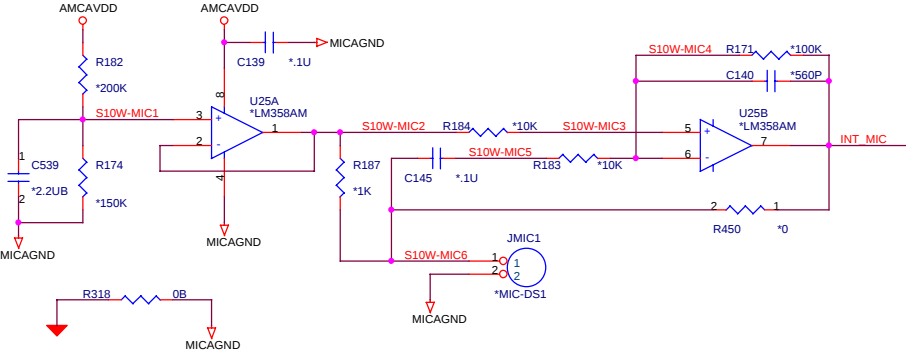
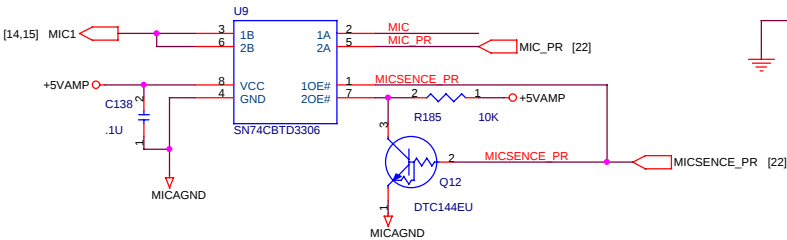
The AMC20493-001 modem is used for mother board family MBAMC20493-00.



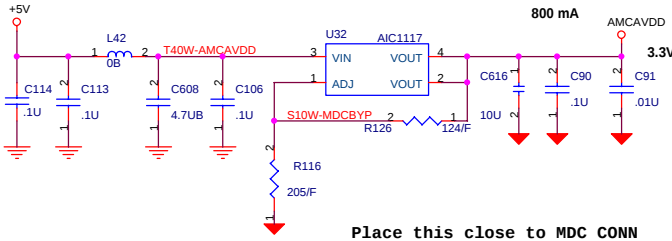
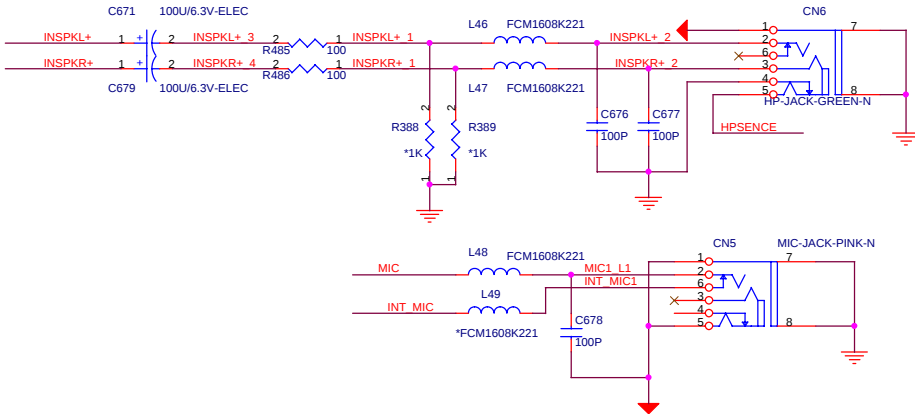
GAIN0	GAIN1	Av
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



Close to RJ11
Close to H3 EMI
Close to RP



AUDIO AMPLIFIER





PROJECT : KT3I

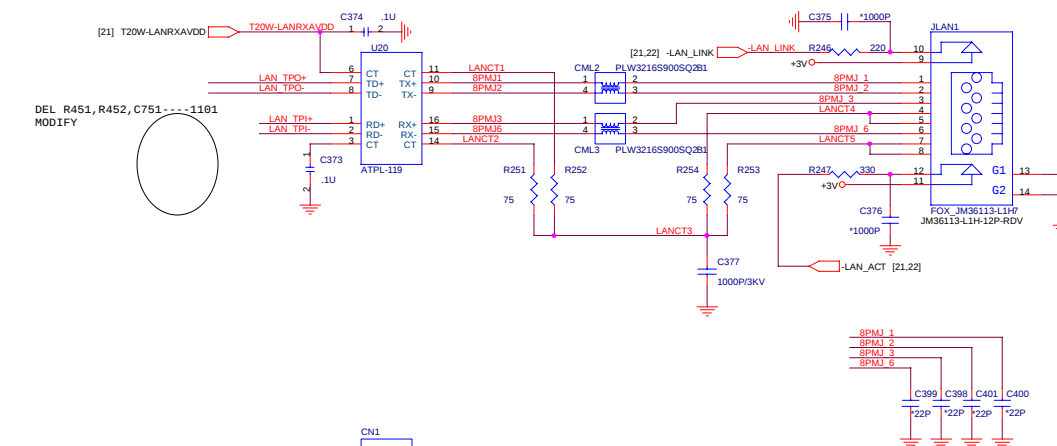
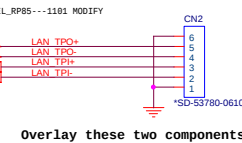
Quanta Computer Inc.

DAKT3IMB6B9

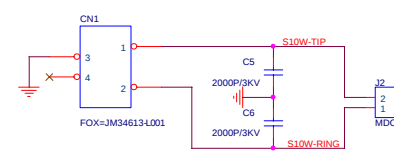
Size	Document Number	Rev
Custom	TPA0312&Audio Jack	3D
Date:	Wednesday, March 19, 2003	Sheet 17 of 29

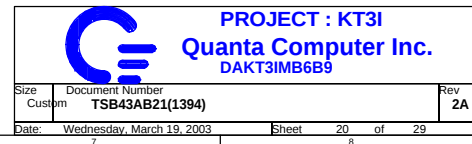
The schematic diagram illustrates the MDC1248 board's internal components and their connections to the JPCDROM1 connector. Key elements include:

- Top Section:** Shows the connection of various capacitors (C621, C620, C619) and resistors (R131, R130, R129) to the JPCDROM1 connector pins. A note states: "Place these parts close to MDC CONN".
- Center Section:** Features the JPCDROM1 connector with pins 1 through 52. Pins 1-12 are labeled with SDRAM-related signals (e.g., SDDR7, SDDR6, SDDR5, SDDR4, SDDR3, SDDR2, SDDR1, SDDR0). Pins 13-24 are labeled with SDRAM-related signals (e.g., SDDR13, SDDR12, SDDR11, SDDR10, SDDR9, SDDR8). Pins 25-34 are labeled with SDRAM-related signals (e.g., SDDR15, SDDR14, SDDR13, SDDR12, SDDR11, SDDR10, SDDR9, SDDR8). Pins 35-49 are labeled with SDRAM-related signals (e.g., SDDR15, SDDR14, SDDR13, SDDR12, SDDR11, SDDR10, SDDR9, SDDR8). Pins 50-52 are labeled with SDRAM-related signals (e.g., SDDR15, SDDR14, SDDR13, SDDR12, SDDR11, SDDR10, SDDR9, SDDR8).
- Bottom Section:** Shows the connection of various capacitors (C346, C345, C342, C341) and resistors (R232, R233, R234, R235, R236, R237) to the JPCDROM1 connector. A note states: "Place these parts close to MDC CONN".
- Right Section:** Shows the connection of various capacitors (C346, C345, C342, C341) and resistors (R232, R233, R234, R235, R236, R237) to the JPCDROM1 connector. A note states: "Place these parts close to MDC CONN".
- Transistors:** Several transistors are shown, including Q26 (DTC144EU), Q10 (*DTA124EU), Q24 (DTA124EU), and Q25 (*DTA124EU). They are connected to various signals like -IDERST, -CDDED, -CDDLED, and ACTIVELED.
- Other Components:** The diagram includes various resistors (R120, R121, R122, R231, R488, R510, R118) and capacitors (C343, C344, C346, C345, C342, C341) connected to different parts of the circuit.



The schematic diagram illustrates the JPHDD1 module's connections. On the left, the Hi8050C331R-00 provides power and control signals: +5V0 to L33, HI8050C331R-00 to T40W-HDD, and T40W-HDD to C414 (10U) and C413 (1000P). The JPHDD1 module has pins for -IDERST, PDDR7, PDDR6, PDDR5, PDDR4, PDDR3, PDDR2, PDDR1, PDDR0, RPDDREQ, RPDIOW, RPDIOR, RPIORBY, RP-DACK, PIQ14, RPDAL, RPDAG, RPDCS1, -HDDLED, and HDD_SUIN. On the right, the PDMA66 [9] is connected to +3V0 via R264 (2 10K) and PPIORBY, and to ground via R262 (100K). Other connections include RPDDREQ to R266 (2 5.6K), PDDR7 to R269 (2 10K), PIQ14 to R263 (2 4.7K), and PCSEL to R265 (2 470).





[4,7,8,13,20,22,30] AD[0..31]

PCLK LAN

[4,7,8,13,20,22,30] -CBE[0..3]

[6] PCLK LAN
[4,8,13,20,22,30] -PCIRST
[4,8,13,20,22,30] PAR
[7,13,20,22,30] -PERR
[4,7,8,13,20,22,30] -SERR
[4,7,8,13,20,22,30] -DEVSEL
[4,7,8,13,20,22,30] -FRAME
[4,7] -GNT2
[4,7] -REQ2
[4,7,8,13,20,22,30] TRDY
[4,7,8,13,20,22,30] -IRDY
[4,7,8,13,20,22,30] -STOP
[7,8] -INTB
LANVCC
[23] -LAN_PME
[9,13,20,22,30] -PCI_PME

LANVCC
C14
.1U

DP83816

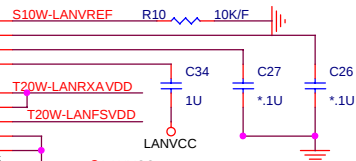
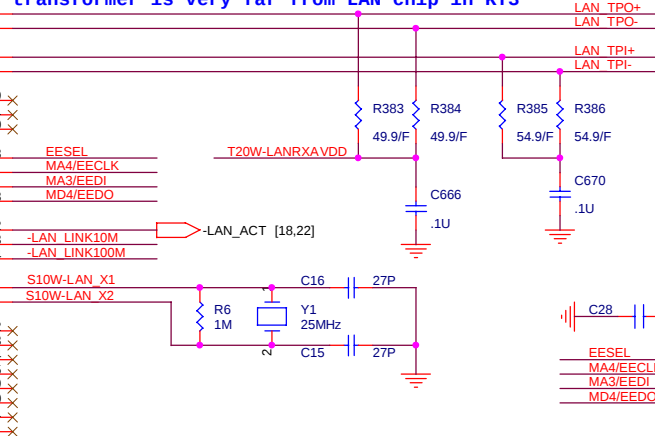
PCI
SIGNALS

MII

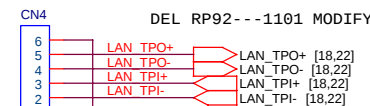
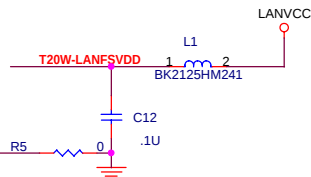
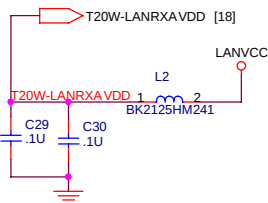
POWER

TP1DP
TP1DM
TP2DP
TP2DM
MCS#
MWR#
MRD#
EESEL
MA4/EECLK
MA3/EEDI
MD4/EEDO
MA0/LEDACK
MA1/LED10LNK
MA2/LED100LNK
X1
X2
MD0
MD1
MD2
MD3
MD5
MD6
MD7
MA5
VREF
BCAP1
BCAP2
BCAP3
RXAVDD1
RXAVDD2
FSVDD
TXDVDD
MACVDD1
MACVDD2
PCIVDD1
PCIVDD2
PCIVDD3
PCIVDD4
PCIVDD5
VDDIO1
VDDIO2
VDDIO3
VDDIO4
VDDIO5
PHYVDD1
PHYVDD2
SUBGND1
SUBGND2
SUBGND3
VSSIO1
VSSIO2
VSSIO3
VSSIO4
VSSIO5
TXIOVSS1
TXIOVSS2
TXDVSS
RXAVSS1
RXAVSS2
MACVSS1
MACVSS2
PCIVSS1
PCIVSS2
PCIVSS3
PCIVSS4
PCIVSS5
PHYVSS1
PHYVSS2
FSVSS

Place R383,R384 and C666 close to Transformer because transformer is very far from LAN chip in KT3

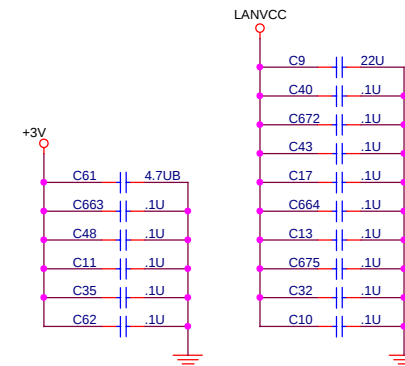


The difference between DP83816 and DP83815 is Pin 19



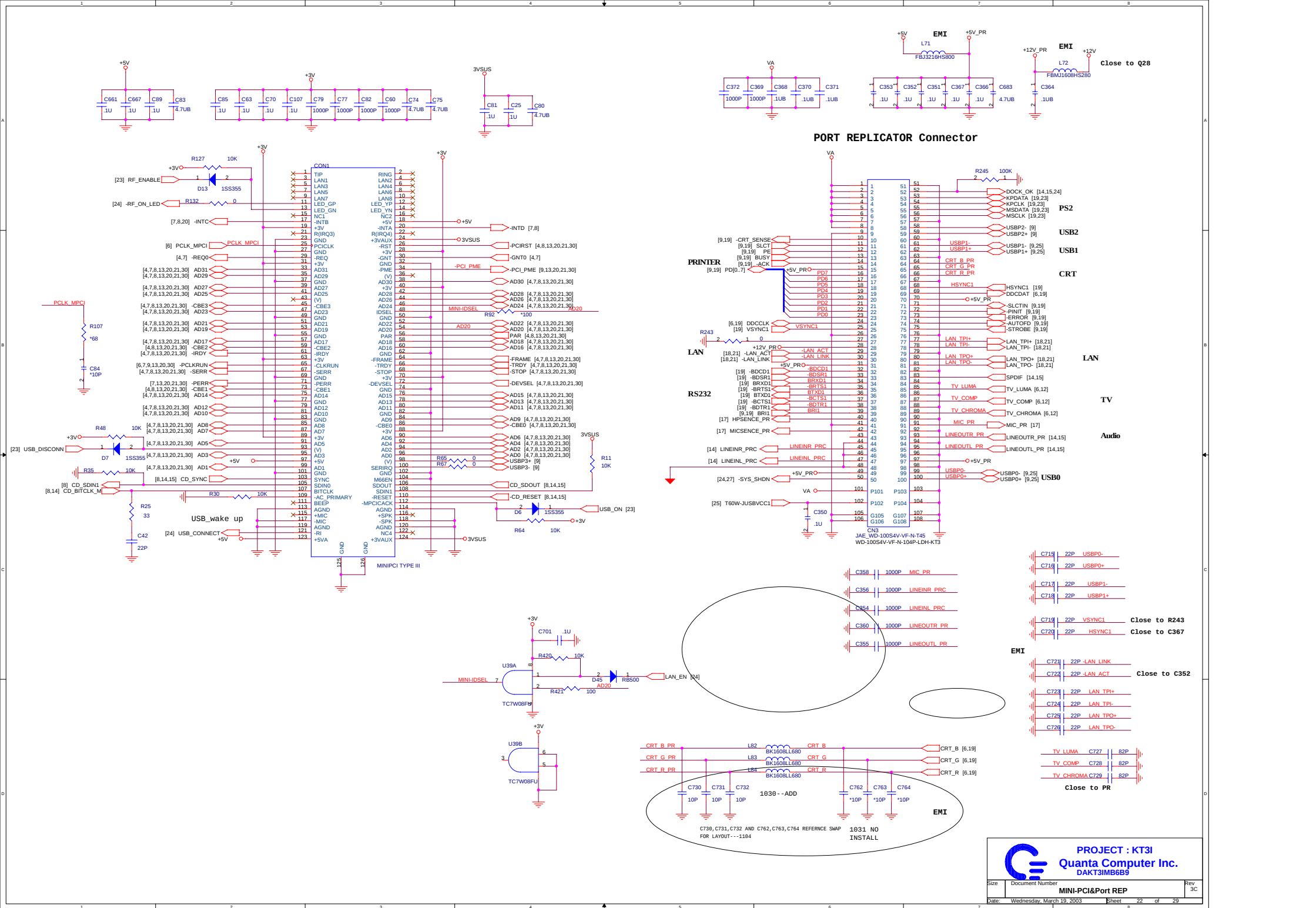
Overlay these two components

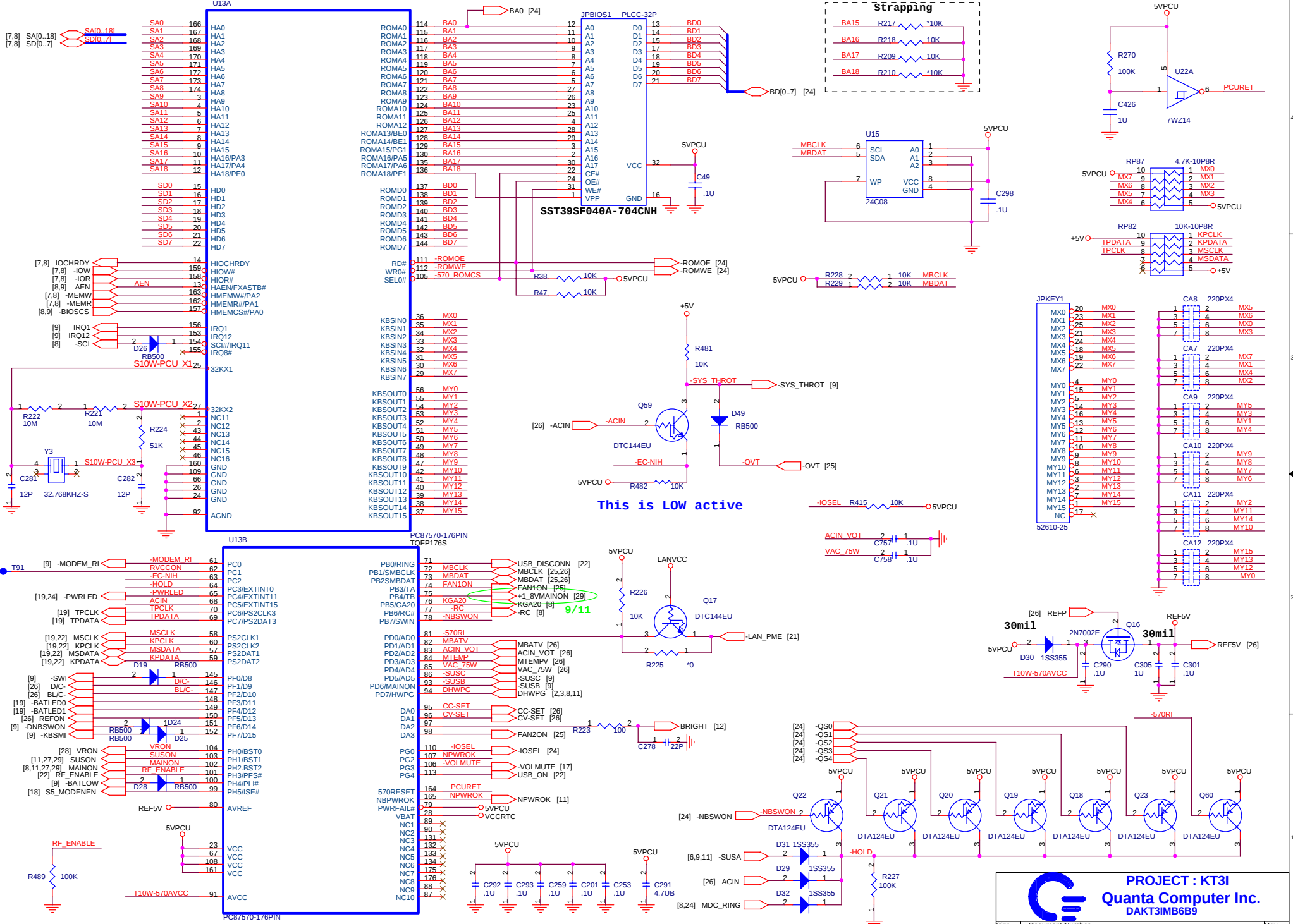
DAP202U Vf=1.2V

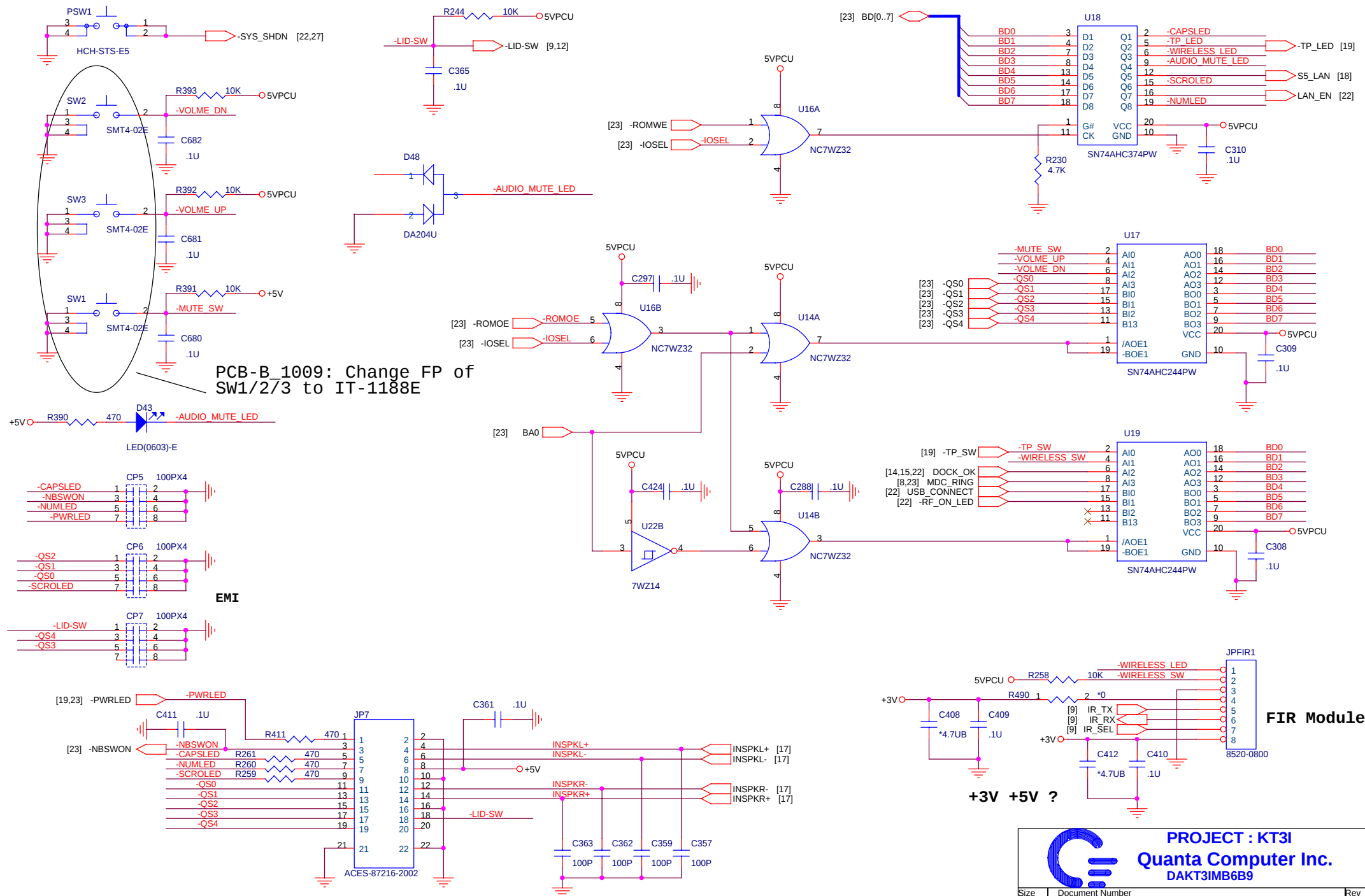


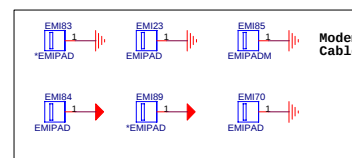
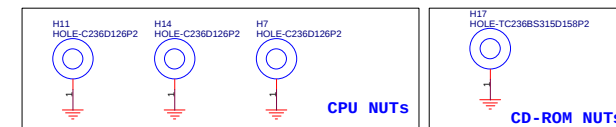
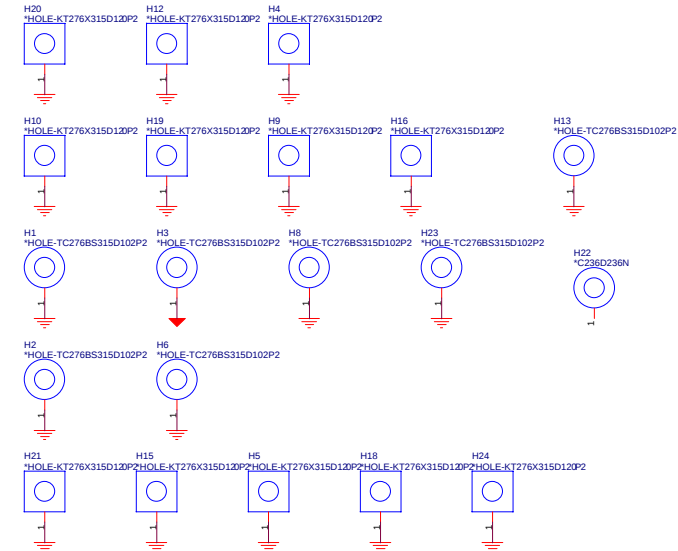
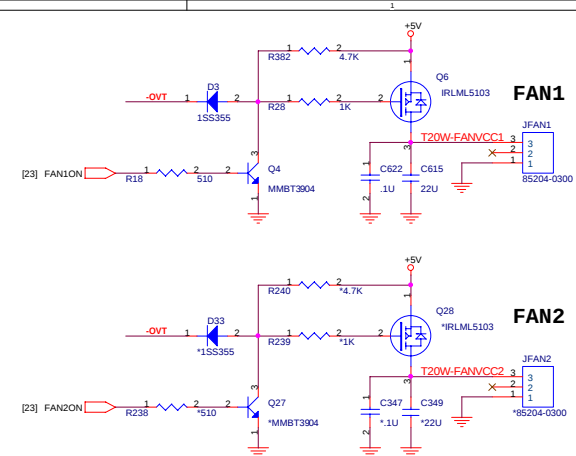
PROJECT : KT3I
Quanta Computer Inc.
DAKT3IMB6B9

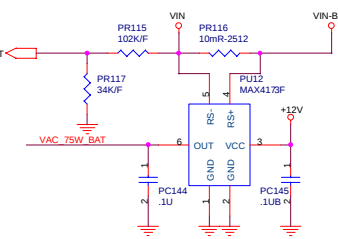
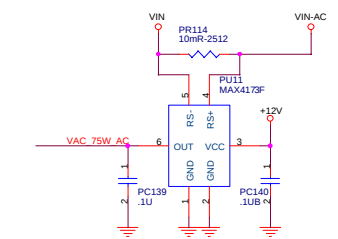
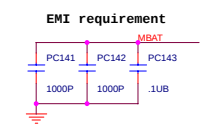
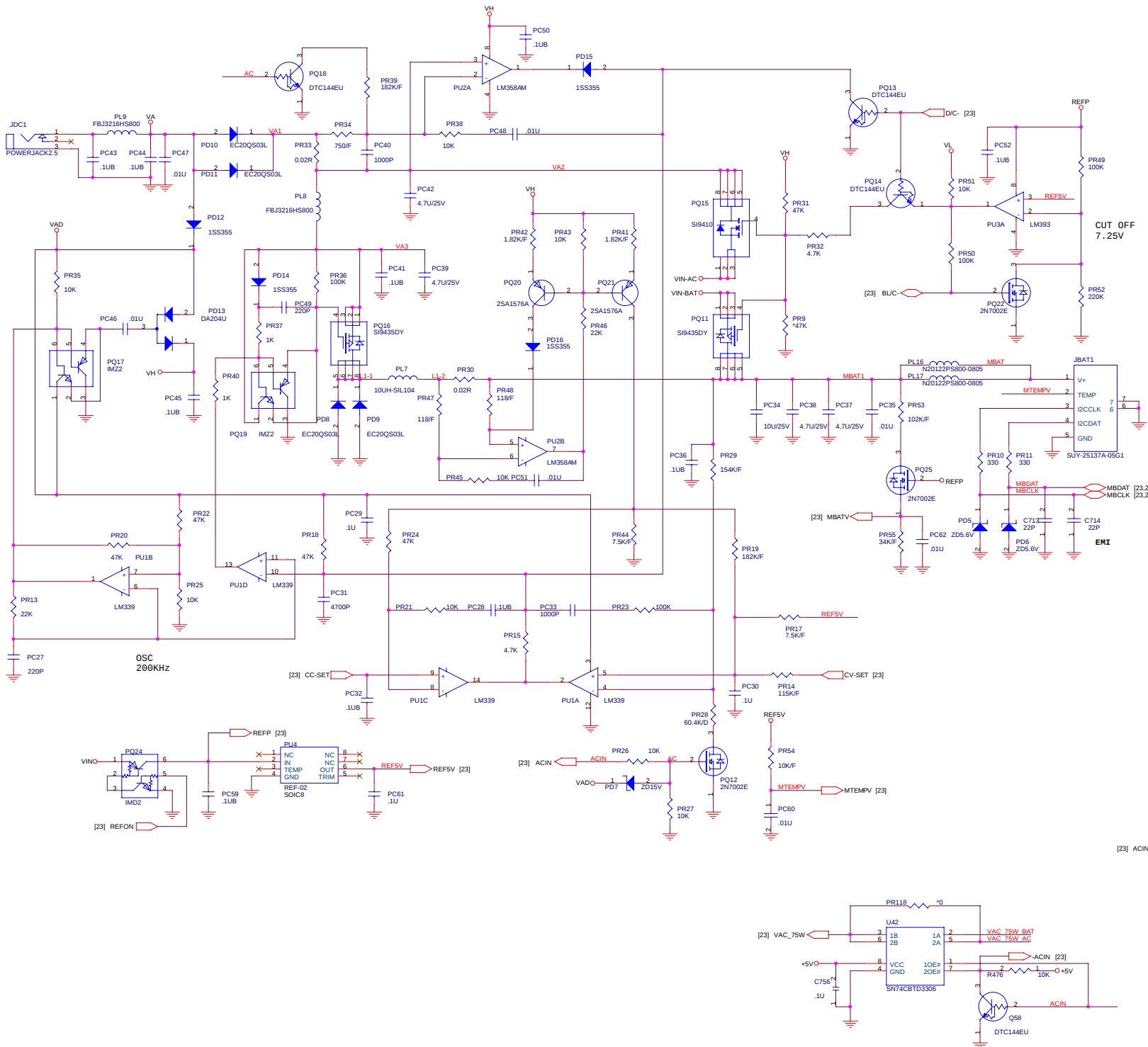
Size B	Document Number NS-83816VNG(LAN)	Rev 3C
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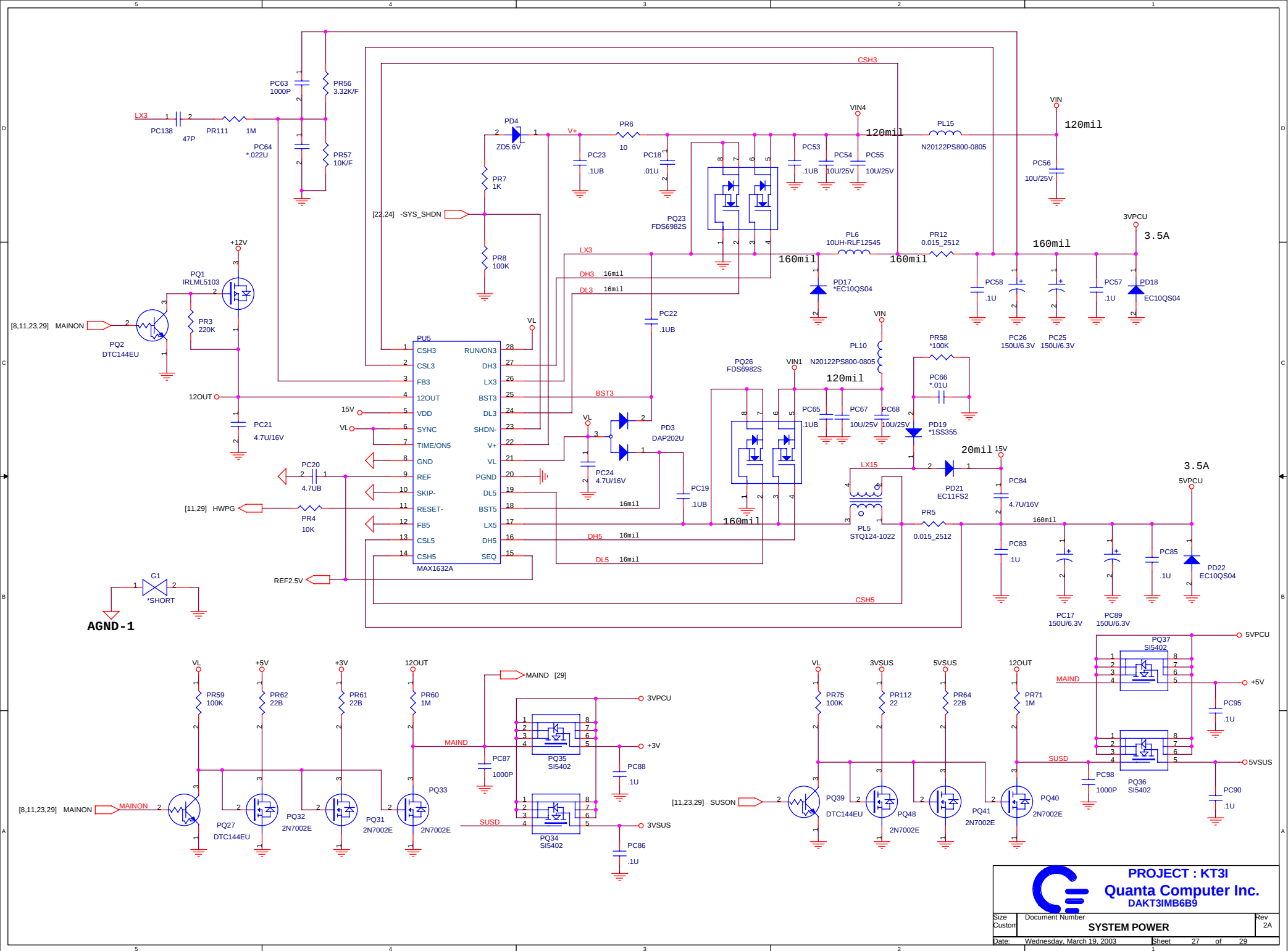










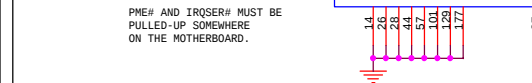


Could change to 5VSUS ?

Use 2.5V CAPs can be better ? 27A

Could change to 5VSUS ?

[13] CB_RSMRST#  CB_RSMRST# R491 1  20



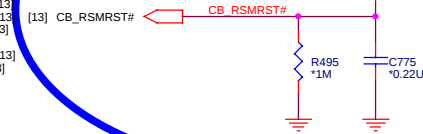
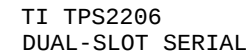
02 MICRO
CARDBUS CONTROLLER
0Z6933 TQFP

THE SERIAL IRQ SIGNAL MUST BE
PULLED-UP BY 10K ON THE MLB.

THE TWO SOCKET ACTIVITY SIGNALS MAY
BE ORED TOGETHER FOR A SINGLE SIGNAL.

THE STRAPPING RESISTORS ON SLATCH AND
SDATA CONFIGURE 026933 FOR SERIAL POW
(SEE BOTTOM OF PAGE)

THE 026933 DEFAULTS TO PCI INT. MODE.
(The BIOS must program PCI/WAY mode)



[8,9] SB_CLK32KO 3  1 SCLK



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