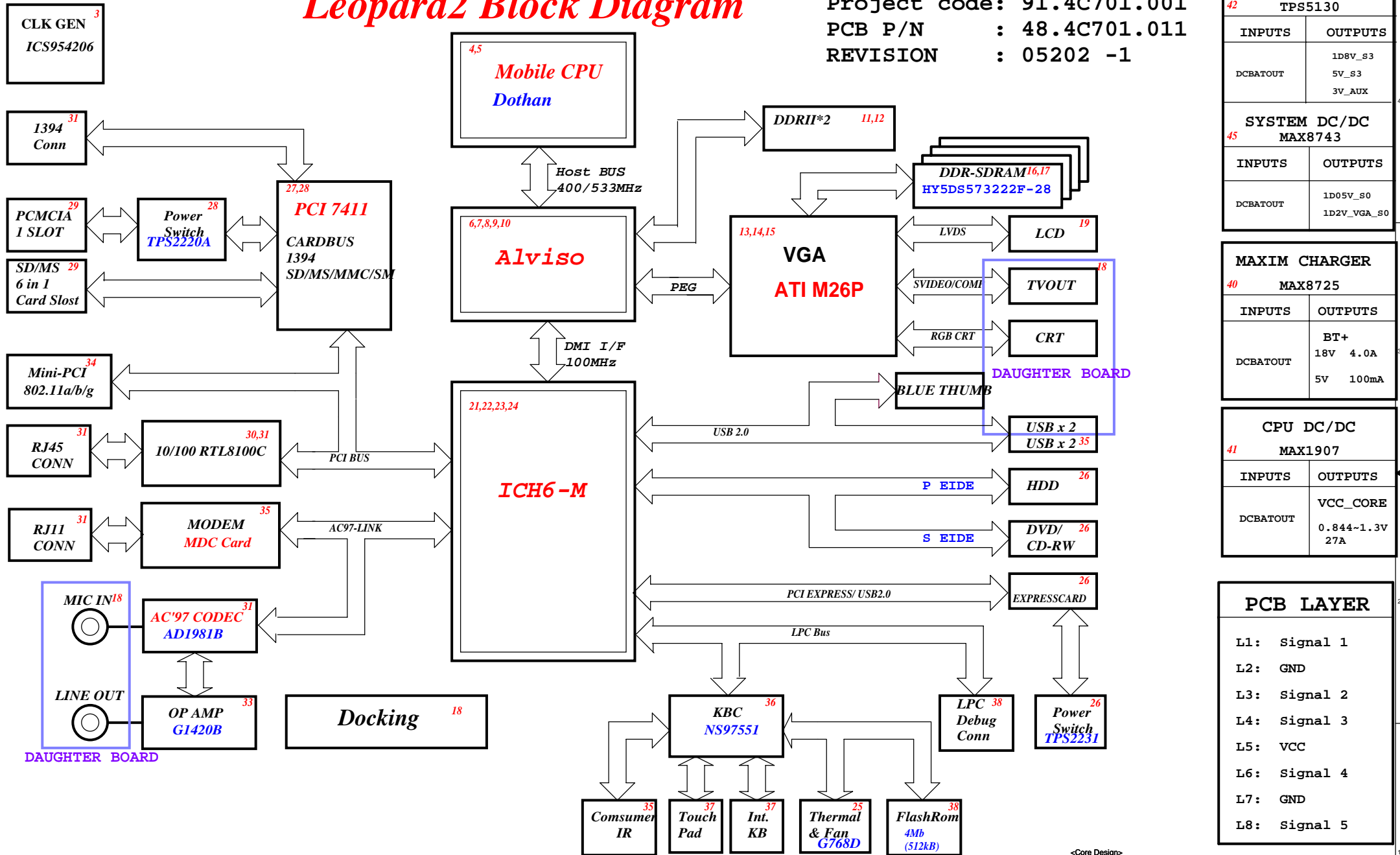


# Leopard2 Block Diagram

Project code: 91.4C701.001  
PCB P/N : 48.4C701.011  
REVISION : 05202 -1



ICH6-M Integrated Pull-up  
and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]/GPO[17], GNT[6]/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series  
Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

Power name description

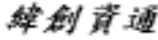
5V\_S0= 5 Voltage power up on system work(S0 state)  
5V\_S3= 5 Voltage suspend to RAM(S3 state)  
5V\_S5= 5 Voltage soft off(S5 state)  
3D3V\_S0= 3.3 Voltage power up on system work(S0 state)  
3D3V\_S3= 3.3 Voltage suspend to RAM(S3 state)  
3D3V\_S5= 3.3 Voltage soft off(S5 state)  
LVDDR\_2D8V= 2.8 Voltage power up on system work(S0 state)  
1D8V\_S3= 1.8 Voltage suspend to RAM(S3 state)  
2D5V\_S0= 2.5 Voltage power up on system work(S0 state)

VCC\_CORE\_S0= CPU VID Voltage power up on system work(S0 state)  
1D5V\_VCCA\_S0= 1.5 Voltage power up on system work(S0 state)  
1D5V\_S0= 1.5 Voltage power up on system work(S0 state)  
1D5V\_S5= 1.5 Voltage soft off(S5 state)  
DDR\_VREF= 0.9 Voltage power up on system work(S0 state)  
1D2V\_VGA\_S0= 1.2 Voltage power up on system work(S0 state) for VGA  
VRAM\_VDDQ= 1.8 Voltage power up on system work(S0 state) for VRAM  
1D05V\_S0= 1.05 Voltage power up on system work(S0 state)  
CORE\_GMCH\_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power  
VCCP\_GMCH\_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0# /GNT0#
Cardbus Controller TI7411	AD22	(CARBUS)P_INTG# (1394)P_INTF# (CARD READER)P_INTG#	REQ1# /GNT1#
LAN	AD23	P_INTE#	REQ2# /GNT2#
Blue Thumb	AD24		

<Core Design>



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Title

ITP

Size  
A3

Document Number  
Leopard2

Rev  
-1

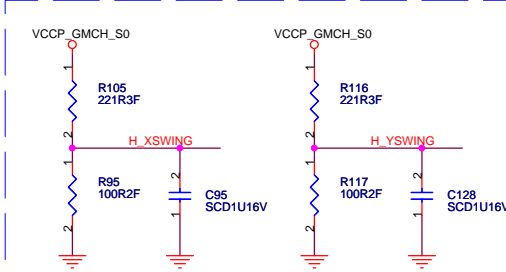
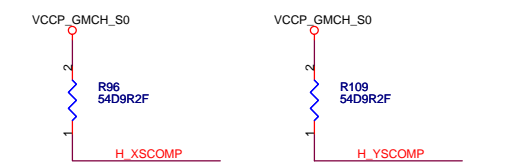
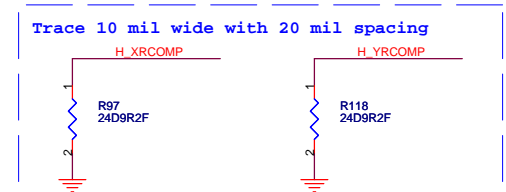
Date: Wednesday, July 06, 2005

Sheet 2 of 47









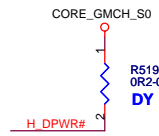
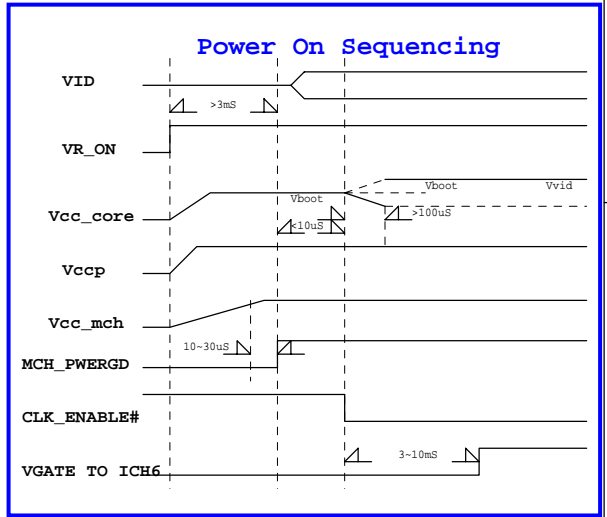
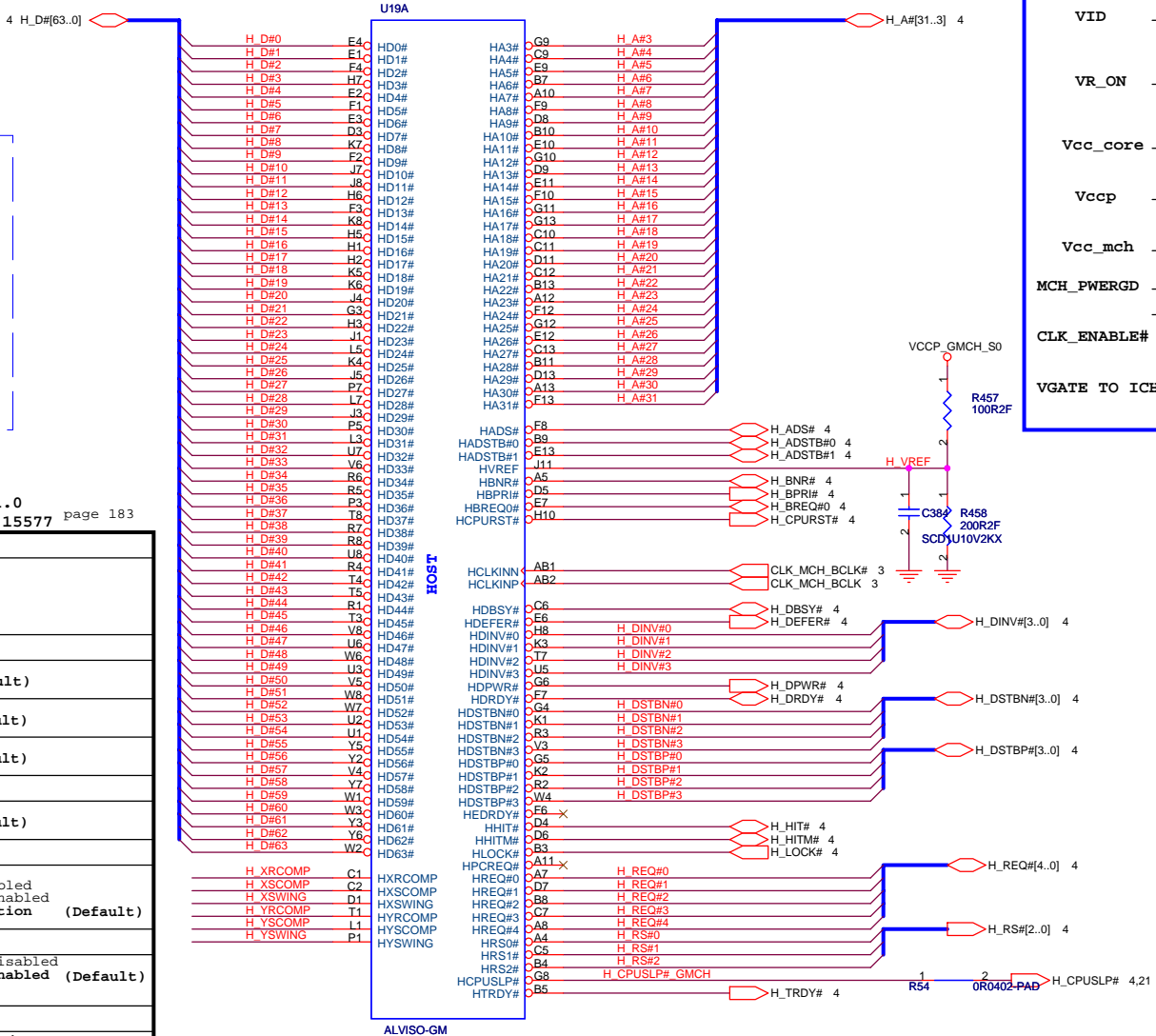
Trace 10 mil wide with 20 mil spacing

## Alviso Strapping Signals and Configuration

REV.NO. 1.0  
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 101 = FSB400 others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	0 = DDR2 1 = DDR1 (Default)
CFG7	CPU Strap	0 = Reserved 1 = Dothan (Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes 1 = Normal (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	GMCH core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCTRL_DATA	SDVO Present	0 = No SDVO device present(Default) 1 = SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORX in signal.



ALVISO-GM:71.0GMCH.08U  
ALVISO-PM:71.0GMCH.0BU  
ALVISO-GML:71.0GMCH.0JU



Alviso will provide SDVO\_CTRLCLK  
and CTRLDATA pulldowns on-die

Intel suggest NC Due to votusly DVO

TPAD30 TP22 SDVO DAT  
TPAD30 TP23 SDVO CLK  
3 CLK\_MCH\_3GPLL  
3 CLK\_MCH\_3GPLL

CORE\_GMCH\_S0

Intel design guide suggest  
Ref no.:14511  
page 210

Note: Intel design guide  
suggest(page 203)  
If the LVDS interface is  
not implemented, all  
signals associated with  
the interface can be left  
as no connects.

Place 150 Ohm termination resistors close to GMCH

Note:  
CRT\_RED,  
CRT\_GREEN,  
CRT\_BLUE, are  
ground  
referenced.

BM\_BUSY#  
EXT\_TS1#  
THRMTRIP#  
PWROK  
RSTIN#  
R536  
100R2  
PLT\_RST1# 13,24,26

DREF\_CLK#  
DREF\_CLKP  
DREF\_SSCLK#  
DREF\_SSCLKP  
DREFSSCLK# 3  
DREFSSCLKP 3

NC1 AP37  
NC2 AN37  
NC3 AP36  
NC4 AP2  
NC5 AN1  
NC6 B1  
NC7 A2  
NC8 B37  
NC9 A36  
NC10 A37  
NC11 A37

## Strapping

CFG[17:3] have internal pullup resistors.  
CFG[19:18] have internal pulldown  
resistors

U19B

U19G

1D5V\_S0

13

13

13

13

13

13

13

13

U19B

U19G

1D5V\_S0

13

13

13

13

13

13

13

13

U19B

U19G

1D5V\_S0

13

13

13

13

13

13

13

13

U19B

U19G

1D5V\_S0

13

13

13

13

13

13

13

13

U19B

U19G

1D5V\_S0

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U19B

U19G

1D5V\_S0

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U19B

U19G

1D5V\_S0

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U19B

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U19G

1D5V\_S0

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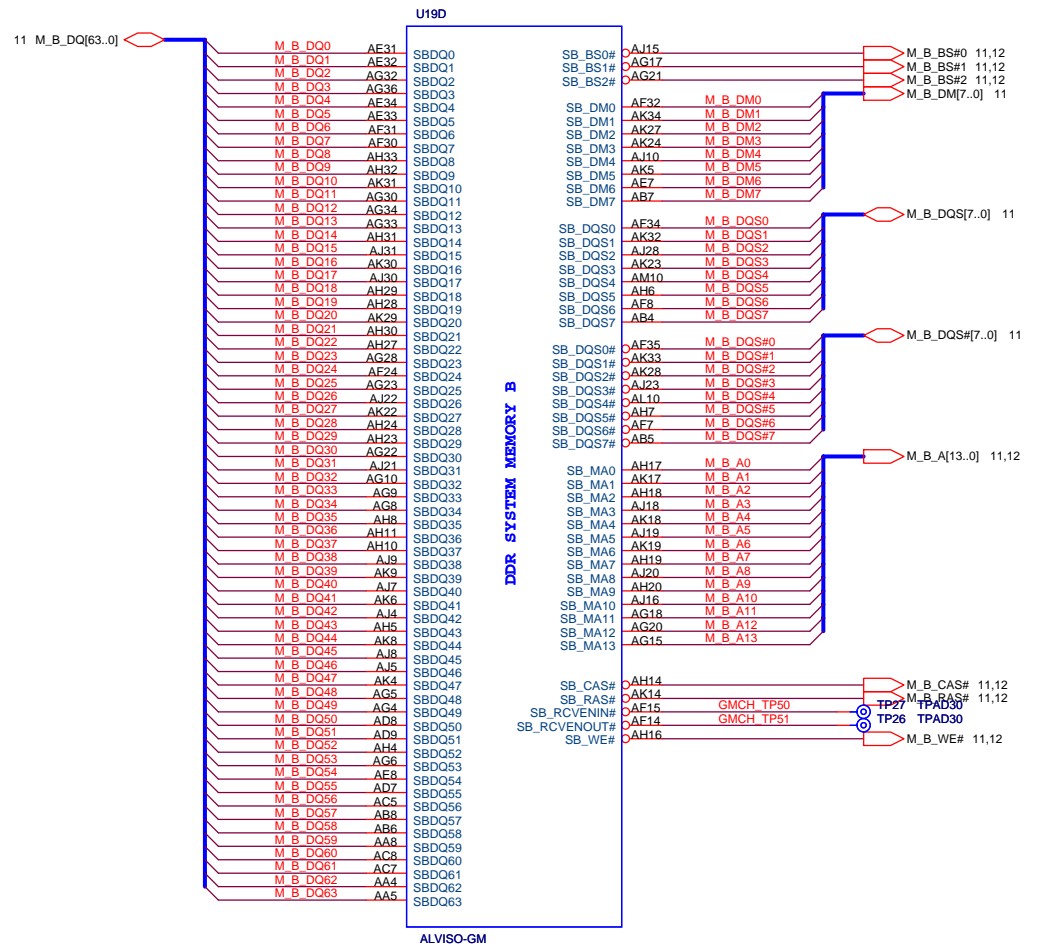
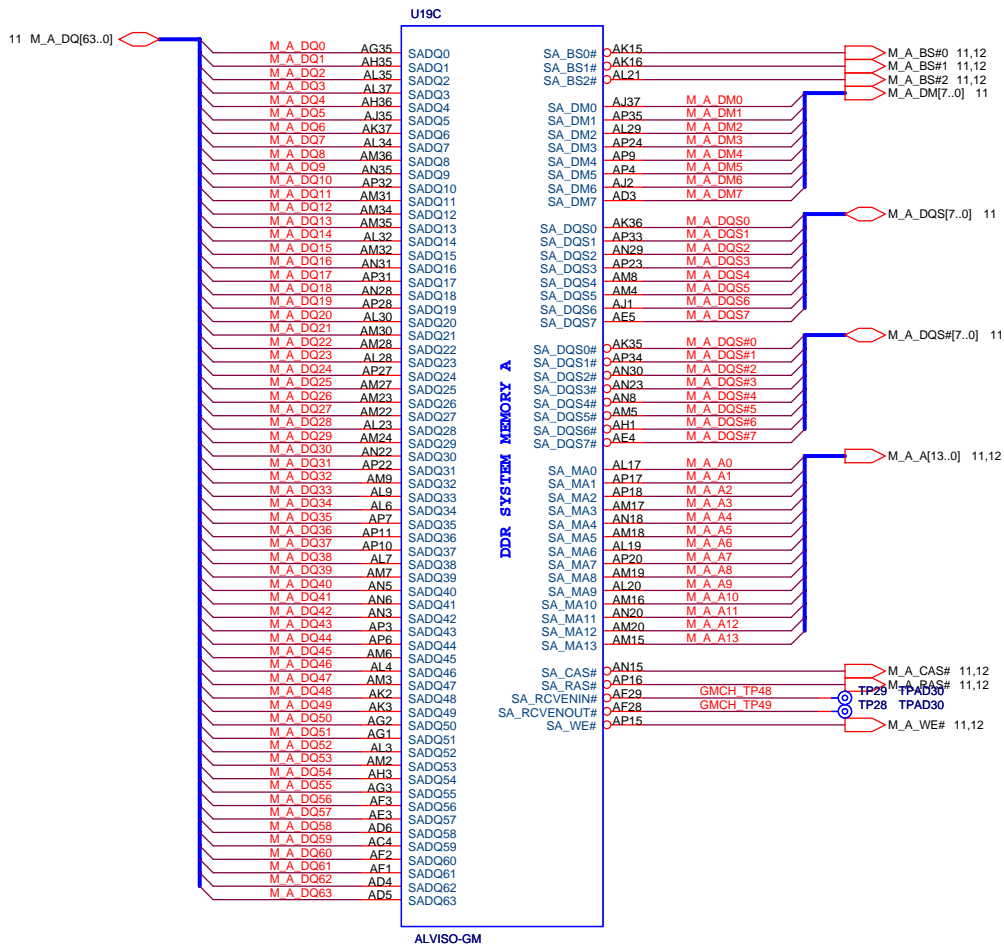
13

13

U19B

U19G

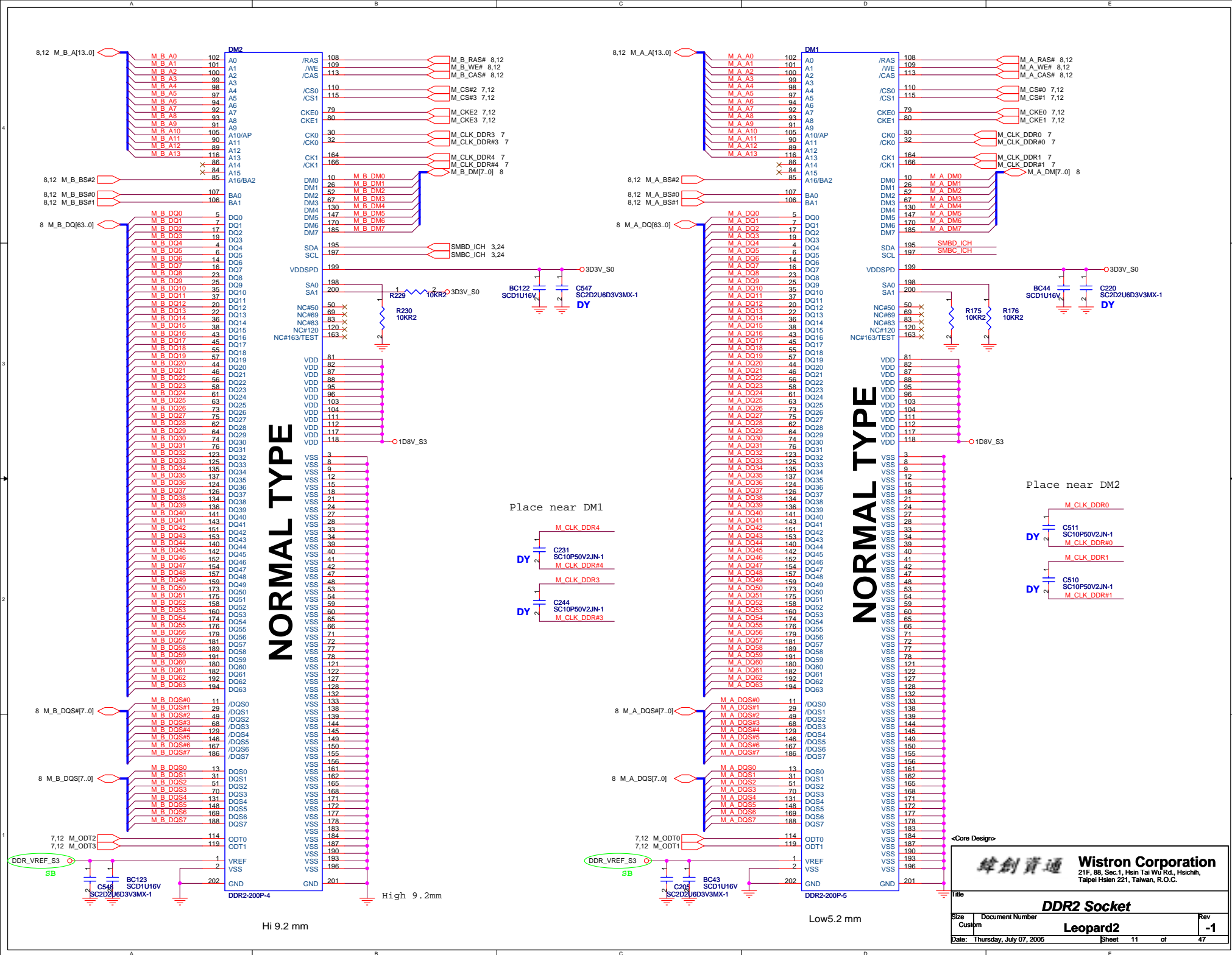
1D5V\_S0









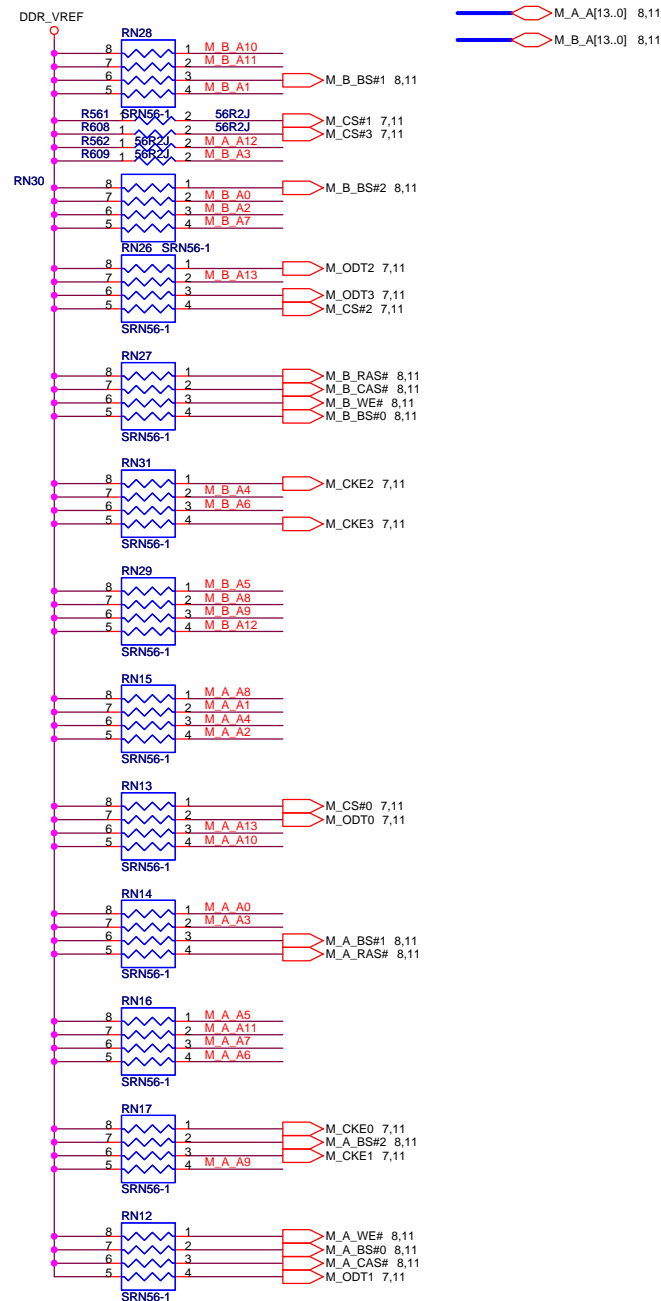


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Title		Rev
DDR2 Socket		-1
Size	Document Number	
Custom		
Date:	Thursday, July 07, 2005	Sheet 11 of 47

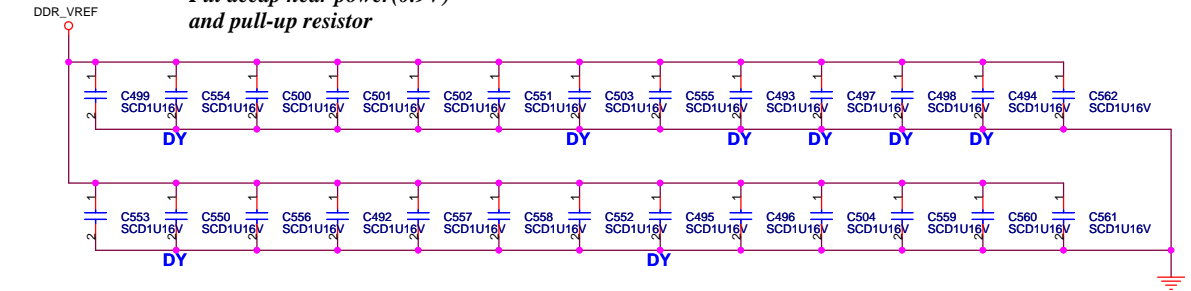
# PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

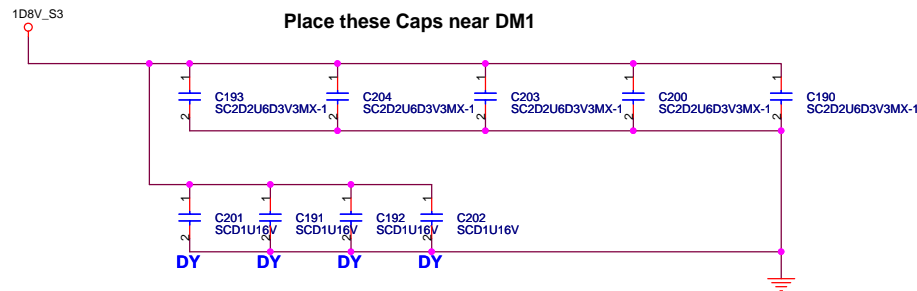


# Decoupling Capacitor

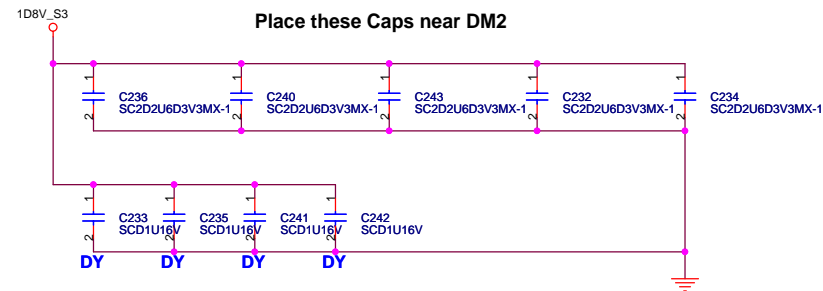
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



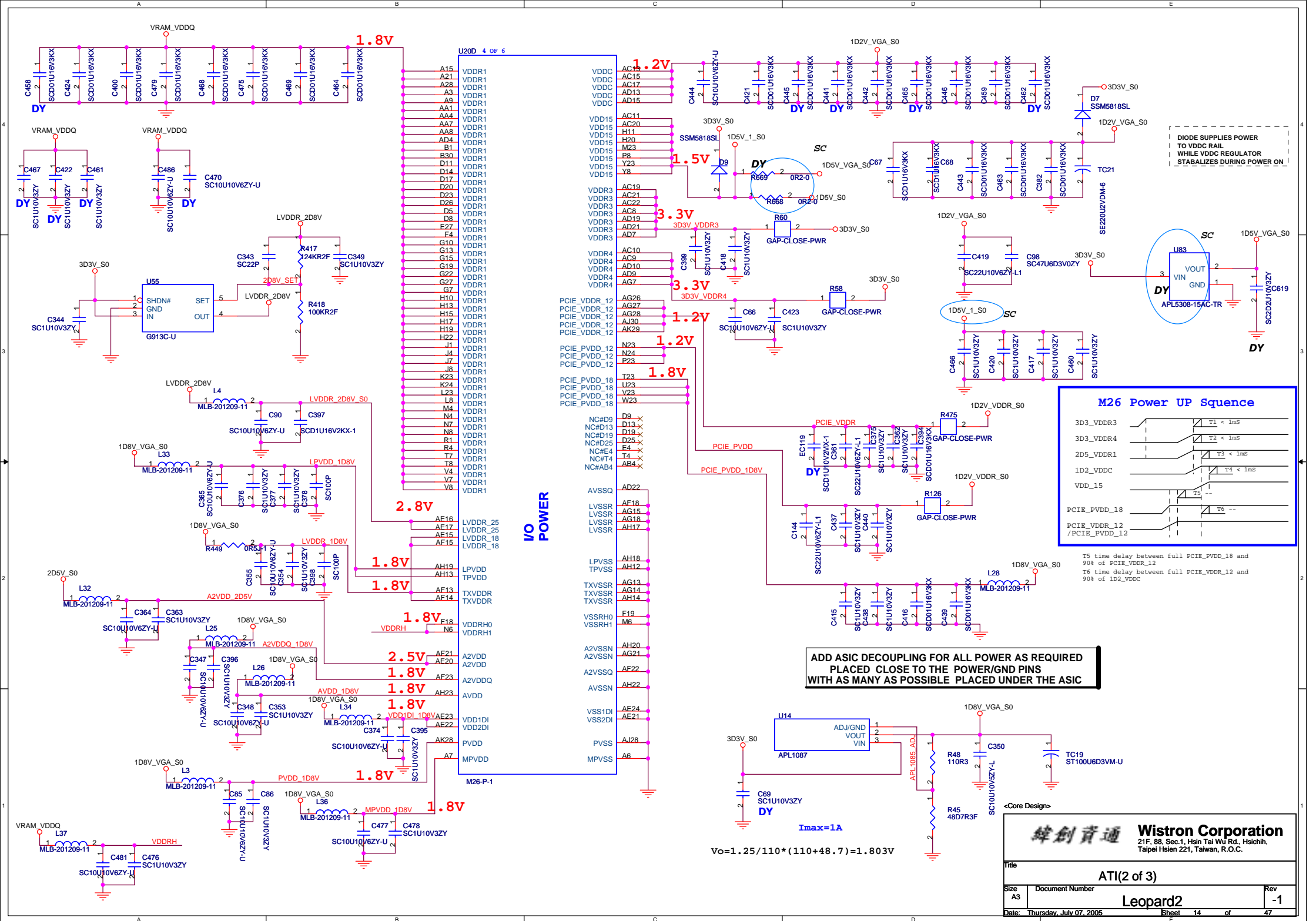
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緯創資通

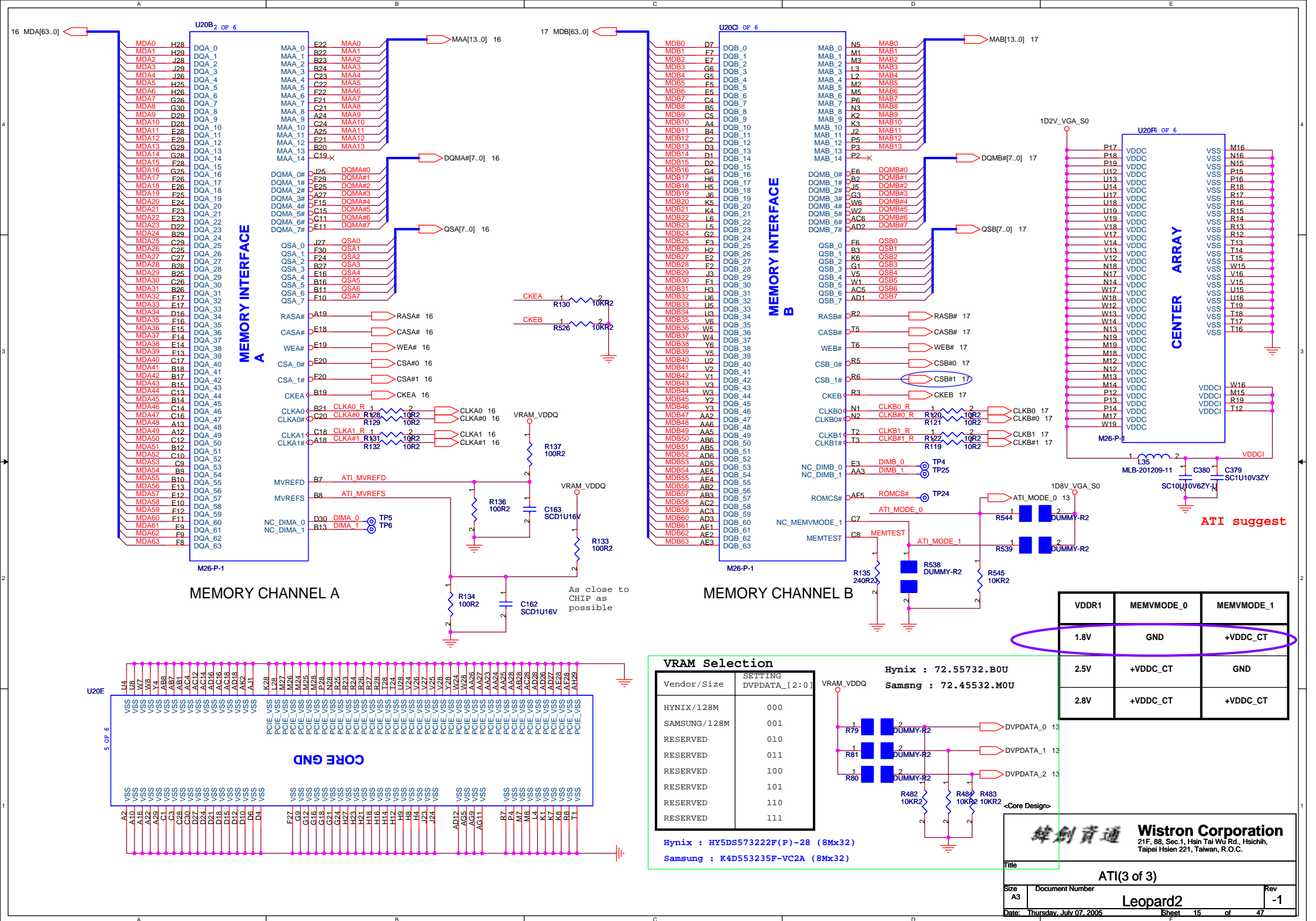
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Title			DDR2 Termination Resistor
Size	Document Number	Rev	
A3		-1	
Date:	Thursday, July 07, 2005	Sheet	12 of 47






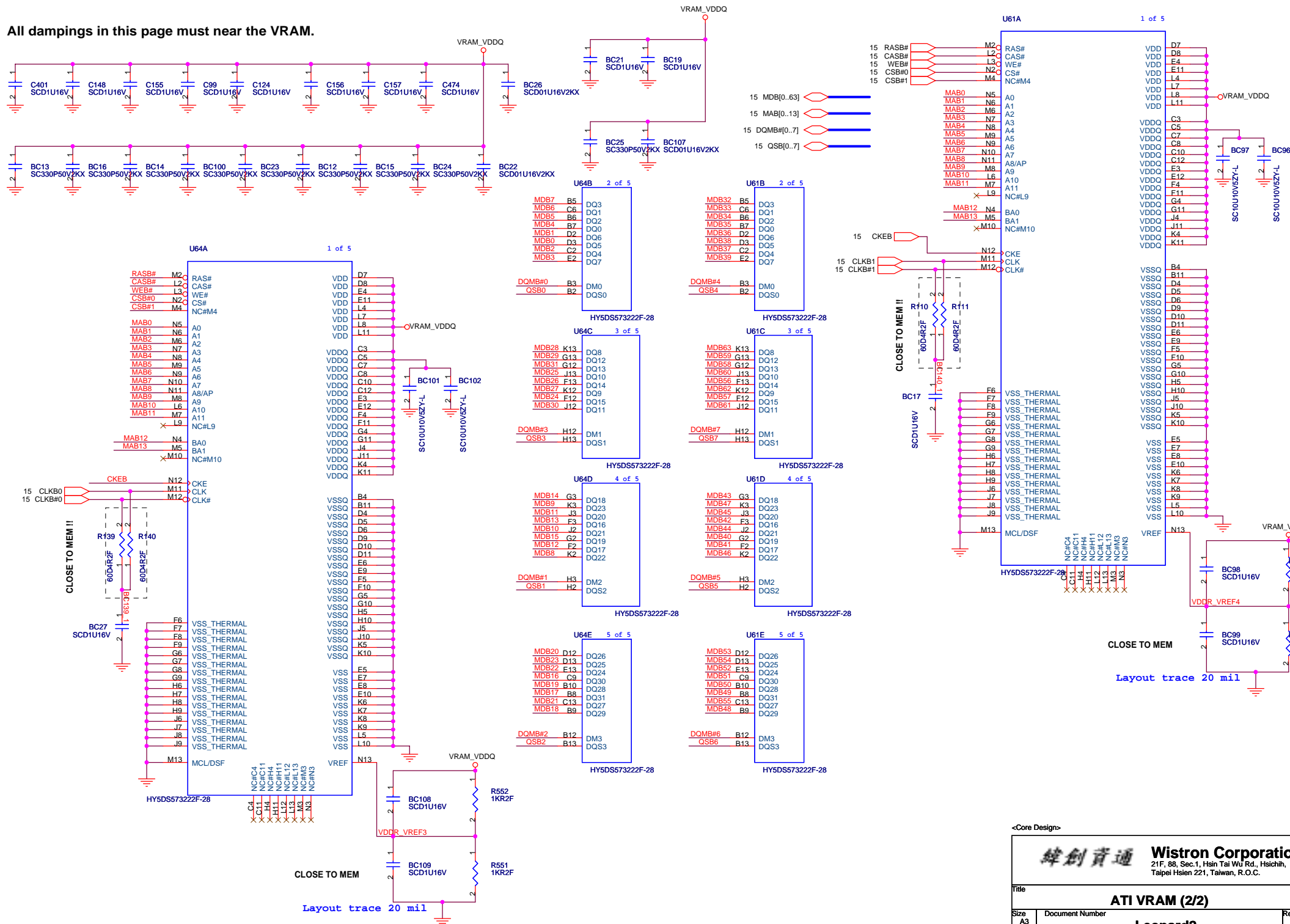




[illegible]

<div> <div>  <div> <div>緯創資通</div> <div> Wistron Corporation  21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  Taipei Hsien 221, Taiwan, R.O.C. </div> </div> </div> </div>			
Title			
ATI VRAM (1/2)			
Size A3	Document Number		Rev -1
Date: Thursday, July 07, 2005		Sheet 16 of	47

All dampings in this page must near the VRAM.



<Core Design>

緯創資通

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Title

**ATI VRAM (2/2)**

Size

Document Number

**Leopard2**

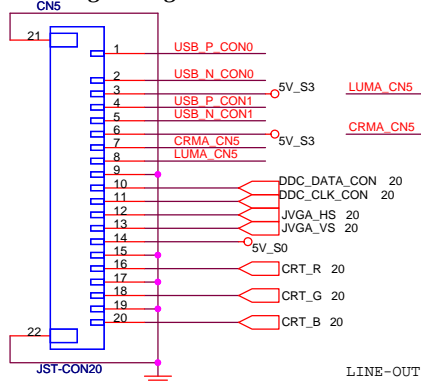
Rev

**-1**

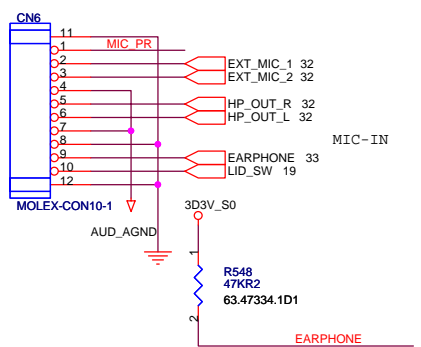
Date: Thursday, July 07, 2005

Sheet 17 of 47

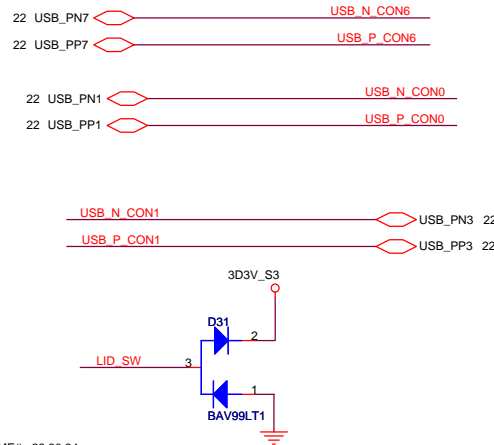
## Digital Signal CONN



## Analog Signal CONN

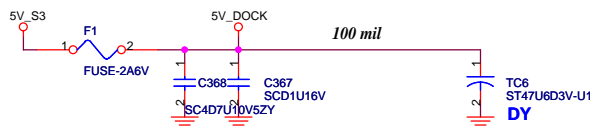
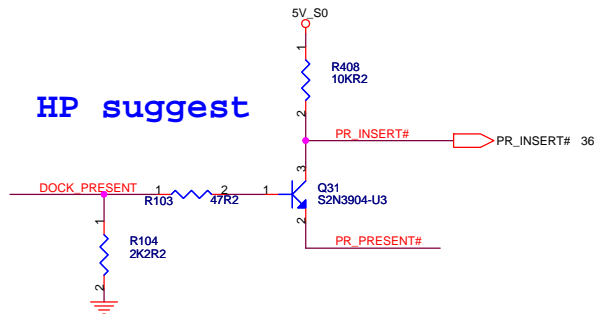


## Close to Docking CN

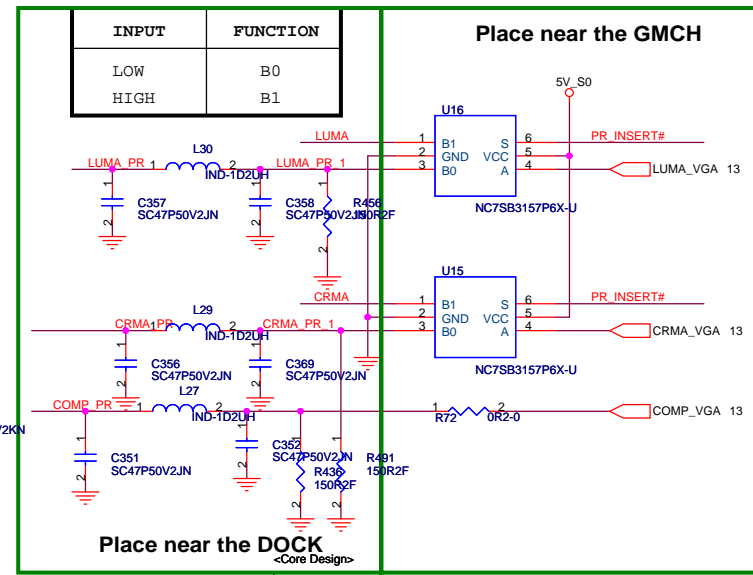
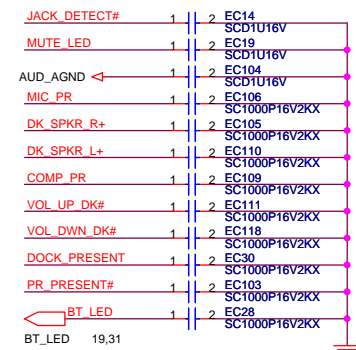
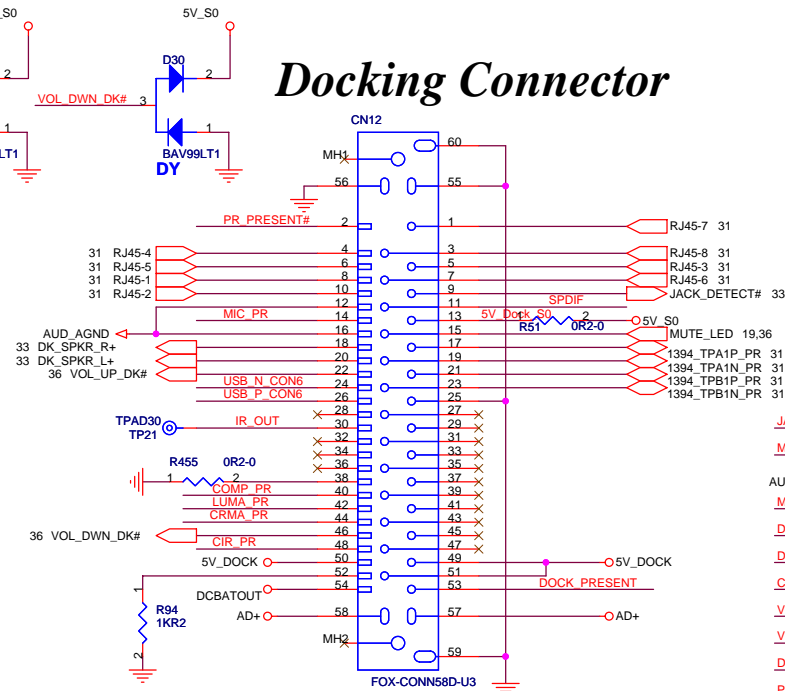


Please close to ICH6

## HP suggest



## Docking Connector

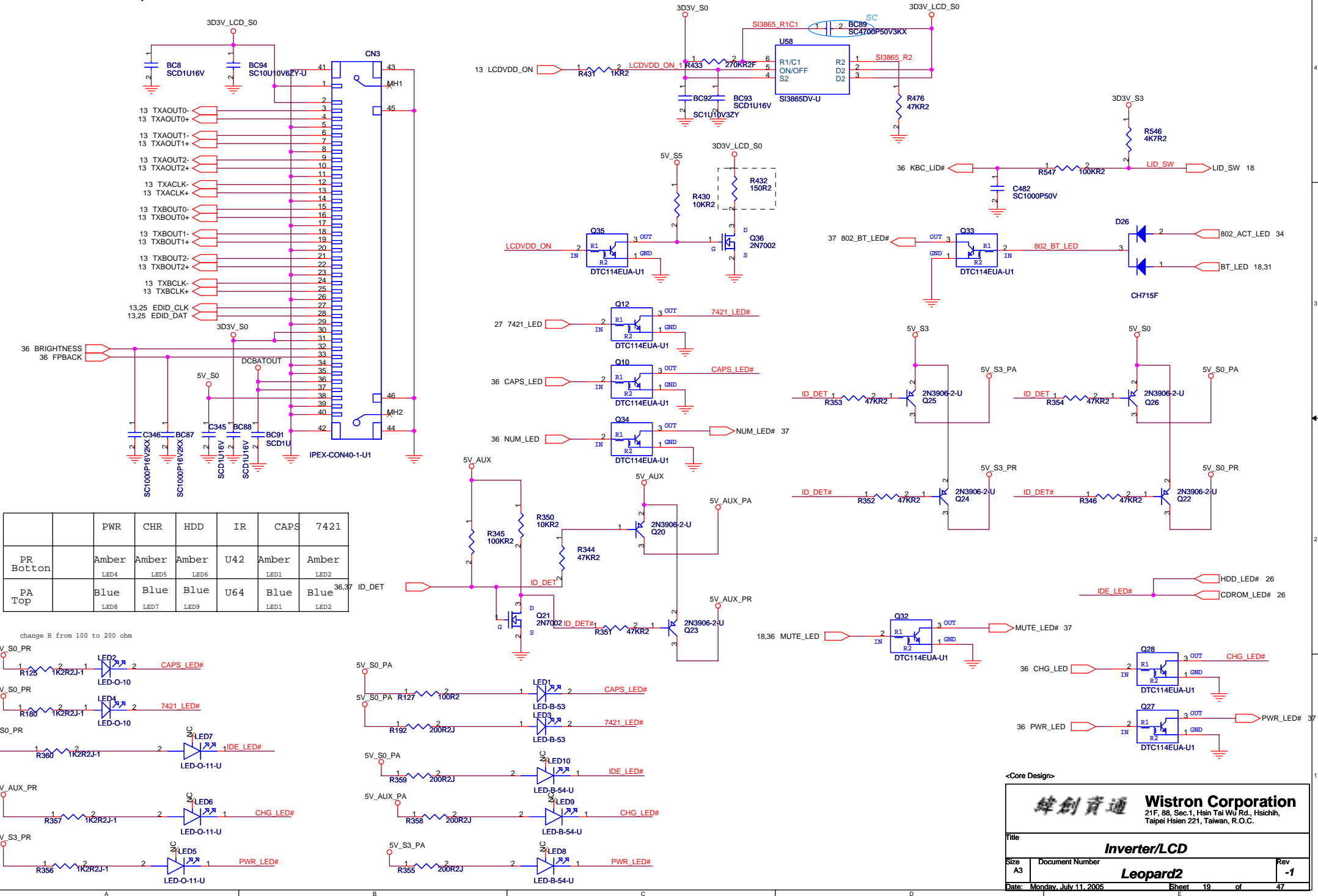


Place near the DOCK  
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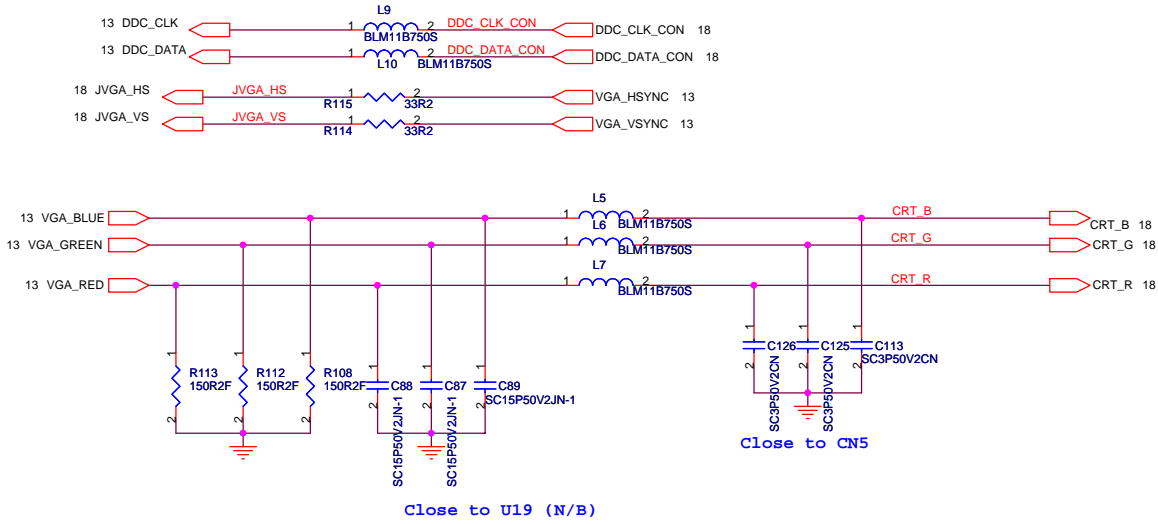
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

CIR, CIR\_PR, CIR\_KBC are connect together. default setting 12/12

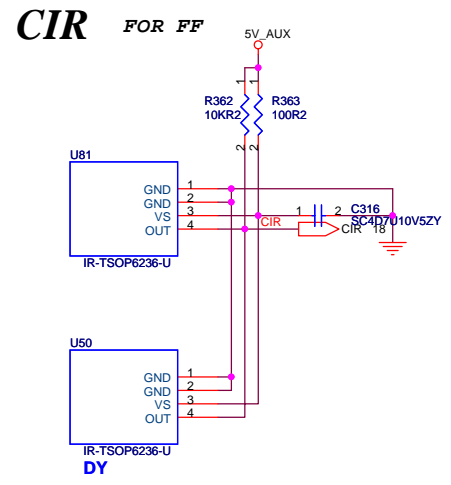
INVERTER / LCD



# CRT

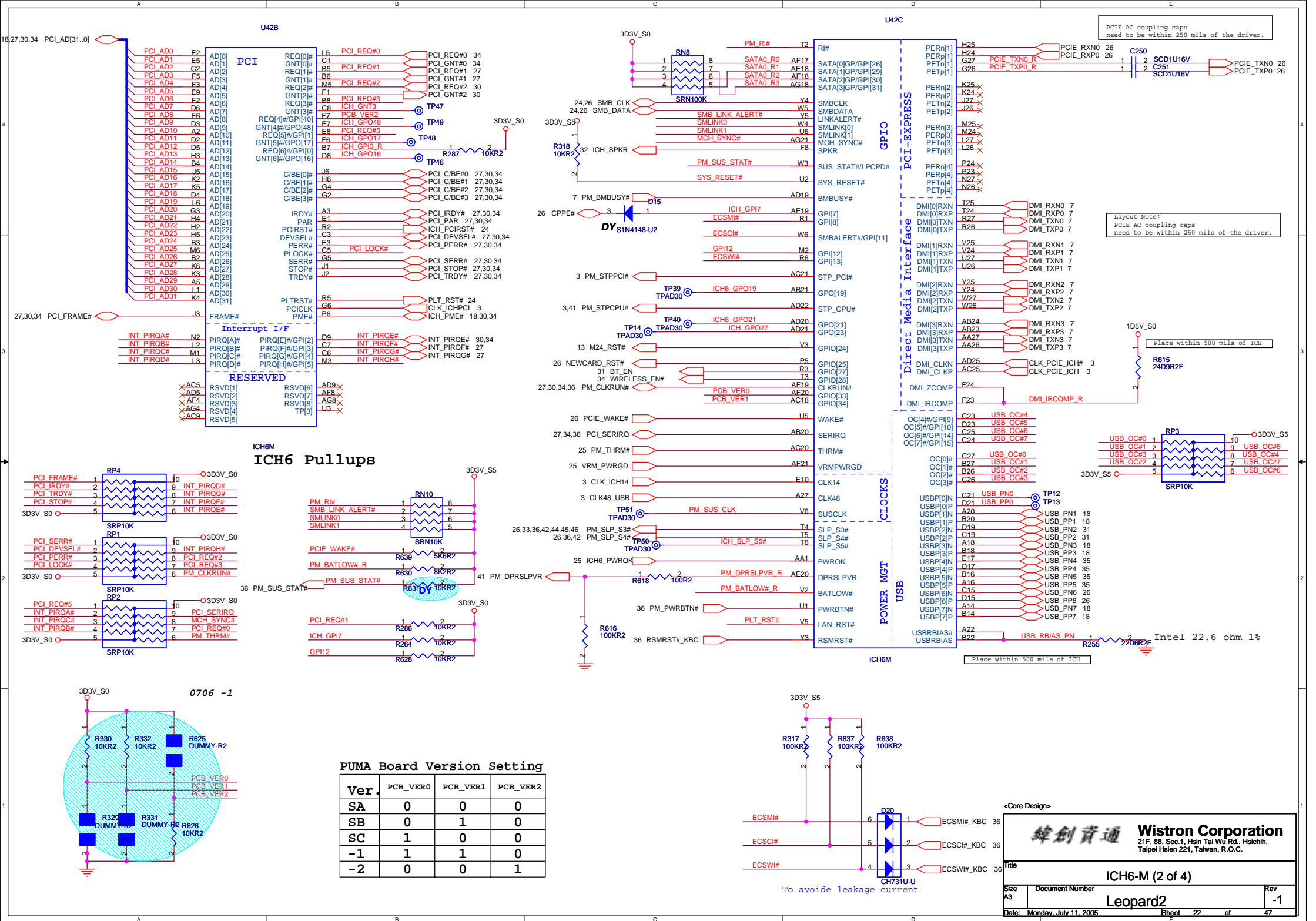


010804 Modified on Astro ID request









Layout Note:  
Place above caps within  
100 mils of ICH near F27, P27, AB27

Layout Note:  
IDE decoupling

Layout Note:  
PCI decoupling

Place within 100  
mils of ICH  
near pin AG5

Place within 100  
mils of ICH  
near pin AG9

Place within 100  
mils of ICH

Place within 100  
mils of ICH  
near E26, E27

Place within 100  
mils of ICH  
pin AG10

Intel dummy  
Place within 100  
mils of ICH  
pin A13

Place within 100  
mils of ICH  
pin V7

Place within 100  
mils of ICH  
pin A17

Layout Note:  
Place near pin AA19

Place within 100  
mils of ICH pin  
AG13, AG16

Layout Note:  
Distribute in PCI section  
near pin A2-A6 near D1-H1

Layout Note:  
Place near U7

Place both  
within 100 mils  
of ICH near D27

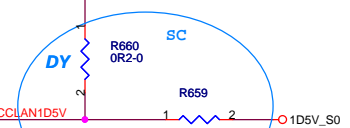
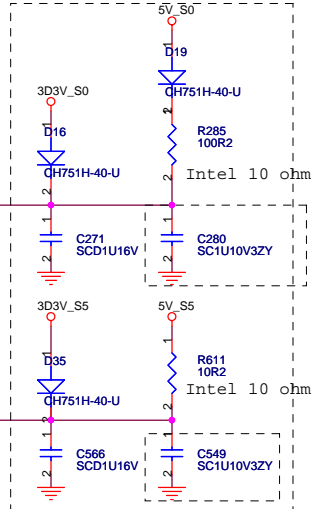
Layout Note:  
Place near AB18

Place within 100  
mils of ICH

Place within 100  
mils of ICH  
pin G10

Layout Note:  
Place near AG23

\*Within a given well, 5VREF needs to be up before the  
corresponding 3.3V rail

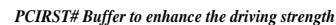
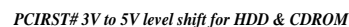
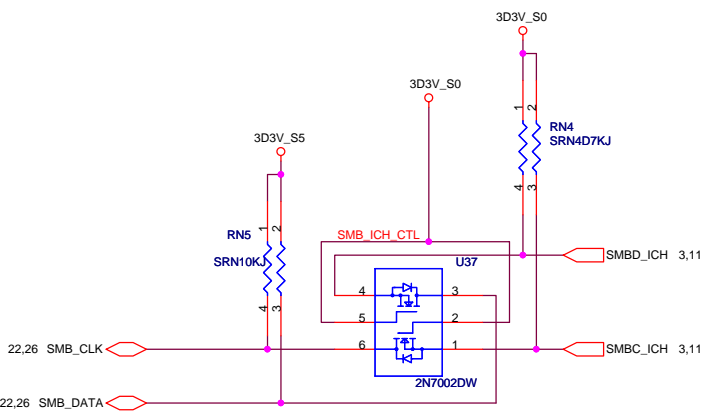



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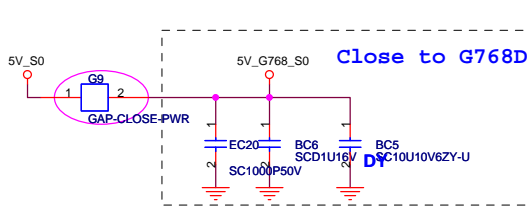
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Size A3 Document Number Rev -1

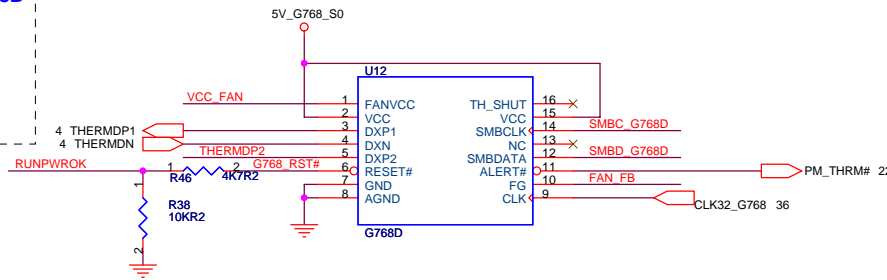
Date: Thursday, July 07, 2005 Sheet 23 of 47



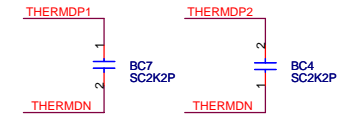
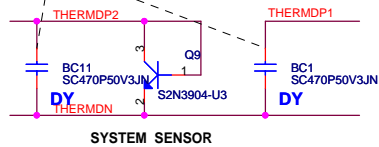
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
		ICH6-M (4 of 4)	
Size A3	Document Number	Rev -1	
Date: Thursday, July 07, 2005		Sheet 24 of 47	
Leopard2			



Reserve for G768B works at High Speed

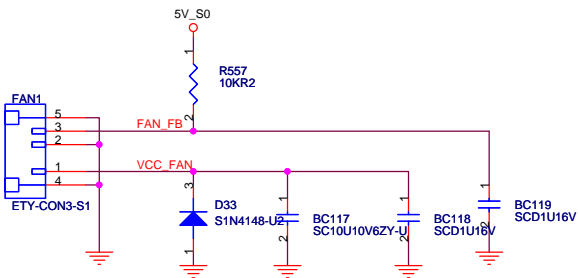


Put these two Caps near the thermal diode.

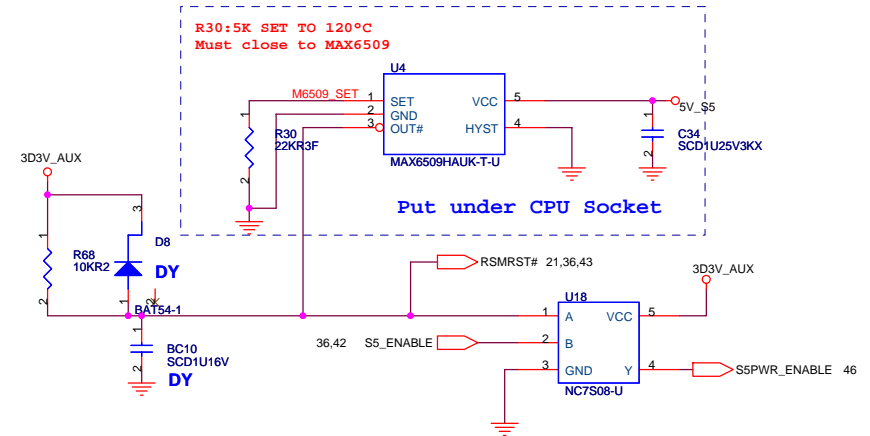
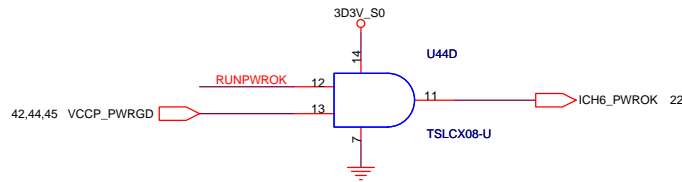
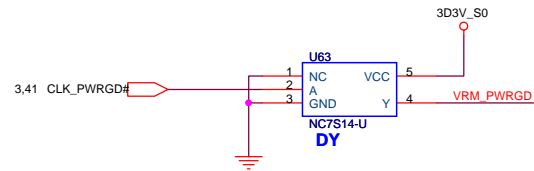


THERMDP1/DP2/THERMDN ON THE SAME LAYER  
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS  
CAPS CLOSE TO G768B

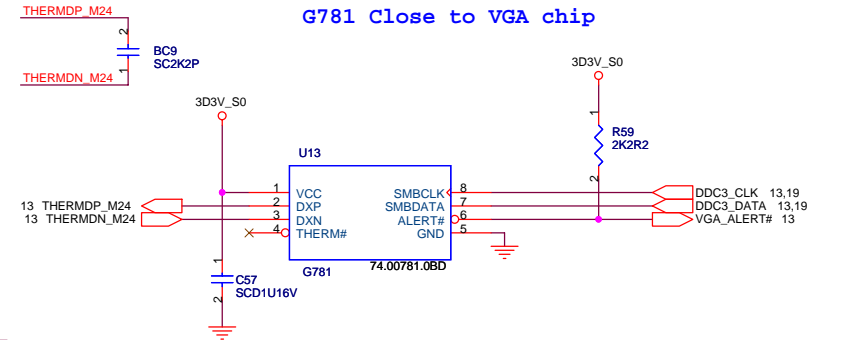
180 ms after VCC\_G768 > 4.38v, p2, 7



The symbol use 2nd source  
The P/N is the main source  
Main source:20.D0152.103  
2nd source:20.D0012.103



G781 Close to VGA chip



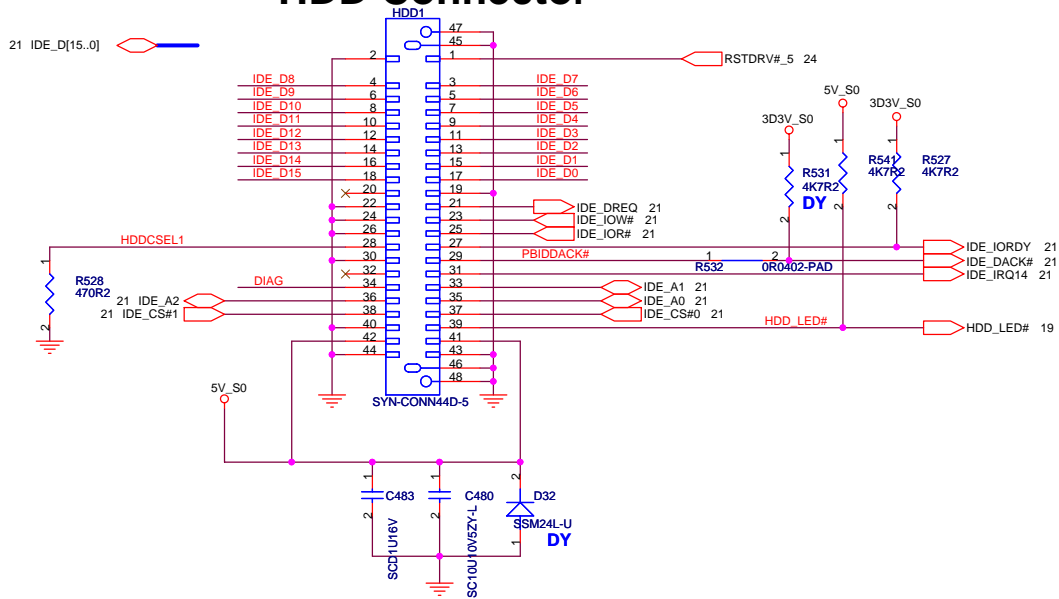
<Core Design>

緯創資通

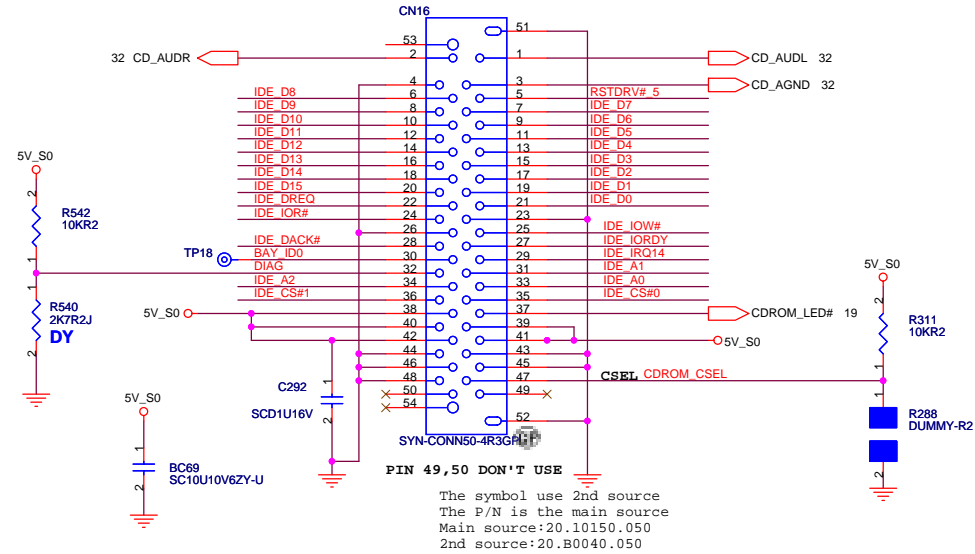
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
G768D		
Size A3	Document Number	Rev -1
Leopard2		
Date: Monday, July 11, 2005	Sheet 25	of 47

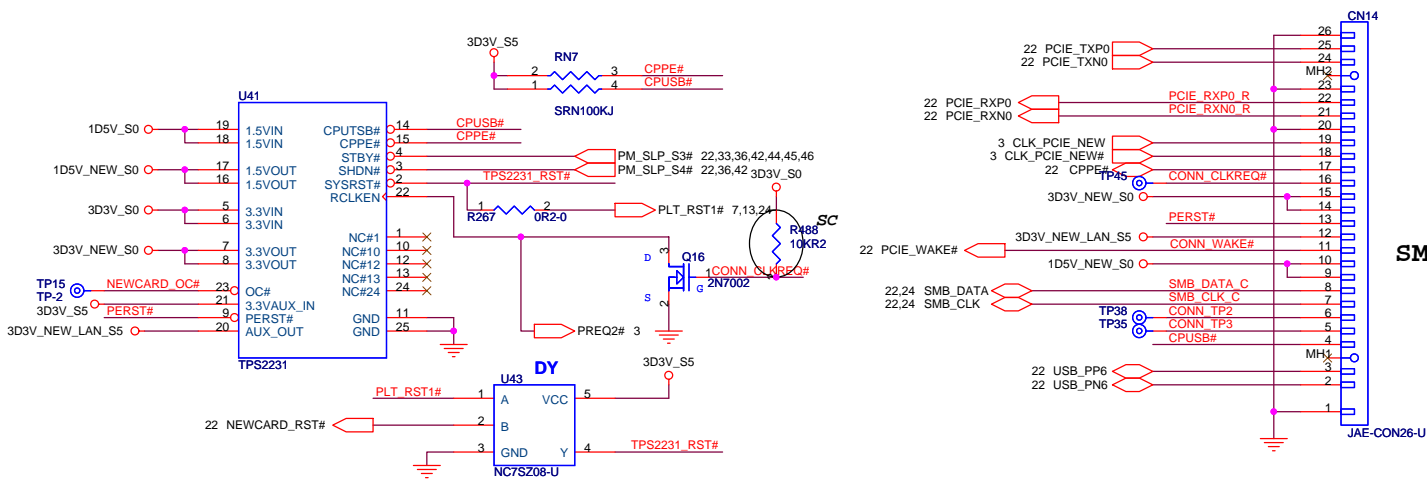
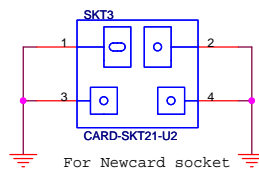
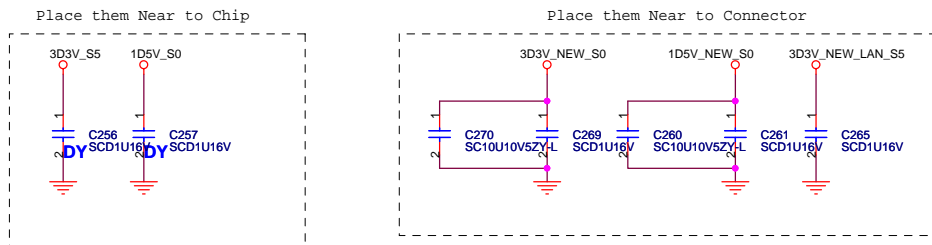
## HDD Connector



## CDROM



## NEWCARD Connector



## SMBUS ( ICH6--NEWCARD, LAN )

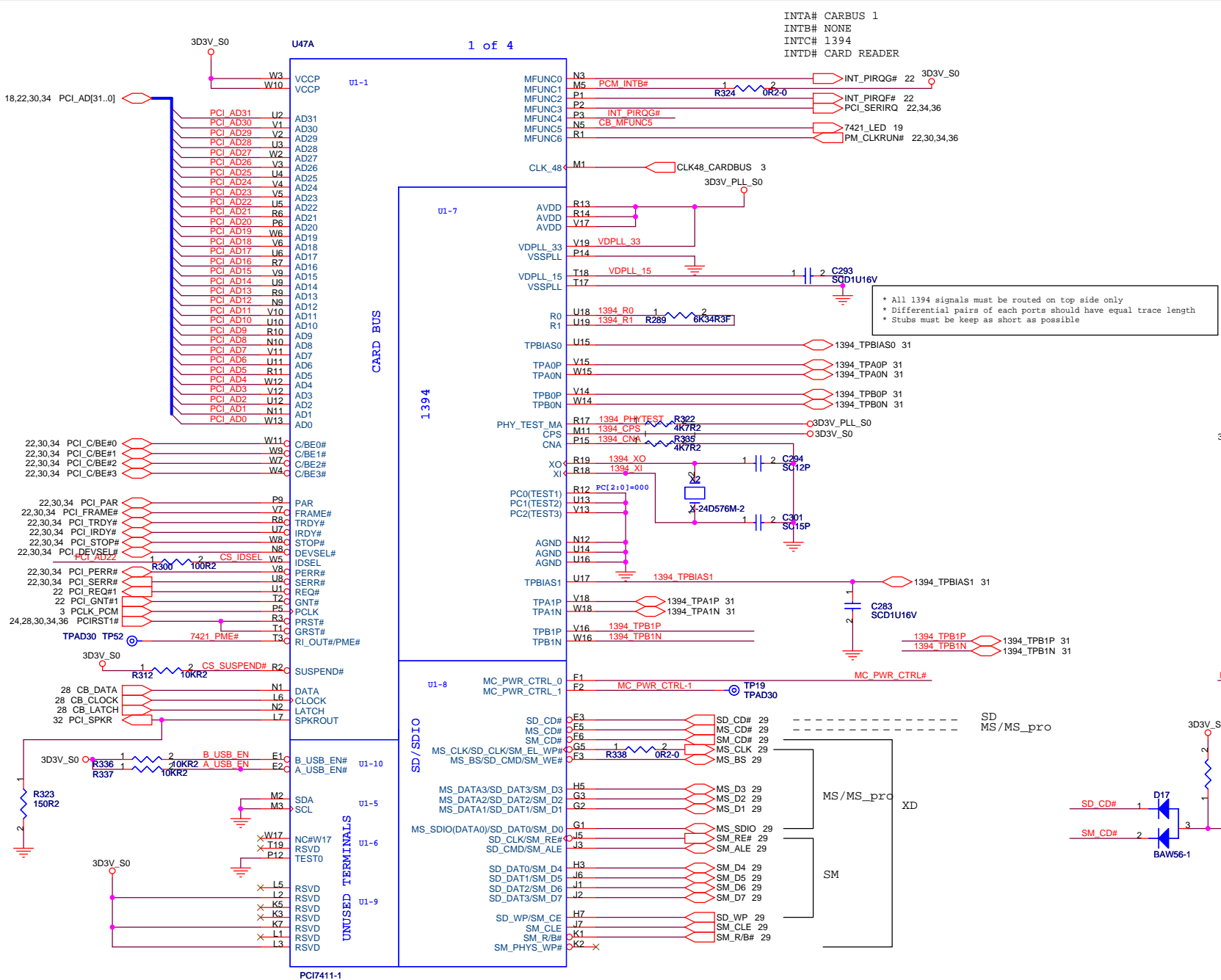
### <Core Design>

緯創資通

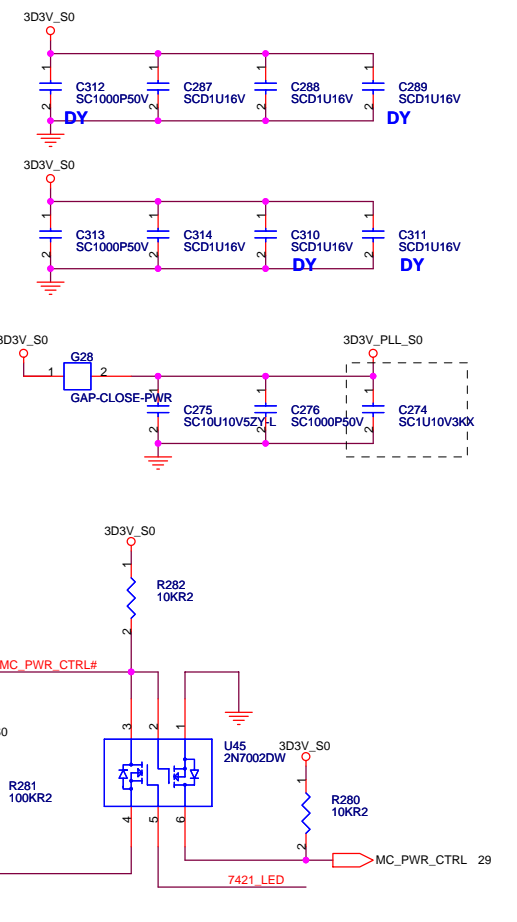
**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>HDD / CDROM/NEWCARD</b>			
Size A3	Document Number		Rev
	Leopard2		-1
Date:	Monday, July 11, 2005	Sheet 26 of	47





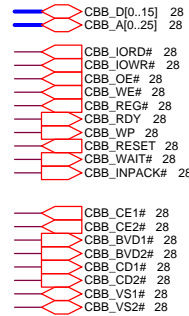
Bypass/Decoupling Capacitors  
Should be placed as close to  
PCI7421 as possible



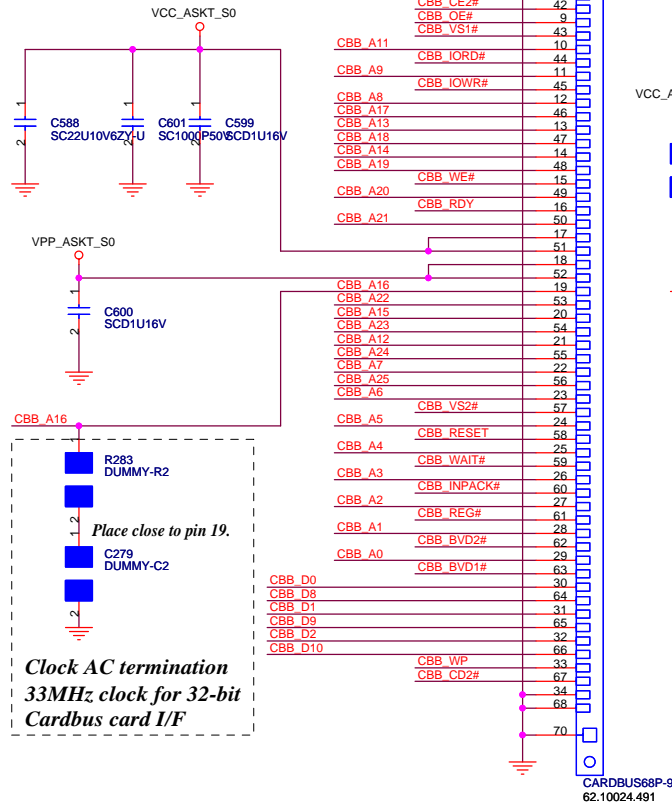
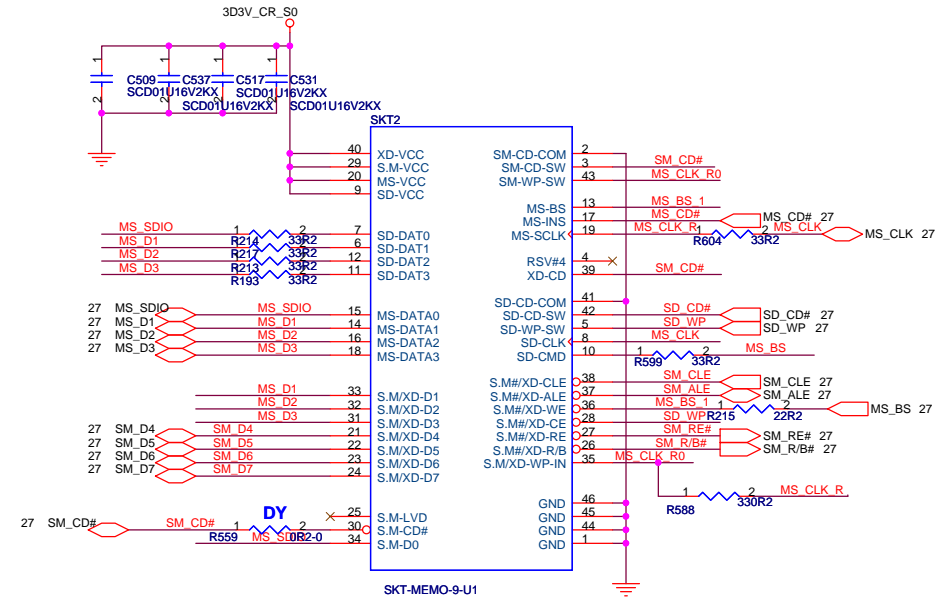


# PCMCIA Socket

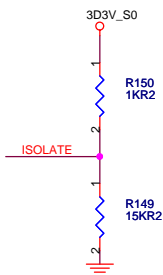
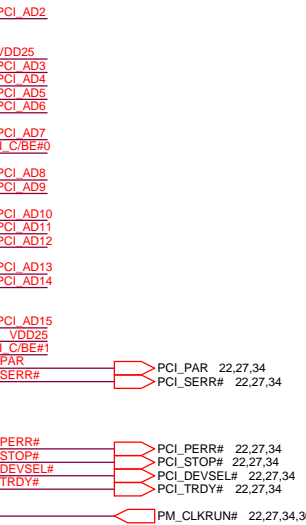
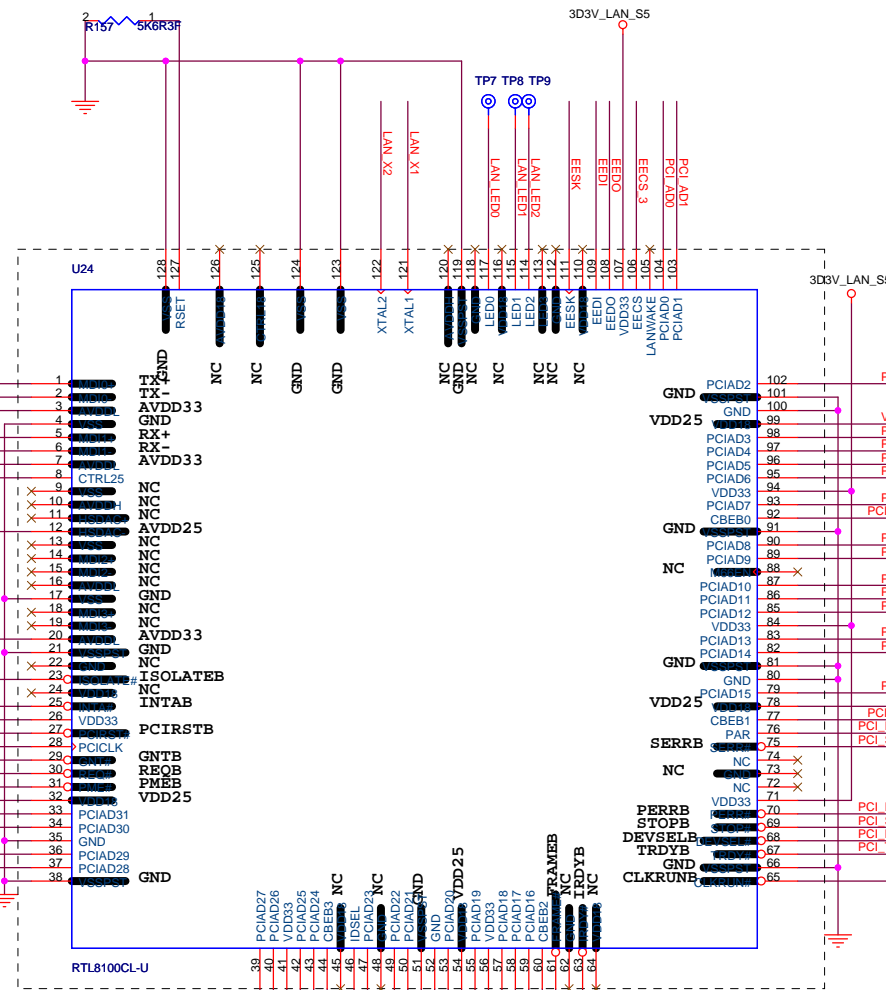
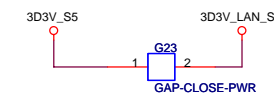
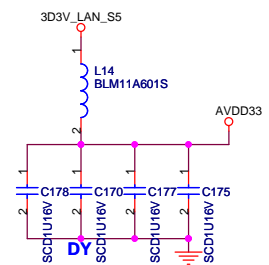
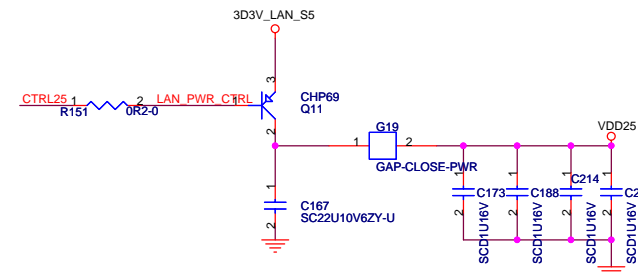
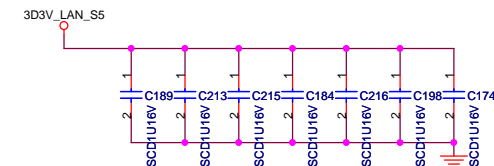
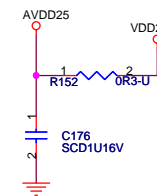
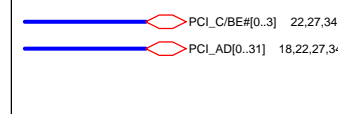
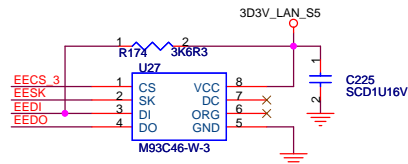
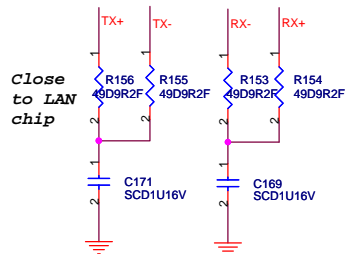
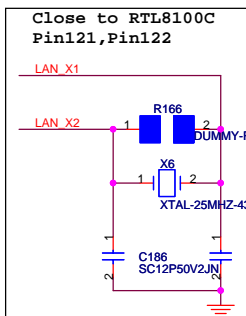
## Cardbus I/F



## 6 in 1 Connector



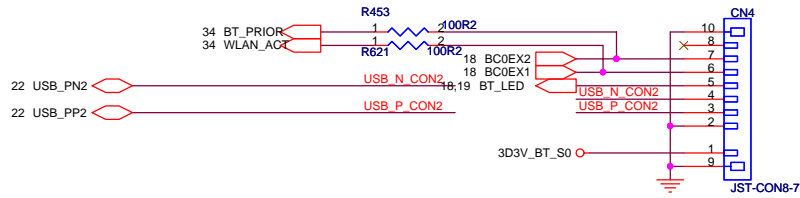
Clock AC termination  
33MHz clock for 32-bit  
Cardbus card I/F



## Blue thumb

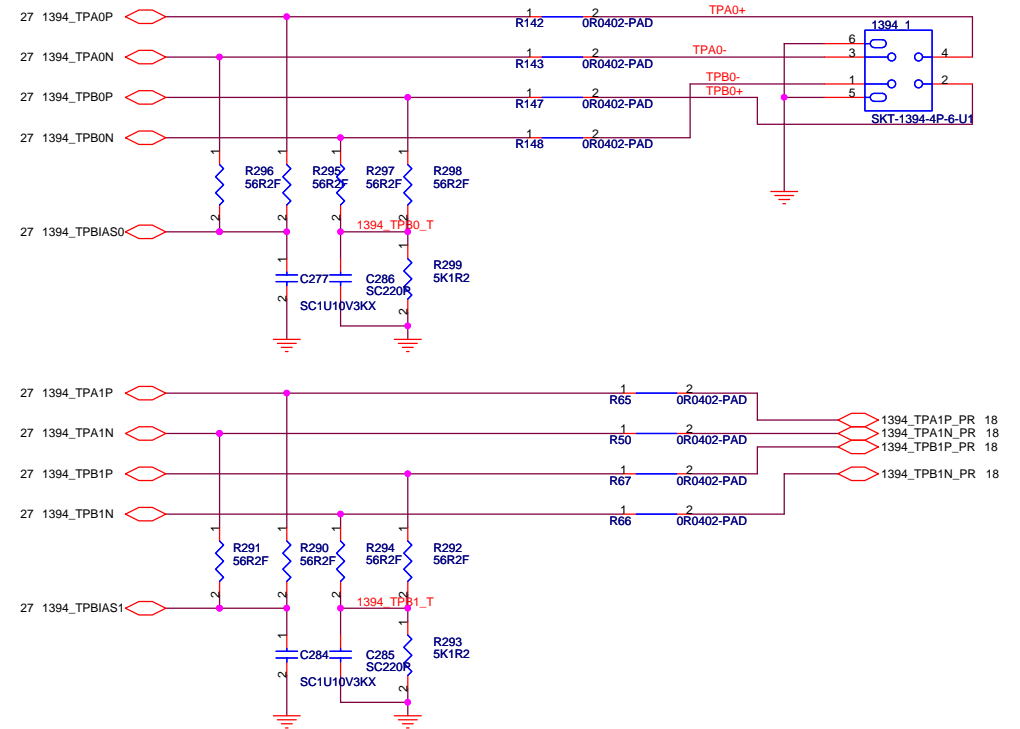
Place on bottom side

From NEW!  
1004-1



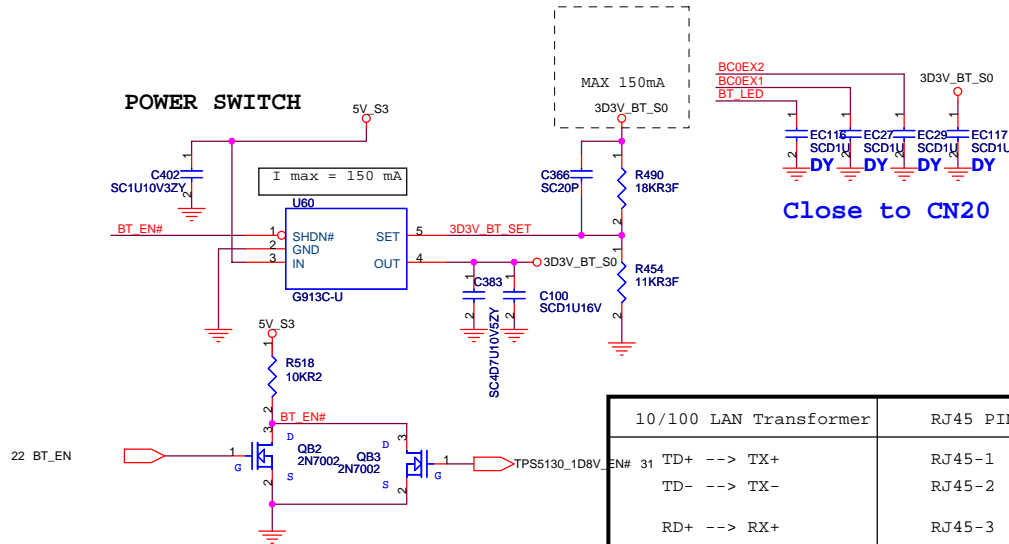
BC0EX2 connect to PCI\_AD22 on main board.  
BC0EX1 connect to ICH\_PME# on main board.

## 1394 Connector



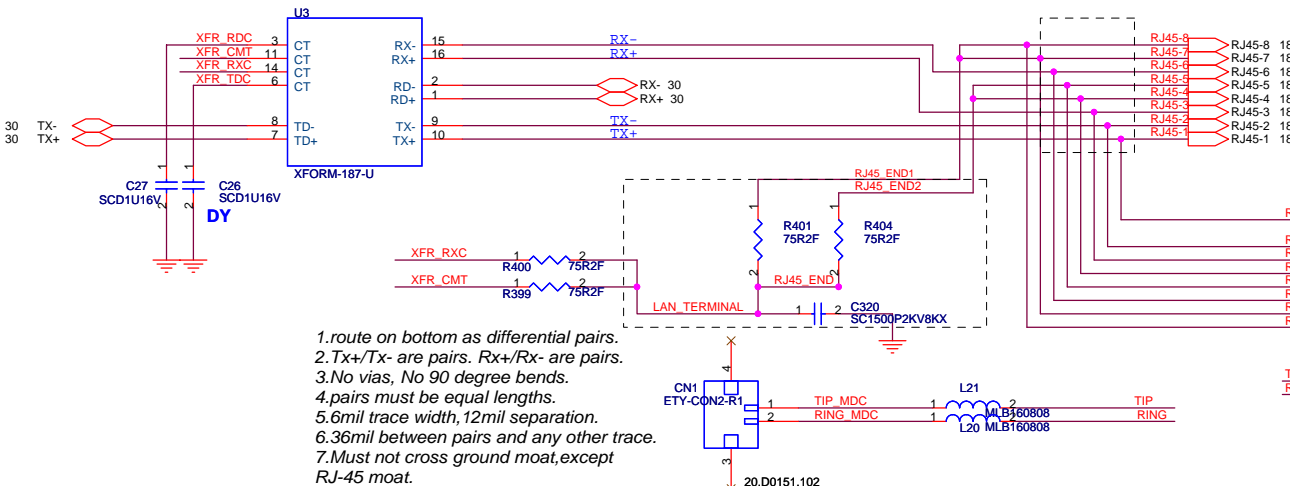
These components near to chip side.

### POWER SWITCH



10/100 LAN Transformer	RJ45 PIN
31 TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

### 10/100M Lan Transformer

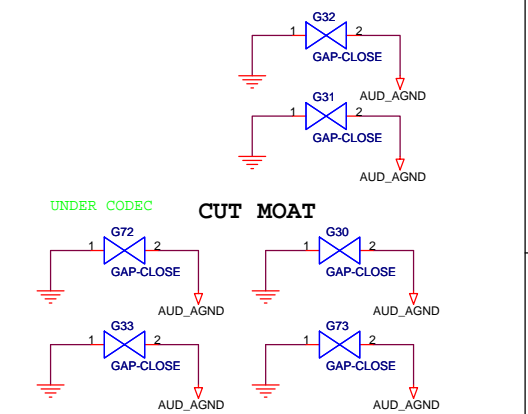
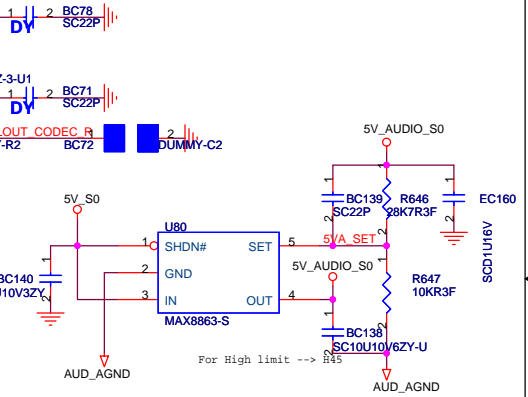
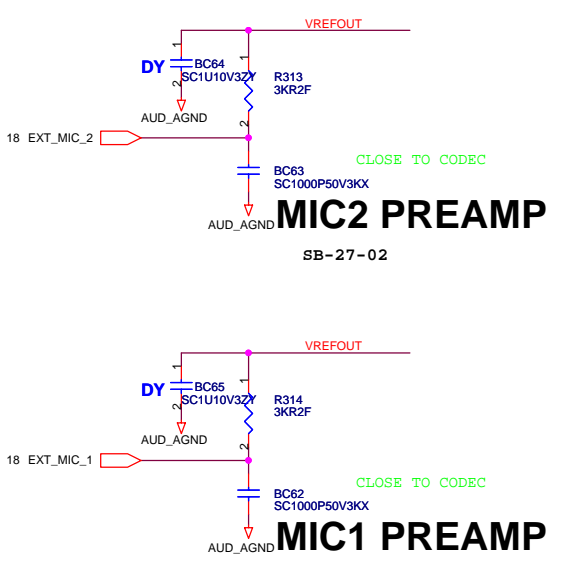
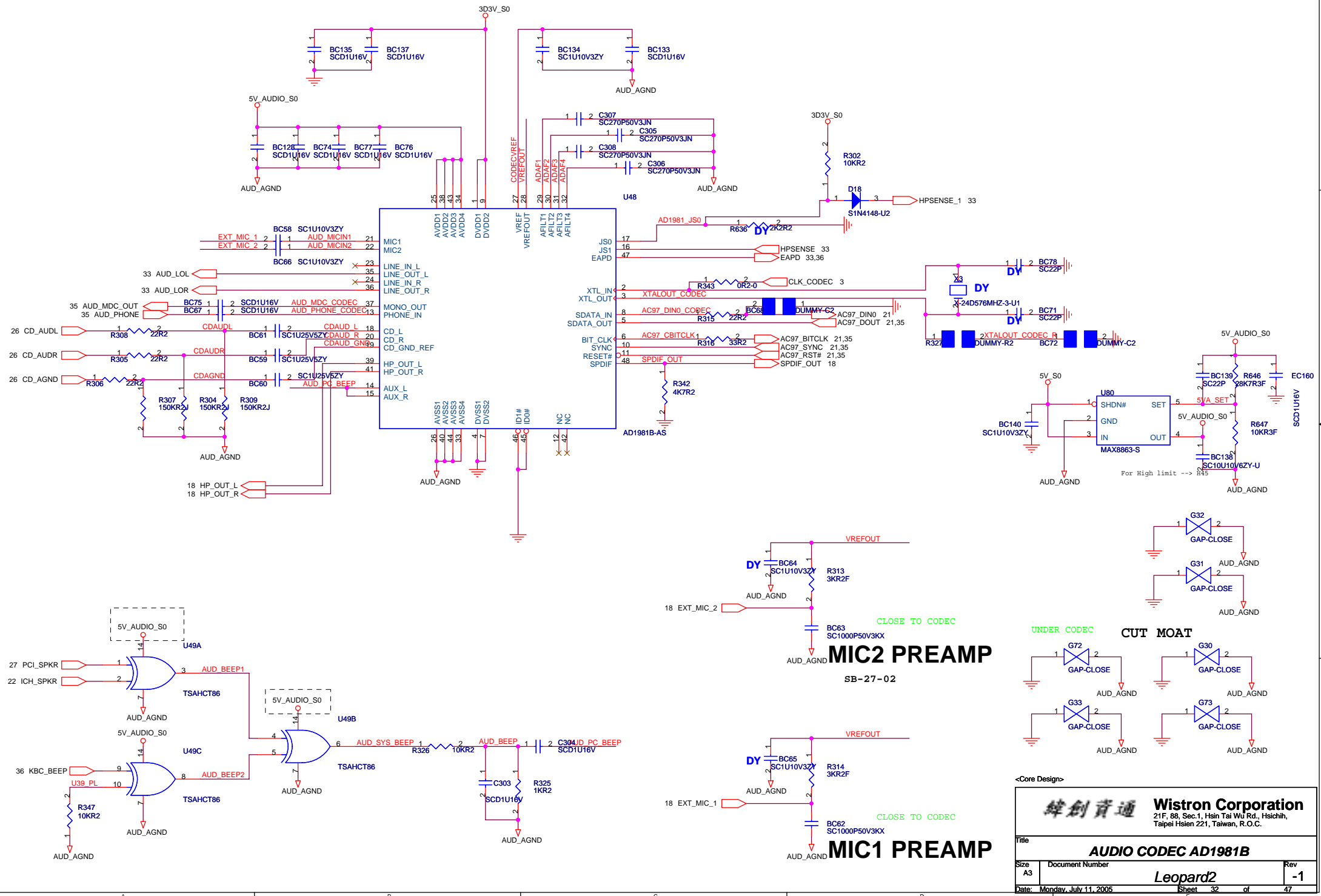


1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

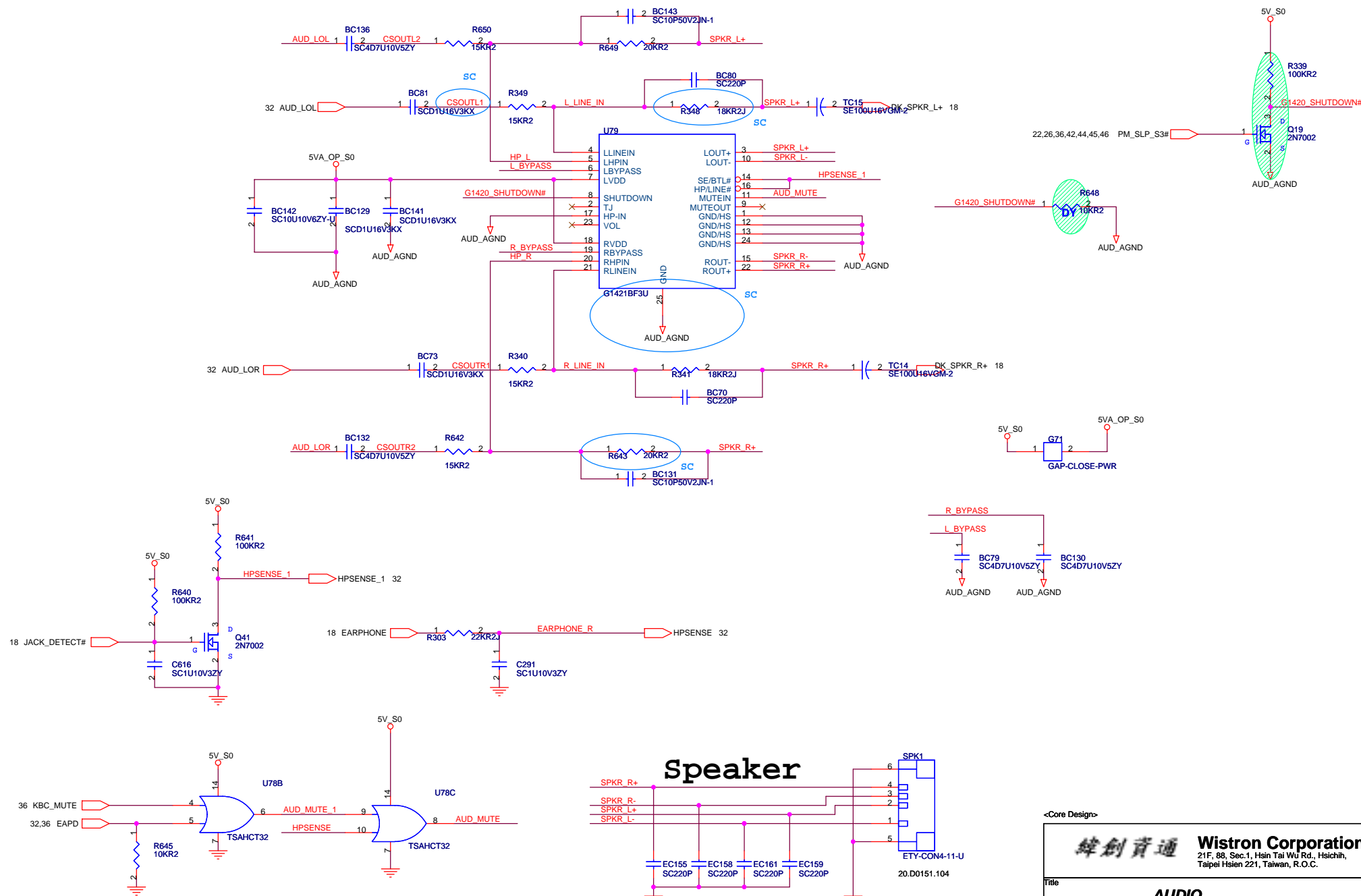
<Core Design>

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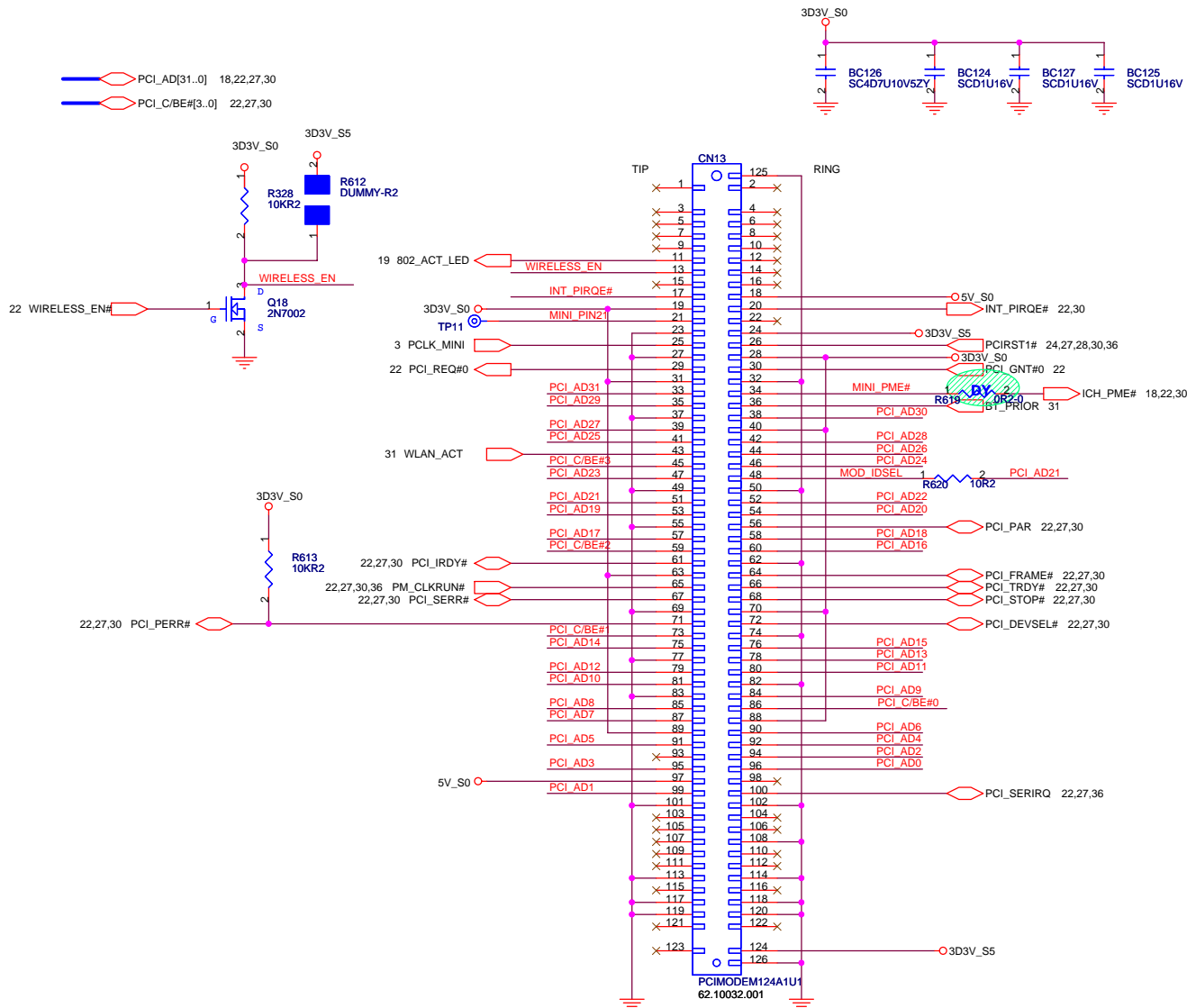
Title	LAN / 1394 Connector		
Size A3	Document Number	Rev	-1
Date: Monday, July 11, 2005	Sheet 31	of 47	





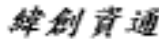


# MINI-PCI

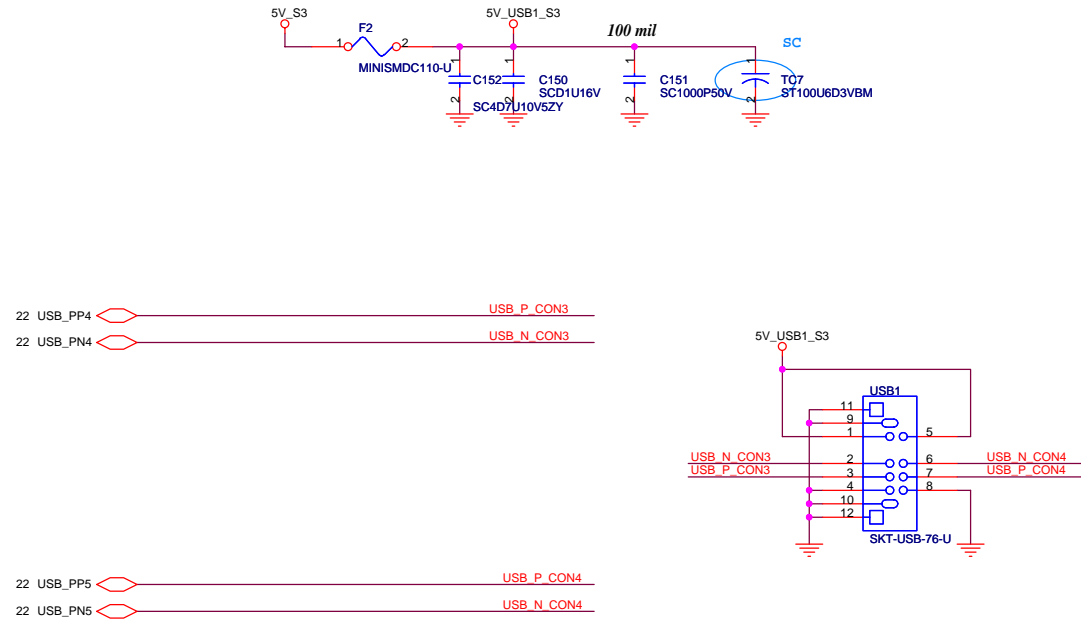


The symbol use 2nd source  
The P/N is the main source  
Main source:62.10032.001  
2nd source:62.10032.031

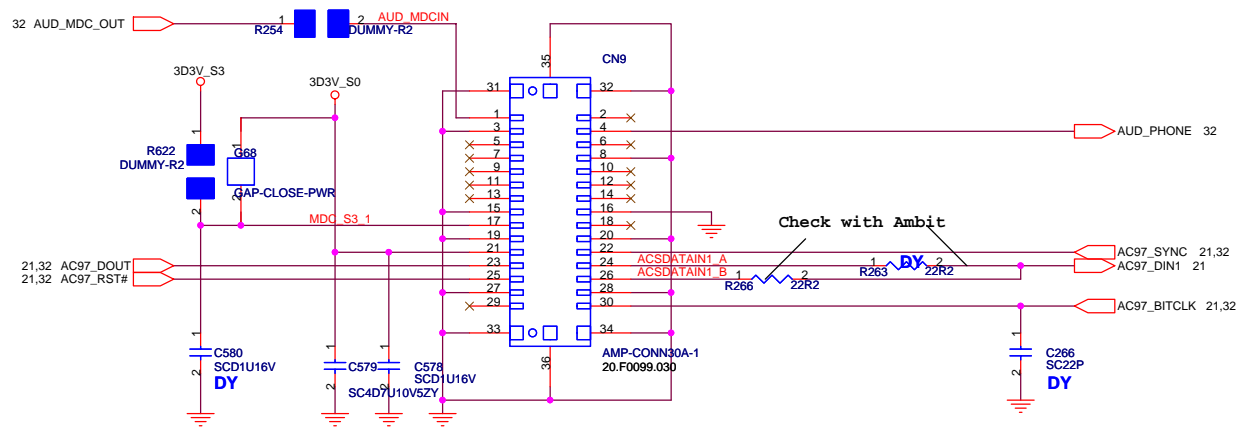
<Core Design>

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Title	
<b>MINI-PCI</b>	
Size	Document Number
A3	Leopard2
Date: Thursday, July 07, 2005	Sheet 34 of 47
Rev	
-1	

## USB POWER



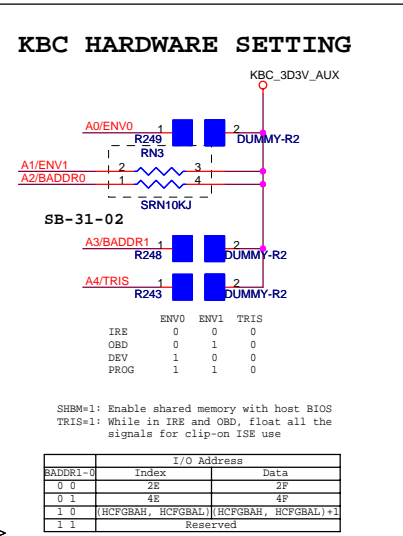
### *MDC Connector*



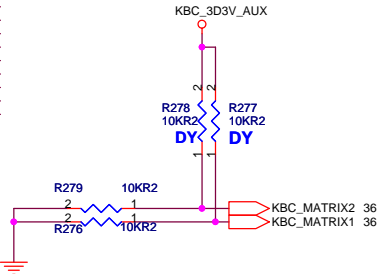
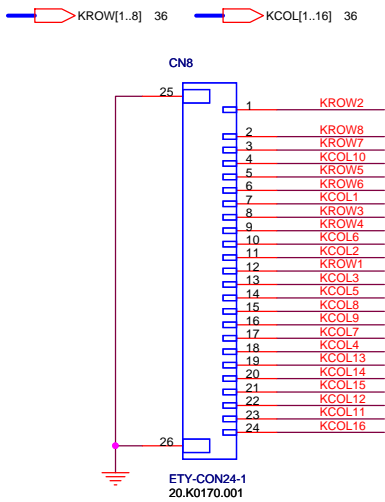
**<Core Design>**

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>USB / MDC CONN.</b>			
Size	Document Number		Rev
A3		<b>Leopard2</b>	<b>-1</b>
Date:	Thursday, July 07, 2005	Sheet 35 of 47	

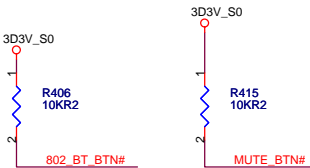
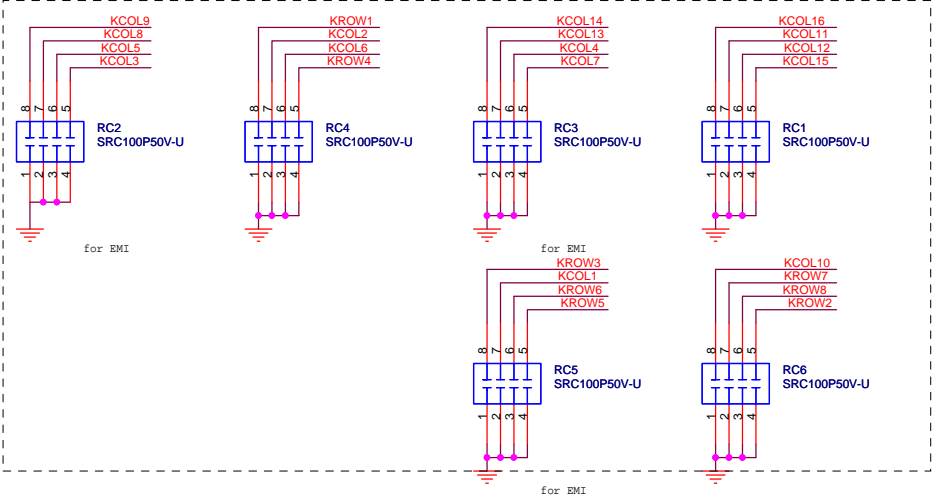


INTERNAL KEYBOARD CONNECTOR



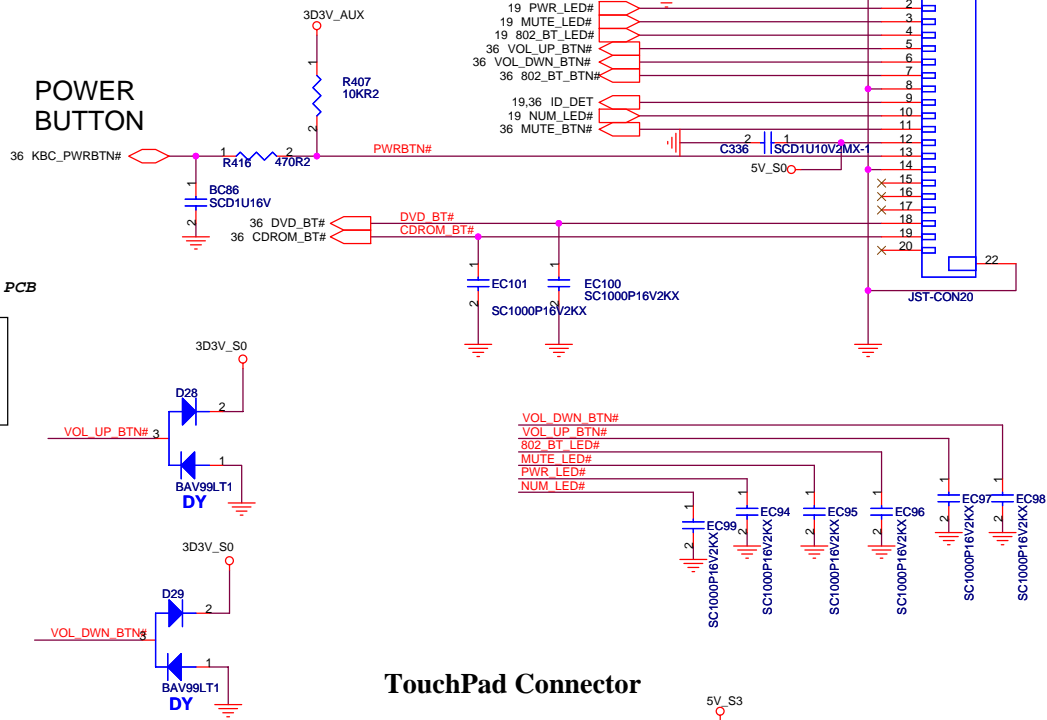
the matrix table for PCB

	PA	PR
Discrete	00	01
UMA	10	11

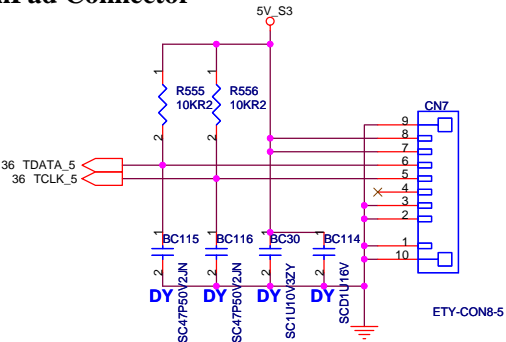


LAUNCH Board

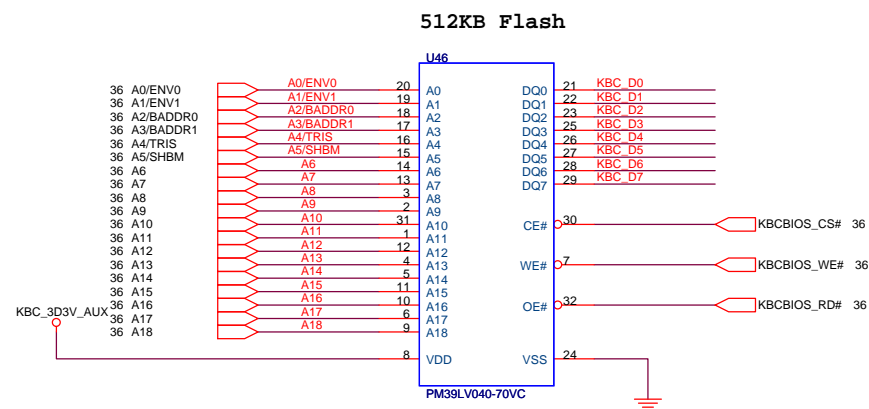
POWER BUTTON



TouchPad Connector



# FLASH ROM



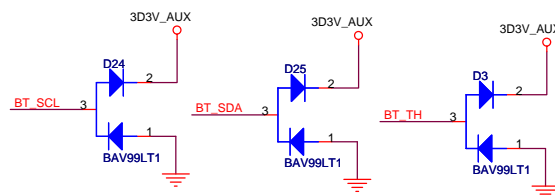
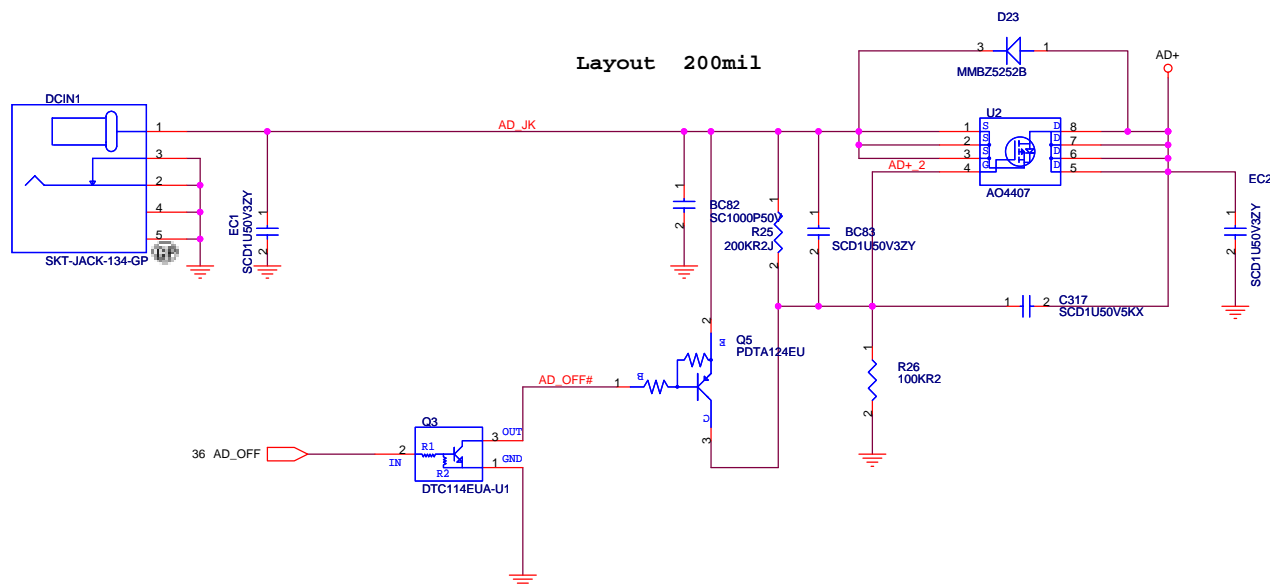
<Core Design>

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Title					
BIOS/GF					
Size	Document Number				Rev
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Date: Thursday, July 07, 2005			Sheet 38 of 47		

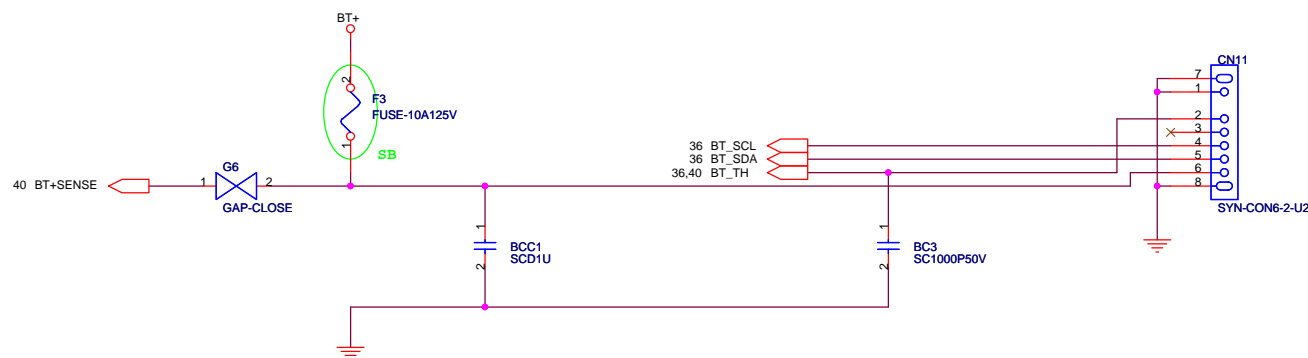


# Adaptor in to generate DCBATOUT

Layout 200mil



## BATTERY CONNECTOR



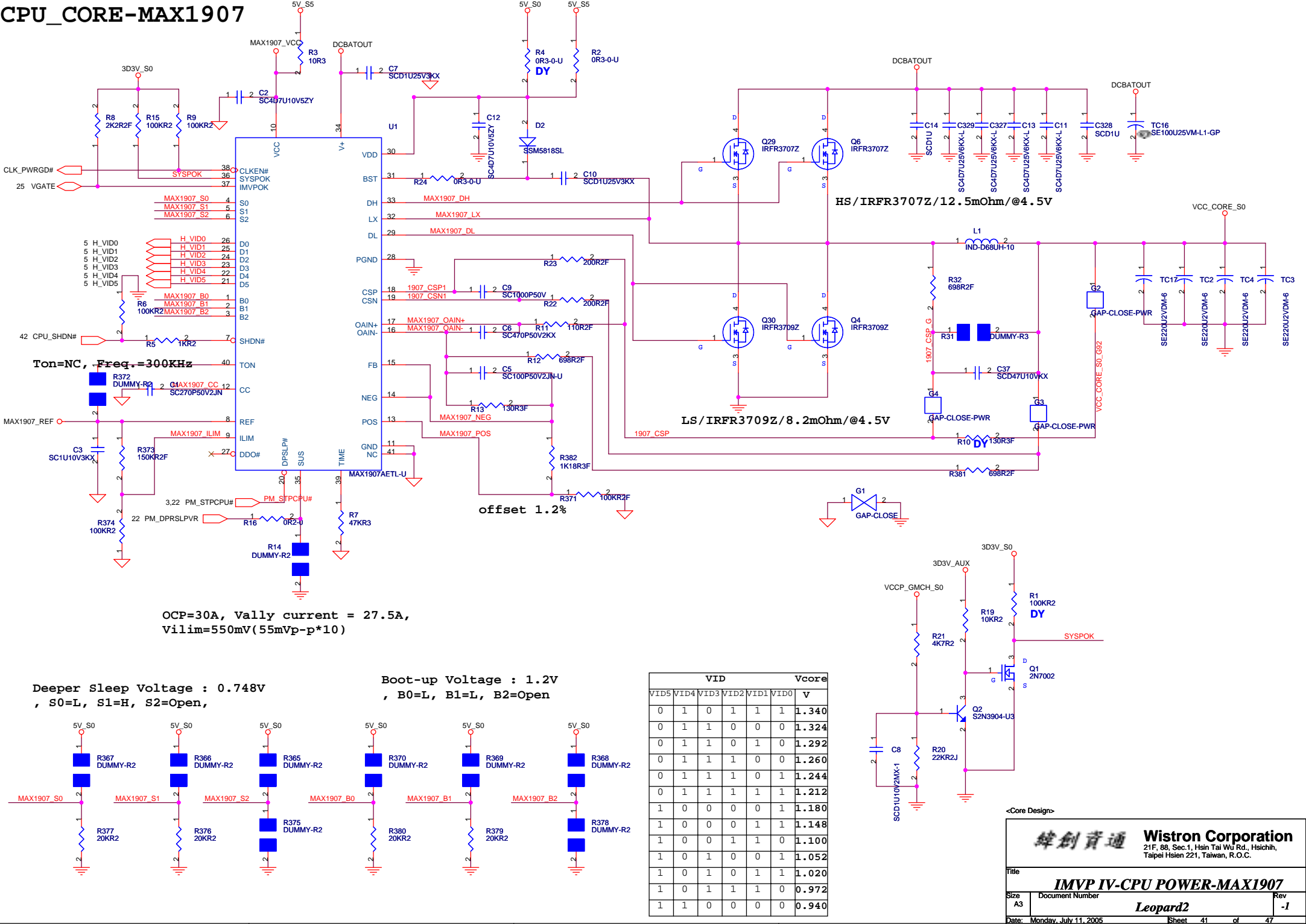
<Core Design>

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Title		Adaptor/ Battery conn.	
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CPU\_CORE-MAX1907



OCP=30A, Vally current = 27.5A,  
Vilim=550mV(55mVp-p\*10)

Deeper Sleep Voltage : 0.748V  
, S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V  
, B0=L, B1=L, B2=Open

VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	v
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title  
**IMVP IV-CPU POWER-MAX1907**

Size  
A3

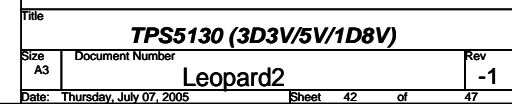
Document Number  
**Leopard2**

Rev  
**-1**

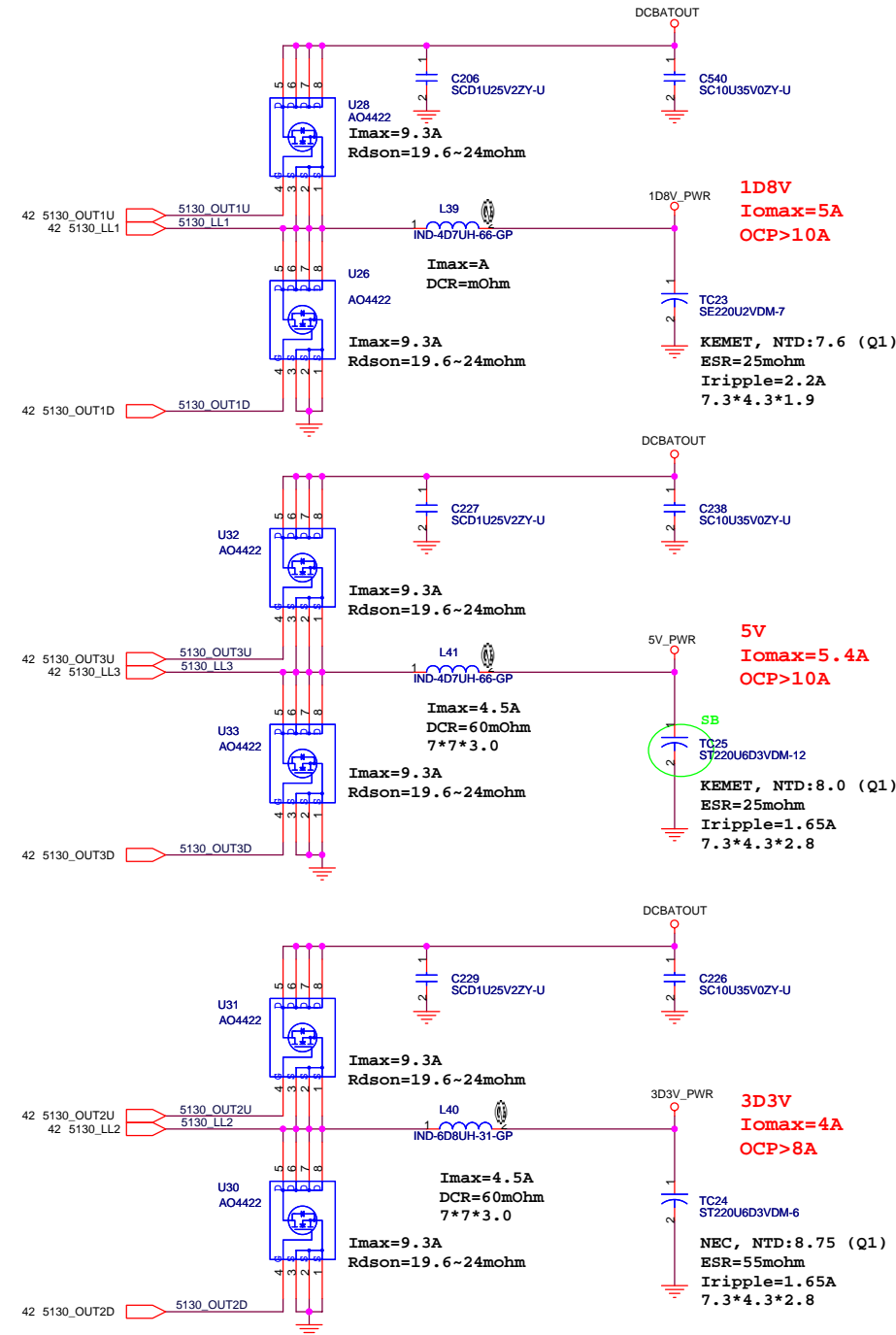
Date: Monday, July 11, 2005

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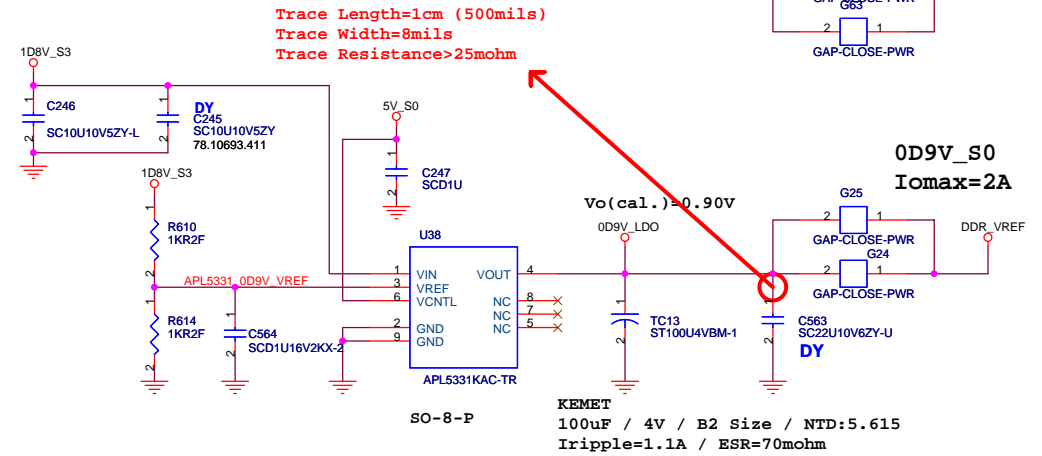
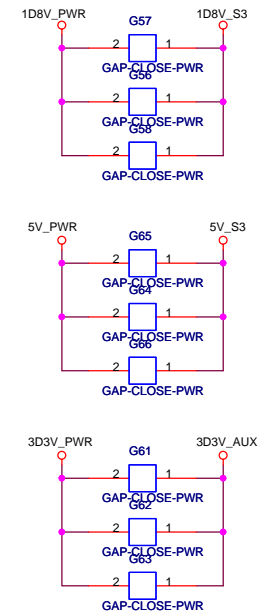
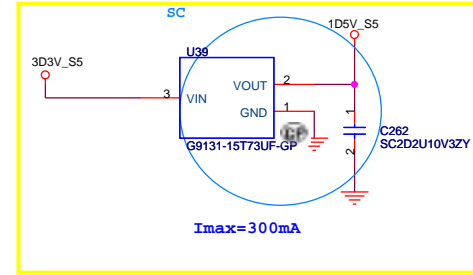
For 5V  
SETTING=5.0915V



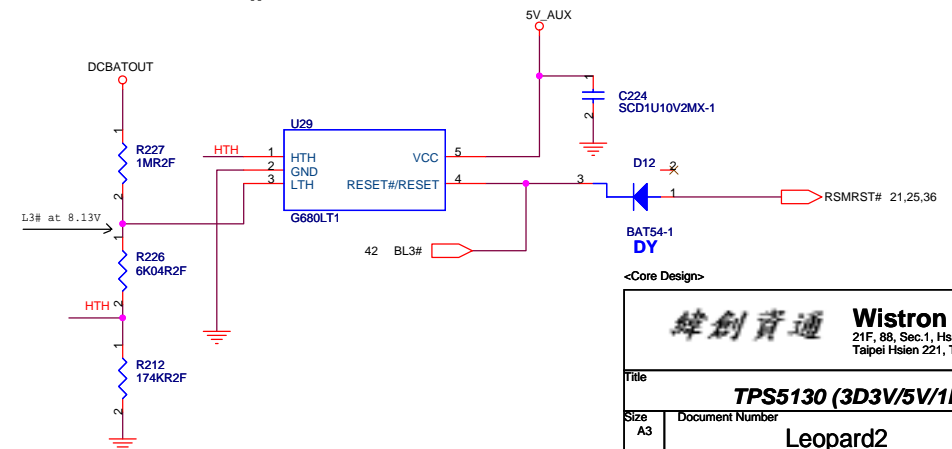
# TI TPS5130 for 1D2V, 5V, 3D3V (1D2V=>CH1 , 5V=>CH2 , 3D3V =>CH3)



## 1.5V\_S5 (For ICH6)



## L3# circuit

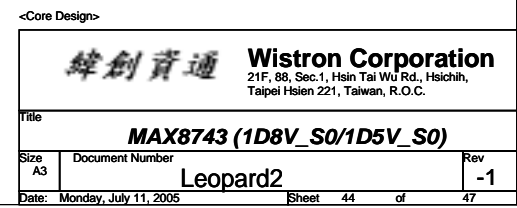


$$I_{ocp} = 4.3 * 1.7 = 7.3A$$

$$R_{ds,on} = 20 * 1.375 = 27.5m\ ohm$$

$$V_{cs2} = I_{ocp} * R_{ds,on} = 201mV$$

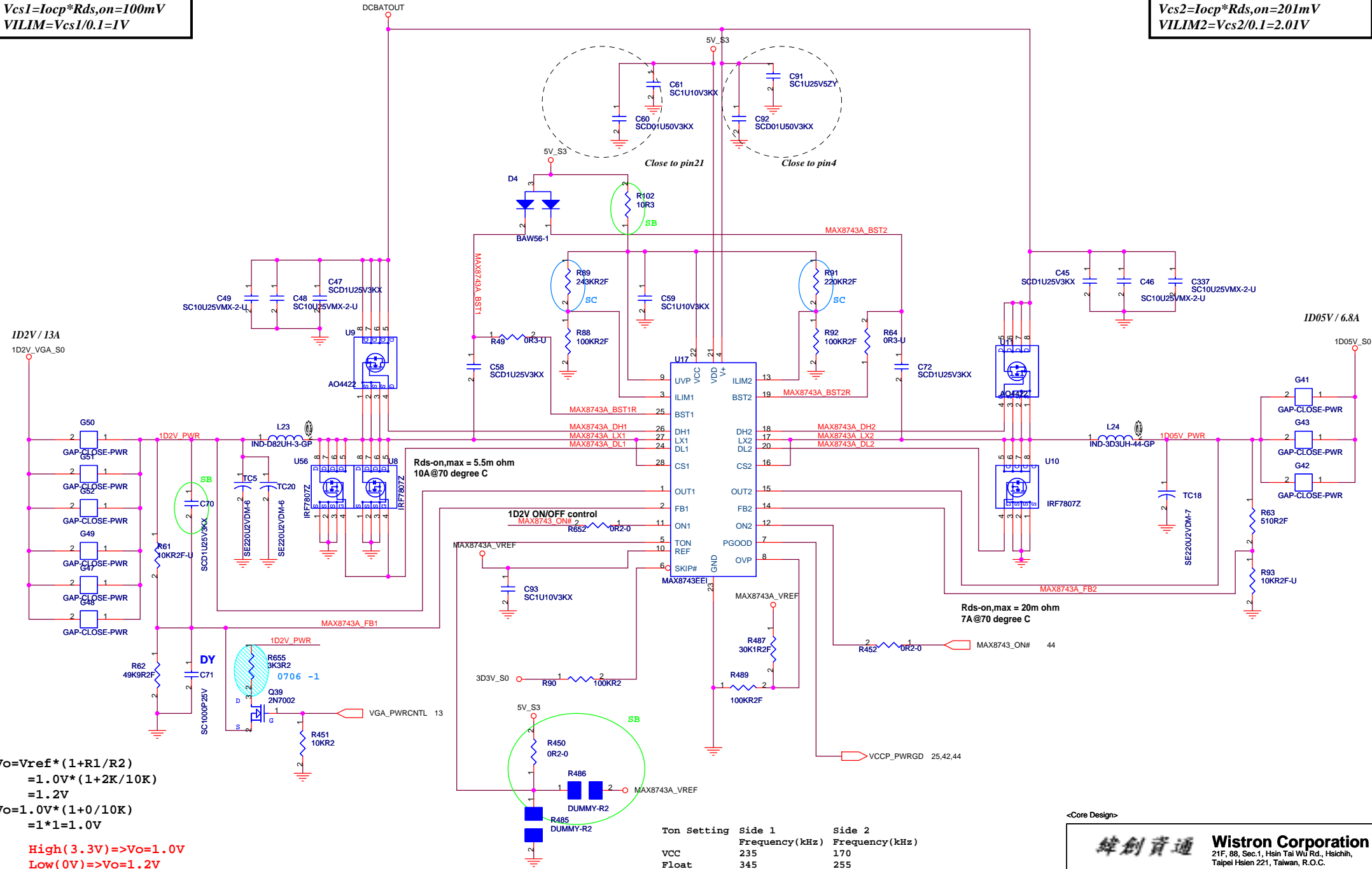
$$V_{ILIM2} = V_{cs2} / 0.1 = 2.01V$$





$I_{ocp}=7.8 * 1.7 = 13.3A$   
 $R_{ds,on}=5.5*1.375=7.563m\ ohm$   
 $V_{cs1}=I_{ocp}*R_{ds,on}=100mV$   
 $V_{ILIM}=V_{cs1}/0.1=1V$

$I_{ocp}=4.3 * 1.7 = 7.3A$   
 $R_{ds,on}=20*1.375=27.5m\ ohm$   
 $V_{cs2}=I_{ocp}*R_{ds,on}=201mV$   
 $V_{ILIM2}=V_{cs2}/0.1=2.01V$



$V_o = V_{ref} * (1 + R1/R2)$   
 $= 1.0V * (1 + 2K/10K)$   
 $= 1.2V$   
 $V_o = 1.0V * (1 + 0/10K)$   
 $= 1 * 1 = 1.0V$   
  
**High (3.3V) =>  $V_o = 1.0V$**   
**Low (0V) =>  $V_o = 1.2V$**

M24/M26 POWER PLAY (VGA\_PWRCNTL)  
high (3.3V) = set lower core voltage (VDDC = 1.0V)  
low (0V) = set higher core voltage (VDDC = 1.2V)

Ton Setting	Side 1	Side 2
	Frequency (kHz)	Frequency (kHz)
VCC	235	170
Float	345	255
VREF	485	355
AGND	620	460

<Core Design>

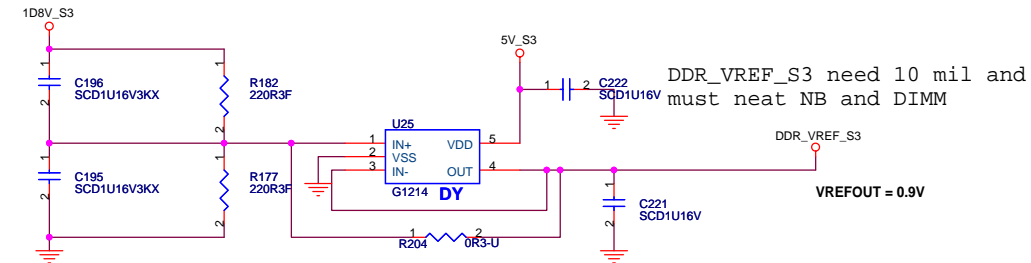
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **MAX8743 (1D2V\_VGA\_S0/1D05V)**

Size A3	Document Number	Rev
	<b>Leopard2</b>	<b>-1</b>

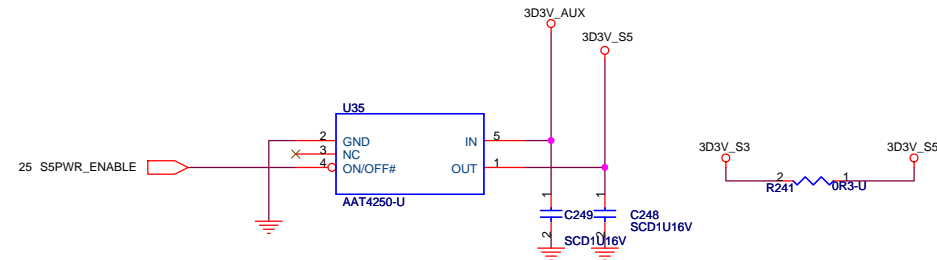
Date: Thursday, July 07, 2005 Sheet 45 of 47

# FOR GMCH Power



# FOR DDR2 Power

## Suspend Power



# Run Power

