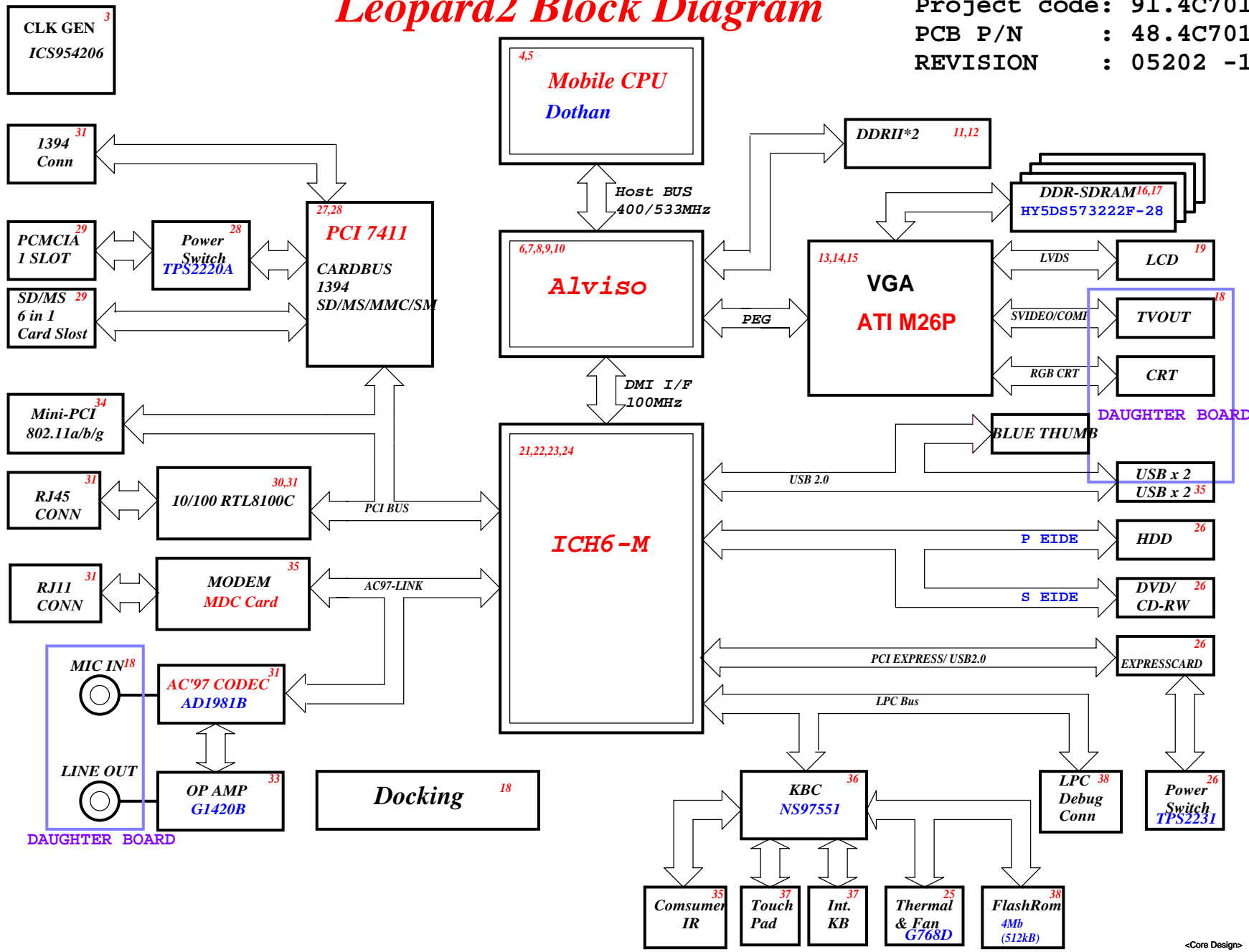


Leopard2 Block Diagram

Project code: 91.4C701.001
 PCB P/N : 48.4C701.011
 REVISION : 05202 -1



| SYSTEM DC/DC | |
|--------------|----------------------------|
| 42 TPS5130 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 1D8V_S3 5V_S3 3V_AUX |

| SYSTEM DC/DC | |
|--------------|-------------------------|
| 45 MAX8743 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 1D05V_S0 1D2V_VGA_S0 |

| MAXIM CHARGER | |
|---------------|-----------------------------|
| 40 MAX8725 | |
| INPUTS | OUTPUTS |
| DCBATOUT | BT+ 18V 4.0A 5V 100mA |

| CPU DC/DC | |
|------------|-------------------------------|
| 41 MAX1907 | |
| INPUTS | OUTPUTS |
| DCBATOUT | VCC_CORE 0.844-1.3V 27A |

| PCB LAYER | |
|-----------|----------|
| L1: | Signal 1 |
| L2: | GND |
| L3: | Signal 2 |
| L4: | Signal 3 |
| L5: | VCC |
| L6: | Signal 4 |
| L7: | GND |
| L8: | Signal 5 |

<Core Design>

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Title: **Block Diagram**

Size: A3 Document Number: **Leopard2** Rev: -1

Date: Monday, July 11, 2005 Sheet 1 of 47

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

| | |
|---|--------------------------------|
| ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]/GPO[17], GNT[6]/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]/PB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3] | ICH6 internal 20K pull-ups |
| LAN_RXD[2:0] | ICH6 internal 10K pull-ups |
| ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR | ICH6 internal 20K pull-downs |
| USB[7:0][P,N] | ICH6 internal 15K pull-downs |
| DD[7], SDDREQ | ICH6 internal 11.5K pull-downs |
| LAN_CLK | ICH6 internal 100K pull-downs |

ICH6-M IDE Integrated Series Termination Resistors

| | |
|--|----------------------|
| DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ | approximately 33 ohm |
|--|----------------------|

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
 5V_S3= 5 Voltage suspend to RAM(S3 state)
 5V_S5= 5 Voltage soft off(S5 state)
 3D3V_S0= 3.3 Voltage power up on system work(S0 state)
 3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
 3D3V_S5= 3.3 Voltage soft off(S5 state)
 LVDDR_2D8V= 2.8 Voltage power up on system work(S0 state)
 1D8V_S3= 1.8 Voltage suspend to RAM(S3 state)
 2D5V_S0= 2.5 Voltage power up on system work(S0 state)

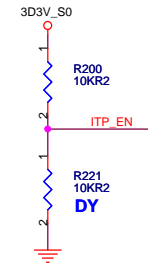
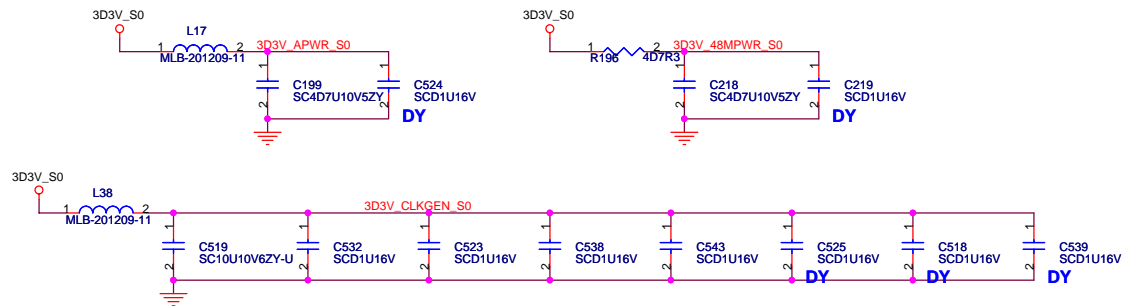
VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
 1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
 1D5V_S0= 1.5 Voltage power up on system work(S0 state)
 1D5V_S5= 1.5 Voltage soft off(S5 state)
 DDR_VREF= 0.9 Voltage power up on system work(S0 state)
 1D2V_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
 VRAM_VDDQ= 1.8 Voltage power up on system work(S0 state) for VRAM
 1D05V_S0= 1.05 Voltage power up on system work(S0 state)
 CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
 VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

PCI RESOURCE TABLE

| DEVICE | IDSEL | PCI IRQ | REQ# / GNT# |
|---------------------------|-------|--|---------------|
| Mini-PCI | AD21 | P_INTE# | REQ0# / GNT0# |
| Cardbus Controller TI7411 | AD22 | (CARBUS)P_INTG# (1394)P_INTF# (CARD READER)P_INTG# | REQ1# / GNT1# |
| LAN | AD23 | P_INTE# | REQ2# / GNT2# |
| Blue Thumb | AD24 | | |

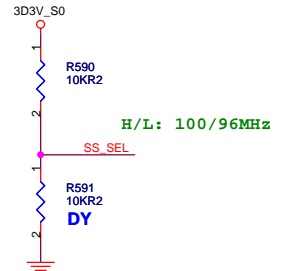
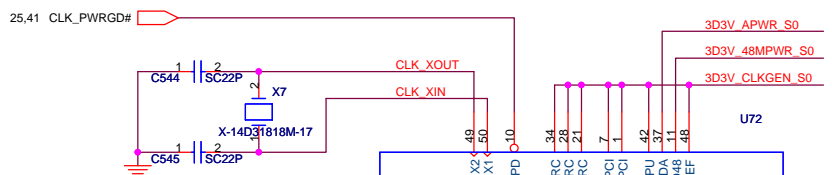
<Core Design>

| | | | |
|---|-----------------|----------------------------|------------------|
| 緯創資通 | | Wistron Corporation | |
| <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small> | | | |
| Title | | ITP | |
| Size A3 | Document Number | Leopard2 | |
| Date: Wednesday, July 06, 2005 | Sheet 2 | of | 47 |
| | | | Rev -1 |

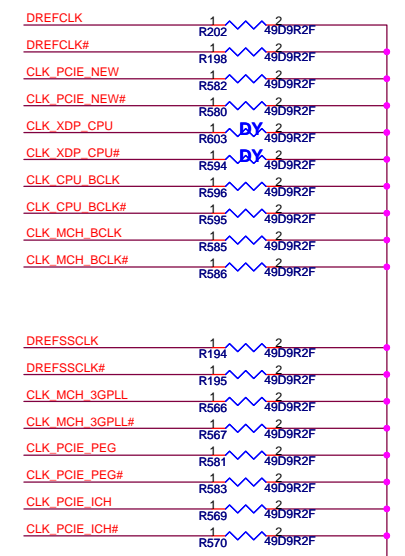
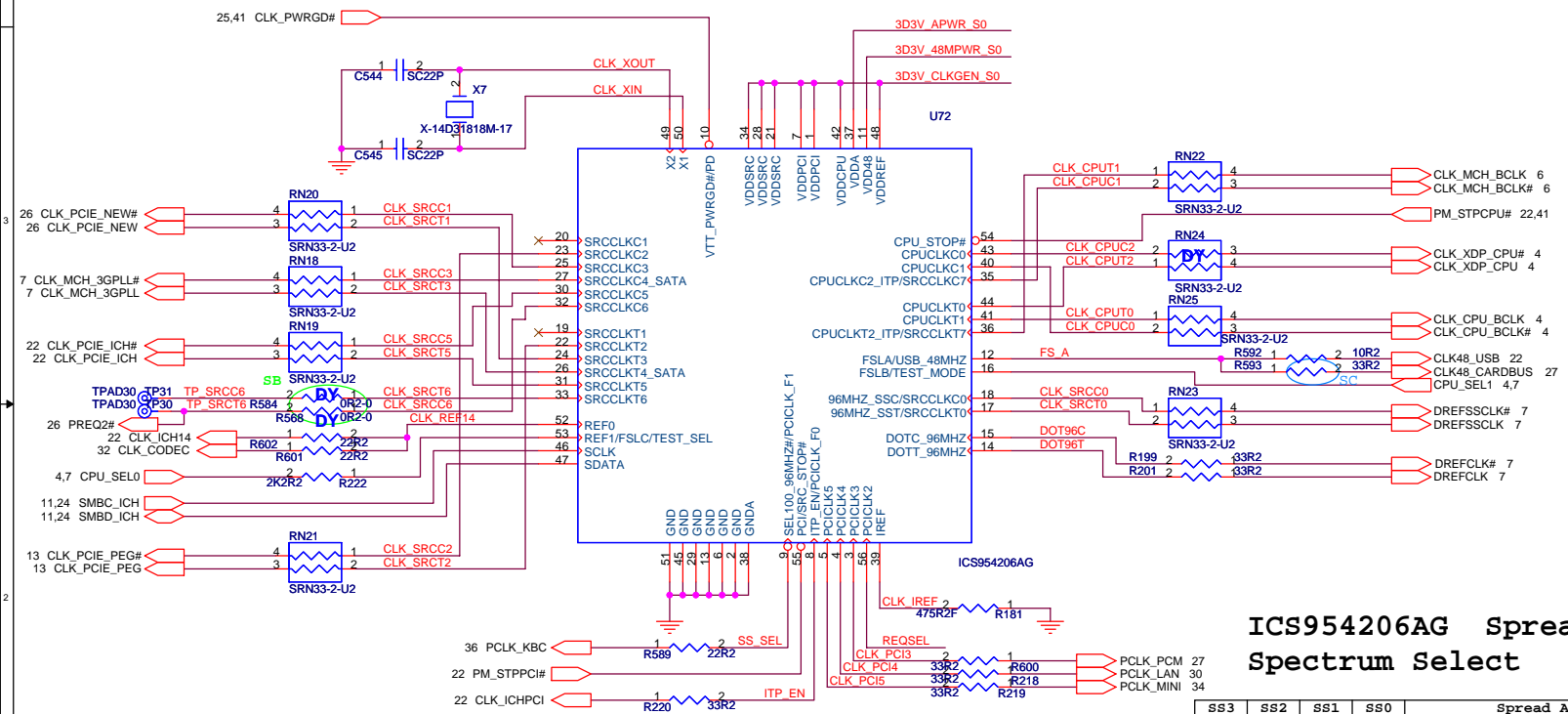


DummyR200(up side),Mounting R221(down side)
--SRC7 on

Mounting R200(up side),DummyR221(down side)
--CPU2_ITP on



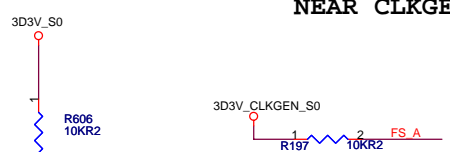
H/L: 100/96MHz



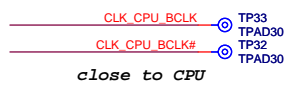
ICS954206AG Spread Spectrum Select

| SS3 | SS2 | SS1 | SS0 | Spread Amount% |
|-----|-----|-----|-----|----------------|
| 0 | 0 | 0 | 0 | -0.8 |
| 0 | 0 | 0 | 1 | -1.0 |
| 0 | 0 | 1 | 0 | -1.25 |
| 0 | 0 | 1 | 1 | -1.5 |
| 0 | 1 | 0 | 0 | -1.75 |
| 0 | 1 | 0 | 1 | -2.0 |
| 0 | 1 | 1 | 0 | -2.5 |
| 0 | 1 | 1 | 1 | -3.0 |
| 1 | 0 | 0 | 0 | +0.3 |
| 1 | 0 | 0 | 1 | +0.4 |
| 1 | 0 | 1 | 0 | +0.5 |
| 1 | 0 | 1 | 1 | +0.6 |
| 1 | 1 | 0 | 0 | +0.8 |
| 1 | 1 | 0 | 1 | +1.0 |
| 1 | 1 | 1 | 0 | +1.25 |
| 1 | 1 | 1 | 1 | +1.5 |

NEAR CLKGEN



| FS_C | FS_B | FS_A | CPU |
|------|------|------|----------|
| 0 | 0 | 0 | 266M |
| 0 | 0 | 1 | 133M |
| 0 | 1 | 0 | 200M |
| 0 | 1 | 1 | 166M |
| 1 | 0 | 0 | 333M |
| 1 | 0 | 1 | 100M |
| 1 | 1 | 0 | 400M |
| 1 | 1 | 1 | Reserved |



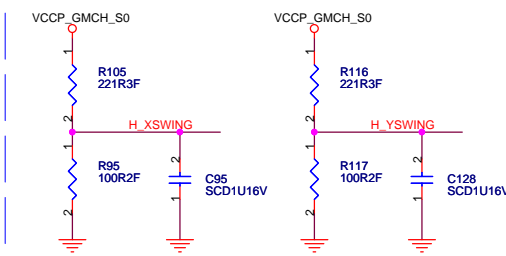
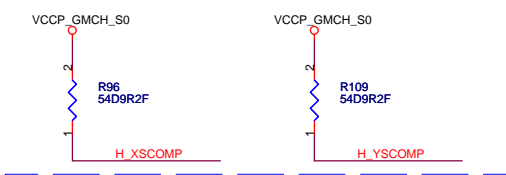
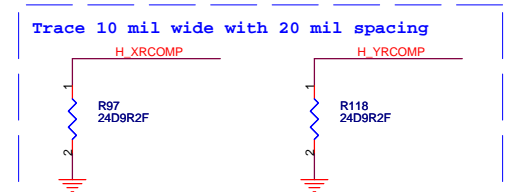
<Core Design>

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Title: **Clock Generator (ICS954206AG)**

Size A3 Document Number **Leopard2** Rev -1

Date: Monday, July 11, 2005 Sheet 3 of 47



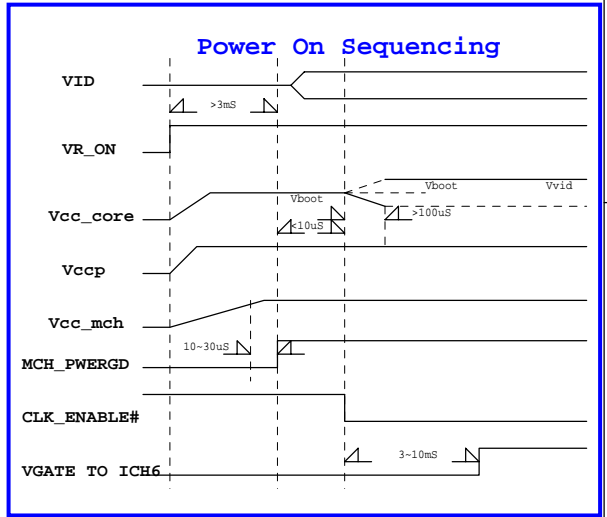
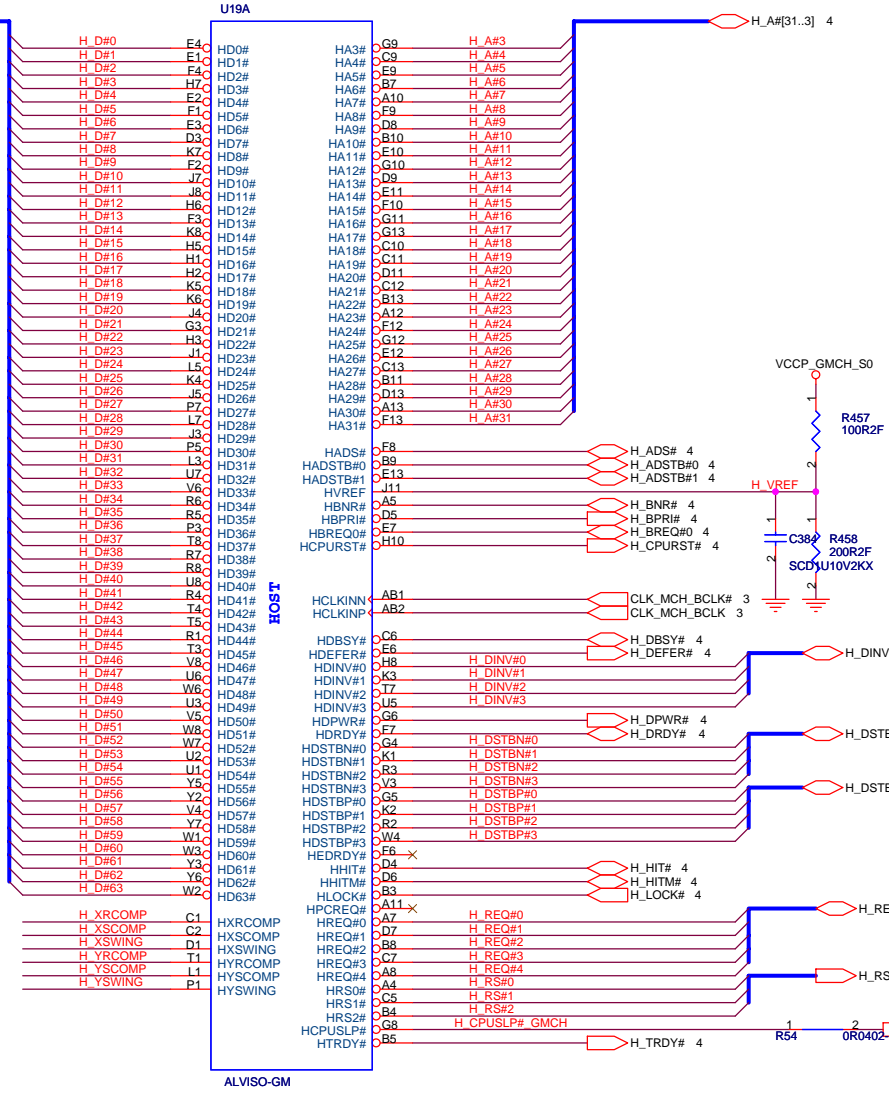
Trace 10 mil wide with 20 mil spacing

Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

| Pin Name | Strap Description | Configuration |
|---------------|------------------------------------|--|
| CFG[2:0] | FSB Frequency Select | 001 = FSB533 101 = FSB400 others = Reversed |
| CFG[4:3] | Reserved | |
| CFG5 | DMI x2 Select | 0 = DMI x2 1 = DMI x4 (Default) |
| CFG6 | Reserved | 0 = DDR2 1 = DDR1 (Default) |
| CFG7 | CPU Strap | 0 = Reserved 1 = Dothan (Default) |
| CFG8 | Reserved | |
| CFG9 | PCI Express Graphics Lane Reversal | 0 = Reserve Lanes 1 = Normal (Default) |
| CFG[11:10] | Reserved | |
| CFG[13:12] | XOR/ALL Z test straps | 00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default) |
| CFG[15:14] | Reserved | |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default) |
| CFG17 | Reserved | |
| CFG18 | GMCH core VCC Select | 0 = 1.05V (Default) 1 = 1.5V |
| CFG19 | CPU VTT Select | 0 = 1.05V (Default) 1 = 1.2V |
| CFG20 | Reserved | |
| SDVOCRTL_DATA | SDVO Present | 0 = No SDVO device present(Default) 1 = SDVO device present |

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORk In signal.



ALVISO-GM: 71.0GMCH.08U
ALVISO-PM: 71.0GMCH.0BU
ALVISO-GML: 71.0GMCH.0JU

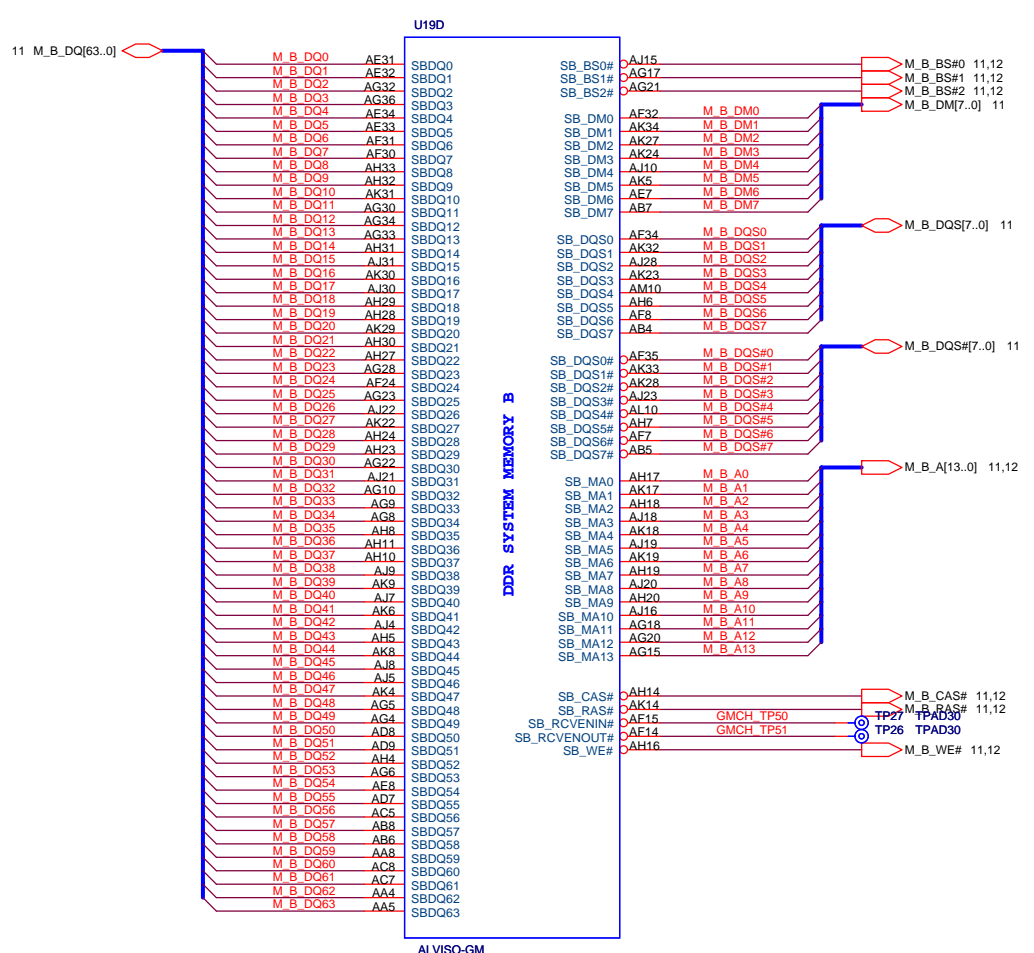
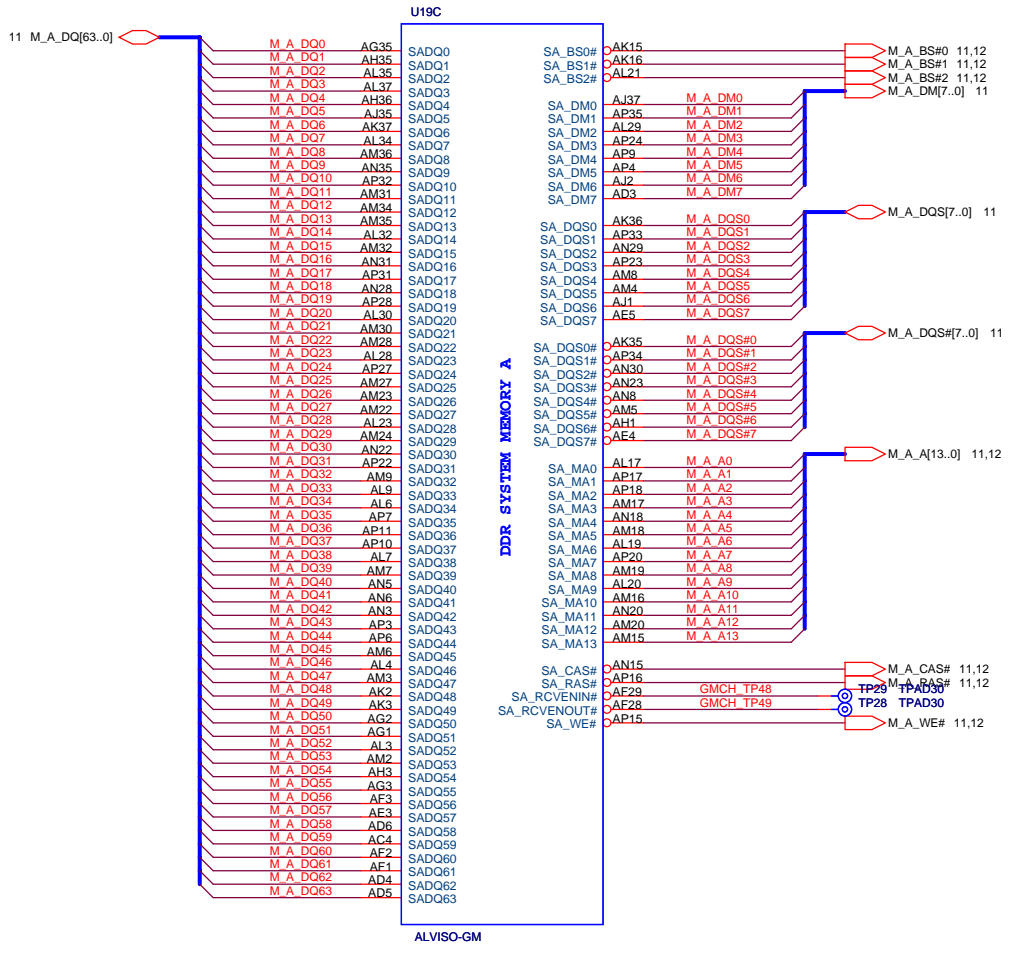
<Core Design>

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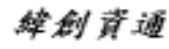
Title: **GMCH (1 of 5)**

Size A3 Document Number **Leopard2** Rev **-1**

Date: Monday, July 11, 2005 Sheet 6 of 47

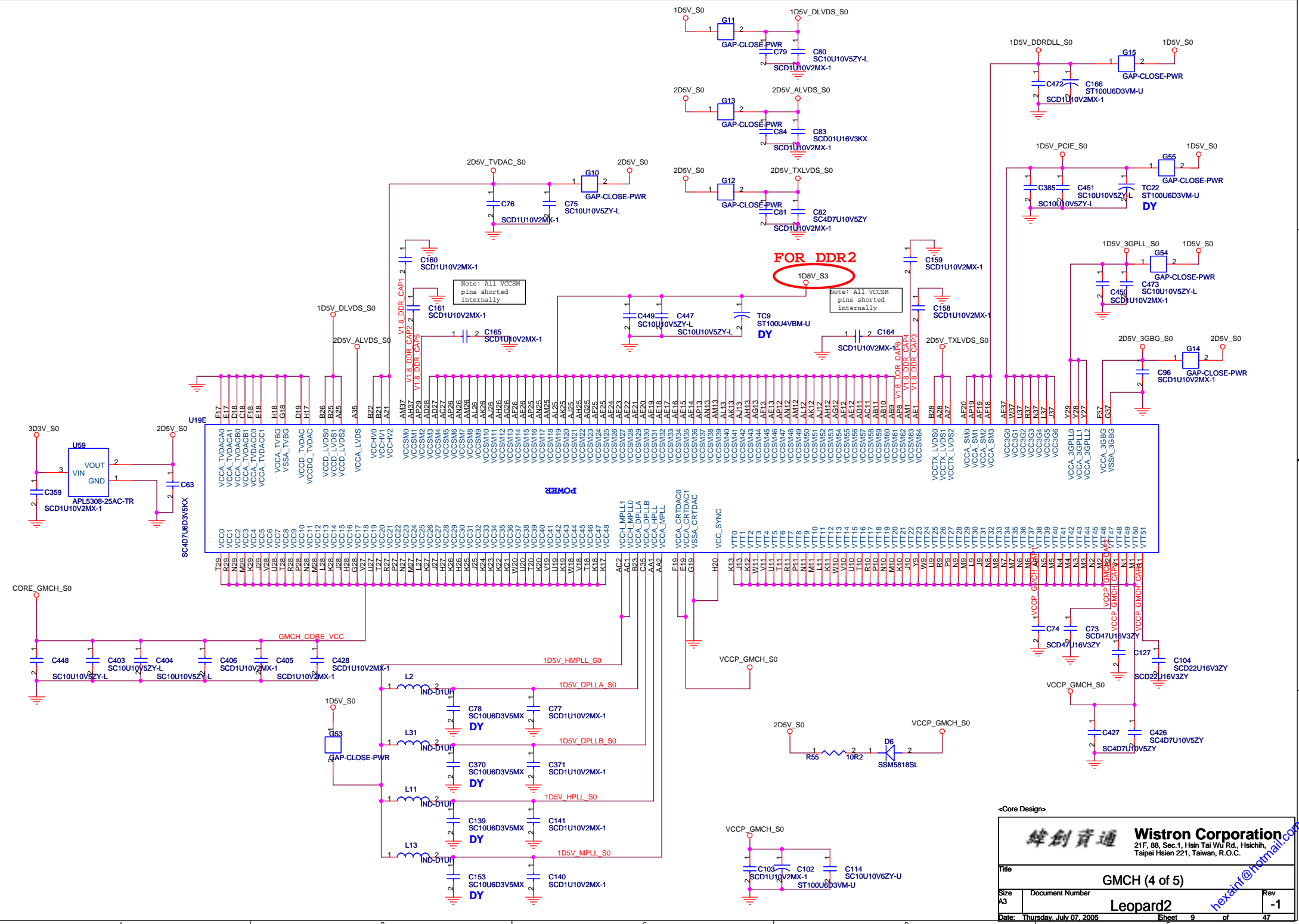


<Core Design>



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| | | | |
|-------|-------------------------|----------------------|---------|
| Title | | GMCH (3 of 5) | |
| Size | Document Number | Rev | |
| A3 | Leopard2 | -1 | |
| Date: | Thursday, July 07, 2005 | Sheet | 8 of 47 |



<Core Design>

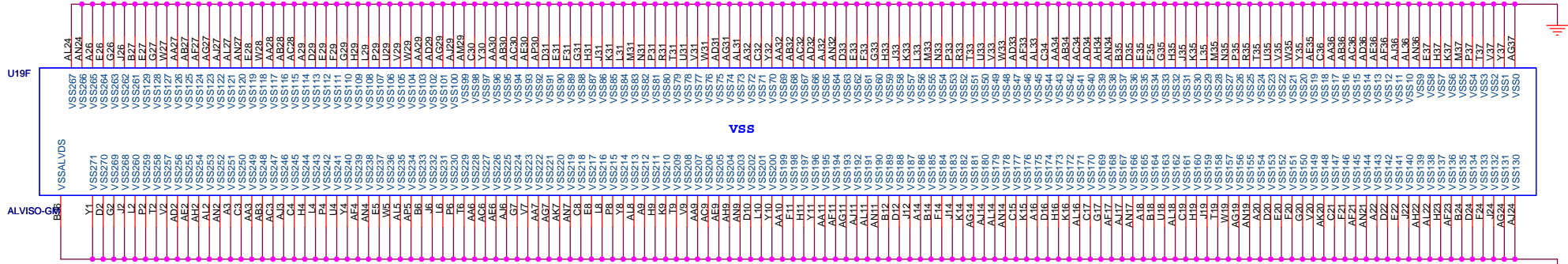
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (4 of 5)**

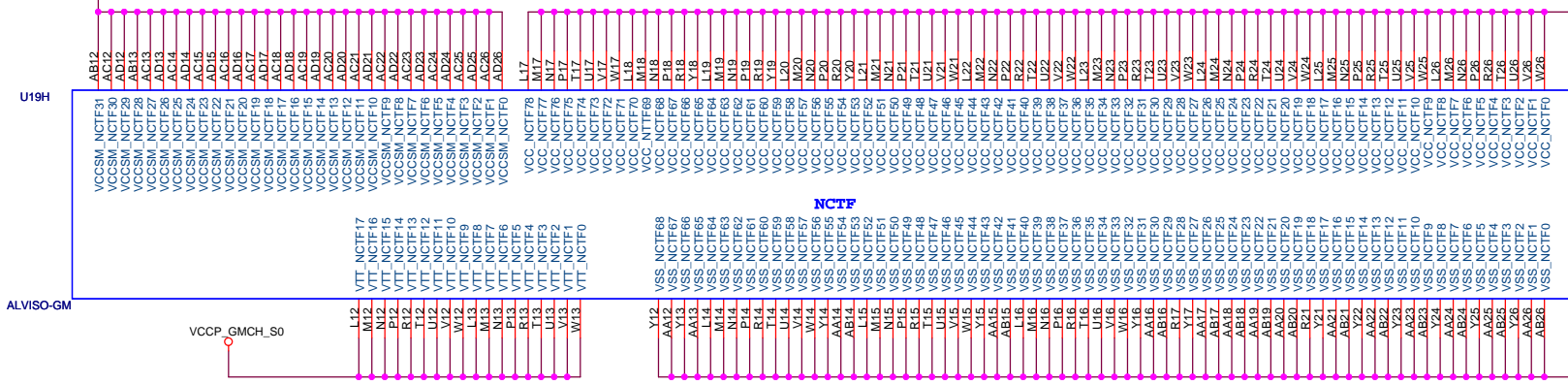
Size: A3 Document Number: **Leopard2** Rev: **-1**

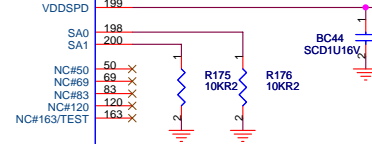
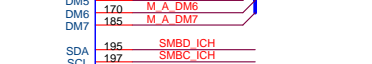
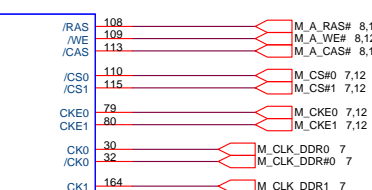
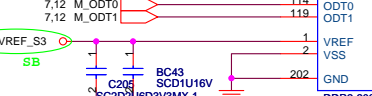
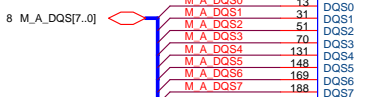
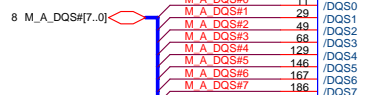
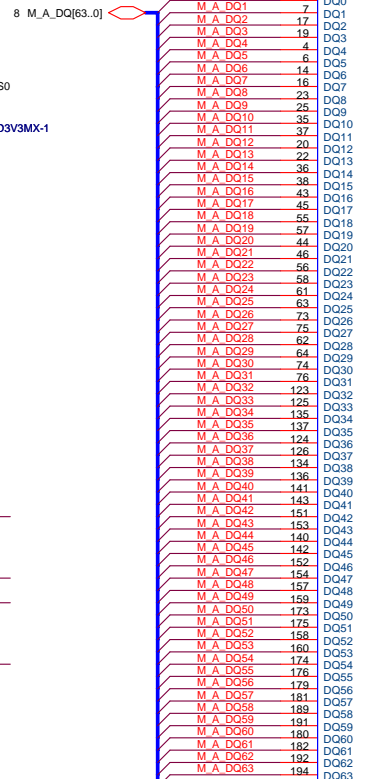
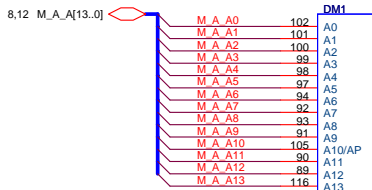
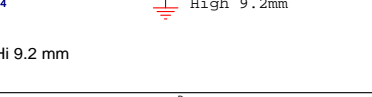
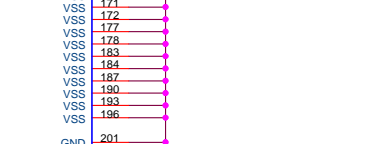
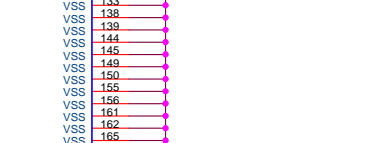
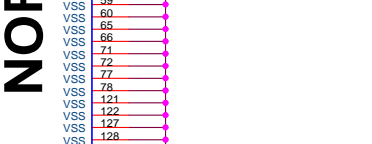
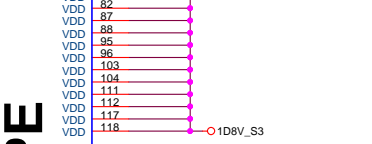
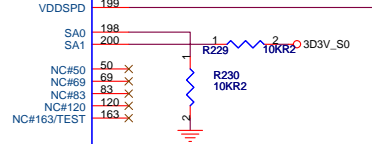
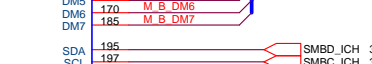
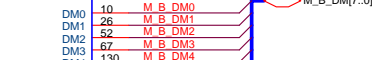
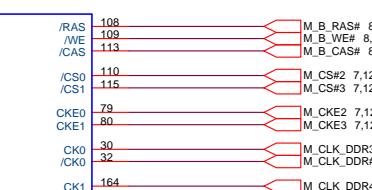
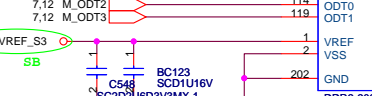
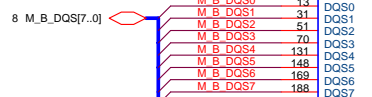
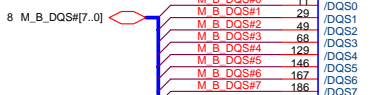
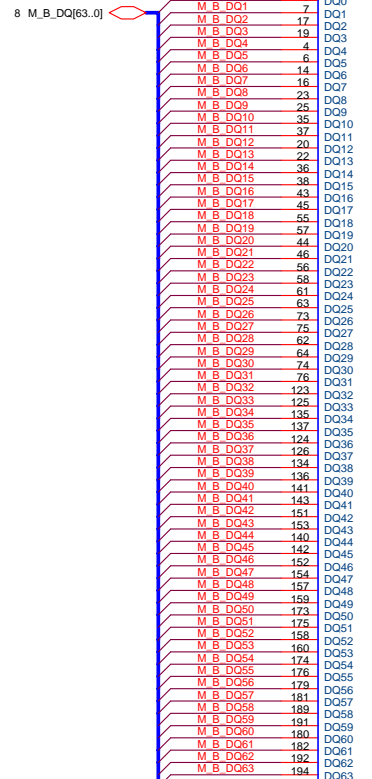
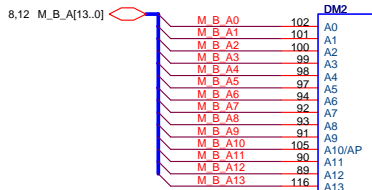
Date: Thursday, July 07, 2005 Sheet: 9 of 47

mailto:hexaint@hotmail.com



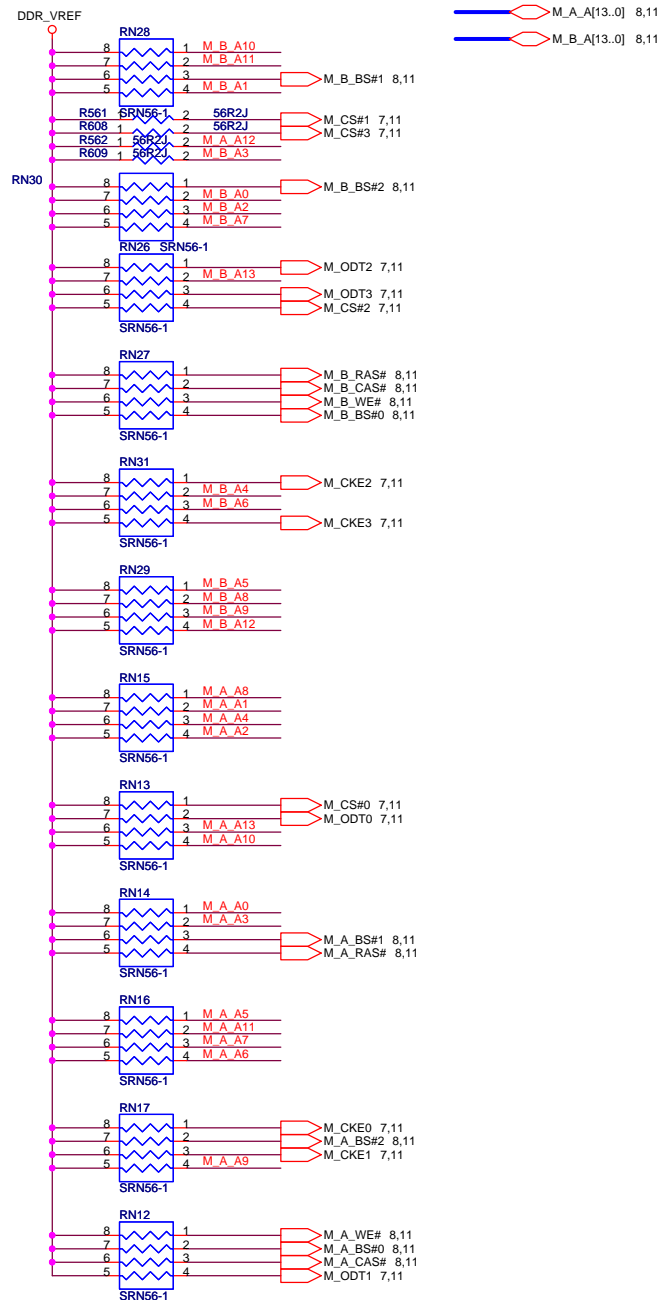
FOR DDR2





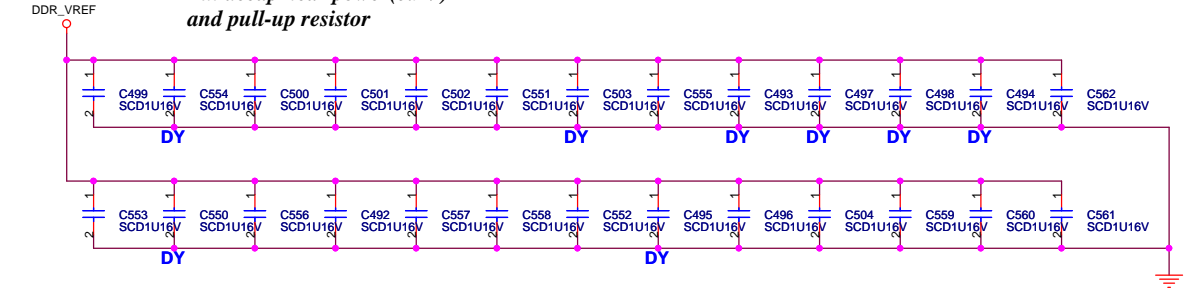
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

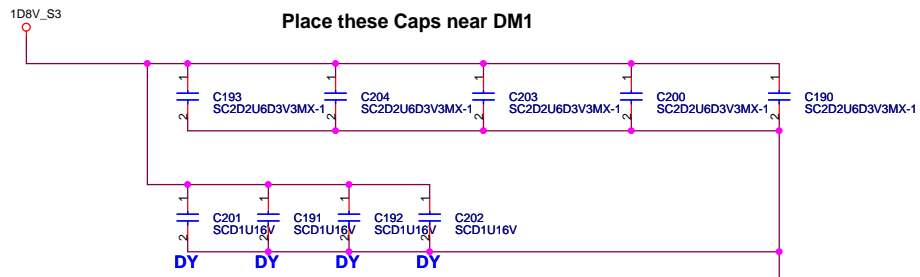


Decoupling Capacitor

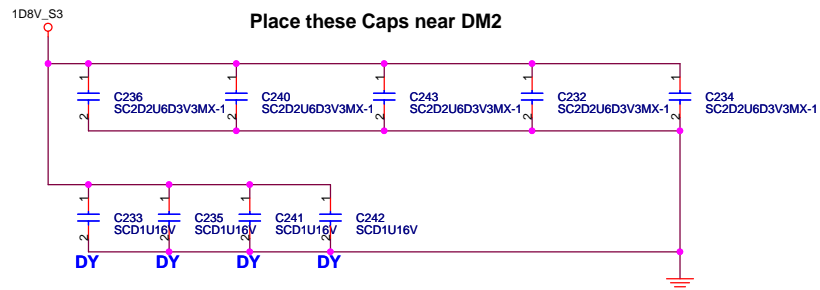
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



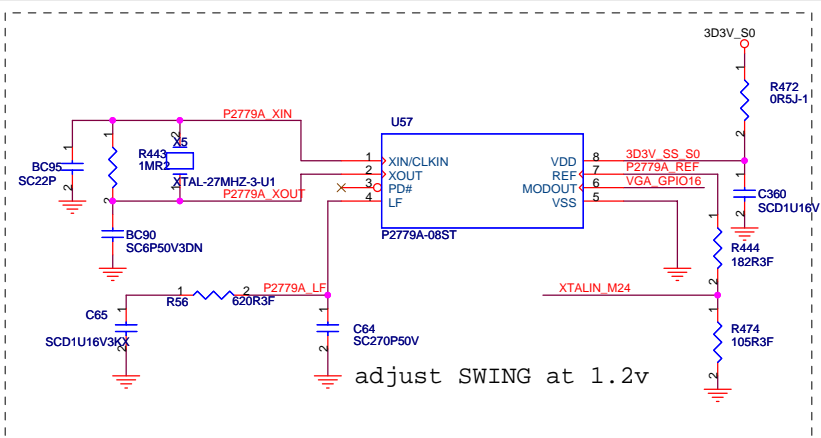
<Core Design>

緯創資通

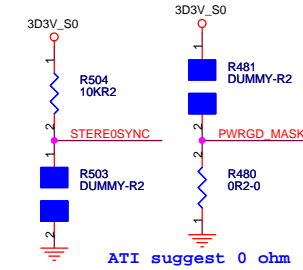
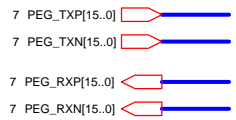
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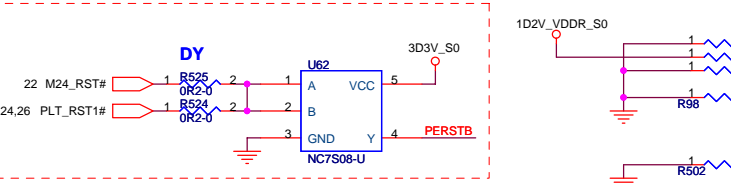
| | | |
|---|------------------------------------|------------------|
| Title DDR2 Termination Resistor | | |
| Size A3 | Document Number Leopard2 | Rev -1 |
| Date: Thursday, July 07, 2005 | Sheet 12 of 47 | |



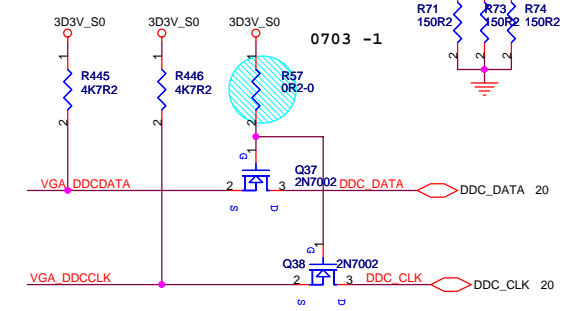
adjust SWING at 1.2v



ATI suggest 0 ohm



DDC_CLK & DATA level shift



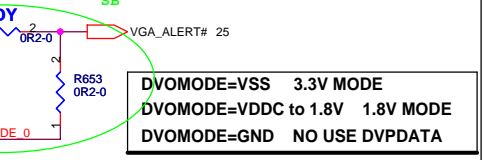
| | | |
|-----------|------|------------|
| PEG_TXP0 | AH30 | PCIE_RX0P |
| PEG_TXN0 | AG30 | PCIE_RX0N |
| PEG_TXP1 | AG29 | PCIE_RX1P |
| PEG_TXN1 | AF29 | PCIE_RX1N |
| PEG_TXP2 | AE29 | PCIE_RX2P |
| PEG_TXN2 | AE30 | PCIE_RX2N |
| PEG_TXP3 | AD29 | PCIE_RX3P |
| PEG_TXN3 | AD29 | PCIE_RX3N |
| PEG_TXP4 | AC29 | PCIE_RX4P |
| PEG_TXN4 | AB29 | PCIE_RX4N |
| PEG_TXP5 | AB30 | PCIE_RX5P |
| PEG_TXN5 | AA30 | PCIE_RX5N |
| PEG_TXP6 | AA29 | PCIE_RX6P |
| PEG_TXN6 | AA29 | PCIE_RX6N |
| PEG_TXP7 | W29 | PCIE_RX7P |
| PEG_TXN7 | W30 | PCIE_RX7N |
| PEG_TXP8 | W30 | PCIE_RX8P |
| PEG_TXN8 | V30 | PCIE_RX8N |
| PEG_TXP9 | V29 | PCIE_RX9P |
| PEG_TXN9 | T29 | PCIE_RX9N |
| PEG_TXP10 | T30 | PCIE_RX10P |
| PEG_TXN10 | R30 | PCIE_RX10N |
| PEG_TXP11 | R29 | PCIE_RX11P |
| PEG_TXN11 | P29 | PCIE_RX11N |
| PEG_TXP12 | N29 | PCIE_RX12P |
| PEG_TXN12 | M30 | PCIE_RX12N |
| PEG_TXP13 | M30 | PCIE_RX13P |
| PEG_TXN13 | M29 | PCIE_RX13N |
| PEG_TXP14 | L29 | PCIE_RX14P |
| PEG_TXN14 | K29 | PCIE_RX14N |
| PEG_TXP15 | K30 | PCIE_RX15P |
| PEG_TXN15 | J30 | PCIE_RX15N |

| | | | | | | |
|-----------|------|---|---|-------|------|------------|
| PEG_RXP0 | C110 | 1 | 2 | RXP0 | AF26 | PCIE_TX0P |
| PEG_RXN0 | C109 | 1 | 2 | RXN0 | AE26 | PCIE_TX0N |
| PEG_RXP1 | C391 | 1 | 2 | RXP1 | AC25 | PCIE_TX1P |
| PEG_RXN1 | C392 | 1 | 2 | RXN1 | AB25 | PCIE_TX1N |
| PEG_RXP2 | C111 | 1 | 2 | RXP2 | AC27 | PCIE_TX2P |
| PEG_RXN2 | C112 | 1 | 2 | RXN2 | AC26 | PCIE_TX2N |
| PEG_RXP3 | C393 | 1 | 2 | RXP3 | AC26 | PCIE_TX3P |
| PEG_RXN3 | C390 | 1 | 2 | RXN3 | AB26 | PCIE_TX3N |
| PEG_RXP4 | C120 | 1 | 2 | RXP4 | Y25 | PCIE_TX4P |
| PEG_RXN4 | C121 | 1 | 2 | RXN4 | W25 | PCIE_TX4N |
| PEG_RXP5 | C412 | 1 | 2 | RXP5 | Y27 | PCIE_TX5P |
| PEG_RXN5 | C414 | 1 | 2 | RXN5 | W27 | PCIE_TX5N |
| PEG_RXP6 | C123 | 1 | 2 | RXP6 | V26 | PCIE_TX6P |
| PEG_RXN6 | C122 | 1 | 2 | RXN6 | W25 | PCIE_TX6N |
| PEG_RXP7 | C413 | 1 | 2 | RXP7 | U27 | PCIE_TX7P |
| PEG_RXN7 | C411 | 1 | 2 | RXN7 | T25 | PCIE_TX7N |
| PEG_RXP8 | C137 | 1 | 2 | RXP8 | U27 | PCIE_TX8P |
| PEG_RXN8 | C134 | 1 | 2 | RXN8 | T27 | PCIE_TX8N |
| PEG_RXP9 | C435 | 1 | 2 | RXP9 | U26 | PCIE_TX9P |
| PEG_RXN9 | C436 | 1 | 2 | RXN9 | T26 | PCIE_TX9N |
| PEG_RXP10 | C135 | 1 | 2 | RXP10 | P26 | PCIE_TX10P |
| PEG_RXN10 | C133 | 1 | 2 | RXN10 | N25 | PCIE_TX10N |
| PEG_RXP11 | C433 | 1 | 2 | RXP11 | N27 | PCIE_TX11P |
| PEG_RXN11 | C434 | 1 | 2 | RXN11 | P27 | PCIE_TX11N |
| PEG_RXP12 | C136 | 1 | 2 | RXP12 | P26 | PCIE_TX12P |
| PEG_RXN12 | C146 | 1 | 2 | RXN12 | N26 | PCIE_TX12N |
| PEG_RXP13 | C455 | 1 | 2 | RXP13 | L26 | PCIE_TX13P |
| PEG_RXN13 | C456 | 1 | 2 | RXN13 | K25 | PCIE_TX13N |
| PEG_RXP14 | C145 | 1 | 2 | RXP14 | L27 | PCIE_TX14P |
| PEG_RXN14 | C147 | 1 | 2 | RXN14 | K27 | PCIE_TX14N |
| PEG_RXP15 | C454 | 1 | 2 | RXP15 | L26 | PCIE_TX15P |
| PEG_RXN15 | C457 | 1 | 2 | RXN15 | K26 | PCIE_TX15N |

| | |
|-------------|--------------|
| AF27 | PCIE_REFCLKP |
| AF27 | PCIE_REFCLKN |
| PCIE_CALRP | AC23 |
| PCIE_CALRN | AB24 |
| PCIE_CALI | AB23 |
| PCIE_TEST | |
| PCIE_TESTIN | AE25 |
| PERSTB | AD25 |
| PWRGD_MASK | AD24 |
| ATI_R2SET | AH21 |
| R2SET | |
| Y_G | |
| C_R_PR | |
| COMP_B_PB | |
| H2SYNC | VS2SYNC |
| VS2SYNC | |
| DDC3CLK | AG22 |
| DDC3DATA | AG23 |
| SSIN | AJ23 |
| SSOUT | AH24 |
| XTALIN | AH28 |
| XTALOUT | AJ29 |
| TESTEN | AH27 |
| TEST_YCLK | E8 |
| TEST_MCLK | B6 |
| PLLTEST | AF25 |
| STEREO_SYNC | AH25 |

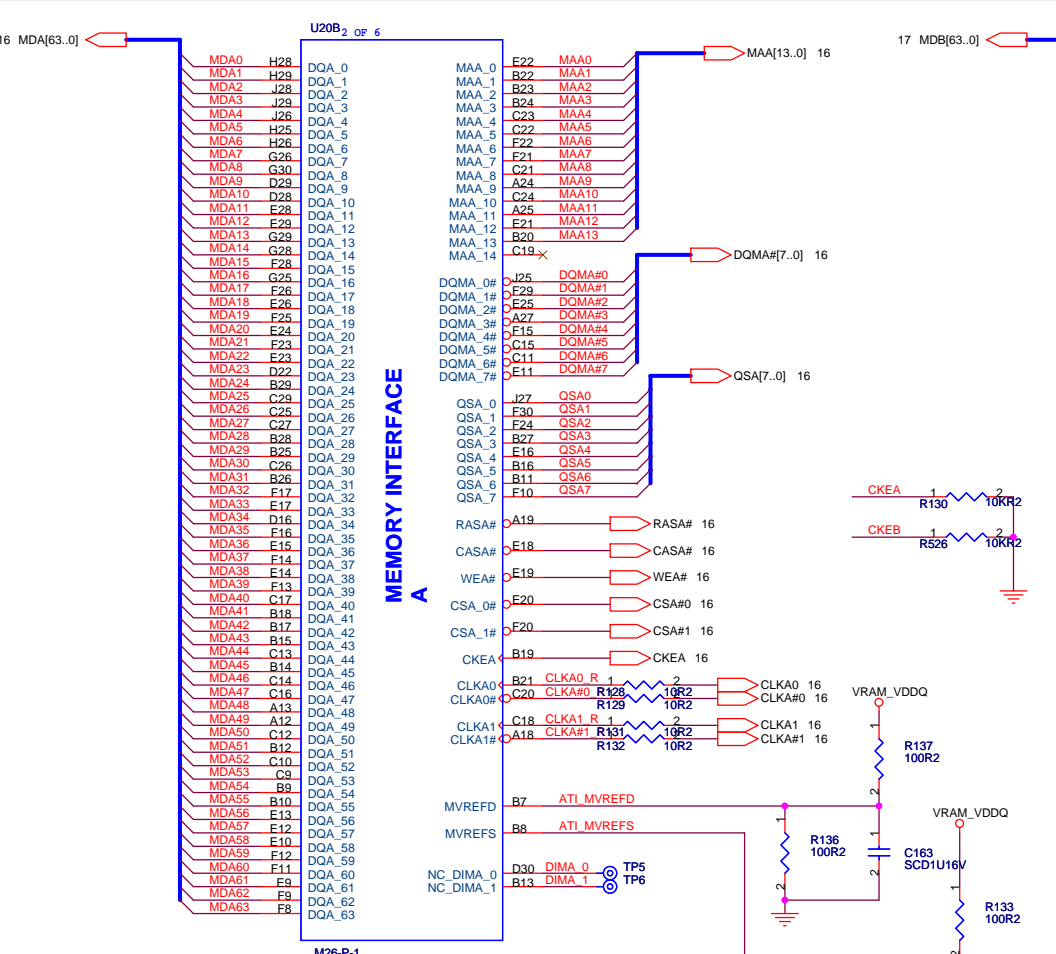
| | | |
|--------------|------|-------------|
| GPIO_0 | AJ5 | VGA_GPIO0 |
| GPIO_1 | AH5 | VGA_GPIO1 |
| GPIO_2 | AJ4 | VGA_GPIO2 |
| GPIO_3 | AK4 | VGA_GPIO3 |
| GPIO_4 | AH4 | VGA_GPIO4 |
| GPIO_5 | AF4 | VGA_GPIO5 |
| GPIO_6 | AJ3 | VGA_GPIO6 |
| GPIO_7 | AK3 | VGA_GPIO7 |
| GPIO_8 | AH3 | VGA_GPIO8 |
| GPIO_9 | AJ2 | VGA_GPIO9 |
| GPIO_10 | AH2 | VGA_GPIO10 |
| GPIO_11 | AH1 | VGA_GPIO11 |
| GPIO_12 | AG2 | VGA_GPIO12 |
| GPIO_13 | AG1 | VGA_GPIO13 |
| GPIO_14 | AG3 | VGA_GPIO14 |
| GPIO_17 | C6 | |
| GPIO_PWRCTRL | AF3 | VGA_PWRCTRL |
| GPIO_MEMSSIN | AF2 | VGA_GPIO16 |
| DVOMODE | AE10 | DVOMODE |
| DVPDATA_0 | AH6 | DVPDATA_0 |
| DVPDATA_1 | AJ6 | DVPDATA_1 |
| DVPDATA_2 | AK6 | DVPDATA_2 |
| DVPDATA_3 | AK7 | |
| DVPDATA_4 | AJ7 | |
| DVPDATA_5 | AH7 | |
| DVPDATA_6 | AJ8 | |
| DVPDATA_7 | AH8 | |
| DVPDATA_8 | AJ9 | |
| DVPDATA_9 | AK9 | |
| DVPDATA_10 | AH10 | |
| DVPDATA_11 | AE8 | |
| DVPDATA_12 | AG6 | |
| DVPDATA_13 | AG7 | |
| DVPDATA_14 | AF6 | |
| DVPDATA_15 | AE7 | |
| DVPDATA_16 | AF7 | |
| DVPDATA_17 | AG8 | |
| DVPDATA_18 | AF8 | |
| DVPDATA_19 | AE9 | |
| DVPDATA_20 | AG9 | |
| DVPDATA_21 | AF9 | |
| DVPDATA_22 | AG10 | |
| DVPDATA_23 | AE10 | |
| DVPCNTL_0 | AJ10 | DVPCNTL_0 |
| DVPCNTL_1 | AK10 | DVPCNTL_1 |
| DVPCNTL_2 | AJ11 | DVPCNTL_2 |
| DVPCNTL_3 | AK11 | DVPCNTL_3 |
| VREFG | AG4 | ATI VREFG |
| TXOUT_L0N | AH15 | TXAOUT0- |
| TXOUT_L0P | AH16 | TXAOUT0+ |
| TXOUT_L1N | AJ16 | TXAOUT1- |
| TXOUT_L1P | AJ17 | TXAOUT1+ |
| TXOUT_L2N | AH18 | TXAOUT2- |
| TXOUT_L2P | AJ20 | TXAOUT2+ |
| TXOUT_L3N | AJ21 | |
| TXOUT_L3P | AK19 | |
| TXCLK_LN | AJ19 | TXACLK- |
| TXCLK_LP | AG16 | TXACLK+ |
| TXOUT_U0N | AG17 | TXBOUT0- |
| TXOUT_U0P | AE16 | TXBOUT0+ |
| TXOUT_U1N | AE17 | TXBOUT1- |
| TXOUT_U1P | AE18 | TXBOUT1+ |
| TXOUT_U2P | AE19 | TXBOUT2+ |
| TXOUT_U3N | AE19 | TXBOUT2- |
| TXOUT_U3P | AE20 | |
| TXCLK_UN | AG20 | TXBCLK- |
| TXCLK_UP | AG20 | TXBCLK+ |
| DIGON | AE12 | LCDVDD_ON |
| BLON | AG12 | BL_ON |
| TX0M | AK13 | |
| TX0P | AJ14 | |
| TX1N | AJ15 | |
| TX1P | AK15 | |
| TX2M | AK16 | |
| TX2P | AJ12 | |
| TXCM | AK12 | |
| TXCP | AK12 | |
| DDC3CLK | AE13 | |
| DDC3DATA | AE14 | |
| HPD1 | AF12 | HPD |
| R_G_B | AK27 | VGA_RED |
| | AJ27 | VGA_GREEN |
| | AJ26 | VGA_BLUE |
| HSYNC | AJ25 | VGA_HSYNC |
| VS2SYNC | AK25 | VGA_VS2SYNC |
| RSET | AH26 | ATI_RSET |
| DDC1DATA | AG25 | VGA_DDCDATA |
| DDC1CLK | AG24 | VGA_DDCCLK |
| GPIO_AUXWIN | AG24 | GPIO_AUXWIN |
| DPLUS | AJ11 | THERMDP_M24 |
| DMINUS | AE11 | THERMDN_M24 |

| |
|----------------------|
| PCI EXPRESS |
| DVO / EXT TMS / GPIO |
| LVDS |
| TMS |
| SS |
| DAC2 |
| DAC1 |
| CLK |
| THERM |



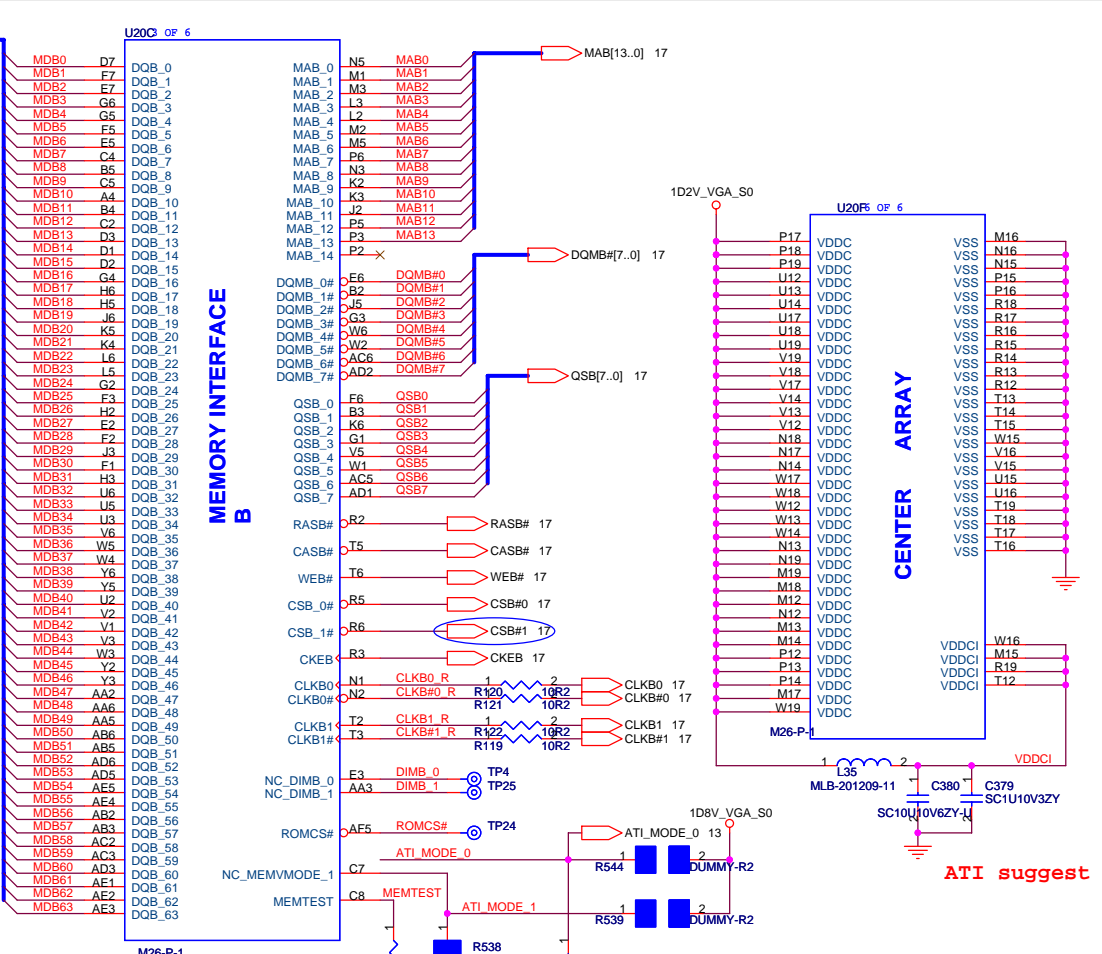
DVOMODE=VSS 3.3V MODE
DVOMODE=VDDC to 1.8V 1.8V MODE
DVOMODE=GND NO USE DVPDATA

| STRAPS | PIN | DEFAULT |
|------------------|-----------|---------|
| CAL_BG_BACKUP | GPIO0 | 0 |
| PLL_CAL_FORCE_EN | GPIO1 | 0 |
| PCIE_MODE(1:0) | GPIO(3:2) | 00 |
| CAL_OFF | GPIO4 | 0 |
| BYPASS_PLL | GPIO | |



MEMORY CHANNEL A

As close to CHIP as possible



MEMORY CHANNEL B

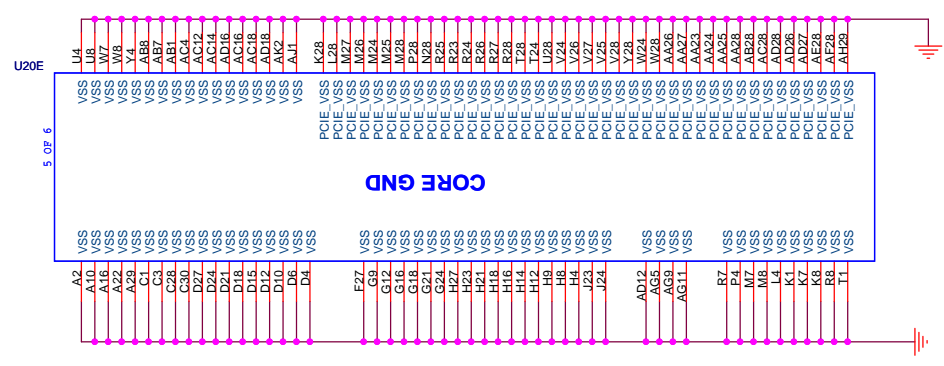
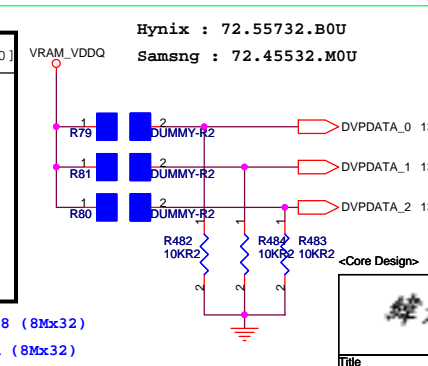
ATI suggest

| VDDR1 | MEMVMODE_0 | MEMVMODE_1 |
|-------|------------|------------|
| 1.8V | GND | +VDDC_CT |
| 2.5V | +VDDC_CT | GND |
| 2.8V | +VDDC_CT | +VDDC_CT |

VRAM Selection

| Vendor/Size | SETTING DVPDATA[2:0] |
|--------------|----------------------|
| HYNIX/128M | 000 |
| SAMSUNG/128M | 001 |
| RESERVED | 010 |
| RESERVED | 011 |
| RESERVED | 100 |
| RESERVED | 101 |
| RESERVED | 110 |
| RESERVED | 111 |

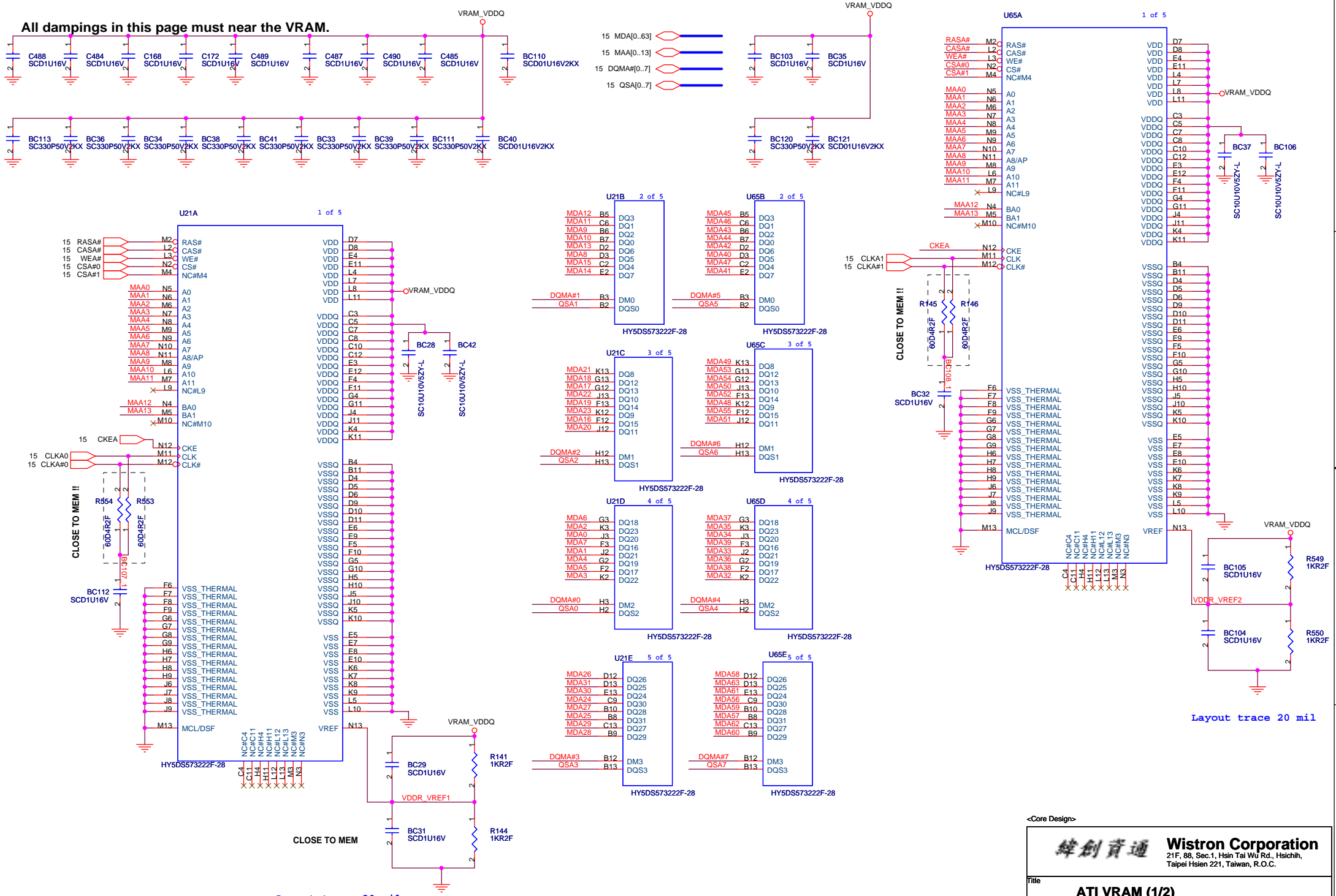
Hynix : HY5DS73222F(P)-28 (8Mx32)
 Samsung : K4D53235F-VC2A (8Mx32)



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ATI(3 of 3)
 Leopard2
 Date: Thursday, July 07, 2005 Sheet 15 of 47

All dampings in this page must near the VRAM.



Layout trace 20 mil

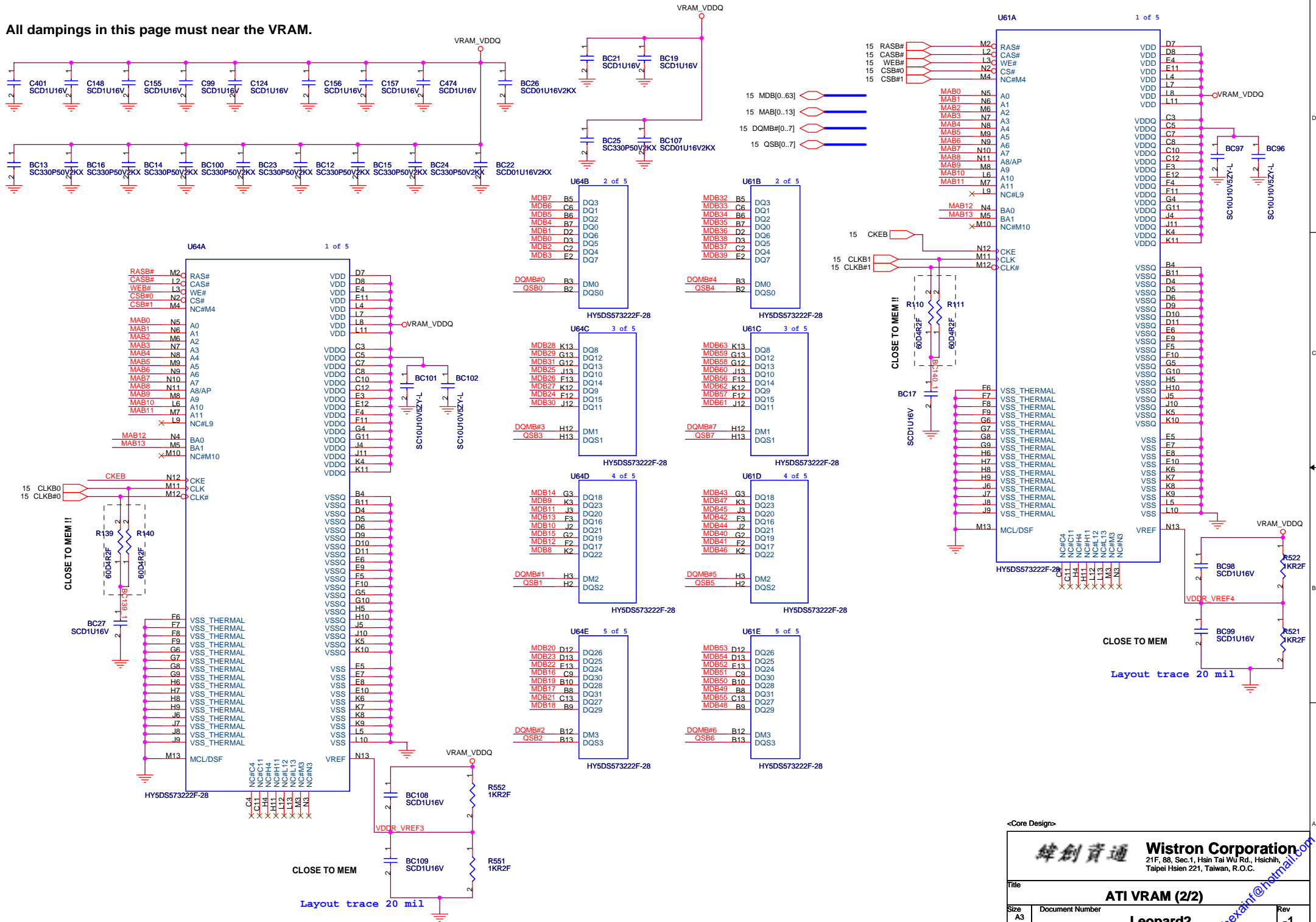
Layout trace 20 mil

<Core Design>

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| | | | |
|-------|-------------------------|-----------------|----------|
| Title | ATI VRAM (1/2) | | Rev |
| Size | A3 | Document Number | Leopard2 |
| Date: | Thursday, July 07, 2005 | Sheet | 16 of 47 |

All dampings in this page must near the VRAM.



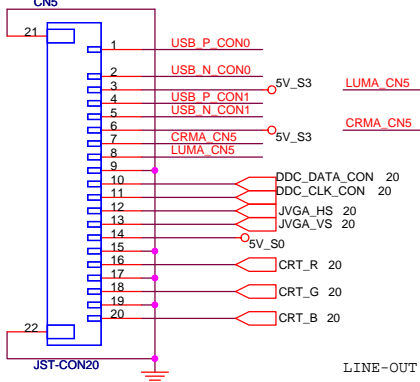
<Core Design>

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

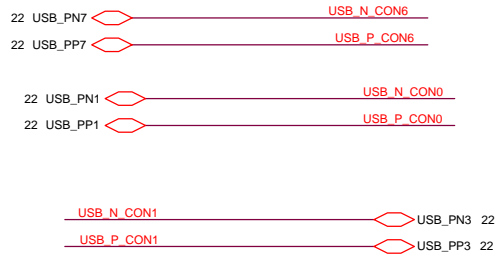
| | | |
|--------------------------------|------------------------------------|------------------|
| Title ATI VRAM (2/2) | | |
| Size A3 | Document Number Leopard2 | Rev -1 |
| Date: Thursday, July 07, 2005 | Sheet 17 | of 47 |

hexair@netmail.com

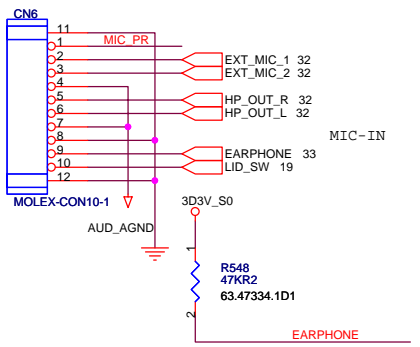
Digital Signal CONN



Close to Docking CN

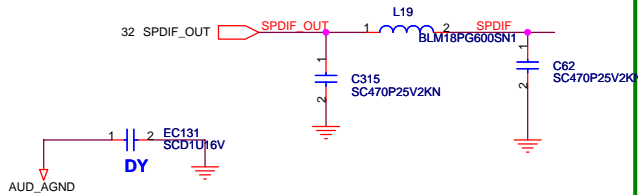
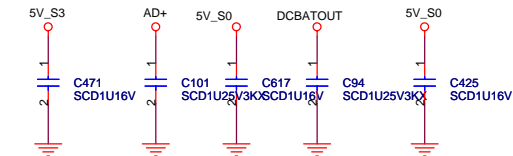
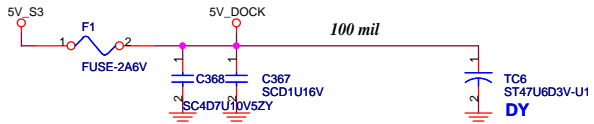
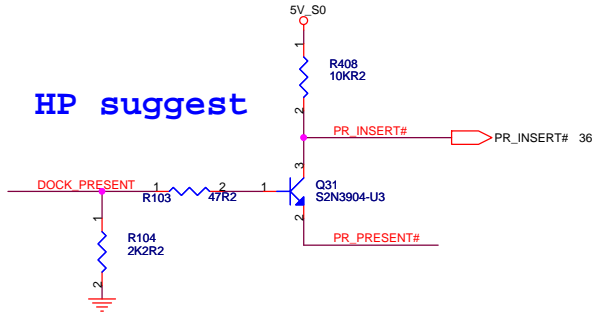


Analog Signal CONN



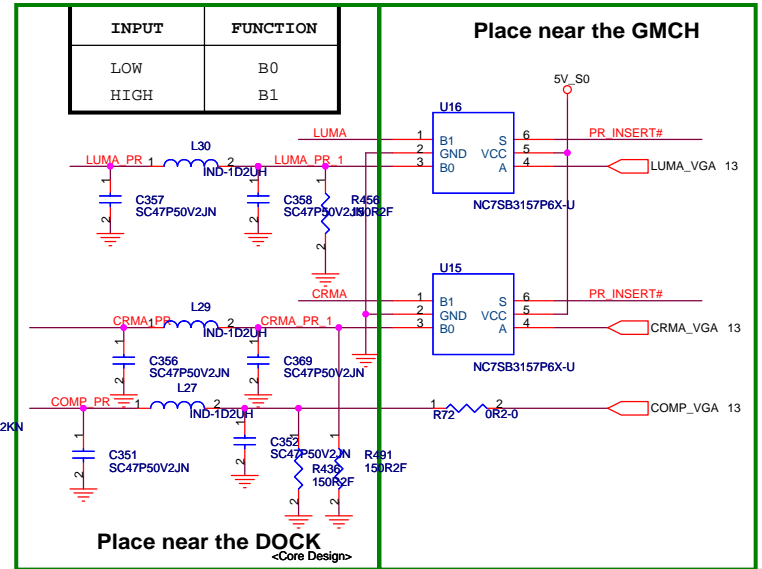
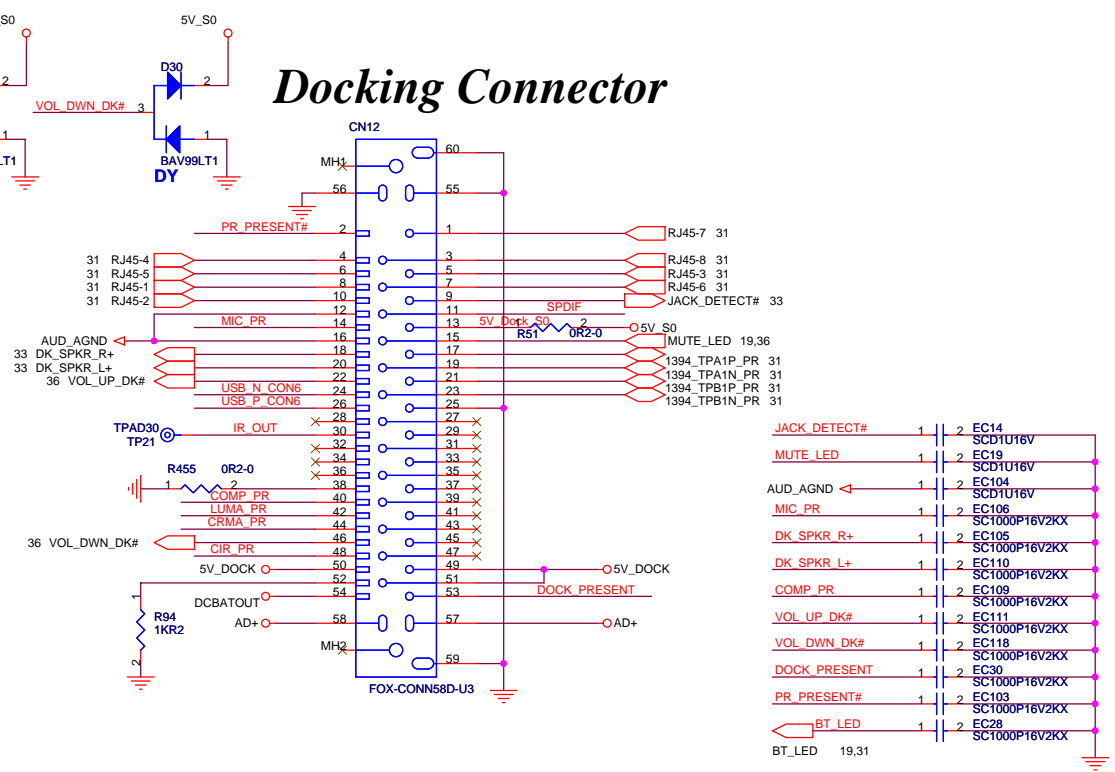
Please close to ICH6

HP suggest



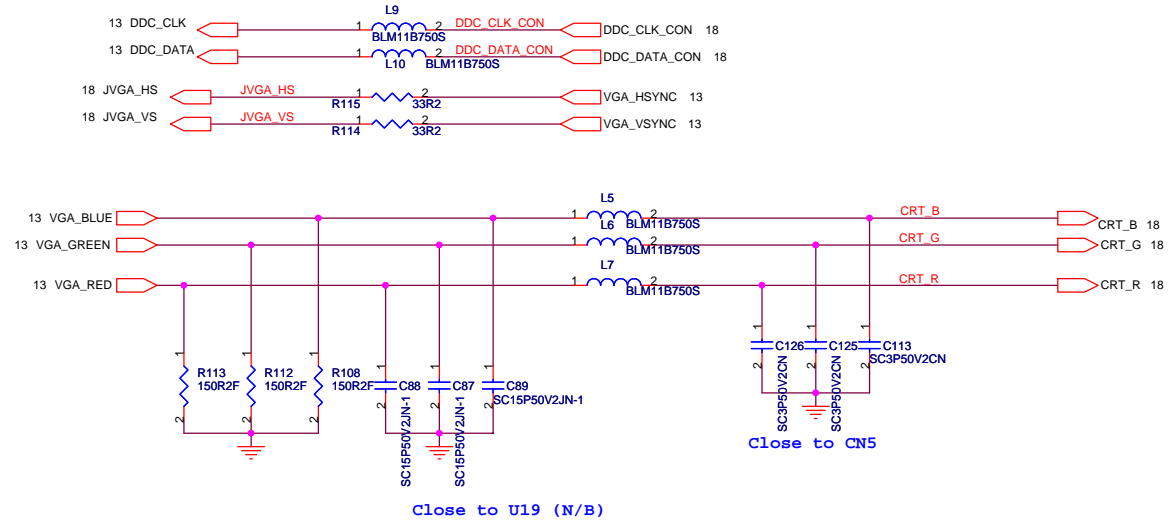
CIR, CIR_PR, CIR_KBC are connect together. default setting 12/12

Docking Connector



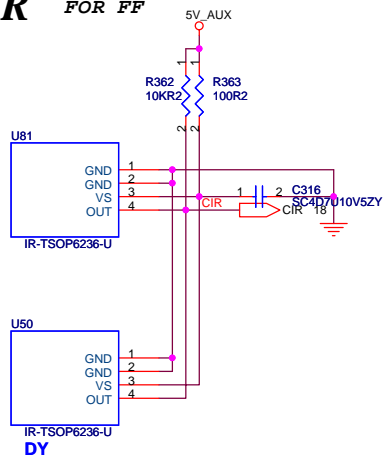
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CRT



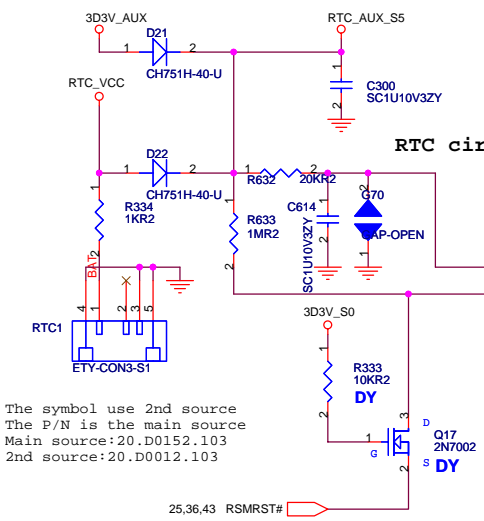
010804 Modified on Astro ID request

CIR FOR FF

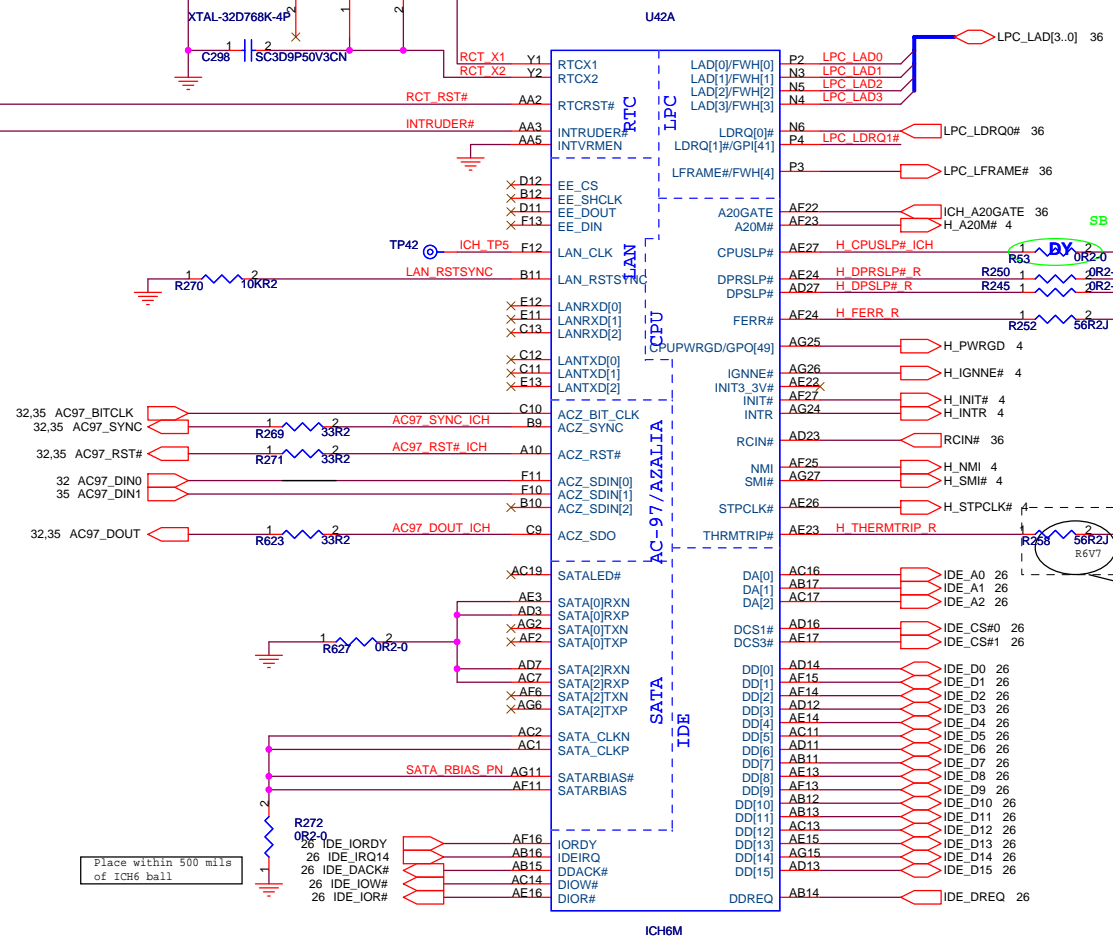


<Core Design>

| | |
|---|---|
|  Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title CRT/ CIR | |
| Size A3 | Document Number Leopard2 |
| Date: Thursday, July 07, 2005 | Rev -1 |
| Sheet 20 of 47 | |



The symbol use 2nd source
 The P/N is the main source
 Main source: 20.D0152.103
 2nd source: 20.D0012.103



Place within 500 mils of ICH6 ball

Layout Note: R6V7 needs to be placed within 2" of ICH6, R6V9 must be placed within 2" of R6V7 w/o stub.

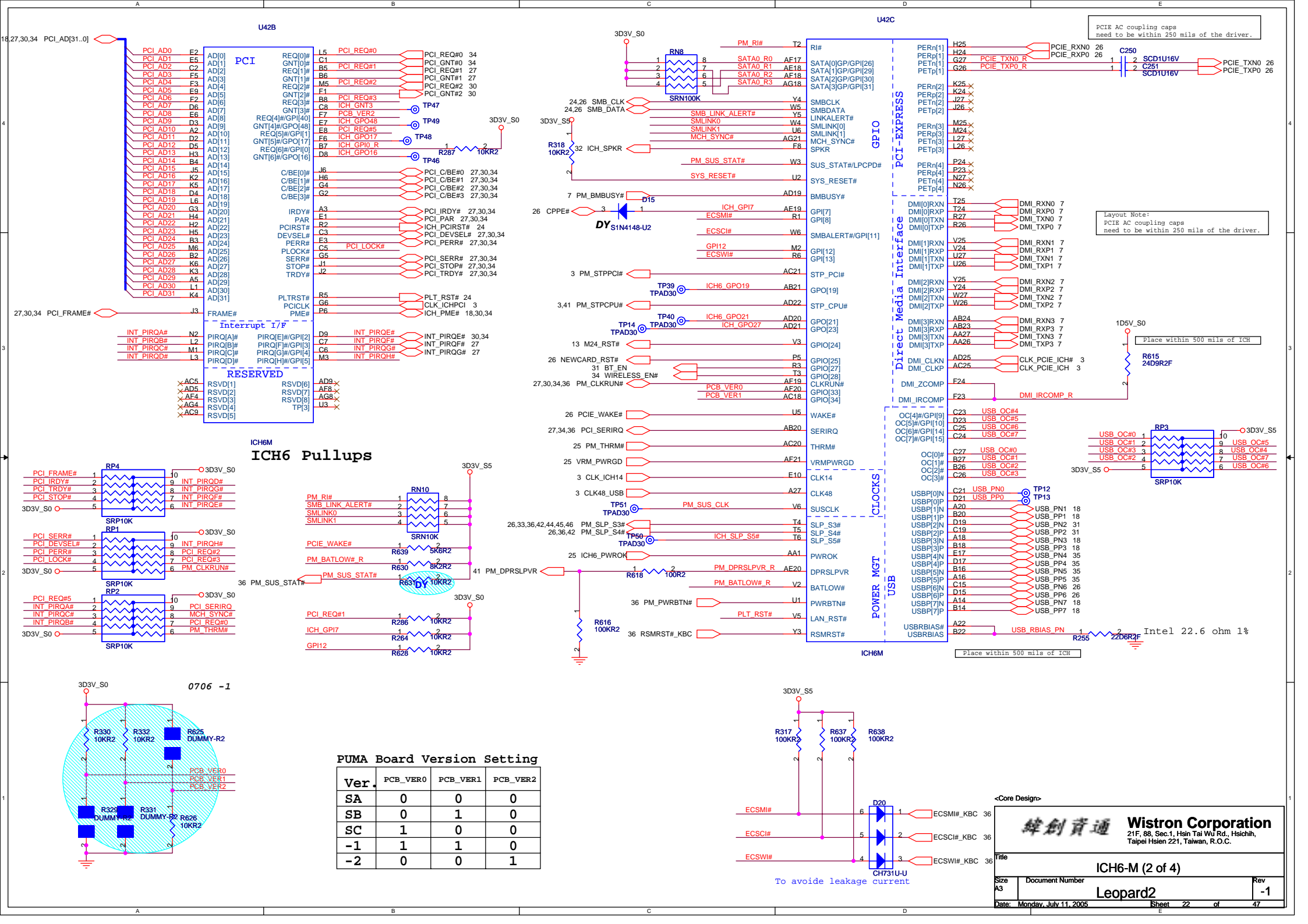
<Core Design>

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Title: **ICH6-M (1 of 4)**

Size: A3 Document Number: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet: 21 of 47



U42B

U42C

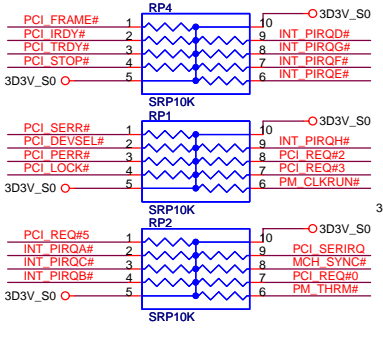
PCI AC coupling caps need to be within 250 mils of the driver.

Layout Note: PCI AC coupling caps need to be within 250 mils of the driver.

Place within 500 mils of ICH

Place within 500 mils of ICH

ICH6M Pullups



0706 -1

PUMA Board Version Setting

| Ver. | PCB_VER0 | PCB_VER1 | PCB_VER2 |
|------|----------|----------|----------|
| SA | 0 | 0 | 0 |
| SB | 0 | 1 | 0 |
| SC | 1 | 0 | 0 |
| -1 | 1 | 1 | 0 |
| -2 | 0 | 0 | 1 |

To avoid leakage current

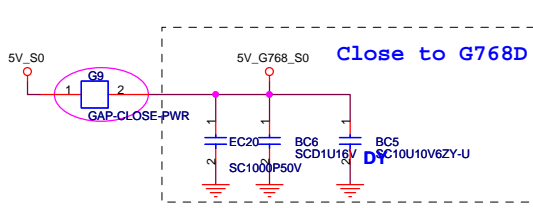
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

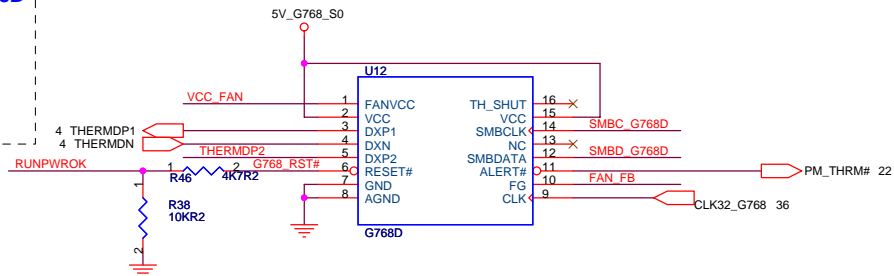
Title: **ICH6-M (2 of 4)**

Size: **Leopard2**

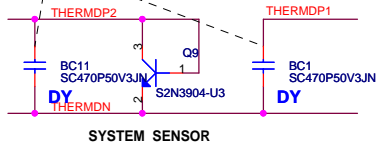
Date: Monday, July 11, 2005 Sheet 22 of 47



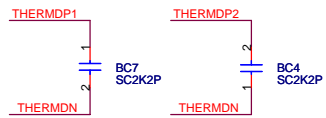
Reserve for G768B works at High Speed



Put these two Caps near the thermal diode.

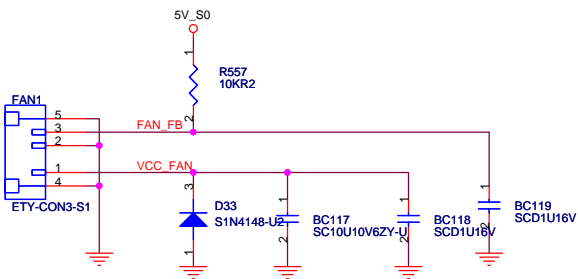


SYSTEM SENSOR

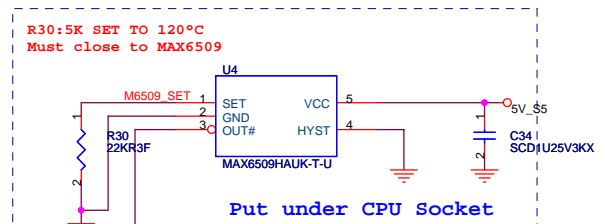
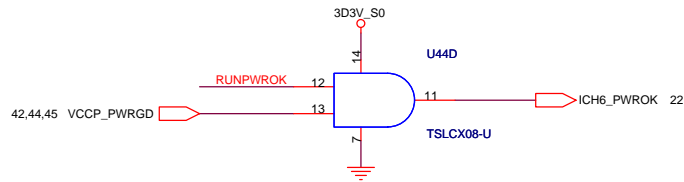
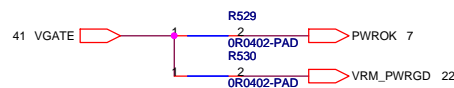
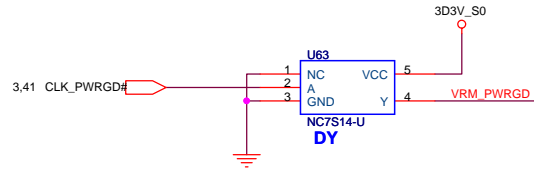


THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B

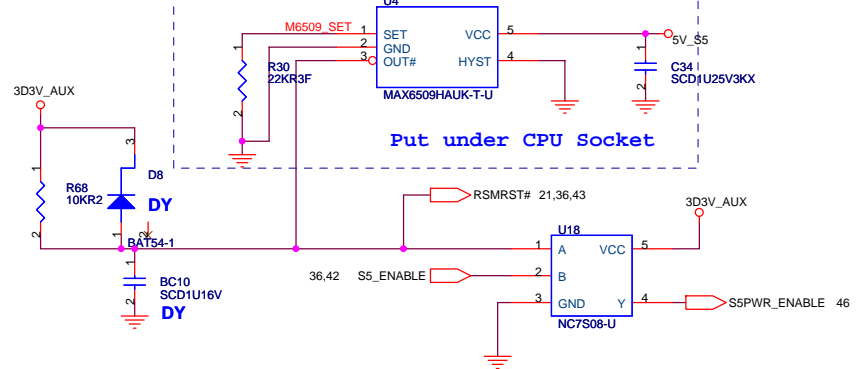
180 ms after VCC_G768 > 4.38v, p2, 7



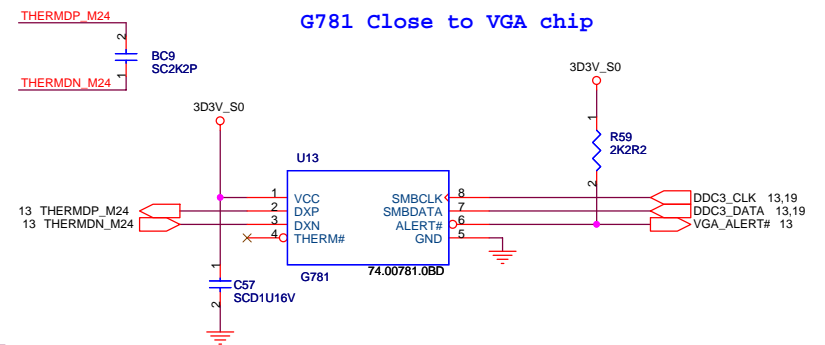
The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103



Put under CPU Socket



G781 Close to VGA chip



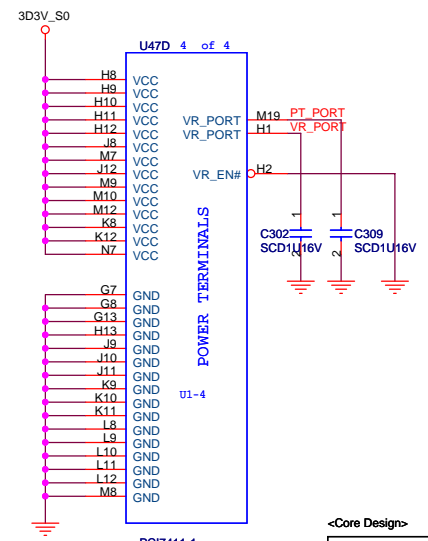
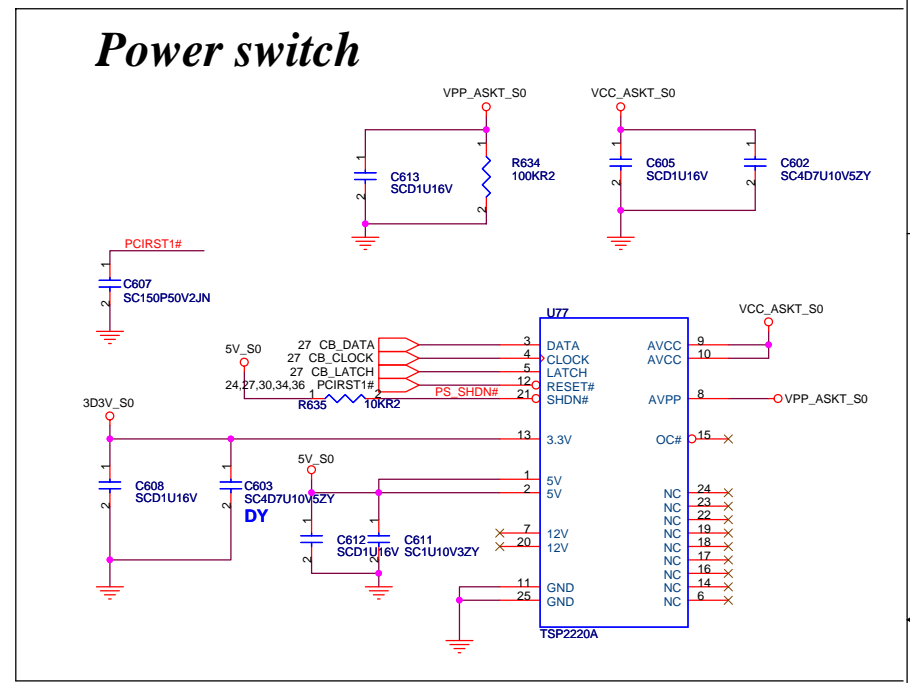
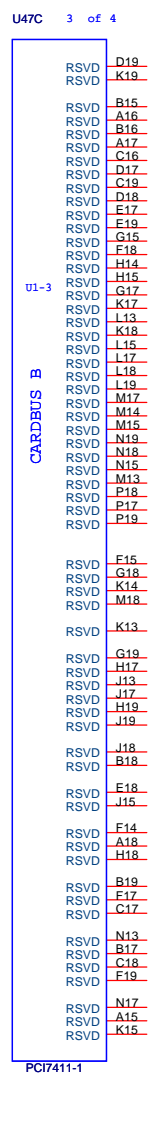
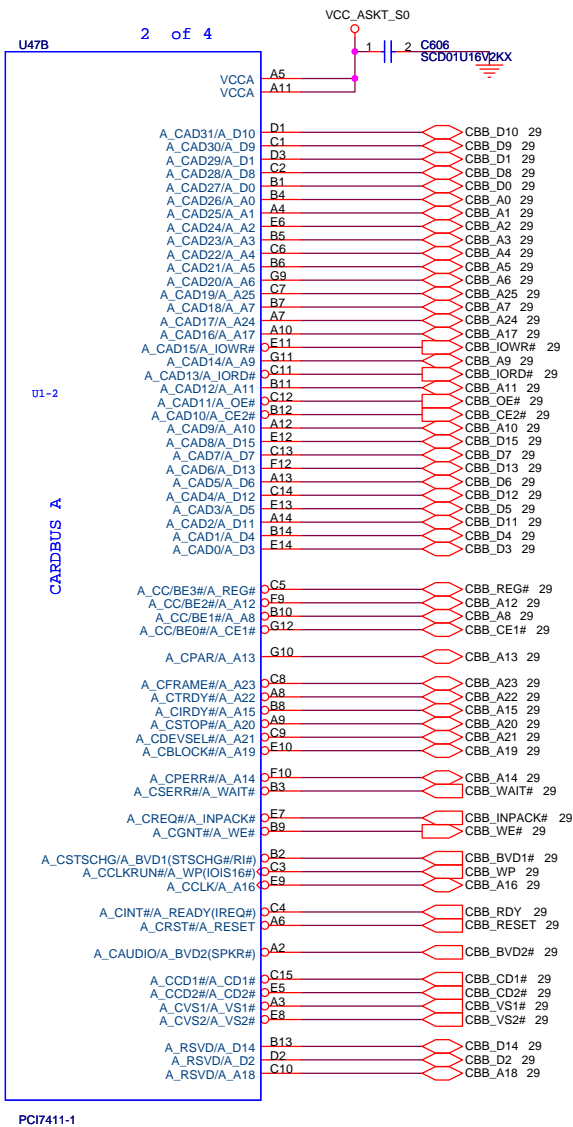
<Core Design>

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Title: **G768D**

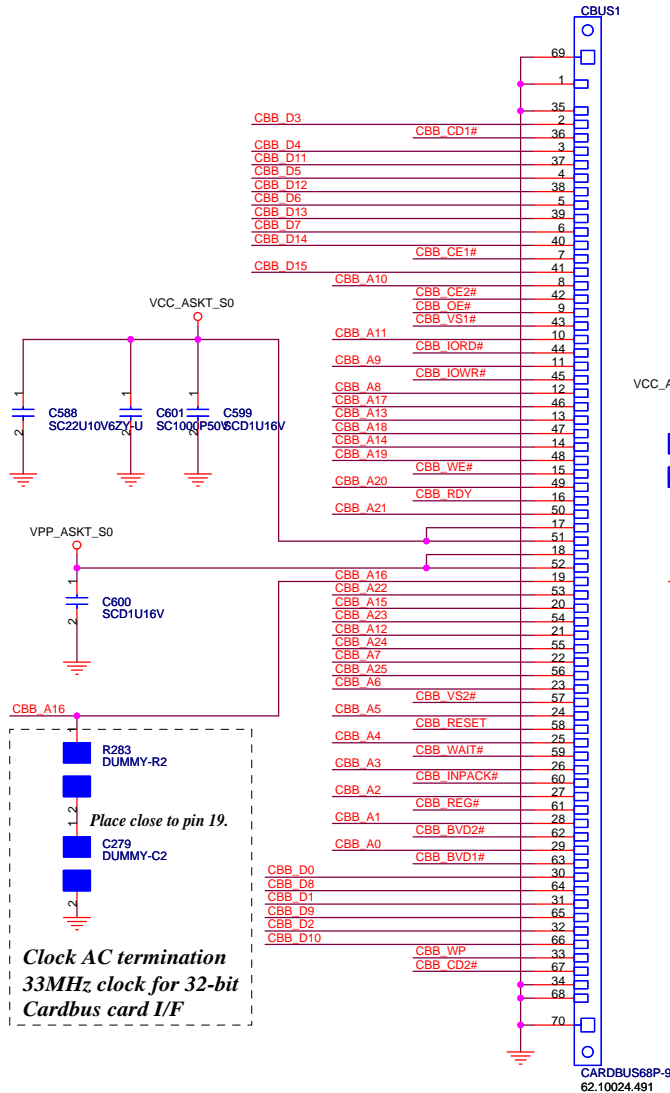
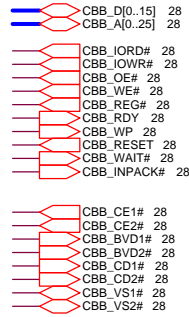
Size: A3 Document Number: **Leopard2** Rev: -1

Date: Monday, July 11, 2005 Sheet 25 of 47

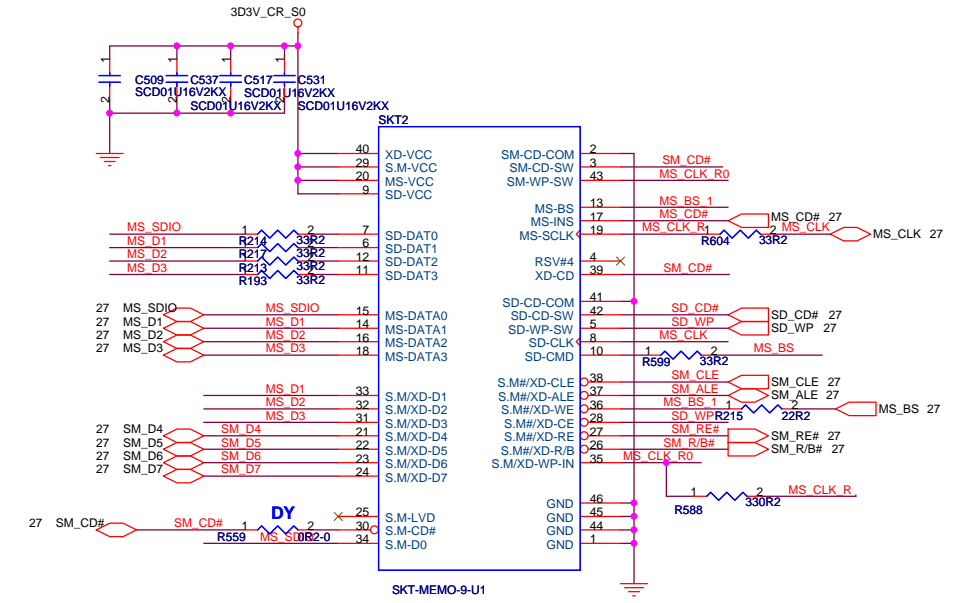


PCMCIA Socket

Cardbus I/F



6 in 1 Connector

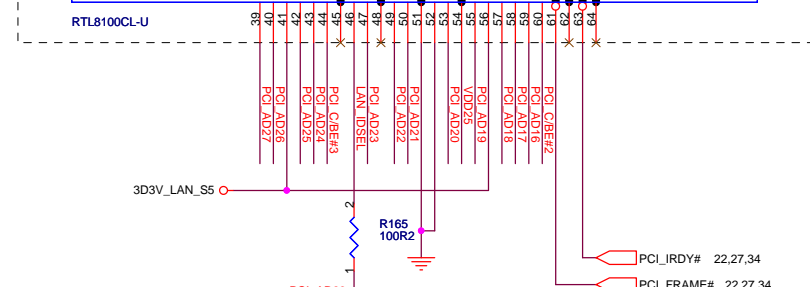
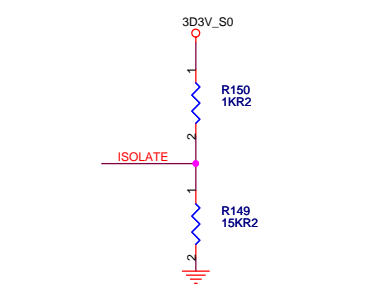
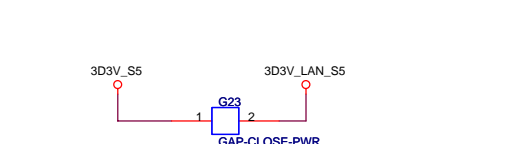
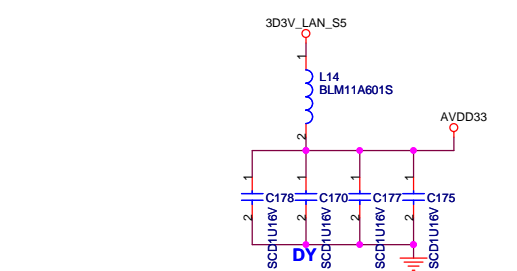
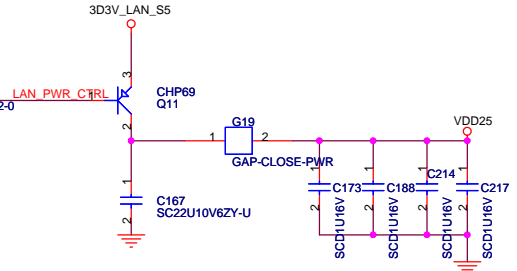
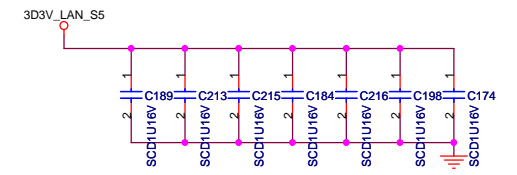
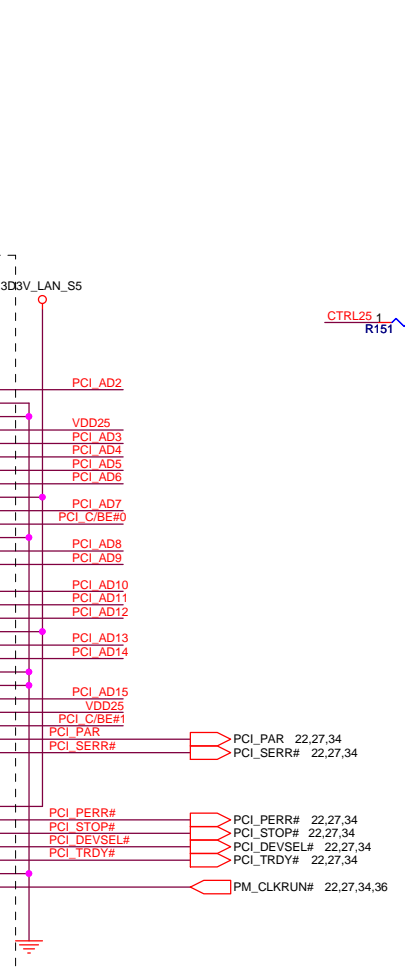
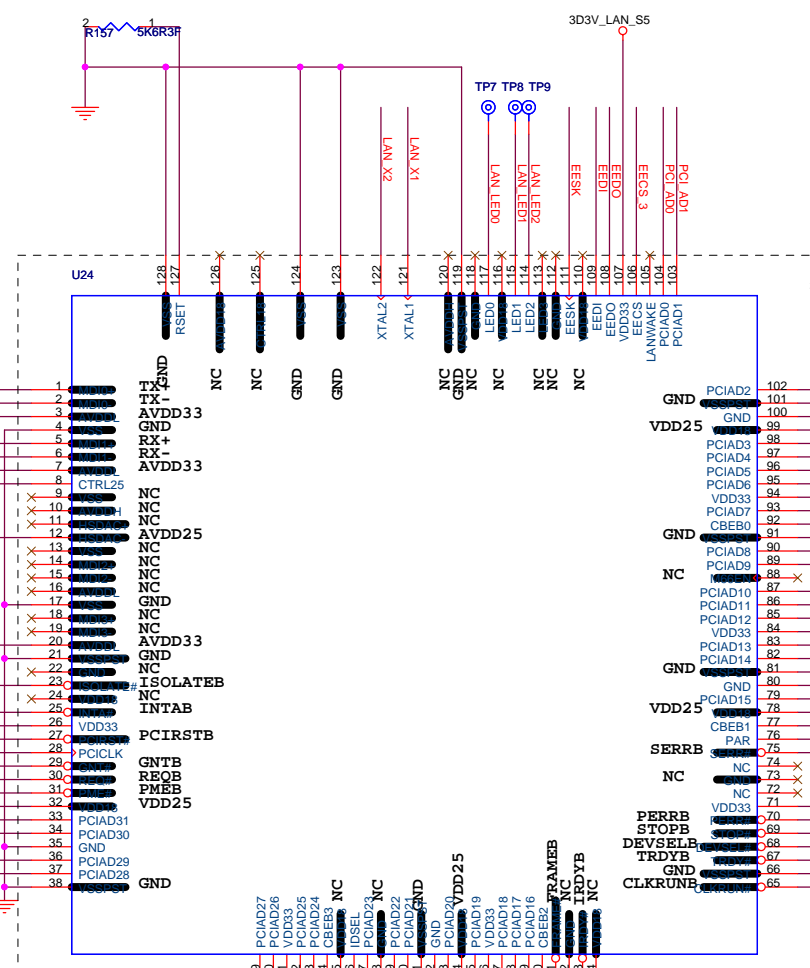
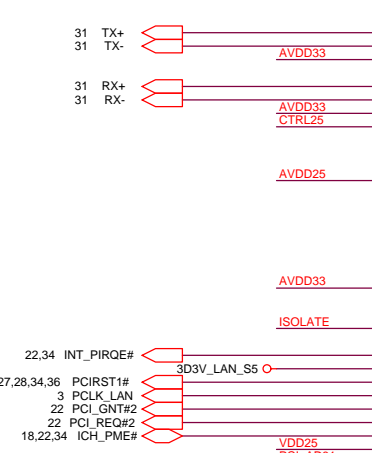
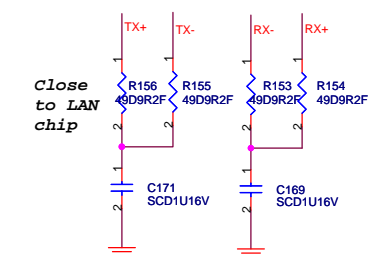
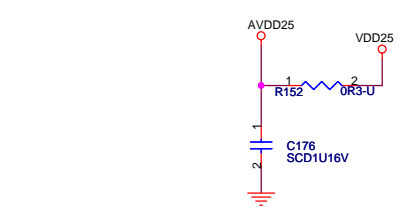
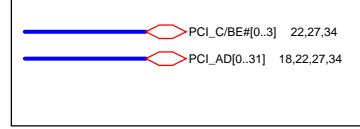
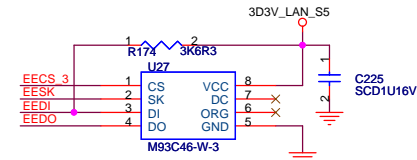
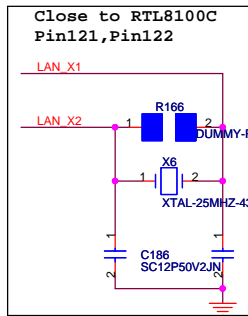


Clock AC termination
33MHz clock for 32-bit
Cardbus card I/F

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

PCMCIA SLOT/ CARDBUS SKT
Leopard2

Title: PCMCIA SLOT/ CARDBUS SKT
 Size: A3
 Document Number: Leopard2
 Date: Thursday, July 07, 2005
 Sheet: 29 of 47



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN RTL8100C**

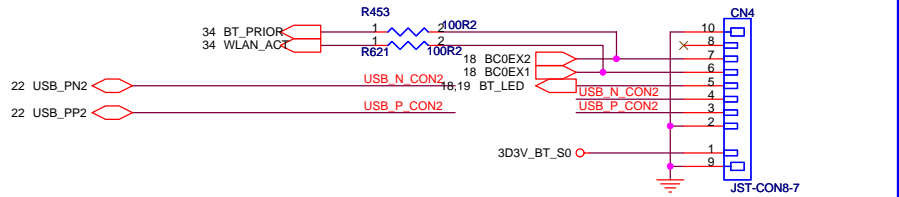
Size A3 Document Number: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet 30 of 47

Blue thumb

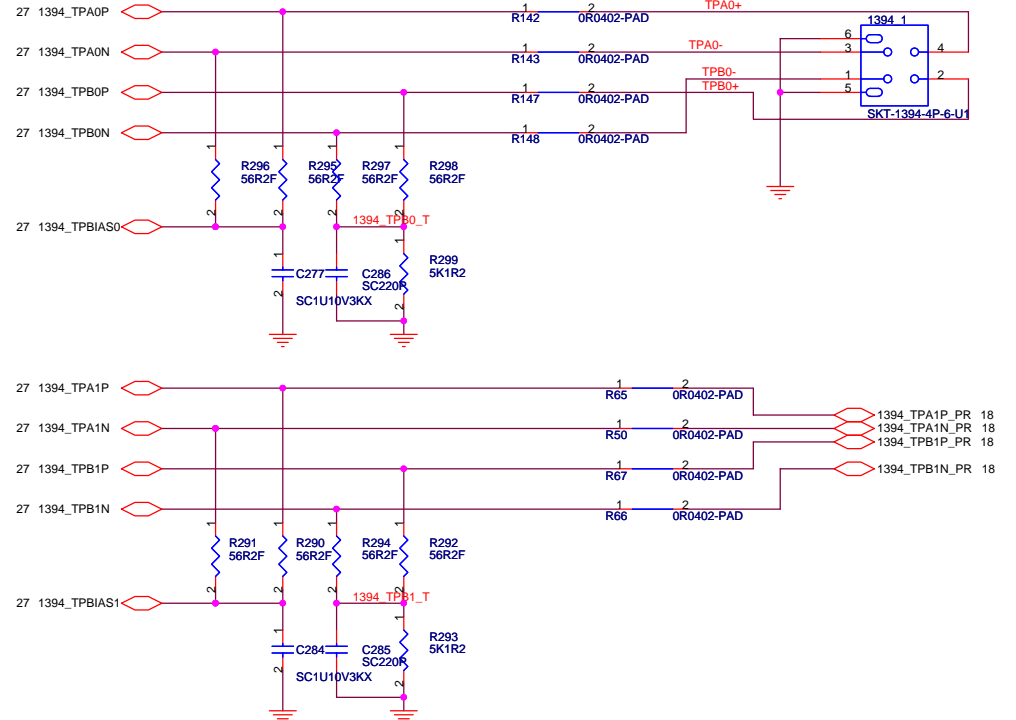
Place on bottom side

From NEW!
1004-1



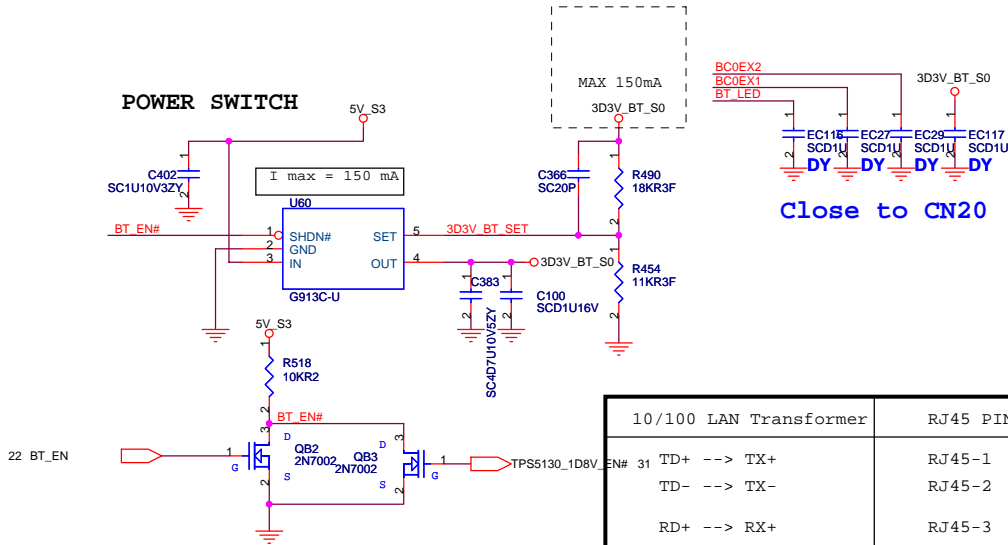
BC0EX2 connect to PCI_AD22 on main board.
BC0EX1 connect to ICH_PMB# on main board.

1394 Connector

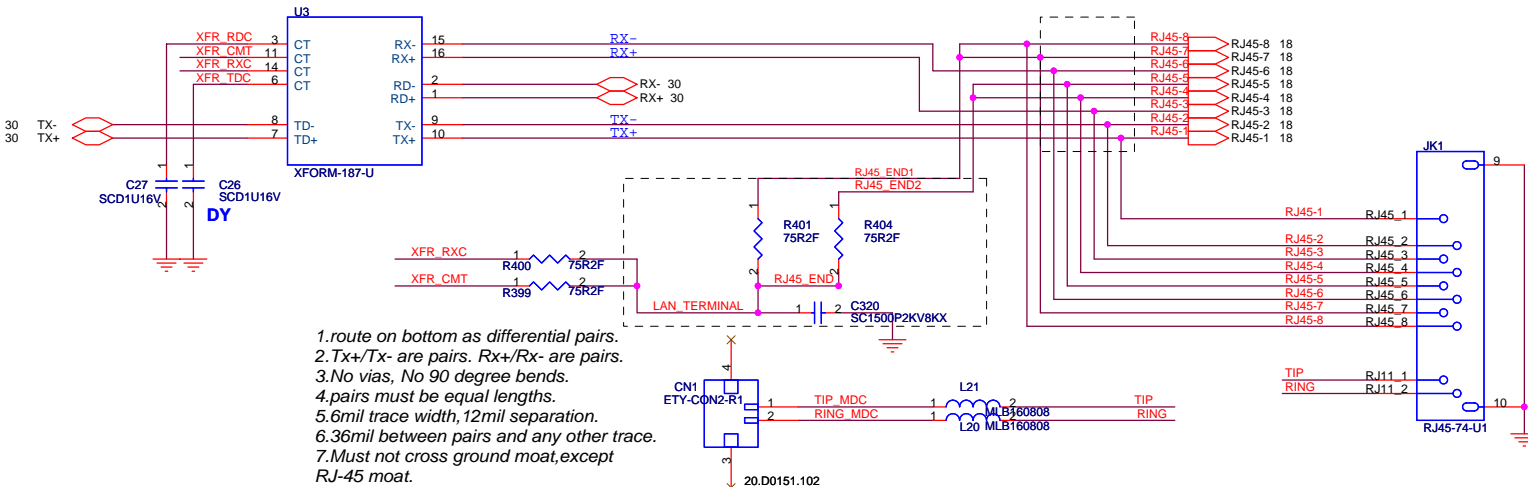


These components near to chip side.

POWER SWITCH



10/100M Lan Transformer



1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

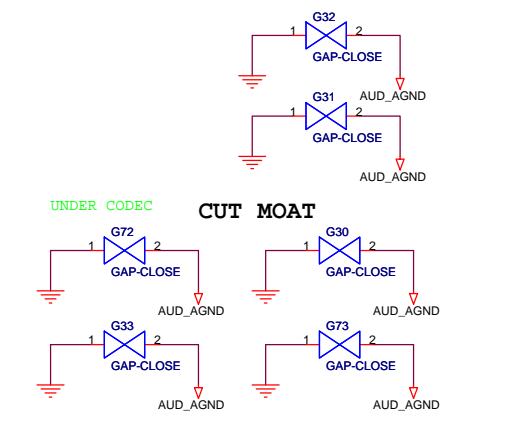
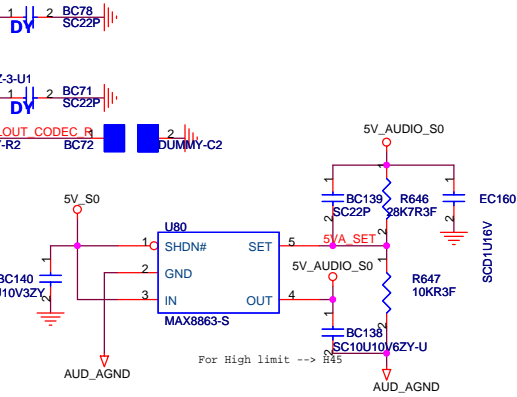
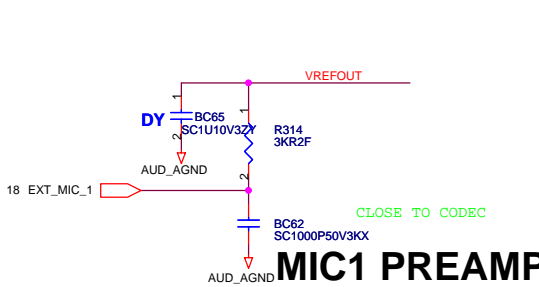
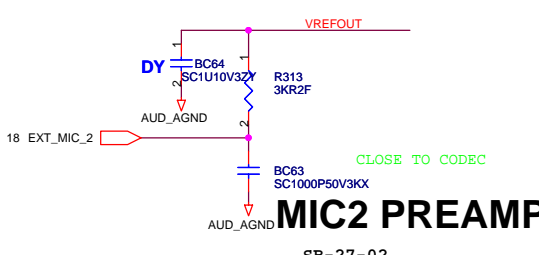
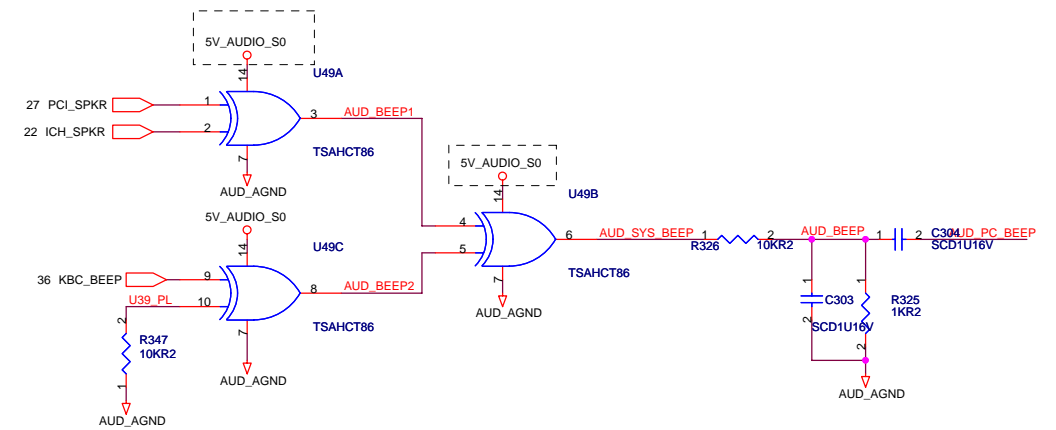
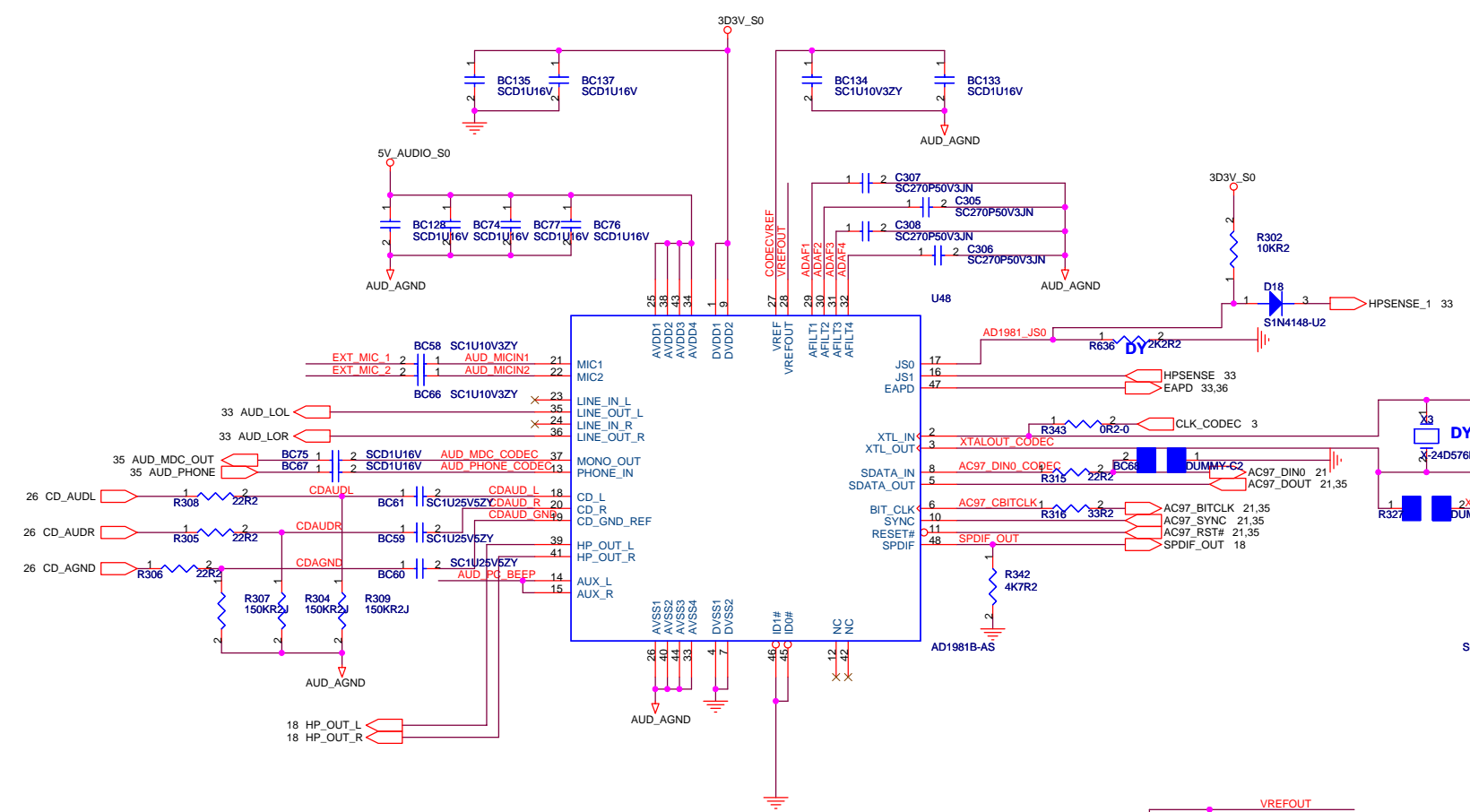
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN / 1394 Connector

Size A3 Document Number Leopard2 Rev -1

Date: Monday, July 11, 2005 Sheet 31 of 47



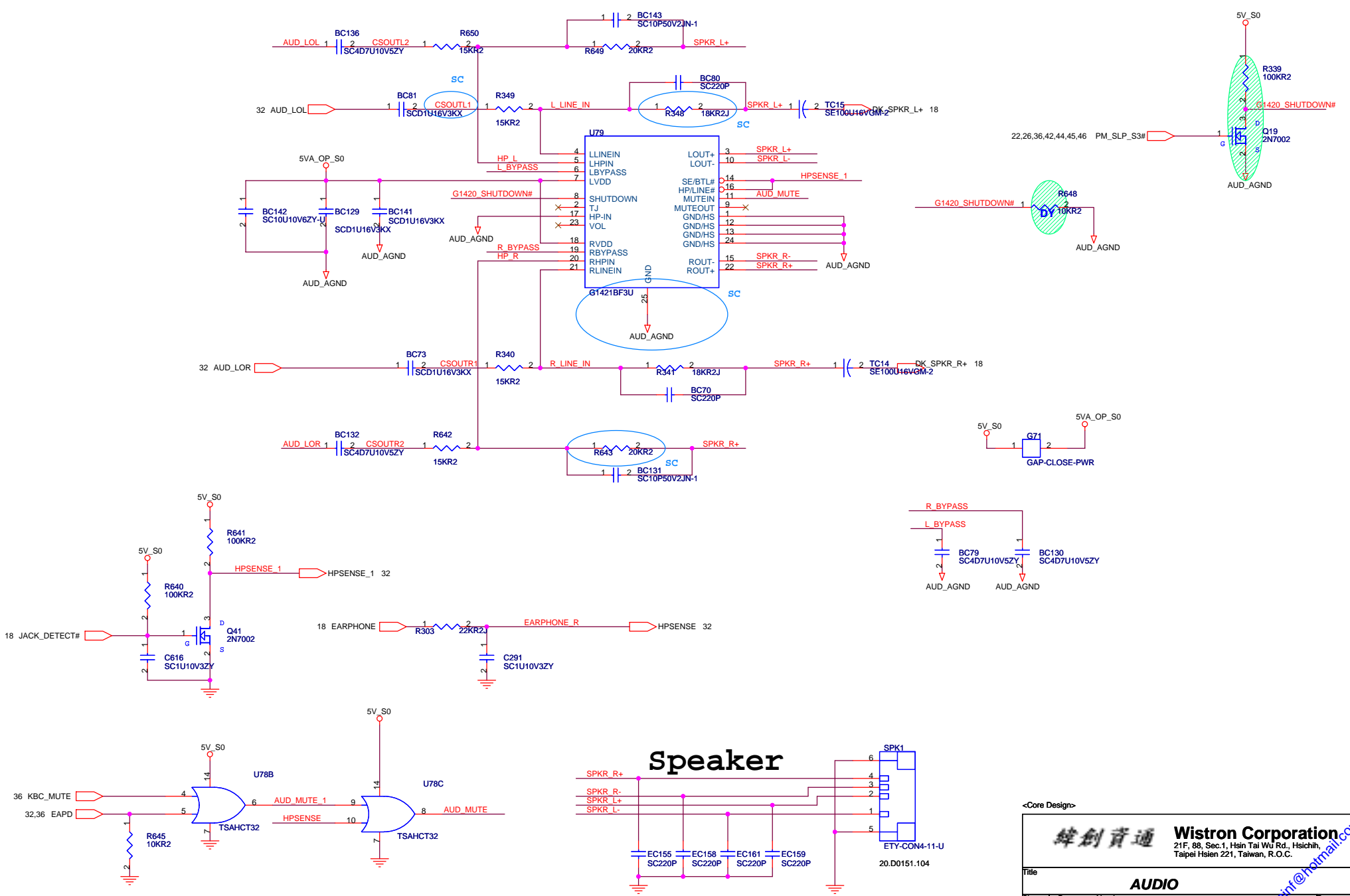
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **AUDIO CODEC AD1981B**

| | | |
|----------|----------------------------------|----------------|
| Size: A3 | Document Number: Leopard2 | Rev: -1 |
|----------|----------------------------------|----------------|

Date: Monday, July 11, 2005 Sheet 32 of 47



<Core Design>

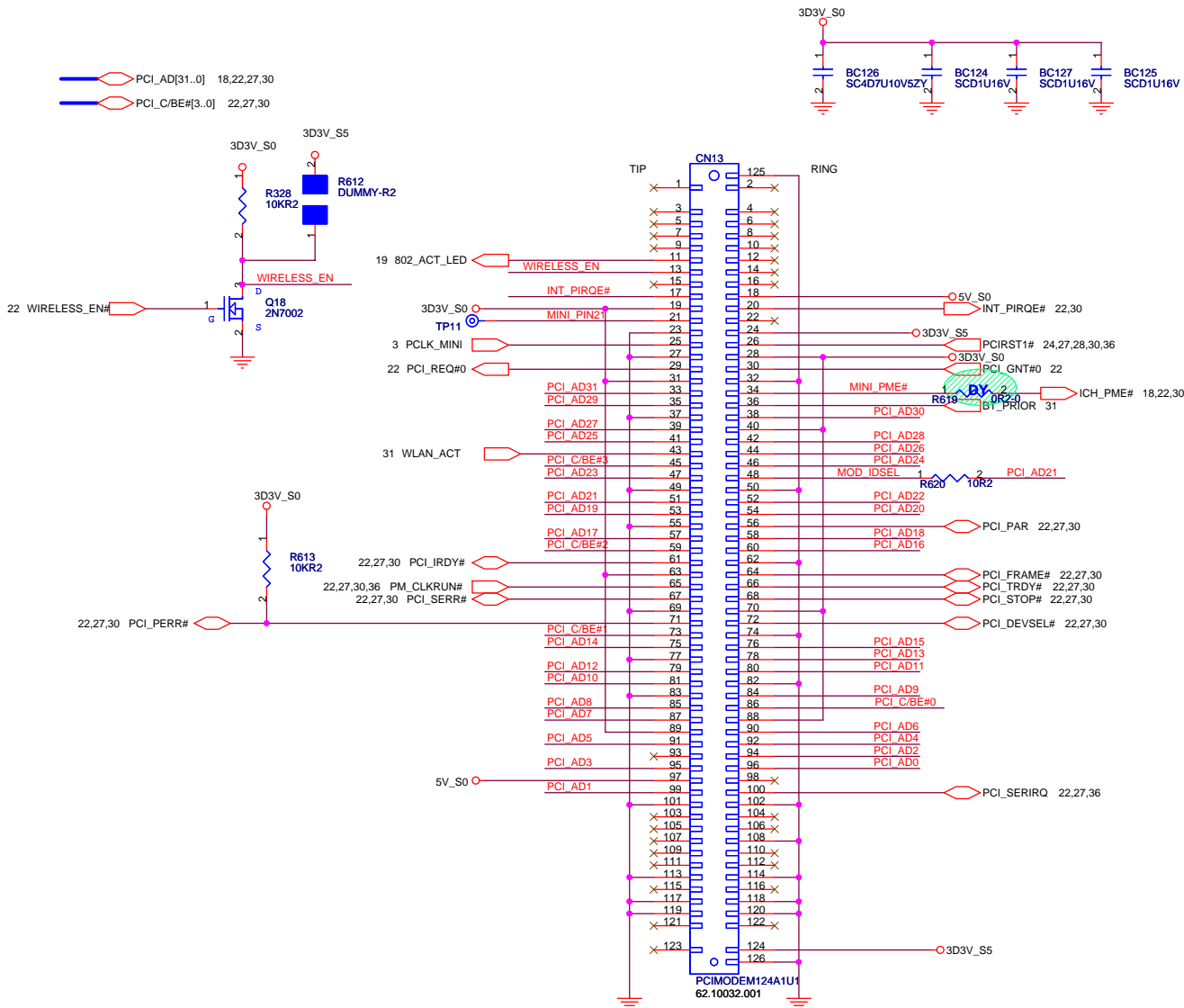
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO**

Size: A3 Document Number: **Leopard2** Rev: **-1**

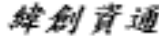
Date: Thursday, July 07, 2005 Sheet: 33 of 47

MINI-PCI

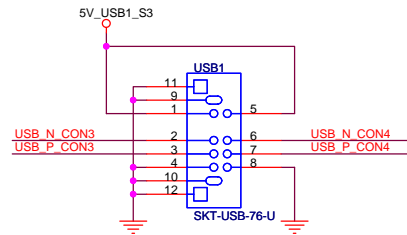
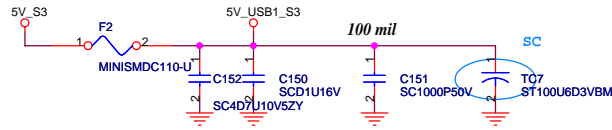


The symbol use 2nd source
 The P/N is the main source
 Main source:62.10032.001
 2nd source:62.10032.031

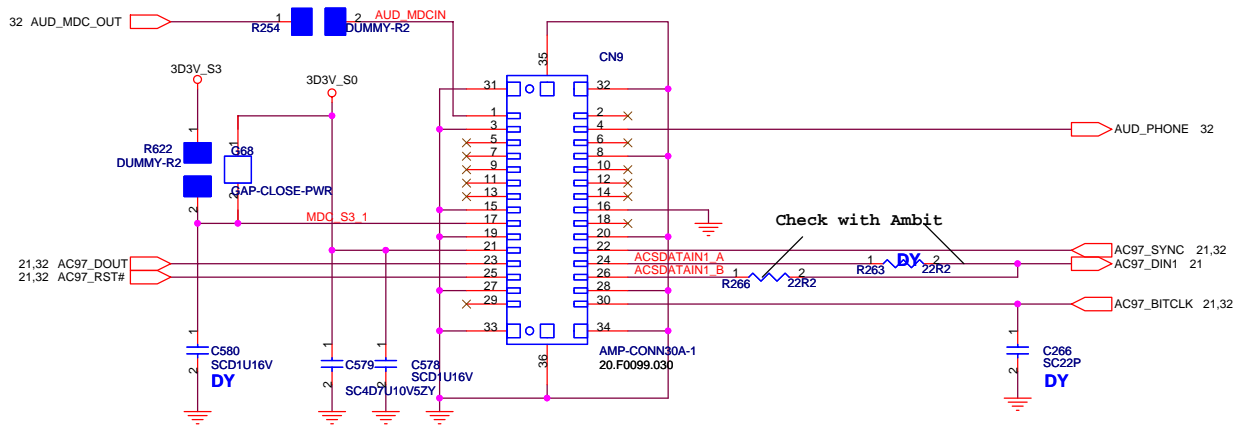
<Core Design>

| | |
|---|------------------------------------|
|  Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| MINI-PCI | |
| Title | |
| Size A3 | Document Number Leopard2 |
| Date: Thursday, July 07, 2005 | Sheet 34 of 47 |
| | Rev -1 |

USB POWER



MDC Connector



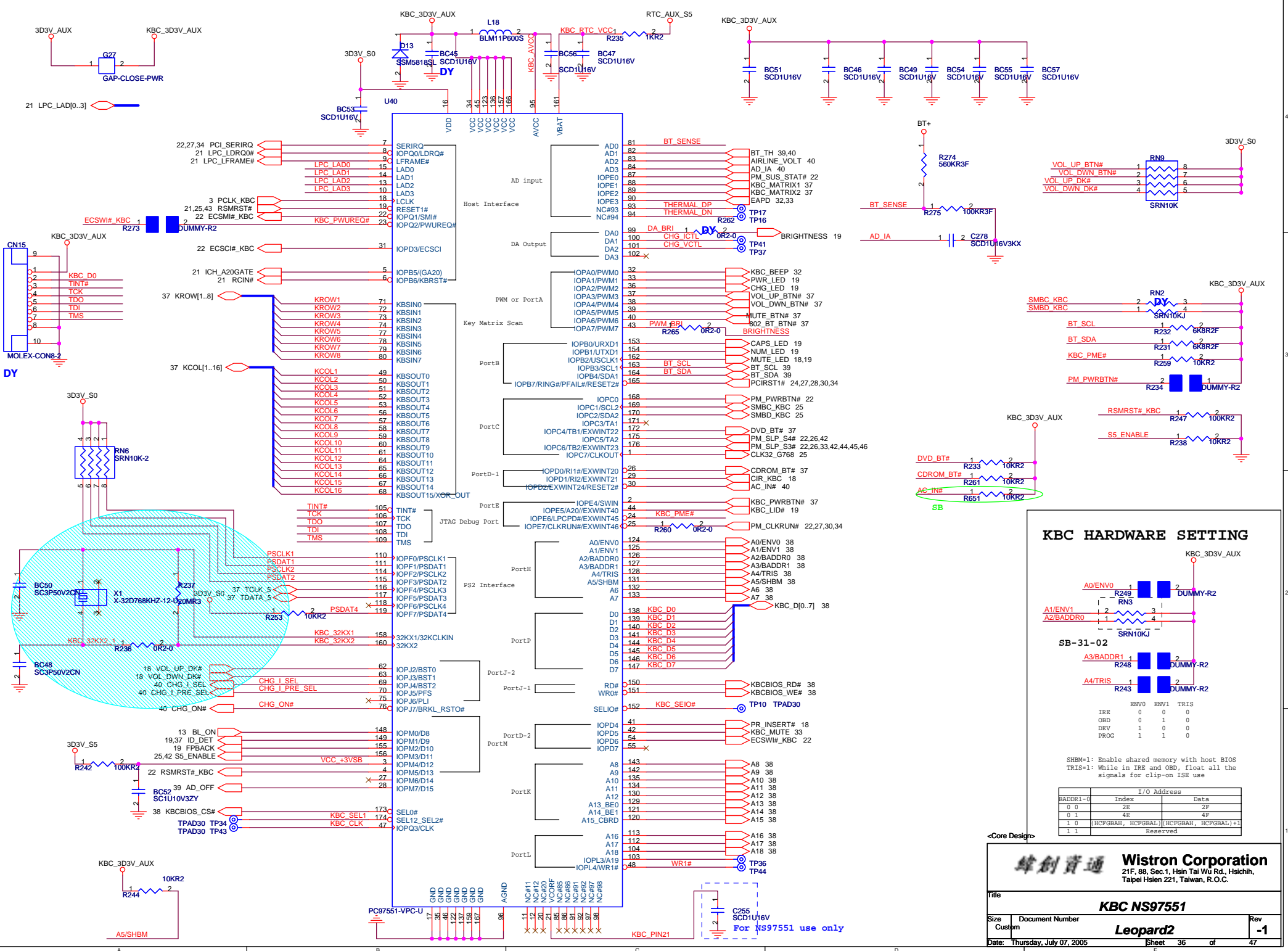
<Core Design>

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB / MDC CONN.**

| | | |
|----------|----------------------------------|----------------|
| Size: A3 | Document Number: Leopard2 | Rev: -1 |
|----------|----------------------------------|----------------|

Date: Thursday, July 07, 2005 Sheet 35 of 47



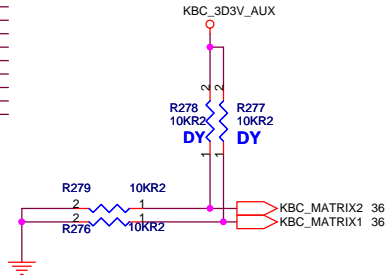
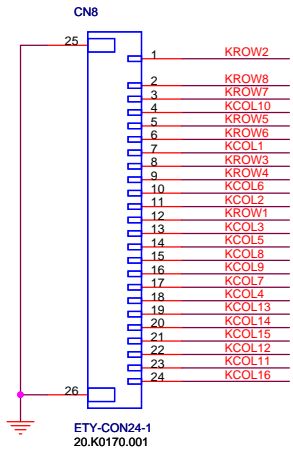
KBC HARDWARE SETTING

SHM=1: Enable shared memory with host BIOS
 TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use

| BADDR1-0 | Index | I/O Address | Data |
|----------|-------|--------------------|----------------------|
| 0 | 0 | 2E | 2F |
| 0 | 1 | 4E | 4F |
| 1 | 0 | {HCFGBAH, HCFGBAL} | {HCFGBAH, HCFGBAL}+1 |
| 1 | 1 | | Reserved |

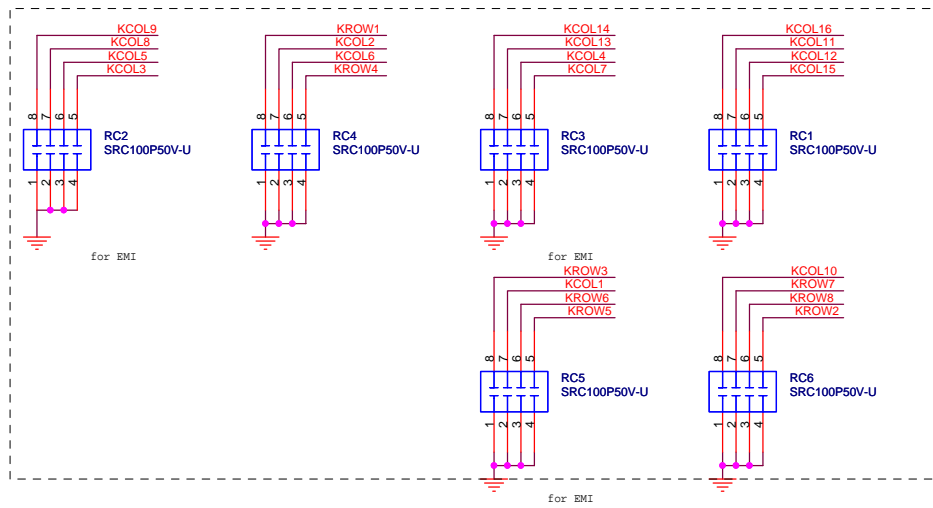
INTERNAL KEYBOARD CONNECTOR

KROW[1..8] 36 KCOL[1..16] 36



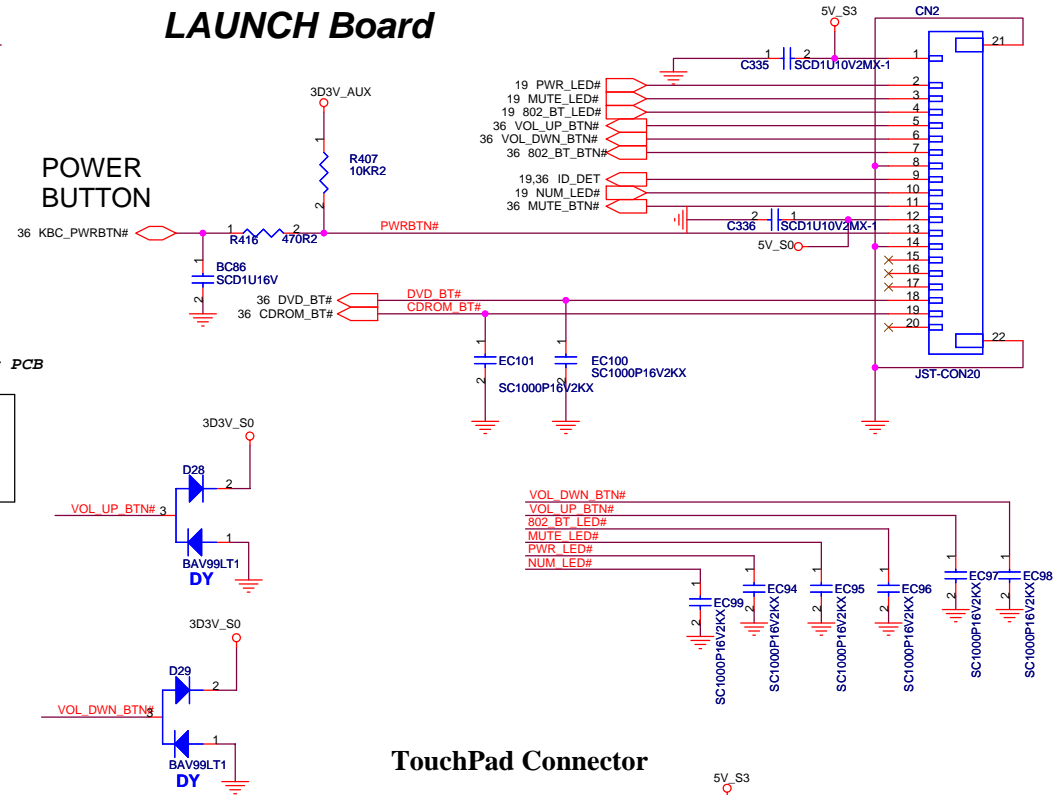
the matrix table for PCB

| | PA | PR |
|----------|----|----|
| Discrete | 00 | 01 |
| UMA | 10 | 11 |

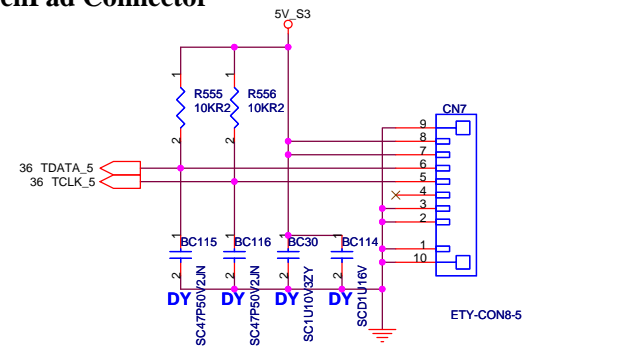


LAUNCH Board

POWER BUTTON



TouchPad Connector



<Core Design>

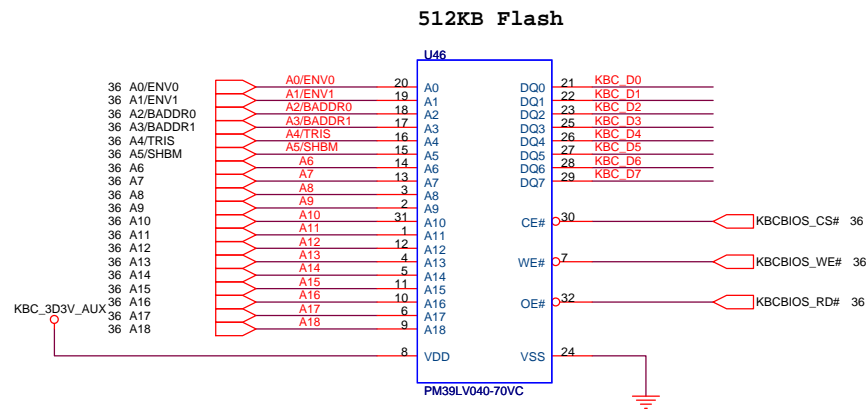
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KEYBOARD/TOUCH PAD/Launch key**

Size: A3 Document Number: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet: 37 of 47

FLASH ROM



KBC_D[0..7] 36

<Core Design>

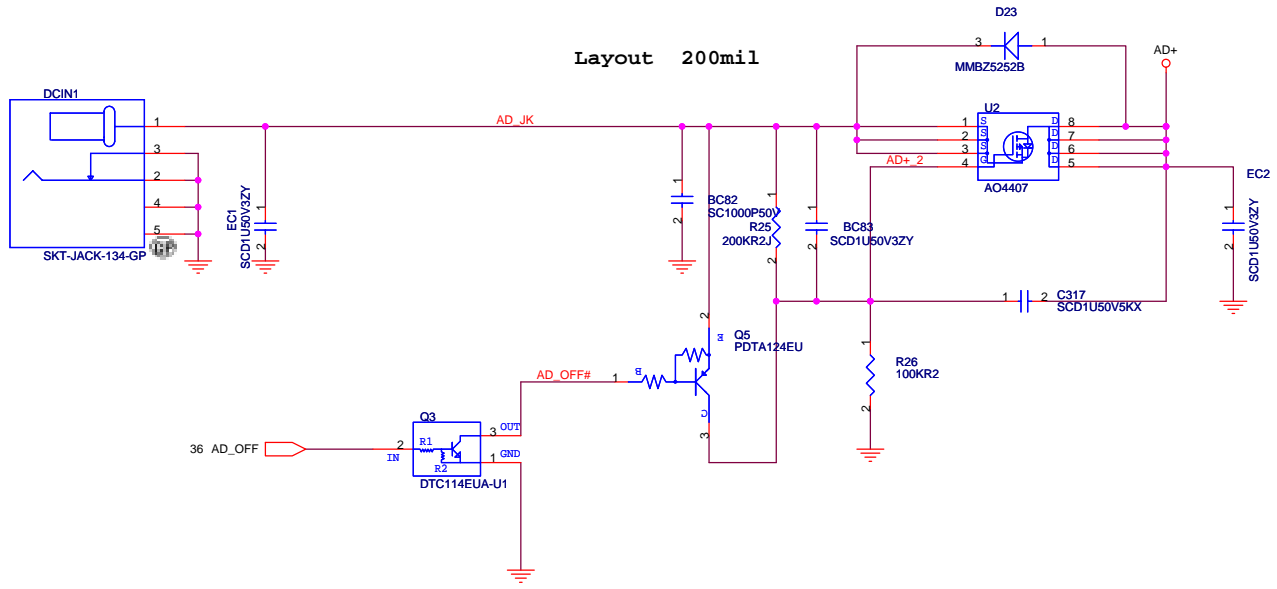
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS/GF**

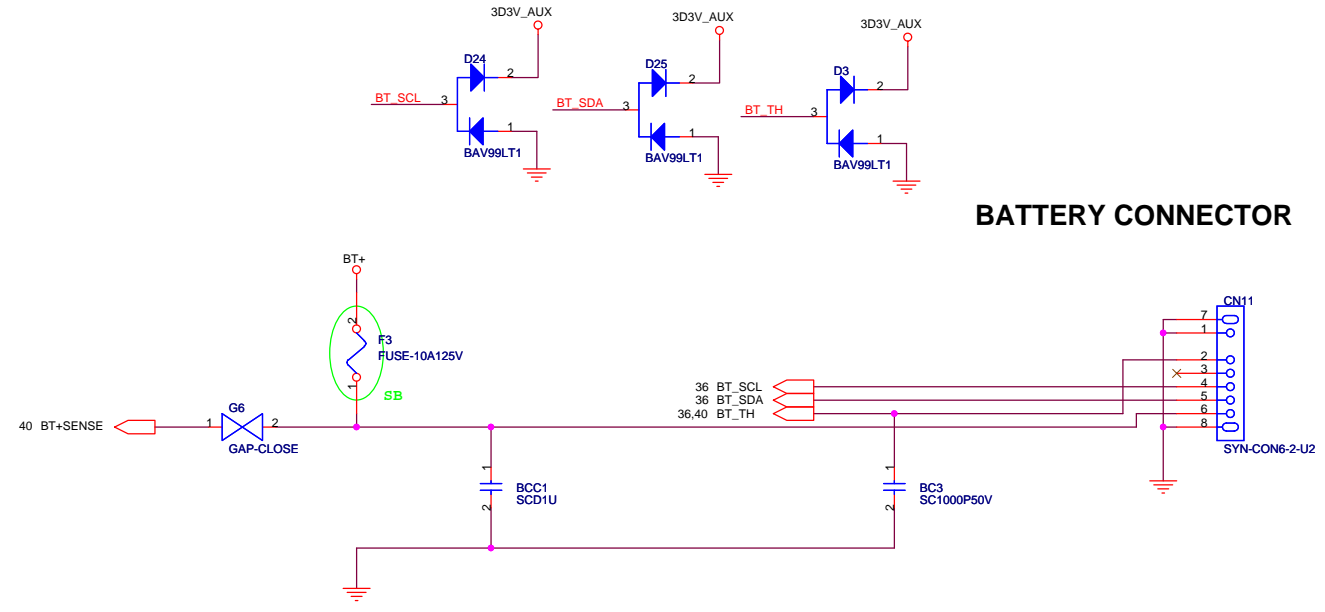
| | | |
|----------|----------------------------------|----------------|
| Size: A3 | Document Number: Leopard2 | Rev: -1 |
|----------|----------------------------------|----------------|

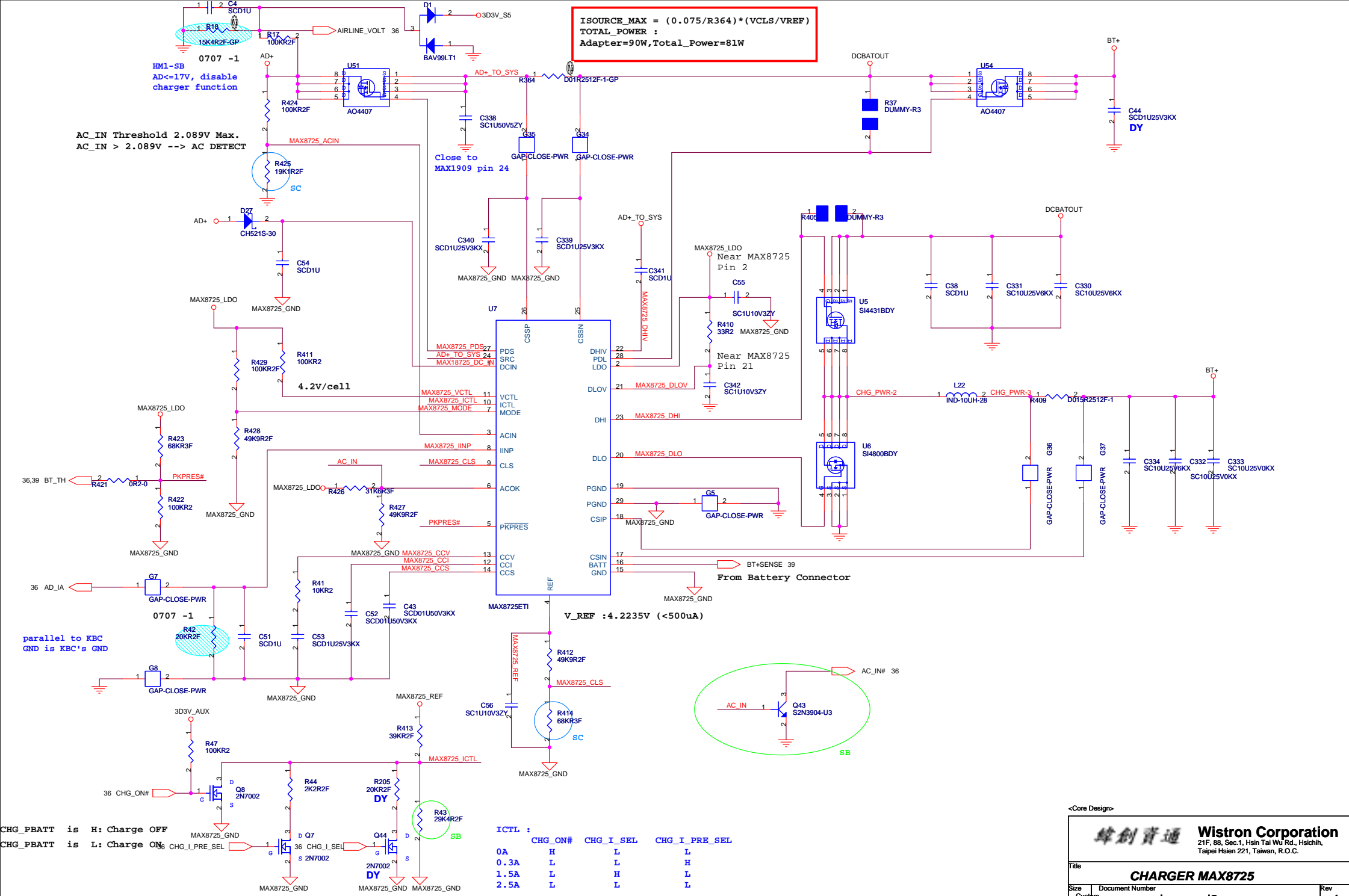
Date: Thursday, July 07, 2005 Sheet 38 of 47

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR





AC_IN Threshold 2.089V Max.
 AC_IN > 2.089V --> AC DETECT

parallel to KBC
 GND is KBC's GND

CHG_PBATT is H: Charge OFF
 CHG_PBATT is L: Charge ON

If Charger is MAX1909, dummy them.

<Core Design>

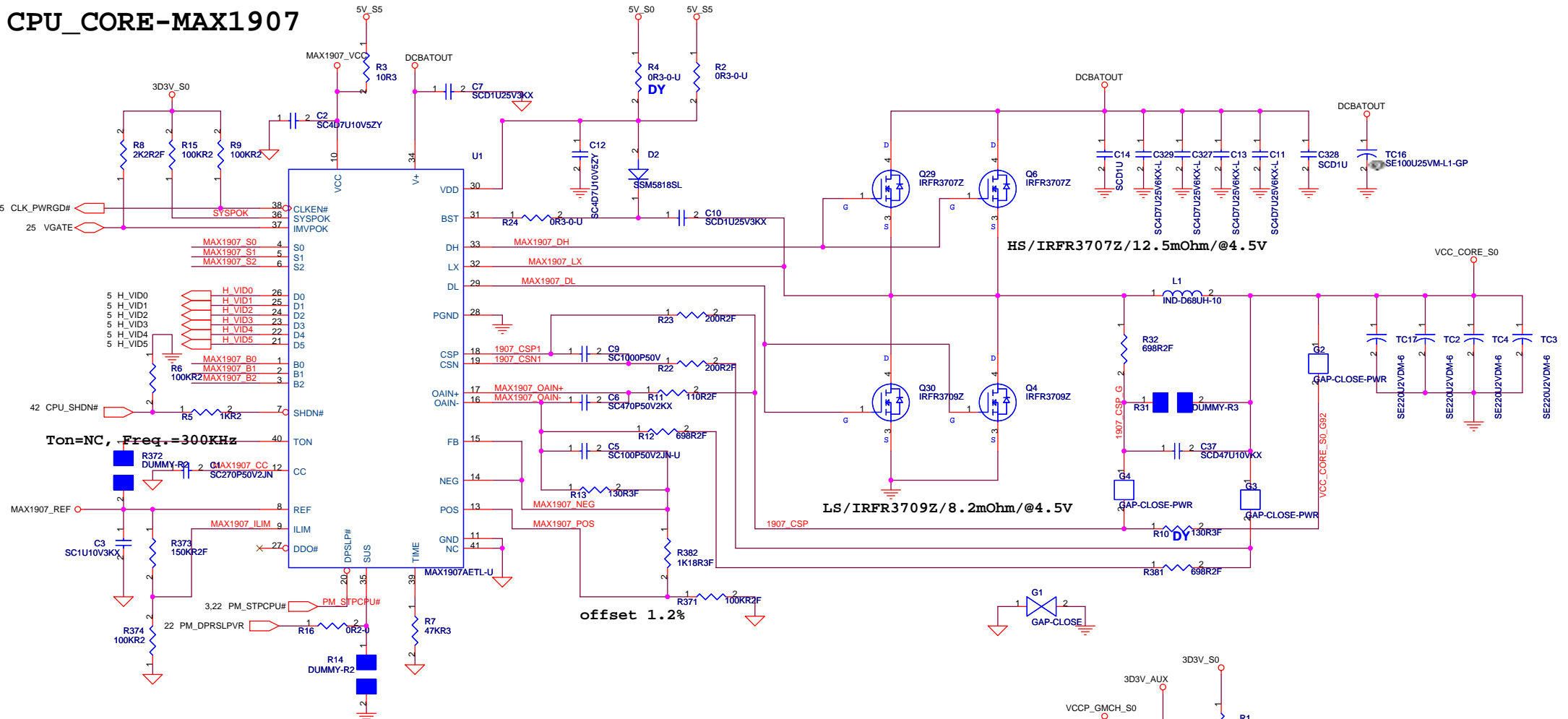
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER MAX8725**

Size: Document Number
 Custom: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet 40 of 47

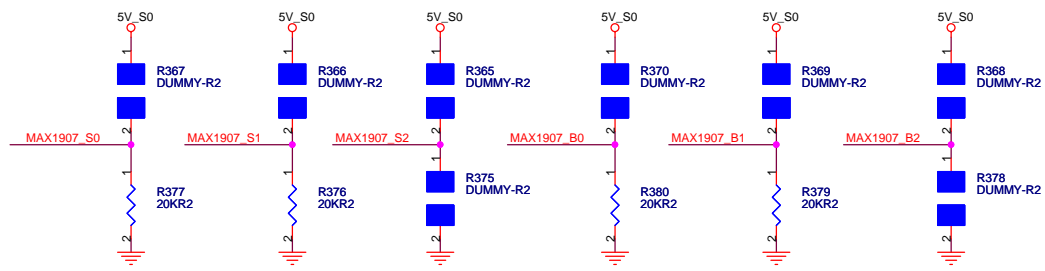
CPU_CORE-MAX1907



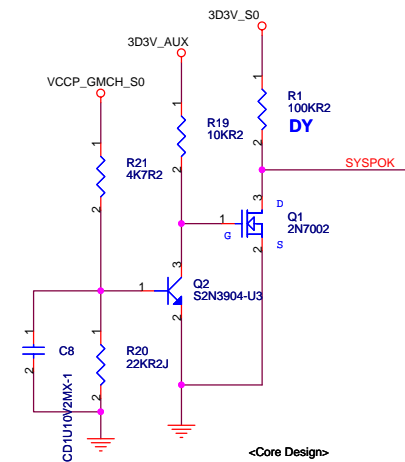
OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.748V
, S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



| VID | | | | | | Vcore |
|------|------|------|------|------|------|-------|
| VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | v |
| 0 | 1 | 0 | 1 | 1 | 1 | 1.340 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1.324 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1.292 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1.260 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1.244 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1.212 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1.180 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1.148 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1.100 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1.052 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1.020 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0.972 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0.940 |



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

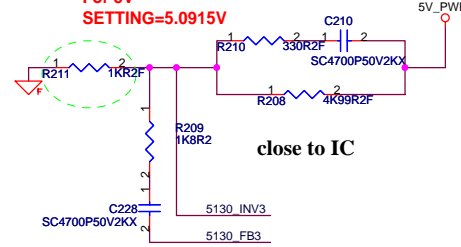
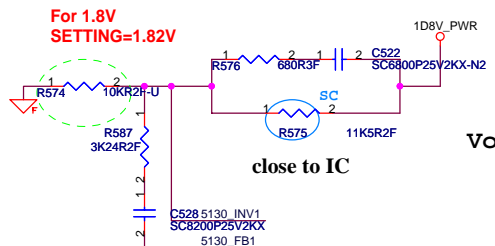
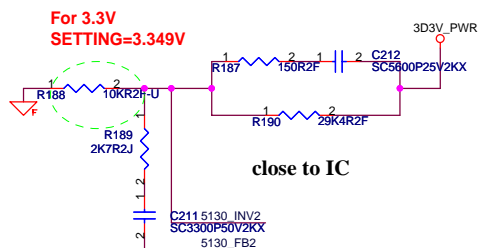
Title: **IMVP IV-CPU POWER-MAX1907**

Size: A3 Document Number: **Leopard2** Rev: **-1**

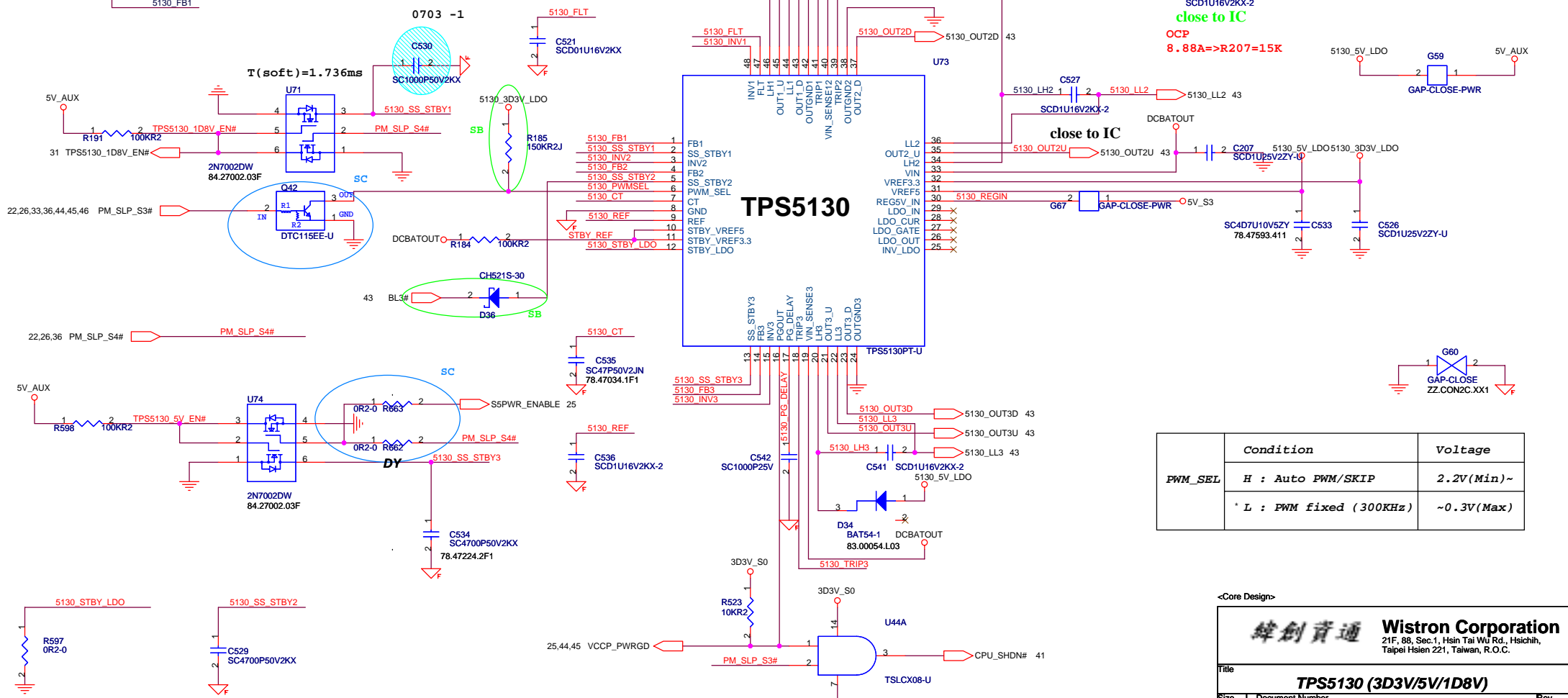
Date: Monday, July 11, 2005 Sheet 41 of 47

TI TPS5130 for 1D8V, 3D3V, 5V

(1D8V=>CH1 , 3D3V=>CH2 , 5V =>CH3)



$$V_o = (R1 * 0.85) / R2 + 0.85$$



| | Condition | Voltage |
|---------|------------------------|-------------|
| PWM_SEL | H : Auto PWM/SKIP | 2.2V (Min)~ |
| | L : PWM fixed (300KHz) | ~0.3V (Max) |

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS5130 (3D3V/5V/1D8V)**

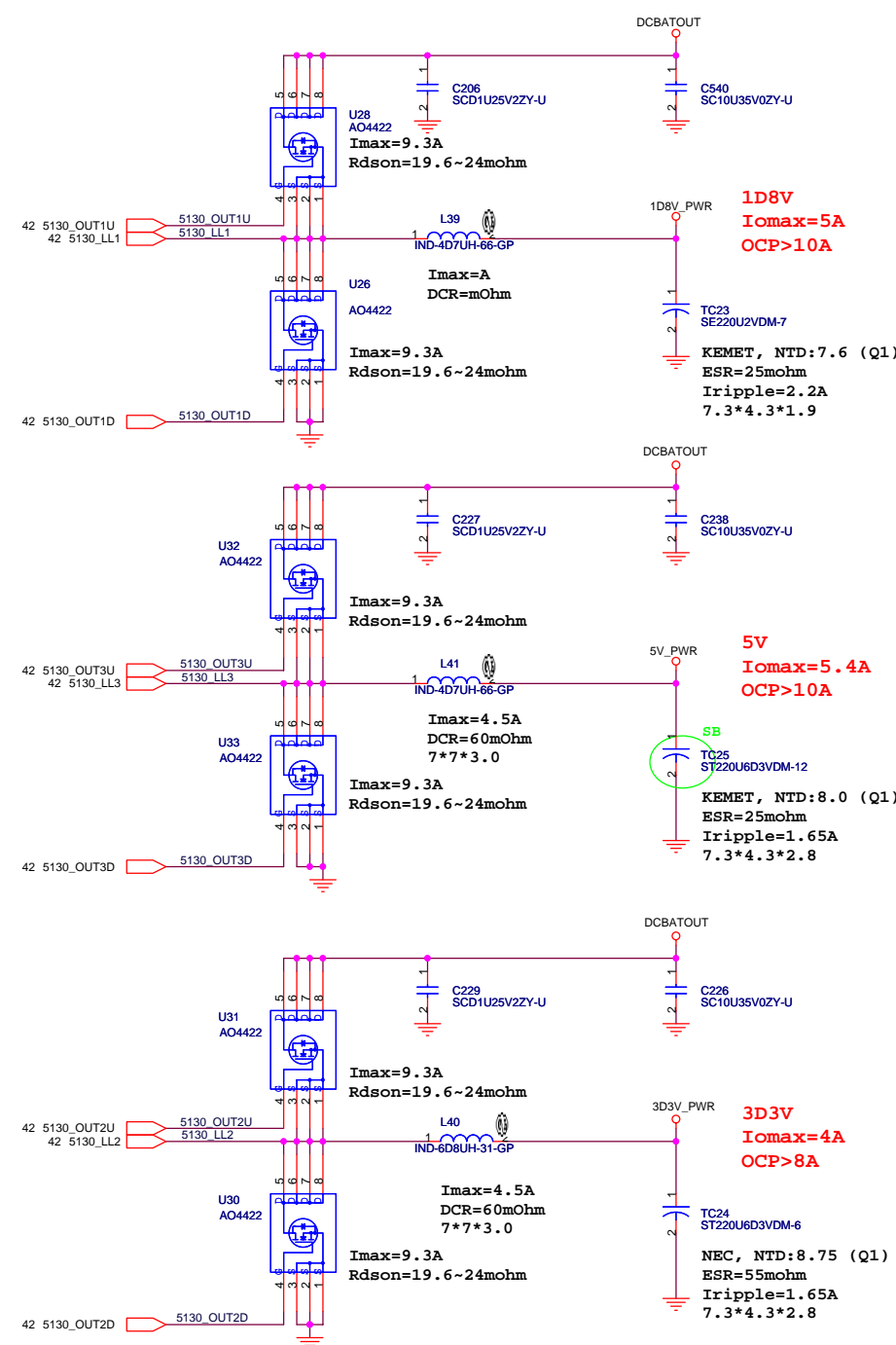
Size: A3 Document Number: **Leopard2** Rev: -1

Date: Thursday, July 07, 2005 Sheet: 42 of 47

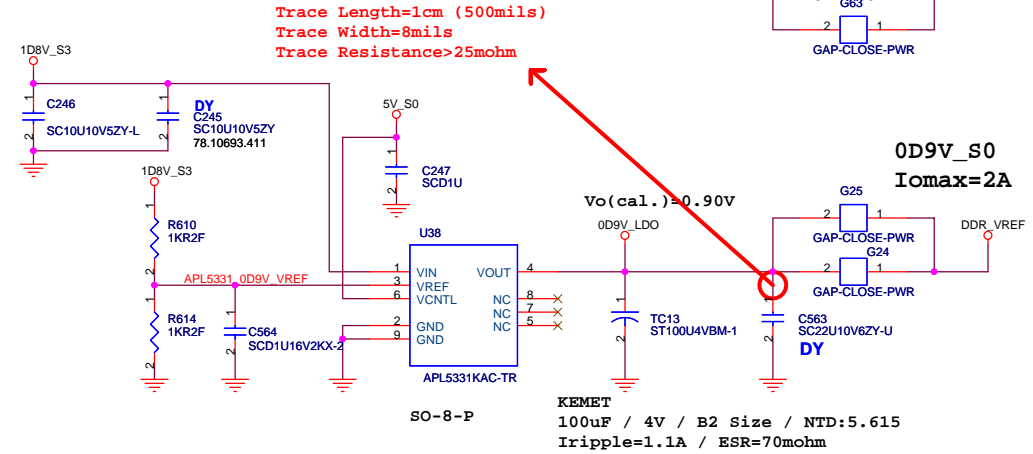
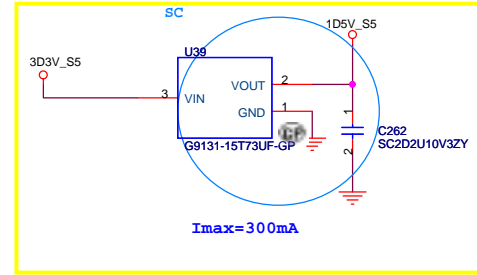
HW Thermal Throttling

TI TPS5130 for 1D2V, 5V, 3D3V

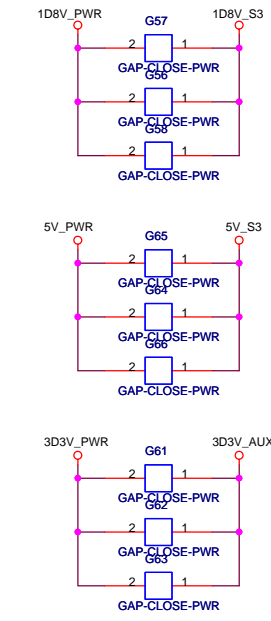
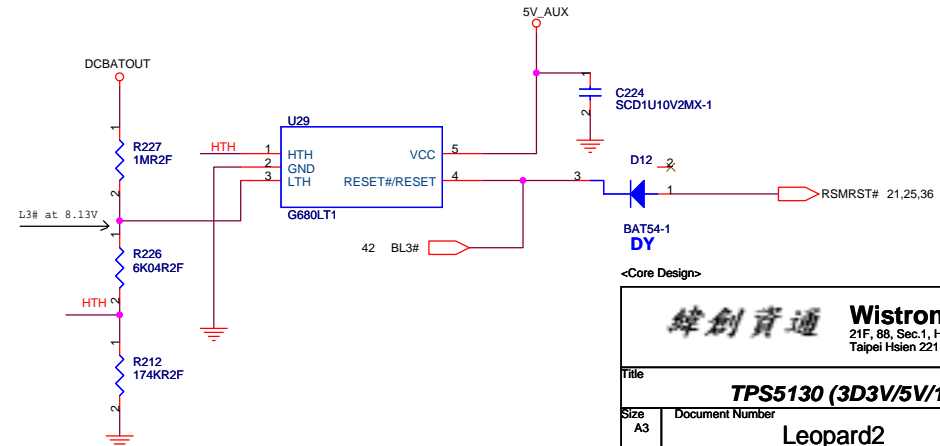
(1D2V=>CH1 , 5V=>CH2 , 3D3V =>CH3)



1.5V_S5 (For ICH6)



L3# circuit



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

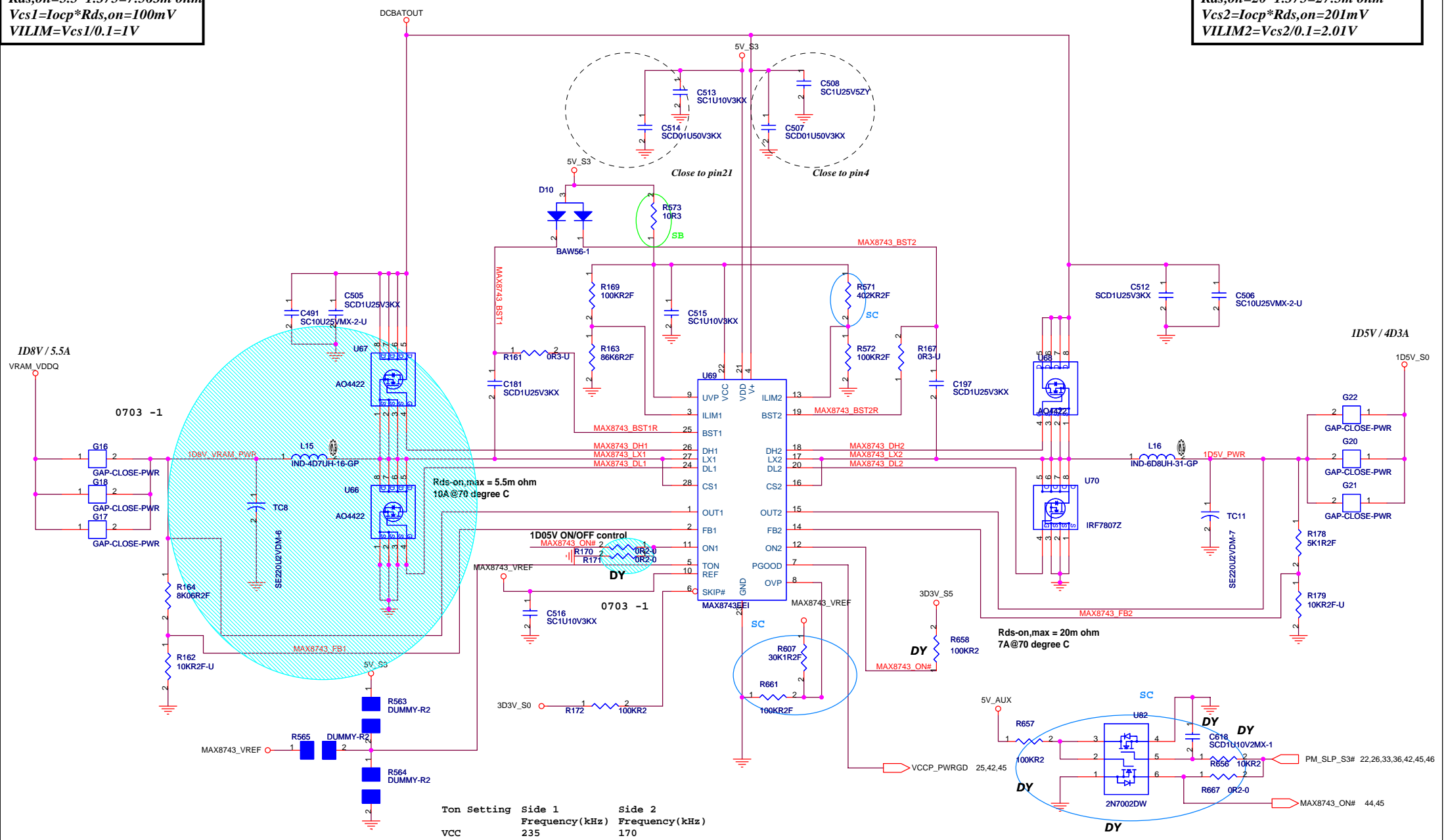
Title: **TPS5130 (3D3V/5V/1D8V/0D9V)**

Size A3 Document Number **Leopard2** Rev -1

Date: Monday, July 11, 2005 Sheet 43 of 47

$I_{ocp} = 7.8 * 1.7 = 13.3A$
 $R_{ds,on} = 5.5 * 1.375 = 7.563m\ \Omega$
 $V_{cs1} = I_{ocp} * R_{ds,on} = 100mV$
 $V_{ILIM} = V_{cs1} / 0.1 = 1V$

$I_{ocp} = 4.3 * 1.7 = 7.3A$
 $R_{ds,on} = 20 * 1.375 = 27.5m\ \Omega$
 $V_{cs2} = I_{ocp} * R_{ds,on} = 201mV$
 $V_{ILIM2} = V_{cs2} / 0.1 = 2.01V$



| Ton Setting | Side 1 | Side 2 |
|-----------------|--------|--------|
| Frequency (kHz) | 235 | 170 |
| VCC | 345 | 255 |
| Float | 485 | 355 |
| VREF | 620 | 460 |
| AGND | | |

<Core Design>

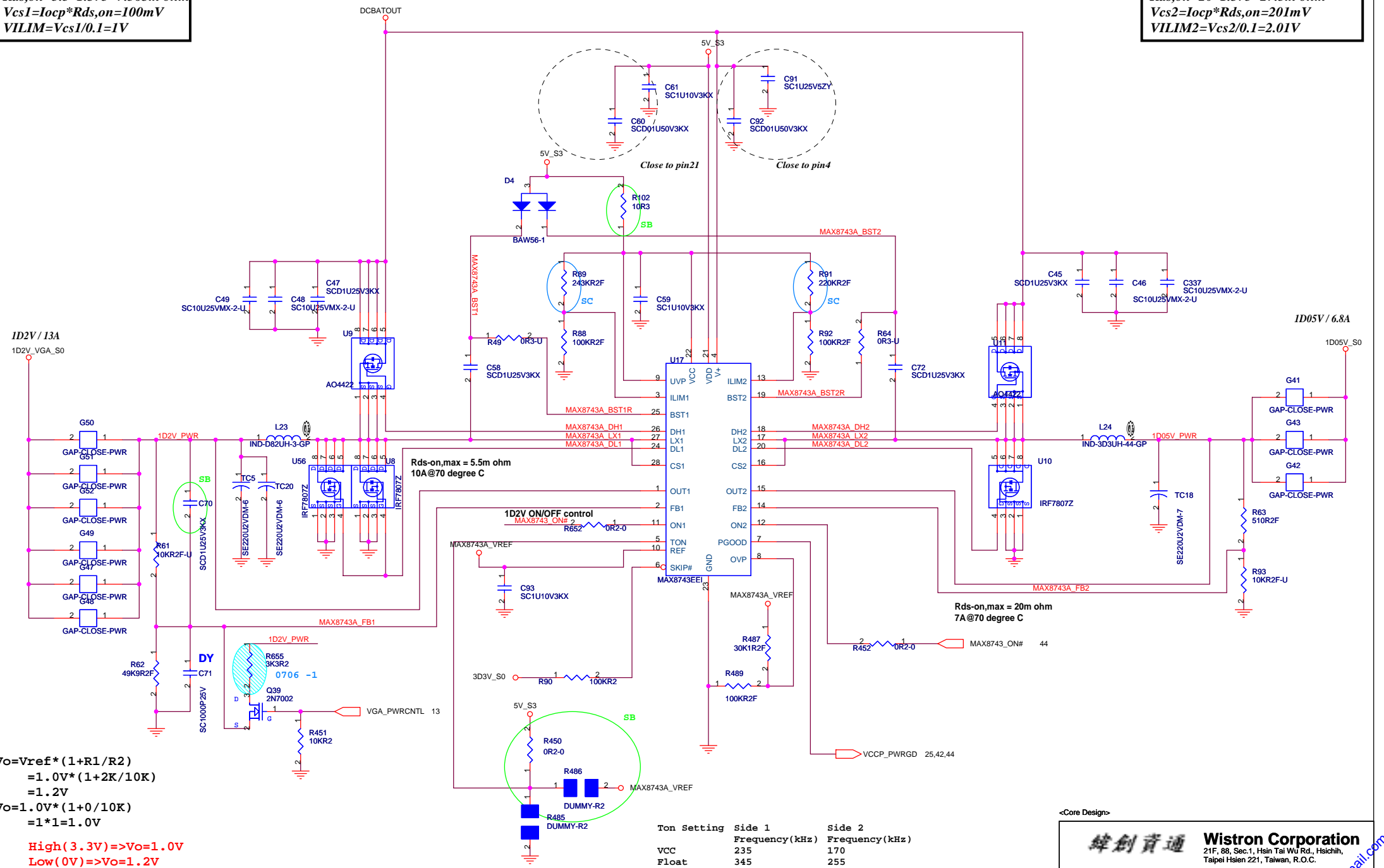
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

MAX8743 (1D8V_S0/1D5V_S0)

| | | |
|-----------------------------|-----------------|-----|
| File | Document Number | Rev |
| Size A3 | Leopard2 | -1 |
| Date: Monday, July 11, 2005 | Sheet 44 of | 47 |

$I_{ocp} = 7.8 * 1.7 = 13.3A$
 $R_{ds,on} = 5.5 * 1.375 = 7.563m\ ohm$
 $V_{cs1} = I_{ocp} * R_{ds,on} = 100mV$
 $V_{ILIM} = V_{cs1} / 0.1 = 1V$

$I_{ocp} = 4.3 * 1.7 = 7.3A$
 $R_{ds,on} = 20 * 1.375 = 27.5m\ ohm$
 $V_{cs2} = I_{ocp} * R_{ds,on} = 201mV$
 $V_{ILIM2} = V_{cs2} / 0.1 = 2.01V$



$V_o = V_{ref} * (1 + R1/R2)$
 $= 1.0V * (1 + 2K/10K)$
 $= 1.2V$
 $V_o = 1.0V * (1 + 0/10K)$
 $= 1 * 1 = 1.0V$

High (3.3V) => $V_o = 1.0V$
Low (0V) => $V_o = 1.2V$

M24/M26 POWER PLAY (VGA_PWRCNTL)
 high (3.3V) = set lower core voltage (VDDC = 1.0V)
 low (0V) = set higher core voltage (VDDC = 1.2V)

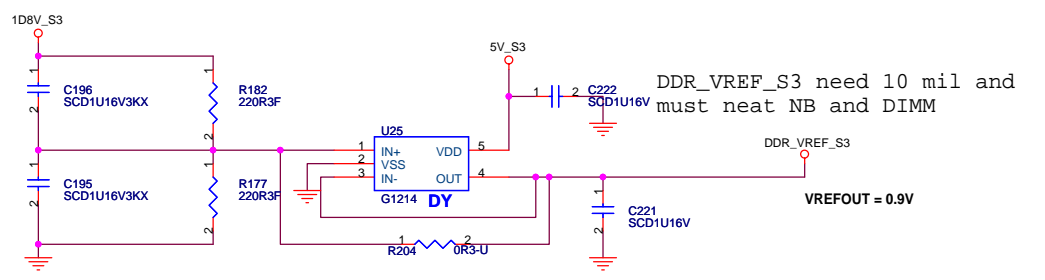
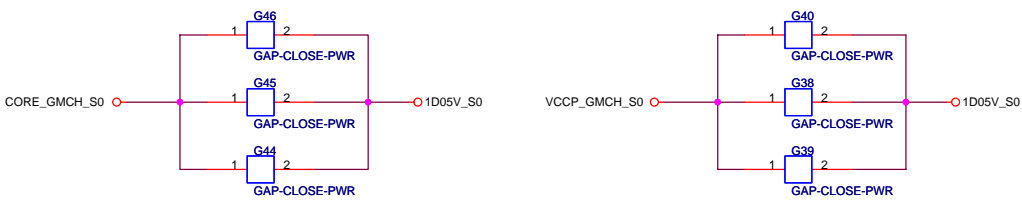
| Ton Setting | Side 1 Frequency (kHz) | Side 2 Frequency (kHz) |
|-------------|---------------------------|---------------------------|
| VCC | 235 | 170 |
| Float | 345 | 255 |
| VREF | 485 | 355 |
| AGND | 620 | 460 |

<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

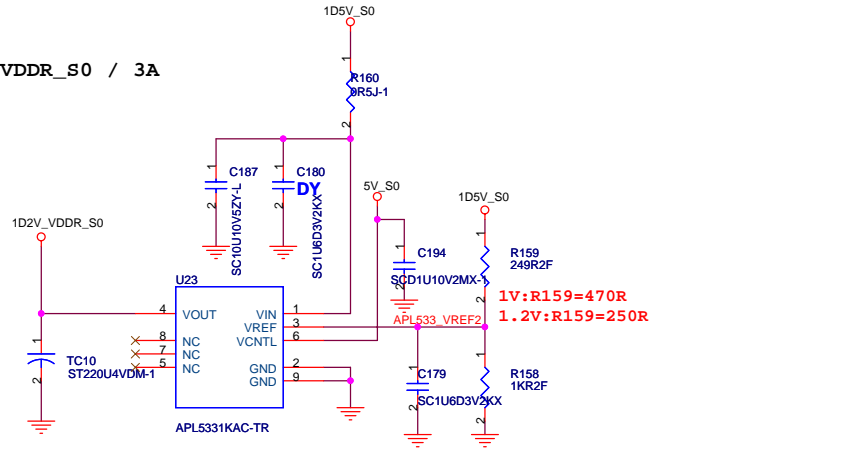
Title: **MAX8743 (1D2V_VGA_S0/1D05V)**
 Size A3 Document Number: **Leopard2** Rev: **-1**
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FOR GMCH Power

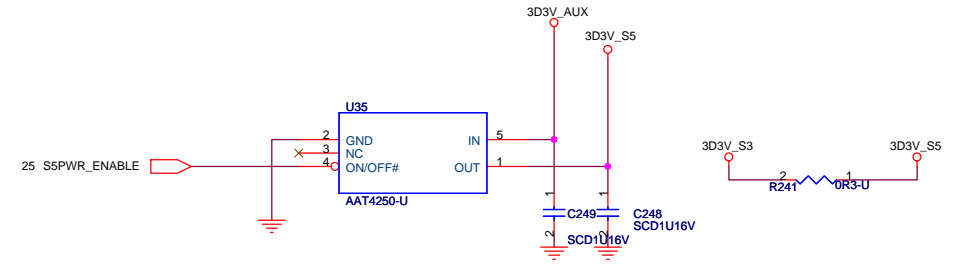


FOR DDR2 Power

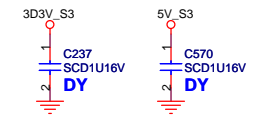
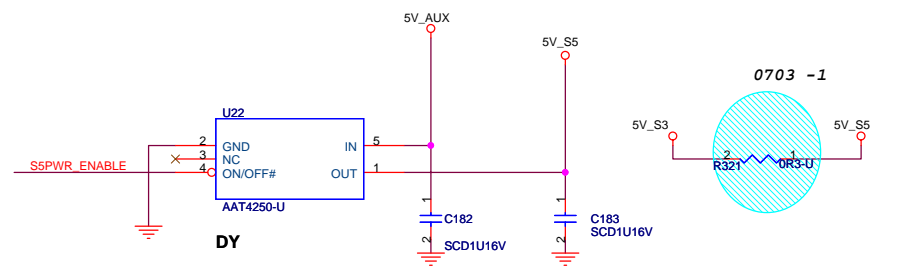
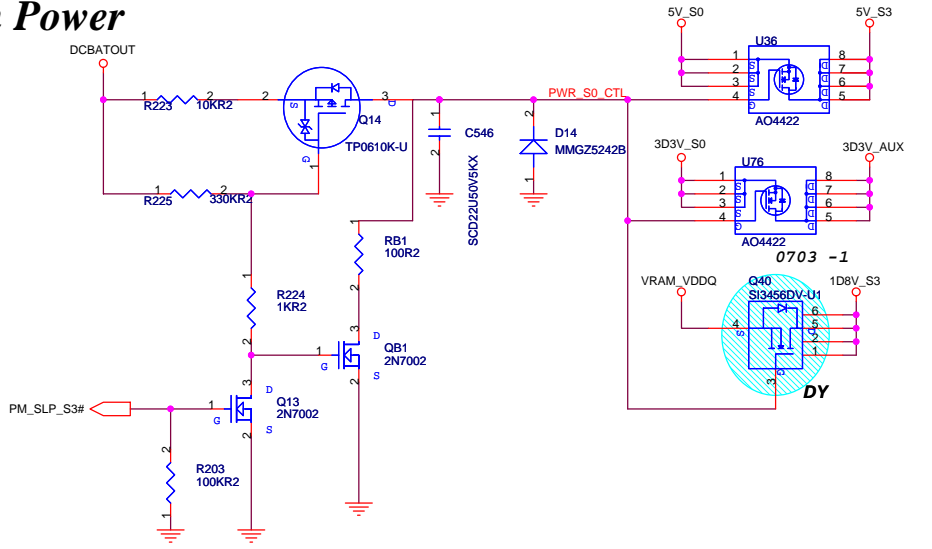
1D2V_VDDR_S0 / 3A



Suspend Power



Run Power



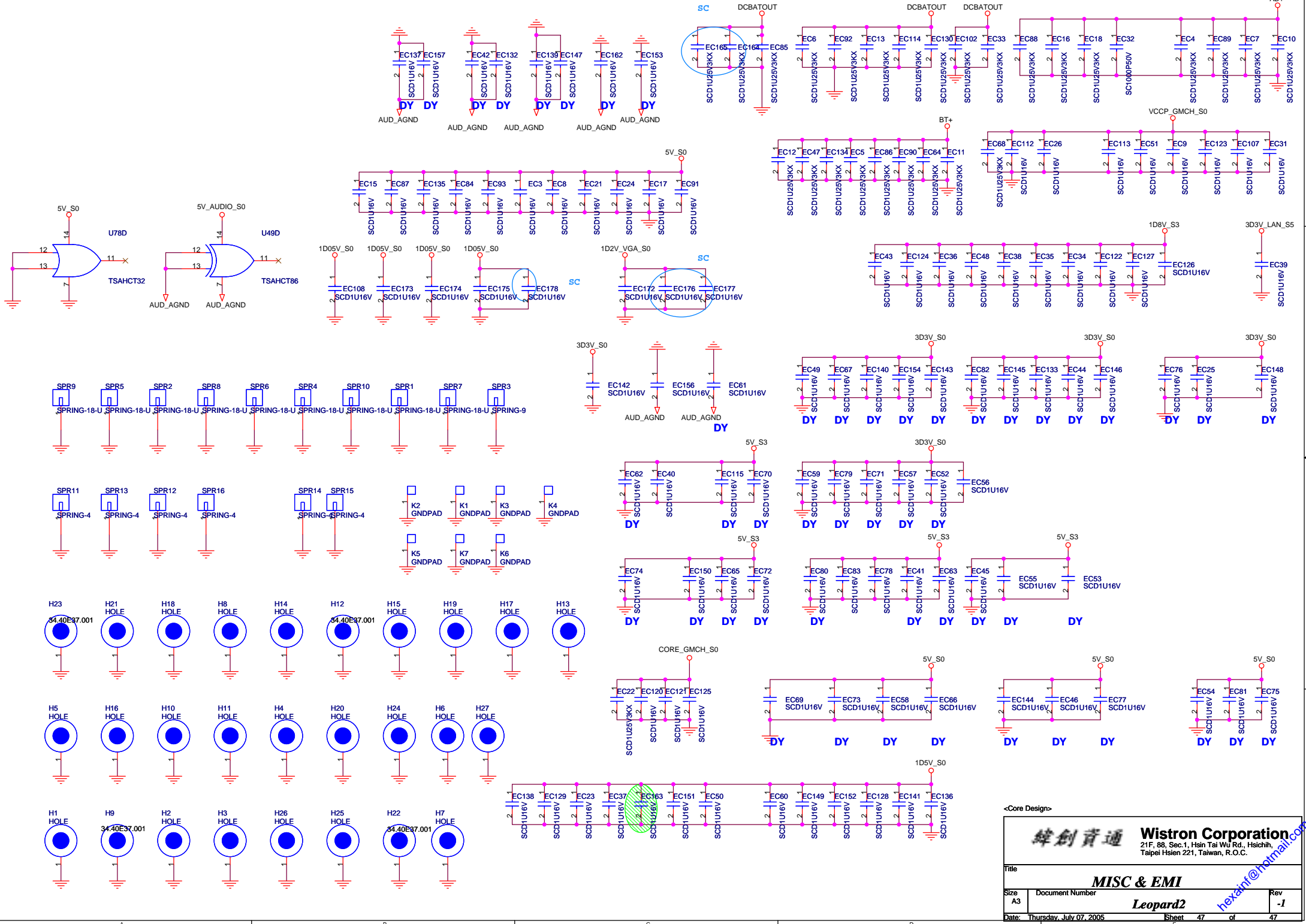
<Core Design>

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Title: **PWRPLANE&RESETLOGIC**

Size A3 Document Number: **Leopard2** Rev: **-1**

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<Core Design>

| | | | | | |
|-------------------------------|-----------------|--|--|--|--------|
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| MISC & EMI | | | | | |
| Title | | | | | |
| Size | Document Number | | | | |
| Leopard2 | | | Sheet 47 of 47 | | Rev -1 |
| Date: Thursday, July 07, 2005 | | | | | |