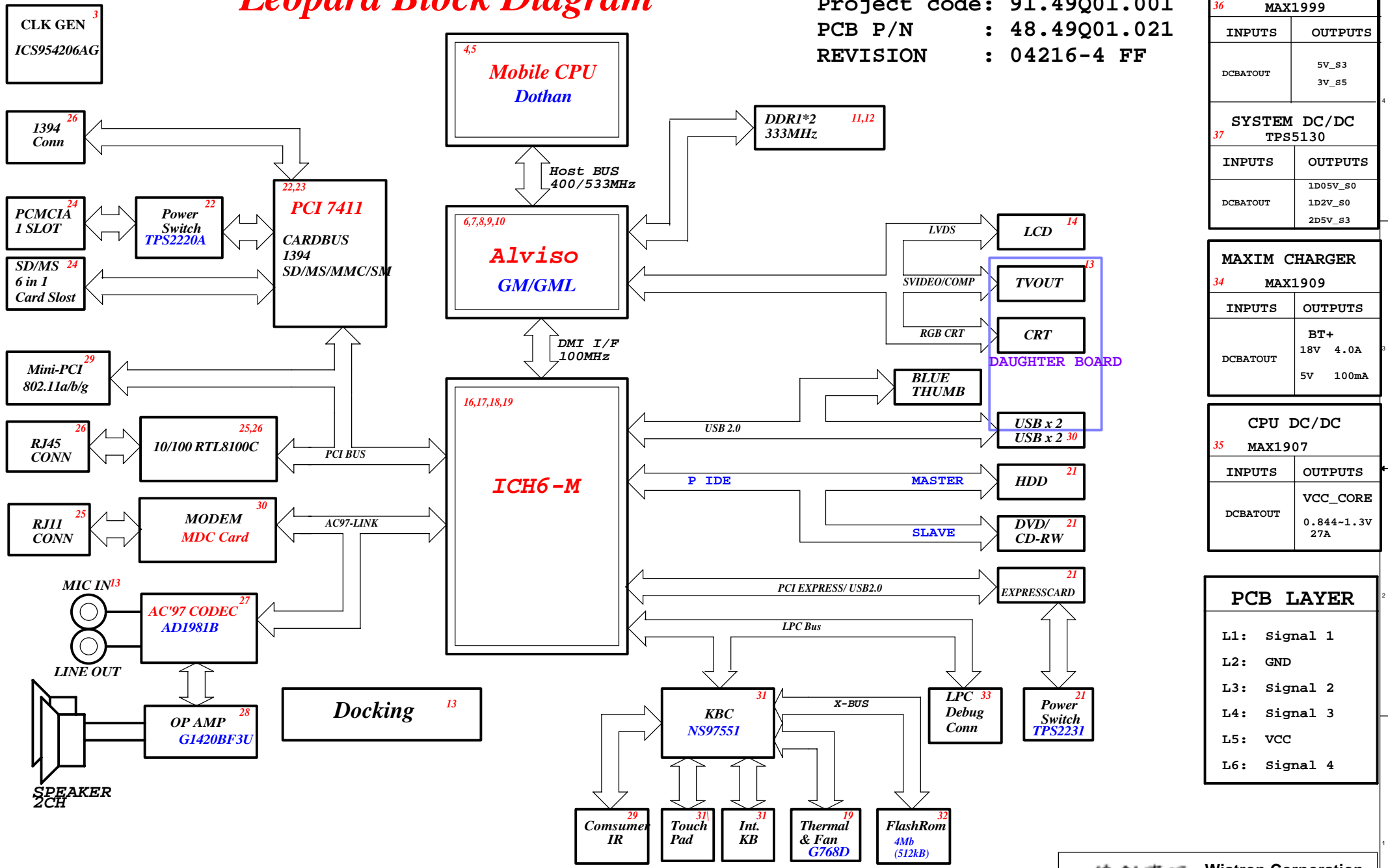


Leopard Block Diagram

Project code: 91.49Q01.001
 PCB P/N : 48.49Q01.021
 REVISION : 04216-4 FF



SYSTEM DC/DC MAX1999	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 2D5V_S3

MAXIM CHARGER MAX1909	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size: A3 Document Number: **Leopard** Rev: -4

Date: Sunday, February 27, 2005 Sheet 1 of 41

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]/GPO[17], GNT[6]/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

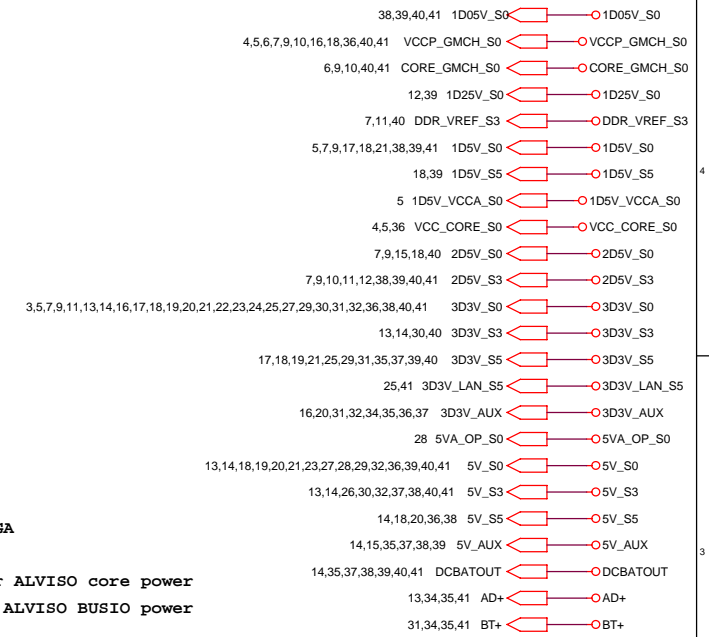
ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
 5V_S3= 5 Voltage suspend to RAM(S3 state)
 5V_S5= 5 Voltage soft off(S5 state)
 3D3V_S0= 3.3 Voltage power up on system work(S0 state)
 3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
 3D3V_S5= 3.3 Voltage soft off(S5 state)
 LVDDR_2D5V= 2.5 Voltage power up on system work(S0 state)
 2D5V_S3= 2.5 Voltage suspend to RAM(S3 state)
 2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
 1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
 1D5V_S0= 1.5 Voltage power up on system work(S0 state)
 1D5V_S5= 1.5 Voltage soft off(S5 state)
 DDR_VREF_S3= 1.25 Voltage suspend to RAM(S3 state)
 1D25V_S0= 1.25 Voltage power up on system work(S0 state)
 1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
 1D05V_S0= 1.05 Voltage power up on system work(S0 state)
 CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
 VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power



PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0# / GNT0#
Cardbus Controller TI7411	AD22	(CARBUS) P_INTG# (1394) P_INTF# (CARD READER) P_INTG#	REQ1# / GNT1#
LAN	AD23	P_INTE#	REQ2# / GNT2#
Blue Thumb	AD24		

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Title: **ITP**

Size: A3	Document Number: Leopard	Rev: -4
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Date: Sunday, February 27, 2005 Sheet 2 of 41

6 H_A#[31..3]

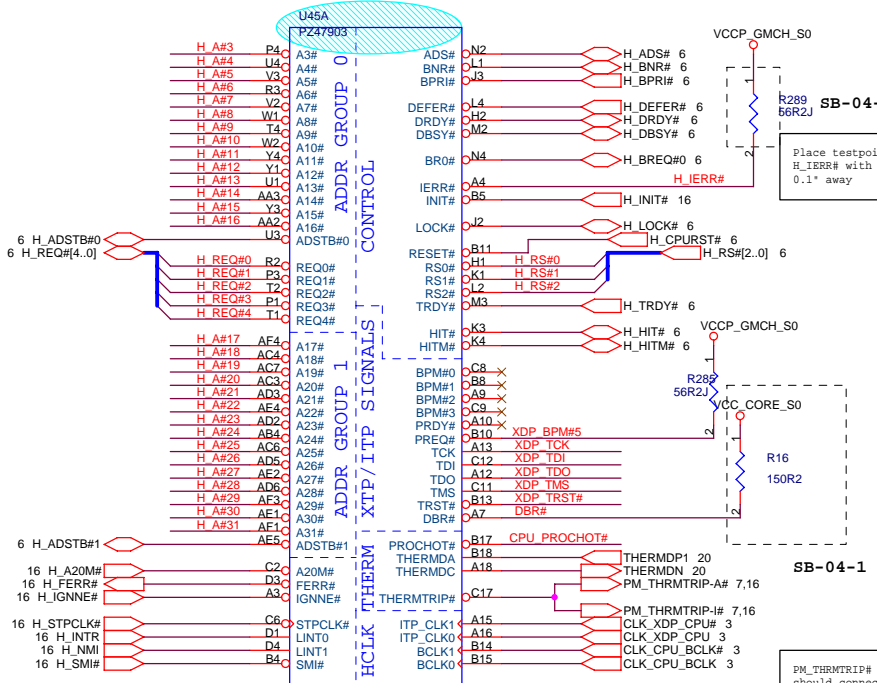
SD 0817

3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41

VCCP_GMCH_S0

5,6,7,9,10,16,18,36,40,41 VCCP_GMCH_S0

3D3V_S0



VCCP_GMCH_S0

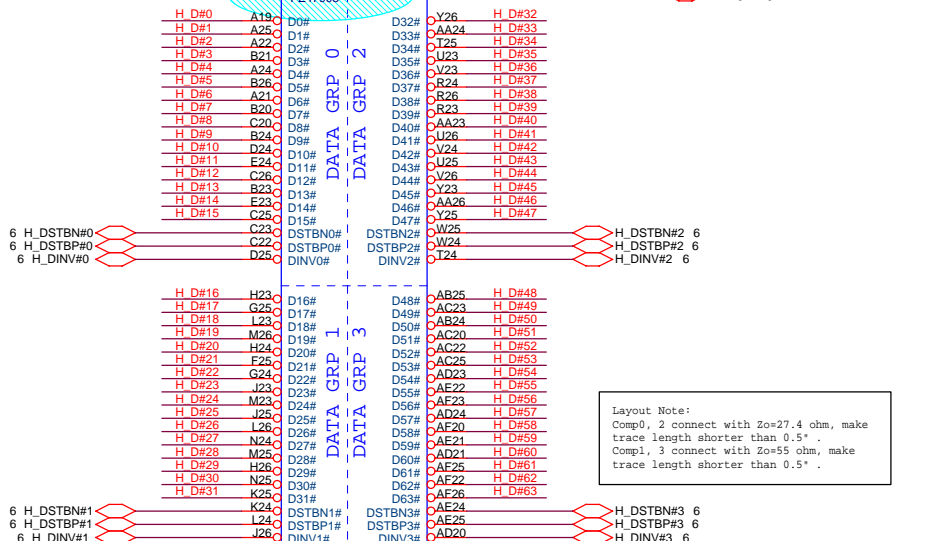
R289 56R2J SB-04-2

Place testpoint on H_IERR# with a GND 0.1" away

SD 0817

U45B (P247903)

H_D#[63..0] 6



R288 56R2J VCC CORE_S0

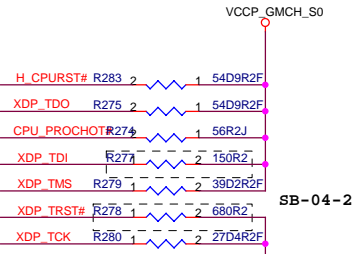
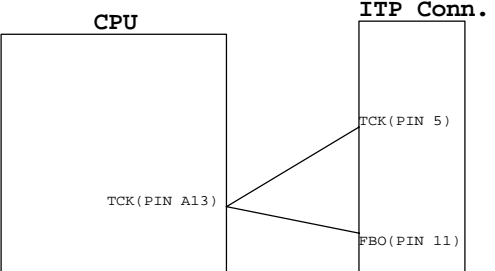
R16 150R2

PM_THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)

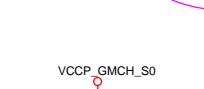
Dothan A: R43,R44=DUMMY
Dothan B: R43,R44=0R

6 H_DSTBN#0
6 H_DSTBP#0
6 H_DIN#0

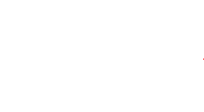
Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".



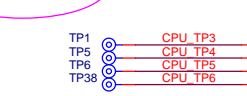
3,7 CPU_SEL0
3,7 CPU_SEL1



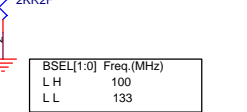
VCCP_GMCH_S0



TP3 PSI# E10



VCCP_GMCH_S0



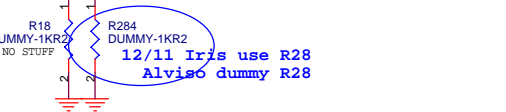
MISC



VCCP_GMCH_S0



VCCP_GMCH_S0

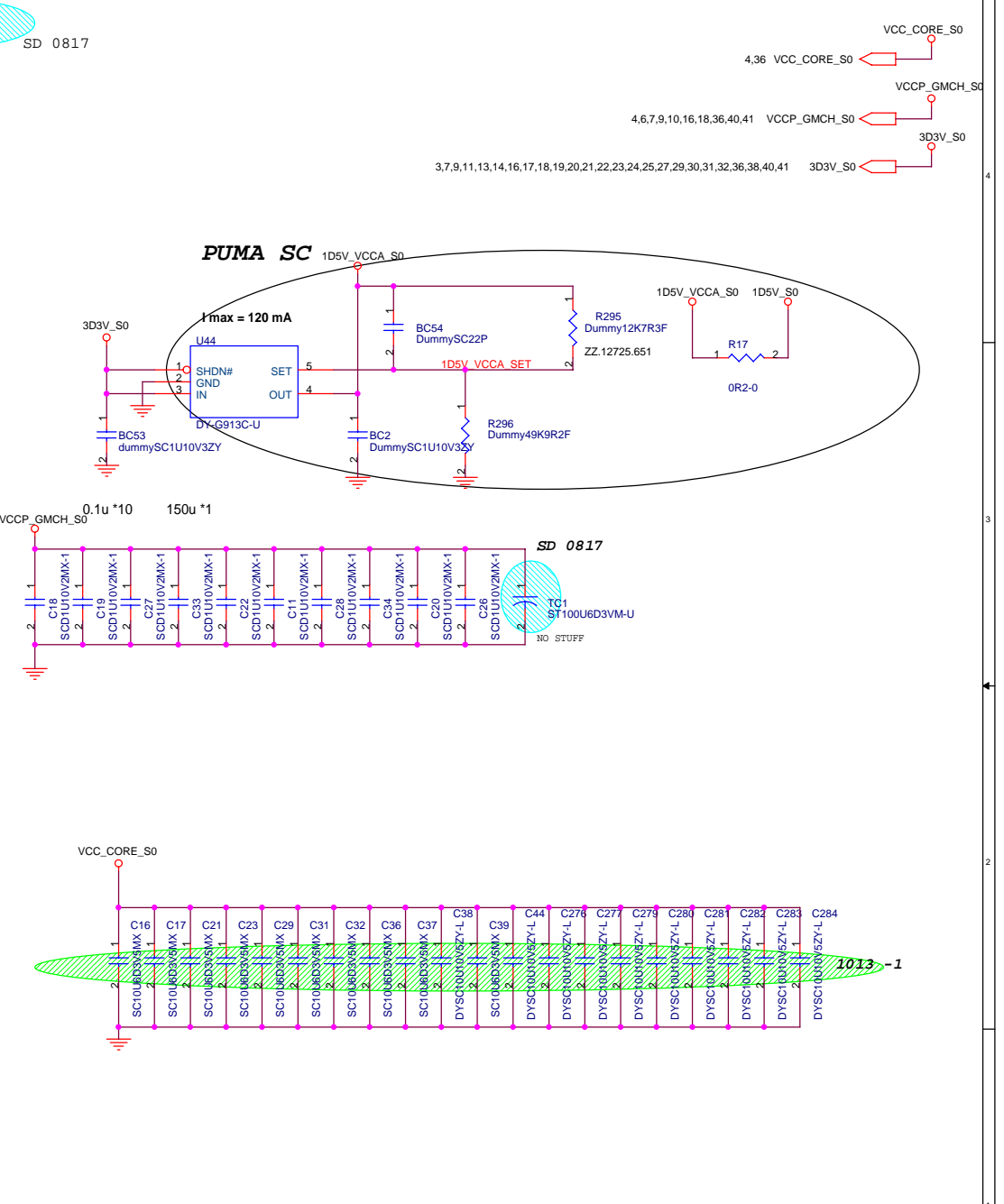
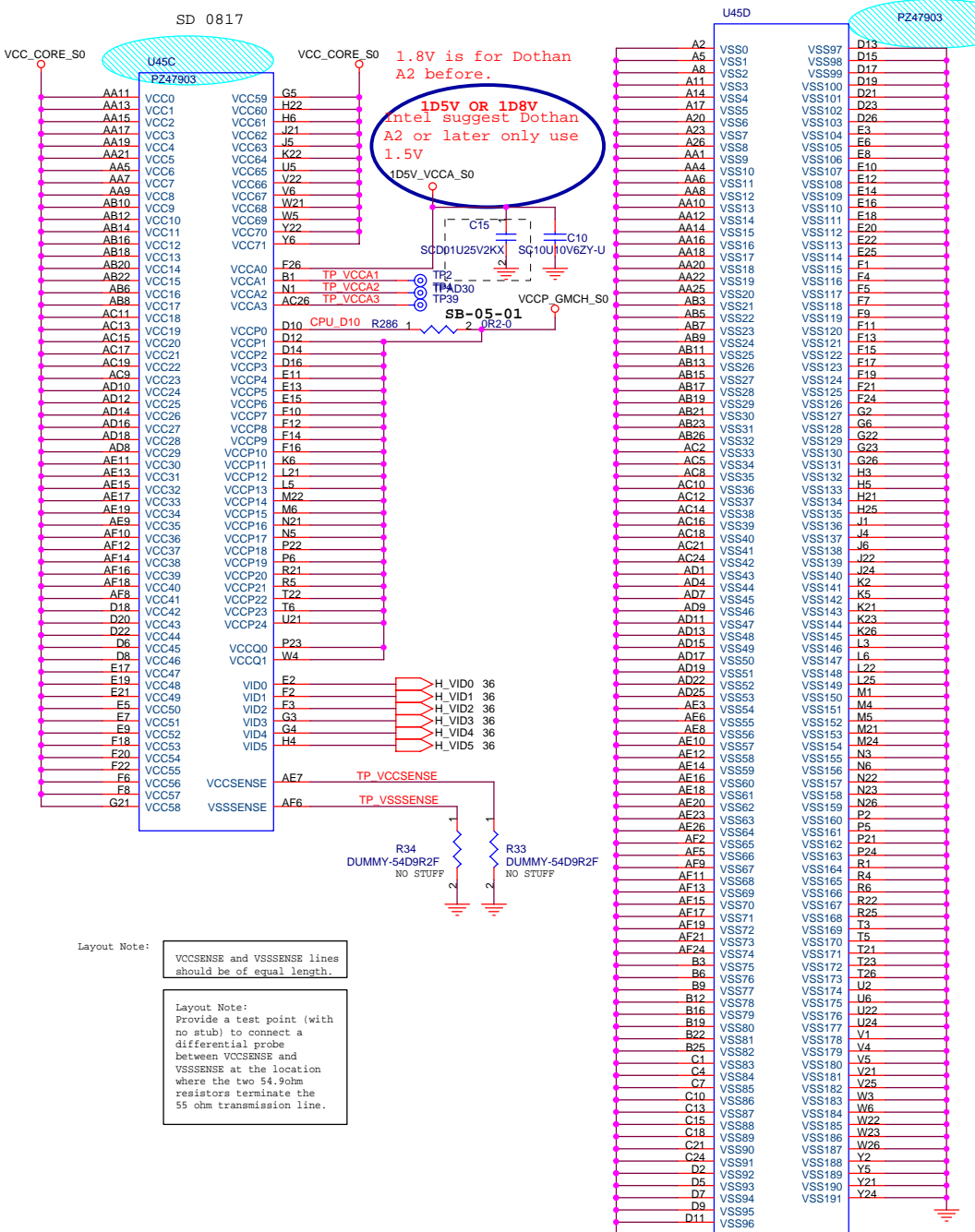


R284 DUMMY-1KR2 12/11 Iris use R28 Alviso dummy R28



Title		
CPU (1 of 2)		
Size	Document Number	Rev
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Date:	Monday, February 28, 2005	Sheet 4 of 41

All place within 2" to CPU



Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

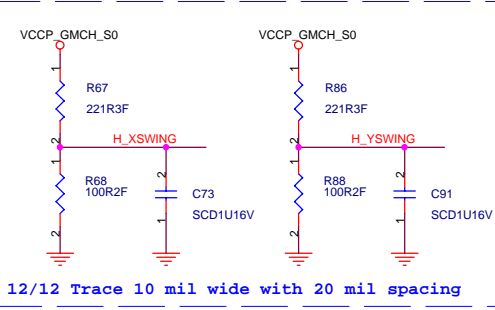
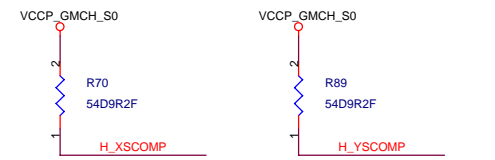
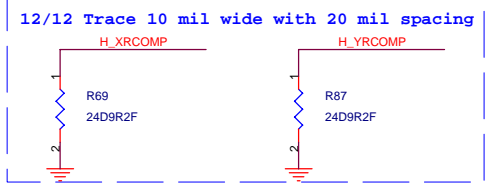
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

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Title: CPU (2 of 2)

Size: A3 Document Number: Leopard Rev: -4

Date: Monday, February 28, 2005 Sheet: 5 of 41

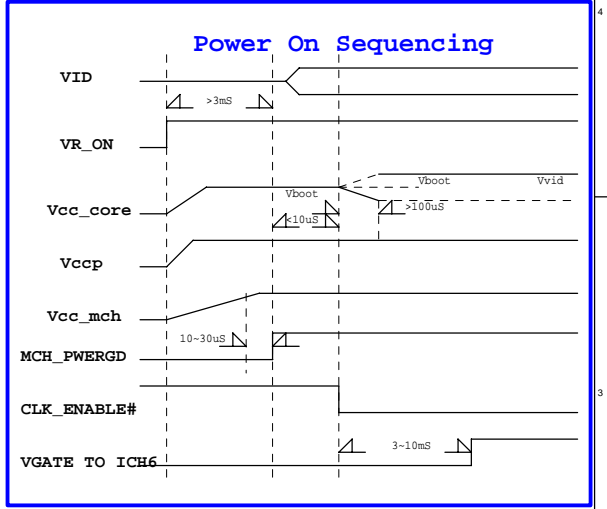
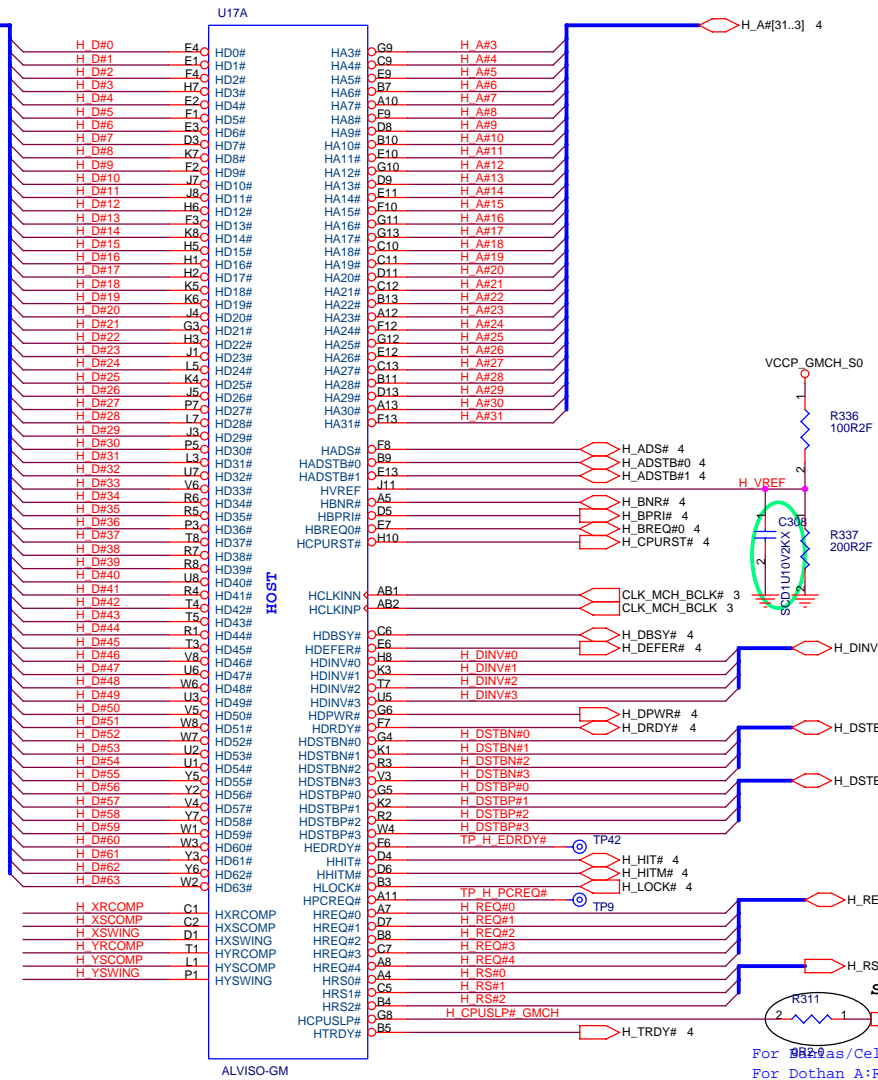


Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 101 = FSB400 others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = DDR1 (Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes 1 = Normal (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	GMCH core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCTRL_DATA	SDVO Present	0 = No SDVO device present(Default) 1 = SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORX In signal.



2/10 HMI-SC
Intel Sightings
issue 54489

SC 0630
For Dothan A:R93=DUMMY
For Dothan B:R93=0R

ALVISO-GM: 71.0GMCH.08U
ALVISO-PM: 71.0GMCH.0BU
ALVISO-GML: 71.0GMCH.0JU

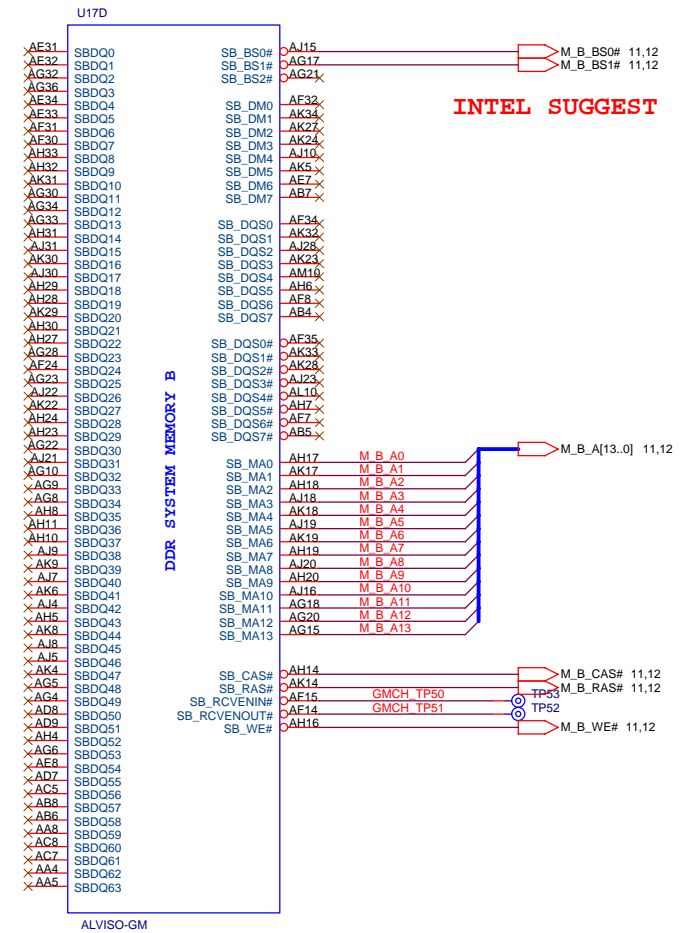
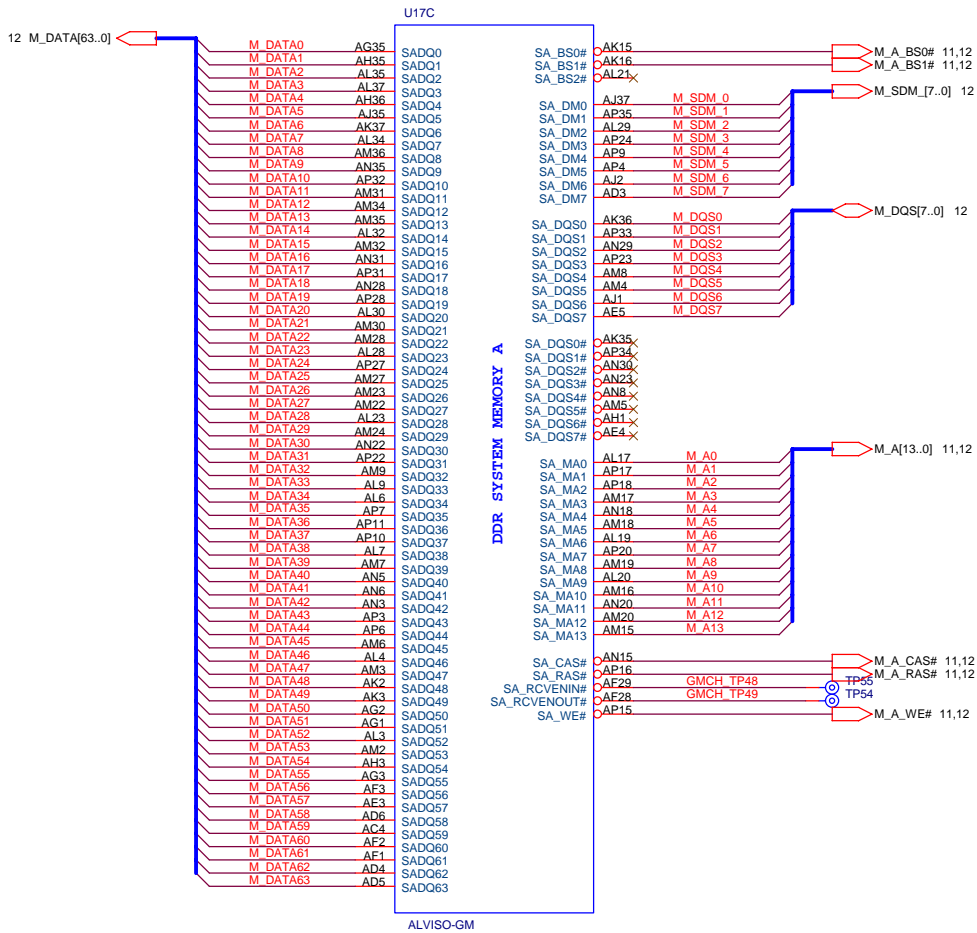
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Title: GMCH (1 of 5)

Size: A3 Document Number: Leopard Rev: -4

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SUPPORT DDR333 ONLY



INTEL SUGGEST

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Title: GMCH (3 of 5)

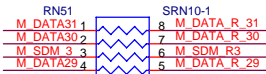
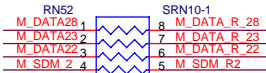
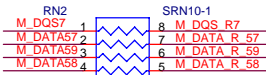
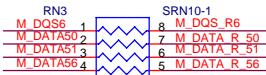
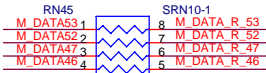
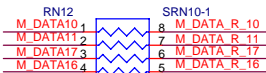
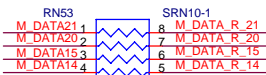
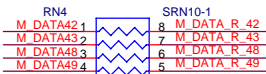
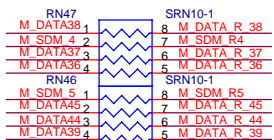
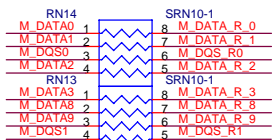
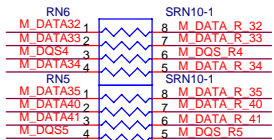
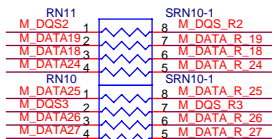
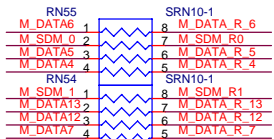
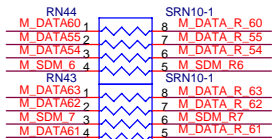
Size: A3
Document Number: Leopard
Rev: -4

Date: Monday, February 28, 2005 Sheet 8 of 41

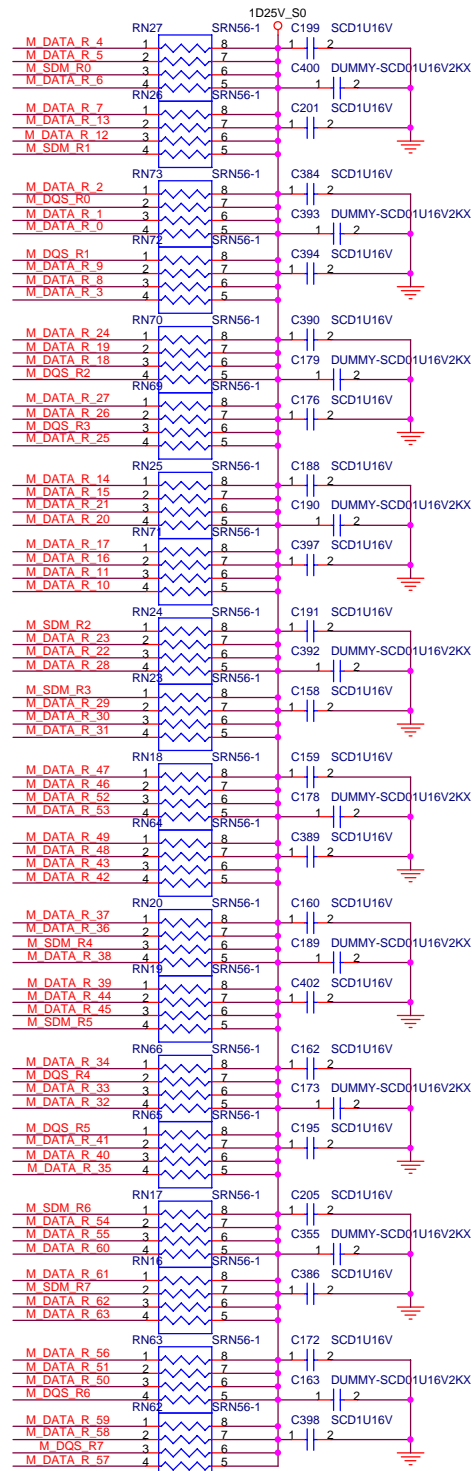
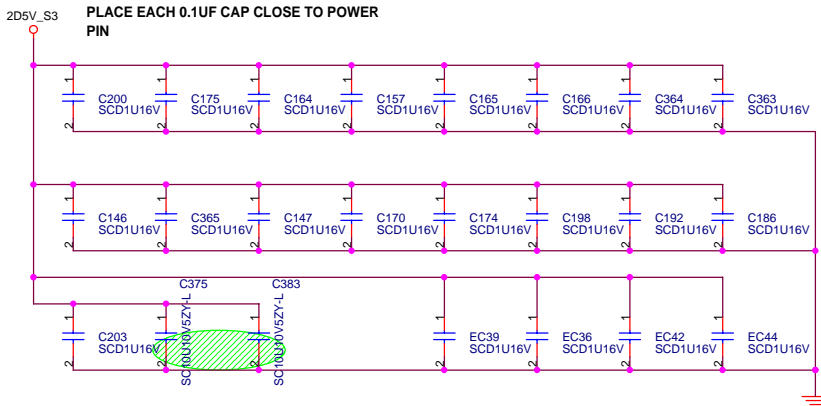
SERIES DAMPING

PUMA-SC

Change RN to small size

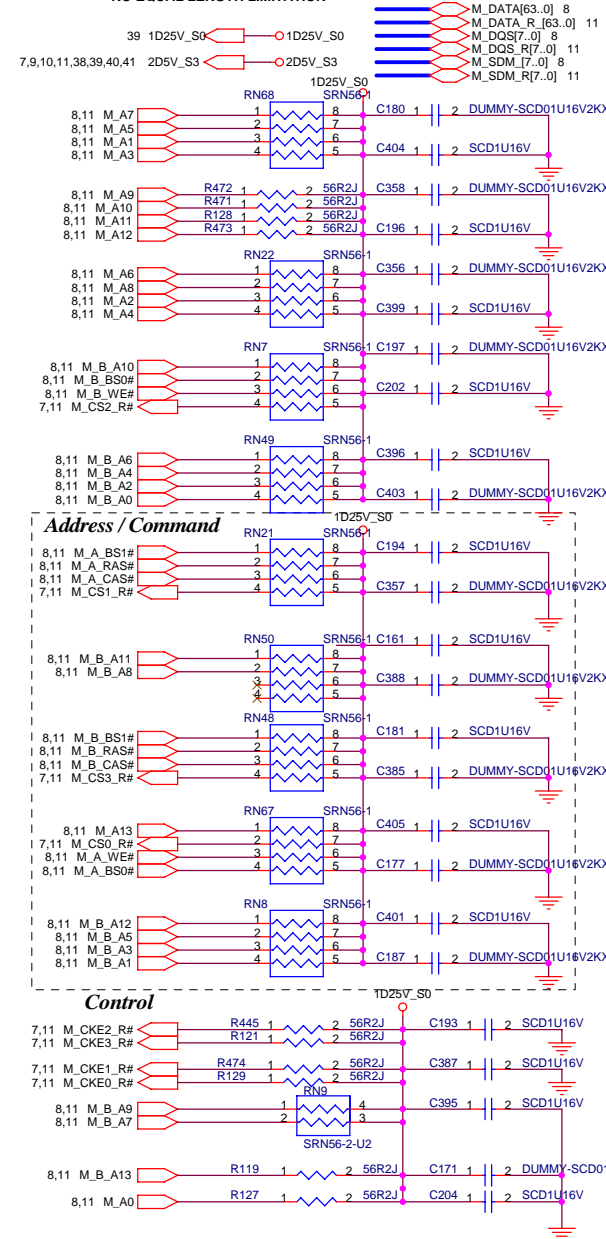


PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER
PIN



PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO DM2
NO EQUAL LENGTH LIMITATION

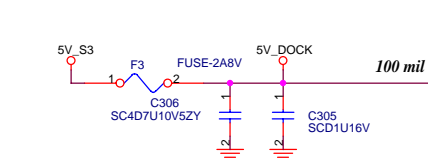
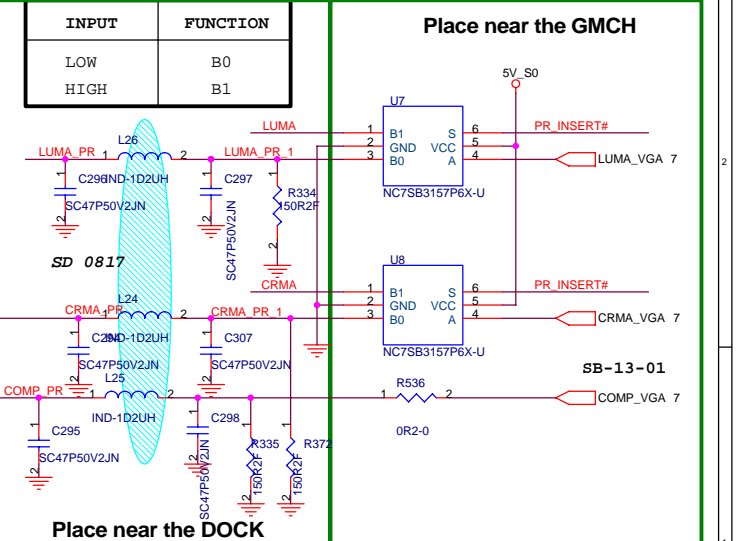
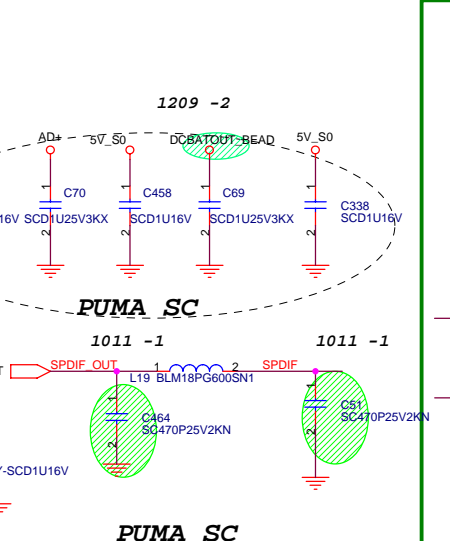
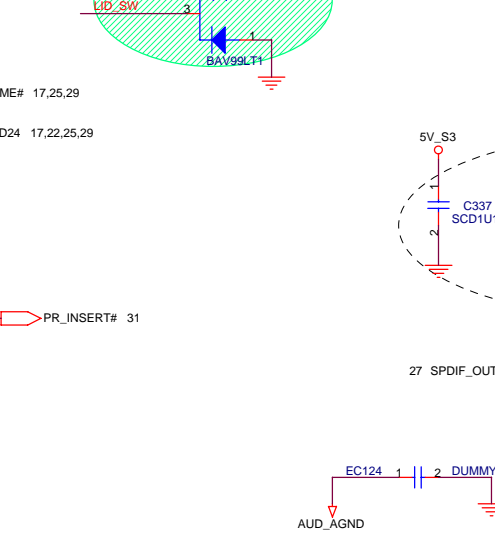
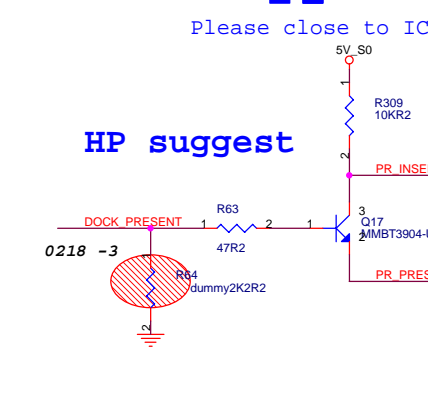
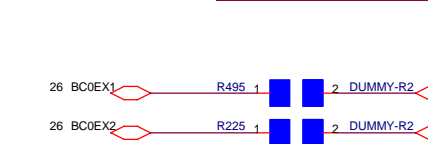
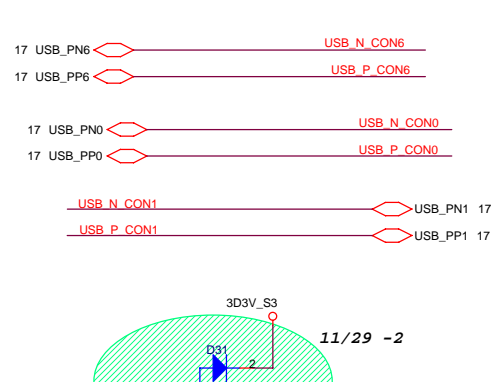
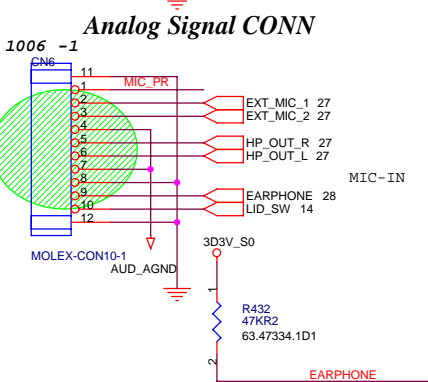
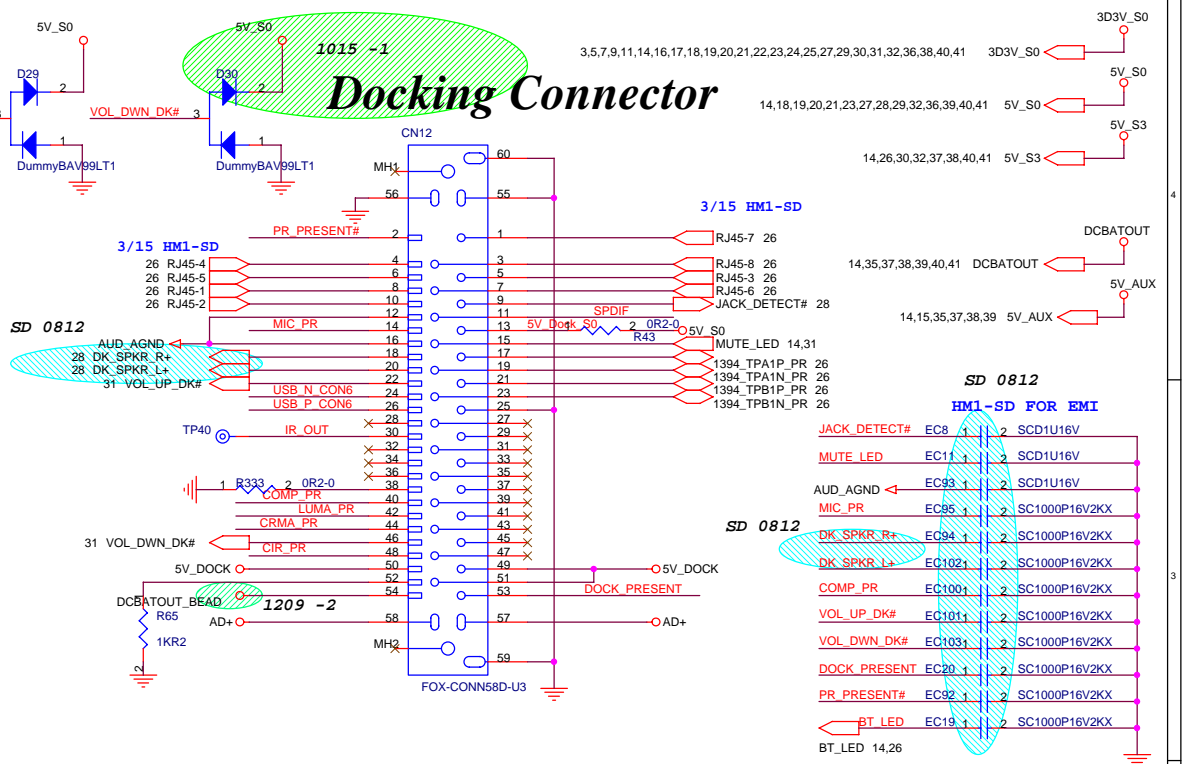
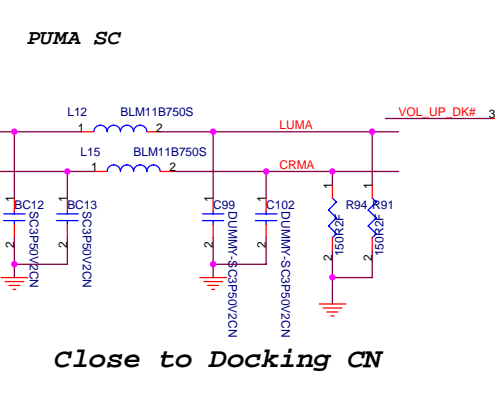
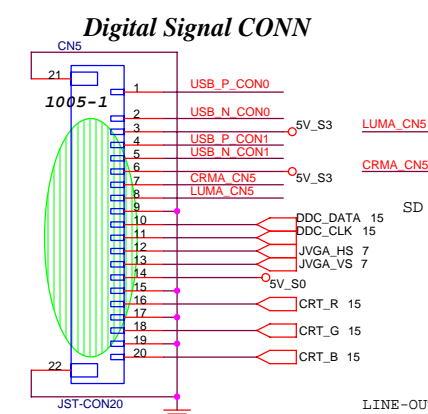


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Title: **DDR Serial/Terminator Resistor**

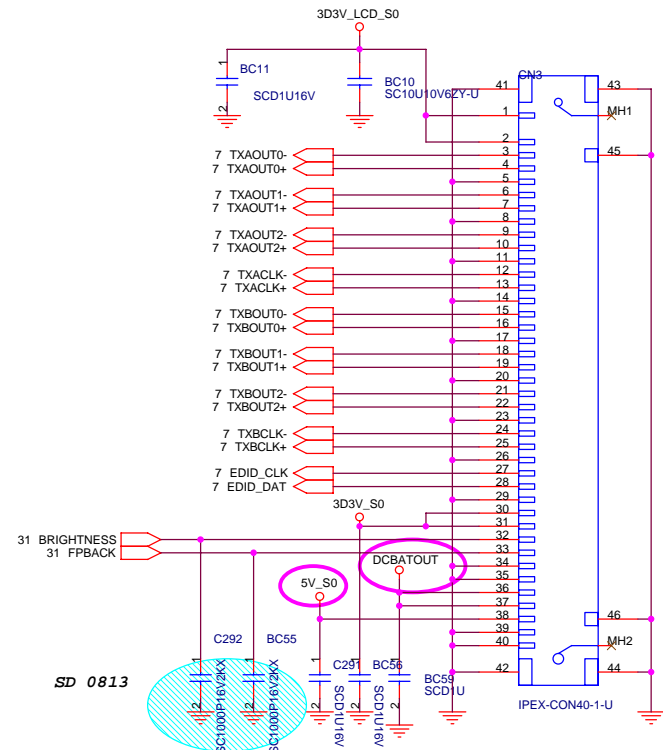
Size: A3 | Document Number: **Leopard** | Rev: **-4**

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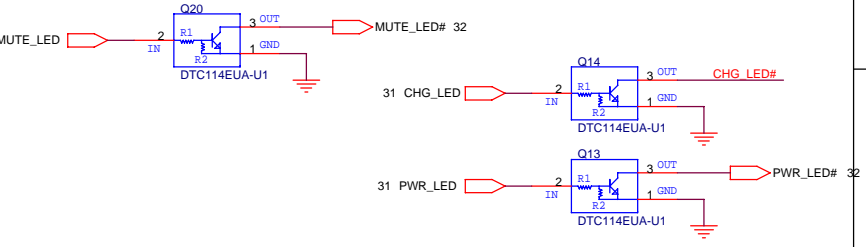
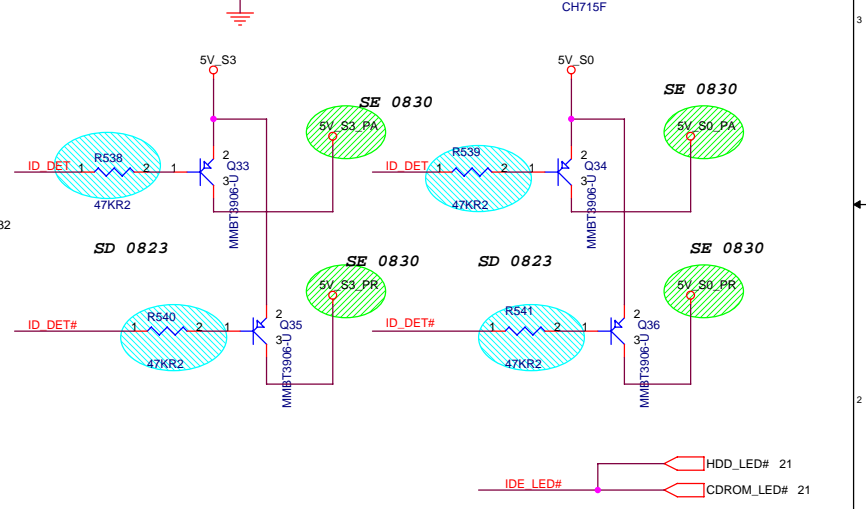
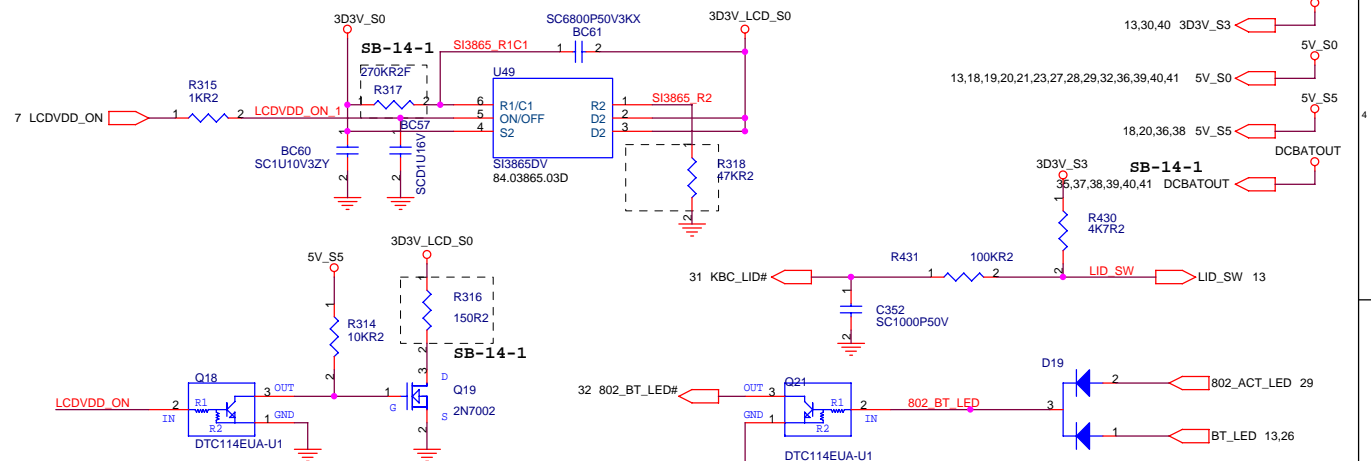
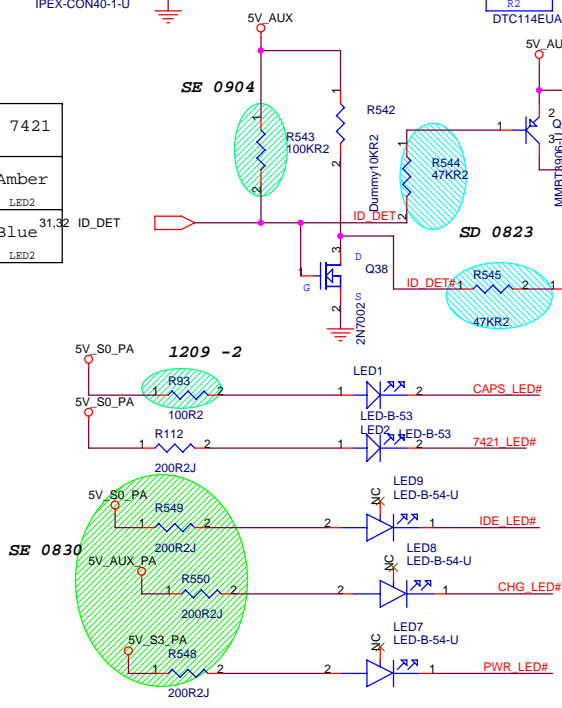
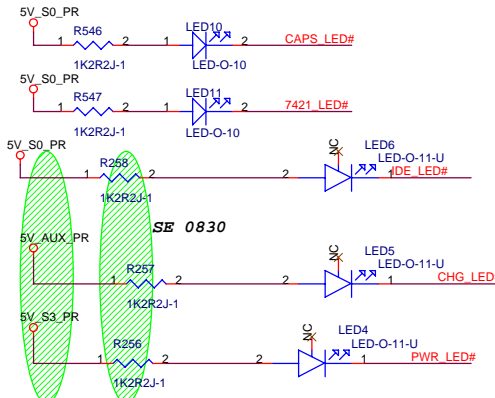
CIR, CIR_PR, CIR_KBC are connect together. default setting 12/12

INVERTER/LCD



	PWR	CHR	HDD	IR	CAPS	7421
PR Botton	Amber LED4	Amber LED5	Amber LED6	U42	Amber LED1	Amber LED2
PA Top	Blue LED8	Blue LED7	Blue LED9	U64	Blue LED1	Blue LED2

SC 0705
change R from 100 to 200 ohm
PUMA SC



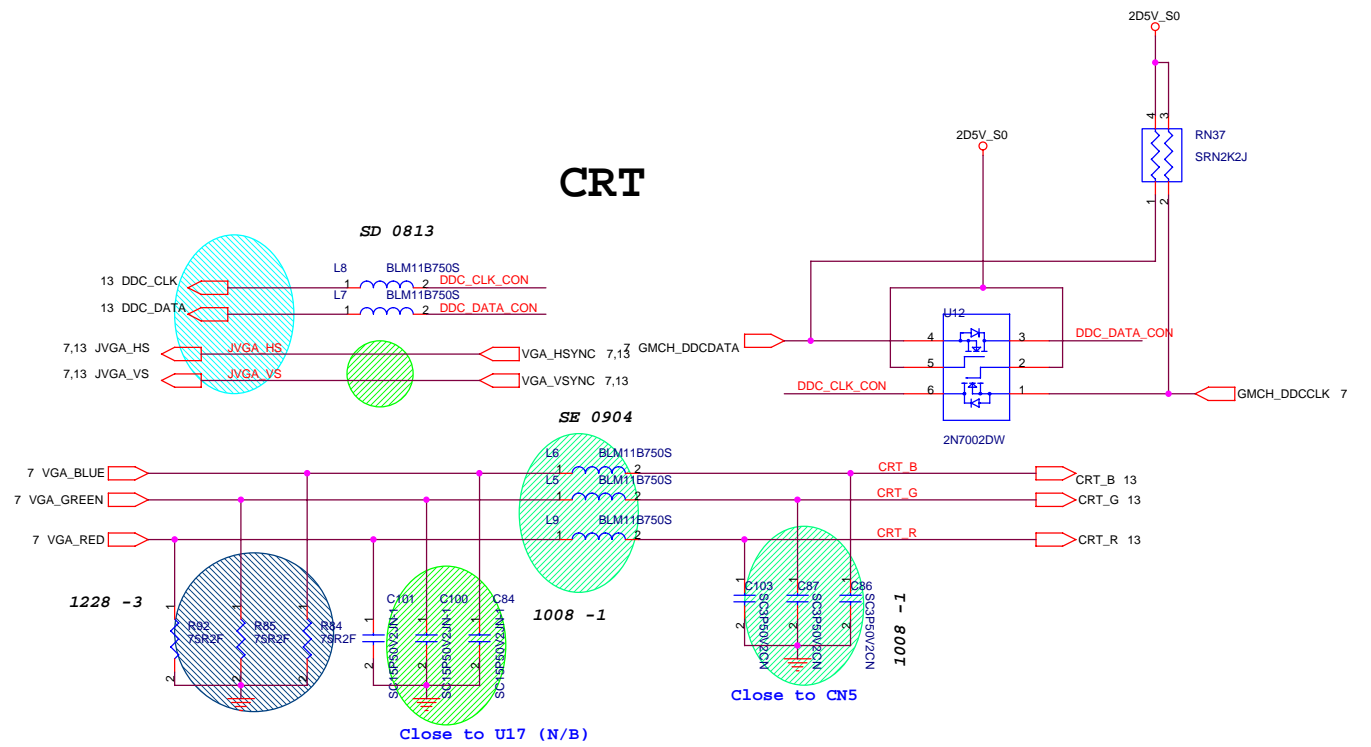
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wj Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title Inverter/LCD		
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PA & PR diffent parts

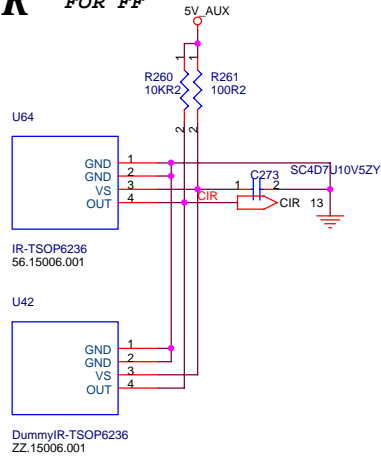
	PA	PR
LED1	83.00190.Y70	83.00190.W70
LED2	83.00190.Y70	83.00190.W70
LED4	Dummy	83.00110.D70
LED5	Dummy	83.00110.D70
LED6	Dummy	83.00110.D70
LED7	83.00110.E70	Dummy
LED8	83.00110.E70	Dummy
LED9	83.00110.E70	Dummy
U64	56.15006.001	Dummy
U42	Dummy	56.15006.001
R256	63.20134.1D1	63.12234.1D1
R257	63.20134.1D1	63.12234.1D1
R258	63.20134.1D1	63.12234.1D1
R93	63.20134.1D1	63.12234.1D1
R112	63.20134.1D1	63.12234.1D1

CBUS1	21.H0088.001	21.H0088.001
R176	63.10334.1D1	Dummy
R177	Dummy	63.10334.1D1



010804 Modified on Astro ID request

CIR FOR FF

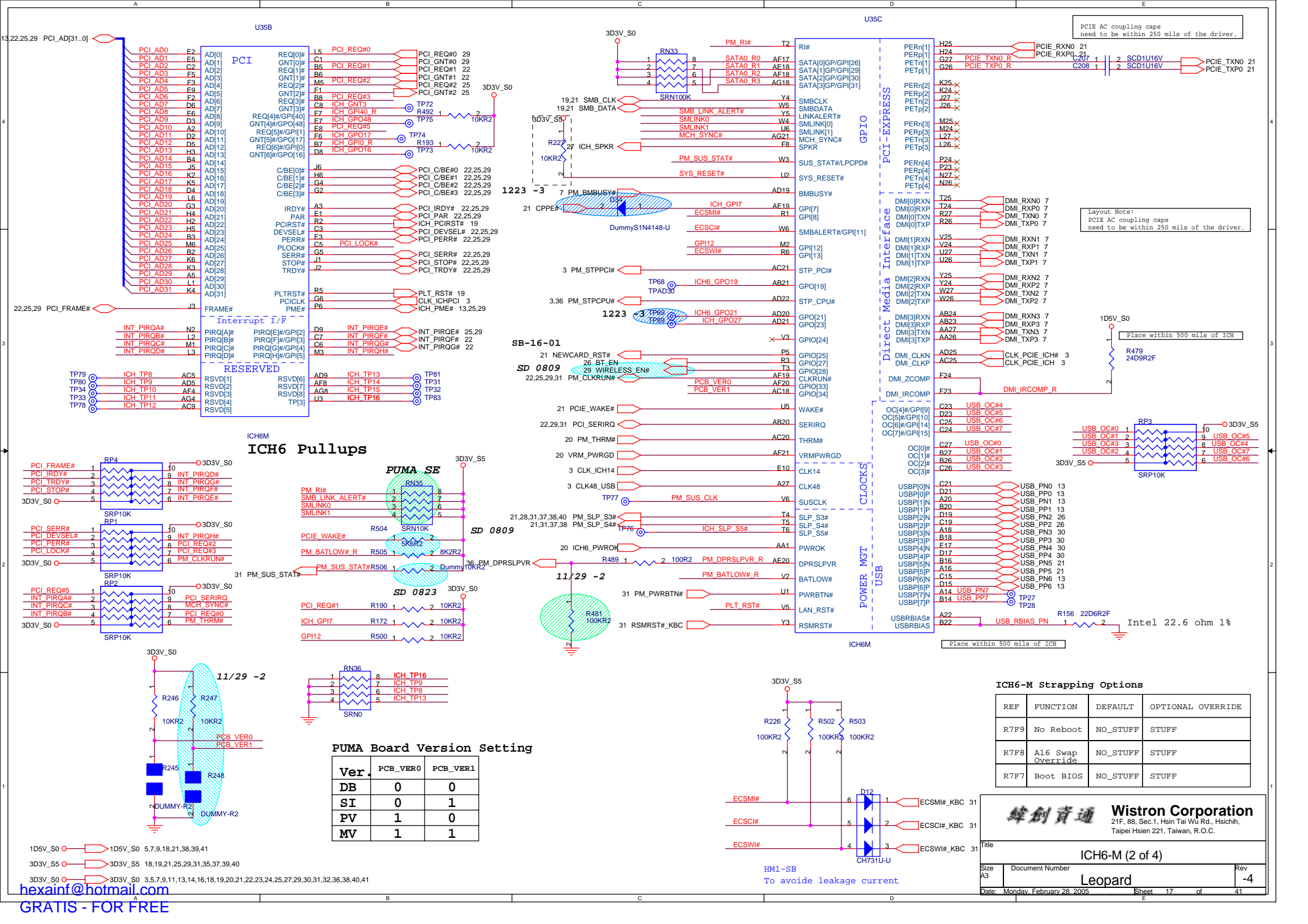


緯創資通 Wistron Corporation
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Title: **CRT/ CIR**

Size: A3 Document Number: **Leopard** Rev: **-4**

Date: Monday, February 28, 2005 Sheet: 15 of 41



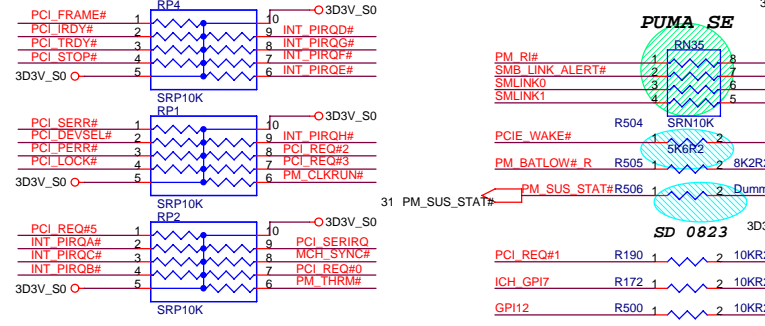
PCIe AC coupling caps need to be within 250 mils of the driver.

Layout Note: PCIe AC coupling caps need to be within 250 mils of the driver.

Place within 500 mils of ICH

Place within 500 mils of ICH

ICH6M ICH6 Pullups



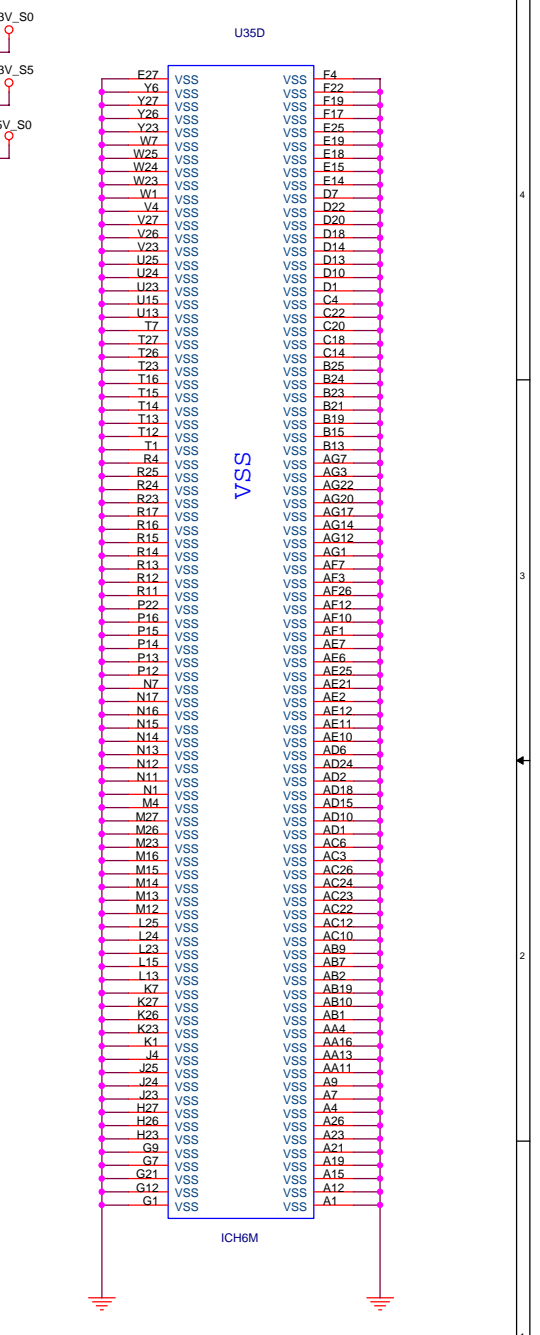
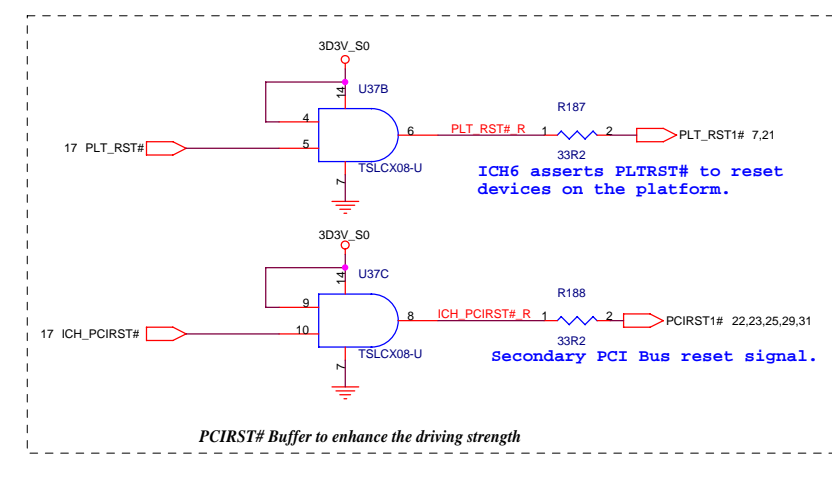
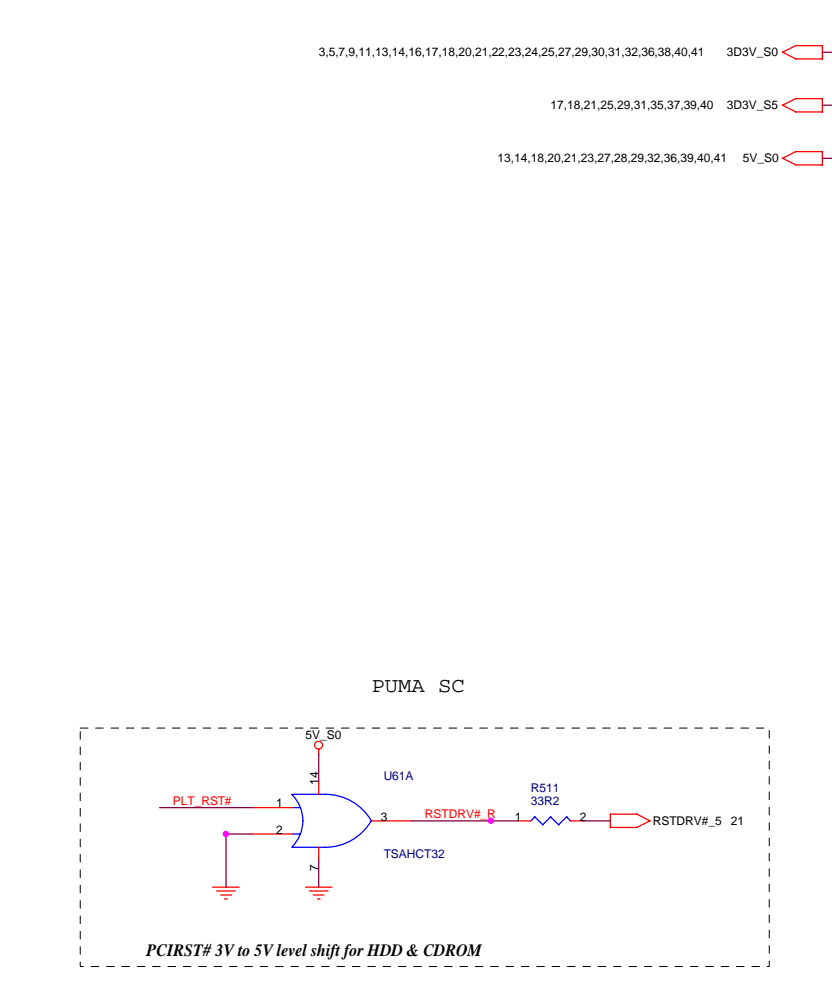
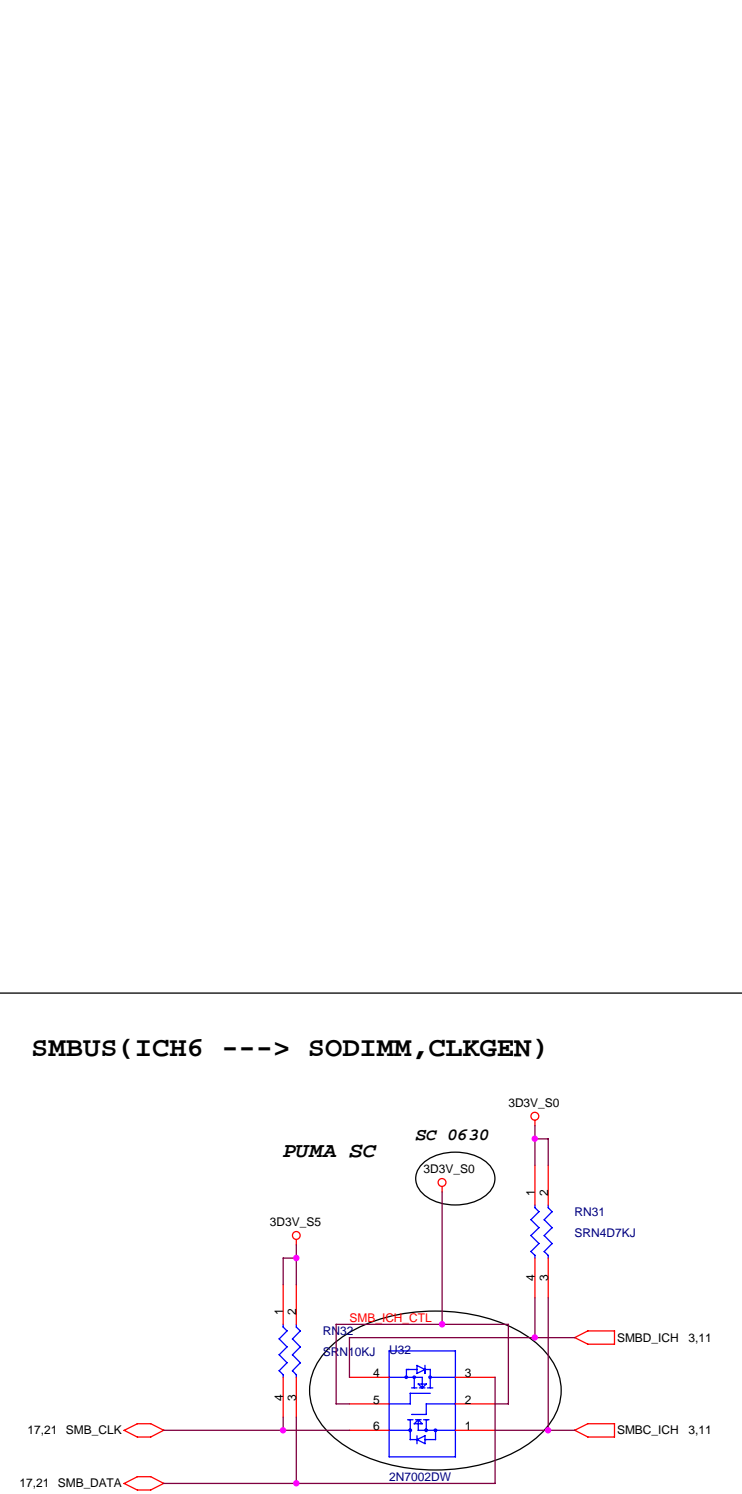
PUMA Board Version Setting

Ver.	PCB_VER0	PCB_VER1
DB	0	0
SI	0	1
PV	1	0
MV	1	1

ICH6-M Strapping Options

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

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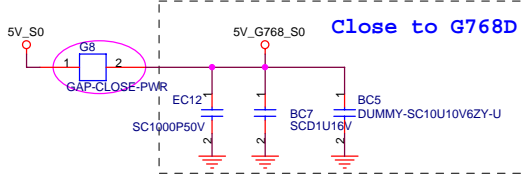


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wj Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

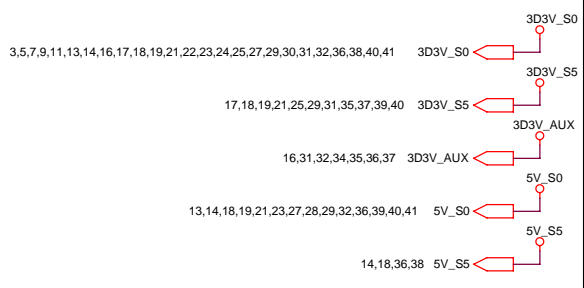
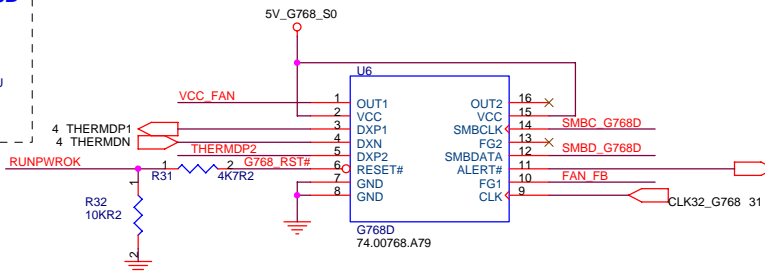
Title: **ICH6-M (4 of 4)**

Size: A3 | Document Number: **Leopard** | Rev: -4

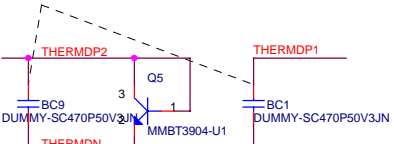
Date: Monday, February 28, 2005 | Sheet: 19 of 41



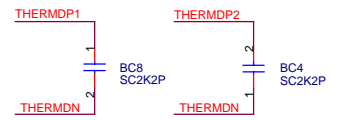
Reserve for G768B works at High Speed



Put these two Caps near the thermal diode.

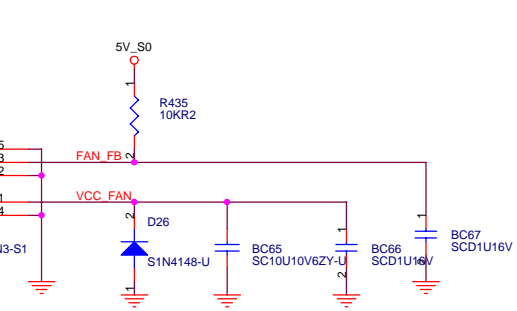


SYSTEM SENSOR

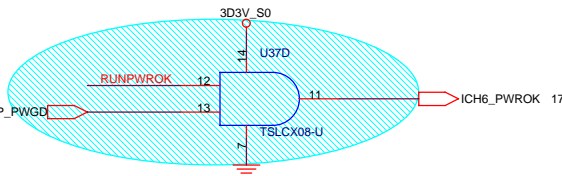
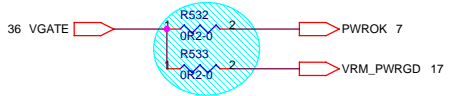
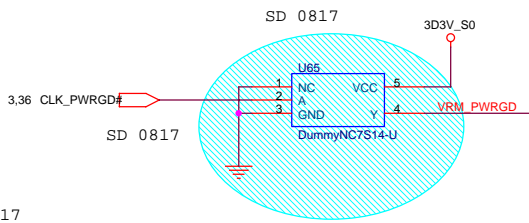


THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B

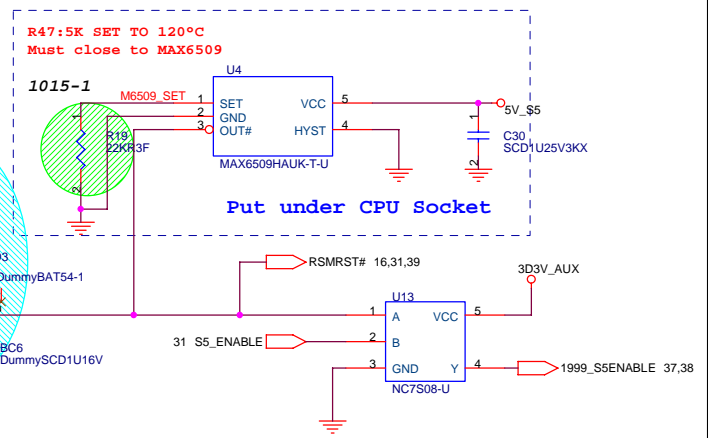
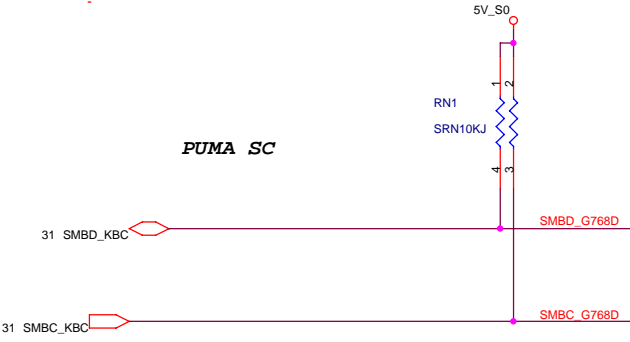
180 ms after VCC_G768 > 4.38v, p2, 7



The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103



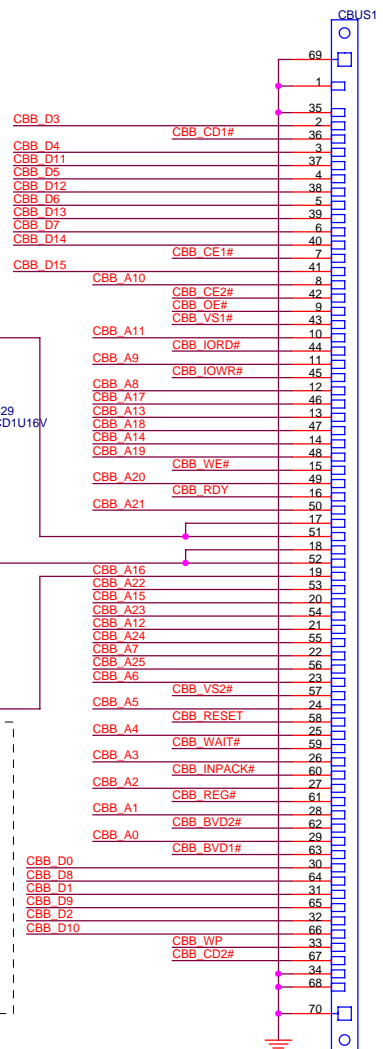
PUMA SC



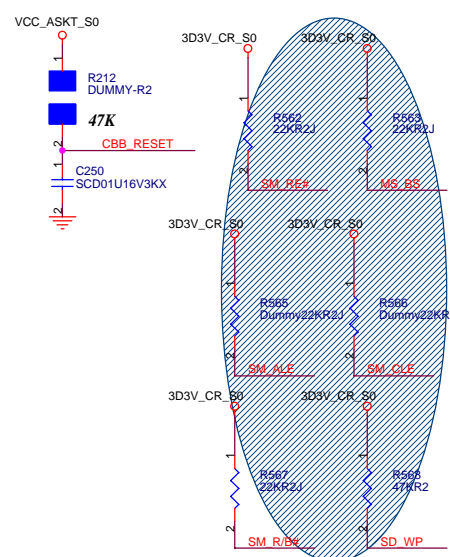
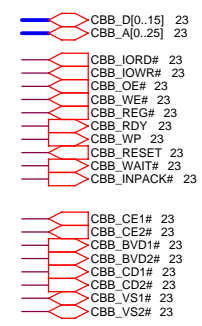
Put under CPU Socket

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Title		
G768D		
Size	Document Number	Rev
A3	Leopard	-4
Date:	Monday, February 28, 2005	Sheet 20 of 41

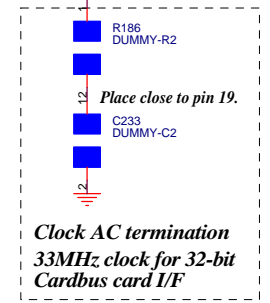
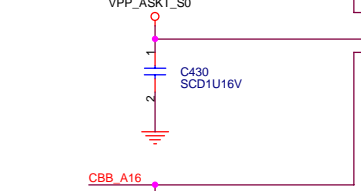
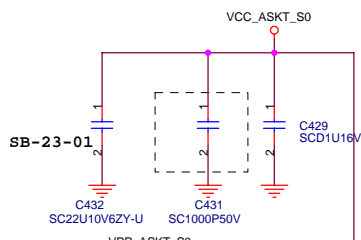
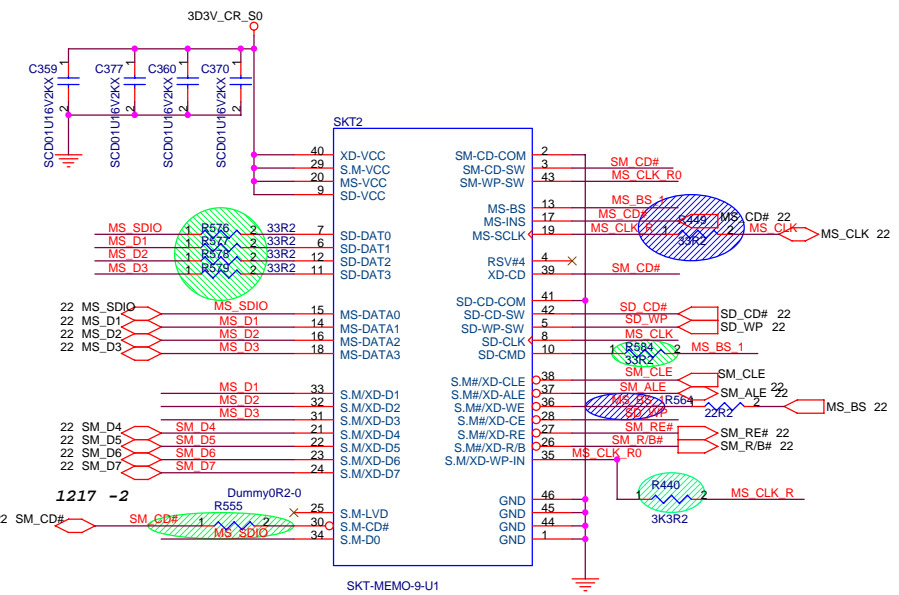
PCMCIA Socket



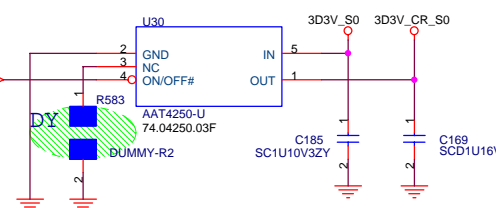
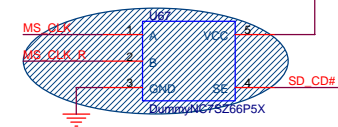
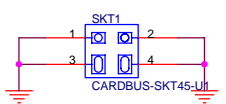
Cardbus I/F



6 in 1 Connector

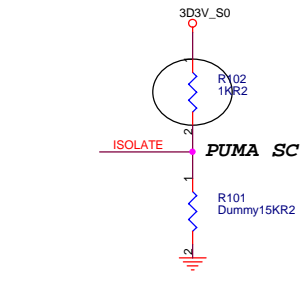
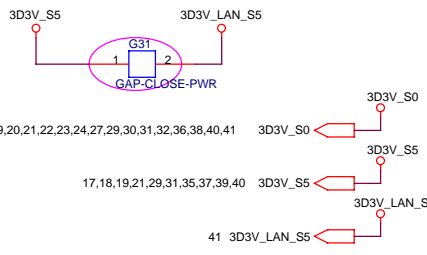
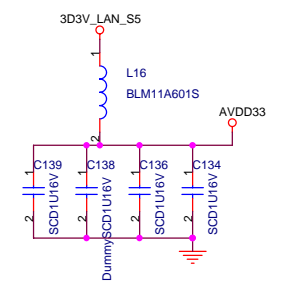
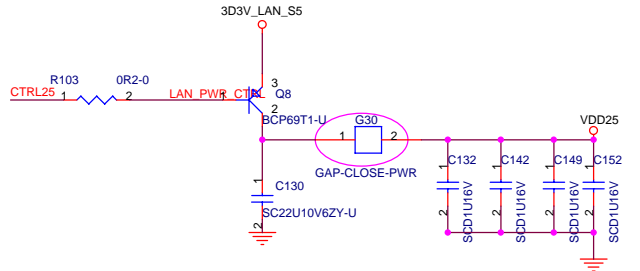
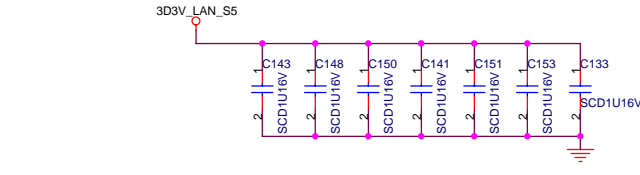
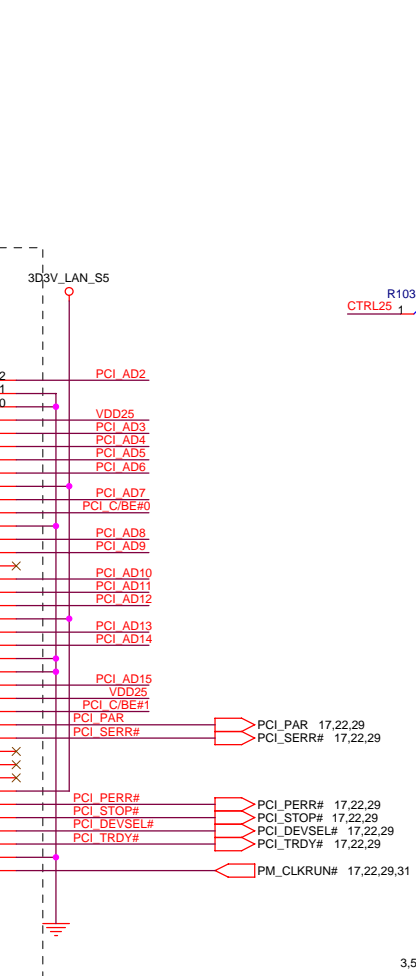
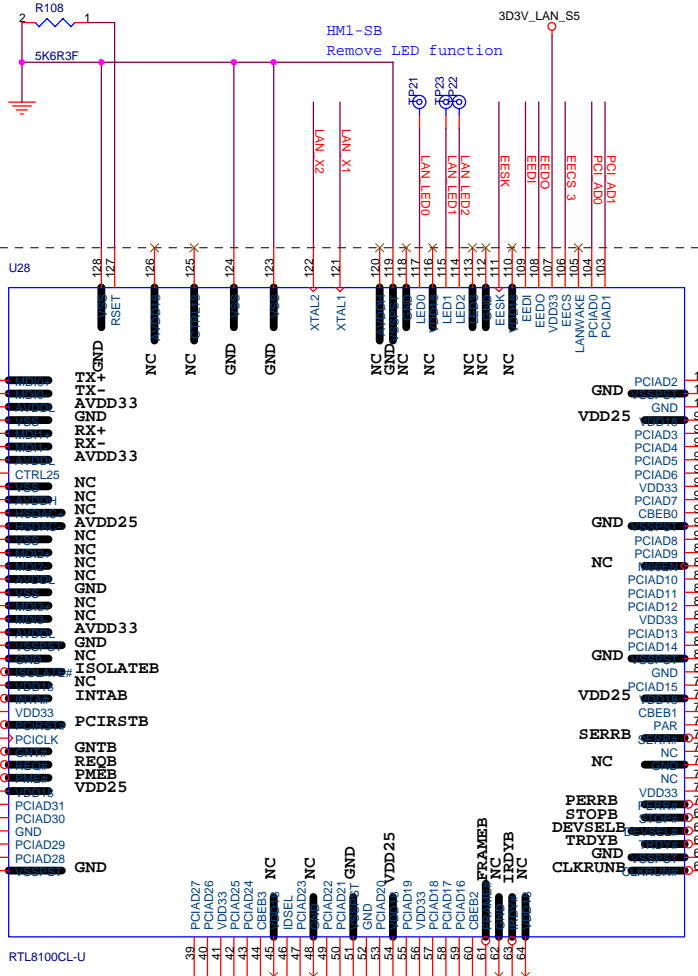
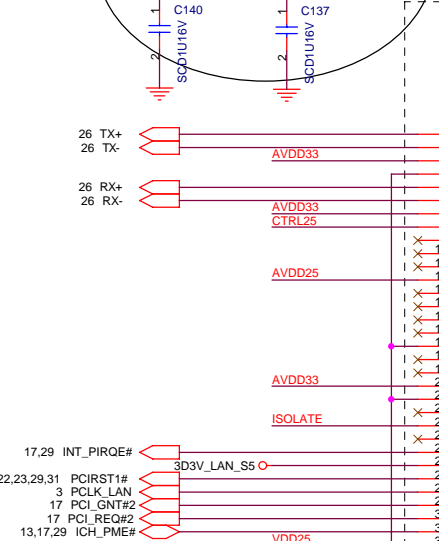
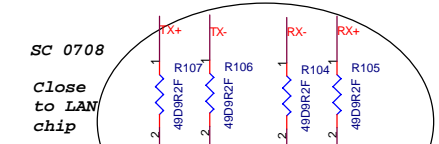
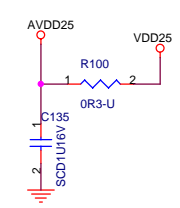
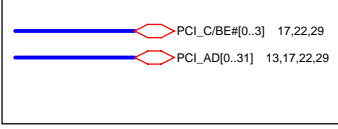
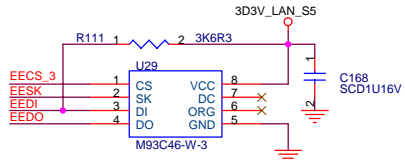
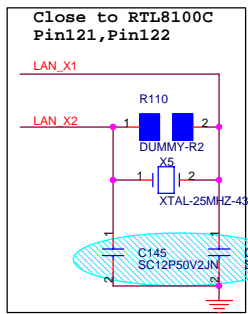


Place close to pin 19.
Clock AC termination
33MHz clock for 32-bit
Cardbus card I/F



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Title: PCMCIA SLOT/ CARDBUS SKT
Size: A3 Document Number: Leopard Rev: -4
Date: Monday, February 28, 2005 Sheet: 24 of 41



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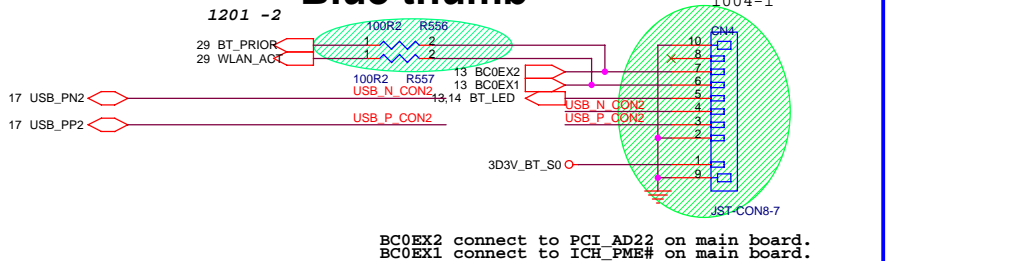
Title: **LAN RTL8100C**

Size: A3 Document Number: **Leopard** Rev: **-4**

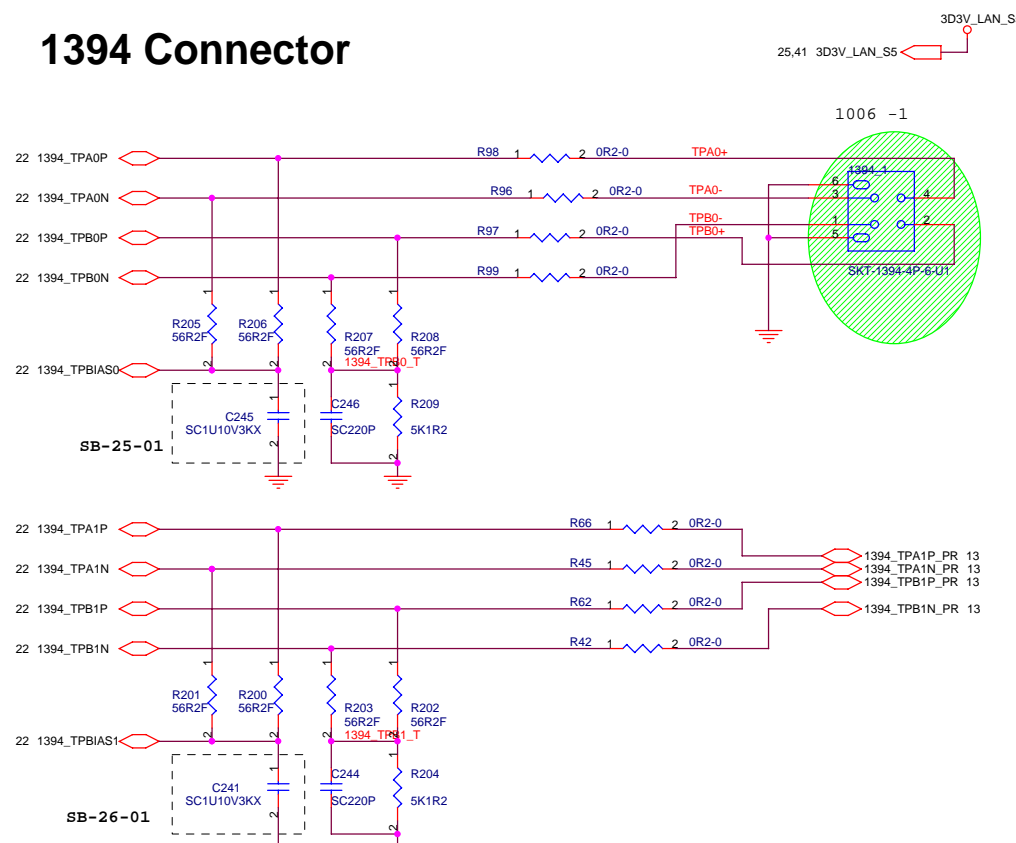
Date: Monday, February 28, 2005 Sheet: 25 of 41

Blue thumb

Place on bottom side

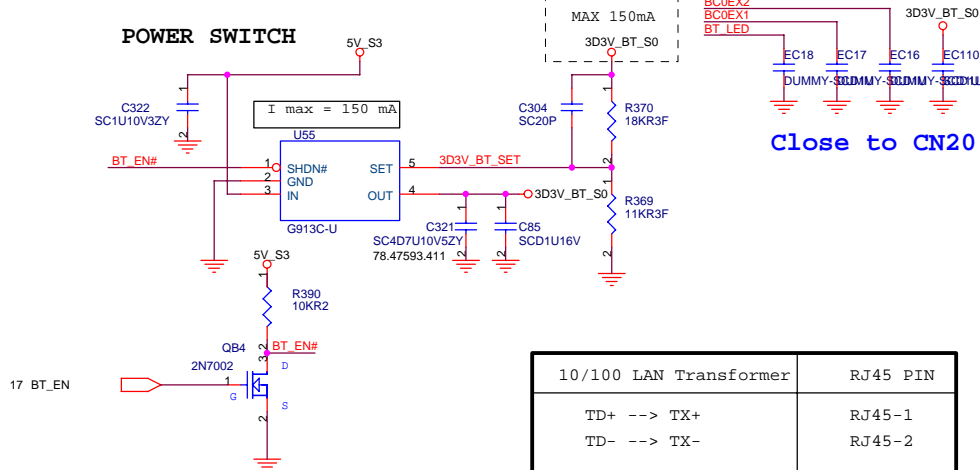


1394 Connector



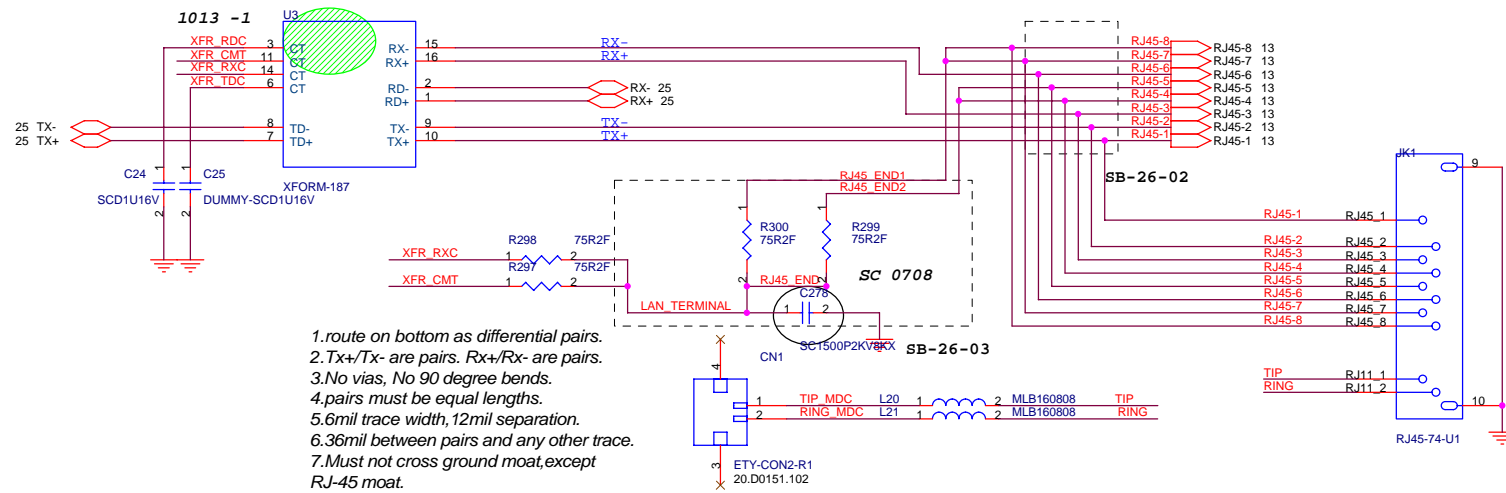
These components near to chip side.

POWER SWITCH

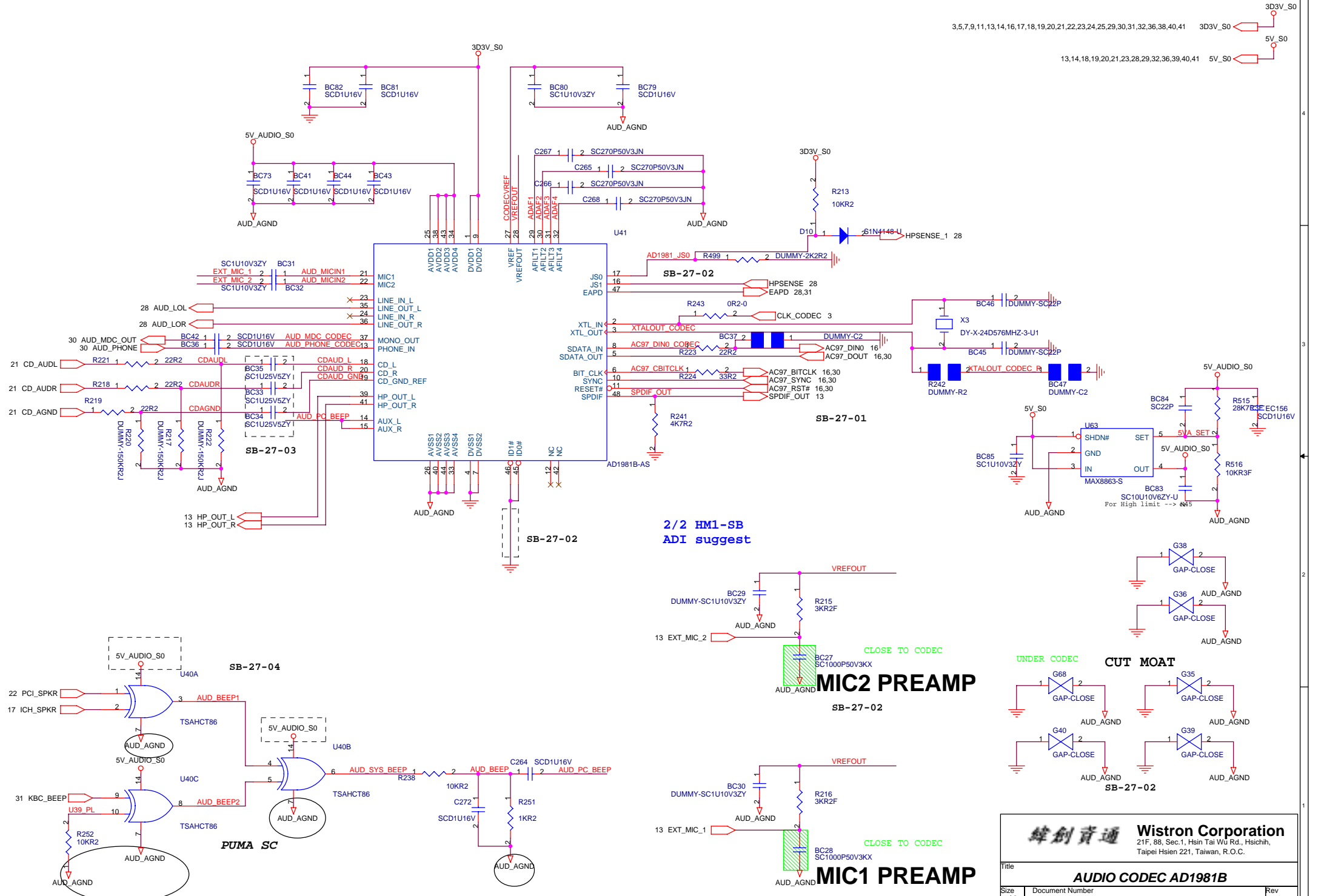


10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

10/100M Lan Transformer



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3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,29,30,31,32,36,38,40,41 3D3V_S0
 13,14,18,19,20,21,23,28,29,32,36,39,40,41 5V_S0

2/2 HM1-SB
 ADI suggest

MIC2 PREAMP
 SB-27-02

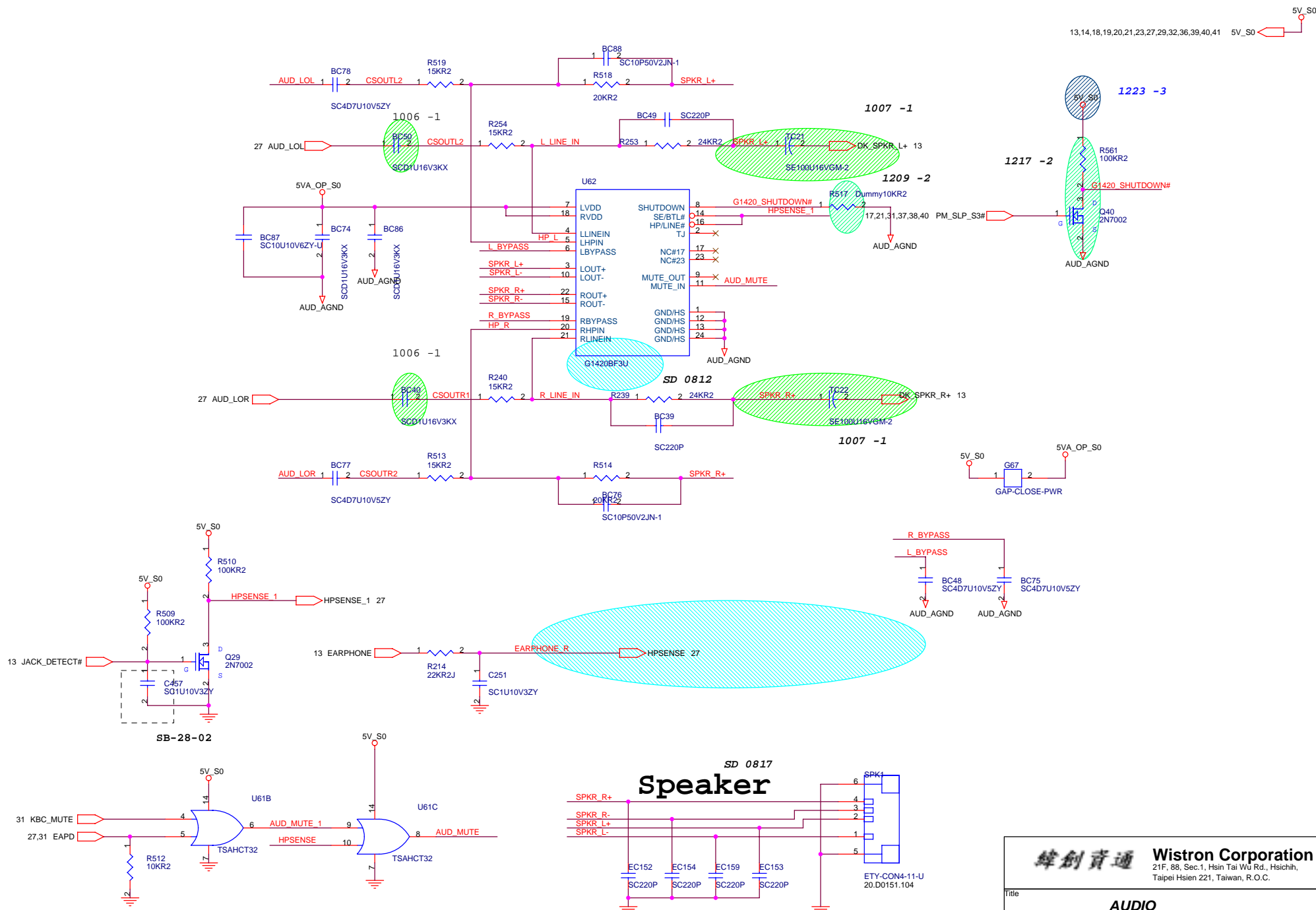
MIC1 PREAMP
 SB-27-02

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC AD1981B**

Size: A3	Document Number:	Rev: -4
Date: Monday, February 28, 2005		Sheet: 27 of 41

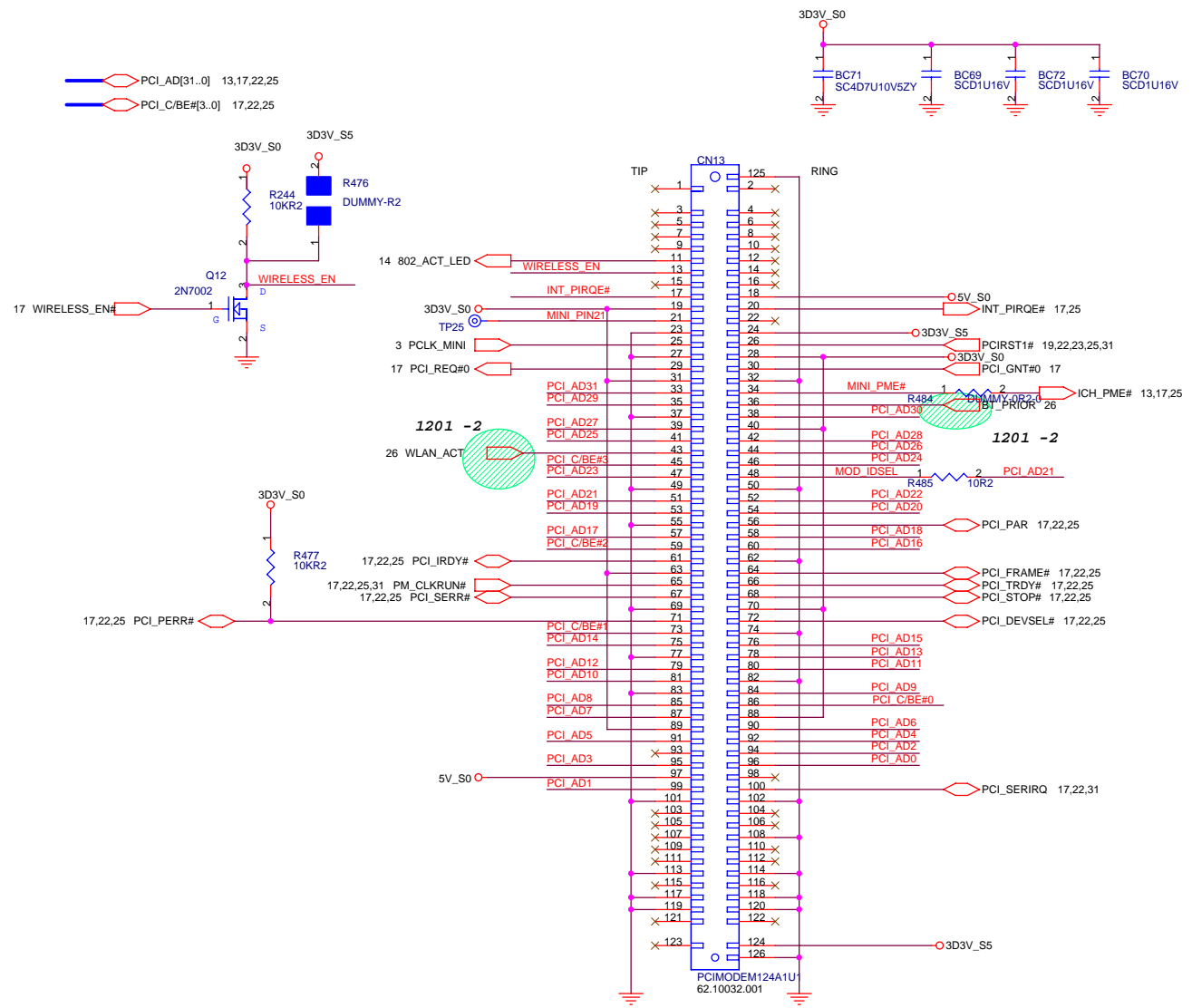
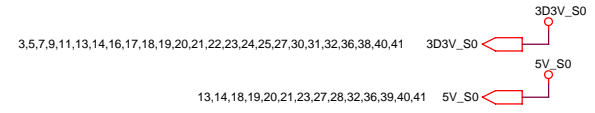
Leopard



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 Taipei Hsien 221, Taiwan, R.O.C.

Title		AUDIO	
Size A3	Document Number	Leopard	
Date: Monday, February 28, 2005		Sheet 28	of 41
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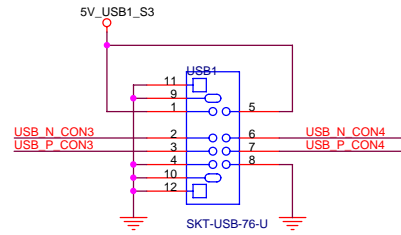
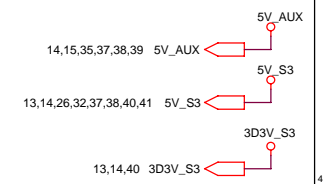
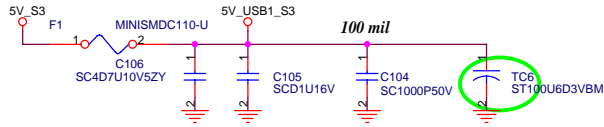
MINI-PCI



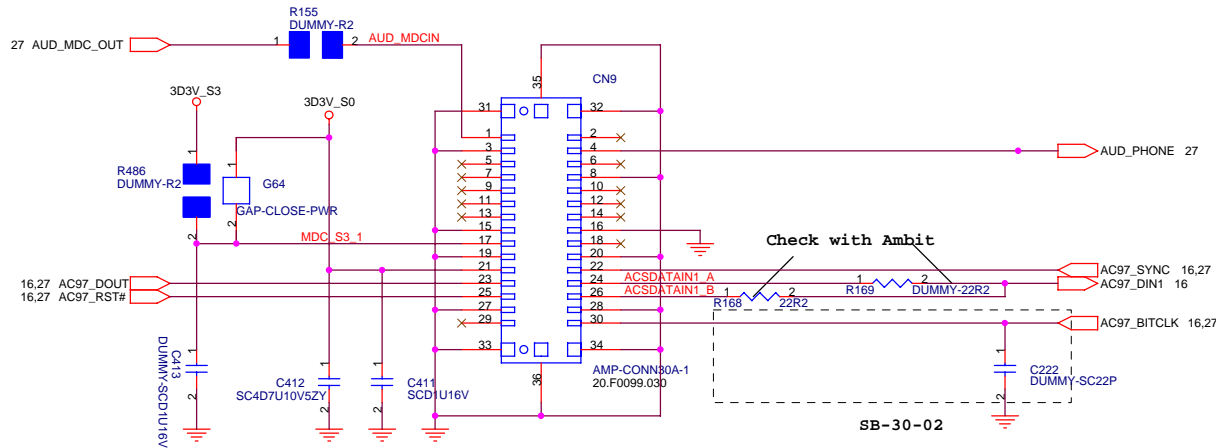
The symbol use 2nd source
 The P/N is the main source
 Main source: 62.10032.001
 2nd source: 62.10032.031

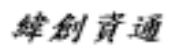
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
MINI-PCI		
Size	Document Number	Rev
A3	Leopard	-4
Date: Monday, February 28, 2005		Sheet 29 of 41

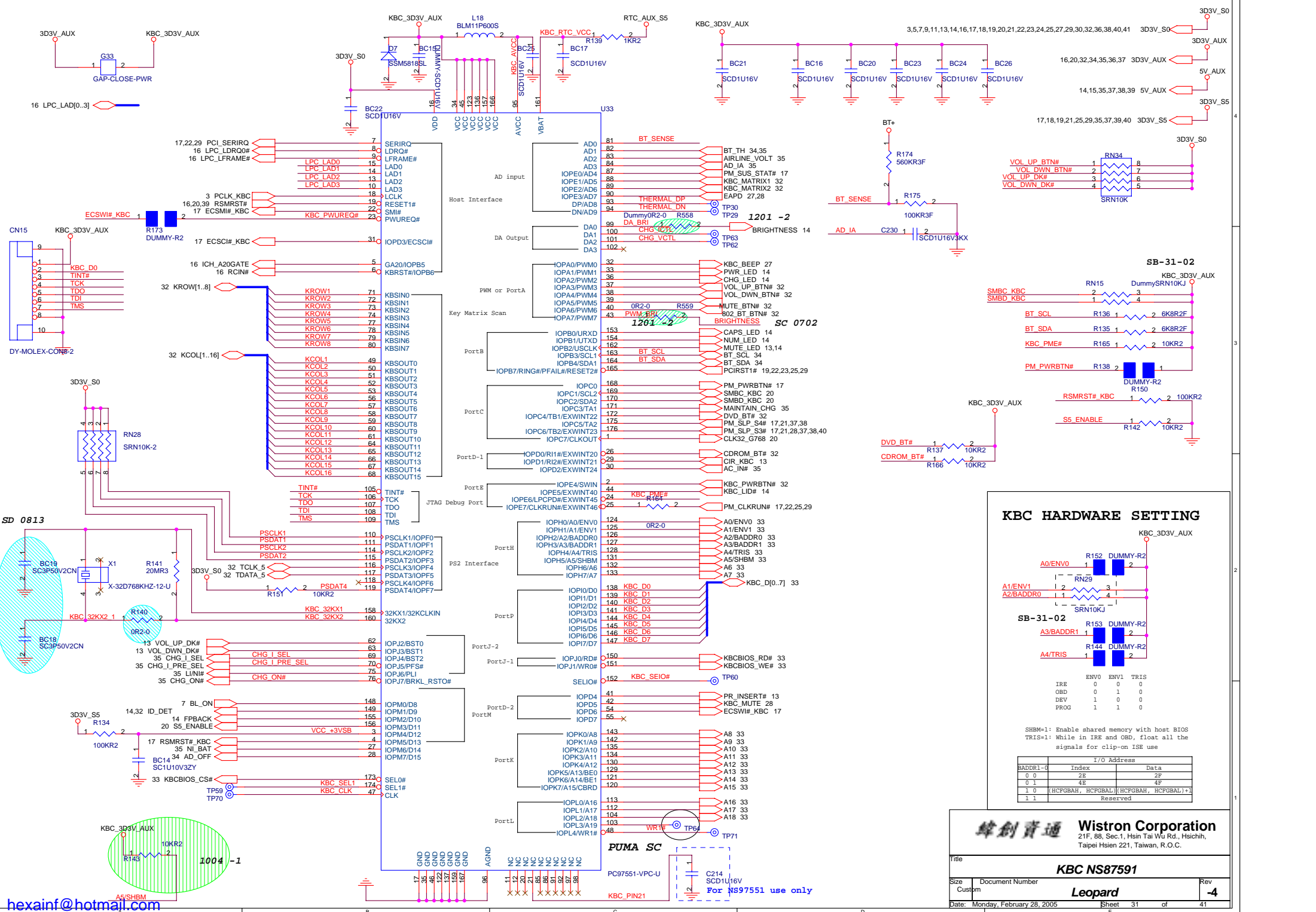
USB POWER



MDC Connector



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USB / MDC CONN.	
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KBC HARDWARE SETTING

KBC_3D3V_AUX

IRE	ENV0	ENV1	TRIS
0	0	0	0
0	0	1	0
1	0	0	0
1	1	0	0

SHBM=1: Enable shared memory with host BIOS
 TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use

BADDR1-0	Index	I/O Address	Data
0 0	2E	2E	2F
0 1	4E	4E	4F
1 0	[HCFGBAH, HCFGBAL][HCFGBH, HCFGBAL]+1		
1 1	Reserved		

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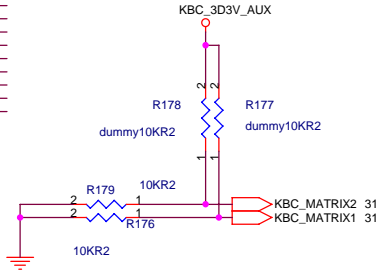
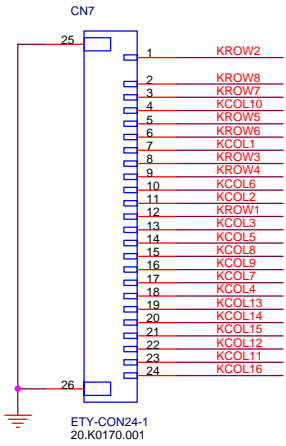
KBC NS87591

Title	Document Number	Rev
Size	Custpm	Sheet
Date: Monday, February 28, 2005	Leopard	31 of 41

hexainf@hotmail.com
 GRATIS - FOR FREE

INTERNAL KEYBOARD CONNECTOR

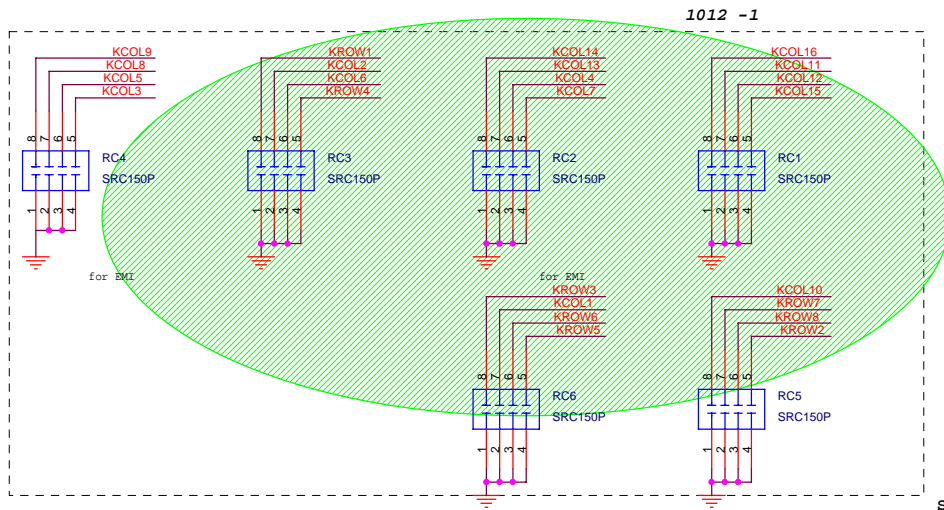
KROW[1..8] 31 KCOL[1..16] 31



the matrix table for PCB

KBC_MATRIX2, KBC_MATRIX1		
PA	PR	
FF	00	01
DF	10	11

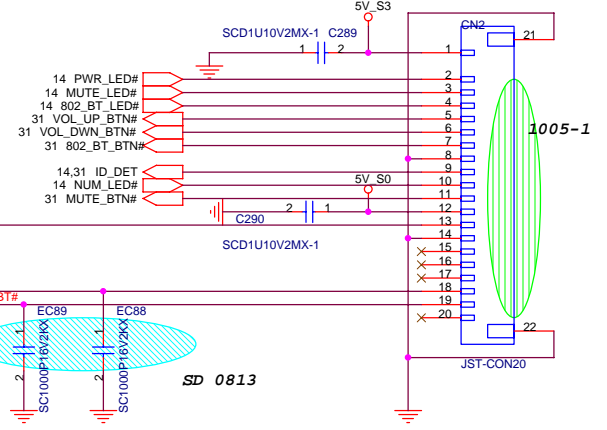
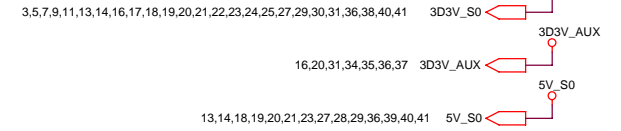
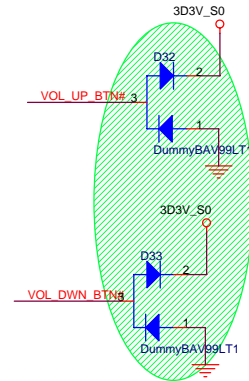
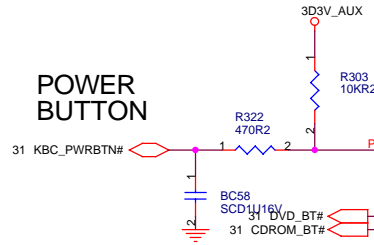
	NONE Quick Play	Quick Play
MATRIXID1#	0	1



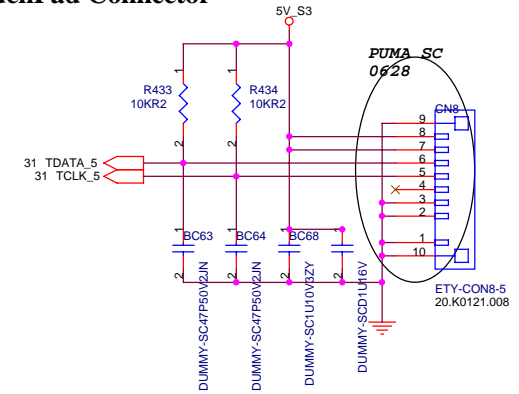
SB-32-01

LAUNCH Board

POWER BUTTON

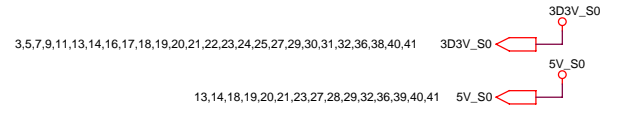


TouchPad Connector

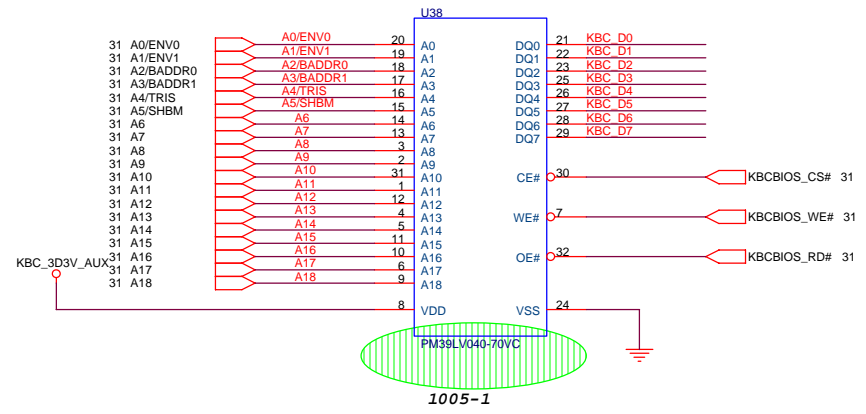


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Title		KEYBOARD/TOUCH PAD/Launch key	
Size	A3	Document Number	Leopard
Date:	Monday, February 28, 2005	Sheet	32 of 41



512KB Flash



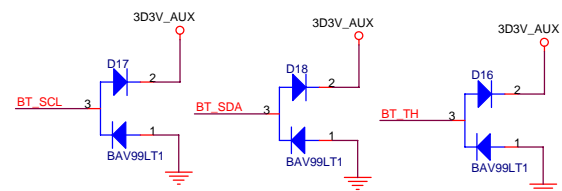
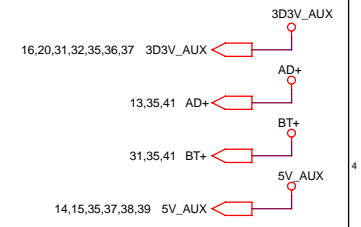
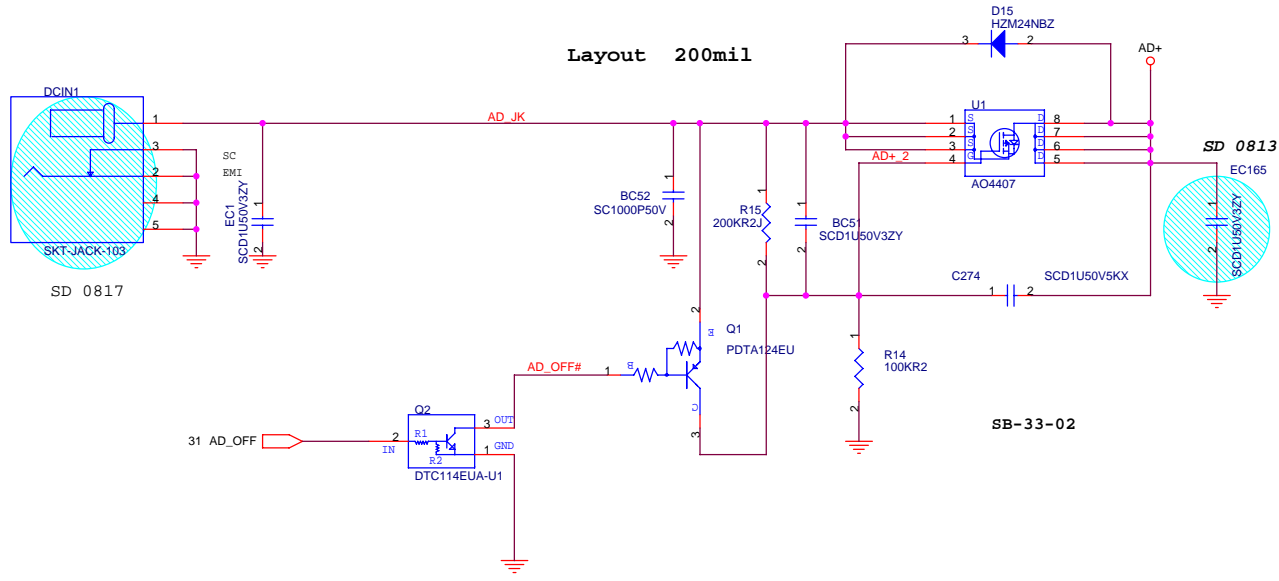
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 21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS/GF**

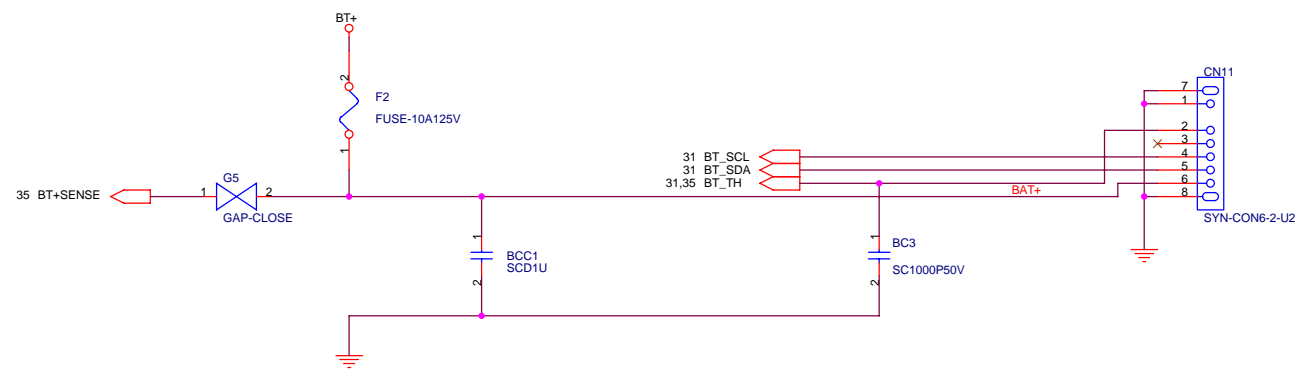
Size: A3 Document Number: **Leopard** Rev: **-4**

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Adaptor in to generate DCBATOUT

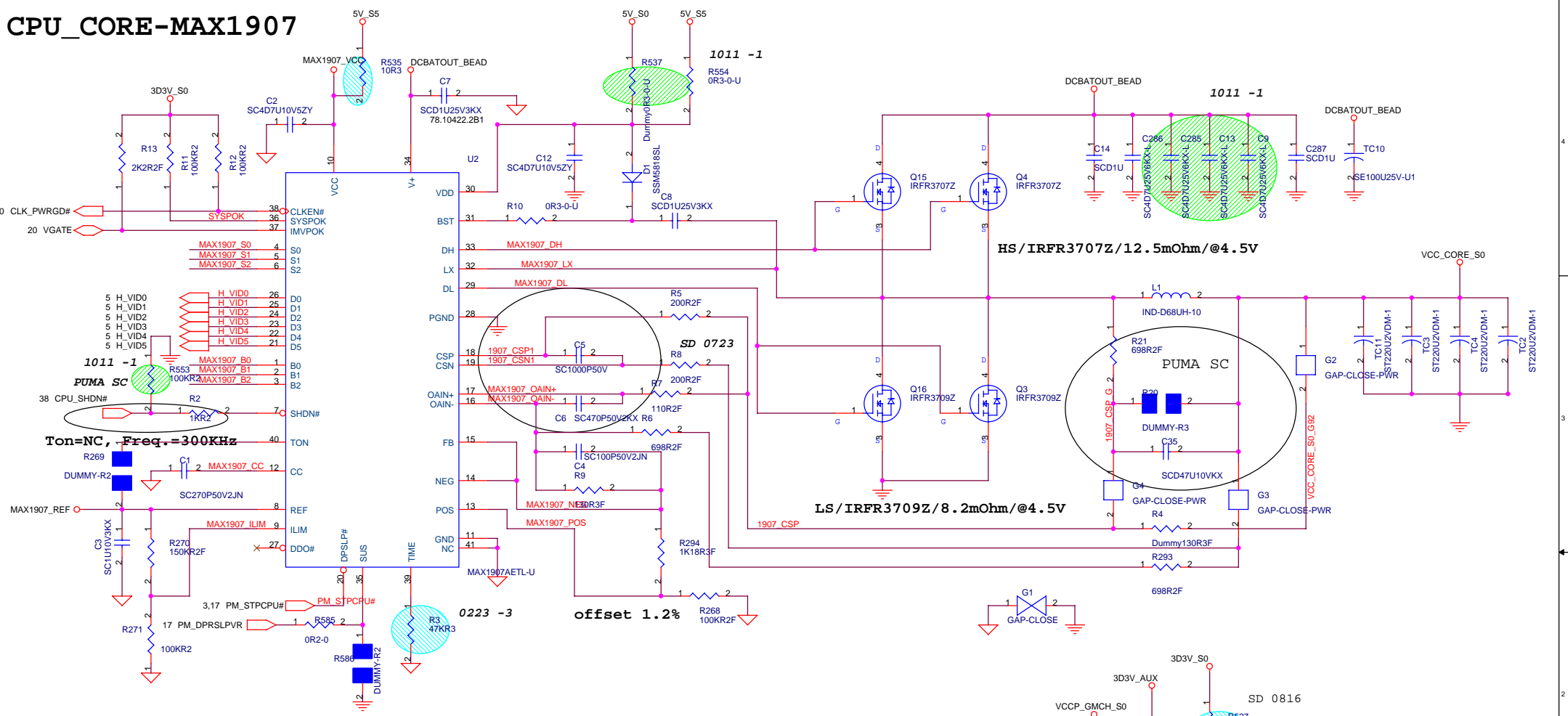


BATTERY CONNECTOR



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Adaptor/ Battery conn.	
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CPU_CORE-MAX1907



MAX1907_S0
MAX1907_S1
MAX1907_S2

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5

MAX1907_B0
MAX1907_B1
MAX1907_B2

Ton=NC, Freq.=300KHz

MAX1907_ILIM

MAX1907_REF

MAX1907_ILIM

MAX1907_ILIM

MAX1907_ILIM

MAX1907_ILIM

MAX1907_ILIM

MAX1907_ILIM

MAX1907_ILIM

MAX1907_ILIM

MAX1907_ILIM

MAX1907_ILIM

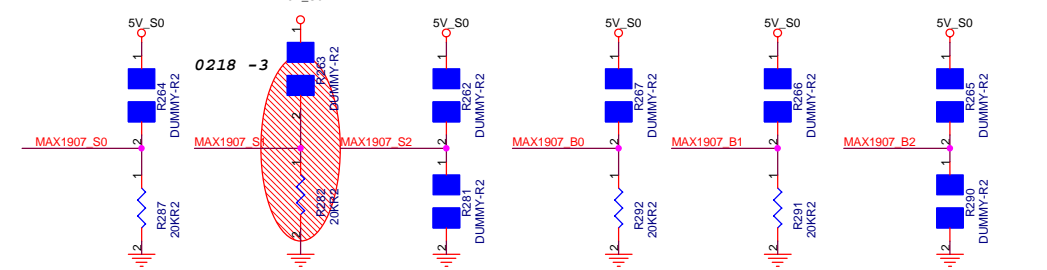
MAX1907_ILIM

MAX1907_ILIM

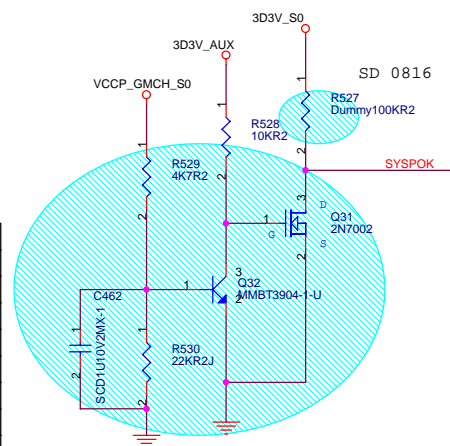
MAX1907_ILIM

OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



VID							Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V	
0	1	0	1	1	1	1.340	
0	1	1	0	0	0	1.324	
0	1	1	0	1	0	1.292	
0	1	1	1	0	0	1.260	
0	1	1	1	0	1	1.244	
0	1	1	1	1	1	1.212	
1	0	0	0	0	1	1.180	
1	0	0	0	1	1	1.148	
1	0	0	1	1	0	1.100	
1	0	1	0	0	1	1.052	
1	0	1	0	1	1	1.020	
1	0	1	1	1	0	0.972	
1	1	0	0	0	0	0.940	



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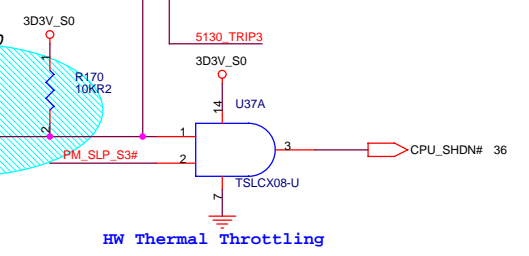
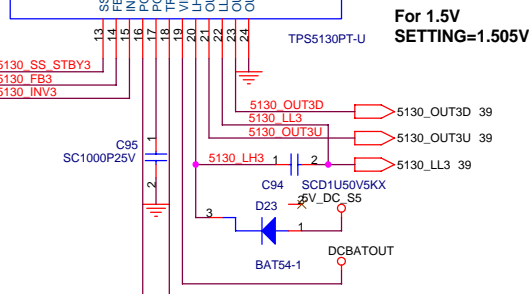
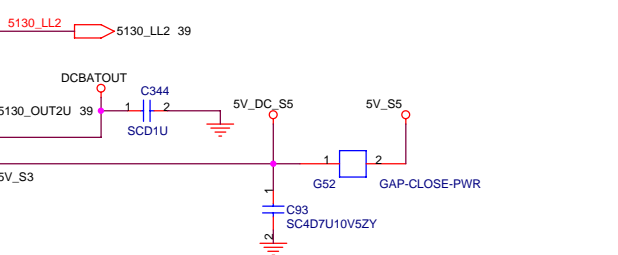
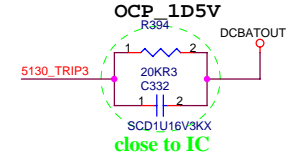
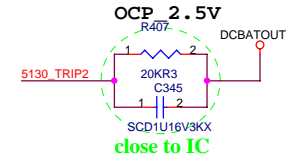
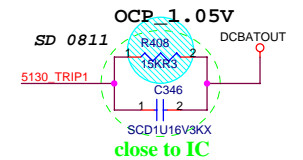
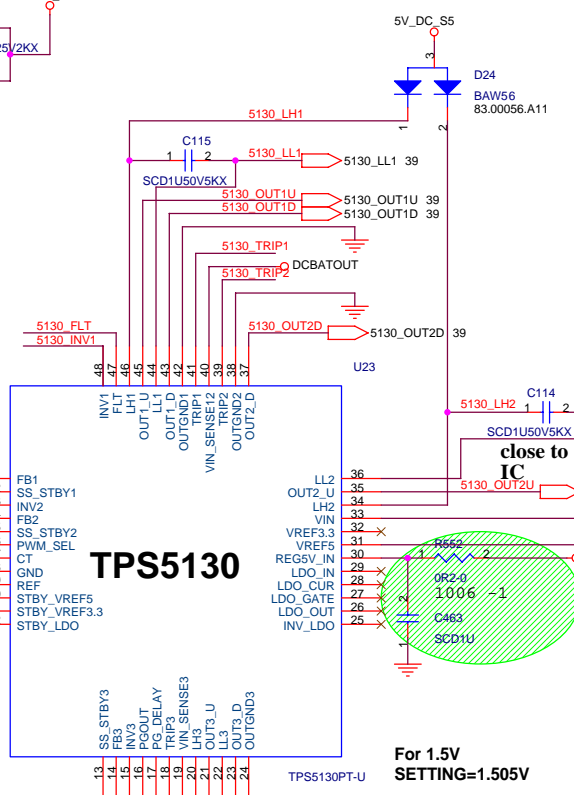
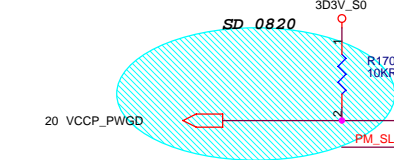
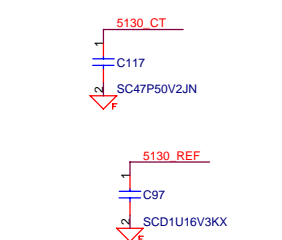
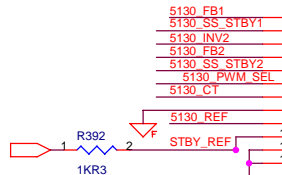
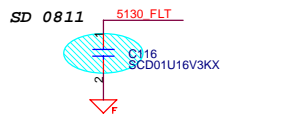
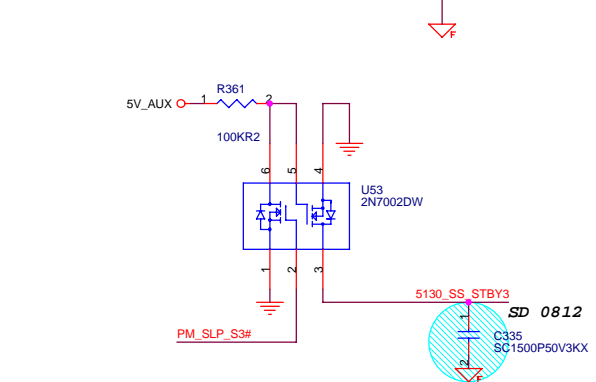
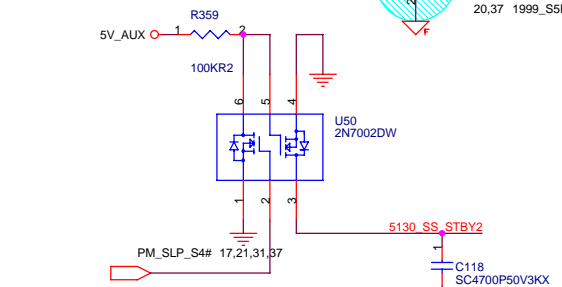
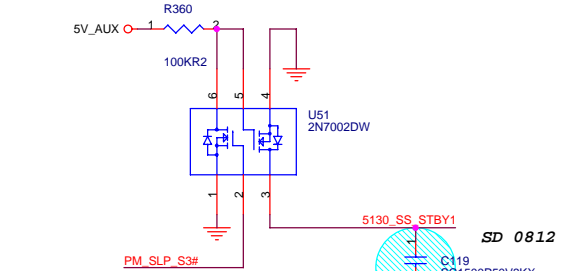
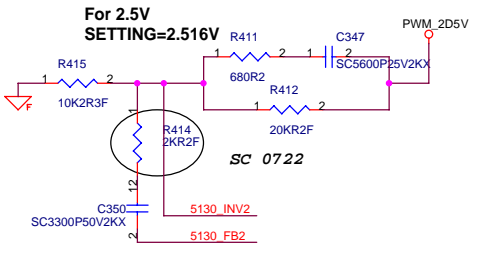
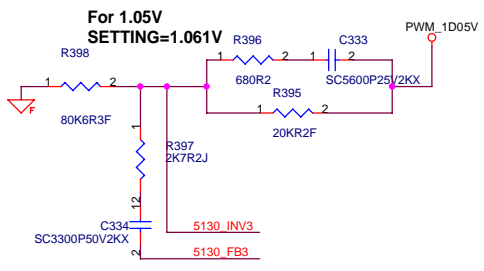
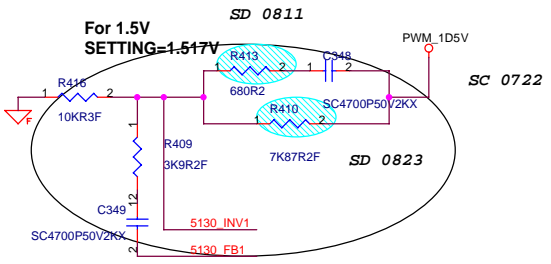
Title: **IMVP IV-CPU POWER-MAX1907**

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TI TPS5130 for 2.5V, 1.5V, 1.05V.

(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)

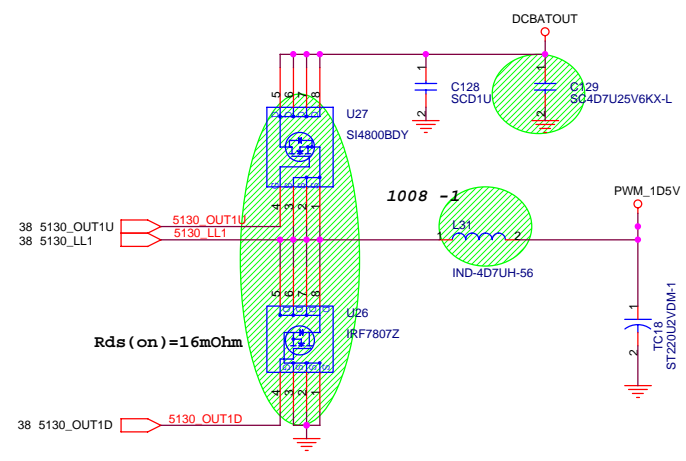


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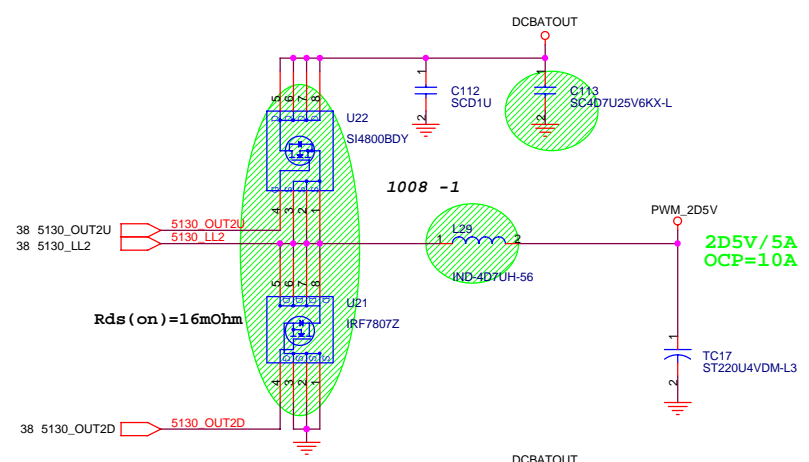
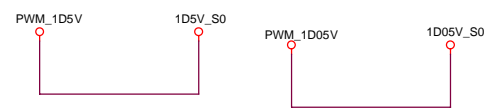
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Size	Document Number	Rev	
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TI TPS5130 for 2.5V, 1.5V, 1.05V

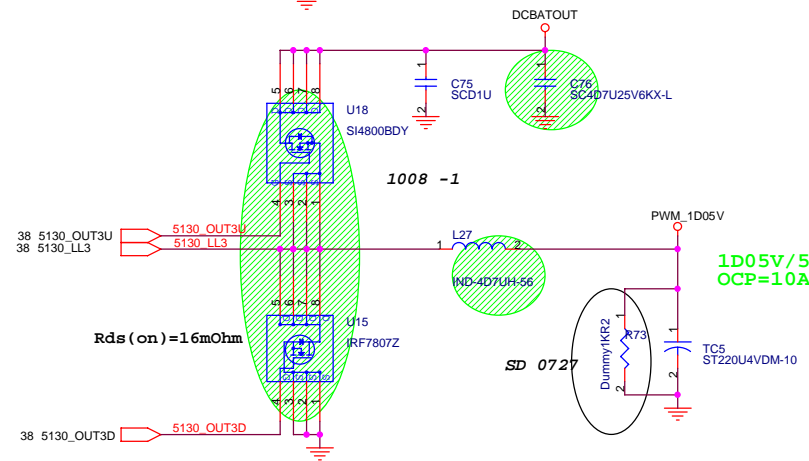
(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)



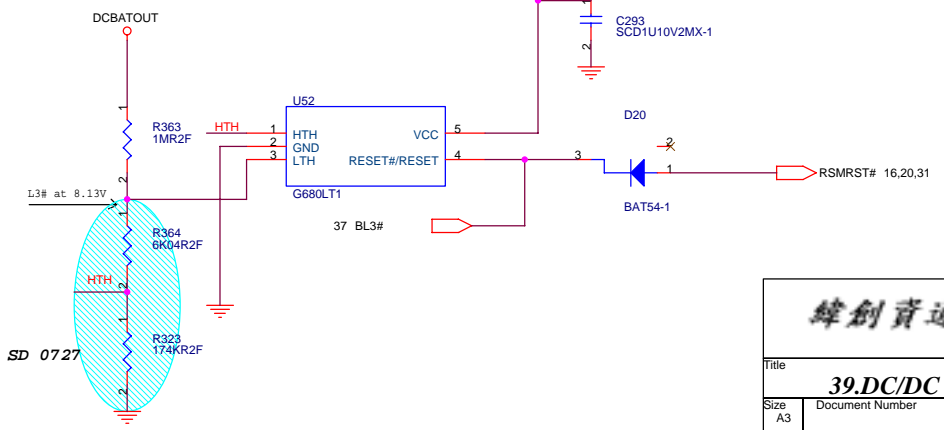
1D5V/5A
OCP=10A



2D5V/5A
OCP=10A

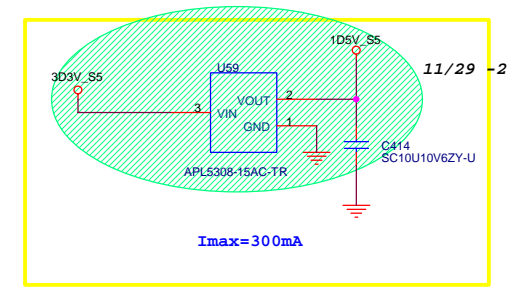


1D05V/5A
OCP=10A

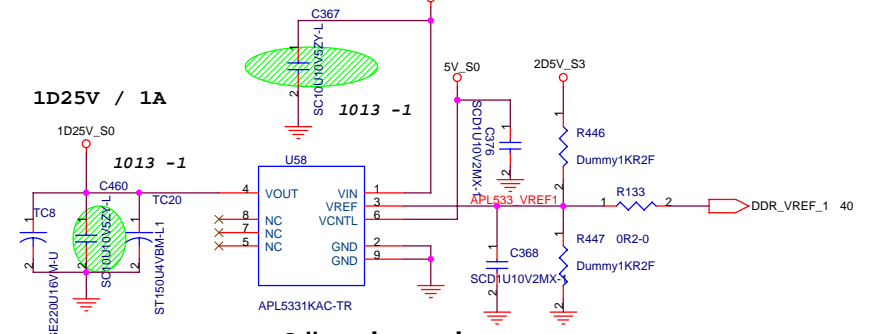


- 14,35,37,38,40,41 DCBATOUT
- 17,18,19,21,25,29,31,35,37,40 3D3V_S5
- 14,15,35,37,38 5V_AUX
- 18 1D5V_S5
- 7,9,10,11,12,38,40,41 2D5V_S3
- 13,14,18,19,20,21,23,27,28,29,32,36,40,41 5V_S0
- 12 1D25V_S0

1.5V_S5 (For ICH6)



Power budget: 1.25V/2.2Apeak (For DDR1_VTT)

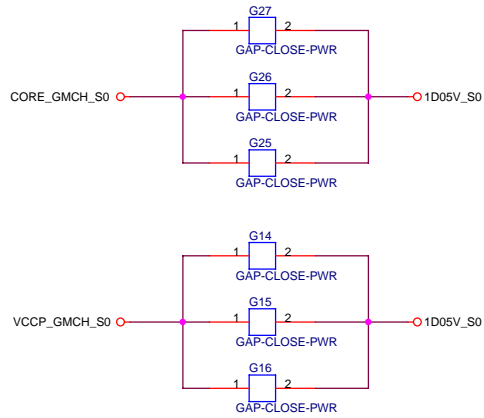


L3# circuit

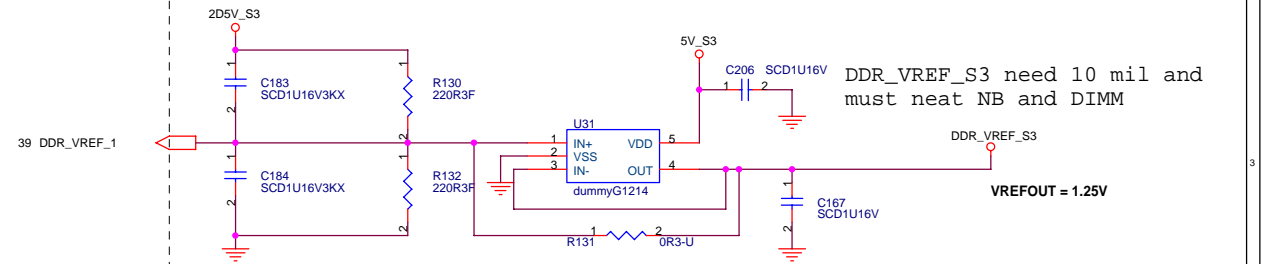
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Title		
39.DC/DC 2D5V/1D5V/1D05V-2		
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FOR GMCH Power



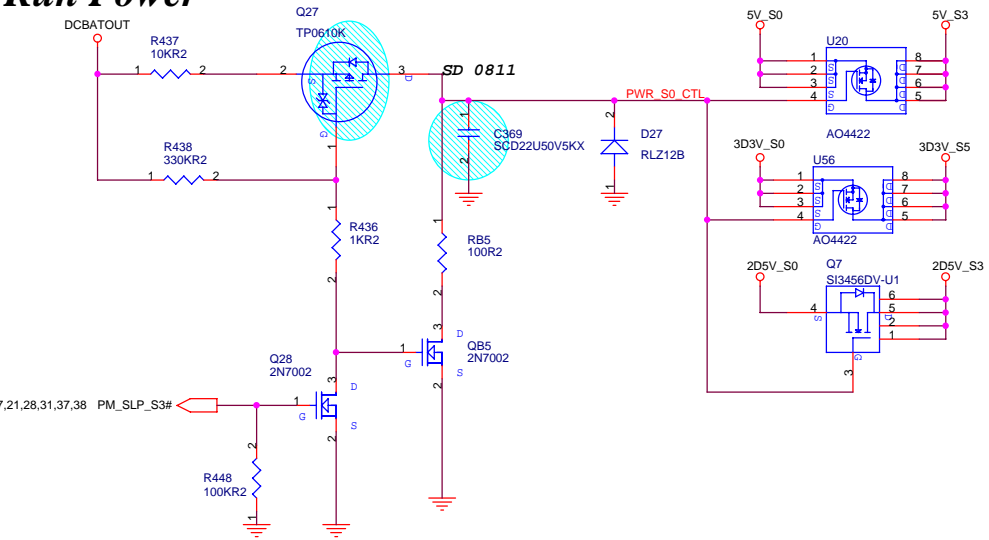
- 3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,41 3D3V_S0
- 13,14,30 3D3V_S3
- 17,18,19,21,25,29,31,35,37,39 3D3V_S5
- 13,14,18,19,20,21,23,27,28,29,32,36,39,41 5V_S0
- 13,14,26,30,32,37,38,41 5V_S3
- 14,18,20,36,38 5V_S5
- 7,9,15,18 2D5V_S0
- 7,9,10,11,12,38,39,41 2D5V_S3
- 7,11 DDR_VREF_S3
- 14,35,37,38,39,41 DCBATOUT
- 38,39,41 1D05V_S0
- 4,5,6,7,9,10,16,18,36,41 VCCP_GMCH_S0
- 6,9,10,41 CORE_GMCH_S0



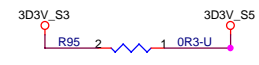
FOR DDR Power

Run Power

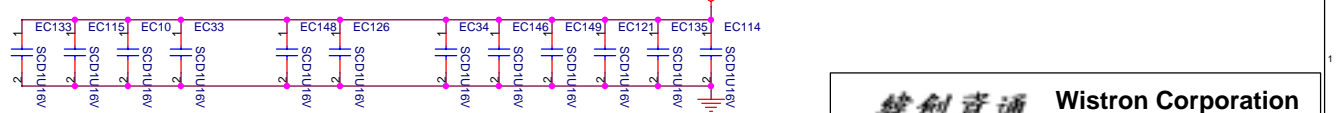
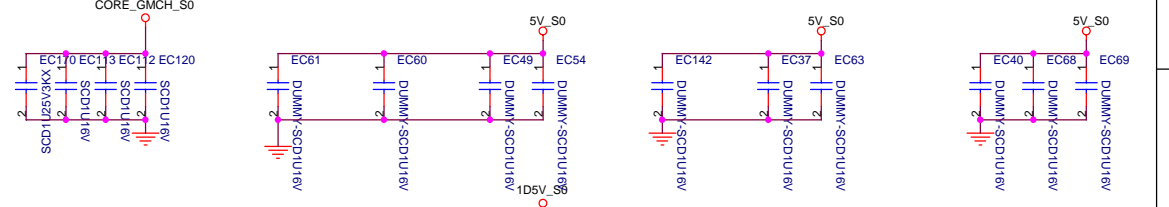
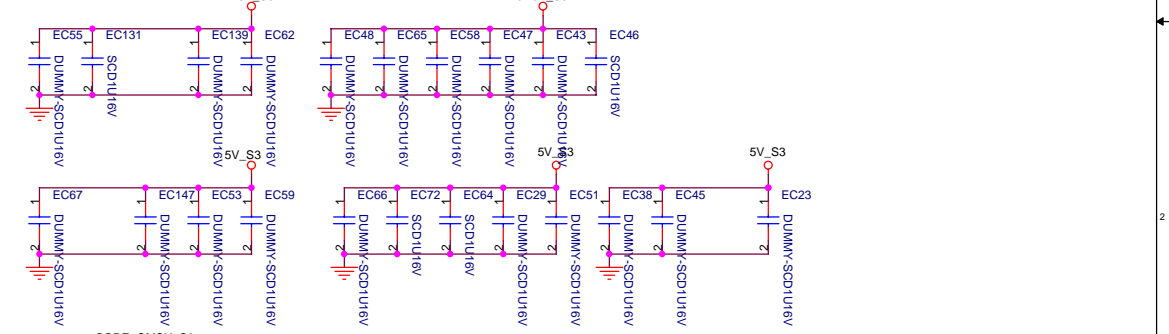
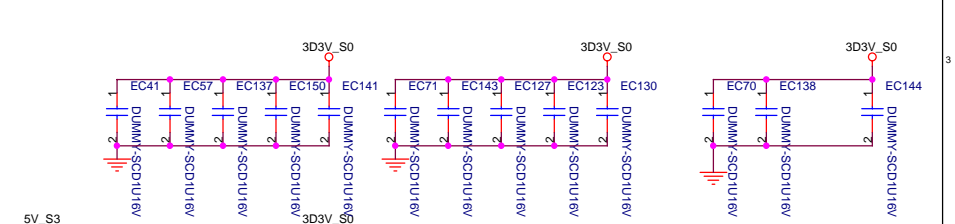
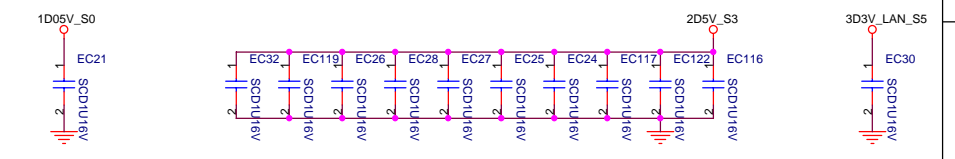
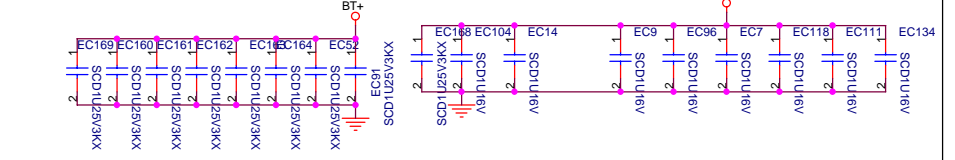
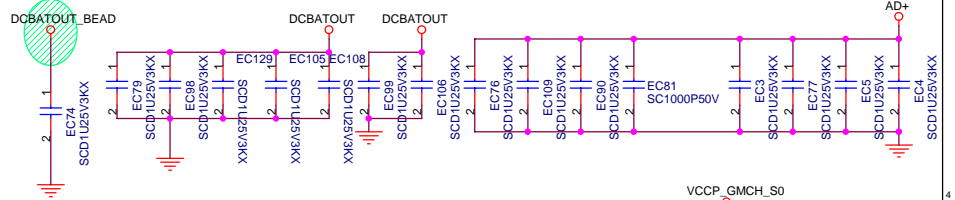
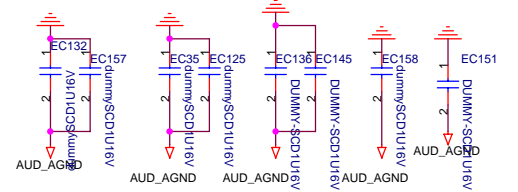
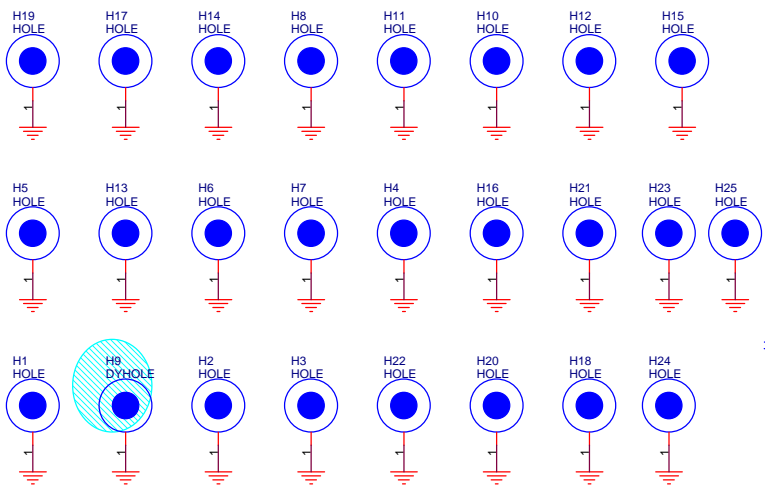
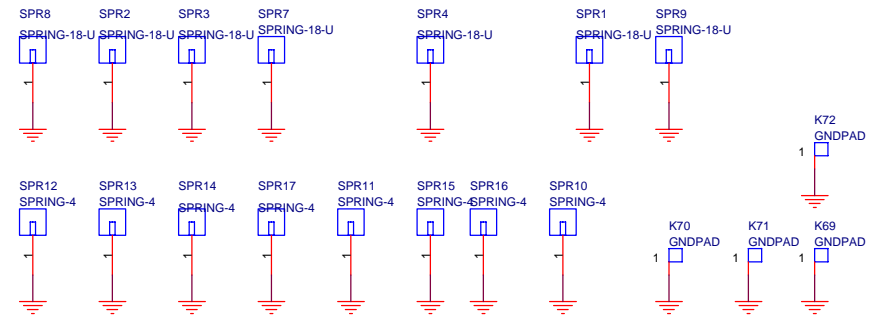
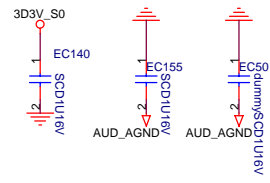
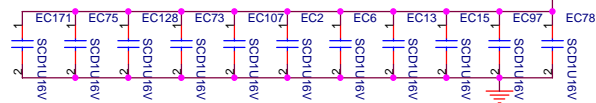
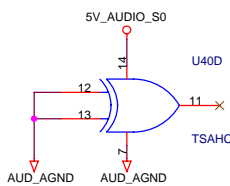
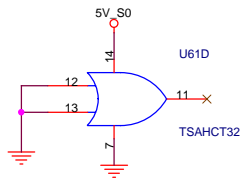
0223 -3



Suspend Power



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Title: PWRPLANE&RESETLOGIC	
Size: A3	Rev: -4
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MISC & EMI		
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