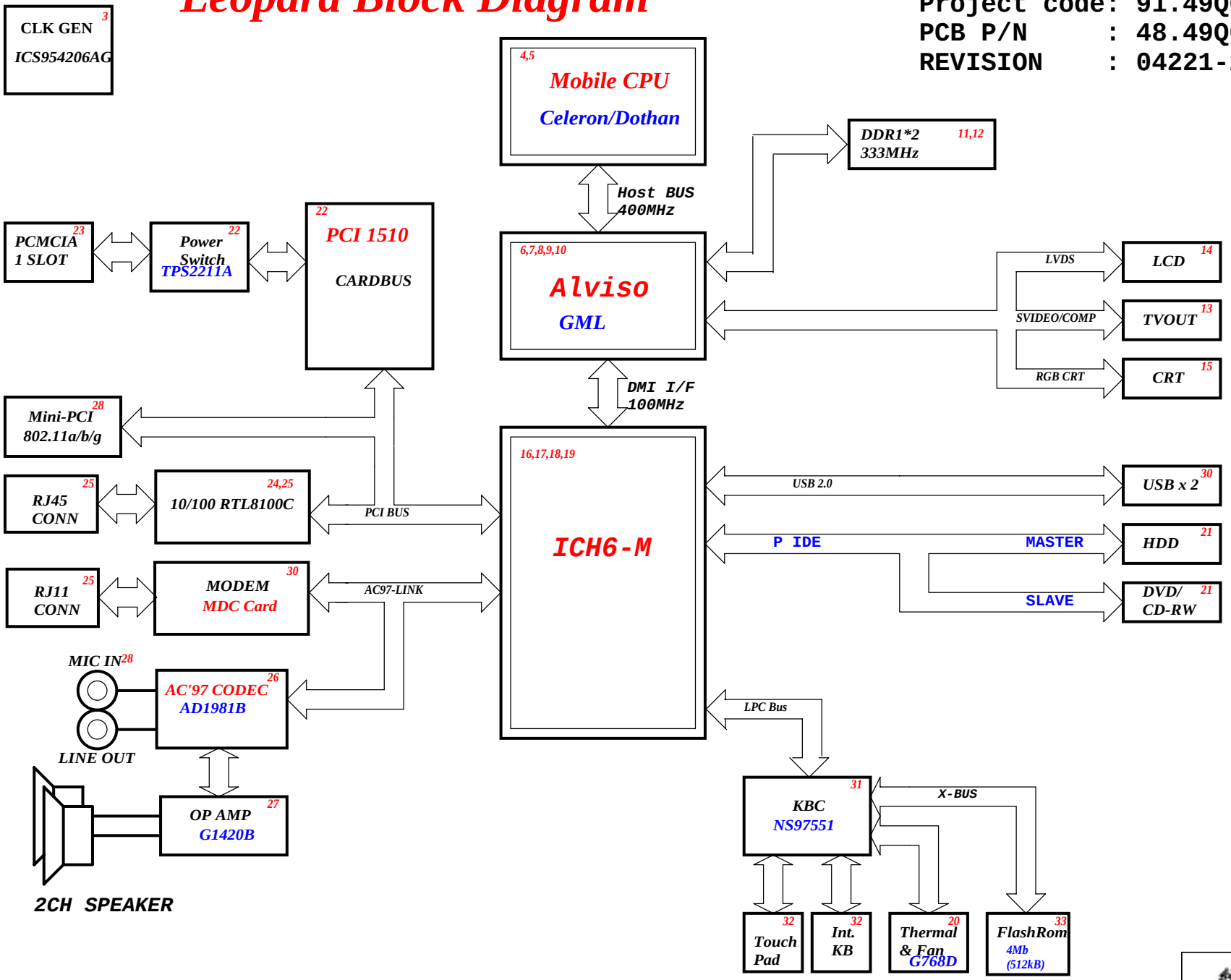
Leopard Block Diagram

Project code: 91.49Q01.001
PCB P/N : 48.49Q01.001
REVISION : 04221-2 DF



SYSTEM DC/DC 37 MAX1999	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC 38,39 TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 2D5V_S3

MAXIM CHARGER 35 MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC 36 MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

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Title: Block Diagram
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ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_2D5V= 2.5 Voltage power up on system work(S0 state)
2D5V_S3= 2.5 Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF_S3= 1.25 Voltage suspend to RAM(S3 state)
1D25V_S0= 1.25 Voltage power up on system work(S0 state)
1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

38,39,40,41 1D05V_S0 — 1D05V_S0
4,5,6,7,9,10,16,18,36,40,41 VCCP_GMCH_S0 — VCCP_GMCH_S0
6,9,10,40,41 CORE_GMCH_S0 — CORE_GMCH_S0
12,39 1D25V_S0 — 1D25V_S0
7,11,40 DDR_VREF_S3 — DDR_VREF_S3
5,7,9,17,18,38,39,41 1D5V_S0 — 1D5V_S0
18,39 1D5V_S5 — 1D5V_S5
5 1D5V_VCCA_S0 — 1D5V_VCCA_S0
4,5,36 VCC_CORE_S0 — VCC_CORE_S0
7,9,15,18,40 2D5V_S0 — 2D5V_S0
7,9,10,11,12,38,39,40,41 2D5V_S3 — 2D5V_S3
3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0 — 3D3V_S0
28,30,40 3D3V_S3 — 3D3V_S3
17,18,19,24,29,31,35,37,39,40 3D3V_S5 — 3D3V_S5
24,41 3D3V_LAN_S5 — 3D3V_LAN_S5
16,20,31,32,34,35,36,37 3D3V_AUX — 3D3V_AUX
27 5VA_OP_S0 — 5VA_OP_S0
14,15,18,19,20,21,22,26,27,29,32,36,39,40,41 5V_S0 — 5V_S0
14,25,30,32,37,38,40,41 5V_S3 — 5V_S3
14,18,20,36,38 5V_S5 — 5V_S5
14,35,37,38,39 5V_AUX — 5V_AUX
14,35,37,38,39,40,41 DCBATOUT — DCBATOUT
34,35,41 AD+ — AD+
31,34,35,41 BT+ — BT+

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0#/GNT0#
Cardbus Controller TI PCI1510	AD22	(CARBUS)P_INTG#	REQ1#/GNT1#
LAN	AD23	P_INTE#	REQ2#/GNT2#

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Title: ITP
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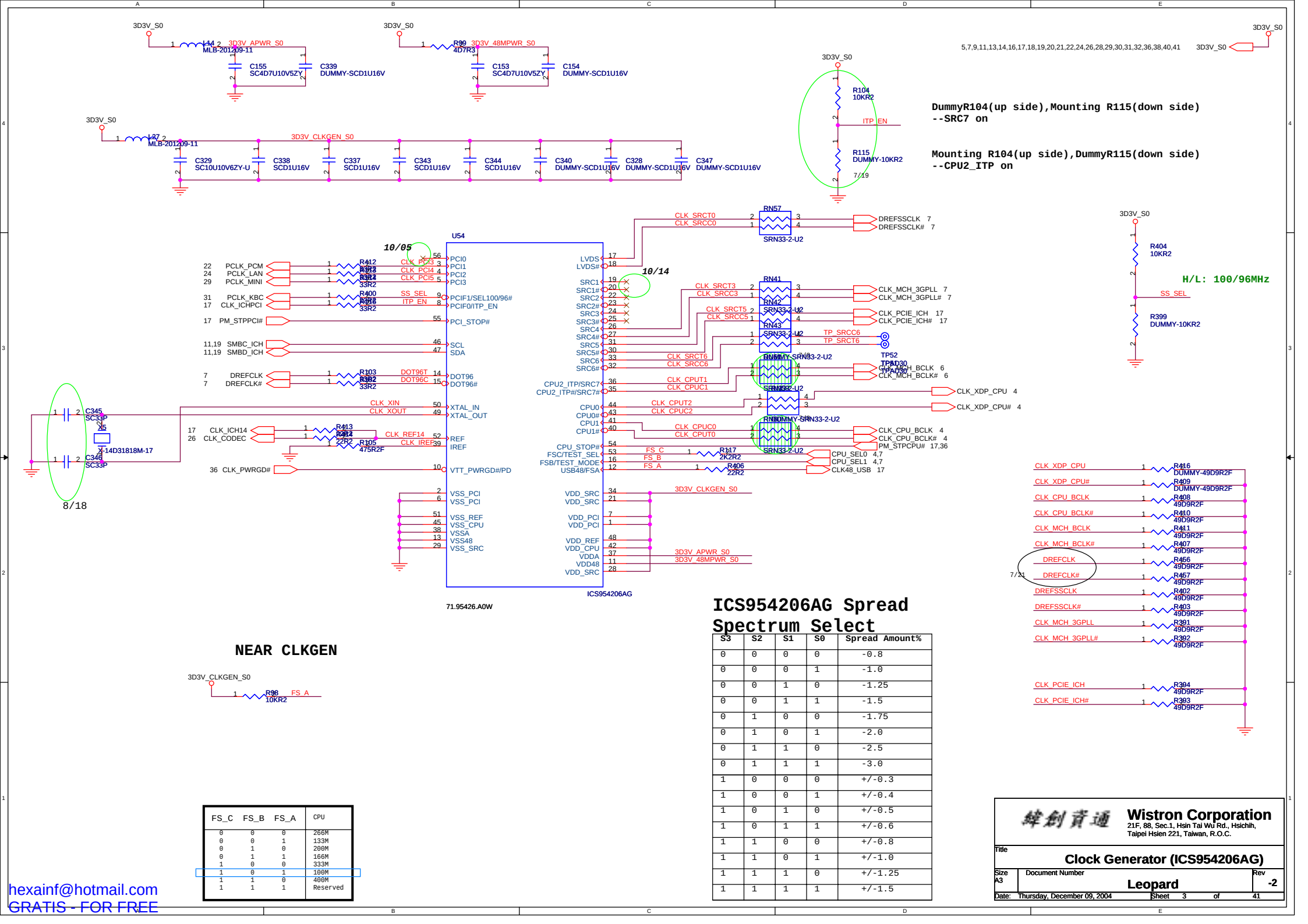
Date: Thursday, December 09, 2004 | Sheet 2 of 41



ICS954206AG Spread Spectrum Select

S3	S2	S1	S0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+/-0.3
1	0	0	1	+/-0.4
1	0	1	0	+/-0.5
1	0	1	1	+/-0.6
1	1	0	0	+/-0.8
1	1	0	1	+/-1.0
1	1	1	0	+/-1.25
1	1	1	1	+/-1.5

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

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Title: Clock Generator (ICS954206AG)

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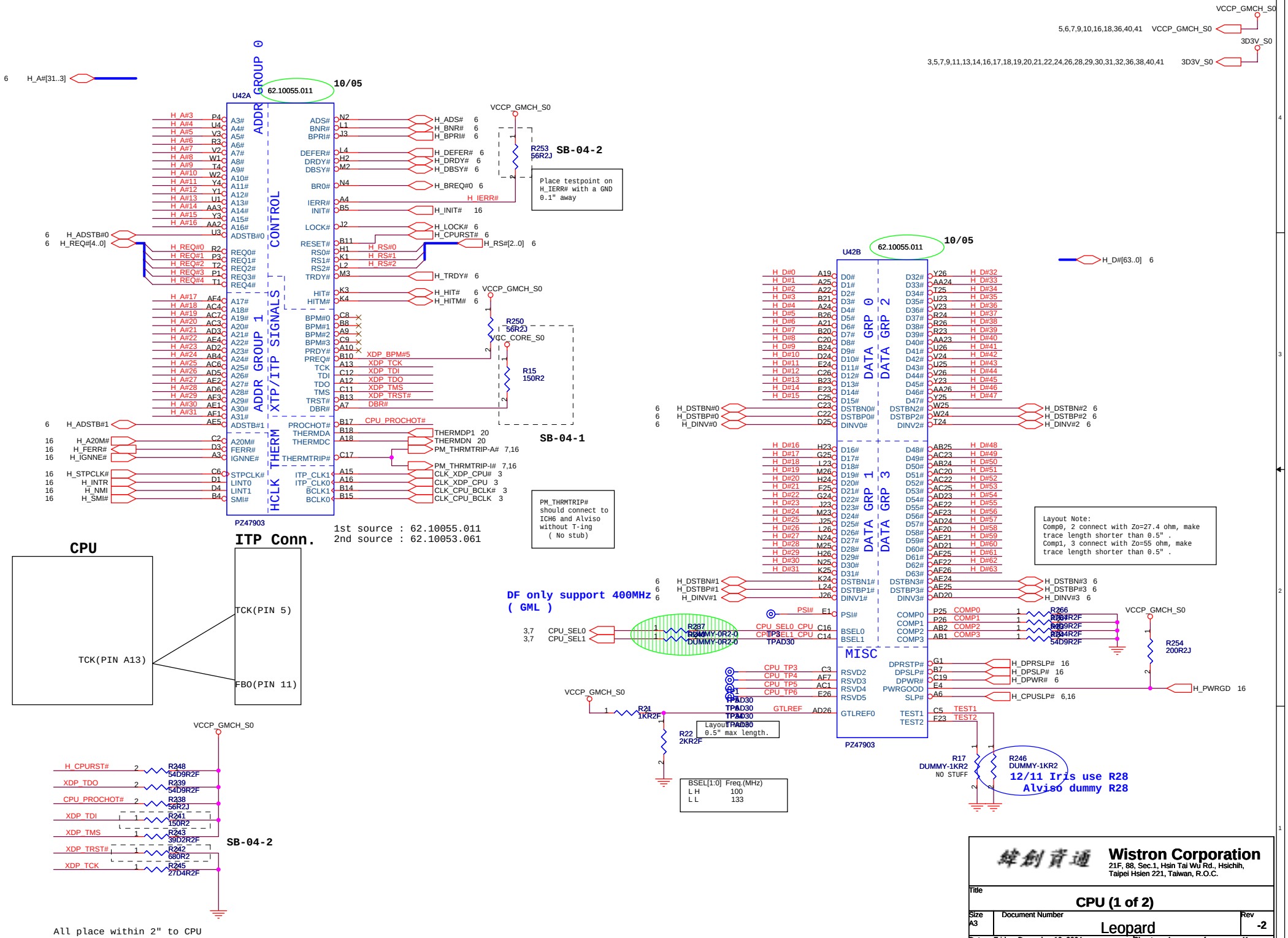

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Title: CPU (1 of 2)

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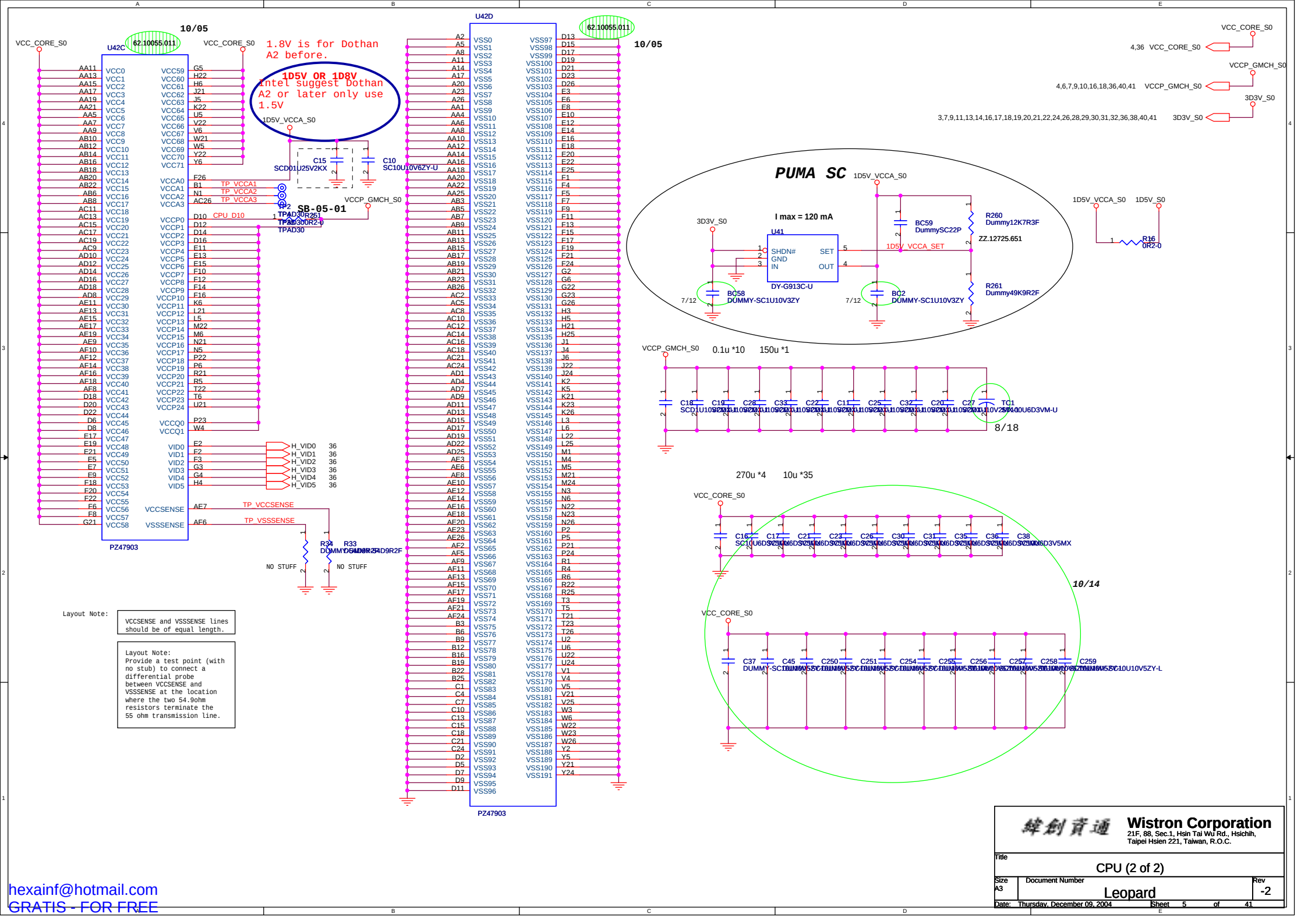


12/12 Trace 10 mil wide with 20 mil spacing

H_XRCOMP — R61 24D9R2F — 2

H_YRCOMP — R80 24D9R2F — 2

VCCP_GMCH_S0 — R63 54D9R2F — H_XSCOMP

VCCP_GMCH_S0 — R81 54D9R2F — H_YSCOMP

VCCP_GMCH_S0 — R60 221R3F — H_XSWING — R62 100R2F — C76 SCD1U16V

VCCP_GMCH_S0 — R78 221R3F — H_YSWING — R79 100R2F — C94 SCD1U16V

12/12 Trace 10 mil wide with 20 mil spacing

Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

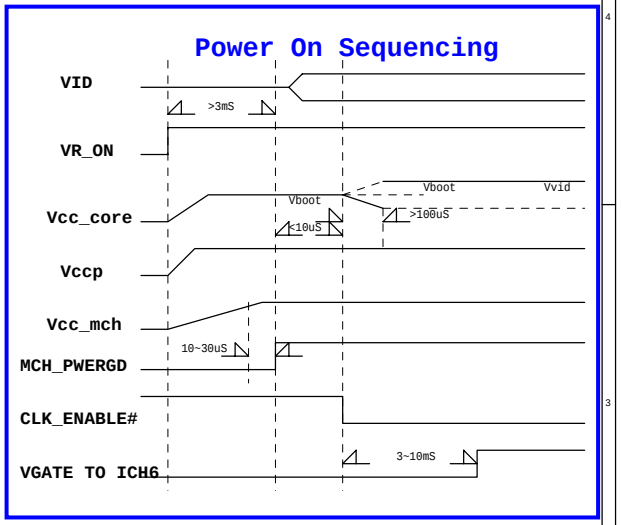
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 **101 = FSB400** others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	Reserved	0 = DDR2 **1 = DDR1 (Default)**
CFG7	CPU Strap	0 = Reserved **1 = Dothan (Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes **1 = Normal (Default)**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation (Default)**
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Reversed	
CFG18	GMCH core VCC Select	**0 = 1.05V (Default)** 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V (Default)** 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present(Default)** 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

CORE_GMCH_S0
9,10,40,41 CORE_GMCH_S0

VCCP_GMCH_S0
4,5,7,9,10,16,18,36,40,41 VCCP_GMCH_S0

Power On Sequencing



4 H_D#[63..0]

U17A

HOST

H_D#0	E4	HD0#	HA3#	G9	H_A#3
H_D#1	E1	HD1#	HA4#	C9	H_A#4
H_D#2	F4	HD2#	HA5#	E9	H_A#5
H_D#3	H7	HD3#	HA6#	B7	H_A#6
H_D#4	E2	HD4#	HA7#	A10	H_A#7
H_D#5	F1	HD5#	HA8#	F9	H_A#8
H_D#6	E3	HD6#	HA9#	D8	H_A#9
H_D#7	D3	HD7#	HA10#	B10	H_A#10
H_D#8	K7	HD8#	HA11#	E10	H_A#11
H_D#9	F2	HD9#	HA12#	G10	H_A#12
H_D#10	J7	HD10#	HA13#	D9	H_A#13
H_D#11	J8	HD11#	HA14#	E11	H_A#14
H_D#12	H6	HD12#	HA15#	F10	H_A#15
H_D#13	F3	HD13#	HA16#	G11	H_A#16
H_D#14	K8	HD14#	HA17#	G13	H_A#17
H_D#15	H5	HD15#	HA18#	C10	H_A#18
H_D#16	H1	HD16#	HA19#	C11	H_A#19
H_D#17	H2	HD17#	HA20#	D11	H_A#20
H_D#18	K5	HD18#	HA21#	C12	H_A#21
H_D#19	K6	HD19#	HA22#	B13	H_A#22
H_D#20	J4	HD20#	HA23#	A12	H_A#23
H_D#21	G3	HD21#	HA24#	E12	H_A#24
H_D#22	H3	HD22#	HA25#	G12	H_A#25
H_D#23	J1	HD23#	HA26#	E12	H_A#26
H_D#24	L5	HD24#	HA27#	C13	H_A#27
H_D#25	K4	HD25#	HA28#	B11	H_A#28
H_D#26	J5	HD26#	HA29#	D13	H_A#29
H_D#27	P7	HD27#	HA30#	A13	H_A#30
H_D#28	L7	HD28#	HA31#	F13	H_A#31
H_D#29	J3	HD29#			
H_D#30	P5	HD30#			
H_D#31	L3	HD31#			
H_D#32	U7	HD32#			
H_D#33	V6	HD33#			
H_D#34	R6	HD34#			
H_D#35	R5	HD35#			
H_D#36	P3	HD36#			
H_D#37	T8	HD37#			
H_D#38	R7	HD38#			
H_D#39	R8	HD39#			
H_D#40	U8	HD40#			
H_D#41	R4	HD41#			
H_D#42	T4	HD42#			
H_D#43	T5	HD43#			
H_D#44	R1	HD44#			
H_D#45	T3	HD45#			
H_D#46	V8	HD46#			
H_D#47	U6	HD47#			
H_D#48	W6	HD48#			
H_D#49	U3	HD49#			
H_D#50	V5	HD50#			
H_D#51	W8	HD51#			
H_D#52	W7	HD52#			
H_D#53	U2	HD53#			
H_D#54	U1	HD54#			
H_D#55	Y5	HD55#			
H_D#56	Y2	HD56#			
H_D#57	V4	HD57#			
H_D#58	Y7	HD58#			
H_D#59	W1	HD59#			
H_D#60	W3	HD60#			
H_D#61	Y3	HD61#			
H_D#62	Y6	HD62#			
H_D#63	W2	HD63#			

H_XRCOMP	C1	HXRCOMP	HADS#	F8	H_ADS# 4
H_XSCOMP	C2	HXSCOMP	HADSTB#0	B9	H_ADSTB#0 4
H_XSWING	D1	HXSWING	HADSTB#1	E13	H_ADSTB#1 4
H_YRCOMP	T1	HYRCOMP	HVREF	J11	H_VREF
H_YSCOMP	L1	HYSCOMP	HBNR#	A5	H_BNR# 4
H_YSWING	P1	HYSWING	HBPRI#	D5	H_BPRI# 4
			HBREQ0#	E7	H_BREQ#0 4
			HCPURST#	H10	H_CPURST# 4
			HCLKINN	AB1	CLK_MCH_BCLK# 3
			HCLKINP	AB2	CLK_MCH_BCLK 3
			HDBSY#	C6	H_DBSY# 4
			HDEFER#	E6	H_DEFER# 4
			HDINV#0	H8	H_DINV#0
			HDINV#1	K3	H_DINV#1
			HDINV#2	T7	H_DINV#2
			HDINV#3	U5	H_DINV#3
			HDPWR#	G6	H_DPWR# 4
			HDRDY#	E7	H_DRDY# 4
			HDSTBN#0	G4	H_DSTBN#0
			HDSTBN#1	K1	H_DSTBN#1
			HDSTBN#2	R3	H_DSTBN#2
			HDSTBN#3	V3	H_DSTBN#3
			HDSTBP#0	G5	H_DSTBP#0
			HDSTBP#1	K2	H_DSTBP#1
			HDSTBP#2	R2	H_DSTBP#2
			HDSTBP#3	W4	H_DSTBP#3
			HEDRDY#	E6	TP_H_EDRDY#
			HHIT#	D4	H_HIT# 4
			HHITM#	D6	H_HITM# 4
			HLOCK#	B3	H_LOCK# 4
			HPCREQ#	A11	TP_H_PCREQ#
			HREQ#0	A7	H_REQ#0
			HREQ#1	D7	H_REQ#1
			HREQ#2	B8	H_REQ#2
			HREQ#3	C7	H_REQ#3
			HREQ#4	A8	H_REQ#4
			HRS0#	A4	H_RS#0
			HRS1#	B4	H_RS#1
			HRS2#	G8	H_RS#2
			HCPUSLP#	B5	H_CPUSLP# GMCH
			HTRDY#		H_TRDY# 4

71.0GMCH.AJU

H_A#[31..3] 4

H_DINV#[3..0] 4

H_DSTBN#[3..0] 4

H_DSTBP#[3..0] 4

H_REQ#[4..0] 4

H_RS#[2..0] 4

H_CPUSLP# 4,16

VCCP_GMCH_S0 — R297 100R2F — H_VREF — C281 SCD1U16V — R298 100R2F

2/10 HM1-SC Intel Sightings issue 54489

CORE_GMCH_S0 — R347 DUMMY-0R2-0 — H_DPWR#

TP37 TPAD30

TP9 TPAD30

PUMA SC

R296 0R2-0

For Banias/Celeron-M:R1079=DUMMY
For Dothan A:R1079=DUMMY
For Dothan B:R1079=0R

ALVISO-GM:71.0GMCH.08U
ALVISO-PM:71.0GMCH.0BU
ALVISO-GML:71.0GMCH.0JU

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Title: GMCH (1 of 5)

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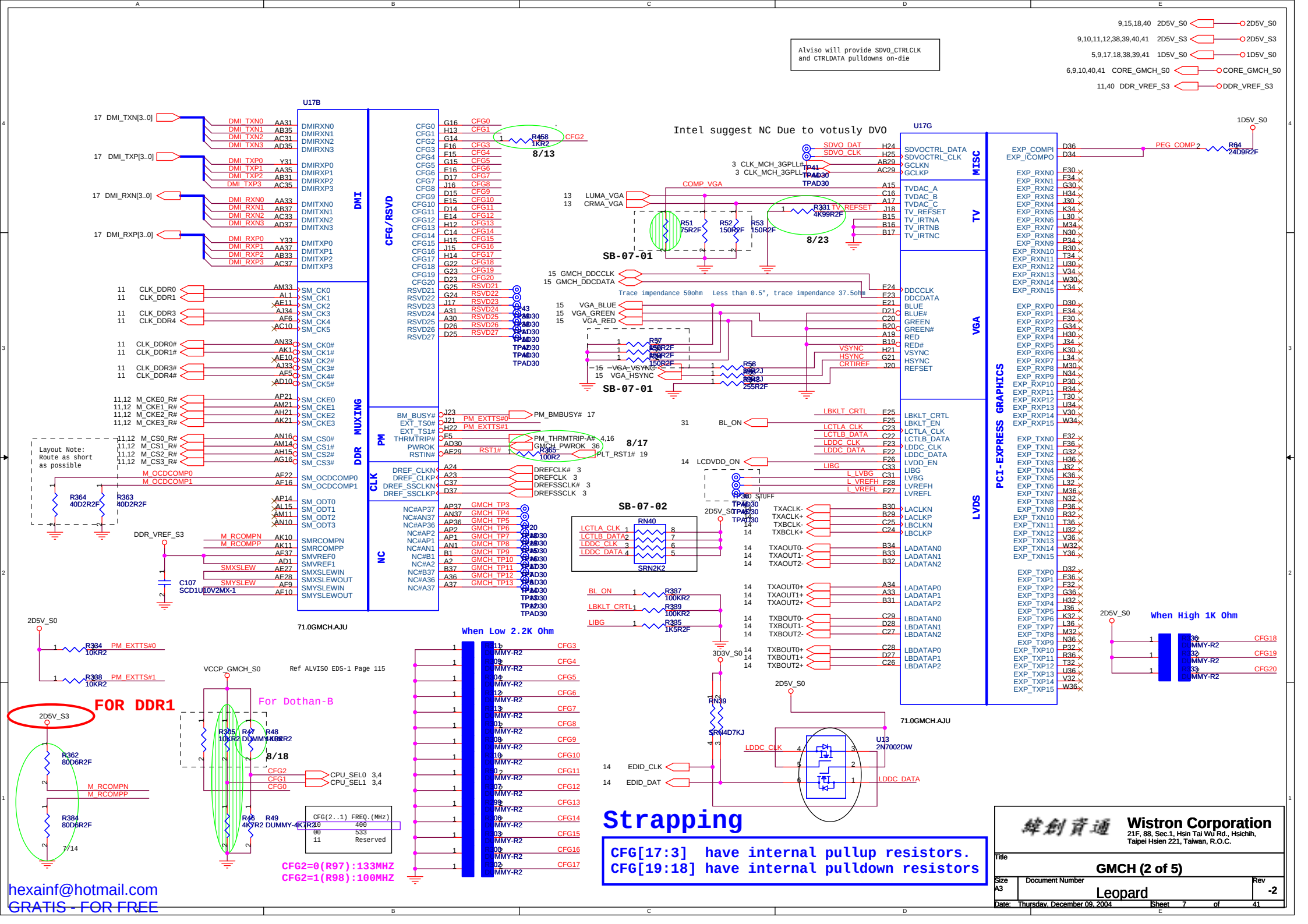
9,15,18,40 2D5V_S0 2D5V_S0
9,10,11,12,38,39,40,41 2D5V_S3 2D5V_S3
5,9,17,18,38,39,41 1D5V_S0 1D5V_S0
6,9,10,40,41 CORE_GMCH_S0 CORE_GMCH_S0
11,40 DDR_VREF_S3 DDR_VREF_S3
Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die
U17B
DMI
CFG/RSVD
DDR MUXING
PM
CLK
NC
U17G
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
Intel suggest NC Due to votusly DVO
SB-07-01
SB-07-02
8/13
8/17
8/18
8/23
Layout Note: Route as short as possible
FOR DDR1
For Dothan-B
When Low 2.2K Ohm
When High 1K Ohm
Ref ALVISO EDS-1 Page 115
71.0GMCH.AJU
CFG(2..1) FREQ.(MHz)
00 400
01 533
11 Reserved
CFG2=0(R97):133MHZ
CFG2=1(R98):100MHZ
Strapping
CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors
hexainf@hotmail.com
GRATIS - FOR FREE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (2 of 5)
Size A3
Document Number Leopard
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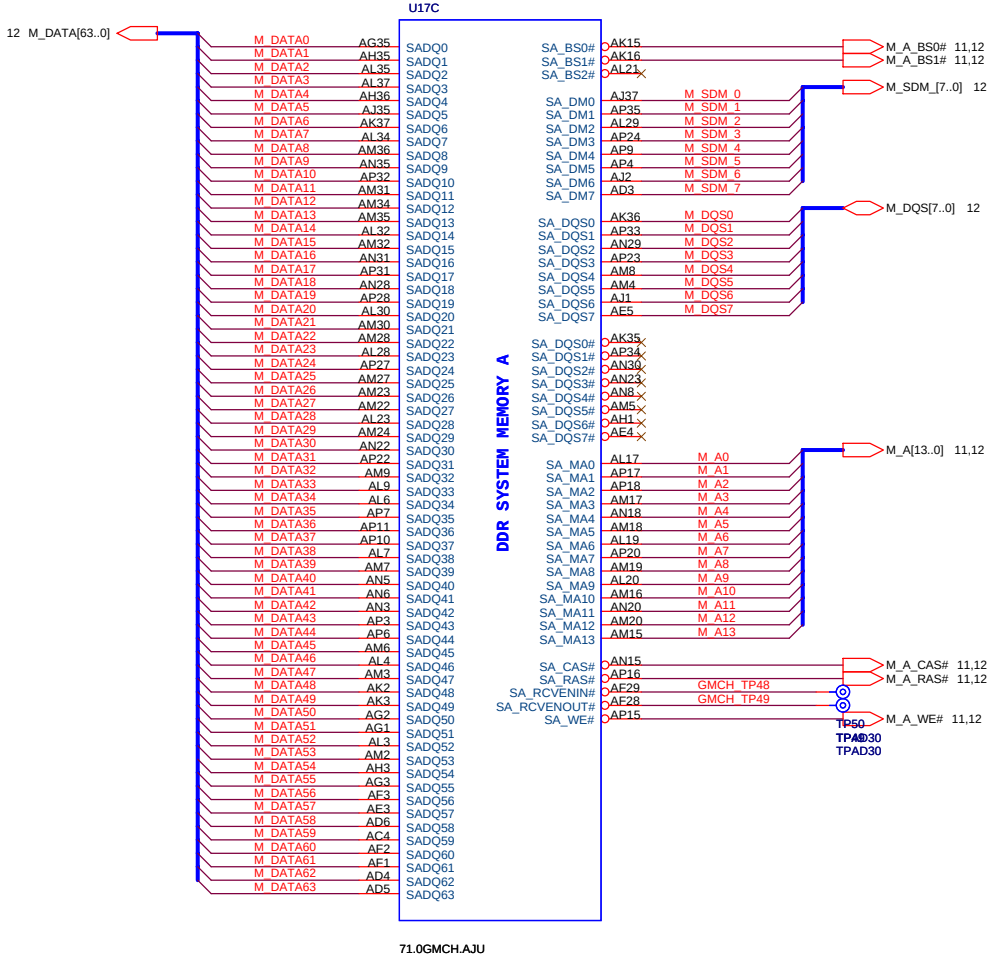
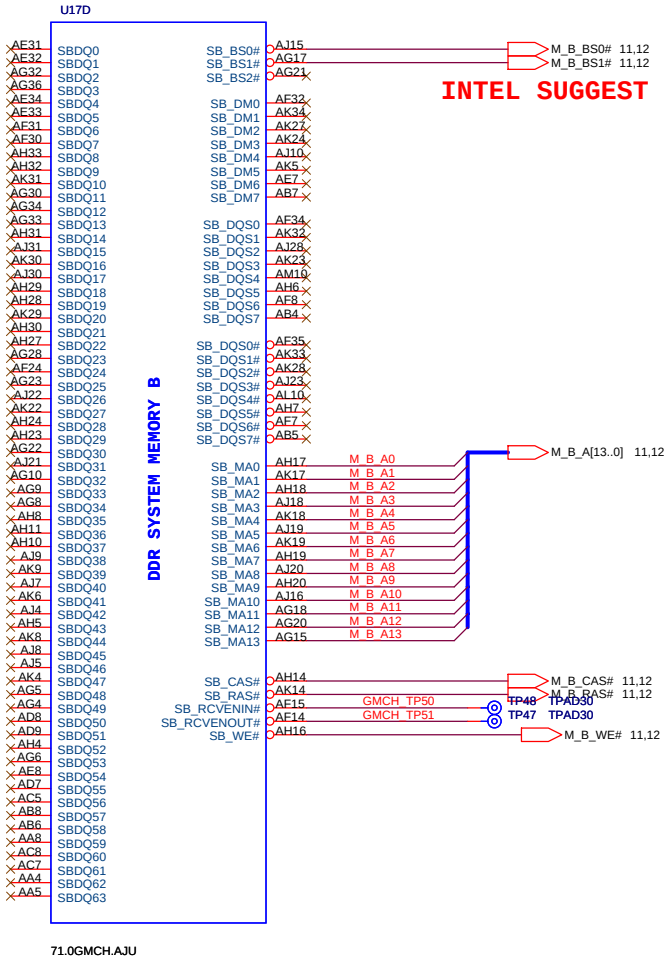
SUPPORT DDR333 ONLY





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Title	GMCH (3 of 5)	
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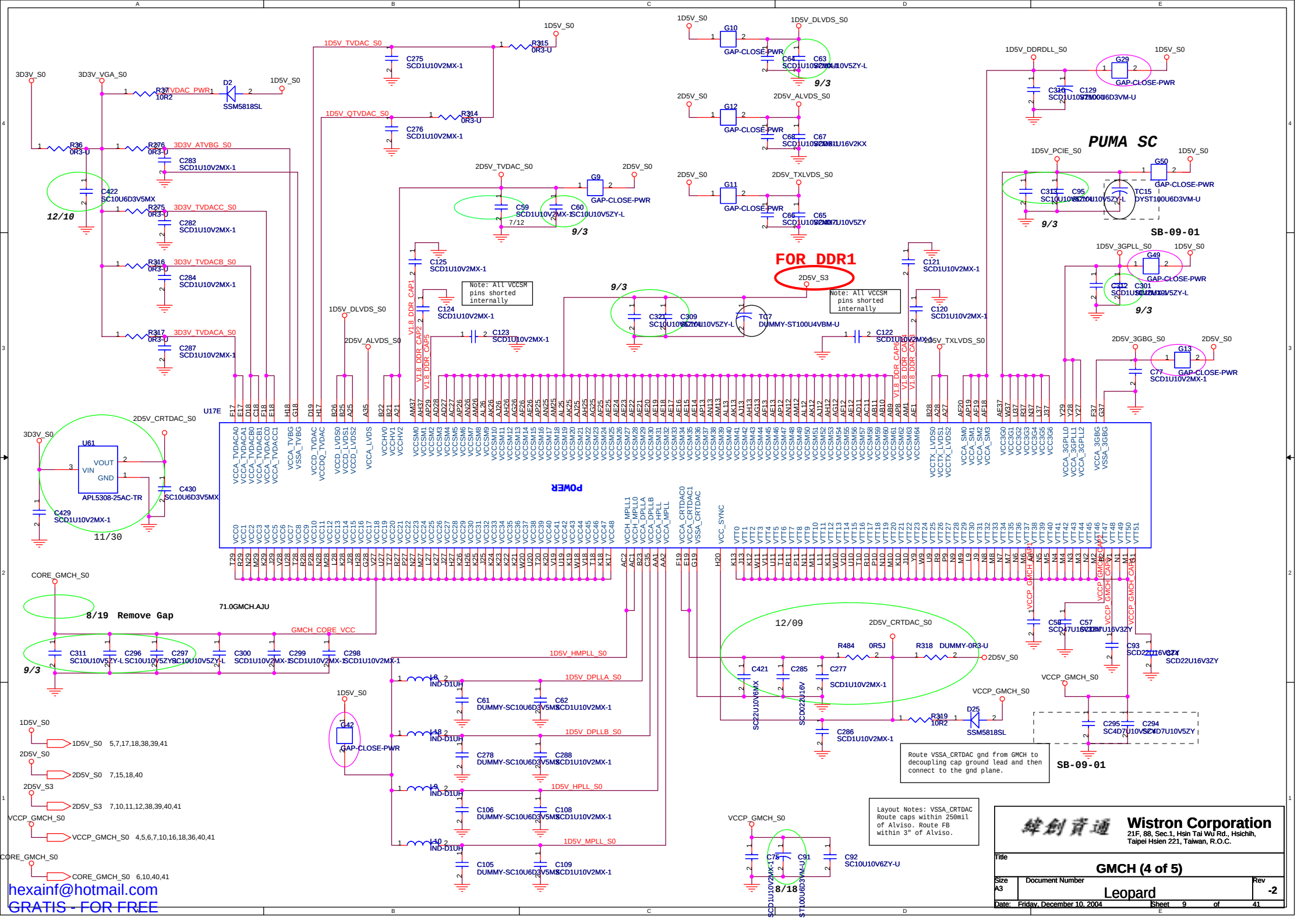
PUMA SC
SB-09-01
FOR DDR1
2D5V_S3
Note: All VCCSM pins shorted internally
POWER
U17E
U61
APL5308-25AC-TR
71.0GMCH.AJU
8/19 Remove Gap
12/09
11/30
12/10
9/3
8/18
Route VSSA_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.
Layout Notes: VSSA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Wistron Corporation
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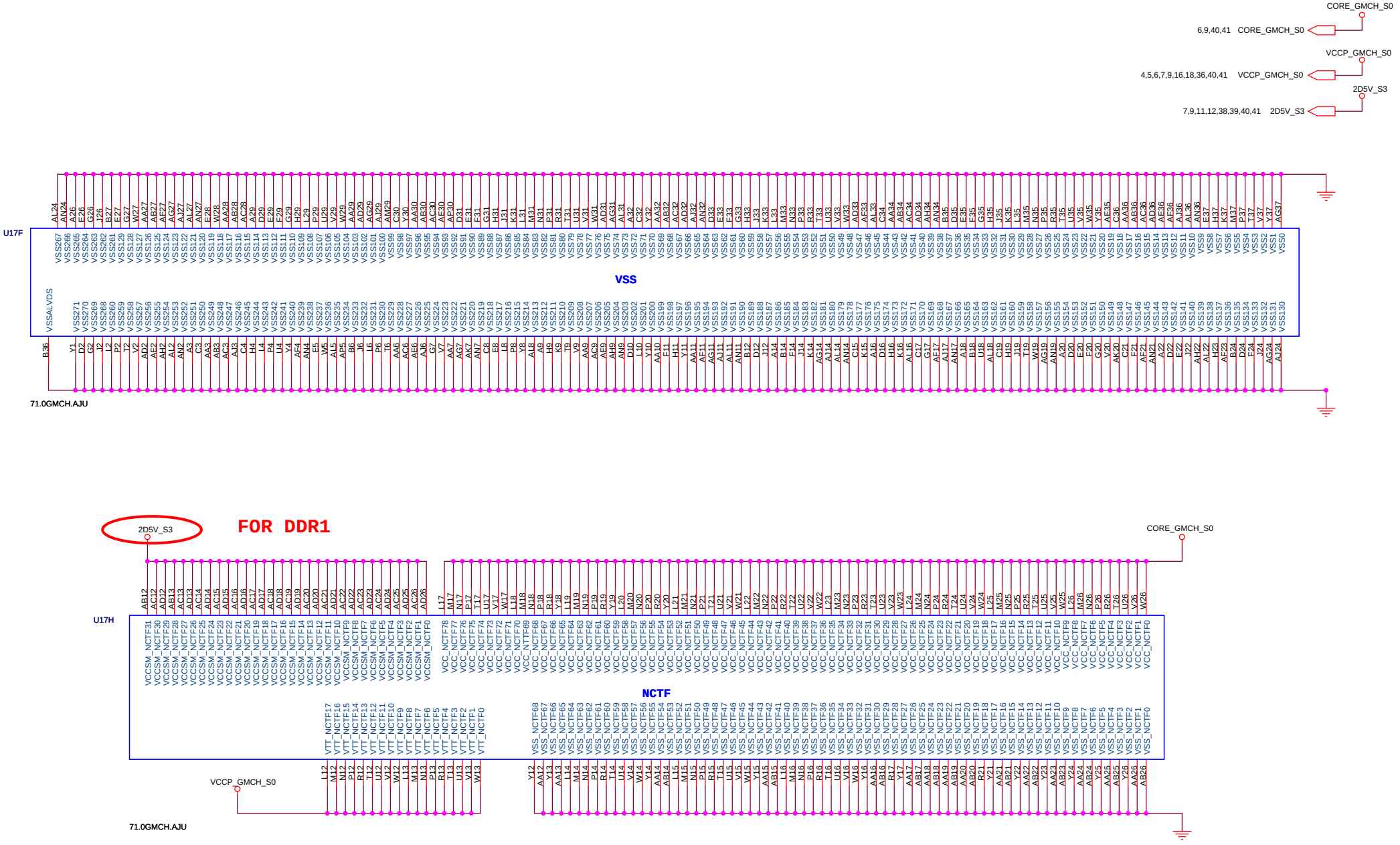
GMCH (4 of 5)
Leopard
Friday, December 10, 2004
hexainf@hotmail.com
GRATIS - FOR FREE



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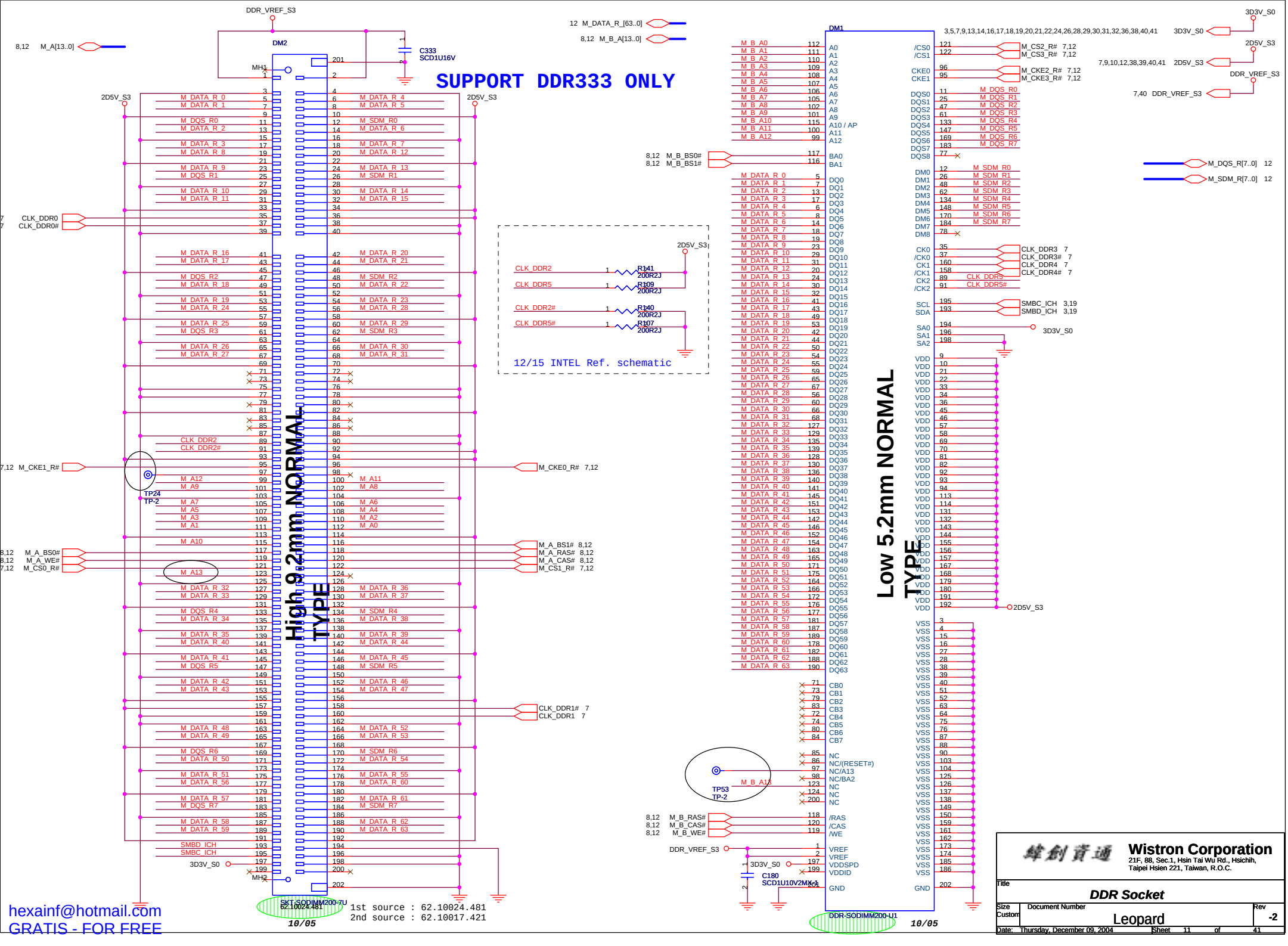
SUPPORT DDR333 ONLY
High 9.2mm NORMAL TYPE
Low 5.2mm NORMAL TYPE
12/15 INTEL Ref. schematic
DDR_VREF_S3
2D5V_S3
3D3V_S0
M_A[13..0]
M_DATA_R_[63..0]
M_B_A[13..0]
M_DATA_R_0
M_DATA_R_1
M_DATA_R_2
M_DATA_R_3
M_DATA_R_4
M_DATA_R_5
M_DATA_R_6
M_DATA_R_7
M_DATA_R_8
M_DATA_R_9
M_DATA_R_10
M_DATA_R_11
M_DATA_R_12
M_DATA_R_13
M_DATA_R_14
M_DATA_R_15
M_DATA_R_16
M_DATA_R_17
M_DATA_R_18
M_DATA_R_19
M_DATA_R_20
M_DATA_R_21
M_DATA_R_22
M_DATA_R_23
M_DATA_R_24
M_DATA_R_25
M_DATA_R_26
M_DATA_R_27
M_DATA_R_28
M_DATA_R_29
M_DATA_R_30
M_DATA_R_31
M_DATA_R_32
M_DATA_R_33
M_DATA_R_34
M_DATA_R_35
M_DATA_R_36
M_DATA_R_37
M_DATA_R_38
M_DATA_R_39
M_DATA_R_40
M_DATA_R_41
M_DATA_R_42
M_DATA_R_43
M_DATA_R_44
M_DATA_R_45
M_DATA_R_46
M_DATA_R_47
M_DATA_R_48
M_DATA_R_49
M_DATA_R_50
M_DATA_R_51
M_DATA_R_52
M_DATA_R_53
M_DATA_R_54
M_DATA_R_55
M_DATA_R_56
M_DATA_R_57
M_DATA_R_58
M_DATA_R_59
M_DATA_R_60
M_DATA_R_61
M_DATA_R_62
M_DATA_R_63
M_DQS_R0
M_DQS_R1
M_DQS_R2
M_DQS_R3
M_DQS_R4
M_DQS_R5
M_DQS_R6
M_DQS_R7
M_SDM_R0
M_SDM_R1
M_SDM_R2
M_SDM_R3
M_SDM_R4
M_SDM_R5
M_SDM_R6
M_SDM_R7
M_A0
M_A1
M_A2
M_A3
M_A4
M_A5
M_A6
M_A7
M_A8
M_A9
M_A10
M_A11
M_A12
M_A13
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_A_BS0#
M_A_WE#
M_CS0_R#
M_A_BS1#
M_A_RAS#
M_A_CAS#
M_CS1_R#
M_CKE0_R#
M_CKE1_R#
M_CS2_R#
M_CS3_R#
M_CKE2_R#
M_CKE3_R#
M_B_BS0#
M_B_BS1#
M_B_RAS#
M_B_CAS#
M_B_WE#
CLK_DDR0
CLK_DDR0#
CLK_DDR1
CLK_DDR1#
CLK_DDR2
CLK_DDR2#
CLK_DDR3
CLK_DDR3#
CLK_DDR4
CLK_DDR4#
CLK_DDR5
CLK_DDR5#
SMBC_ICH
SMBD_ICH
R141 200R2J
R109 200R2J
R140 200R2J
R107 200R2J
C333 SCD1U16V
C180 SCD1U10V2MX-1
DM2
DM1
DDR-SODIMM200-7U
DDR-SODIMM200-U1
TP24 TP-2
TP53 TP-2
MH1
MH2
62.10024.481
1st source : 62.10024.481
2nd source : 62.10017.421
10/05
hexainf@hotmail.com
GRATIS - FOR FREE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR Socket
Size
Custom
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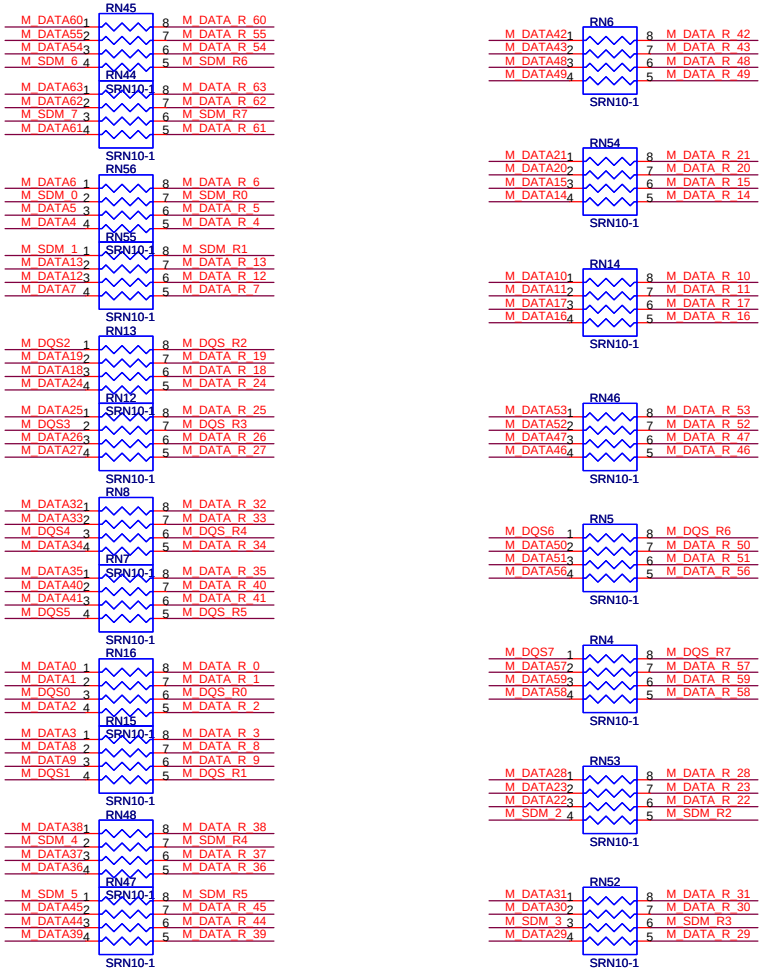
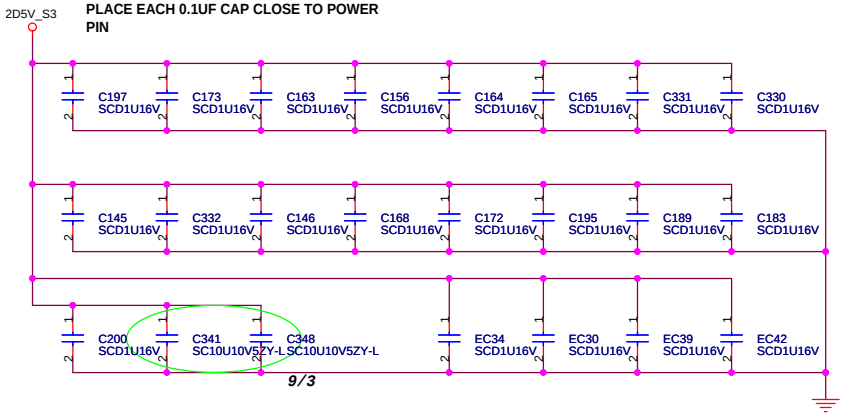
SERIES DAMPING

SC

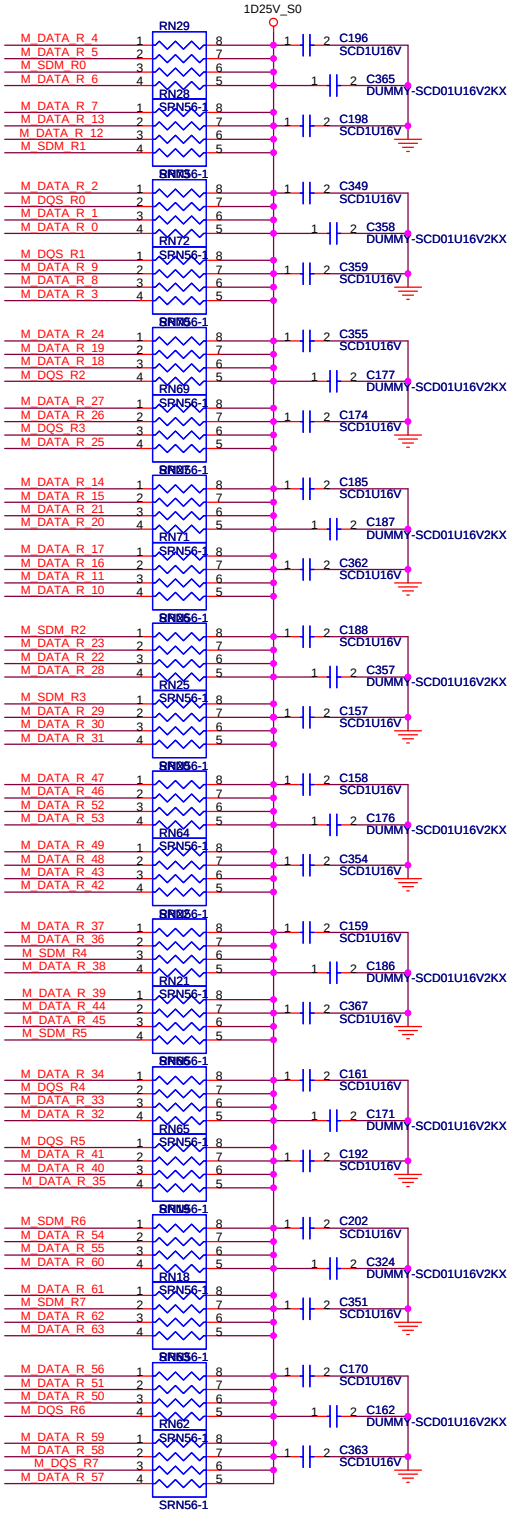
Change RN to small size



PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN

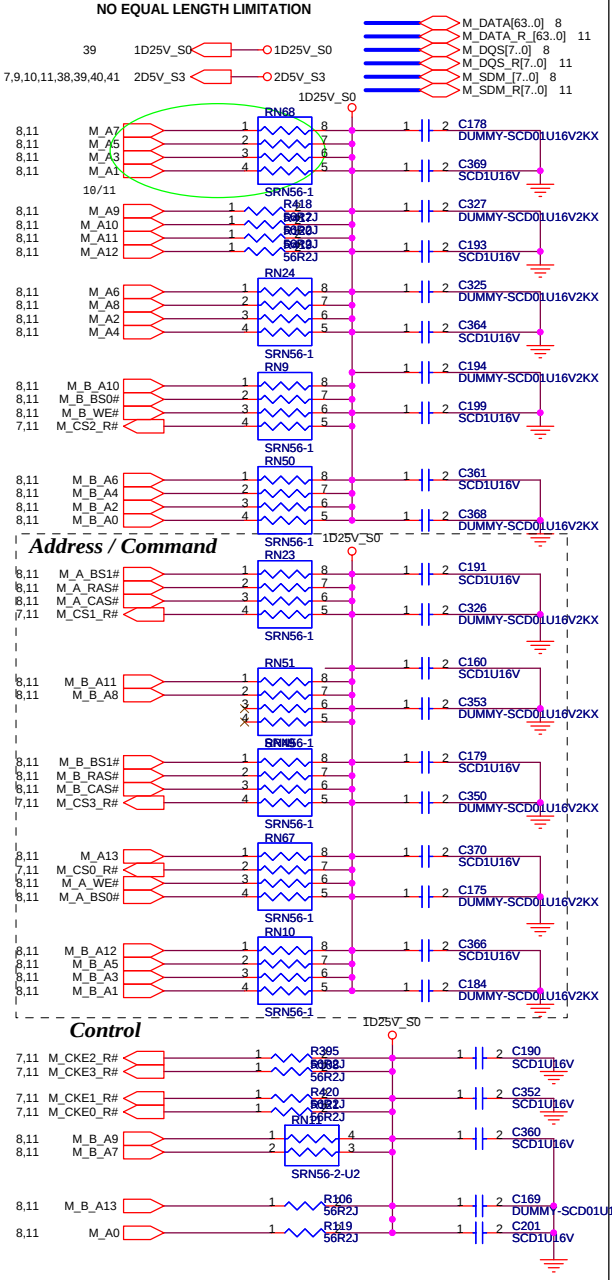


9/3



PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO DM2
NO EQUAL LENGTH LIMITATION



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Title: **DDR Serial/Terminator Resistor**

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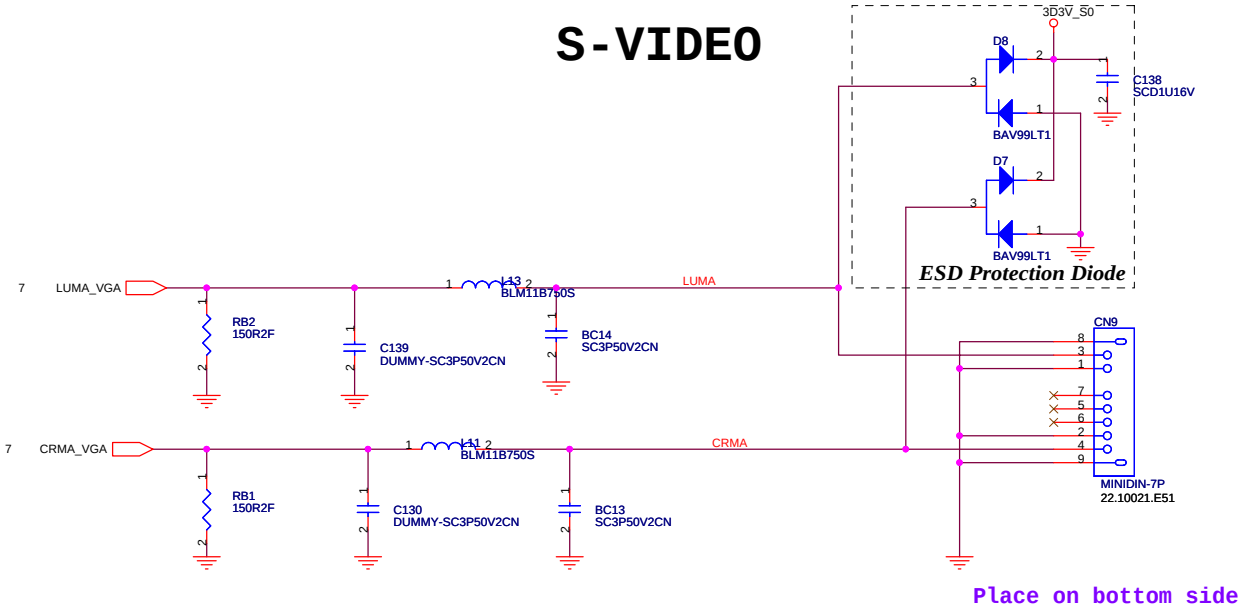
3D3V_S0

3,5,7,9,11,14,16,17,18,19,20,21,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0

S-VIDEO



Place on bottom side

緯創資通 Wistron Corporation
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Title	S-VIDEO	
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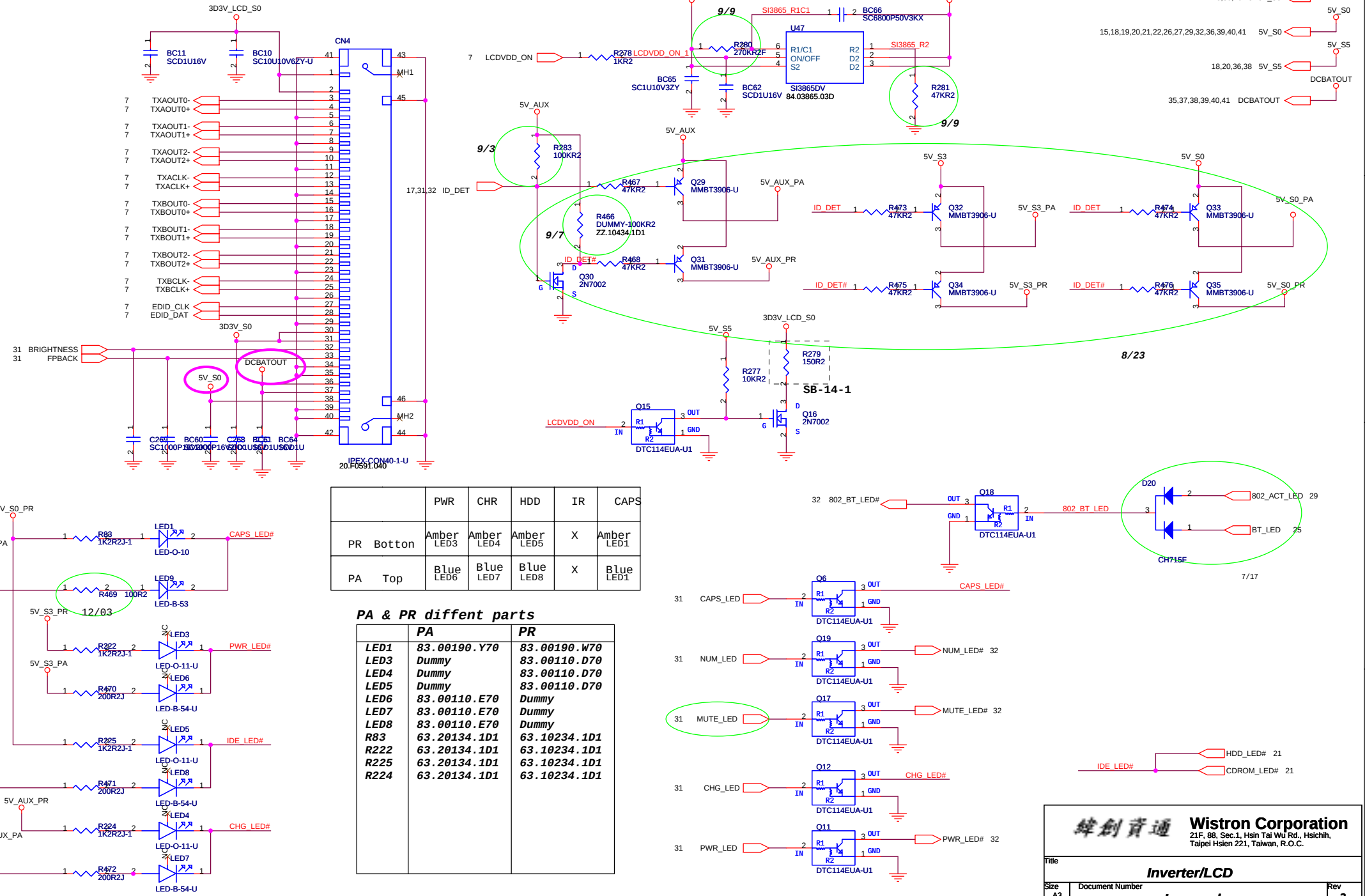
INVERTER/LCD



	PWR	CHR	HDD	IR	CAPS
PR Botton	Amber LED3	Amber LED4	Amber LED5	X	Amber LED1
PA Top	Blue LED6	Blue LED7	Blue LED8	X	Blue LED1

PA & PR diffent parts

	PA	PR
LED1	83.00190.Y70	83.00190.W70
LED3	Dummy	83.00110.D70
LED4	Dummy	83.00110.D70
LED5	Dummy	83.00110.D70
LED6	83.00110.E70	Dummy
LED7	83.00110.E70	Dummy
LED8	83.00110.E70	Dummy
R83	63.20134.1D1	63.10234.1D1
R222	63.20134.1D1	63.10234.1D1
R225	63.20134.1D1	63.10234.1D1
R224	63.20134.1D1	63.10234.1D1

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Title: *Inverter/LCD*

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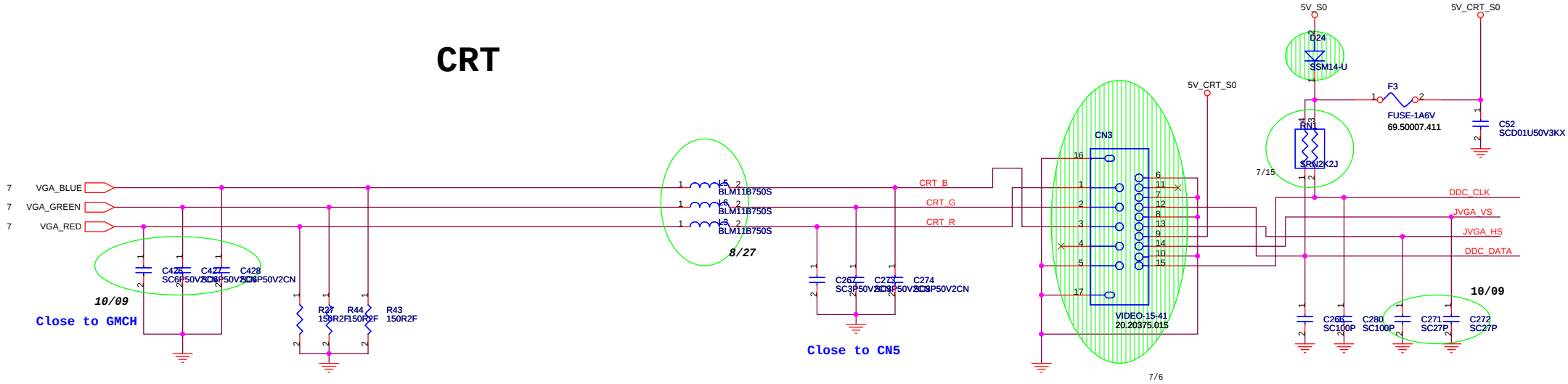
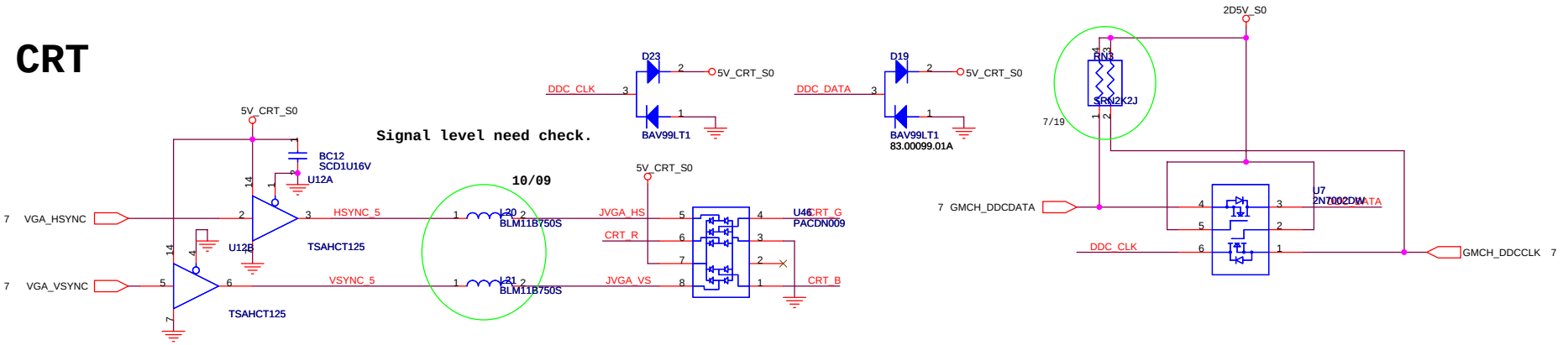
CRT CONN

CRT



CRT



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Title	CRT/ CIR	
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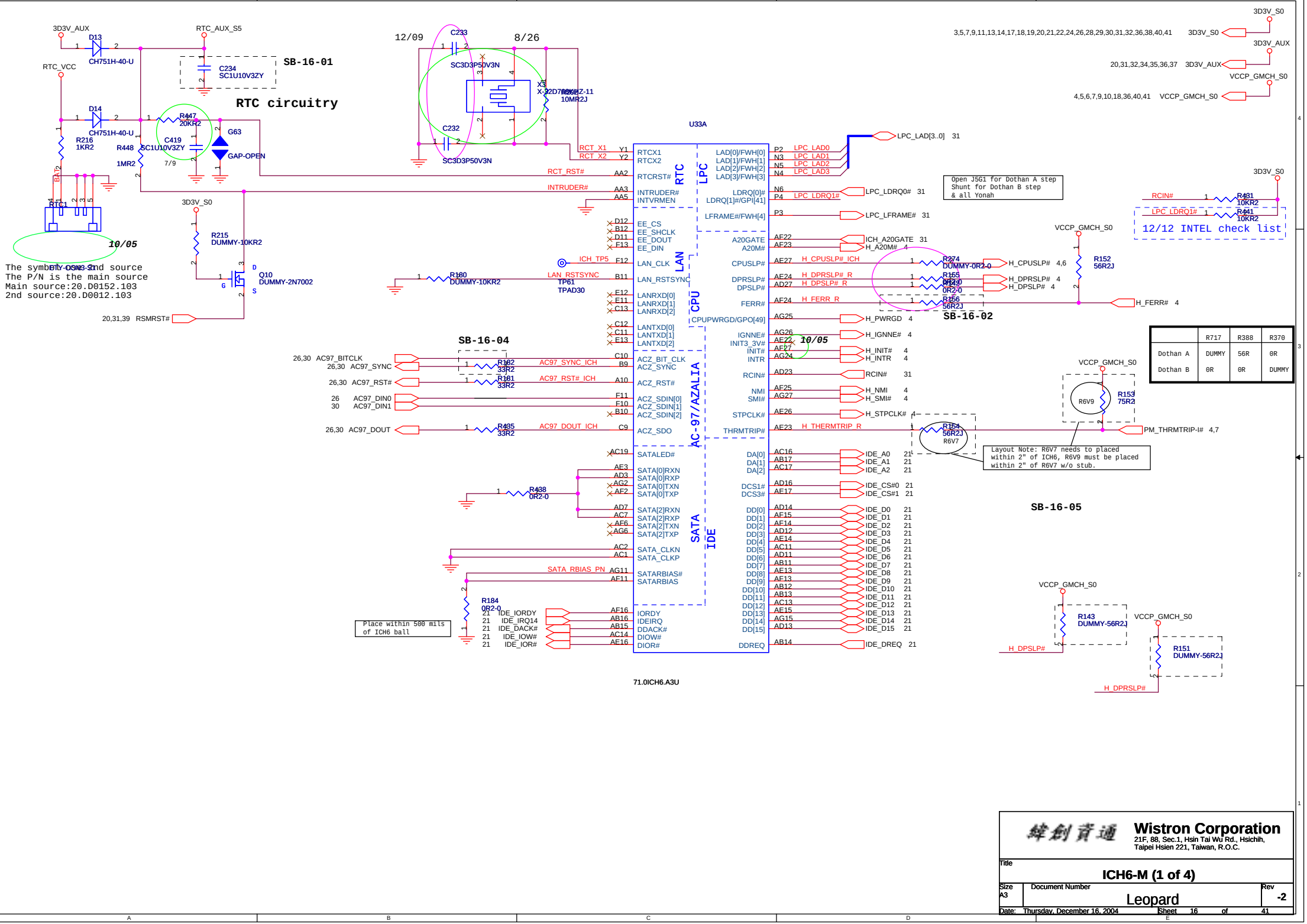
RTC circuitry
SB-16-01
SB-16-02
SB-16-04
SB-16-05
10/05
12/09
8/26
12/12 INTEL check list
The symbol is 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103
Open J561 for Dothan A step
Shunt for Dothan B step
& all Yonah
Place within 500 mils
of ICH6 ball
Layout Note: R6V7 needs to placed
within 2" of ICH6, R6V9 must be placed
within 2" of R6V7 w/o stub.
U33A
RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE
71.0ICH6.A3U
Dothan A
Dothan B
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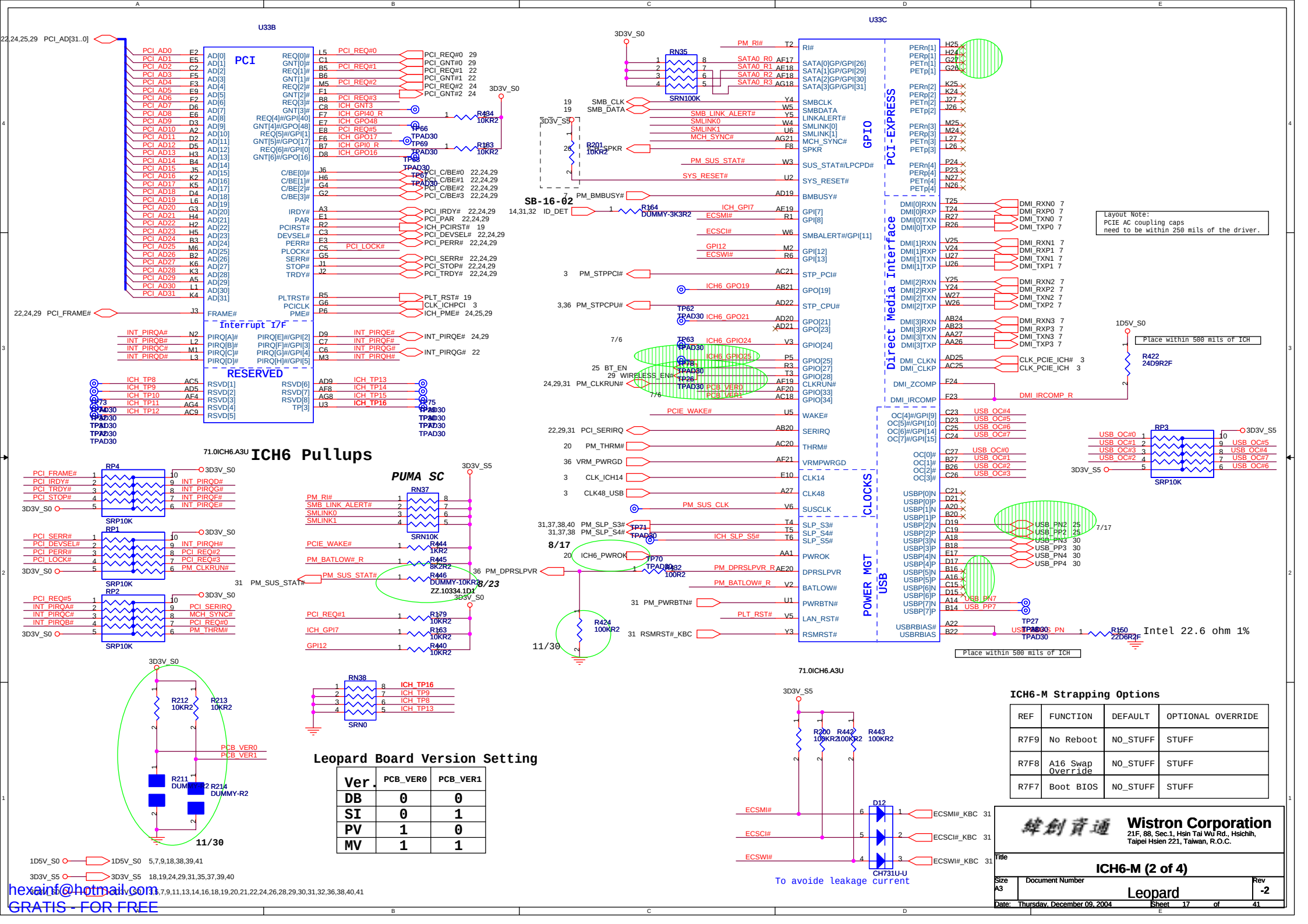
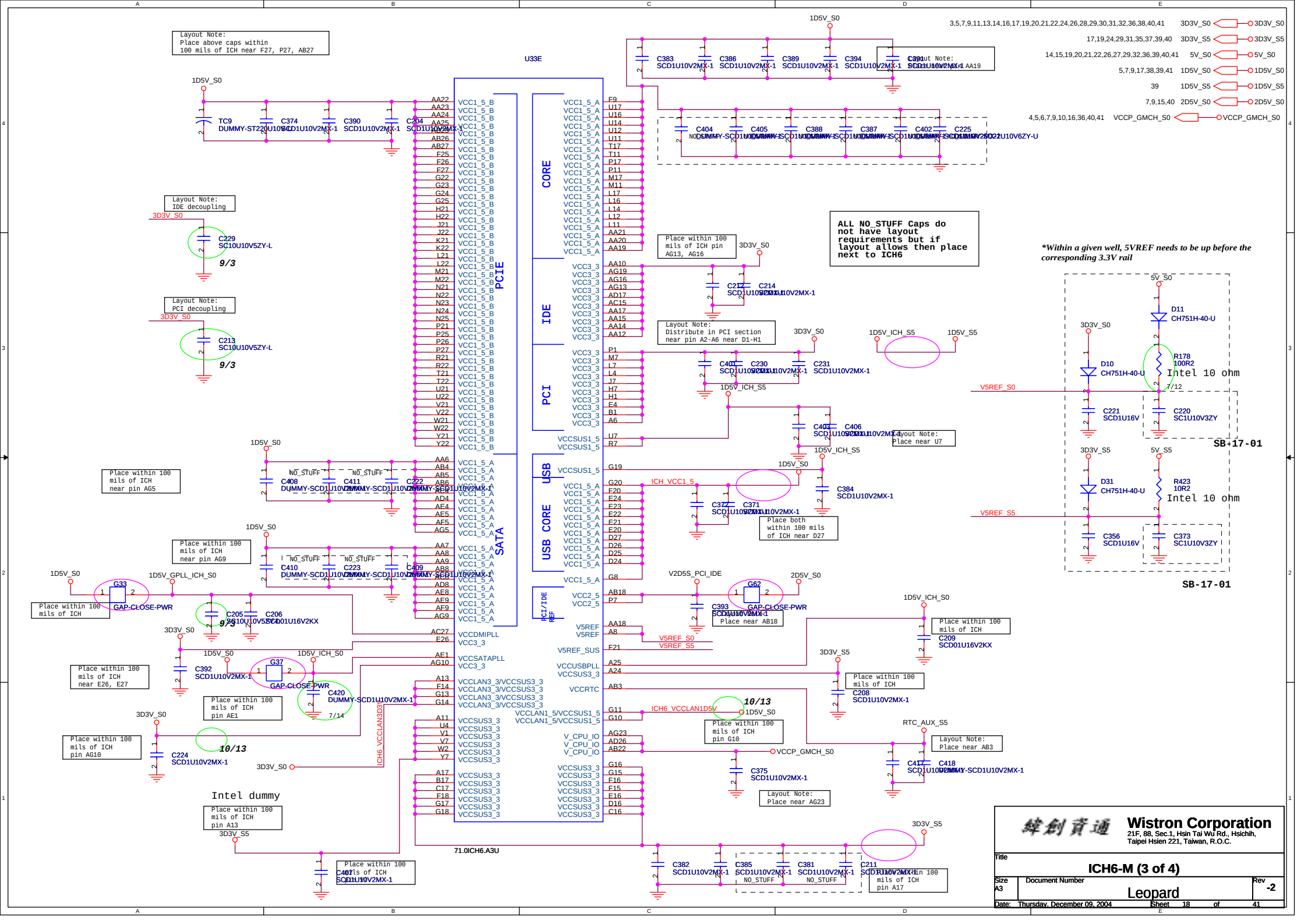
ICH6-M (1 of 4)
Leopard
Thursday, December 16, 2004



Ver.	PCB_VER0	PCB_VER1
DB	0	0
SI	0	1
PV	1	0
MV	1	1

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF


U33E
PCIE
SATA
USB
USB CORE
CORE
IDE
PCI
Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27
Layout Note:
IDE decoupling
Layout Note:
PCI decoupling
Place within 100
mils of ICH
near pin AG5
Place within 100
mils of ICH
near pin AG9
Place within 100
mils of ICH
near E26, E27
Place within 100
mils of ICH
pin AE1
Place within 100
mils of ICH
pin AG10
Place within 100
mils of ICH
pin A13
Place within 100
mils of ICH
pin A17
Intel dummy
ALL NO_STUFF Caps do
not have layout
requirements but if
layout allows then place
next to ICH6
*Within a given well, 5VREF needs to be up before the
corresponding 3.3V rail
Place within 100
mils of ICH pin
AG13, AG16
Layout Note:
Distribute in PCI section
near pin A2-A6 near D1-H1
Layout Note:
Place near U7
Place both
within 100 mils
of ICH near D27
Place near AB18
Layout Note:
Place near AG23
Layout Note:
Place near AB3
Intel 10 ohm
SB-17-01
ICH6_VCCLAN3D3
ICH_VCC1_5
ICH6_VCCLAN1D5V
V5REF_S0
V5REF_S5
VCCP_GMCH_S0
V2D5S_PCI_IDE
71.0ICH6.A3U
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Title
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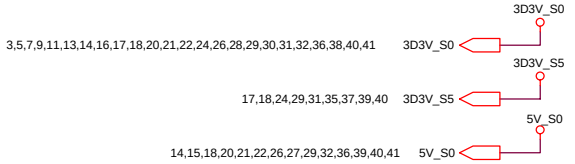
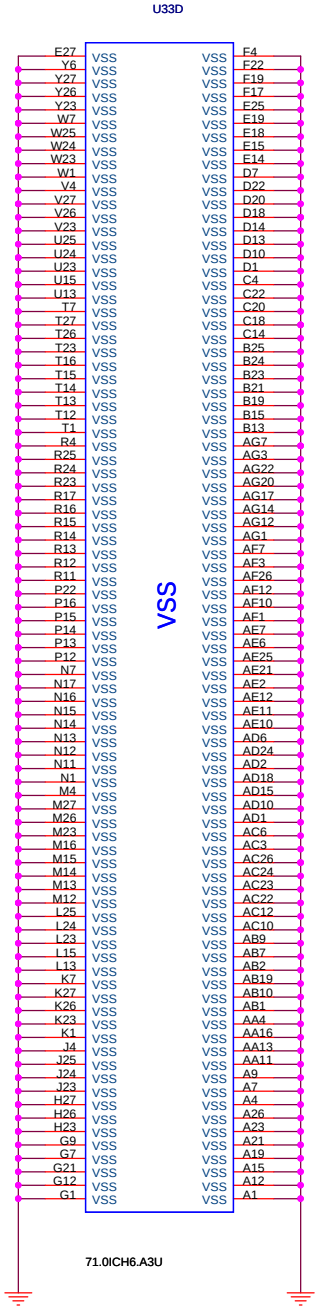
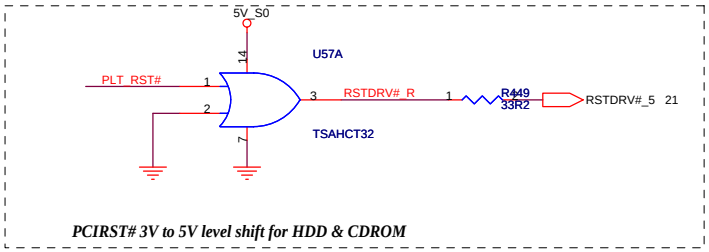




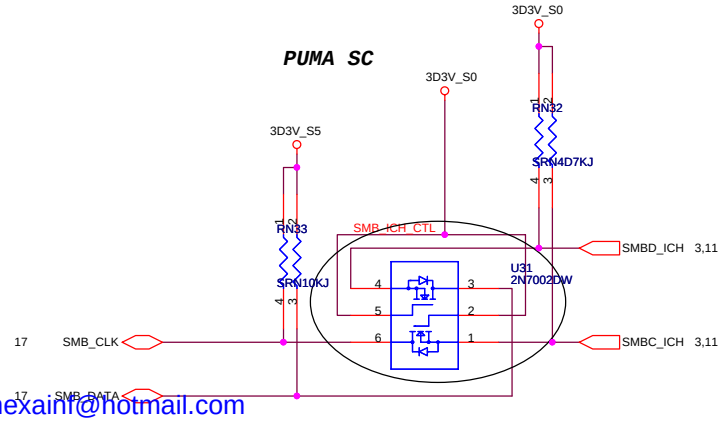
Cougar
SC

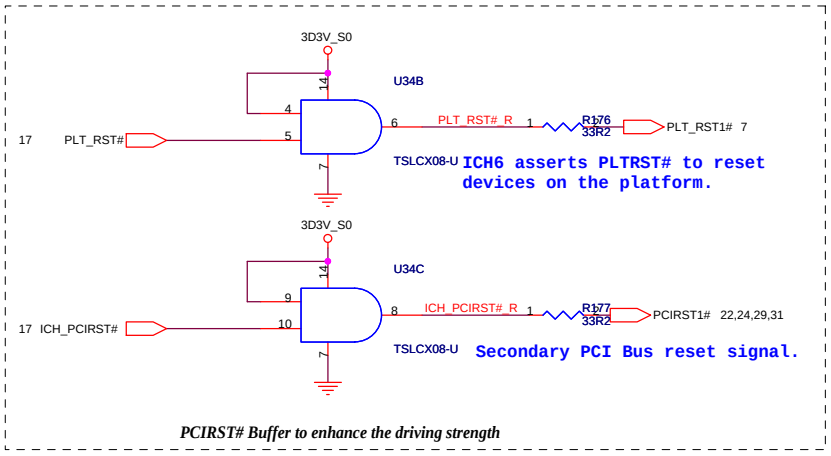


PCIRST# 3V to 5V level shift for HDD & CDROM

SMBUS(ICH6 ---> SODIMM,CLKGEN)

PUMA SC





PCIRST# Buffer to enhance the driving strength

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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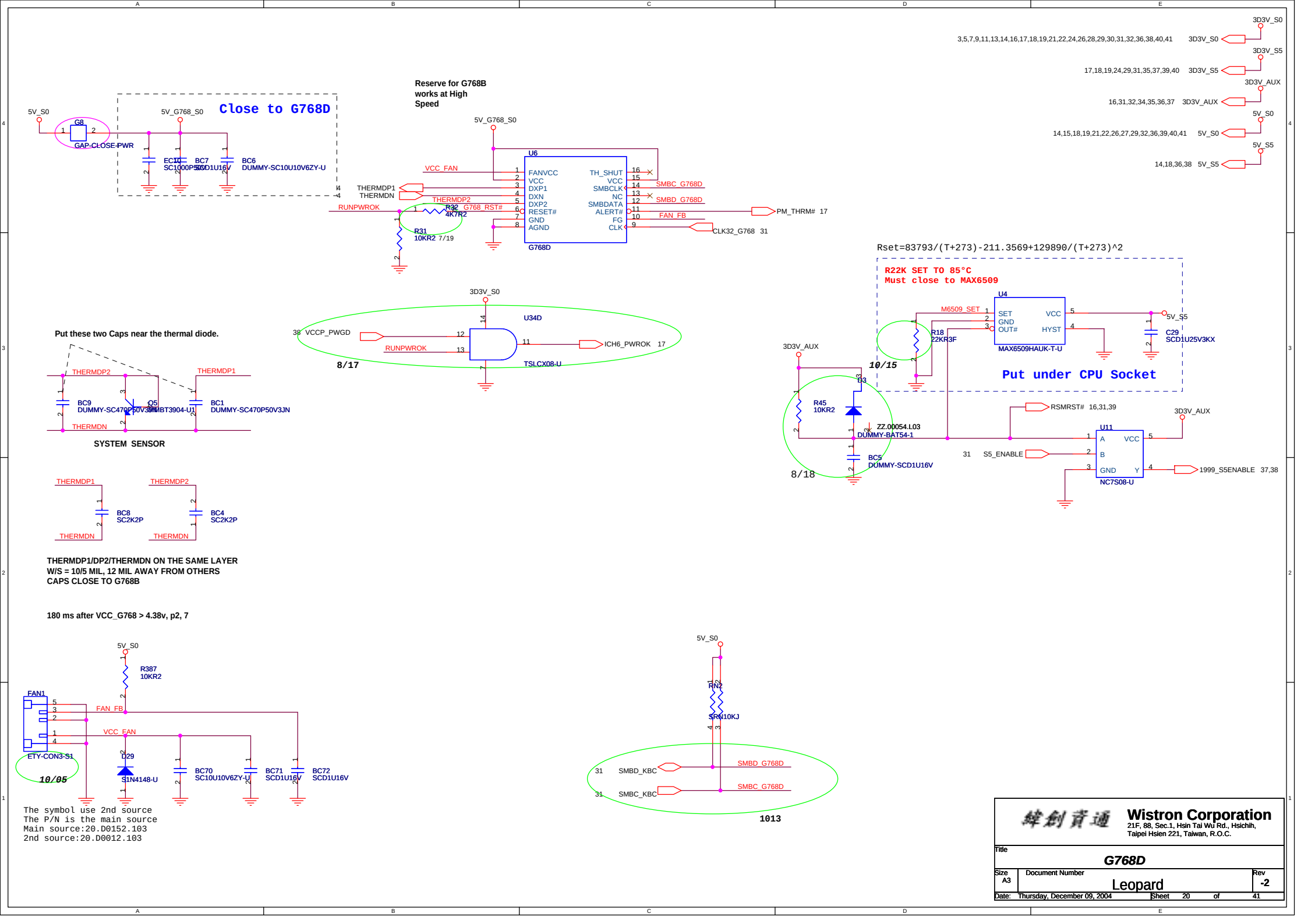
Close to G768D
5V_S0
5V_G768_S0
G8
GAP-CLOSE-PWR
EC10
SC1000P50V
BC7
SCD1U16V
BC6
DUMMY-SC10U10V6ZY-U
Reserve for G768B
works at High
Speed
U6
VCC_FAN
THERMDP1
THERMDN
THERMDP2
RUNPWROK
R32
4K7R2
G768_RST#
R31
10KR2 7/19
FANVCC
VCC
DXP1
DXN
DXP2
RESET#
GND
AGND
TH_SHUT
VCC
SMBCLK
NC
SMBDATA
ALERT#
FG
CLK
SMBC_G768D
SMBD_G768D
FAN_FB
PM_THRM# 17
CLK32_G768 31
G768D
3D3V_S0
3,5,7,9,11,13,14,16,17,18,19,21,22,24,26,28,29,30,31,32,36,38,40,41
3D3V_S5
17,18,19,24,29,31,35,37,39,40
3D3V_AUX
16,31,32,34,35,36,37
14,15,18,19,21,22,26,27,29,32,36,39,40,41
14,18,36,38
Rset=83793/(T+273)-211.3569+129890/(T+273)^2
R22K SET TO 85°C
Must close to MAX6509
U4
M6509_SET
SET
GND
OUT#
VCC
HYST
MAX6509HAUK-T-U
R18
22KR3F
C29
SCD1U25V3KX
Put under CPU Socket
10/15
Put these two Caps near the thermal diode.
THERMDP2
THERMDP1
THERMDN
BC9
DUMMY-SC470P50V3JN
Q5
MMBT3904-U1
BC1
DUMMY-SC470P50V3JN
SYSTEM SENSOR
U34D
38 VCCP_PWGD
RUNPWROK
ICH6_PWROK 17
TSLCX08-U
8/17
3D3V_AUX
D3
R45
10KR2
ZZ.00054.L03
DUMMY-BAT54-1
BC5
DUMMY-SCD1U16V
8/18
RSMRST# 16,31,39
31 S5_ENABLE
U11
A
B
GND
VCC
Y
NC7S08-U
1999_S5ENABLE 37,38
THERMDP1
THERMDP2
BC8
SC2K2P
BC4
SC2K2P
THERMDN
THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B
180 ms after VCC_G768 > 4.38v, p2, 7
R387
10KR2
FAN1
FAN_FB
VCC_FAN
ETY-CON3-S1
D29
S1N4148-U
BC70
SC10U10V6ZY-U
BC71
SCD1U16V
BC72
SCD1U16V
10/05
RN2
SRN10KJ
31 SMBD_KBC
31 SMBC_KBC
SMBD_G768D
SMBC_G768D
1013
The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103
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Title
G768D
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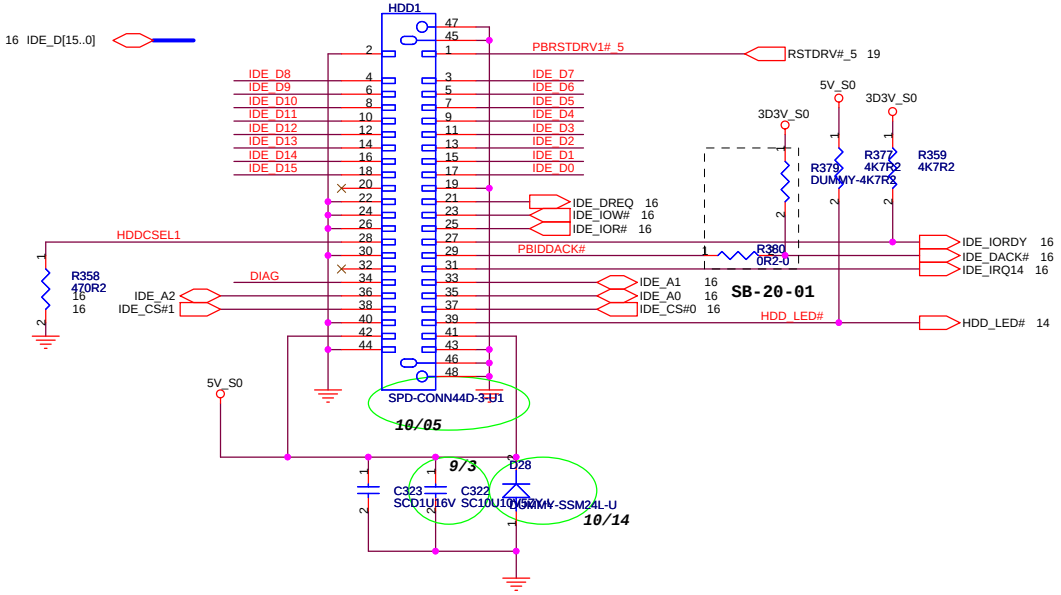
HDD Connector



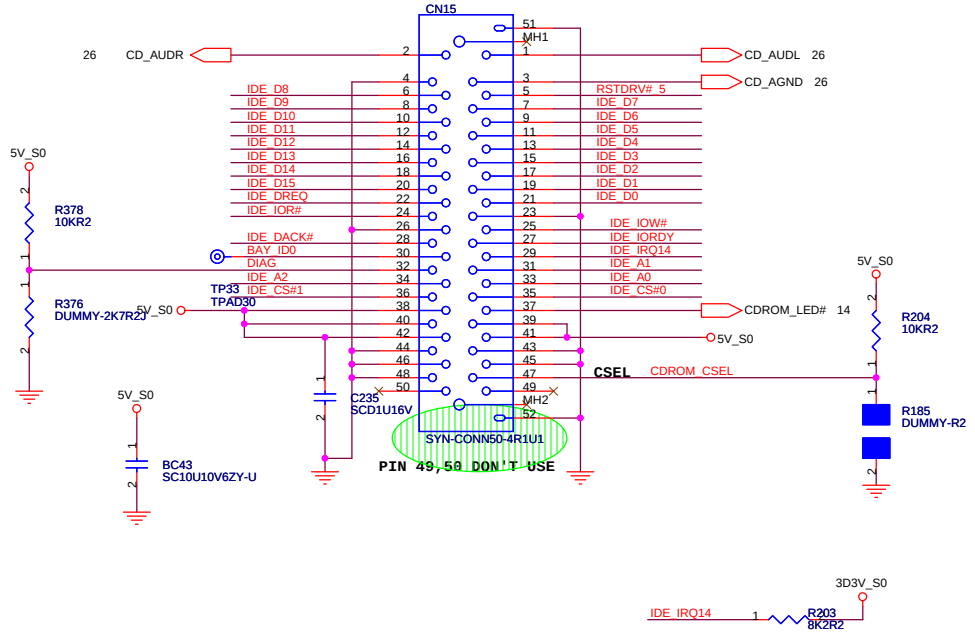
3,5,7,9,11,13,14,16,17,18,19,20,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0 — 3D3V_S0

24,41 3D3V_LAN_S5 — 3D3V_LAN_S5

14,15,18,19,20,22,26,27,29,32,36,39,40,41 5V_S0 — 5V_S0

5,7,9,17,18,38,39,41 1D5V_S0 — 1D5V_S0

CDROM



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD / CDROM***	
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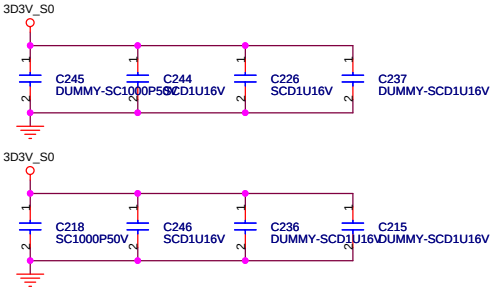
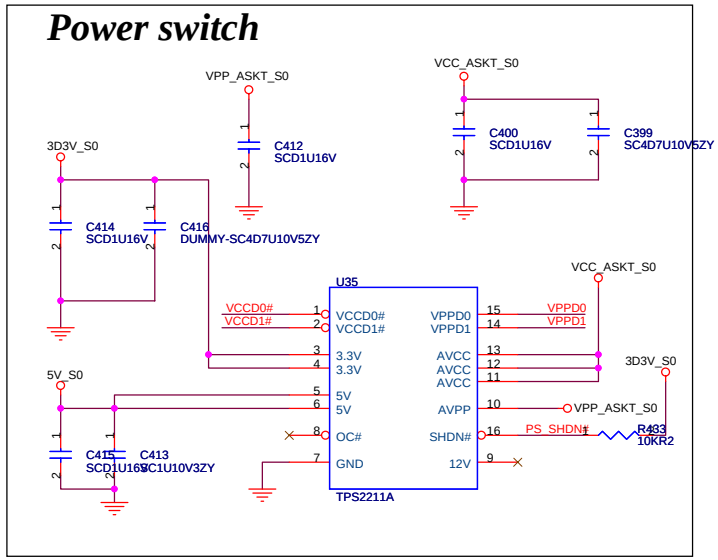
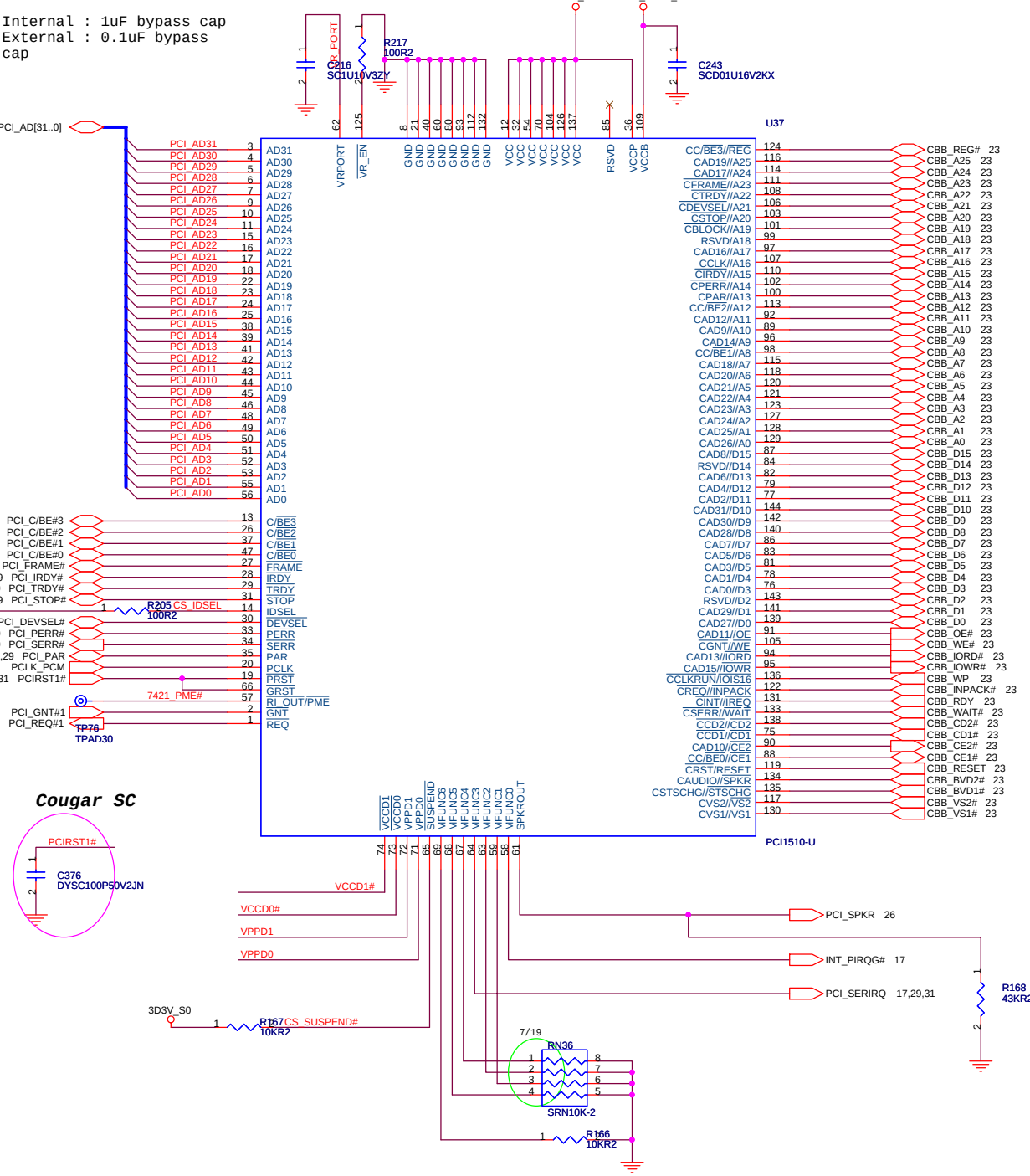
Internal : 1uF bypass cap
External : 0.1uF bypass cap

3,5,7,9,11,13,14,16,17,18,19,20,21,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0

Bypass/Decupoling Capacitors Should be places as close to PCI1510 as possible







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Title	TI PCI1510
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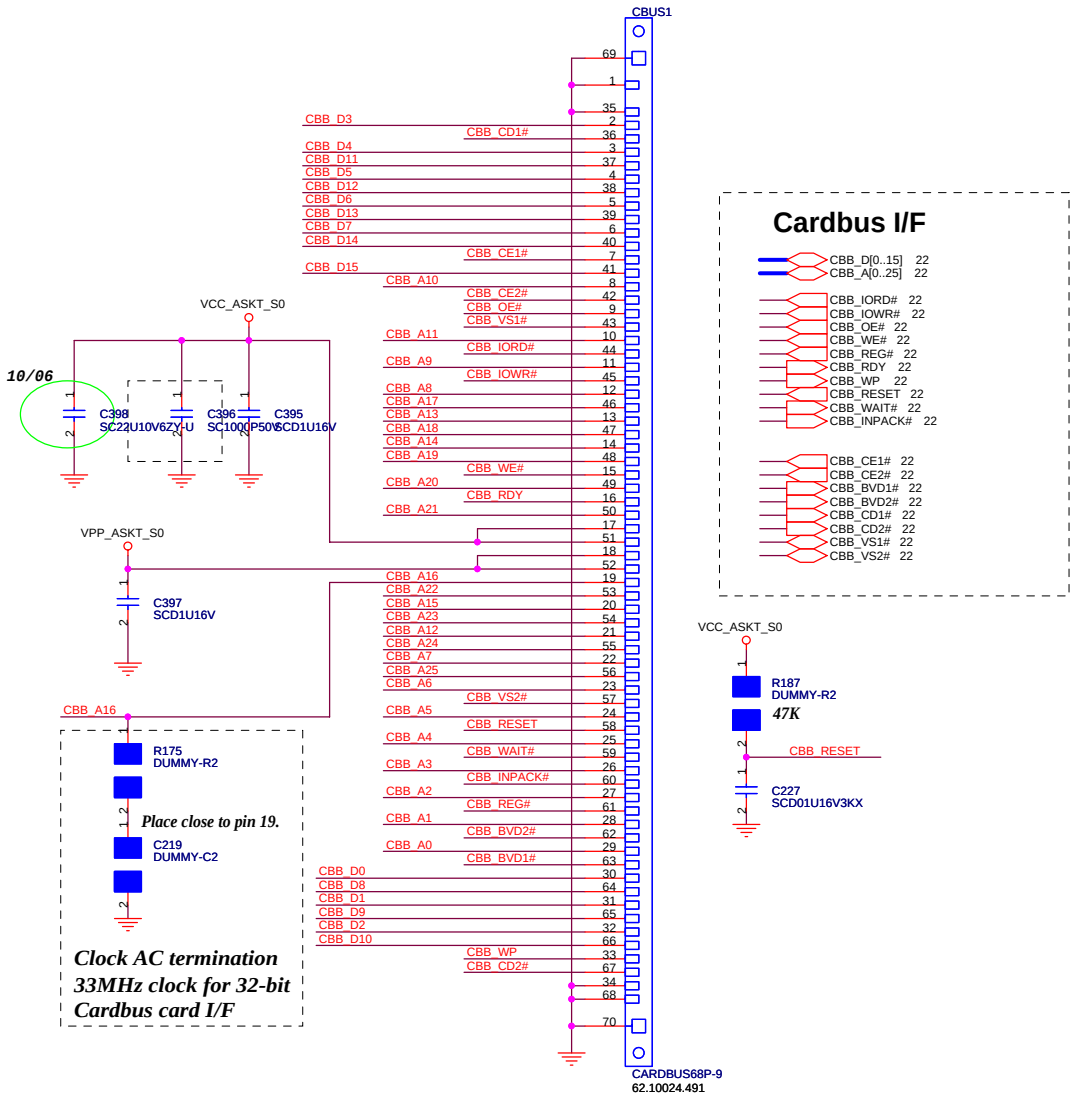
PCMCIA Socket

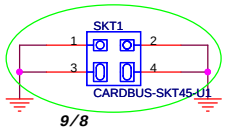


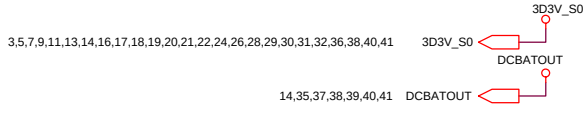
Cardbus I/F

CBB_D[0..15] 22
CBB_A[0..25] 22

CBB_IORD# 22
CBB_IOWR# 22
CBB_OE# 22
CBB_WE# 22
CBB_REG# 22
CBB_RDY 22
CBB_WP 22
CBB_RESET 22
CBB_WAIT# 22
CBB_INPACK# 22

CBB_CE1# 22
CBB_CE2# 22
CBB_BVD1# 22
CBB_BVD2# 22
CBB_CD1# 22
CBB_CD2# 22
CBB_VS1# 22
CBB_VS2# 22





Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA SLOT

Size: A3 | Document Number: Leopard | Rev: -2

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Close to RTL8100C
Pin121,Pin122

HM1-SB
Remove LED function

RTL8100CL-U

SB-24-01

Cougar SC

Title	LAN RTL8100C
Size	A3
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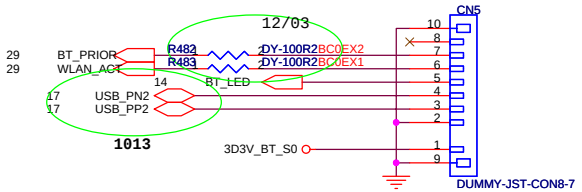
Sheet	24 of 41

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

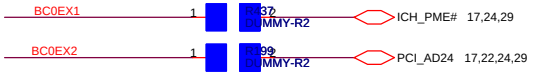
Cougar SC

Blue thumb

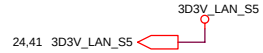
Place on bottom side
From NEW!

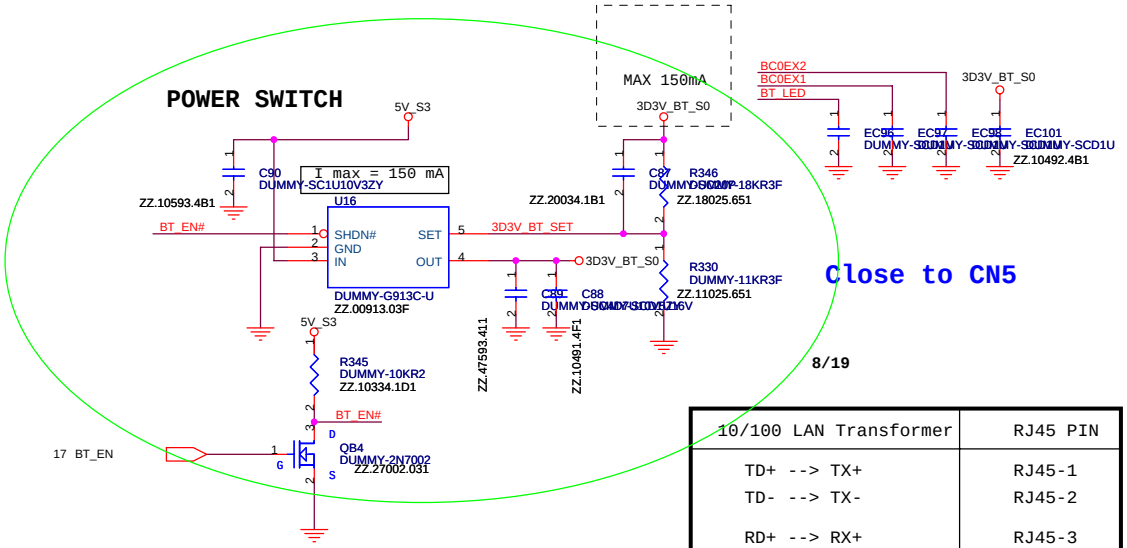


BC0EX2 connect to PCI_AD22 on main board.
BC0EX1 connect to ICH_PME# on main board.



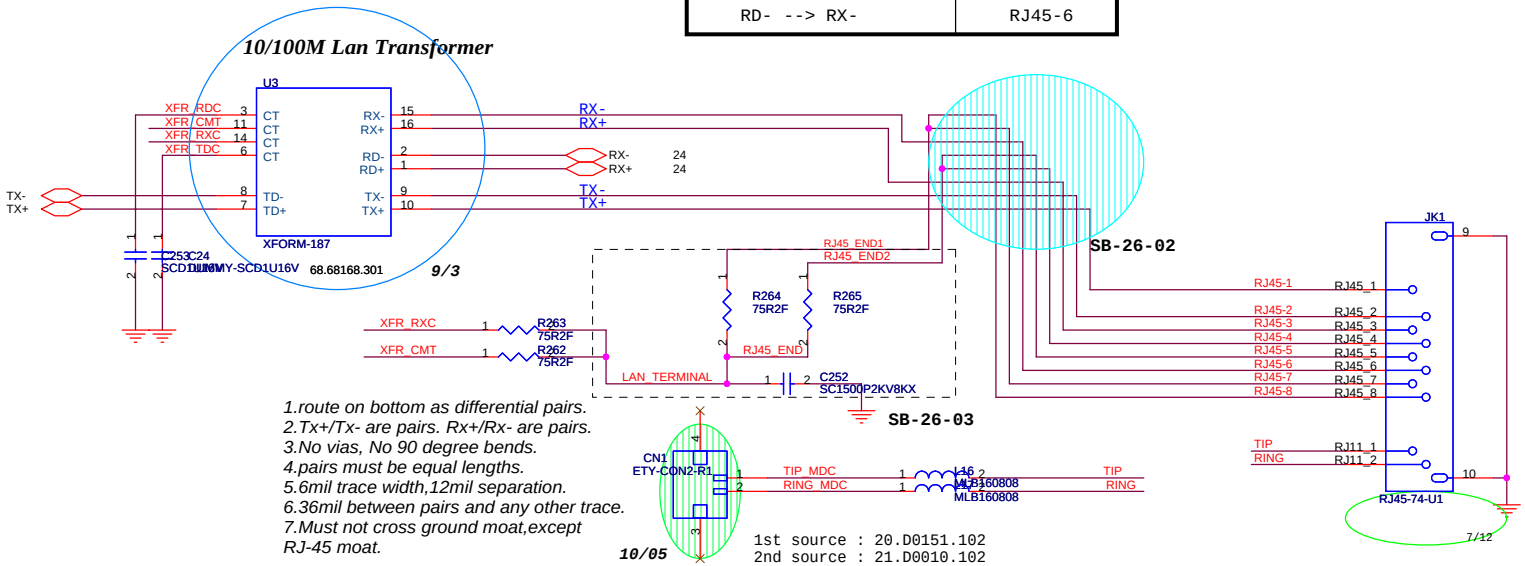
Please close to ICH6





Close to CN5

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

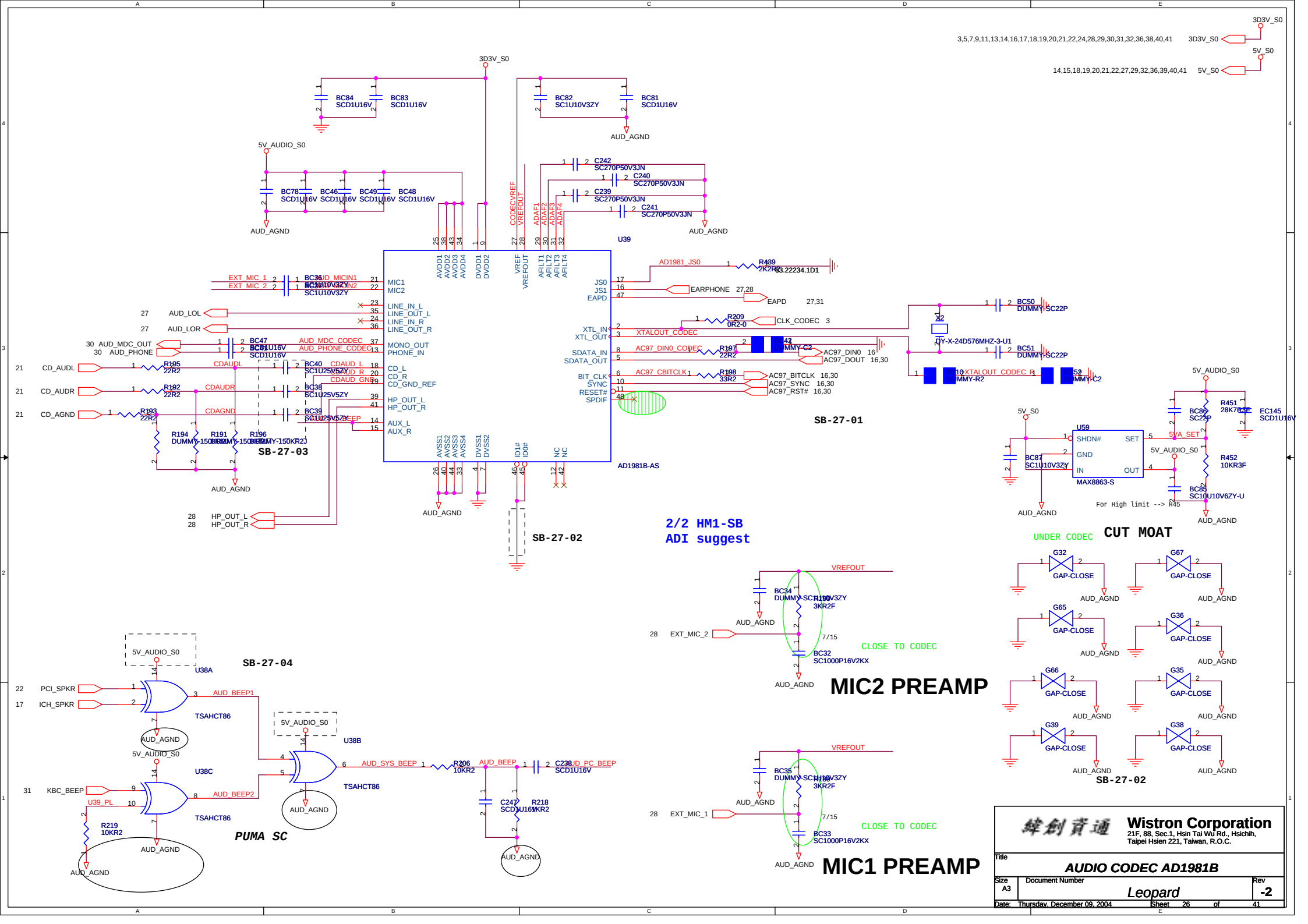


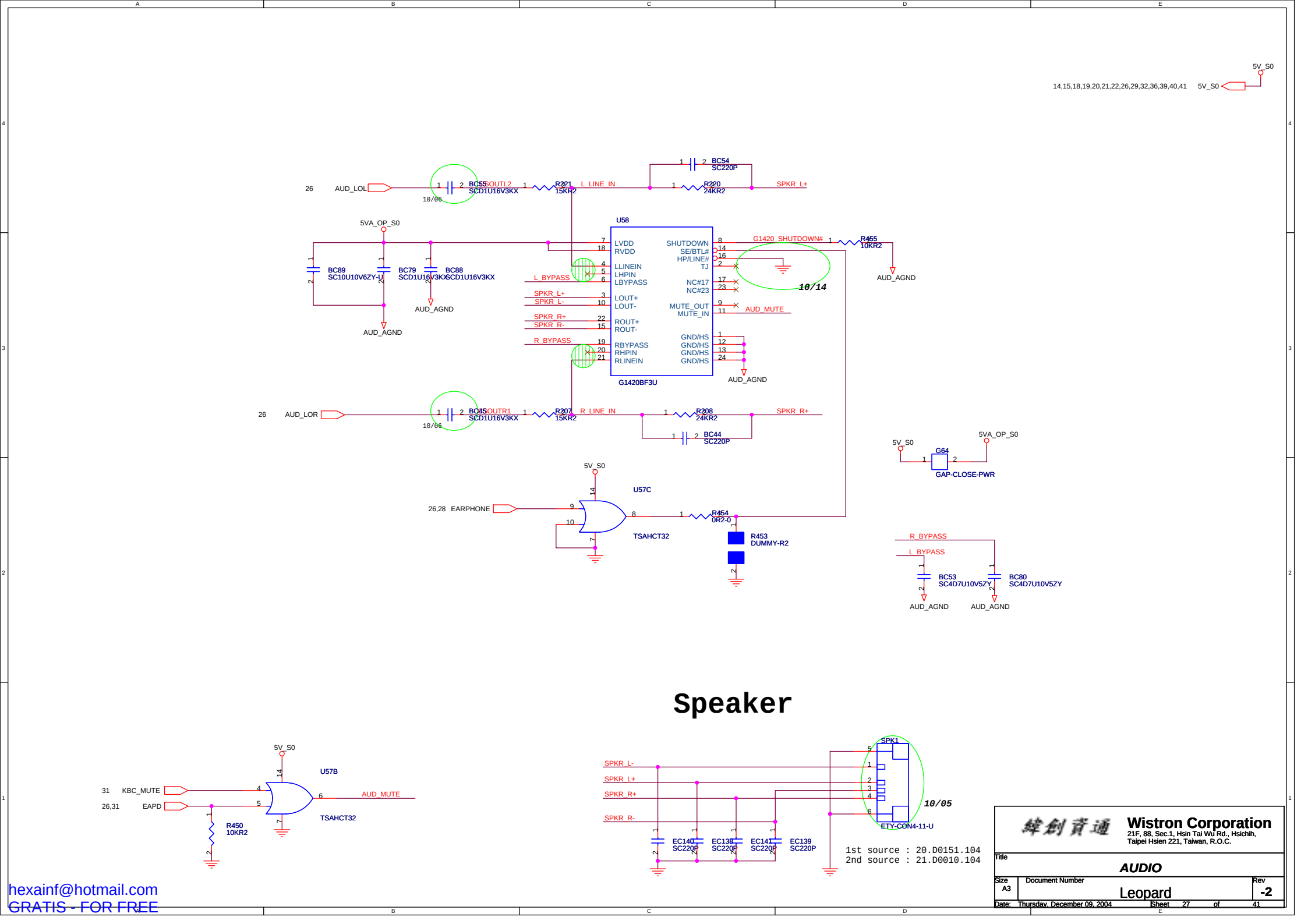
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

1st source : 20.D0151.102
2nd source : 21.D0010.102

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN / 1394 Connector
Size: A3 | Document Number: Leopard | Rev: -2
Date: Thursday, December 09, 2004 | Sheet 25 of 41


3D3V_S0
5V_S0
5V_AUDIO_S0
AUD_AGND
U39
AD1981B-AS
SB-27-01
SB-27-02
SB-27-03
SB-27-04
2/2 HM1-SB
ADI suggest
CUT MOAT
UNDER CODEC
MIC2 PREAMP
MIC1 PREAMP
CLOSE TO CODEC
PUMA SC
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO CODEC AD1981B
Leopard
Thursday, December 09, 2004


5V_S0
14,15,18,19,20,21,22,26,29,32,36,39,40,41
5V_S0
26
AUD_LOL
BC55
SCD1U16V3KX
10/06
SOUTL2
R221
15KR2
L_LINE_IN
BC54
SC220P
R220
24KR2
SPKR_L+
5VA_OP_S0
BC89
SC10U10V6ZY-U
BC79
SCD1U16V3KX
BC88
SCD1U16V3KX
AUD_AGND
AUD_AGND
U58
LVDD
RVDD
LLINEIN
LHPIN
LBYPASS
LOUT+
LOUT-
ROUT+
ROUT-
RBYPASS
RHPIN
RLINEIN
L_BYPASS
SPKR_L+
SPKR_L-
SPKR_R+
SPKR_R-
R_BYPASS
SHUTDOWN
SE/BTL#
HP/LINE#
TJ
NC#17
NC#23
MUTE_OUT
MUTE_IN
GND/HS
GND/HS
GND/HS
GND/HS
G1420_SHUTDOWN#
R455
10KR2
AUD_AGND
10/14
AUD_MUTE
AUD_AGND
G1420BF3U
26
AUD_LOR
BC45
SCD1U16V3KX
10/06
SOUTR1
R207
15KR2
R_LINE_IN
R208
24KR2
SPKR_R+
BC44
SC220P
5V_S0
U57C
26,28
EARPHONE
TSAHCT32
R454
0R2-0
R453
DUMMY-R2
5V_S0
G64
5VA_OP_S0
GAP-CLOSE-PWR
R_BYPASS
L_BYPASS
BC53
SC4D7U10V5ZY
BC80
SC4D7U10V5ZY
AUD_AGND
AUD_AGND
Speaker
5V_S0
U57B
31
KBC_MUTE
26,31
EAPD
AUD_MUTE
TSAHCT32
R450
10KR2
SPKR_L-
SPKR_L+
SPKR_R+
SPKR_R-
SPK1
10/05
ETY-CON4-11-U
EC140
SC220P
EC138
SC220P
EC141
SC220P
EC139
SC220P
1st source : 20.D0151.104
2nd source : 21.D0010.104
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO
Size
A3
Document Number
Leopard
Rev
-2
Date: Thursday, December 09, 2004
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hexainf@hotmail.com
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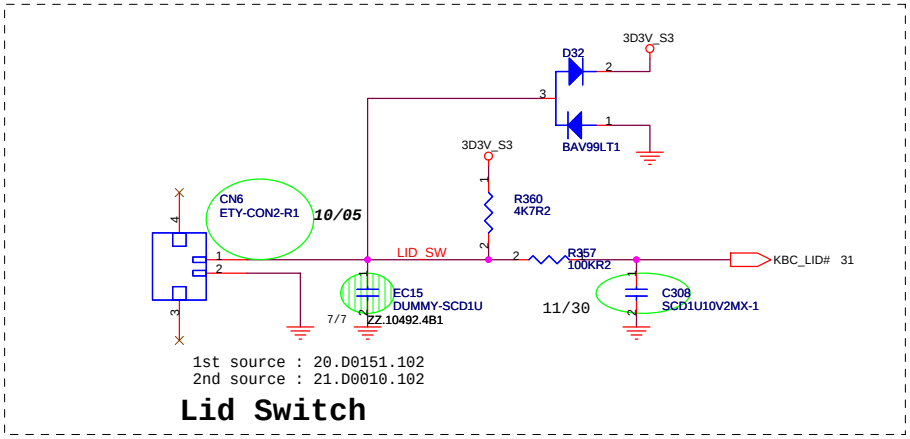
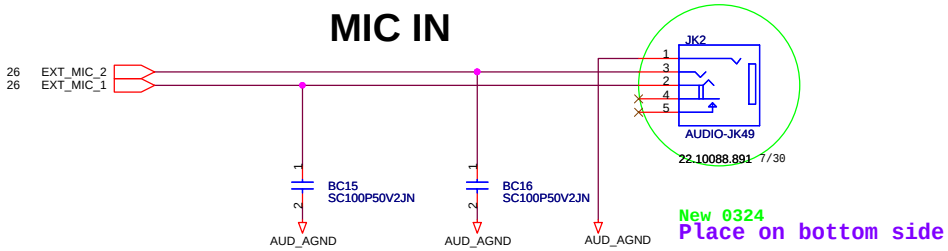
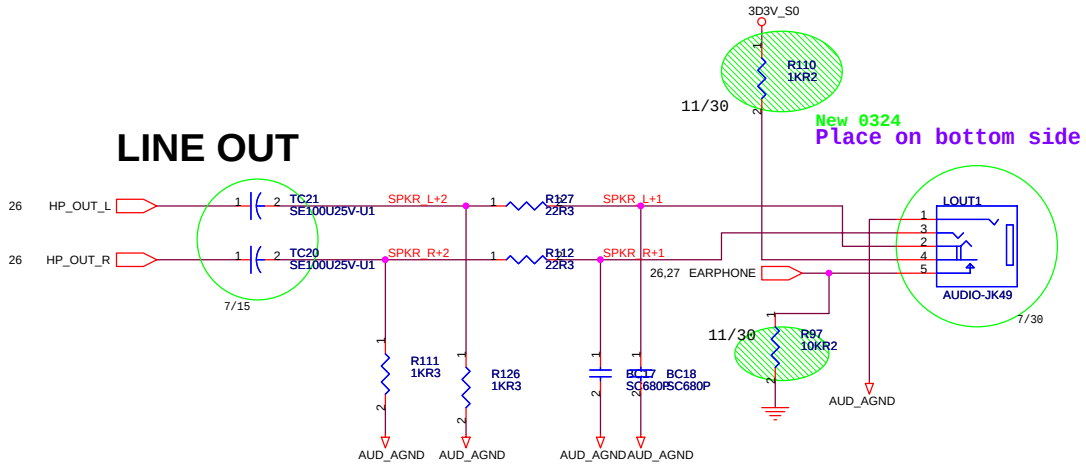
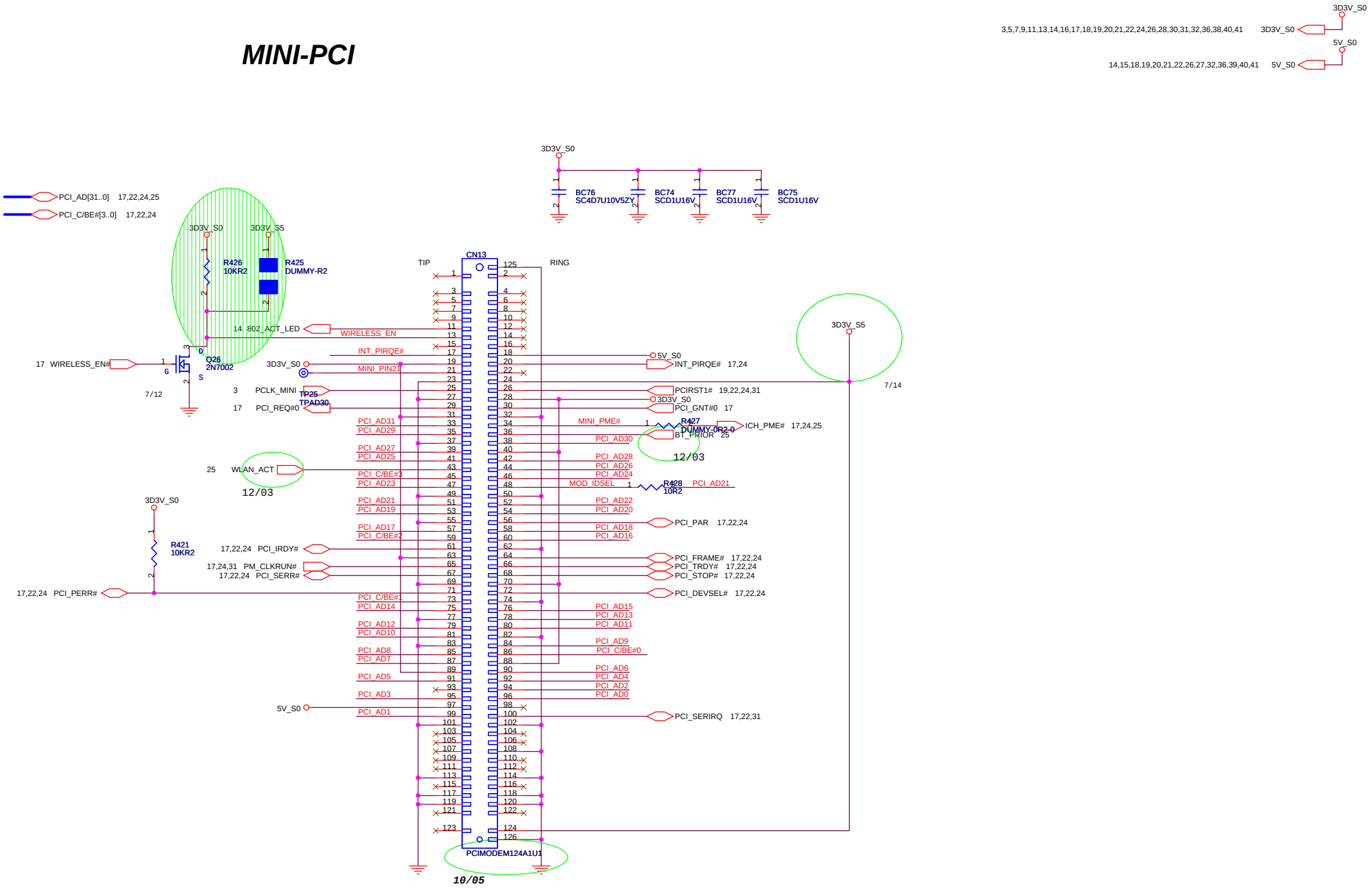






緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO CONN/LID switch		
Size: A3	Document Number: Leopard	Rev: -2
Date: Thursday, December 09, 2004	Sheet 28 of 41	

MINI-PCI

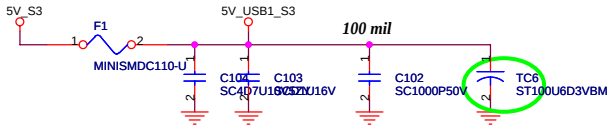


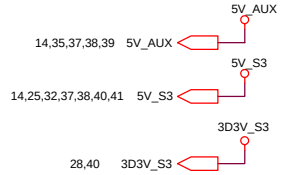
The symbol use 2nd source
The P/N is the main source
Main source:62.10032.001
2nd source:62.10032.031

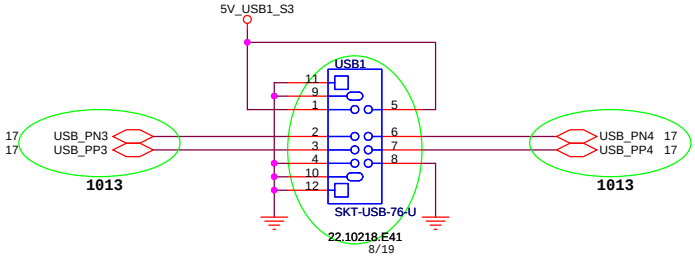
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MINI-PCI	
Size A3	Document Number Leopard	Rev -2
Date: Thursday, December 09, 2004	Sheet 29 of 41	

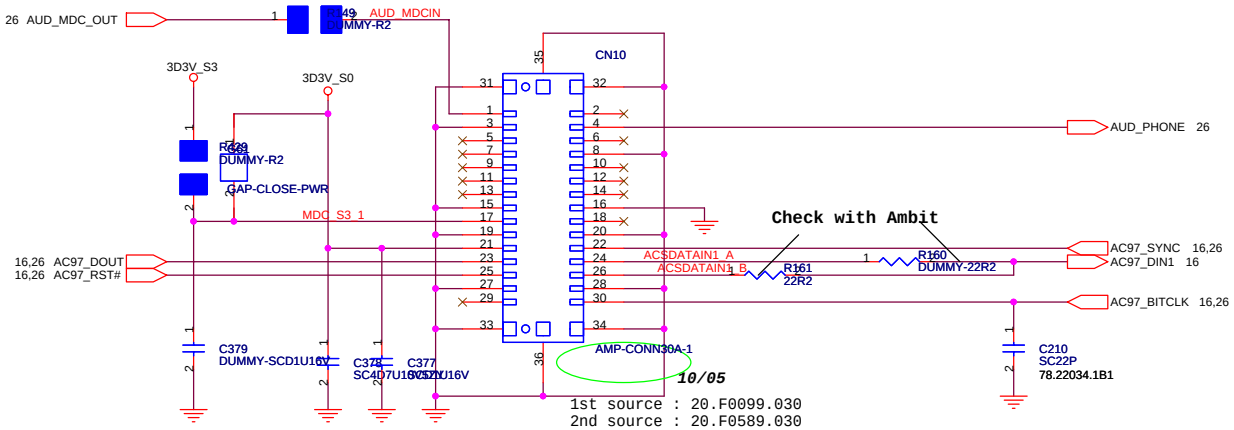
USB POWER



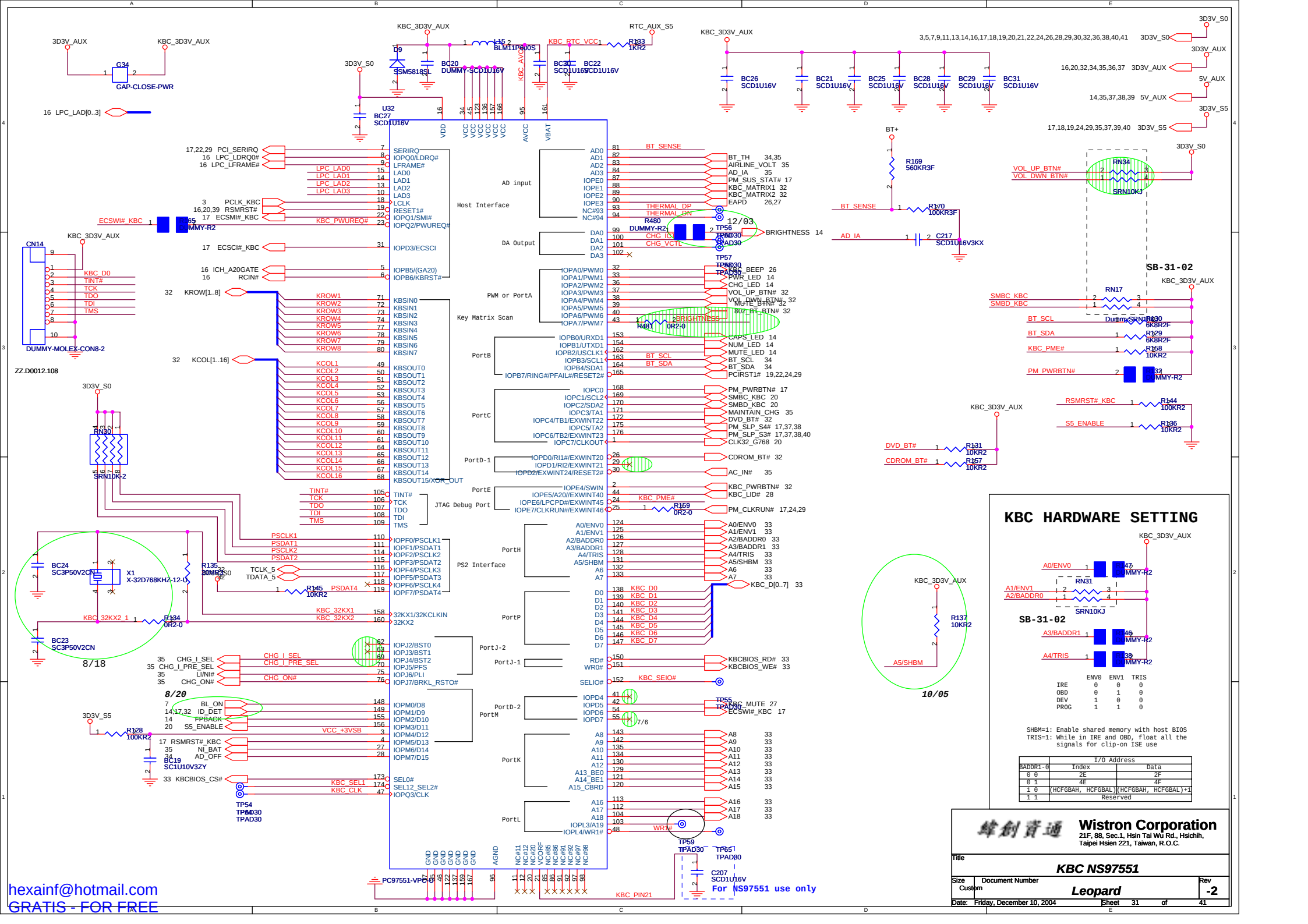




MDC Connector



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB / MDC CONN.		
Size: A3	Document Number: Leopard	Rev: -2
Date: Thursday, December 09, 2004	Sheet 30 of 41	


KBC HARDWARE SETTING
SB-31-02
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC NS97551
Leopard
-2
Friday, December 10, 2004
Sheet 31 of 41
For NS97551 use only
hexainf@hotmail.com
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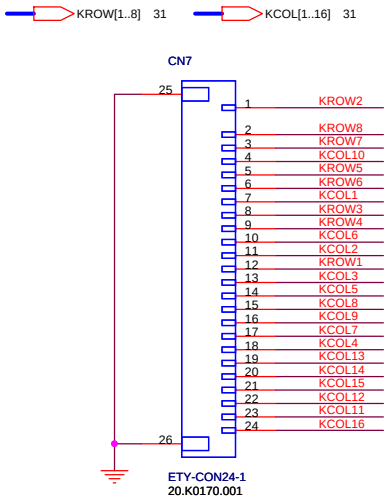
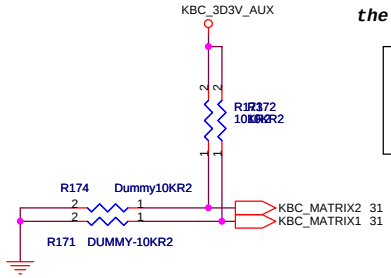
INTERNAL KEYBOARD CONNECTOR



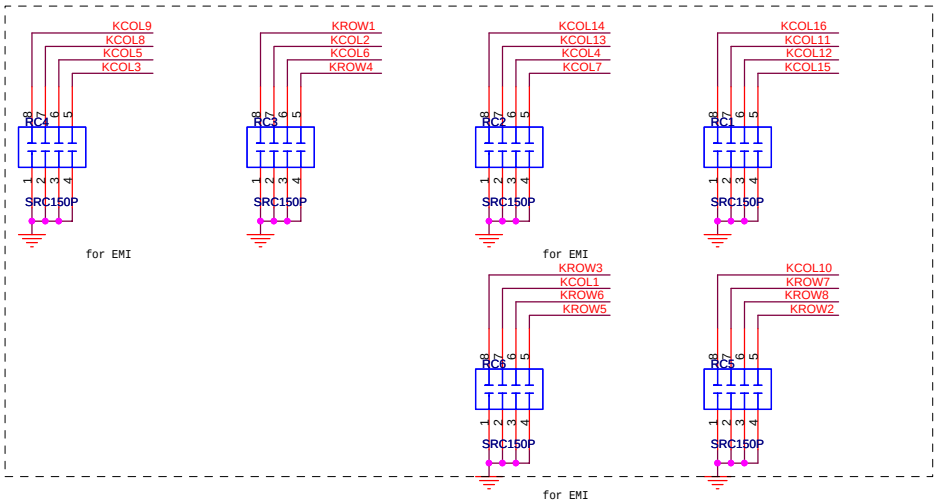


the matrix table for PCB

KBC_MATRIX2,KBC_MATRIX1

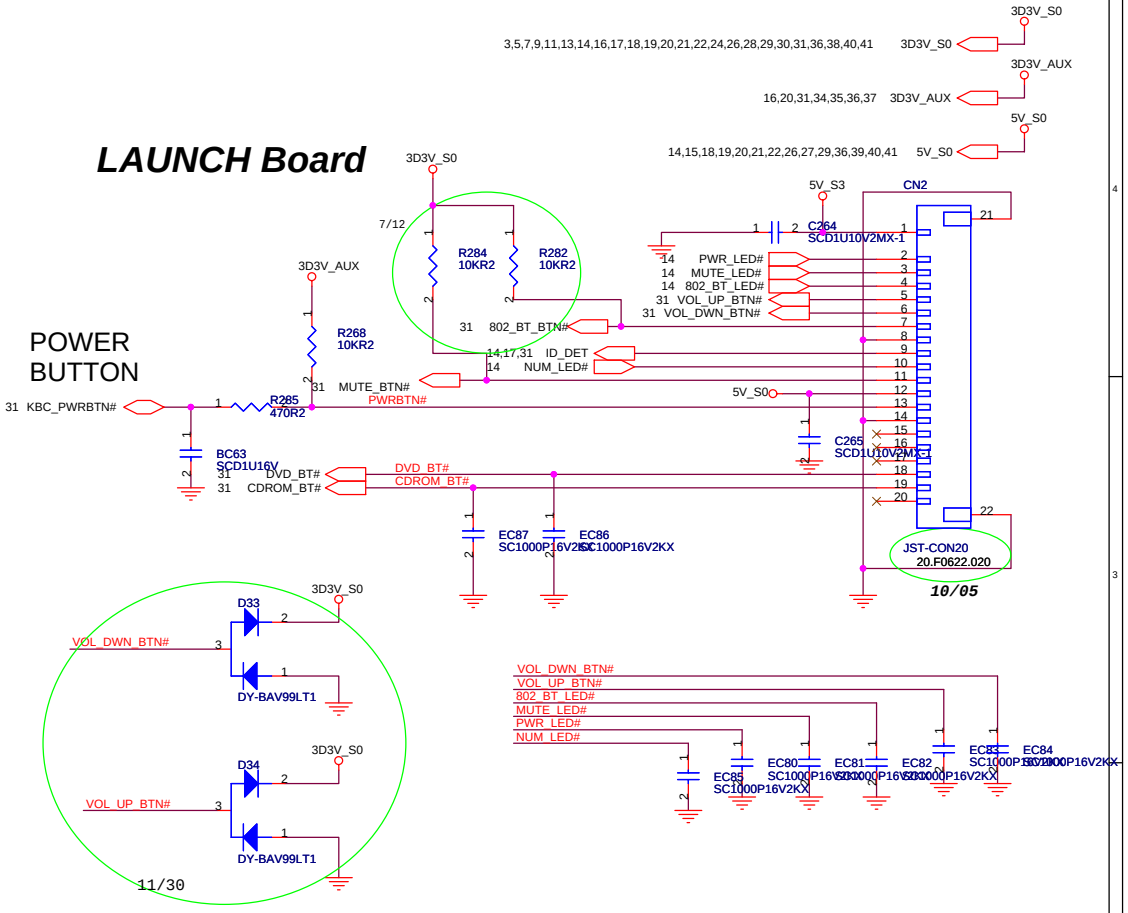
	PA	PR
FF	00	01
DF	10	11

	NONE Quick Play	Quick Play
MATRIXID1#	0	1

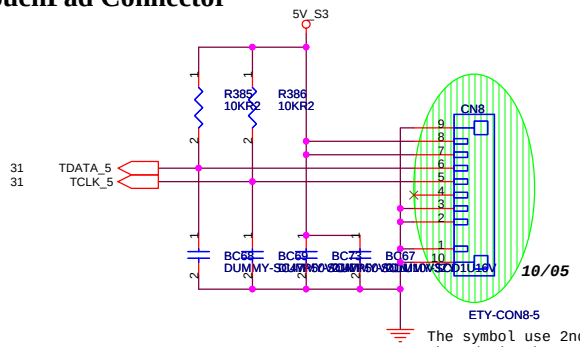


SB-32-01

LAUNCH Board



TouchPad Connector



The symbol use 2nd source
The P/N is the main source
Main source:20.D0151.108
2nd source:21.D0010.108

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***KEYBOARD/TOUCH PAD/Launch key***	
Size A3	Document Number ***Leopard***	Rev ***-2***
Date: Friday, December 10, 2004	Sheet 32 of 41	

3D3V_S0

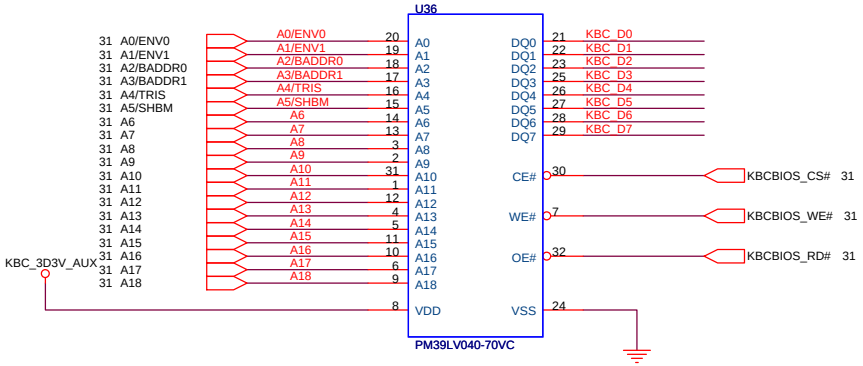
3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0

5V_S0

14,15,18,19,20,21,22,26,27,29,32,36,39,40,41 5V_S0

KBC_D[0..7] 31

512KB Flash



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BIOS/GF***	
Size A3	Document Number ***Leopard***	Rev **-2**
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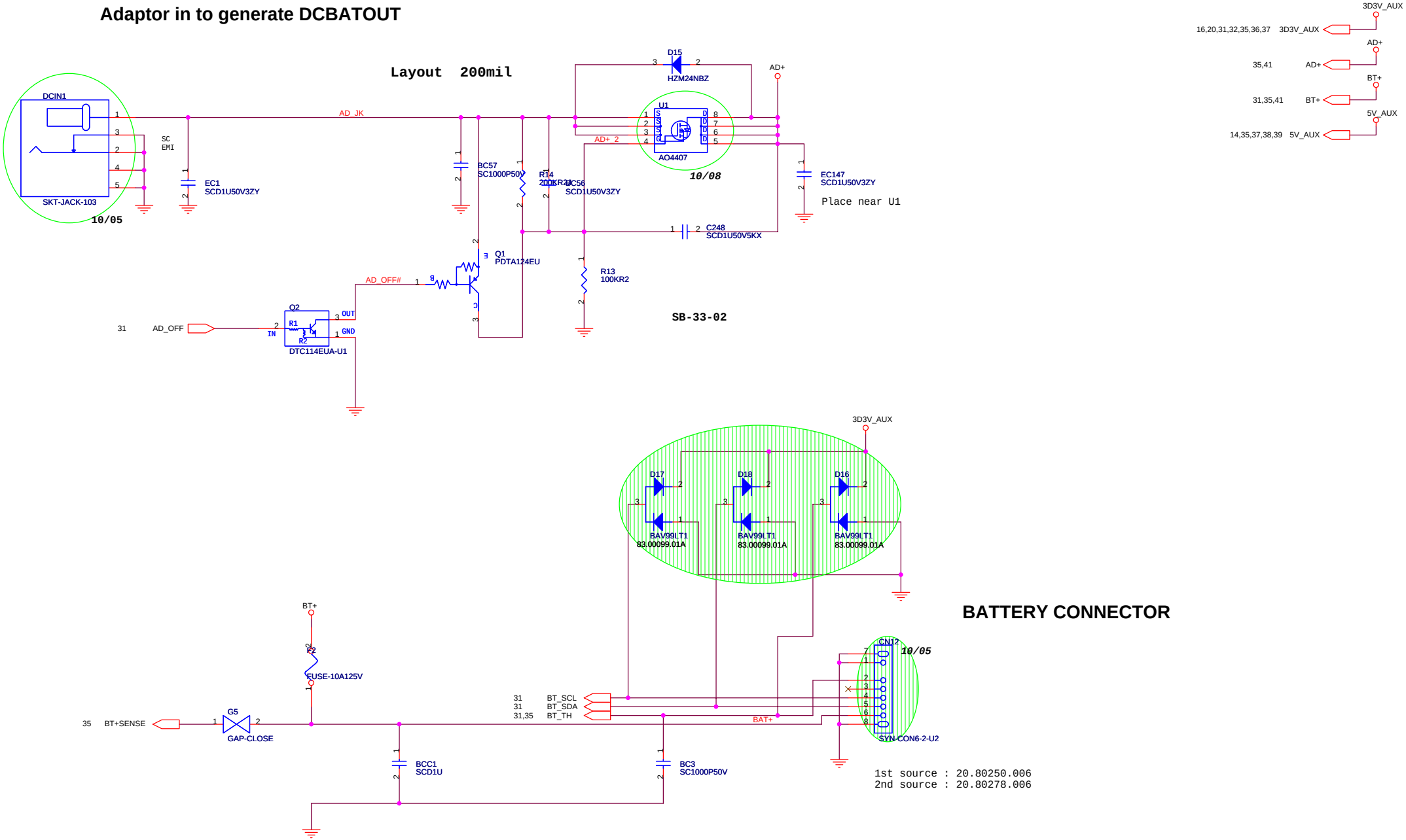
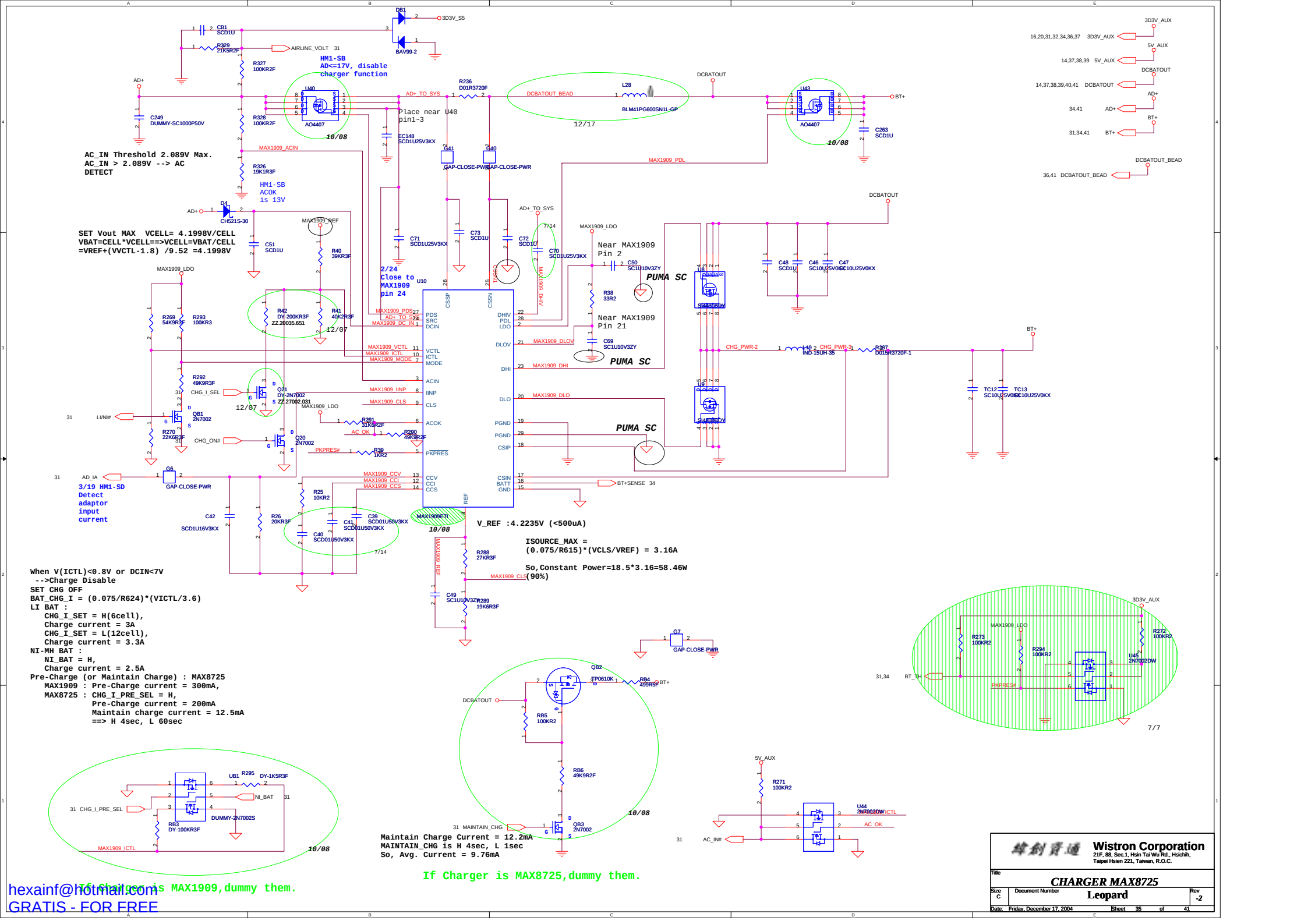
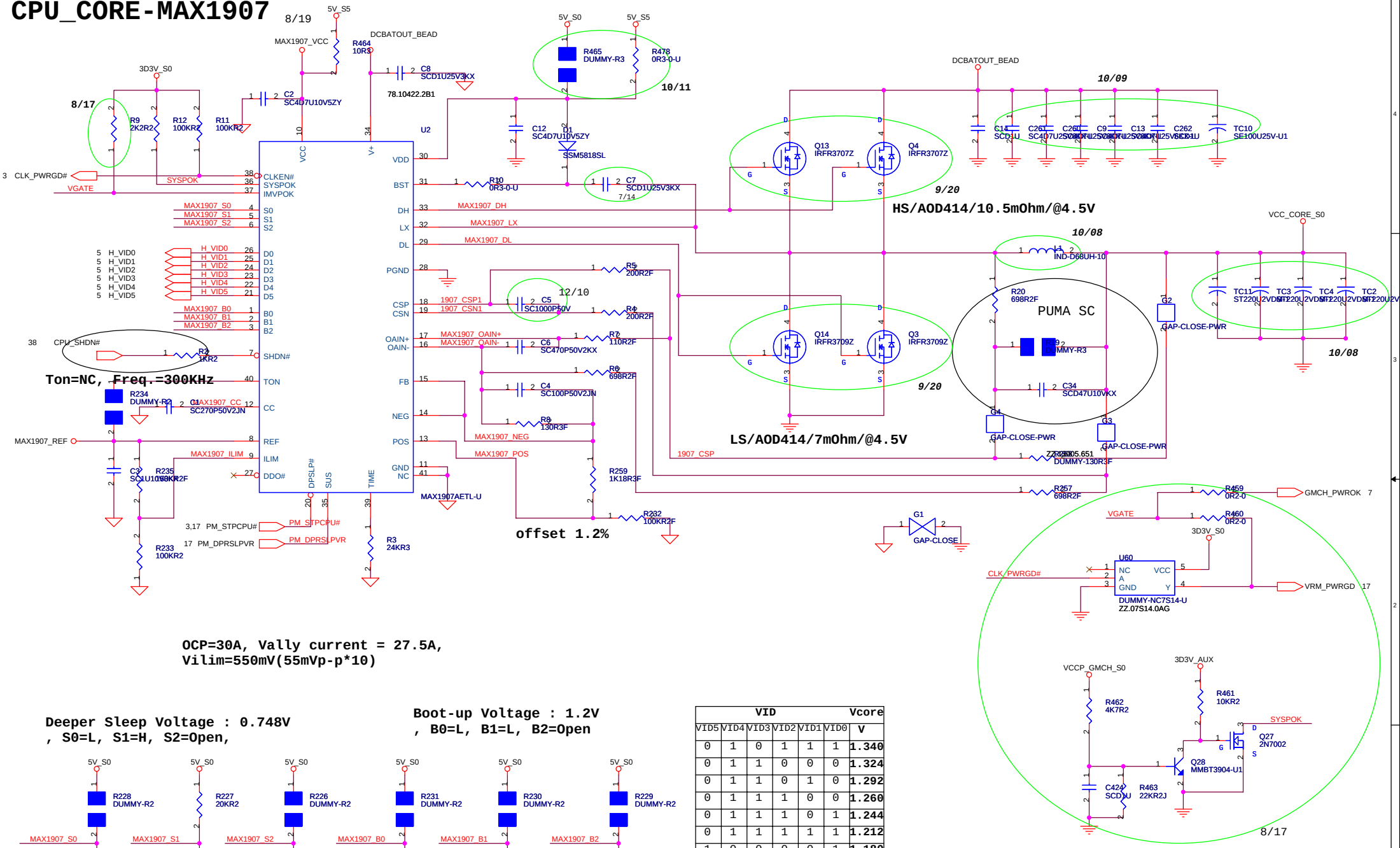
Adaptor in to generate DCBATOUT



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Adaptor/ Bettery conn.*		
Size: A3	Document Number: Leopard	Rev: -2
Date: Thursday, December 09, 2004	Sheet 34 of 41	



CPU_CORE-MAX1907



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: IMVP IV-CPU POWER-MAX1907

Size: A3 | Document Number: Leopard | Rev: -2

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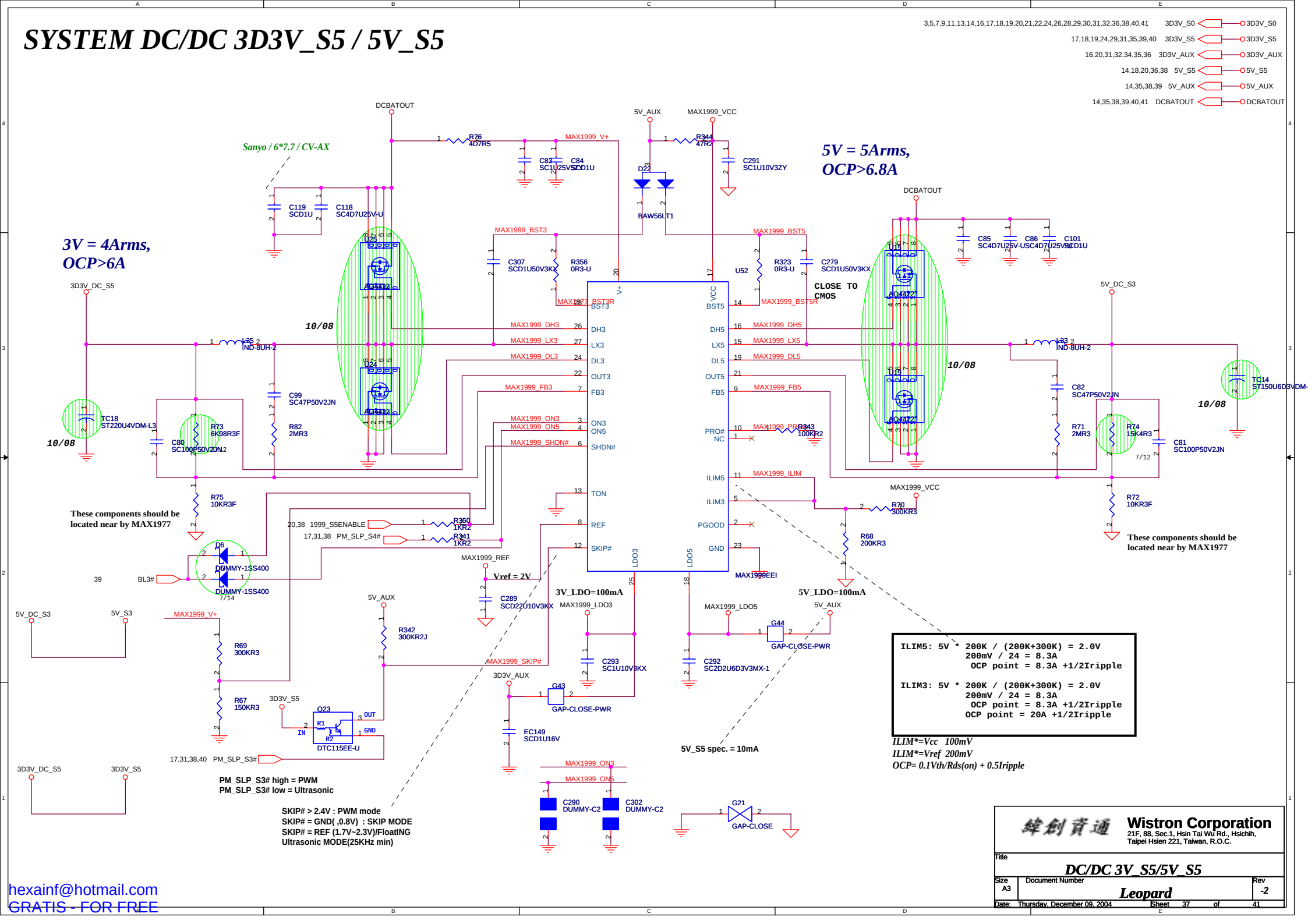
SYSTEM DC/DC 3D3V_S5 / 5V_S5



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC/DC 3V_S5/5V_S5	
Size A3	Document Number Leopard	Rev -2
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TI TPS5130 for 2.5V, 1.5V, 1.05V.

(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)

For 1.5V
SETTING=1.517V

PWM_1D5V
R372 680R2
C318 SC4700P50V2KX
R374 10KR3F
R369 7K87R2F
R368 8K9R2F
C319 SC4700P50V2KX
5130_INV1
5130_FB1

7/30

For 2.5V
SETTING=2.516V

PWM_2D5V
R370 680R2
C317 SC5600P25V2KX
R375 10K2R3F
R371 20KR2F
R373 2KR2F
C320 SC3300P50V2KX
5130_INV2
5130_FB2

For 1.05V
SETTING=1.061V

PWM_1D05V
R353 680R2
C304 SC5600P25V2KX
R355 80K6R3F
R352 20KR2F
R354 2K7R2J
C305 SC3300P50V2KX
5130_INV3
5130_FB3

7/12

OCP_1.05V

5130_TRIP1
R367 15KR3
C316 SCD1U16V3KX
DCBATOUT
close to IC

OCP_2.5V

5130_TRIP2
R366 20KR3
C315 SCD1U16V3KX
DCBATOUT
close to IC

OCP_1D5V

5130_TRIP3
R361 20KR3
C303 SCD1U16V3KX
DCBATOUT
close to IC

G28 GAP-CLOSE

5V_DC_S5
D27 BAW56
83.00056.A11

5130_LH1
C113 SCD1U50V5KX
5130_LL1
5130_LL1 39

5130_OUT1U
5130_OUT1D
5130_OUT1U 39
5130_OUT1D 39

5130_TRIP1
5130_TRIP2
DCBATOUT

5130_OUT2D
5130_OUT2D 39

5130_FLT
C114 SCD01U16V3KX

5130_FLT
5130_INV1

U23

INV1 FLT LH1 OUT1_LL1 OUT1_D OUTGND1 TRIP1 VIN_SENSE1.2 TRIP2 OUTGND2 OUT2_D

5130_LH2
C112 SCD1U50V5KX
5130_LL2
5130_LL2 39

close to IC

5130_FB1
5130_SS_STBY1
5130_INV2
5130_FB2
5130_SS_STBY2
5130_PWM_SEL
5130_CT
5130_REF
STBY_REF
R349 1KR3
7/14

FB1 SS_STBY1 INV2 FB2 SS_STBY2 PWM_SEL CT GND REF STBY_VREF5 STBY_VREF3.3 STBY_LDO

TPS5130

LL2 OUT2_U LH2 VIN VREF3.3 VREF5 REG5V_IN LDO_IN LDO_CUR LDO_GATE LDO_OUT INV_LDO

5130_OUT2U
5130_OUT2U 39
C314 SCD1U
DCBATOUT
5V_DC_S5
5V_S5
G51 GAP-CLOSE-PWR
C96 SC4D7U10V5ZY
R477 0R2-0
5V_S3
C425 SCD1U

10/11

SS_STBY3 FB3 INV3 PGOUT PG_DELAY TRIP3 VIN_SENSE3 LH3 OUT3_U LL3 OUT3_D OUTGND3

For 1.5V
SETTING=1.505V

TPS5130PT-U

5130_CT
C115 SC47P50V2JN

5130_SS_STBY3
5130_FB3
5130_INV3

5130_OUT3D
5130_LL3
5130_OUT3U
5130_OUT3D 39
5130_OUT3U 39
C98 SC1000P25V
5130_LH3
C97 SCD1U50V5KX
5130_LL3
5130_LL3 39

5130_REF
C100 SCD1U16V3KX

D26
5V_DC_S5
7/8
DCBATOUT
BAT54-1

5130_TRIP3
3D3V_S0
R162 10KR2
20 VCCP_PWGD
8/17
PM_SLP_S3#
U34A
TSLCX08-U
CPU_SHDN# 36
R479 100KR2
10/11

HW Thermal Throttling

5V_AUX
R320 100KR2
U49 2N7002DW
PM_SLP_S3#
5130_SS_STBY1
C117 SC1500P50V3KX
20,37 1999_S5ENABLE

5V_AUX
R321 100KR2
U48 2N7002DW
PM_SLP_S4# 17,31,37
5130_SS_STBY2
C116 SC4700P50V3KX

5V_AUX
R322 100KR2
U51 2N7002DW
PM_SLP_S3#
5130_SS_STBY3
C306 SC1500P50V3KX

5V_AUX
R340 300KR2J
5130_PWM_SEL
17,31,37,40 PM_SLP_S3#
Q22 DTC115EE-U
R1 IN
R2 OUT GND

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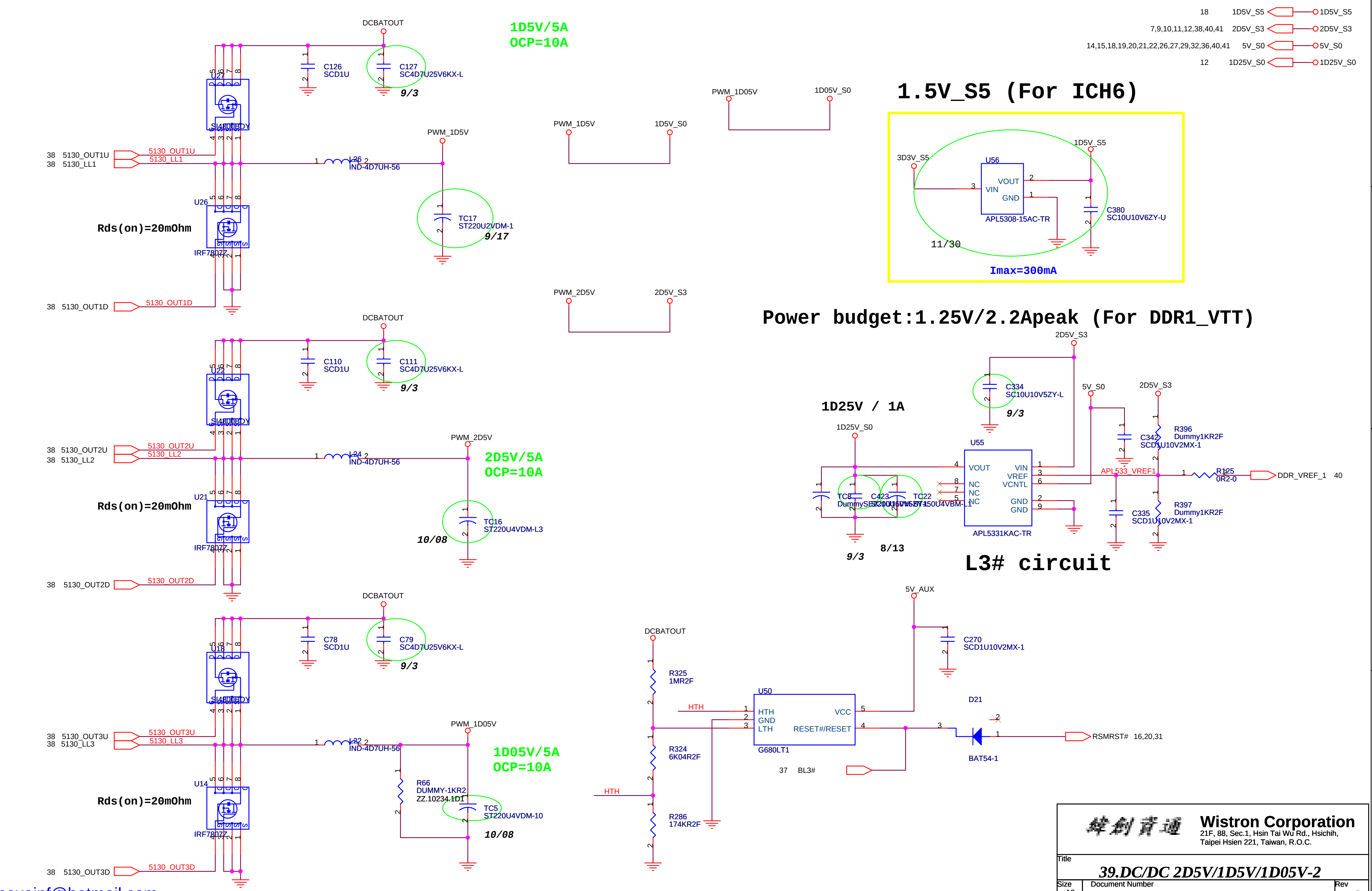
TI TPS5130 for 2.5V, 1.5V, 1.05V

(2D5V=>CH1 , 3D3V=>CH2 , 5V =>CH3)



14,35,37,38,40,41 DCBATOUT DCBATOUT
17,18,19,24,29,31,35,37,40 3D3V_S5 3D3V_S5
14,35,37,38 5V_AUX 5V_AUX
18 1D5V_S5 1D5V_S5
7,9,10,11,12,38,40,41 2D5V_S3 2D5V_S3
14,15,18,19,20,21,22,26,27,29,32,36,40,41 5V_S0 5V_S0
12 1D25V_S0 1D25V_S0
1D5V/5A
OCP=10A
2D5V/5A
OCP=10A
1D05V/5A
OCP=10A
Rds(on)=20mOhm
Rds(on)=20mOhm
Rds(on)=20mOhm
38 5130_OUT1U
38 5130_LL1
38 5130_OUT1D
38 5130_OUT2U
38 5130_LL2
38 5130_OUT2D
38 5130_OUT3U
38 5130_LL3
38 5130_OUT3D
U27 SI4800BDY
U26 IRF7807Z
U22 SI4800BDY
U21 IRF7807Z
U18 SI4800BDY
U14 IRF7807Z
C126 SCD1U
C127 SC4D7U25V6KX-L
C110 SCD1U
C111 SC4D7U25V6KX-L
C78 SCD1U
C79 SC4D7U25V6KX-L
L26 IND-4D7UH-56
L24 IND-4D7UH-56
L22 IND-4D7UH-56
TC17 ST220U2VDM-1
TC16 ST220U4VDM-L3
TC5 ST220U4VDM-10
R66 DUMMY-1KR2 ZZ.10234.1D1
PWM_1D5V
PWM_2D5V
PWM_1D05V
1D5V_S0
2D5V_S3
1D05V_S0
9/3
9/17
10/08
1.5V_S5 (For ICH6)
3D3V_S5
1D5V_S5
U56
VIN VOUT GND
APL5308-15AC-TR
C380 SC10U10V6ZY-U
11/30
Imax=300mA
Power budget:1.25V/2.2Apeak (For DDR1_VTT)
1D25V / 1A
1D25V_S0
5V_S0
C334 SC10U10V5ZY-L
U55
VOUT NC NC NC VIN VREF VCNTL GND GND
APL5331KAC-TR
TC8 DummySE100U6V5BY
C423 SC10U10V6ZY
TC22 ST150U4VBM-L1
C342 SCD1U10V2MX-1
C335 SCD1U10V2MX-1
R396 Dummy1KR2F
R397 Dummy1KR2F
APL533_VREF1
R125 0R2-0
DDR_VREF_1 40
8/13
L3# circuit
DCBATOUT
5V_AUX
R325 1MR2F
R324 6K04R2F
R286 174KR2F
HTH
U50
HTH GND LTH VCC RESET#/RESET
G680LT1
37 BL3#
C270 SCD1U10V2MX-1
D21
BAT54-1
RSMRST# 16,20,31

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*39.DC/DC 2D5V/1D5V/1D05V-2*
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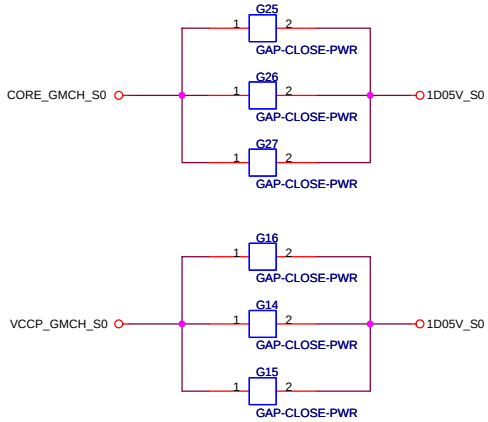
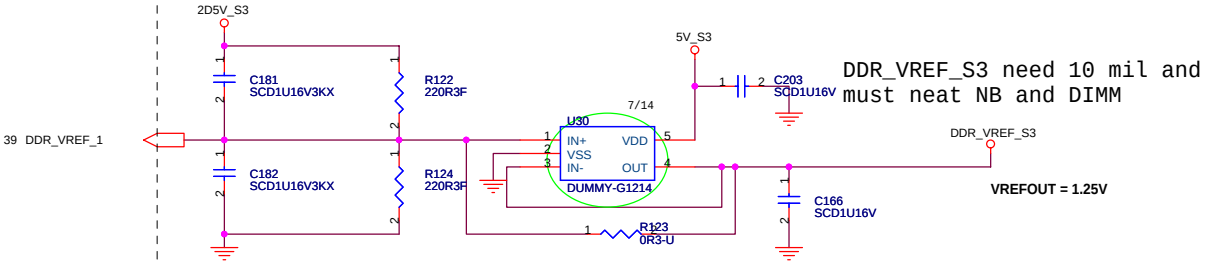
hexainf@hotmail.com

FOR GMCH Power

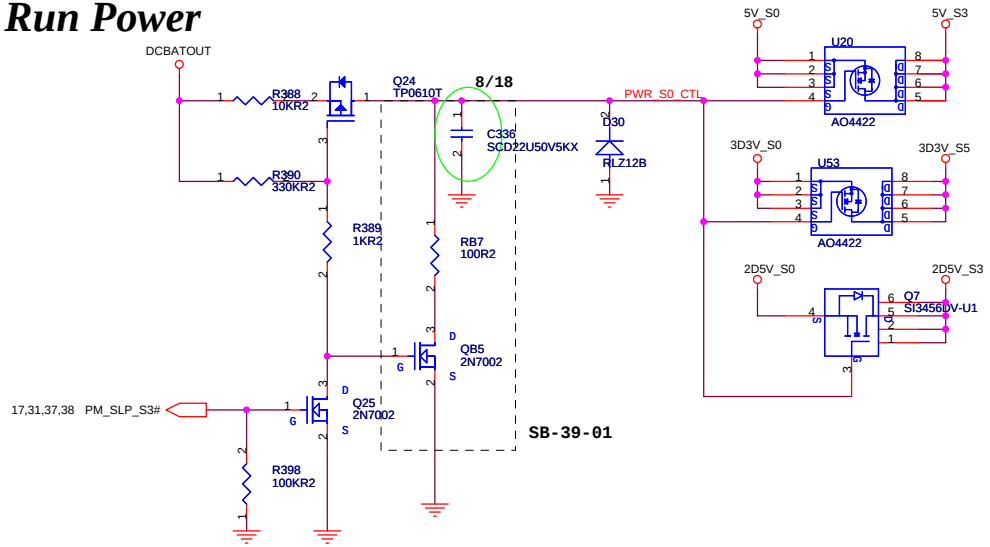


3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,28,29,30,31,32,36,38,41 3D3V_S0 — 3D3V_S0
28,30 3D3V_S3 — 3D3V_S3
17,18,19,24,29,31,35,37,39 3D3V_S5 — 3D3V_S5
14,15,18,19,20,21,22,26,27,29,32,36,39,41 5V_S0 — 5V_S0
14,25,30,32,37,38,41 5V_S3 — 5V_S3
14,18,20,36,38 5V_S5 — 5V_S5
7,9,15,18 2D5V_S0 — 2D5V_S0
7,9,10,11,12,38,39,41 2D5V_S3 — 2D5V_S3
7,11 DDR_VREF_S3 — DDR_VREF_S3
14,35,37,38,39,41 DCBATOUT — DCBATOUT
38,39,41 1D05V_S0 — 1D05V_S0
4,5,6,7,9,10,16,18,36,41 VCCP_GMCH_S0 — VCCP_GMCH_S0
6,9,10,41 CORE_GMCH_S0 — CORE_GMCH_S0

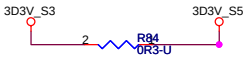


FOR DDR Power

Run Power



Suspend Power



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Title	**PWRPLANE&RESETLOGIC**	
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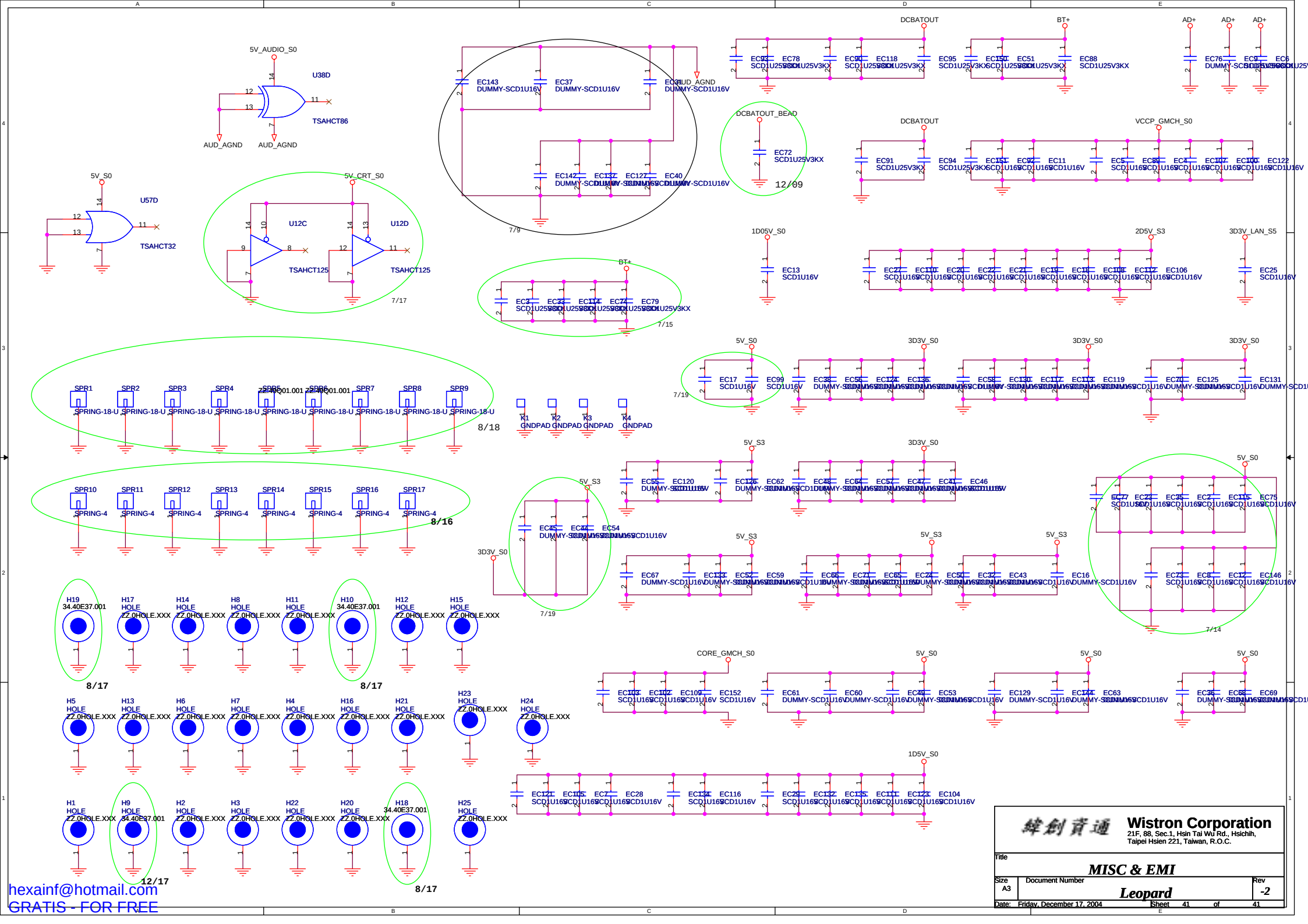
5V_AUDIO_S0
U38D
TSAHCT86
AUD_AGND
AUD_AGND
DCBATOUT
BT+
AD+
AD+
AD+
EC143 DUMMY-SCD1U16V
EC37 DUMMY-SCD1U16V
EC23 DUMMY-SCD1U16V
AUD_AGND
EC142 DUMMY-SCD1U16V
EC137 DUMMY-SCD1U16V
EC127 DUMMY-SCD1U16V
EC40 DUMMY-SCD1U16V
7/9
DCBATOUT_BEAD
EC72 SCD1U25V3KX
12/09
DCBATOUT
VCCP_GMCH_S0
EC91 SCD1U25V3KX
EC94 SCD1U25V3KX
5V_S0
U57D
TSAHCT32
5V_CRT_S0
U12C
U12D
TSAHCT125
TSAHCT125
7/17
BT+
EC3 SCD1U25V3KX
EC79 SCD1U25V3KX
7/15
1D05V_S0
EC13 SCD1U16V
2D5V_S3
3D3V_LAN_S5
EC25 SCD1U16V
5V_S0
3D3V_S0
3D3V_S0
3D3V_S0
EC17 SCD1U16V
EC99 SCD1U16V
7/19
SPR1 SPRING-18-U
SPR2 SPRING-18-U
SPR3 SPRING-18-U
SPR4 SPRING-18-U
SPR5 SPRING-18-U
SPR6 SPRING-18-U
SPR7 SPRING-18-U
SPR8 SPRING-18-U
SPR9 SPRING-18-U
8/18
K1 GNDPAD
K2 GNDPAD
K3 GNDPAD
K4 GNDPAD
5V_S3
3D3V_S0
EC55 EC120
5V_S3
3D3V_S0
EC45 EC42 EC54
7/19
5V_S0
7/14
SPR10 SPRING-4
SPR11 SPRING-4
SPR12 SPRING-4
SPR13 SPRING-4
SPR14 SPRING-4
SPR15 SPRING-4
SPR16 SPRING-4
SPR17 SPRING-4
8/16
3D3V_S0
5V_S3
5V_S3
5V_S3
EC67 DUMMY-SCD1U16V
EC16 DUMMY-SCD1U16V
H19 34.40E37.001
H17 HOLE ZZ.0HOLE.XXX
H14 HOLE ZZ.0HOLE.XXX
H8 HOLE ZZ.0HOLE.XXX
H11 HOLE ZZ.0HOLE.XXX
H10 34.40E37.001
H12 HOLE ZZ.0HOLE.XXX
H15 HOLE ZZ.0HOLE.XXX
8/17
8/17
CORE_GMCH_S0
5V_S0
5V_S0
5V_S0
EC103 EC102 EC109 EC152 SCD1U16V
EC61 DUMMY-SCD1U16V
EC129 DUMMY-SCD1U16V
EC63 DUMMY-SCD1U16V
EC36 EC58 EC69
H5 HOLE ZZ.0HOLE.XXX
H13 HOLE ZZ.0HOLE.XXX
H6 HOLE ZZ.0HOLE.XXX
H7 HOLE ZZ.0HOLE.XXX
H4 HOLE ZZ.0HOLE.XXX
H16 HOLE ZZ.0HOLE.XXX
H21 HOLE ZZ.0HOLE.XXX
H23 HOLE ZZ.0HOLE.XXX
H24 HOLE ZZ.0HOLE.XXX
1D5V_S0
EC121 EC105 EC7 EC28 EC134 EC116 EC29 EC132 EC135 EC111 EC123 EC104
H1 HOLE ZZ.0HOLE.XXX
H9 HOLE 34.40E37.001
H2 HOLE ZZ.0HOLE.XXX
H3 HOLE ZZ.0HOLE.XXX
H22 HOLE ZZ.0HOLE.XXX
H20 HOLE ZZ.0HOLE.XXX
H18 34.40E37.001
H25 HOLE ZZ.0HOLE.XXX
12/17
8/17
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
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MISC & EMI
Size A3
Document Number
Leopard
Rev -2
Date: Friday, December 17, 2004
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