

Compal confidential

Schematics Document

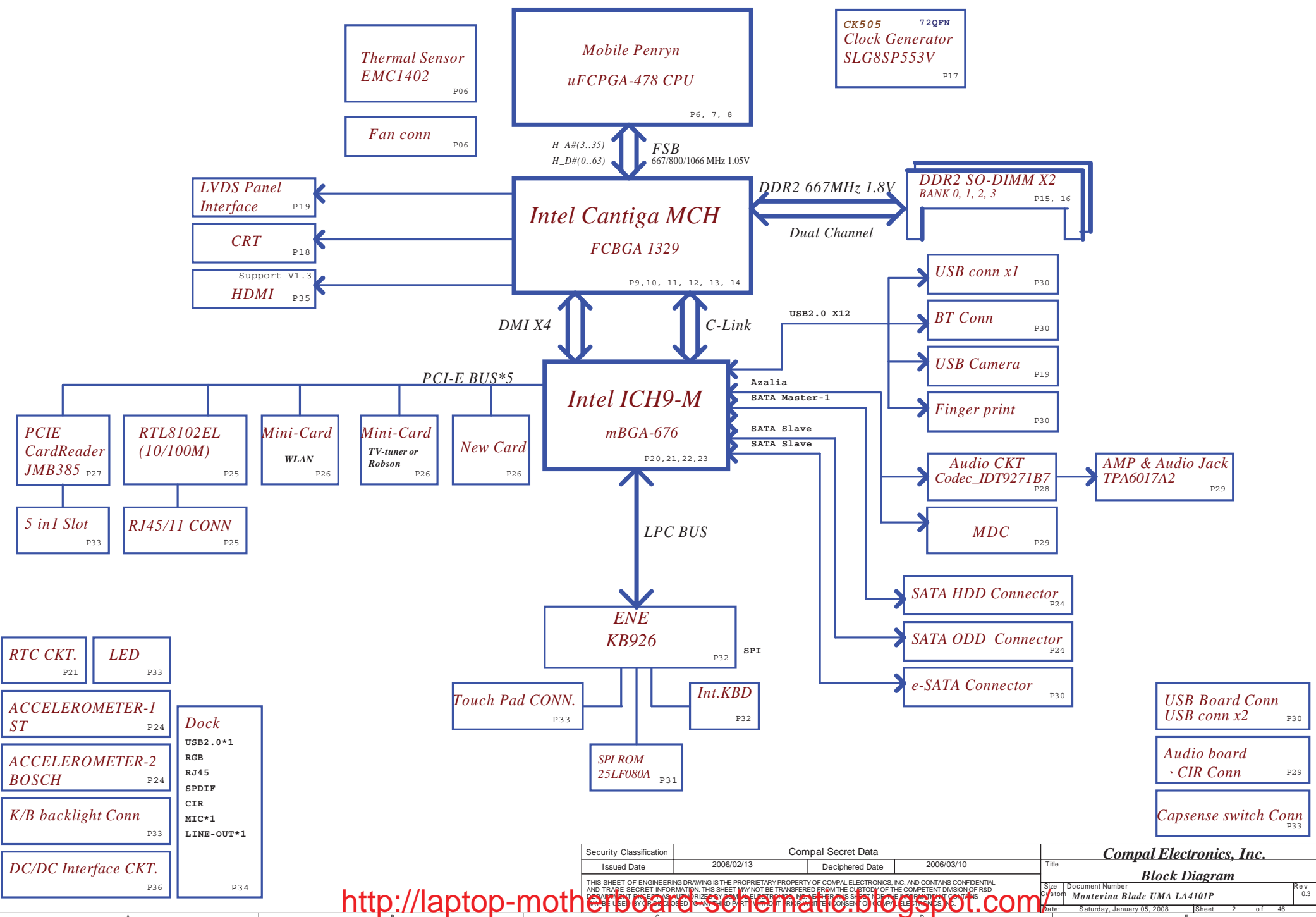
Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M core logic

2008-01-01

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	產出人員	
	產出日期	
	解密日期	

Security Classification	Compal Secret Data			Title		
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Cover Sheet		
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				Cust	Montevina Blade UMA LA4101P	0.3
Date: Saturday, January 05, 2008				Sheet	1	of 46

Montevina Consumer 14" UMA

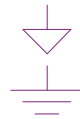


Voltage Rails

O MEANS ON X MEANS OFF

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



: means Digital Ground



: means Analog Ground

@ :	means just reserve , no build
45 @ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
DOCK@ :	means just reserve for Docking
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot

USB assignment:

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	Dock
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

PCIe-1	TV /WWAN/Robeson
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	Card reader
PCIe-6	New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

43154432L01 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/Multi@/2MiniC@
 43154432L02 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/2MiniC@
 43154432L03 : Main@/DEBUG@/DOCK@/NewC@/FP@/2MiniC@
 43154432L04 : OPP@/DEBUG@
 43154432L05 : OPP@/DEBUG@

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

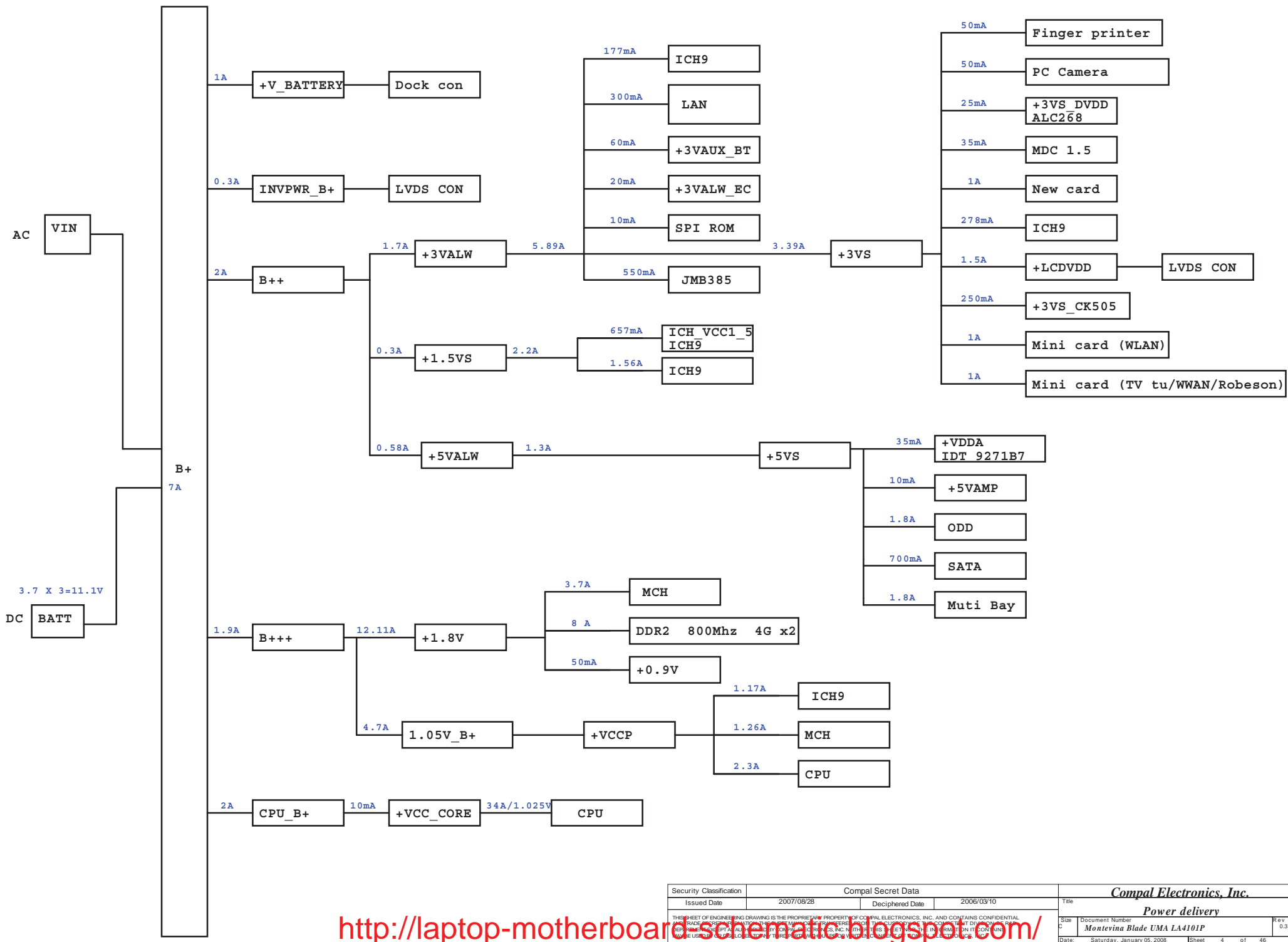
43154432L01 : UMA GM PA FF (SI-1)
 43154432L02 : UMA GM PR FF (SI-1)
 43154432L03 : UMA GL PR FF-
 43154432L04 : UMA GM OPP (SI-1)
 43154432L05 : UMA GL OPP

Cantiga GM45 B0(QR32) : SA00001P930
 ICH9M A2 ES2 Base : SA00002AN10

DA600007100 --->Main
 DAZ03V00100 --->OPP

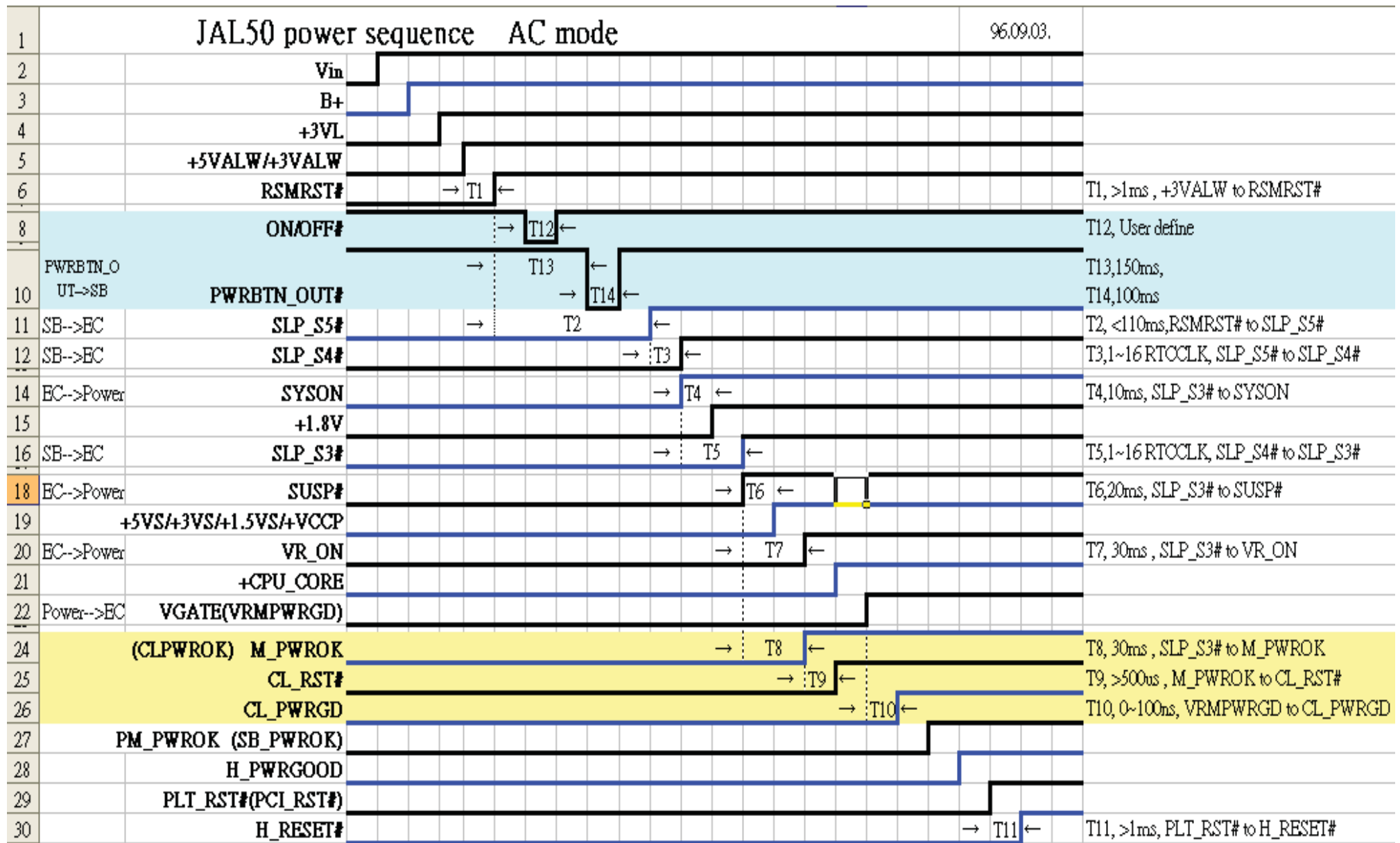
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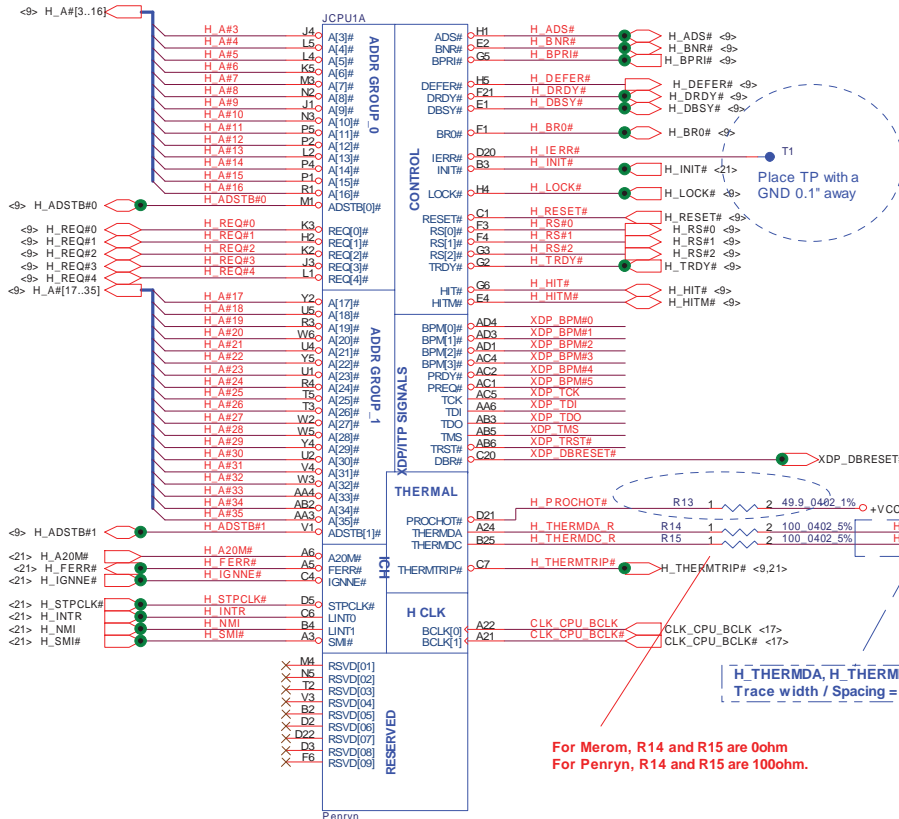
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Size	Document Number					Rev
	Montevina Blade UMA LA4101P					0.3
Date	Saturday, January 05, 2008			Sheet	3 of 46	



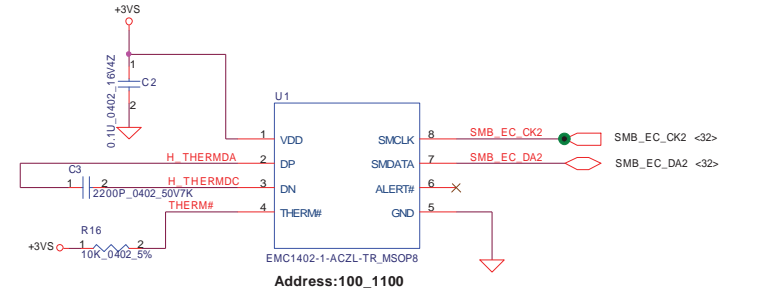
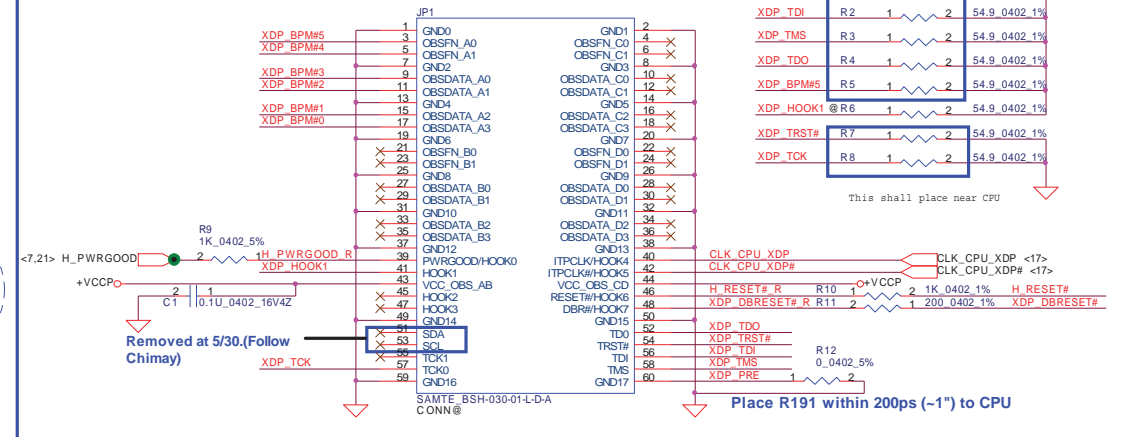
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C				03
Date	Saturday, January 05, 2008	Sheet	4	of 46

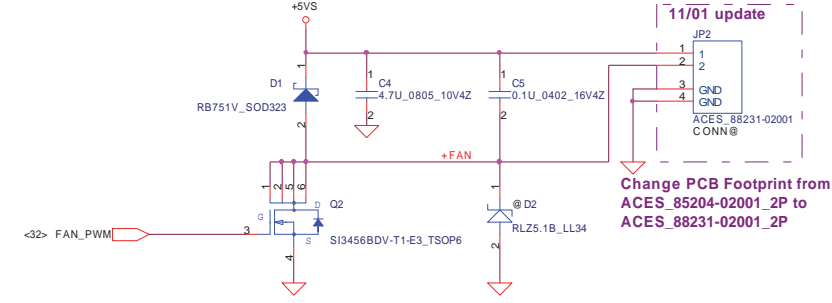




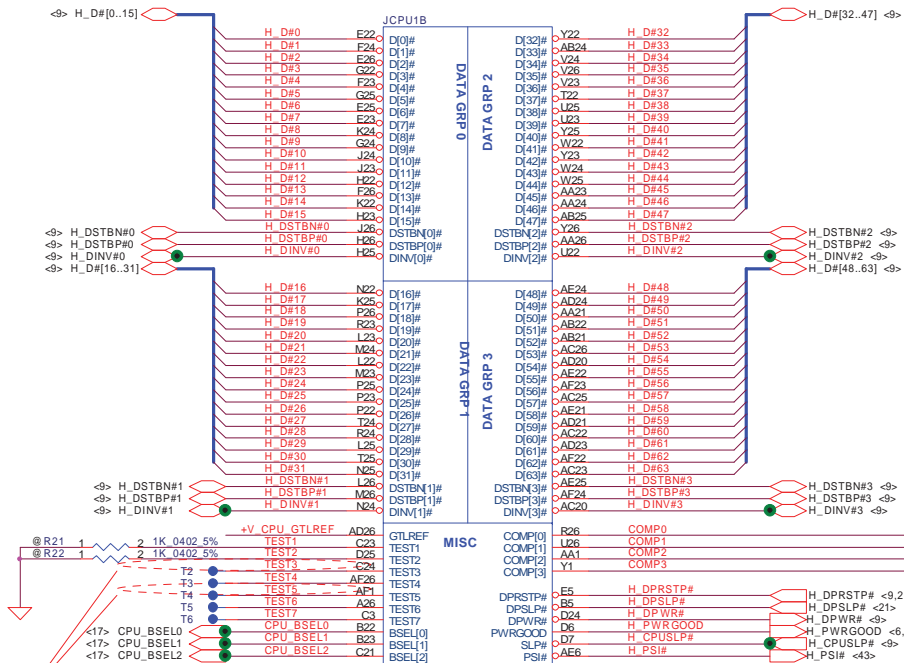
ITP-XDP Connector



PWM Fan Control circuit



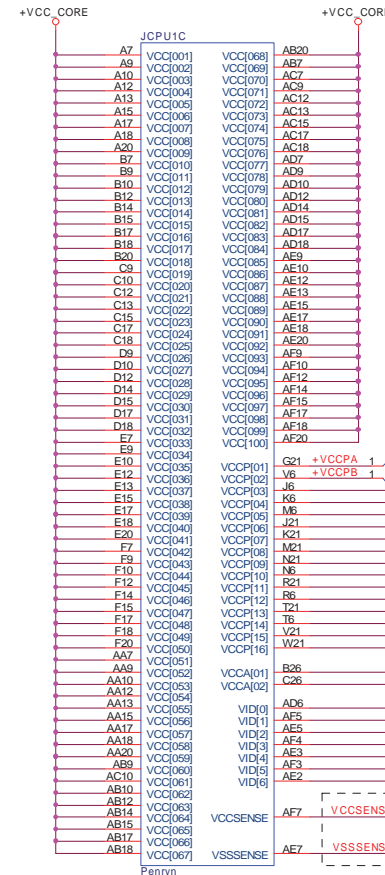
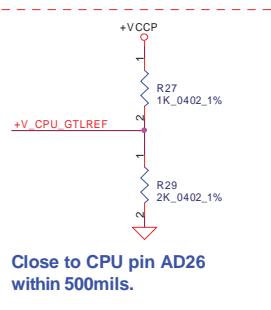
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Size	Document Number	Montevina Blade UMA LA4101P	Rev	0.3	
Date	Saturday, January 05, 2008	Sheet	6	of 46	



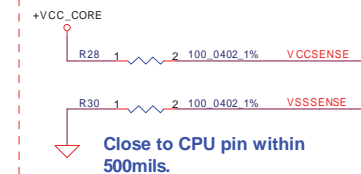
* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

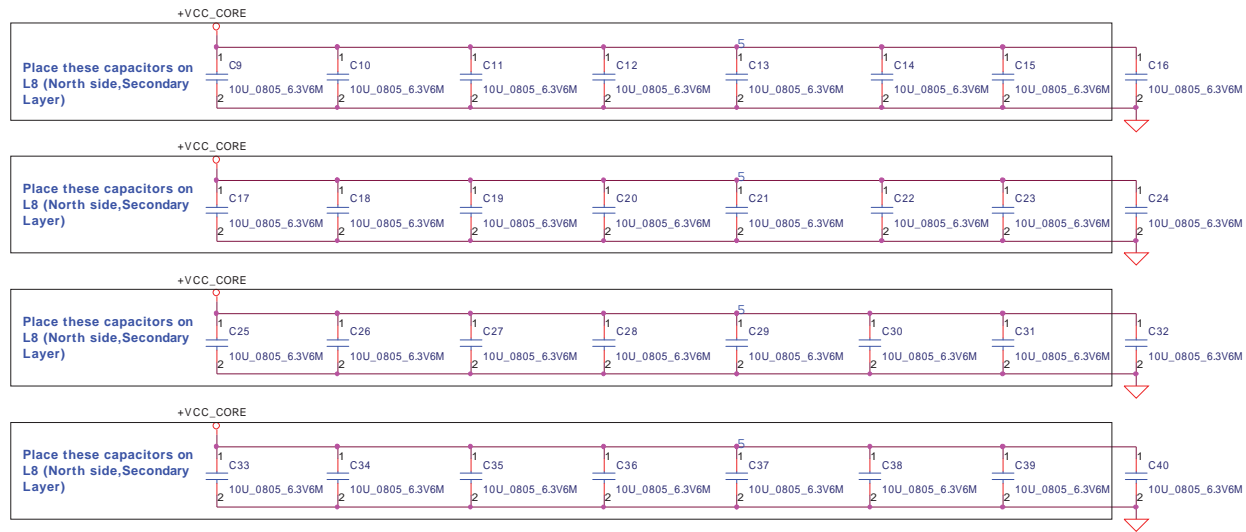
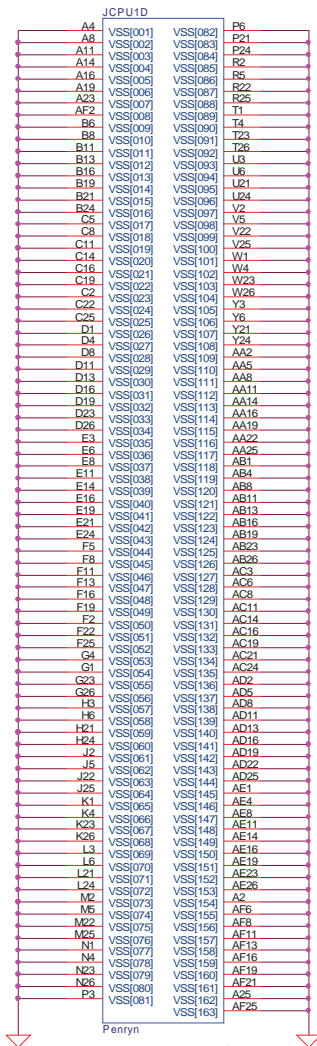
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.

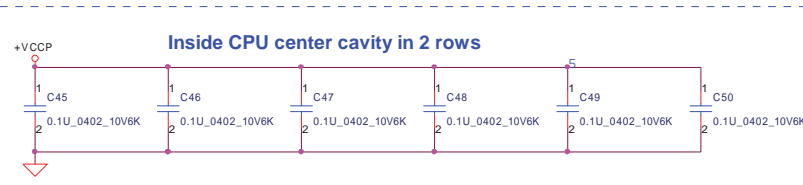
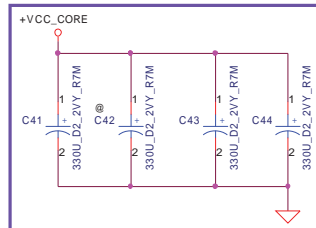




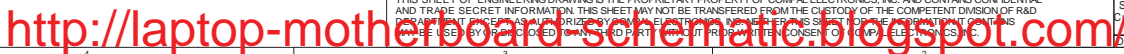
Mid Frequency Decoupling

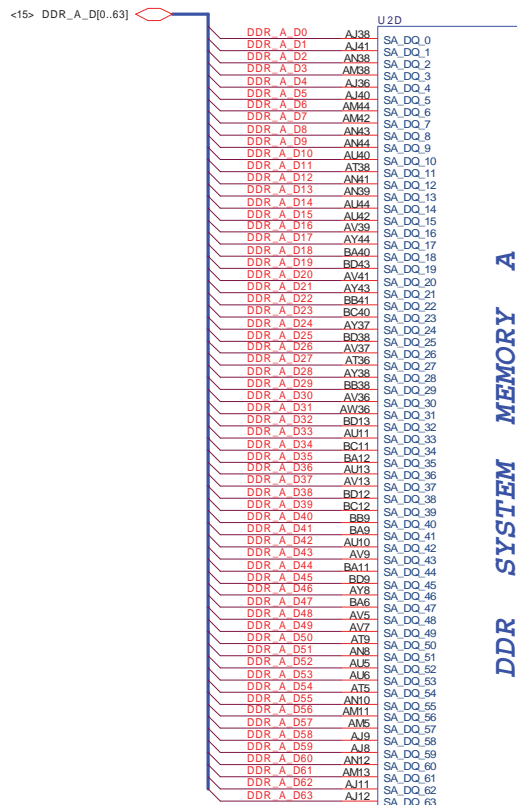
Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF

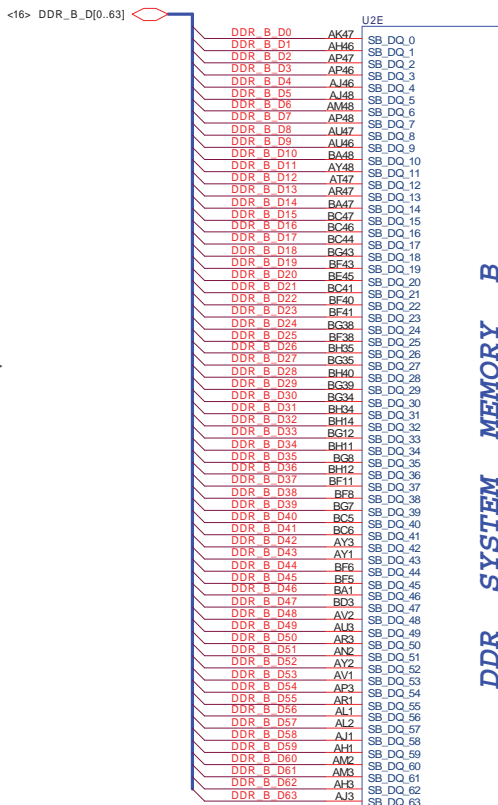
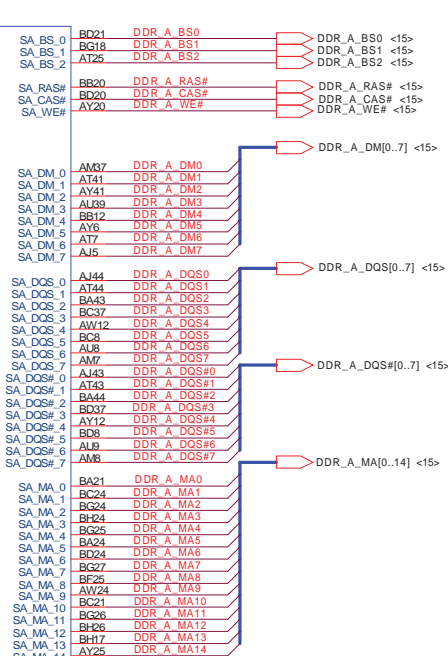


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				Date	Saturday, January 05, 2008
				Sheet	8 of 46
				Rev	0.3

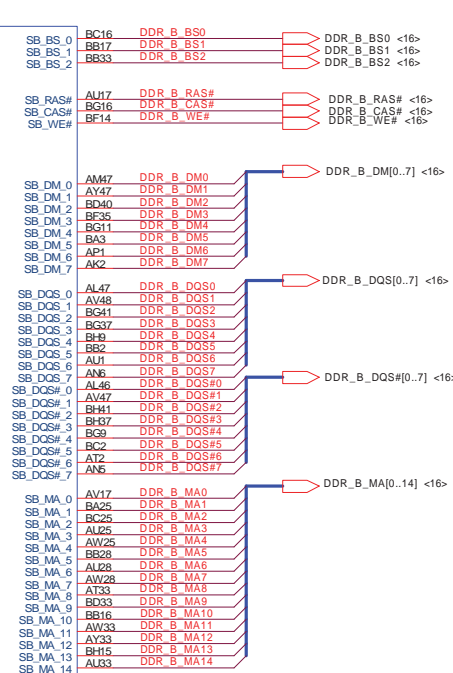




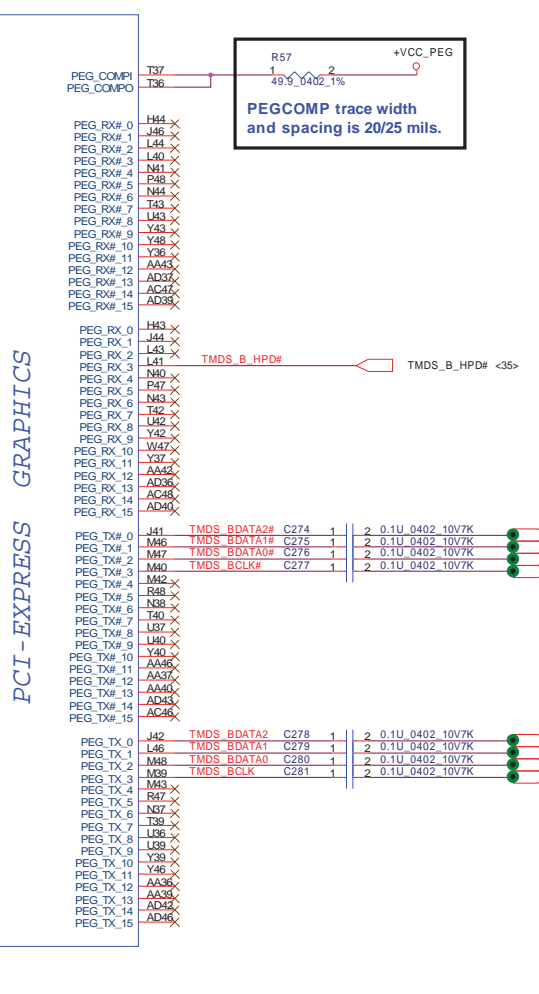
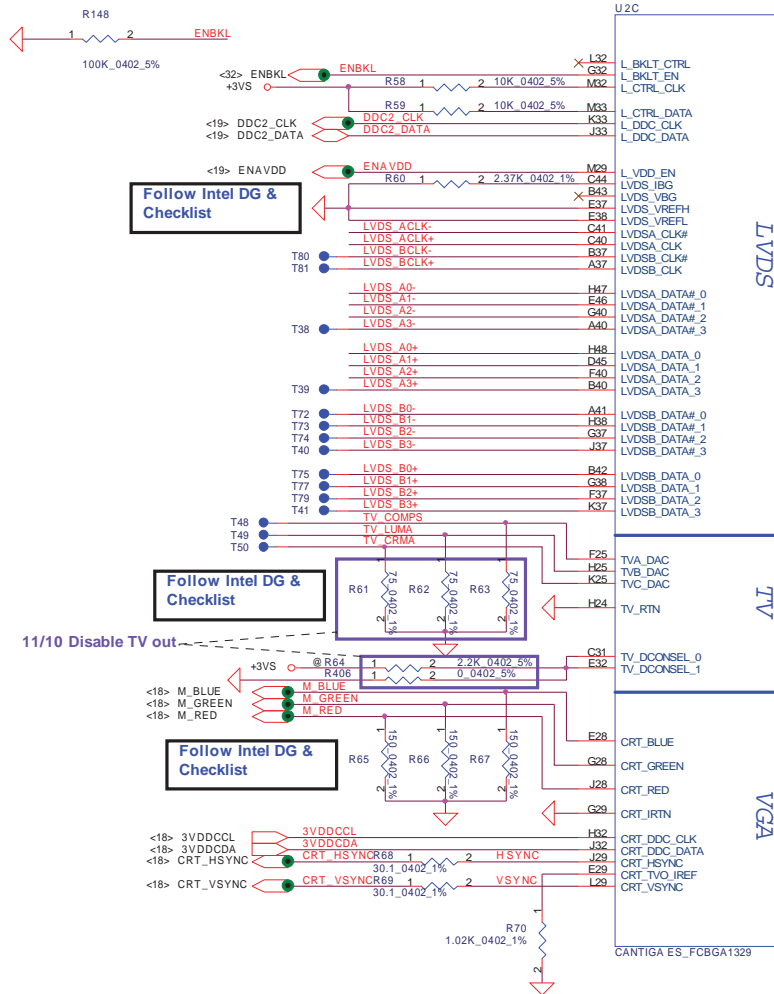
CANTIGA ES_FCBGA1329



CANTIGA ES_FCBGA1329



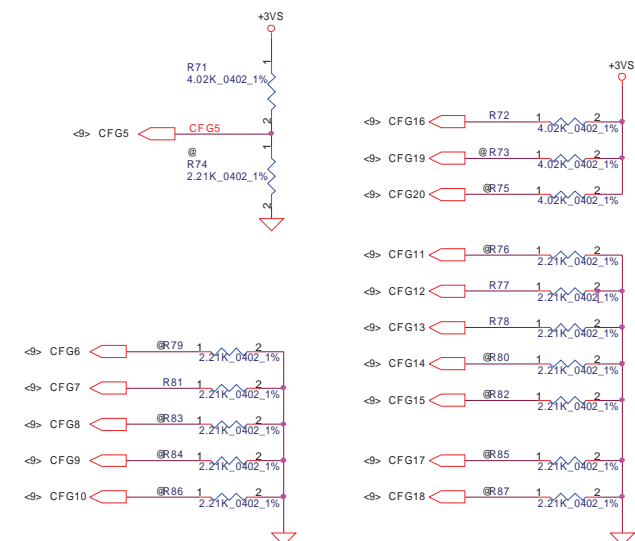
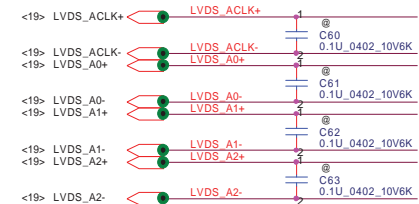
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				Size	Document Number
				Custom	Montevina Blade UMA LA4101P
				Date	Rev
				Saturday, January 05, 2008	0.3
				Sheet	10 of 46



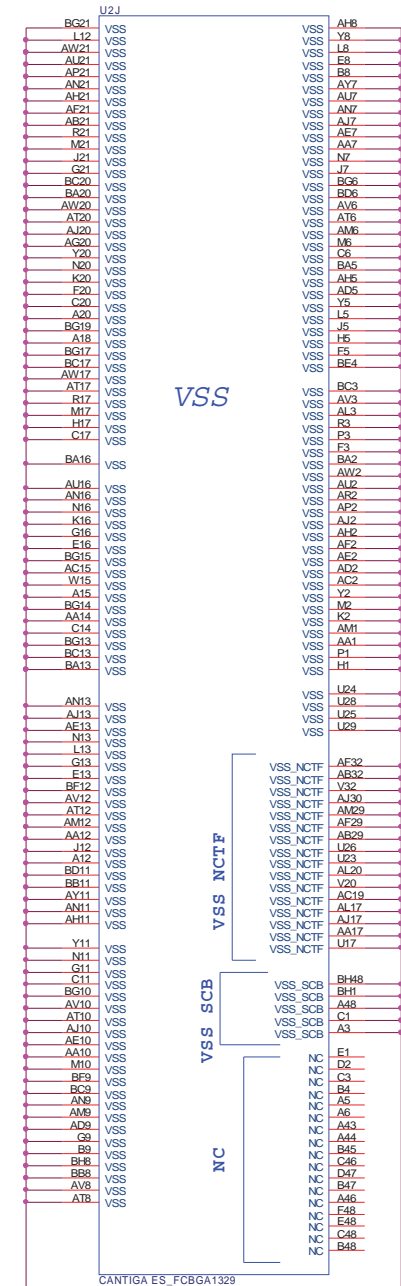
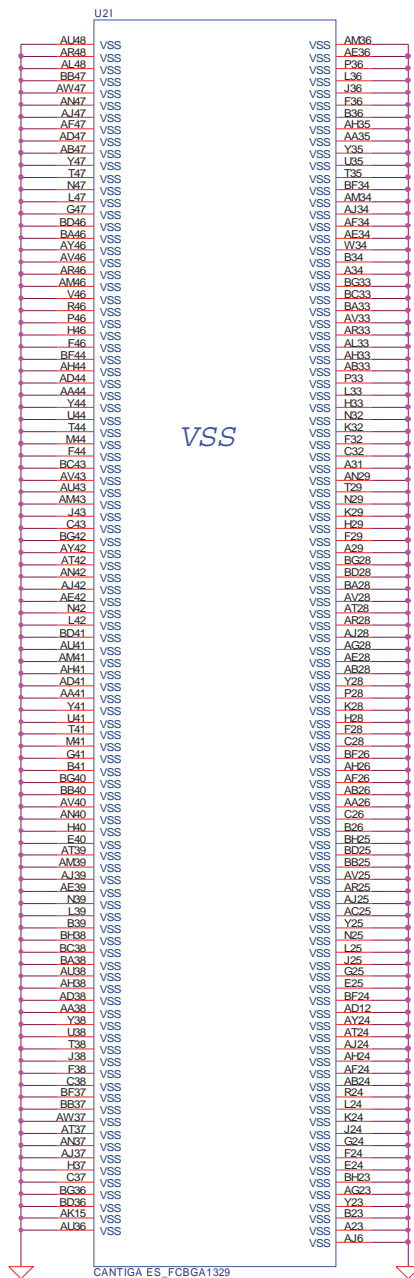
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

Solve 3G WWAN issue

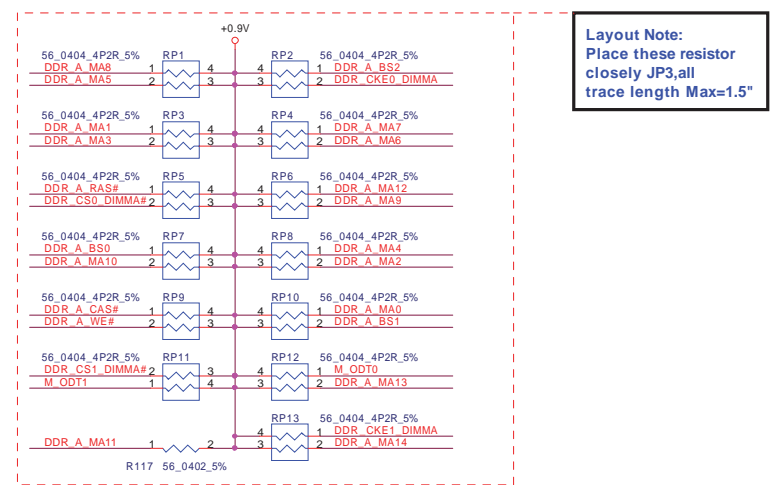


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				Rev 0.3
				Date: Saturday, January 05, 2008
				Sheet 11 of 46

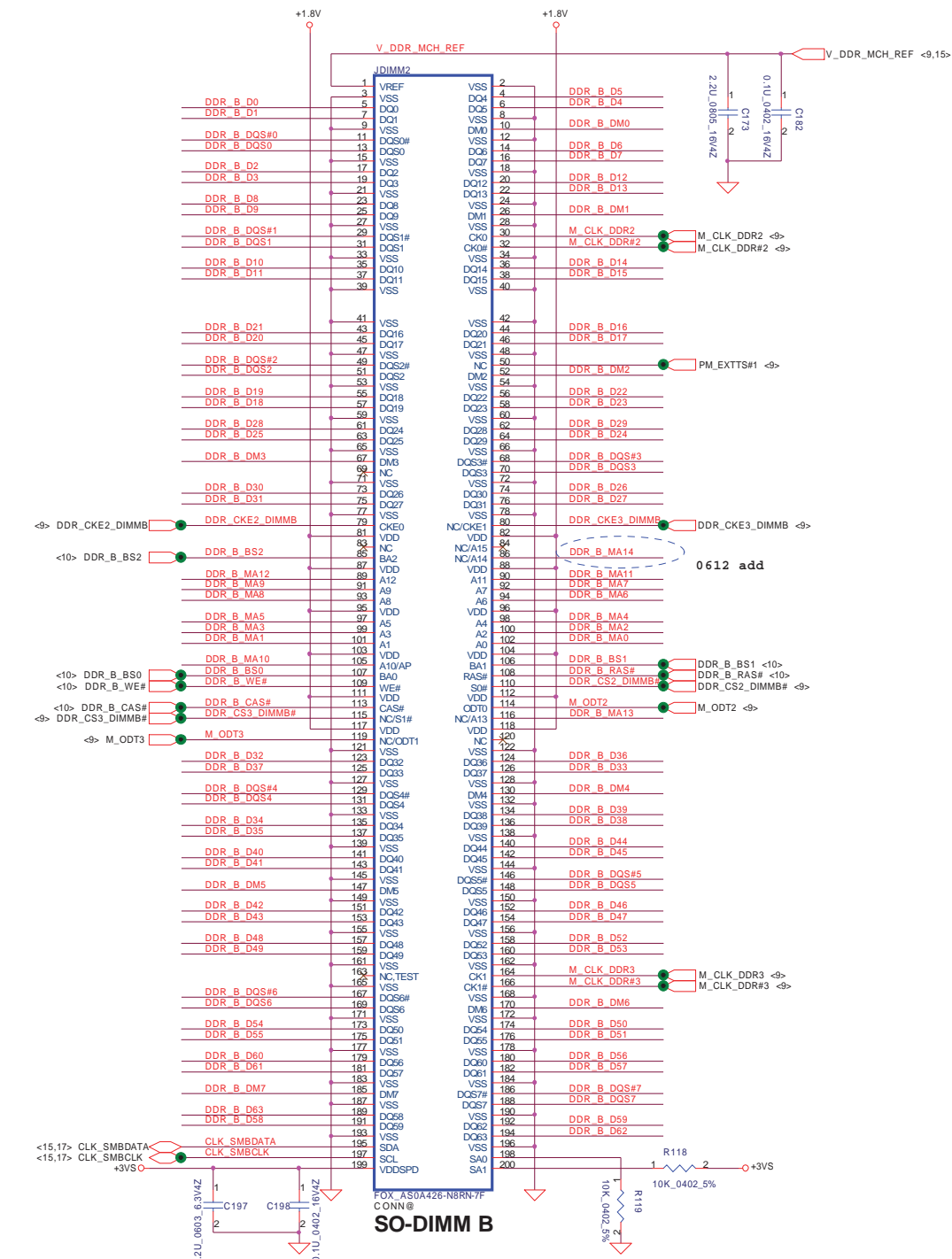
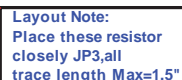
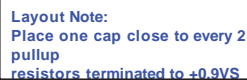


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Size		Document Number		Rev	
C		Montevina Blade UMA LA4101P		0.3	
Date:		Saturday, January 05, 2008		Sheet 14 of 46	

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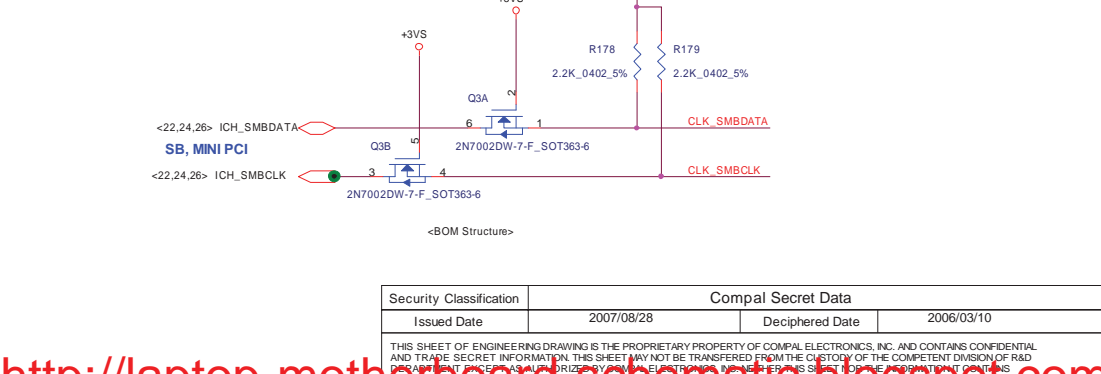
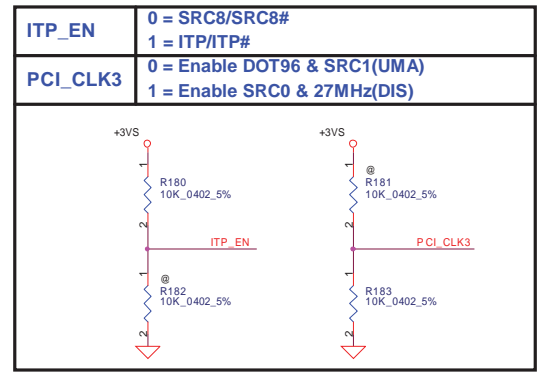
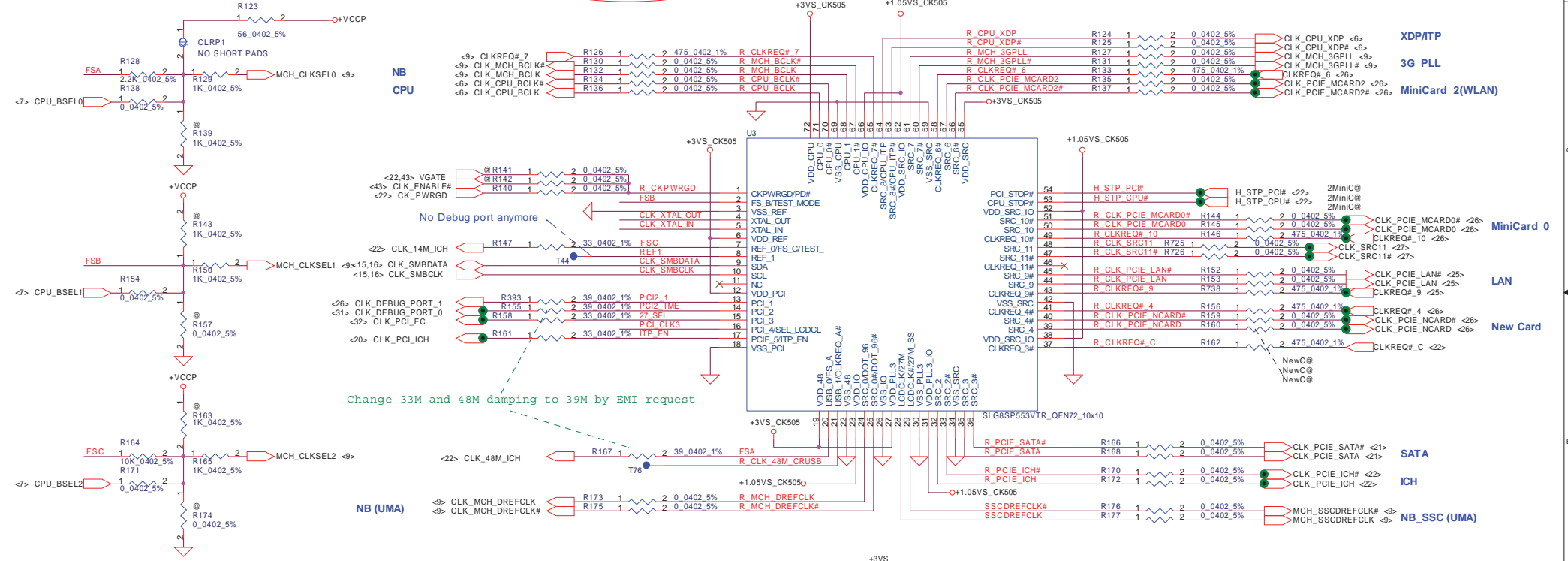
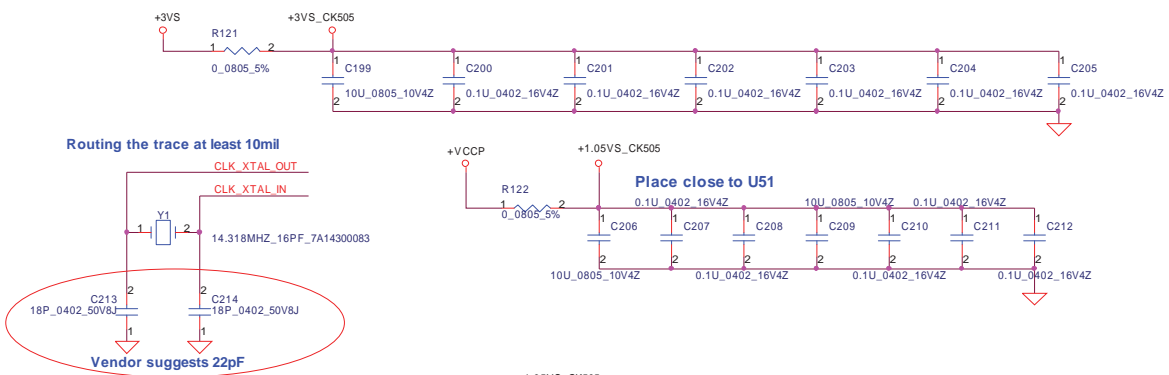


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				Disto	Montevina Blade UMA LA4101P	0.3
				Date:	Saturday, January 05, 2008	Sheet 15 of 46



Security Classification	Compal Secret Data			Compal Electronics, Inc. DDRII-SODIMM SLOT2		
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					Montevia Blade UMA LA4101P	0.3
				Date:	Saturday, January 05, 2008	Sheet 16 of 46

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								

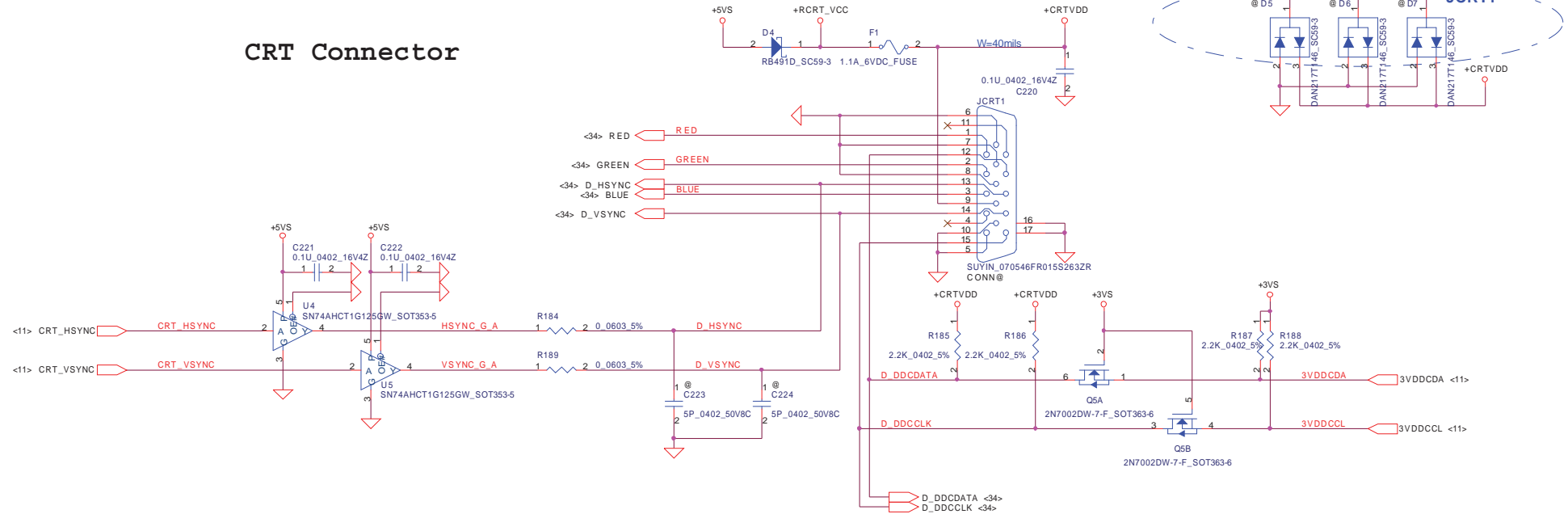


@C215	5P_0402_50V8C	2	1	CLK_48M_ICH
@C216	4.7P_0402_50V8C	2	1	CLK_14M_ICH
@C217	4.7P_0402_50V8C	2	1	CLK_PCI_ICH
@C218	4.7P_0402_50V8C	2	1	CLK_PCI_EC
@C219	5P_0402_50V8C	2	1	CLK_DEBUG_PORT_0

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Date: Saturday, January 05, 2008				Sheet 17 of 46

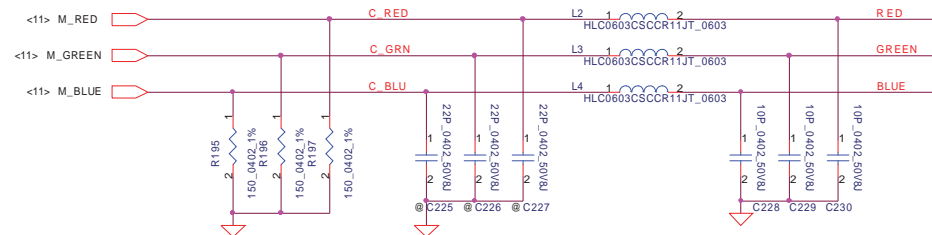
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CRT Connector

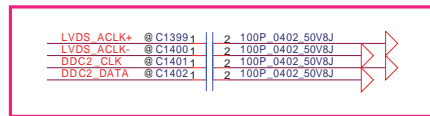
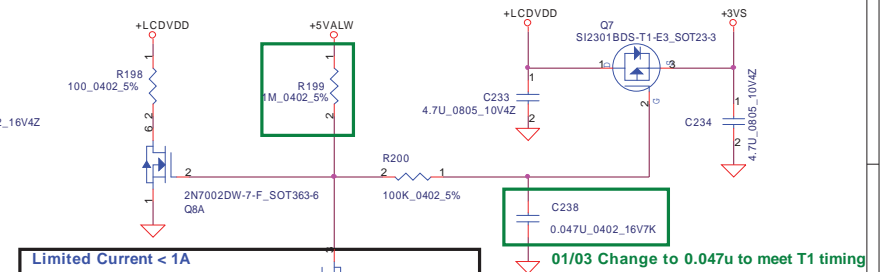
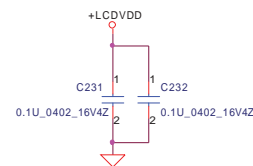
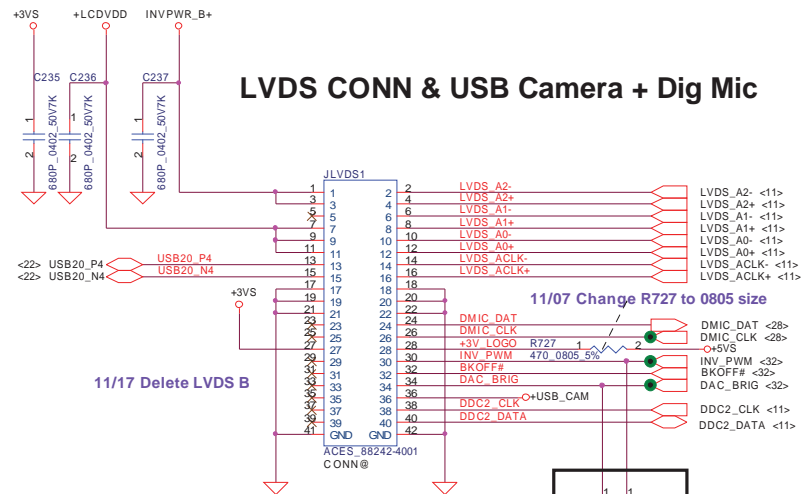


CRT Termination/EMI Filter

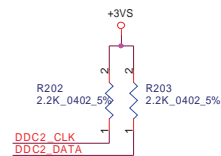
11/07 Change CRT louting NB-->Docking-->CRT connector



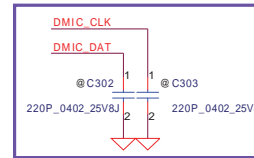
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					Montevina Blade UMA LA4101P
				Date:	Saturday, January 05, 2008
				Sheet	18 of 46
				Rev	0.3



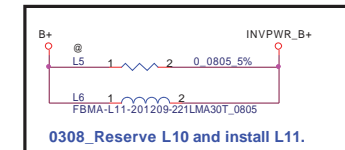
0831 EMI request



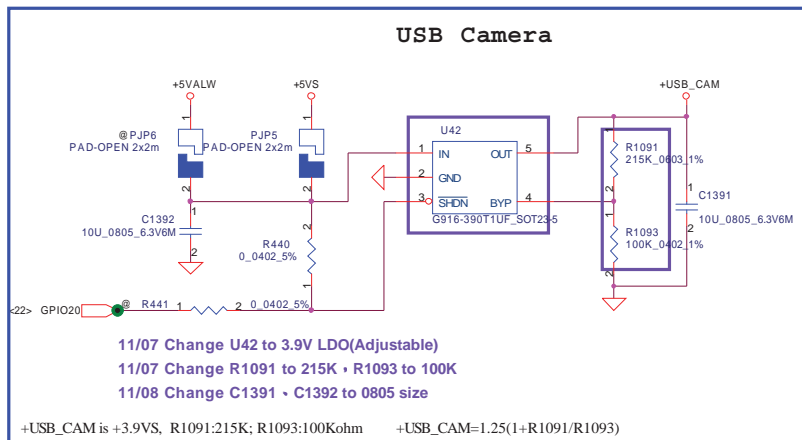
Must close JLVS1 pin 24 - 26



11/09 EMI reserver



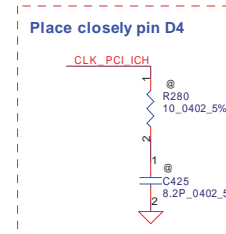
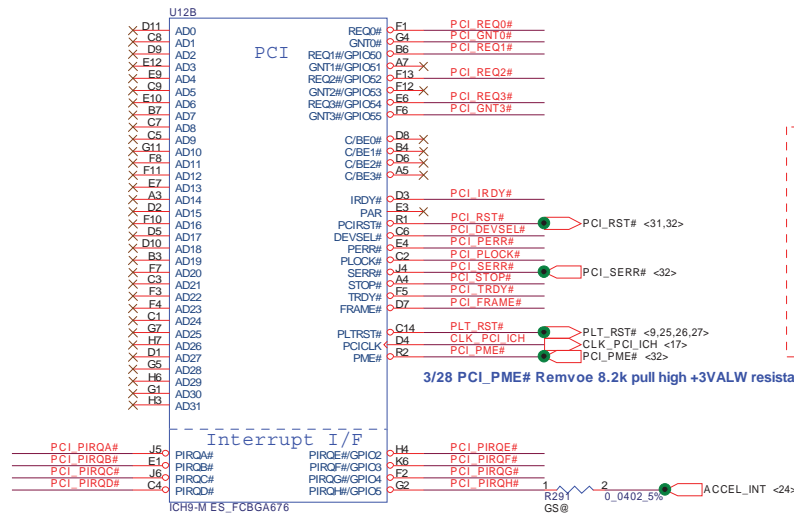
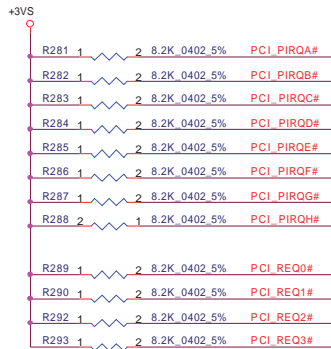
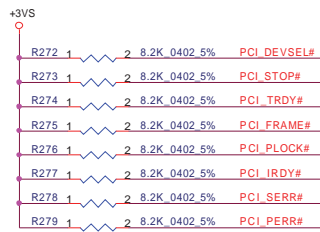
0308_Rserve L10 and install L11.



11/07 Change U42 to 3.9V LDO(Adjustable)
11/07 Change R1091 to 215K + R1093 to 100K
11/08 Change C1391 + C1392 to 0805 size

+USB_CAM is +3.9VS, R1091:215K; R1093:100Kohm +USB_CAM=1.25(1+R1091/R1093)

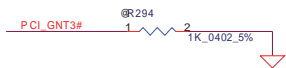
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				Montevina Blade UMA LA4101P	
				Date	Rev
				Saturday, January 05, 2008	0.3
				Sheet	19 of 46



3/28 PCI_PME# Remove 8.2K pull high +3VALW resistance.

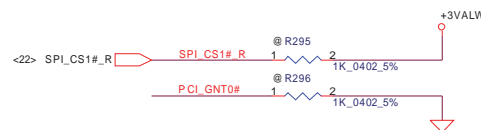
A16 swap override Strap

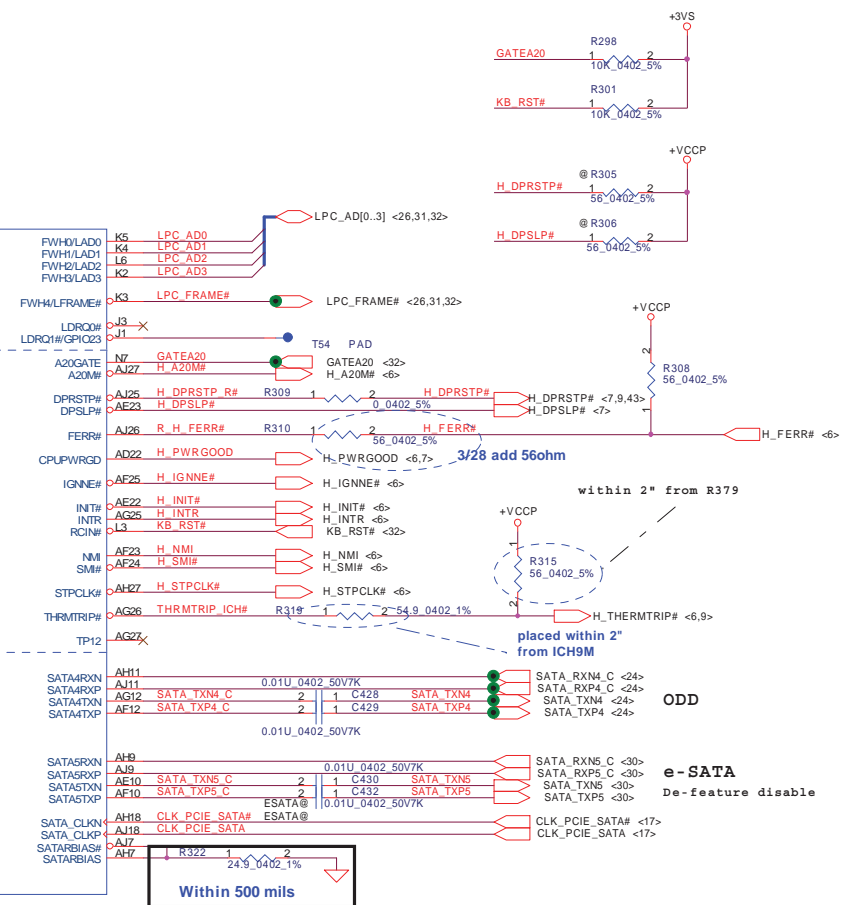
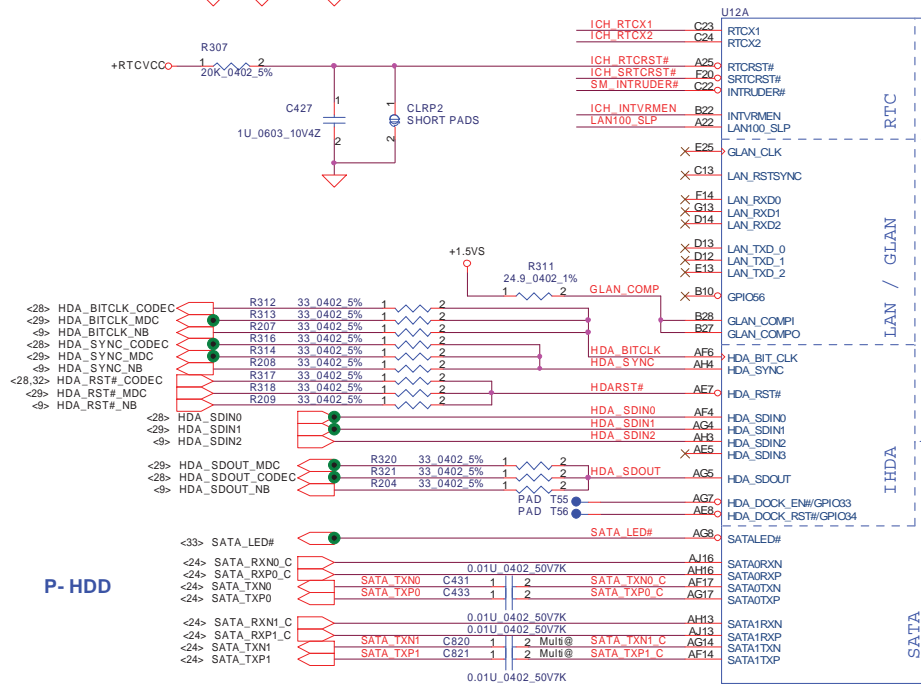
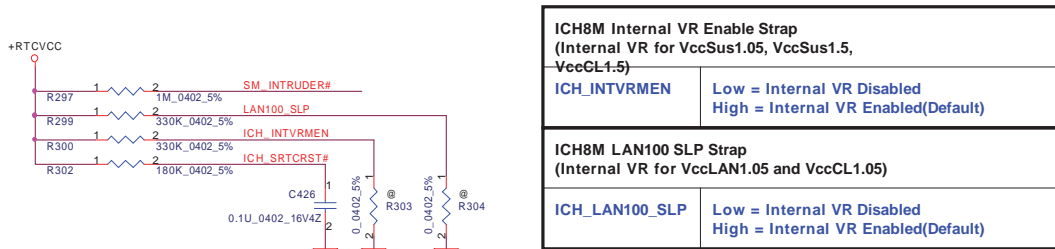
PCI_GNT3# Low= A16 swap override Enable
High= Default *



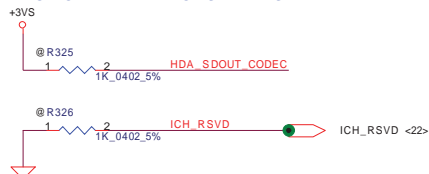
Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



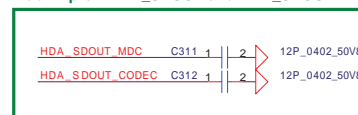


XOR CHAIN ENTRANCE STRAP:RSVD

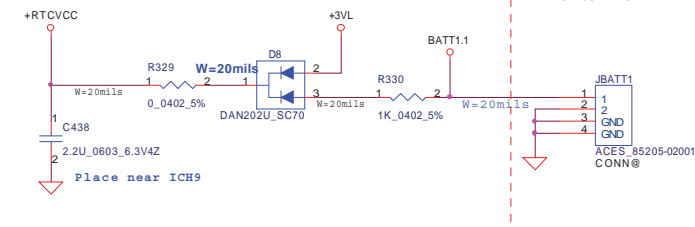
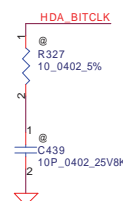
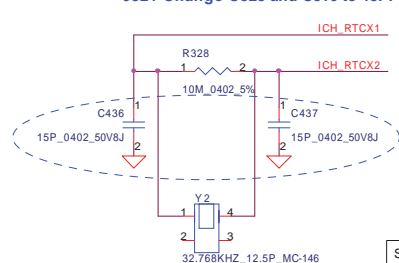


ICH_RSVD	HDA_SDOUT_CODEC
0	0
0	1
1	0
1	1

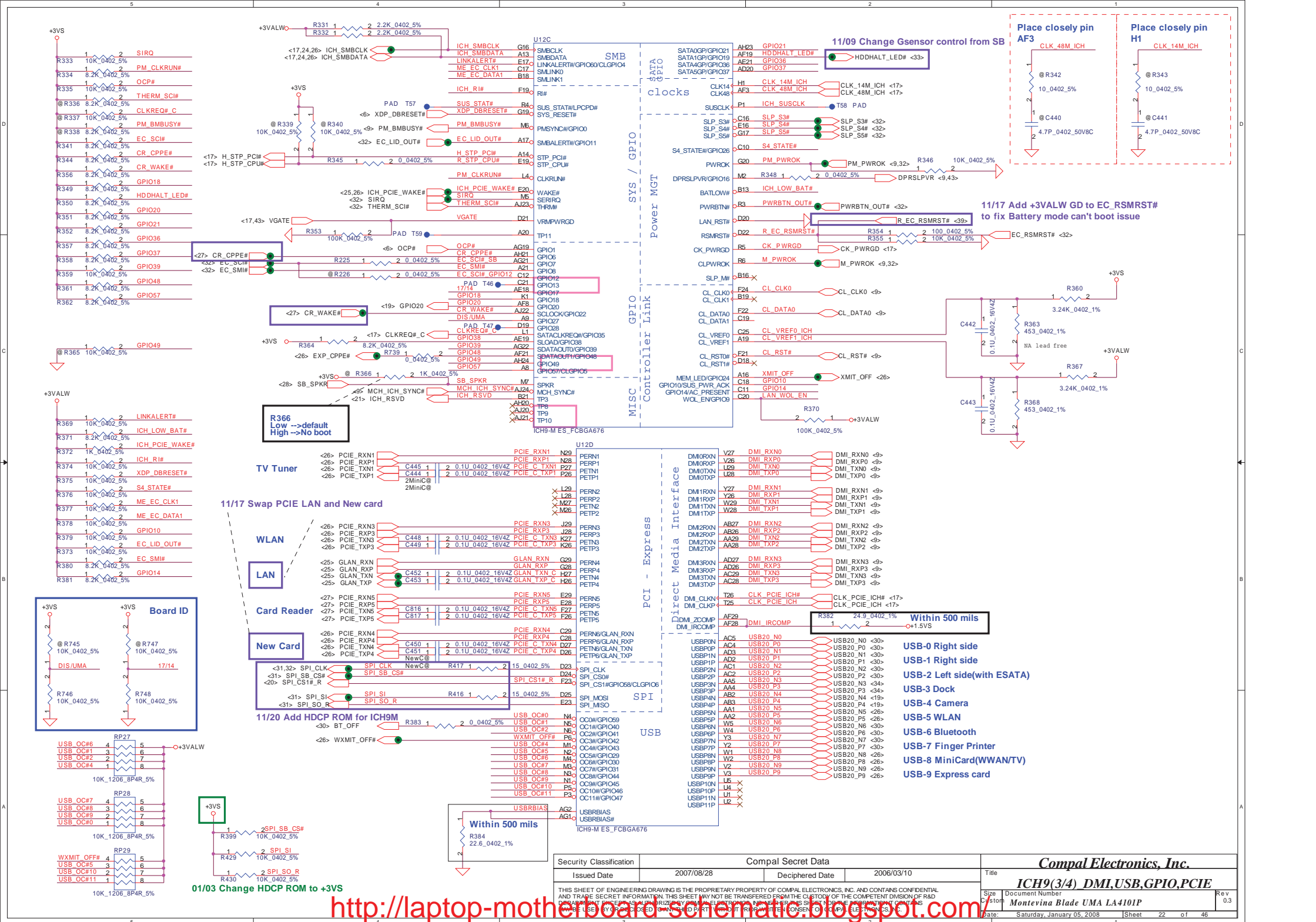
Add 12p on HDA_SDOUT and HDA_SDOUT



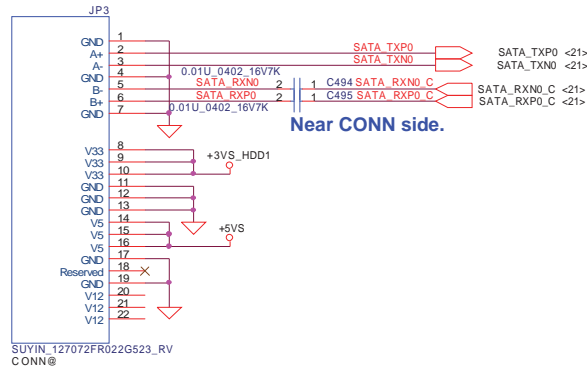
0821 Change C528 and C516 to 15PF



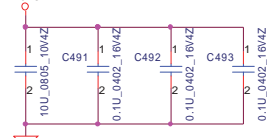
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				Date:	Rev
				Saturday, January 05, 2008	0.3
				Sheet	21 of 46



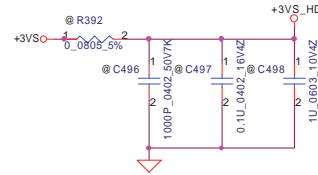
HDD Connector



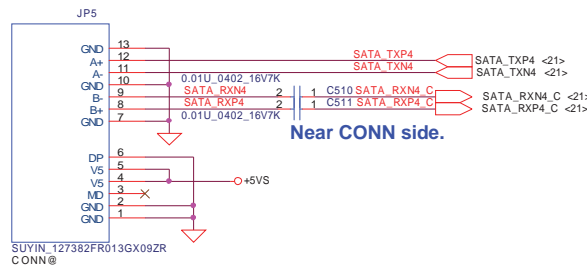
Place near HDD CONN (JP3)



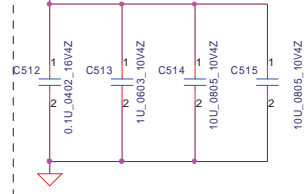
Place near HDD CONN



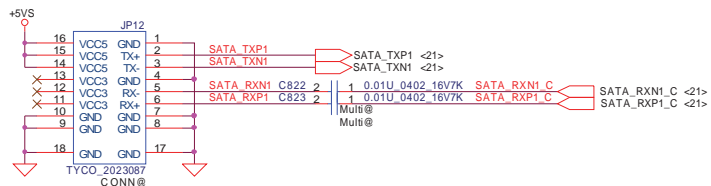
CD-ROM Connector



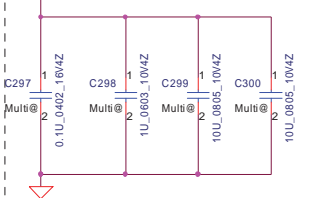
Place caps. near ODD CONN.



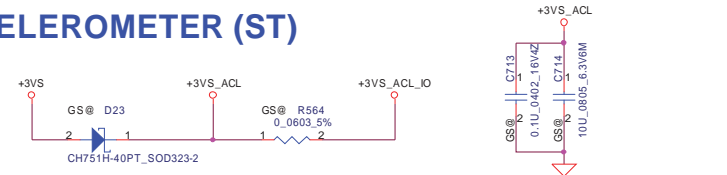
Multi Bay



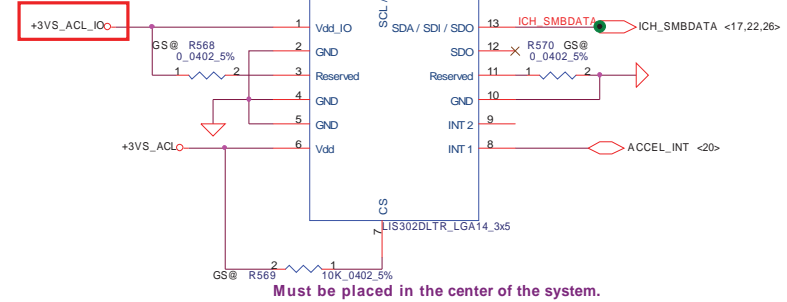
Place caps. near Multi Bay CONN.



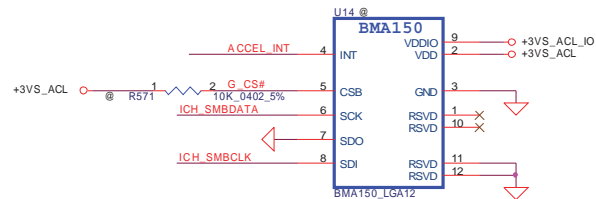
ACCELEROMETER (ST)



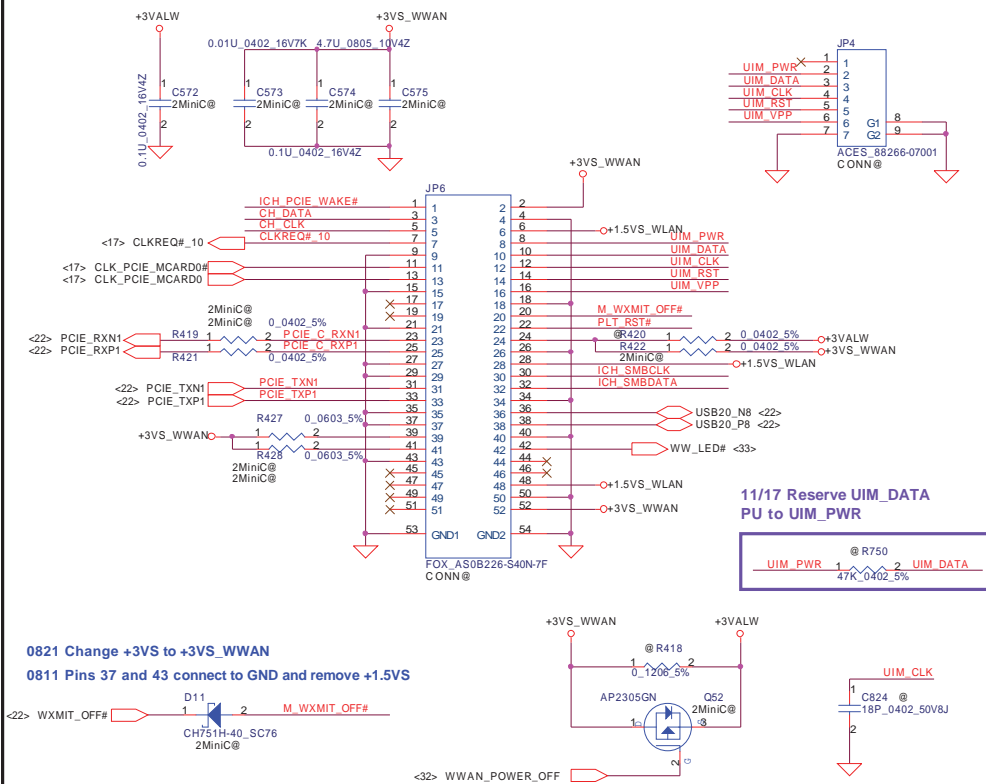
VDDIO absolute man
rating is VDD+0.1



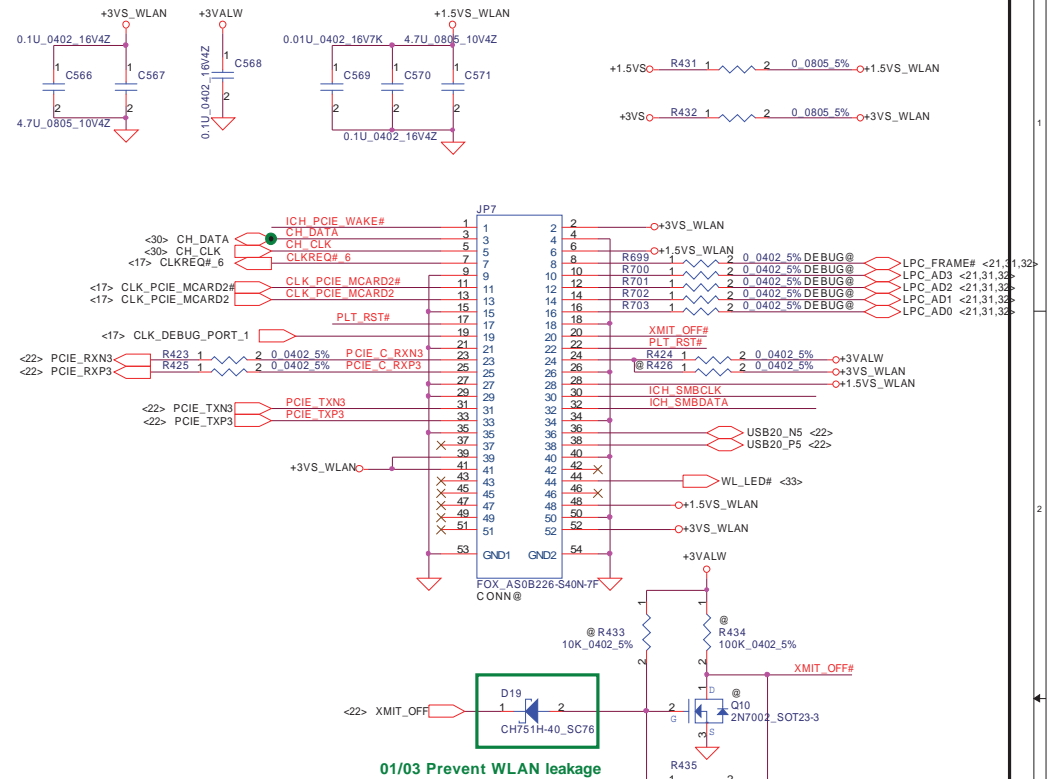
ACCELEROMETER (Bosch)



Mini Card 0--TV tuner/WWAN/Robson SIM card Connector

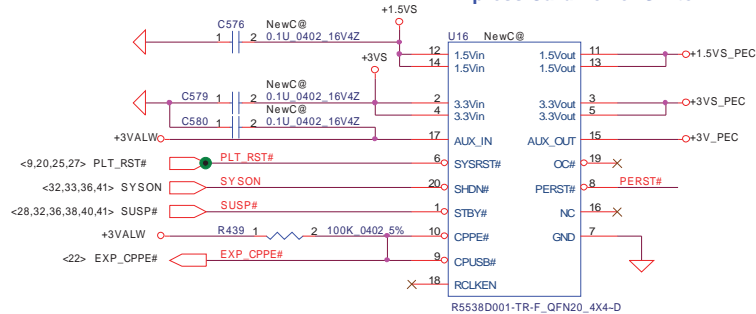


Mini Card 2---WLAN

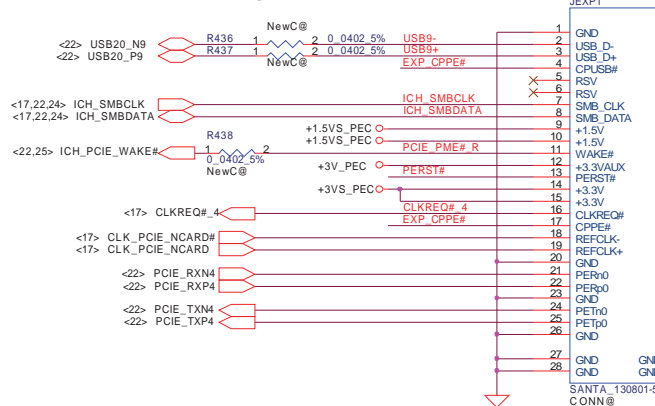


New Card

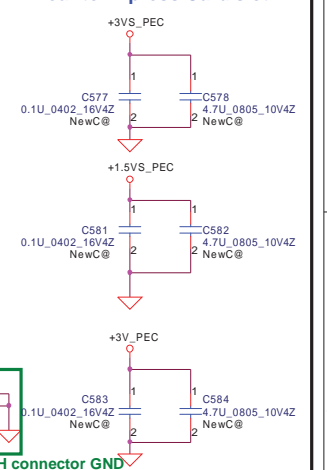
Express Card Power Switch



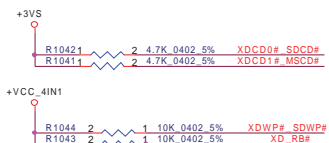
Close to JEXP



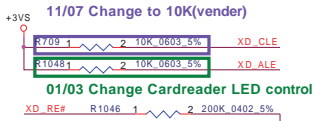
Near to Express Card slot.



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Date: Saturday, January 05, 2008				Sheet 26 of 46

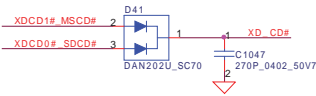
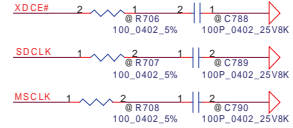


09/26 (JMicon) recommend width/length: 12mil / <250mil for PREXT signal (pin 7)



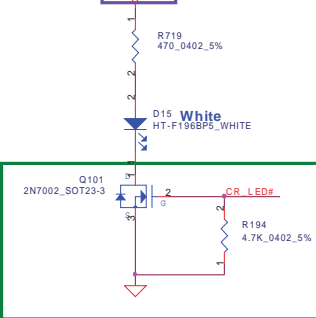
11/07 Change to 8.2K(vender)

09/26 (JMicon) recommend add a test point for pin 13 + 14

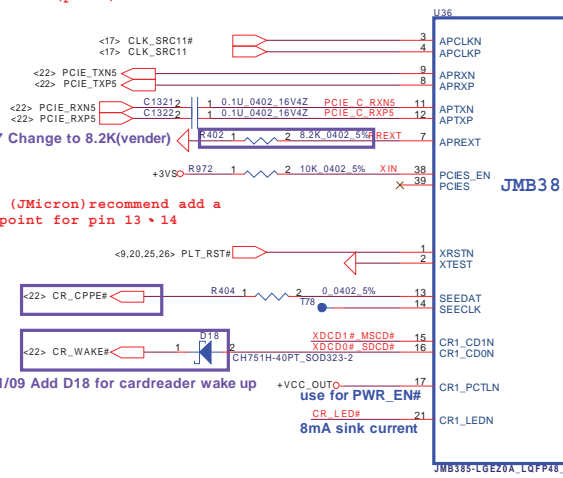


White LED: VF=3V, IF = 5mA, Res = 56ohm

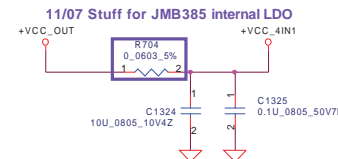
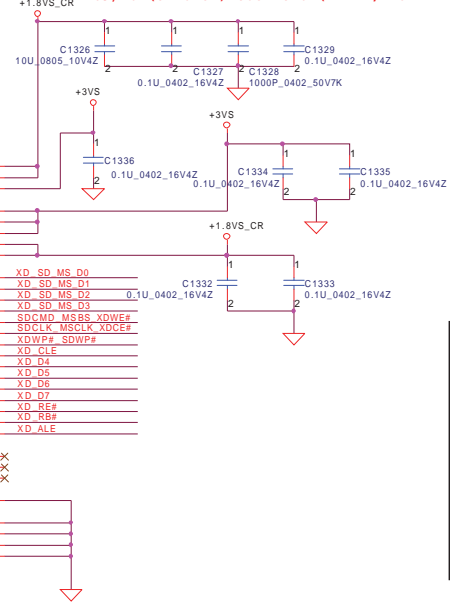
11/09 don't support DIM function



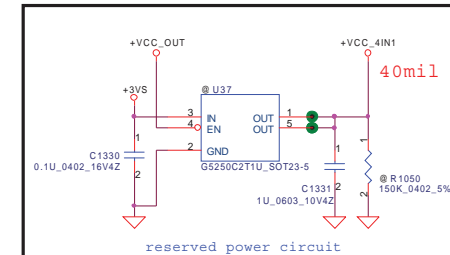
01/03 Change Cardreader LED control



09/26 (JMicon) recommend C1328/1000pF close to U36 pin5
09/26 (JMicon) recommend place C1329/0.1uF near by C1328
09/26 (JMicon) recommend (APVDD, 20 mil width, less than 120mil long)

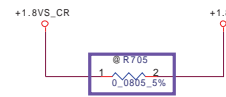


Use 0603 type and over 20 mils trace width on both side
09/26 (JMicon) recommend change to 0805 Size
09/26 (JMicon) recommend +VCC_OUT >30mil



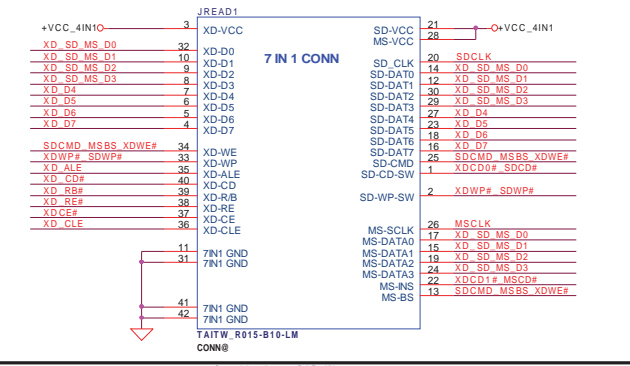
11/07 Change U37 correct PCBFootprint SOT23
11/07 BOM delete for JMB385 internal LDO

09/26 Must change P mos FET



11/07 Don't stuff for JMB385 internal LDO

Card Reader Connector



11/17 Update CIS library

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				Custom	Montevina Blade UMA LA4101P
				Date	Saturday, January 05, 2008
				Sheet	27 of 48
				Rev	0.3

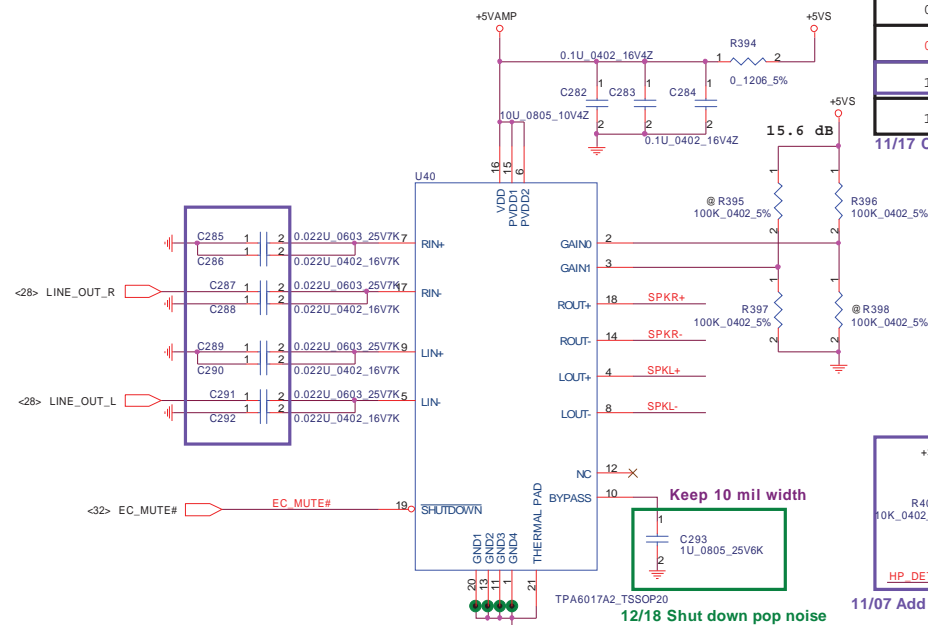
(4.75V(4.56~4.94V))
300mA



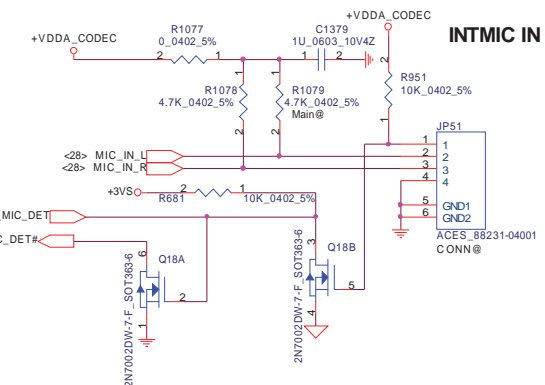
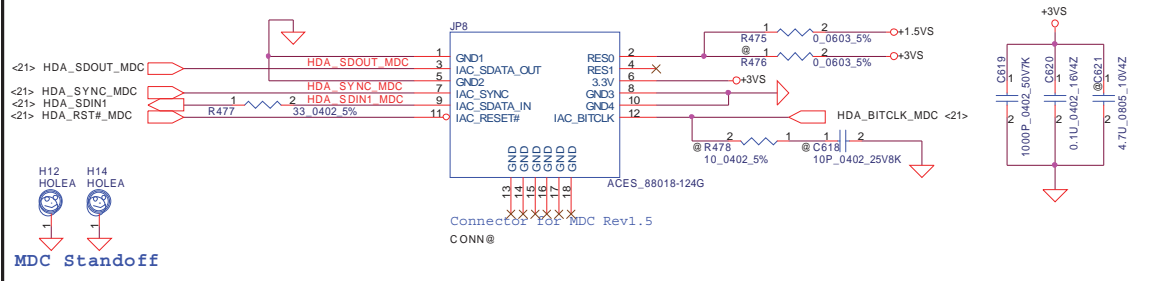
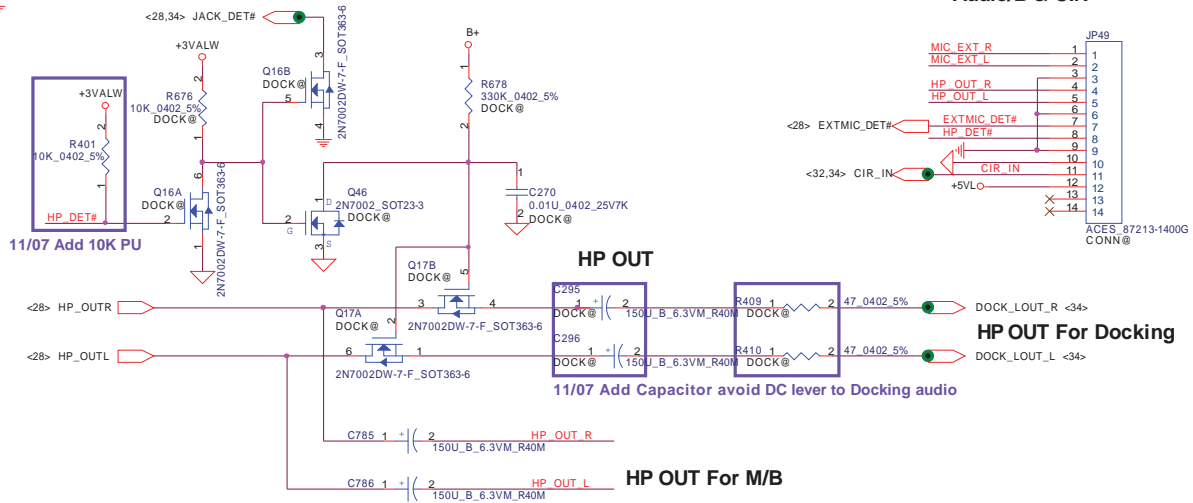
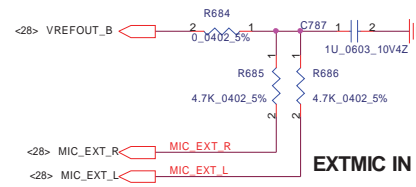
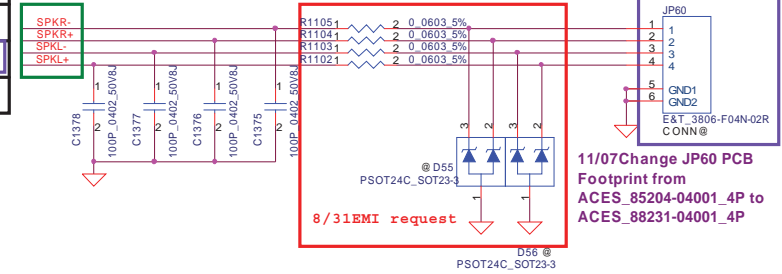
SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

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Size	Document Number			Rev	
A3	Montevina Blade UMA LA4101P			0.3	
Date:	Saturday, January 05, 2008	Sheet	28	of 46	

<http://laptop-motherboard-schematic.blogspot.com>

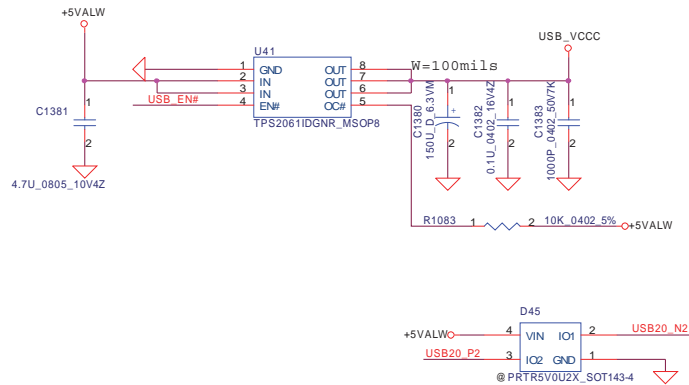


GAIN0	GAIN1	Av(inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

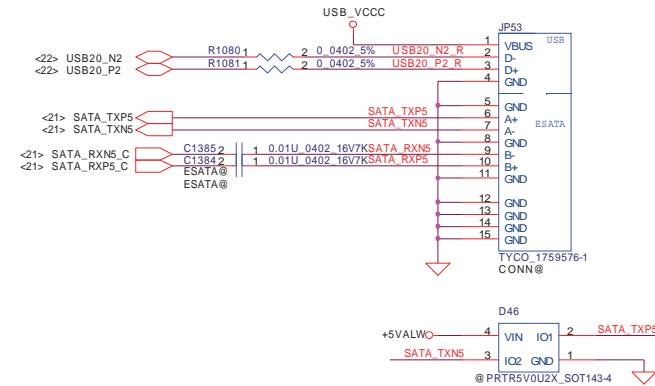


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					Size	Document Number		Rev
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					Date:	Saturday, January 05, 2008	Sheet	29 of 46

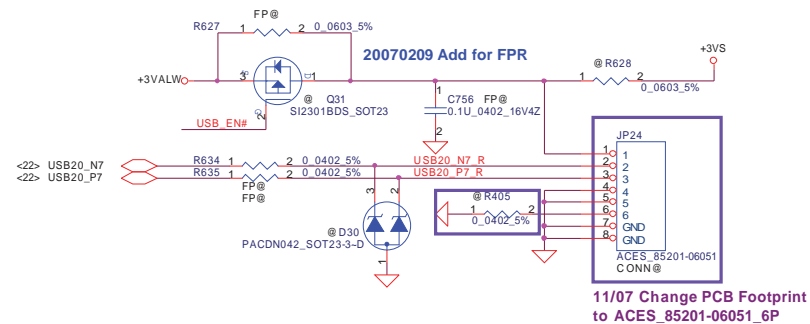
Left side USB Connector



Left side ESATA/USB combination Connector

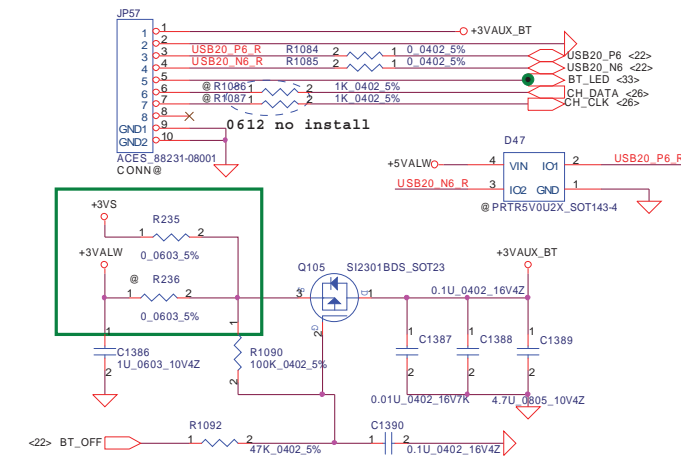


Finger printer



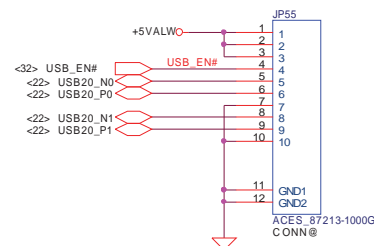
BT Connector

Need change to New version



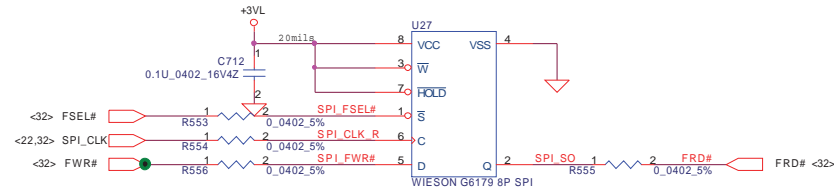
01/03 Change BT power to +3VS

USB cable connector for Right side

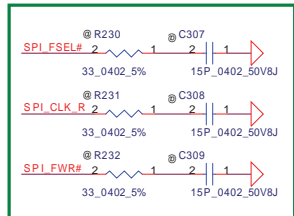


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				Rev	0.3
				Montevina Blade UMA LA4101P	
				Date	Saturday, January 05, 2008
				Sheet	30 of 46

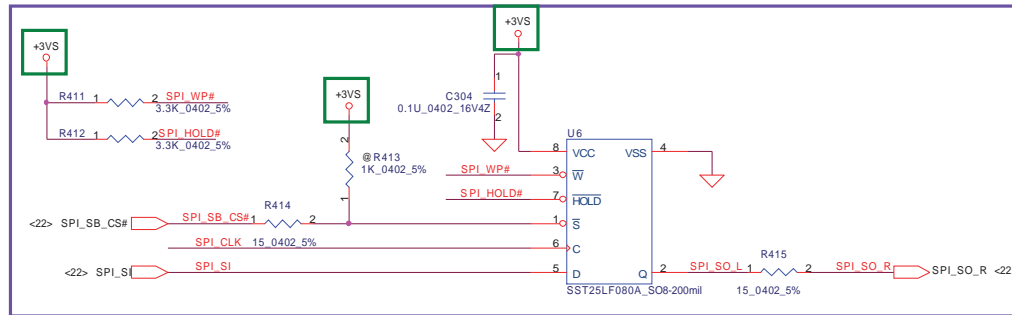
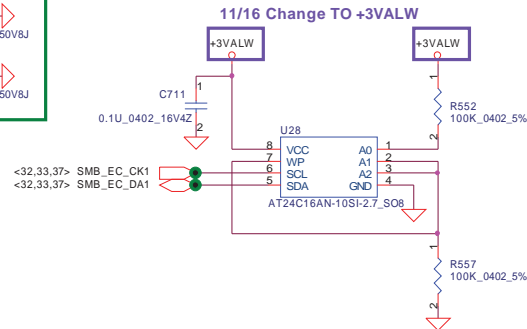
SPI ROM



SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH
WIESO_G6179-100000_8P



12/27EMI request

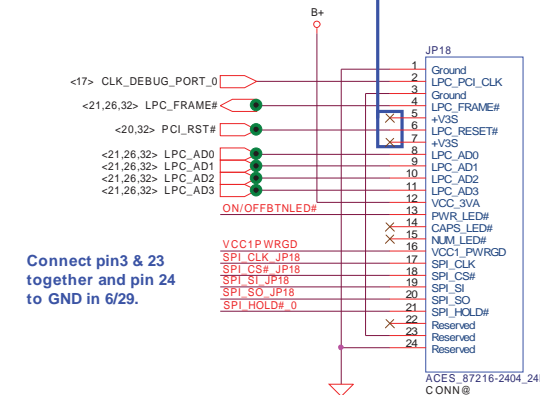


11/17 Add SB HDCP ROM

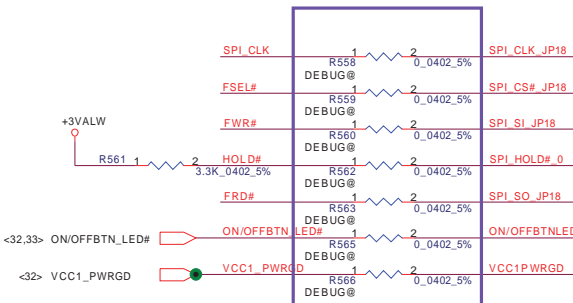
01/03 Change HDCP ROM to +3VS

LPC Debug Port

Change from +3VL to +3VS. 6/9
Removed +3VS. 6/13



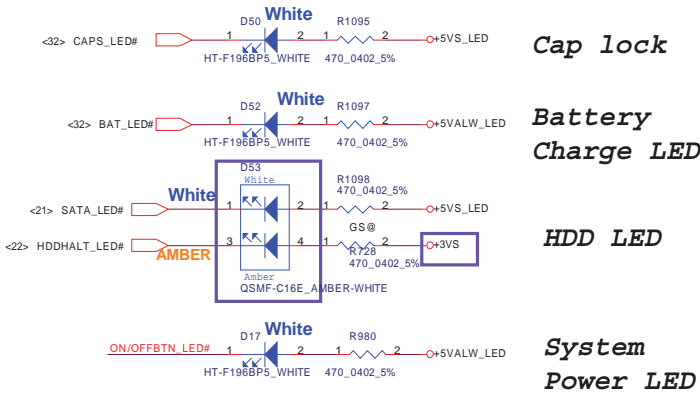
Connect pin3 & 23
together and pin 24
to GND in 6/29.



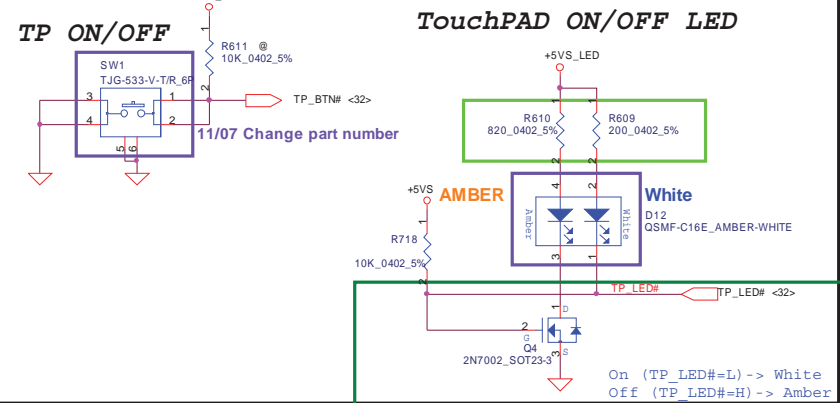
11/07 Add 0 Ohm for debug port

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Date: Saturday, January 05, 2008				Sheet	31 of 46

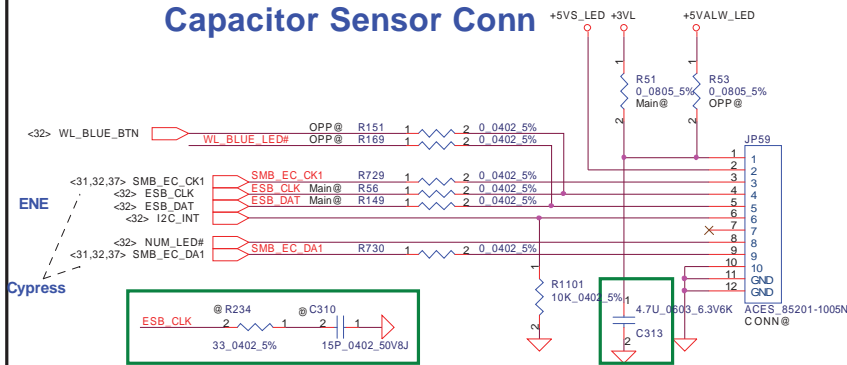
System LED



T/P Board (Inclue T/P_ON/OFF)

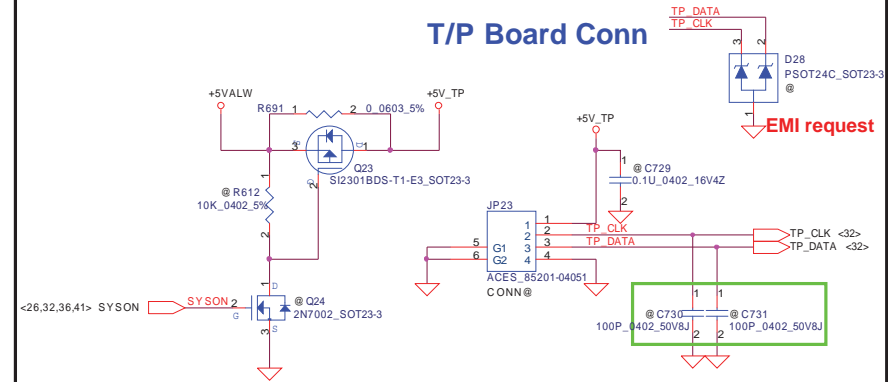


Capacitor Sensor Conn

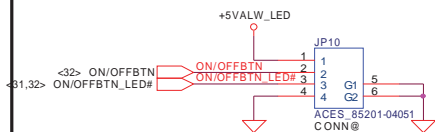


01/03 EMI request

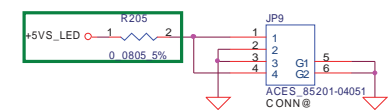
T/P Board Conn



ON/OFF Button Connector

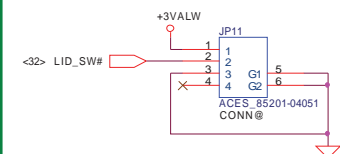


Keyboard backlight Conn



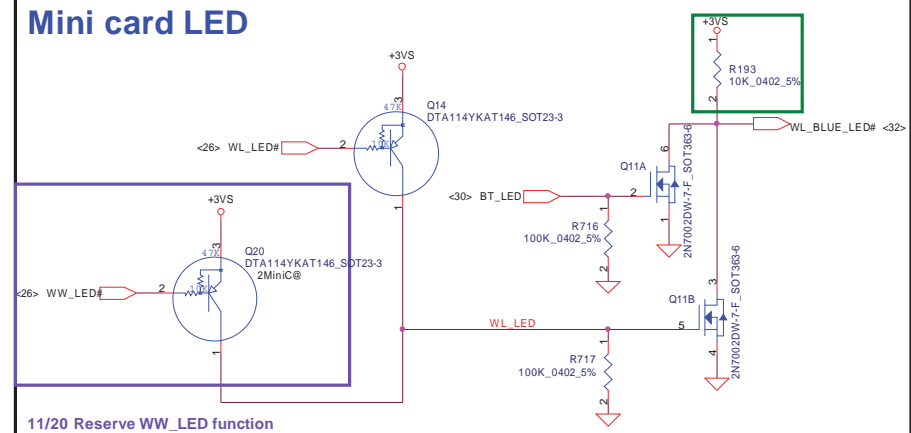
01/03 Keyboard backlight reserve a 0805 size resistor

Lid Switch Connector



01/03 Change lid switch connector type

Mini card LED



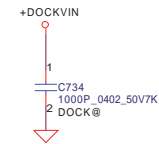
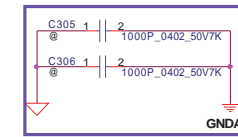
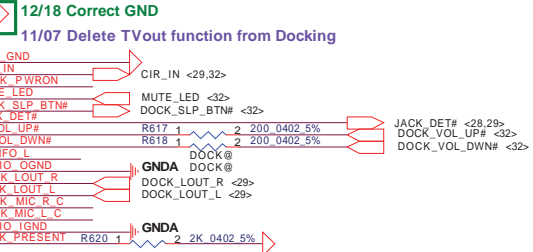
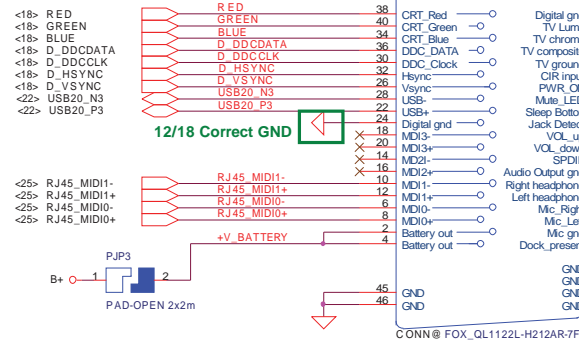
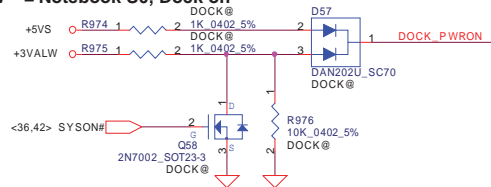
11/20 Reserve WW_LED function

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Date: Saturday, January 05, 2008				Size	Document Number
Sheet 33 of 46				Montevina Blade UMA LA4101P	
				Rev	0.3

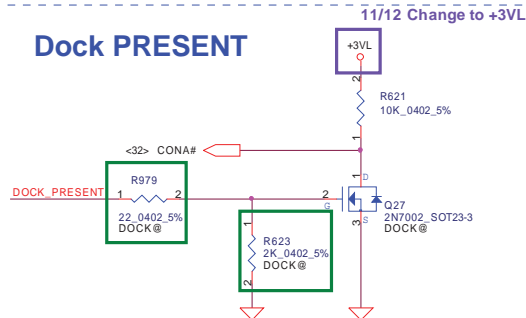
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Atlas/ Saturn Dock

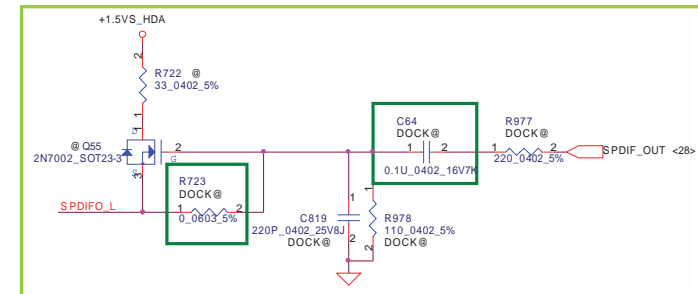
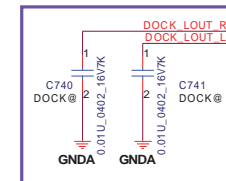
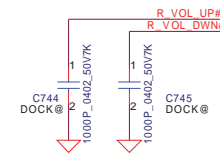
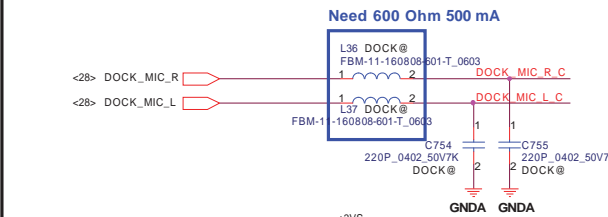
DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on



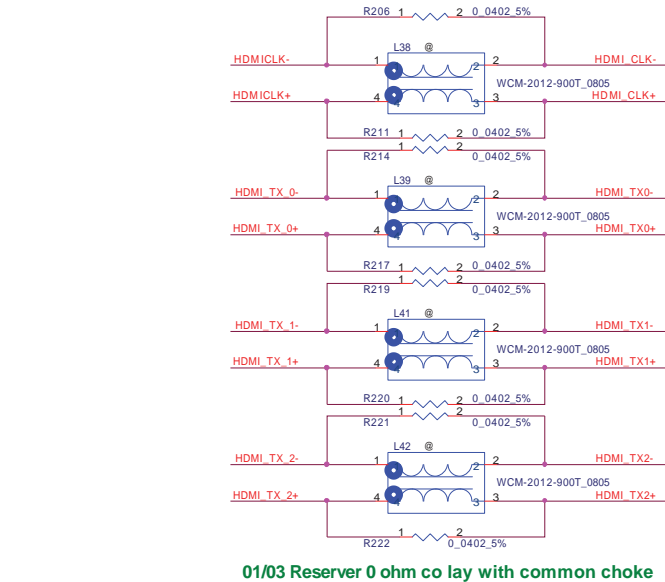
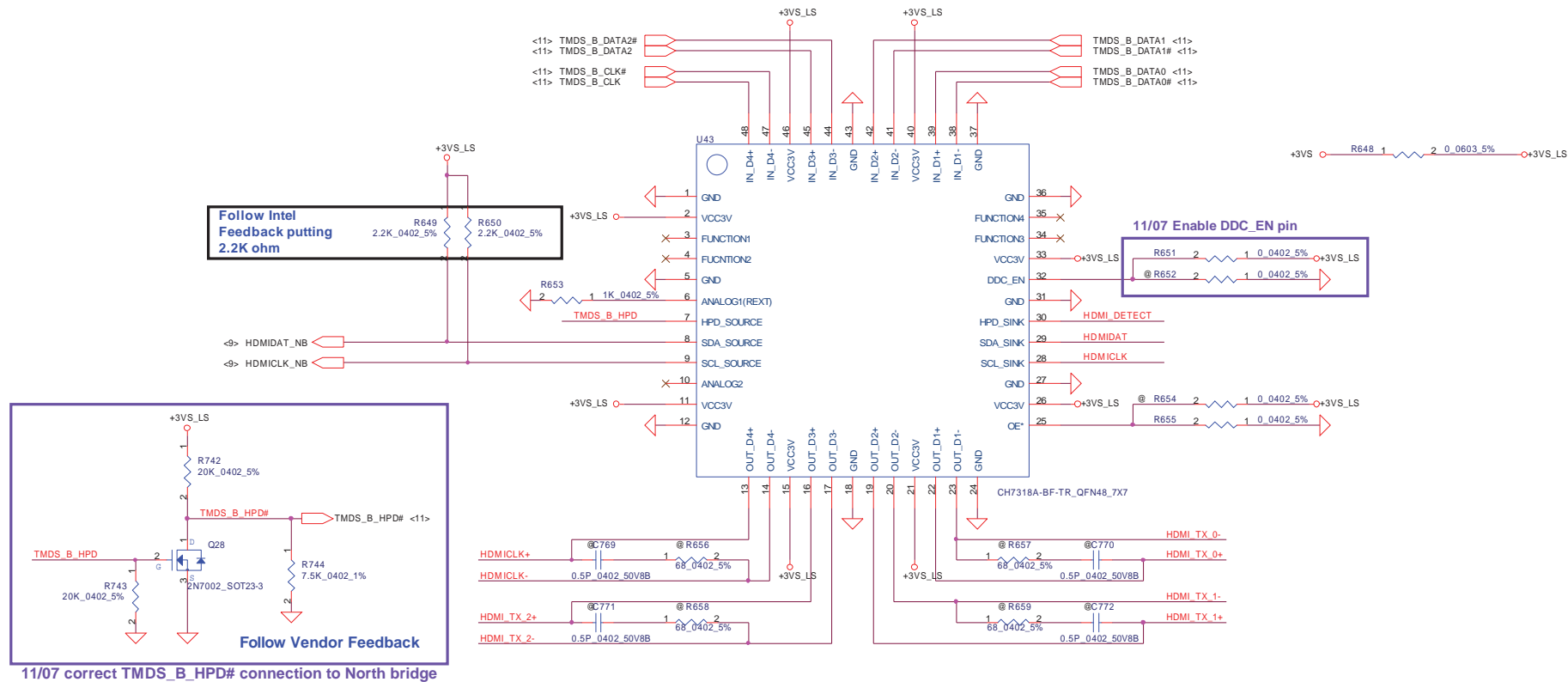
Dock PRESENT



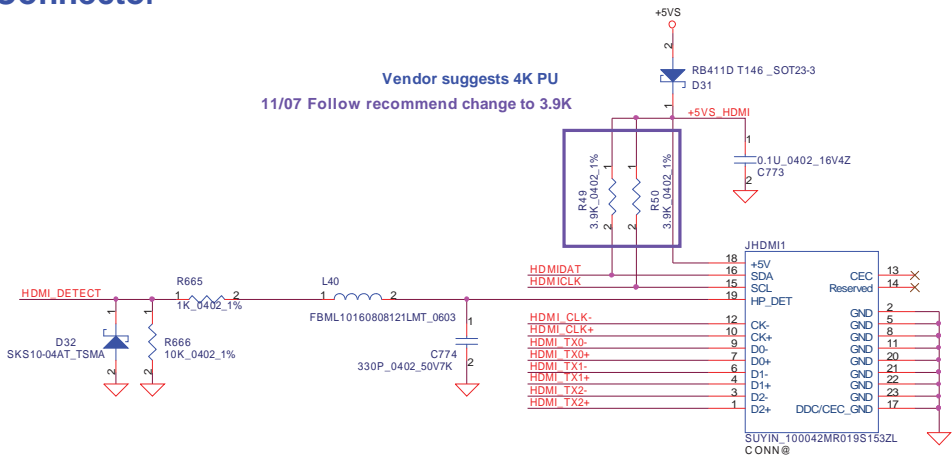
MIC_Dock



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Size	Document Number					Rev
Custom	Montevina Blade UMA LA4101P					0.3
Saturday, January 05, 2008						
Sheet 34 of 46						

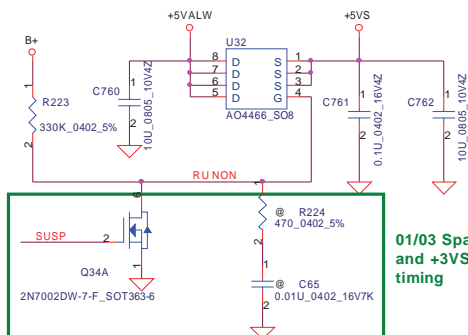


HDMI Connector



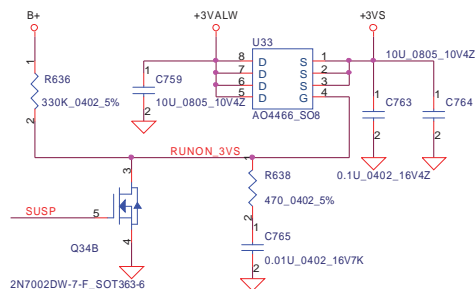
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				Date	Saturday, January 05, 2008
				Sheet	35 of 46
				Rev	0.3

+5VALW to +5VS Transfer

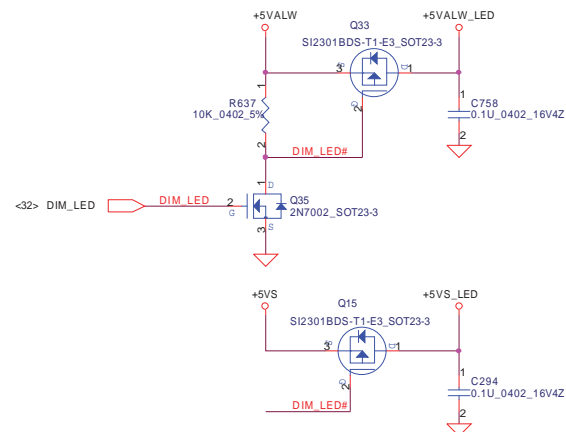


01/03 Sparate+5VS
and +3VS power
timing

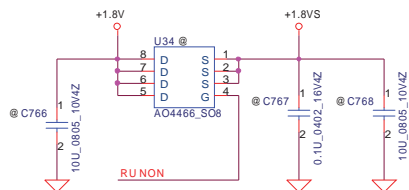
+3VALW to +3VS Transfer



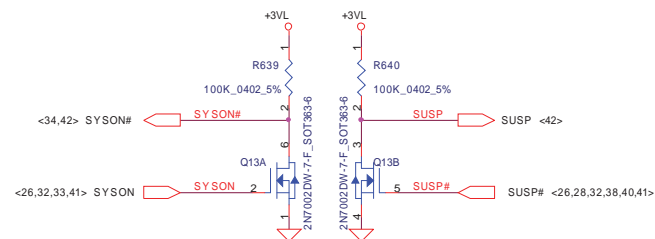
DIM LED



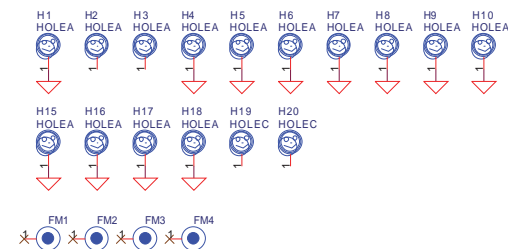
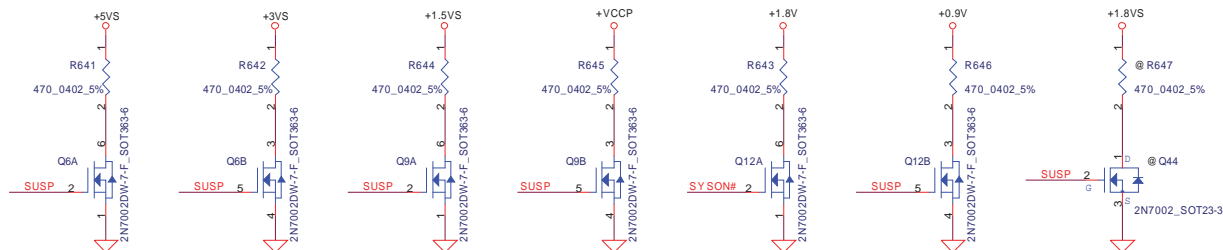
+1.8V to +1.8VS Transfer



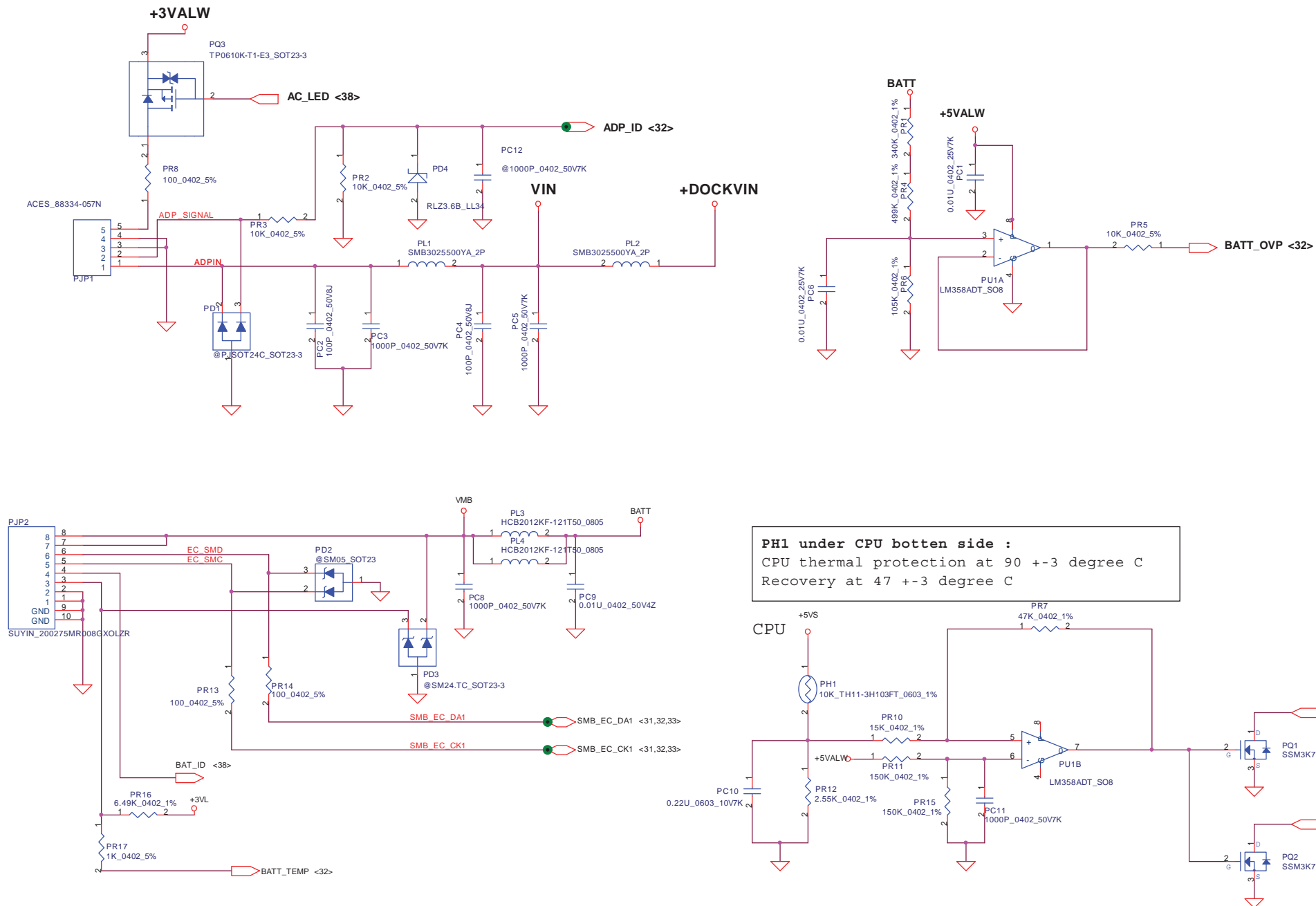
11/07 BOM Delete +1.8VS for Cardreader internal LDO



Discharge circuit

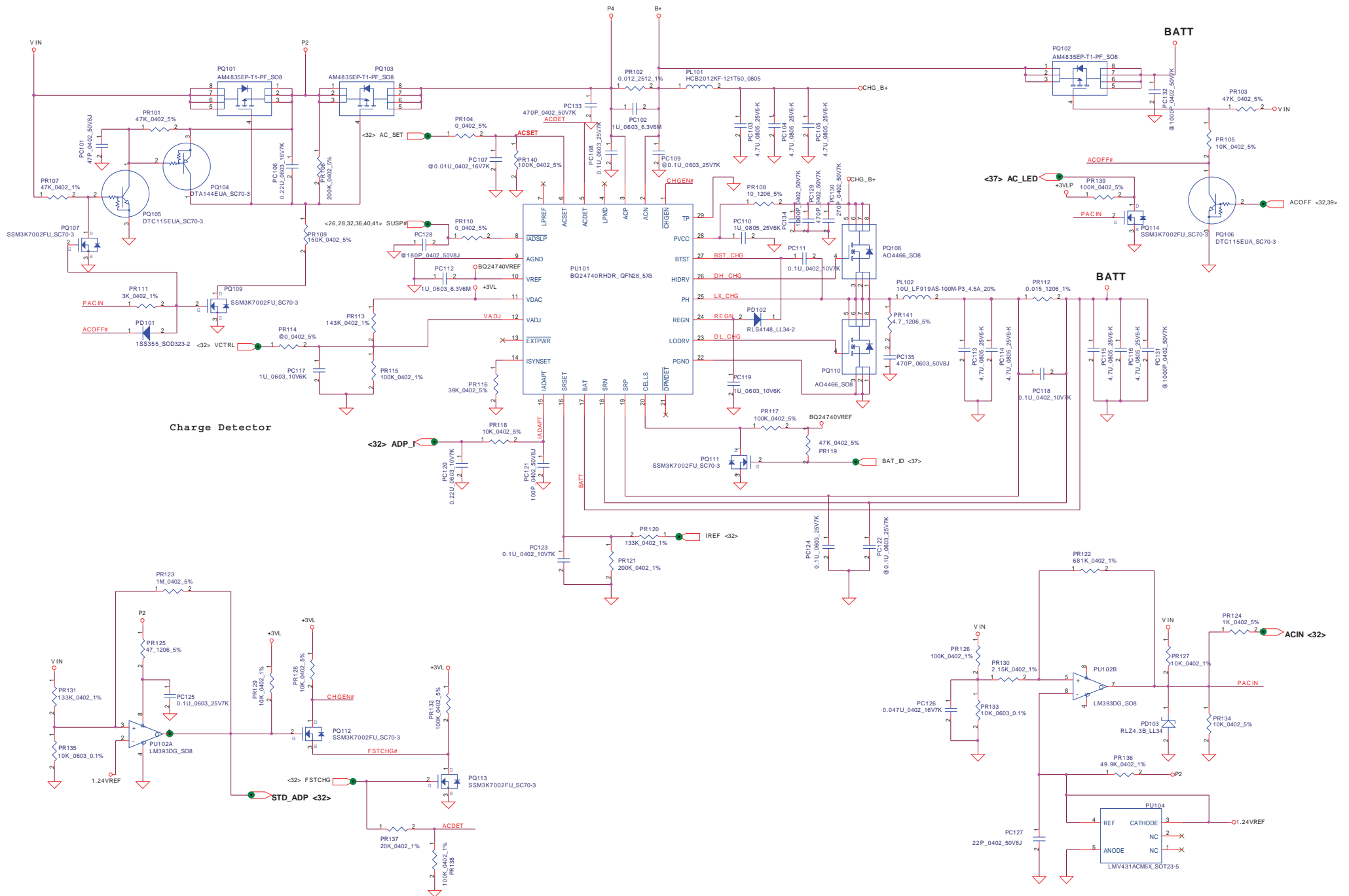


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				Rev	
				0.3	
				Date: Saturday, January 05, 2008	
				Sheet 36 of 46	



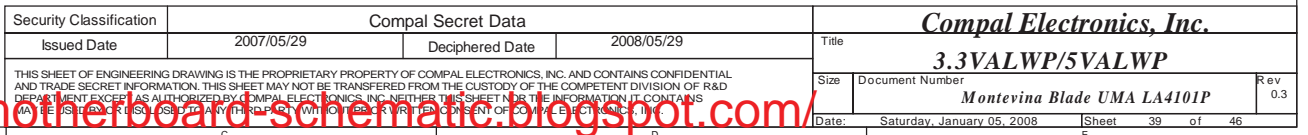
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				Date:	Saturday, January 05, 2008	Sheet 37 of 46

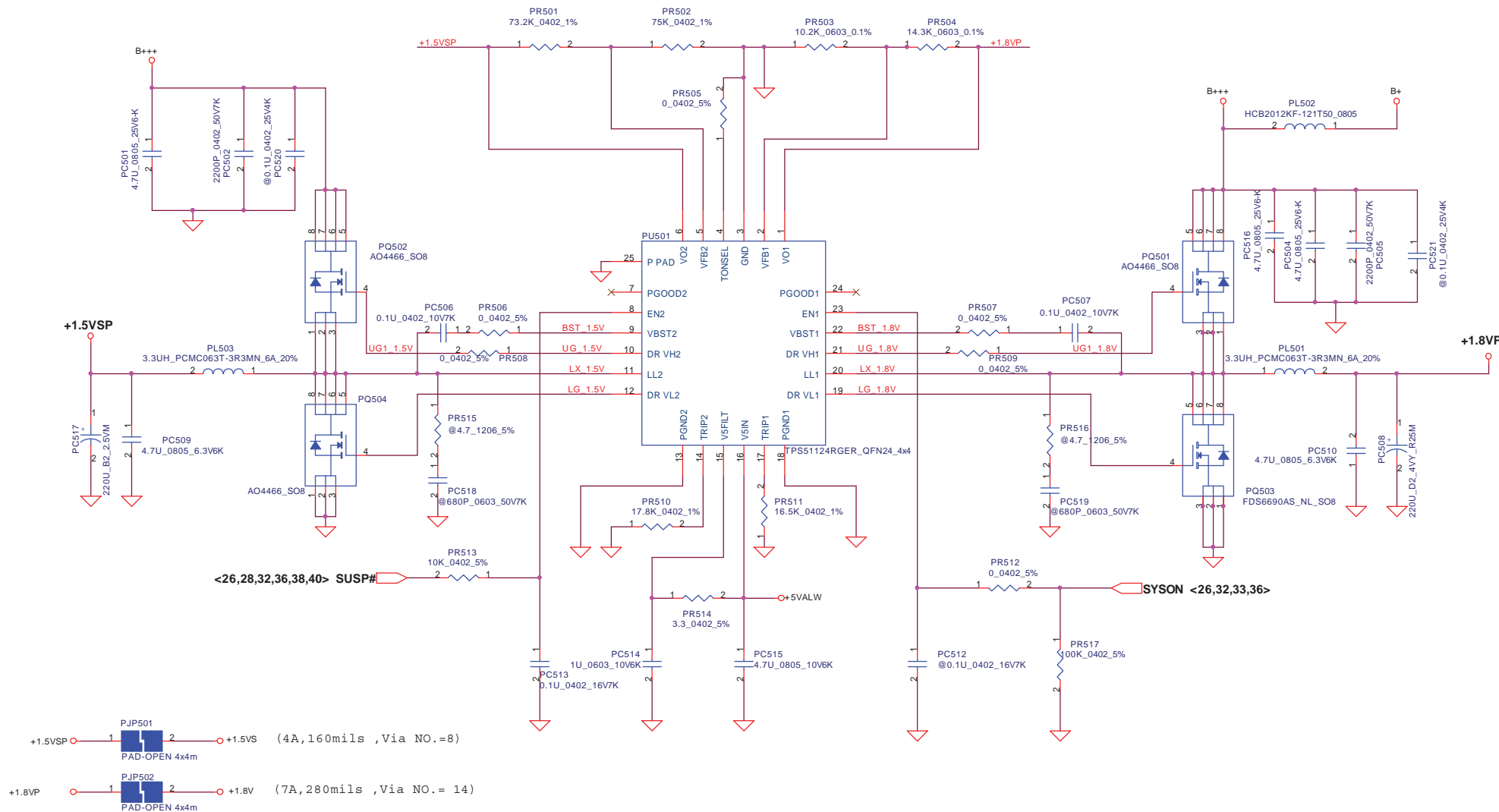
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<http://laptop-motherboard.schematicblogspot.com/>

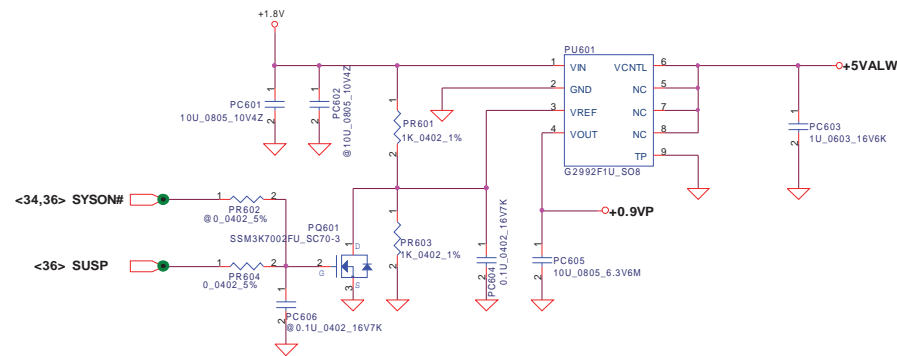
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2007/05/29		2008/05/29		Montevina Blade UMA LA4101P	
Size		Document Number		Rev	
0.3		Saturday, January 05, 2008		Sheet 38 of 46	



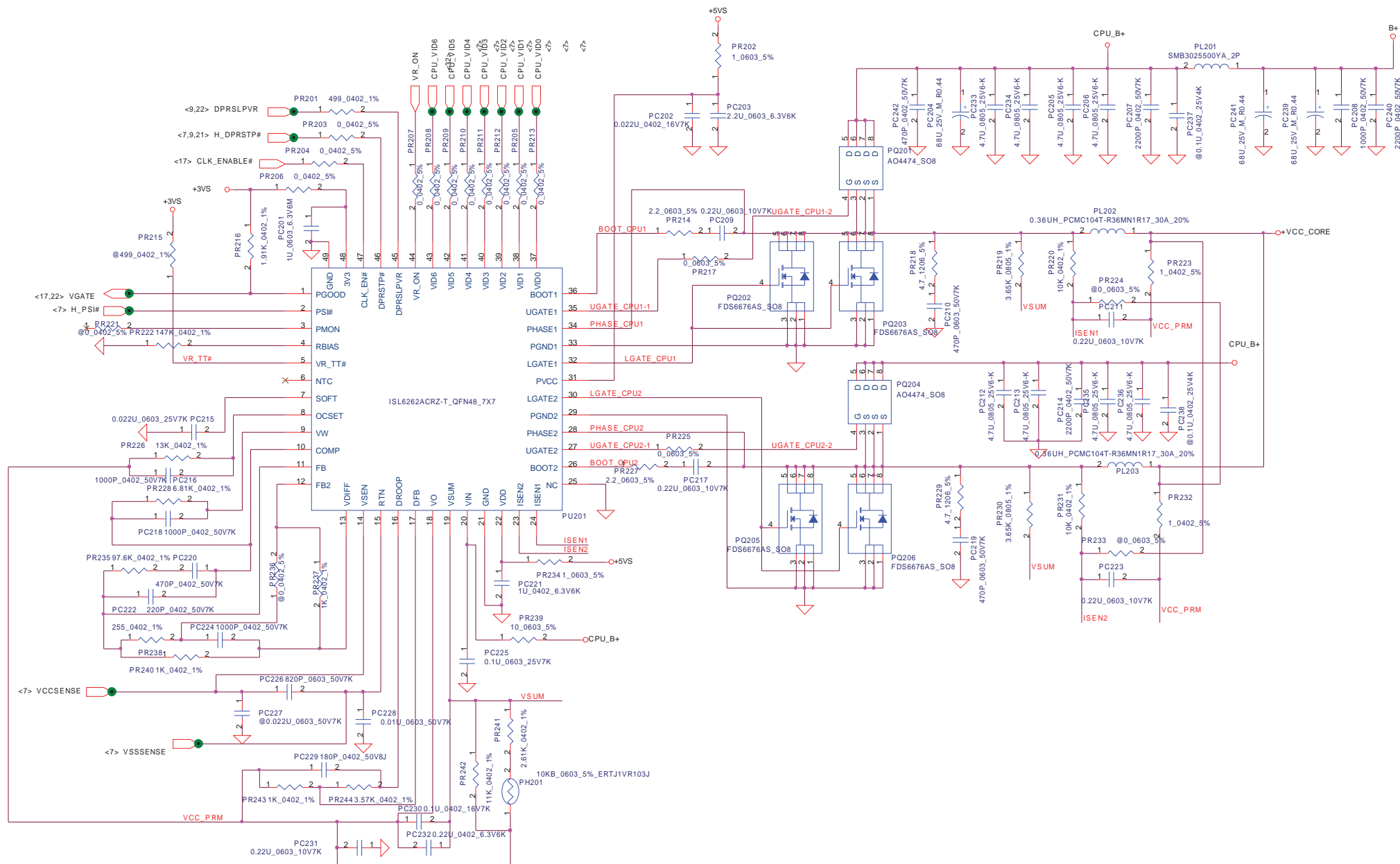


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Size	Document Number	Montevina Blade UMA LA4101P		Rev	0.3
Date:	Saturday, January 05, 2008	Sheet	41	of	46

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					Montevina Blade UMA LA4101P	0.3
				Date	Saturday, January 05, 2008	Sheet 42 of 48



Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Transation Fail	08	C41、C42、C43、C44 Change ESR=7m ohm	11/21	SI-1
2	Disable TV out function from Docking	11、34	R61、R62、R63 change to 75 Ohm、TV_DCONSEL_0、TV_DCONSEL_1 connect to GND	11/07	SI-1
3	Update Connetor Library		CRT(JCRT1)、HDMI(JHDMI1)、ESATA(JP53)、Finger print(JJP24)、FAN(JP2)、Speaker(JP60)、Multi bay(JP12)、Dual LED(D53、D12)	11/17	SI-1
4	Delete LVDS B channel	11、19	Schematic Delete	11/17	SI-1
5	USB camera Footprint error	19	Change U42 to G916-390T1UF SOT23, it adjustable mode, R1091=215K、R1093=100K	11/07	SI-1
6	Reserve Card reader D3E function	22、27	GPIO6= CR_CPPE#、GPIO22=CR_WAKE#	11/17	SI-1
7	Swap PCIE LAN and New card	22	Swap PCIE4 and PICE6	11/17	SI-1
8	Add HDCP ROM for ICH9M	22、31	Add HDCP ROM for ICH9M	11/17	SI-1
9	Change G sensor control from SB、LED drive by +5VS	22、33	Change G sensor control from SB	11/17	SI-1
10	Avoid Battery mode can't boot issue	22、39	Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue	11/17	SI-1
11	Add G sensor ST and Bosch	24	Add G sensor ST and Bosch	11/17	SI-1
12	Change LAN solution (Marvell to Realtek)	25	Change LAN solution (Marvell to Realtek)	11/17	SI-1
13	LAN can't work	25	U46 Change to correct transformer type	11/17	SI-1
14	Cardreader schematic review and update, add D3E function	27	R709-->10K、R402-->8.2K、R704-->Stuff、R705-->@、U37-->@、Cardreader LED-->+5VS、add D3E function	11/17	SI-1
15	Jack can't detect normal	28	R1059 change from 39.2 to 39.2K	11/17	SI-1
16	Speaker work un normal	28	Add and Stuff C1362、R1065、R596	11/17	SI-1
17	HP audio team recommend	28、29	C285-C292、C1352、C1354 change to 0.022U、Amp output setup to 15.6 dB、Reserve C305、C306 for GNDA and GND	11/17	SI-1
18	Audio jack can't detect normal	29	Add Pull up resistor R401 to +3VALW	11/17	SI-1
19	Docking HP audio test fail	29	Add C295□BC296 to avoid DC level, and add R409、R410 to reduce HP out level	11/17	SI-1
20	Leakage problem	32	Correct direction prectect leakage	11/07	SI-1
21	EC pin define update	32	Delete EC_PME#、SYSON PU、SUSP# PU、LiD_SW# change to +3VALW、Delete CLKRUN#、R582->@ for C0 chip、CIR PU+5VL、add 100P to BATT_OVP(EC recommend)	11/07	SI-1
22	Can't Hibernation(SLP_S4#)	32	Connect SLP_S4# to SB	11/17	SI-1
23	EC can't receive docking present	34	CONA# change +3VL	11/12	SI-1
24	HDMI can't detect	35	DDC_EN must enable、TMDS_B_HPDP# inverse	11/07	SI-1
25	LVDS power on timing	19	C238 change to 0.047u to meet TI timing	01/03	SI-2
26	Prevent WWAN nosie	21	Add 12p on HDA_SDOUT and HDA_SDOUT	01/03	SI-2
27	Power leakage	21、31	Change HDCP ROM to +3VS power plane	01/03	SI-2
28	Prevent WLAN leakage	26	Add Diode prevent WLAN leakage	01/03	SI-2

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
29	New card PTH connector GND	26	New card PTH connector GND	01/03	SI-2
30	Change Cardreader LED control	27	Change Cardreader LED control	01/03	SI-2
31	Change SPDIF to SPDIF1	28	Change to SPDIF1	01/03	SI-2
32	Shut down pop noise	29	Change C293 to 1U	01/03	SI-2
33	Change BT power to +3VS	30	Change BT power to +3VS	01/03	SI-2
34	EMI Request	31	SPI_FSEL#、SPI_CLK_R、SPI_FWR# reserver RC	01/03	SI-2
35	Reserver 0 ohm co lay with common choke	35	Reserver 0 ohm co lay with common choke	01/03	SI-2
36	Sparate+5VS and +3VS power timing	36	Sparate+5VS and +3VS power timing	01/03	SI-2
37	Keyboard backlight reserve a 0805 size resistor	33	Keyboard backlight reserve a 0805 size resistor	01/03	SI-2
38	Change Lid switch connector type	33	Change Lid switch connector type	01/03	SI-2
39					
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Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	DC Connector /CPU_OTP	11/06	Compal	Add PD4 & PC12	Add PD4 & PC12	
2	39	3.3VALWP/5VALWP	11/06	Compal	for Layout	Change PQ301 cancel PQ303	
3	38	Charger	11/06	Compal	EMI solution	Add pc128	
4	43	+CPU_CORE	11/06	Compal	EMI solution	Add PC240	
5	39	3.3VALWP/5VALWP	11/14	Compal	for Layout	Change PL303 and PC310	
6	38	Charger	12/31	Compal	EMI solution	Add PC129, PC130, PC131, PC132, PC133	
7	43	+CPU_CORE	12/31	Compal	EMI solution	Add PC242	
8	39	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
9							
10							
11							
12							
13							
14							

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				Date:	Saturday, January 05, 2008	Sheet 46 of 46

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