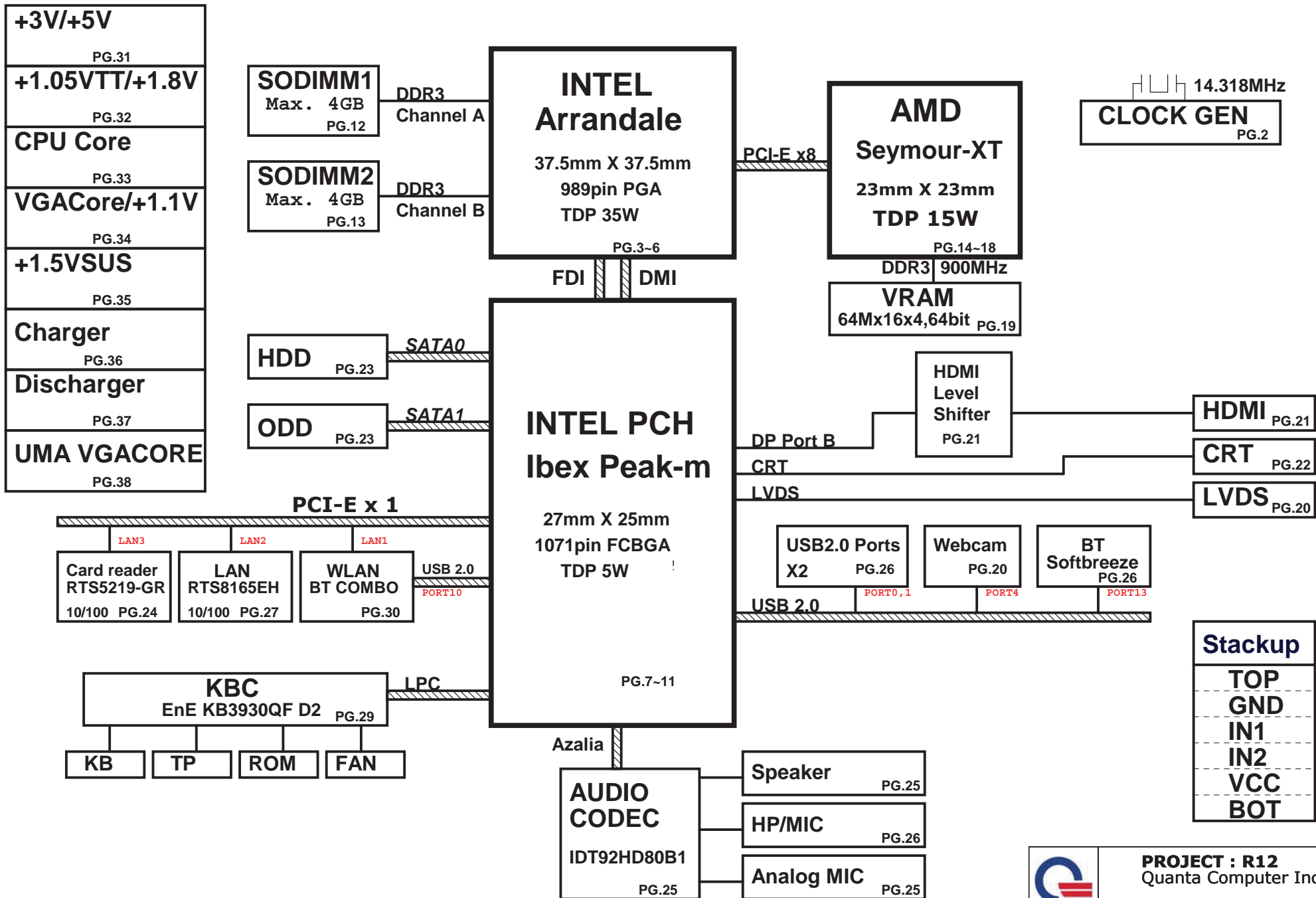
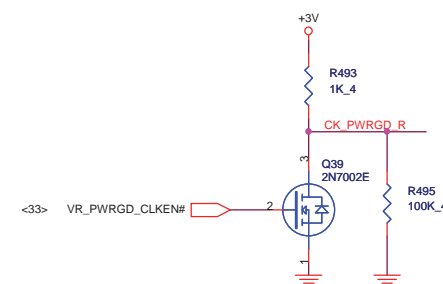
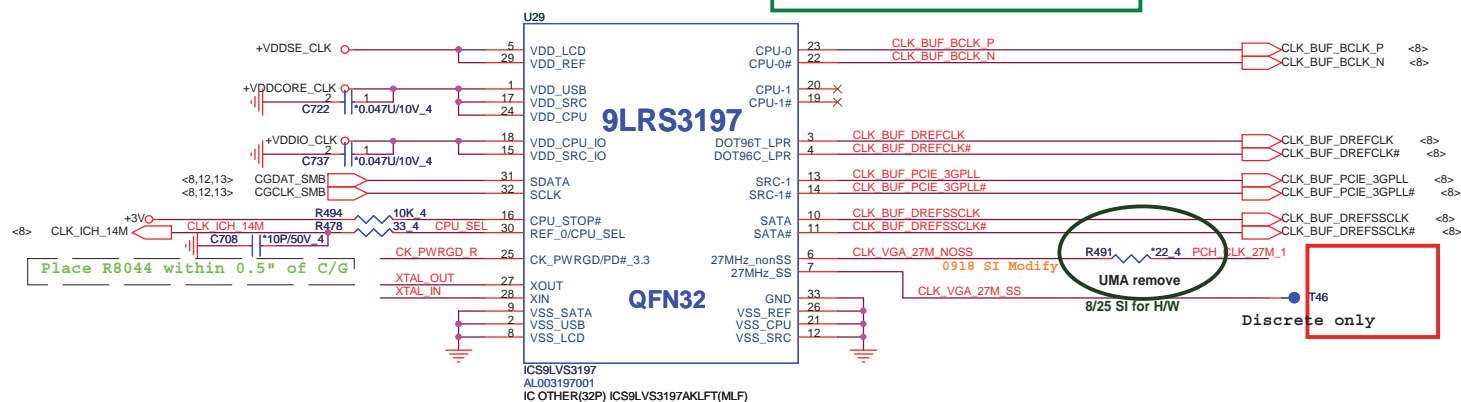
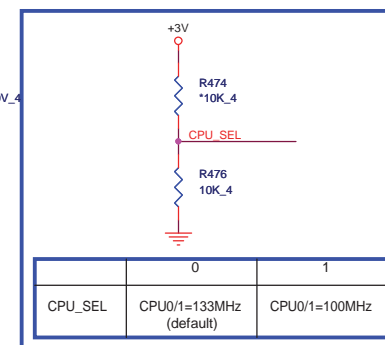
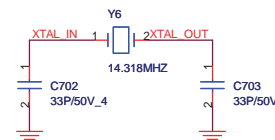
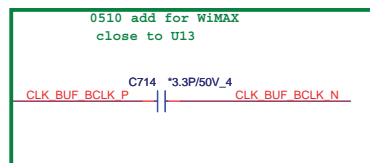
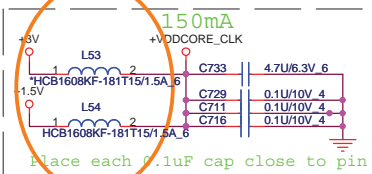
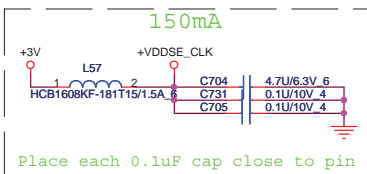
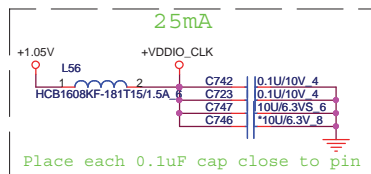
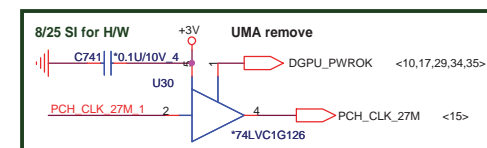


R12 INTEL UMA/DISCRETE SYSTEM DIAGRAM





Vender	Part	Part Number	Part Description
ICS	ICS9LV3197	AL003197000	IC OTHER(32P) ICS9LV3197AKLFT(MLF)
Realtek	RTM890N-632	AL000890000	IC OTHER(32P) RTM890N-632-GRT(QFN)
Silego	SLG8LV595VTR	AL000595000	IC OTHER(32P)SLG8LV595VTR(QFN)

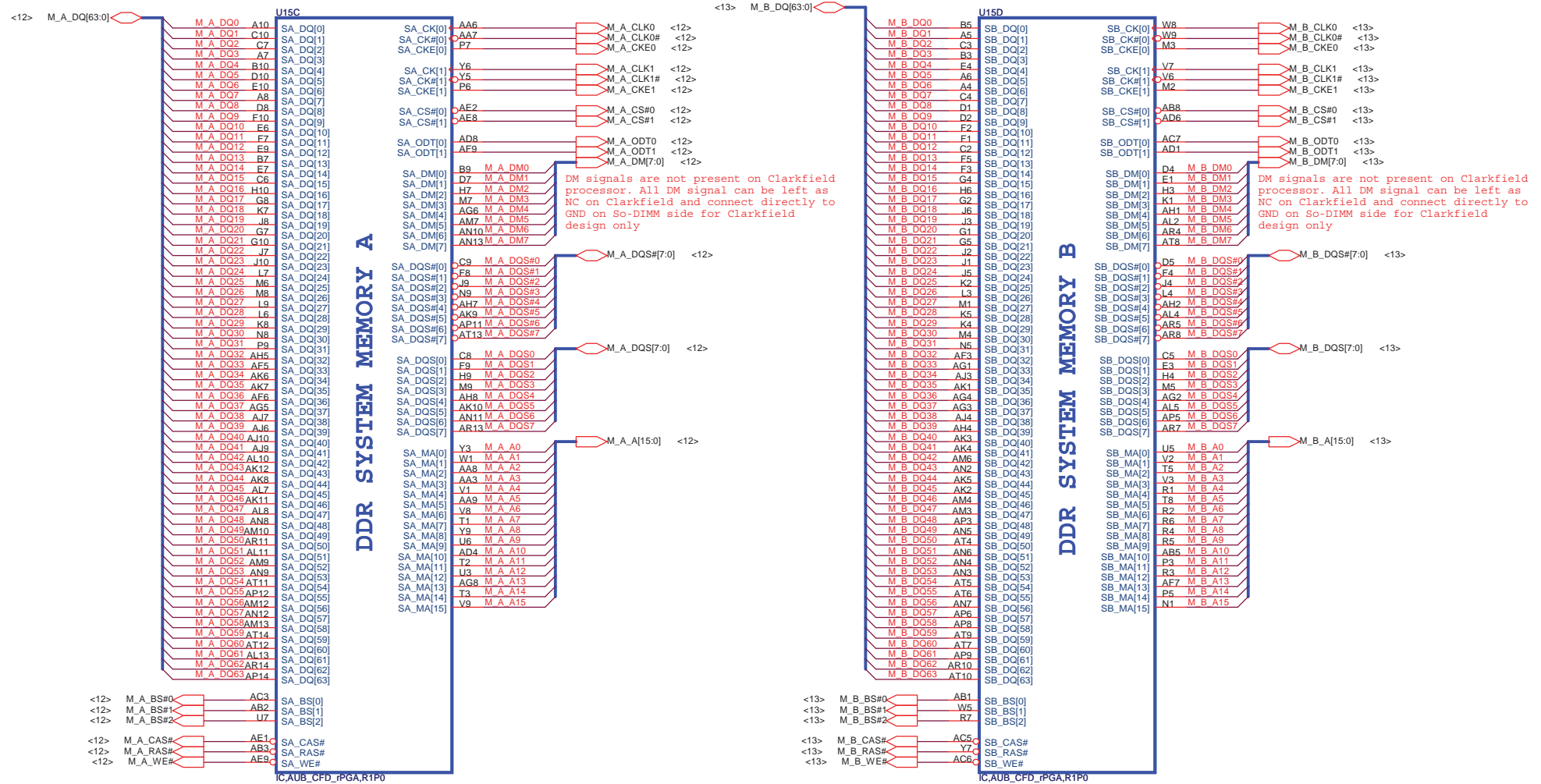


+1.05V <7,8,9,11,39>
+1.5V <5,30>
+3V <3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36>





AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



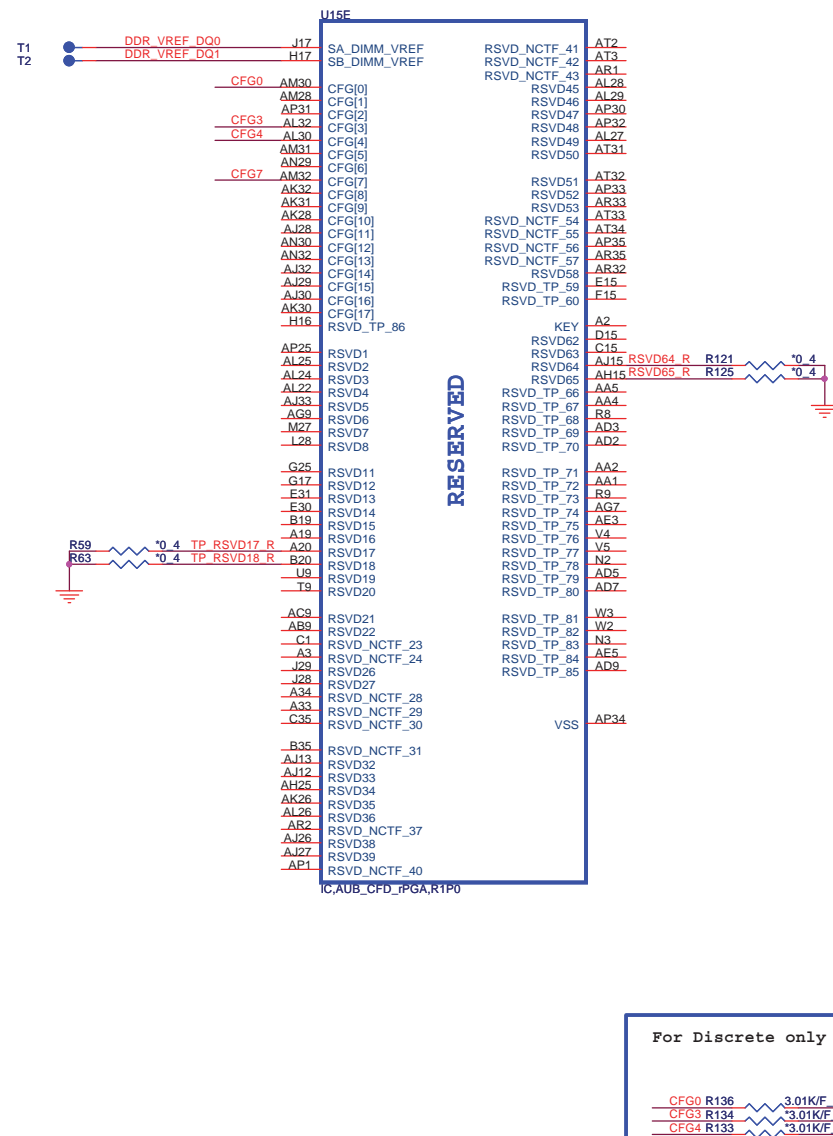
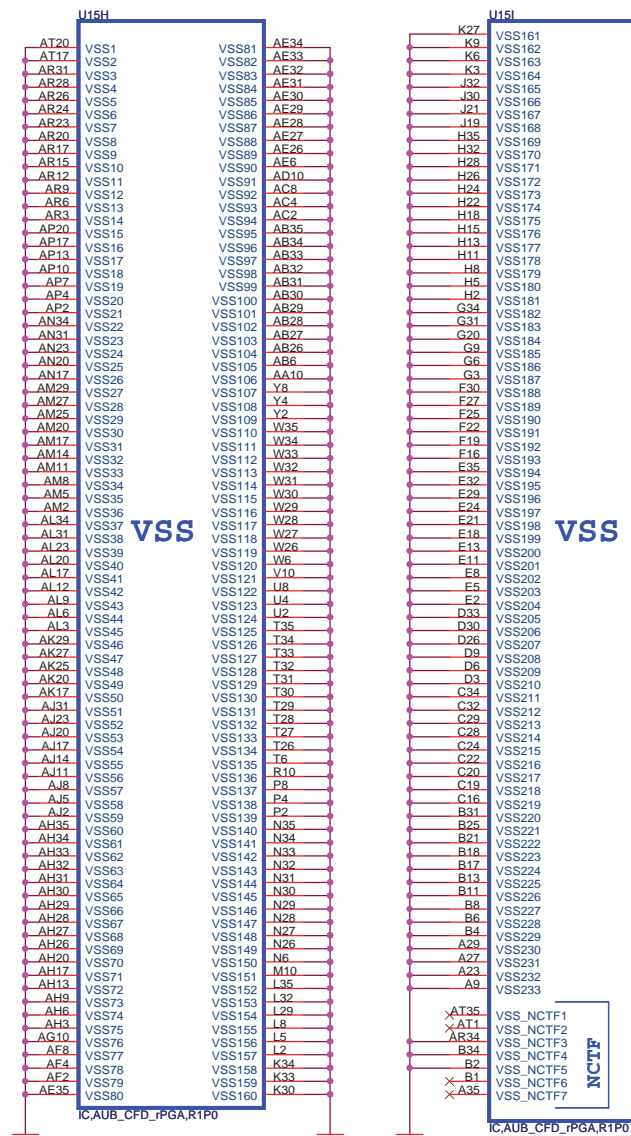
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSOR 2/4(DDR)	1A
Date: Tuesday, September 14, 2010	Sheet 4 of 39	



AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



For Discrete only



CFG[1:0] - PCI_Epress Configuration Select

* 11= 1 x 16 PEG

* 10= 2 x 8 PEG

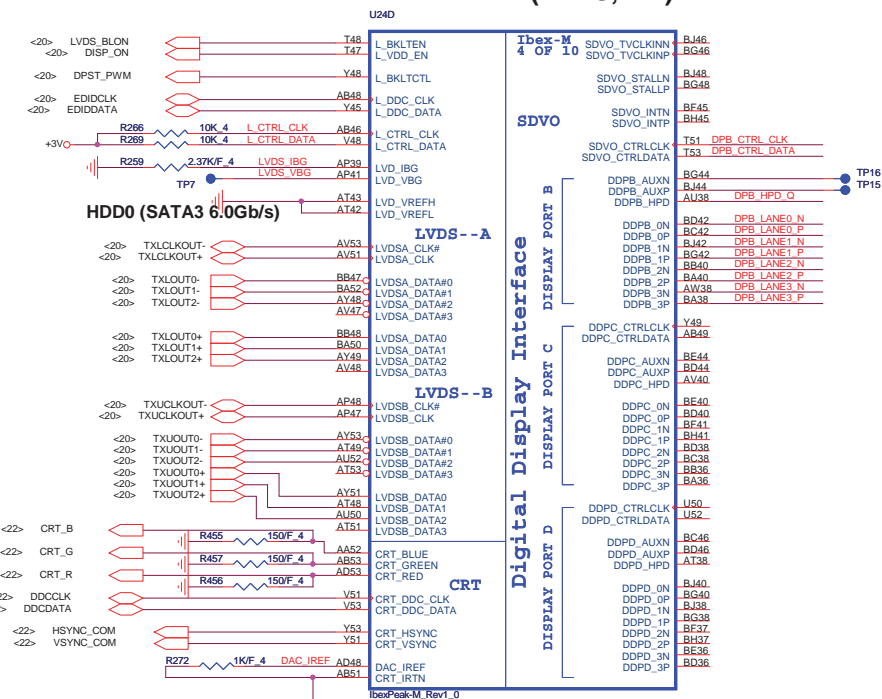


PROJECT : R12
Quanta Computer Inc.

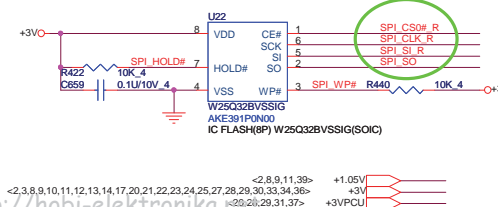
Size Custom Document Number
PROCESSOR 4/4 (GND)
 Date: Sunday, September 19, 2010 | Sheet 6 of 39

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1

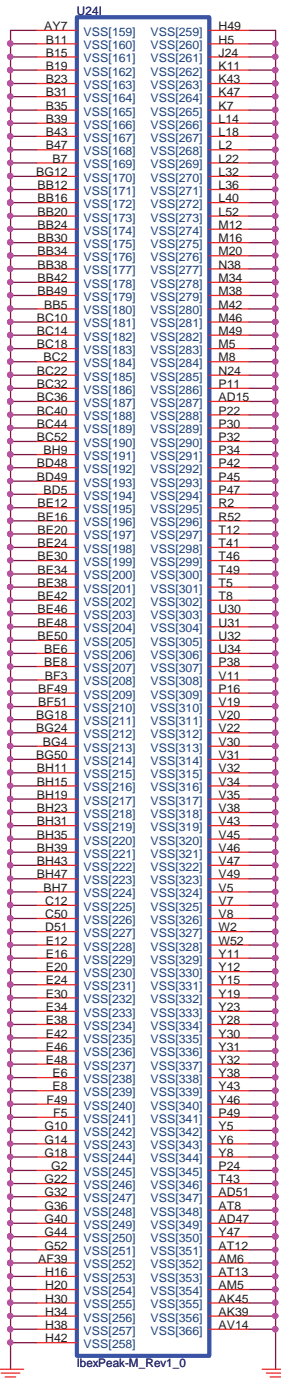
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



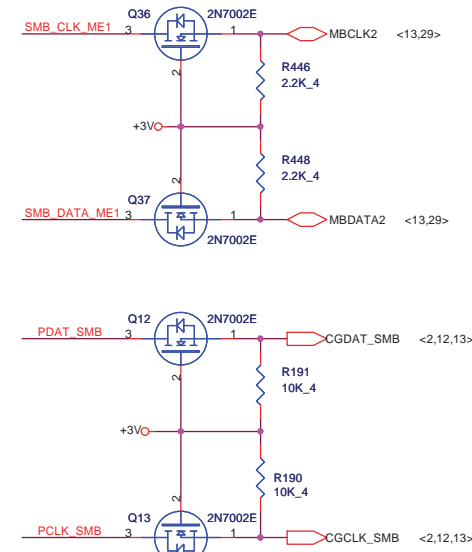
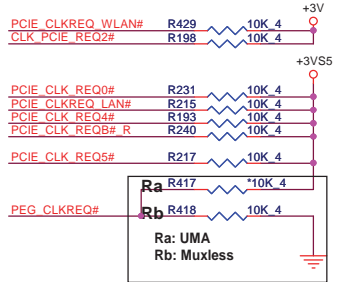
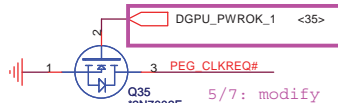
Vender
Socket DG008000031
EON - EN25F32-100HIP
AKE39FN0Q00 IC FLASH(8P) EN25F32-100HIP (SOIC)
WINBOND - W25Q32BVSSIG
AKE391P0N00 IC FLASH(8P) W25Q32BVSSIG(SOIC)



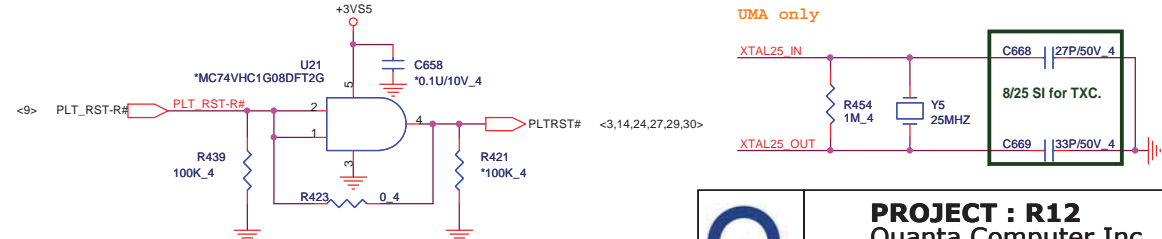
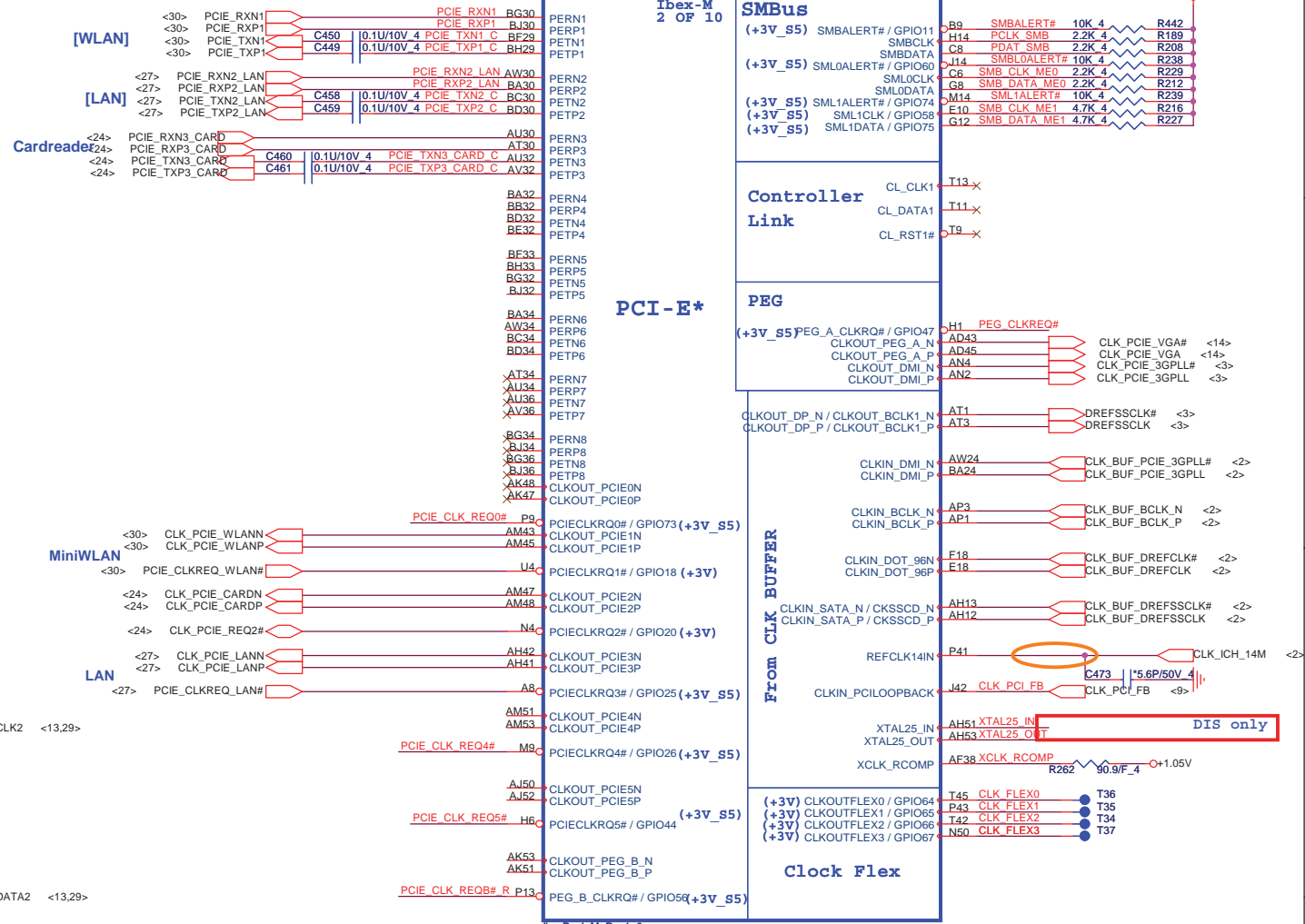
PROJECT : R12
Quanta Computer Inc.



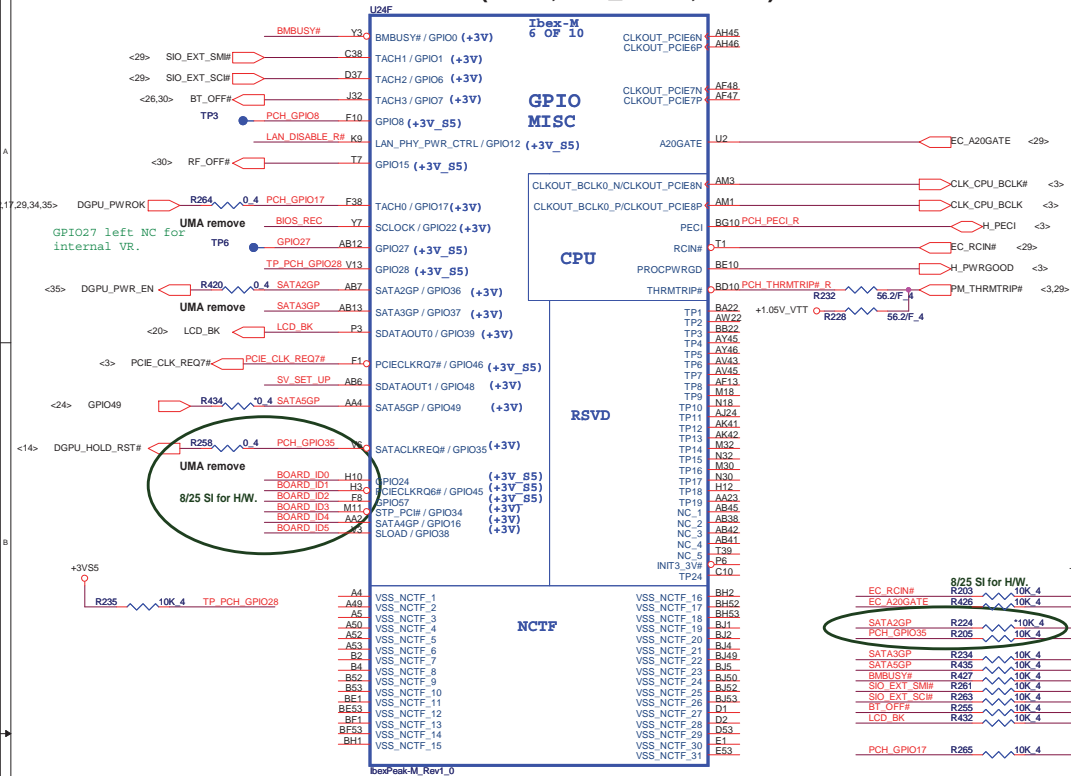
PEG Clock detect (SG only)



IBEX PEAK-M (PCI-E, SMBUS, CLK)



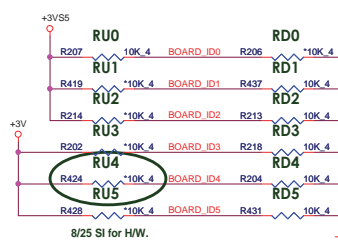
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



ibexPeak-M_Rev1.0

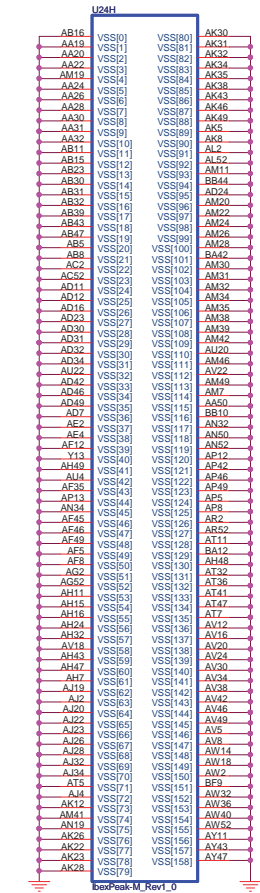
R12.MB P/N	ID0	ID1	ID2	ID3	ID4	ID5
UMA						
31R12MB0000 (PIM)	0	0	0	0	0	0
31R12MB0010 (PDT)	0	0	0	0	0	0
Seymour XT						
31R12MB0020 (PIM)	1	0	0	0	0	0
31R12MB0030 (PDT)	1	0	0	0	0	0
Samsung 512						
31R12MB0040 (PIM)	1	0	0	0	0	0
31R12MB0050 (PDT)	1	0	0	0	0	0
Hynix 1G						
31R12MB0060 (PIM)	1	0	0	0	0	0
31R12MB0070 (PDT)	1	0	0	0	0	0
Samsung 1G						
31R12MB0080 (PIM)	1	0	0	0	0	0
31R12MB0090 (PDT)	1	0	0	0	0	0

Board ID	ID0 GPIO24	ID1 GPIO45	ID2 GPIO57	ID3 GPIO34	ID4 GPIO35	ID5 GPIO38
UMA	0=UMA 1=DIS.					
Reserve		0=No 1=Yes				
Reserve			0=No 1=Yes			
Reserve				0=No 1=Yes		
Reserve					0=No 1=Yes	
Reserve						0=No 1=Yes



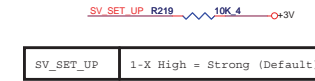
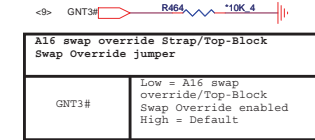
8/25 SI for H.W.

IBEX PEAK-M (GND)



ibexPeak-M_Rev1.0

10



PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SP1

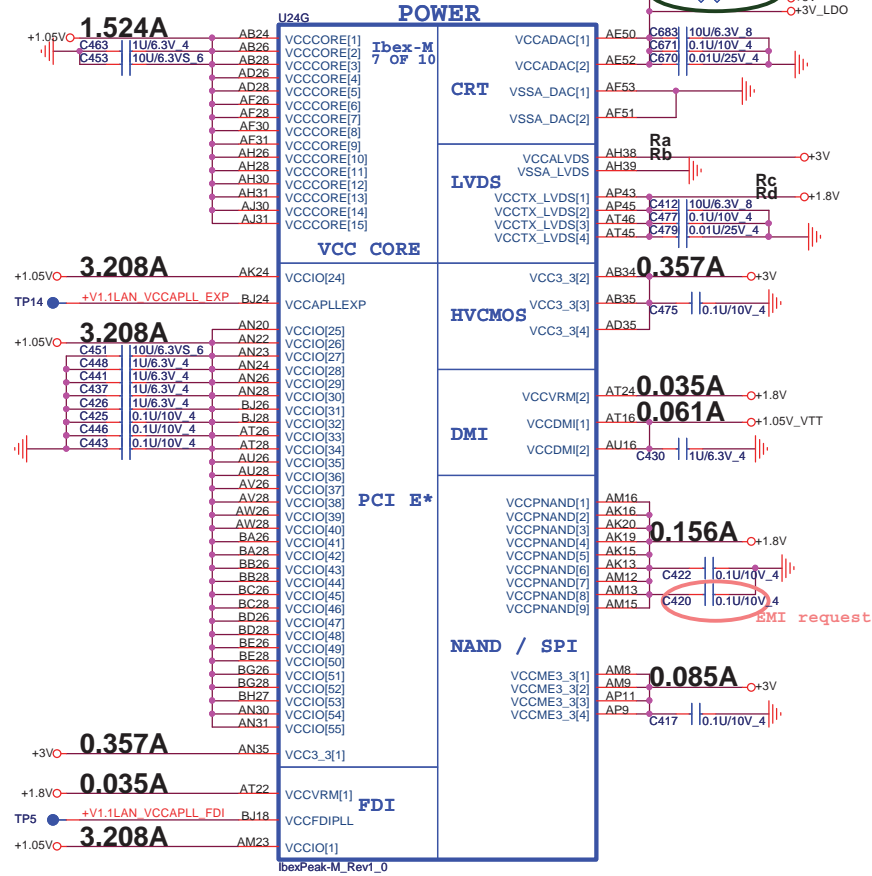
Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

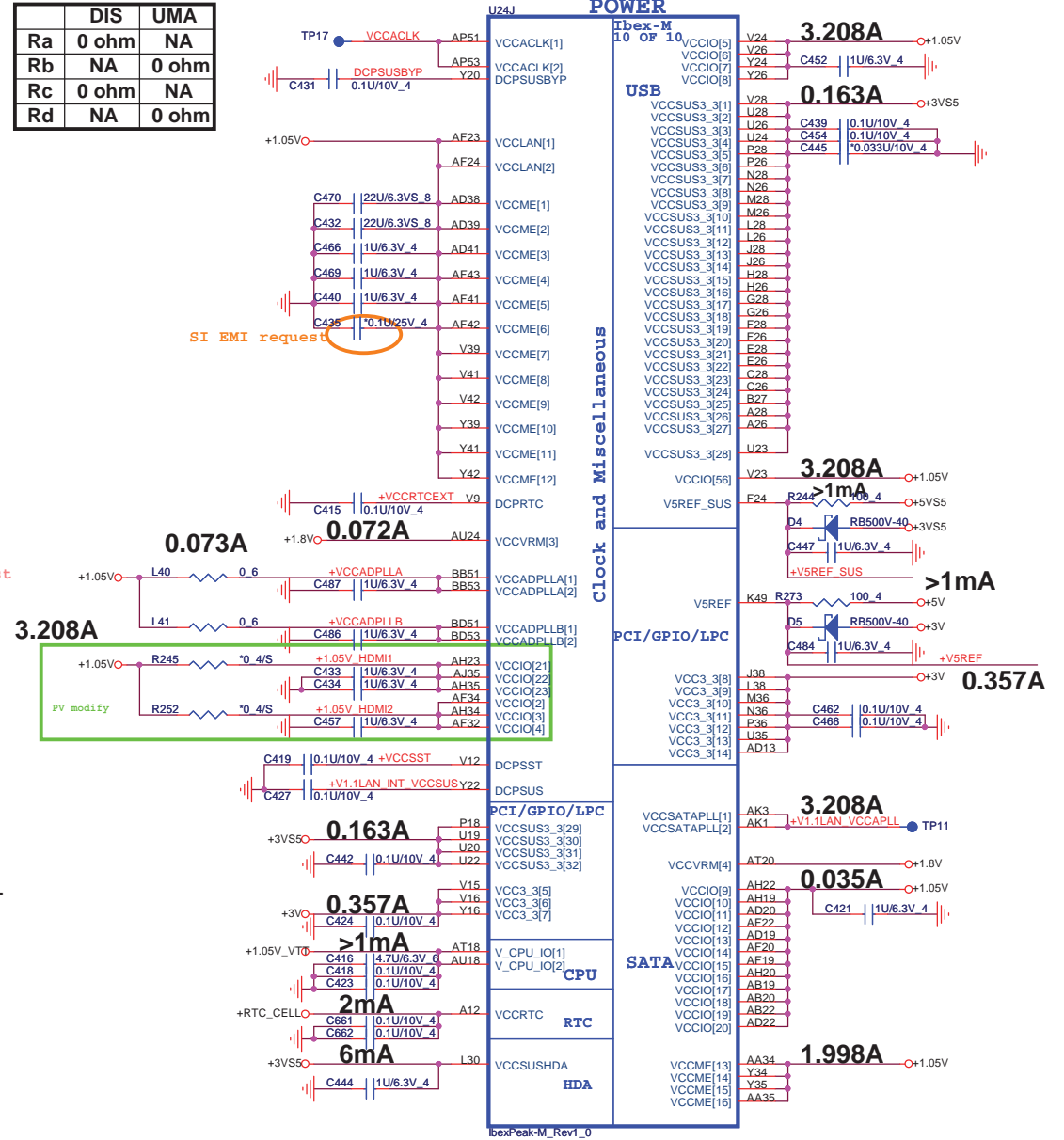
No Reboot Strap



8/25 SI modify
Uninstall on UMA
Install on DIS



	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

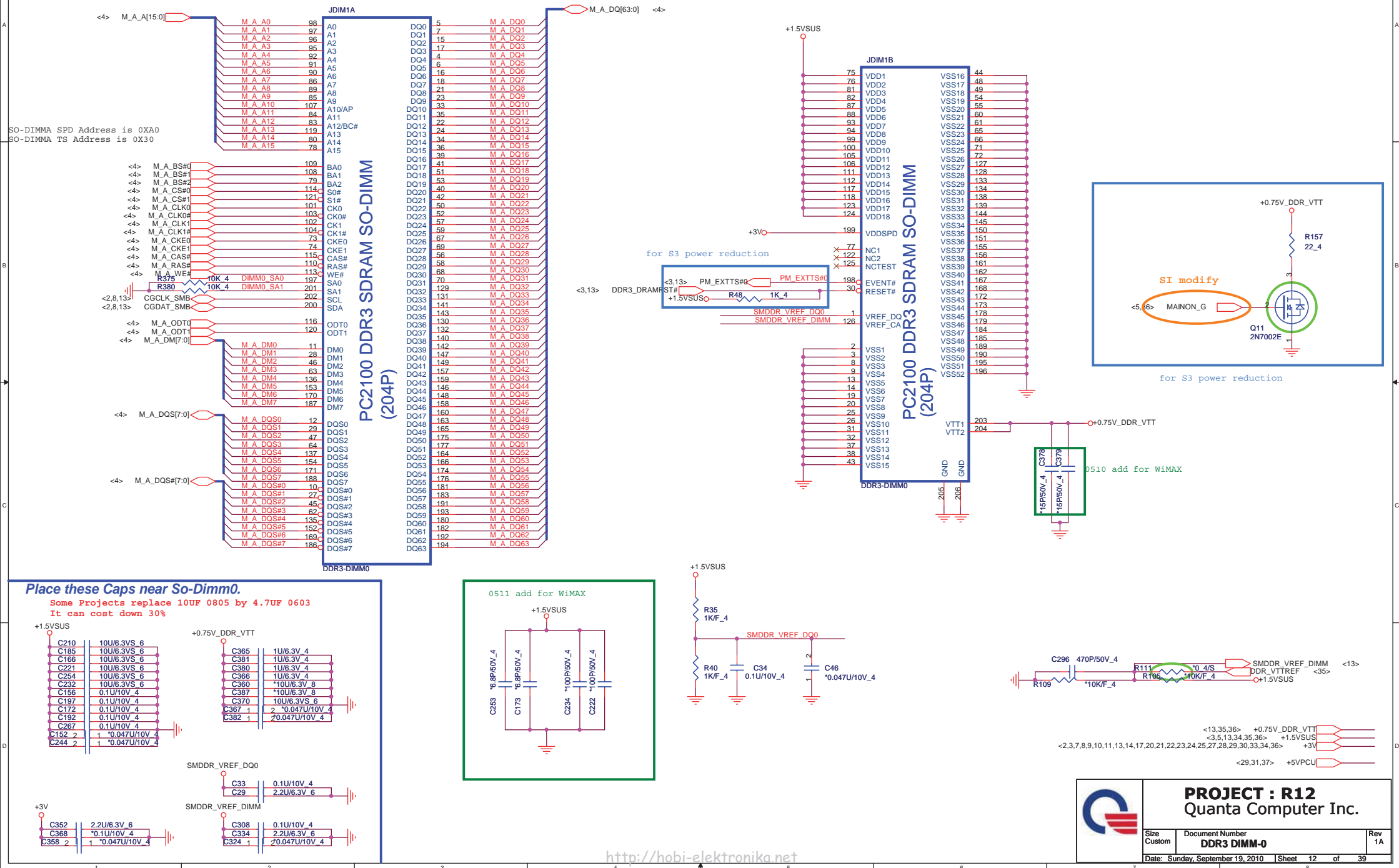


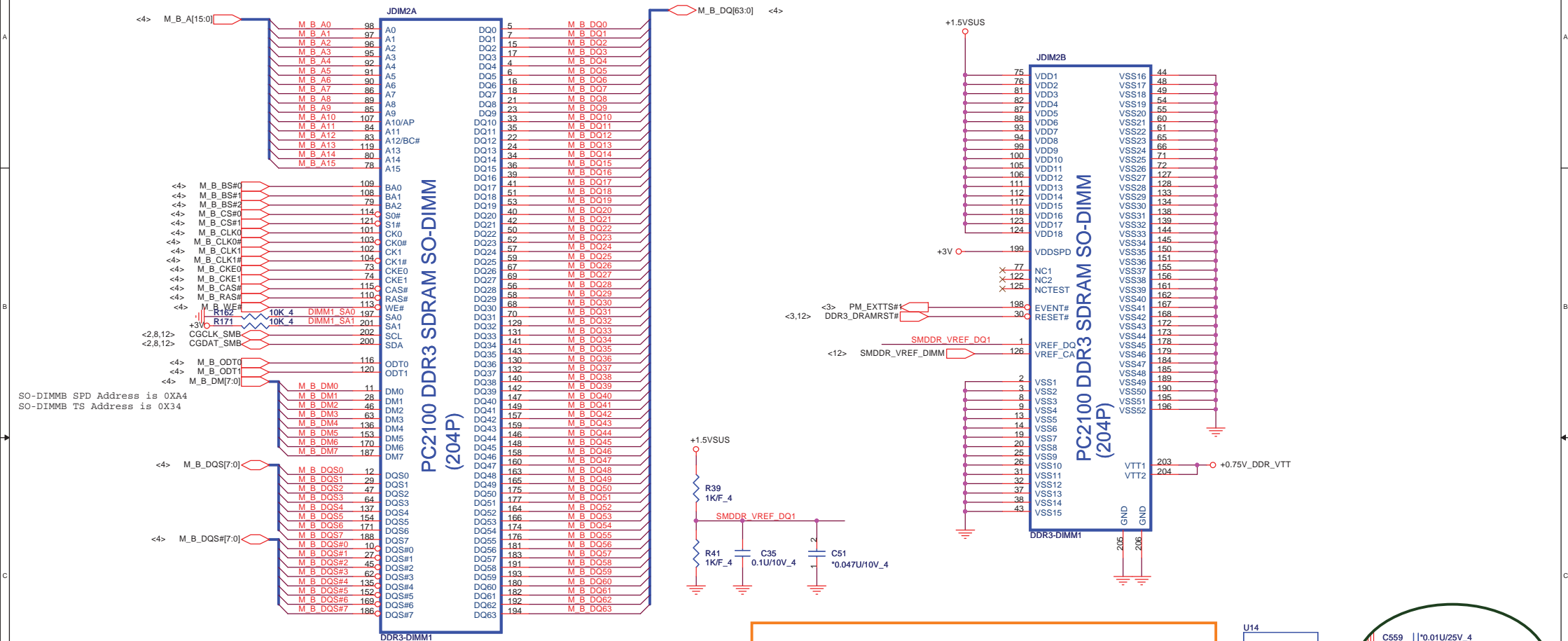
<2,7,8,9,39>	+1.05V
<3,5,10,29,32,33,38>	+1.05V_VTT
<5,32>	+1.8V
<3,7,8,9,10,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36>	+3V
<3,7,8,9,10,26,31,32,34,35,36,38>	+3VS5
<17,21,22,23,25,28,30,36>	+5V
<20,26,31,32,33,34,35,36,38,39>	+5VS5



PROJECT : R12
Quanta Computer Inc.

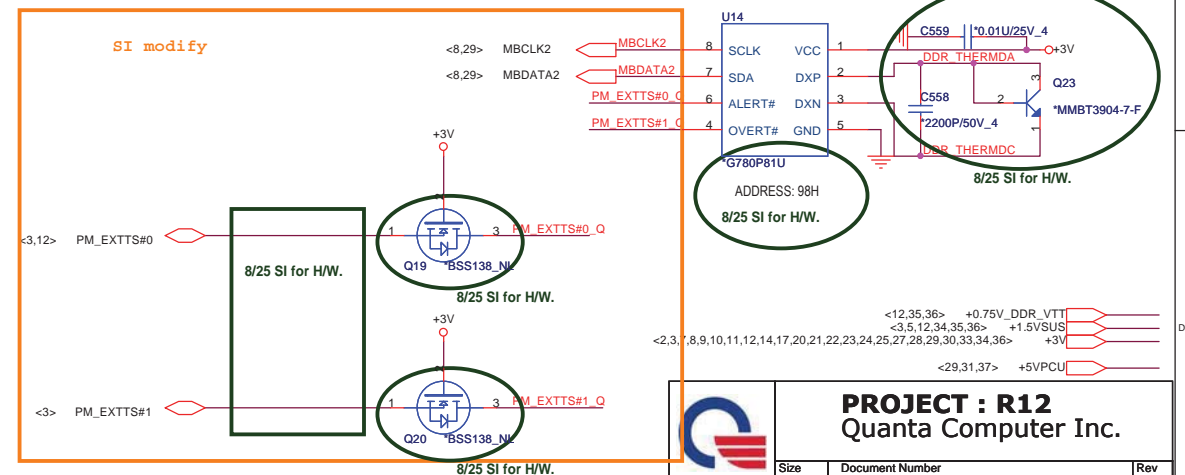
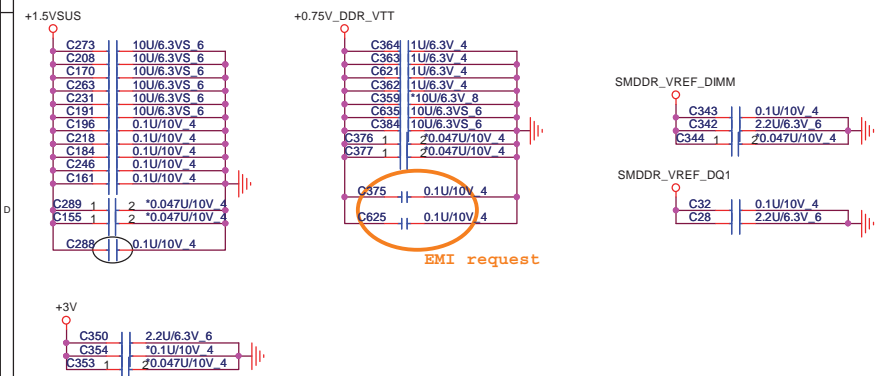
Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	1A
Date:	Sunday, September 19, 2010	Sheet 11 of 39

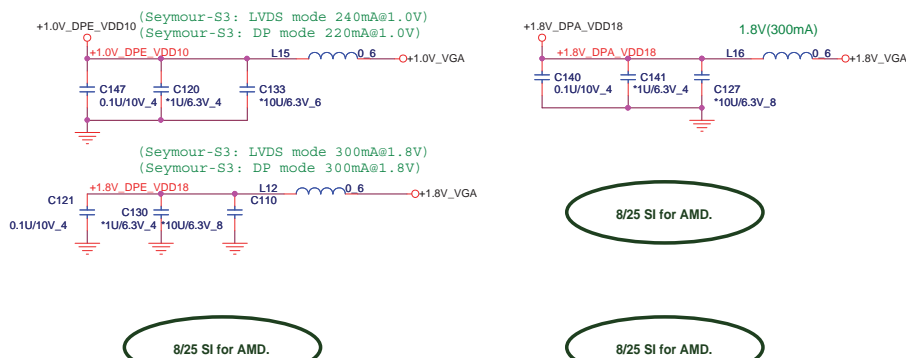
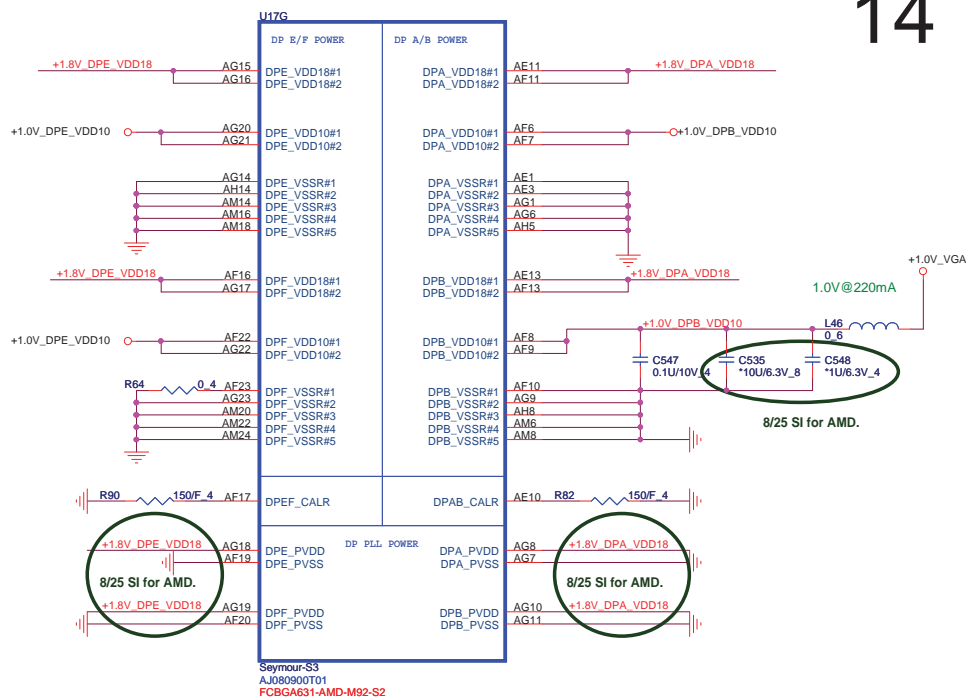
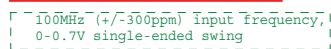




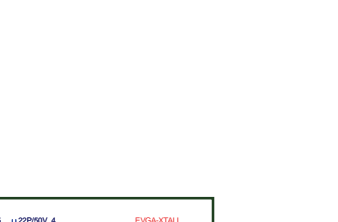
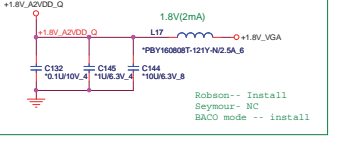
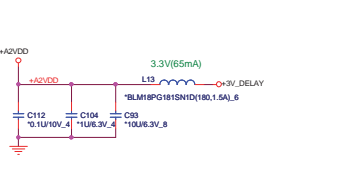
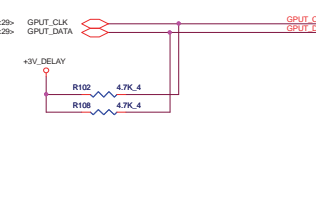
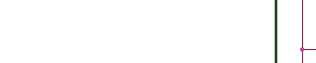
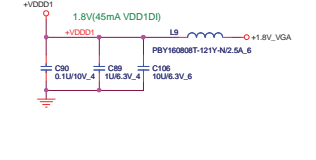
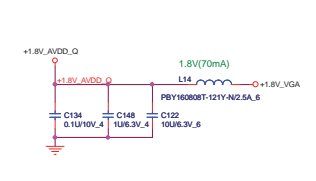
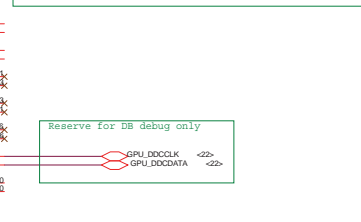
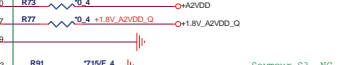
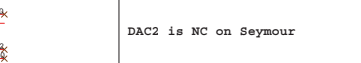
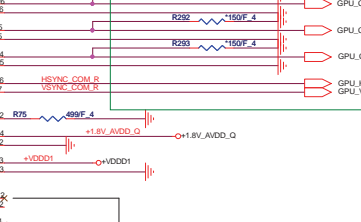
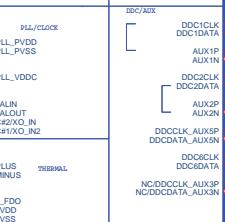
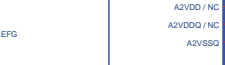
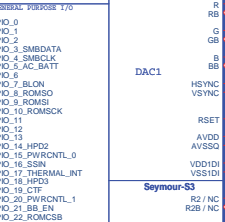
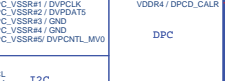
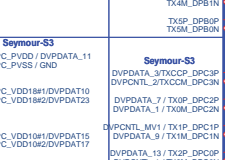
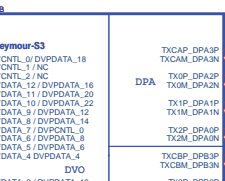
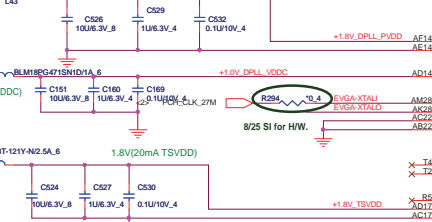
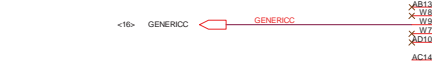
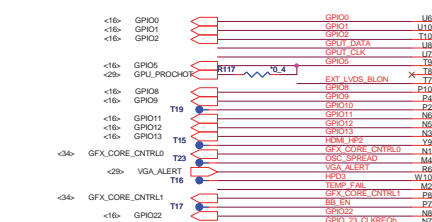
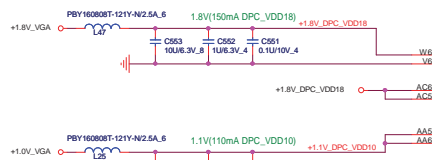
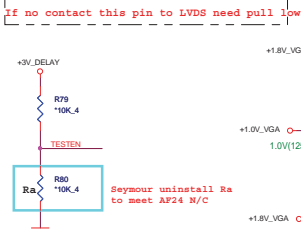
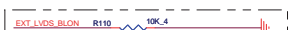
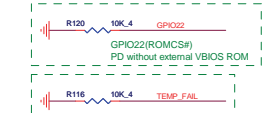
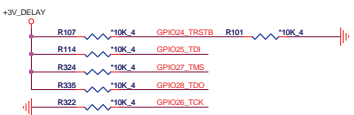
Place these Caps near So-Dimm1.

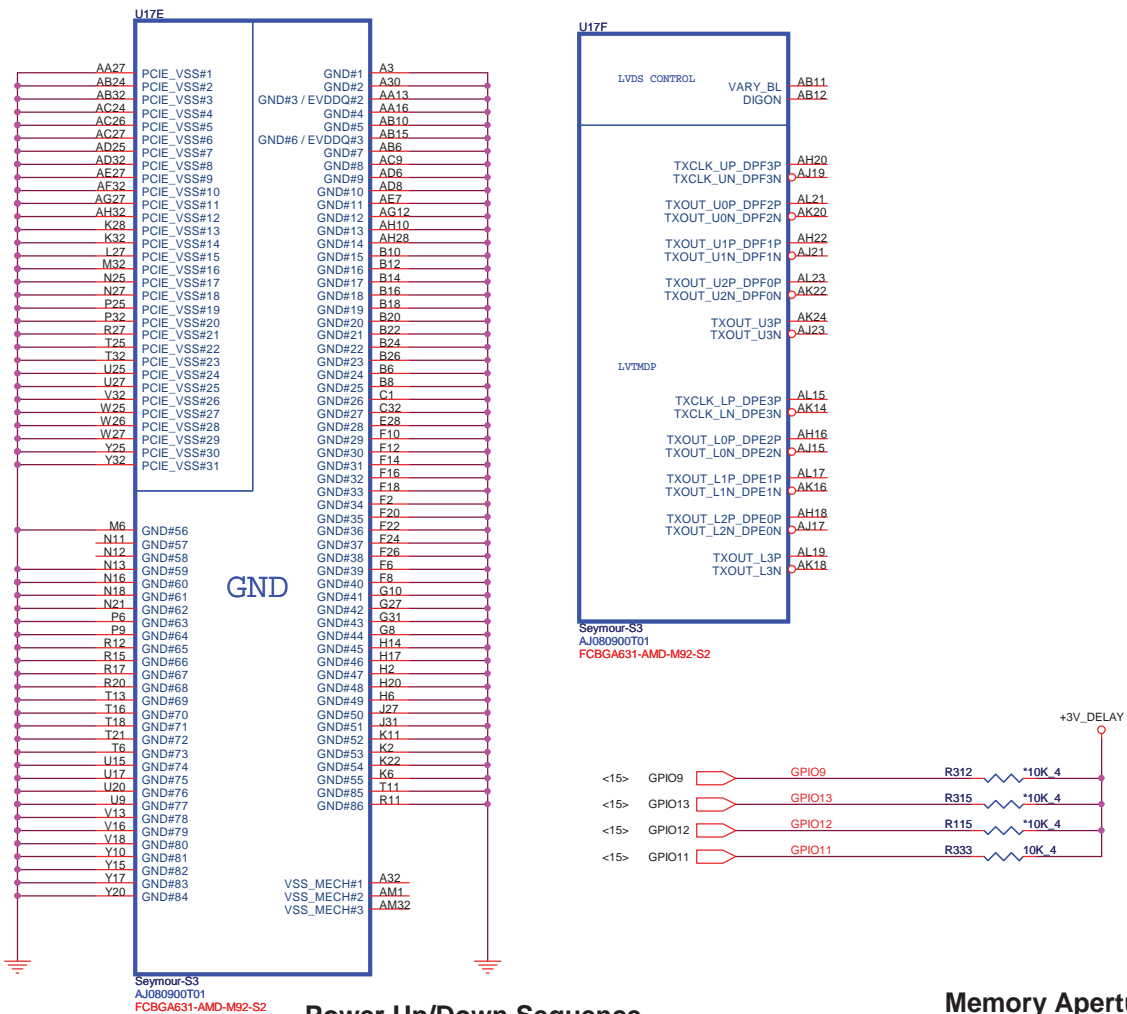
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%





GPIO15 GPIO20			
Seymour	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	0.95V
H	1	0	1.12V (Default)
TBD	1	1	NA





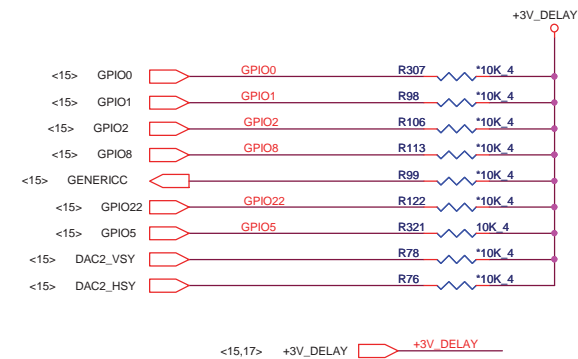
CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS		
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

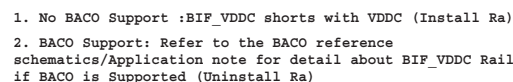


PROJECT : R12
Quanta Computer Inc.

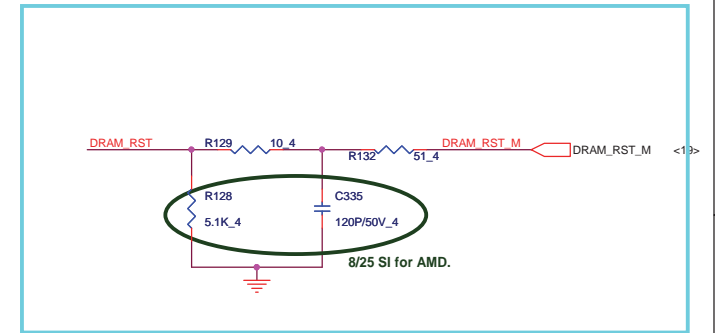
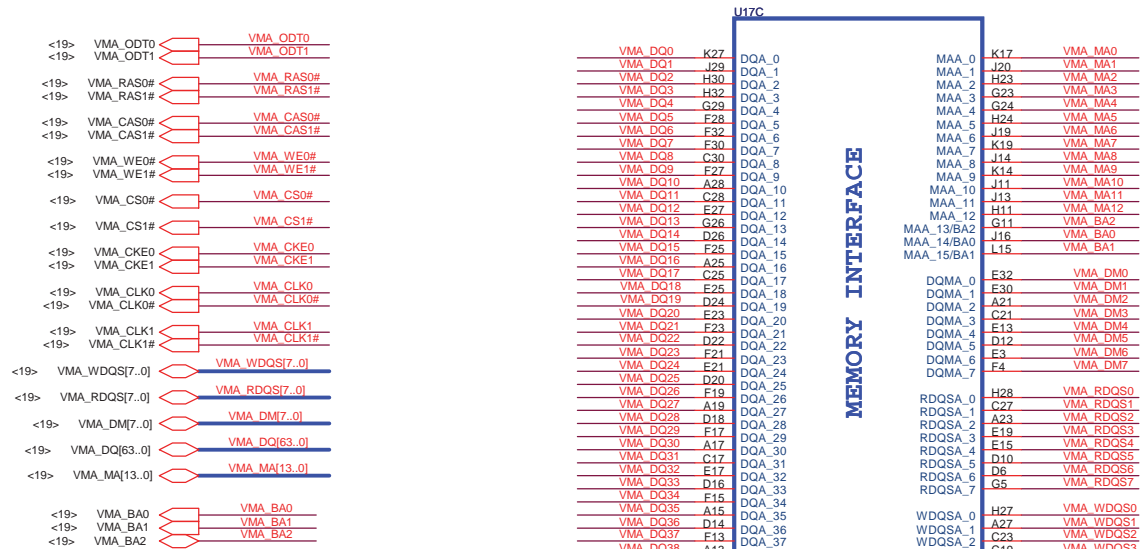
Size Custom	Document Number Seymour GND / LVDS / Straps	Rev 1A
Date: Sunday, September 19, 2010	Sheet 16 of 39	



PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE



Size Custom	Document Number Seymour_Power_and_NC	Re 1
Date: Sunday, September 19, 2010	Sheet 17 of 39	

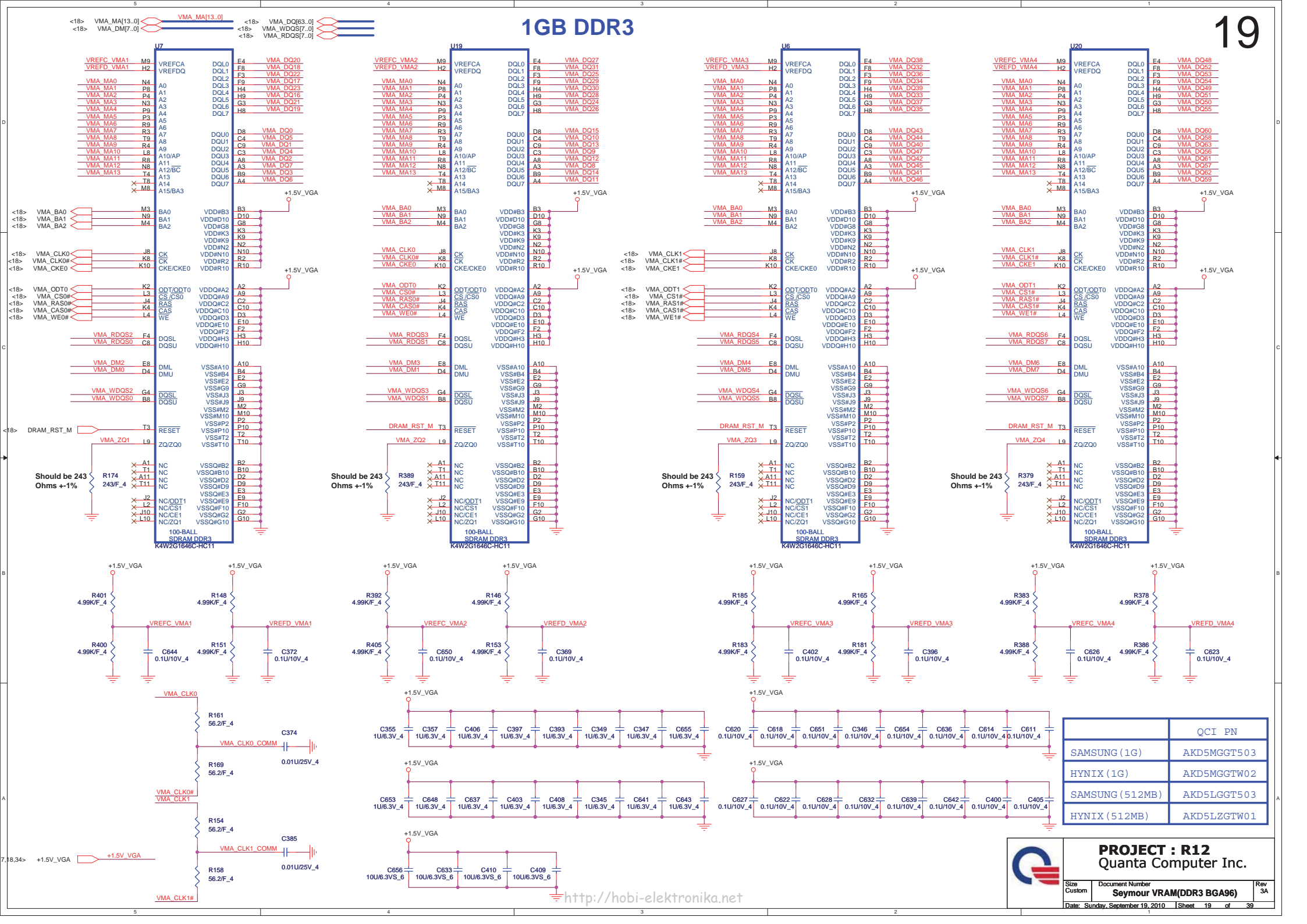


Seymour-S3
A089900101
FCBGA631-AMD-M92-S2
8/25 SI for SMT.



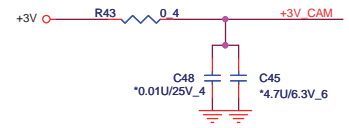
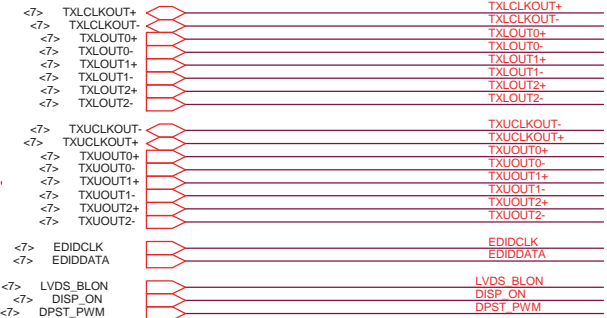
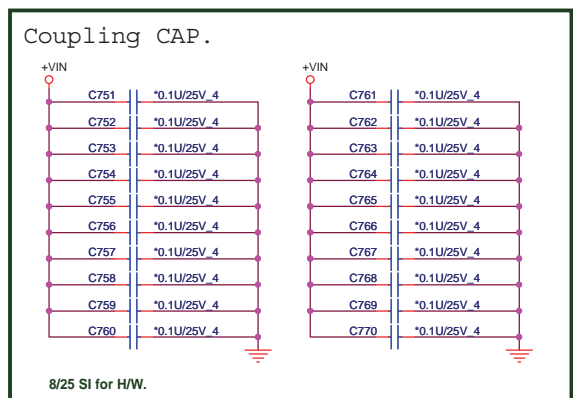
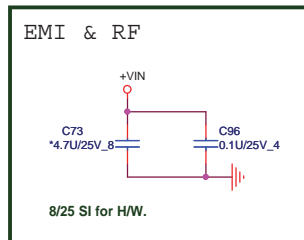
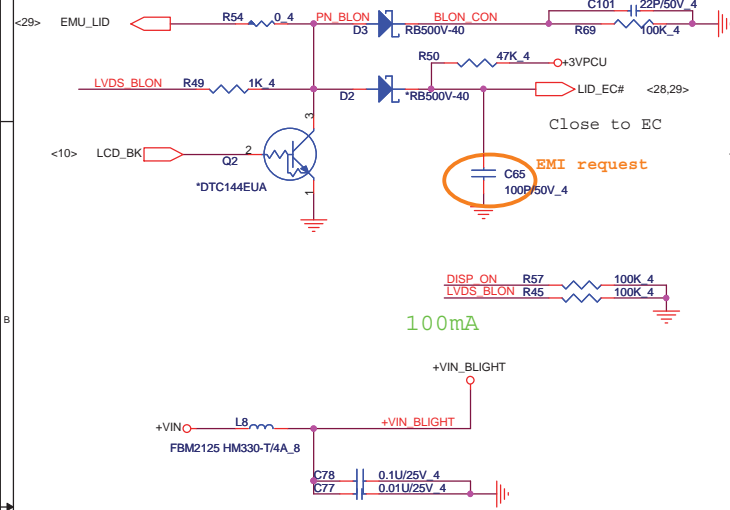
PROJECT : R12
Quanta Computer Inc.

1GB DDR3



LID Switch

20

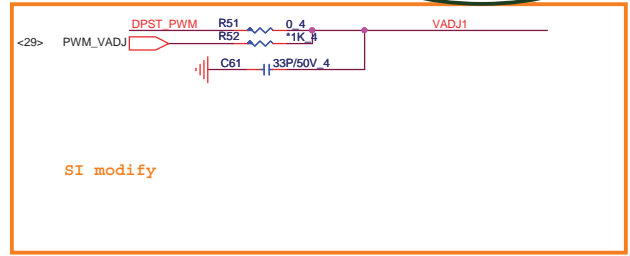
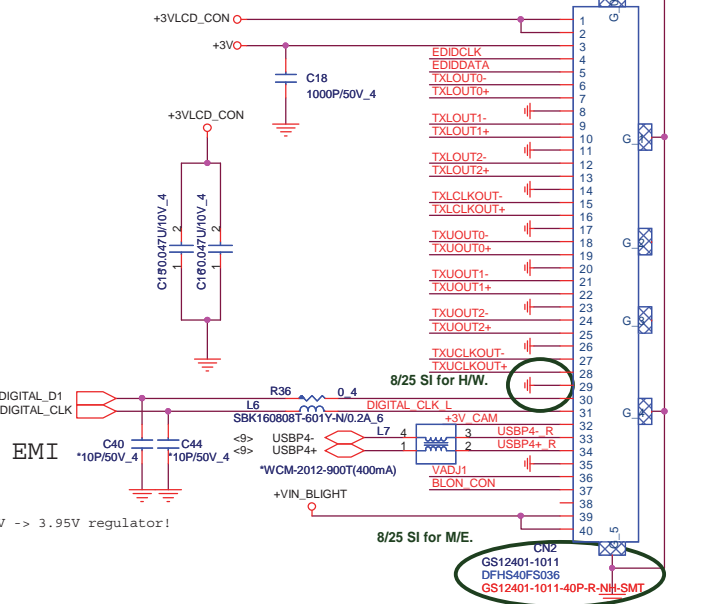
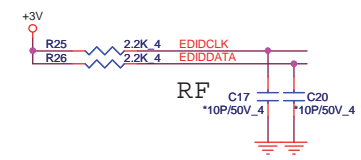
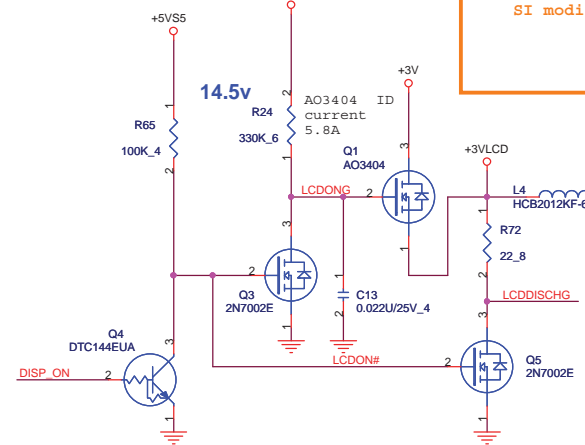


follow L4 location

USBP4- R44 0.4 USBP4- R

USBP4+ R46 0.4 USBP4+ R

change to +5VS5



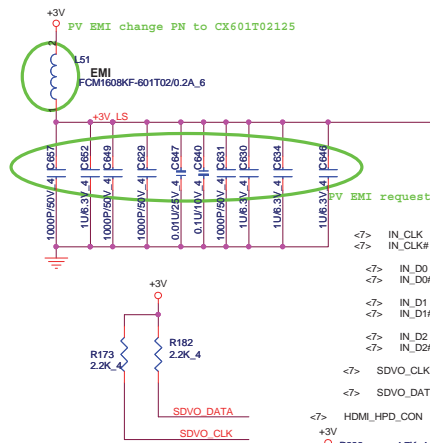
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
Date:	Sunday, September 19, 2010	Sheet 20 of 39

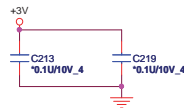
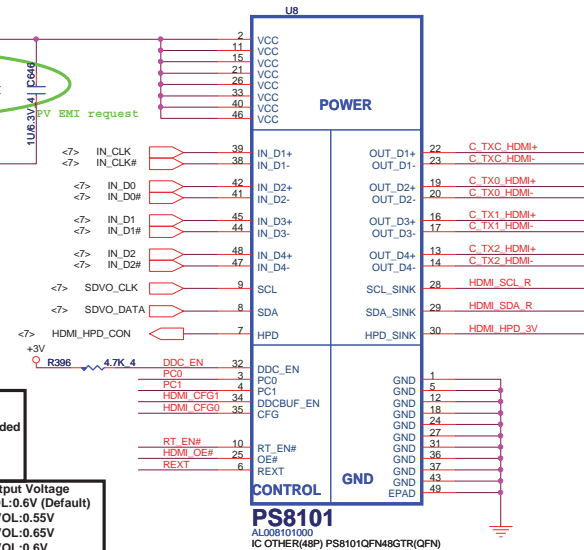
The schematic diagram illustrates the HDMI input section of the 4P2R-S-33 module. A 3V supply is connected to a network of resistors and capacitors. The network consists of resistors Rg, Ra, Rb, Rc, Re, and Rf, and capacitors R403, R393, R407, R406, R397, R391, R408, and R404. The network is connected to the HDMI input pins (HDMI_0E#, HDMI_CFG0, HDMI_CFG1) and the HDMI input signal lines (HDMI_SCL R, HDMI_SDA R). The output of the network is connected to the HDMI input pins of the 4P2R-S-33 module.

9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

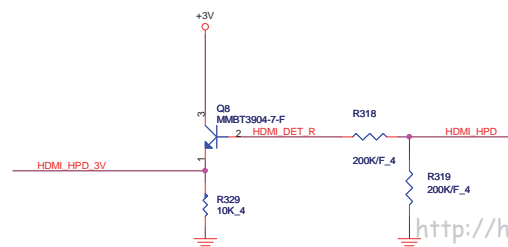
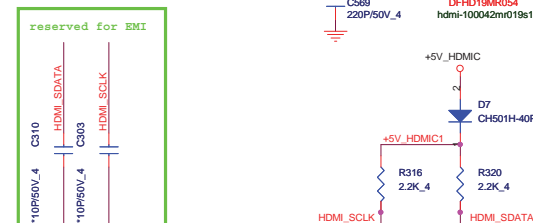
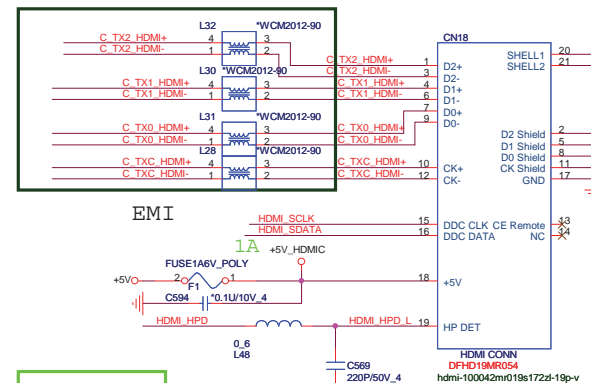
CHR : need Na R1182, add R1027 for capella



SCLZ/SDAZ Low-level input/output Voltage	
CFG1:CFG0=0:0	VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1	VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0	VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1	VIL:<0.36V VOL:0.6V



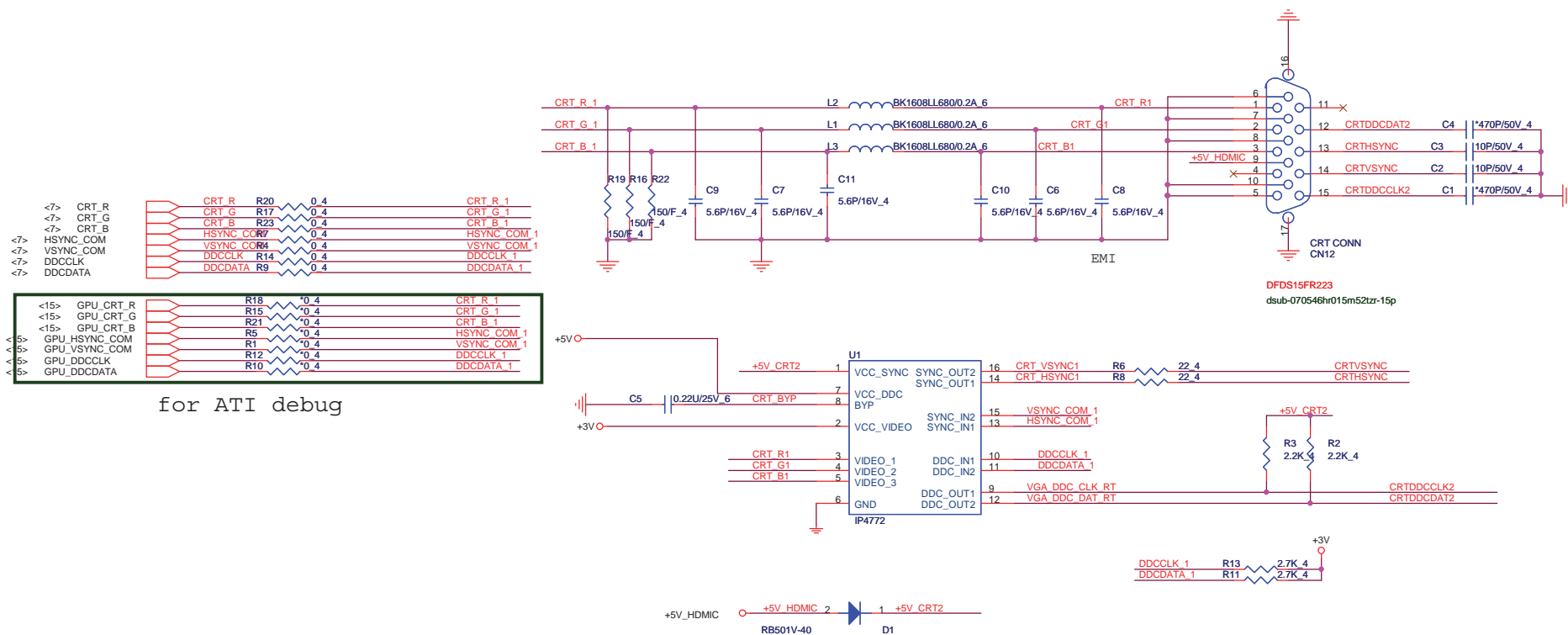
C_TX2_HDMI+	R504	*100/F 4	C_TX2_HDMI-
C_TX1_HDMI+	R505	*100/F 4	C_TX1_HDMI-
C_TX0_HDMI+	R506	*100/F 4	C_TX0_HDMI-
C_TXC_HDMI+	R507	*100/F 4	C_TXC_HDMI-



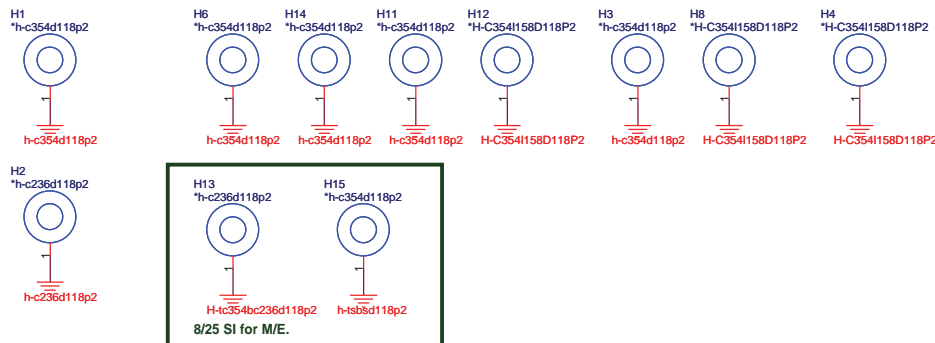
PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number HDMI CONN	Rev 1A
Date: Sunday, September 19, 2010	Sheet 21 of 39	

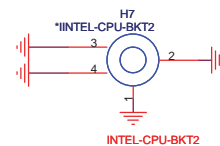
CRT PORT



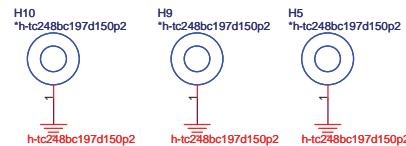
HOLE



CPU

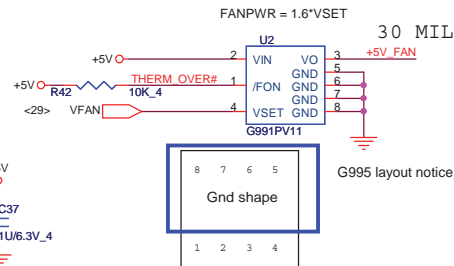
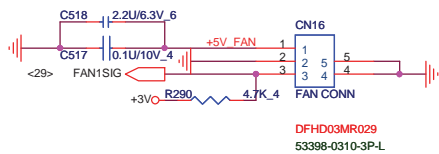


VGA



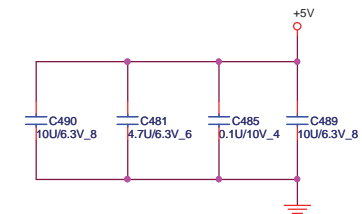
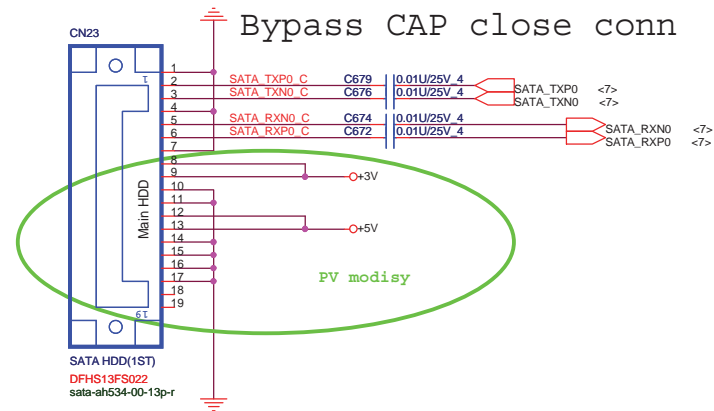
PROJECT : R12
Quanta Computer Inc.

CPU FAN

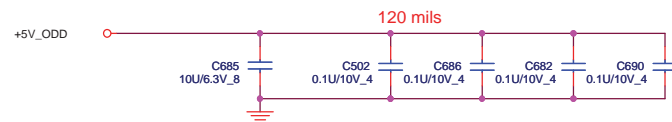
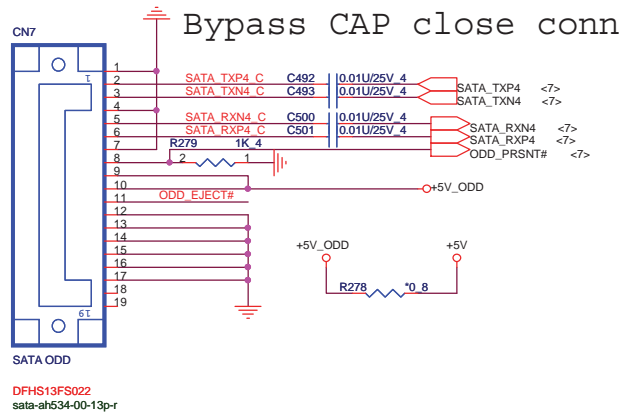


SATA HDD CONNECTOR

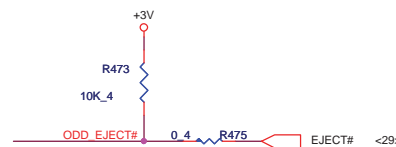
23



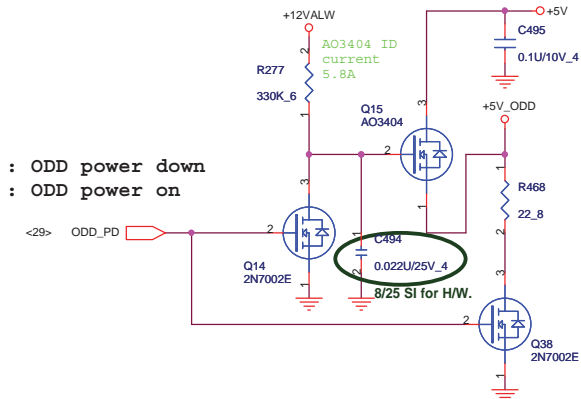
SATA ODD CONNECTOR



follow INTEL DG change eject PU to +3V.

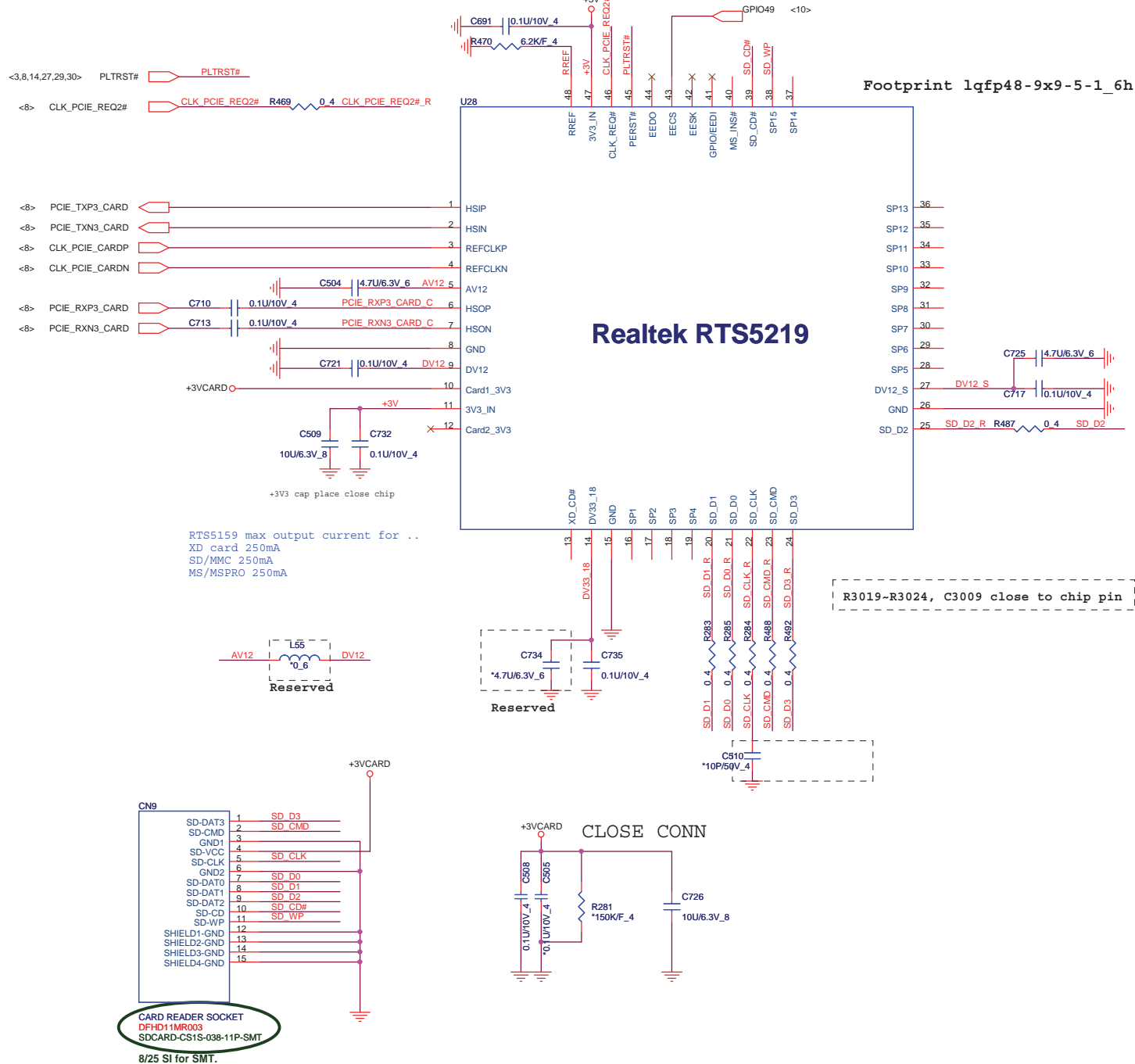


High : ODD power down
Low : ODD power on



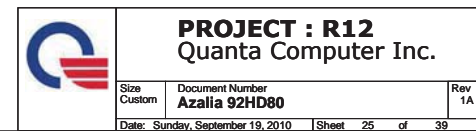
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A
Date: Sunday, September 19, 2010	Sheet 23 of 39	

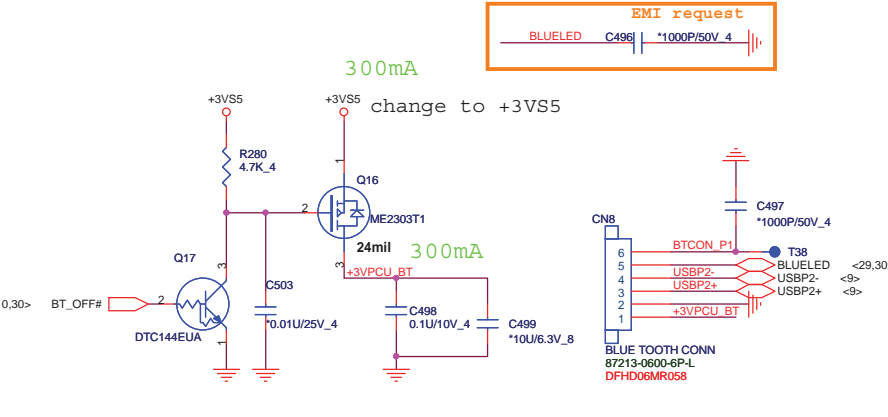


PROJECT : R12
Quanta Computer Inc.

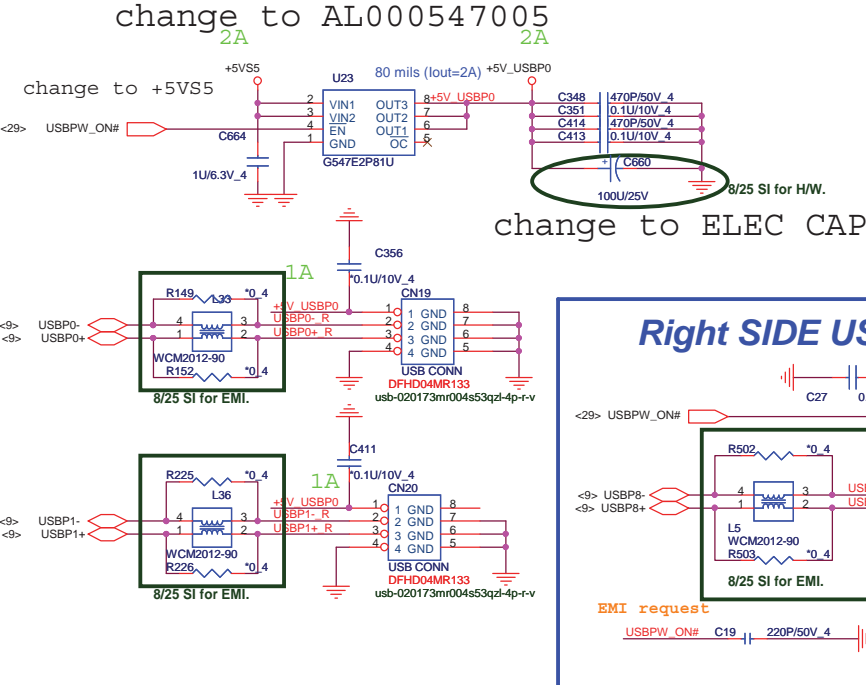
Size	Document Number	Rev
Custom	RTS5219 & CR SOCKET & HOLE	1A
Date:	Sunday, September 19, 2010	Sheet 24 of 39



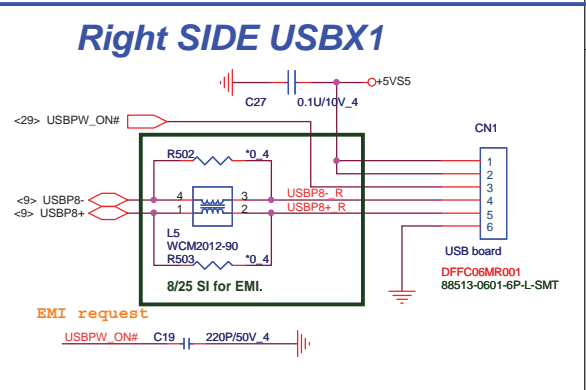
BLUETOOTH



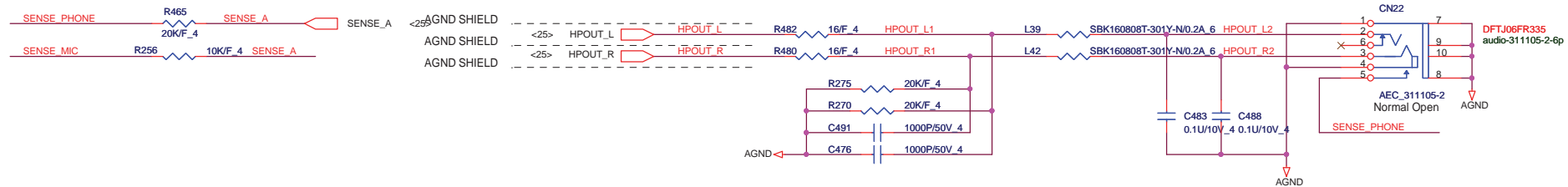
LEFT SIDE USB2



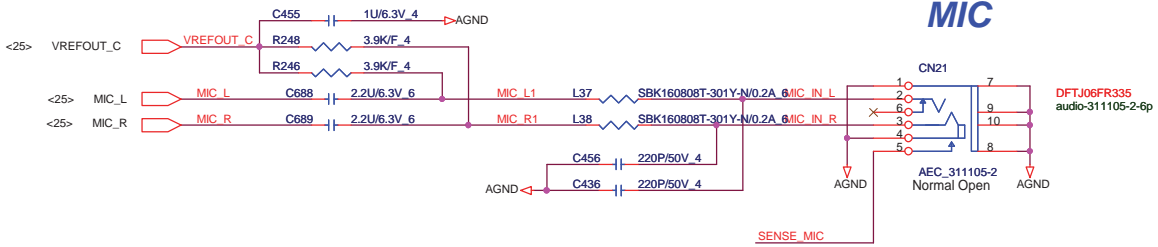
Right SIDE USBX1



Line out

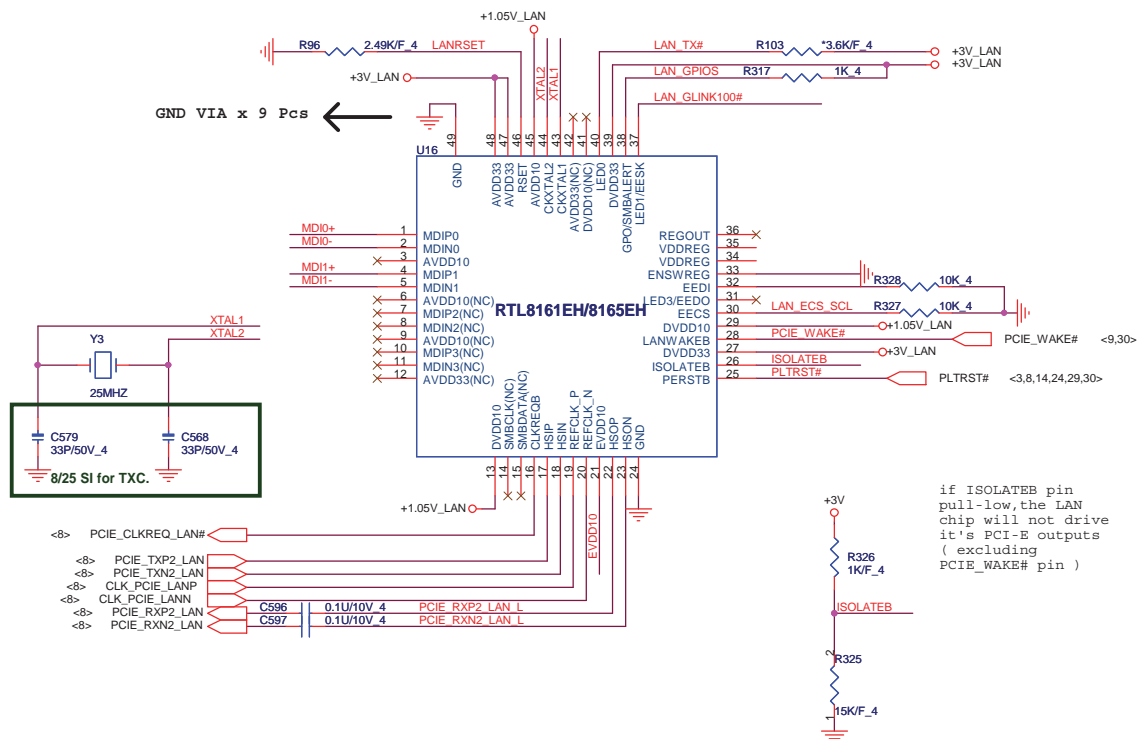


MIC



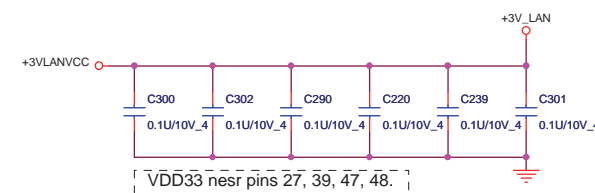
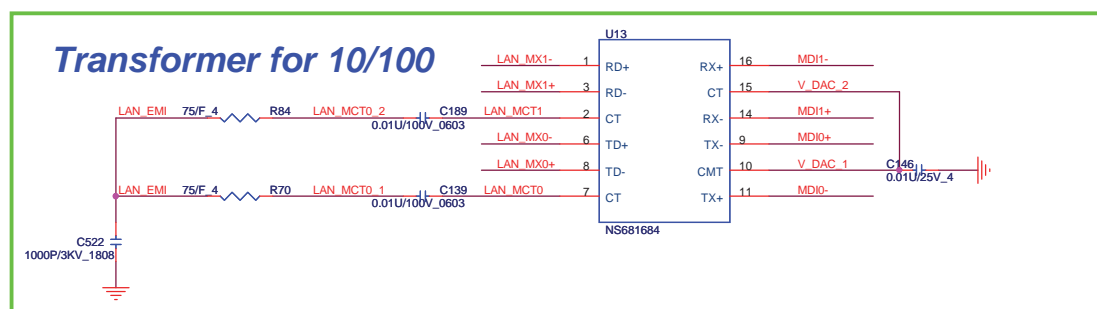
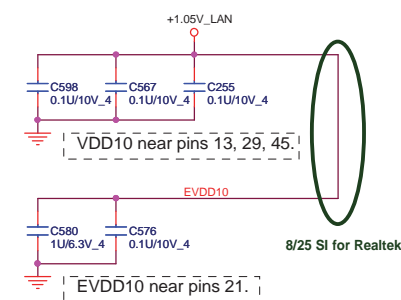
PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number USB/BT/Audio Jack	Rev 1A
Date: Sunday, September 19, 2010	Sheet 26 of 39	

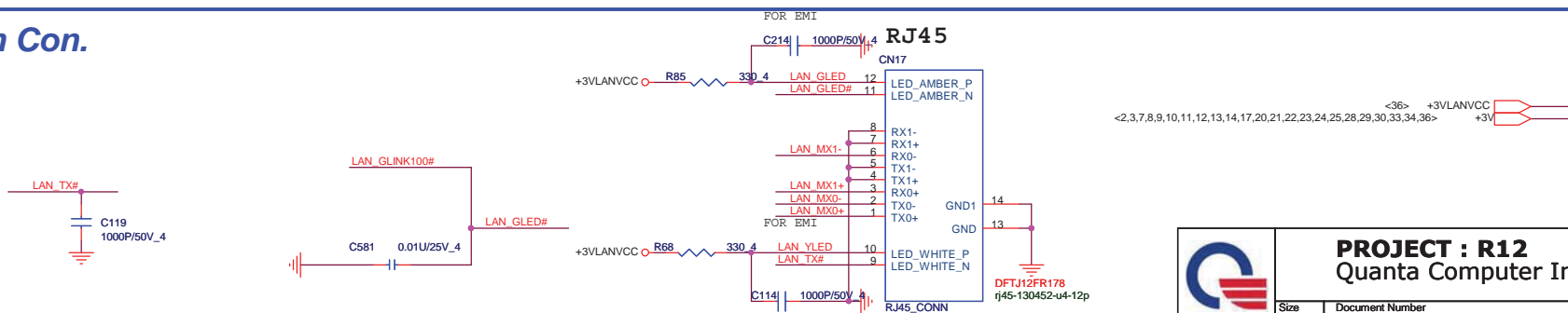


IND SMD 4.7UH +-20% 680MA (CBC2518T4R7M)
CV-4707MZ00

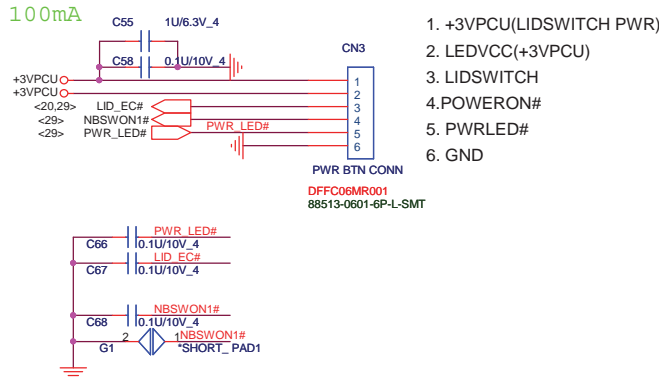
Power trace Layout 寬度> 60mil
>60mil



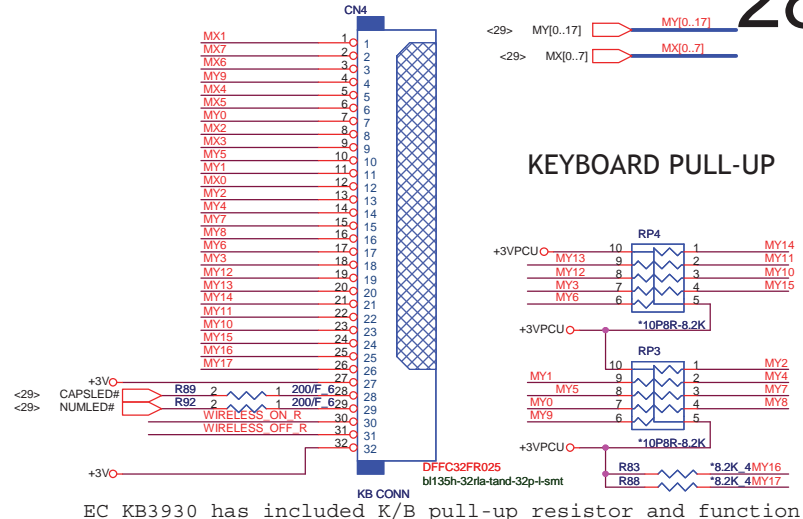
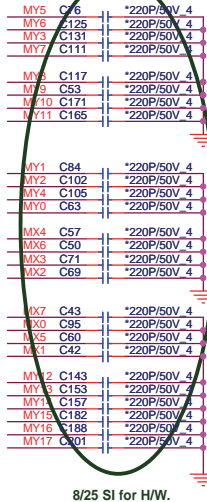
Lan Con.



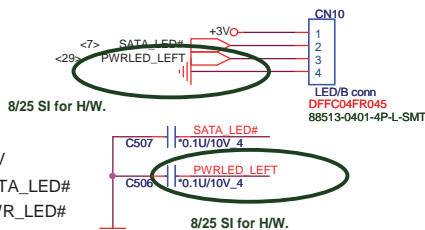
POWER BOTTON CONNECT



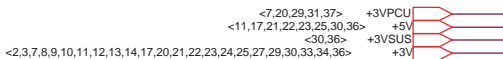
KEYBOARD Con.



LED Con.

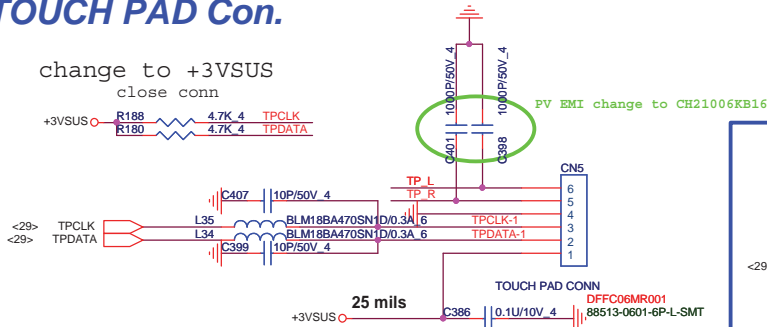


1. +3V
2. SATA_LED#
3. PWR_LED#
4. GND

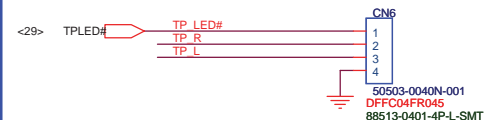


TOUCH PAD Con.

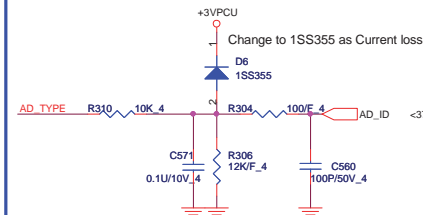
```
change to +3VSUS
close conn
```



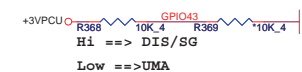
To TOUCH PAD SW board



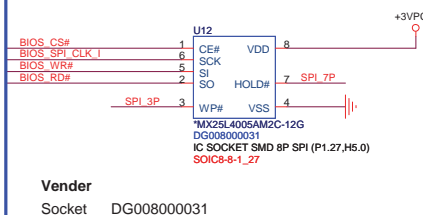
PROJECT : R12
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adapter select for EC

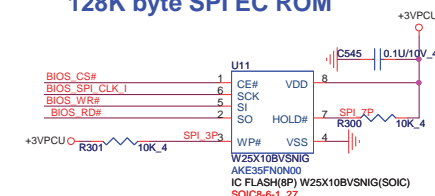


512K byte SPI EC ROM



Vender
Socket DG008000031

128K byte SPI EC ROM



Vender
Socket DG008000031
EON - EN25F10-100GIP
AKE35FN0Q00 IC FLASH(8P) EN25F10-100GIP(SOIC)
WINBOND - W25X10BVSNIG
AKE35FN0N00 IC FLASH(8P) W25X10BVSNIG(SOIC)

FOR SG/IS

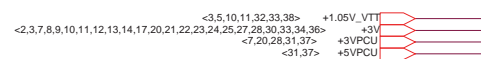
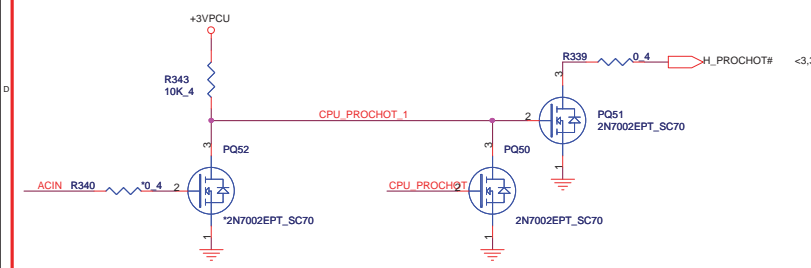
UMA remove

<210,17,34,35> DGPU_PWROK R360 0.4 EC_GPXD1

<34,35> DGPU_PR_EN R359 0.4 DGPU_PR_EN_E

R358 100K_4

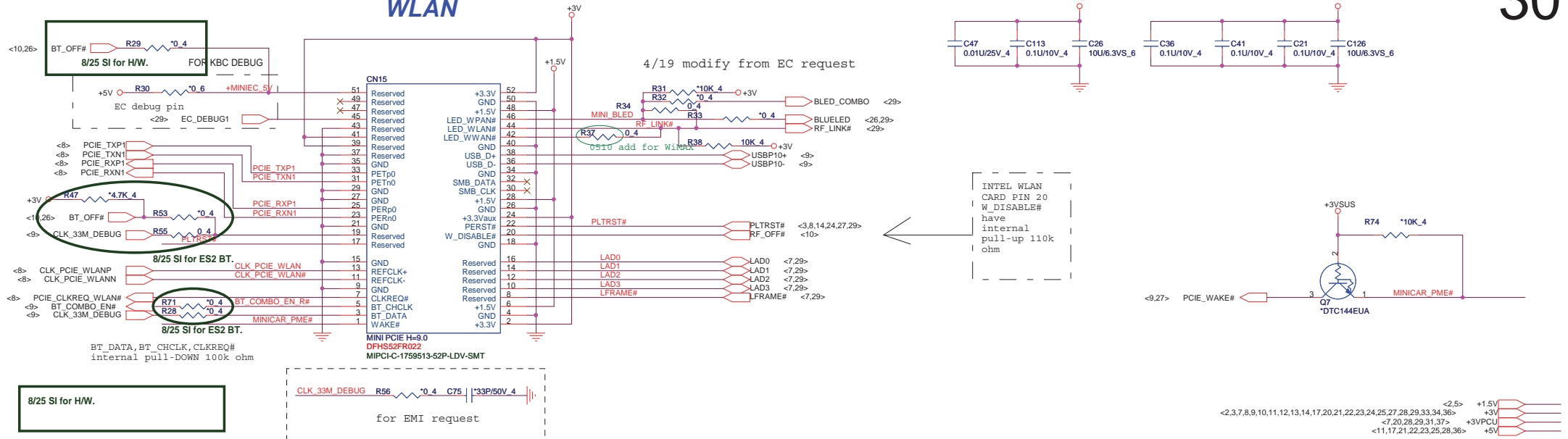
8/25 SI for H

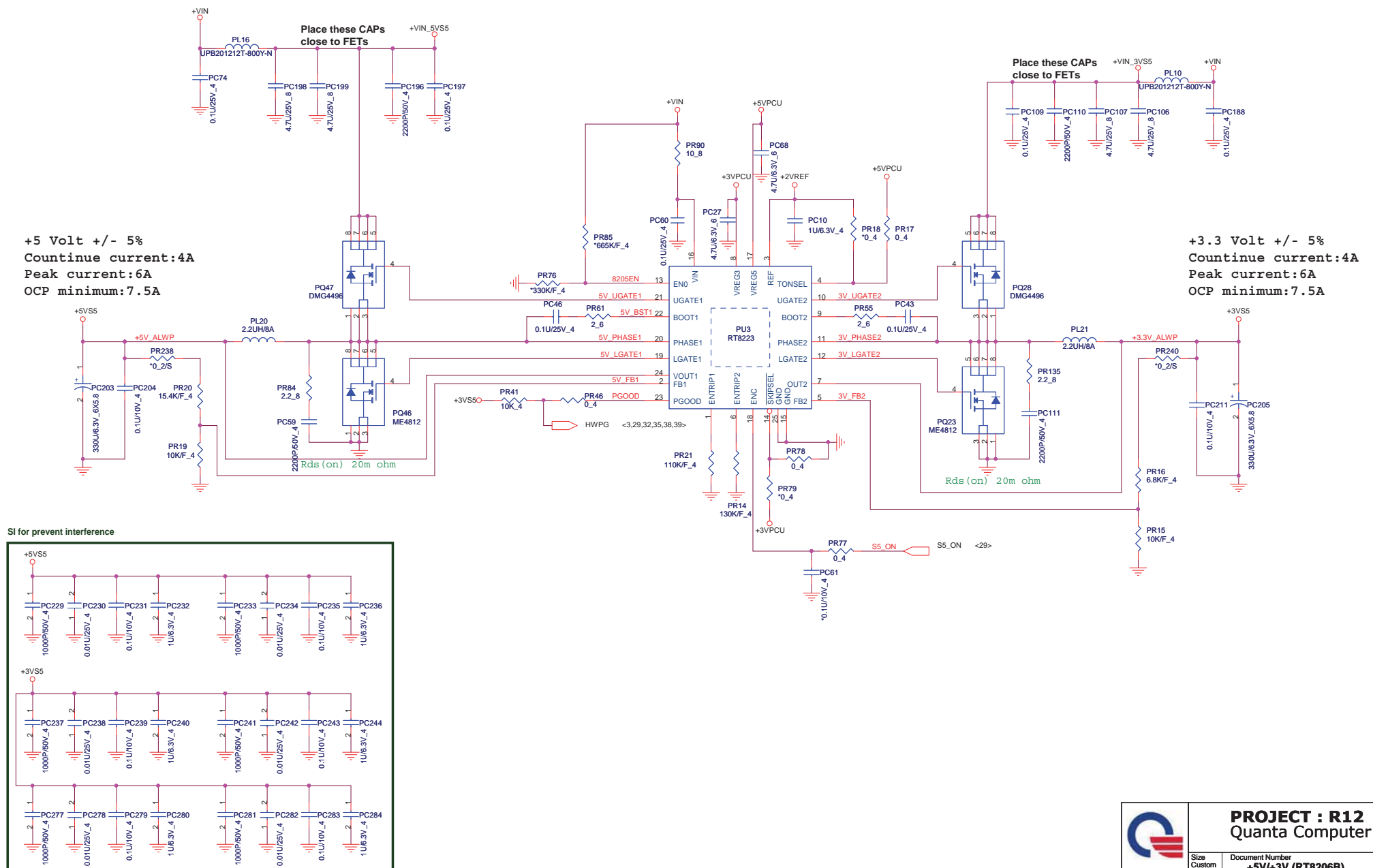


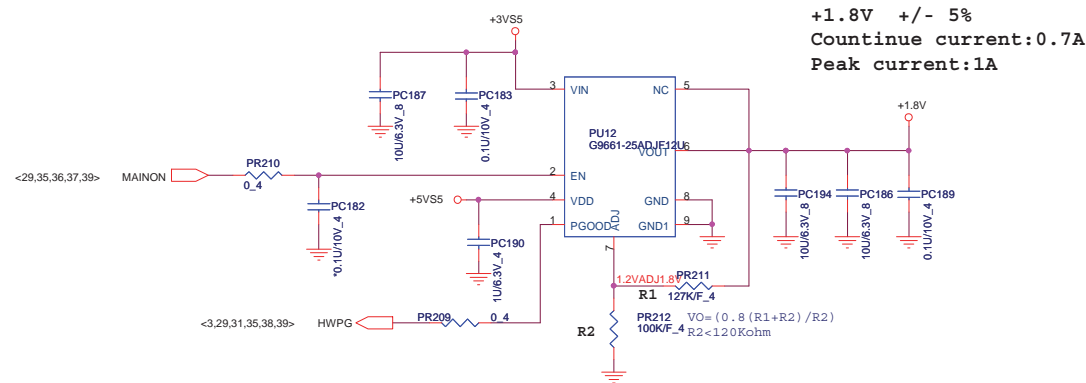
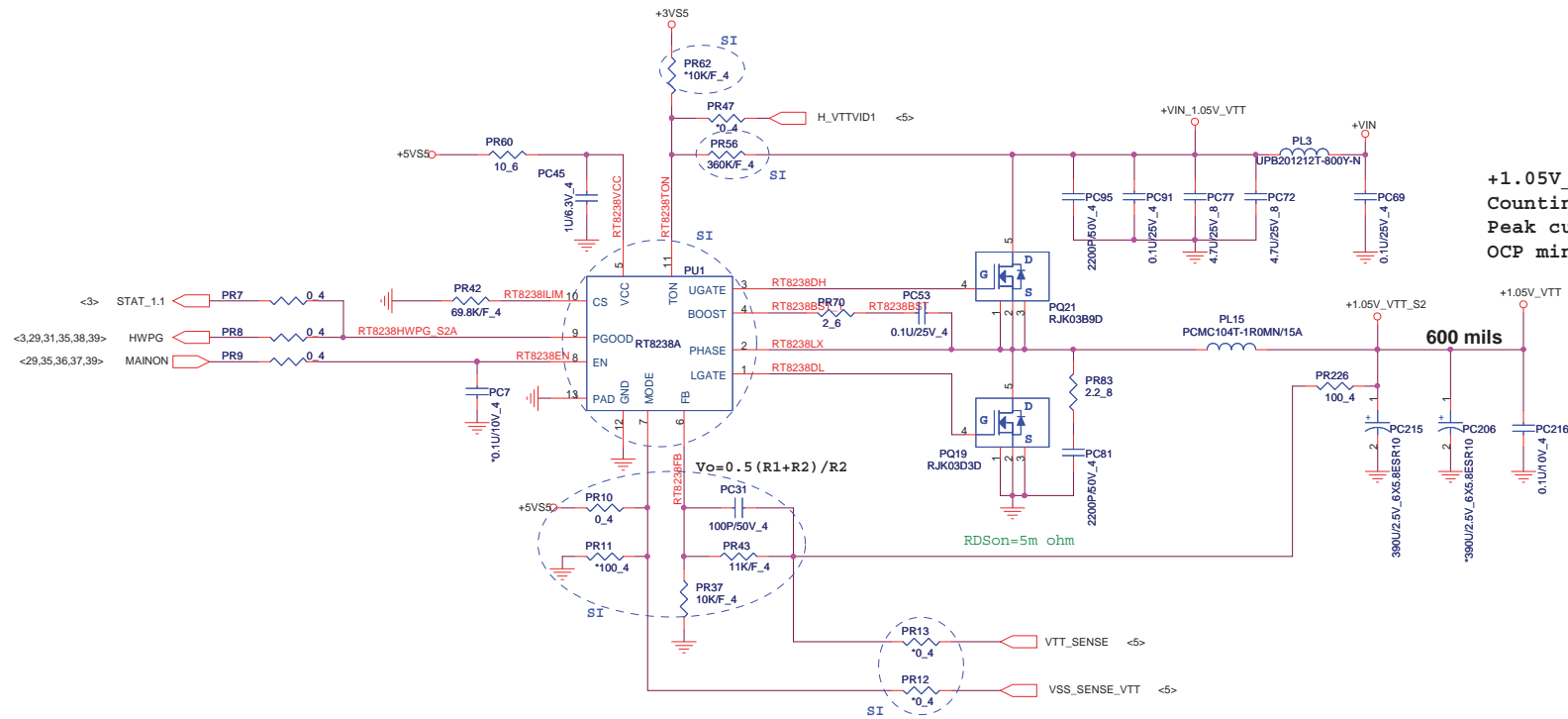
Mini PCI-E Card 1


WLAN

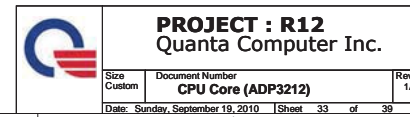
30





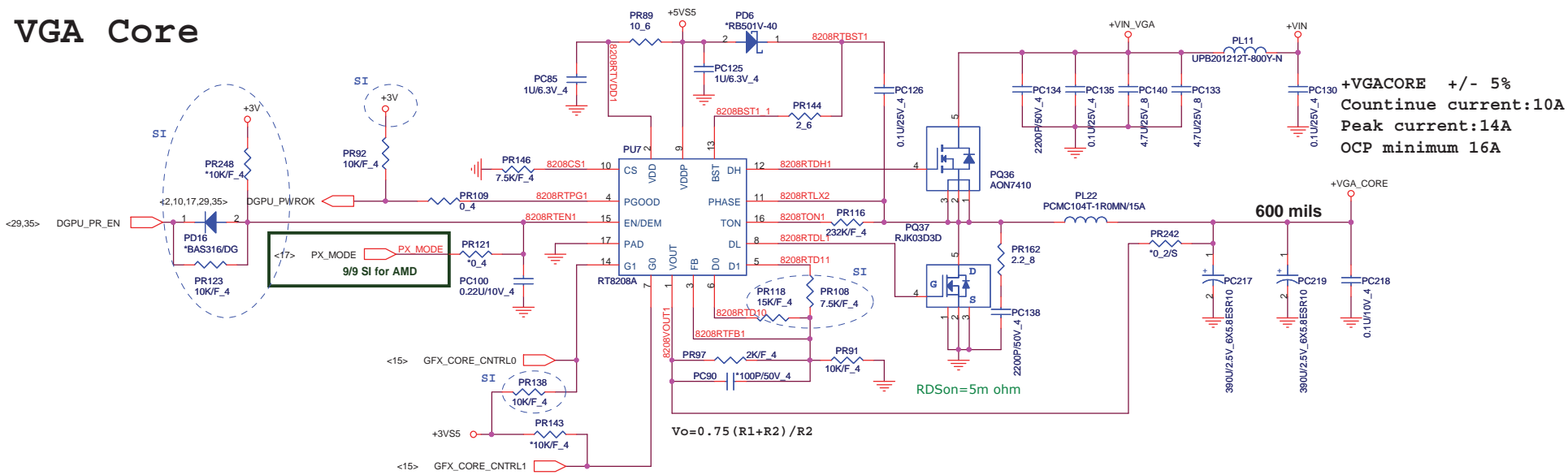


 PROJECT : R12 Quanta Computer Inc.		
Size Custom	Document Number +1.1V VTT / PCH	Rev 1A
Date: Sunday, September 19, 2010	Sheet 32	of 39

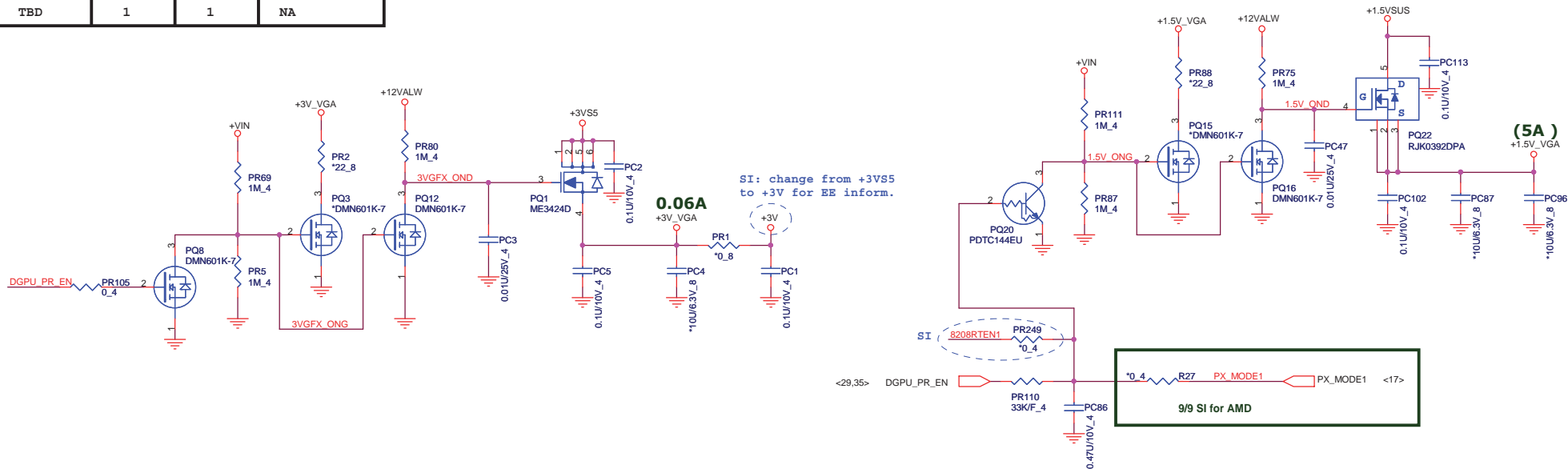


VGA Core

34

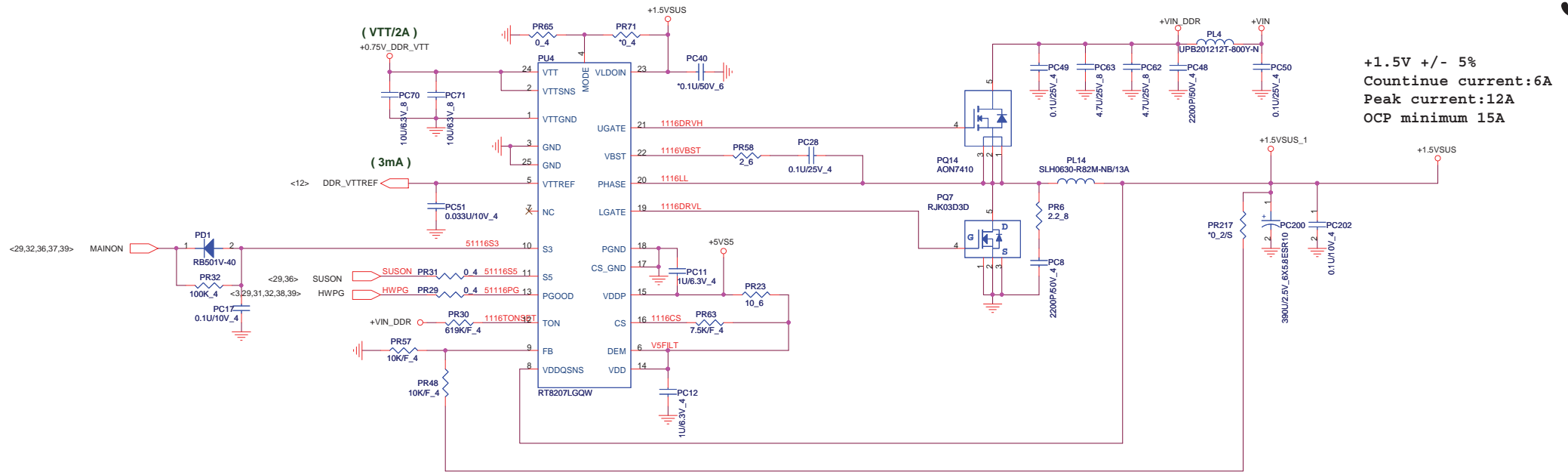


Seymour-XT	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA

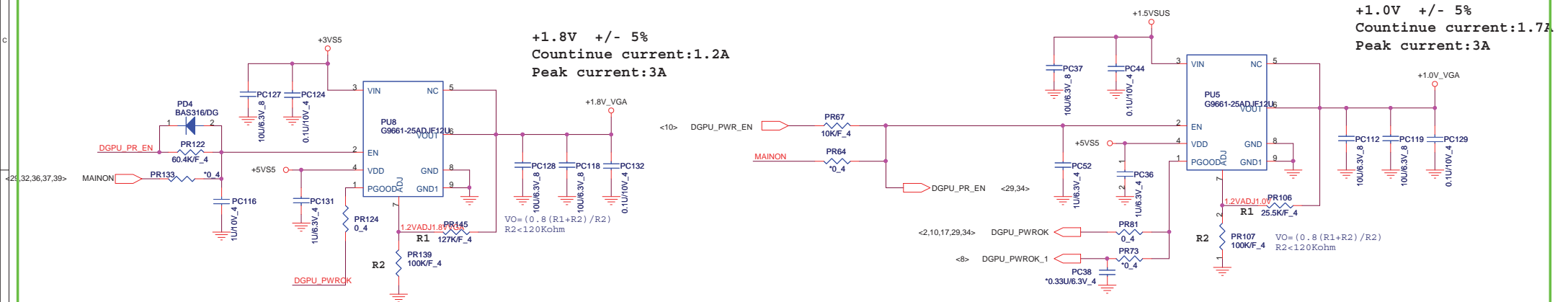


PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number +VGACORE (RT8208/1.8V)	Rev 1A
Date: Saturday, September 18, 2010	Sheet 34	of 39

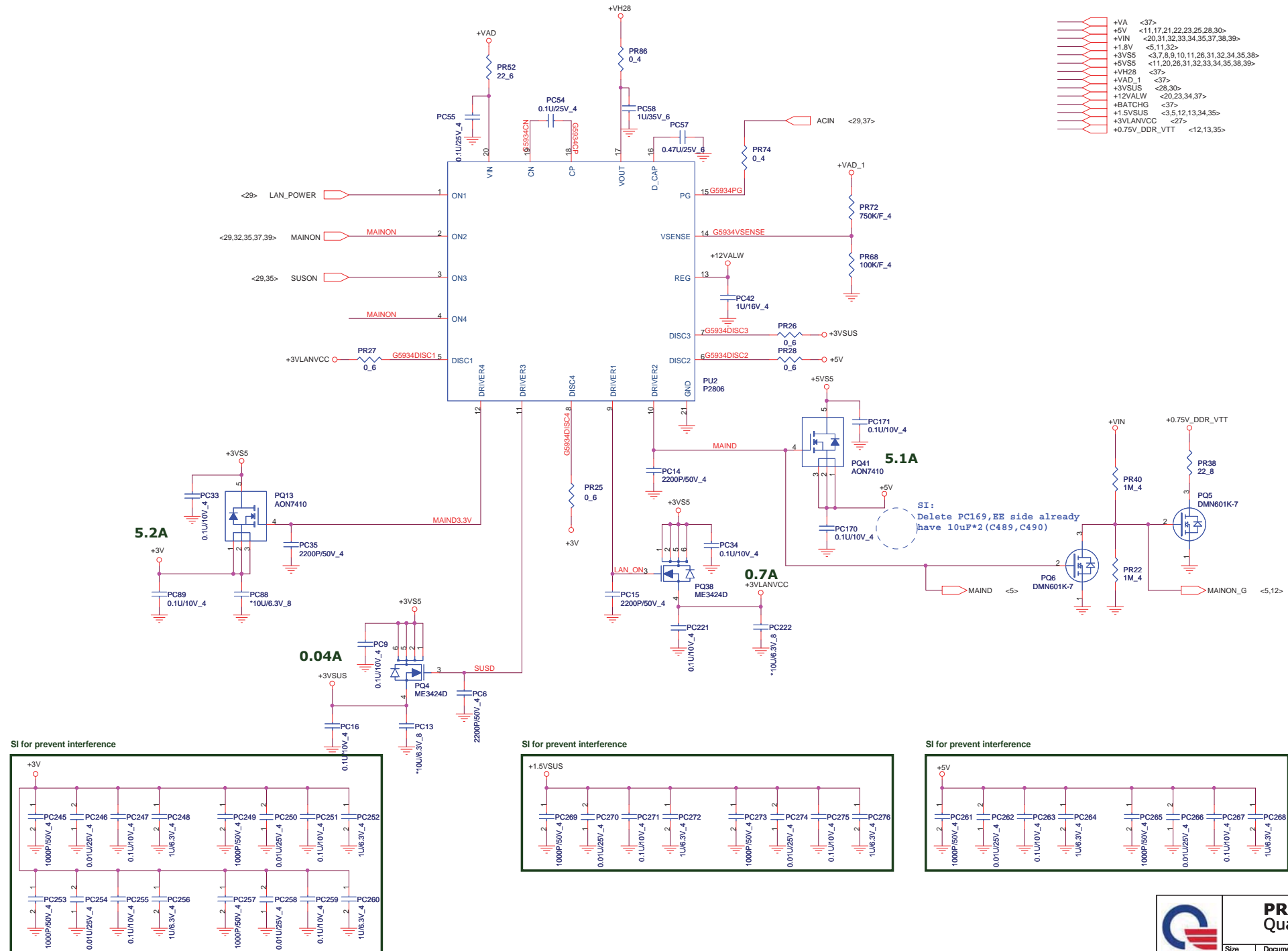


SG & Discrete Only



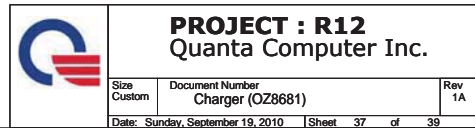
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A
Date: Sunday, September 19, 2010	Sheet 35 of 39	

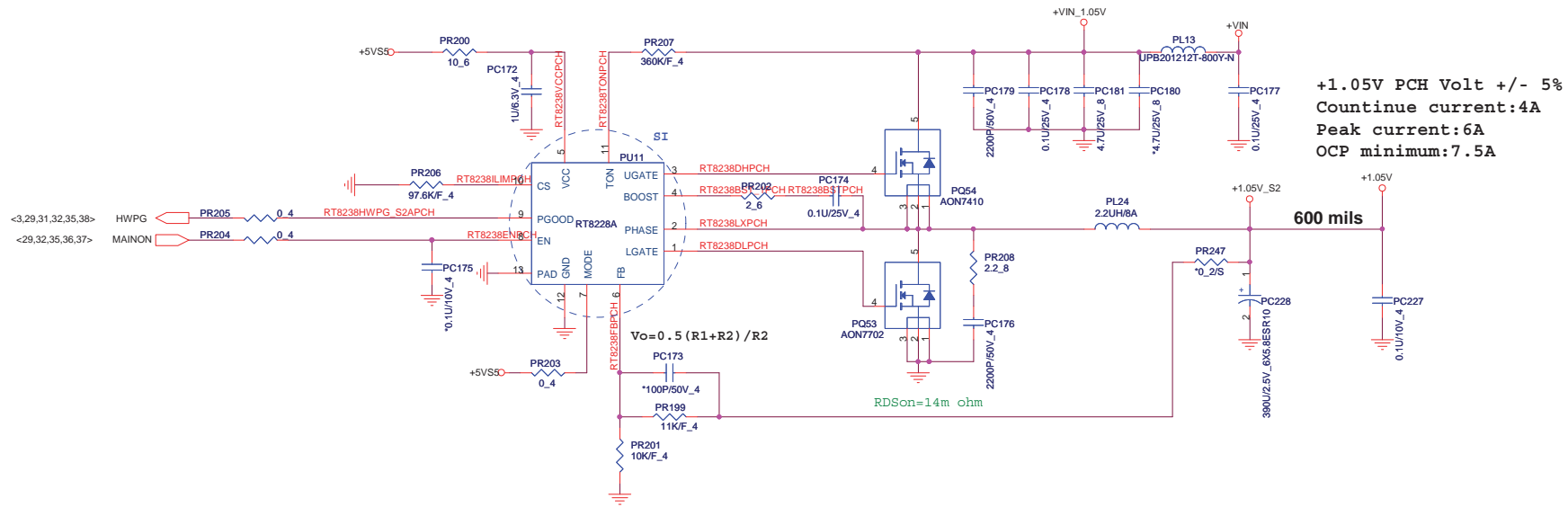



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	1A
Date: Sunday, September 19, 2010	Sheet 36 of 39	







 PROJECT : R12 Quanta Computer Inc.		
Size Custom	Document Number +1.05V (RT8238A)	Rev 1A
Date: Sunday, September 19, 2010 Sheet 39 of 39		