GA-M61VME-S2

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02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
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05	PROCESSOR DDR2 INTERFACE
06	PROCESSOR CONTROL & DEBUG
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12	MCP61-PCIe
13	MCP61-DAC, RGMII
14	MCP61-PCI
15	MCP61-SATA, IDE
16	MCP61-USB, HD-Audio, GPIO
17	MCP61-Power, Gnd
18	PCI EXPRESS x16, x1 SLOT
19	PCI 1,2,SLOT
20	ITE 8716GB/CX
21	Realtek 8201 CL
22	H/W MONITOR & FAN CONTROL
23	IDE/FDD/COM/LPT
24	F_USB/ R_USB
25	ALC883 HD-AUDIO

SHEET	TITLE
26	AUDIO JACK, L_OUT, F_AUDIO
27	FRONT PANEL POWER SEQUENCE
28	ATX POWER, BIOS, VCC12_DUAL, VDDA25
29	PWM ISL6566

Revision: 1.01

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Title: BLOCK DIAGRAM

Size: Custom | Document Number: GA-M61VME-S2 | Rev: 1.01

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Model Name:GA-M61VME-S2 1.01

Component value change history

P-Code: A95085-1

Date	Change Item	Reason
2006.06.02	0.1 E_BOM issue PCB:0.1	
2006.07.03	0.2 E_BOM issue PCB:0.2	Add IDERST level shift for nVidia comment Power ok level shift PCI_E right push
2006.??.??	1.0A D_BOM issue PCB:1.0	LFRAME, ACZ_SDOUT change to VCC3 pull up CLKOUT_25MHZ pull to GND by 4.7U

Circuit or PCB layout change for next version

Date	Change Item	Reason
2006.07.03	0.2 Gerber Out	Modify from M61SME-S2 0.1
2006.08.07	1.0 Gerber Out	SPI change to ITE.

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Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: GA-M61VME-S2 | Rev: 1.01

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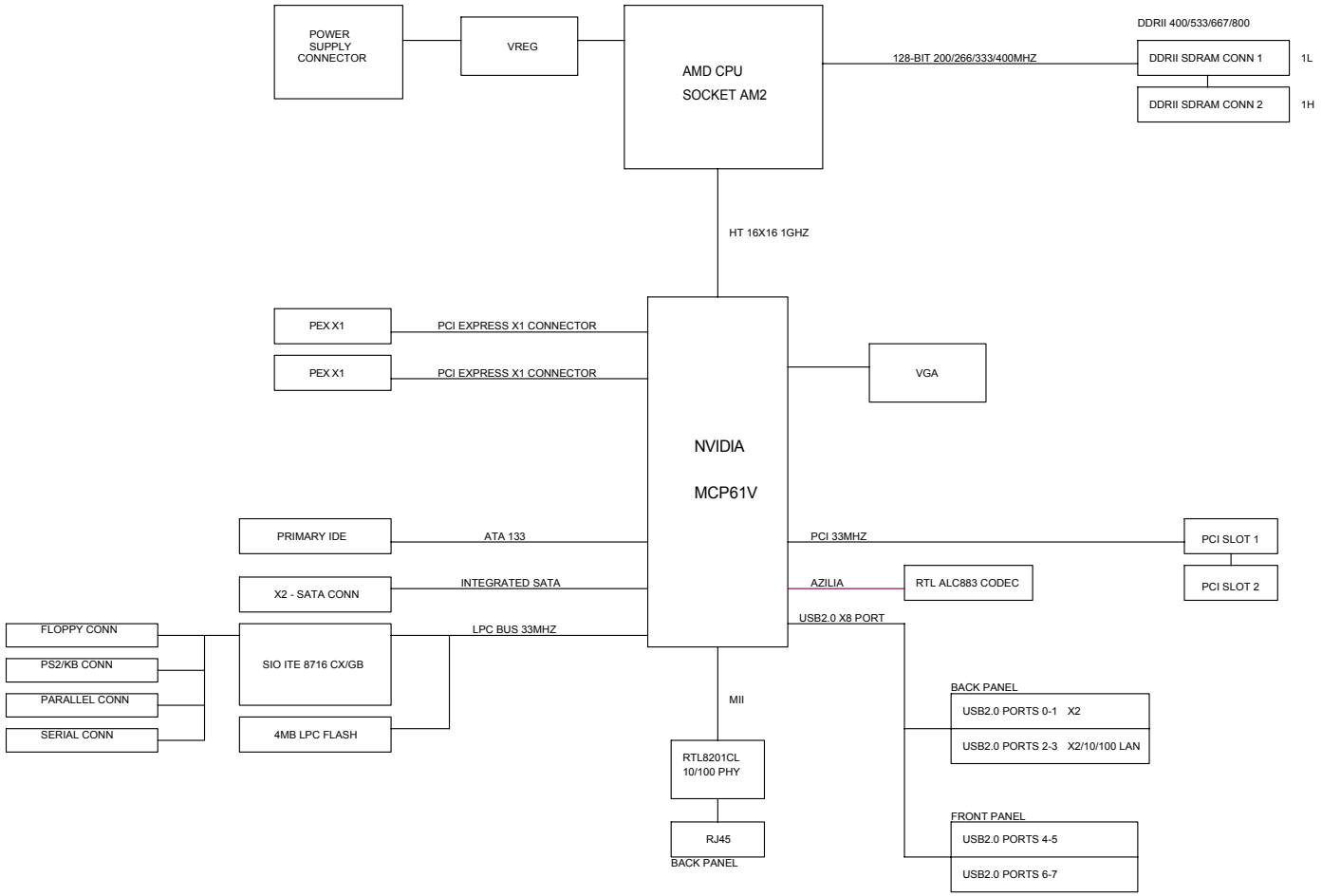
BLOCK DIAGRAM



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Title: BLOCK DIAGRAM

Size	Document Number	Rev
Custom	GA-M61VME-S2	1.01

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L0_CADIN_L[0..15] L0_CADIN_L[0..15] <11>
L0_CADIN_H[0..15] L0_CADIN_H[0..15] <11>
L0_CLKIN_L[0..1] L0_CLKIN_L[0..1] <11>
L0_CLKIN_H[0..1] L0_CLKIN_H[0..1] <11>
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] <11>
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] <11>
L0_CLKOUT_L[0..1] L0_CLKOUT_L[0..1] <11>
L0_CLKOUT_H[0..1] L0_CLKOUT_H[0..1] <11>

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

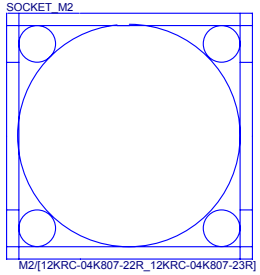
VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

HYPERTRANSPORT

L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1		
L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1		
L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0		
L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0		
VCC12_HT R3 49.9/4/1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	1	TP78	
GND R4 49.9/4/1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	1	TP79	
<11> L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	<11> L0_CTLOUT_H0	
<11> L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	<11> L0_CTLOUT_L0	
L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15		
L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15		
L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14		
L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14		
L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13		
L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13		
L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12		
L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12		
L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11		
L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11		
L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10		
L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10		
L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9		
L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9		
L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8		
L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8		
L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7		
L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7		
L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6		
L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6		
L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5		
L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5		
L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4		
L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4		
L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3		
L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3		
L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2		
L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2		
L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1		
L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1		
L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0		
L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0		

SOCKET_M2



M2/[12KRC-04K807-22R_12KRC-04K807-23R]

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Title	CPU HYPER TRANSPORT	
Size: Custom	Document Number: GA-M61VME-S2	Rev: 1.01
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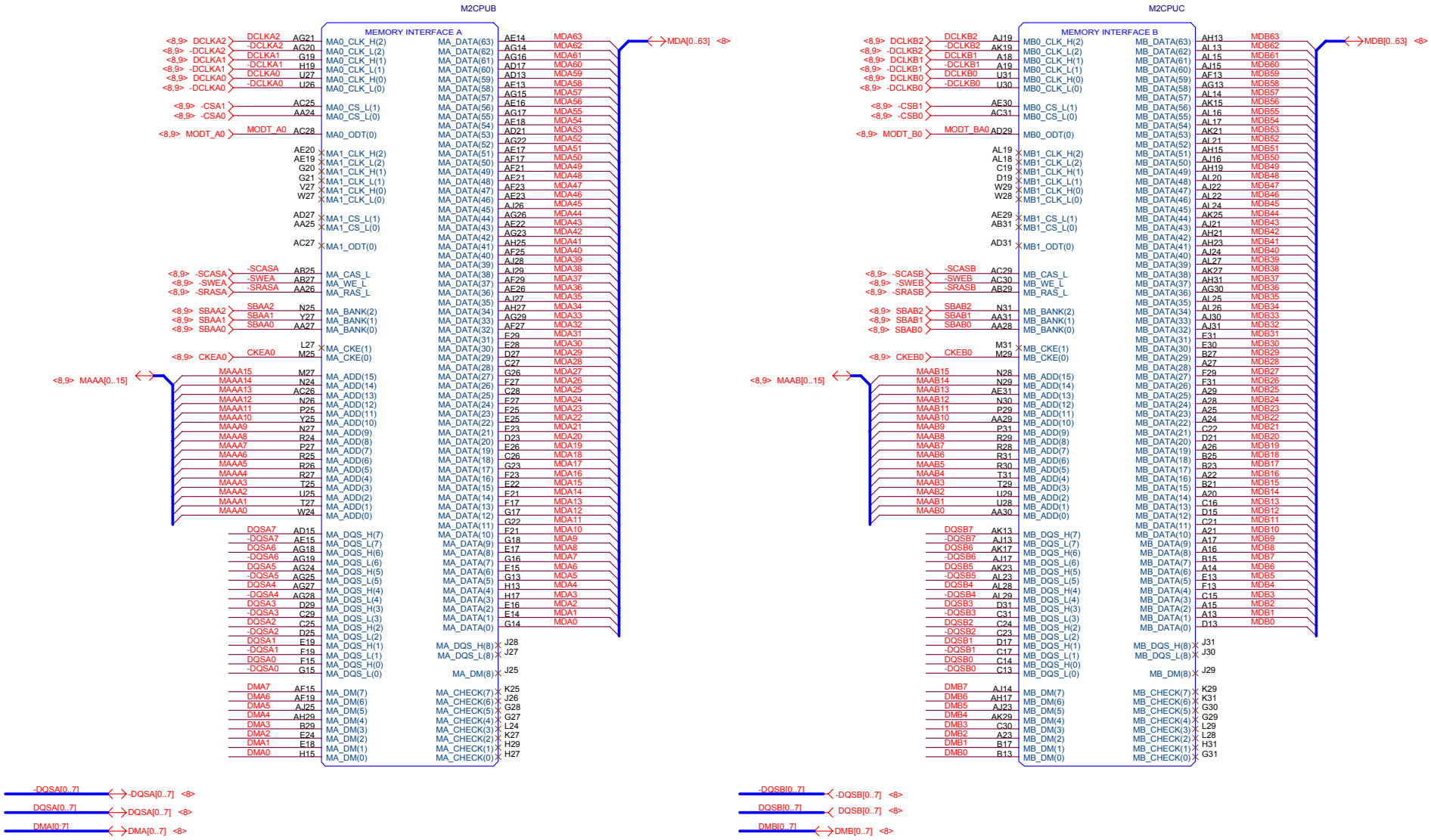

Title			
GIGABYTE	CPU DDRII MEMORY		
Size: Custom	Document Number: GA-M61VME-S2		Rev: 1.01
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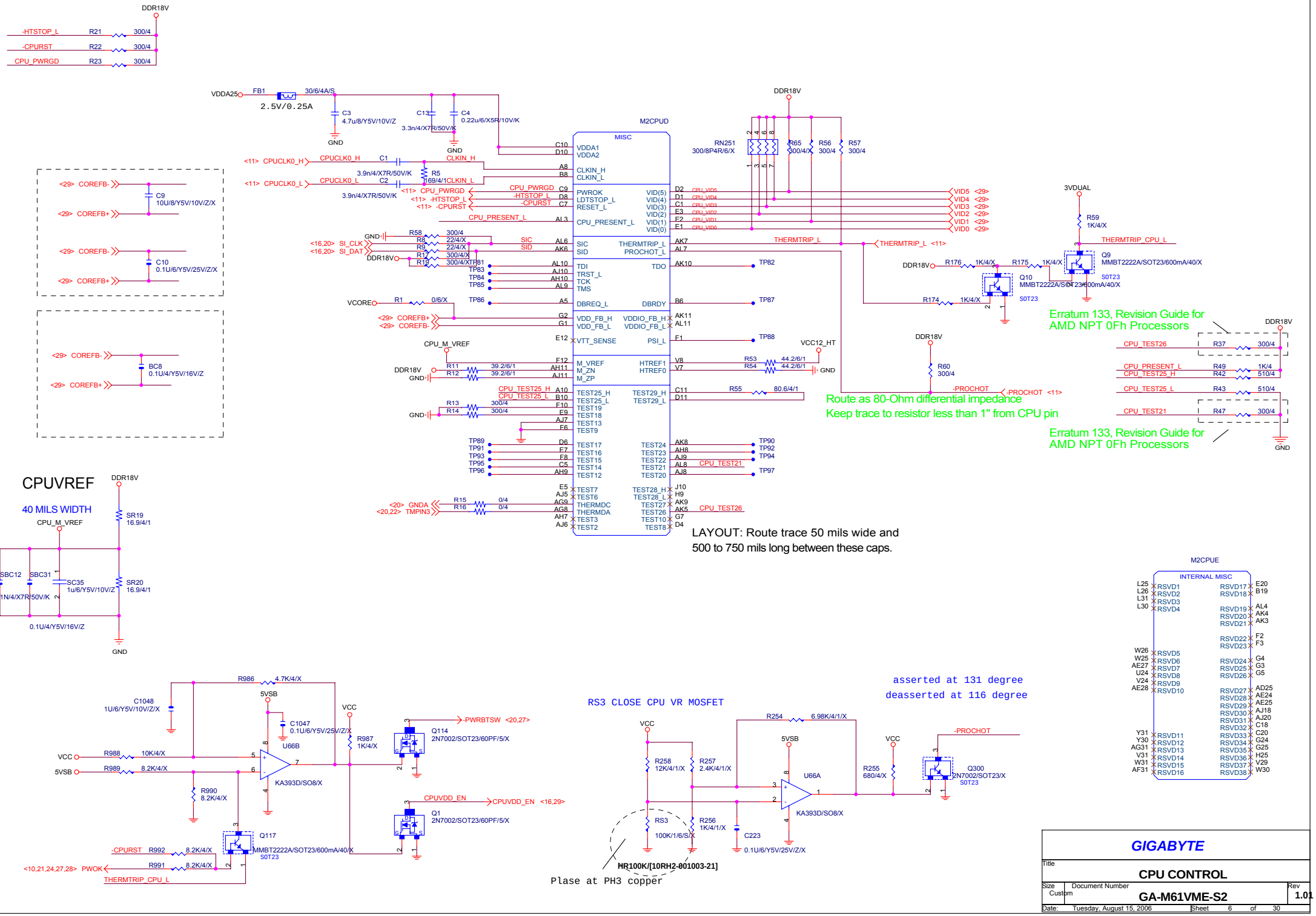
DDR18V
-HTSTOP_L R21 300/4
-CPURST R22 300/4
CPU_PWRGD R23 300/4
VDDA25
FB1 30/6/4A/S
2.5V/0.25A
C3 4.7u/8/Y5V/10V/Z
C13 3.3n/4/X7R/50V/K
C4 0.22u/6/X5R/10V/K
GND
M2CPUD
MISC
VDDA1
VDDA2
CLKIN_H
CLKIN_L
PWROK
LDTSTOP_L
RESET_L
CPU_PRESENT_L
SIC
SID
TDI
TRST_L
TCK
TMS
DBREQ_L
DBRDY
VDD_FB_H
VDD_FB_L
VTT_SENSE
VDDIO_FB_H
VDDIO_FB_L
PSI_L
M_VREF
M_ZN
M_ZP
HTREF1
HTREF0
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST17
TEST16
TEST15
TEST14
TEST12
TEST29_H
TEST29_L
TEST24
TEST23
TEST22
TEST21
TEST20
TEST7
TEST6
THERMDC
THERMDA
TEST3
TEST2
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
THERMTRIP_L
PROCHOT_L
TDO
DBRDY
VID(5)
VID(4)
VID(3)
VID(2)
VID(1)
VID(0)
RN251 300/8P4R/6/X
R65 300/4/X
R56 300/4
R57 300/4
THERMTRIP_L <11>
3VDUAL
R59 1K/4/X
THERMTRIP_CPU_L
Q9 MMBT2222A/SOT23/600mA/40/X
Q10 MMBT2222A/SOT23/600mA/40/X
S0T23
R176 1K/4/X
R175 1K/4/X
R174 1K/4/X
Erratum 133, Revision Guide for AMD NPT 0Fh Processors
CPU_TEST26 R37 300/4
CPU_PRESENT_L R49 1K/4
CPU_TEST25_H R42 510/4
CPU_TEST25_L R43 510/4
CPU_TEST21 R47 300/4
R58 300/4
R8 22/4/X
R9 22/4/X
R1 300/4/X
R12 300/4/X
TP81
TP83
TP84
TP85
TP86
TP82
TP87
TP88
TP89
TP91
TP93
TP95
TP96
TP90
TP92
TP94
TP97
VCORE
R1 0/6/X
CPU_M_VREF
R11 39.2/6/1
R12 39.2/6/1
R13 300/4
R14 300/4
R53 44.2/6/1
R54 44.2/6/1
VCC12_HT
R60 300/4
-PROCHOT
-PROCHOT <11>
R55 80.6/4/1
CPU_TEST25_H
CPU_TEST25_L
CPU_TEST21
CPU_TEST26
R15 0/4
R16 0/4
<20> GNDA
<20,22> TMPIN3
Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin
LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.
<29> COREFB-
<29> COREFB+
C9 10U/8/Y5V/10V/Z/X
C10 0.1U/6/Y5V/25V/Z/X
BC8 0.1U/4/Y5V/16V/Z
CPUVREF
40 MILS WIDTH
SR19 16.9/4/1
SR20 16.9/4/1
SBC12 1N/4/X7R/50V/K
SBC31
SC35 1u/6/Y5V/10V/Z
0.1U/4/Y5V/16V/Z
R986 4.7K/4/X
5VSB
C1048 1U/6/Y5V/10V/Z/X
C1047 0.1U/6/Y5V/25V/Z/X
U66B
KA393D/SO8/X
VCC
R988 10K/4/X
R989 8.2K/4/X
R990 8.2K/4/X
R987 1K/4/X
Q114 2N7002/SOT23/60PF/5/X
-PWRBTSW <20,27>
CPUVDD_EN
CPUVDD_EN <16,29>
Q1 2N7002/SOT23/60PF/5/X
Q117 MMBT2222A/SOT23/600mA/40/X
S0T23
-CPURST R992 8.2K/4/X
R991 8.2K/4/X
<10,21,24,27,28> PWOK
THERMTRIP_CPU_L
RS3 CLOSE CPU VR MOSFET
asserted at 131 degree
deasserted at 116 degree
R254 6.98K/4/1/X
R258 12K/4/1/X
R257 2.4K/4/1/X
R255 680/4/X
R256 1K/4/1/X
RS3 100K/1/6/S/X
C223 0.1U/6/Y5V/25V/Z/X
U66A
KA393D/SO8/X
Q300 2N7002/SOT23/X
S0T23
HR100K/[10RH2-001003-21]
Plase at PH3 copper
M2CPUE
INTERNAL MISC
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD15
RSVD16
RSVD17
RSVD18
RSVD19
RSVD20
RSVD21
RSVD22
RSVD23
RSVD24
RSVD25
RSVD26
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
RSVD32
RSVD33
RSVD34
RSVD35
RSVD36
RSVD37
RSVD38
GIGABYTE
Title
CPU CONTROL
Size Custom
Document Number GA-M61VME-S2
Rev 1.01
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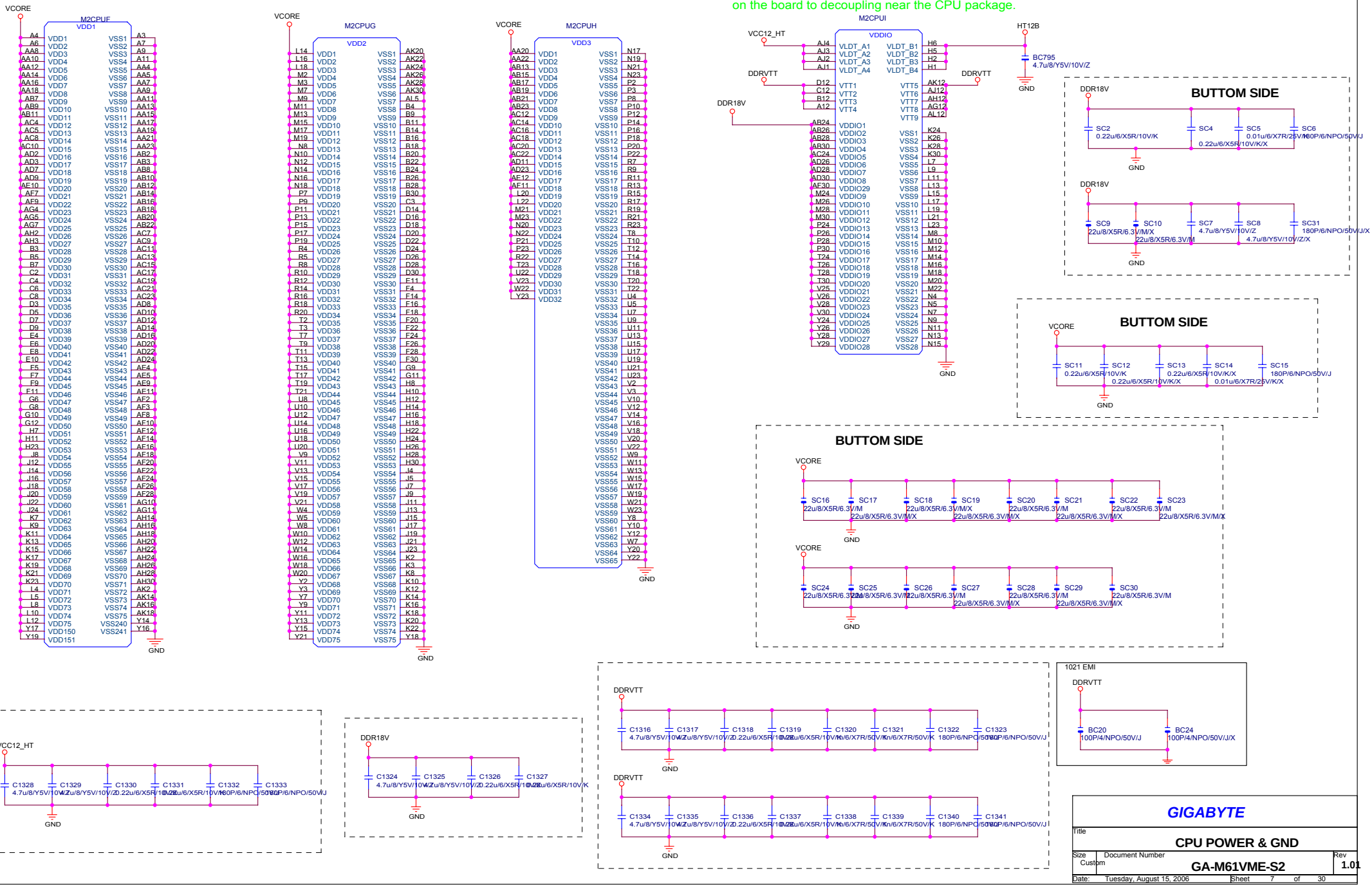
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



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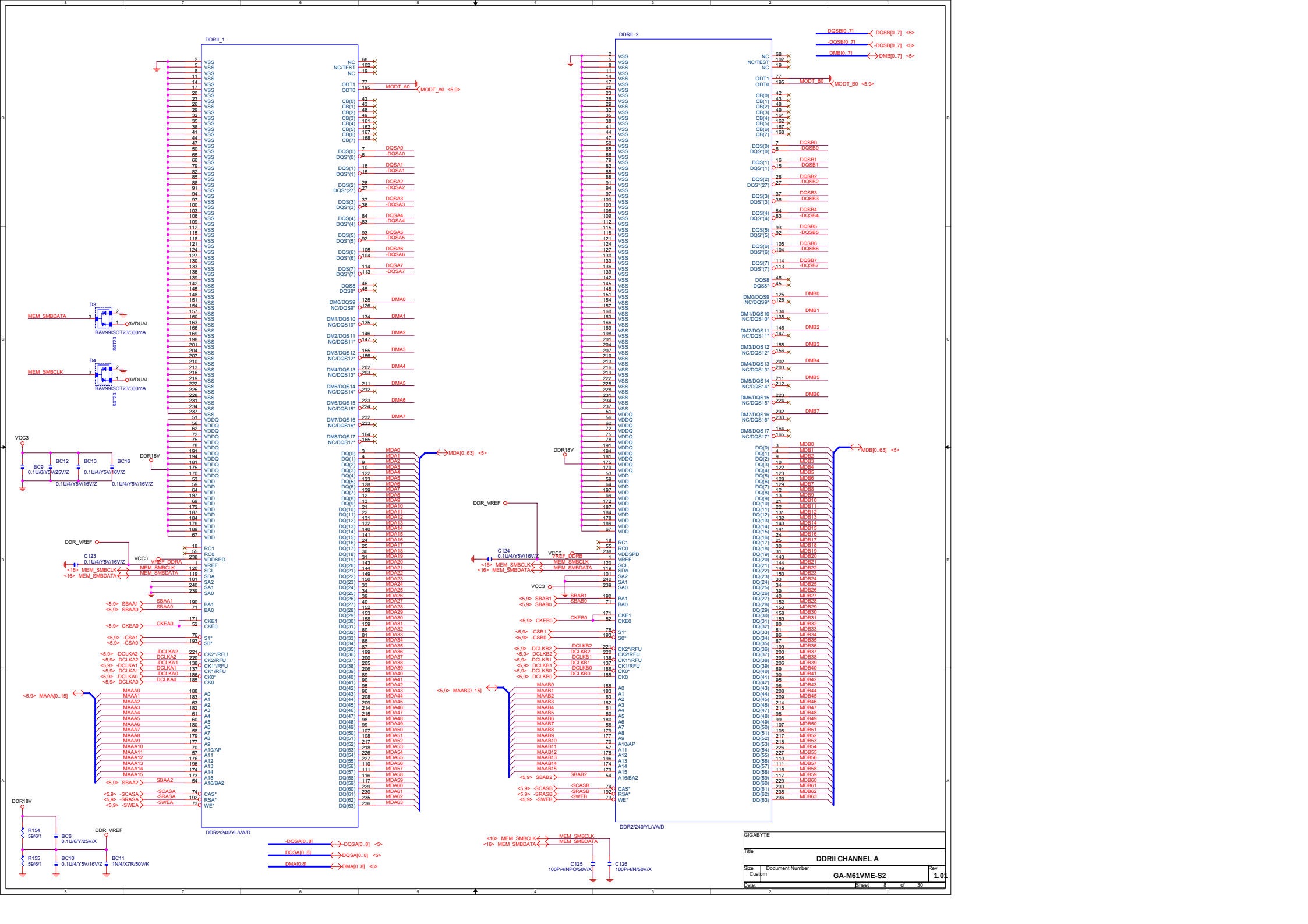
Title	CPU POWER & GND	
Size: Custom	Document Number: GA-M61VME-S2	Rev: 1.01
Date: Tuesday, August 15, 2006	Sheet 7 of 30	


DDRII_1
DDRII_2
DDR2/240/YL/VA/D
MEM_SMBDATA
MEM_SMBCLK
D3
D4
BAV99/SOT23/300mA
SOT23
3VDUAL
VCC3
DDR18V
DDR_VREF
BC9 0.1U/6/Y5V/25V/Z
BC12
BC13
BC16
0.1U/4/Y5V/16V/Z
C123 0.1U/4/Y5V/16V/Z
C124 0.1U/4/Y5V/16V/Z
C125 100P/4/NPO/50V/X
C126 100P/4/N/50V/X
R154 59/6/1
R155 59/6/1
BC6 0.1U/6/Y/25V/X
BC10 0.1U/4/Y5V/16V/Z
BC11 1N/4/X7R/50V/K
VREF_DDRA
VREF_DDRB
MEM_SMBCLK
MEM_SMBDATA
MODT_A0
MODT_B0
DQSB[0..7]
-DQSB[0..7]
DMB[0..7]
MDA[0..63]
MDB[0..63]
-DQSA[0..8]
DQSA[0..8]
DMA[0..8]
MAAA[0..15]
MAAB[0..15]
SBAA1
SBAA0
SBAB1
SBAB0
CKEA0
CKEB0
-CSA1
-CSA0
-CSB1
-CSB0
-DCLKA2
DCLKA2
-DCLKA1
DCLKA1
-DCLKA0
DCLKA0
-DCLKB2
DCLKB2
-DCLKB1
DCLKB1
-DCLKB0
DCLKB0
SBAA2
SBAB2
-SCASA
-SRASA
-SWEA
-SCASB
-SRASB
-SWEB
GIGABYTE
DDRII CHANNEL A
GA-M61VME-S2
1.01
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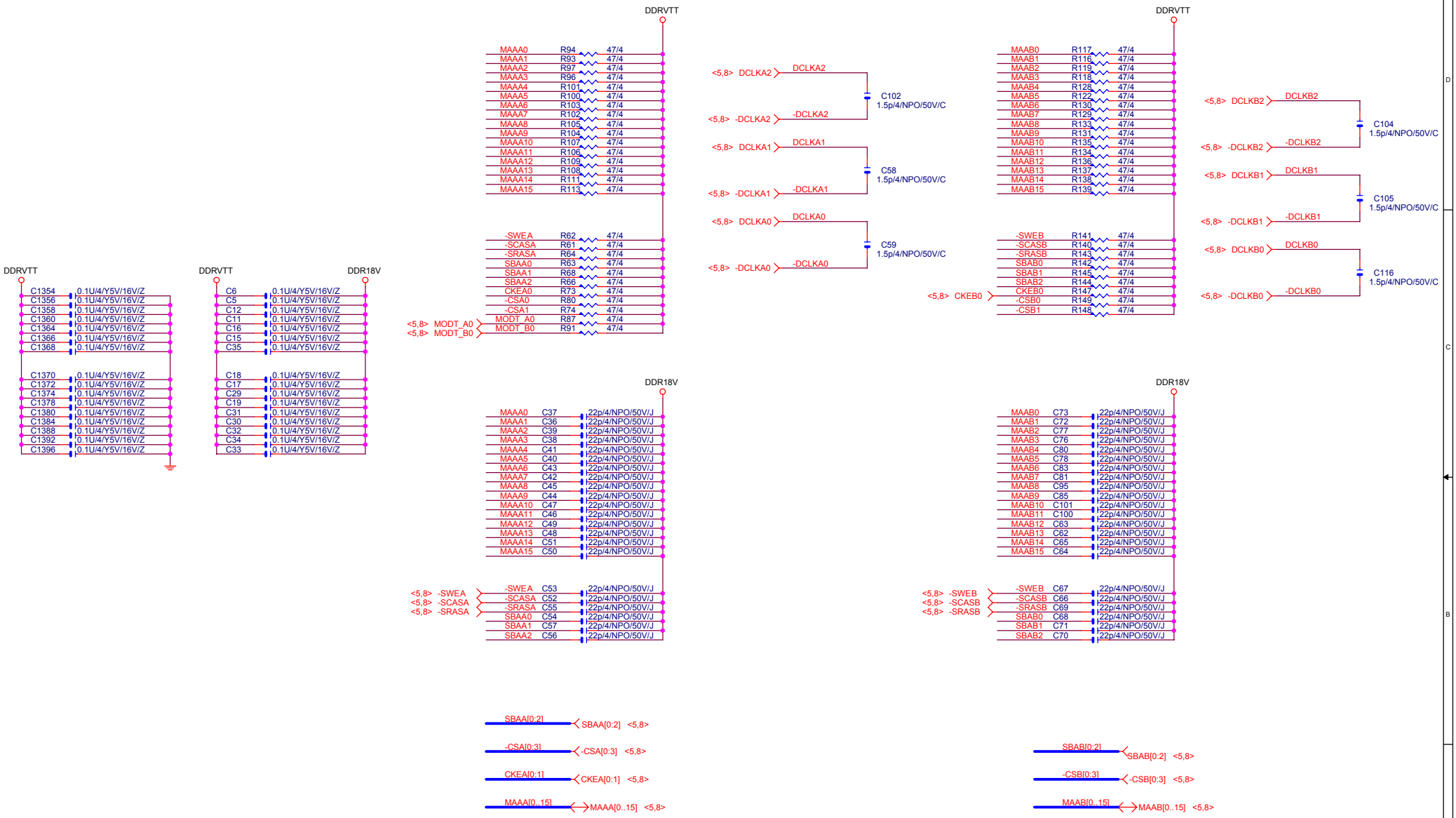
DDRVTT
C1354 0.1U/4/Y5V/16V/Z
C1356 0.1U/4/Y5V/16V/Z
C1358 0.1U/4/Y5V/16V/Z
C1360 0.1U/4/Y5V/16V/Z
C1364 0.1U/4/Y5V/16V/Z
C1366 0.1U/4/Y5V/16V/Z
C1368 0.1U/4/Y5V/16V/Z
C1370 0.1U/4/Y5V/16V/Z
C1372 0.1U/4/Y5V/16V/Z
C1374 0.1U/4/Y5V/16V/Z
C1378 0.1U/4/Y5V/16V/Z
C1380 0.1U/4/Y5V/16V/Z
C1384 0.1U/4/Y5V/16V/Z
C1388 0.1U/4/Y5V/16V/Z
C1392 0.1U/4/Y5V/16V/Z
C1396 0.1U/4/Y5V/16V/Z
DDRVTT
DDR18V
C6 0.1U/4/Y5V/16V/Z
C5 0.1U/4/Y5V/16V/Z
C12 0.1U/4/Y5V/16V/Z
C11 0.1U/4/Y5V/16V/Z
C16 0.1U/4/Y5V/16V/Z
C15 0.1U/4/Y5V/16V/Z
C35 0.1U/4/Y5V/16V/Z
C18 0.1U/4/Y5V/16V/Z
C17 0.1U/4/Y5V/16V/Z
C29 0.1U/4/Y5V/16V/Z
C19 0.1U/4/Y5V/16V/Z
C31 0.1U/4/Y5V/16V/Z
C30 0.1U/4/Y5V/16V/Z
C32 0.1U/4/Y5V/16V/Z
C34 0.1U/4/Y5V/16V/Z
C33 0.1U/4/Y5V/16V/Z
DDRVTT
MAAA0 R94 47/4
MAAA1 R93 47/4
MAAA2 R97 47/4
MAAA3 R96 47/4
MAAA4 R101 47/4
MAAA5 R100 47/4
MAAA6 R103 47/4
MAAA7 R102 47/4
MAAA8 R105 47/4
MAAA9 R104 47/4
MAAA10 R107 47/4
MAAA11 R106 47/4
MAAA12 R109 47/4
MAAA13 R108 47/4
MAAA14 R111 47/4
MAAA15 R113 47/4
-SWEA R62 47/4
-SCASA R61 47/4
-SRASA R64 47/4
SBAA0 R63 47/4
SBAA1 R68 47/4
SBAA2 R66 47/4
CKEA0 R73 47/4
-CSA0 R80 47/4
-CSA1 R74 47/4
MODT_A0 R87 47/4
MODT_B0 R91 47/4
<5,8> MODT_A0
<5,8> MODT_B0
<5,8> DCLKA2
DCLKA2
C102 1.5p/4/NPO/50V/C
<5,8> -DCLKA2
-DCLKA2
<5,8> DCLKA1
DCLKA1
C58 1.5p/4/NPO/50V/C
<5,8> -DCLKA1
-DCLKA1
<5,8> DCLKA0
DCLKA0
C59 1.5p/4/NPO/50V/C
<5,8> -DCLKA0
-DCLKA0
DDR18V
MAAA0 C37 22p/4/NPO/50V/J
MAAA1 C36 22p/4/NPO/50V/J
MAAA2 C39 22p/4/NPO/50V/J
MAAA3 C38 22p/4/NPO/50V/J
MAAA4 C41 22p/4/NPO/50V/J
MAAA5 C40 22p/4/NPO/50V/J
MAAA6 C43 22p/4/NPO/50V/J
MAAA7 C42 22p/4/NPO/50V/J
MAAA8 C45 22p/4/NPO/50V/J
MAAA9 C44 22p/4/NPO/50V/J
MAAA10 C47 22p/4/NPO/50V/J
MAAA11 C46 22p/4/NPO/50V/J
MAAA12 C49 22p/4/NPO/50V/J
MAAA13 C48 22p/4/NPO/50V/J
MAAA14 C51 22p/4/NPO/50V/J
MAAA15 C50 22p/4/NPO/50V/J
-SWEA C53 22p/4/NPO/50V/J
-SCASA C52 22p/4/NPO/50V/J
-SRASA C55 22p/4/NPO/50V/J
SBAA0 C54 22p/4/NPO/50V/J
SBAA1 C57 22p/4/NPO/50V/J
SBAA2 C56 22p/4/NPO/50V/J
<5,8> -SWEA
<5,8> -SCASA
<5,8> -SRASA
SBAA[0:2]
SBAA[0:2] <5,8>
-CSA[0:3]
-CSA[0:3] <5,8>
CKEA[0:1]
CKEA[0:1] <5,8>
MAAA[0..15]
MAAA[0..15] <5,8>
DDRVTT
MAAB0 R117 47/4
MAAB1 R116 47/4
MAAB2 R119 47/4
MAAB3 R118 47/4
MAAB4 R128 47/4
MAAB5 R122 47/4
MAAB6 R130 47/4
MAAB7 R129 47/4
MAAB8 R133 47/4
MAAB9 R131 47/4
MAAB10 R135 47/4
MAAB11 R134 47/4
MAAB12 R136 47/4
MAAB13 R137 47/4
MAAB14 R138 47/4
MAAB15 R139 47/4
-SWEB R141 47/4
-SCASB R140 47/4
-SRASB R143 47/4
SBAB0 R142 47/4
SBAB1 R145 47/4
SBAB2 R144 47/4
CKEB0 R147 47/4
-CSB0 R149 47/4
-CSB1 R148 47/4
<5,8> CKEB0
<5,8> DCLKB2
DCLKB2
C104 1.5p/4/NPO/50V/C
<5,8> -DCLKB2
-DCLKB2
<5,8> DCLKB1
DCLKB1
C105 1.5p/4/NPO/50V/C
<5,8> -DCLKB1
-DCLKB1
<5,8> DCLKB0
DCLKB0
C116 1.5p/4/NPO/50V/C
<5,8> -DCLKB0
-DCLKB0
DDR18V
MAAB0 C73 22p/4/NPO/50V/J
MAAB1 C72 22p/4/NPO/50V/J
MAAB2 C77 22p/4/NPO/50V/J
MAAB3 C76 22p/4/NPO/50V/J
MAAB4 C80 22p/4/NPO/50V/J
MAAB5 C78 22p/4/NPO/50V/J
MAAB6 C83 22p/4/NPO/50V/J
MAAB7 C81 22p/4/NPO/50V/J
MAAB8 C95 22p/4/NPO/50V/J
MAAB9 C85 22p/4/NPO/50V/J
MAAB10 C101 22p/4/NPO/50V/J
MAAB11 C100 22p/4/NPO/50V/J
MAAB12 C63 22p/4/NPO/50V/J
MAAB13 C62 22p/4/NPO/50V/J
MAAB14 C65 22p/4/NPO/50V/J
MAAB15 C64 22p/4/NPO/50V/J
-SWEB C67 22p/4/NPO/50V/J
-SCASB C66 22p/4/NPO/50V/J
-SRASB C69 22p/4/NPO/50V/J
SBAB0 C68 22p/4/NPO/50V/J
SBAB1 C71 22p/4/NPO/50V/J
SBAB2 C70 22p/4/NPO/50V/J
<5,8> -SWEB
<5,8> -SCASB
<5,8> -SRASB
SBAB[0:2]
SBAB[0:2] <5,8>
-CSB[0:3]
-CSB[0:3] <5,8>
MAAB[0..15]
MAAB[0..15] <5,8>
GIGABYTE
Title
DDRII TERMINATOR
Size B
Document Number
GA-M61VME-S2
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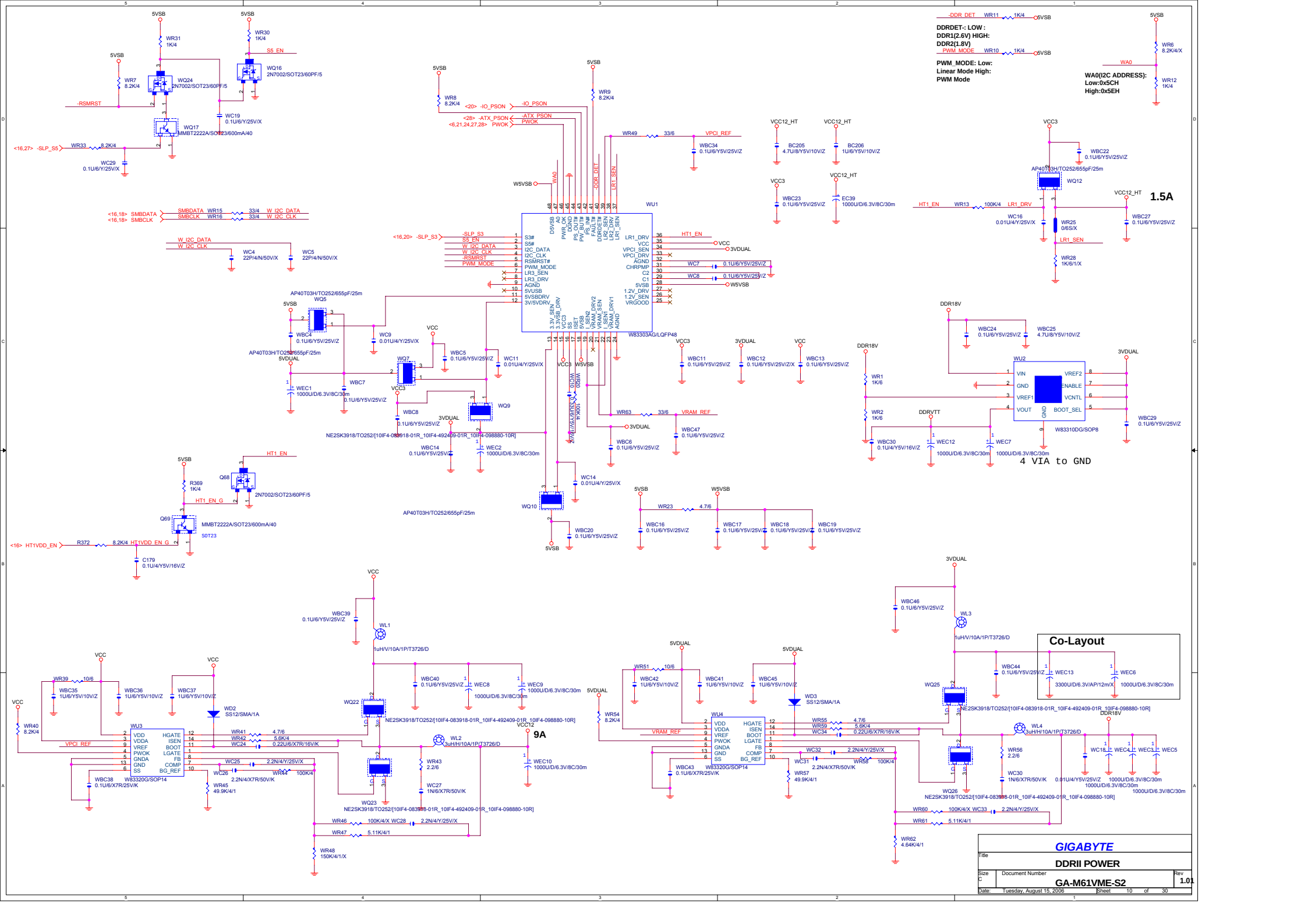
DDRDET-: LOW :
DDR1(2.6V) HIGH:
DDR2(1.8V)
PWM_MODE: Low:
Linear Mode High:
PWM Mode
WA0(I2C ADDRESS):
Low:0x5CH
High:0x5EH
1.5A
9A
4 VIA to GND
Co-Layout
W83303AG/LQFP48
W83310DG/SOP8
W83320G/SOP14
NE2SK3918/TO252/[10IF4-083918-01R_10IF4-492409-01R_10IF4-098880-10R]
AP40T03H/TO252/655pF/25m
MMBT2222A/SOT23/600mA/40
2N7002/SOT23/60PF/5
SS12/SMA/1A
GIGABYTE
DDRII POWER
GA-M61VME-S2
1.01
Tuesday, August 15, 2006
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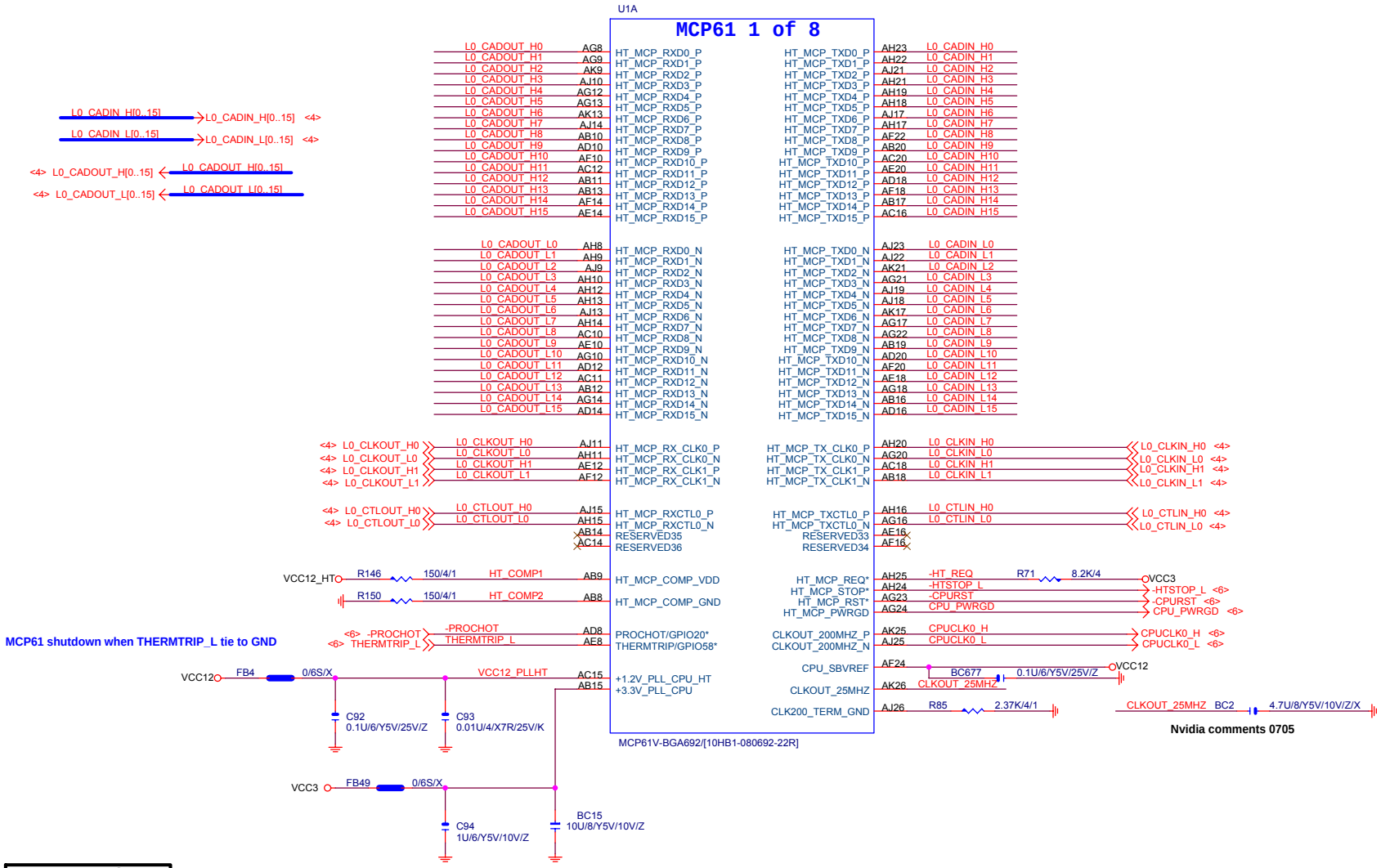

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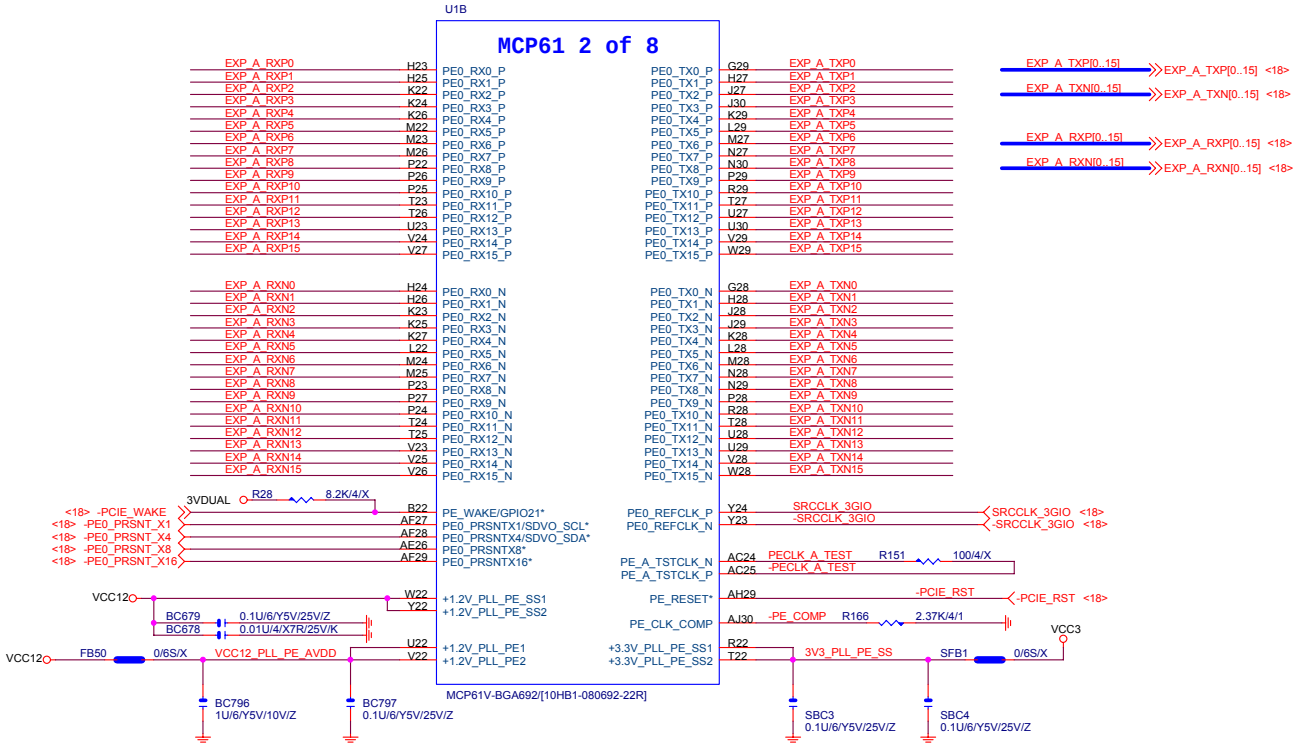
Size	Custom
Document Number	GA-M61VME-S2
Rev	1.01
Date:	Tuesday, August 15, 2006
Sheet	11 of 30

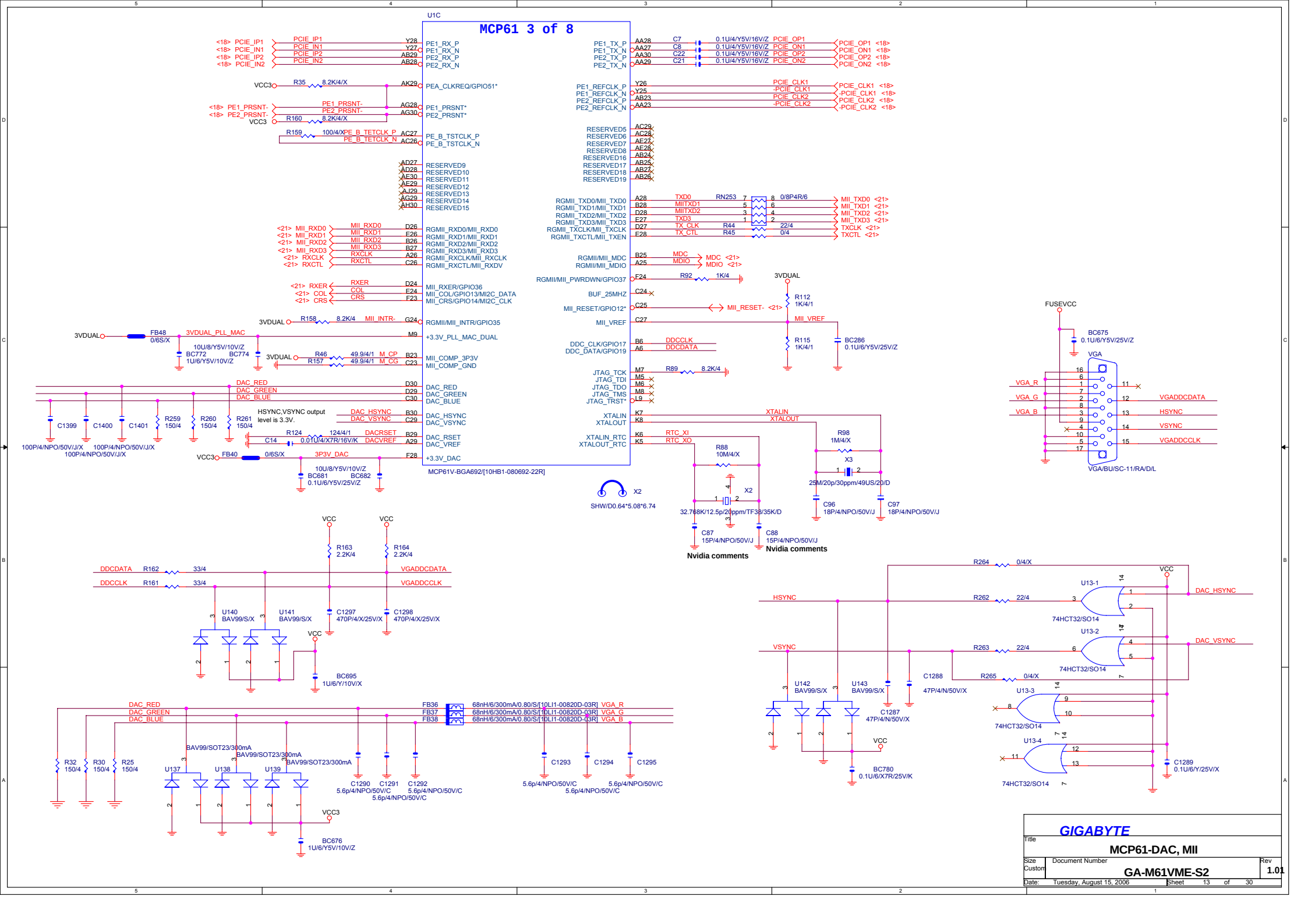


GIGABYTE

Title: MCP61-PCI EXPRESS

Size: Custom | Document Number: GA-M61VME-S2 | Rev: 1.01

Date: Tuesday, August 15, 2006 | Sheet 12 of 30



Title	MCP61-DAC, MII
Size	Custom
Document Number	GA-M61VME-S2
Rev	1.01
Date:	Tuesday, August 15, 2006
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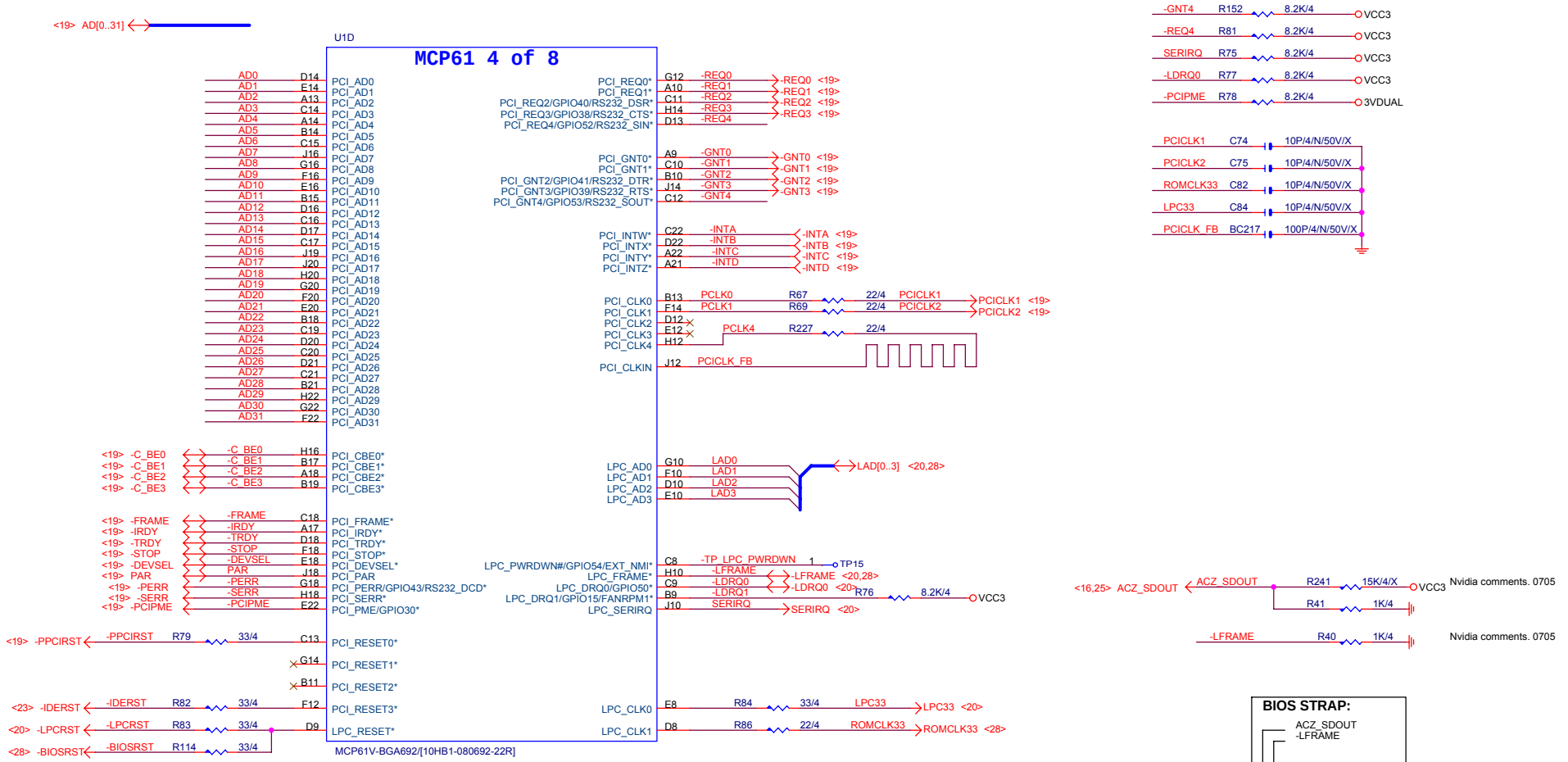

GIGABYTE

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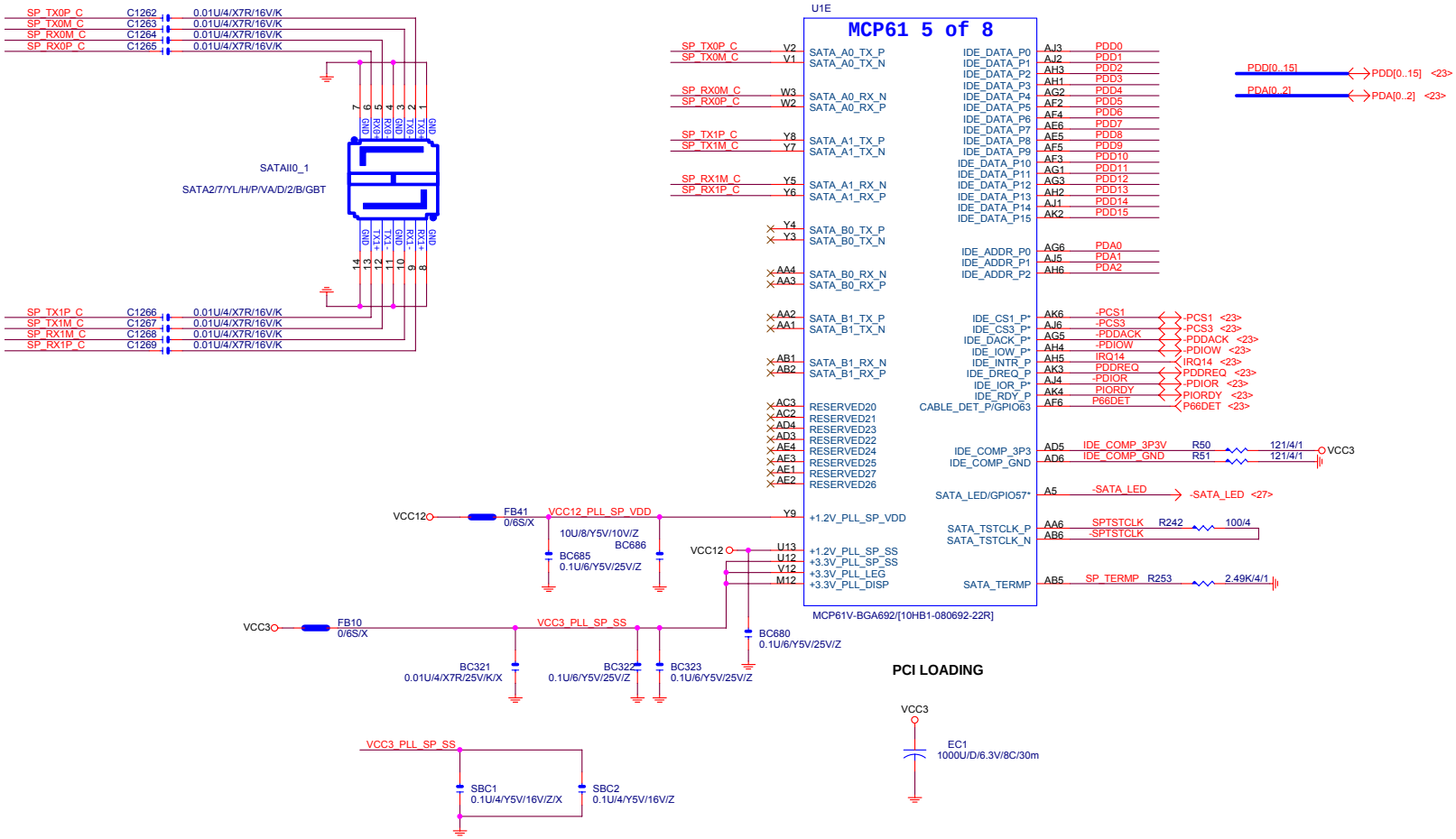
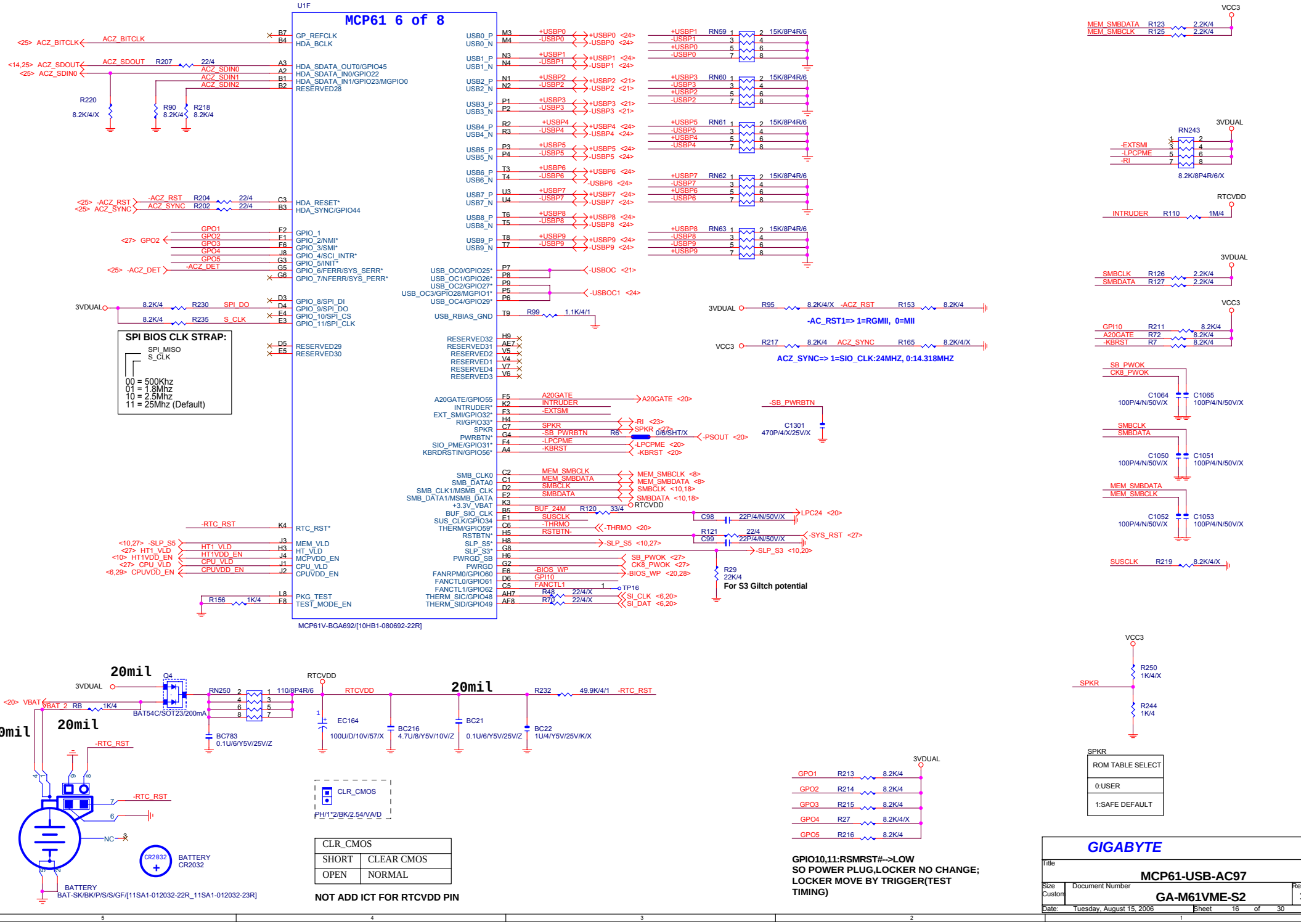
Size: Custom	Document Number: GA-M61VME-S2	Rev: 1.01
Date: Tuesday, August 15, 2006	Sheet 14 of 30	



GIGABYTE			
Title: MCP61-SATA/IDE			
Size: Custom	Document Number: GA-M61VME-S2		Rev: 1.01
Date: Tuesday, August 15, 2006	Sheet 15 of 30		


U1F
MCP61 6 of 8
MCP61V-BGA692/[10HB1-080692-22R]
SPI BIOS CLK STRAP:
SPI_MISO
S_CLK
00 = 500Khz
01 = 1.8Mhz
10 = 2.5Mhz
11 = 25Mhz (Default)
-AC_RST1=> 1=RGMII, 0=MII
ACZ_SYNC=> 1=SIO_CLK:24MHZ, 0:14.318MHZ
For S3 Glitch potential
20mil
BAT54C/SOT23/200mA
BATTERY
BAT-SK/BK/P/S/GF/[11SA1-012032-22R_11SA1-012032-23R]
CLR_CMOS
PH/1*2/BK/2.54/VA/D
CLR_CMOS
SHORT CLEAR CMOS
OPEN NORMAL
NOT ADD ICT FOR RTCVDD PIN
SPKR
ROM TABLE SELECT
0:USER
1:SAFE DEFAULT
GPIO10,11:RSMRST#-->LOW
SO POWER PLUG,LOCKER NO CHANGE;
LOCKER MOVE BY TRIGGER(TEST TIMING)
GIGABYTE
MCP61-USB-AC97
GA-M61VME-S2
1.01
Tuesday, August 15, 2006
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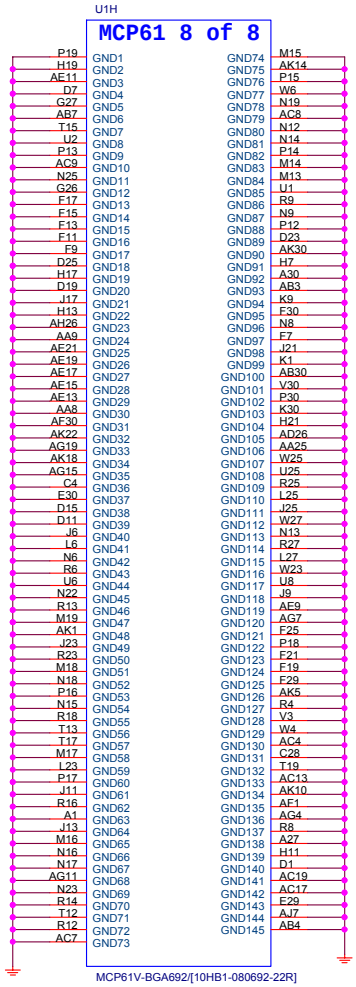

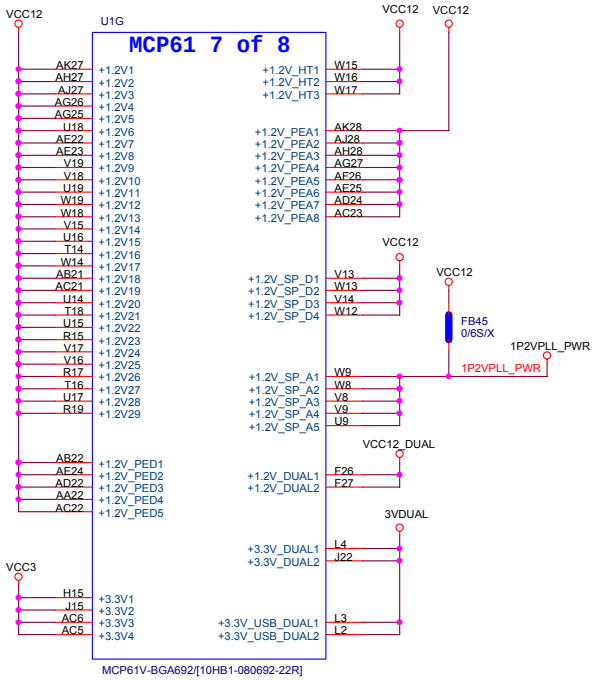

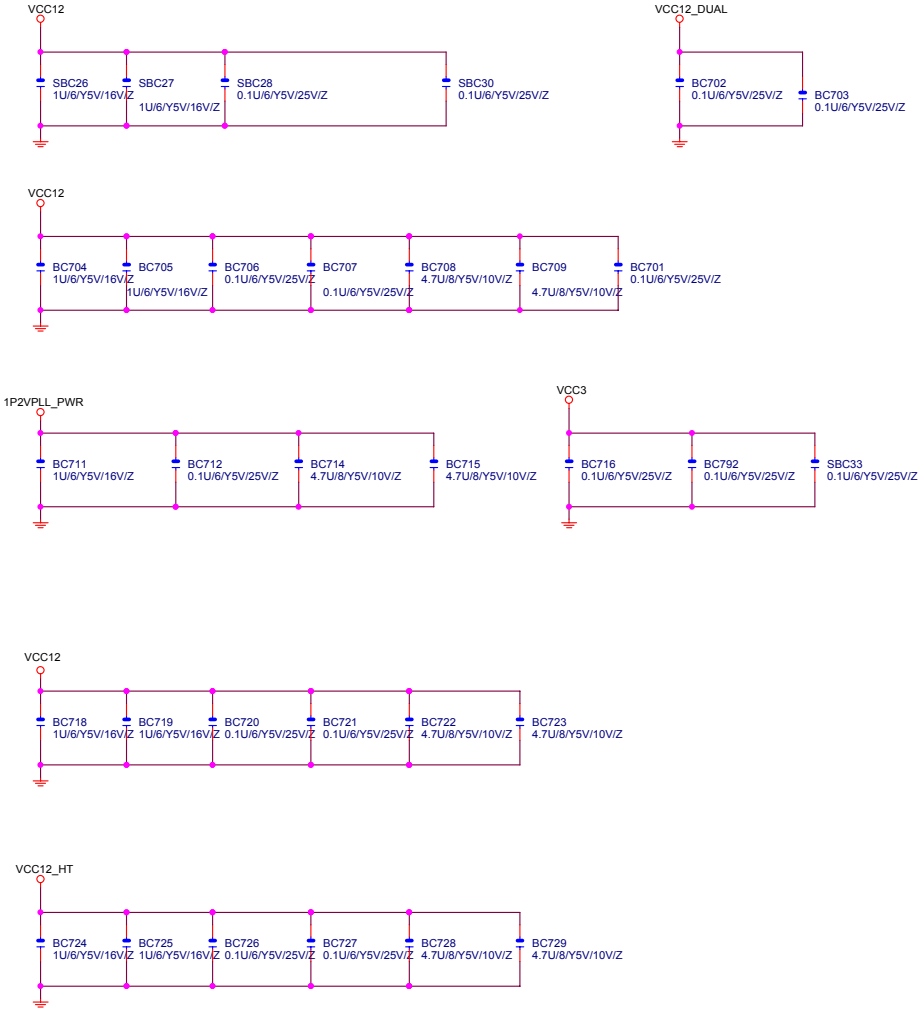

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Title	MCP61-Power	
Size: Custom	Document Number: GA-M61VME-S2	Rev: 1.01
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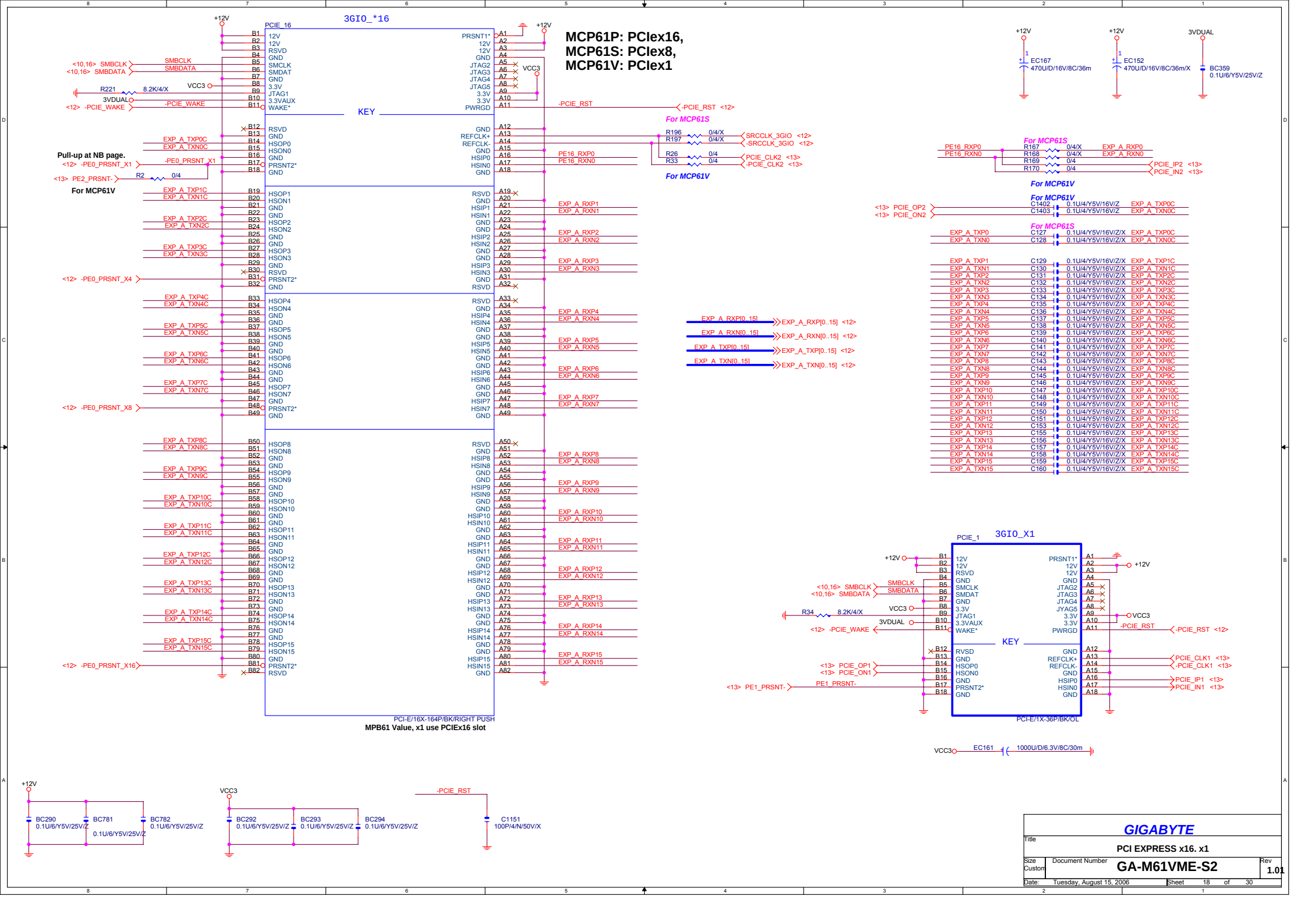
MCP61P: PCIex16,
MCP61S: PCIex8,
MCP61V: PCIex1
3GIO_*16
PCIE_16
KEY
PCI-E/16X-164P/BK/RIGHT PUSH
MPB61 Value, x1 use PCIEx16 slot
Pull-up at NB page.
For MCP61V
For MCP61S
3GIO_X1
PCIE_1
PCI-E/1X-36P/BK/OL
GIGABYTE
PCI EXPRESS x16. x1
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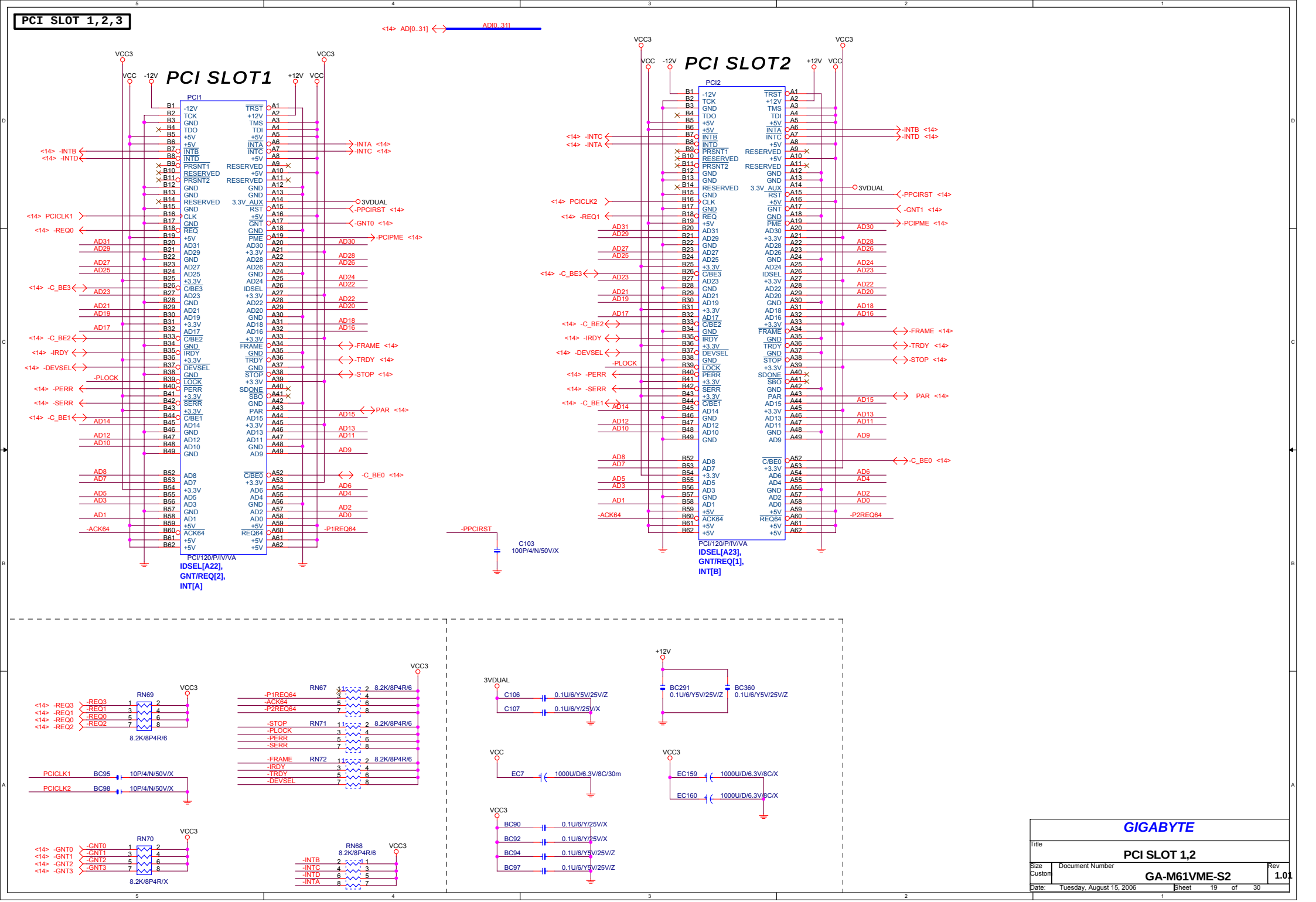
PCI SLOT 1,2,3



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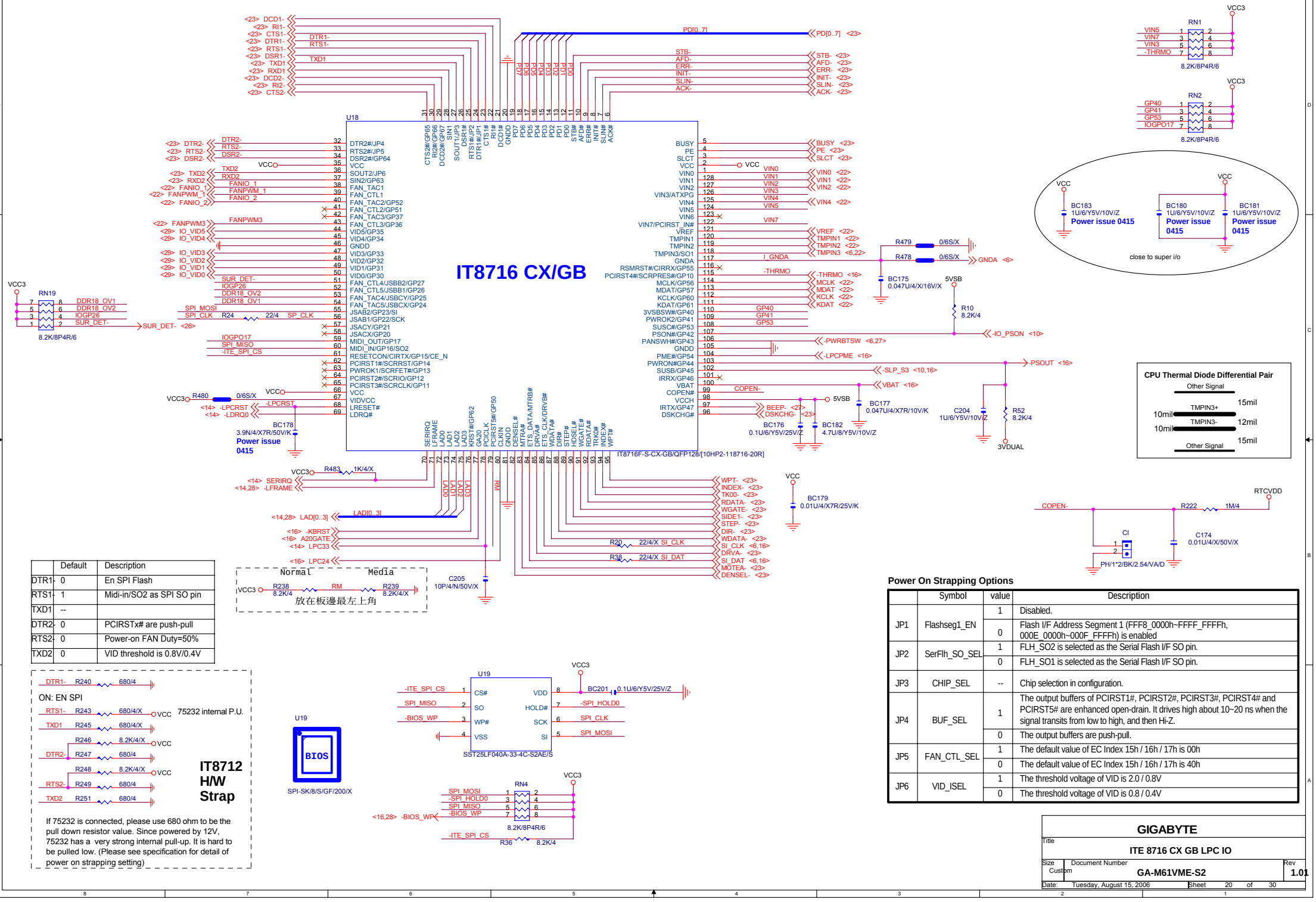
Title	PCI SLOT 1,2	
Size: Custom	Document Number: GA-M61VME-S2	Rev: 1.01
Date: Tuesday, August 15, 2006	Sheet 19 of 30	



	Default	Description
DTR1-	0	En SPI Flash
RTS1-	1	Midi-in/SO2 as SPI SO pin
TXD1	--	
DTR2-	0	PCIRSTx# are push-pull
RTS2-	0	Power-on FAN Duty=50%
TXD2	0	VID threshold is 0.8V/0.4V

Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

GIGABYTE

Title: ITE 8716 CX GB LPC IO

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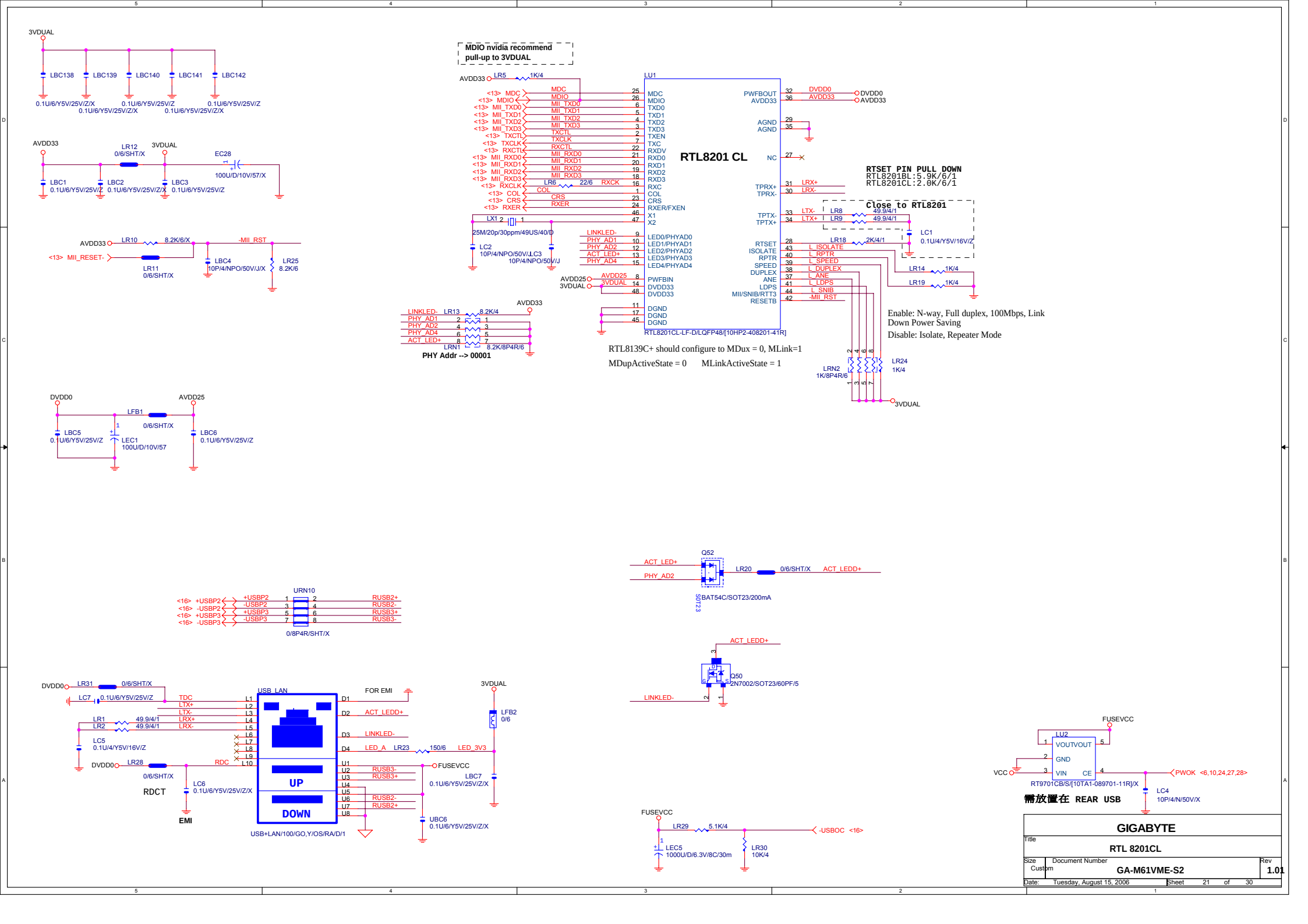
3VDUAL
LBC138
LBC139
LBC140
LBC141
LBC142
0.1U/6/Y5V/25V/Z/X
0.1U/6/Y5V/25V/Z
0.1U/6/Y5V/25V/Z/X
0.1U/6/Y5V/25V/Z/X
0.1U/6/Y5V/25V/Z
AVDD33
LR12
0/6/SHT/X
3VDUAL
EC28
100U/D/10V/57/X
LBC1
0.1U/6/Y5V/25V/Z
LBC2
0.1U/6/Y5V/25V/Z/X
LBC3
0.1U/6/Y5V/25V/Z
AVDD33
LR10
8.2K/6/X
-MII_RST
<13> MII_RESET-
LR11
0/6/SHT/X
LBC4
10P/4/NPO/50V/J/X
LR25
8.2K/6
MDIO nvidia recommend
pull-up to 3VDUAL
AVDD33
LR5
1K/4
LU1
<13> MDC
<13> MDIO
<13> MII_TXD0
<13> MII_TXD1
<13> MII_TXD2
<13> MII_TXD3
<13> TXCTL
<13> TXCLK
<13> RXCTL
<13> MII_RXD0
<13> MII_RXD1
<13> MII_RXD2
<13> MII_RXD3
<13> RXCLK
<13> COL
<13> CRS
<13> RXER
LR6
22/6
RXCK
LX1
25M/20p/30ppm/49US/40/D
LC2
10P/4/NPO/50V/.LC3
10P/4/NPO/50V/J
RTL8201 CL
MDC
MDIO
TXD0
TXD1
TXD2
TXD3
TXEN
TXC
RXDV
RXD0
RXD1
RXD2
RXD3
RXC
COL
CRS
RXER/FXEN
X1
X2
LED0/PHYAD0
LED1/PHYAD1
LED2/PHYAD2
LED3/PHYAD3
LED4/PHYAD4
PWFBIN
DVDD33
DVDD33
DGND
DGND
DGND
RTL8201CL-LF-D/LQFP48/[10HP2-408201-41R]
LINKLED-
PHY_AD1
PHY_AD2
ACT_LED+
PHY_AD4
AVDD25
3VDUAL
PWFBOUT
AVDD33
DVDD0
AVDD33
AGND
AGND
NC
TPRX+
TPRX-
TPTX-
TPTX+
RTSET
ISOLATE
RPTR
SPEED
DUPLEX
ANE
LDPS
MII/SNIB/RTT3
RESETB
LRX+
LRX-
LTX-
LTX+
LR8
LR9
49.9/4/1
LR18
2K/4/1
L_ISOLATE
L_RPTR
L_SPEED
L_DUPLEX
L_ANE
L_LDPS
L_SNIB
-MII_RST
LR14
LR19
1K/4
LC1
0.1U/4/Y5V/16V/Z
RTSET PIN PULL DOWN
RTL8201BL:5.9K/6/1
RTL8201CL:2.0K/6/1
Close to RTL8201
Enable: N-way, Full duplex, 100Mbps, Link Down Power Saving
Disable: Isolate, Repeater Mode
LRN2
1K/8P4R/6
LR24
1K/4
3VDUAL
AVDD33
LINKLED-
PHY_AD1
PHY_AD2
PHY_AD4
ACT_LED+
LR13
8.2K/4
LRN1
8.2K/8P4R/6
PHY Addr --> 00001
RTL8139C+ should configure to MDux = 0, MLink=1
MDupActiveState = 0 MLinkActiveState = 1
DVDD0
AVDD25
LFB1
0/6/SHT/X
LBC5
0.1U/6/Y5V/25V/Z
LEC1
100U/D/10V/57
LBC6
0.1U/6/Y5V/25V/Z
URN10
<16> +USBP2
<16> -USBP2
<16> +USBP3
<16> -USBP3
+USBP2
-USBP2
+USBP3
-USBP3
RUSB2+
RUSB2-
RUSB3+
RUSB3-
0/8P4R/SHT/X
Q52
ACT_LED+
PHY_AD2
LR20
0/6/SHT/X
ACT_LEDD+
SOT23
BAT54C/SOT23/200mA
ACT_LEDD+
Q50
2N7002/SOT23/60PF/5
LINKLED-
DVDD0
LR31
0/6/SHT/X
LC7
0.1U/6/Y5V/25V/Z
LR1
LR2
49.9/4/1
LC5
0.1U/4/Y5V/16V/Z
DVDD0
LR28
0/6/SHT/X
RDCT
EMI
LC6
0.1U/6/Y5V/25V/Z/X
TDC
LTX+
LTX-
LRX+
LRX-
RDC
USB_LAN
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
UP
DOWN
USB+LAN/100/GO,Y/OS/RA/D/1
FOR EMI
D1
D2
D3
D4
ACT_LEDD+
LINKLED-
LED_A
LR23
150/6
LED_3V3
U1
U2
U3
U4
U5
U6
U7
U8
RUSB3-
RUSB3+
RUSB2-
RUSB2+
FUSEVCC
LBC7
0.1U/6/Y5V/25V/Z/X
UBC6
0.1U/6/Y5V/25V/Z/X
3VDUAL
LFB2
0/6
FUSEVCC
LR29
5.1K/4
-USBOC <16>
LEC5
1000U/D/6.3V/8C/30m
LR30
10K/4
FUSEVCC
LU2
VOUTVOUT
GND
VIN
CE
VCC
PWOK <6,10,24,27,28>
RT9701CB/S/[10TA1-089701-11R]/X
LC4
10P/4/N/50V/X
需放置在 REAR USB
GIGABYTE
Title
RTL 8201CL
Size
Custom
Document Number
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Rev
1.01
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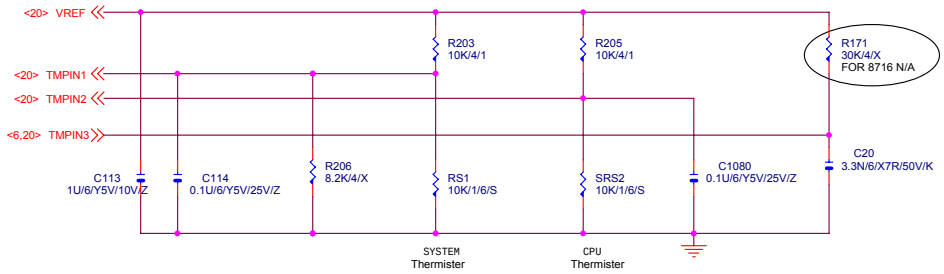
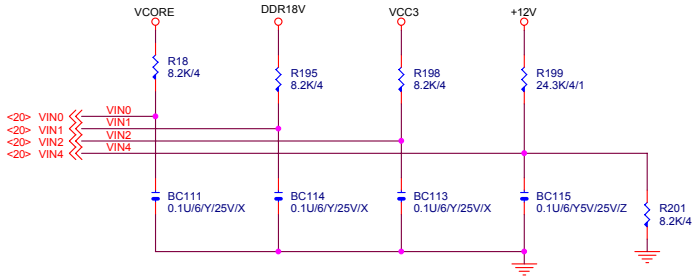
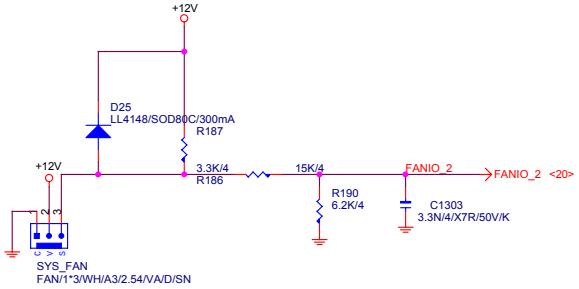
Hardware Monitor circuits

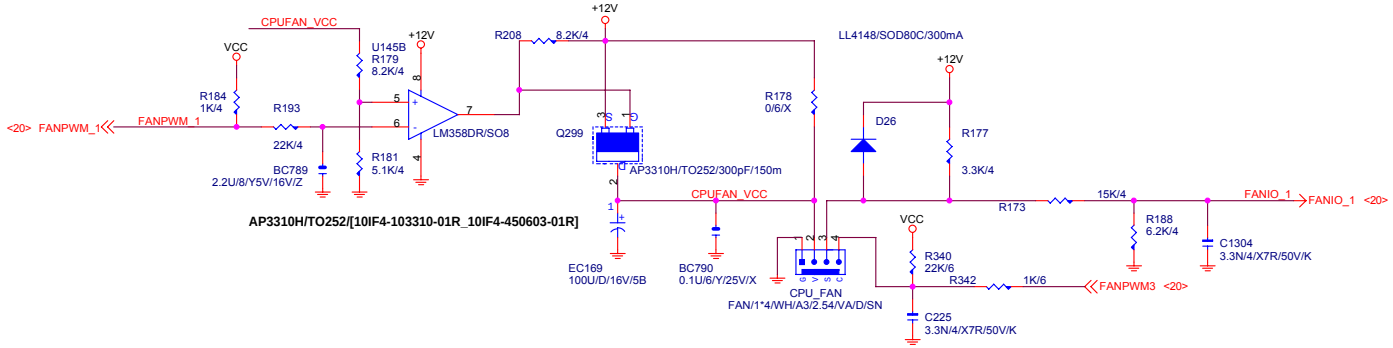




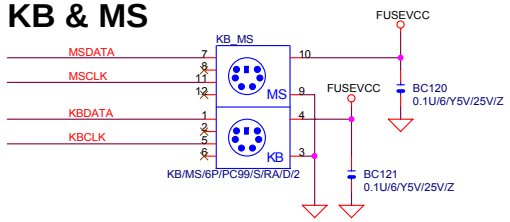
SYSTEM FAN

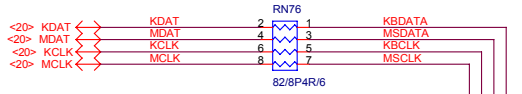


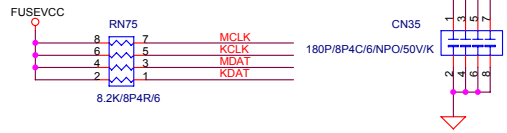
CPU FAN



KB & MS







GIGABYTE

Title: FAN/HWMO KB/MS

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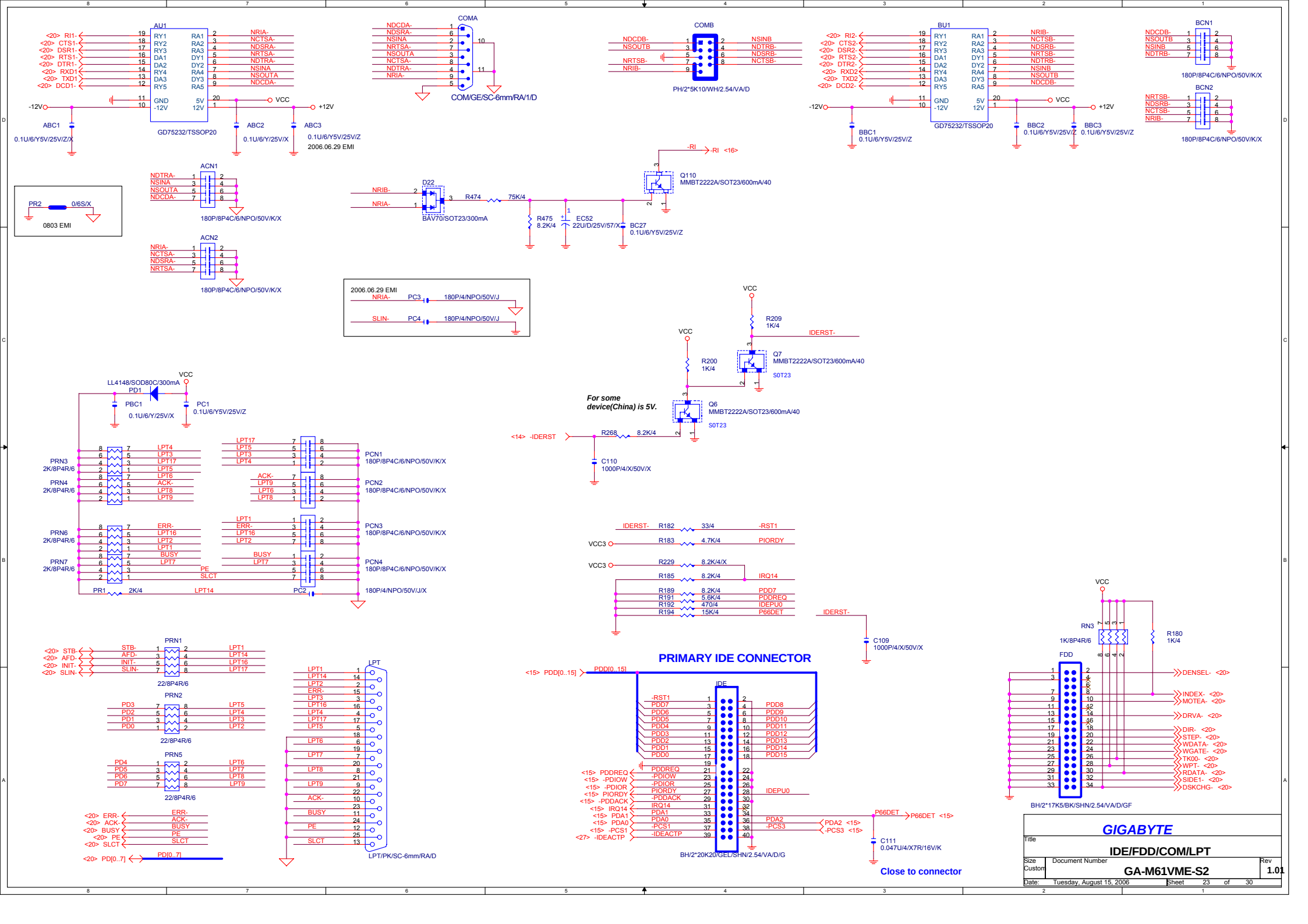
AU1
GD75232/TSSOP20
ABC1
0.1U/6/Y5V/25V/Z/X
ABC2
0.1U/6/Y/25V/X
ABC3
0.1U/6/Y5V/25V/Z
2006.06.29 EMI
COMA
COM/GE/SC-6mm/RA/1/D
COMB
PH/2*5K10/WH/2.54/VA/D
BU1
GD75232/TSSOP20
BBC1
0.1U/6/Y5V/25V/Z
BBC2
0.1U/6/Y5V/25V/Z
BBC3
0.1U/6/Y5V/25V/Z
BCN1
BCN2
180P/8P4C/6/NPO/50V/K/X
PR2
0/6S/X
0803 EMI
ACN1
ACN2
180P/8P4C/6/NPO/50V/K/X
D22
BAV70/SOT23/300mA
R474
75K/4
R475
8.2K/4
EC52
22U/D/25V/57/X
BC27
0.1U/6/Y5V/25V/Z
Q110
MMBT2222A/SOT23/600mA/40
2006.06.29 EMI
PC3
PC4
180P/4/NPO/50V/J
LL4148/SOD80C/300mA
PD1
PBC1
0.1U/6/Y/25V/X
PC1
0.1U/6/Y5V/25V/Z
PRN3
2K/8P4R/6
PRN4
2K/8P4R/6
PRN6
2K/8P4R/6
PRN7
2K/8P4R/6
PR1
2K/4
PC2
PCN1
PCN2
PCN3
PCN4
180P/8P4C/6/NPO/50V/K/X
180P/4/NPO/50V/J/X
For some device(China) is 5V.
R209
1K/4
R200
1K/4
Q7
MMBT2222A/SOT23/600mA/40
S0T23
Q6
MMBT2222A/SOT23/600mA/40
S0T23
R268
8.2K/4
C110
1000P/4/X/50V/X
R182
33/4
R183
4.7K/4
R229
8.2K/4/X
R185
8.2K/4
R189
8.2K/4
R191
5.6K/4
R192
470/4
R194
15K/4
C109
1000P/4/X/50V/X
PRN1
22/8P4R/6
PRN2
22/8P4R/6
PRN5
22/8P4R/6
LPT
LPT/PK/SC-6mm/RA/D
PRIMARY IDE CONNECTOR
IDE
BH/2*20K20/GEL/SHN/2.54/VA/D/G
C111
0.047U/4/X7R/16V/K
Close to connector
RN3
1K/8P4R/6
R180
1K/4
FDD
BH/2*17K5/BK/SHN/2.54/VA/D/GF
GIGABYTE
Title
IDE/FDD/COM/LPT
Size
Custom
Document Number
GA-M61VME-S2
Rev
1.01
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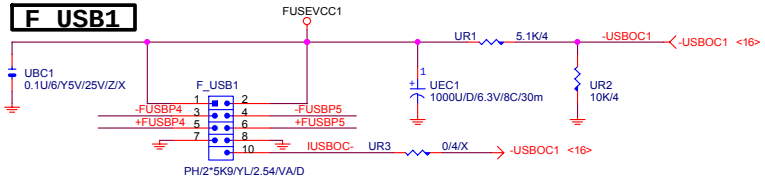

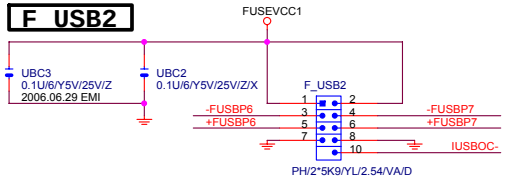

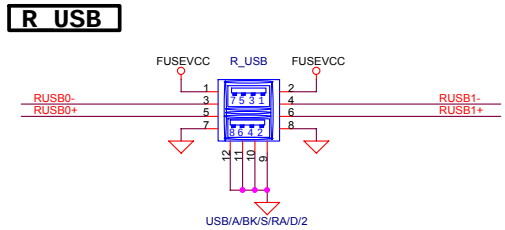

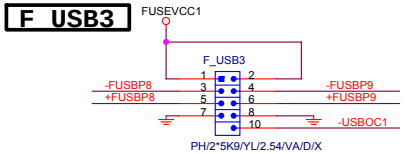

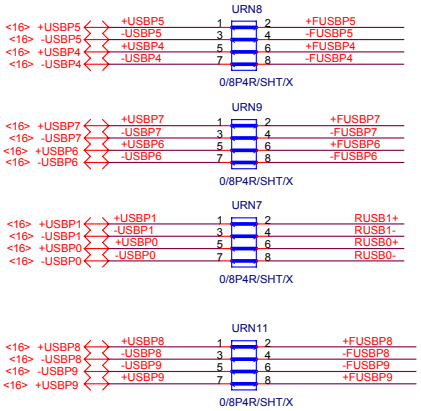

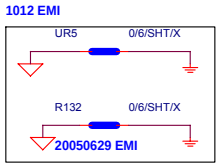

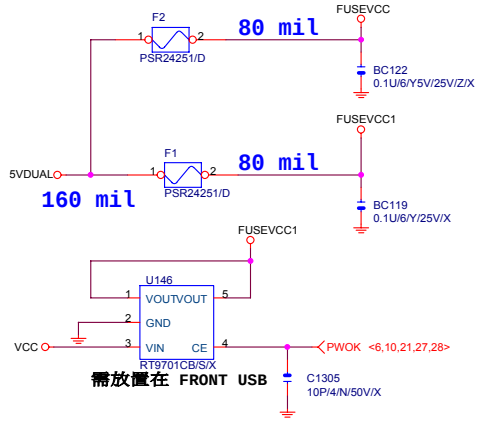

GIGABYTE

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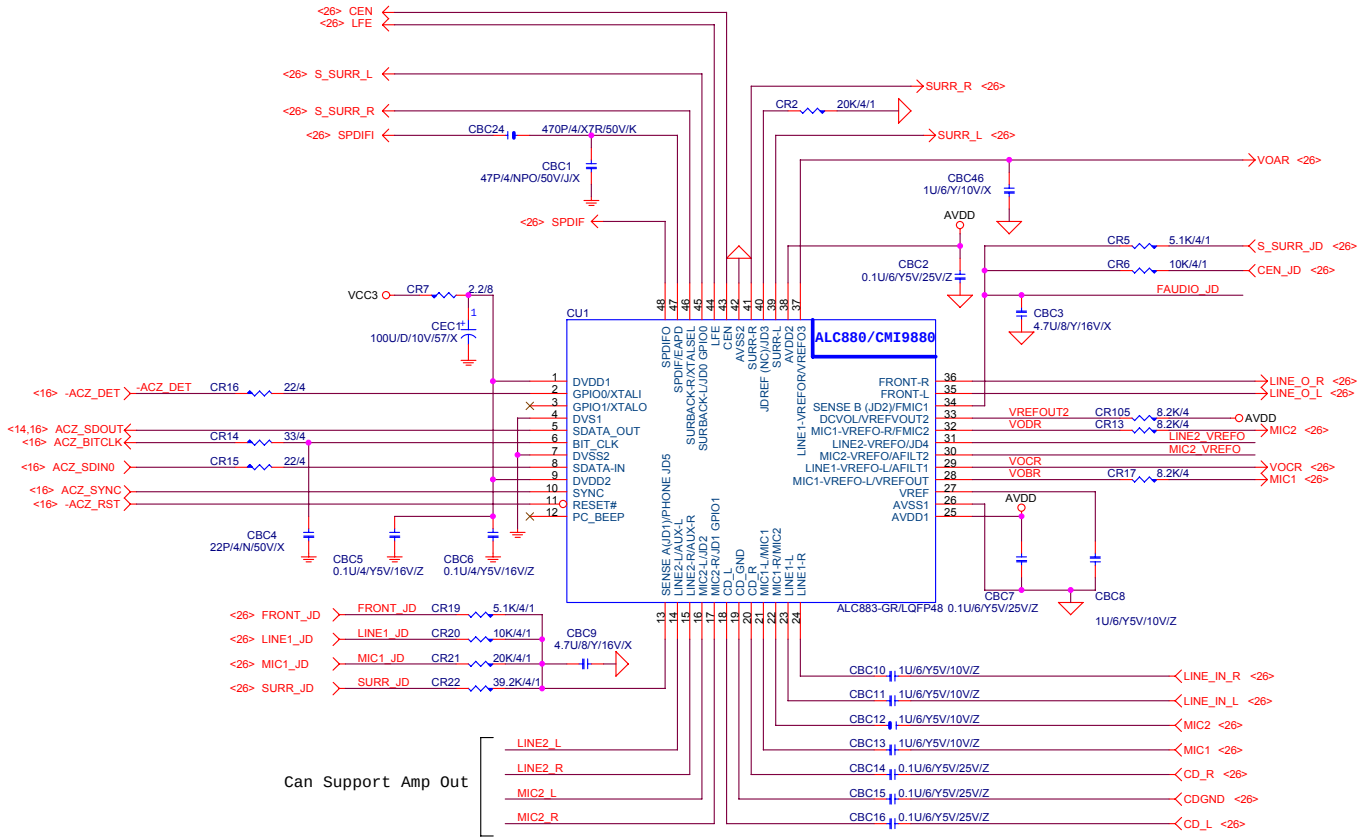

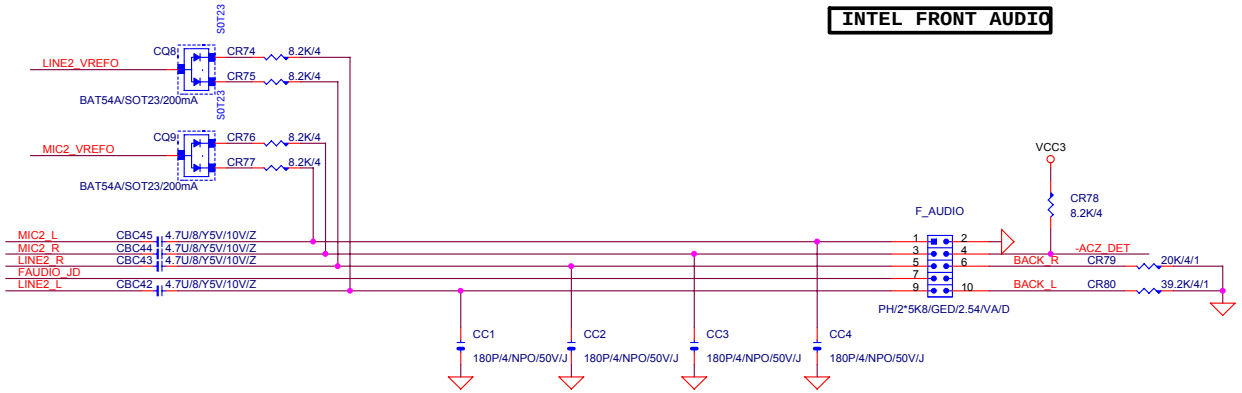

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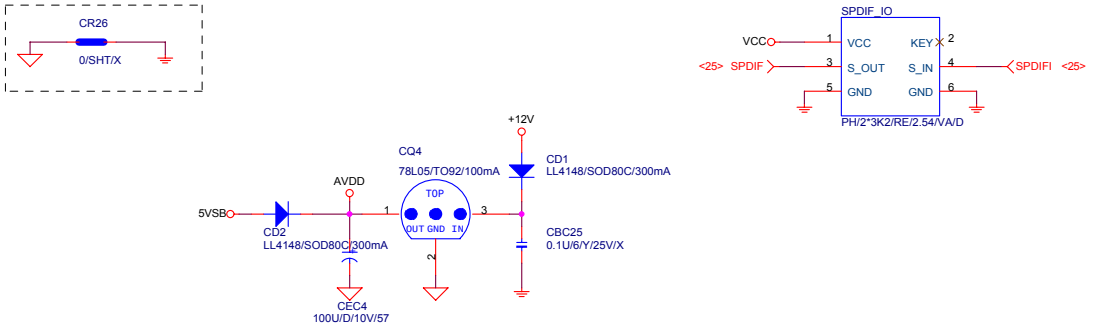
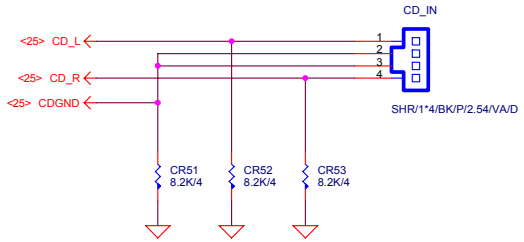
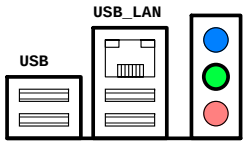
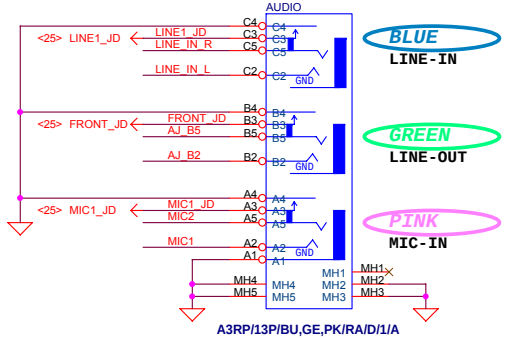
Size: Custom	Document Number: GA-M61VME-S2	Rev: 1.01
Date: Tuesday, August 15, 2006	Sheet 25 of 30	

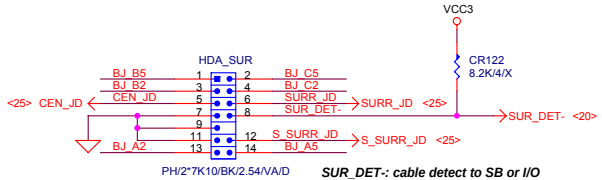


CD IN





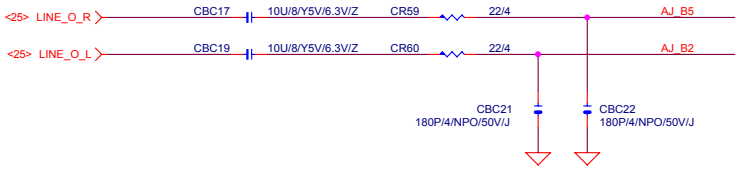




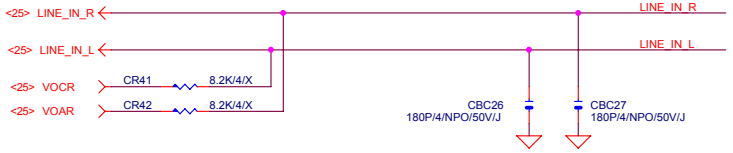
SUR_DET-: cable detect to SB or I/O
insert cable: low, default : high

A3RJ/13P/B/[11NR6-403006-01_11NR6-403006-02]
3RJ+15F/[11NR6-403004-11]

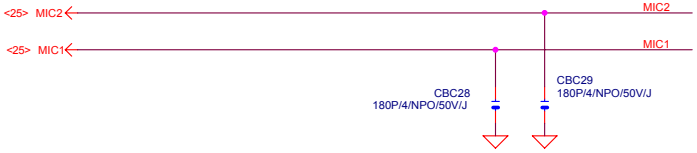
LINE OUT FRONT OUT



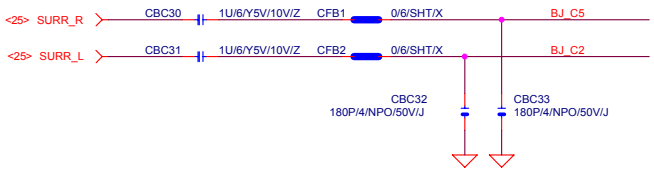
LINE-IN



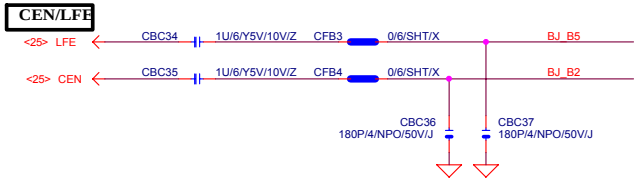
MIC



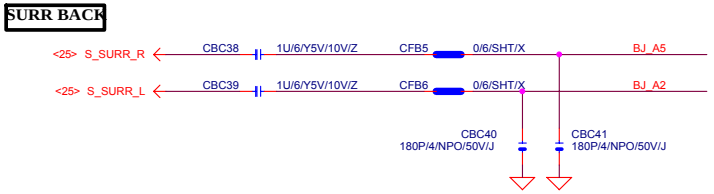
SURROUND



CEN/LFE



SURR BACK



GIGABYTE			
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Size: Custom	Document Number: GA-M61VME-S2		Rev: 1.01
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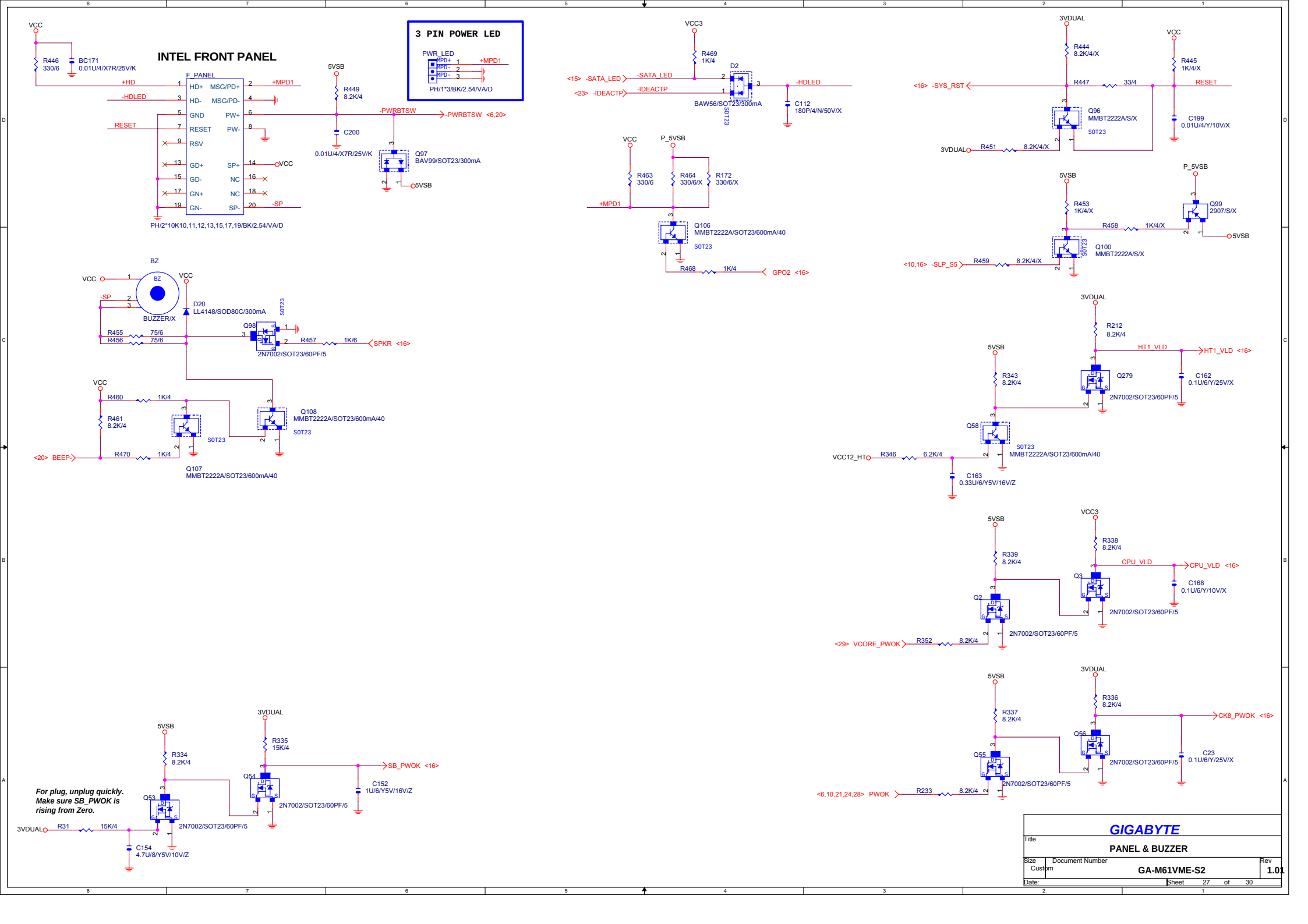
INTEL FRONT PANEL
F_PANEL
PH/2*10K10,11,12,13,15,17,19/BK/2.54/VA/D
3 PIN POWER LED
PWR_LED
PH/1*3/BK/2.54/VA/D
BUZZER/X
D20
LL4148/SOD80C/300mA
2N7002/SOT23/60PF/5
Q107
MMBT2222A/SOT23/600mA/40
Q108
MMBT2222A/SOT23/600mA/40
D2
BAW56/SOT23/300mA
Q97
BAV99/SOT23/300mA
Q106
MMBT2222A/SOT23/600mA/40
Q96
MMBT2222A/S/X
Q100
MMBT2222A/S/X
Q99
2907/S/X
Q279
Q58
MMBT2222A/SOT23/600mA/40
Q2
Q3
Q56
Q55
Q53
Q54
For plug, unplug quickly.
Make sure SB_PWOK is
rising from Zero.
GIGABYTE
PANEL & BUZZER
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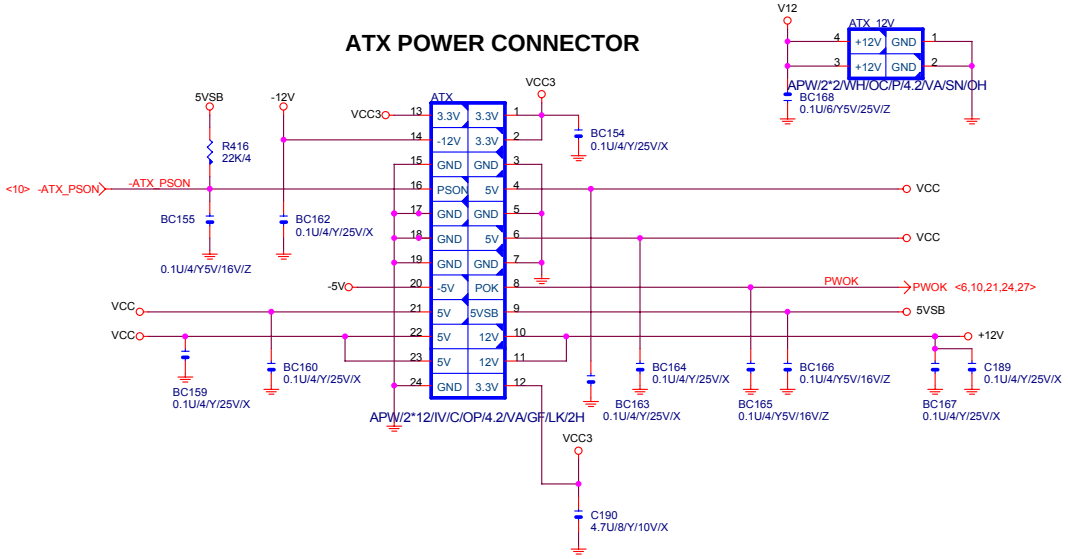
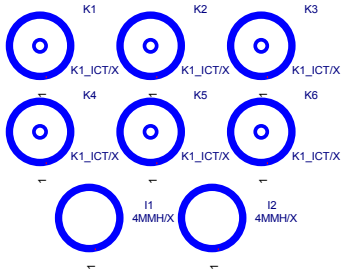
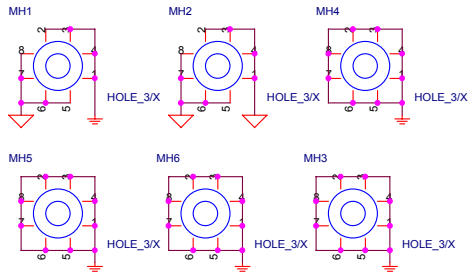
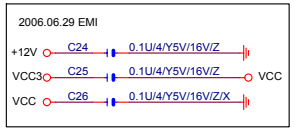
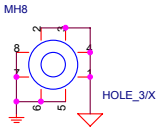
ATX POWER CONNECTOR

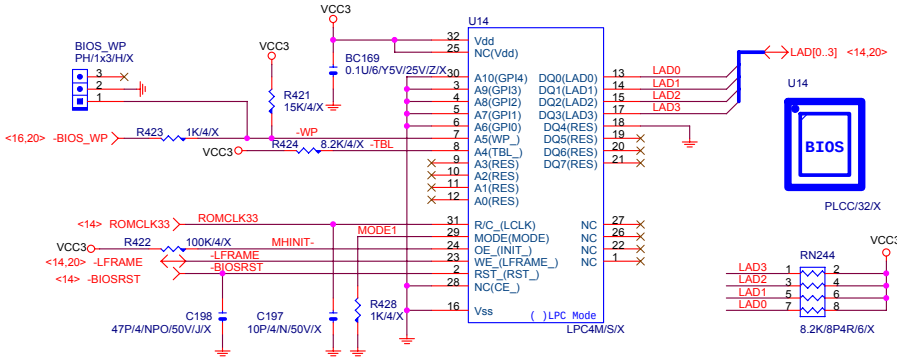


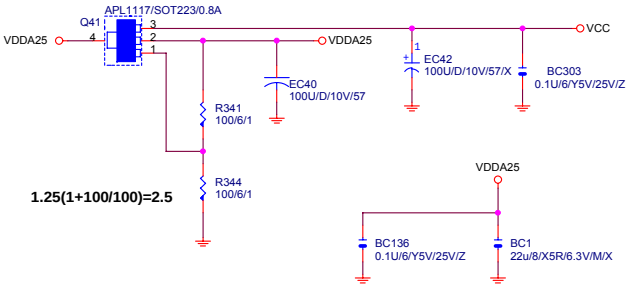


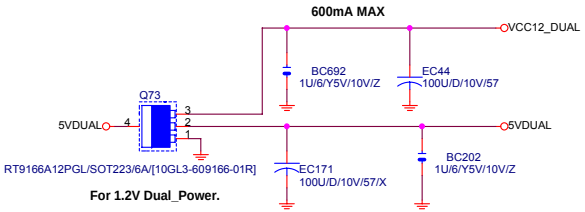


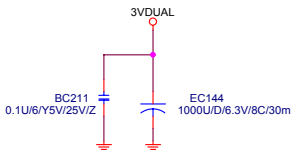












GIGABYTE

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Size: Custom	Document Number: GA-M61VME-S2	Rev: 1.01
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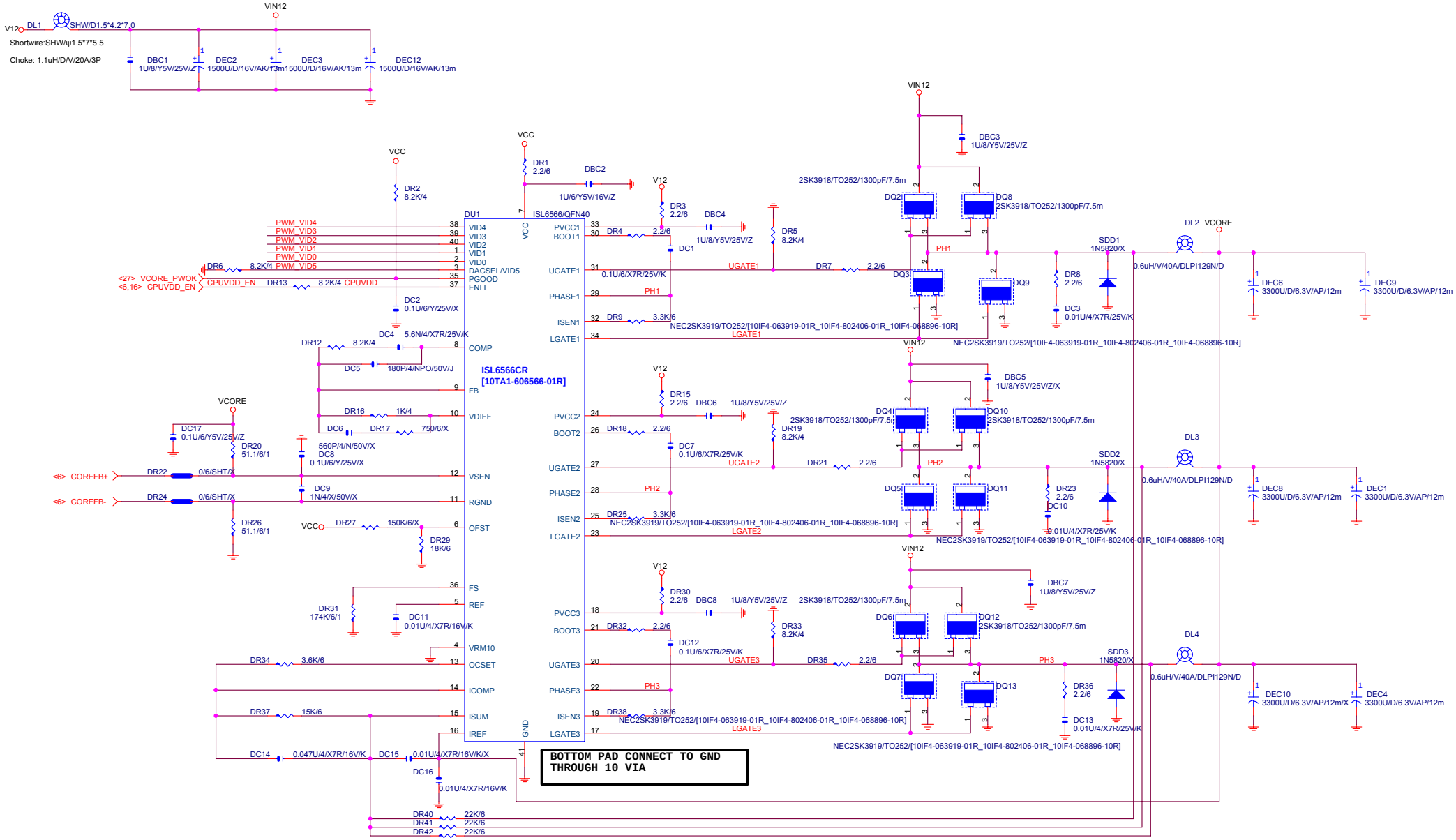

GIGABYTE

Title	VCORE (PWM ISL6566CR)	
Size: Custom	Document Number: GA-M61VME-S2	Rev: 1.01
Date: Tuesday, August 15, 2006	Sheet 29 of 30	