GIGABYTE GA-M55SLI-S4 Schematics

Revision:1.0

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04	M2 CPU Hyper Transport
05	M2 CPU DDR II
06	M2 CPU Control
07	M2 CPU POWER & GND
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10	DDRII TERMINATION
11	CK804 HT
12	CK804 PCI-EXPRESS
13	CK804 PCI, LPC, CLOCK
14	CK804 IDE,SATA
15	CK804 AC97,USB,MII,GPIO
16	CK804 POWER,GND
17	PCI EXPRESS X16 SLOT
18	PCI EXPRESS X8 SLOT
19	PCI EXPRESS X1 SLOT1,2
20	PCI 1,2 SLOT
21	CODEC 850/655/658
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SHEET	TITLE
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29	Discrete Power
30	DDRII Power & Standby Power
31	BIOS (LPC ROM & SPI Flash)
32	FRONT PANEL
33	MARVELL 88E1116 GbE Phy
34	TI 1394A
35	NV-SLI Swirch Board
36	COMA , LPT
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GIGABYTE Technology

Title: Cover Sheet

Size: Custom | Document Number: GA-M55SLI-S4 | Rev: 1.0

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Model Name:GA-M55SLI-S4 1.0

Component value change history

Date	Change Item	Reason
95.03.27_0.1	Rev 0.1 pilot-run BOM	
	M55SLI-S3-00-02	
	Change RN29 to 220/8P4R	For signals level
	Add R536 to 8.2K ohm	
95/05/22	M55SLI-S3-00-10A	
	Location: COAXITL change 11NR6-501004-81 to 11NR6-501004-81R	
	Change COMA to COM/GE/SC-6mm/RA/1/D	
	Remove R255, change C222 to 2.2n/4	
	Del socket_M2 10SC1-A01940-21替料	
	Change F1_1394,F2_1394 to PH/2*5K9/GY/2.54/VA/D	
	Change PCB to rev:1.0	

Circuit or PCB layout change for next version

Date	Change Item	Reason
95.03.27_0.1	1'st version pilot-run	
95/04/26	REV:0.2	
	NB_HS改Footprint:BGAHSINK45X45-5	For LPC enable
	Del LPC flash rom	
	Add DDR protect	
	Change R0603 to R0402-2	
95/05/22	REV:1.0	
	Modify COAXIAL pin 1	
	Del VCC15_OV2	

GIGABYTE Technology

Title: BOM & PCB MODIFY HISTORY

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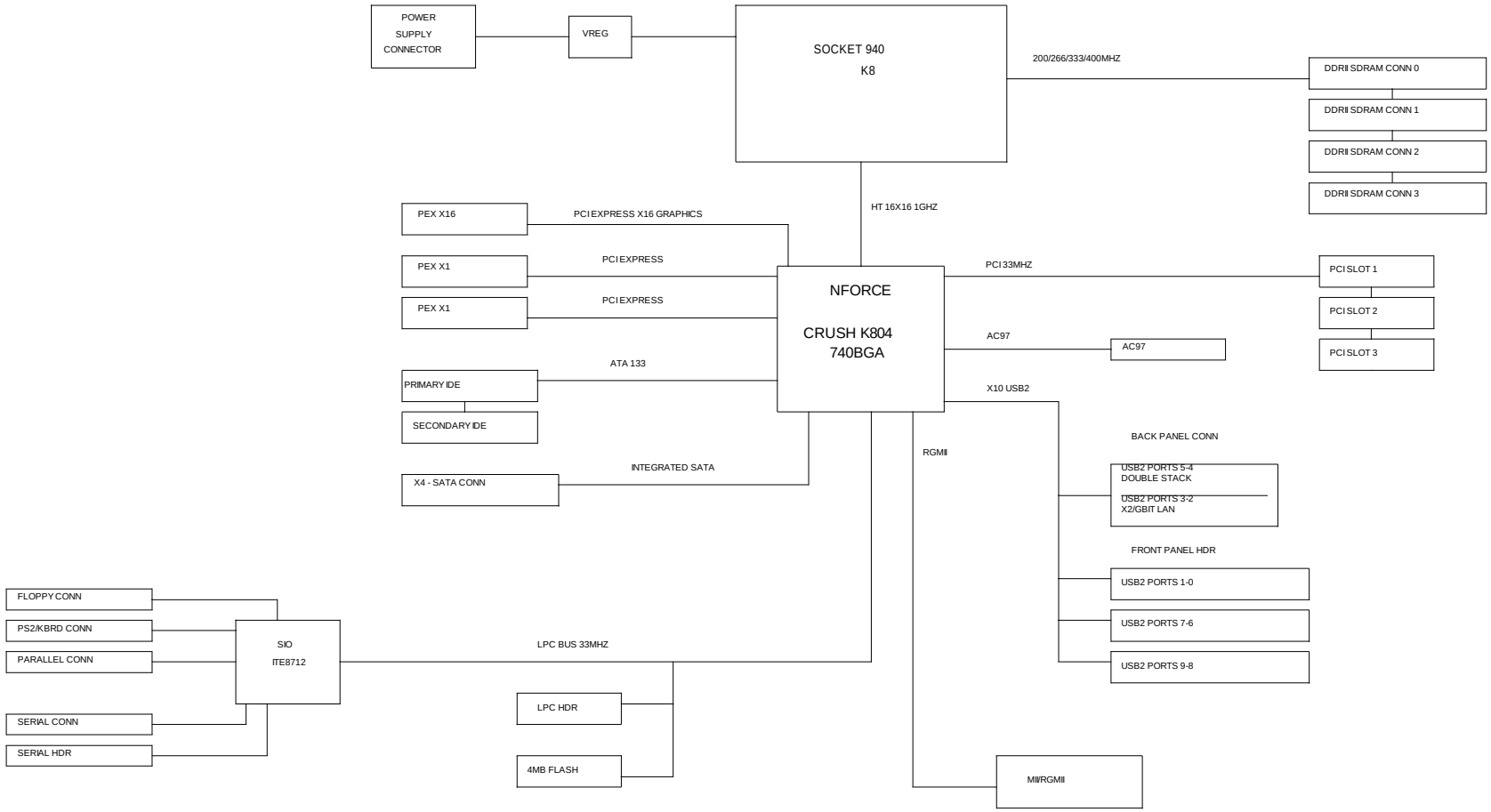
BLOCK DIAGRAM



GIGABYTE Technology		
Title: BLOCK DIAGRAM		
Size: Custom	Document Number: GA-M55SLI-S4	Rev: 1.0
Date: Wednesday, May 24, 2006	Sheet 3 of 36	

L0_CADIN_L[0..15]
L0_CADIN_H[0..15]
L0_CLKIN_L[0..1]
L0_CLKIN_H[0..1]
L0_CADOUT_L[0..15]
L0_CADOUT_H[0..15]
L0_CLKOUT_L[0..1]
L0_CLKOUT_H[0..1]

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

SOCKET_M2A

HYPERTRANSPORT

L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1		
L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1		
L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0		
L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0		
				Y6	L0_CTLOUT_H1	1	TP1
				W6	L0_CTLOUT_L1	1	TP2
11 L0_CTLIN_H0	U1	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	W2	L0_CTLOUT_H0		11 L0_CTLOUT_H0
11 L0_CTLIN_L0	V1	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W3	L0_CTLOUT_L0		11 L0_CTLOUT_L0
		L0_CTLIN_H(0)	L0_CTLOUT_H(0)				
		L0_CTLIN_L(0)	L0_CTLOUT_L(0)				
L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15		
L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15		
L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14		
L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14		
L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13		
L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13		
L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12		
L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12		
L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11		
L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11		
L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10		
L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10		
L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9		
L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9		
L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8		
L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8		
L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7		
L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7		
L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6		
L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6		
L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5		
L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5		
L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4		
L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4		
L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3		
L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3		
L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2		
L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2		
L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1		
L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1		
L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0		
L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0		

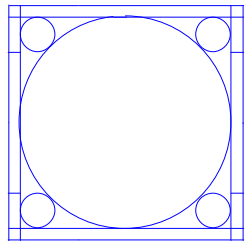
VCC12_HT
R1 49.9/4/1
R2 49.9/4/1

CPU-SK/940AM2/S/15u

VCORE
SC1 0.01U/4/Y5V/50V/Z
SC2 0.01U/4/Y5V/50V/Z
SC3 0.01U/4/Y5V/50V/Z

CLOSE CHIPSET & CROSSING BOUNDARY

SOCKET_M2



K8-940AM2/RM/BP-M/SC/BK/3M/[12KRC-04K807-41R]

GIGABYTE Technology

Title: CPU HYPER TRANSPORT

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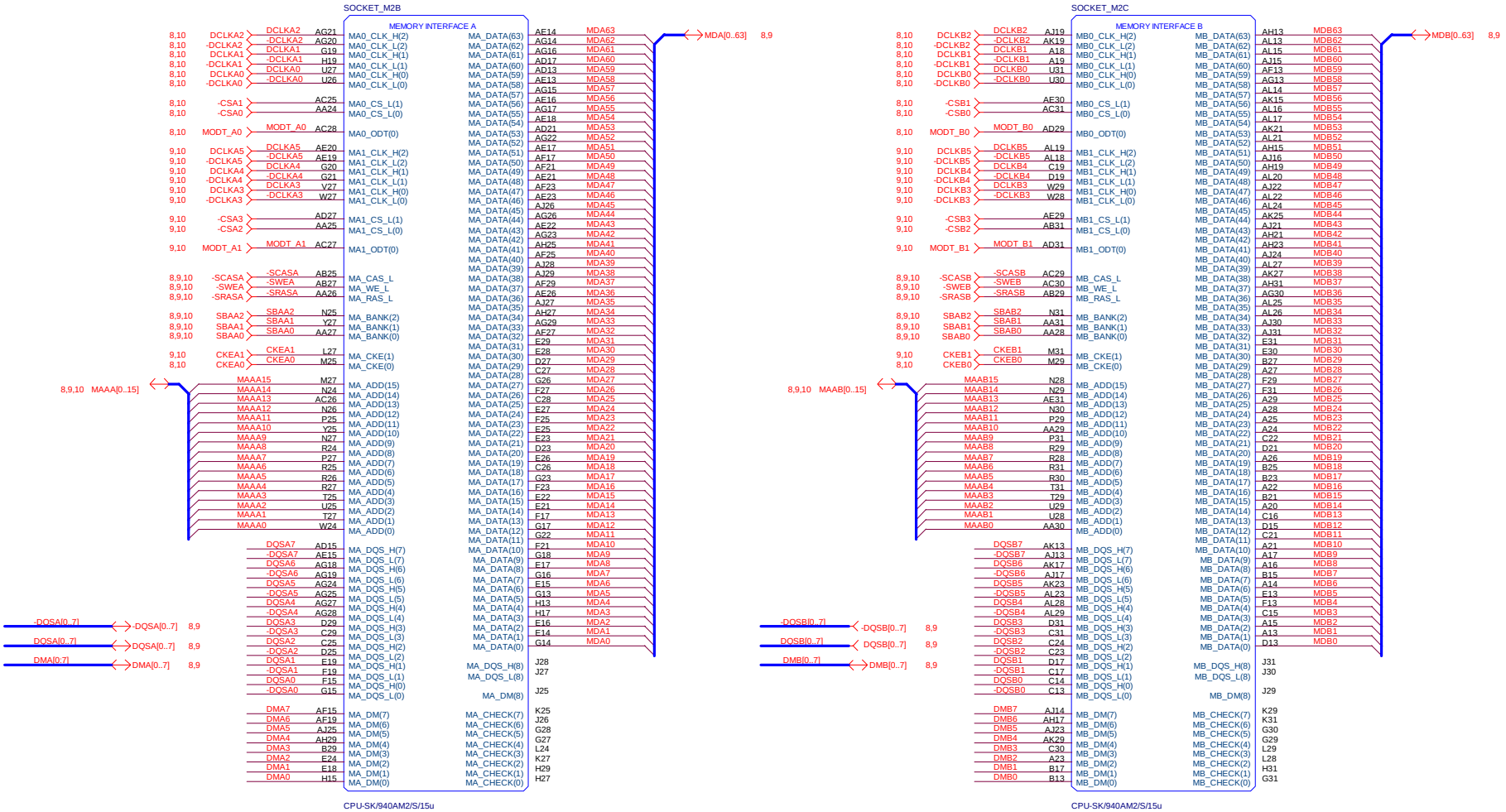

GIGABYTE Technology		
Title	CPU DDRII MEMORY	
Size: Custom	Document Number: GA-M55SLI-S4	Rev: 1.0
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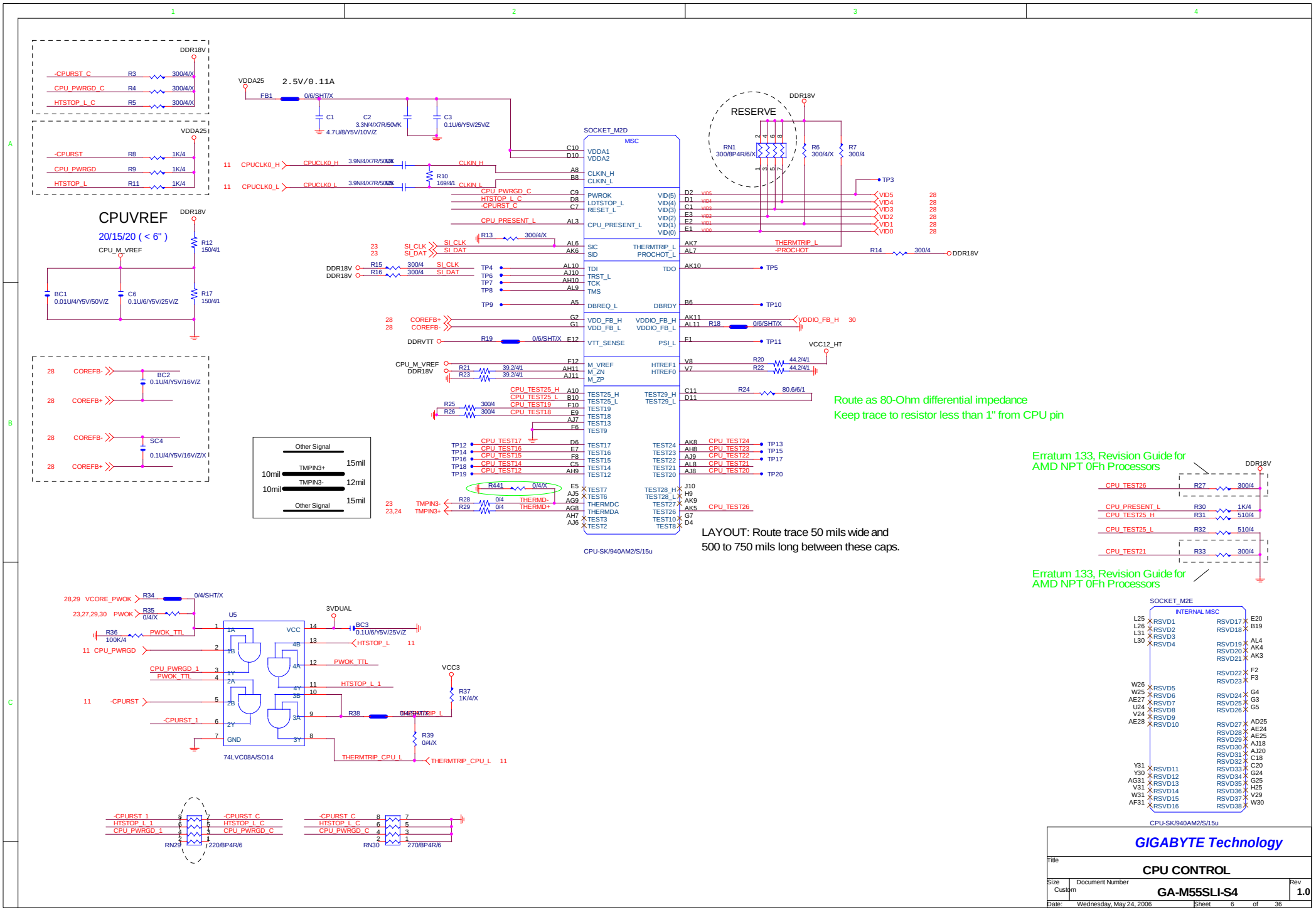
DDR18V
-CPURST_C R3 300/4/X
CPU_PWRGD_C R4 300/4/X
HTSTOP_L_C R5 300/4/X
VDDA25
-CPURST R8 1K/4
CPU_PWRGD R9 1K/4
HTSTOP_L R11 1K/4
CPUVREF
20/15/20 (< 6")
CPU_M_VREF
R12 150/4/1
R17 150/4/1
BC1 0.01U/4/Y5V/50V/Z
C6 0.1U/6/Y5V/25V/Z
28 COREFB- BC2 0.1U/4/Y5V/16V/Z
28 COREFB+
28 COREFB- SC4 0.1U/4/Y5V/16V/Z/X
28 COREFB+
VDDA25 2.5V/0.11A
FB1 0/6/SHT/X
C1 4.7U/8/Y5V/10V/Z
C2 3.3N/4/X7R/50V/K
C3 0.1U/6/Y5V/25V/Z
11 CPUCLK0_H CPUCLK0_H 3.9N/4/X7R/50V/K CLKIN_H
11 CPUCLK0_L CPUCLK0_L 3.9N/4/X7R/50V/K CLKIN_L
R10 169/4/1
SOCKET_M2D
MISC
C10 VDDA1
D10 VDDA2
A8 CLKIN_H
B8 CLKIN_L
C9 PWROK
D8 LDTSTOP_L
C7 RESET_L
CPU_PWRGD_C
HTSTOP_L_C
-CPURST_C
CPU_PRESENT_L AL3
R13 300/4/X
23 SI_CLK AL6 SIC
23 SI_DAT AK6 SID
DDR18V R15 300/4 SI_CLK TP4 AL10 TDI
DDR18V R16 300/4 SI_DAT TP6 AJ10 TRST_L
TP7 AH10 TCK
TP8 AL9 TMS
TP9 A5 DBREQ_L
28 COREFB+ G2 VDD_FB_H
28 COREFB- G1 VDD_FB_L
DDRVTT R19 0/6/SHT/X E12 VTT_SENSE
CPU_M_VREF DDR18V R21 39.2/4/1 R23 39.2/4/1 F12 M_VREF AH11 M_ZN AJ11 M_ZP
CPU_TEST25_H A10 TEST25_H
CPU_TEST25_L B10 TEST25_L
CPU_TEST19 F10 TEST19
CPU_TEST18 F9 TEST18
AJ7 TEST13
F6 TEST9
R25 300/4 R26 300/4
TP12 CPU_TEST17 D6 TEST17
TP14 CPU_TEST16 E7 TEST16
TP16 CPU_TEST15 F8 TEST15
TP18 CPU_TEST14 C5 TEST14
TP19 CPU_TEST12 AH9 TEST12
R441 0/4/X E5 TEST7
AJ5 TEST6
23 TMPIN3- R28 0/4 THERMD- AG9 THERMDC
23,24 TMPIN3+ R29 0/4 THERMD+ AG8 THERMDA
AH7 TEST3
AJ6 TEST2
VID(5) D2 VID5
VID(4) D1 VID4
VID(3) C1 VID3
VID(2) E3 VID2
VID(1) E2 VID1
VID(0) E1 VID0
AK7 THERMTRIP_L
AL7 PROCHOT_L
TDO AK10 TP5
DBRDY B6 TP10
VDDIO_FB_H AK11
VDDIO_FB_L AL11 R18 0/6/SHT/X VDDIO_FB_H 30
PSI_L F1 TP11
HTREF1 V8 R20 44.2/4/1
HTREF0 V7 R22 44.2/4/1
TEST29_H C11 R24 80.6/6/1
TEST29_L D11
TEST28_H J10
TEST28_L H9
TEST27 AK9
TEST26 AK5 CPU_TEST26
TEST10 G7
TEST8 D4
TEST24 AK8 CPU_TEST24 TP13
TEST23 AH8 CPU_TEST23 TP15
TEST22 AJ9 CPU_TEST22 TP17
TEST21 AL8 CPU_TEST21
TEST20 AJ8 CPU_TEST20 TP20
CPU-SK/940AM2/S/15u
RESERVE
RN1 300/8P4R/6/X
R6 300/4/X
R7 300/4
TP3
R14 300/4 DDR18V
VCC12_HT
Other Signal
TMPIN3+
15mil
10mil
TMPIN3-
12mil
10mil
Other Signal
LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.
Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin
Erratum 133, Revision Guide for AMD NPT 0Fh Processors
CPU_TEST26 R27 300/4
CPU_PRESENT_L R30 1K/4
CPU_TEST25_H R31 510/4
CPU_TEST25_L R32 510/4
CPU_TEST21 R33 300/4
Erratum 133, Revision Guide for AMD NPT 0Fh Processors
SOCKET_M2E
INTERNAL MISC
L25 RSVD1
L26 RSVD2
L31 RSVD3
L30 RSVD4
W26 RSVD5
W25 RSVD6
AE27 RSVD7
U24 RSVD8
V24 RSVD9
AE28 RSVD10
Y31 RSVD11
Y30 RSVD12
AG31 RSVD13
V31 RSVD14
W31 RSVD15
AF31 RSVD16
RSVD17 E20
RSVD18 B19
RSVD19 AL4
RSVD20 AK4
RSVD21 AK3
RSVD22 F2
RSVD23 F3
RSVD24 G4
RSVD25 G3
RSVD26 G5
RSVD27 AD25
RSVD28 AE24
RSVD29 AE25
RSVD30 AJ18
RSVD31 AJ20
RSVD32 C18
RSVD33 C20
RSVD34 G24
RSVD35 G25
RSVD36 H25
RSVD37 V29
RSVD38 W30
CPU-SK/940AM2/S/15u
28,29 VCORE_PWOK R34 0/4/SHT/X
23,27,29,30 PWOK R35 0/4/X
R36 100K/4 PWOK_TTL
11 CPU_PWRGD
CPU_PWRGD_1
PWOK_TTL
11 -CPURST
-CPURST_1
U5
74LVC08A/SO14
3VDUAL
BC3 0.1U/6/Y5V/25V/Z
HTSTOP_L 11
PWOK_TTL
HTSTOP_L_1
VCC3
R37 1K/4/X
R38
R39 0/4/X
THERMTRIP_CPU_L
THERMTRIP_CPU_L 11
-CPURST_1 HTSTOP_L_1 CPU_PWRGD_1 -CPURST_C HTSTOP_L_C CPU_PWRGD_C RN29 220/8P4R/6
-CPURST_C HTSTOP_L_C CPU_PWRGD_C RN30 270/8P4R/6
GIGABYTE Technology
Title
CPU CONTROL
Size Custom
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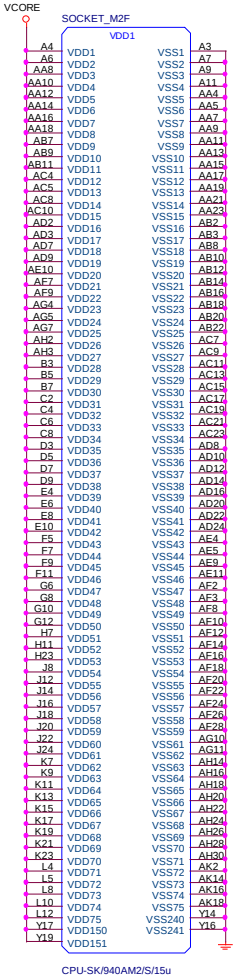
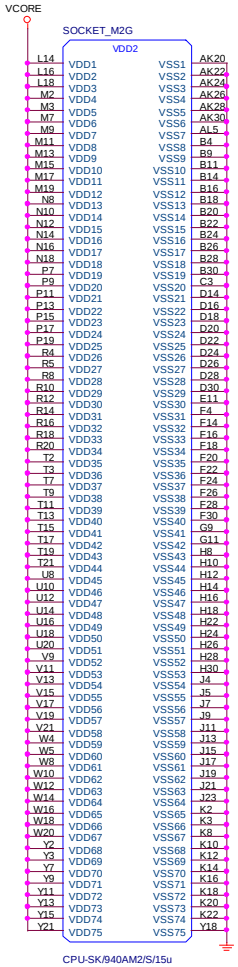
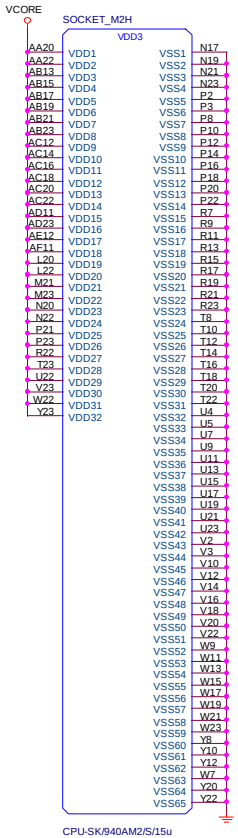
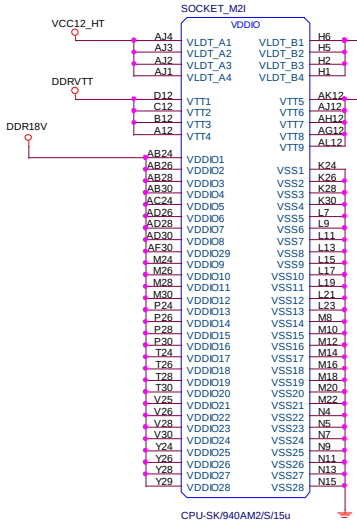
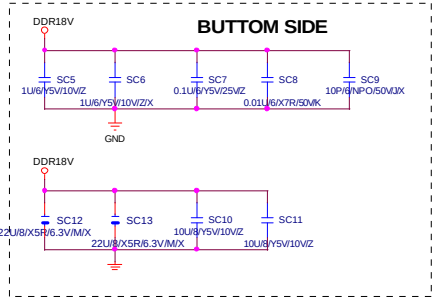
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

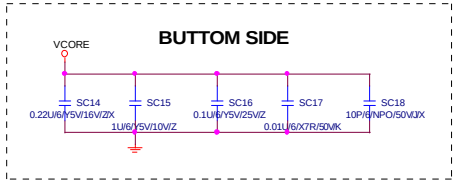


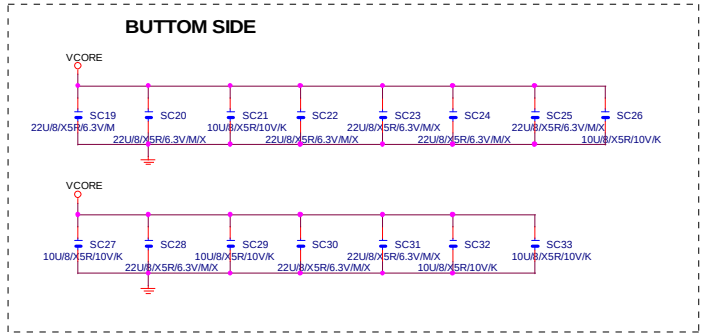


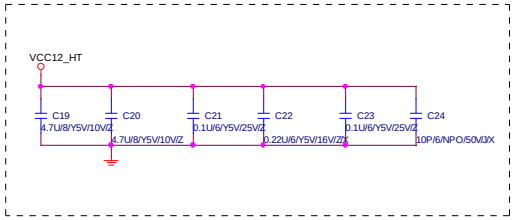


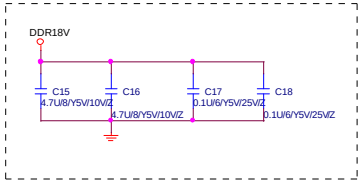


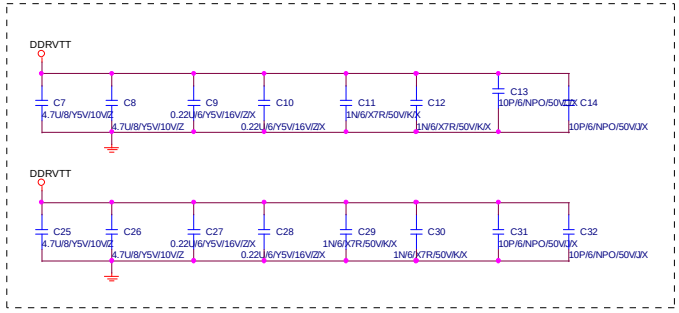












GIGABYTE Technology

Title: CPU POWER & GND

Size: Custom | Document Number: GA-M55SLI-S4 | Rev: 1.0

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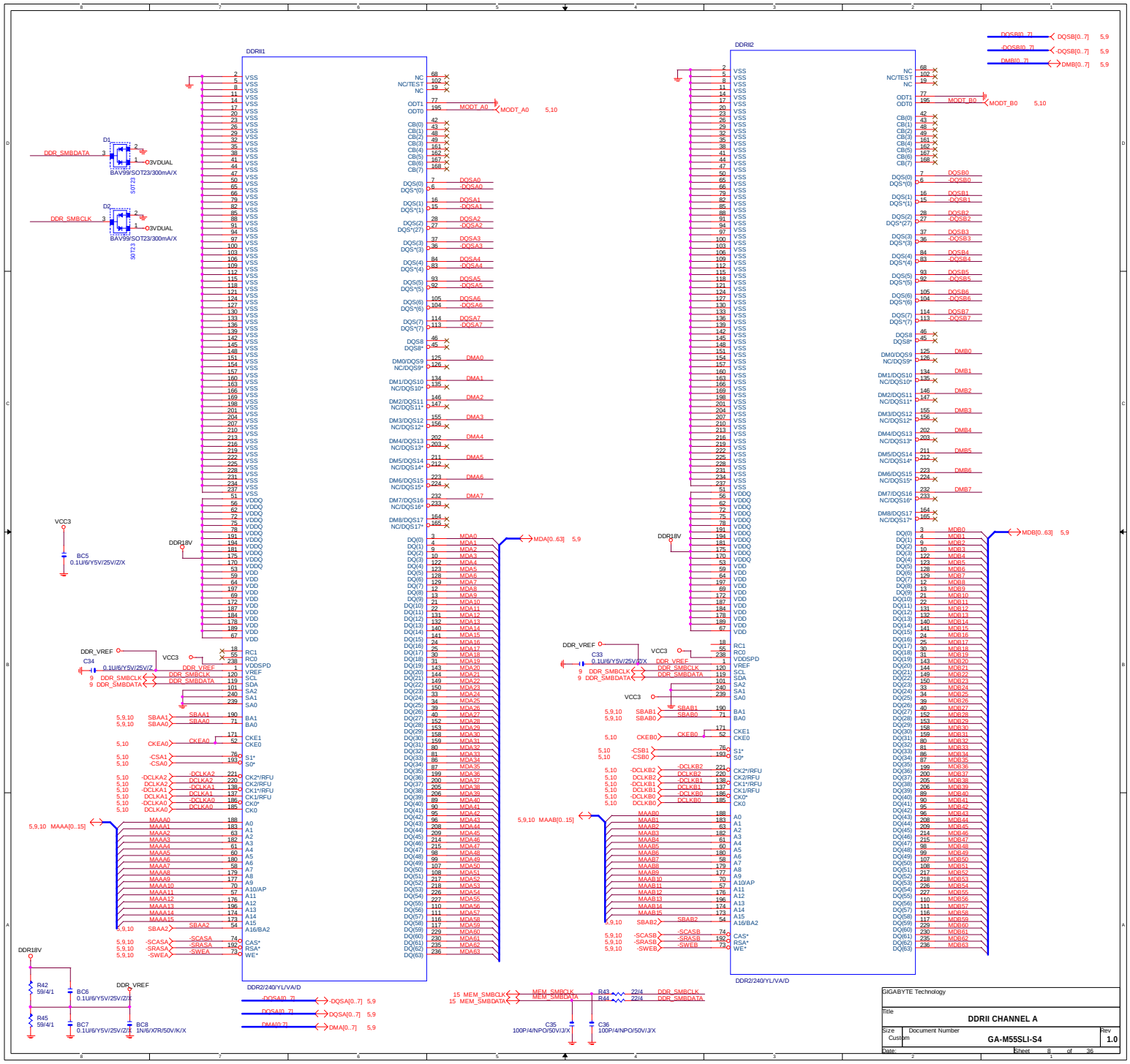
DDRII1
DDRII2
DDR2/240/YL/VA/D
DDR18V
VCC3
DDR_VREF
DDR_SMBDATA
DDR_SMBCLK
BAV99/SOT23/300mA/X
3VDUAL
BC5 0.1U/6/Y5V/25V/Z/X
BC6 0.1U/6/Y5V/25V/Z/X
BC7 0.1U/6/Y5V/25V/Z/X
BC8 1N/6/X7R/50V/K/X
R42 59/4/1
R45 59/4/1
C34 0.1U/6/Y5V/25V/Z/X
C33 0.1U/6/Y5V/25V/Z/X
R43 22/4
R44 22/4
C35 100P/4/NPO/50V/J/X
C36 100P/4/NPO/50V/J/X
MEM_SMBCLK
MEM_SMBDATA
MODT_A0
MODT_B0
MDA[0..63]
MDB[0..63]
DQSA[0..7]
DQSB[0..7]
DMA[0..7]
DMB[0..7]
MAAA[0..15]
MAAB[0..15]
GIGABYTE Technology
DDRII CHANNEL A
GA-M55SLI-S4
Custom
1.0
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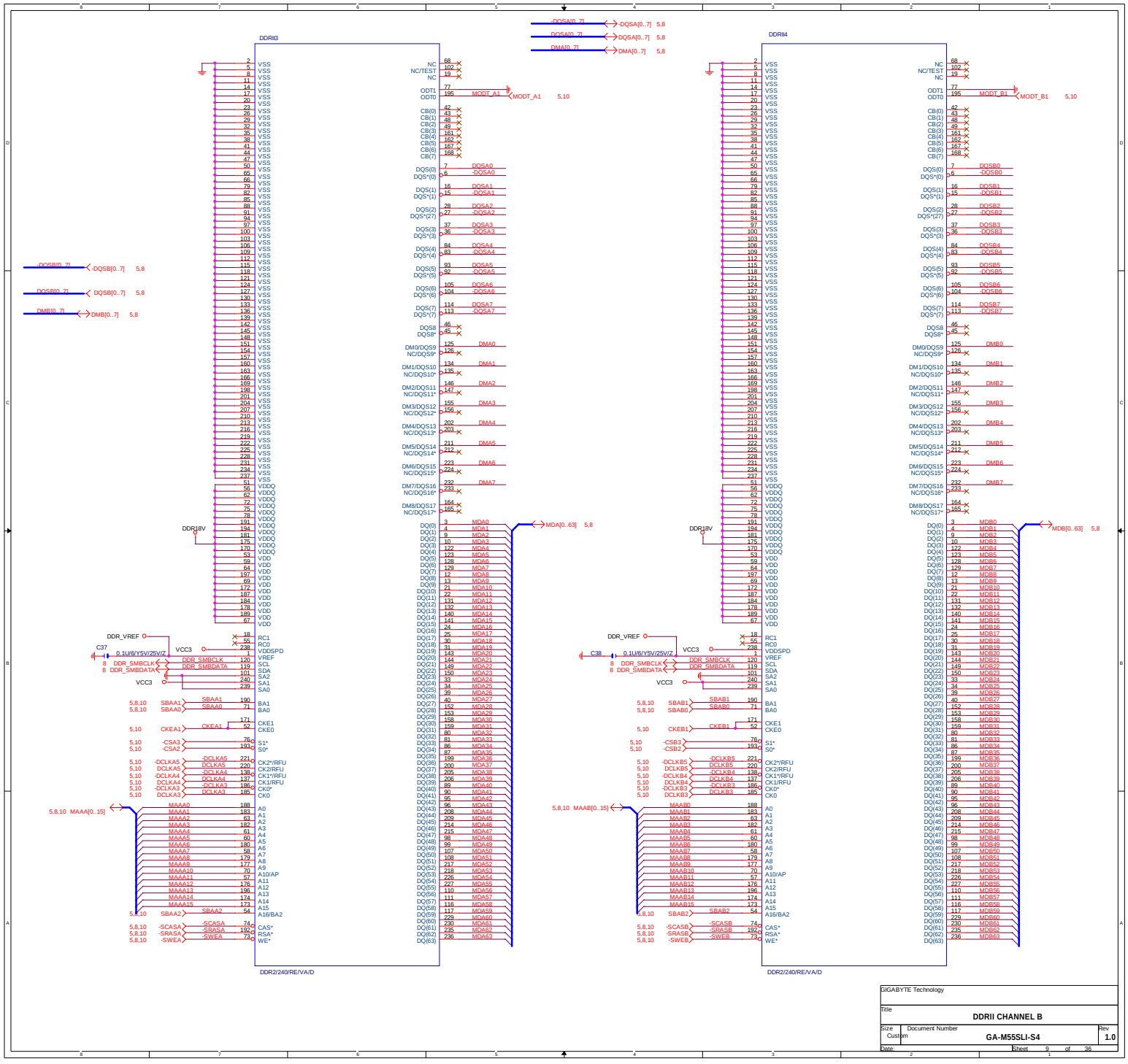

GIGABYTE Technology	
Title	DDRII CHANNEL B
Size: Custom	Document Number: GA-M55SLI-S4
Rev	1.0
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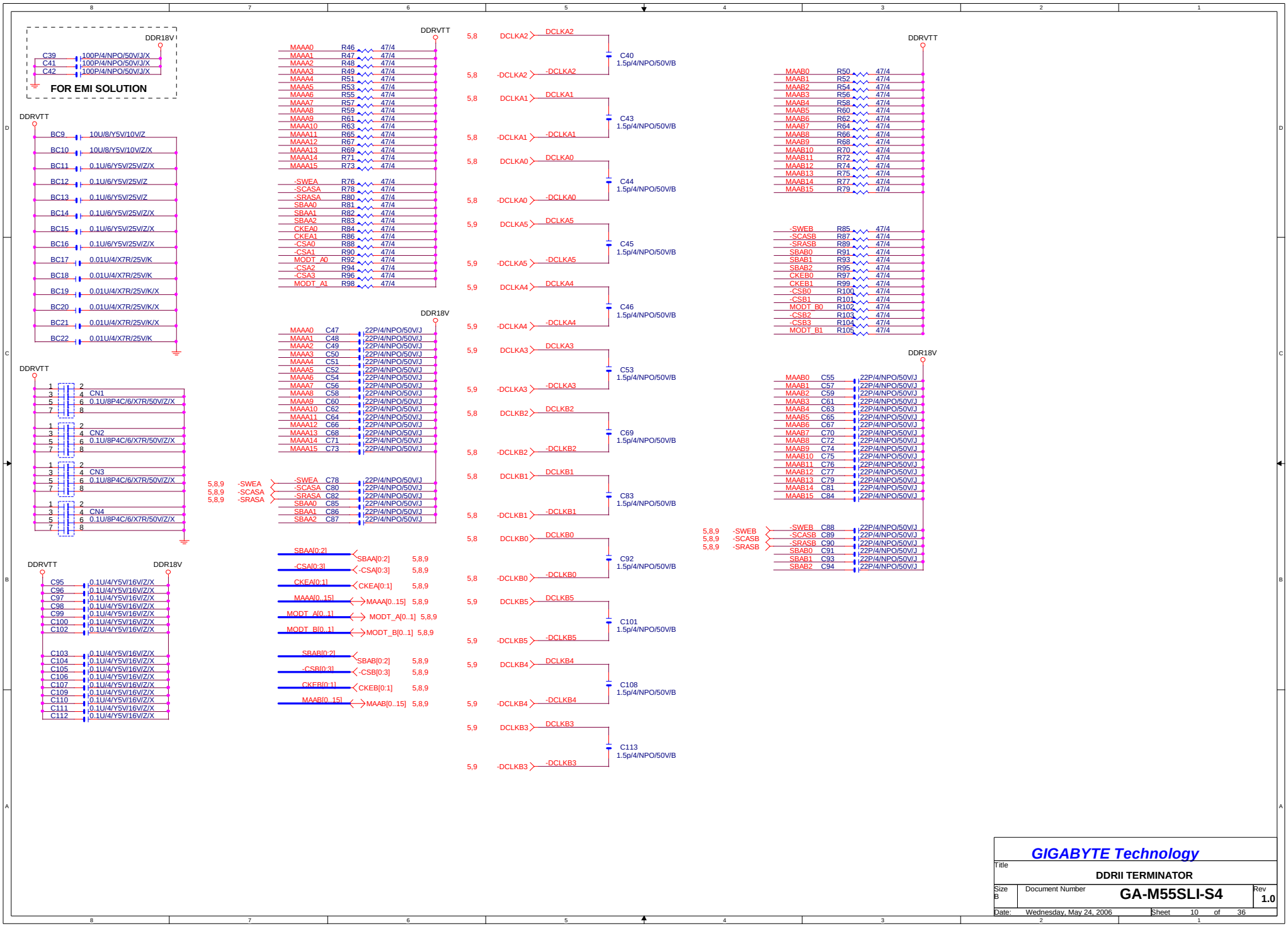
DDR18V
C39 100P/4/NPO/50V/J/X
C41 100P/4/NPO/50V/J/X
C42 100P/4/NPO/50V/J/X
FOR EMI SOLUTION
DDRVTT
BC9 10U/8/Y5V/10V/Z
BC10 10U/8/Y5V/10V/Z/X
BC11 0.1U/6/Y5V/25V/Z/X
BC12 0.1U/6/Y5V/25V/Z
BC13 0.1U/6/Y5V/25V/Z
BC14 0.1U/6/Y5V/25V/Z/X
BC15 0.1U/6/Y5V/25V/Z/X
BC16 0.1U/6/Y5V/25V/Z/X
BC17 0.01U/4/X7R/25V/K
BC18 0.01U/4/X7R/25V/K
BC19 0.01U/4/X7R/25V/K/X
BC20 0.01U/4/X7R/25V/K/X
BC21 0.01U/4/X7R/25V/K/X
BC22 0.01U/4/X7R/25V/K
DDRVTT
CN1 0.1U/8P4C/6/X7R/50V/Z/X
CN2 0.1U/8P4C/6/X7R/50V/Z/X
CN3 0.1U/8P4C/6/X7R/50V/Z/X
CN4 0.1U/8P4C/6/X7R/50V/Z/X
DDRVTT
DDR18V
C95 0.1U/4/Y5V/16V/Z/X
C96 0.1U/4/Y5V/16V/Z/X
C97 0.1U/4/Y5V/16V/Z/X
C98 0.1U/4/Y5V/16V/Z/X
C99 0.1U/4/Y5V/16V/Z/X
C100 0.1U/4/Y5V/16V/Z/X
C102 0.1U/4/Y5V/16V/Z/X
C103 0.1U/4/Y5V/16V/Z/X
C104 0.1U/4/Y5V/16V/Z/X
C105 0.1U/4/Y5V/16V/Z/X
C106 0.1U/4/Y5V/16V/Z/X
C107 0.1U/4/Y5V/16V/Z/X
C109 0.1U/4/Y5V/16V/Z/X
C110 0.1U/4/Y5V/16V/Z/X
C111 0.1U/4/Y5V/16V/Z/X
C112 0.1U/4/Y5V/16V/Z/X
DDRVTT
MAA0 R46 47/4
MAA1 R47 47/4
MAA2 R48 47/4
MAA3 R49 47/4
MAA4 R51 47/4
MAA5 R53 47/4
MAA6 R55 47/4
MAA7 R57 47/4
MAA8 R59 47/4
MAA9 R61 47/4
MAA10 R63 47/4
MAA11 R65 47/4
MAA12 R67 47/4
MAA13 R69 47/4
MAA14 R71 47/4
MAA15 R73 47/4
-SWEA R76 47/4
-SCASA R78 47/4
-SRASA R80 47/4
SBA0 R81 47/4
SBA1 R82 47/4
SBA2 R83 47/4
CKEA0 R84 47/4
CKEA1 R86 47/4
-CSA0 R88 47/4
-CSA1 R90 47/4
MODT_A0 R92 47/4
-CSA2 R94 47/4
-CSA3 R96 47/4
MODT_A1 R98 47/4
DDR18V
MAA0 C47 22P/4/NPO/50V/J
MAA1 C48 22P/4/NPO/50V/J
MAA2 C49 22P/4/NPO/50V/J
MAA3 C50 22P/4/NPO/50V/J
MAA4 C51 22P/4/NPO/50V/J
MAA5 C52 22P/4/NPO/50V/J
MAA6 C54 22P/4/NPO/50V/J
MAA7 C56 22P/4/NPO/50V/J
MAA8 C58 22P/4/NPO/50V/J
MAA9 C60 22P/4/NPO/50V/J
MAA10 C62 22P/4/NPO/50V/J
MAA11 C64 22P/4/NPO/50V/J
MAA12 C66 22P/4/NPO/50V/J
MAA13 C68 22P/4/NPO/50V/J
MAA14 C71 22P/4/NPO/50V/J
MAA15 C73 22P/4/NPO/50V/J
5,8,9 -SWEA -SWEA C78 22P/4/NPO/50V/J
5,8,9 -SCASA -SCASA C80 22P/4/NPO/50V/J
5,8,9 -SRASA -SRASA C82 22P/4/NPO/50V/J
SBA0 C85 22P/4/NPO/50V/J
SBA1 C86 22P/4/NPO/50V/J
SBA2 C87 22P/4/NPO/50V/J
SBA[0:2] SBA[0:2] 5,8,9
-CSA[0:3] -CSA[0:3] 5,8,9
CKEA[0:1] CKEA[0:1] 5,8,9
MAA[0..15] MAA[0..15] 5,8,9
MODT_A[0..1] MODT_A[0..1] 5,8,9
MODT_B[0..1] MODT_B[0..1] 5,8,9
SBAB[0:2] SBAB[0:2] 5,8,9
-CSB[0:3] -CSB[0:3] 5,8,9
CKEB[0:1] CKEB[0:1] 5,8,9
MAAB[0..15] MAAB[0..15] 5,8,9
5,8 DCLKA2 DCLKA2
C40 1.5p/4/NPO/50V/B
5,8 -DCLKA2 -DCLKA2
5,8 DCLKA1 DCLKA1
C43 1.5p/4/NPO/50V/B
5,8 -DCLKA1 -DCLKA1
5,8 DCLKA0 DCLKA0
C44 1.5p/4/NPO/50V/B
5,8 -DCLKA0 -DCLKA0
5,9 DCLKA5 DCLKA5
C45 1.5p/4/NPO/50V/B
5,9 -DCLKA5 -DCLKA5
5,9 DCLKA4 DCLKA4
C46 1.5p/4/NPO/50V/B
5,9 -DCLKA4 -DCLKA4
5,9 DCLKA3 DCLKA3
C53 1.5p/4/NPO/50V/B
5,9 -DCLKA3 -DCLKA3
5,8 DCLKB2 DCLKB2
C69 1.5p/4/NPO/50V/B
5,8 -DCLKB2 -DCLKB2
5,8 DCLKB1 DCLKB1
C83 1.5p/4/NPO/50V/B
5,8 -DCLKB1 -DCLKB1
5,8 DCLKB0 DCLKB0
C92 1.5p/4/NPO/50V/B
5,8 -DCLKB0 -DCLKB0
5,9 DCLKB5 DCLKB5
C101 1.5p/4/NPO/50V/B
5,9 -DCLKB5 -DCLKB5
5,9 DCLKB4 DCLKB4
C108 1.5p/4/NPO/50V/B
5,9 -DCLKB4 -DCLKB4
5,9 DCLKB3 DCLKB3
C113 1.5p/4/NPO/50V/B
5,9 -DCLKB3 -DCLKB3
DDRVTT
MAAB0 R50 47/4
MAAB1 R52 47/4
MAAB2 R54 47/4
MAAB3 R56 47/4
MAAB4 R58 47/4
MAAB5 R60 47/4
MAAB6 R62 47/4
MAAB7 R64 47/4
MAAB8 R66 47/4
MAAB9 R68 47/4
MAAB10 R70 47/4
MAAB11 R72 47/4
MAAB12 R74 47/4
MAAB13 R75 47/4
MAAB14 R77 47/4
MAAB15 R79 47/4
-SWEB R85 47/4
-SCASB R87 47/4
-SRASB R89 47/4
SBAB0 R91 47/4
SBAB1 R93 47/4
SBAB2 R95 47/4
CKEB0 R97 47/4
CKEB1 R99 47/4
-CSB0 R100 47/4
-CSB1 R101 47/4
MODT_B0 R102 47/4
-CSB2 R103 47/4
-CSB3 R104 47/4
MODT_B1 R105 47/4
DDR18V
MAAB0 C55 22P/4/NPO/50V/J
MAAB1 C57 22P/4/NPO/50V/J
MAAB2 C59 22P/4/NPO/50V/J
MAAB3 C61 22P/4/NPO/50V/J
MAAB4 C63 22P/4/NPO/50V/J
MAAB5 C65 22P/4/NPO/50V/J
MAAB6 C67 22P/4/NPO/50V/J
MAAB7 C70 22P/4/NPO/50V/J
MAAB8 C72 22P/4/NPO/50V/J
MAAB9 C74 22P/4/NPO/50V/J
MAAB10 C75 22P/4/NPO/50V/J
MAAB11 C76 22P/4/NPO/50V/J
MAAB12 C77 22P/4/NPO/50V/J
MAAB13 C79 22P/4/NPO/50V/J
MAAB14 C81 22P/4/NPO/50V/J
MAAB15 C84 22P/4/NPO/50V/J
5,8,9 -SWEB -SWEB C88 22P/4/NPO/50V/J
5,8,9 -SCASB -SCASB C89 22P/4/NPO/50V/J
5,8,9 -SRASB -SRASB C90 22P/4/NPO/50V/J
SBAB0 C91 22P/4/NPO/50V/J
SBAB1 C93 22P/4/NPO/50V/J
SBAB2 C94 22P/4/NPO/50V/J
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Title
DDRII TERMINATOR
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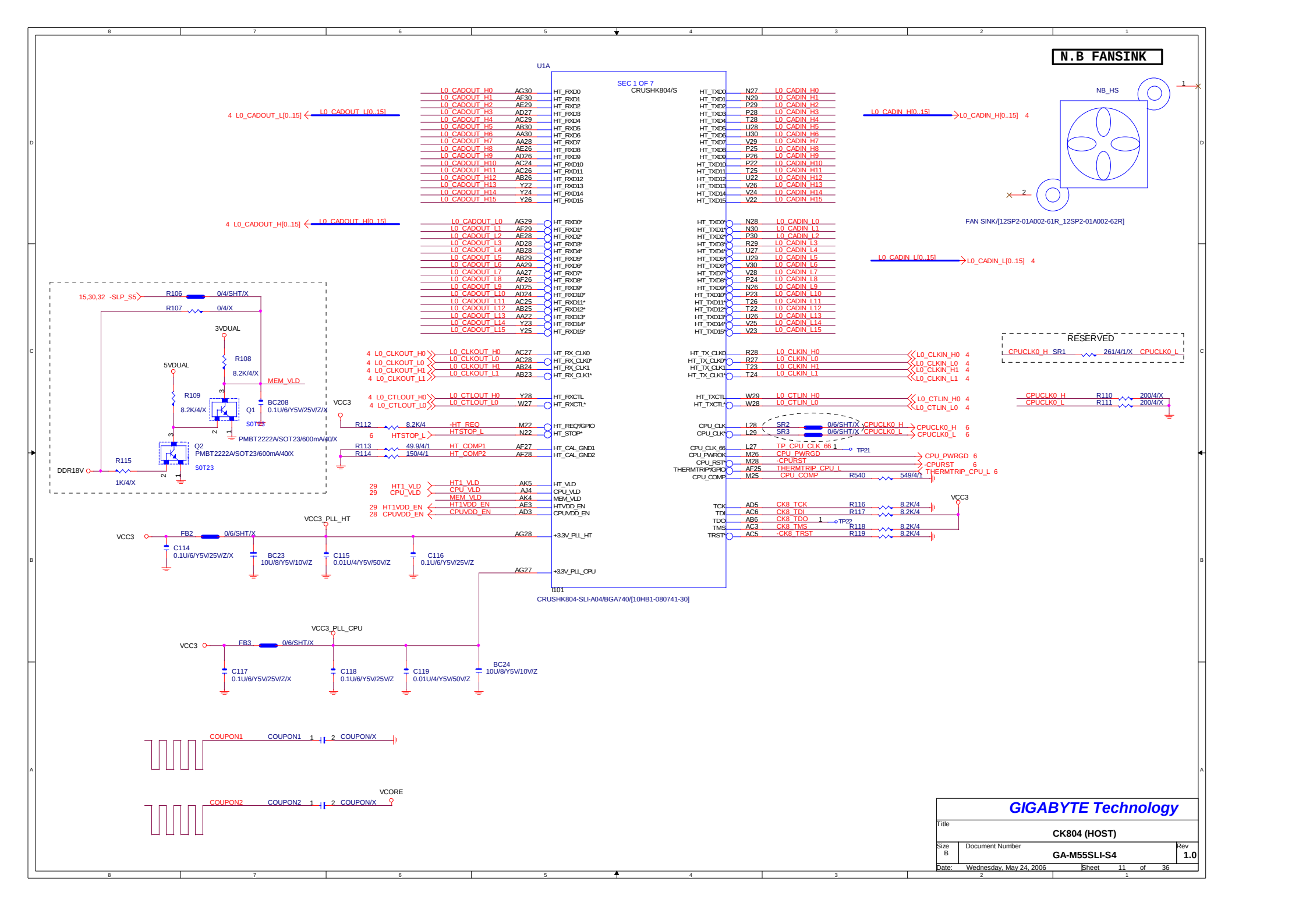
N.B FANSINK



Title	CK804 (HOST)
Size	B
Document Number	GA-M55SLI-S4
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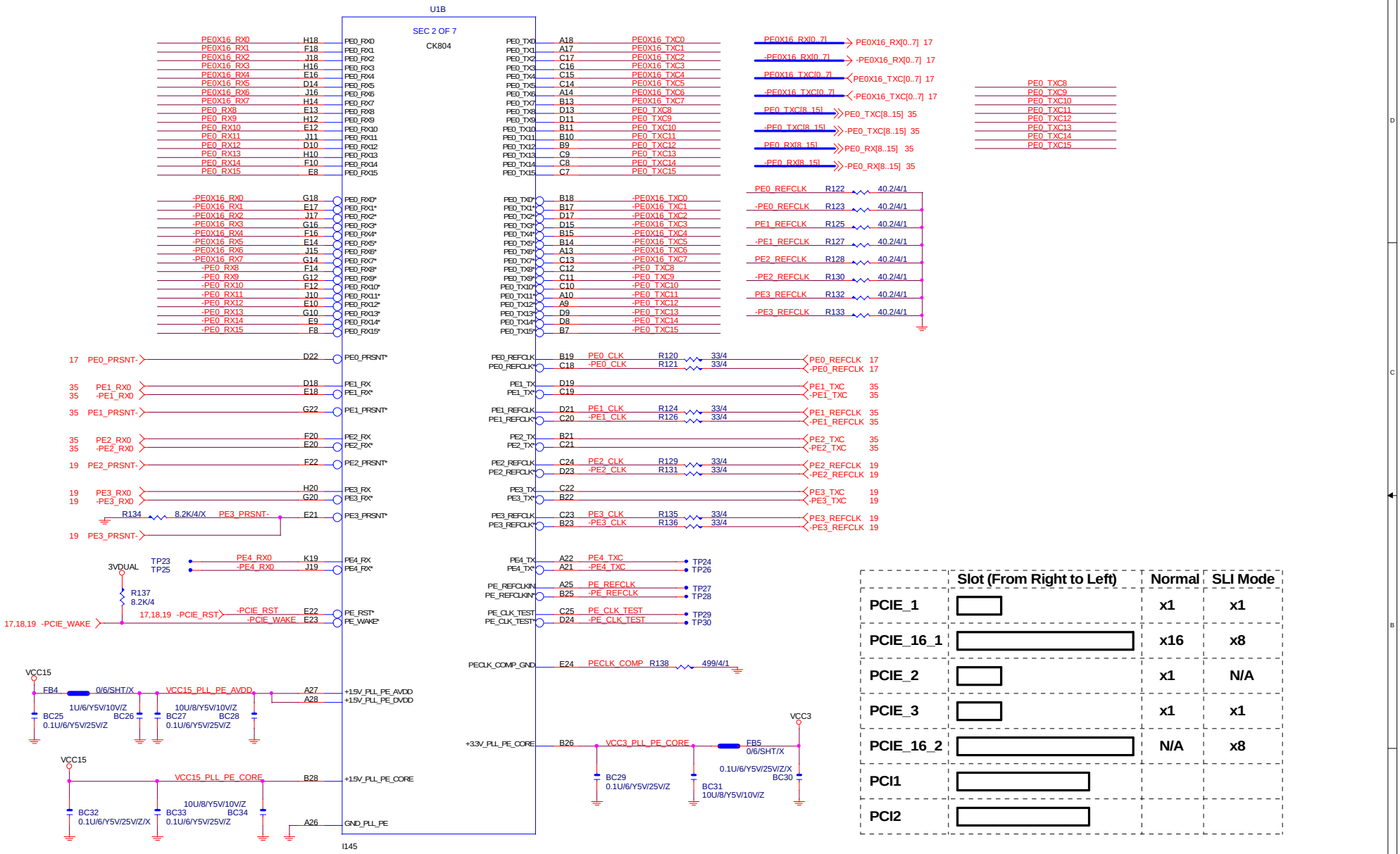
GIGABYTE Technology



	Slot (From Right to Left)	Normal	SLI Mode
PCIE_1		x1	x1
PCIE_16_1		x16	x8
PCIE_2		x1	N/A
PCIE_3		x1	x1
PCIE_16_2		N/A	x8
PCI1			
PCI2			

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Title	CK804 (PCI EXPRESS)	
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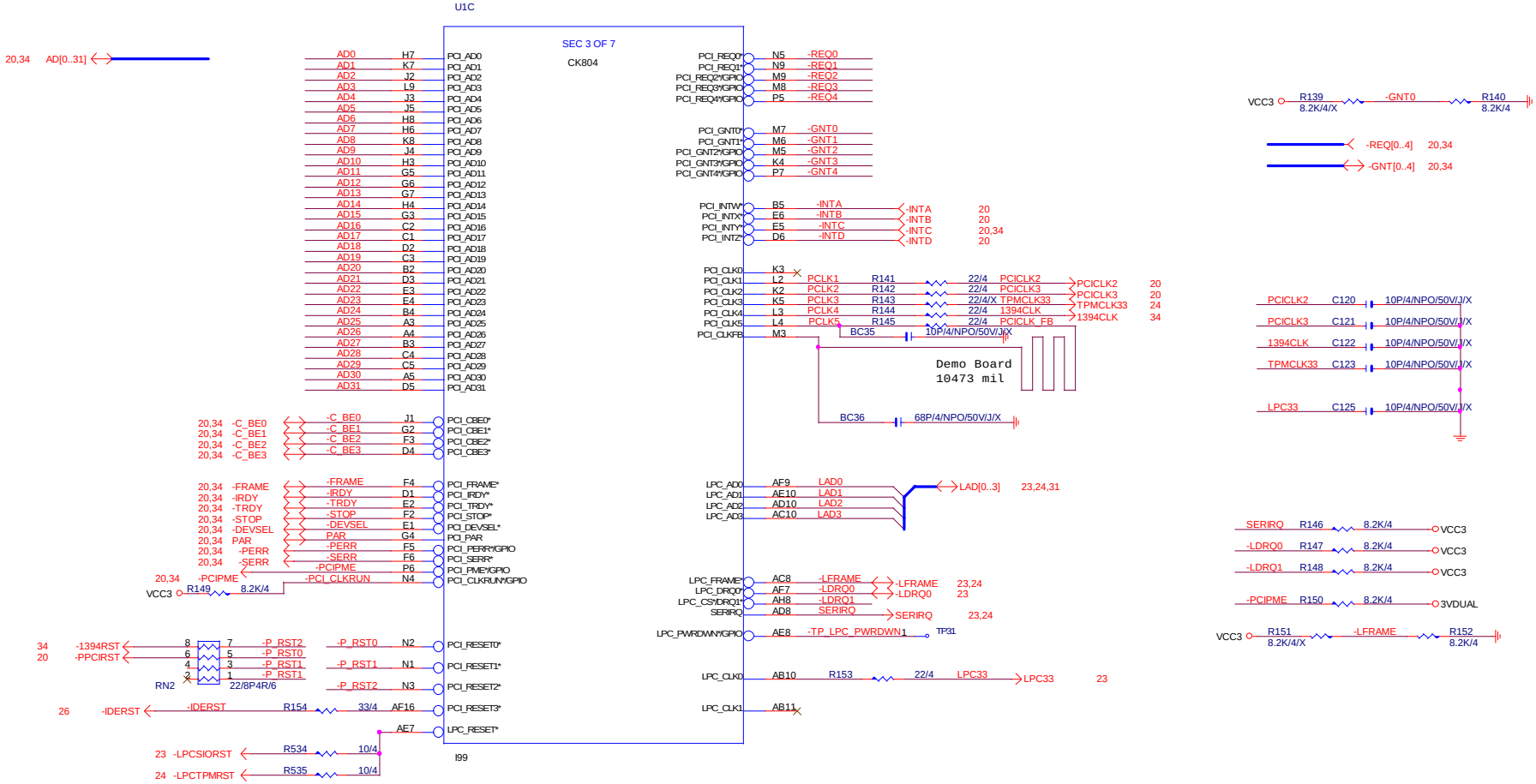

GIGABYTE Technology		
Title: CK804 (PCI BUS,LPC,CLOCK)		
Size: B	Document Number: GA-M55SLI-S4	Rev: 1.0
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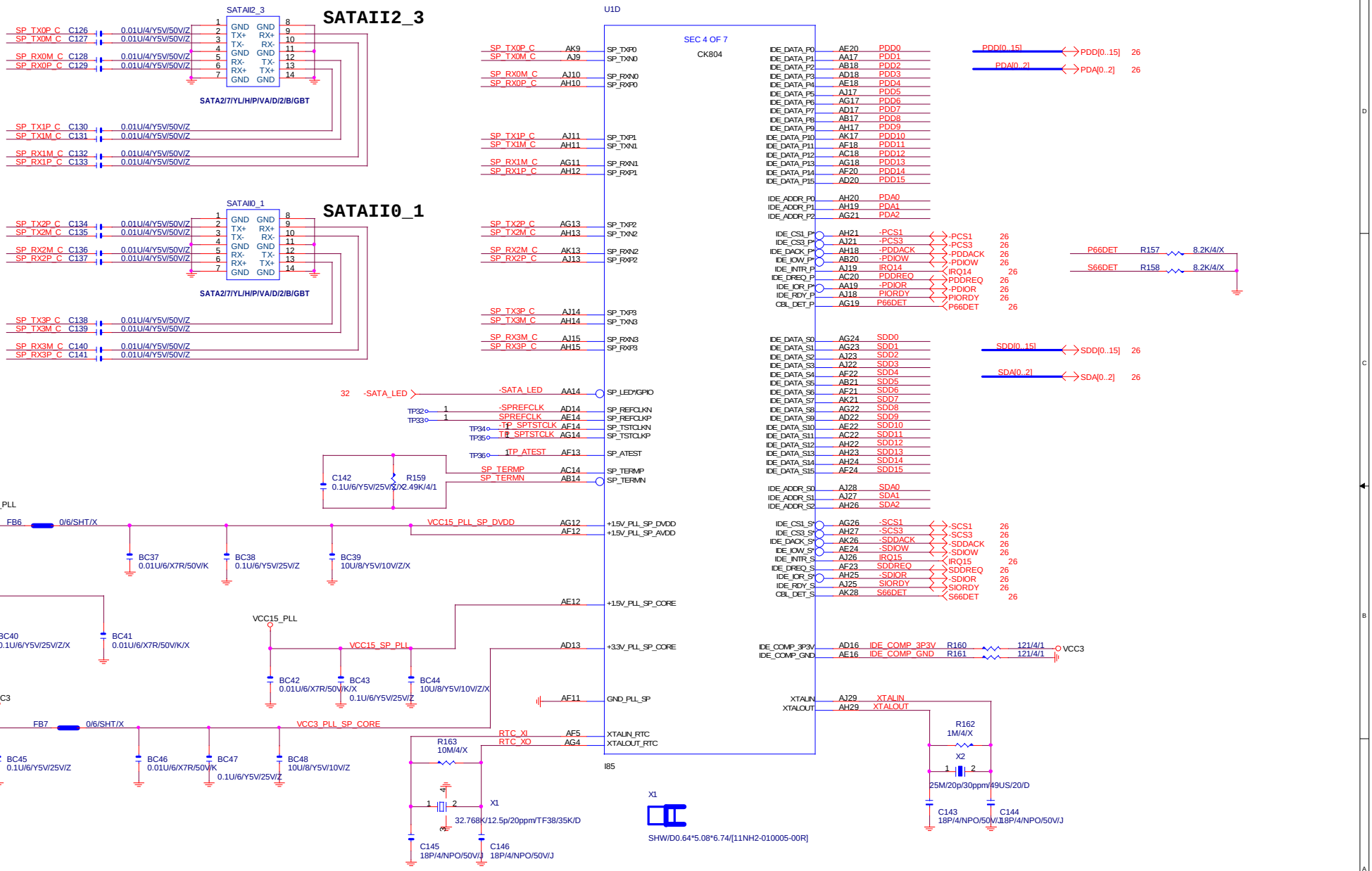

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Title	CK804 (SATA,IDE)	
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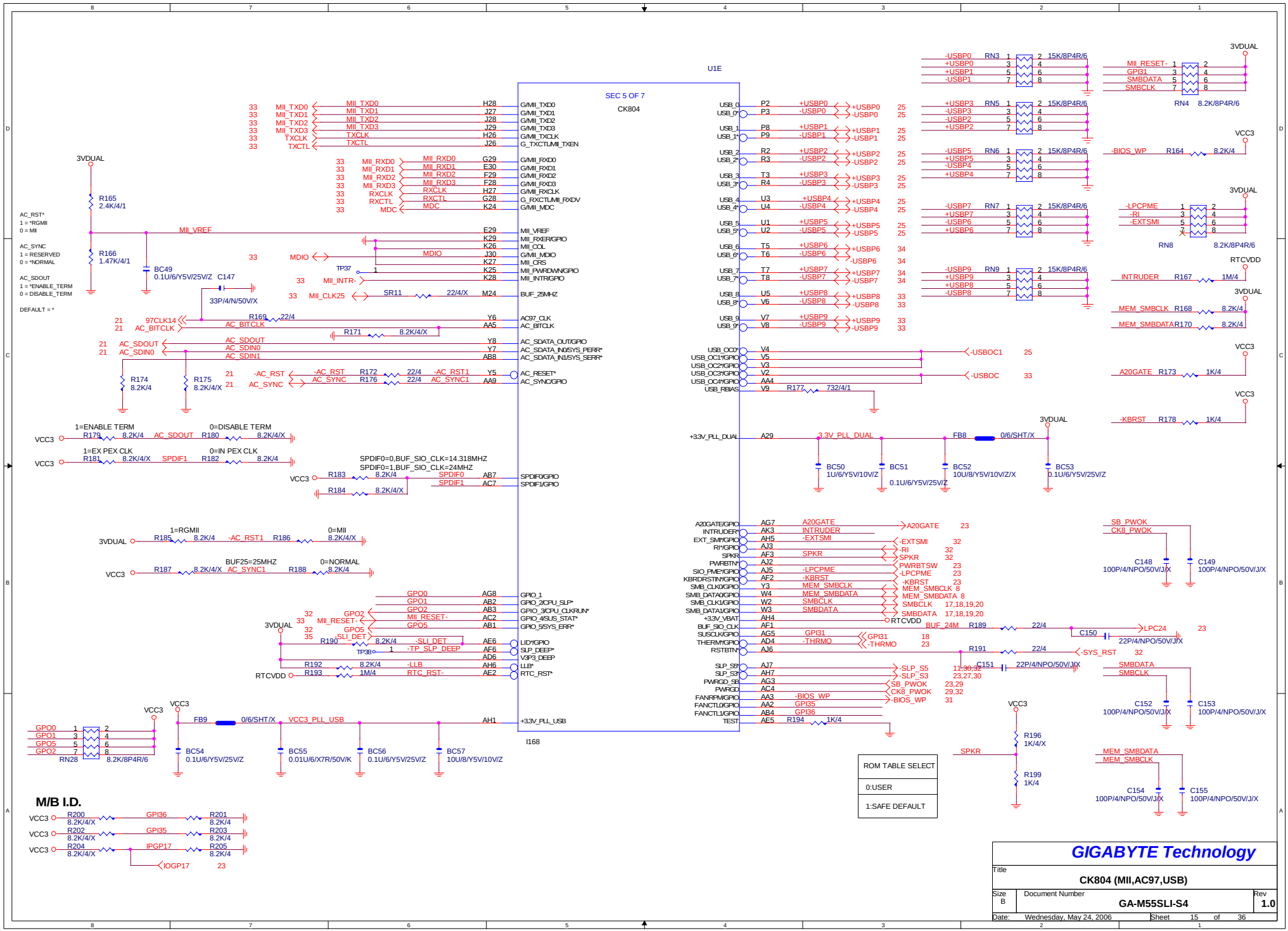
U1E
SEC 5 OF 7
CK804
I168
3VDUAL
VCC3
RTCVDD
MII_VREF
MII_TXD0
MII_TXD1
MII_TXD2
MII_TXD3
TXCLK
TXCTL
MII_RXD0
MII_RXD1
MII_RXD2
MII_RXD3
RXCLK
RXCTL
MDC
MDIO
MII_INTR-
MII_CLK25
AC_BITCLK
AC_SDOUT
AC_SDIN0
AC_SDIN1
-AC_RST
AC_SYNC
SPDIF0
SPDIF1
-SLI_DET
-TP_SLP_DEEP
-LLB
RTC_RST-
GPO0
GPO1
GPO2
MII_RESET-
GPO5
-BIOS_WP
GPI36
GPI35
IPGP17
IOGP17
3.3V_PLL_DUAL
VCC3_PLL_USB
A20GATE
INTRUDER
-EXTSMI
-RI
SPKR
PWRBTN
-LPCPME
-KBRST
MEM_SMBCLK
MEM_SMBDATA
SMBCLK
SMBDATA
-THRMO
GPI31
-SLP_S5
-SLP_S3
SB_PWOK
CK8_PWOK
-SYS_RST
LPC24
-USBOC
-USBOC1
-USBP0
+USBP0
-USBP1
+USBP1
-USBP2
+USBP2
-USBP3
+USBP3
-USBP4
+USBP4
-USBP5
+USBP5
-USBP6
+USBP6
-USBP7
+USBP7
-USBP8
+USBP8
-USBP9
+USBP9
ROM TABLE SELECT
0:USER
1:SAFE DEFAULT
M/B I.D.
GIGABYTE Technology
CK804 (MII,AC97,USB)
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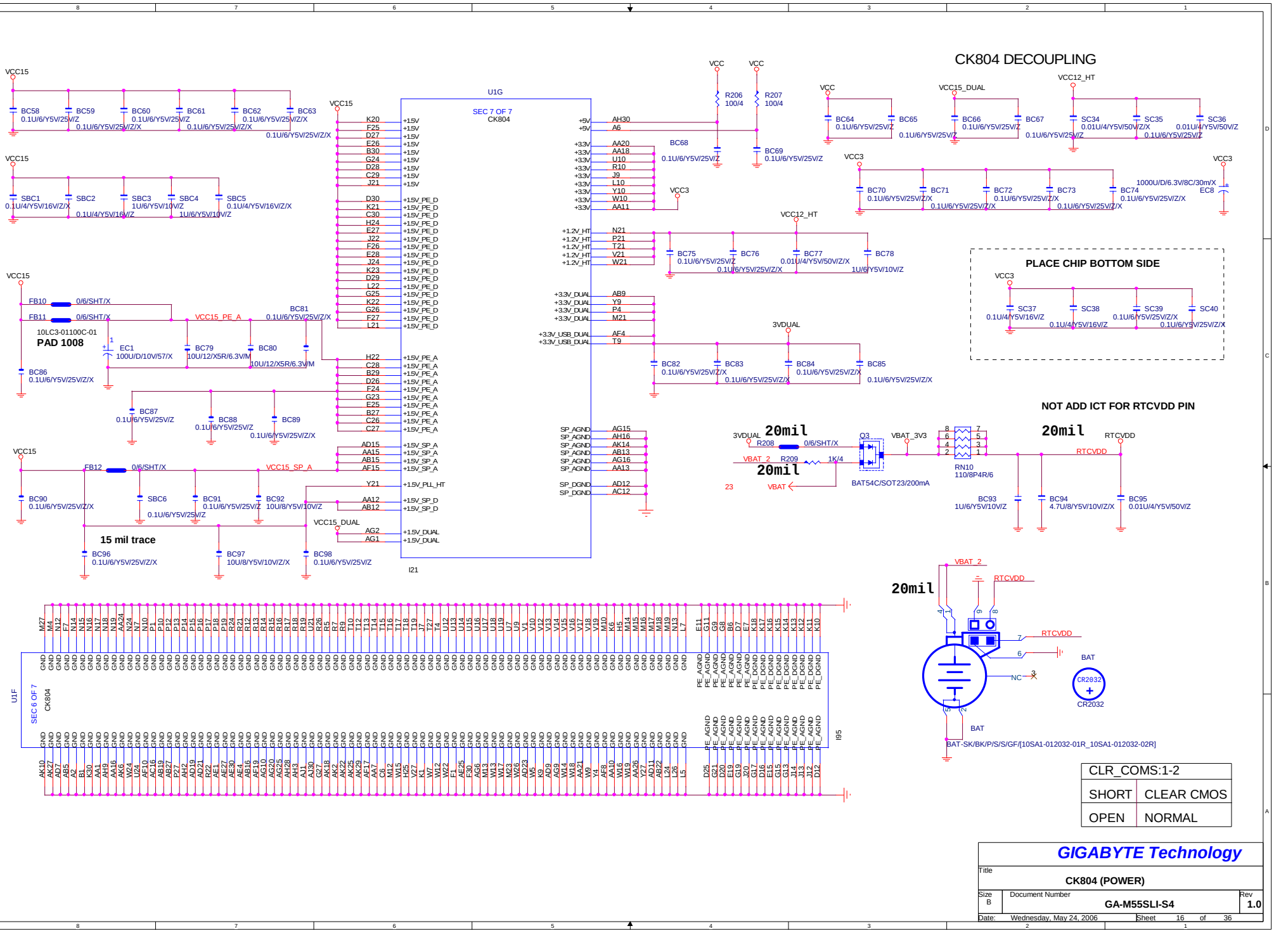
CK804 DECOUPLING
U1G
SEC 7 OF 7
CK804
I21
PLACE CHIP BOTTOM SIDE
NOT ADD ICT FOR RTCVDD PIN
PAD 1008
10LC3-01100C-01
15 mil trace
20mil
20mil
20mil
U1F
SEC 6 OF 7
CK804
I95
BAT54C/SOT23/200mA
RN10
110/8P4R6
BAT-SK/BK/P/S/S/GF/[10SA1-012032-01R_10SA1-012032-02R]
CR2032
CLR_COMS:1-2
SHORT
CLEAR CMOS
OPEN
NORMAL
GIGABYTE Technology
Title
CK804 (POWER)
Size
B
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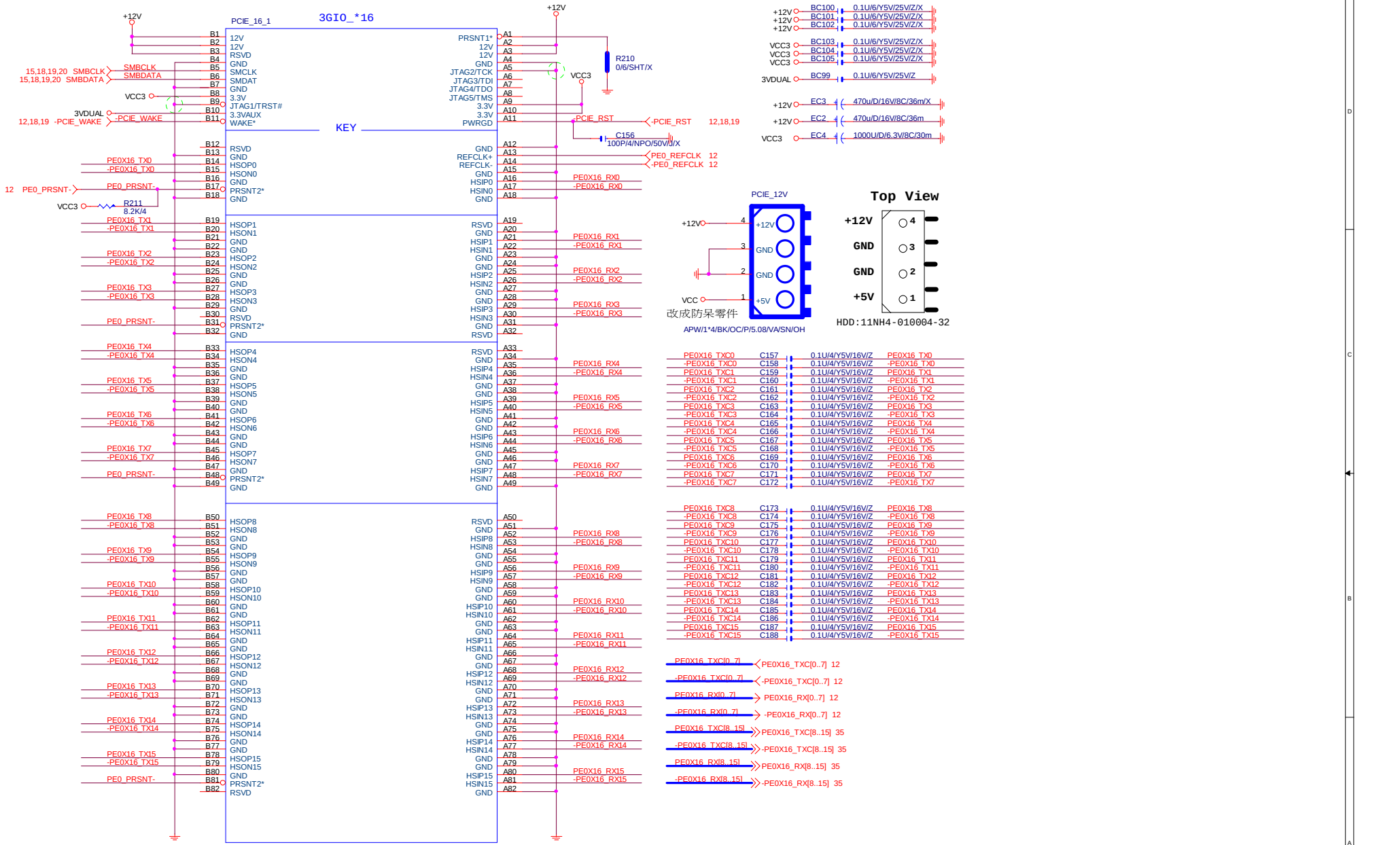

Title	PCI EXPRESS X 16
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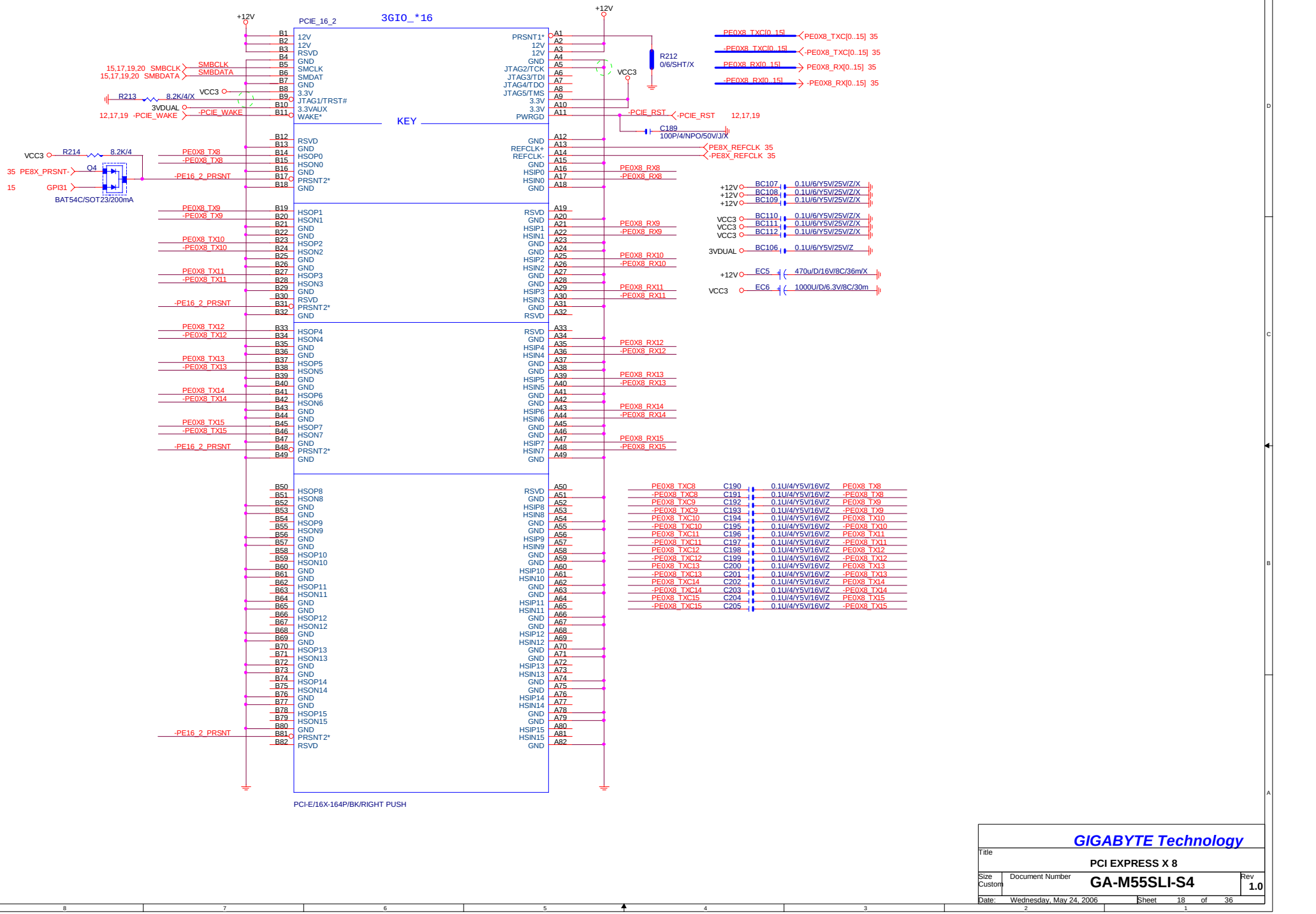
PCIE_16_2
3GIO_*16
KEY
PCI-E/16X-164P/BK/RIGHT PUSH
BAT54C/SOT23/200mA
R212 0/6/SHT/X
C189 100P/4/NPO/50V/J/X
R213 8.2K/4/X
R214 8.2K/4
Q4
BC107 BC108 BC109 BC110 BC111 BC112 BC106 0.1U/6/Y5V/25V/Z/X
EC5 470u/D/16V/8C/36m/X
EC6 1000U/D/6.3V/8C/30m
C190 C191 C192 C193 C194 C195 C196 C197 C198 C199 C200 C201 C202 C203 C204 C205 0.1U/4/Y5V/16V/Z
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PCI EXPRESS X 8
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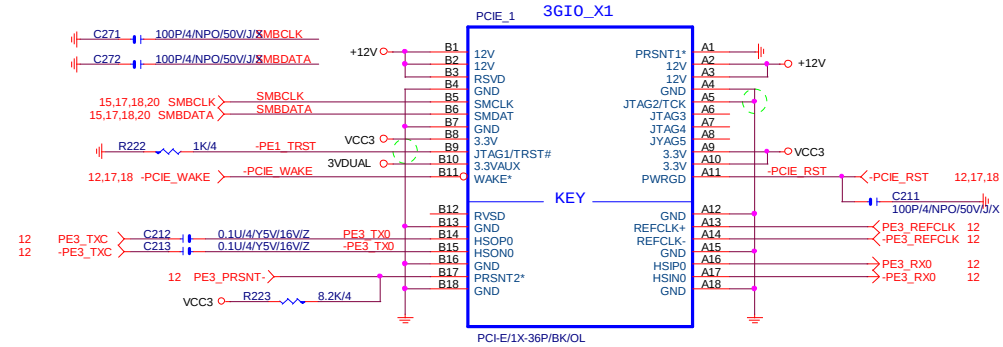

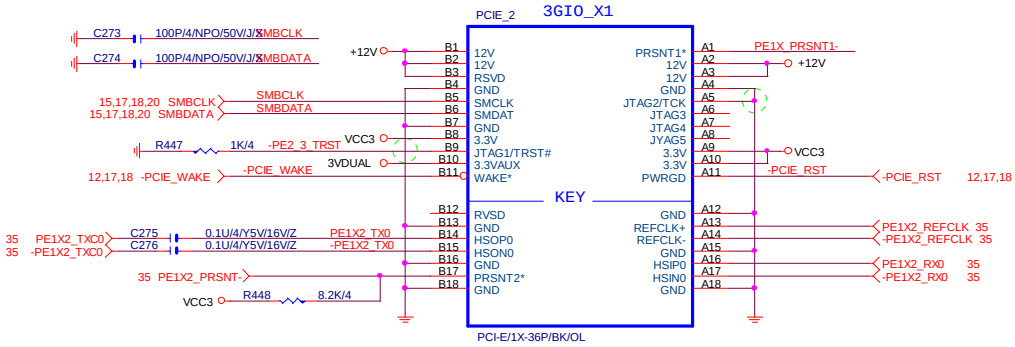

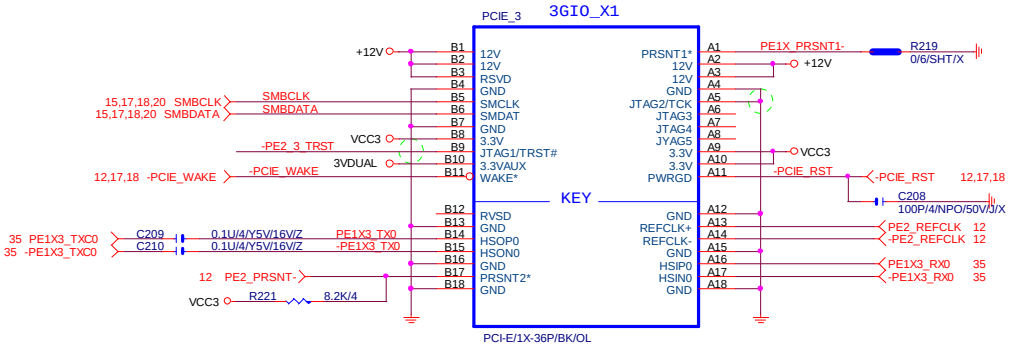

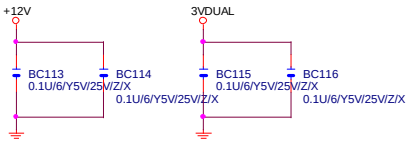

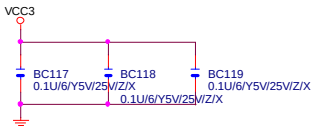

Normal Mode

Right to Left	PRSNT#	LANE(Tx/Rx)	REFCLK
PCIE_1	PE3_PRSNT#	PE3	PE3_REFCLK
PCIE_16_1	PE0_PRSNT#	PE0[0..15]	PE0_REFCLK
PCIE_2	PE1_PRSNT#	PE1	PE1_REFCLK
PCIE_3	PE2_PRSNT#	PE2	PE2_REFCLK
PCIE_16_2	---	---	---

SLI Mode

Right to Left	PRSNT#	LANE(Tx/Rx)	REFCLK
PCIE_1	PE3_PRSNT#	PE3	PE3_REFCLK
PCIE_16_1	PE0_PRSNT#	PE0[0..7]	PE0_REFCLK
PCIE_2	---	---	---
PCIE_3	PE2_PRSNT#	PE1	PE2_REFCLK
PCIE_16_2	PE1_PRSNT#	PE0[8..15]	PE1_REFCLK

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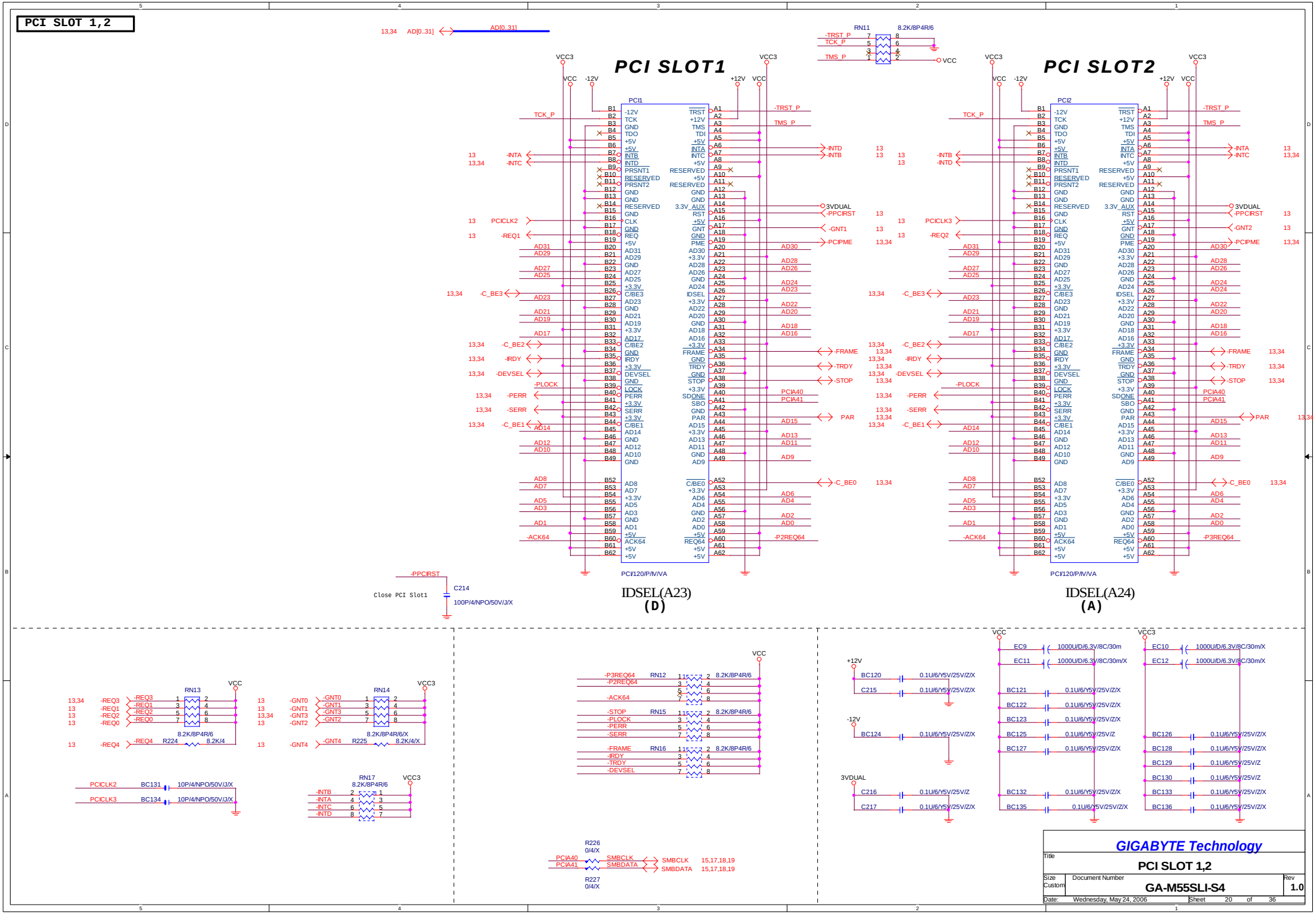
PCI SLOT 1,2


PCI SLOT1
PCI SLOT2
IDSEL(A23)
(D)
IDSEL(A24)
(A)
PCI1
PCI2
PCI/120/P/N/VA
RN11
8.2K/8P4R/6
RN13
RN14
RN15
RN16
RN17
8.2K/8P4R/6
8.2K/8P4R/6/X
R224
R225
R226
R227
0/4/X
C214
100P/4/NPO/50V/J/X
Close PCI Slot1
BC131
BC134
10P/4/NPO/50V/J/X
EC9
EC10
EC11
EC12
1000U/D/6.3V/8C/30m
1000U/D/6.3V/8C/30m/X
BC120
C215
BC121
BC122
BC123
BC124
BC125
BC126
BC127
BC128
BC129
BC130
BC132
BC133
BC135
BC136
C216
C217
0.1U/6/Y5V/25V/Z/X
0.1U/6/Y5V/25V/Z
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Title
PCI SLOT 1,2
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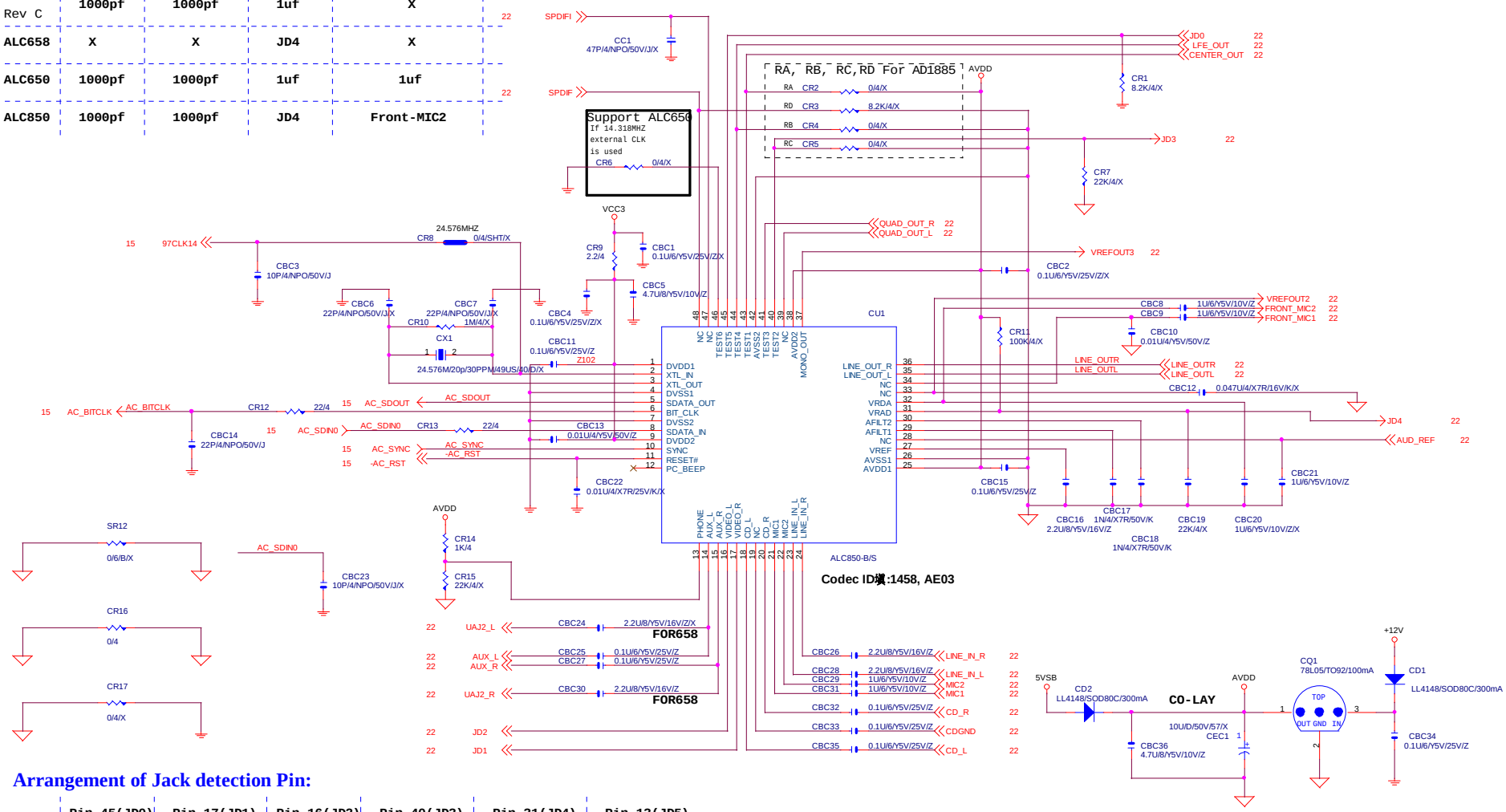
Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2



Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT Exernal pull high is needed	for LINE-IN Exernal pull high is needed	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out

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Title	ALC850	
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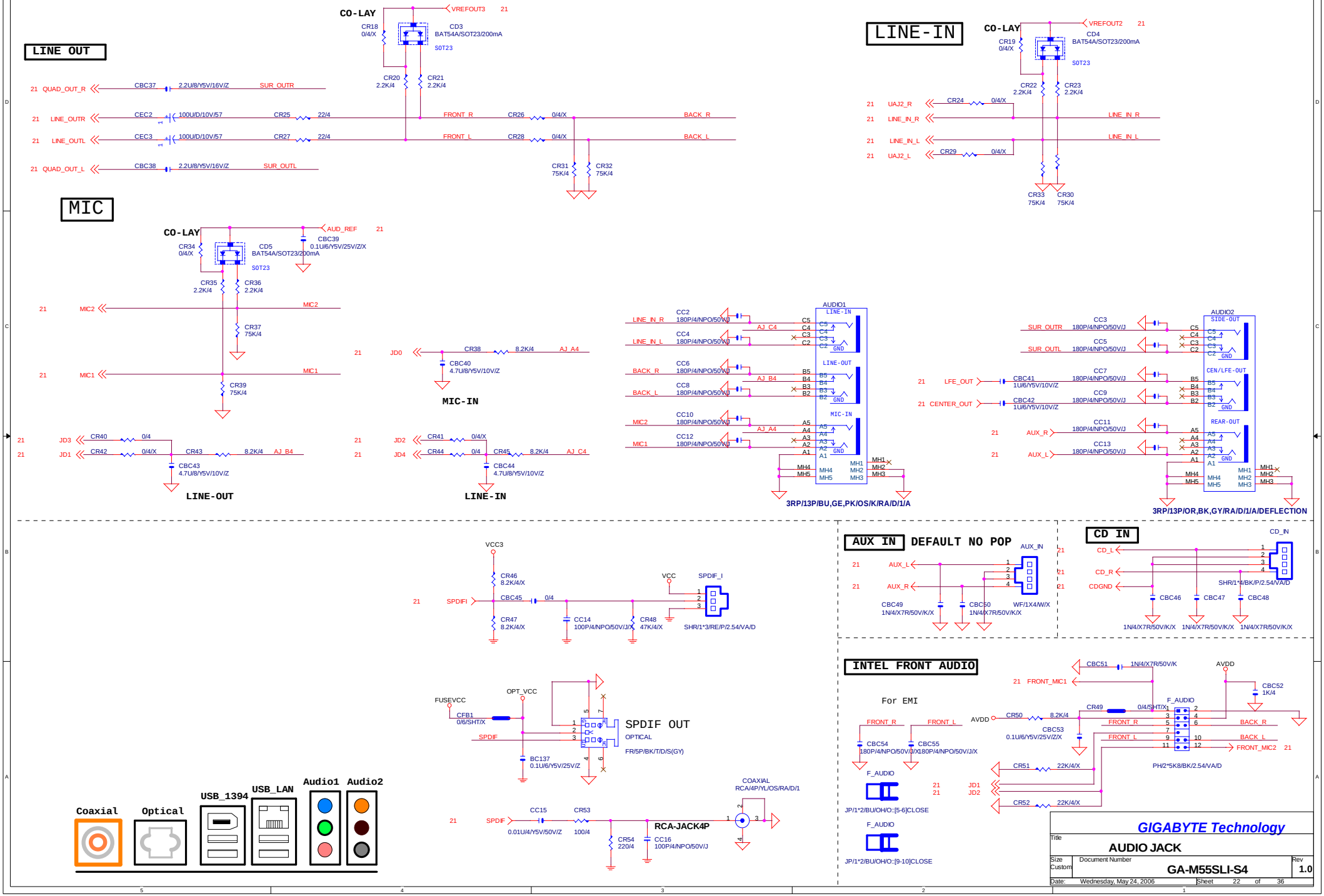
LINE OUT
CO-LAY
VREFOUT3
CR18 0/4/X
CD3 BAT54A/SOT23/200mA
SOT23
CR20 2.2K/4
CR21 2.2K/4
21 QUAD_OUT_R
CBC37 2.2U/8/Y5V/16V/Z
SUR_OUTR
21 LINE_OUTR
CEC2 100U/D/10V/57
CR25 22/4
FRONT_R
CR26 0/4/X
BACK_R
21 LINE_OUTL
CEC3 100U/D/10V/57
CR27 22/4
FRONT_L
CR28 0/4/X
BACK_L
21 QUAD_OUT_L
CBC38 2.2U/8/Y5V/16V/Z
SUR_OUTL
CR31 75K/4
CR32 75K/4
LINE-IN
CO-LAY
VREFOUT2
CR19 0/4/X
CD4 BAT54A/SOT23/200mA
SOT23
CR22 2.2K/4
CR23 2.2K/4
21 UAJ2_R
CR24 0/4/X
21 LINE_IN_R
LINE_IN_R
21 LINE_IN_L
LINE_IN_L
21 UAJ2_L
CR29 0/4/X
CR33 75K/4
CR30 75K/4
MIC
CO-LAY
AUD_REF
CBC39 0.1U/6/Y5V/25V/Z/X
CR34 0/4/X
CD5 BAT54A/SOT23/200mA
SOT23
CR35 2.2K/4
CR36 2.2K/4
21 MIC2
MIC2
CR37 75K/4
21 MIC1
MIC1
CR39 75K/4
21 JD3
CR40 0/4
21 JD1
CR42 0/4/X
CR43 8.2K/4
AJ_B4
CBC43 4.7U/8/Y5V/10V/Z
LINE-OUT
21 JD0
CR38 8.2K/4
AJ_A4
CBC40 4.7U/8/Y5V/10V/Z
MIC-IN
21 JD2
CR41 0/4/X
21 JD4
CR44 0/4
CR45 8.2K/4
AJ_C4
CBC44 4.7U/8/Y5V/10V/Z
LINE-IN
LINE_IN_R
CC2 180P/4/NPO/50V/J
AJ_C4
LINE_IN_L
CC4 180P/4/NPO/50V/J
BACK_R
CC6 180P/4/NPO/50V/J
AJ_B4
BACK_L
CC8 180P/4/NPO/50V/J
MIC2
CC10 180P/4/NPO/50V/J
AJ_A4
MIC1
CC12 180P/4/NPO/50V/J
AUDIO1
LINE-IN
LINE-OUT
MIC-IN
GND
MH1 MH2 MH3 MH4 MH5
3RP/13P/BU,GE,PK/OS/K/RA/D/1/A
SUR_OUTR
CC3 180P/4/NPO/50V/J
SUR_OUTL
CC5 180P/4/NPO/50V/J
21 LFE_OUT
CBC41 1U/6/Y5V/10V/Z
CC7 180P/4/NPO/50V/J
21 CENTER_OUT
CBC42 1U/6/Y5V/10V/Z
CC9 180P/4/NPO/50V/J
21 AUX_R
CC11 180P/4/NPO/50V/J
21 AUX_L
CC13 180P/4/NPO/50V/J
AUDIO2
SIDE-OUT
CEN/LFE-OUT
REAR-OUT
3RP/13P/OR,BK,GY/RA/D/1/A/DEFLECTION
VCC3
CR46 8.2K/4/X
21 SPDIFI
CBC45 0/4
CR47 8.2K/4/X
CC14 100P/4/NPO/50V/J/X
CR48 47K/4/X
VCC
SPDIF_I
SHR/1*3/RE/P/2.54/VA/D
AUX IN DEFAULT NO POP
AUX_IN
21 AUX_L
21 AUX_R
CBC49 1N/4/X7R/50V/K/X
CBC50 1N/4/X7R/50V/K/X
WF/1X4/W/X
CD IN
CD_IN
21 CD_L
21 CD_R
21 CDGND
CBC46
CBC47
CBC48
SHR/1*4/BK/P/2.54/VA/D
1N/4/X7R/50V/K/X
FUSEVCC
CFB1 0/6/SHT/X
OPT_VCC
SPDIF
BC137 0.1U/6/Y5V/25V/Z
SPDIF OUT
OPTICAL
FR/5P/BK/T/D/S(GY)
21 SPDIF
CC15 0.01U/4/Y5V/50V/Z
CR53 100/4
CR54 220/4
CC16 100P/4/NPO/50V/J
RCA-JACK4P
COAXIAL
RCA/4P/YL/OS/RA/D/1
INTEL FRONT AUDIO
For EMI
21 FRONT_MIC1
CBC51 1N/4/X7R/50V/K
AVDD
CBC52 1K/4
CR49 0/4/SHT/X
F_AUDIO
CR50 8.2K/4
FRONT_R
FRONT_L
CBC53 0.1U/6/Y5V/25V/Z/X
CBC54 180P/4/NPO/50V/J/X
CBC55 180P/4/NPO/50V/J/X
BACK_R
BACK_L
FRONT_MIC2
PH/2*5K8/BK/2.54/VA/D
CR51 22K/4/X
CR52 22K/4/X
21 JD1
21 JD2
JP/1*2/BU/OH/O:[5-6]CLOSE
JP/1*2/BU/OH/O:[9-10]CLOSE
Coaxial
Optical
USB_1394
USB_LAN
Audio1
Audio2
GIGABYTE Technology
Title
AUDIO JACK
Size Custom
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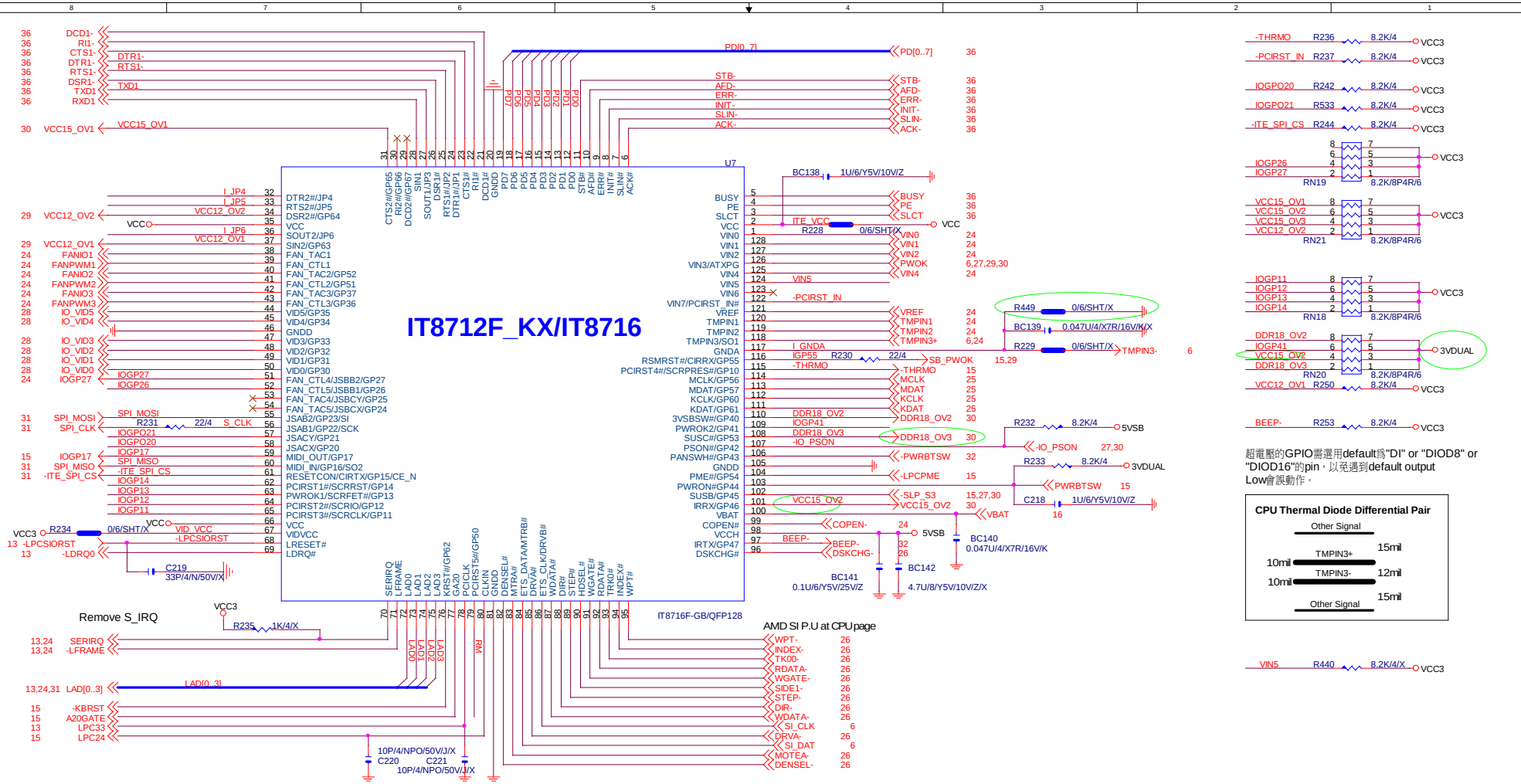

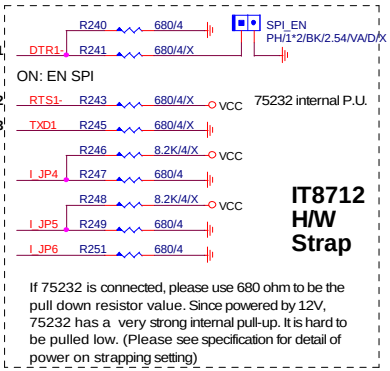

	Default	Description
JP1	0	En SPI Flash
JP2	1	Midi-in/SO2 as SPI SO pin
JP3	--	
JP4	0	PCIRSTx# are push-pull
JP5	0	Power-on FAN Duty=50%
JP6	0	VID threshold is 0.8V/0.4V

Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

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Title	ITE 8712KX/ IT8716	
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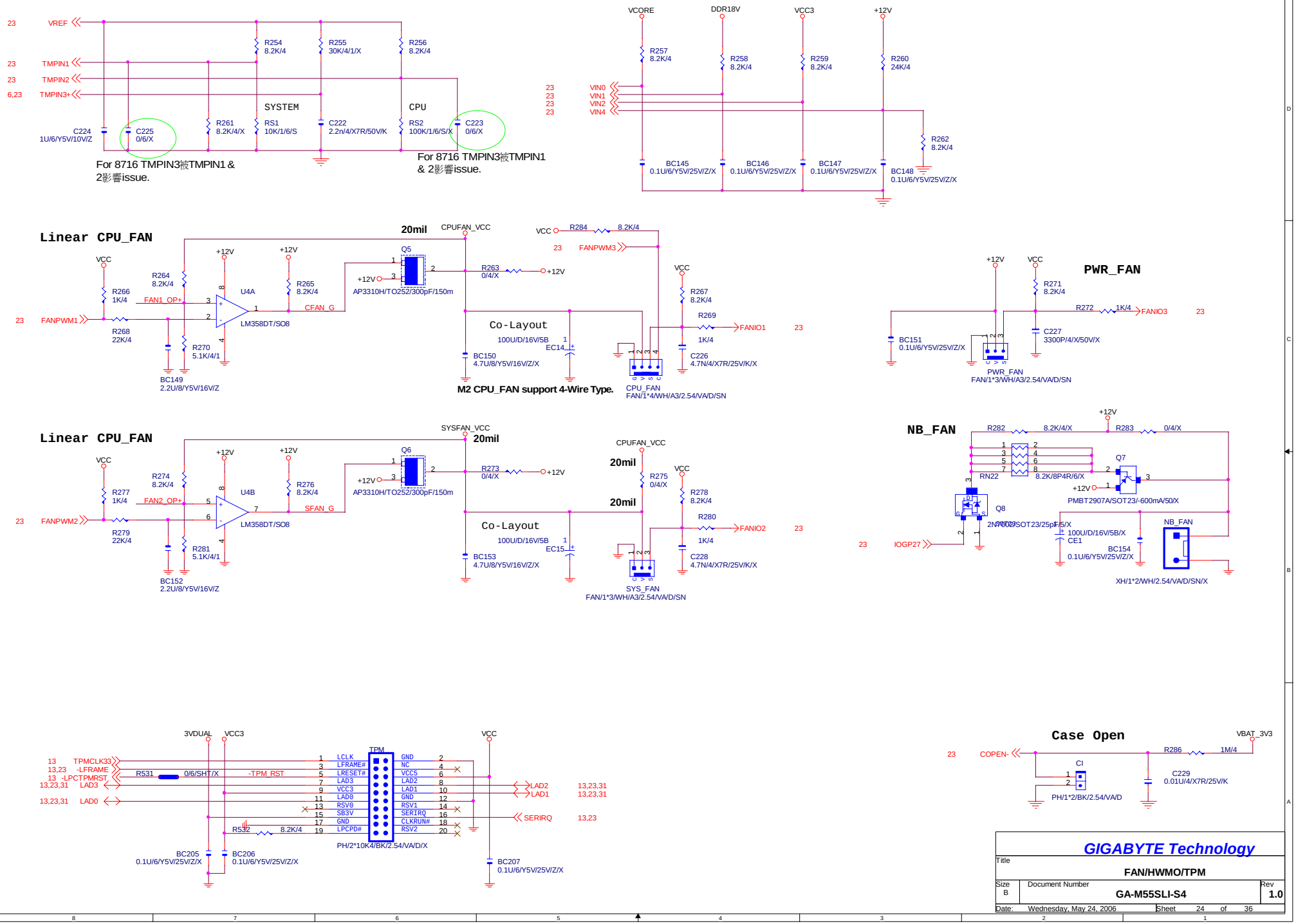
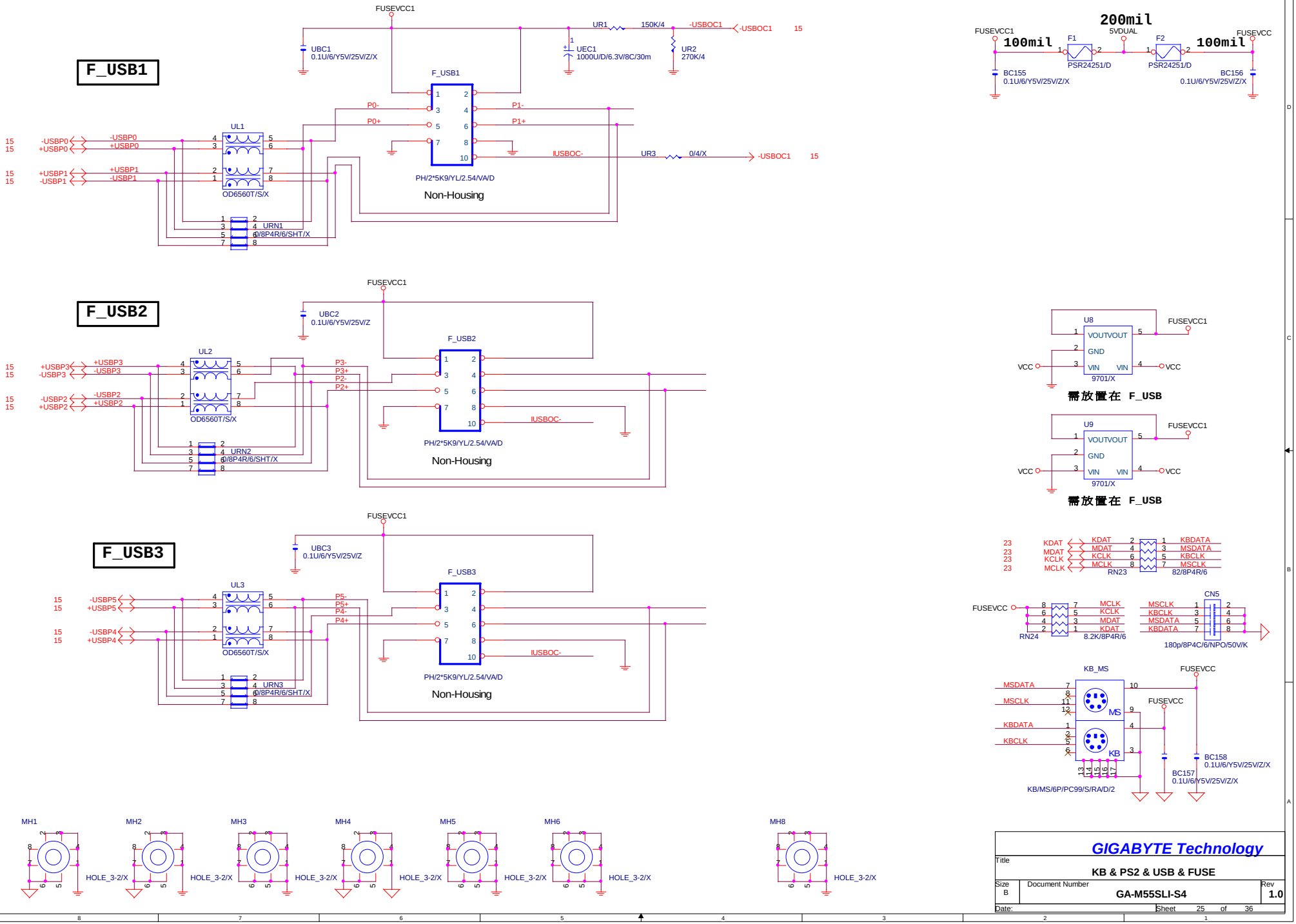


GIGABYTE Technology			
Title: FAN/HWMO/TPM			
Size: B	Document Number: GA-M55SLI-S4		Rev: 1.0
Date: Wednesday, May 24, 2006	Sheet 24 of 36		



GIGABYTE Technology

Title: KB & PS2 & USB & FUSE

Size	Document Number	Rev
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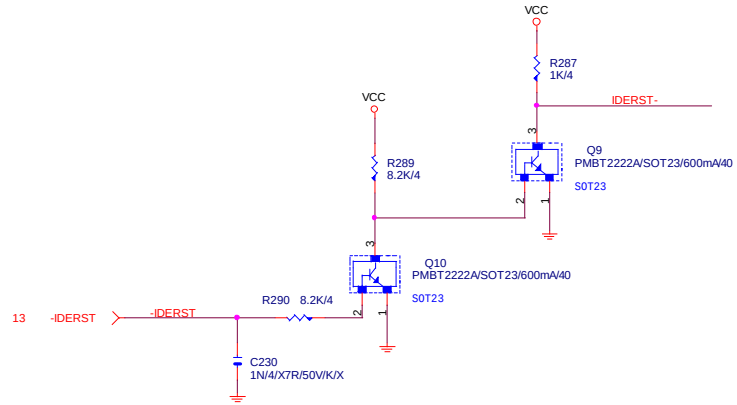
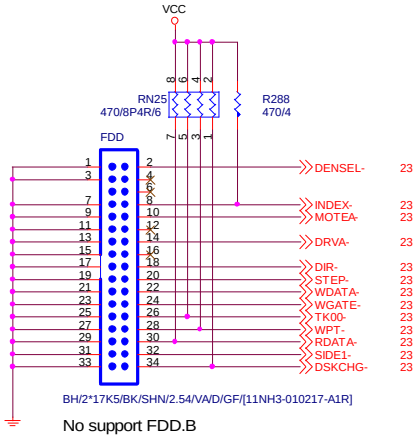
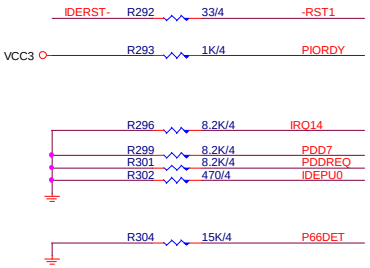
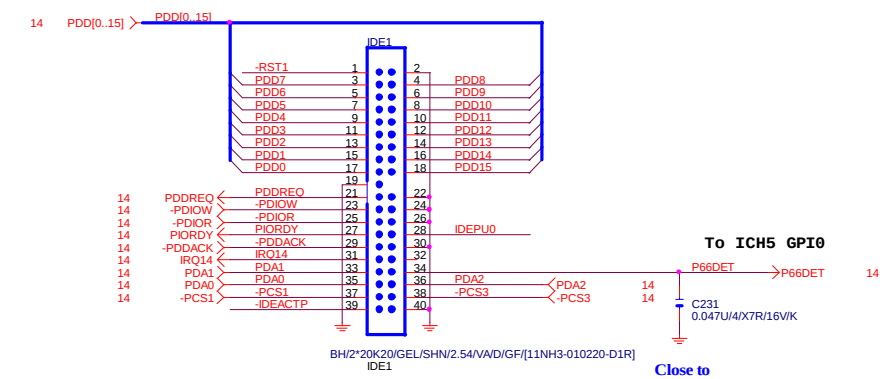


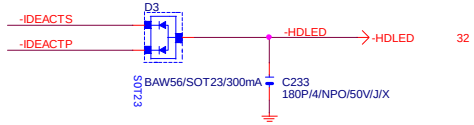


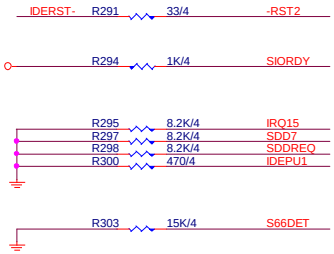
No support FDD.B



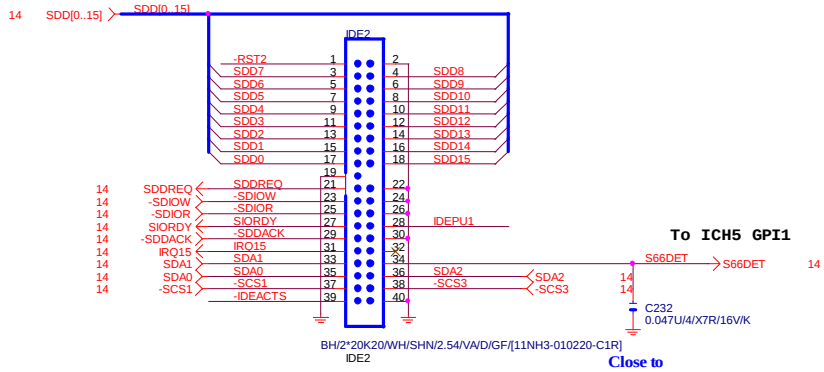
PRIMARY IDE CONNECTOR







SECONDARY IDE CONNECTOR



GIGABYTE Technology		
Title: IDE / FDD		
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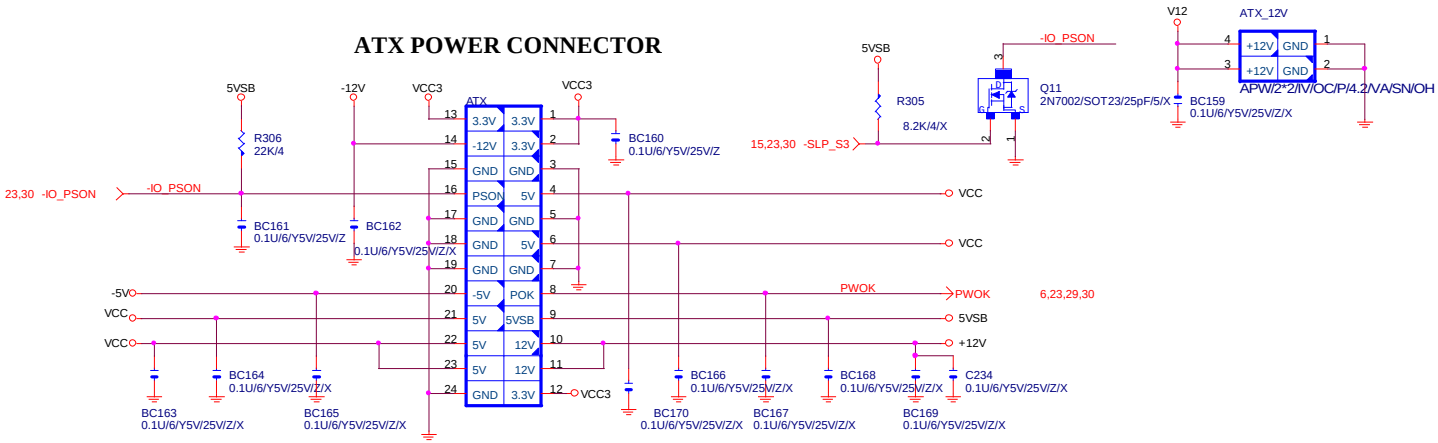
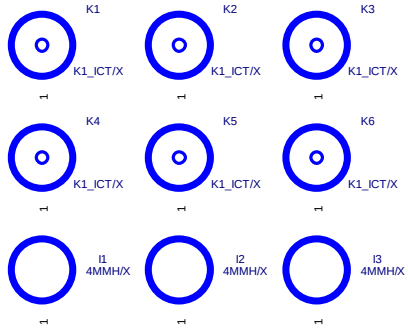
ATX POWER CONNECTOR





GIGABYTE Technology		
Title: ATX POWER		
Size: B	Document Number: GA-M55SLI-S4	Rev: 1.0
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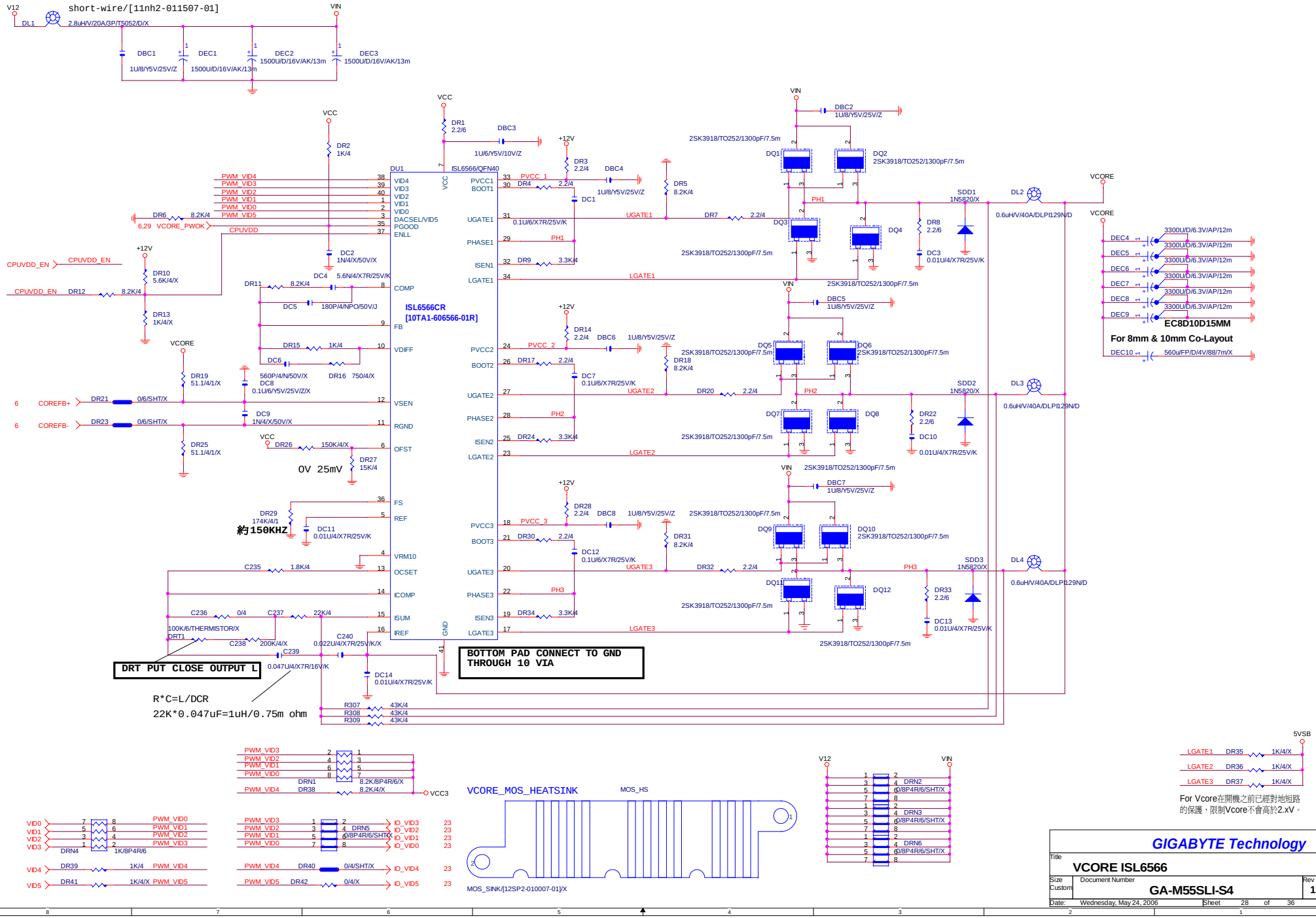
short-wire/[11nh2-011507-01]
ISL6566CR
[10TA1-606566-01R]
EC8D10D15MM
For 8mm & 10mm Co-Layout
0V 25mV
約150KHZ
DRT PUT CLOSE OUTPUT L
BOTTOM PAD CONNECT TO GND THROUGH 10 VIA
R*C=L/DCR
22K*0.047uF=1uH/0.75m ohm
VCORE_MOS_HEATSINK
MOS_HS
MOS_SINK/[12SP2-010007-01]/X
For Vcore在開機之前已經對地短路的保護，限制Vcore不會高於2.xV。
GIGABYTE Technology
VCORE ISL6566
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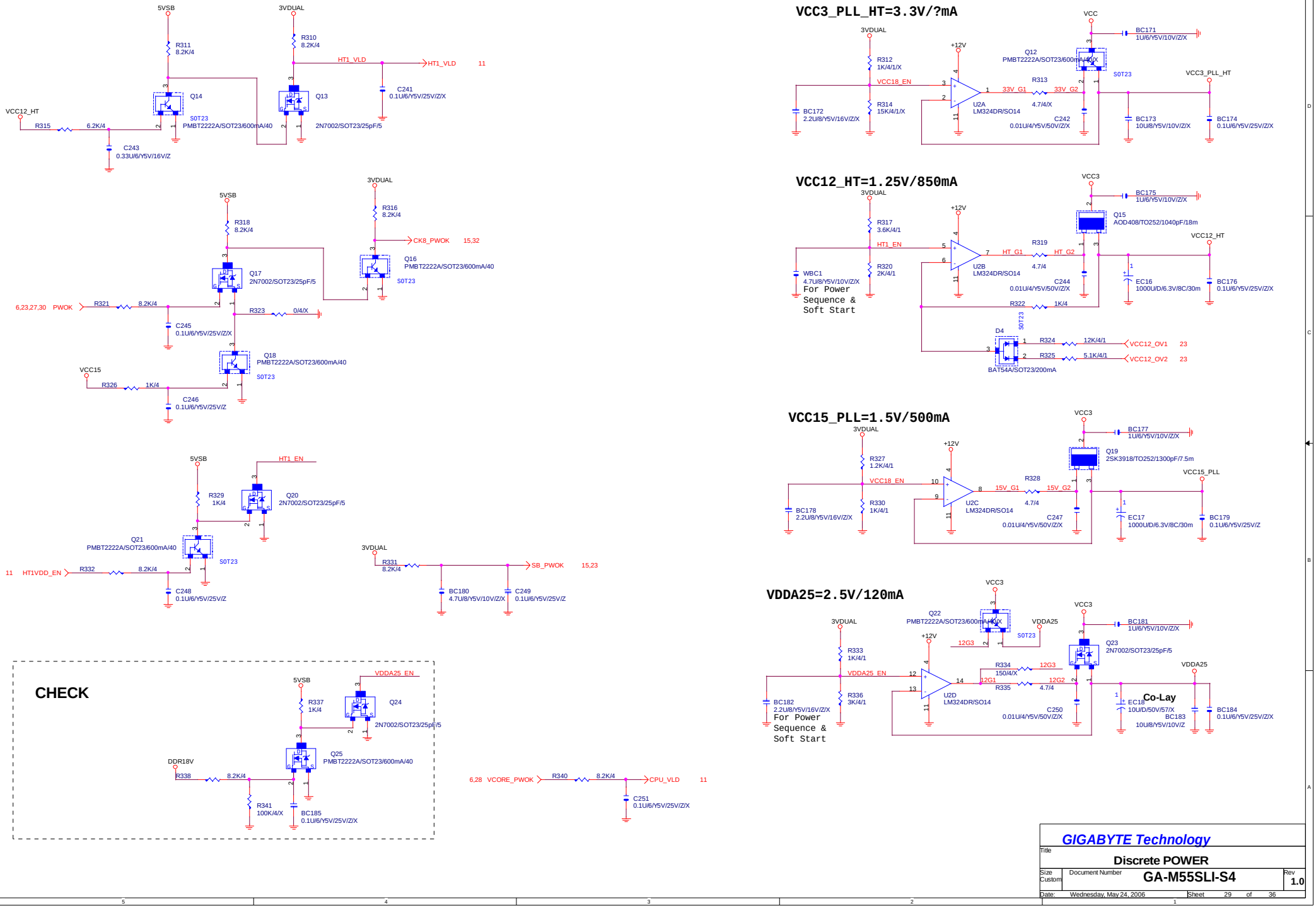
VCC3_PLL_HT=3.3V/?mA
VCC12_HT=1.25V/850mA
VCC15_PLL=1.5V/500mA
VDDA25=2.5V/120mA
CHECK
For Power Sequence & Soft Start
Co-Lay
5VSB
3VDUAL
VCC
VCC3
VCC12_HT
VCC15
VCC15_PLL
VDDA25
+12V
DDR18V
R311 8.2K/4
R310 8.2K/4
HT1_VLD
HT1_VLD 11
Q14
Q13
S0T23
PMBT2222A/SOT23/600mA/40
2N7002/SOT23/25pF/5
VCC12_HT
R315 6.2K/4
C243 0.33U/6/Y5V/16V/Z
C241 0.1U/6/Y5V/25V/Z/X
R312 1K/4/1/X
R314 15K/4/1/X
VCC18_EN
U2A LM324DR/SO14
33V_G1
33V_G2
R313 4.7/4/X
Q12 PMBT2222A/SOT23/600mA/40/X
BC171 1U/6/Y5V/10V/Z/X
VCC3_PLL_HT
BC172 2.2U/8/Y5V/16V/Z/X
C242 0.01U/4/Y5V/50V/Z/X
BC173 10U/8/Y5V/10V/Z/X
BC174 0.1U/6/Y5V/25V/Z/X
R316 8.2K/4
R318 8.2K/4
CK8_PWOK 15,32
Q16 PMBT2222A/SOT23/600mA/40
Q17 2N7002/SOT23/25pF/5
6,23,27,30 PWOK
R321 8.2K/4
R323 0/4/X
C245 0.1U/6/Y5V/25V/Z/X
Q18 PMBT2222A/SOT23/600mA/40
R326 1K/4
C246 0.1U/6/Y5V/25V/Z
R317 3.6K/4/1
R320 2K/4/1
HT1_EN
U2B LM324DR/SO14
HT_G1
HT_G2
R319 4.7/4
Q15 AOD408/TO252/1040pF/18m
BC175 1U/6/Y5V/10V/Z/X
WBC1 4.7U/8/Y5V/10V/Z/X
C244 0.01U/4/Y5V/50V/Z/X
EC16 1000U/D/6.3V/8C/30m
BC176 0.1U/6/Y5V/25V/Z/X
R322 1K/4
D4
R324 12K/4/1
R325 5.1K/4/1
VCC12_OV1 23
VCC12_OV2 23
BAT54A/SOT23/200mA
R329 1K/4
Q20 2N7002/SOT23/25pF/5
Q21 PMBT2222A/SOT23/600mA/40
11 HT1VDD_EN
R332 8.2K/4
C248 0.1U/6/Y5V/25V/Z
R331 8.2K/4
SB_PWOK 15,23
BC180 4.7U/8/Y5V/10V/Z/X
C249 0.1U/6/Y5V/25V/Z
R327 1.2K/4/1
R330 1K/4/1
U2C LM324DR/SO14
15V_G1
15V_G2
R328 4.7/4
Q19 2SK3918/TO252/1300pF/7.5m
BC177 1U/6/Y5V/10V/Z/X
BC178 2.2U/8/Y5V/16V/Z/X
C247 0.01U/4/Y5V/50V/Z/X
EC17 1000U/D/6.3V/8C/30m
BC179 0.1U/6/Y5V/25V/Z
R333 1K/4/1
R336 3K/4/1
VDDA25_EN
U2D LM324DR/SO14
12G1
12G2
12G3
R334 150/4/X
R335 4.7/4
Q22 PMBT2222A/SOT23/600mA/4/X
Q23 2N7002/SOT23/25pF/5
BC181 1U/6/Y5V/10V/Z/X
BC182 2.2U/8/Y5V/16V/Z/X
C250 0.01U/4/Y5V/50V/Z/X
EC18 10U/D/50V/57/X
BC183 10U/8/Y5V/10V/Z
BC184 0.1U/6/Y5V/25V/Z/X
R337 1K/4
Q24
Q25 PMBT2222A/SOT23/600mA/40
R338 8.2K/4
R341 100K/4/X
BC185 0.1U/6/Y5V/25V/Z/X
6,28 VCORE_PWOK
R340 8.2K/4
CPU_VLD 11
C251 0.1U/6/Y5V/25V/Z/X
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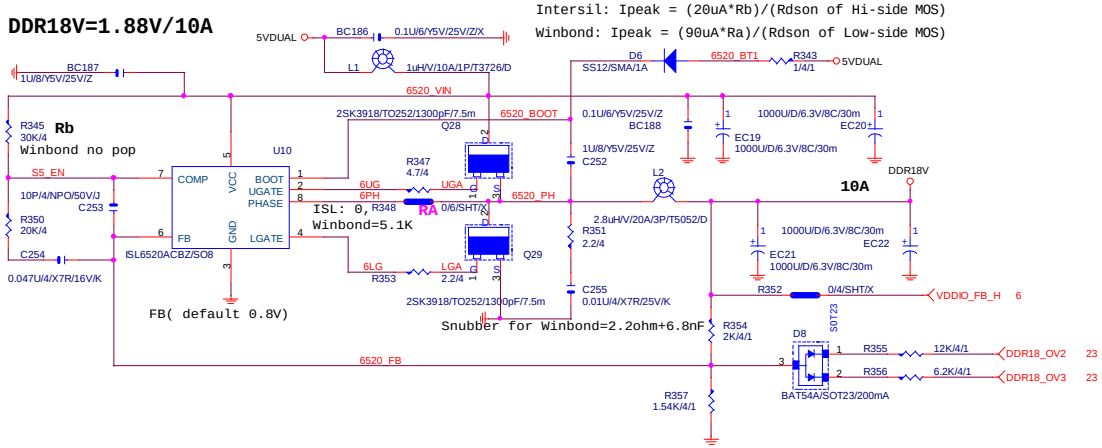
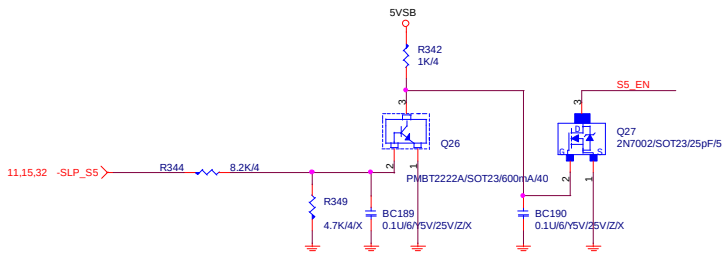
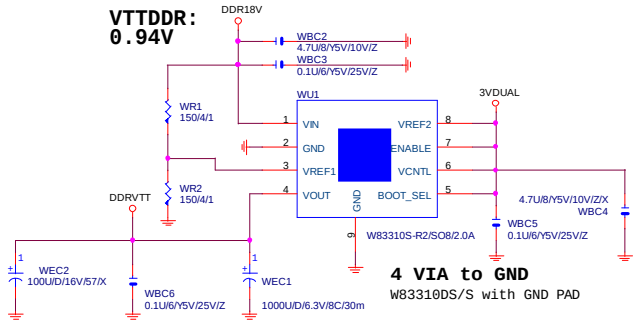
DDR18V=1.88V/10A

Intersil: Ipeak = (20uA*Rb)/(Rdson of Hi-side MOS)
Winbond: Ipeak = (90uA*Ra)/(Rdson of Low-side MOS)



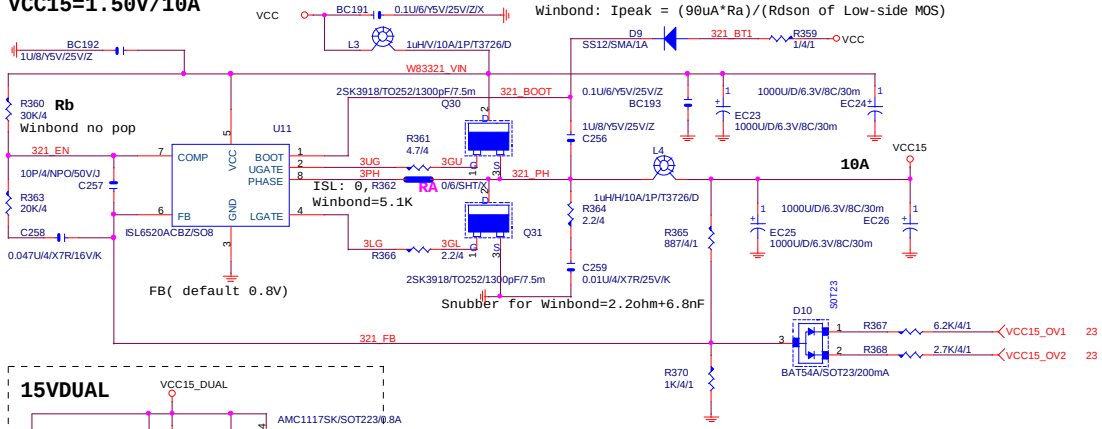


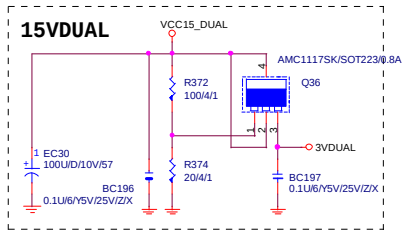
VTTDDR: 0.94V

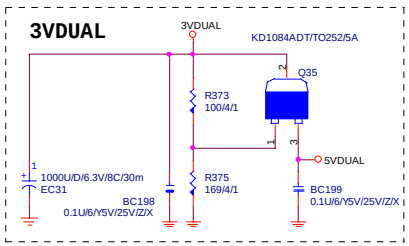


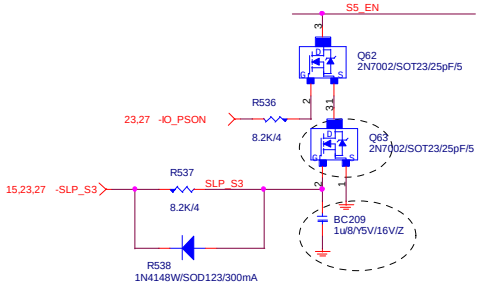
VCC15=1.50V/10A

Intersil: Ipeak = (20uA*Rb)/(Rdson of Hi-side MOS)
Winbond: Ipeak = (90uA*Ra)/(Rdson of Low-side MOS)

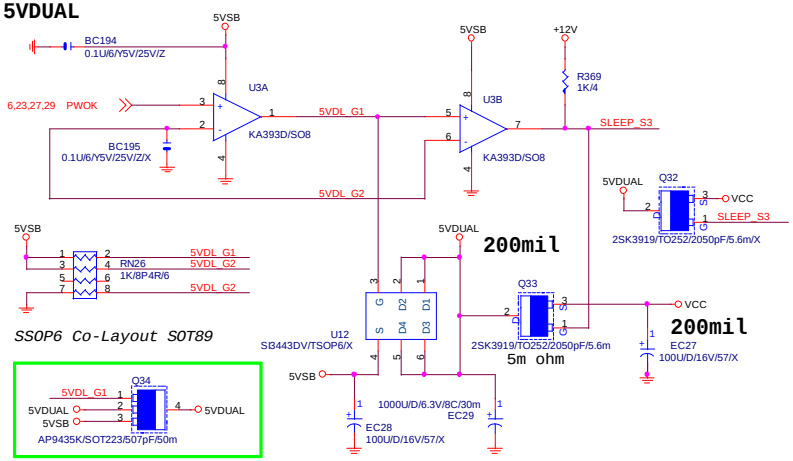








5VDUAL



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Title	DDRII & STAND-BY POWER	
Size: Custom	Document Number: GA-M55SLI-S4	Rev: 1.0
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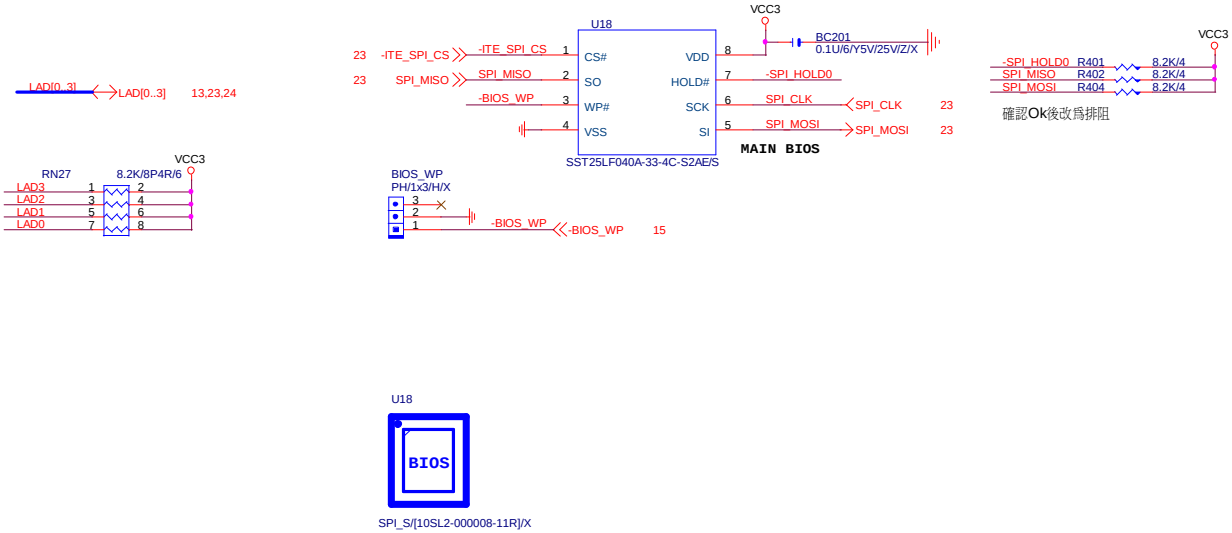

DUAL BIOS SELECTION

	Main	Backup
GPIO20	0	1
GPIO21	1	0

GIGABYTE Technology

Title: **BIOS (LPC & SPI)**

Size: B | Document Number: **GA-M55SLI-S4** | Rev: **1.0**

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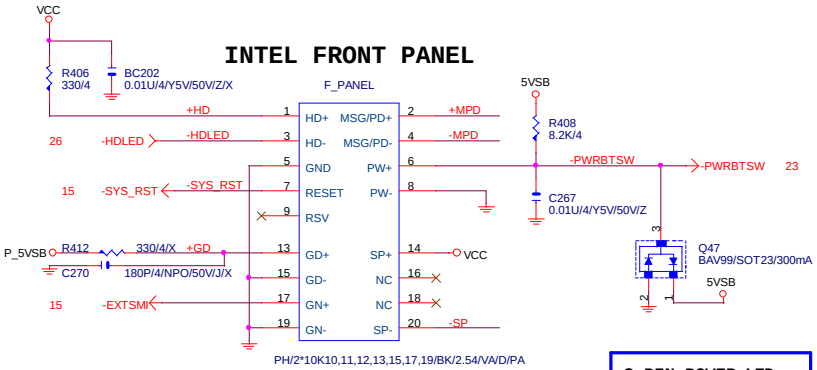
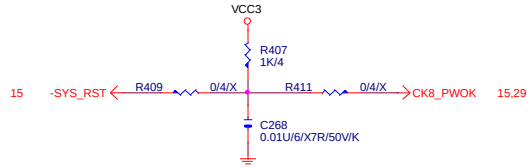
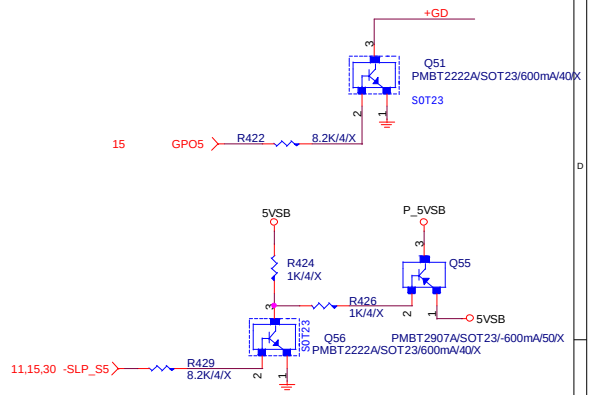
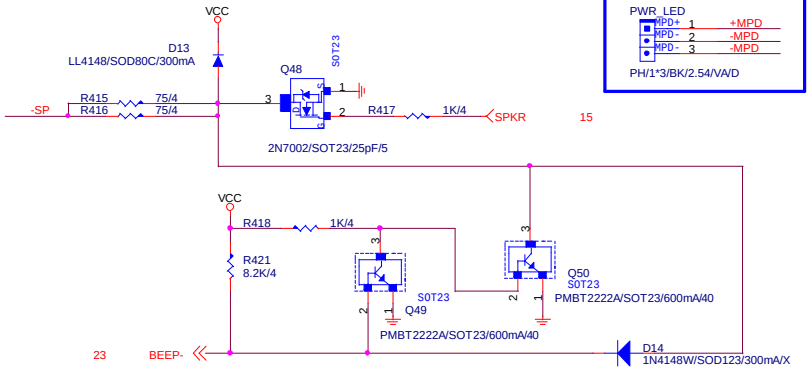
INTEL FRONT PANEL

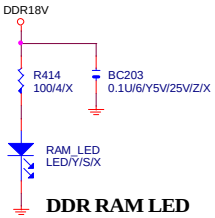




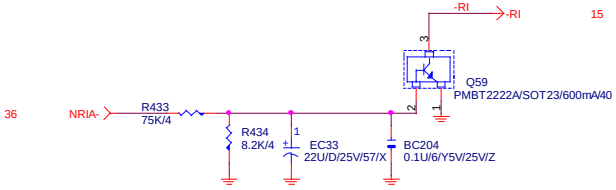


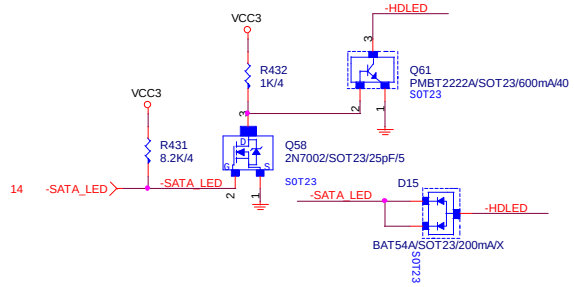


3 PIN POWER LED



DDR RAM LED





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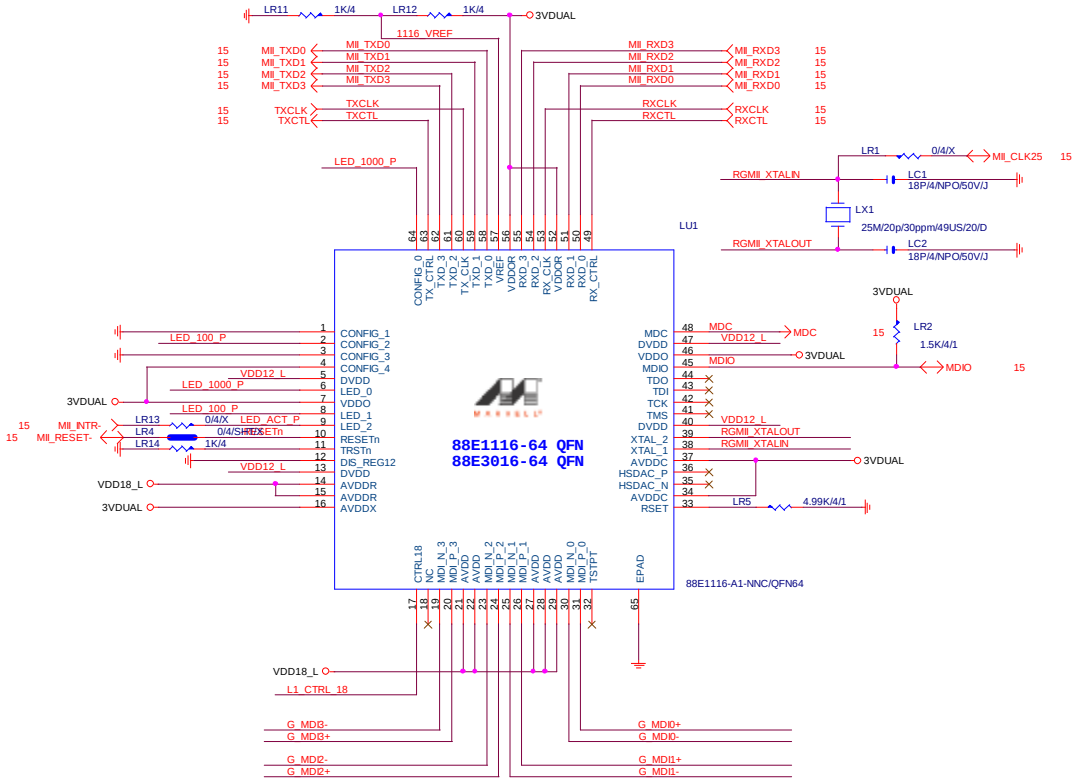
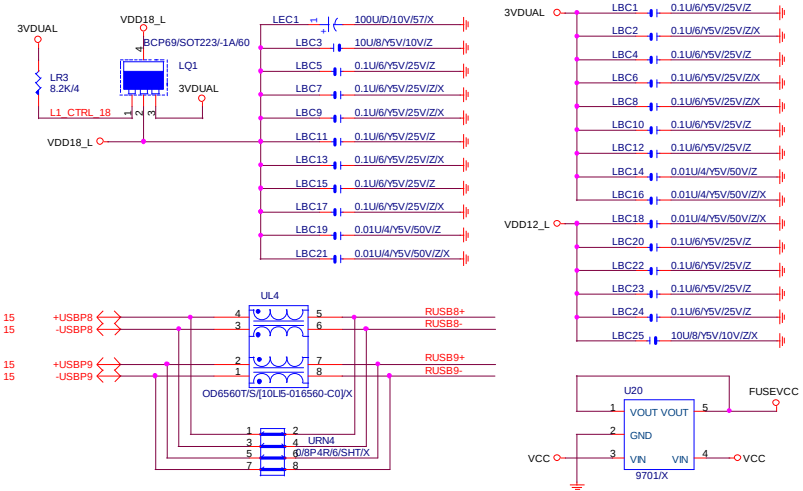
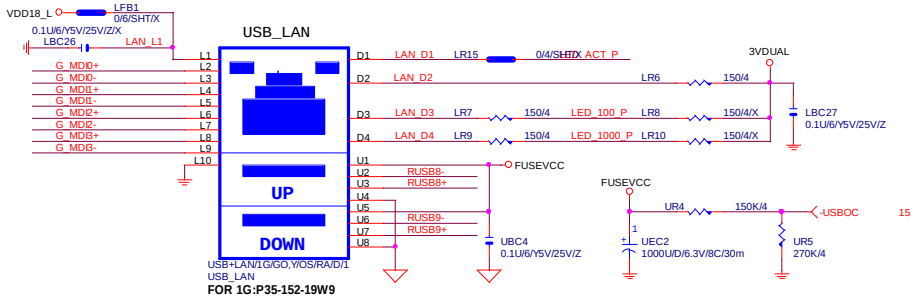


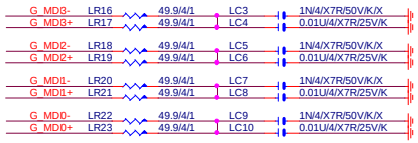
Hardware Configuration: See config _0:4
1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities

E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.

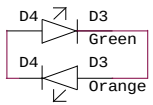




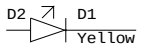
Close to Marvell 88E1116



Dual Color LED



Single Color LED



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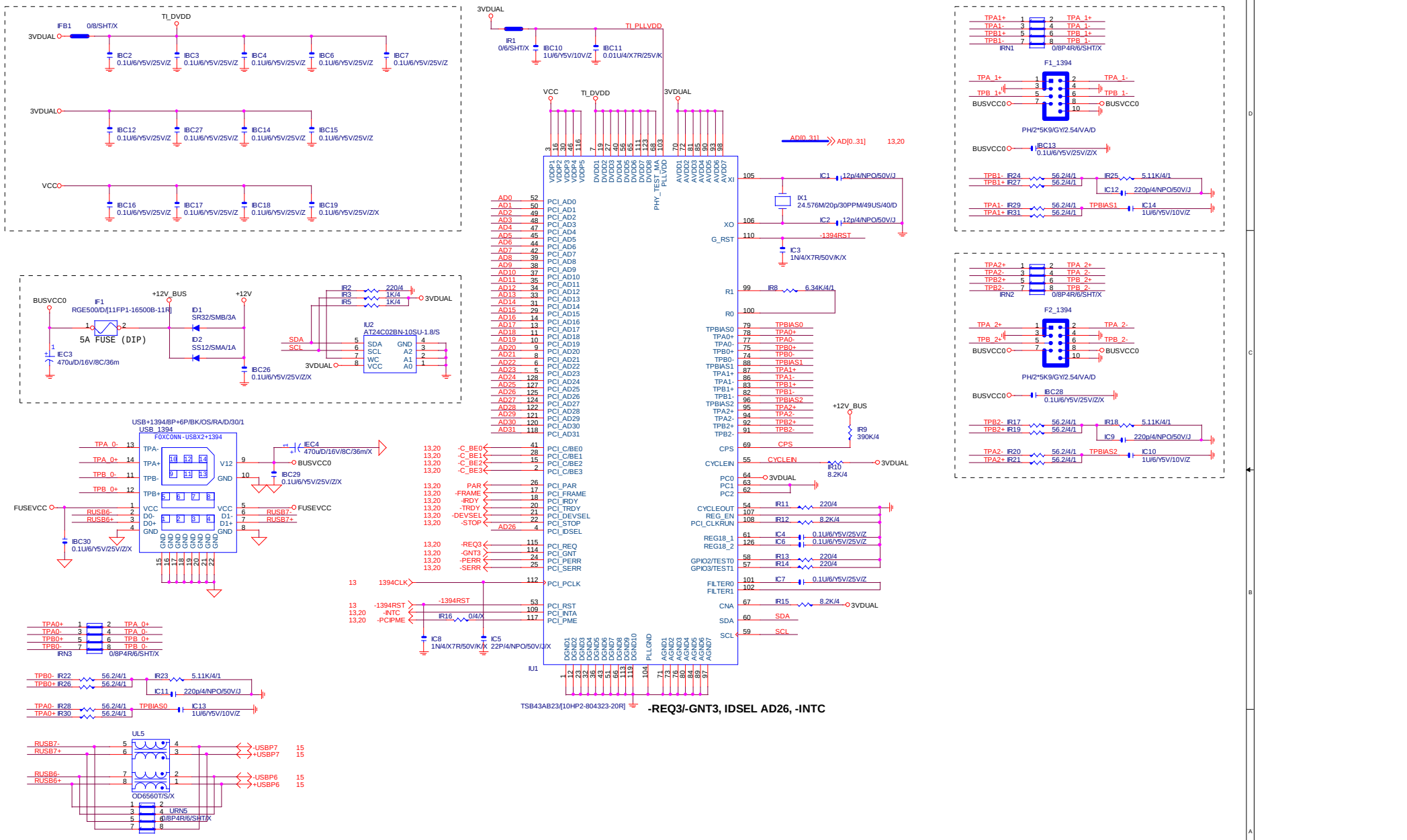

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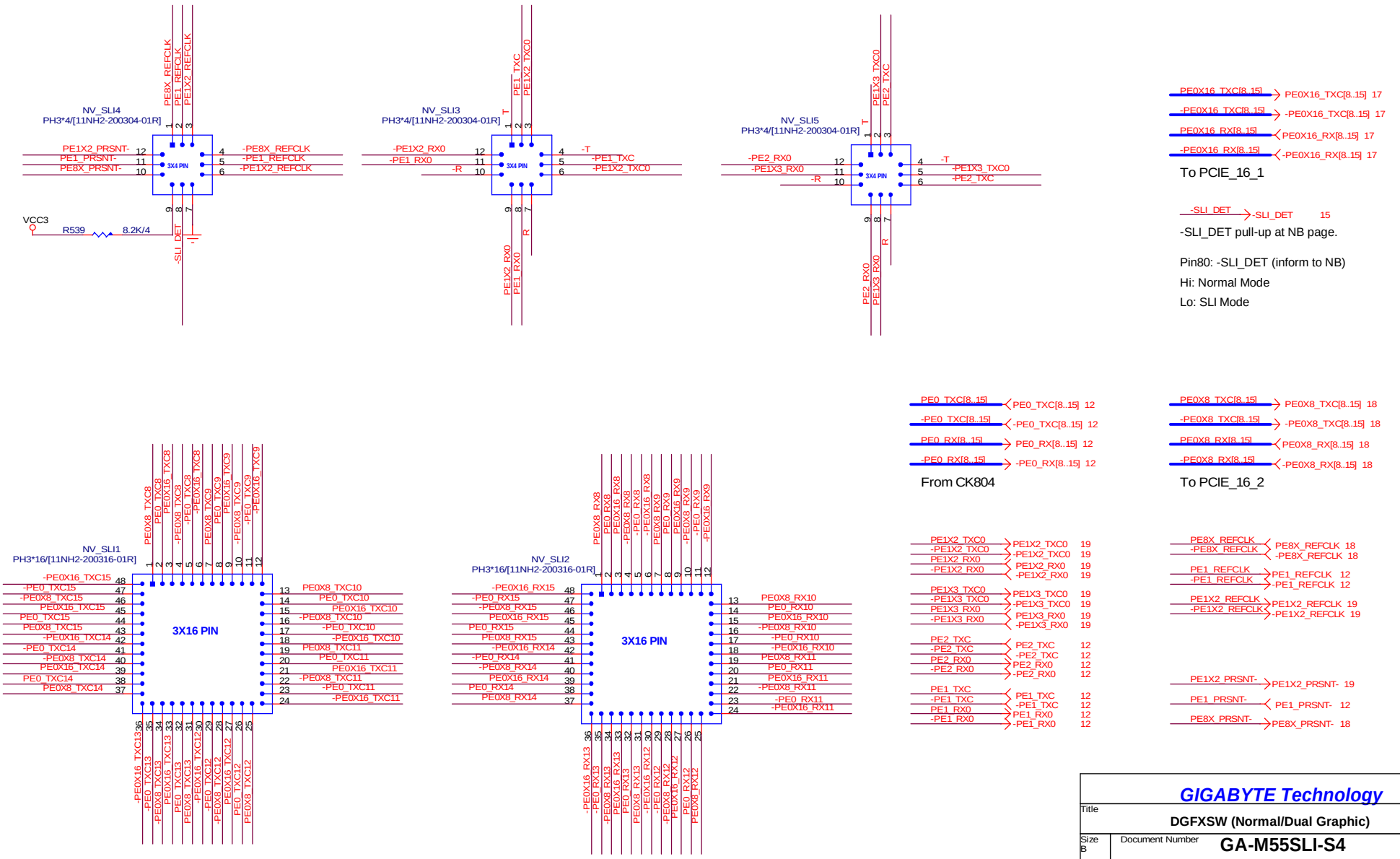
NV_SLI4
PH3*4/[11NH2-200304-01R]
PE8X_REFCLK
PE1_REFCLK
PE1X2_REFCLK
PE1X2_PRSNT-
PE1_PRSNT-
PE8X_PRSNT-
-PE8X_REFCLK
-PE1_REFCLK
-PE1X2_REFCLK
3X4 PIN
VCC3
R539
8.2K/4
-SLI_DET
NV_SLI3
PH3*4/[11NH2-200304-01R]
PE1_TXC
PE1X2_TXC0
-PE1X2_RX0
-PE1_RX0
-R
-T
-PE1_TXC
-PE1X2_TXC0
PE1X2_RX0
PE1_RX0
NV_SLI5
PH3*4/[11NH2-200304-01R]
PE1X3_TXC0
PE2_TXC
-PE2_RX0
-PE1X3_RX0
-R
-T
-PE1X3_TXC0
-PE2_TXC
PE2_RX0
PE1X3_RX0
PE0X16_TXC[8..15]
PE0X16_TXC[8..15] 17
-PE0X16_TXC[8..15]
-PE0X16_TXC[8..15] 17
PE0X16_RX[8..15]
PE0X16_RX[8..15] 17
-PE0X16_RX[8..15]
-PE0X16_RX[8..15] 17
To PCIE_16_1
-SLI_DET
-SLI_DET 15
-SLI_DET pull-up at NB page.
Pin80: -SLI_DET (inform to NB)
Hi: Normal Mode
Lo: SLI Mode
NV_SLI1
PH3*16/[11NH2-200316-01R]
3X16 PIN
PE0X8_TXC8
PE0_TXC8
PE0X16_TXC8
-PE0X8_TXC8
-PE0_TXC8
-PE0X16_TXC8
PE0X8_TXC9
PE0_TXC9
PE0X16_TXC9
-PE0X8_TXC9
-PE0_TXC9
-PE0X16_TXC9
-PE0X16_TXC15
-PE0_TXC15
-PE0X8_TXC15
PE0X16_TXC15
PE0_TXC15
PE0X8_TXC15
-PE0X16_TXC14
-PE0_TXC14
-PE0X8_TXC14
PE0X16_TXC14
PE0_TXC14
PE0X8_TXC14
PE0X8_TXC10
PE0_TXC10
PE0X16_TXC10
-PE0X8_TXC10
-PE0_TXC10
-PE0X16_TXC10
PE0X8_TXC11
PE0_TXC11
PE0X16_TXC11
-PE0X8_TXC11
-PE0_TXC11
-PE0X16_TXC11
-PE0X16_TXC13
-PE0_TXC13
-PE0X8_TXC13
PE0X16_TXC13
PE0_TXC13
PE0X8_TXC13
-PE0X16_TXC12
-PE0_TXC12
-PE0X8_TXC12
PE0X16_TXC12
PE0_TXC12
PE0X8_TXC12
NV_SLI2
PH3*16/[11NH2-200316-01R]
3X16 PIN
PE0X8_RX8
PE0_RX8
PE0X16_RX8
-PE0X8_RX8
-PE0_RX8
-PE0X16_RX8
PE0X8_RX9
PE0_RX9
PE0X16_RX9
-PE0X8_RX9
-PE0_RX9
-PE0X16_RX9
-PE0X16_RX15
-PE0_RX15
-PE0X8_RX15
PE0X16_RX15
PE0_RX15
PE0X8_RX15
-PE0X16_RX14
-PE0_RX14
-PE0X8_RX14
PE0X16_RX14
PE0_RX14
PE0X8_RX14
PE0X8_RX10
PE0_RX10
PE0X16_RX10
-PE0X8_RX10
-PE0_RX10
-PE0X16_RX10
PE0X8_RX11
PE0_RX11
PE0X16_RX11
-PE0X8_RX11
-PE0_RX11
-PE0X16_RX11
-PE0X16_RX13
-PE0_RX13
-PE0X8_RX13
PE0X16_RX13
PE0_RX13
PE0X8_RX13
-PE0X16_RX12
-PE0_RX12
-PE0X8_RX12
PE0X16_RX12
PE0_RX12
PE0X8_RX12
PE0_TXC[8..15]
PE0_TXC[8..15] 12
-PE0_TXC[8..15]
-PE0_TXC[8..15] 12
PE0_RX[8..15]
PE0_RX[8..15] 12
-PE0_RX[8..15]
-PE0_RX[8..15] 12
From CK804
PE0X8_TXC[8..15]
PE0X8_TXC[8..15] 18
-PE0X8_TXC[8..15]
-PE0X8_TXC[8..15] 18
PE0X8_RX[8..15]
PE0X8_RX[8..15] 18
-PE0X8_RX[8..15]
-PE0X8_RX[8..15] 18
To PCIE_16_2
PE1X2_TXC0
-PE1X2_TXC0
PE1X2_RX0
-PE1X2_RX0
PE1X2_TXC0 19
-PE1X2_TXC0 19
PE1X2_RX0 19
-PE1X2_RX0 19
PE1X3_TXC0
-PE1X3_TXC0
PE1X3_RX0
-PE1X3_RX0
PE1X3_TXC0 19
-PE1X3_TXC0 19
PE1X3_RX0 19
-PE1X3_RX0 19
PE2_TXC
-PE2_TXC
PE2_RX0
-PE2_RX0
PE2_TXC 12
-PE2_TXC 12
PE2_RX0 12
-PE2_RX0 12
PE1_TXC
-PE1_TXC
PE1_RX0
-PE1_RX0
PE1_TXC 12
-PE1_TXC 12
PE1_RX0 12
-PE1_RX0 12
PE8X_REFCLK
-PE8X_REFCLK
PE8X_REFCLK 18
-PE8X_REFCLK 18
PE1_REFCLK
-PE1_REFCLK
PE1_REFCLK 12
-PE1_REFCLK 12
PE1X2_REFCLK
-PE1X2_REFCLK
PE1X2_REFCLK 19
-PE1X2_REFCLK 19
PE1X2_PRSNT-
PE1X2_PRSNT- 19
PE1_PRSNT-
PE1_PRSNT- 12
PE8X_PRSNT-
PE8X_PRSNT- 18
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DGFXSW (Normal/Dual Graphic)
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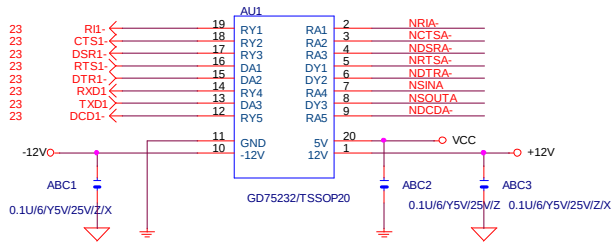

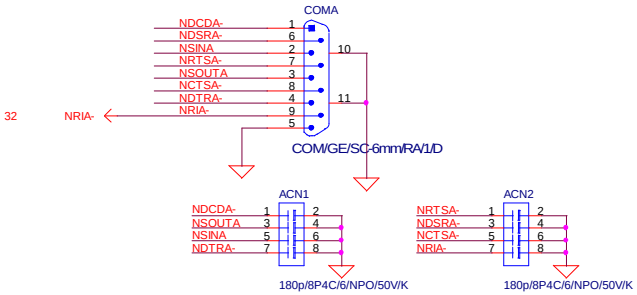

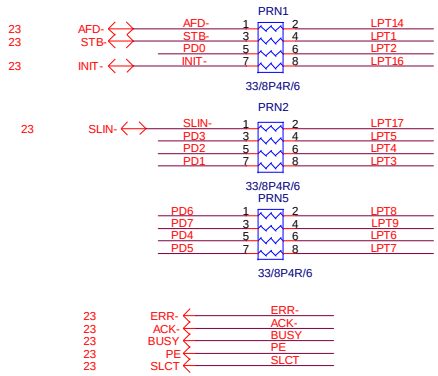

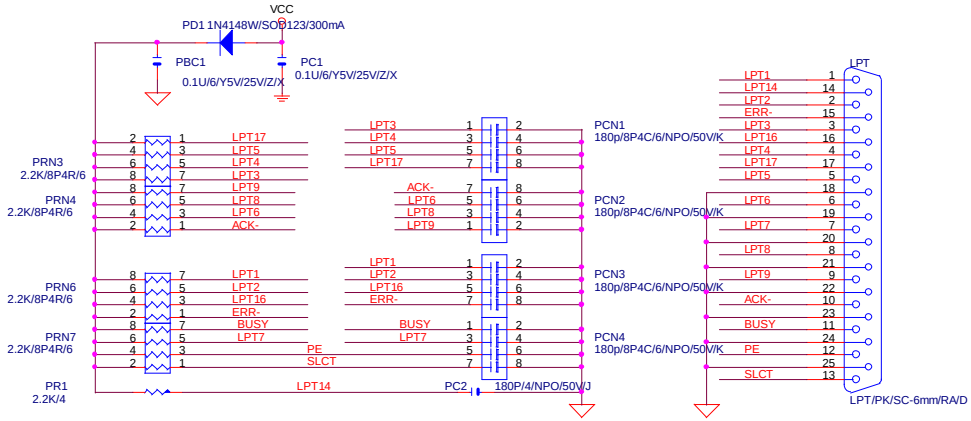

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