

GIGABYTE GA-M55S-S3 Schematics

Revision:1.0

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	PROCESSOR HT INTERFACE
05	PROCESSOR DDR INTERFACE
06	PROCESSOR DDR INTERFACE
07	PROCESSOR CONTROL & DEBUG
08	DIMM A0,B0
09	DIMM A1,B1
10	DIMM TERMINATION
11	MCP55 HT/CLK
12	MCP55 PCIE X16
13	MCP55 PCIE X8 X1
14	MCP55 PCI
15	MCP55 SATA , IDE
16	MCP55 AUDIO , USB , MISC
17	MCP55 DUAL RGMII
18	MCP55 PWR/GND
19	MCP55 DECOUPLING
20	PCI EXPRESS X16 SLOT
21	PCI EXPRESS X8 SLOT
22	PCI EXPRESS X1 SLOT1,2,3
23	PCI 1,2 SLOT
24	CODEC 883
25	AUDIO JACK, L_OUT, F_AUDIO

SHEET

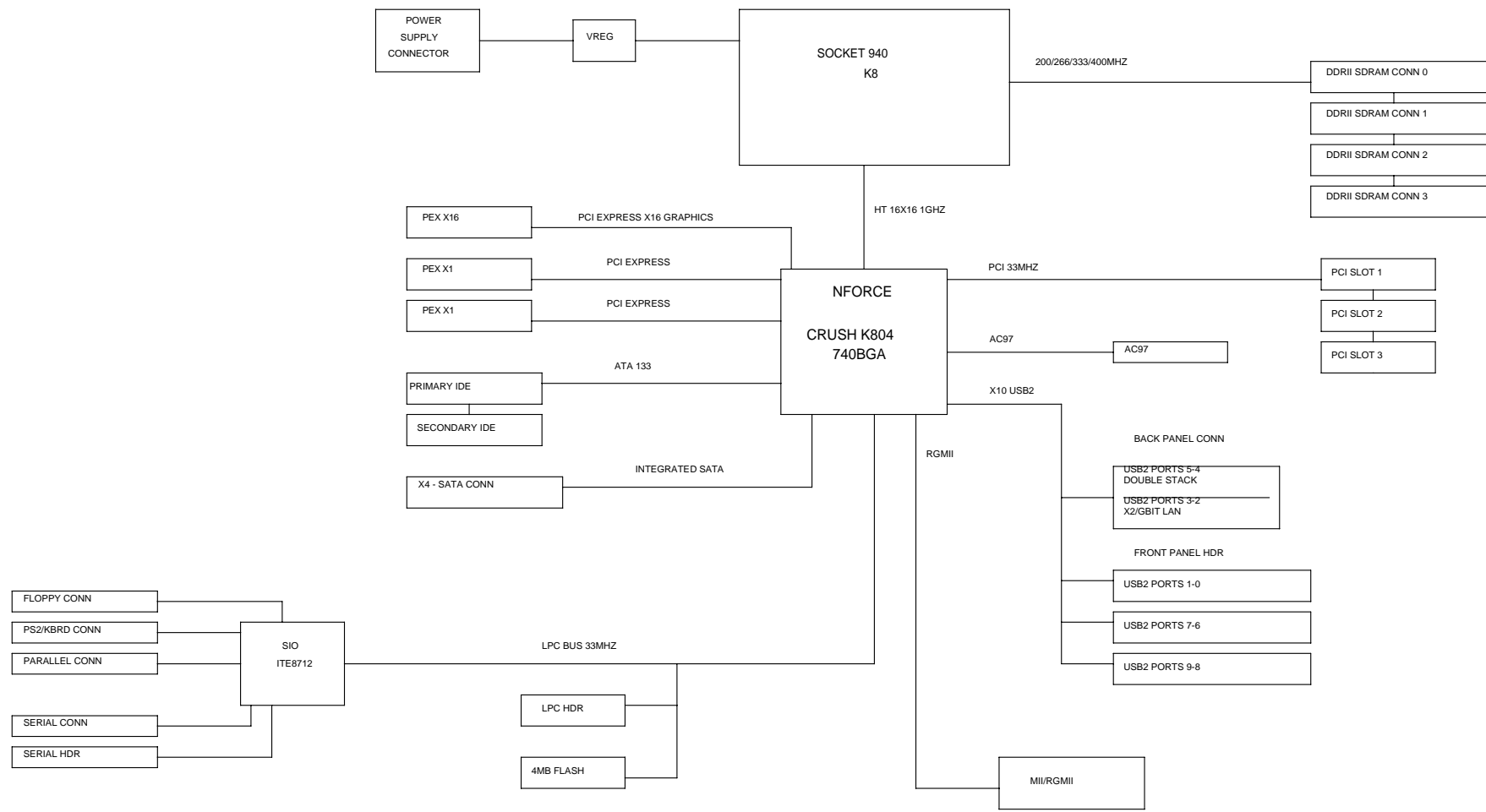
TITLE

26	IDE1/FDD
27	KB_MS/FUSEVCC
28	VCORE POWER
29	VCC12_HT,VCCA25,PLL POWER
30	PWR SEQUENCE PWR
31	DDR18 , DDRVTT , 5VDUAL
32	ATX POWER CONNCTOR,VCC15
33	DUAL BIOS
34	FRONT PANEL
35	ITE 8716F (GB)
36	FAN/HW MONITOR
37	F_USB1/F_USB2/F_USB3 CONNECTOR
38	COMA , LPT , TPM , R_USB
39	MARVELL 1116 RGMII PHY -A
40	TI TSB43AB23 1394A
41	
42	
43	
44	

GIGABYTE CORP.

Title			BLOCK DIAGRAM		
Size	Document Number	Rev			
Custom	GA-M55S-S3	1.0			
Date:	Wednesday, July 19, 2006	Sheet	1	of	41

BLOCK DIAGRAM



GIGABYTE CORP.

Title			BLOCK DIAGRAM
Size	Document Number	Rev	
Custom	GA-M55S-S3	1.0	
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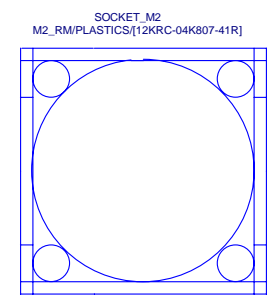
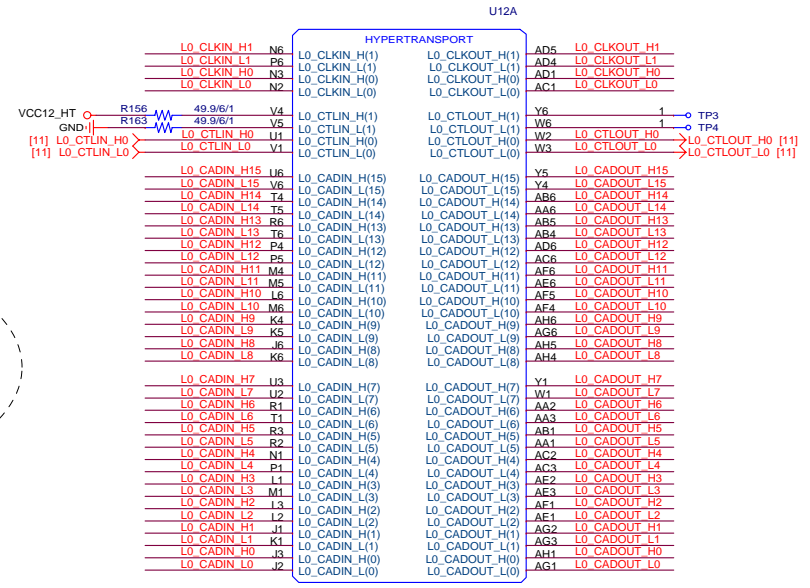
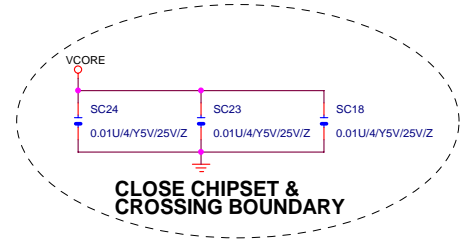
- L0_CADIN_L10..15 <L0_CADIN_L10..15 [11]
- L0_CADIN_H10..15 <L0_CADIN_H10..15 [11]
- L0_CLKIN_L10..1 <L0_CLKIN_L10..1 [11]
- L0_CLKIN_H10..1 <L0_CLKIN_H10..1 [11]
- L0_CADOUT_L10..15 <L0_CADOUT_L10..15 [11]
- L0_CADOUT_H10..15 <L0_CADOUT_H10..15 [11]
- L0_CLKOUT_L10..1 <L0_CLKOUT_L10..1 [11]
- L0_CLKOUT_H10..1 <L0_CLKOUT_H10..1 [11]

CPU_VDDA_RUN = VDDA25
 CPU_VDDIO_SUS = DDR18V
 CPU_VTT_SUS = DDRVTT

CPU_VDD_RUN = VCORE

VLDT_RUN = VCC12_HT

VLDT_A = VCC12_HT
 VLDT_B = HT12B



U12B

U12C

MEMORY INTERFACE A

MEMORY INTERFACE B

[8,10] DCLKA2	DCLKA2	AG21	MA0_CLK_H(2)
[8,10] -DCLKA2	-DCLKA2	AG20	MA0_CLK_L(2)
[8,10] DCLKA1	-DCLKA1	H19	MA0_CLK_H(1)
[8,10] -DCLKA1	DCLKA1	G19	MA0_CLK_L(1)
[8,10] DCLKA0	-DCLKA0	U27	MA0_CLK_H(0)
[8,10] -DCLKA0	DCLKA0	U26	MA0_CLK_L(0)
[8,10] -CSA1	AC25	MA0_CS_L(1)	
[8,10] -CSA0	AA24	MA0_CS_L(0)	
[8,10] MODT_A0	MODT_A0	AC28	MA0_ODT(0)
[9,10] DCLKA5	DCLKA5	AE20	MA1_CLK_H(2)
[9,10] -DCLKA5	-DCLKA5	AE19	MA1_CLK_L(2)
[9,10] DCLKA4	-DCLKA4	G20	MA1_CLK_H(1)
[9,10] -DCLKA4	DCLKA4	V27	MA1_CLK_L(1)
[9,10] DCLKA3	-DCLKA3	W27	MA1_CLK_H(0)
[9,10] -DCLKA3	DCLKA3	W27	MA1_CLK_L(0)
[9,10] -CSA3	AD27	MA1_CS_L(1)	
[9,10] -CSA2	AB25	MA1_CS_L(0)	
[9,10] MODT_A1	MODT_A1	AC27	MA1_ODT(0)
[8,9,10] -SCASA	-SCASA	AB25	MA_CAS_L
[8,9,10] -SWEA	-SWEA	AB27	MA_WE_L
[8,9,10] -SRASA	-SRASA	AA26	MA_RAS_L
[8,9,10] SBAA2	SBAA2	N25	MA_BANK(2)
[8,9,10] SBAA1	SBAA1	Y27	MA_BANK(1)
[8,9,10] SBAA0	SBAA0	AA27	MA_BANK(0)
[9,10] CKEA1	CKEA1	L27	MA_CKE(1)
[9,10] CKEA0	CKEA0	M25	MA_CKE(0)
[8,9,10] MAAA15	MAAA15	M27	MA_ADD(15)
[8,9,10] MAAA14	MAAA14	N24	MA_ADD(14)
[8,9,10] MAAA13	MAAA13	AC28	MA_ADD(13)
[8,9,10] MAAA12	MAAA12	N26	MA_ADD(12)
[8,9,10] MAAA11	MAAA11	P25	MA_ADD(11)
[8,9,10] MAAA10	MAAA10	Y25	MA_ADD(10)
[8,9,10] MAAA9	MAAA9	N27	MA_ADD(9)
[8,9,10] MAAA8	MAAA8	R24	MA_ADD(8)
[8,9,10] MAAA7	MAAA7	P27	MA_ADD(7)
[8,9,10] MAAA6	MAAA6	R25	MA_ADD(6)
[8,9,10] MAAA5	MAAA5	R26	MA_ADD(5)
[8,9,10] MAAA4	MAAA4	R27	MA_ADD(4)
[8,9,10] MAAA3	MAAA3	T25	MA_ADD(3)
[8,9,10] MAAA2	MAAA2	U25	MA_ADD(2)
[8,9,10] MAAA1	MAAA1	T27	MA_ADD(1)
[8,9,10] MAAA0	MAAA0	W24	MA_ADD(0)
[8,9,10] DQSA7	DQSA7	AD15	MA_DQS_H(7)
[8,9,10] -DQSA7	-DQSA7	AE15	MA_DQS_L(7)
[8,9,10] DQSA6	DQSA6	AG18	MA_DQS_H(6)
[8,9,10] -DQSA6	-DQSA6	AG18	MA_DQS_L(6)
[8,9,10] DQSA5	DQSA5	AG24	MA_DQS_H(5)
[8,9,10] -DQSA5	-DQSA5	AG25	MA_DQS_L(5)
[8,9,10] DQSA4	DQSA4	AG27	MA_DQS_H(4)
[8,9,10] -DQSA4	-DQSA4	AG28	MA_DQS_L(4)
[8,9,10] DQSA3	DQSA3	D29	MA_DQS_H(3)
[8,9,10] -DQSA3	-DQSA3	C29	MA_DQS_L(3)
[8,9,10] DQSA2	DQSA2	C25	MA_DQS_H(2)
[8,9,10] -DQSA2	-DQSA2	D25	MA_DQS_L(2)
[8,9,10] DQSA1	DQSA1	E19	MA_DQS_H(1)
[8,9,10] -DQSA1	-DQSA1	F19	MA_DQS_L(1)
[8,9,10] DQSA0	DQSA0	F15	MA_DQS_H(0)
[8,9,10] -DQSA0	-DQSA0	G15	MA_DQS_L(0)
[8,9,10] DMA7	DMA7	AF15	MA_DM(7)
[8,9,10] DMA6	DMA6	AF19	MA_DM(6)
[8,9,10] DMA5	DMA5	AJ25	MA_DM(5)
[8,9,10] DMA4	DMA4	AB29	MA_DM(4)
[8,9,10] DMA3	DMA3	B29	MA_DM(3)
[8,9,10] DMA2	DMA2	E24	MA_DM(2)
[8,9,10] DMA1	DMA1	E18	MA_DM(1)
[8,9,10] DMA0	DMA0	H15	MA_DM(0)

MA_DATA(63)	AE14	MDA63
MA_DATA(62)	AG14	MDA62
MA_DATA(61)	AG16	MDA61
MA_DATA(60)	AD17	MDA60
MA_DATA(59)	AD13	MDA59
MA_DATA(58)	AE13	MDA58
MA_DATA(57)	AE16	MDA57
MA_DATA(56)	AG17	MDA56
MA_DATA(55)	AE18	MDA55
MA_DATA(54)	AG17	MDA54
MA_DATA(53)	AD21	MDA53
MA_DATA(52)	AG22	MDA52
MA_DATA(51)	AE17	MDA51
MA_DATA(50)	AF17	MDA50
MA_DATA(49)	AF21	MDA49
MA_DATA(48)	AE21	MDA48
MA_DATA(47)	AE23	MDA47
MA_DATA(46)	AE23	MDA46
MA_DATA(45)	AJ26	MDA45
MA_DATA(44)	AG26	MDA44
MA_DATA(43)	AE22	MDA43
MA_DATA(42)	AG23	MDA42
MA_DATA(41)	AH25	MDA41
MA_DATA(40)	AF25	MDA40
MA_DATA(39)	AJ28	MDA39
MA_DATA(38)	AJ29	MDA38
MA_DATA(37)	AF29	MDA37
MA_DATA(36)	AE26	MDA36
MA_DATA(35)	AJ27	MDA35
MA_DATA(34)	AH27	MDA34
MA_DATA(33)	AG29	MDA33
MA_DATA(32)	AF27	MDA32
MA_DATA(31)	E29	MDA31
MA_DATA(30)	E28	MDA30
MA_DATA(29)	D27	MDA29
MA_DATA(28)	C27	MDA28
MA_DATA(27)	G26	MDA27
MA_DATA(26)	AH27	MDA26
MA_DATA(25)	C26	MDA25
MA_DATA(24)	E27	MDA24
MA_DATA(23)	F25	MDA23
MA_DATA(22)	E25	MDA22
MA_DATA(21)	F23	MDA21
MA_DATA(20)	D23	MDA20
MA_DATA(19)	E26	MDA19
MA_DATA(18)	C26	MDA18
MA_DATA(17)	G23	MDA17
MA_DATA(16)	E22	MDA16
MA_DATA(15)	F23	MDA15
MA_DATA(14)	E21	MDA14
MA_DATA(13)	F17	MDA13
MA_DATA(12)	G17	MDA12
MA_DATA(11)	G22	MDA11
MA_DATA(10)	F21	MDA10
MA_DATA(9)	G18	MDA9
MA_DATA(8)	F17	MDA8
MA_DATA(7)	G16	MDA7
MA_DATA(6)	F15	MDA6
MA_DATA(5)	G13	MDA5
MA_DATA(4)	H13	MDA4
MA_DATA(3)	F16	MDA3
MA_DATA(2)	E14	MDA2
MA_DATA(1)	G14	MDA1
MA_DATA(0)	G14	MDA0
MA_DQS_H(8)	J28	DQSA8
MA_DQS_L(8)	J27	-DQSA8
MA_DM(8)	J25	DMA8
MA_CHECK(7)	K25	SACB7
MA_CHECK(6)	J26	SACB6
MA_CHECK(5)	G28	SACB5
MA_CHECK(4)	G27	SACB4
MA_CHECK(3)	L24	SACB3
MA_CHECK(2)	K27	SACB2
MA_CHECK(1)	H29	SACB1
MA_CHECK(0)	H27	SACB0

MAI[0..63] [8,9]

MAAB[0..15] [8,9,10]

DQSB[0..8] [8,9]

DQSB[0..8] [8,9]

DMB[0..8] [8,9]

SBCB[0..7] [8,9]

[8,10] DCLKB2	DCLKB2	AJ19	MB0_CLK_H(2)
[8,10] -DCLKB2	-DCLKB2	AK19	MB0_CLK_L(2)
[8,10] DCLKB1	-DCLKB1	A19	MB0_CLK_H(1)
[8,10] -DCLKB1	DCLKB1	A19	MB0_CLK_L(1)
[8,10] DCLKB0	-DCLKB0	U31	MB0_CLK_H(0)
[8,10] -DCLKB0	DCLKB0	U30	MB0_CLK_L(0)
[8,10] -CSB1	AE30	MB0_CS_L(1)	
[8,10] -CSB0	AC31	MB0_CS_L(0)	
[8,10] MODT_B0	MODT_B0	AD29	MB0_ODT(0)
[9,10] DCLKB5	DCLKB5	AL19	MB1_CLK_H(2)
[9,10] -DCLKB5	-DCLKB5	AL18	MB1_CLK_L(2)
[9,10] DCLKB4	-DCLKB4	C19	MB1_CLK_H(1)
[9,10] -DCLKB4	DCLKB4	D12	MB1_CLK_L(1)
[9,10] DCLKB3	-DCLKB3	W28	MB1_CLK_H(0)
[9,10] -DCLKB3	DCLKB3	W28	MB1_CLK_L(0)
[9,10] -CSB3	AE29	MB1_CS_L(1)	
[9,10] -CSB2	AB31	MB1_CS_L(0)	
[9,10] MODT_B1	MODT_B1	AD31	MB1_ODT(0)
[8,9,10] -SCASB	-SCASB	AC29	MB_CAS_L
[8,9,10] -SWEB	-SWEB	AC30	MB_WE_L
[8,9,10] -SRASB	-SRASB	AB29	MB_RAS_L
[8,9,10] SBAB2	SBAB2	N31	MB_BANK(2)
[8,9,10] SBAB1	SBAB1	AA31	MB_BANK(1)
[8,9,10] SBAB0	SBAB0	AA28	MB_BANK(0)
[9,10] CKEB1	CKEB1	M31	MB_CKE(1)
[9,10] CKEB0	CKEB0	M29	MB_CKE(0)
[8,9,10] MAAB15	MAAB15	N28	MB_ADD(15)
[8,9,10] MAAB14	MAAB14	N29	MB_ADD(14)
[8,9,10] MAAB13	MAAB13	AE31	MB_ADD(13)
[8,9,10] MAAB12	MAAB12	N30	MB_ADD(12)
[8,9,10] MAAB11	MAAB11	P29	MB_ADD(11)
[8,9,10] MAAB10	MAAB10	AA29	MB_ADD(10)
[8,9,10] MAAB9	MAAB9	P31	MB_ADD(9)
[8,9,10] MAAB8	MAAB8	R29	MB_ADD(8)
[8,9,10] MAAB7	MAAB7	R28	MB_ADD(7)
[8,9,10] MAAB6	MAAB6	R31	MB_ADD(6)
[8,9,10] MAAB5	MAAB5	T31	MB_ADD(5)
[8,9,10] MAAB4	MAAB4	R30	MB_ADD(4)
[8,9,10] MAAB3	MAAB3	T29	MB_ADD(3)
[8,9,10] MAAB2	MAAB2	U29	MB_ADD(2)
[8,9,10] MAAB1	MAAB1	U28	MB_ADD(1)
[8,9,10] MAAB0	MAAB0	AA30	MB_ADD(0)
[8,9,10] DQSB7	DQSB7	AK13	MB_DQS_H(7)
[8,9,10] -DQSB7	-DQSB7	AJ13	MB_DQS_L(7)
[8,9,10] DQSB6	DQSB6	AK17	MB_DQS_H(6)
[8,9,10] -DQSB6	-DQSB6	AJ17	MB_DQS_L(6)
[8,9,10] DQSB5	DQSB5	AK23	MB_DQS_H(5)
[8,9,10] -DQSB5	-DQSB5	AL23	MB_DQS_L(5)
[8,9,10] DQSB4	DQSB4	AL28	MB_DQS_H(4)
[8,9,10] -DQSB4	-DQSB4	AL29	MB_DQS_L(4)
[8,9,10] DQSB3	DQSB3	C31	MB_DQS_H(3)
[8,9,10] -DQSB3	-DQSB3	C31	MB_DQS_L(3)
[8,9,10] DQSB2	DQSB2	C24	MB_DQS_H(2)
[8,9,10] -DQSB2	-DQSB2	C23	MB_DQS_L(2)
[8,9,10] DQSB1	DQSB1	D17	MB_DQS_H(1)
[8,9,10] -DQSB1	-DQSB1	C17	MB_DQS_L(1)
[8,9,10] DQSB0	DQSB0	C14	MB_DQS_H(0)
[8,9,10] -DQSB0	-DQSB0	C13	MB_DQS_L(0)
[8,9,10] DMB7	DMB7	AJ14	MB_DM(7)
[8,9,10] DMB6	DMB6	AH17	MB_DM(6)
[8,9,10] DMB5	DMB5	AJ23	MB_DM(5)
[8,9,10] DMB4	DMB4	AK29	MB_DM(4)
[8,9,10] DMB3	DMB3	C30	MB_DM(3)
[8,9,10] DMB2	DMB2	A23	MB_DM(2)
[8,9,10] DMB1	DMB1	B17	MB_DM(1)
[8,9,10] DMB0	DMB0	B13	MB_DM(0)

MBI[0..63] [8,9]

MAAB[0..15] [8,9,10]

DQSB[0..8] [8,9]

DQSB[0..8] [8,9]

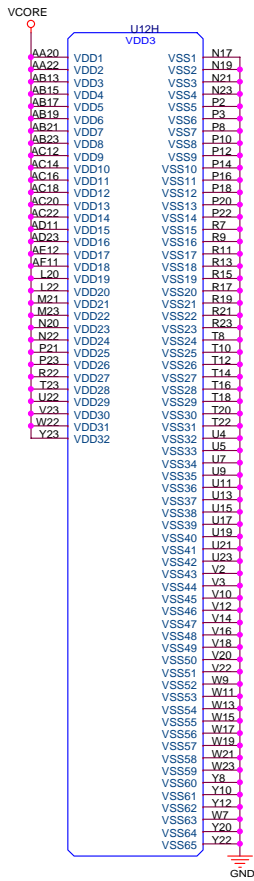
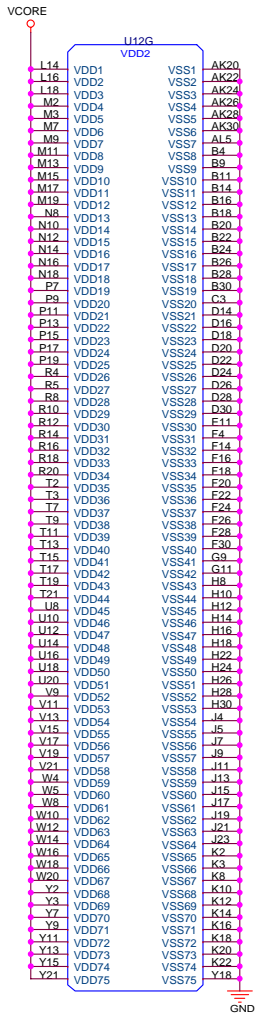
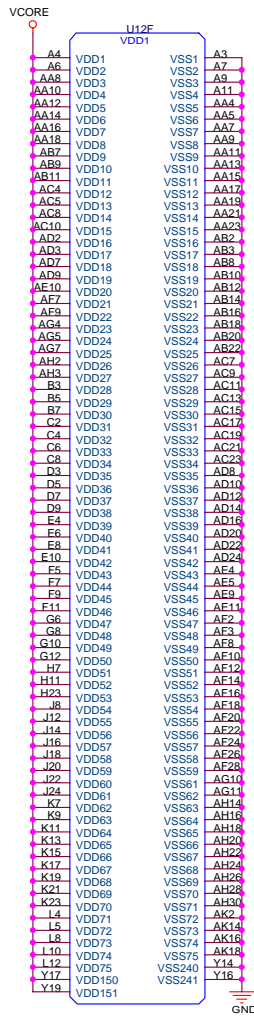
DMB[0..8] [8,9]

SBCB[0..7] [8,9]

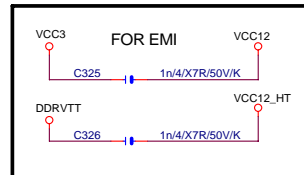
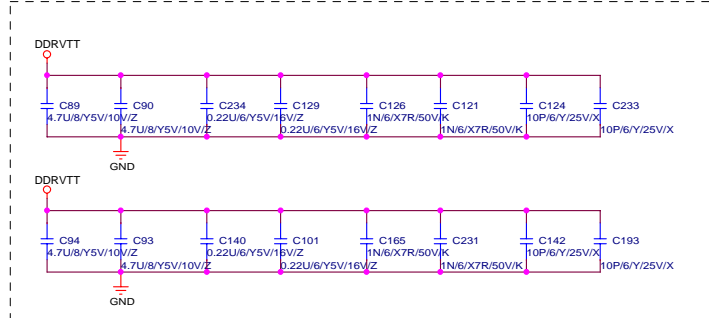
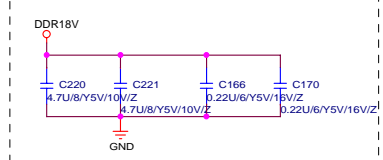
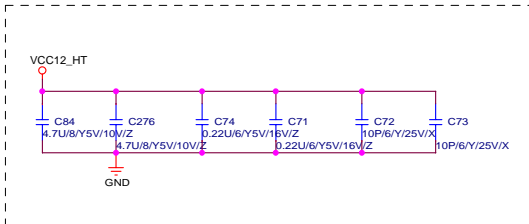
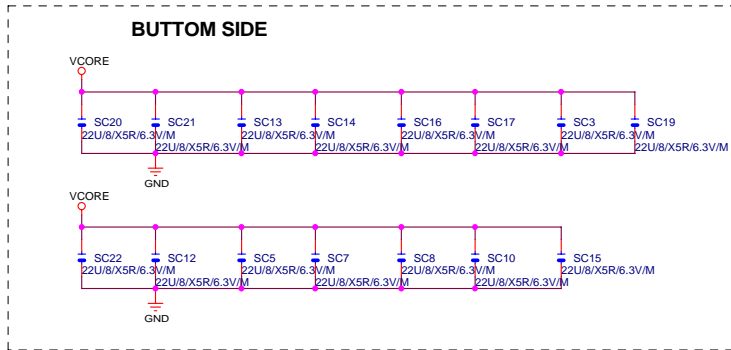
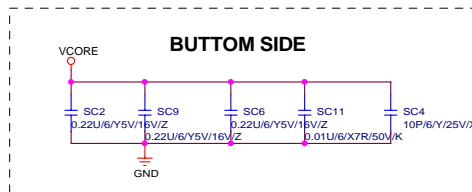
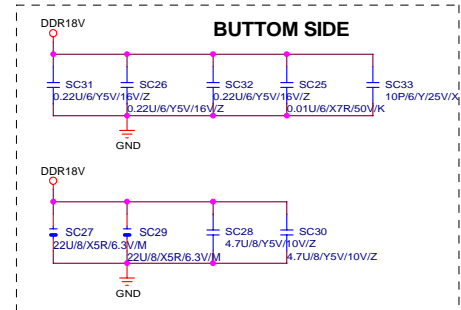
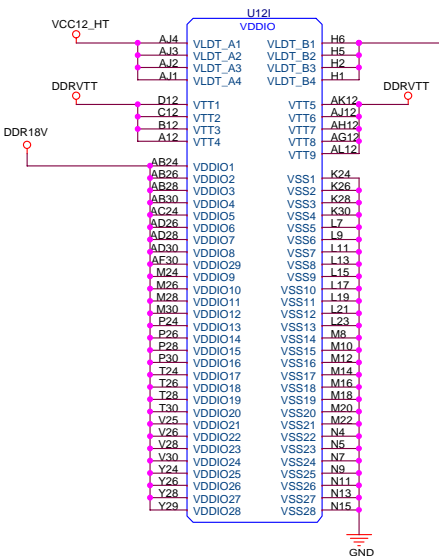
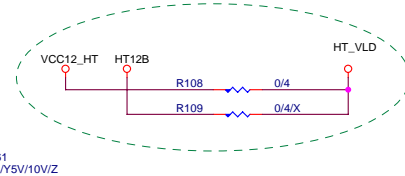
MB_DATA(63)	AH13	MDB63
MB_DATA(62)	AL13	MDB62
MB_DATA(61)	AL15	MDB61
MB_DATA(60)	AJ15	MDB60
MB_DATA(59)	AF13	MDB59
MB_DATA(58)	AG13	MDB58
MB_DATA(57)	AL14	MDB57
MB_DATA(56)	AK15	MDB56
MB_DATA(55)	AL16	MDB55
MB_DATA(54)	AL17	MDB54
MB_DATA(53)	AK21	MDB53
MB_DATA(52)	AL21	MDB52
MB_DATA(51)	AH15	MDB51
MB_DATA(50)	AJ16	MDB50
MB_DATA(49)	AH19	MDB49
MB_DATA(48)	AL20	MDB48
MB_DATA(47)	AJ22	MDB47
MB_DATA(46)	AL22	MDB46
MB_DATA(45)	AL24	MDB45
MB_DATA(44)	AK25	MDB44
MB_DATA(43)	AH21	MDB43
MB_DATA(42)	AH23	MDB42
MB_DATA(41)	AJ24	MDB41
MB_DATA(40)	AL27	MDB40
MB_DATA(39)	AK27	MDB39
MB_DATA(38)	AH31	MDB38
MB_DATA(37)	AG30	MDB37
MB_DATA(36)	AL25	MDB36
MB_DATA(35)	AL26	MDB35
MB_DATA(34)	AJ30	MDB34
MB_DATA(33)	AJ31	MDB33
MB_DATA(32)	E31	MDB32
MB_DATA(31)	E30	MDB31
MB_DATA(30)	B27	MDB29
MB_DATA(29)	A27	MDB28
MB_DATA(28)	F29	MDB27
MB_DATA(27)	F21	MDB26
MB_DATA(26)	A29	MDB25
MB_DATA(25)	A28	MDB24
MB_DATA(24)	A25	MDB23
MB_DATA(23)	A24	MDB22
MB_DATA(22)	C22	MDB21
MB_DATA(21)	D21	MDB20
MB_DATA(20)	A26	MDB19
MB_DATA(19)	B25	MDB18
MB_DATA(18)	B23	MDB17
MB_DATA(17)	B21	MDB16
MB_DATA(16)	B21	MDB15
MB_DATA(15)	A20	MDB14
MB_DATA(14)	C16	MDB13
MB_DATA(13)	D15	MDB12
MB_DATA(12)	C21	MDB11
MB_DATA(11)	A21	MDB10
MB_DATA(10)	A17	MDB9
MB_DATA(9)	A16	MDB8
MB_DATA(8)	B15	MDB7
MB_DATA(7)	A14	MDB6
MB_DATA(6)	E13	MDB5
MB_DATA(5)	MB_DATA(5)	MB04
MB_DATA(4)	C15	MDB3
MB_DATA(3)	A15	MDB2
MB_DATA(2)	A13	MDB1
MB_DATA(1)	D13	MB0
MB_DATA(0)	J31	DQSB8
MB_DQS_H(8)	J30	-DQSB8
MB_DQS_L(8)	J29	DMB8
MB_DM(8)	K29	SBCB7
MB_CHECK(7)	K31	SBCB6
MB_CHECK(6)	G30	SBCB5
MB_CHECK(5)	G29	SBCB4
MB_CHECK(4)	L29	SBCB3
MB_CHECK(3)	L28	SBCB2
MB_CHECK(2)	H31	SBCB1
MB_CHECK(1)	G31	SBCB0

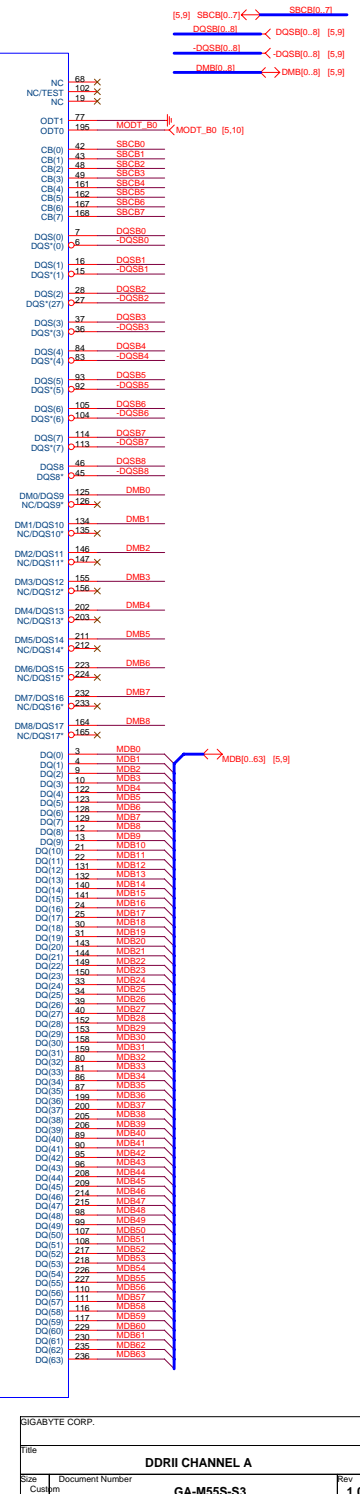
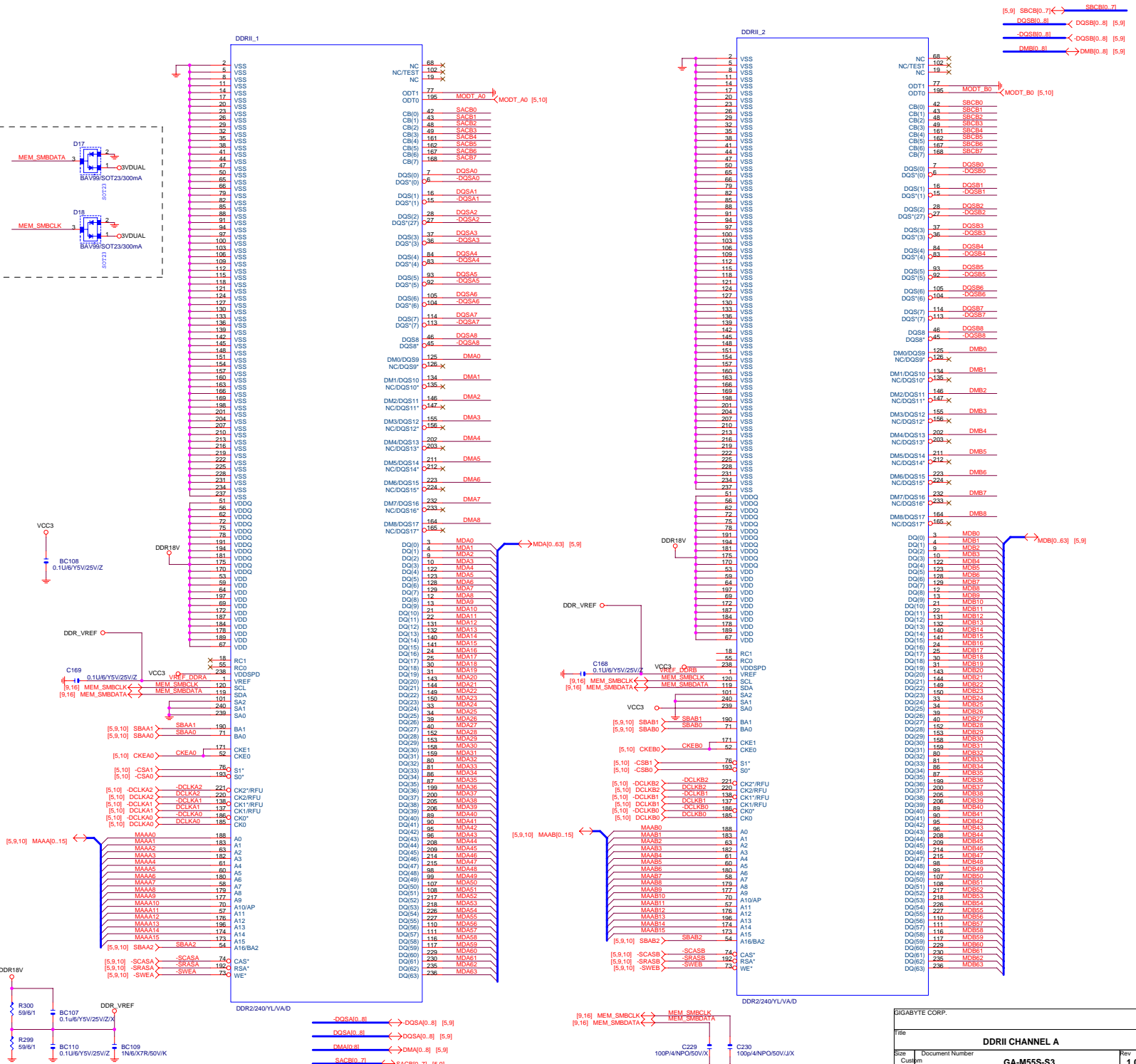
GIGABYTE CORP.

Title		
CPU DDRII MEMORY		
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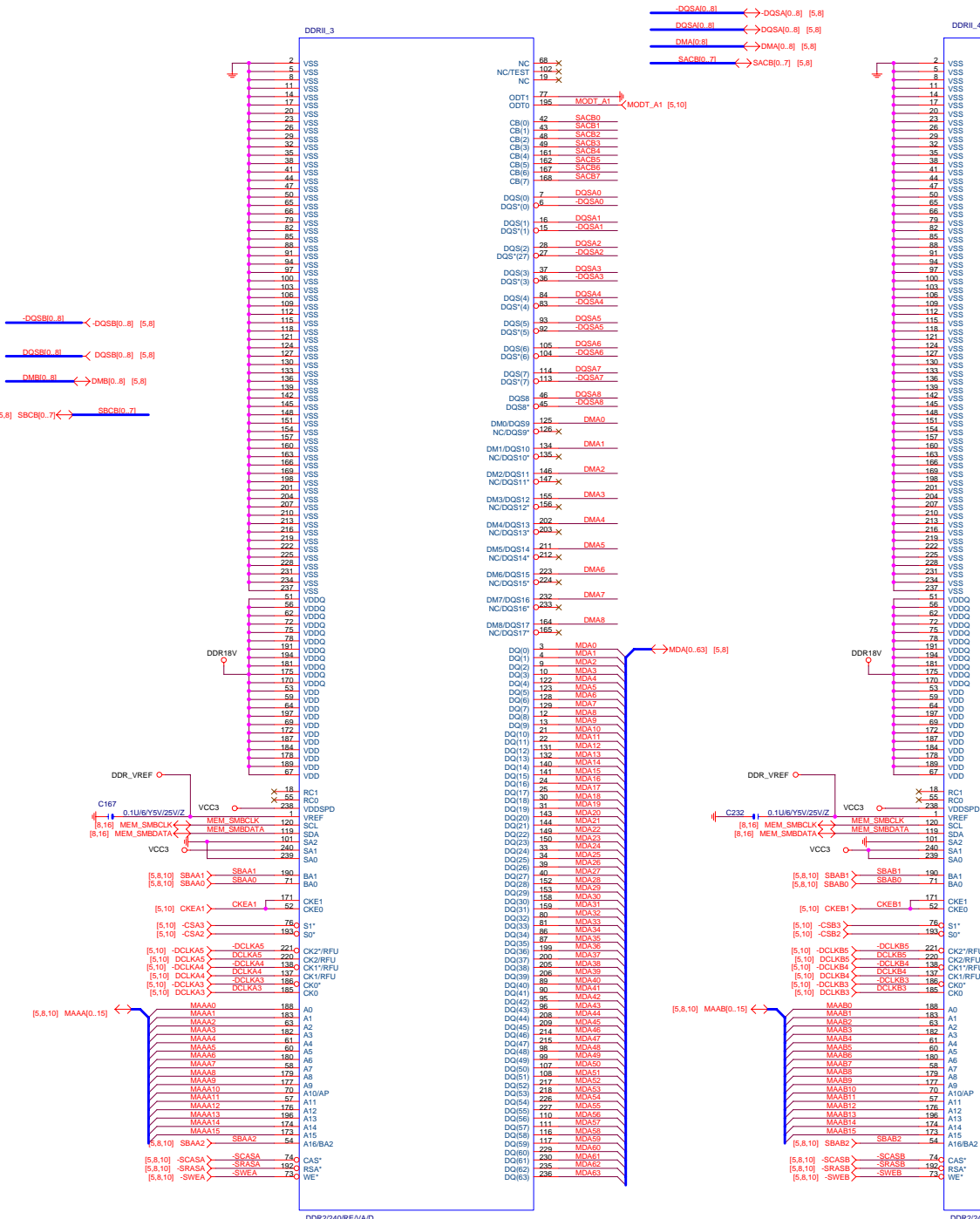


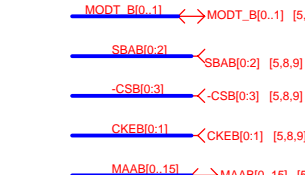
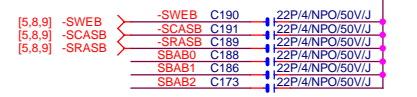
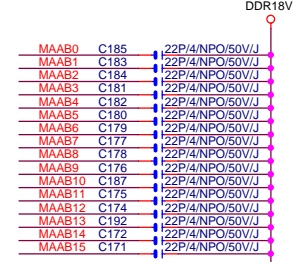
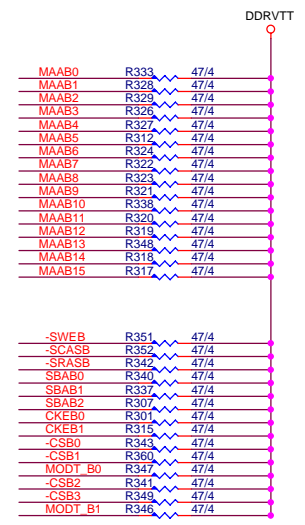
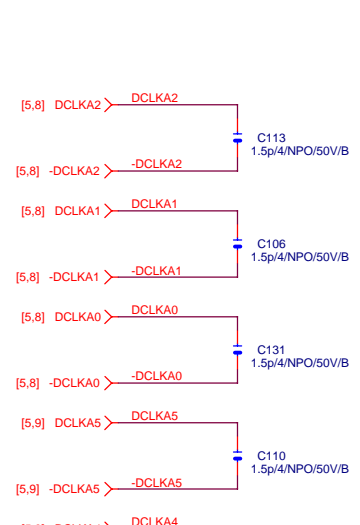
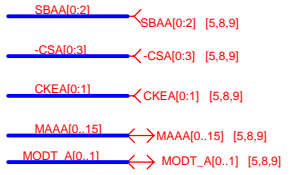
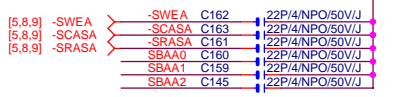
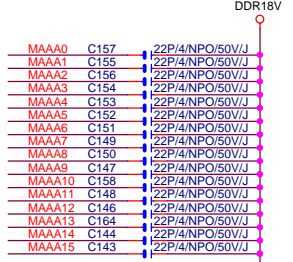
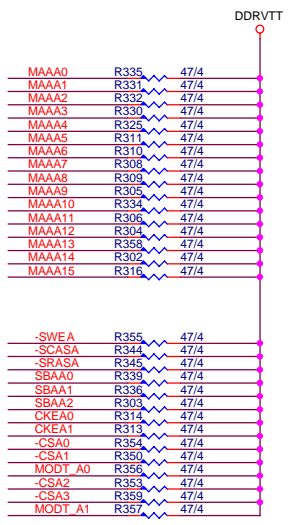
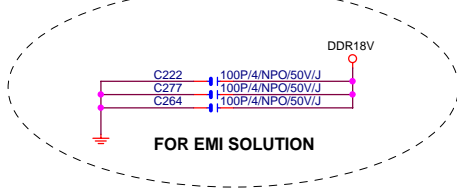
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



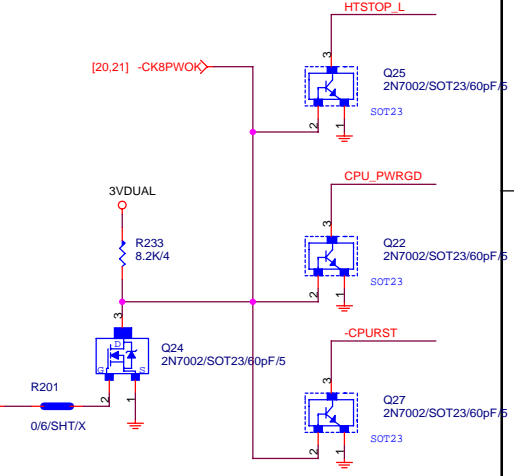
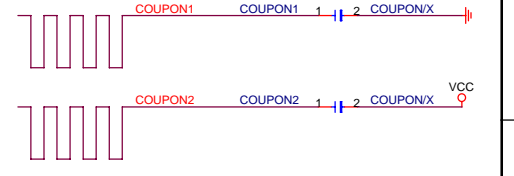
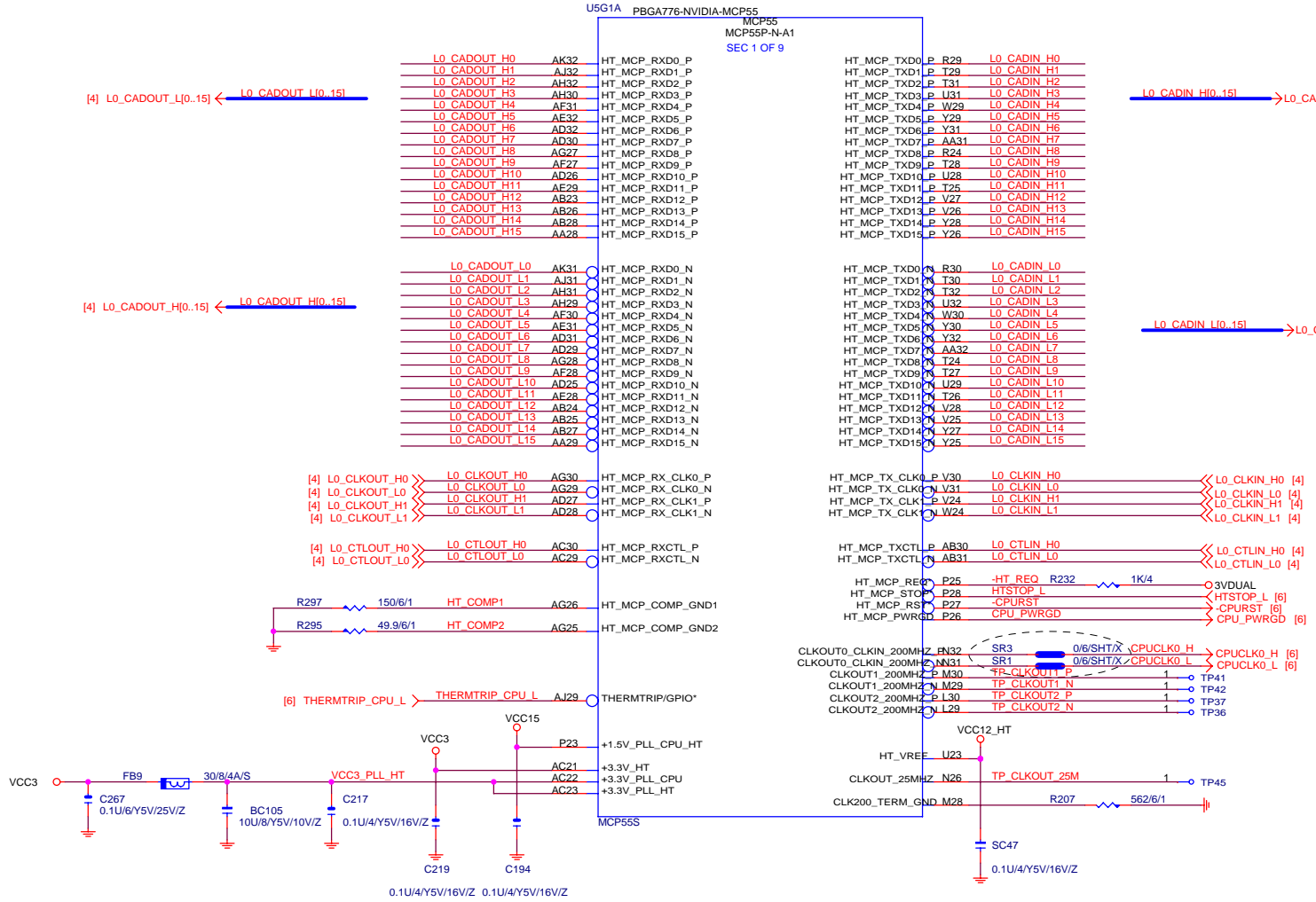
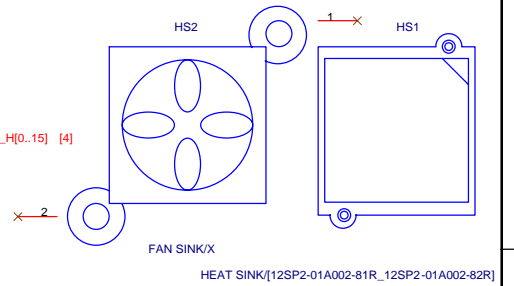


SIGNALYTES CORP.	
Title	
DDR2 CHANNEL A	
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N.B HEATSINK or FANSINK



GIGABYTE CORP.

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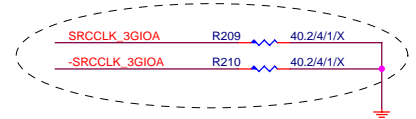
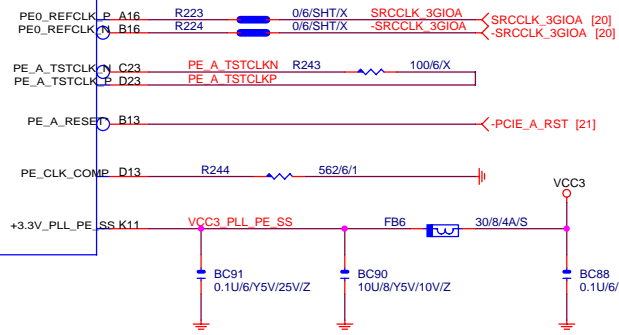
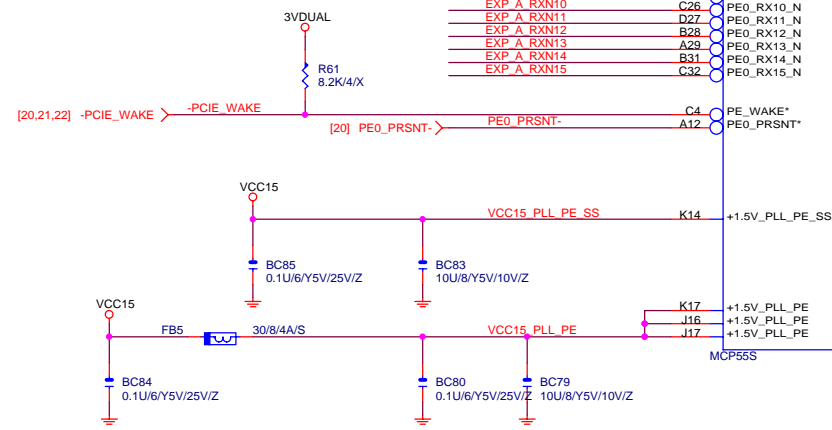
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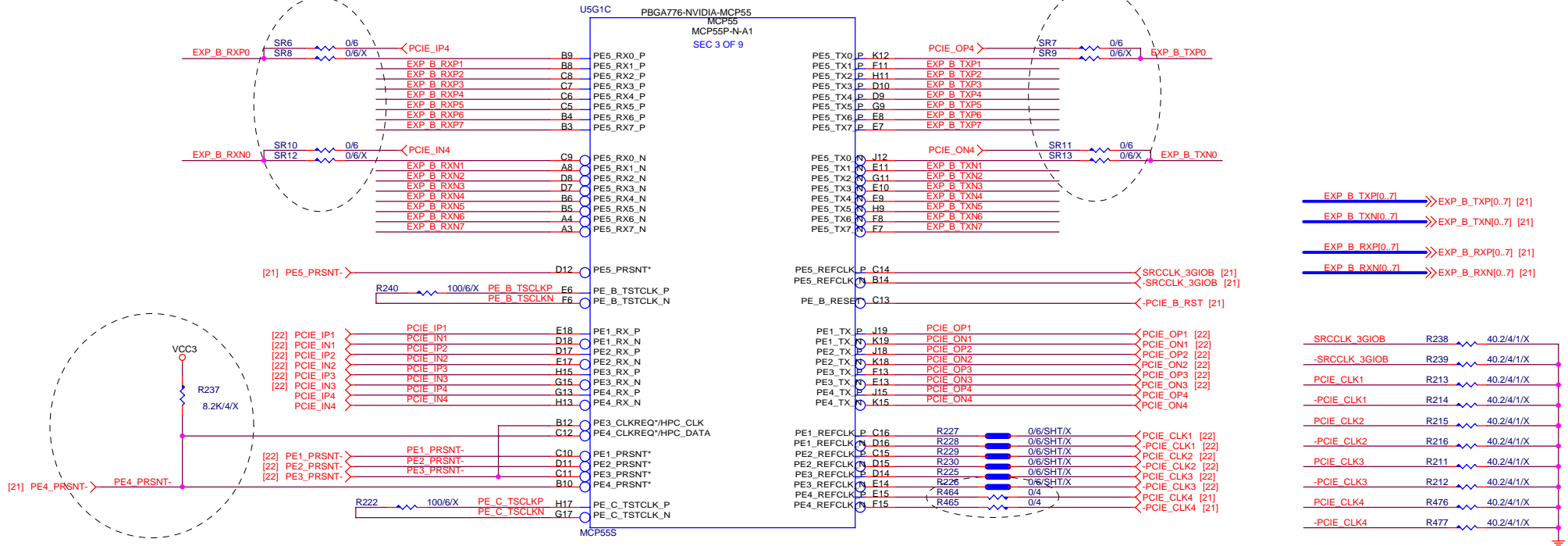
U5G1B PBGA776-NVIDIA-MCP55
MCP55
MCP55P-N-A1
SEC 2 OF 9

EXP_A_RXP0	B17	PE0_RX0_P	PE0_TX0_P	E19	EXP_A_TXP0
EXP_A_RXP1	B18	PE0_RX1_P	PE0_TX1_P	G19	EXP_A_TXP1
EXP_A_RXP2	D19	PE0_RX2_P	PE0_TX2_P	K20	EXP_A_TXP2
EXP_A_RXP3	D20	PE0_RX3_P	PE0_TX3_P	H21	EXP_A_TXP3
EXP_A_RXP4	A20	PE0_RX4_P	PE0_TX4_P	C21	EXP_A_TXP4
EXP_A_RXP5	B21	PE0_RX5_P	PE0_TX5_P	D21	EXP_A_TXP5
EXP_A_RXP6	B22	PE0_RX6_P	PE0_TX6_P	E22	EXP_A_TXP6
EXP_A_RXP7	D24	PE0_RX7_P	PE0_TX7_P	E23	EXP_A_TXP7
EXP_A_RXP8	A24	PE0_RX8_P	PE0_TX8_P	G23	EXP_A_TXP8
EXP_A_RXP9	B25	PE0_RX9_P	PE0_TX9_P	E24	EXP_A_TXP9
EXP_A_RXP10	B26	PE0_RX10_P	PE0_TX10_P	D25	EXP_A_TXP10
EXP_A_RXP11	C27	PE0_RX11_P	PE0_TX11_P	E26	EXP_A_TXP11
EXP_A_RXP12	C28	PE0_RX12_P	PE0_TX12_P	E27	EXP_A_TXP12
EXP_A_RXP13	A28	PE0_RX13_P	PE0_TX13_P	D28	EXP_A_TXP13
EXP_A_RXP14	A31	PE0_RX14_P	PE0_TX14_P	B29	EXP_A_TXP14
EXP_A_RXP15	C31	PE0_RX15_P	PE0_TX15_P	B30	EXP_A_TXP15
EXP_A_RXN0	C17	PE0_RX0_N	PE0_TX0_N	E19	EXP_A_TXN0
EXP_A_RXN1	C18	PE0_RX1_N	PE0_TX1_N	H19	EXP_A_TXN1
EXP_A_RXN2	C19	PE0_RX2_N	PE0_TX2_N	J20	EXP_A_TXN2
EXP_A_RXN3	C20	PE0_RX3_N	PE0_TX3_N	J21	EXP_A_TXN3
EXP_A_RXN4	B20	PE0_RX4_N	PE0_TX4_N	E21	EXP_A_TXN4
EXP_A_RXN5	C21	PE0_RX5_N	PE0_TX5_N	E21	EXP_A_TXN5
EXP_A_RXN6	C22	PE0_RX6_N	PE0_TX6_N	D22	EXP_A_TXN6
EXP_A_RXN7	C24	PE0_RX7_N	PE0_TX7_N	E23	EXP_A_TXN7
EXP_A_RXN8	B24	PE0_RX8_N	PE0_TX8_N	H23	EXP_A_TXN8
EXP_A_RXN9	C25	PE0_RX9_N	PE0_TX9_N	F24	EXP_A_TXN9
EXP_A_RXN10	C26	PE0_RX10_N	PE0_TX10_N	E25	EXP_A_TXN10
EXP_A_RXN11	D27	PE0_RX11_N	PE0_TX11_N	E26	EXP_A_TXN11
EXP_A_RXN12	B28	PE0_RX12_N	PE0_TX12_N	F27	EXP_A_TXN12
EXP_A_RXN13	A29	PE0_RX13_N	PE0_TX13_N	E28	EXP_A_TXN13
EXP_A_RXN14	B31	PE0_RX14_N	PE0_TX14_N	C29	EXP_A_TXN14
EXP_A_RXN15	C32	PE0_RX15_N	PE0_TX15_N	C30	EXP_A_TXN15

EXP_A_TXP[0..15] >>> EXP_A_TXP[0..15] [20]
 EXP_A_TXN[0..15] >>> EXP_A_TXN[0..15] [20]
 EXP_A_RXP[0..15] >>> EXP_A_RXP[0..15] [20]
 EXP_A_RXN[0..15] >>> EXP_A_RXN[0..15] [20]



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EXP_B_TXP[0..7] >>> EXP_B_TXP[0..7] [21]
 EXP_B_TXN[0..7] >>> EXP_B_TXN[0..7] [21]
 EXP_B_RXP[0..7] >>> EXP_B_RXP[0..7] [21]
 EXP_B_RXN[0..7] >>> EXP_B_RXN[0..7] [21]

SRCLK_3GIOB R238 40.2/4/1/X
 -SRCCLK_3GIOB R239 40.2/4/1/X
 PCIE_CLK1 R213 40.2/4/1/X
 -PCIE_CLK1 R214 40.2/4/1/X
 PCIE_CLK2 R215 40.2/4/1/X
 -PCIE_CLK2 R216 40.2/4/1/X
 PCIE_CLK3 R211 40.2/4/1/X
 -PCIE_CLK3 R212 40.2/4/1/X
 PCIE_CLK4 R476 40.2/4/1/X
 -PCIE_CLK4 R477 40.2/4/1/X

GIGABYTE CORP.		
Title MCP55 PCIe X8 , X1		
Size Custom	Document Number GA-M55S-S3	Rev 1.0
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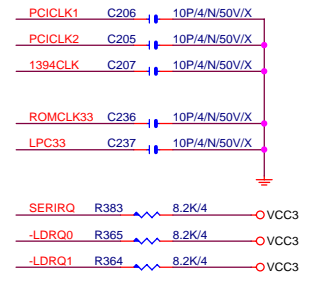
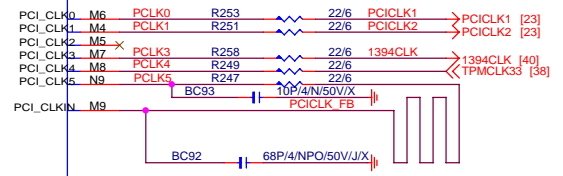
A

U5G1D PBGA776-NVIDIA-MCP55
MCP55
MCP55P-N-A1
SEC 4 OF 9

AD0	AA4	PCI_AD0
AD1	AB3	PCI_AD1
AD2	AB2	PCI_AD2
AD3	AA3	PCI_AD3
AD4	Y10	PCI_AD4
AD5	AA2	PCI_AD5
AD6	Y9	PCI_AD6
AD7	Y8	PCI_AD7
AD8	Y7	PCI_AD8
AD9	Y4	PCI_AD9
AD10	Y5	PCI_AD10
AD11	Y1	PCI_AD11
AD12	Y3	PCI_AD12
AD13	Y2	PCI_AD13
AD14	V9	PCI_AD14
AD15	V8	PCI_AD15
AD16	U2	PCI_AD16
AD17	U3	PCI_AD17
AD18	U8	PCI_AD18
AD19	T9	PCI_AD19
AD20	T7	PCI_AD20
AD21	T8	PCI_AD21
AD22	T6	PCI_AD22
AD23	T3	PCI_AD23
AD24	T1	PCI_AD24
AD25	T2	PCI_AD25
AD26	R3	PCI_AD26
AD27	R4	PCI_AD27
AD28	T5	PCI_AD28
AD29	P9	PCI_AD29
AD30	P7	PCI_AD30
AD31	P8	PCI_AD31

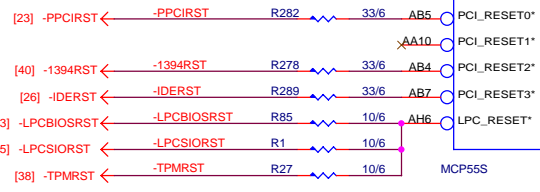
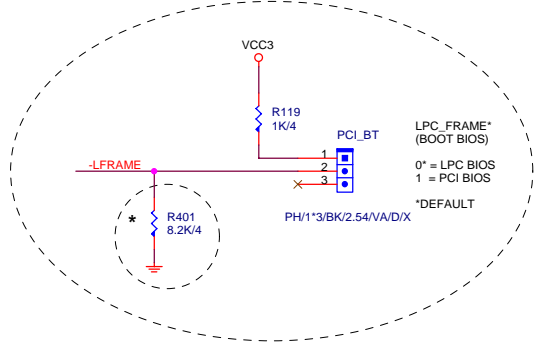
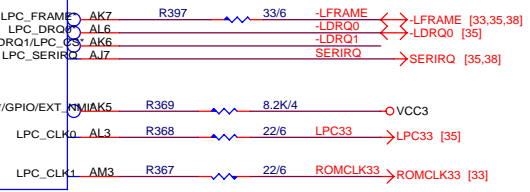
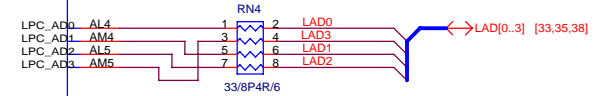
PCI_REQ0	N4	-REQ0
PCI_REQ1	P3	-REQ1
PCI_REQ2*/GPIO	P4	-REQ2
PCI_REQ3*/GPIO	P5	-REQ3
PCI_REQ4*/FANRPM	P6	-REQ4
PCI_GNT0	M1	-GNT0
PCI_GNT1	M2	-GNT1
PCI_GNT2*/GPIO	N2	-GNT2
PCI_GNT3*/GPIO	N3	-GNT3
PCI_GNT4*/RS232_D	P2	-GNT4

PCI_INT0	L7	-INTA	<-INTA [23]
PCI_INT1	L5	-INTB	<-INTB [23]
PCI_INT2	M3	-INTC	<-INTC [23,40]
PCI_INT3	L3	-INTD	<-INTD [23]



[23,40] -C_BE0	<-C_BE0	Y6	PCI_CBE0*
[23,40] -C_BE1	<-C_BE1	V9	PCI_CBE1*
[23,40] -C_BE2	<-C_BE2	V2	PCI_CBE2*
[23,40] -C_BE3	<-C_BE3	T4	PCI_CBE3*

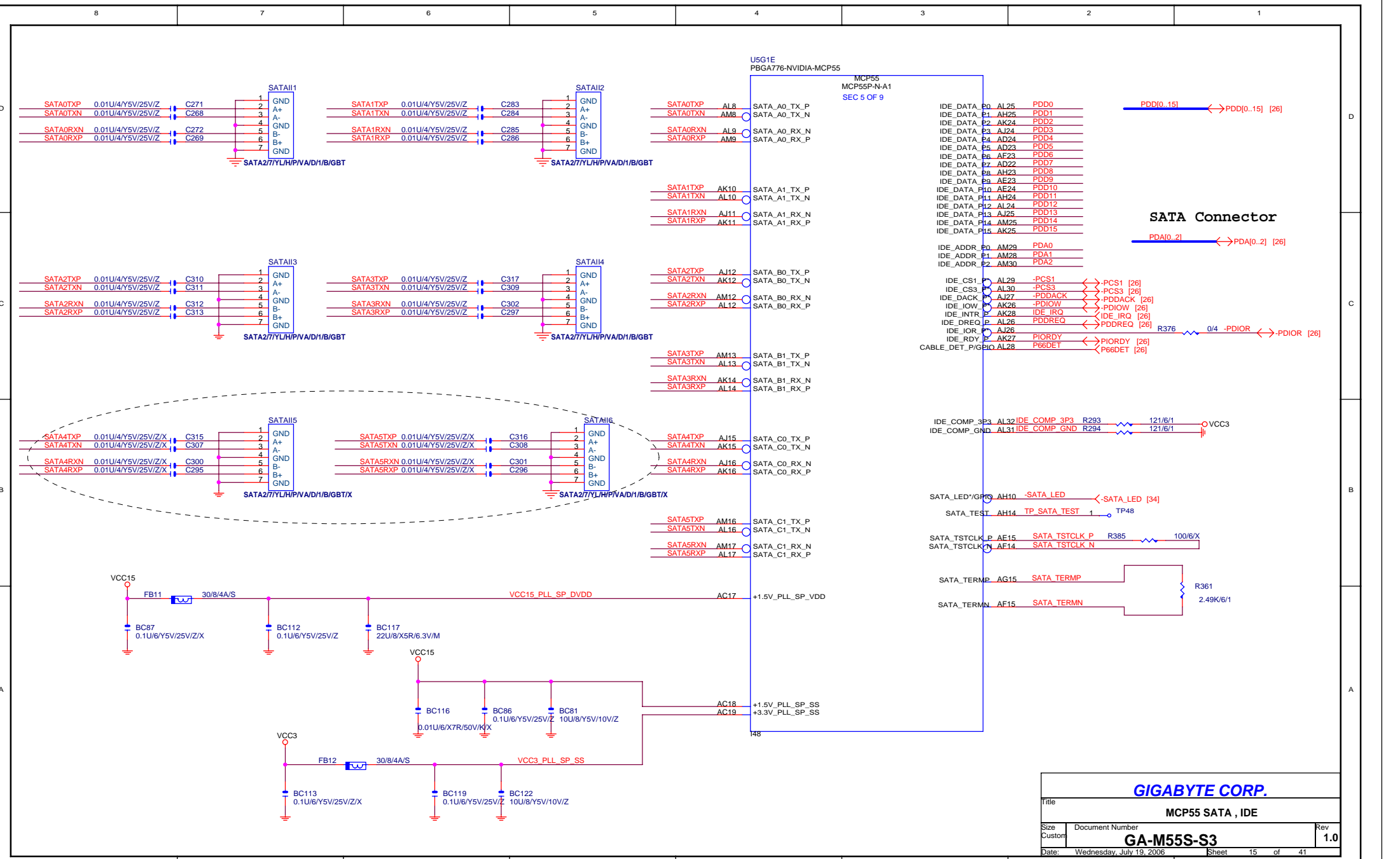
[23,40] -FRAME	<-FRAME	U4	PCI_FRAME*
[23,40] -IRDY	<-IRDY	V3	PCI_IRDY*
[23,40] -TRDY	<-TRDY	V4	PCI_TRDY*
[23,40] -STOP	<-STOP	W4	PCI_STOP*
[23,40] -DEVSEL	<-DEVSEL	W3	PCI_DEVSEL*
[23,40] PAR	<-PAR	V7	PCI_PAR
[23,40] -PERR	<-PERR	V5	PCI_PERR*/GPIO
[23,40] -SERR	<-SERR	V6	PCI_SERR*
[23,40] -PCIPME	<-PCIPME	AB6	PCI_PME*/GPIO



GIGABYTE CORP.

MCP55 PCI

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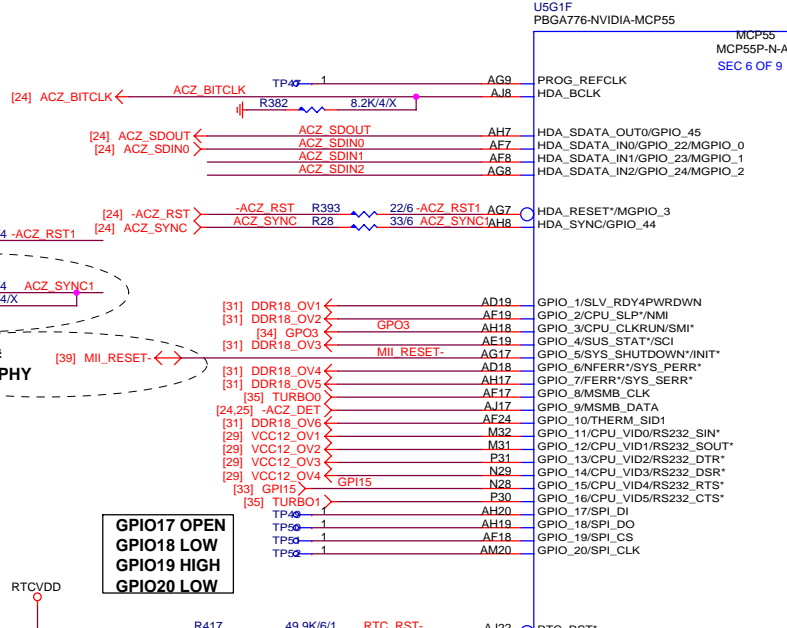


GIGABYTE CORP.		
Title MCP55 SATA , IDE		
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HDA_RST* (MAC 0)
1* = RGMII
0 = MII

HDA_SYNC (SIO CLK)
1* = 24MHz
0 = 14.318MHz

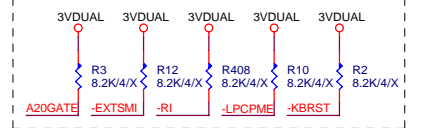
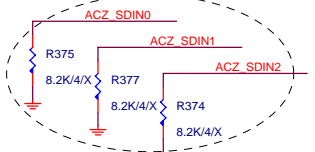
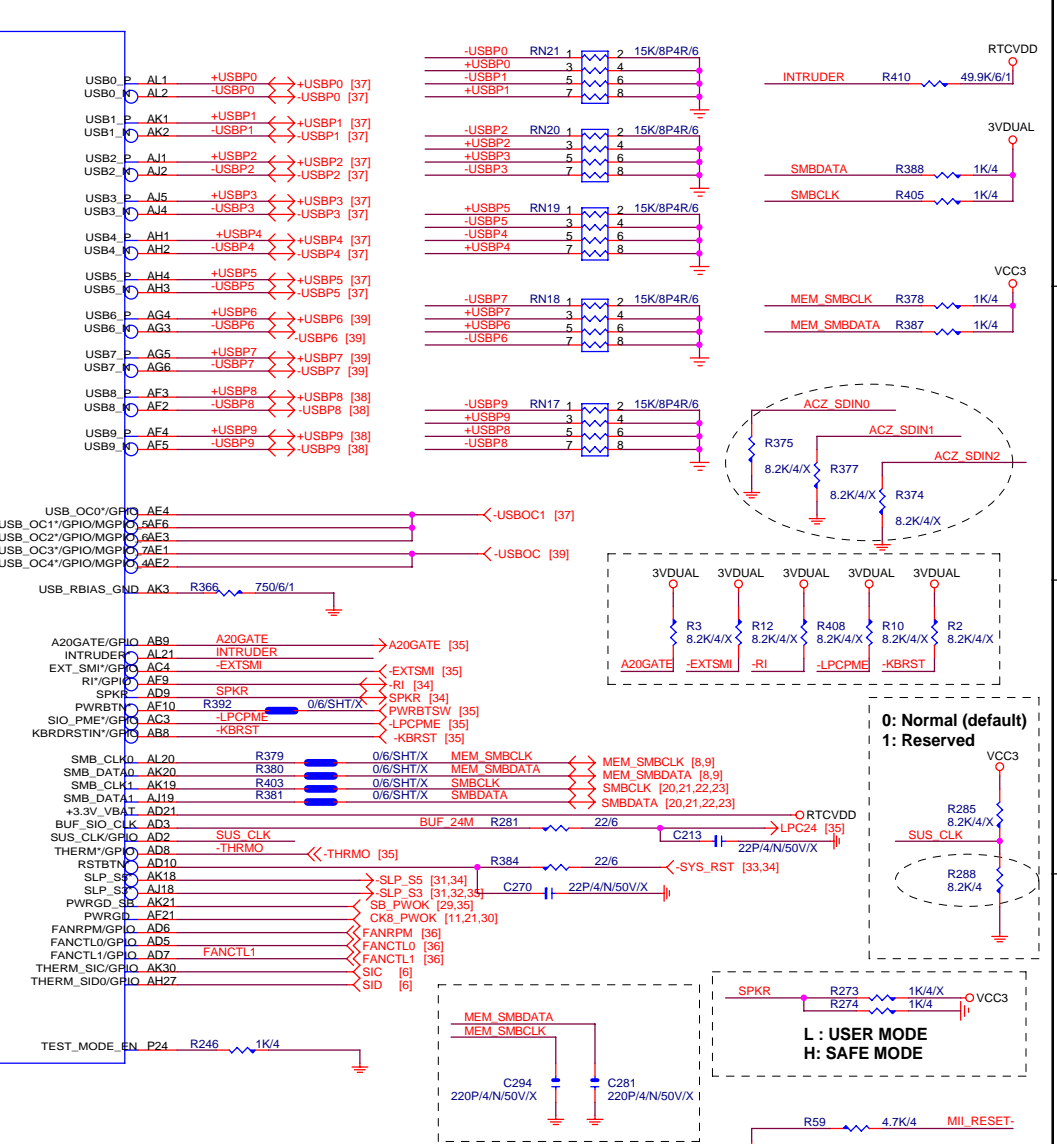
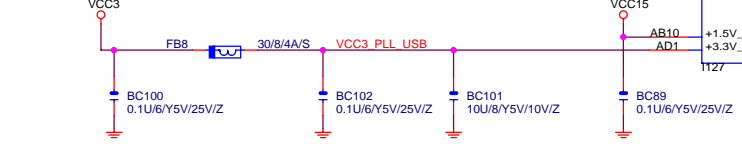
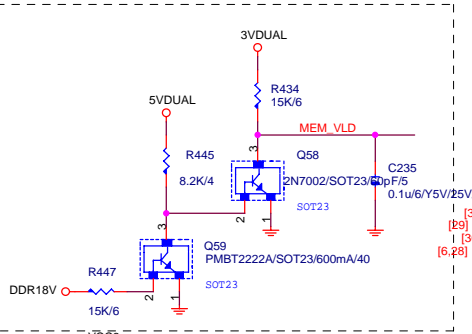
*DEFAULT



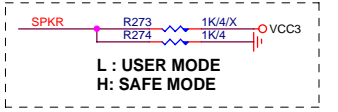
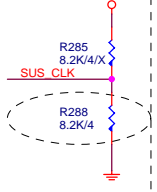
GPI05/INIT# FOR RGMII PHY

[39] MII_RESET- <->

GPIO17 OPEN
GPIO18 LOW
GPIO19 HIGH
GPIO20 LOW



0: Normal (default)
1: Reserved



GIGABYTE CORP.		
MCP55 AUDIO , USB , MISC		
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03013
PBGAT76-NVIDIA-MCP55

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[39] MII_RXD0	F3	RGMII0_RXD0/II0_RXD0
[39] MII_RXD1	F5	RGMII0_RXD1/II0_RXD1
[39] MII_RXD2	E2	RGMII0_RXD2/II0_RXD2
[39] MII_RXD3	D1	RGMII0_RXD3/II0_RXD3
[39] RXCLK	E1	RGMII0_RXC/II0_RXCLK
[39] RXCTL	F4	RGMII0_RXCTL/II0_RXDV

RGMII0_TXD0/II0_TXD0D3	LR29	22/6	→ MII_TXD0 [39]
RGMII0_TXD1/II0_TXD1E4	LR30	22/6	→ MII_TXD1 [39]
RGMII0_TXD2/II0_TXD2B1	LR35	22/6	→ MII_TXD2 [39]
RGMII0_TXD3/II0_TXD3C2	LR34	22/6	→ MII_TXD3 [39]
RGMII0_TXC/II0_TXCLKB2	LR33	22/6	→ TXCLK [39]
RGMII0_TXCTL/II0_TXEND4	LR32	22/6	→ TXCTL [39]

RGMII0/II0_MDC_C1		→ MDC [39]	
RGMII0/II0_MDIO_D2		→ MDIO [39]	
RGMII0/II0_PWRDWN/GPICK3	1	TP35	
BUF0_25MHZ_D5	LR31	22/6/X	← MII_CLK25 [39]

RGMII1_TXD0_H4	×
RGMII1_TXD1_G7	×
RGMII1_TXD2_G3	×
RGMII1_TXD3_G8	×
RGMII1_TXC_G5	×
RGMII1_TXCTL_H3	×

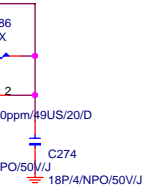
TP 進入限制區

RGMII1_MDC_H2	LR50	8.2K/4	→
RGMII1_MDIO_H1			
RGMII1_PWRDWN/GPIOK4	1	TP39	
BUF1_25MHZ_E5	1	TP21	

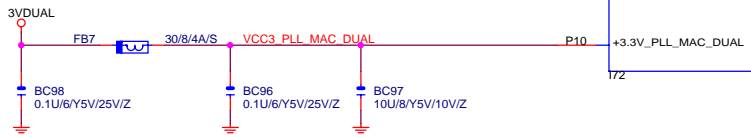
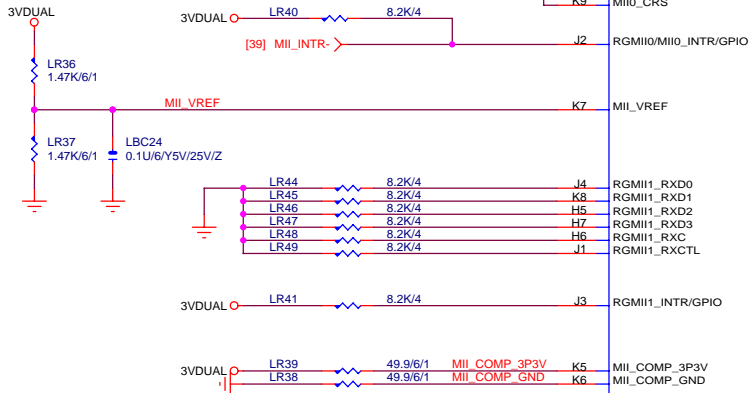
JTAG_TCK_M25	JTAG_TCK	R208	8.2K/4	→
JTAG_TDI_M26	1	TP43		
JTAG_TDO_M27	1	TP40		
JTAG_TMS_M23	1	TP44		
JTAG_TRST_M24	1	TP46		

XTALIN_AJ23	XTALIN		
XTALOUT_AK23	XTALOUT		

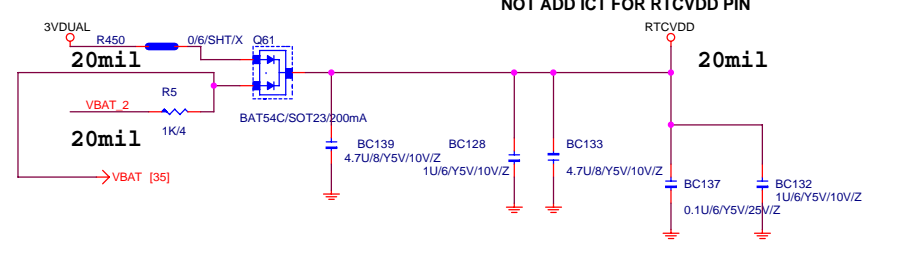
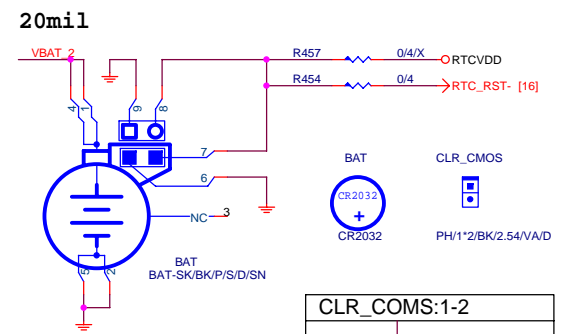
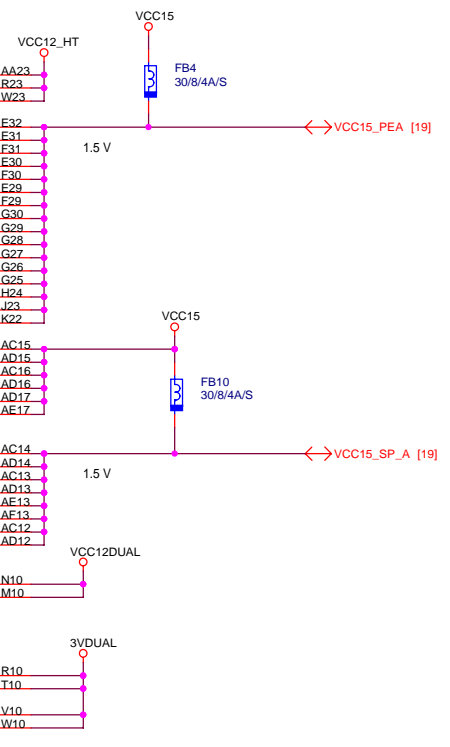
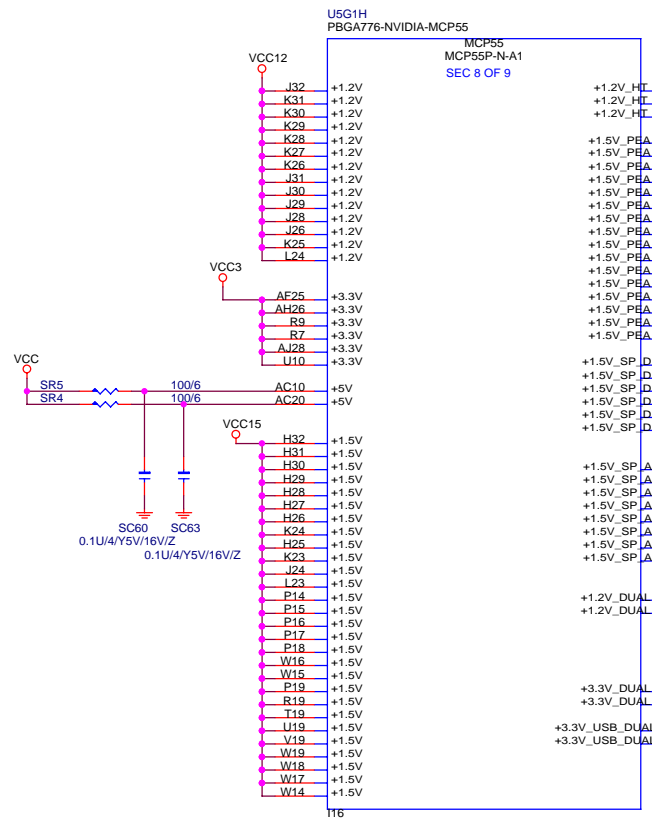
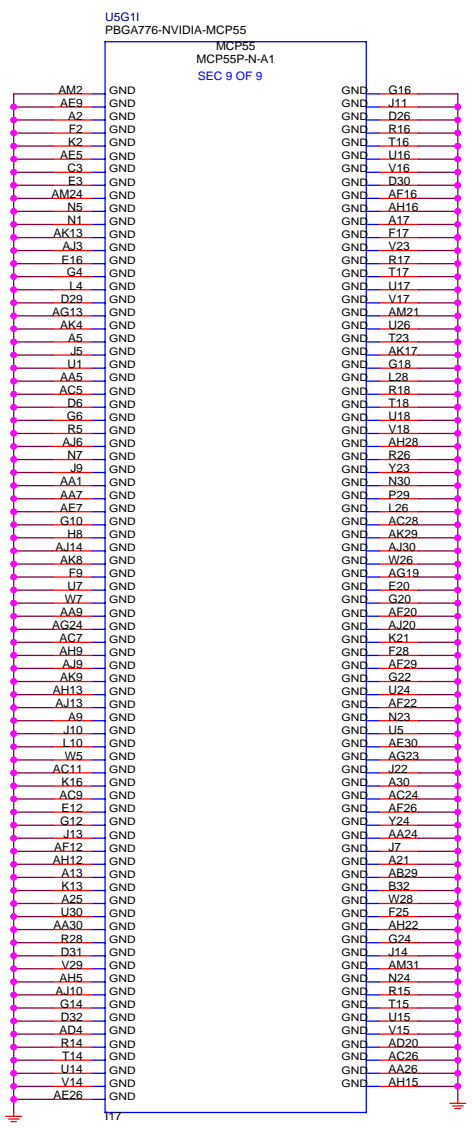
XTALIN_RTC_AL22	RTC_XI		
XTALOUT_RTC_AK22	RTC_XO		



X2 SHW/D0.64*5.08*6.74



GIGABYTE CORP.		
Title MCP55 DUAL RGMII		
Size Custom	Document Number GA-M55S-S3	Rev 1.0
Date: Wednesday, July 19, 2006	Sheet 17	of 41



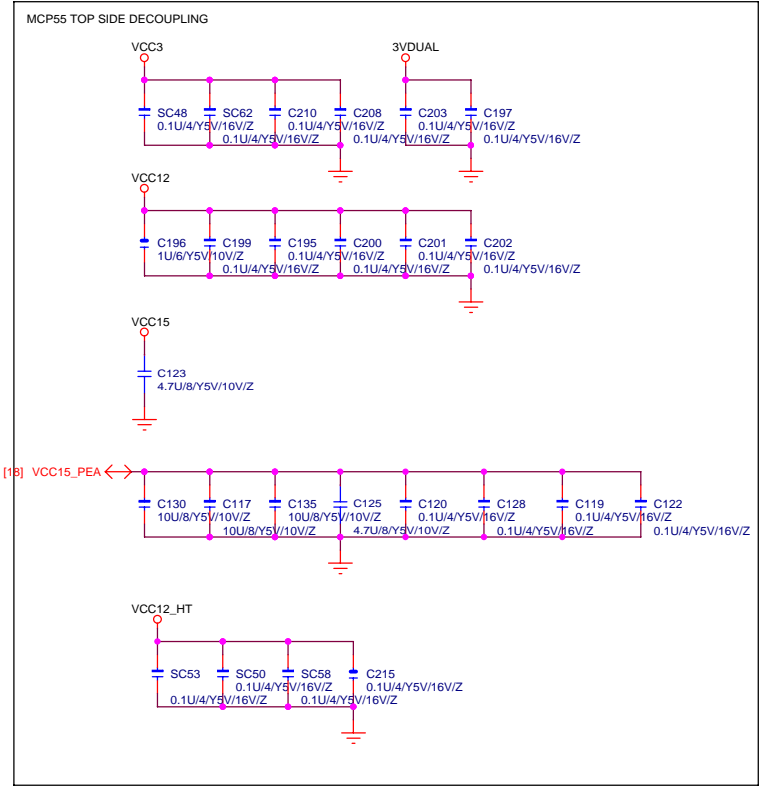
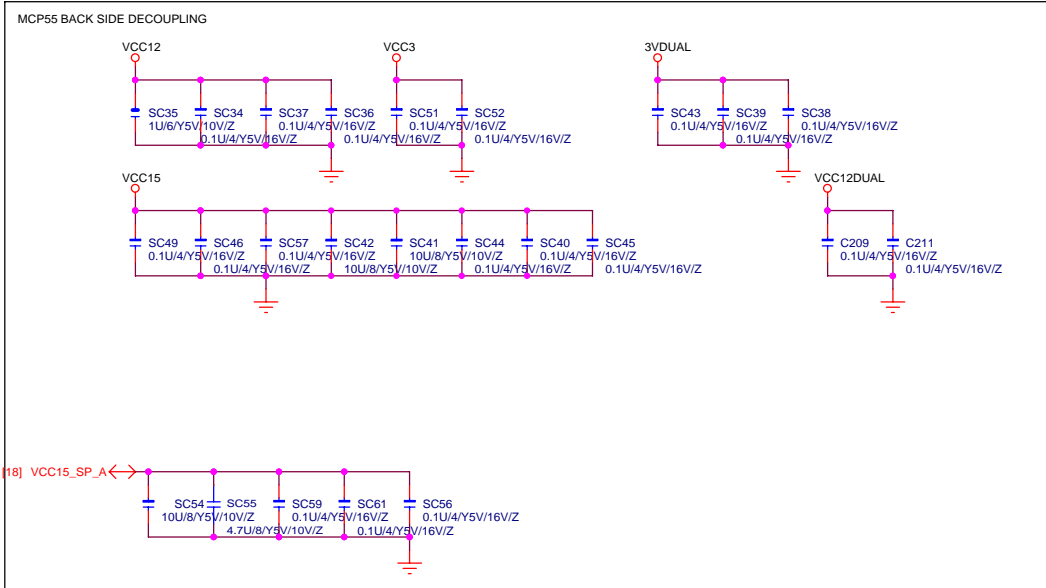
CLR_COMS:1-2	
SHORT	CLEAR CMOS
OPEN	NORMAL

GIGABYTE CORP.

Title: MCP55 PWR/GND

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MCP55 INTERNAL PULL-UP/PULL-DOWN

PIN	VOLTAGE
A20GATE/GPIO	+3.3V
EXT_SMI*/GPIO	+3.3V_DUAL
HDA_SDATA_IN0/GPIO_22/MGPIO_0	+3.3V_DUAL/GND
HDA_SDATA_IN1/GPIO_23/MGPIO_1	+3.3V_DUAL/GND
HDA_SDATA_IN2/GPIO_24/MGPIO_2	+3.3V_DUAL/GND
HDA_SDATA_OUT/GPIO_45	+3.3V_DUAL/GND
JTAG_TDI	+3.3V
JTAG_TMS	+3.3V
JTAG_TRST*	GND
KBRDRSTIN*/GPIO	+3.3V
PE_WAKE*	+3.3V_DUAL
SIO_PME*/GPIO	+3.3V_DUAL
THERM*/GPIO	+3.3V

GIGABYTE CORP.

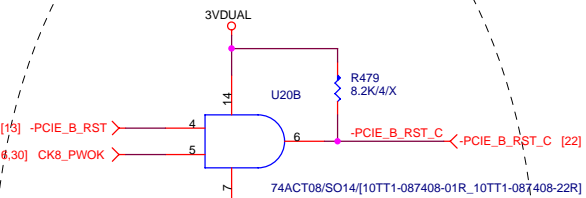
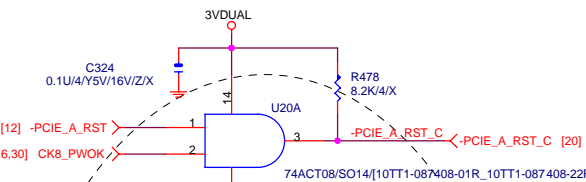
MCP55 DECOUPLING

Title	MCP55 DECOUPLING		Rev
Size	Document Number	GA-M55S-S3	
Custom			1.0
Date:	Wednesday, July 19, 2006	Sheet	19 of 41

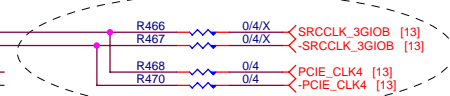
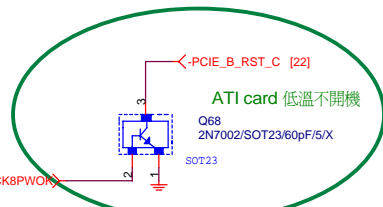
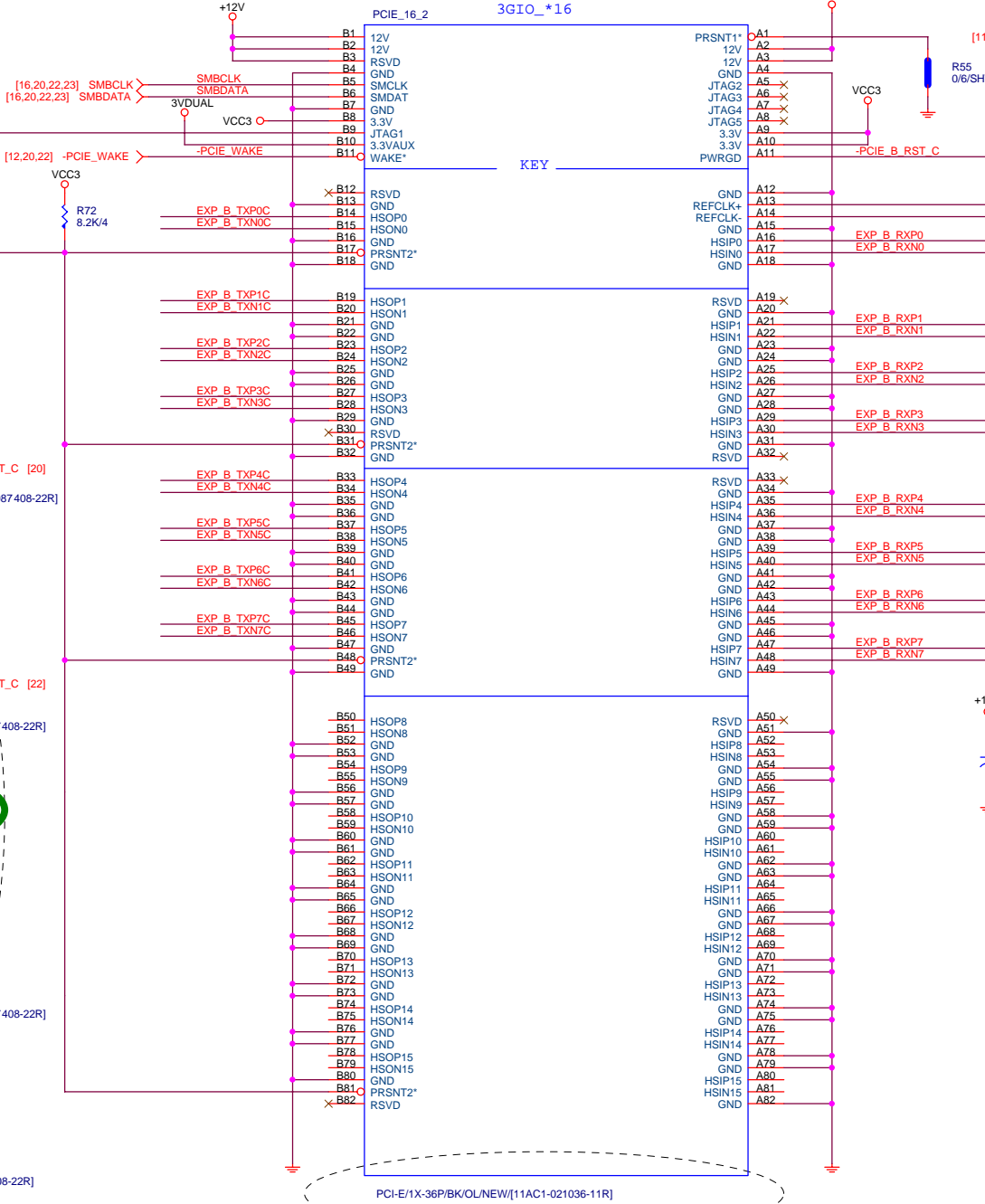
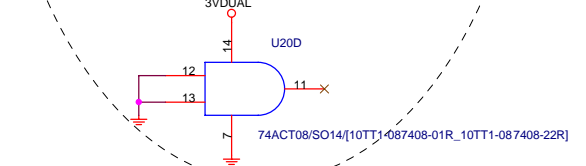
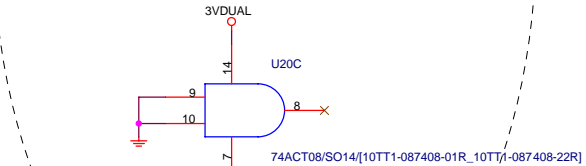
EXP_B_TXP0	C17	0.1U/4/Y5V/16V/Z	EXP_B_TXP0C
EXP_B_TXN0	C21	0.1U/4/Y5V/16V/Z	EXP_B_TXN0C
EXP_B_TXP1	C30	0.1U/4/Y5V/16V/Z/X	EXP_B_TXP1C
EXP_B_TXN1	C31	0.1U/4/Y5V/16V/Z/X	EXP_B_TXN1C
EXP_B_TXP2	C34	0.1U/4/Y5V/16V/Z/X	EXP_B_TXP2C
EXP_B_TXN2	C35	0.1U/4/Y5V/16V/Z/X	EXP_B_TXN2C
EXP_B_TXP3	C38	0.1U/4/Y5V/16V/Z/X	EXP_B_TXP3C
EXP_B_TXN3	C39	0.1U/4/Y5V/16V/Z/X	EXP_B_TXN3C
EXP_B_TXP4	C46	0.1U/4/Y5V/16V/Z/X	EXP_B_TXP4C
EXP_B_TXN4	C49	0.1U/4/Y5V/16V/Z/X	EXP_B_TXN4C
EXP_B_TXP5	C52	0.1U/4/Y5V/16V/Z/X	EXP_B_TXP5C
EXP_B_TXN5	C54	0.1U/4/Y5V/16V/Z/X	EXP_B_TXN5C
EXP_B_TXP6	C56	0.1U/4/Y5V/16V/Z/X	EXP_B_TXP6C
EXP_B_TXN6	C59	0.1U/4/Y5V/16V/Z/X	EXP_B_TXN6C
EXP_B_TXP7	C62	0.1U/4/Y5V/16V/Z/X	EXP_B_TXP7C
EXP_B_TXN7	C64	0.1U/4/Y5V/16V/Z/X	EXP_B_TXN7C

EXP_B_TXP0..7] >> EXP_B_TXP0.[0..7] [13]
 EXP_B_TXN0..7] >> EXP_B_TXN0.[0..7] [13]

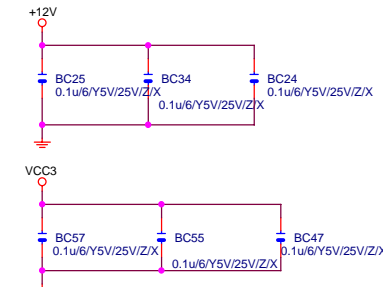
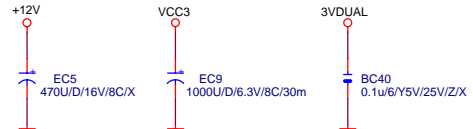
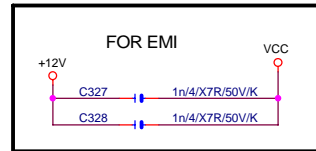
[13] PE5_PRSNT- >> R469 0/4/X
 [13] PE4_PRSNT- >> R471 0/4



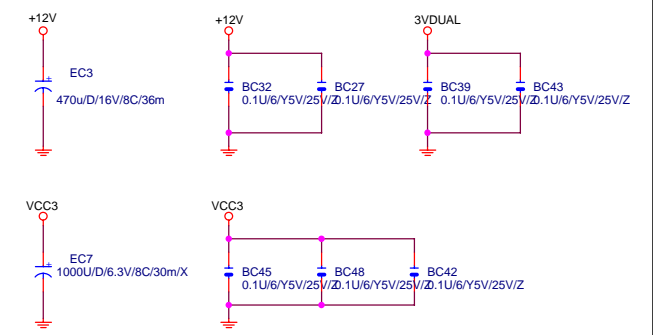
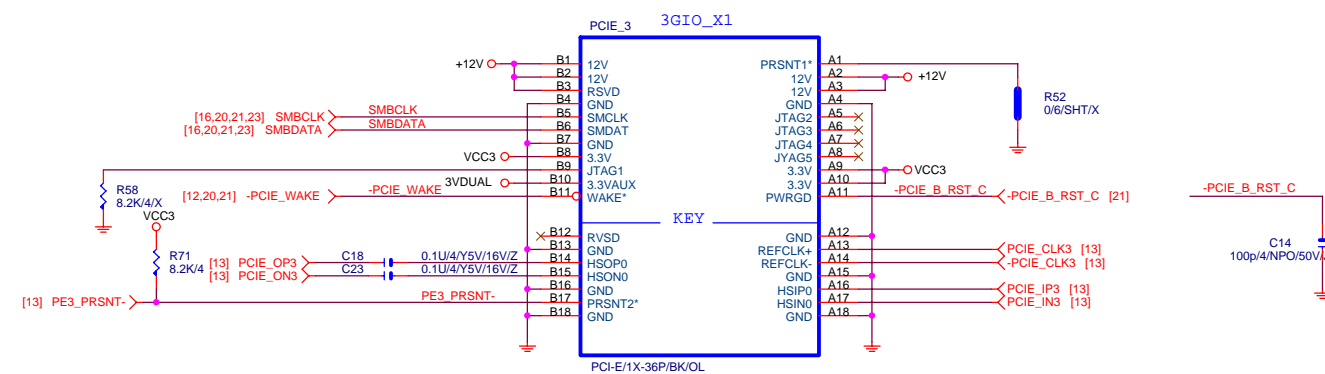
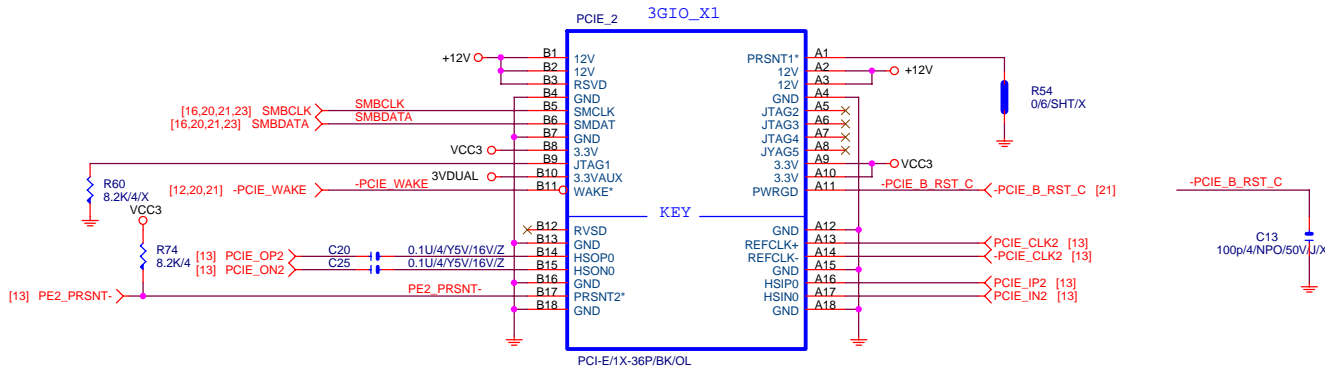
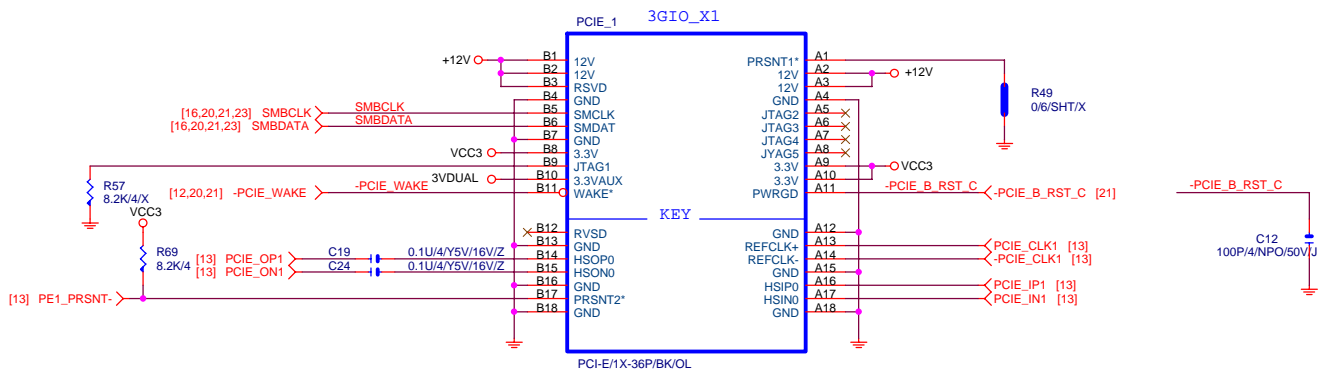
**VCC3 10% to Core power 90% < 30mS
 else, PCIE_RST add 74ACT08**



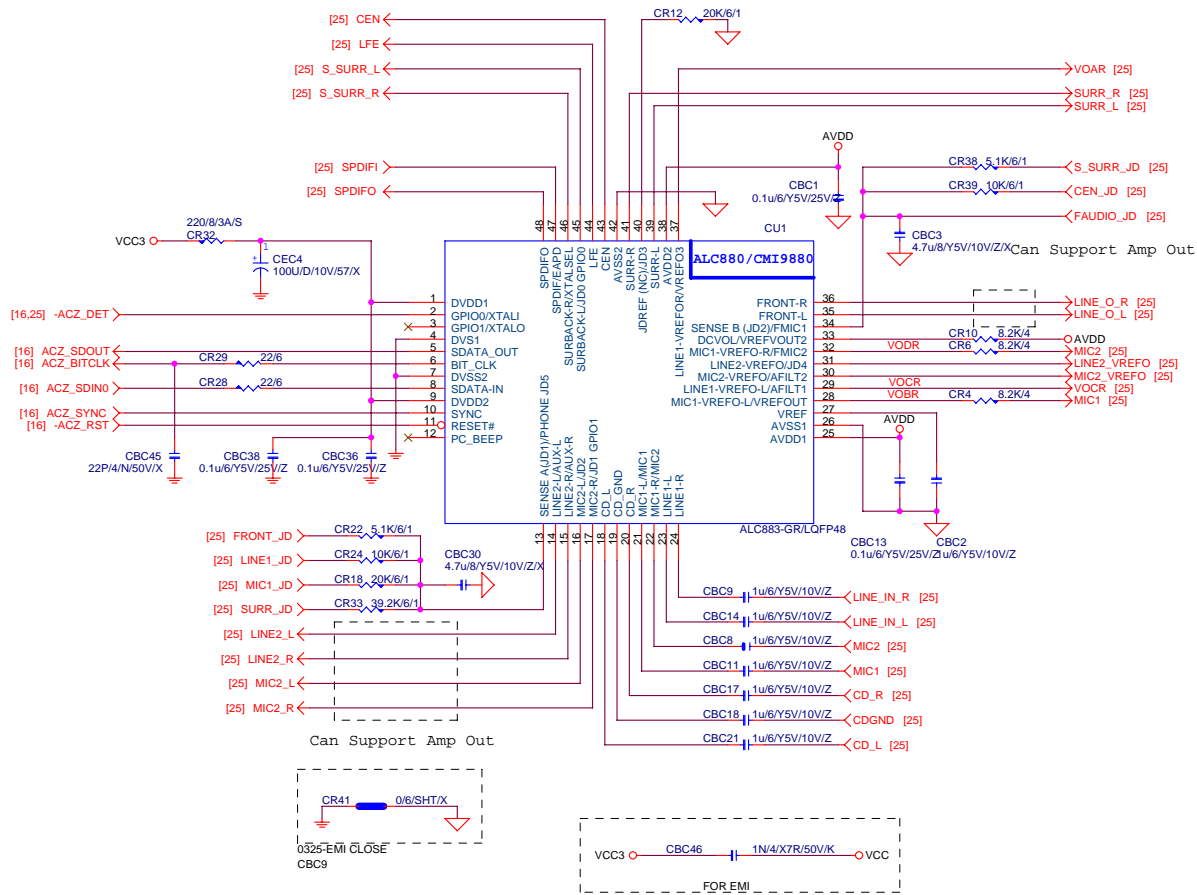
EXP_B_RXP0..7] >> EXP_B_RXP0.[0..7] [13]
 EXP_B_RXN0..7] >> EXP_B_RXN0.[0..7] [13]



GIGABYTE CORP.		
PCI EXPRESS X 8		
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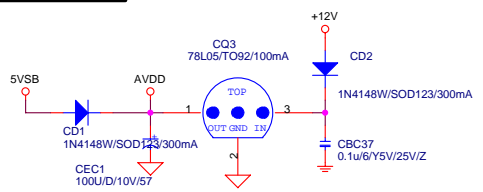


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Title		
PCI E SLOT 1, 2		
GA-M55S-S3		
Size	Document Number	Rev
B		1.0
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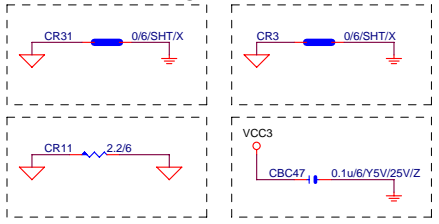


GIGABYTE CORP.		
Title		
AZALIA-ALC883		
Size	Document Number	Rev
Custom	GA-M55S-S3	1.0
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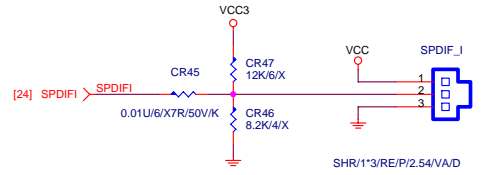
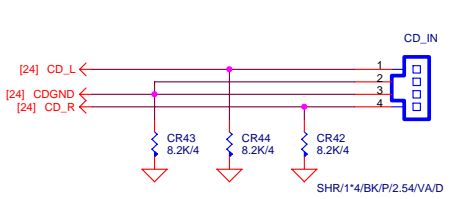
CODEC POWER/EMI PAD



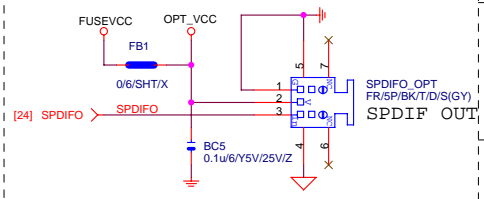
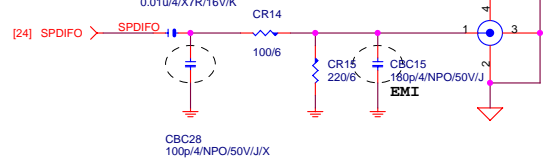
FOR EMI



CD IN

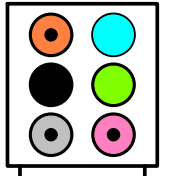


SPDIF

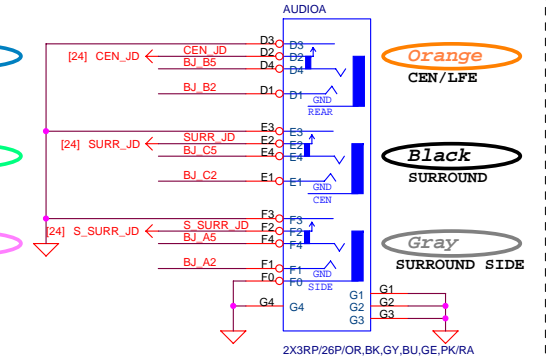
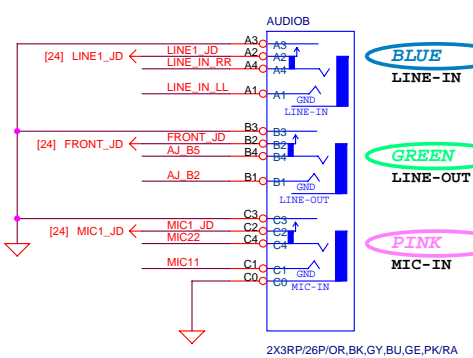


AZALIA JACK

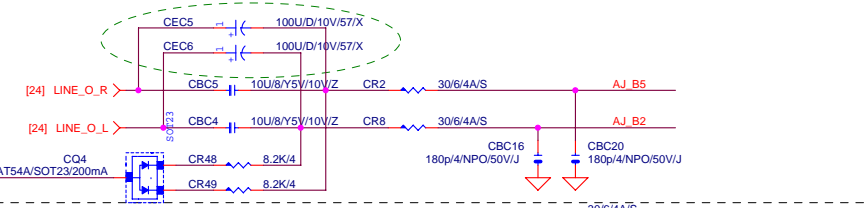
BTX AZALIA CONNECTOR



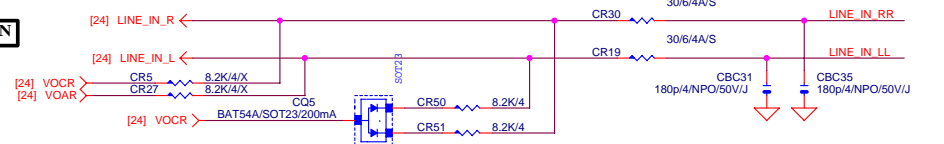
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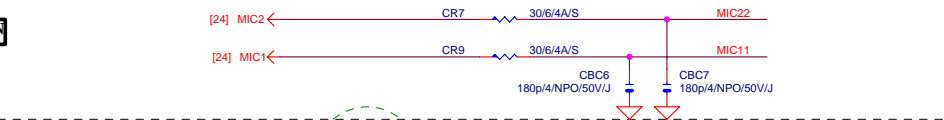
LINE-OUT



LINE-IN



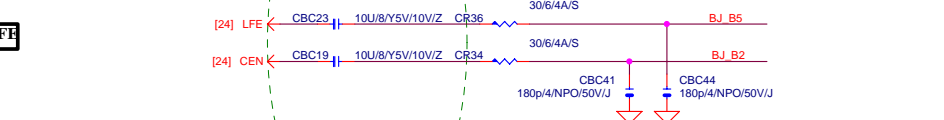
MIC-IN



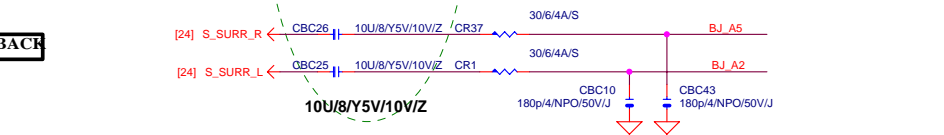
SURROUND



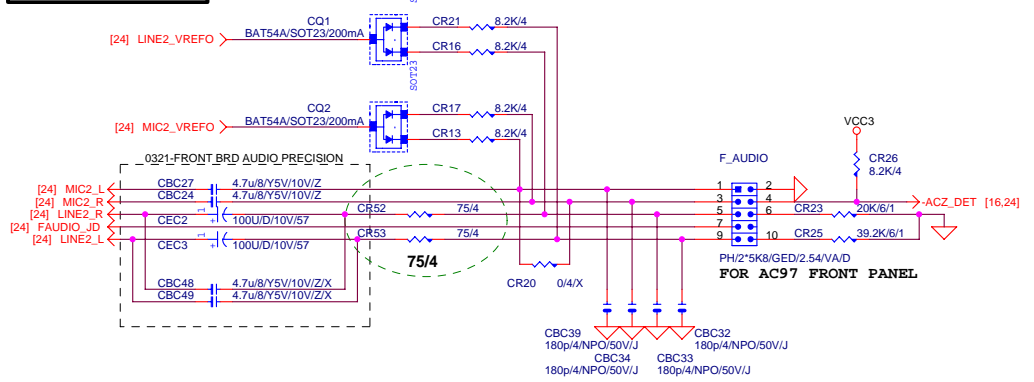
CEN/LFE



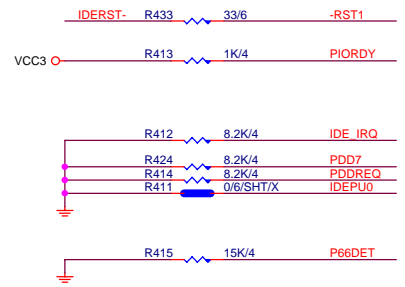
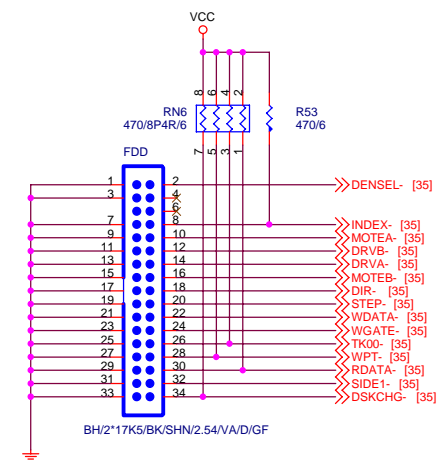
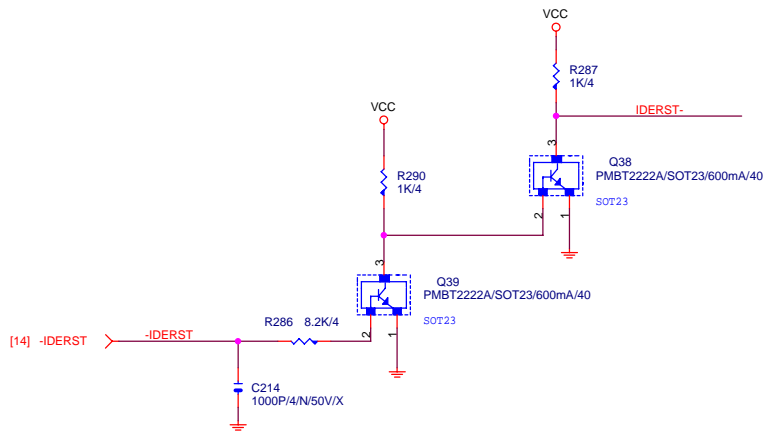
SURR BACK



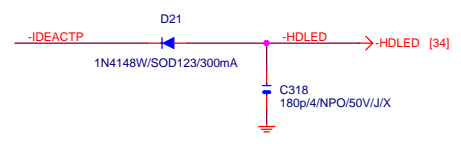
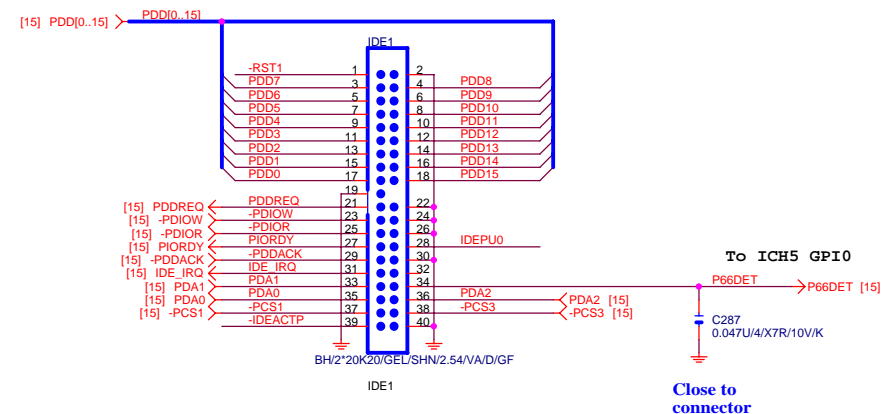
AZALIA FRONT PANEL



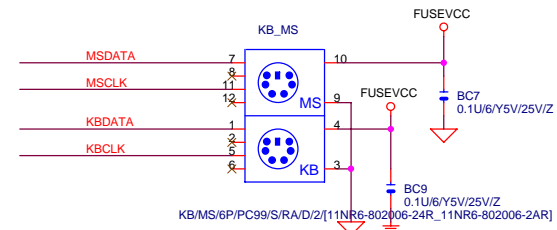
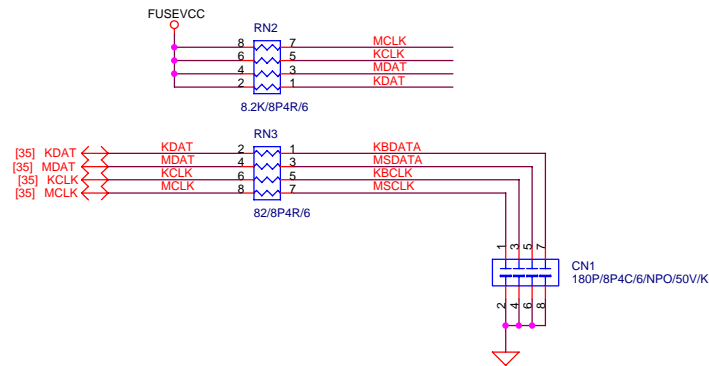
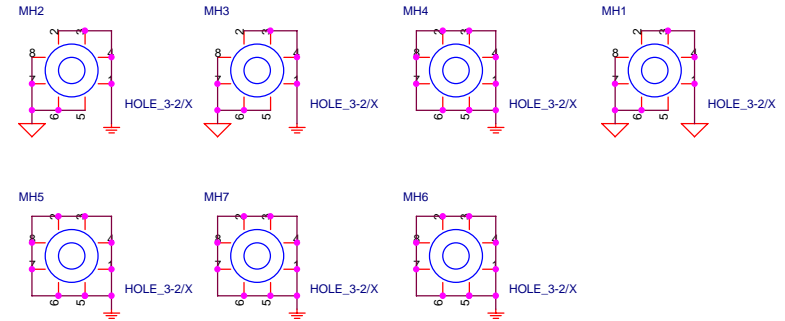
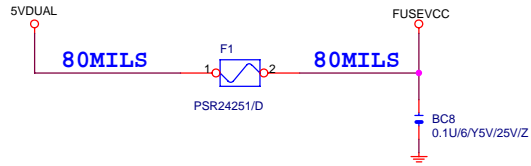
GIGABYTE CORP.		
AUDIO JACK		
GA-M55S-S3		
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PRIMARY IDE CONNECTOR

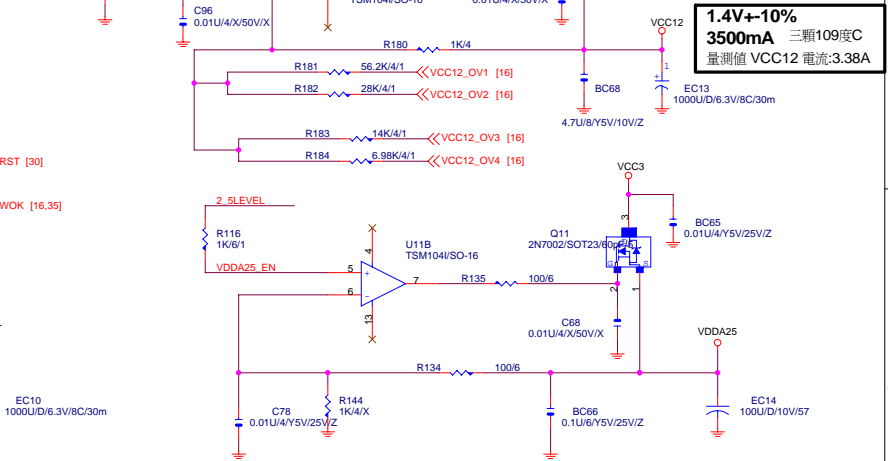
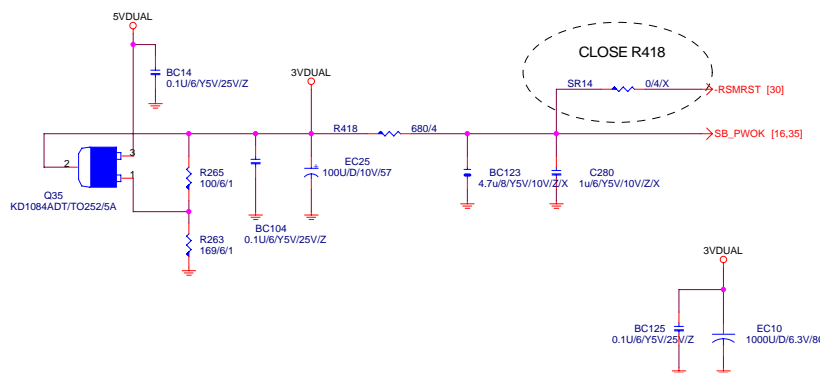
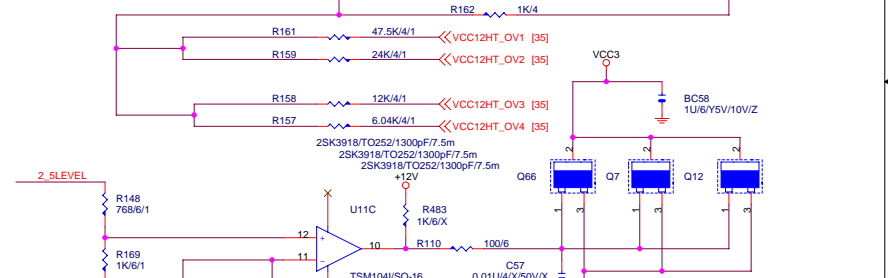
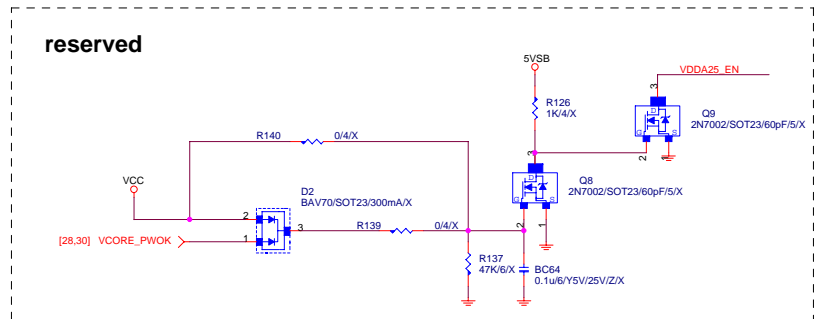
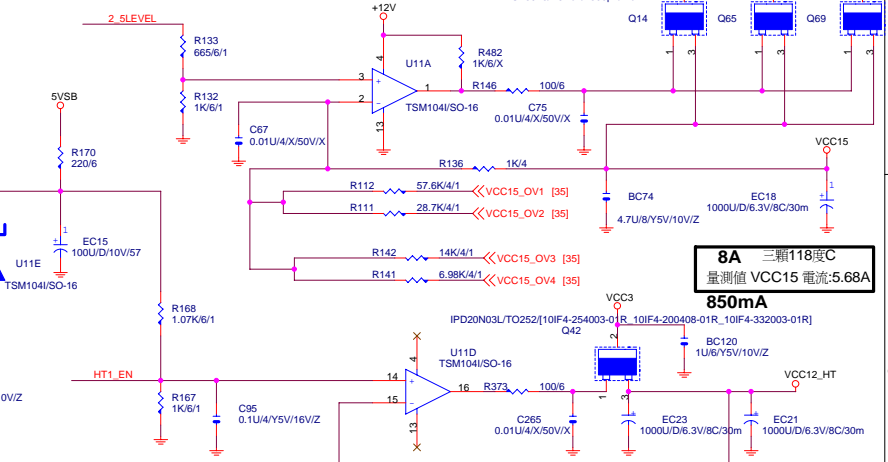
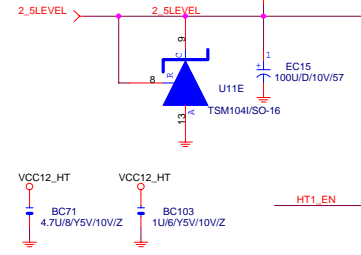
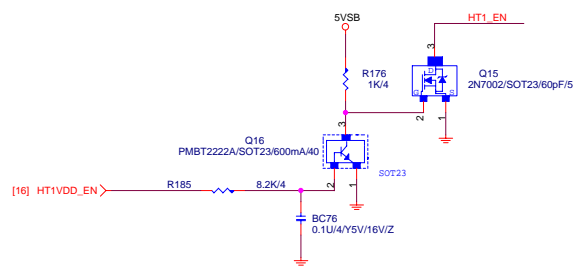
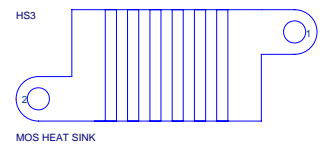
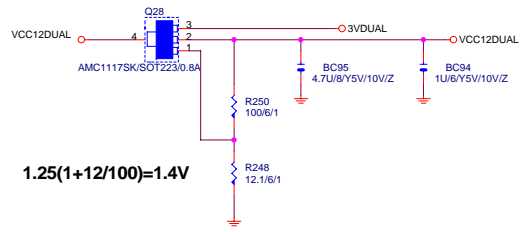


GIGABYTE CORP.		
Title IDE CONNECTOR		
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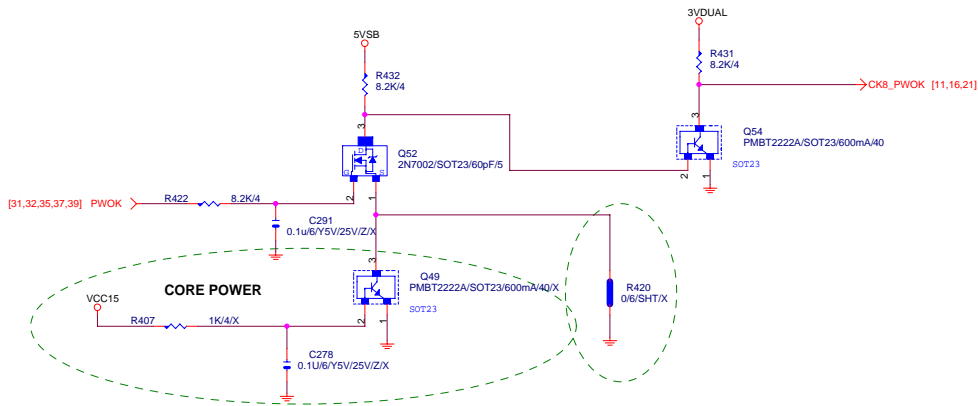
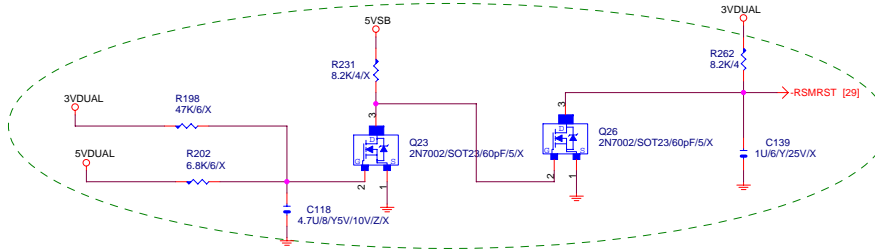
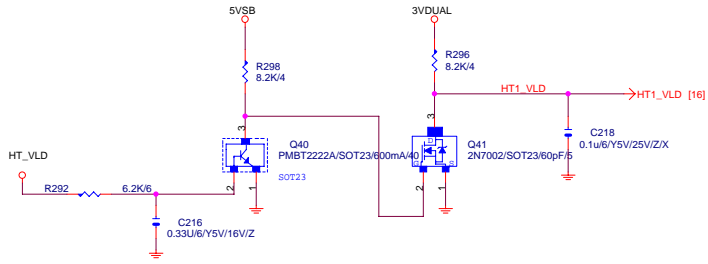


1.4V@150mA Max

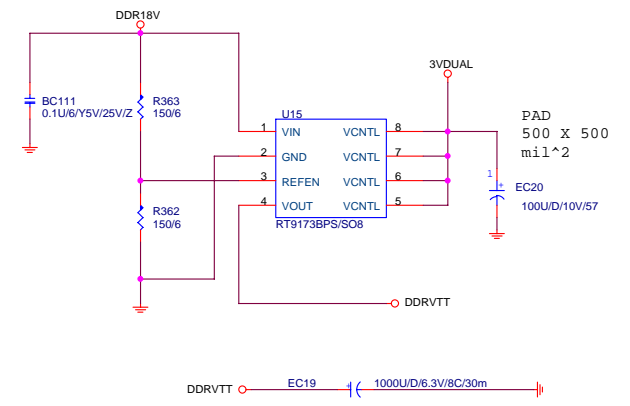
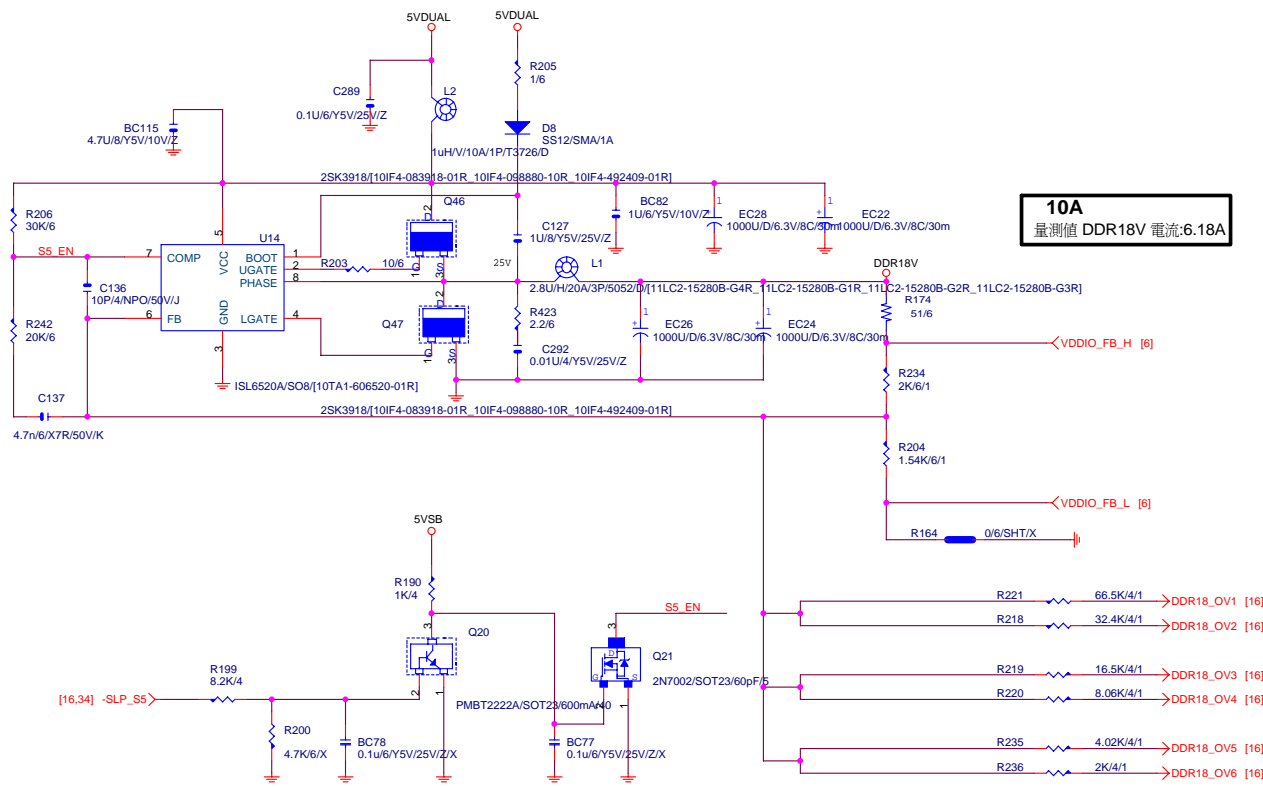
VCC3 10% to Core power 90% < 30ms else , PCIE_RST add T4ACT08



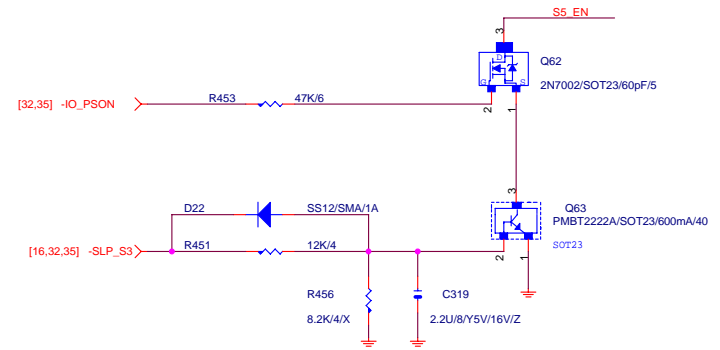
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Title VCC12 HT,VCCA25,PLL POWER		
Size	Document Number GA-M55S-S3	Rev 1.0
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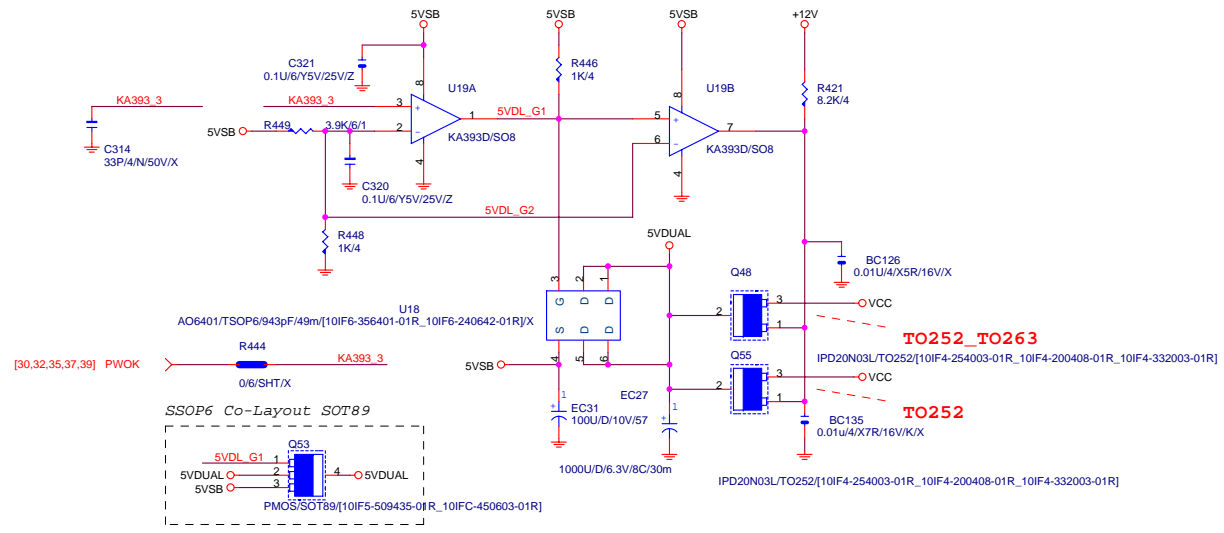
GIGABYTE CORP.		
Title		
POWER SEQUENCE POWER		
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for G3 to G2 status



	G2	S5/S4	S3	S1/S0
-SLP_S5	H	L	H	H
-IO_PSON	H	H	H	L
-SLP_S3	H	L	L	H
DDR18V				

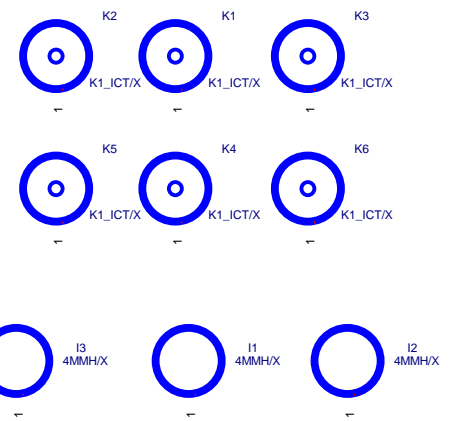
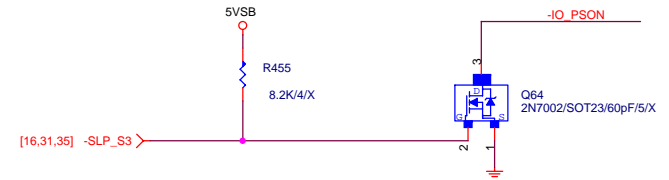
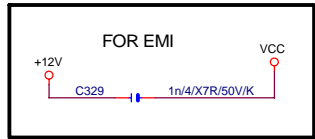
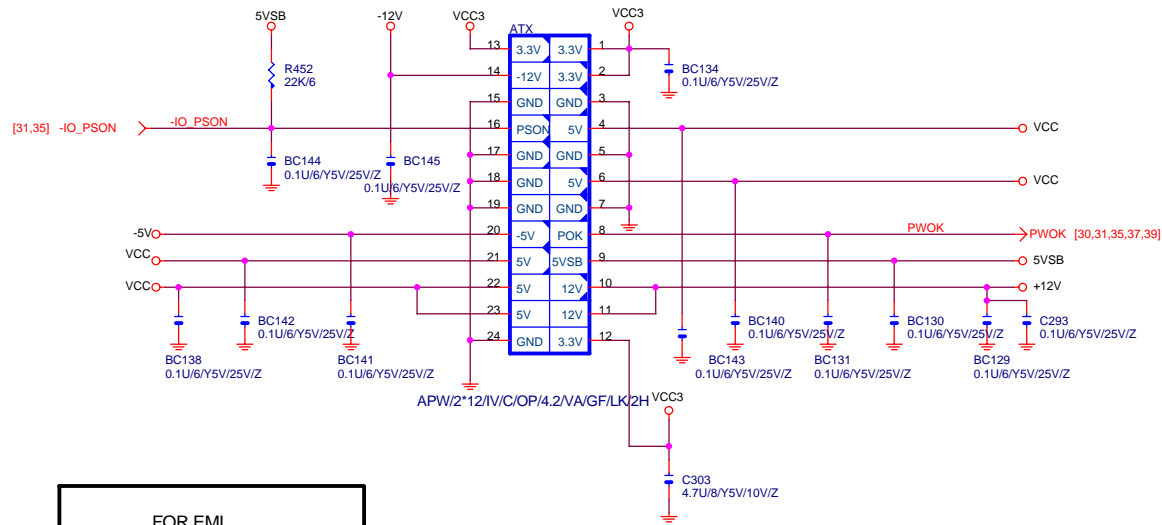


GIGABYTE CORP.

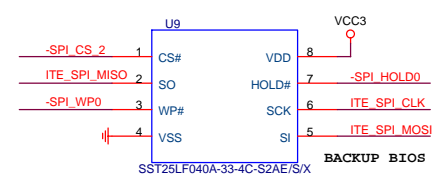
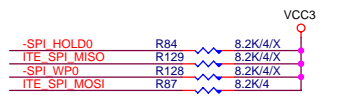
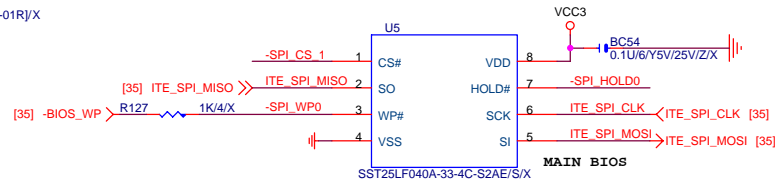
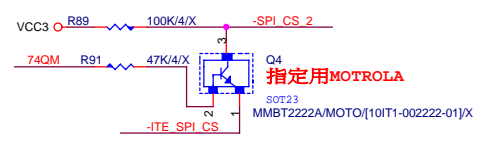
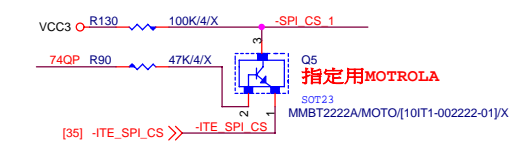
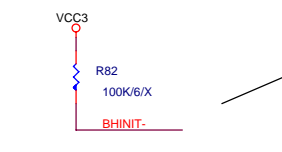
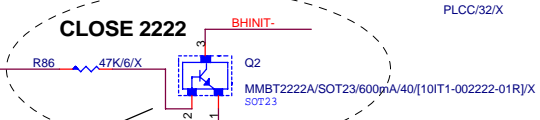
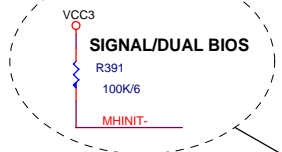
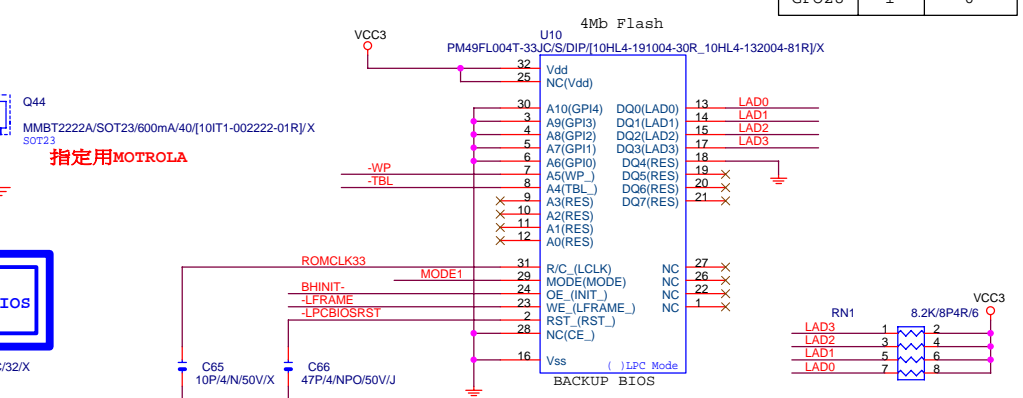
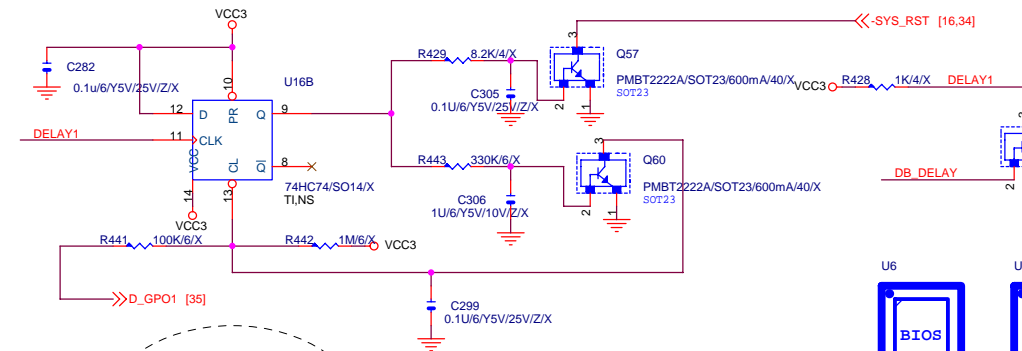
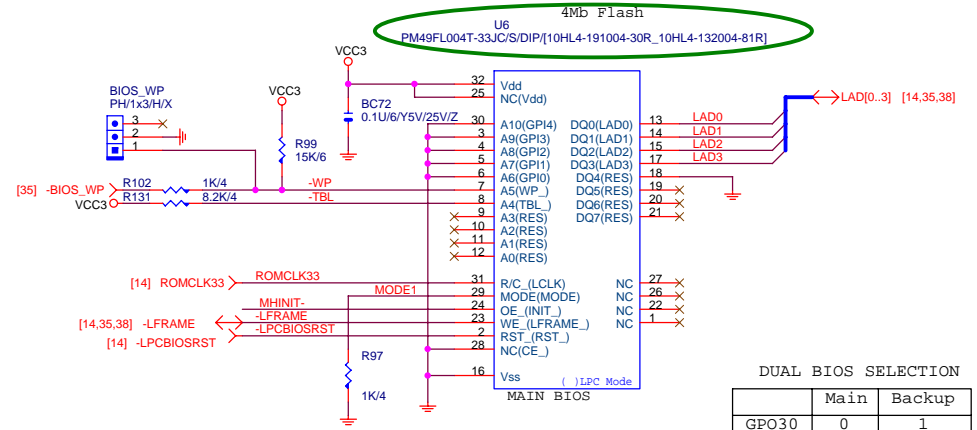
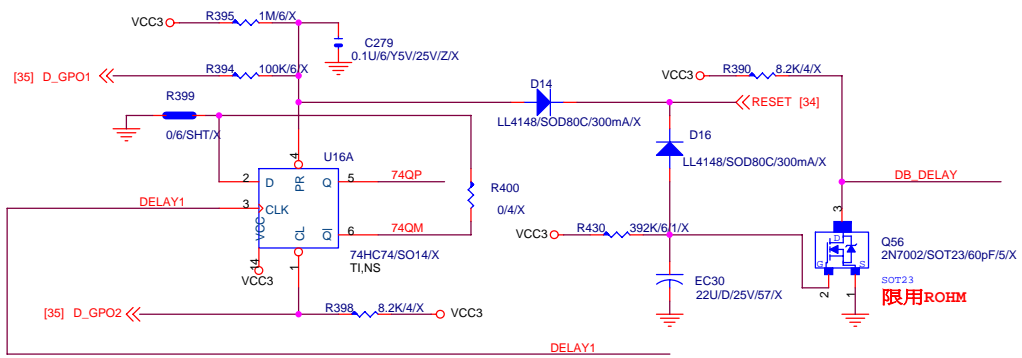
DDR18 , DDRVTT , 5VDUAL

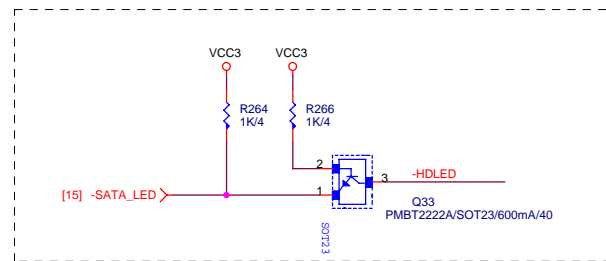
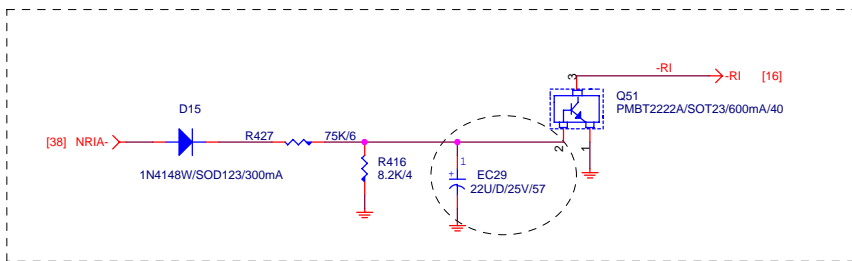
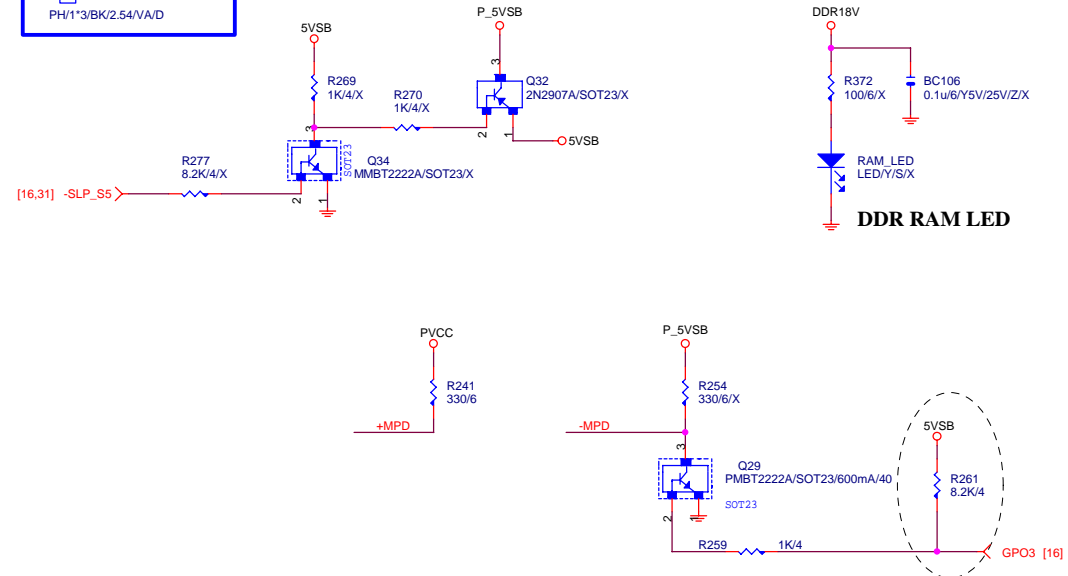
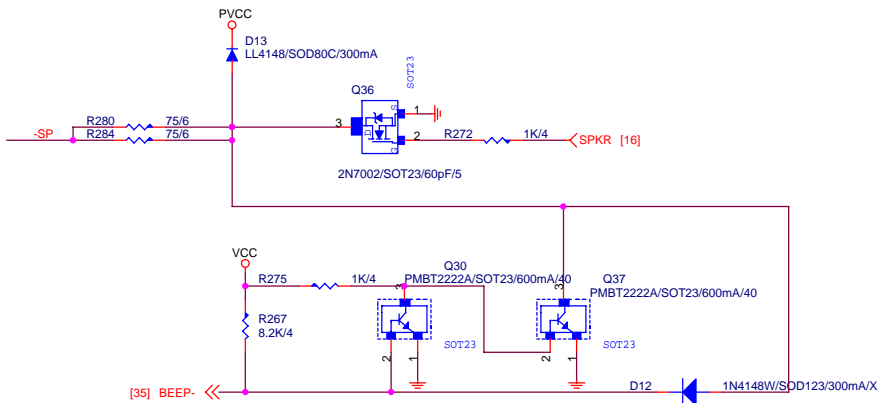
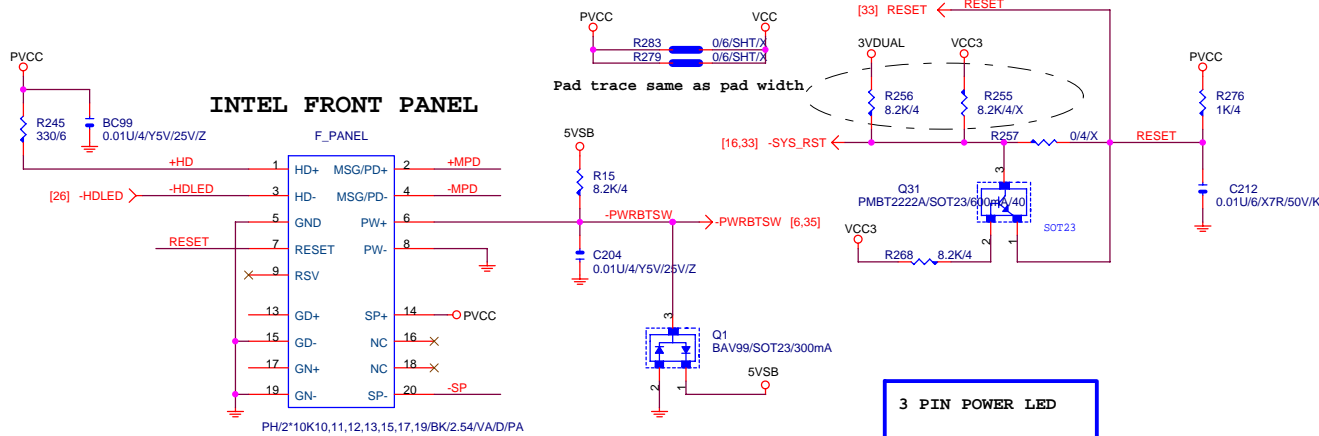
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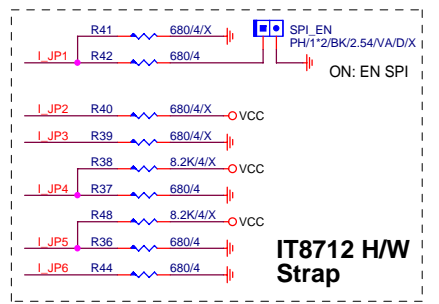
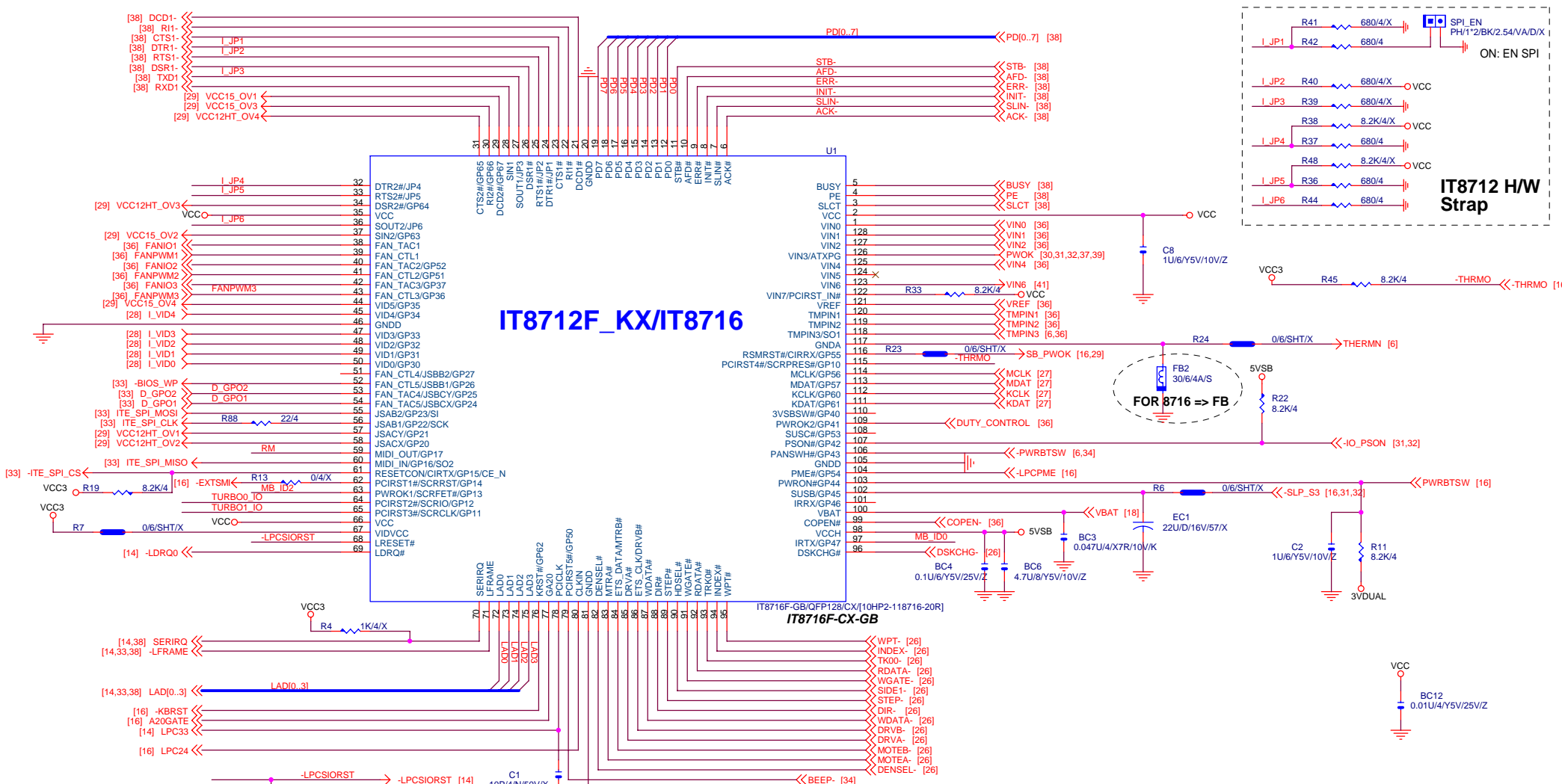
ATX POWER CONNECTOR



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Title		
Misc. PWR & ATX CONN.		
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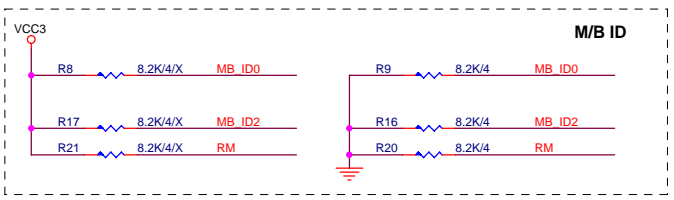
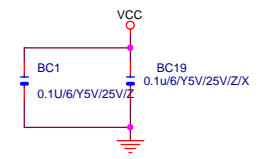


IT8712F_KX/IT8716

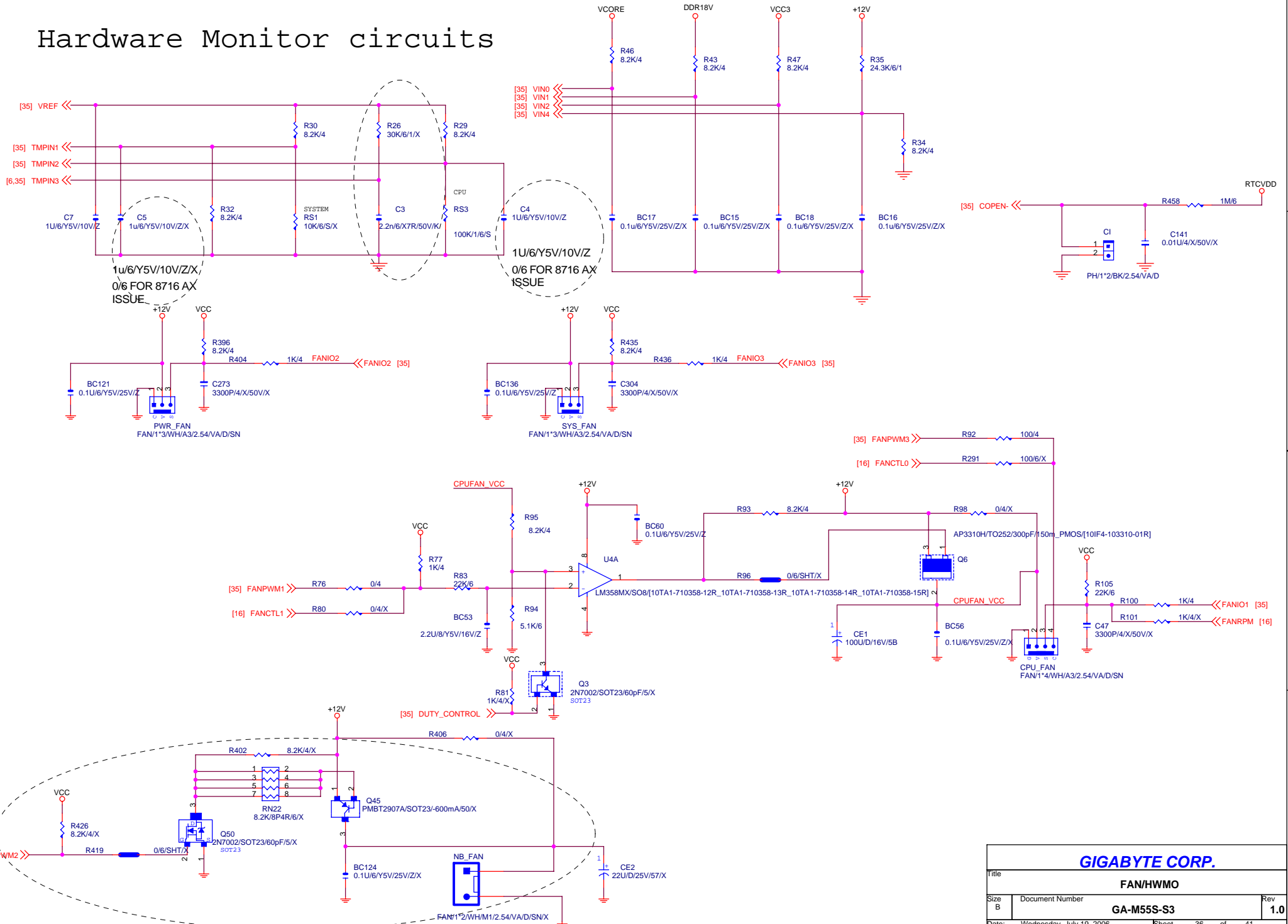
IT8716F-CX-GB

Power On Strapping Options

Symbol	value	Description
JP1	Flashseg1_EN	1 Disabled. 0 Flash I/F Address Segment 1 (FFF8_0000h-FFFF_FFFFh, 000E_0000h-000F_FFFFh) is enabled En SPI Flash
JP2	SerFlh_SO_SEL	1 FLH_SO2 is selected as the Serial Flash I/F SO pin. 0 FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	-- Chip selection in configuration.
JP4	BUF_SEL	1 The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10-20 ns when the signal transits from low to high, and then Hi-Z. 0 The output buffers are push-pull.
JP5	FAN_CTL_SEL	1 The default value of EC Index 15h / 16h / 17h is 00h (Duty=100%) 0 The default value of EC Index 15h / 16h / 17h is 40h (Duty=50%)
JP6	VID_ISEL	1 The threshold voltage of VID is 2.0 / 0.8V 0 The threshold voltage of VID is 0.8 / 0.4V

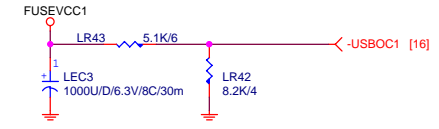
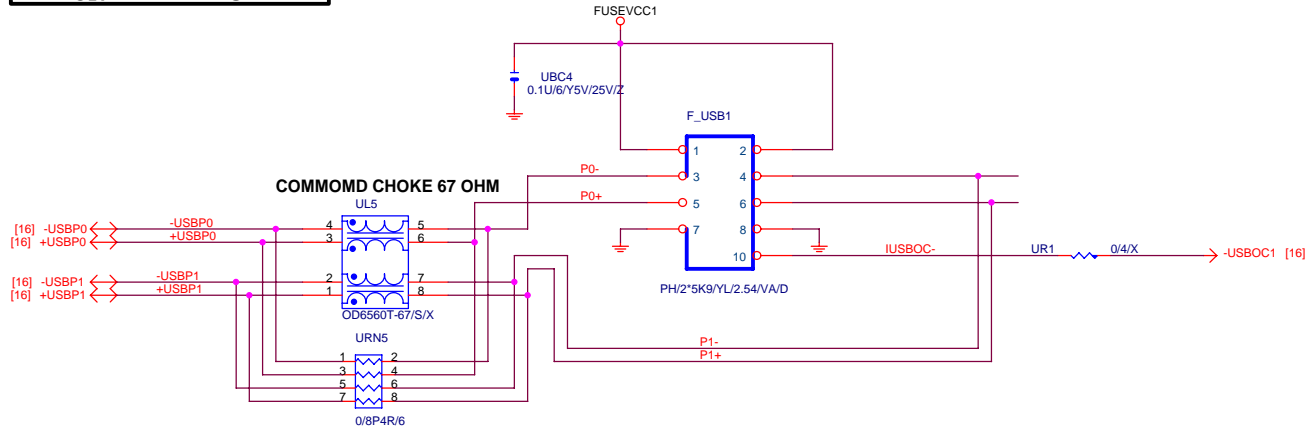


Hardware Monitor circuits

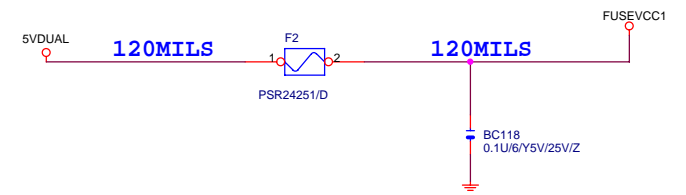
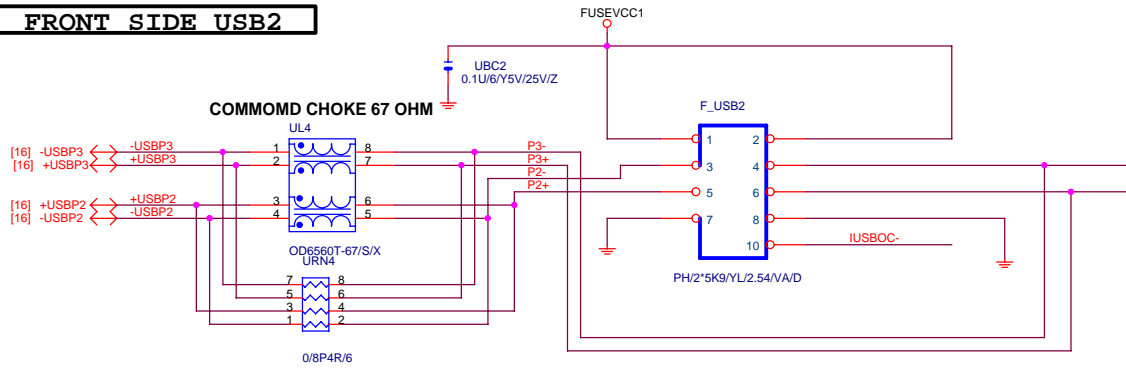


GIGABYTE CORP.		
FAN/HWMO		
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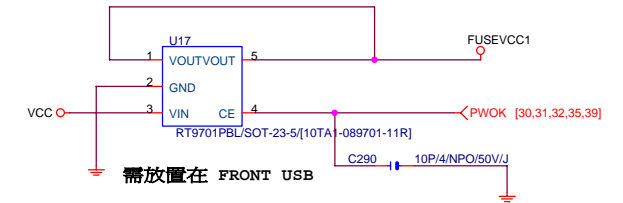
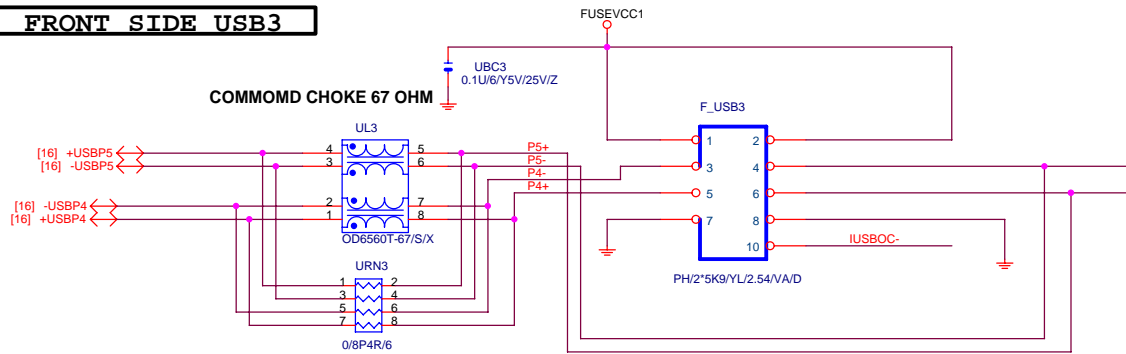
FRONT SIDE USB1



FRONT SIDE USB2



FRONT SIDE USB3



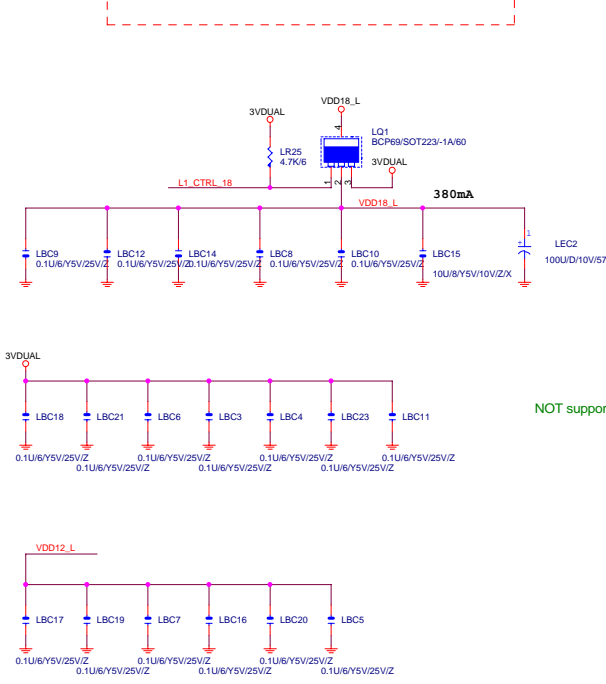
GIGABYTE CORP.

Title		
USB PORT		
Size B	Document Number	Rev
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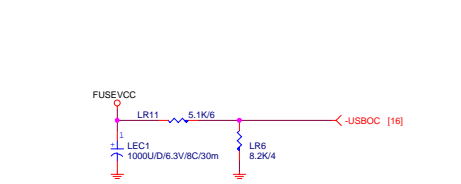
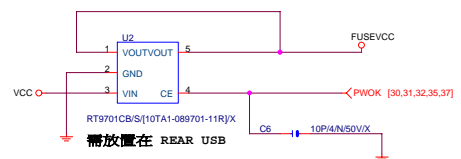
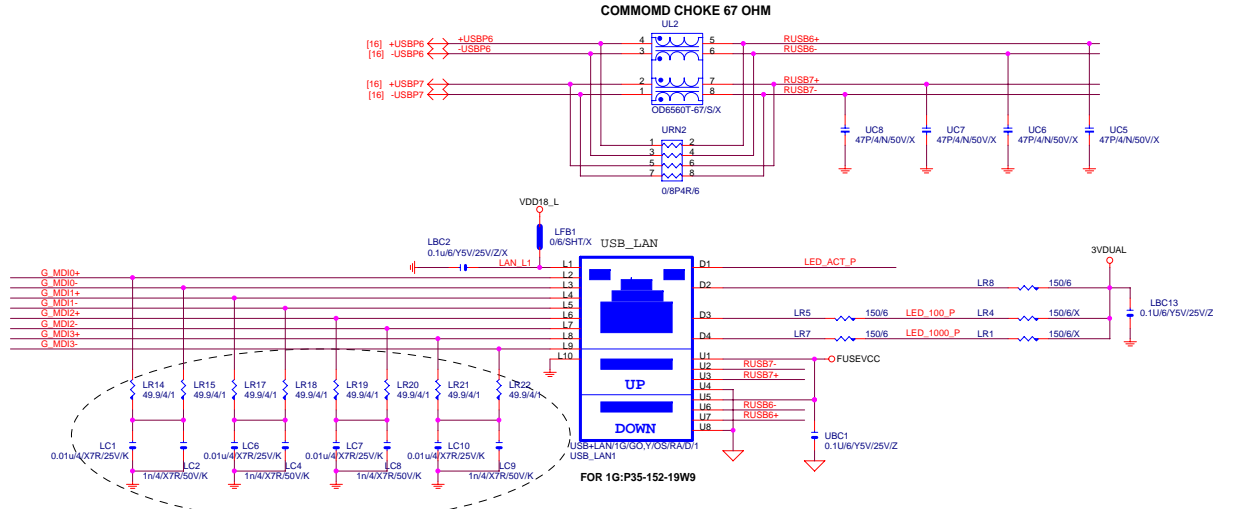
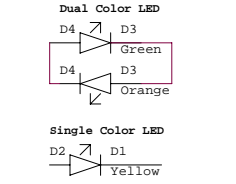
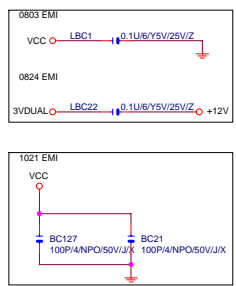
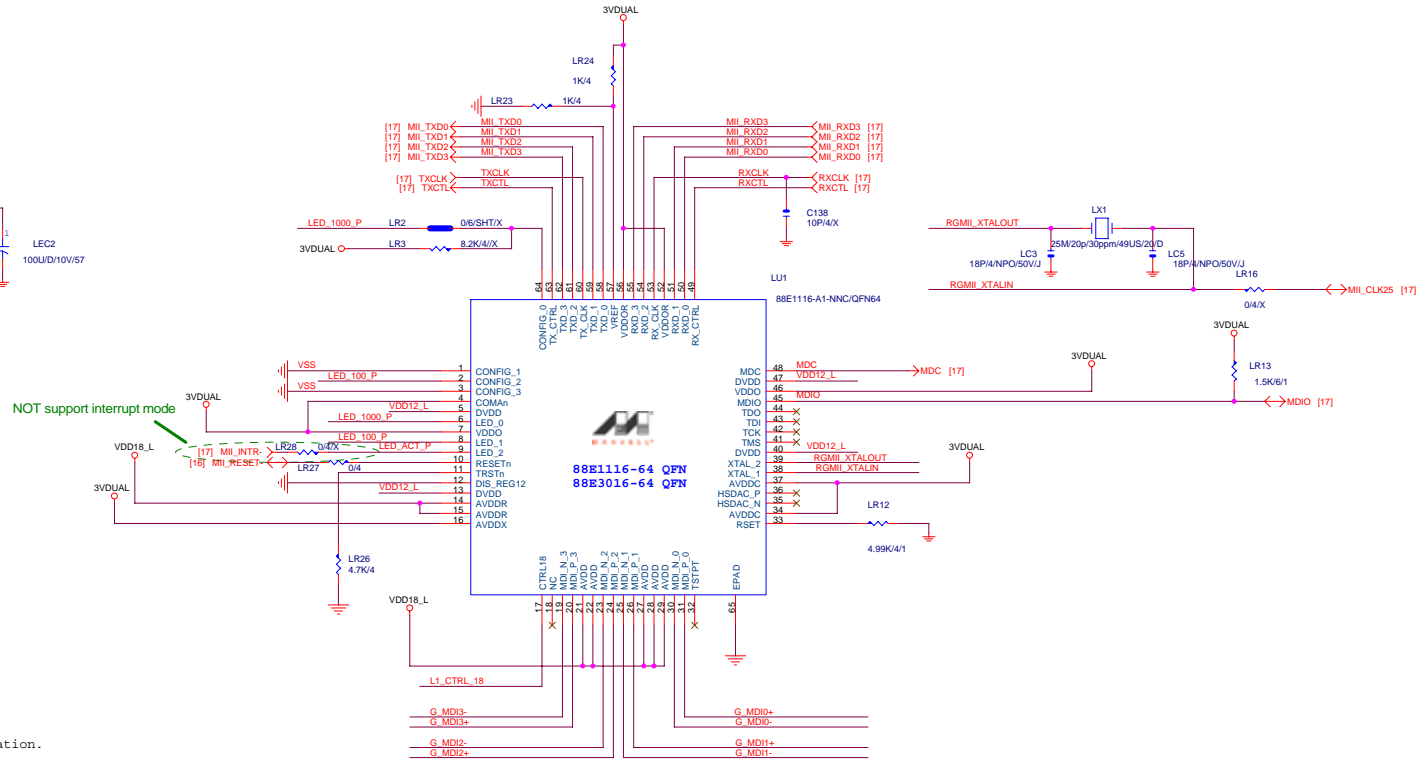
Hardware Configuration: See config_0:4

1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities

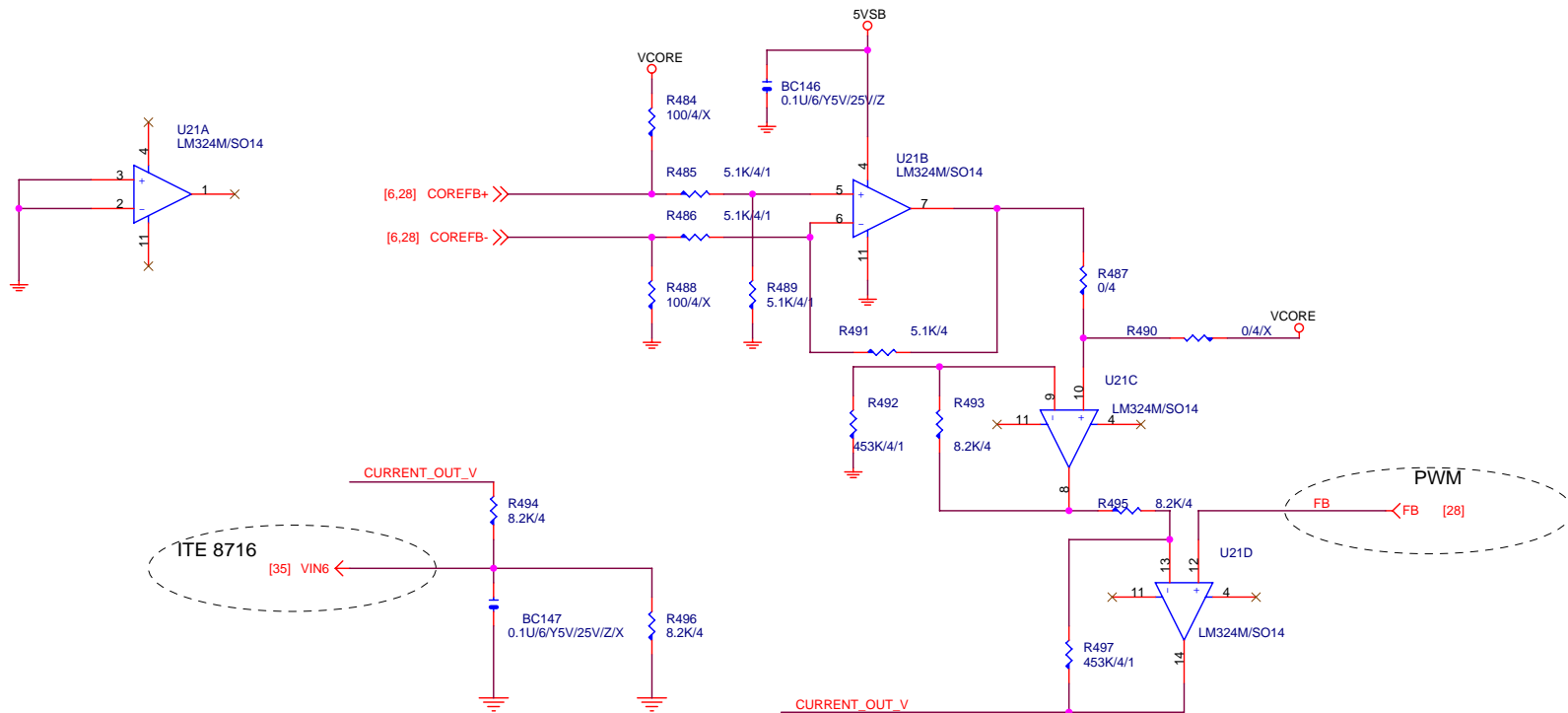
E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.



Bypass cap can share. User check it by layout consideration.



File		
Marvell_88E1116_88E1116_88E3016		
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GIGABYTE CORP.		
Title CURRENT_OUT		
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