

GA-M55plus-S3G

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	PROCESSOR HT INTERFACE
05	PROCESSOR DDR2 INTERFACE
06	PROCESSOR DDR2 INTERFACE
07	PROCESSOR CONTROL & DEBUG
08	DIMM 1,2
09	DIMM 3,4
10	DIMM TERMINATION
11	C51 CPU
12	C51 HT
13	C51 PCI-EXPRESS
14	C51 RGB
15	C51 PWR/GND
16	MCP51 HT BUS
17	MCP51 PCI BUS/CLOCK/RESET
18	MCP51 SATA/IDE
19	MCP51 AZILIA/USB
20	MCP51 RGMII
21	MCP51 PWR/GND
22	PCI EXPRESS X16 SLOT
23	F_USB1/F_USB2 CONN /PCI_E x1 SLOT
24	PCI 1,2,3 SLOT
25	PCI 4 SLOT

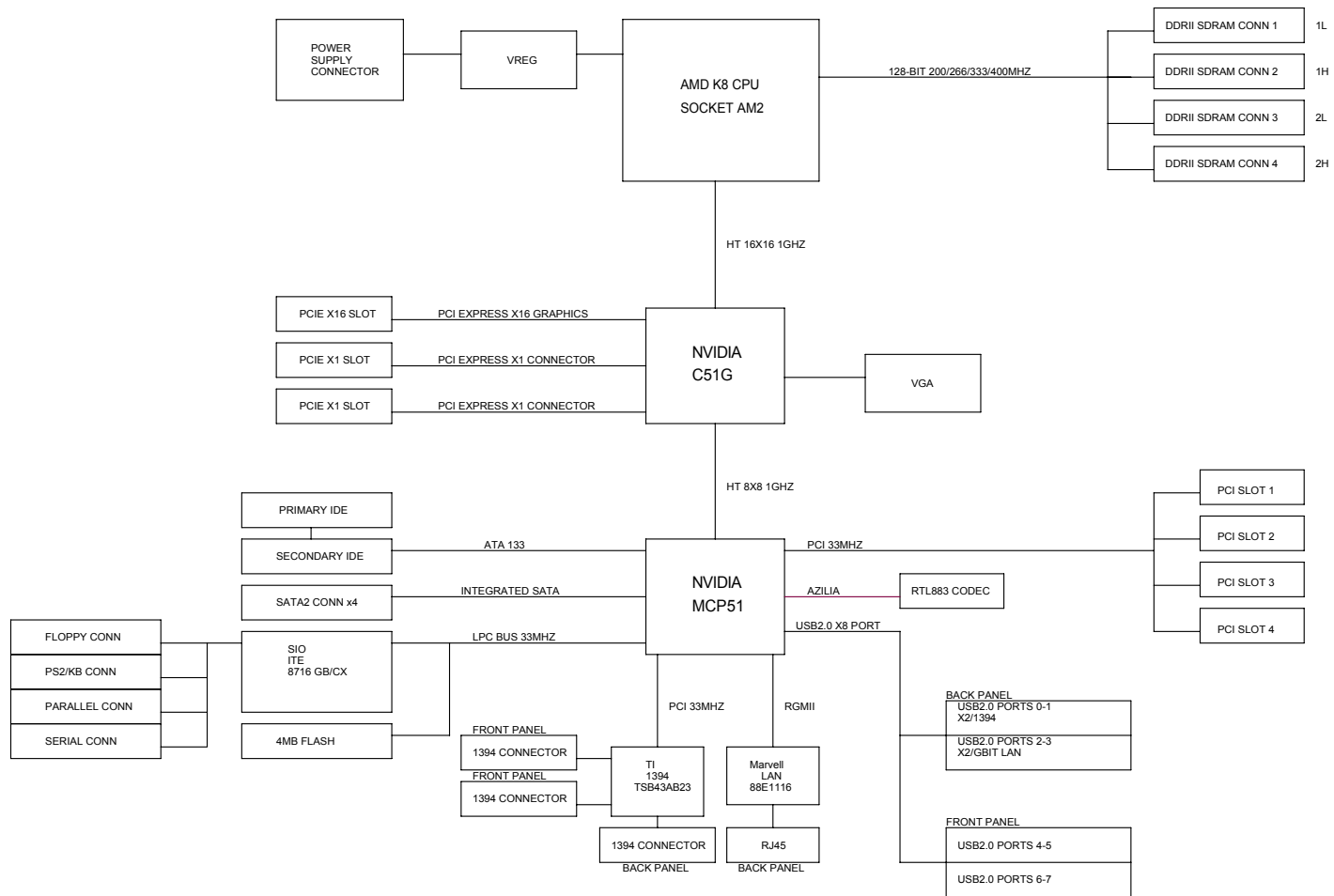
SHEET TITLE

26	CODEC ALC883
27	AUDIO JACK, L_OUT, F_AUDIO
28	H/W MONITOR & FAN CONTROL
29	IDE1/IDE2/FDD
30	PWM ISL6566
31	COMA, LPT PORT
32	DDR18V,DDRVT,5VDAUL,VCC12, POWER
33	POWER SEQUENCE
34	BIOS ATX POWER CONNCTOR
35	FRONT PANEL
36	ITE 8716GB/CX
37	Marvell 88E1116
38	TI TSB43AB23 1394

Revision:1.0

GIGABYTE			
Title COVER SHEET			
Size Custom	Document Number GA-M55plus-S3G	Rev 1.0	
Date: Friday, May 05, 2006	Sheet 1	of 38	

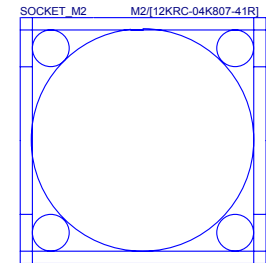
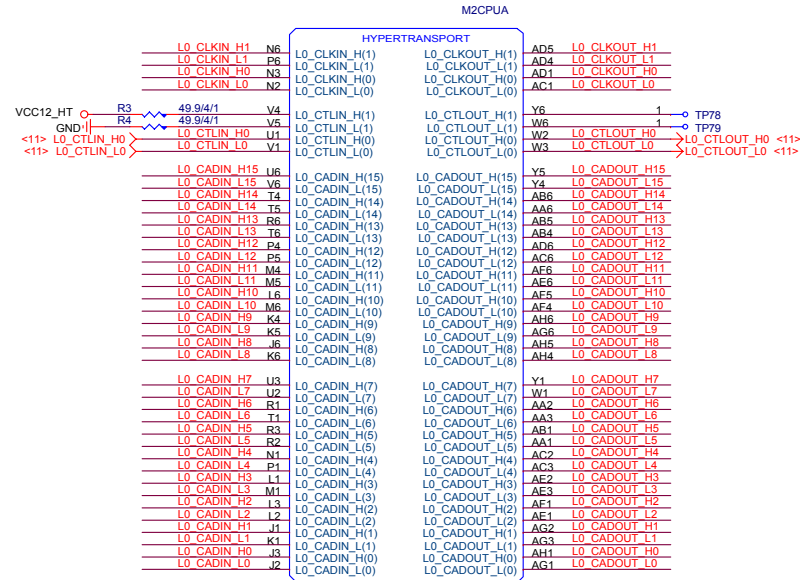
BLOCK DIAGRAM



L0_CADIN_L[0..15] <L0_CADIN_L[0..15] <11>
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] <11>
L0_CLKIN_L[0..1] <L0_CLKIN_L[0..1] <11>
L0_CLKIN_H[0..1] <L0_CLKIN_H[0..1] <11>
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] <11>
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] <11>
L0_CLKOUT_L[0..1] <L0_CLKOUT_L[0..1] <11>
L0_CLKOUT_H[0..1] <L0_CLKOUT_H[0..1] <11>

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B



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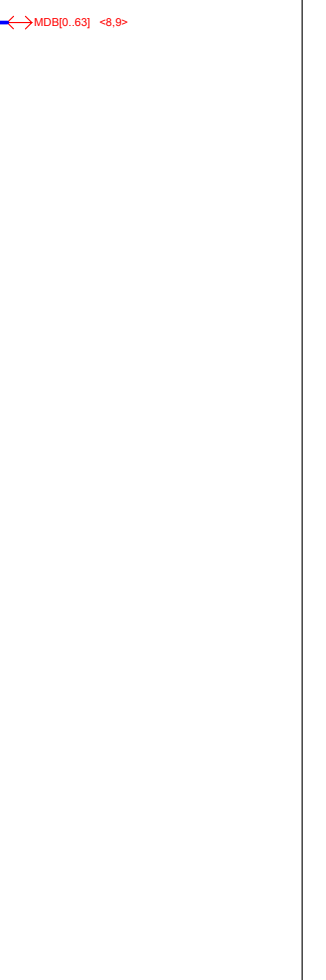
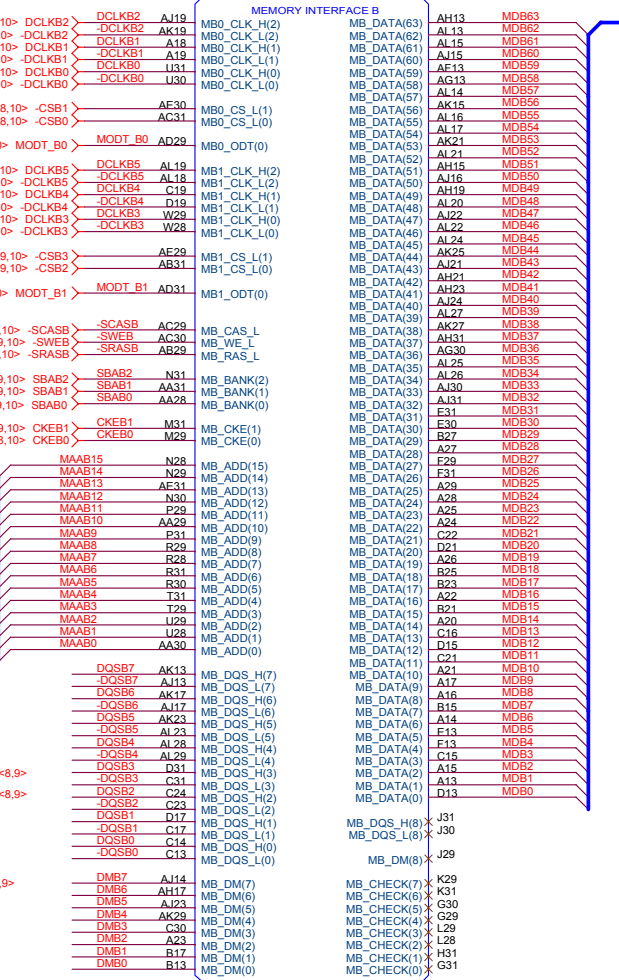
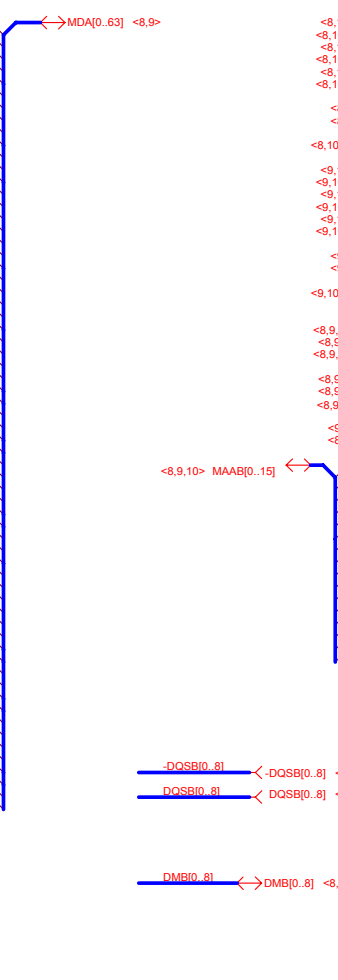
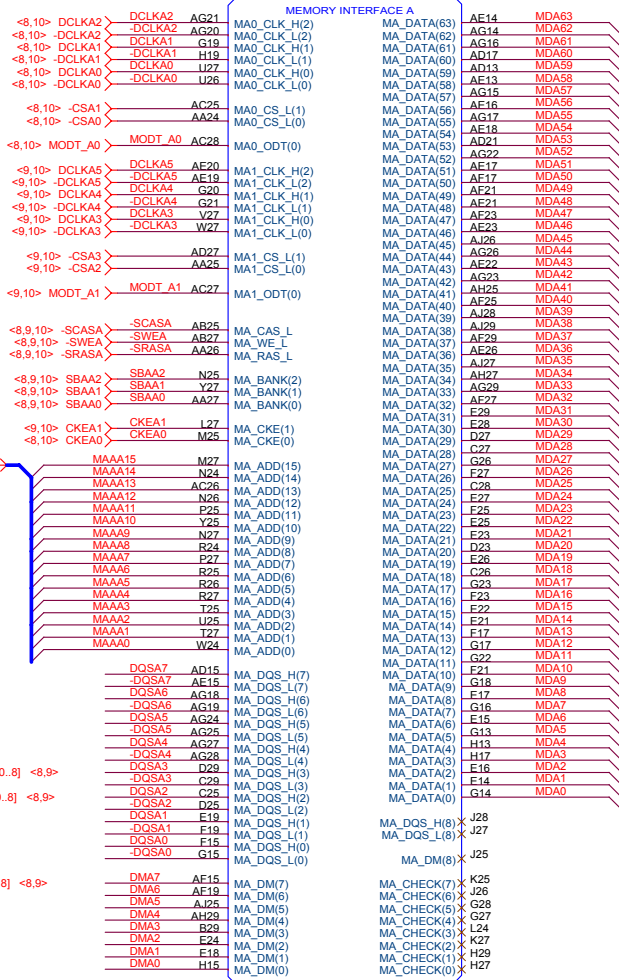
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CPU HYPER TRANSPORT			
Size	Document Number	Rev	
Custom	GA-M55plus-S3G	1.0	
Date:	Friday, May 05, 2006	Sheet	4 of 38

M2CPUB

M2CPUC

MEMORY INTERFACE A

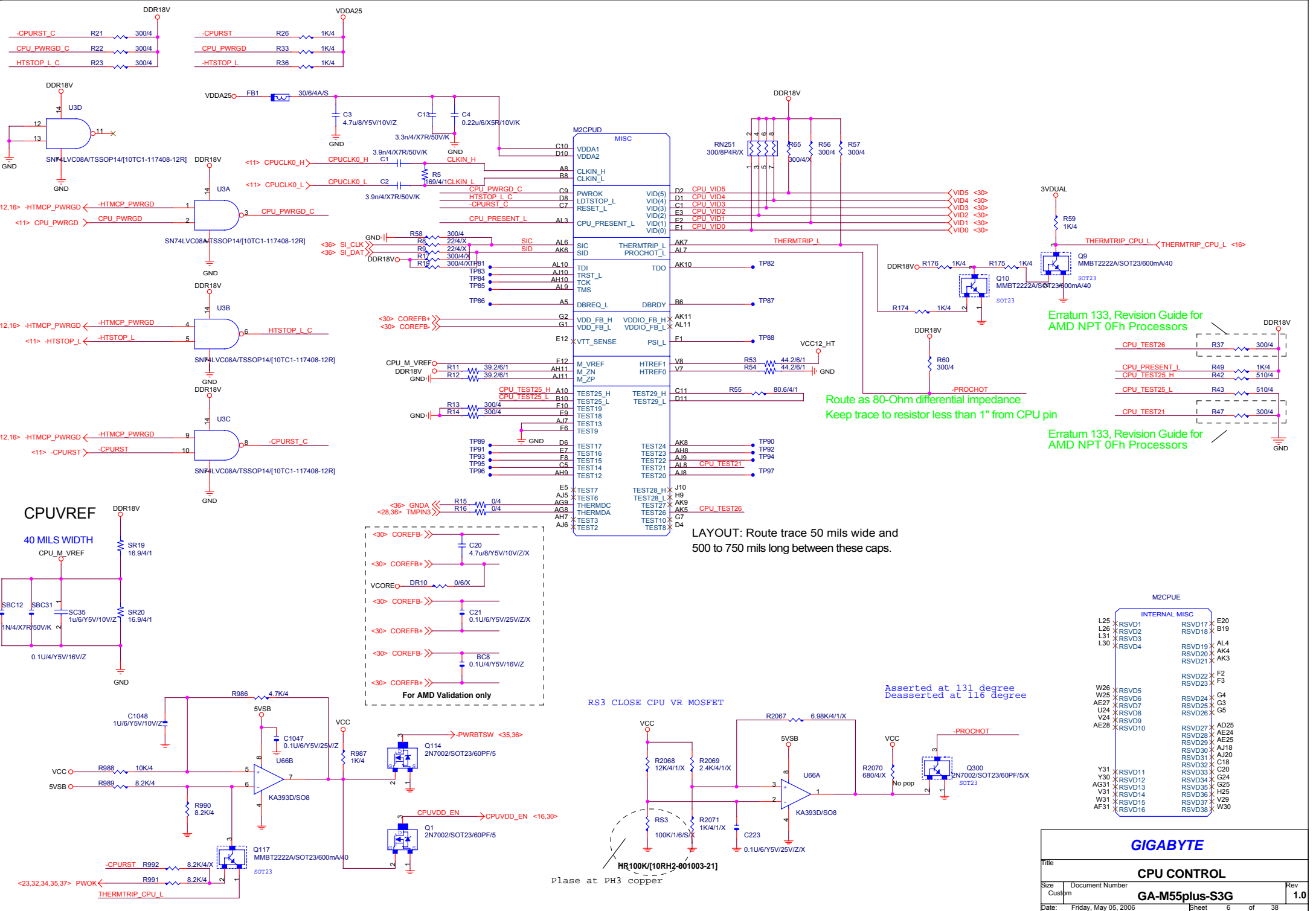
MEMORY INTERFACE B



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CPU DDRII MEMORY

Title		
CPU DDRII MEMORY		
Size	Document Number	Rev
Custom	GA-M55plus-S3G	1.0
Date:	Friday, May 05, 2006	Sheet 5 of 38



Erratum 133, Revision Guide for AMD NPT 0Fh Processors

Erratum 133, Revision Guide for AMD NPT 0Fh Processors

Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin

LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.

Asserted at 131 degree
Deasserted at 116 degree

HR100K(10RH2-001003-21)
Please at PH3 copper

M2CPUE

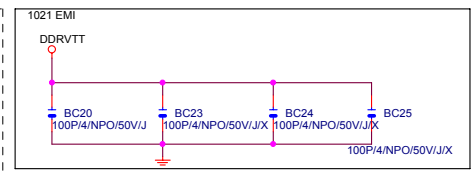
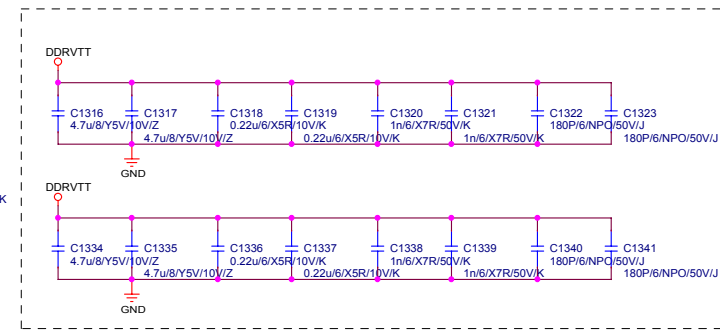
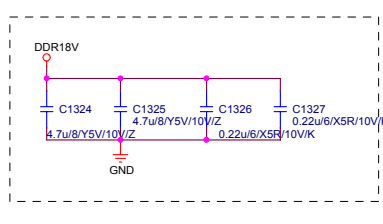
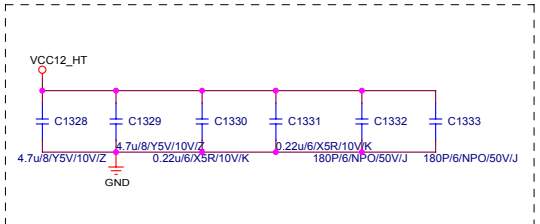
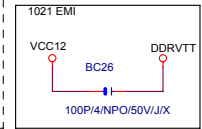
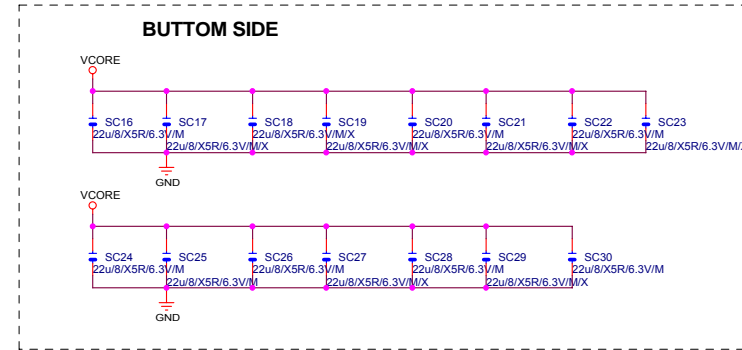
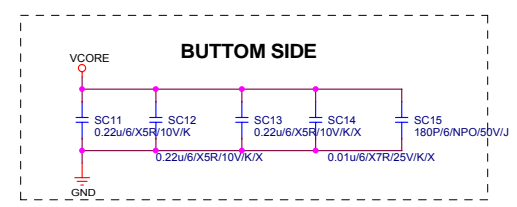
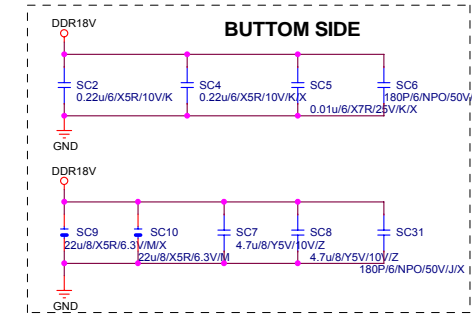
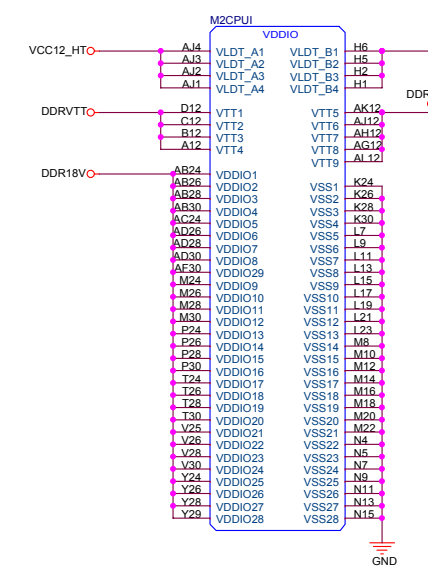
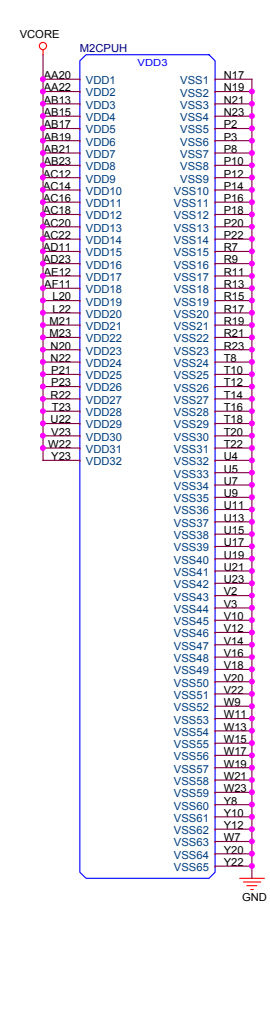
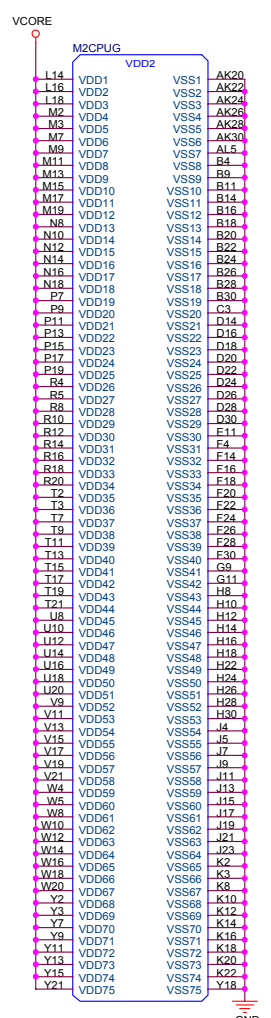
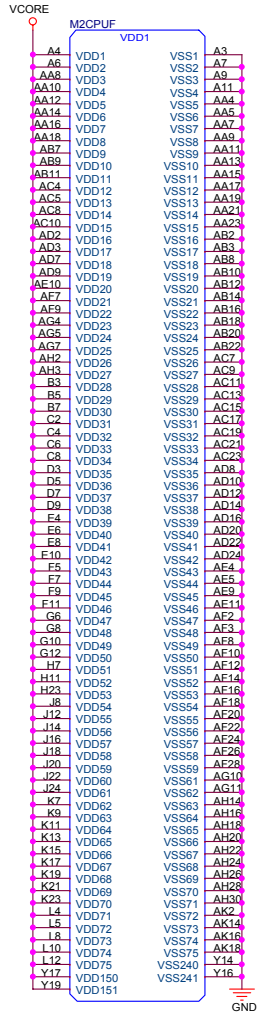
INTERNAL MISC		
L25	RSVD1	RSVD17
L26	RSVD2	RSVD18
L31	RSVD3	
L30	RSVD4	
		RSVD19
		RSVD20
		RSVD21
		RSVD22
		RSVD23
		RSVD24
		RSVD25
		RSVD26
		RSVD27
		RSVD28
		RSVD29
		RSVD30
		RSVD31
		RSVD32
		RSVD33
		RSVD34
		RSVD35
		RSVD36
		RSVD37
		RSVD38
Y31	RSVD11	AD25
Y30	RSVD12	AE25
AG31	RSVD13	AJ18
V31	RSVD14	AJ20
W31	RSVD15	C18
AF31	RSVD16	C20
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		H25
		G25
		V29
		W30

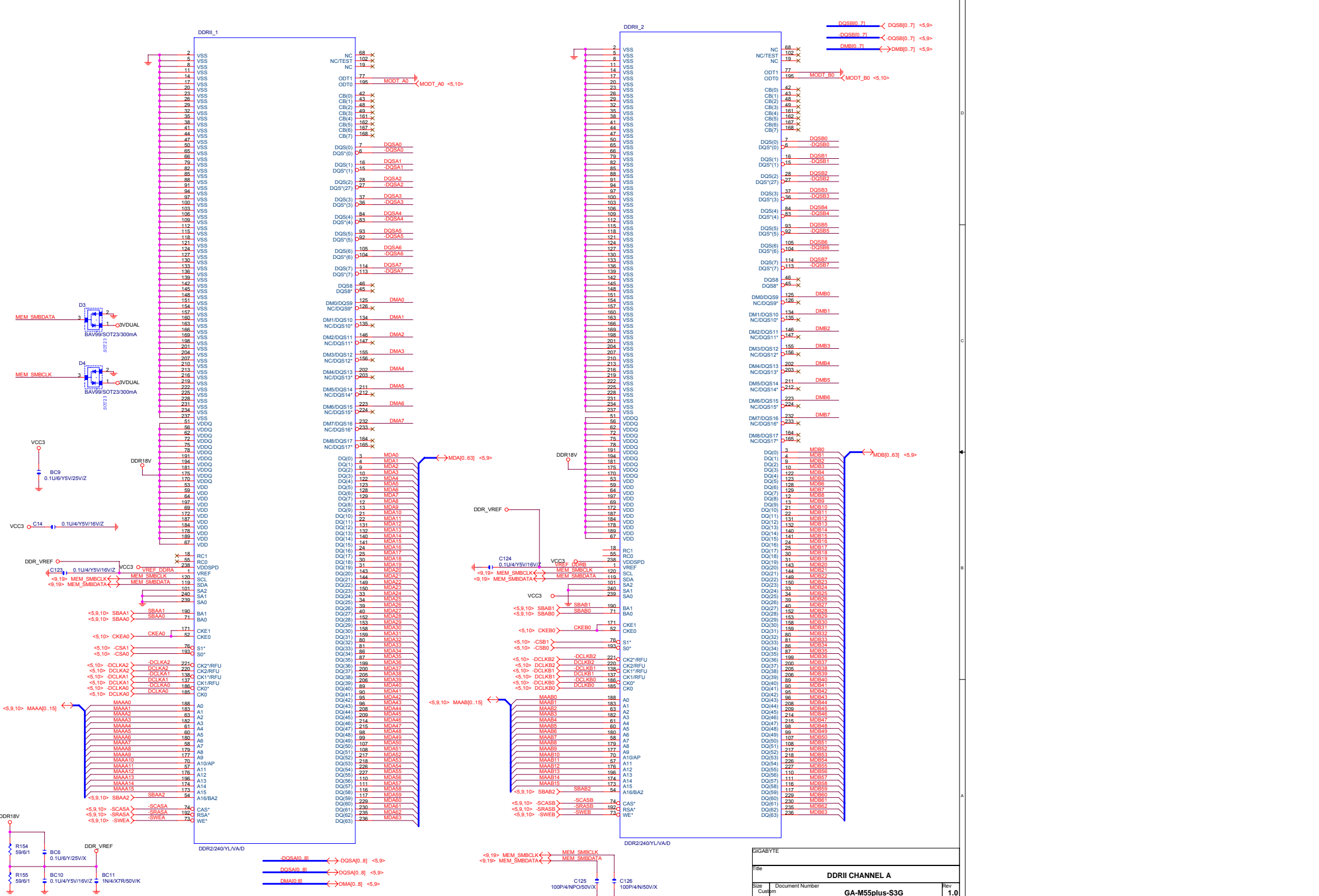
GIGABYTE

CPU CONTROL

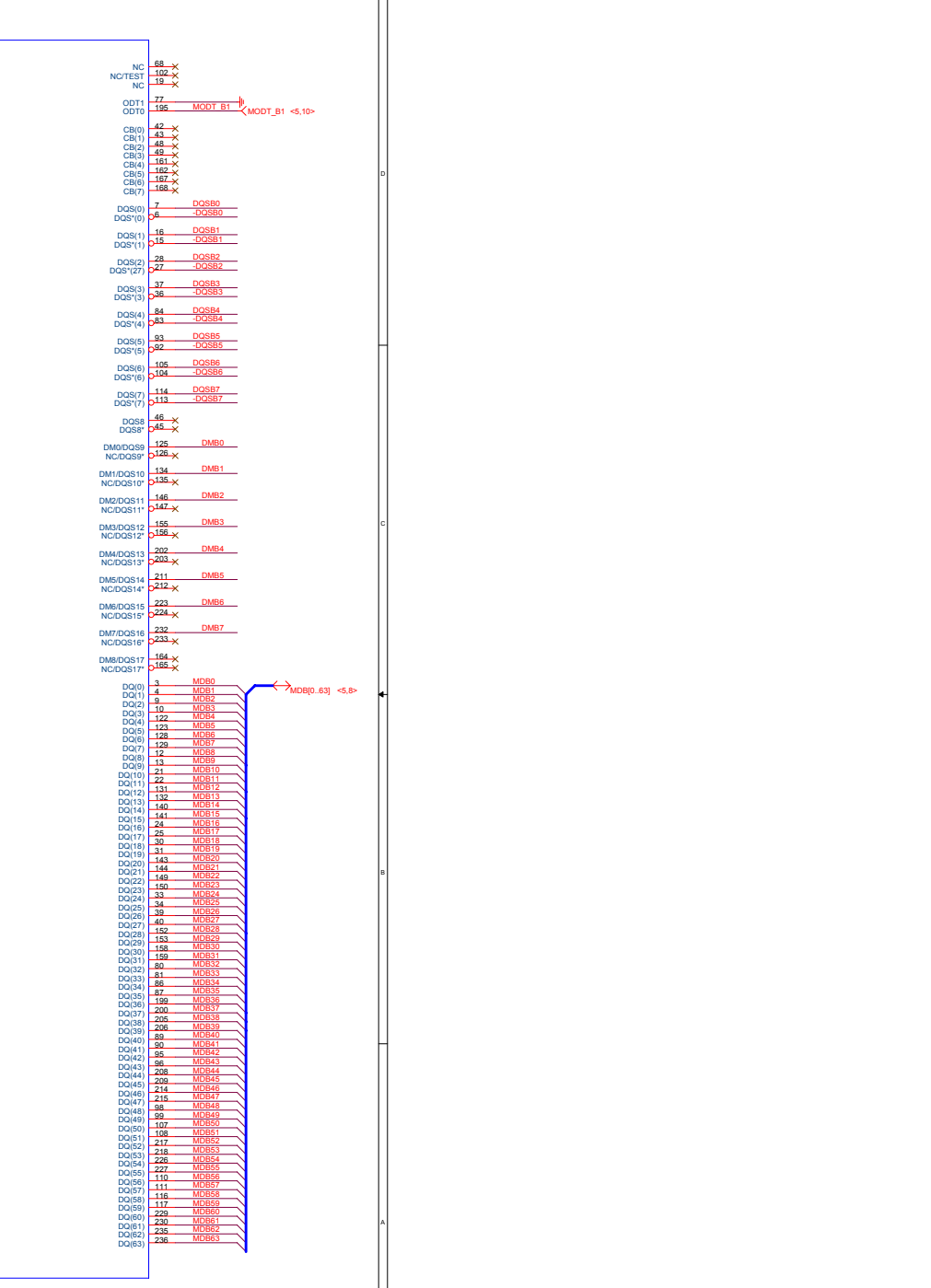
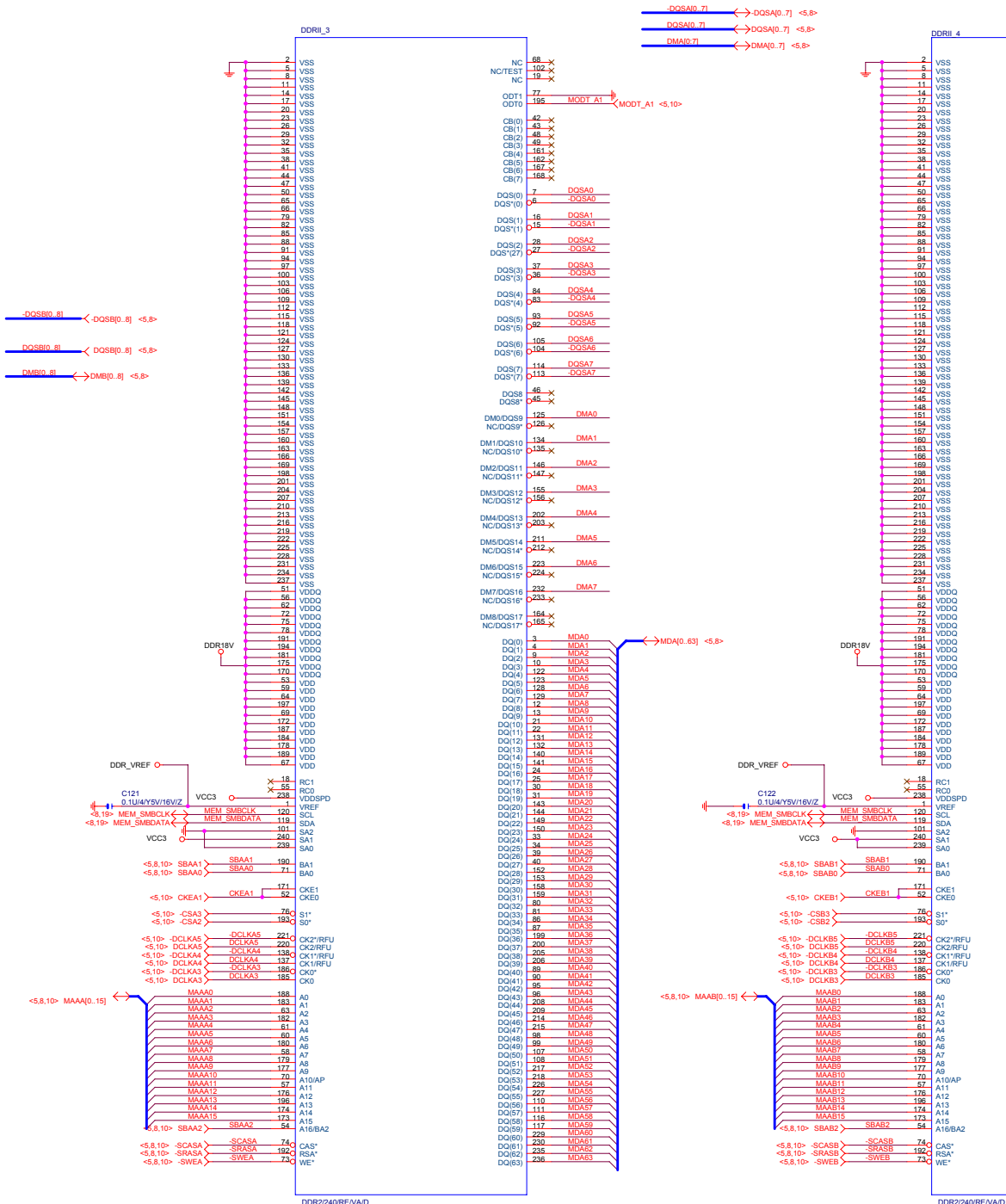
Title	Document Number	Rev
	GA-M55plus-S3G	1.0
Date:	Friday, May 05, 2006	Sheet 6 of 38

VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

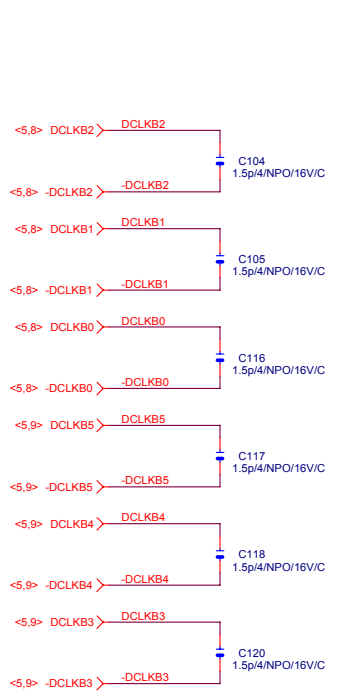
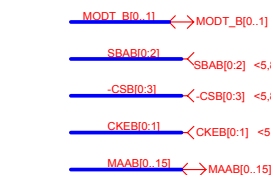
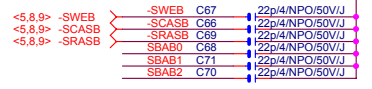
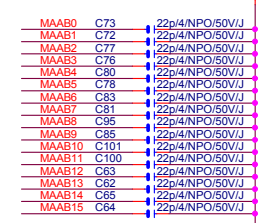
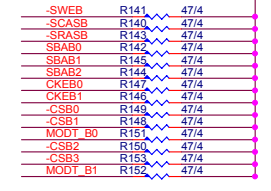
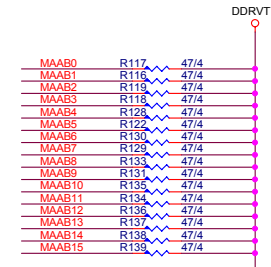
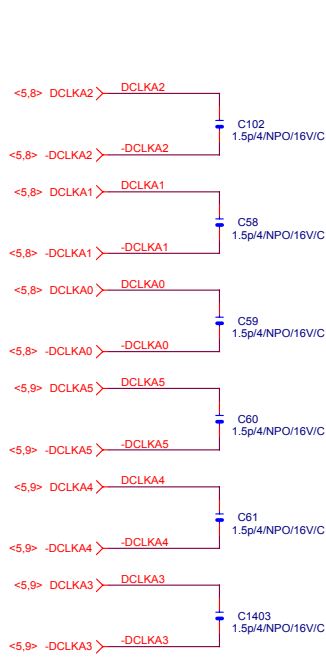
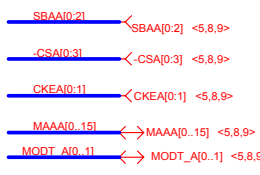
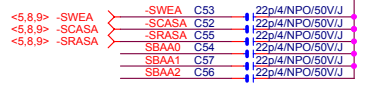
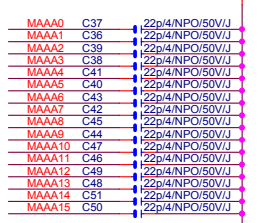
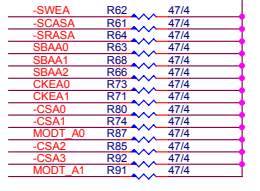
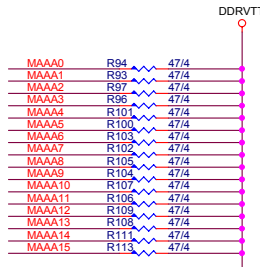
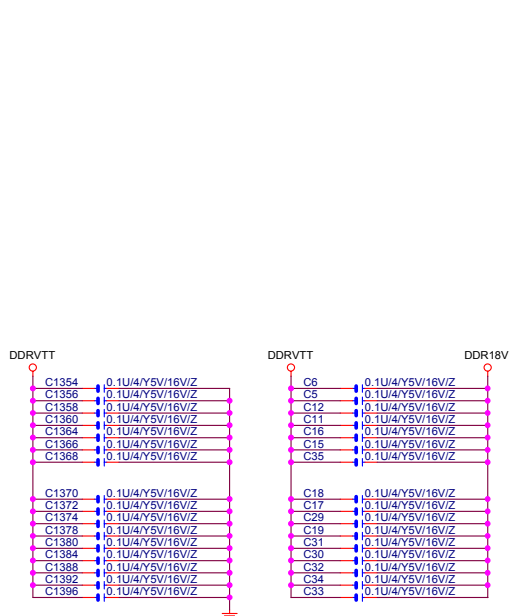




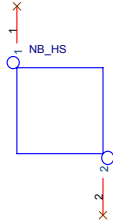
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Title	DDR2 CHANNEL A
Size	Custom
Document Number	GA-M55plus-S3G
Date:	Rev 1.0
Sheet	8 of 38



SIGABYTE	
Title	DDR11 CHANNEL B
Size	Document Number
Custom	GA-M55plus-S3G
Date:	Rev 1.0
	Sheet 9 of 38

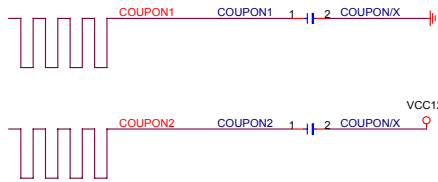
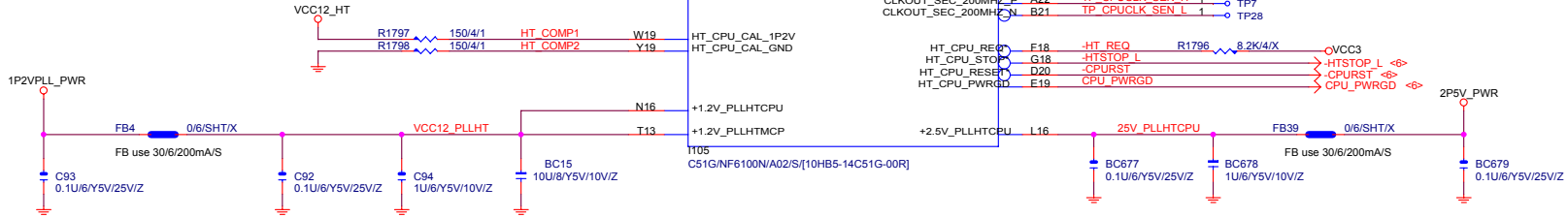


N.B HEATSINK

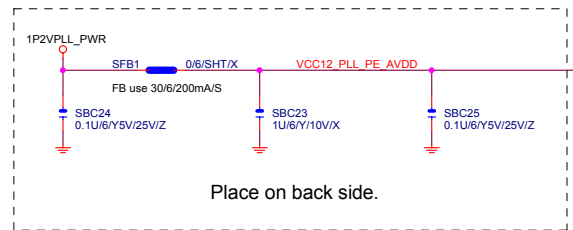
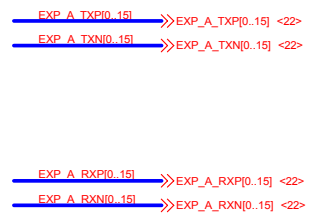
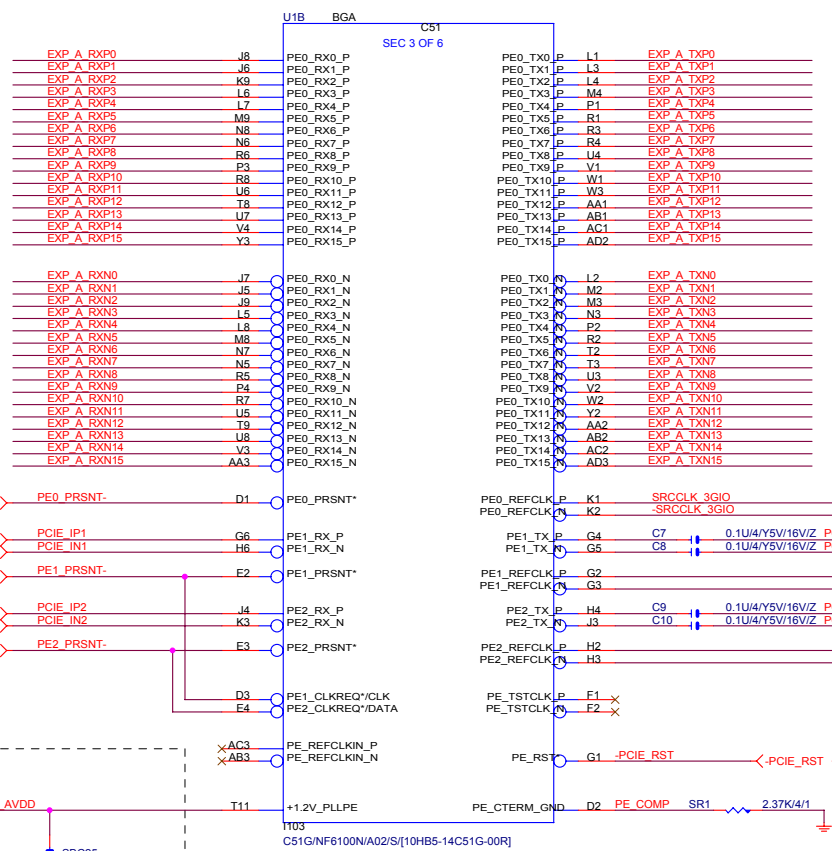


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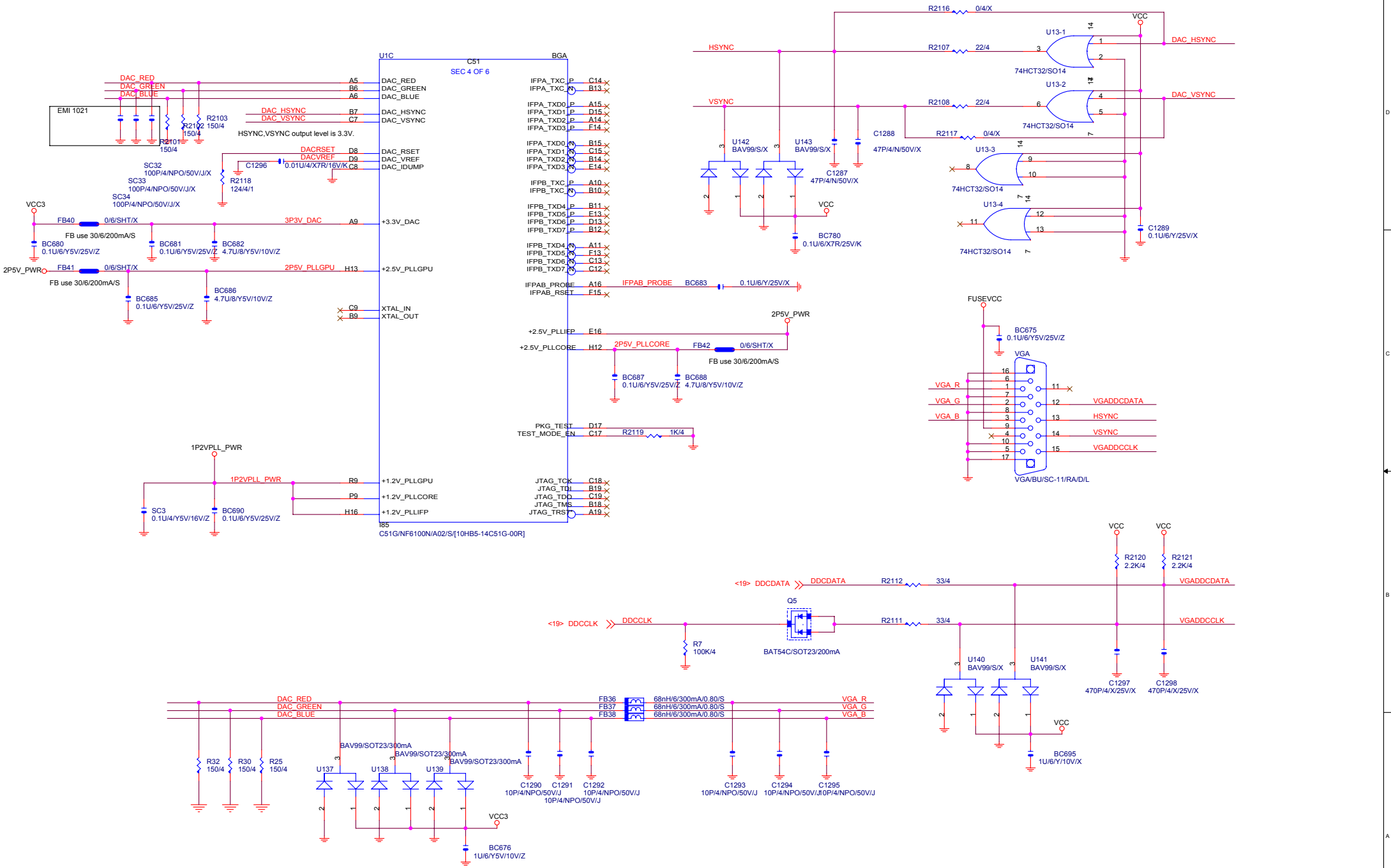


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Size Custom	Document Number GA-M55plus-S3G	Rev 1.0
Date: Friday, May 05, 2006	Sheet 11	of 38

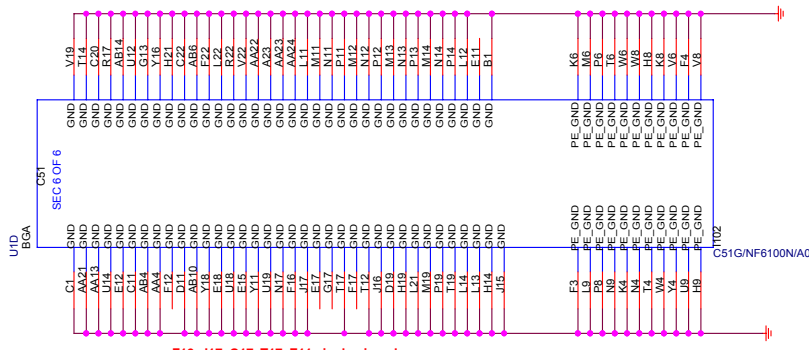
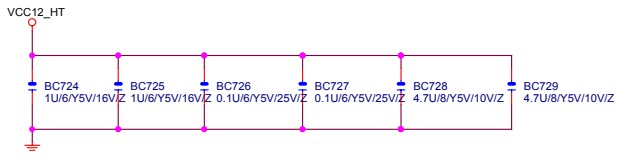
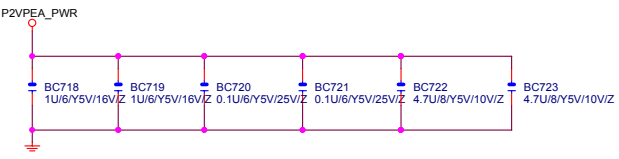
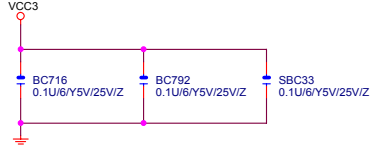
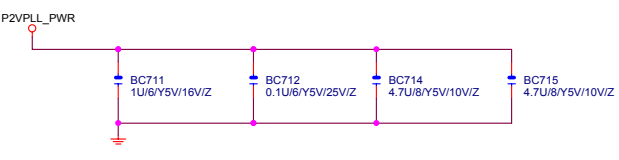
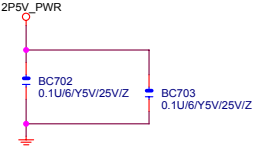
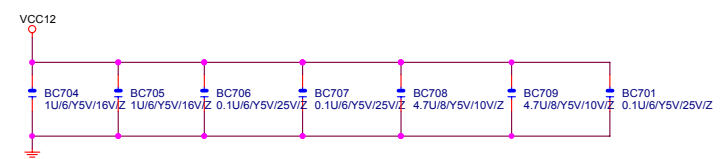
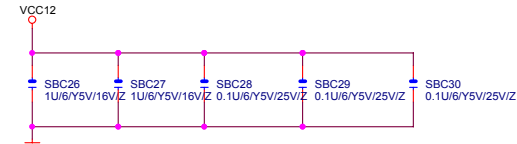
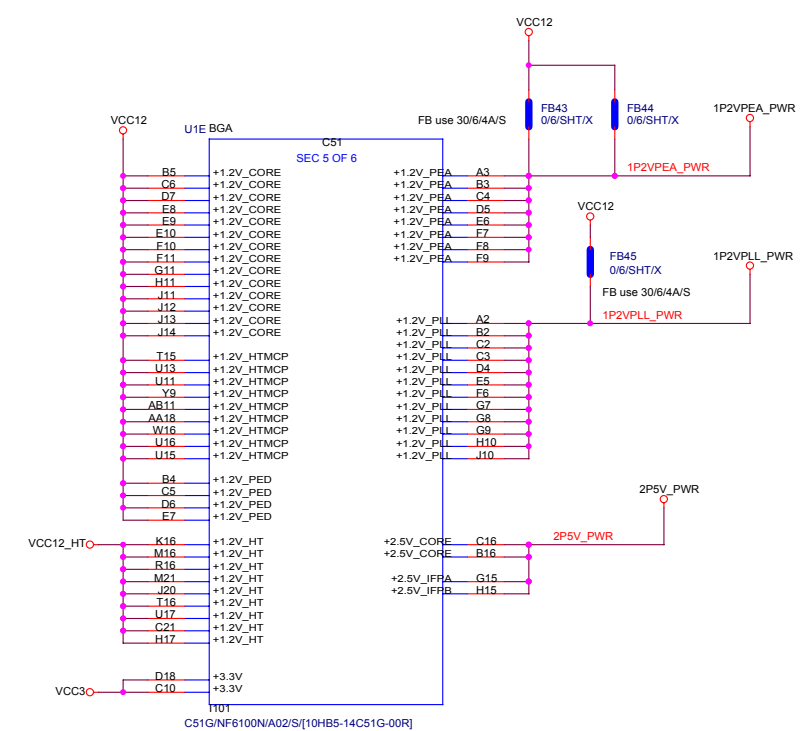


Place on back side.

GIGABYTE		
Title C51-PCI EXPRESS		
Size	Document Number	Rev
Custom	GA-M55plus-S3G	1.0
Date:	Friday, May 05, 2006	Sheet 13 of 38

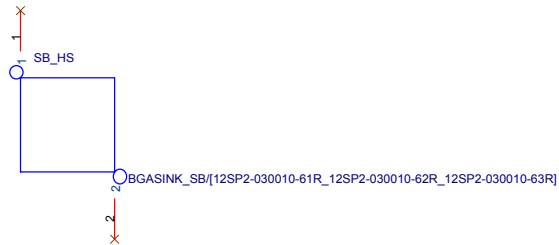


GIGABYTE		
C51-RGB		
Size	Document Number	Rev
Custom	GA-M55plus-S3G	1.0
Date:	Friday, May 05, 2006	Sheet 14 of 38



F12, J17, G17, T17, E11 single pin only.

GIGABYTE			
Title C51-PWR/GND			
Size	Document Number	Rev	
Custom	GA-M55plus-S3G	1.0	
Date:	Thursday, April 20, 2006	Sheet	15 of 38

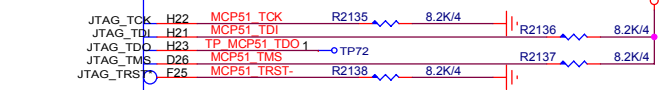
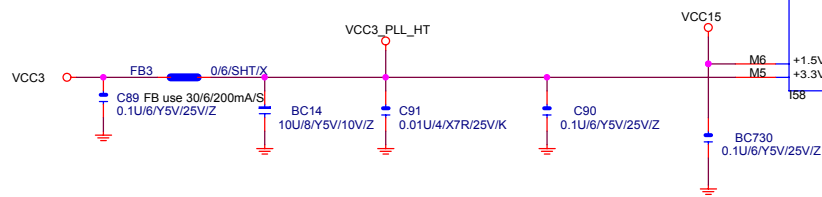
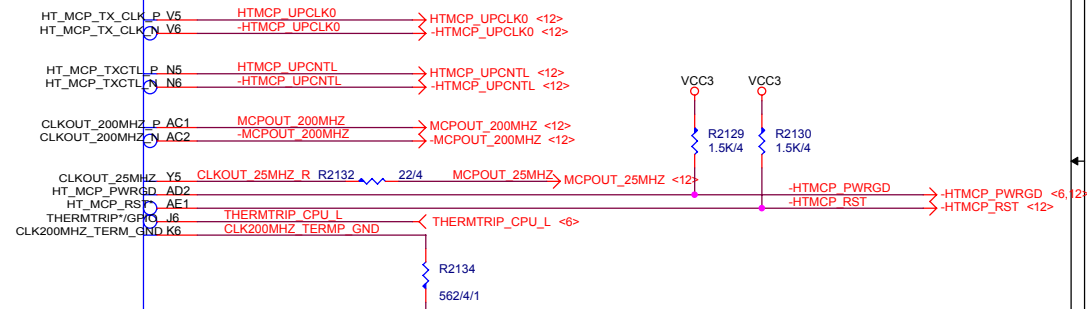
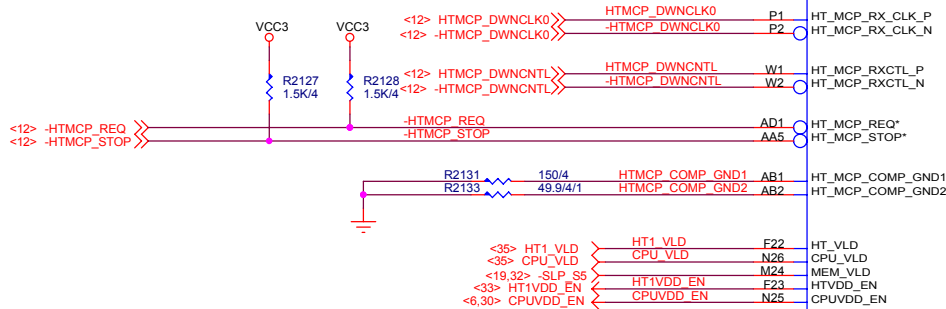
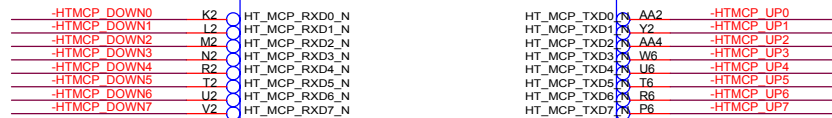
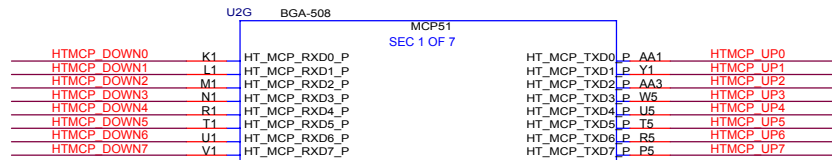


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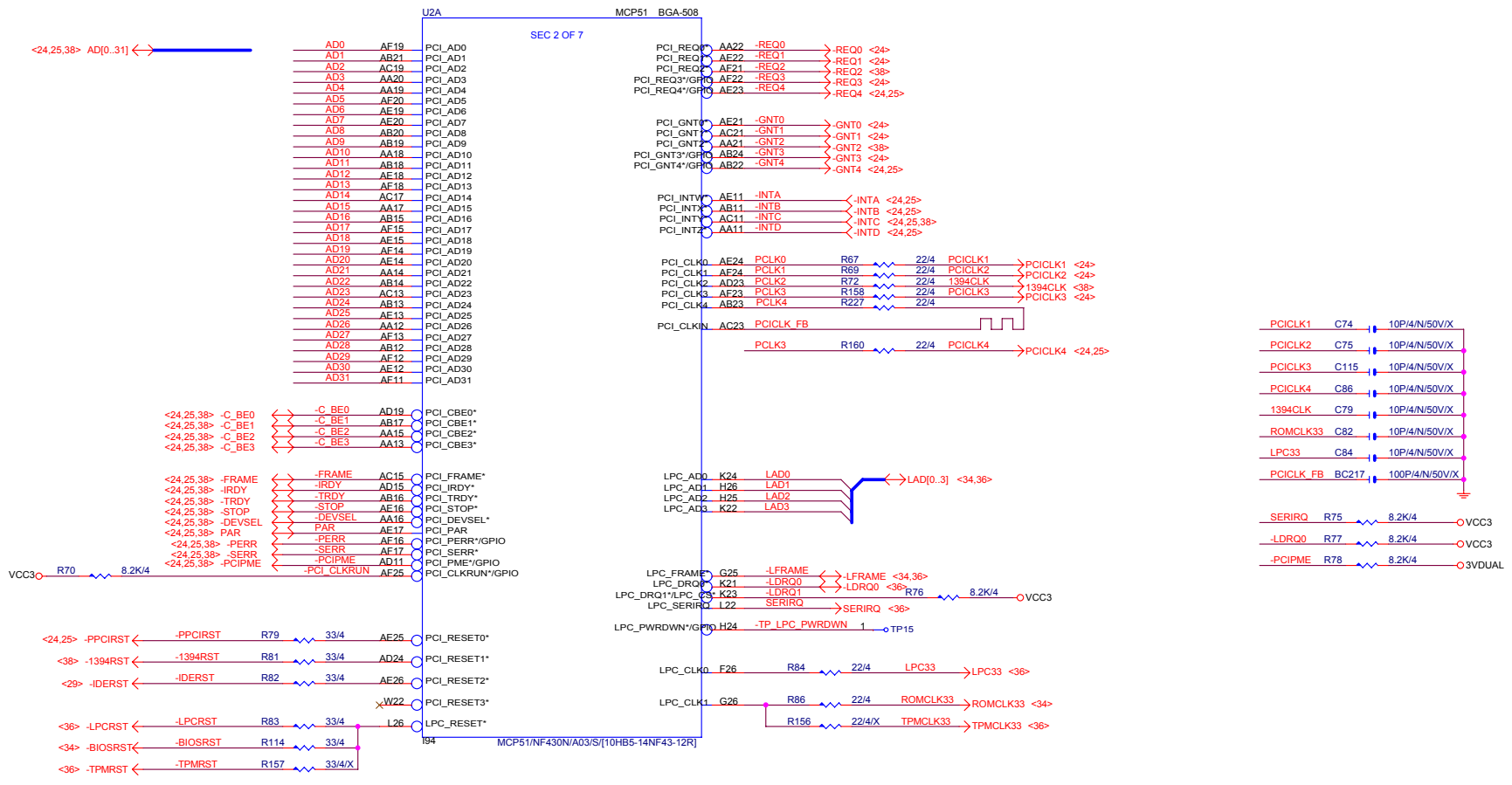
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HTMCP_UP0_7I -> HTMCP_UP[0..7] <12>

-HTMCP_UP0_7I -> -HTMCP_UP[0..7] <12>



GIGABYTE		
MCP51-HT BUS		
Title		
Size	Document Number	Rev
Custom	GA-M55plus-S3G	1.0
Date:	Friday, May 05, 2006	Sheet 16 of 38



SP TX2P_C C1270 0.01U/4/X7R/16V/K
 SP TX2M_C C1271 0.01U/4/X7R/16V/K
 SP RX2M_C C1272 0.01U/4/X7R/16V/K
 SP RX2P_C C1273 0.01U/4/X7R/16V/K

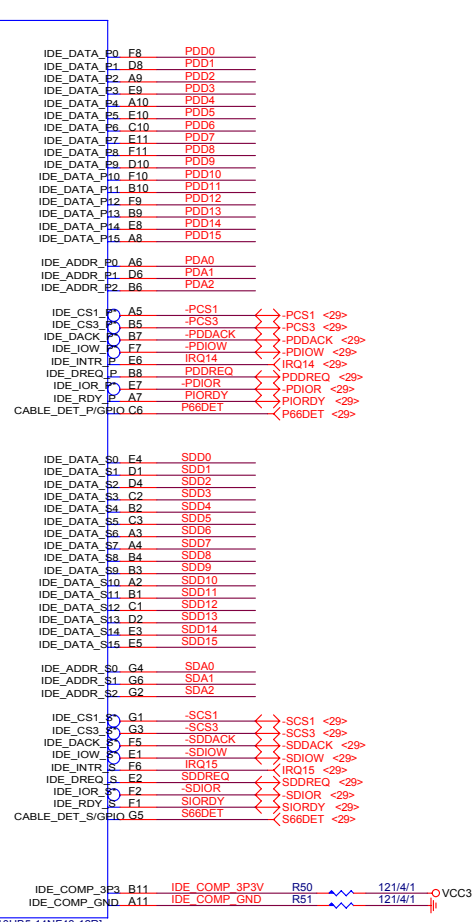
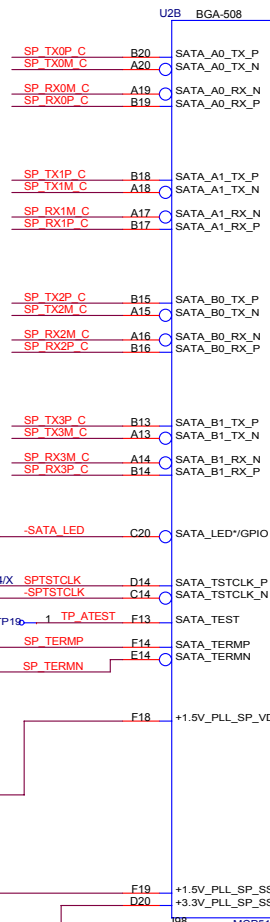
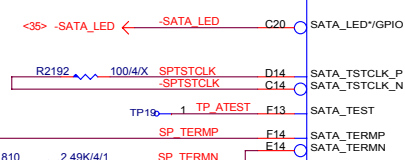
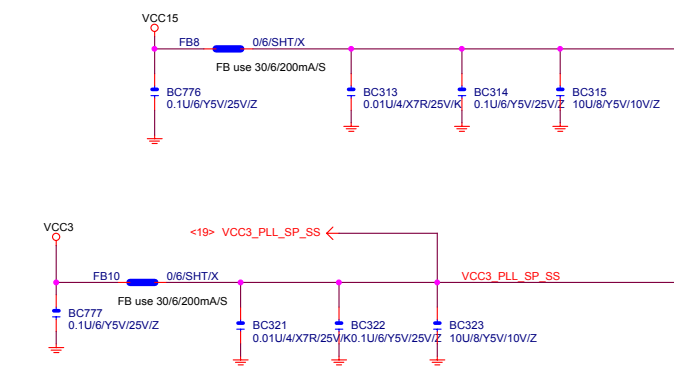
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 SP RX3M_C C1276 0.01U/4/X7R/16V/K
 SP RX3P_C C1277 0.01U/4/X7R/16V/K

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 SP RX0P_C C1265 0.01U/4/X7R/16V/K

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 SP TX1M_C C1267 0.01U/4/X7R/16V/K
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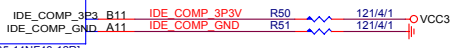
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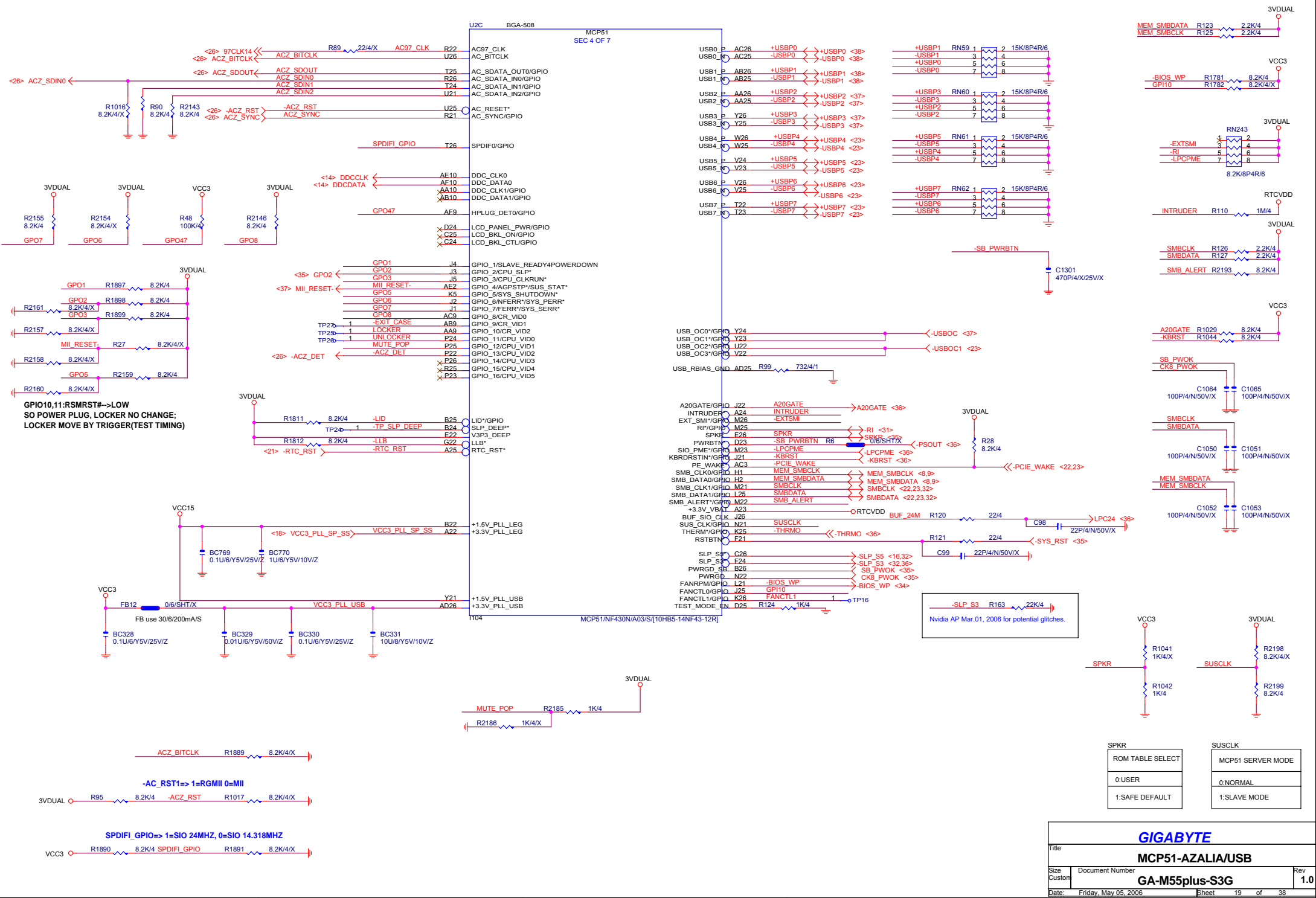
SATAII0_1
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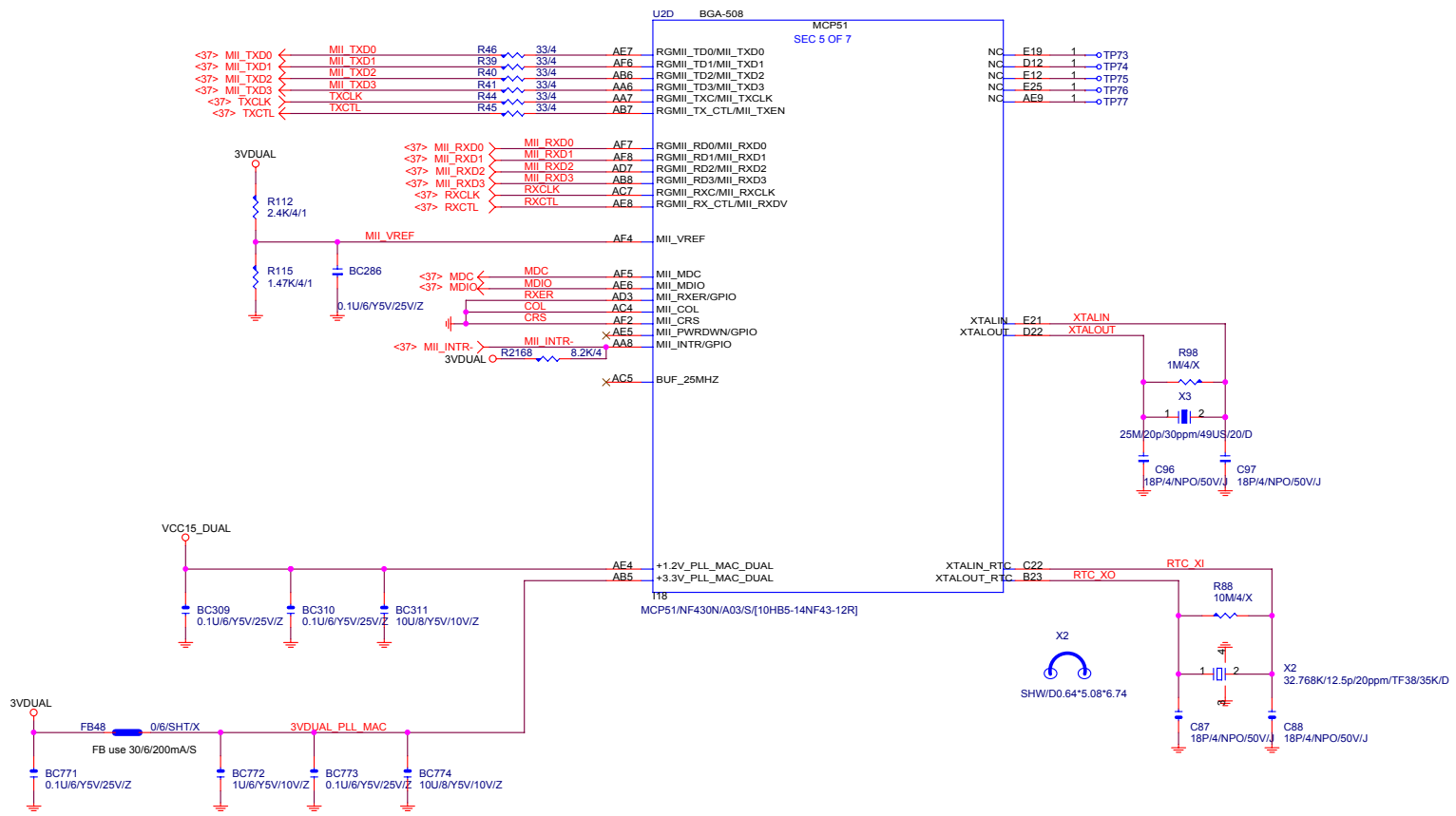


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 PDAI0_21 <-> PDAI[0..21] <-29>

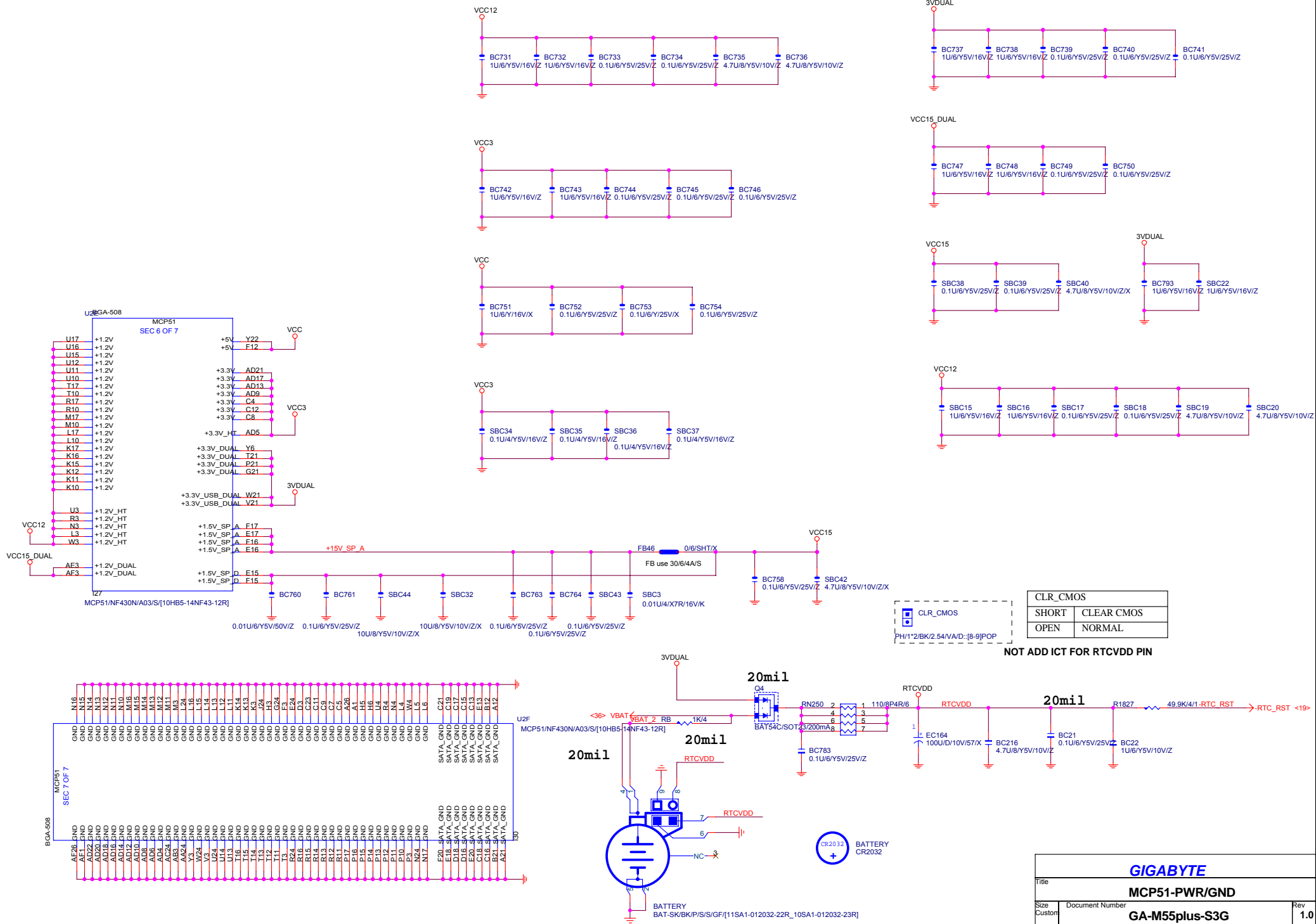
SDDI0_15 <-> SDDI[0..15] <-29>
 SDAI0_21 <-> SDAI[0..21] <-29>







GIGABYTE		
MCP51-RGMII		
Title	Rev 1.0	
Size	Document Number	GA-M55plus-S3G
Custom	Date: Friday, May 05, 2006	Sheet 20 of 38



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

EXP_A_RXP0_15] >> EXP_A_RXP[0..15] <-13>

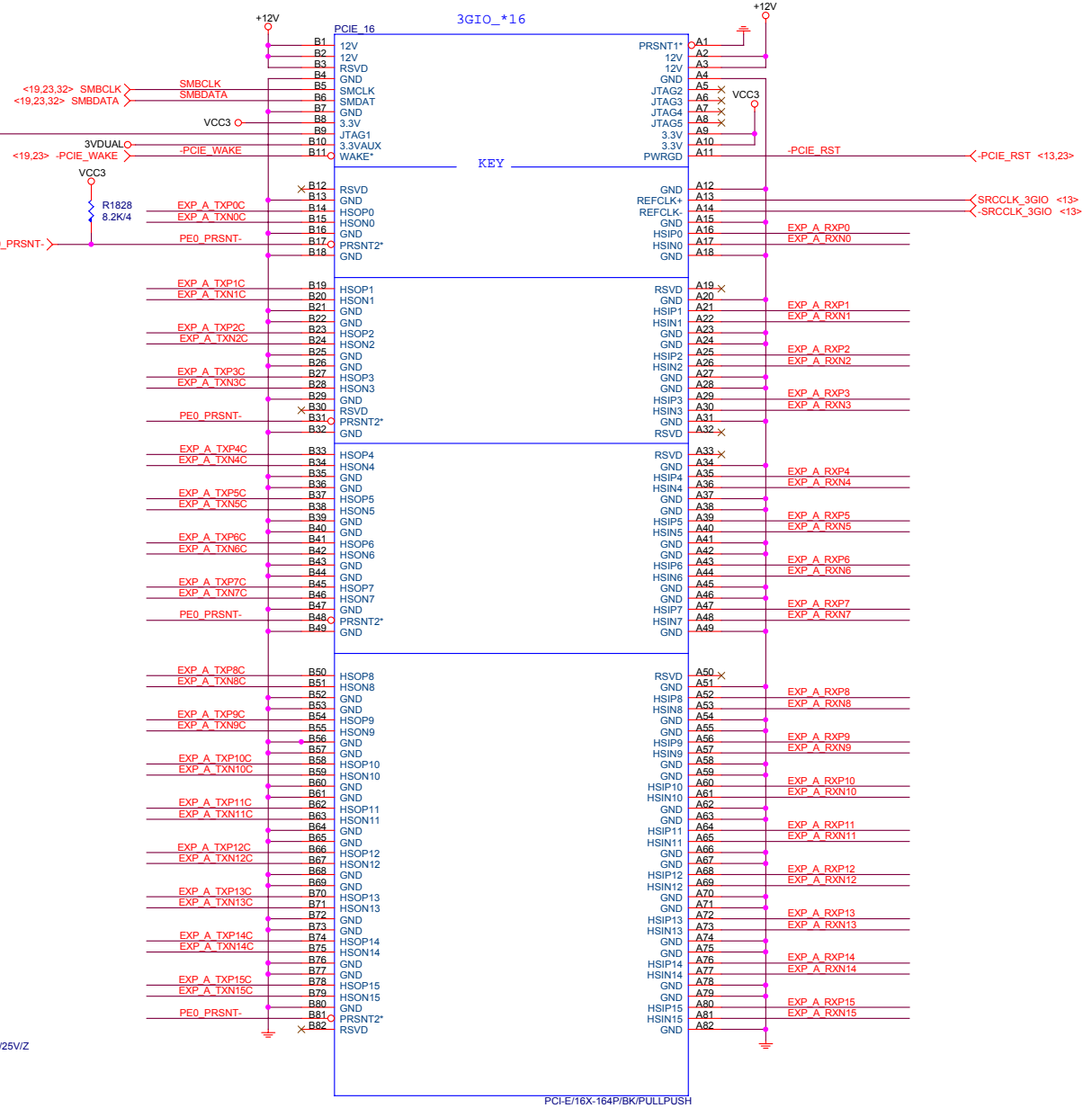
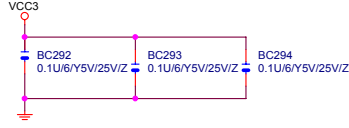
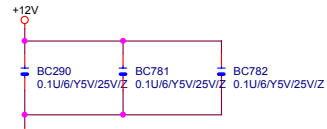
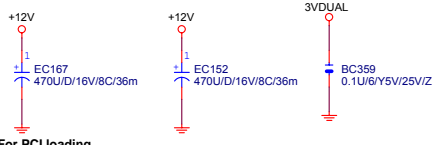
EXP_A_RXN0_15] >> EXP_A_RXN[0..15] <-13>

-PCIE_RST

EXP_A_TXP0_15] >> EXP_A_TXP[0..15] <-13>

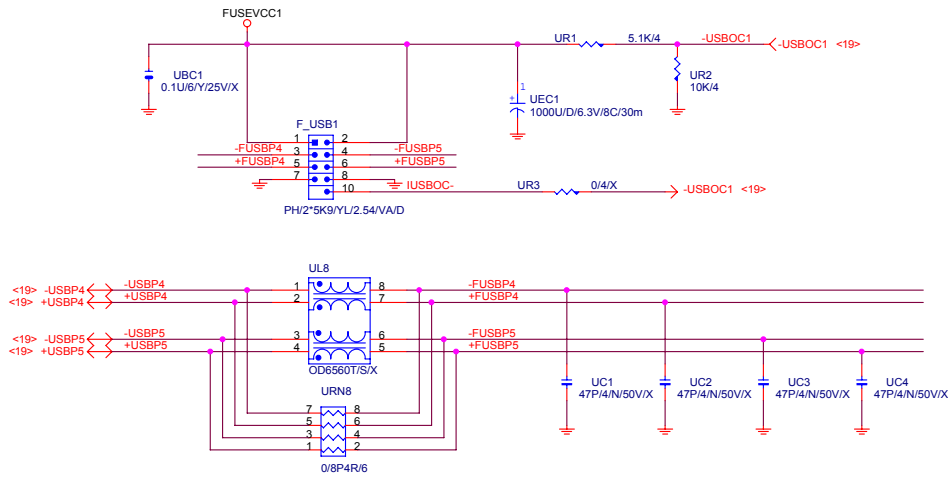
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EXP_A_TXP1	C129	0.1U/4/Y5V/16V/Z	EXP_A_TXP1C
EXP_A_TXN1	C130	0.1U/4/Y5V/16V/Z	EXP_A_TXN1C
EXP_A_TXP2	C131	0.1U/4/Y5V/16V/Z	EXP_A_TXP2C
EXP_A_TXN2	C132	0.1U/4/Y5V/16V/Z	EXP_A_TXN2C
EXP_A_TXP3	C133	0.1U/4/Y5V/16V/Z	EXP_A_TXP3C
EXP_A_TXN3	C134	0.1U/4/Y5V/16V/Z	EXP_A_TXN3C
EXP_A_TXP4	C135	0.1U/4/Y5V/16V/Z	EXP_A_TXP4C
EXP_A_TXN4	C136	0.1U/4/Y5V/16V/Z	EXP_A_TXN4C
EXP_A_TXP5	C137	0.1U/4/Y5V/16V/Z	EXP_A_TXP5C
EXP_A_TXN5	C138	0.1U/4/Y5V/16V/Z	EXP_A_TXN5C
EXP_A_TXP6	C139	0.1U/4/Y5V/16V/Z	EXP_A_TXP6C
EXP_A_TXN6	C140	0.1U/4/Y5V/16V/Z	EXP_A_TXN6C
EXP_A_TXP7	C141	0.1U/4/Y5V/16V/Z	EXP_A_TXP7C
EXP_A_TXN7	C142	0.1U/4/Y5V/16V/Z	EXP_A_TXN7C
EXP_A_TXP8	C143	0.1U/4/Y5V/16V/Z	EXP_A_TXP8C
EXP_A_TXN8	C144	0.1U/4/Y5V/16V/Z	EXP_A_TXN8C
EXP_A_TXP9	C145	0.1U/4/Y5V/16V/Z	EXP_A_TXP9C
EXP_A_TXN9	C146	0.1U/4/Y5V/16V/Z	EXP_A_TXN9C
EXP_A_TXP10	C147	0.1U/4/Y5V/16V/Z	EXP_A_TXP10C
EXP_A_TXN10	C148	0.1U/4/Y5V/16V/Z	EXP_A_TXN10C
EXP_A_TXP11	C149	0.1U/4/Y5V/16V/Z	EXP_A_TXP11C
EXP_A_TXN11	C150	0.1U/4/Y5V/16V/Z	EXP_A_TXN11C
EXP_A_TXP12	C151	0.1U/4/Y5V/16V/Z	EXP_A_TXP12C
EXP_A_TXN12	C153	0.1U/4/Y5V/16V/Z	EXP_A_TXN12C
EXP_A_TXP13	C155	0.1U/4/Y5V/16V/Z	EXP_A_TXP13C
EXP_A_TXN13	C156	0.1U/4/Y5V/16V/Z	EXP_A_TXN13C
EXP_A_TXP14	C157	0.1U/4/Y5V/16V/Z	EXP_A_TXP14C
EXP_A_TXN14	C158	0.1U/4/Y5V/16V/Z	EXP_A_TXN14C
EXP_A_TXP15	C159	0.1U/4/Y5V/16V/Z	EXP_A_TXP15C
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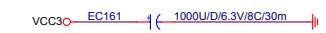
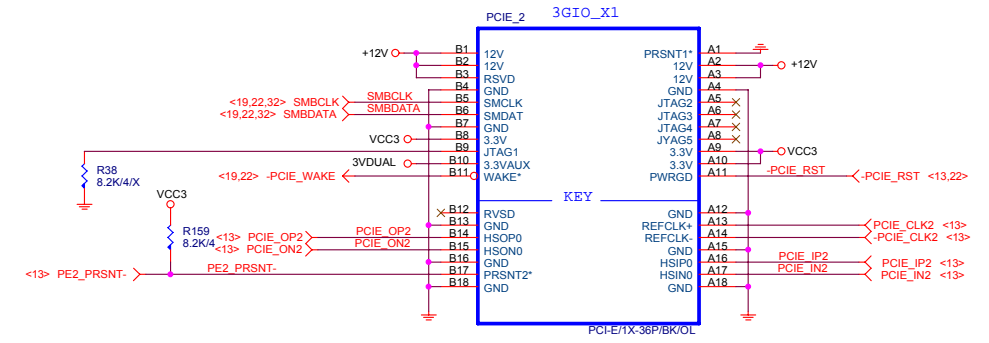
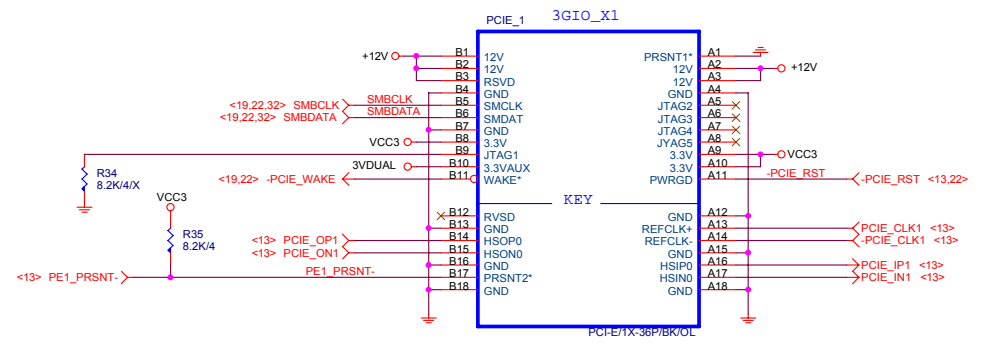
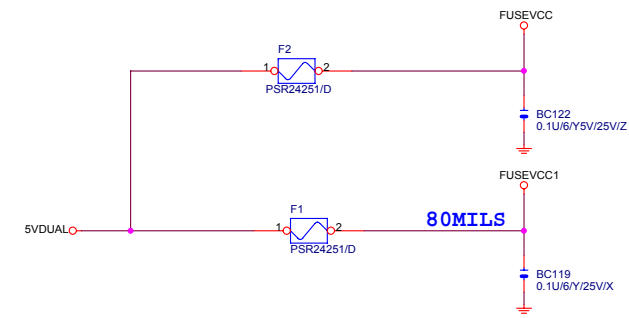
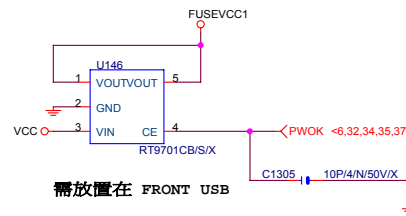
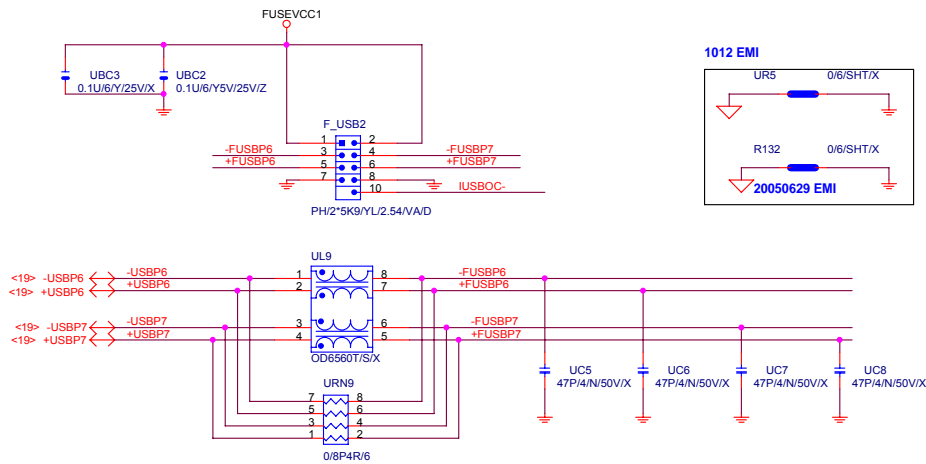


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Size Custom	Document Number GA-M55plus-S3G	Rev 1.0
Date	Friday, May 05, 2006	Sheet 22 of 38

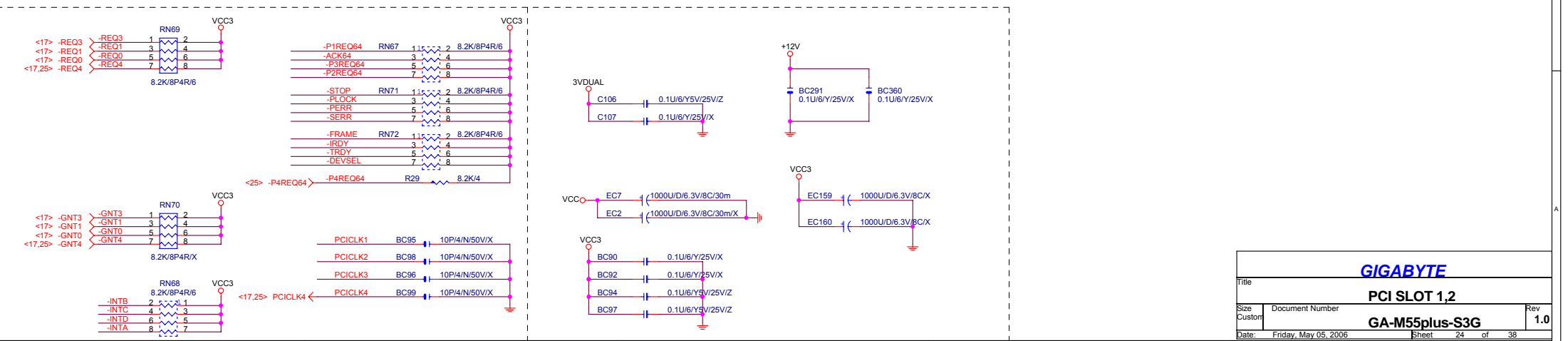
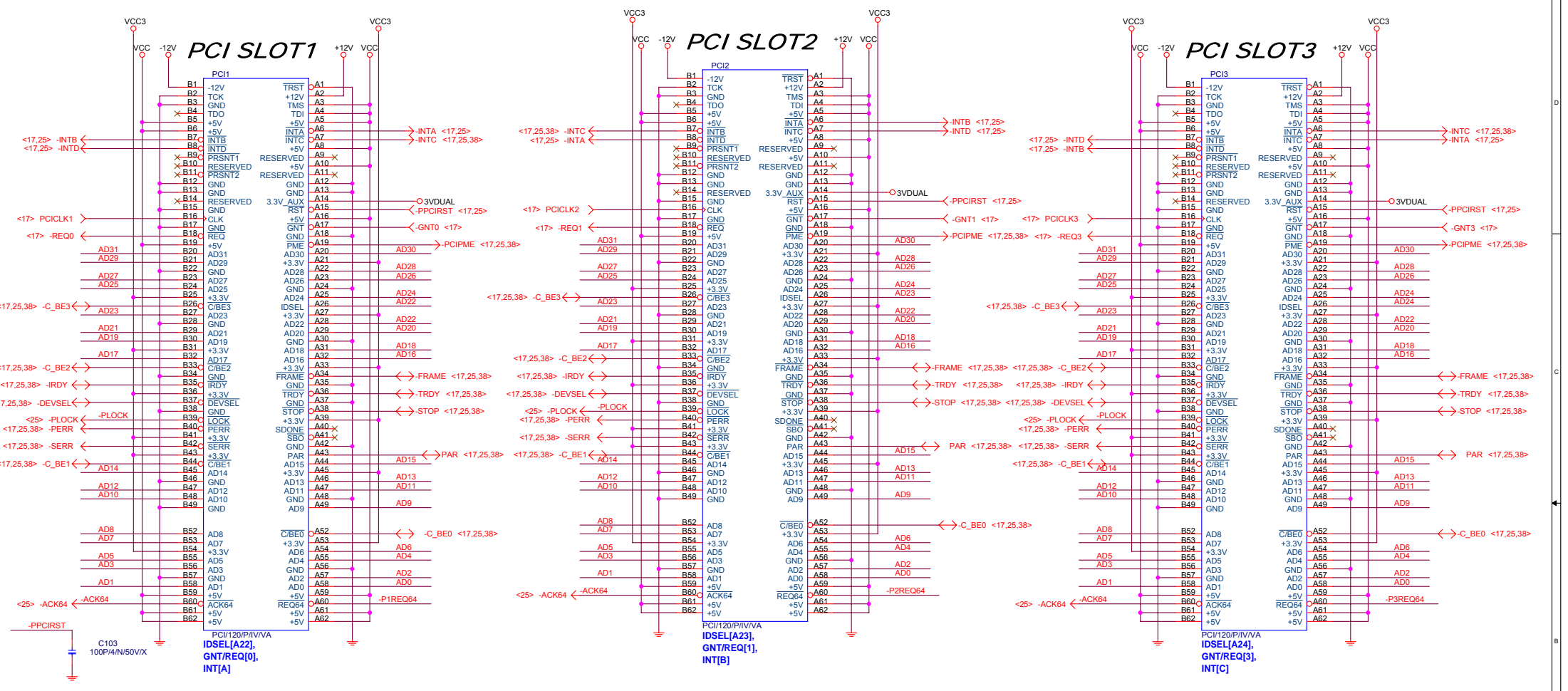
FRONT SIDE USB1



FRONT SIDE USB2



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Size	Document Number	Rev
Custom	GA-M55plus-S3G	1.0
Date:	Sheet 23 of 38	

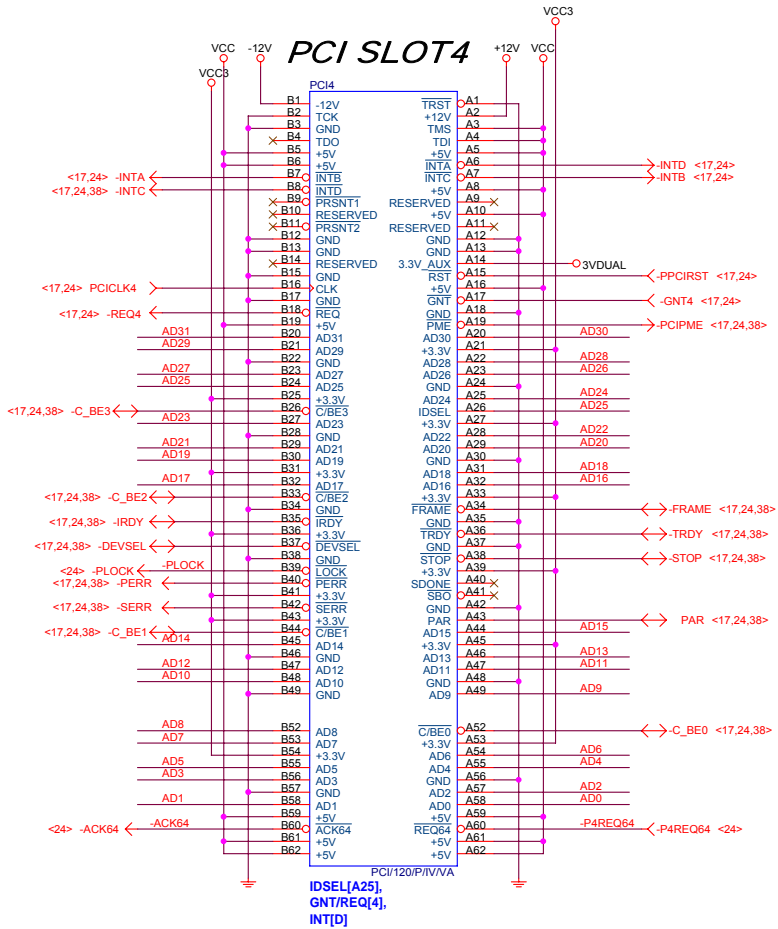


GIGABYTE		
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Title	Document Number	Rev
	GA-M55plus-S3G	1.0
Size Custom	Date: Friday, May 05, 2006	Sheet 24 of 38

PCI SLOT 4

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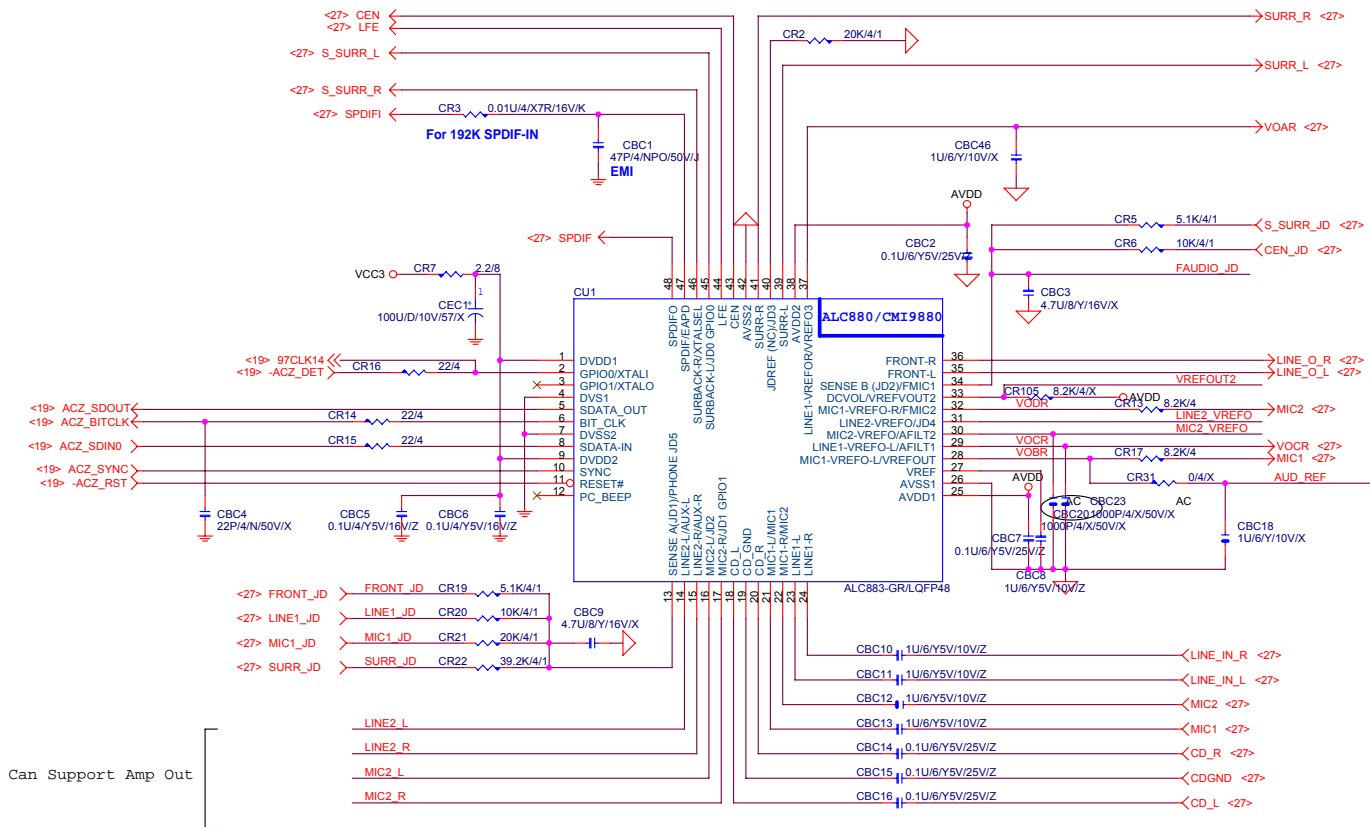
PCI SLOT 4



PCI120/P1/VVA
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 INT[D]

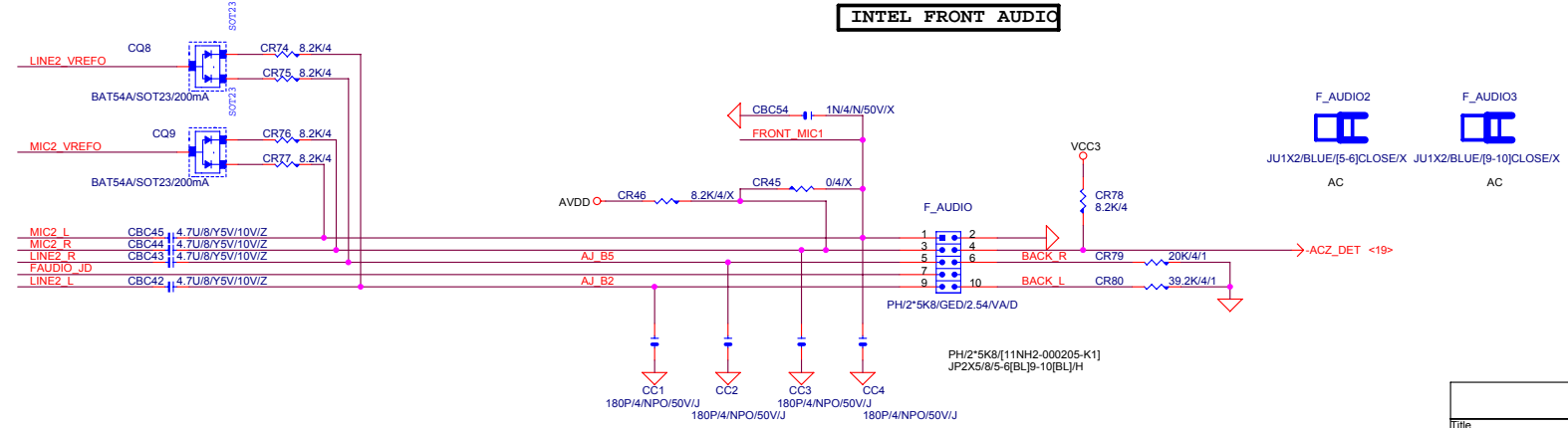
GIGABYTE

Title			PCI SLOT 1,2,3		
Size	Document Number				Rev
Custom	GA-M55plus-S3G				1.0
Date:	Friday, May 05, 2006	Sheet	25	of	38

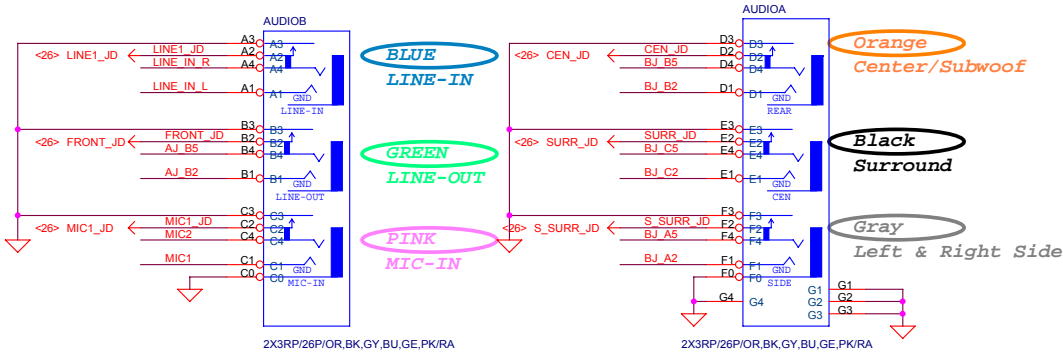
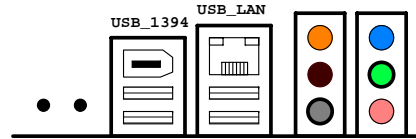
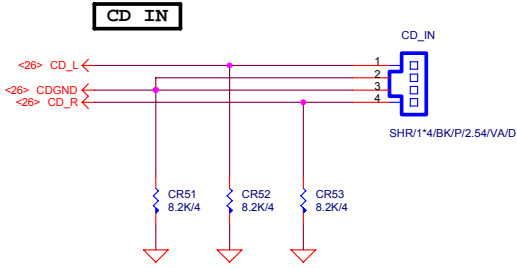
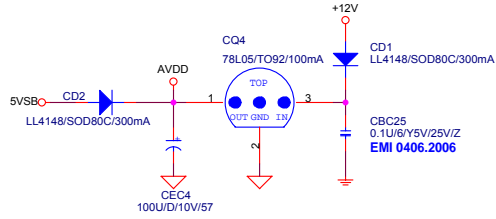
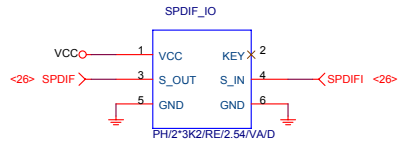
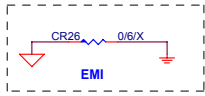


Can Support Amp Out

INTEL FRONT AUDIC



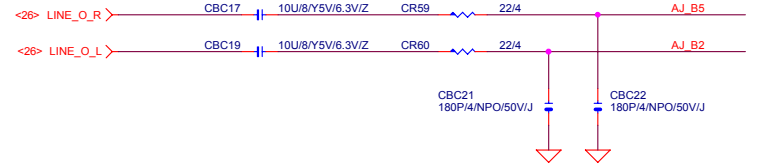
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Title ALC883			
Size Custom	Document Number	GA-M55plus-S3G	
Date: Friday, May 05, 2006	Sheet	26	of 38
			Rev 1.0



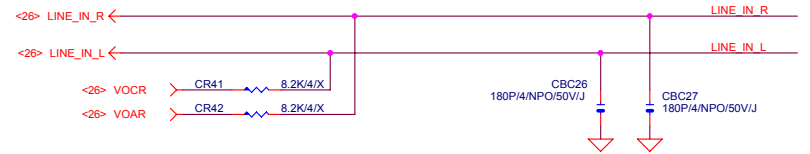
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3RJ+15F/[11NR6-403004-11]

A3RJ13P/OBG/[11NR6-403006-71]
3RJ+15F/[11NR6-403004-31]

LINE OUT FRONT OUT



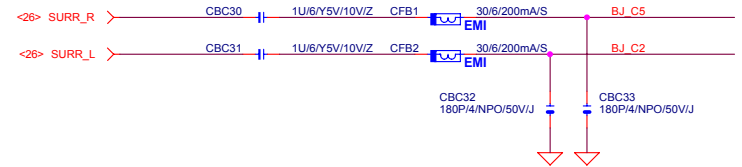
LINE-IN



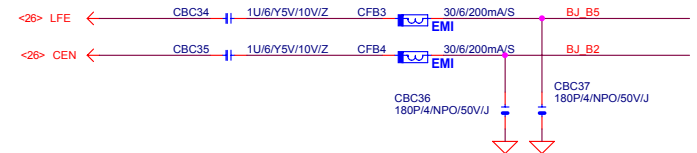
MIC



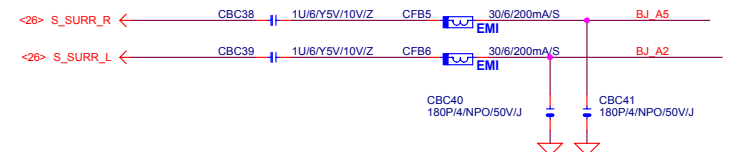
SURROUND



CEN/LFE

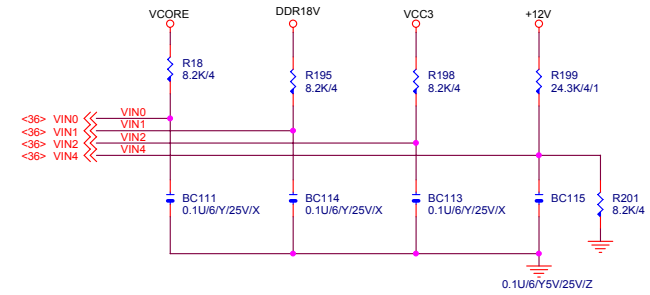
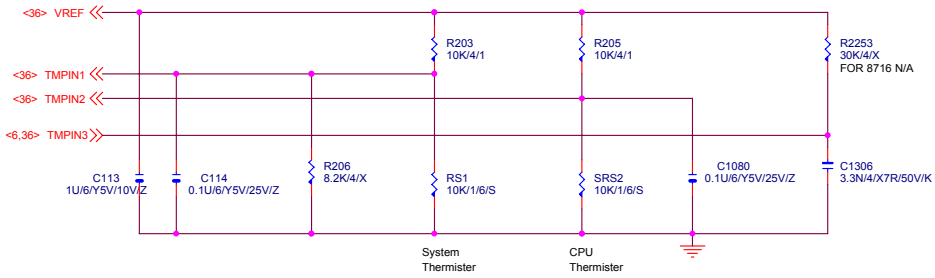


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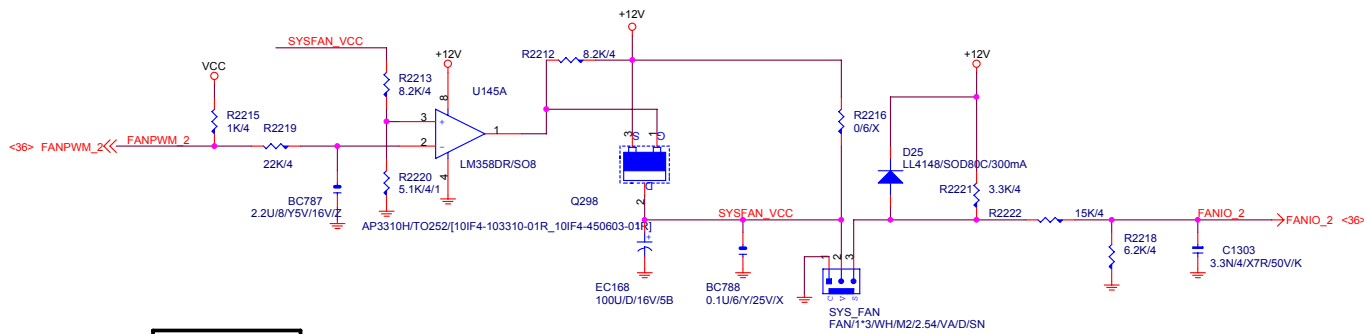


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AUDIO JACK		
Document Number	GA-M55plus-S3G	
Date:	Friday, May 05, 2006	Rev 1.0
Sheet	27	of 38

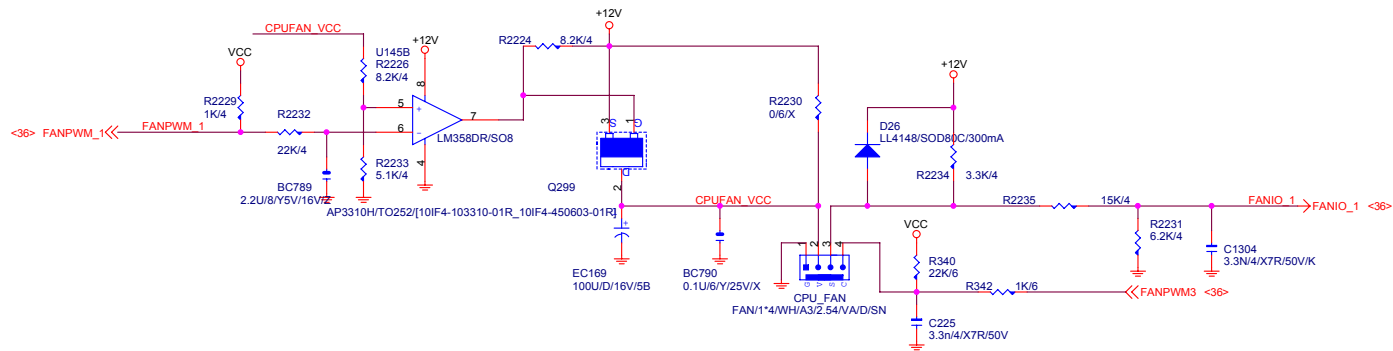
Hardware Monitor circuits



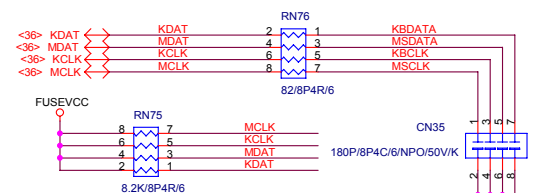
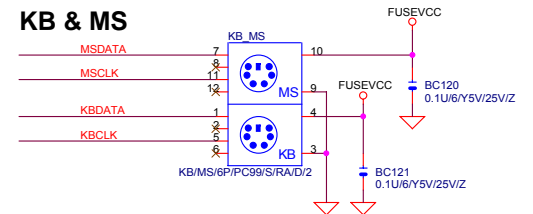
SYSTEM FAN



CPU FAN

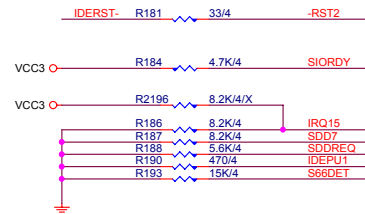
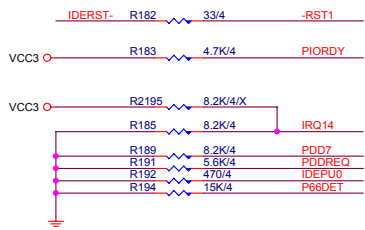
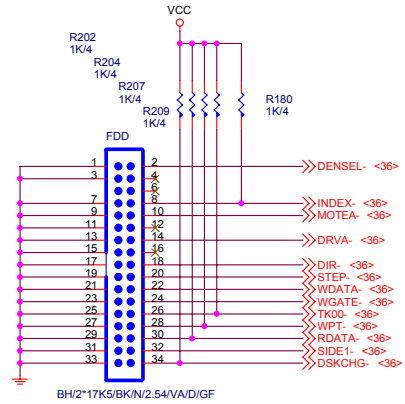
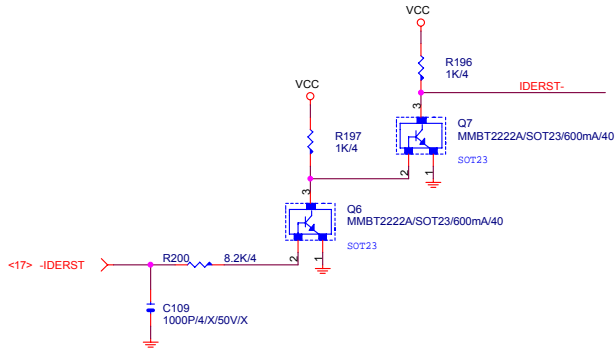


KB & MS

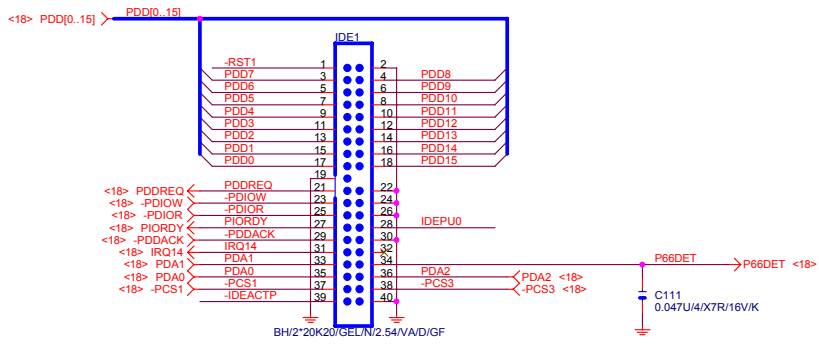


GIGABYTE

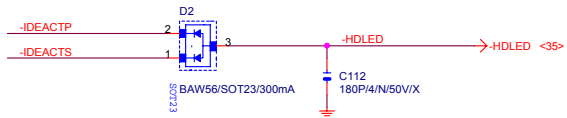
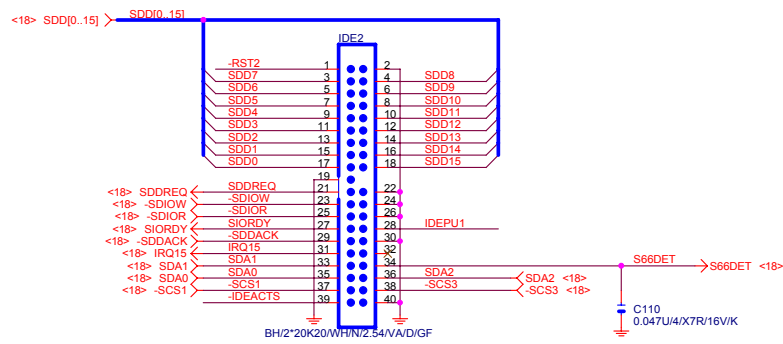
Title			FAN/HWMO KB/MS		
Size	Document Number	GA-M55plus-S3G			Rev
Custom					1.0
Date:	Friday, May 05, 2006	Sheet	28	of	38



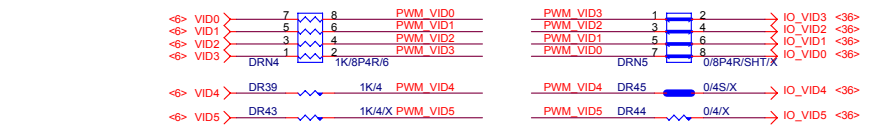
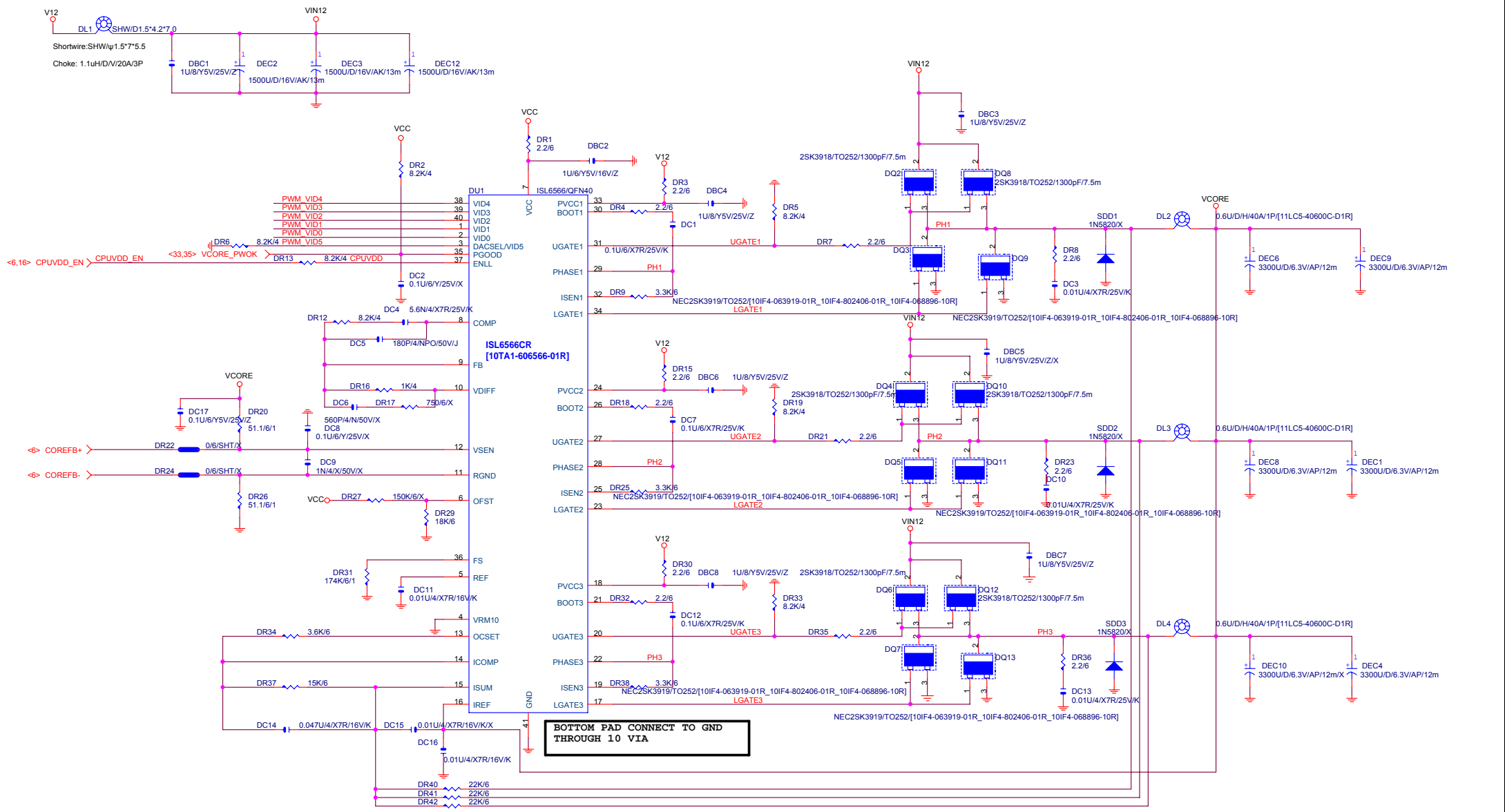
PRIMARY IDE CONNECTOR



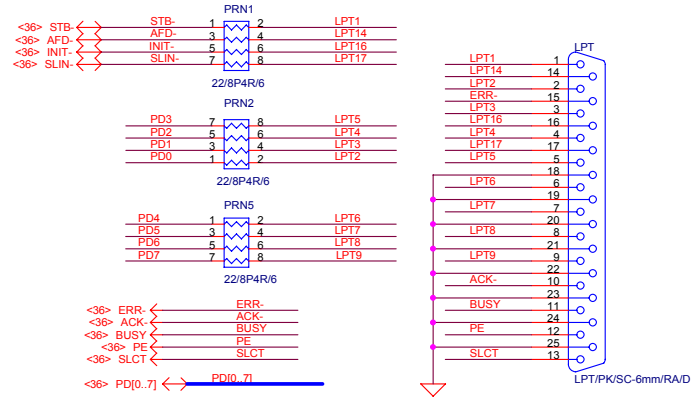
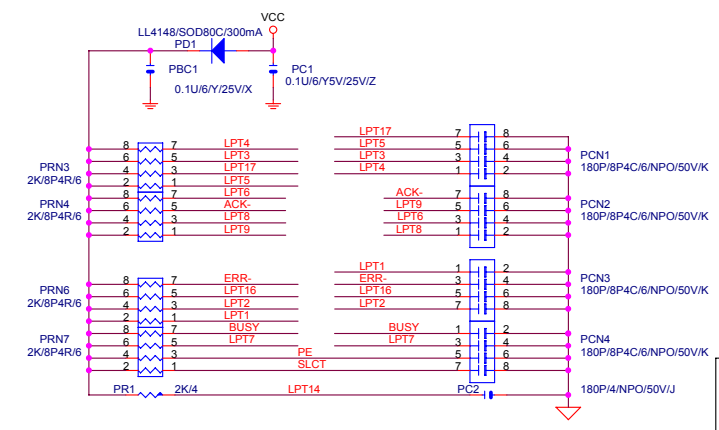
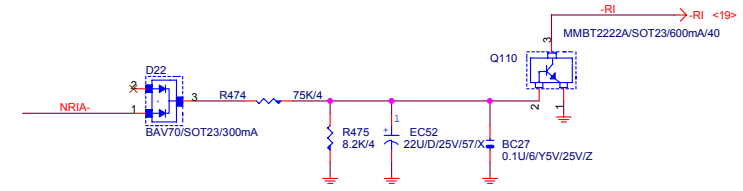
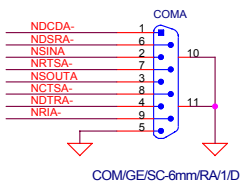
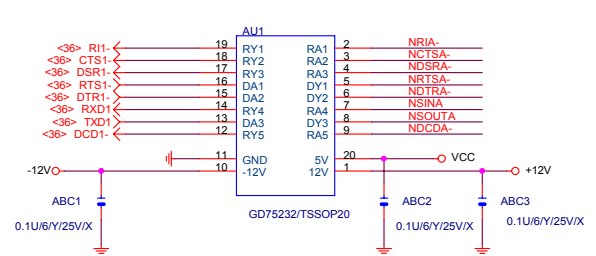
SECONDARY IDE CONNECTOR



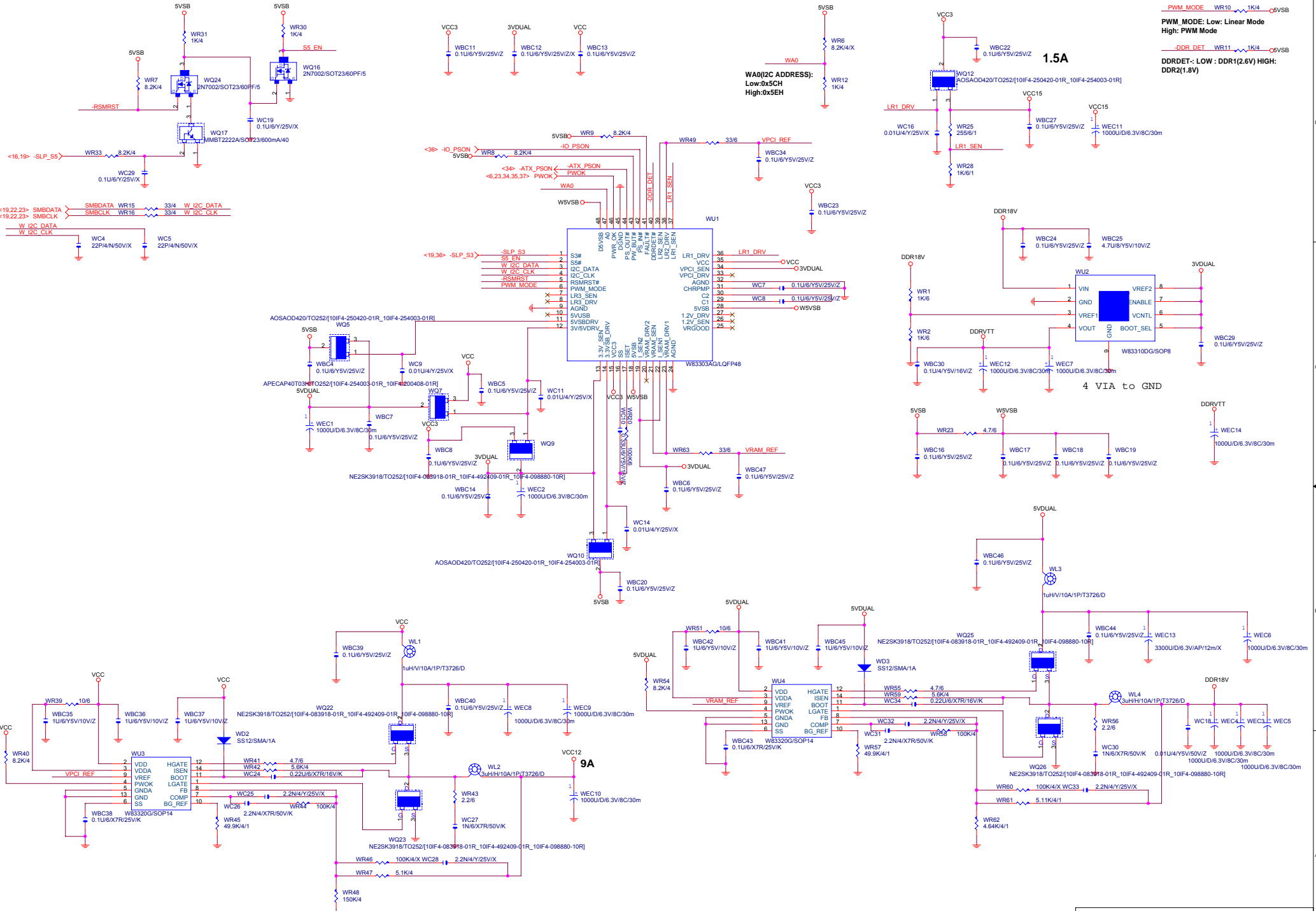
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IDE CONNECTOR		
Title	Document Number	Rev
	GA-M55plus-S3G	1.0
Date:	Sheet 29 of 38	

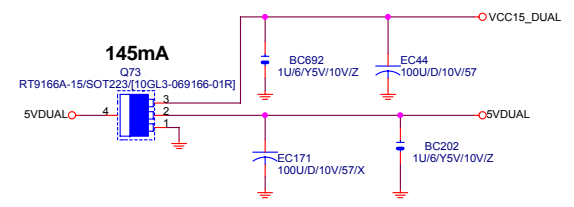
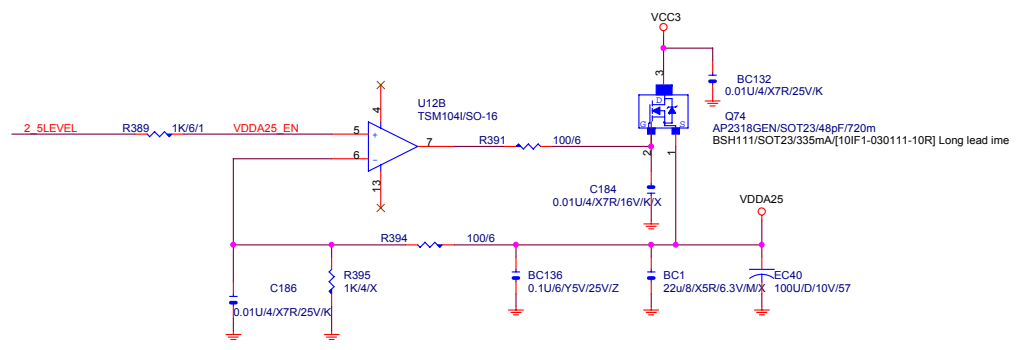
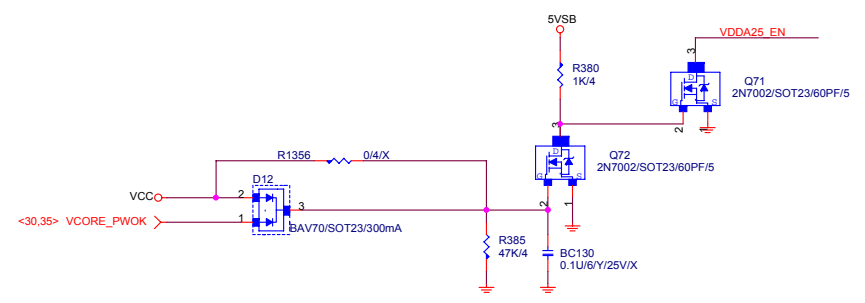
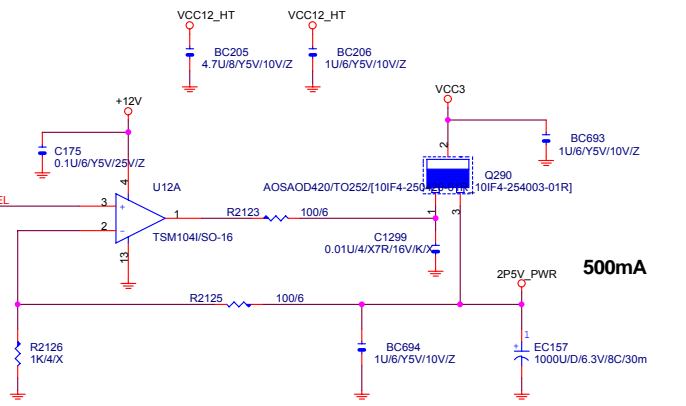
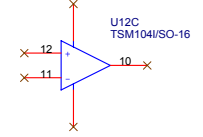
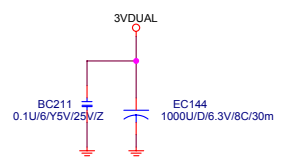
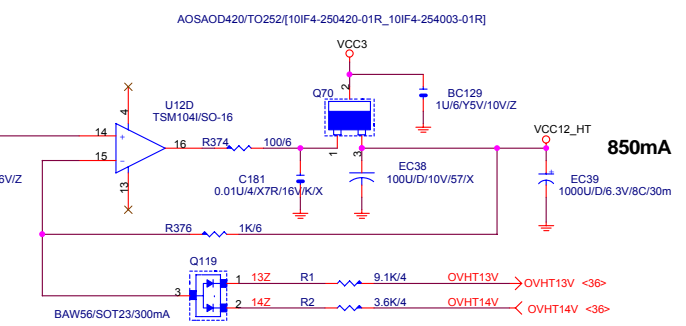
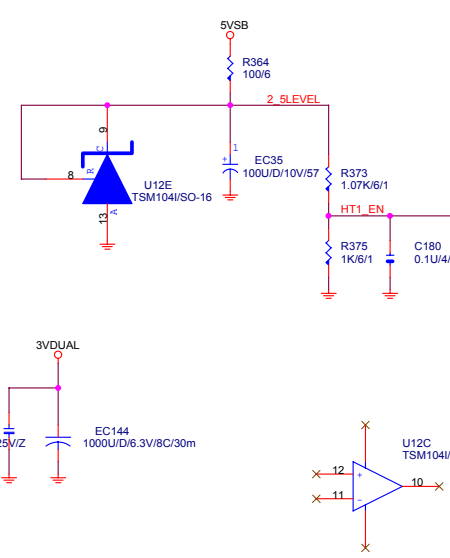
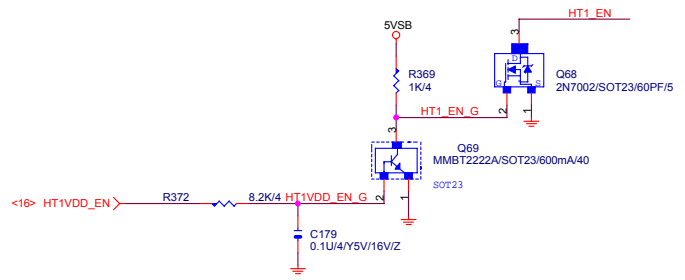


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VCORE (PWM ISL6559BC+6602B+6601B)		
Title	Document Number	Rev
Size	GA-M55plus-S3G	1.0
Custom		
Date:	Friday, May 05, 2006	Sheet 30 of 38



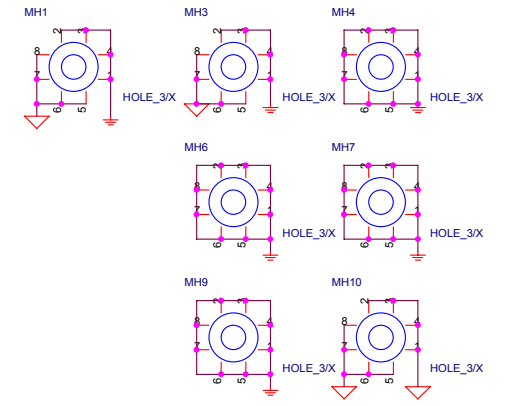
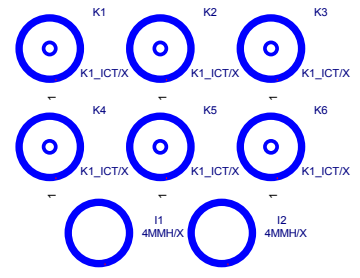
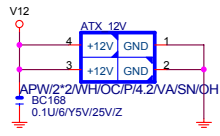
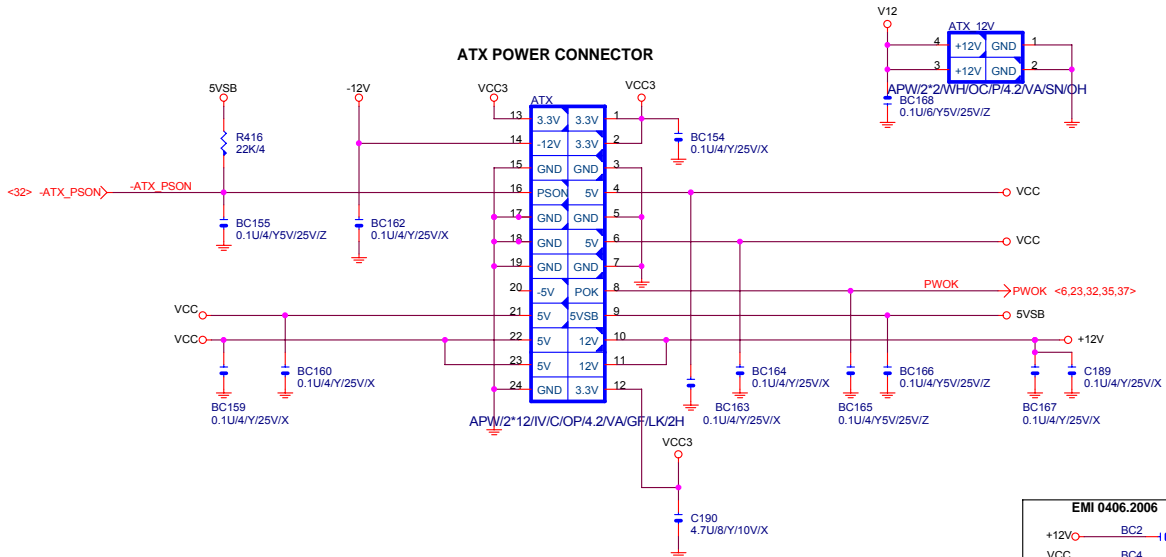
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Title	Rev 1.0	
Size	Document Number	GA-M55plus-S3G
Custom	Date: Friday, May 05, 2006	Sheet 31 of 38





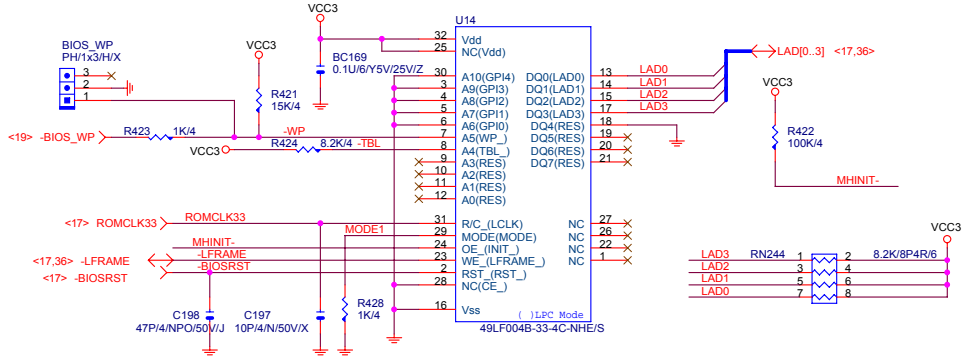
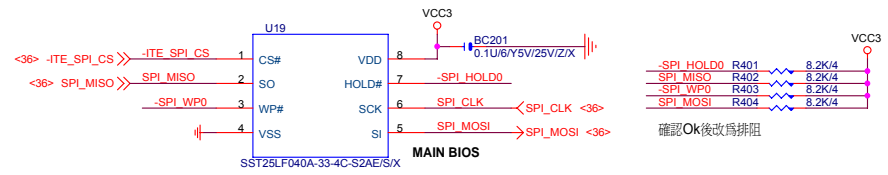
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Size	Document Number	Rev
	GA-M55plus-S3C	1.0
Date:	Friday, May 05, 2006	Sheet 33 of 38

ATX POWER CONNECTOR

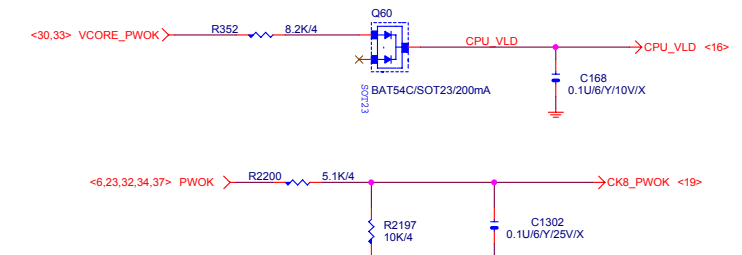
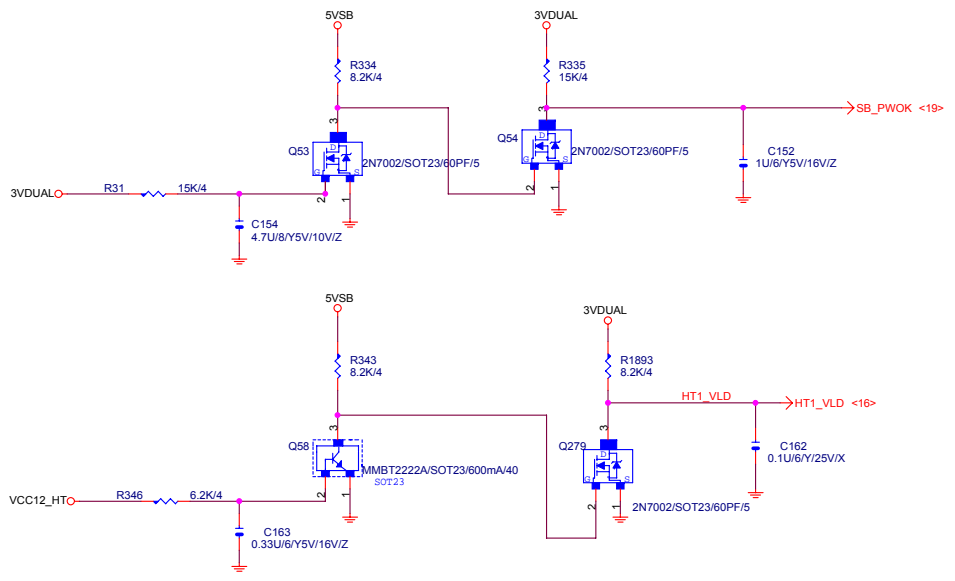
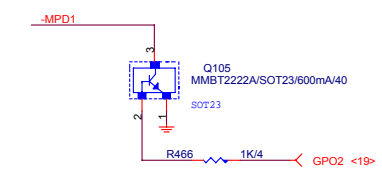
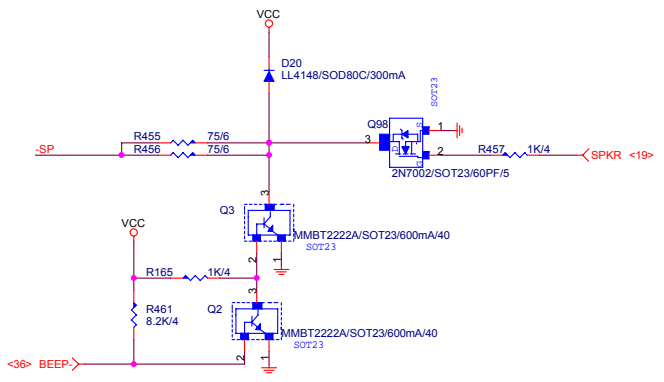
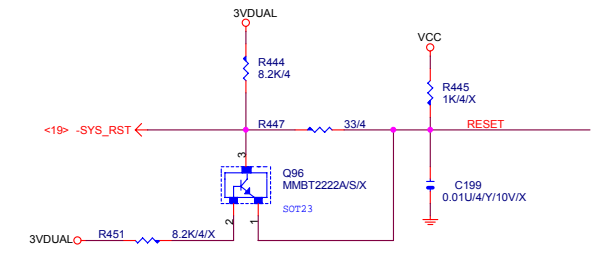
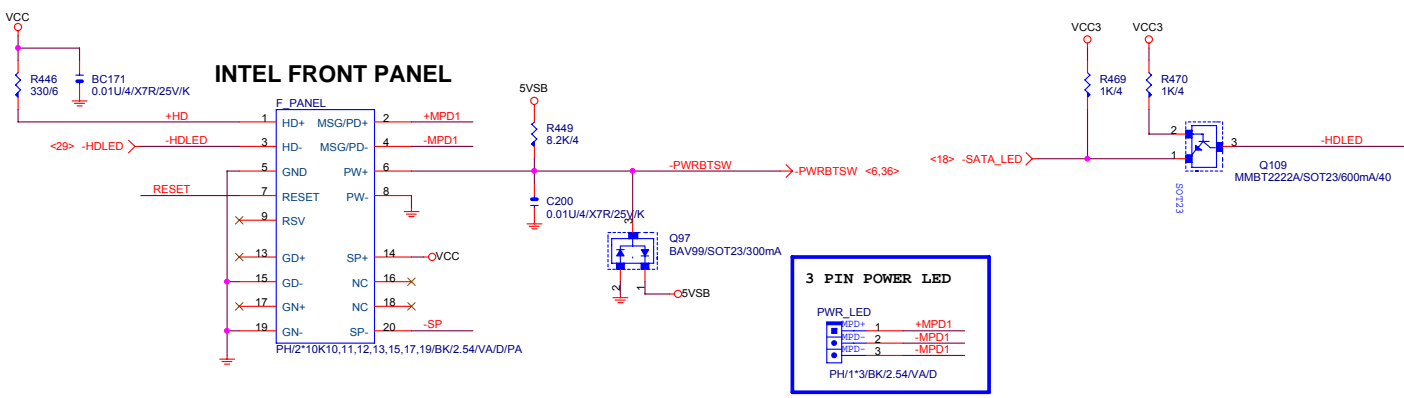


EMI 0406.2006

+12V	BC2	0.1U/6/Y/5V/25V/Z/X	VCC
VCC	BC4	0.1U/4/Y/5V/25V/Z/X	VCC3
VCC	BC3	0.1U/4/Y/5V/25V/Z/X	VCC3
VCC	BC5	0.1U/6/Y/5V/25V/Z/X	
VCC	BC7	0.1U/6/Y/5V/25V/Z/X	



GIGABYTE		
Title ATX CONN & BIOS		
Size Custom	Document Number GA-M55plus-S3G	Rev 1.0
Date:	Sheet 34	of 38

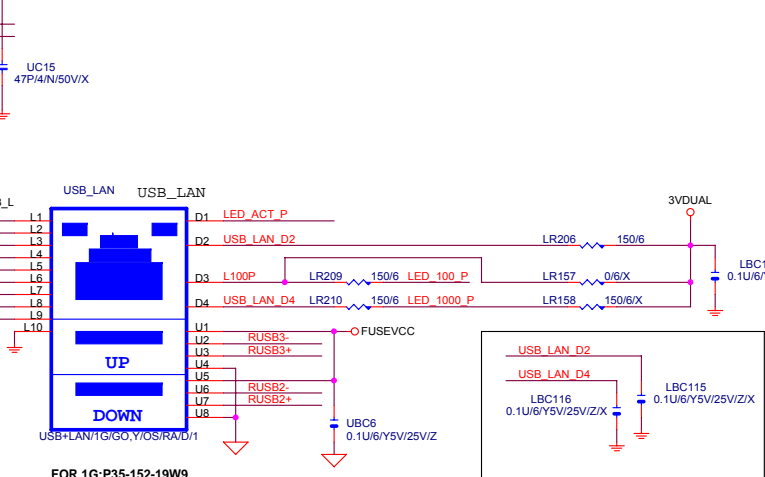
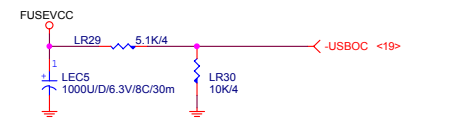
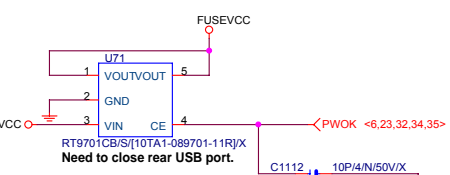
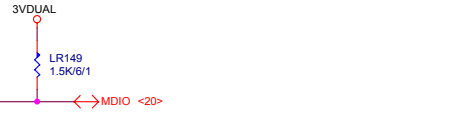
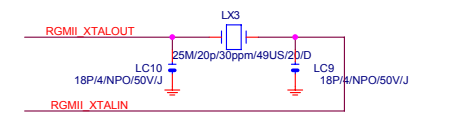
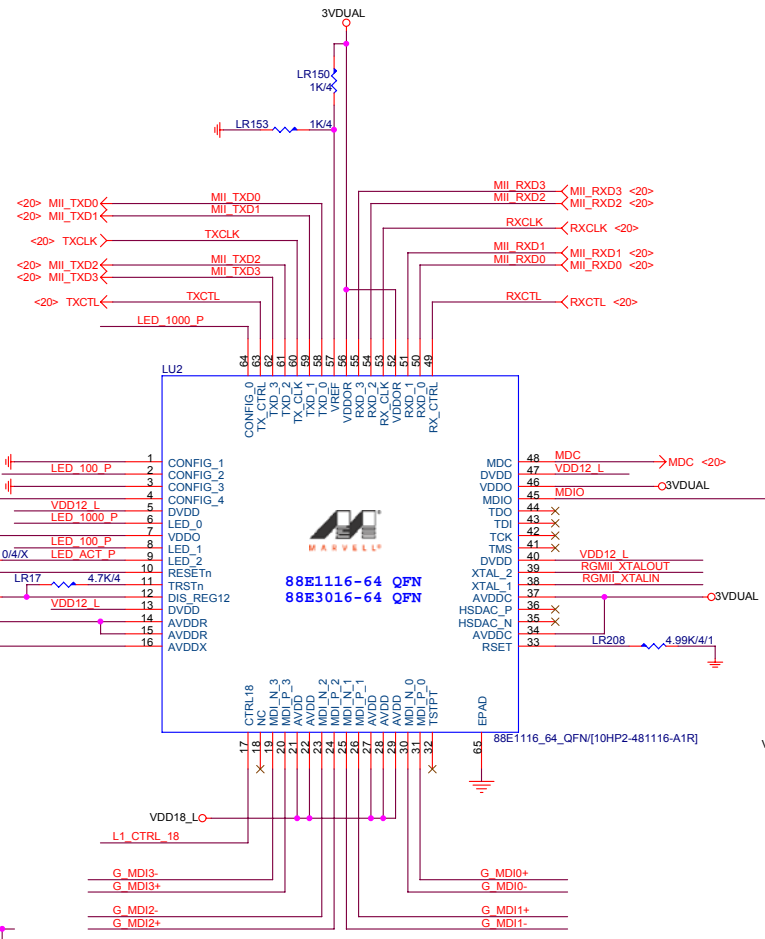
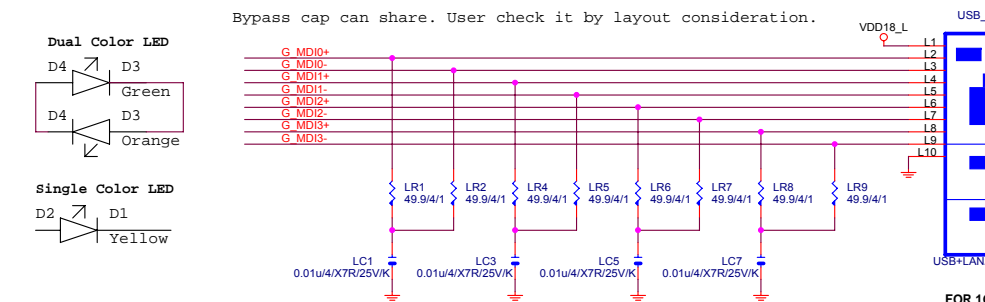
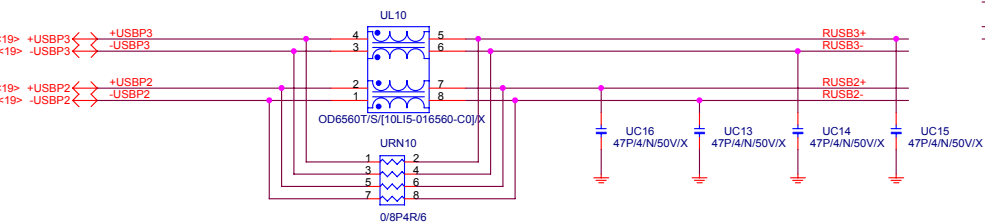
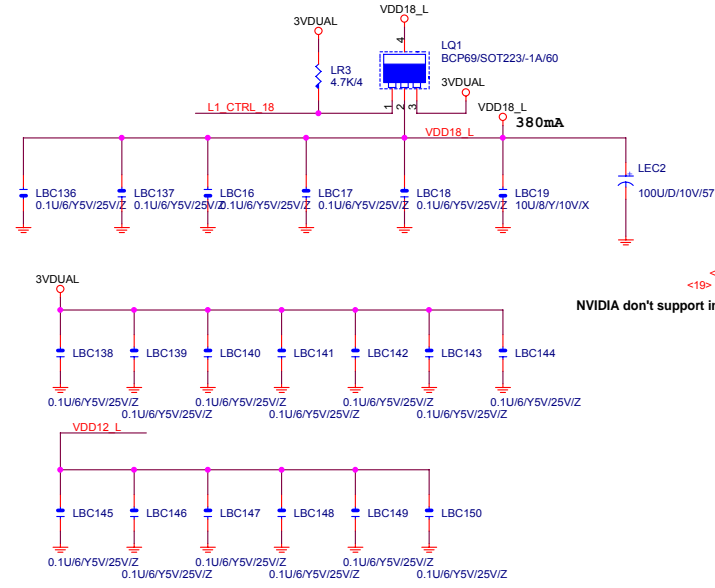


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PANEL & BUZZER			
Title	Document Number		Rev
Size	GA-M55plus-S3G		1.0
Custom			
Date:	Sheet	35	of 38

E1116 use external 2.5V single power supply.
 1.8V create by PNP and 1.2V use internal reg.

Hardware Configuration: See config_0:4

1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities



Title			Marvell_88E1116		
Size	Document Number				Rev
Custom	GA-M55plus-S3G			1.0	
Date:	Friday, May 05, 2006	Sheet	37	of	38

