

# GA-8S661FXM-775 Schematics

Revision : 1.0

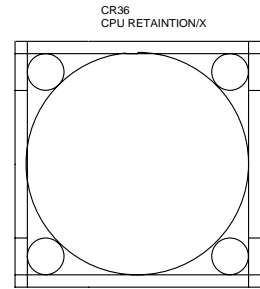
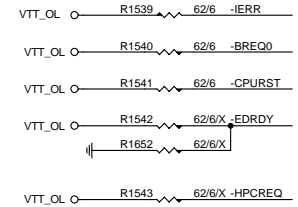
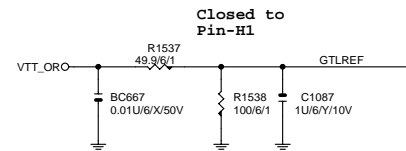
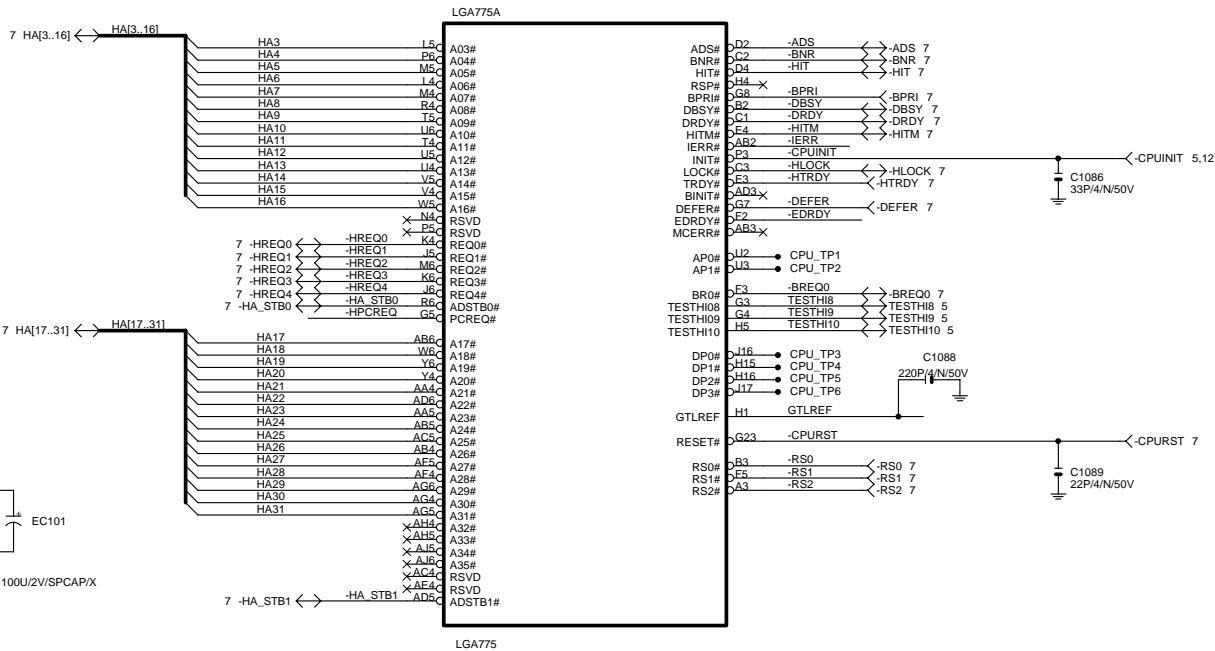
SHEET	TITLE
1	COVER SHEET
2	BOM & PCB MODIFY HISTORY
3	BLOCK DIAGRAM
4,5,6	INTEL CPU_WMT_478
7-10	SIS661FX (NORTH BRIDGE) HOST; DDR; AGP,HYPER ZIP
11-14	SIS964L (SOUTH BIRDGE)
15	CLOCK GENERATOR (ICS952018AF), BUFFER(ICS93722)
16,17	DDR SDRAM DIMMS 1,2
18	AGP SLOT
19	PCI SLOT 1,2,3
20	IDE,FRONT USB,PCIRST#
21	LPCIO_IT8705
22	BIOS
23	COM,PRT,FDD,KB/MS,IR
24	AC 97 ALC655
25	AUDIO JACK,SPDIF
26	FAN, IR
27	PANEL,STR LED,FANS ,CPU GN
28	VCORE PWM FAN5019 + FAN5009
29	VDDQ,VCC18,VTT_GMCH DC POWER
30	ATX CONN, GPIO LIST
31	DDR POWER

SHEET	TITLE
32	MARVELL 88E8001
33	ICS LAN PHY
34	VGA CONNECTOR

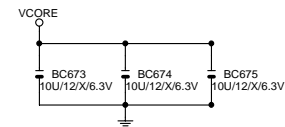
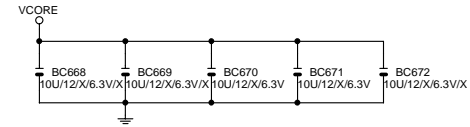
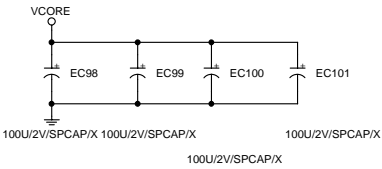
PCB Size: 244\*244 mm

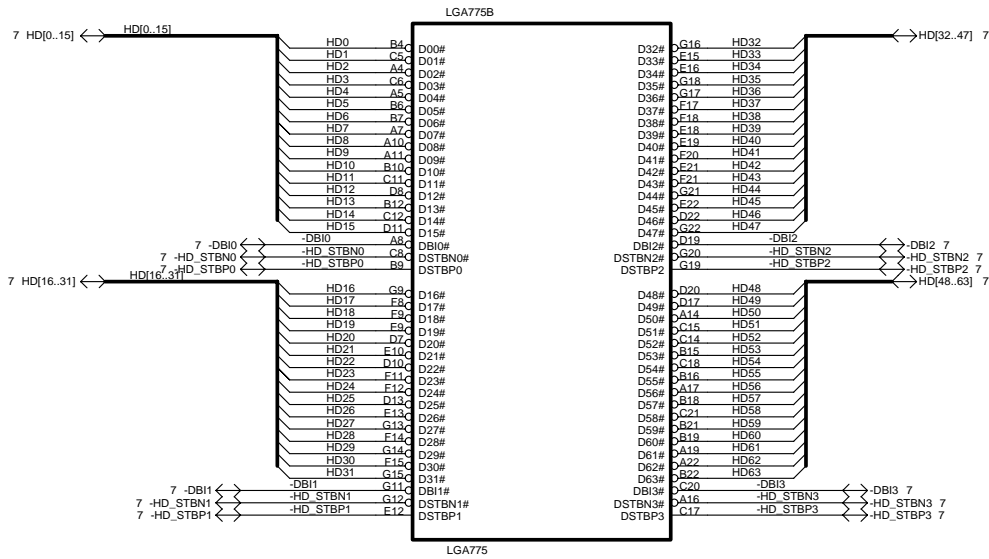
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Size Custom	Document Number <b>GIGABYTE</b>
Date: 星期一, 九月 06, 2004	Rev <b>1.0</b>
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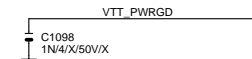
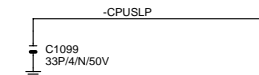
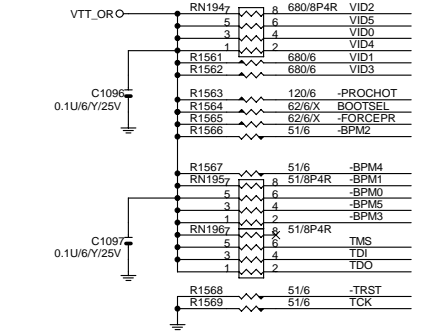
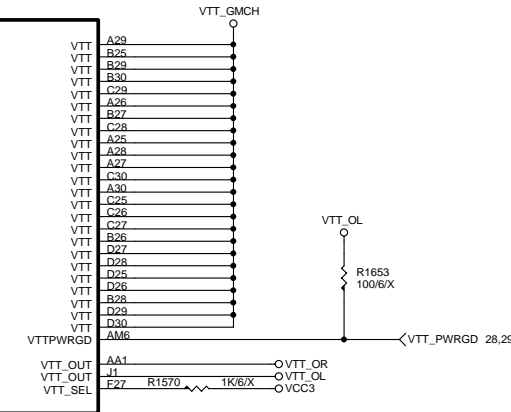
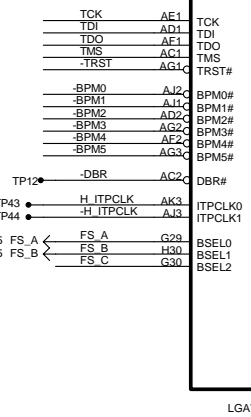
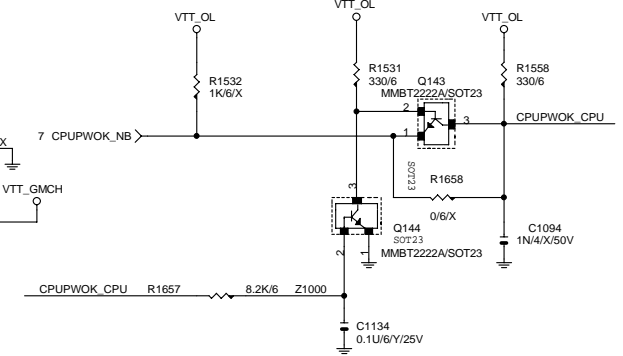
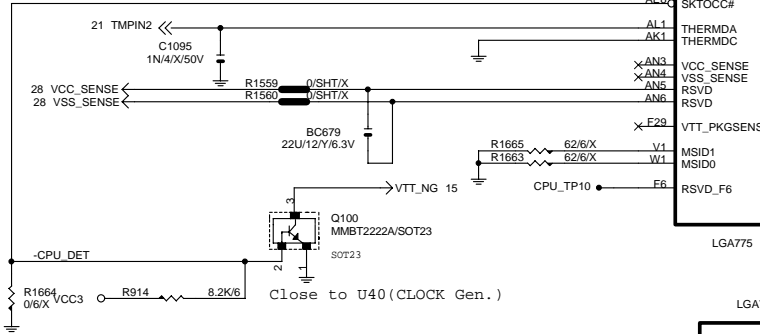
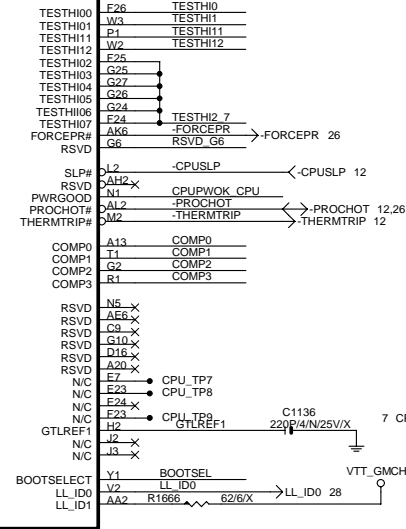
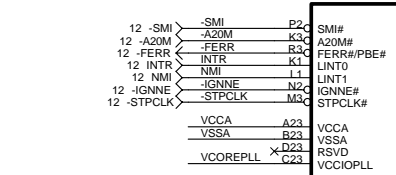
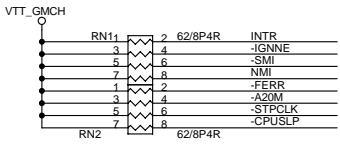
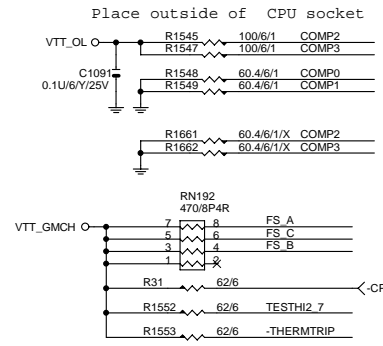
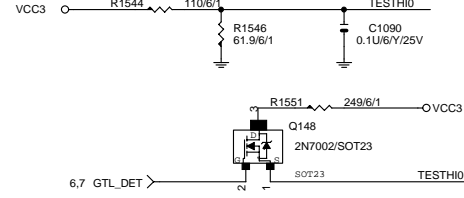
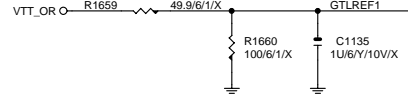
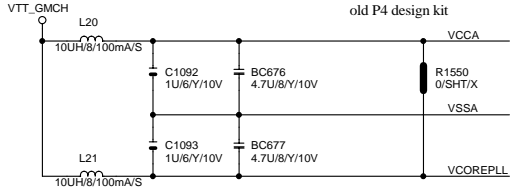


**SP-CAP X 4PCS**

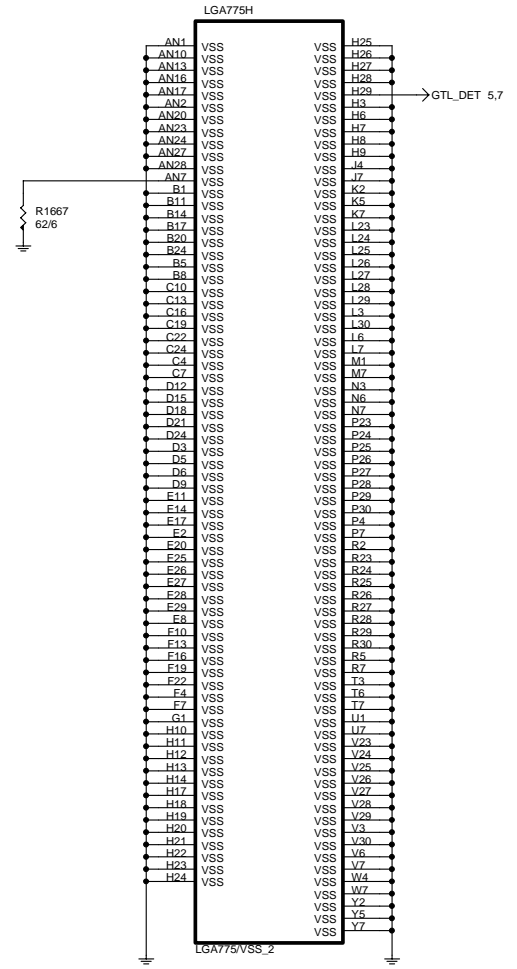
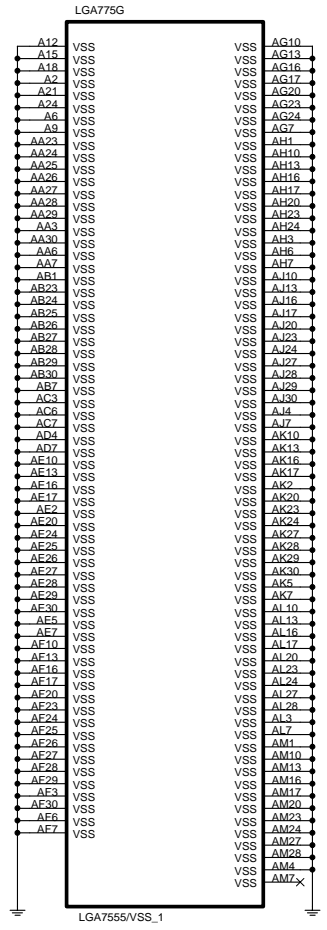
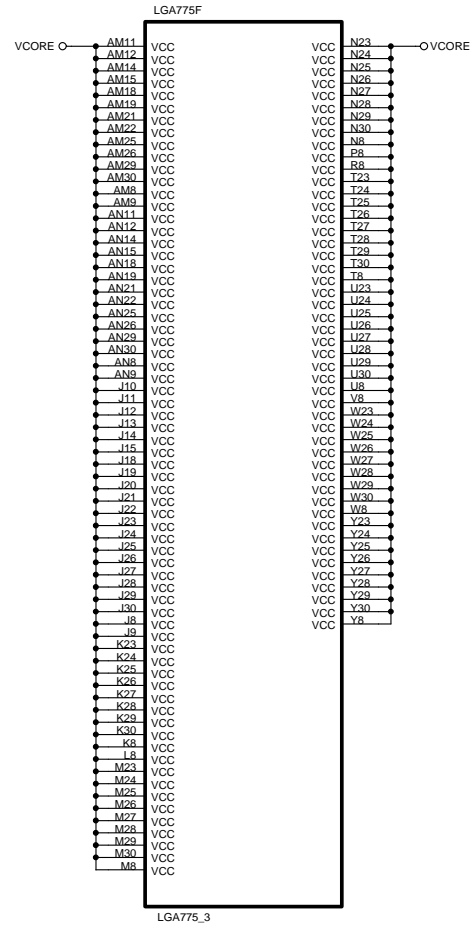
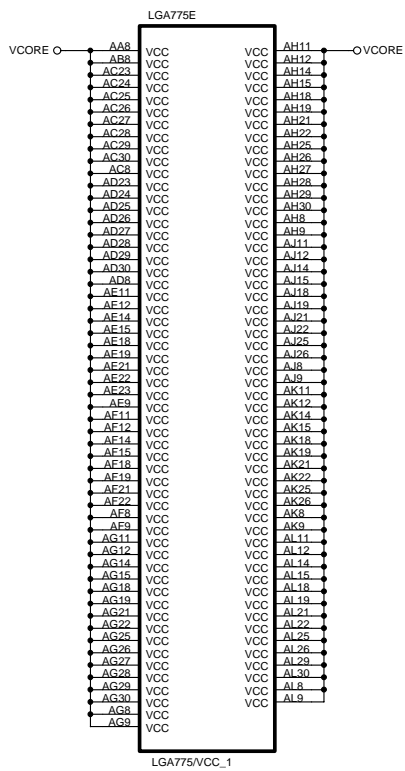


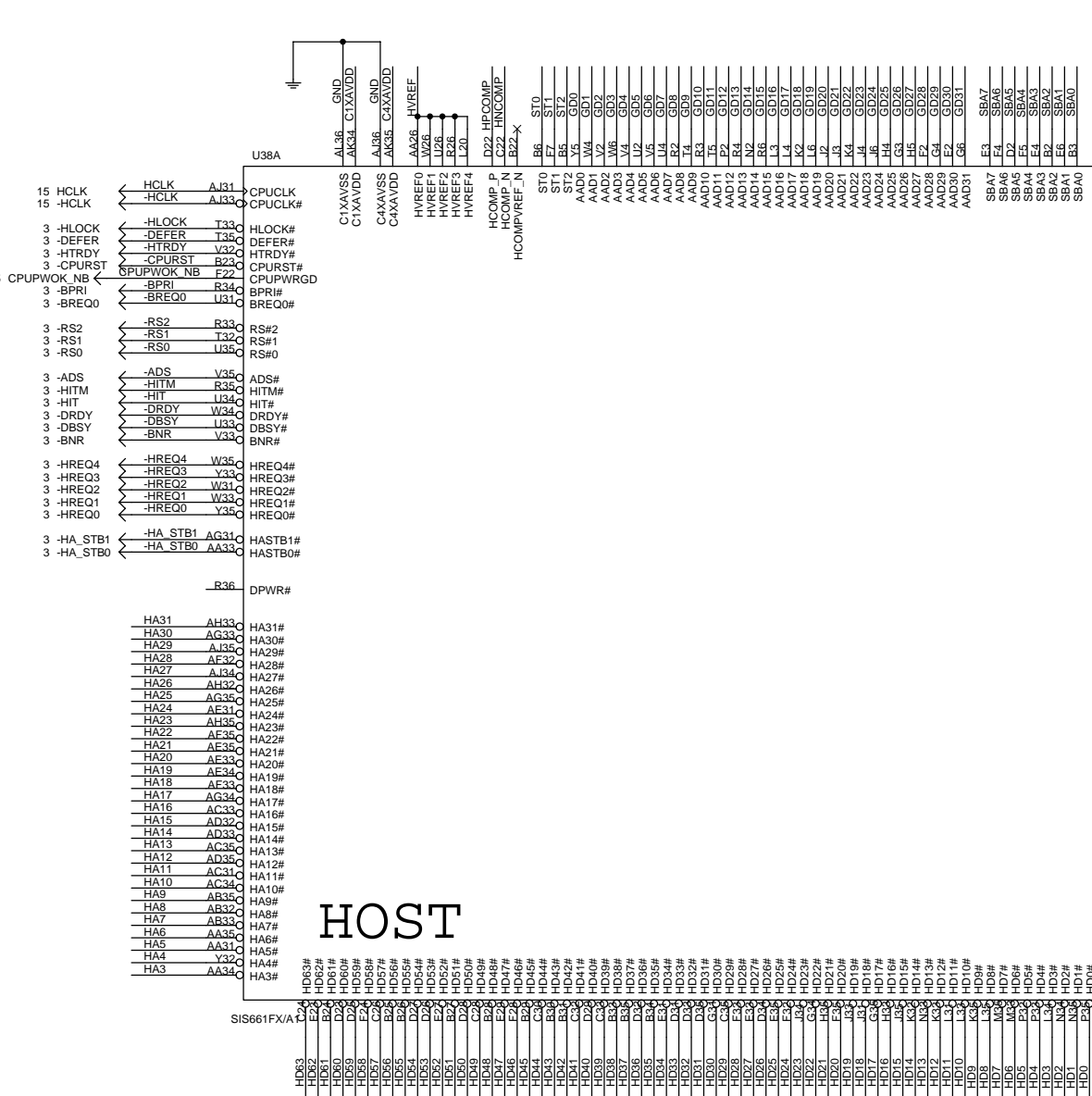


**Note:**  
VCCA & VCOREPLL  
define doesn't same as  
old P4 design kit

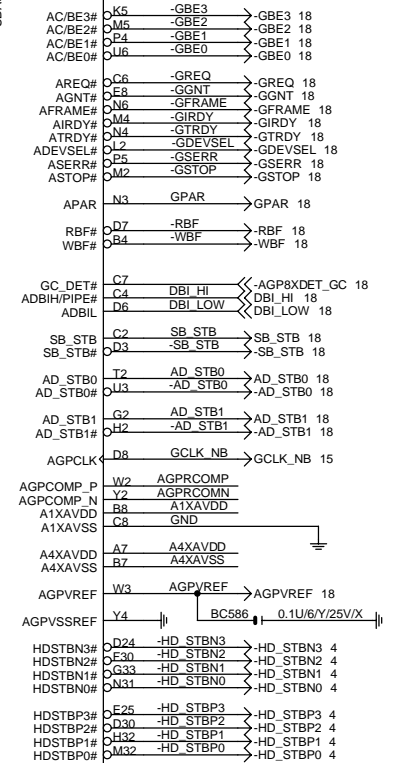
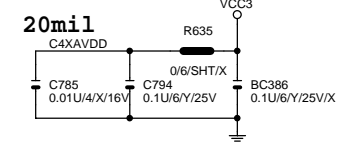
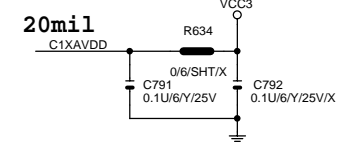
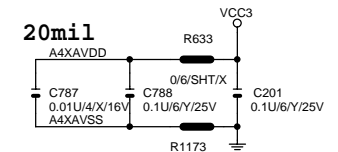
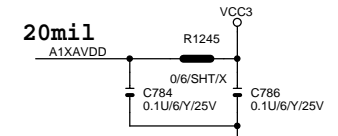
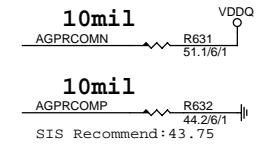
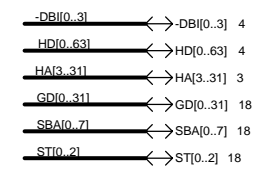
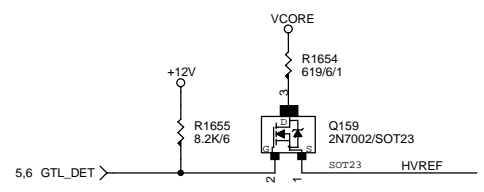
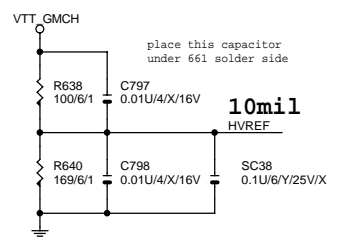
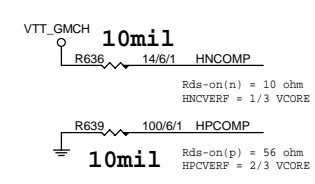


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Size Custom	Document Number <b>GIGABYTE</b>	Rev <b>1.0</b>
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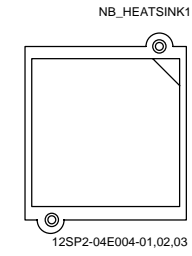




HOST

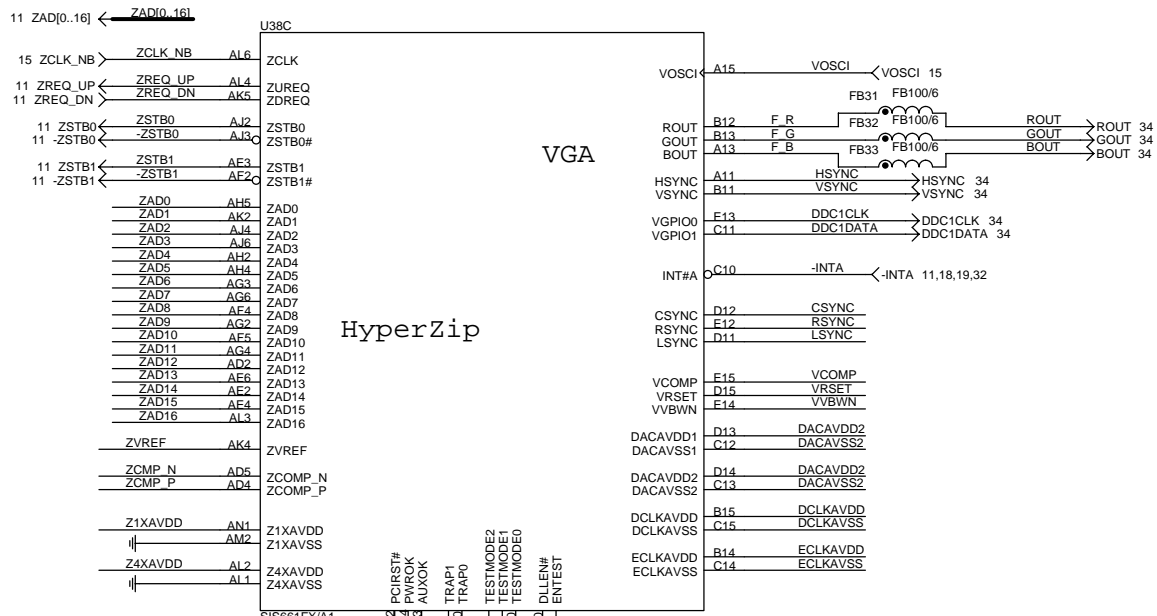


N.B HEATSINK



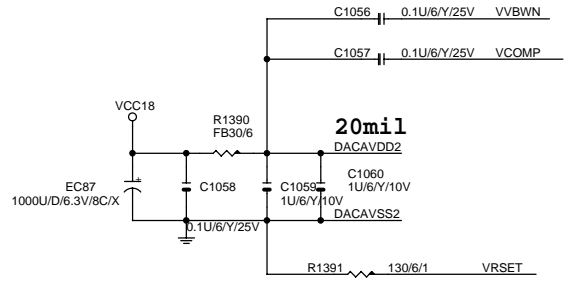
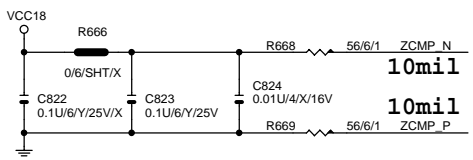
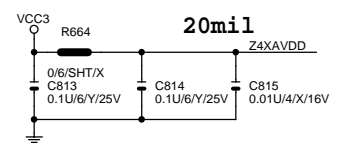
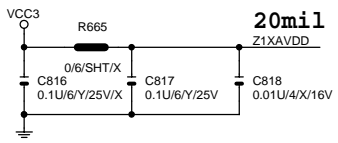
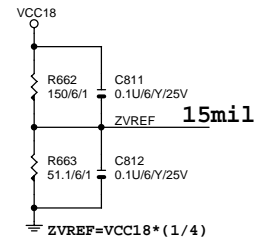
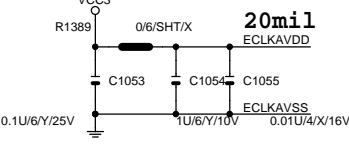
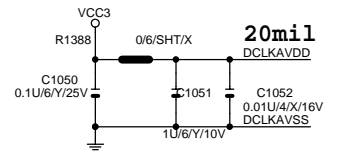
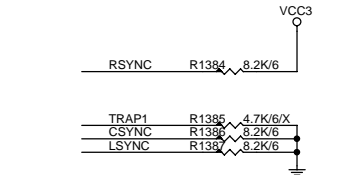
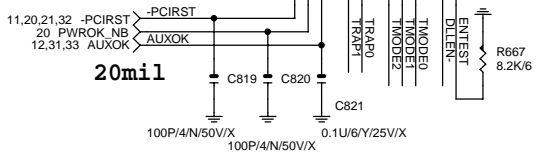
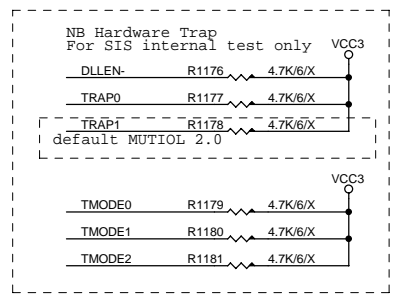
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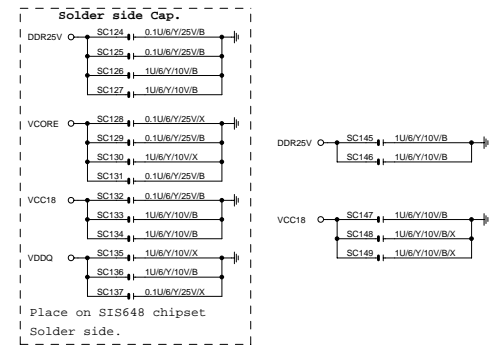
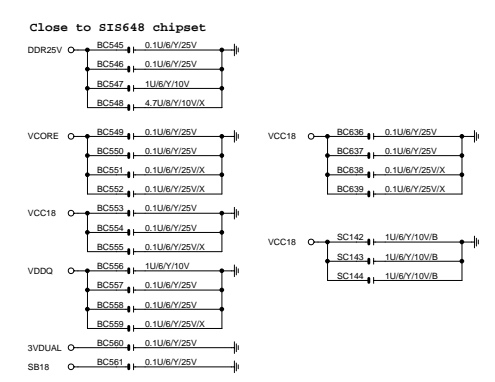
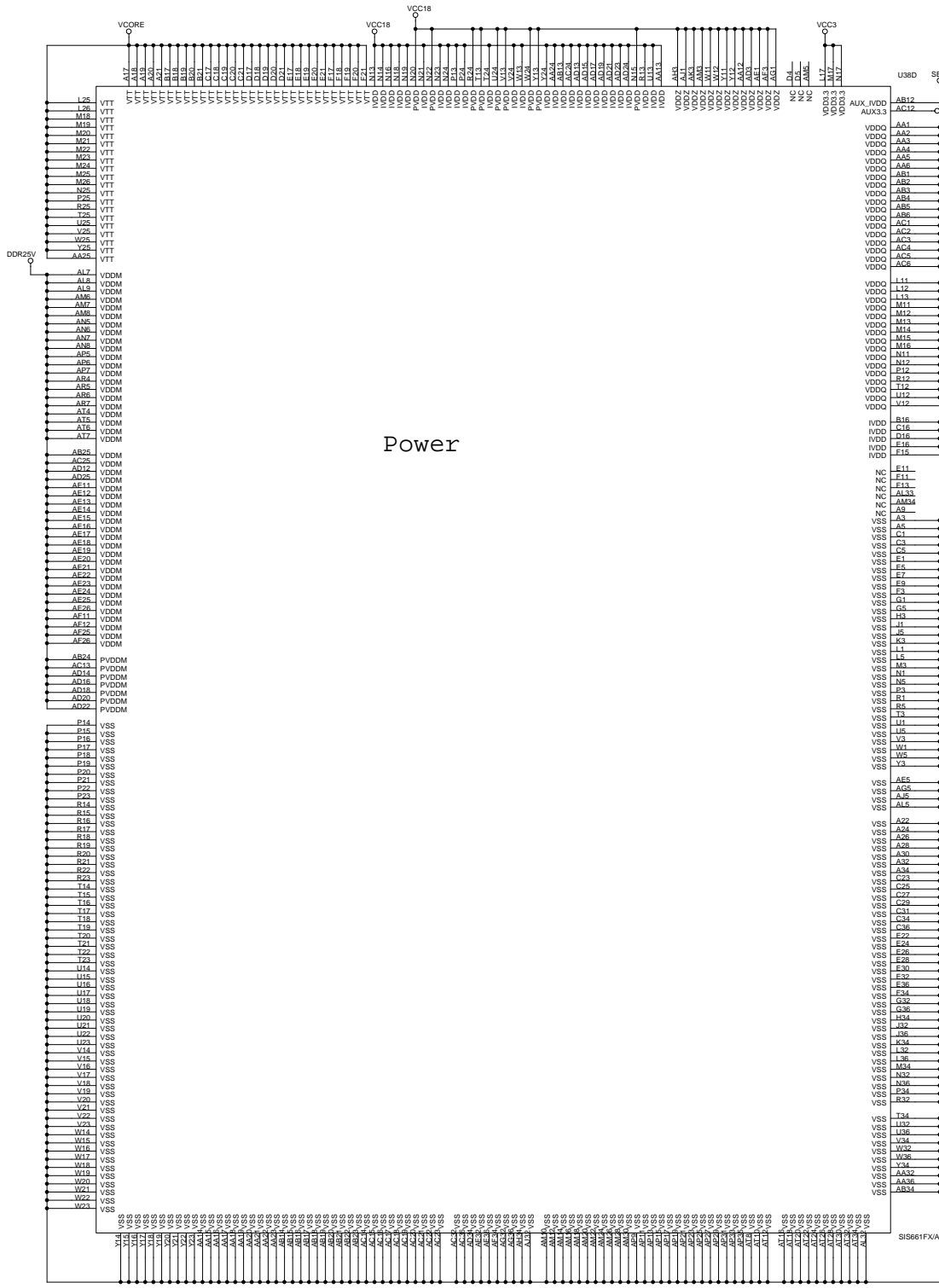


For debug mode

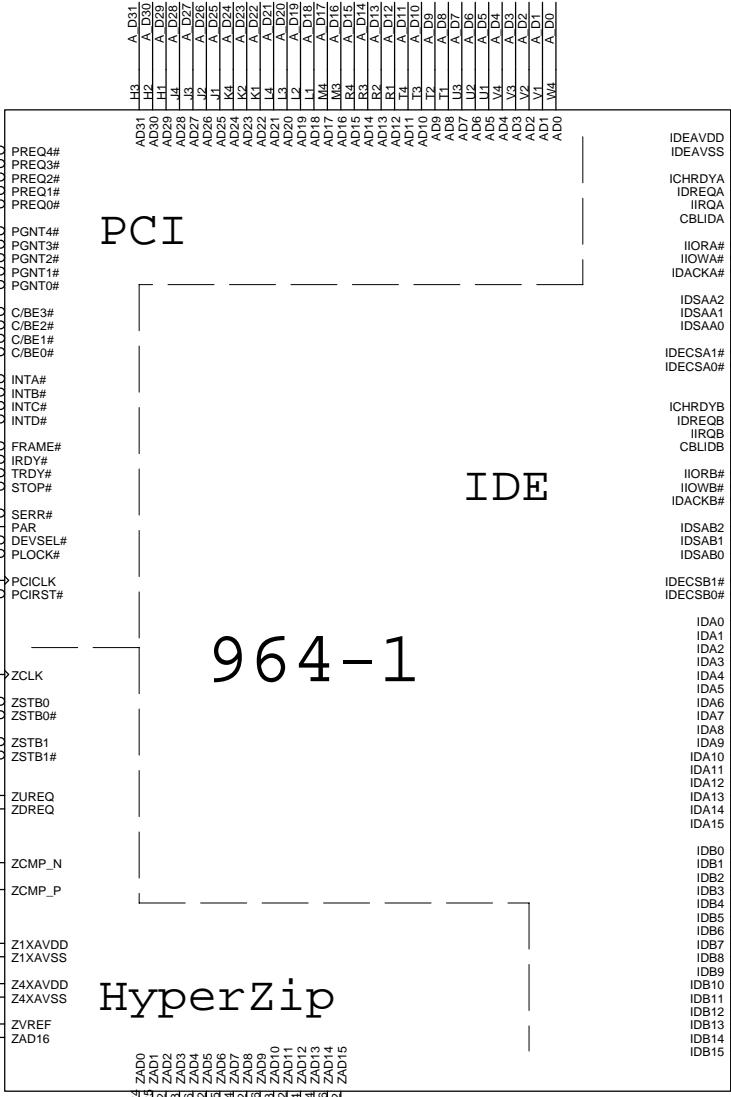
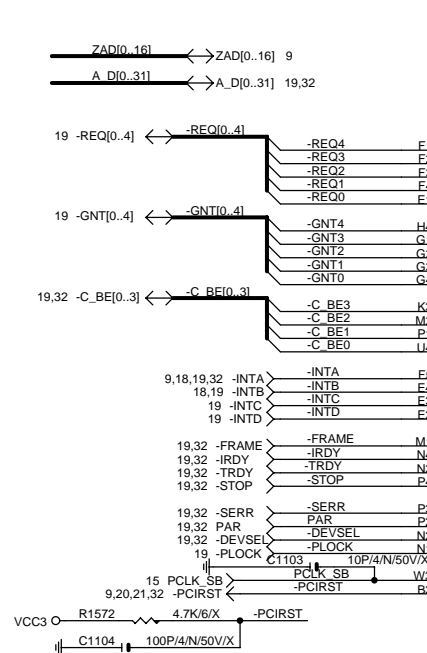
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TMODE1	
TMODE2	
TRAP1	
DLLEN	



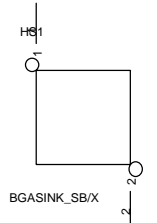
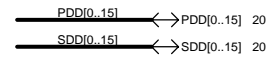
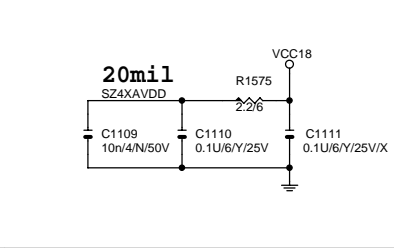
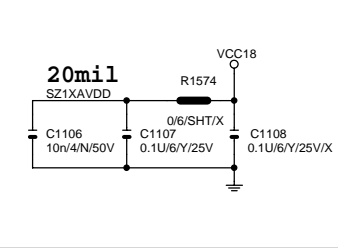
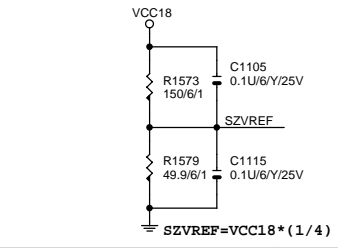
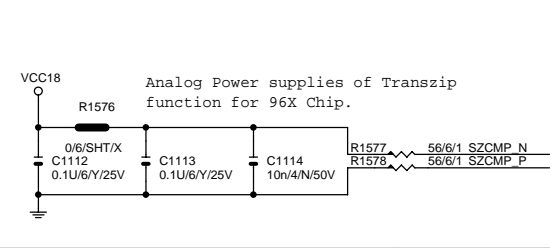
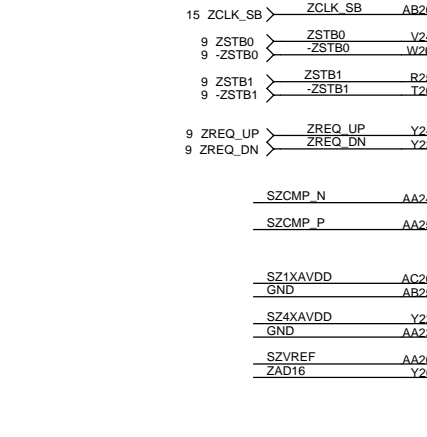
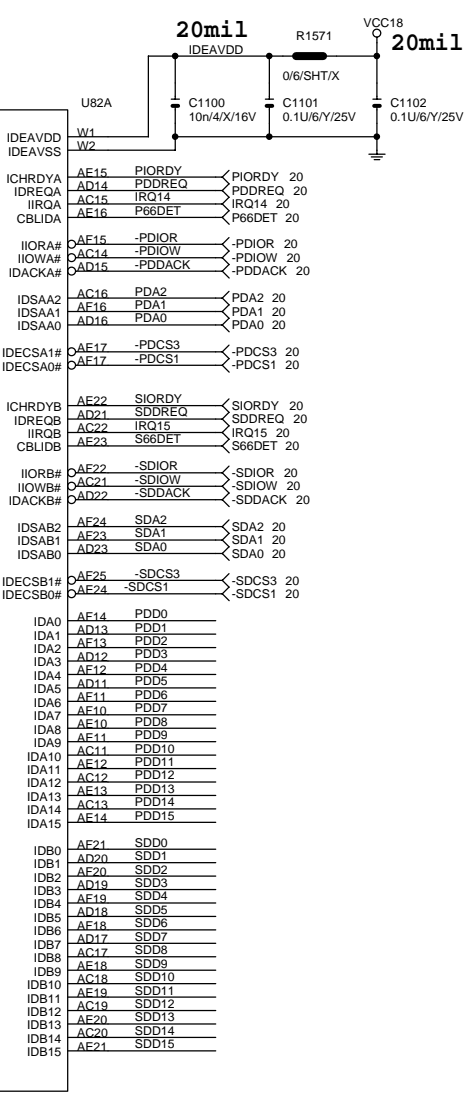
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Size Custom	Document Number <b>GIGABYTE</b>	Rev <b>1.0</b>
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Size	Document Number	Rev.
Customer	<b>GIGABYTE</b>	
Date	日期 - 五月 06, 2004	Sheet 10 of 34
		<b>1.0</b>

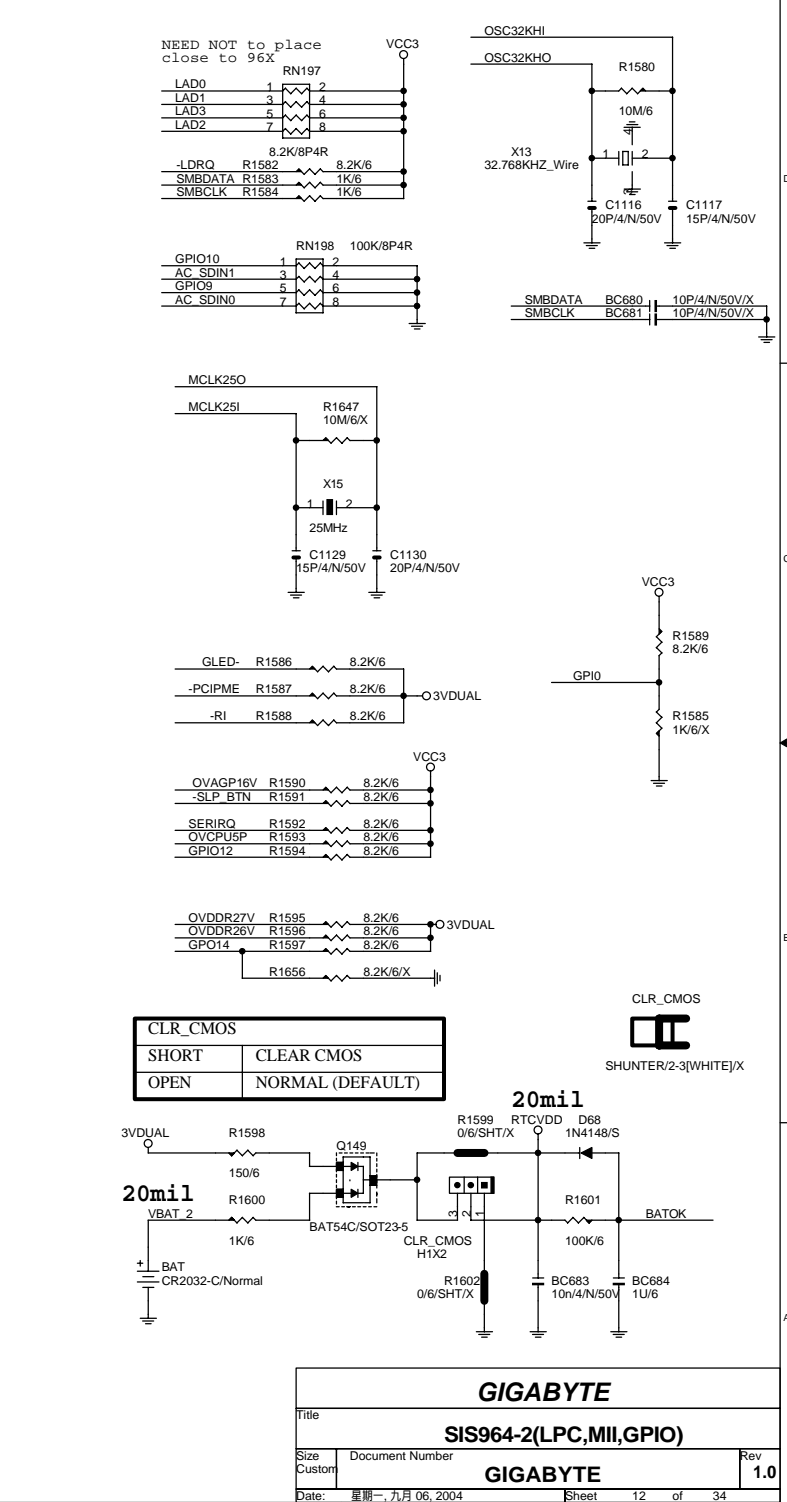
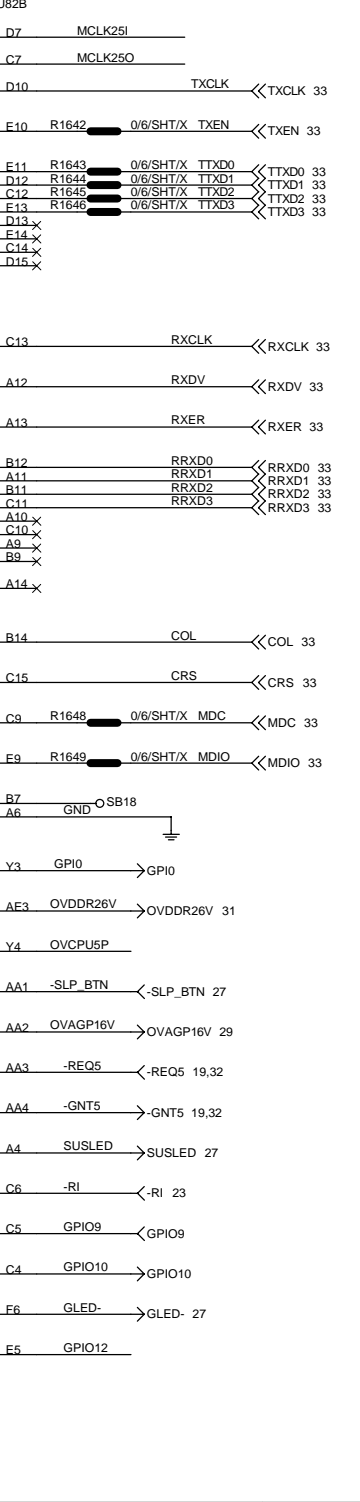
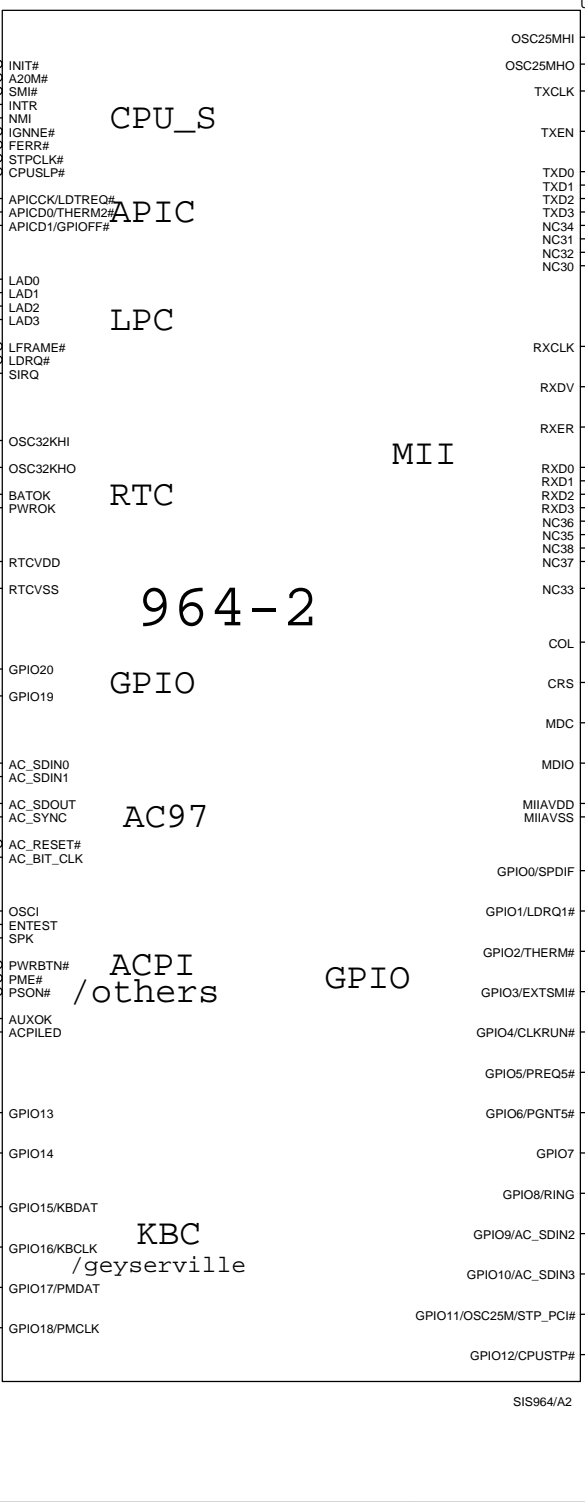
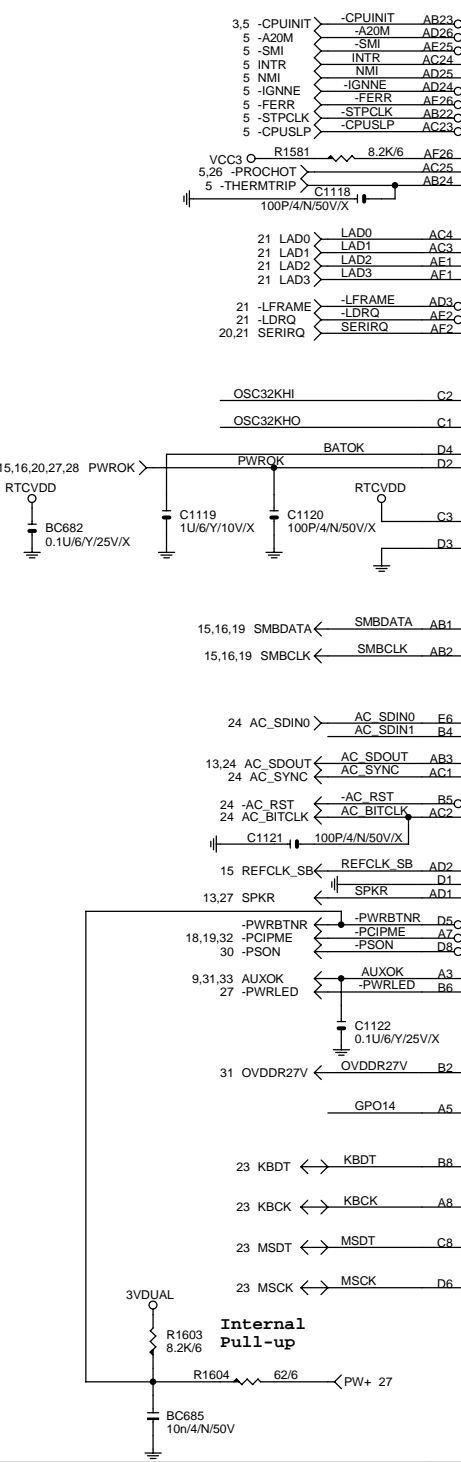


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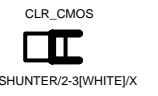


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Size Custom	Document Number <b>GIGABYTE</b>	Rev <b>1.0</b>
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Programmable on-die pull-high strength for CPU\_S:  
 (\* Infinite, 150, 110, 56 Ohm)

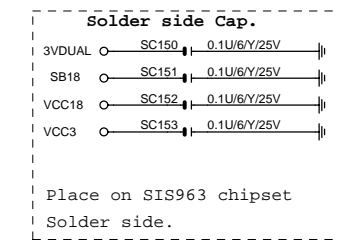
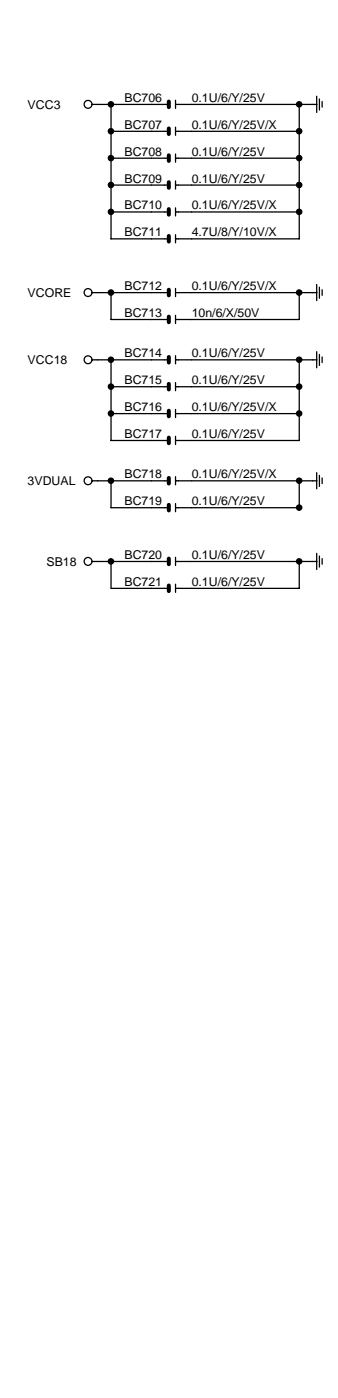
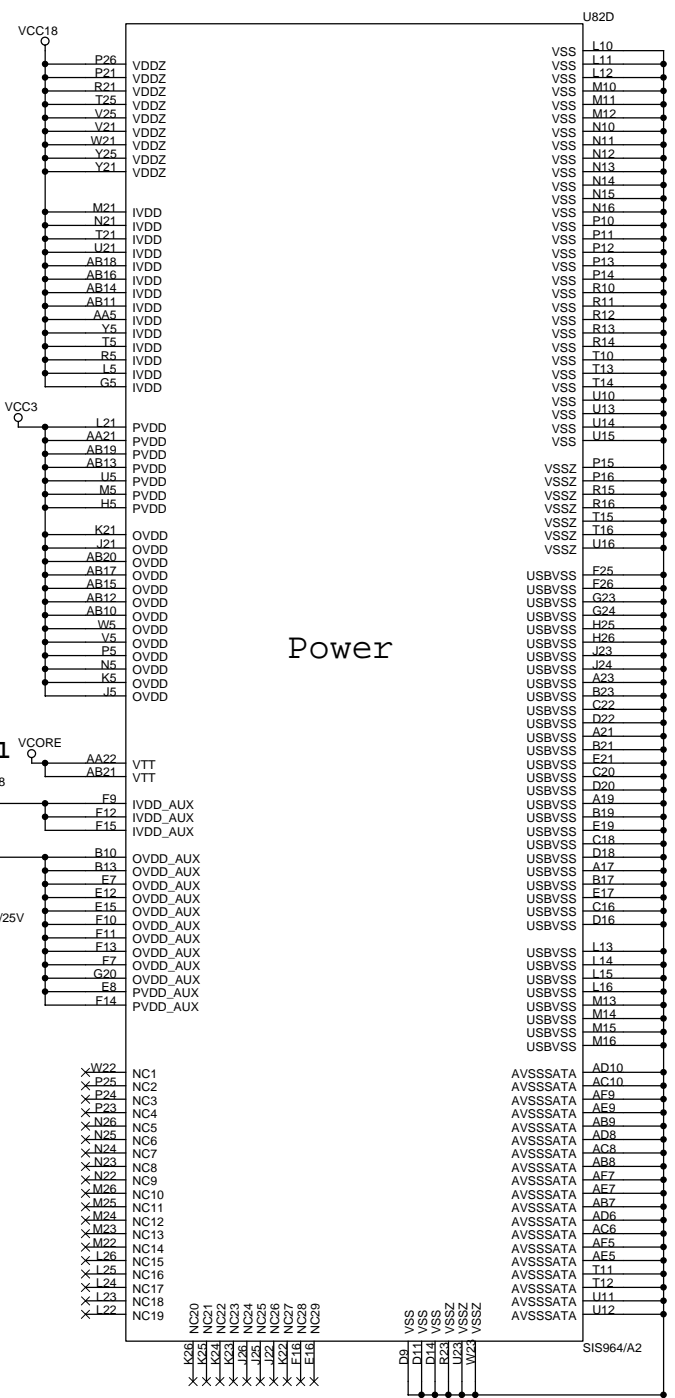


CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL (DEFAULT)



<b>GIGABYTE</b>		
SIS964-2(LPC,MII,GPIO)		
Title	Document Number	Rev
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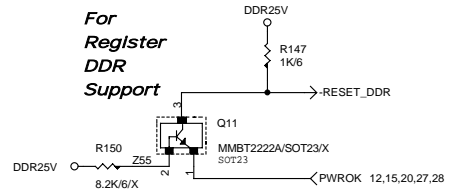
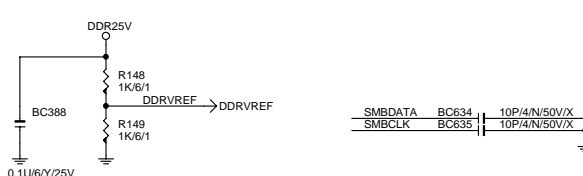
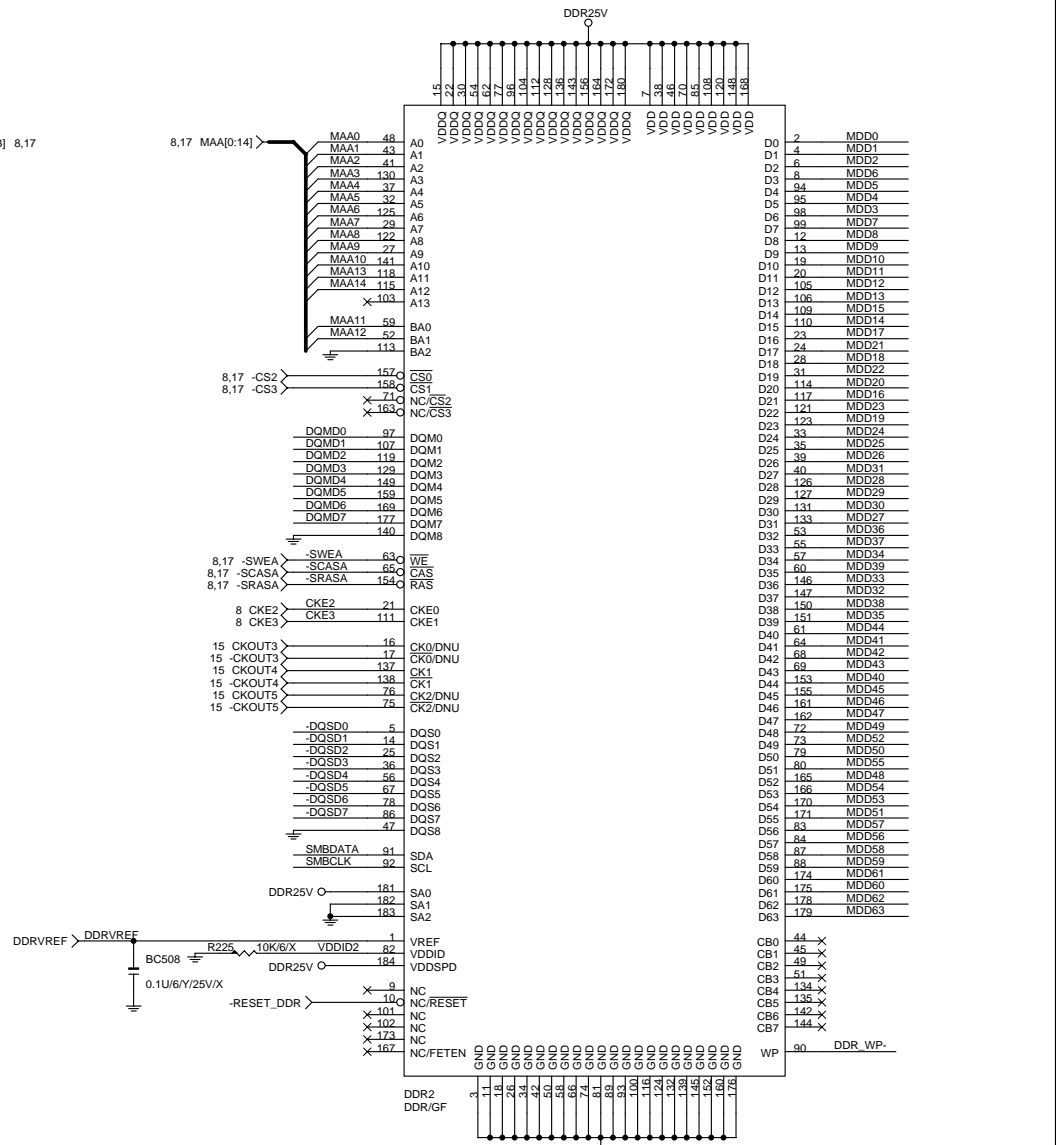
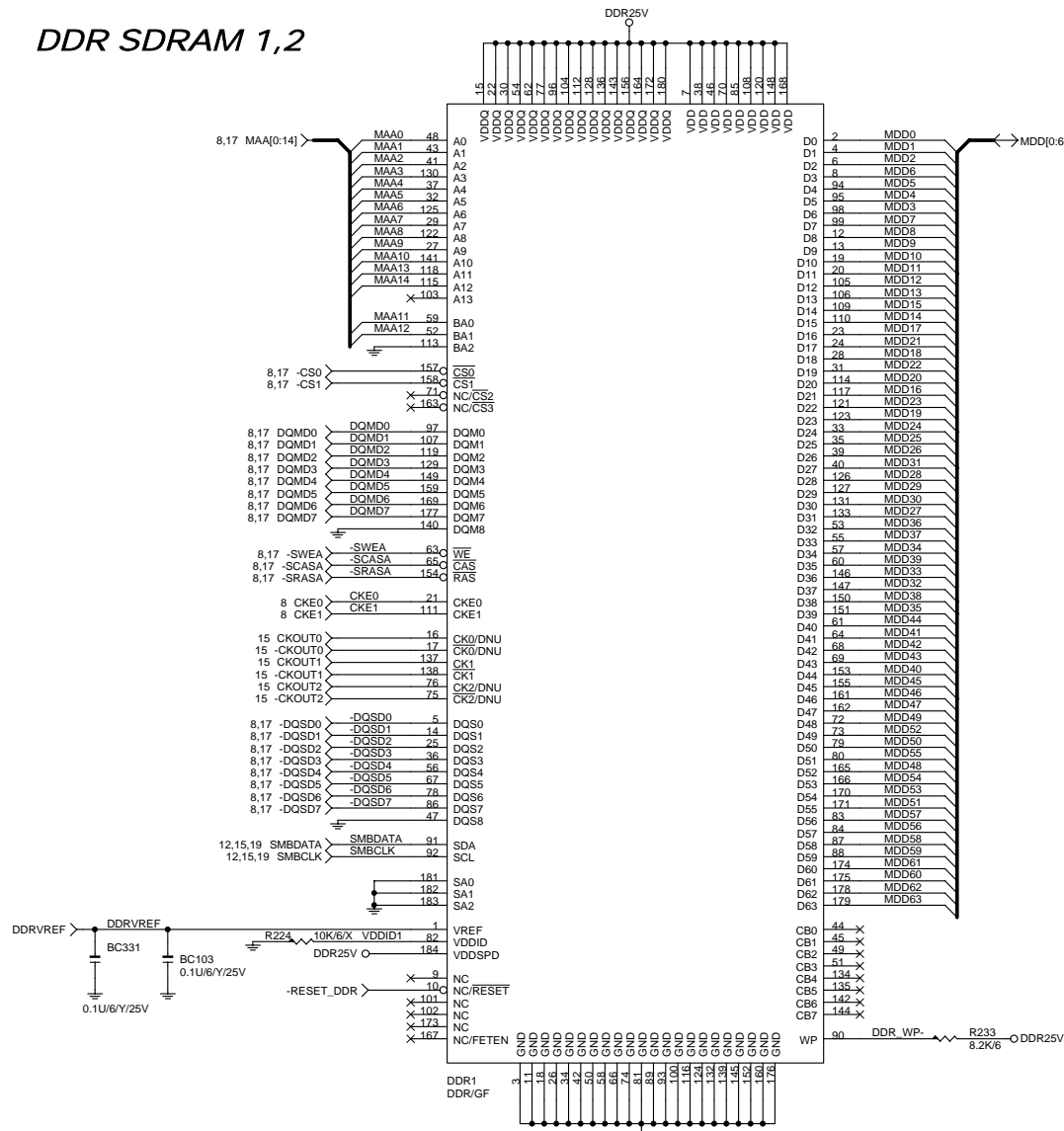




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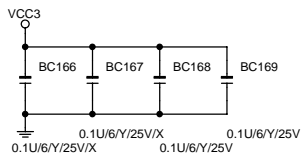
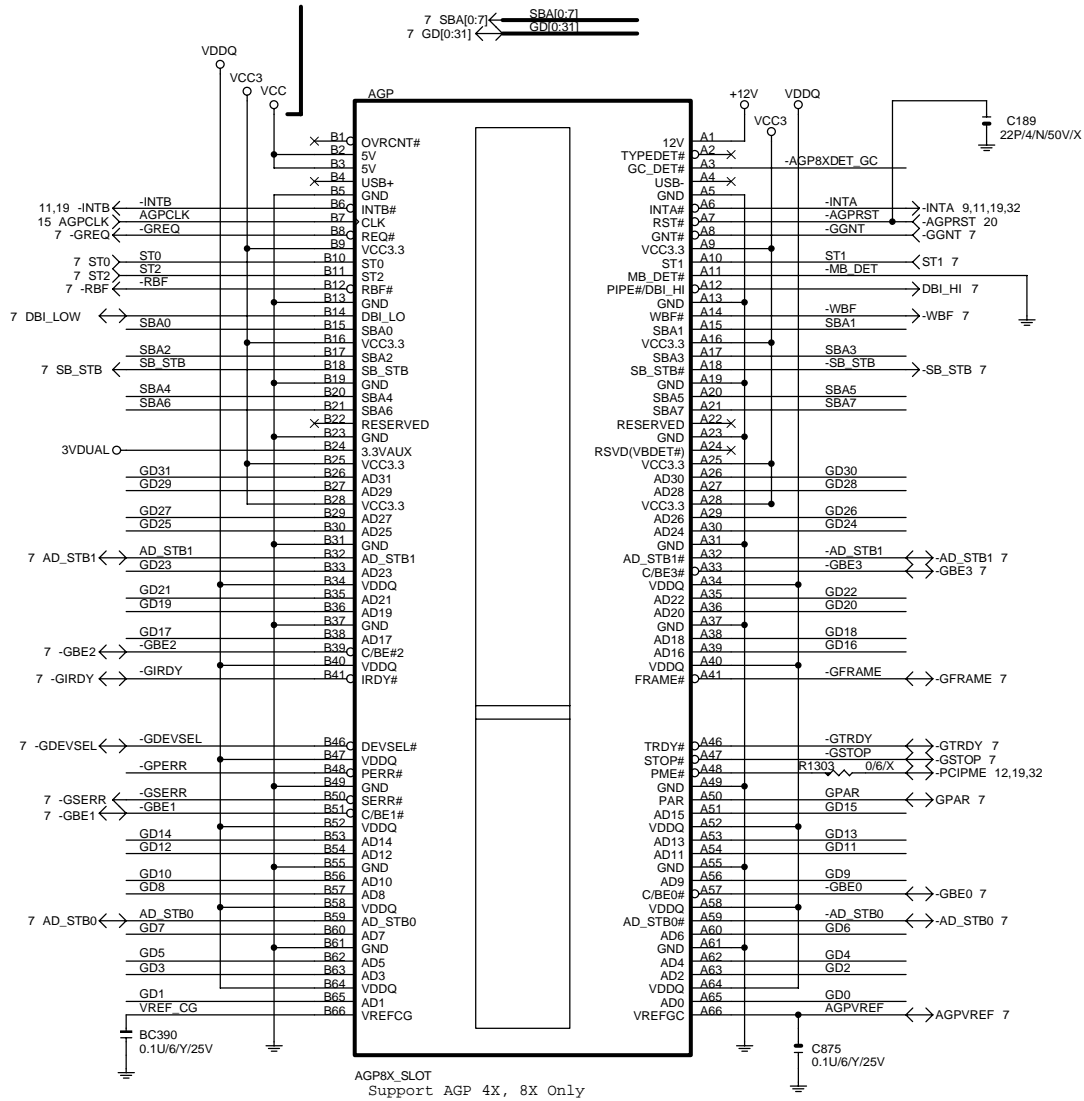
# DDR SDRAM 1,2



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<b>DDR UNBUFFERED 1,2</b>		
Size Custom	Document Number	Rev <b>1.0</b>
<b>GIGABYTE</b>		
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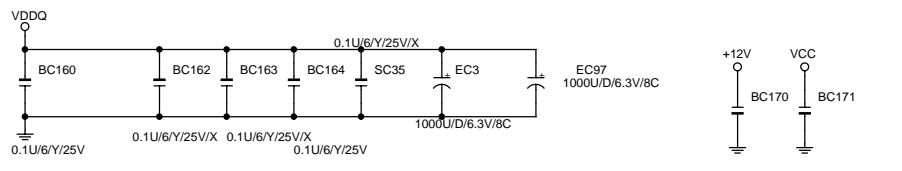


VCC : 80 mil



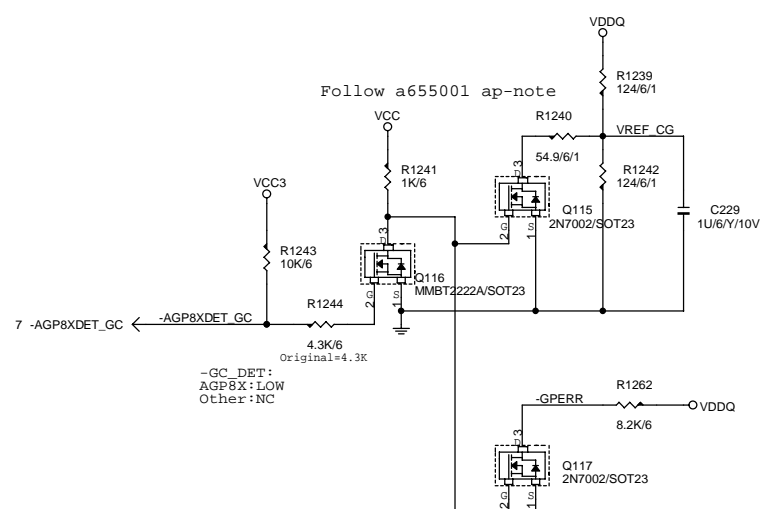
Place 1 at each pair of 3.3V pins

Decoupling capacitors  
(Place near AGP slot)



Place 1 at each pair of VDDQ pins

Place an additional for spread from A14 - A33

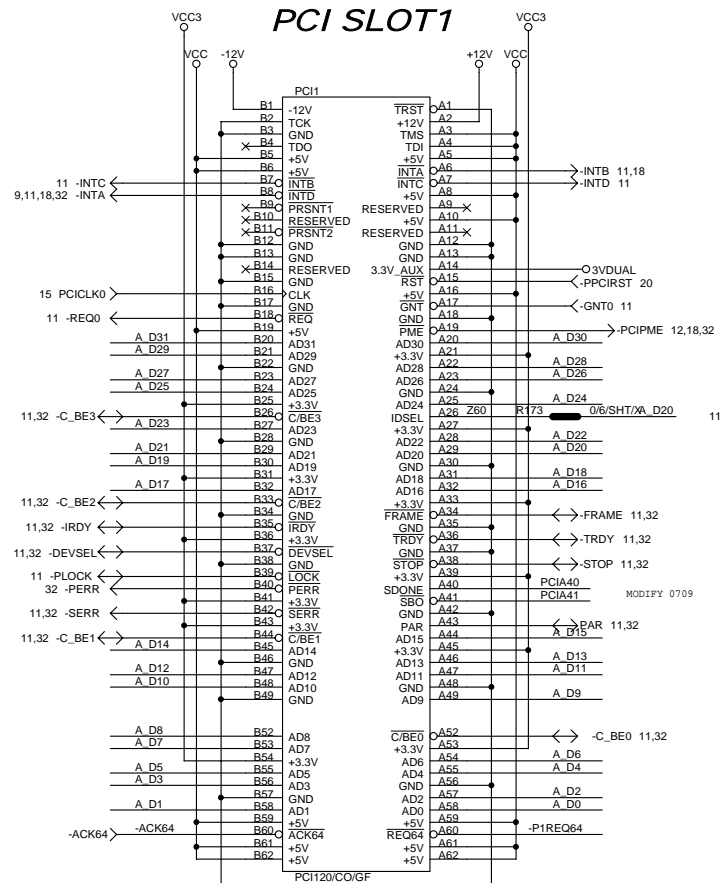


<b>GIGABYTE</b>		
<b>AGP SLOT</b>		
Size Custom	Document Number	Rev
<b>GIGABYTE</b>		<b>1.0</b>
Date:	星期一, 九月 06, 2004	Sheet 18 of 34

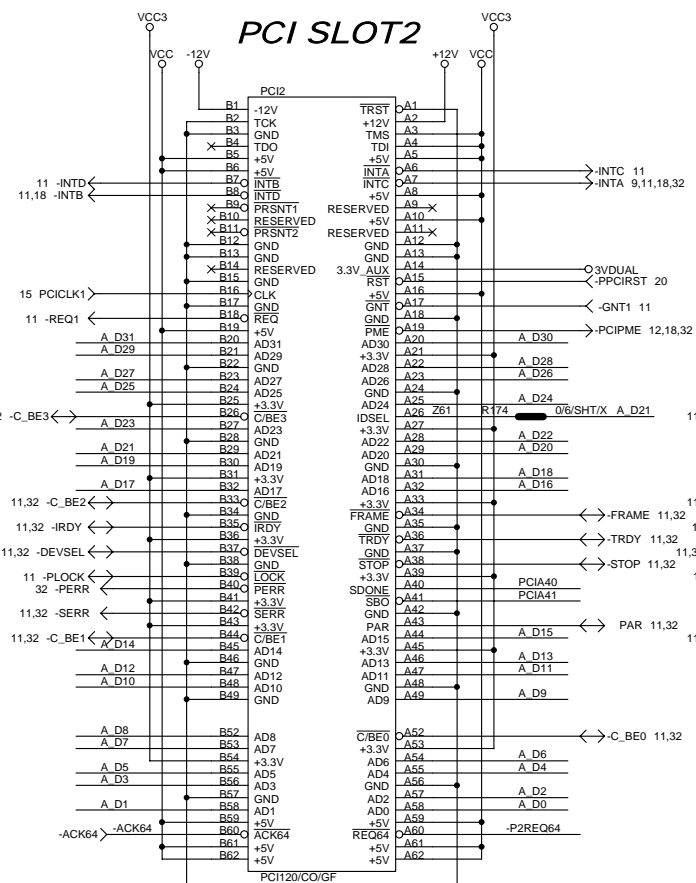
PCI SLOT1

PCI SLOT2

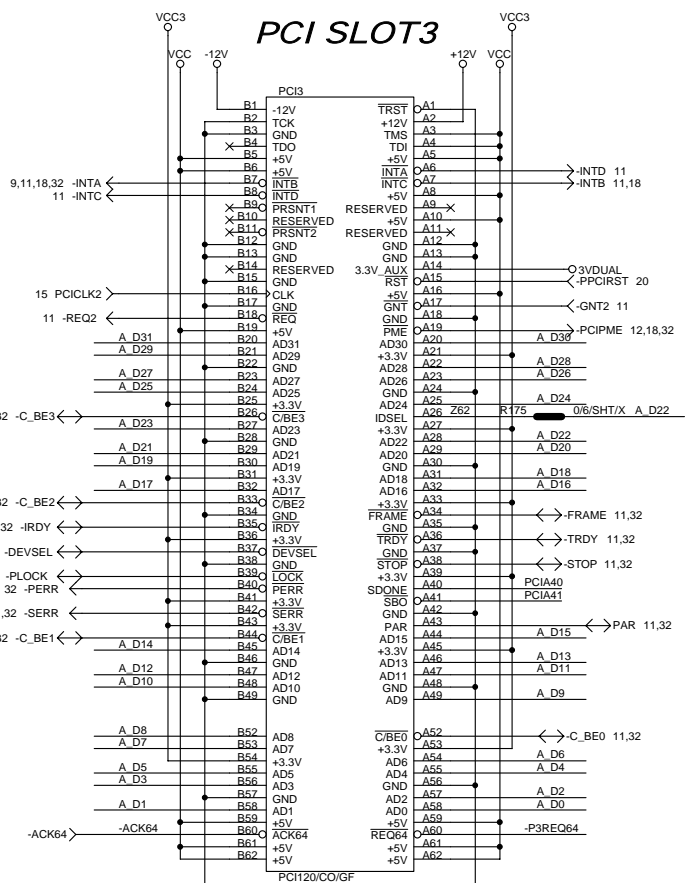
PCI SLOT3



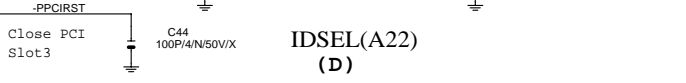
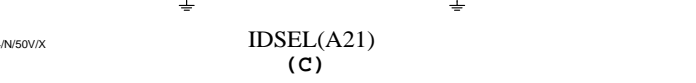
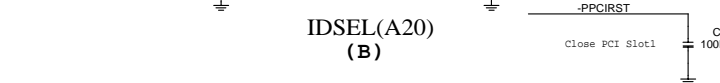
IDSEL(A20)  
(B)



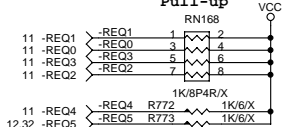
IDSEL(A21)  
(C)



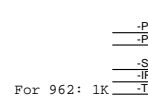
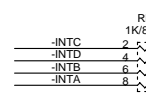
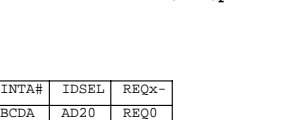
IDSEL(A22)  
(D)



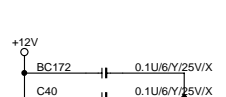
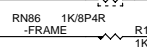
Internal Pull-up



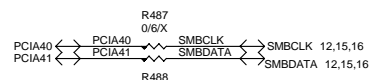
Internal Pull-up



For 962: 1K Pull-up



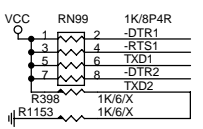
	INTA#	IDSEL	REQx-
PCI1	BCDA	AD20	REQ0
PCI2	CDAB	AD21	REQ1
PCI3	DABC	AD22	REQ2
RTL8101	CD	AD26	REQ5



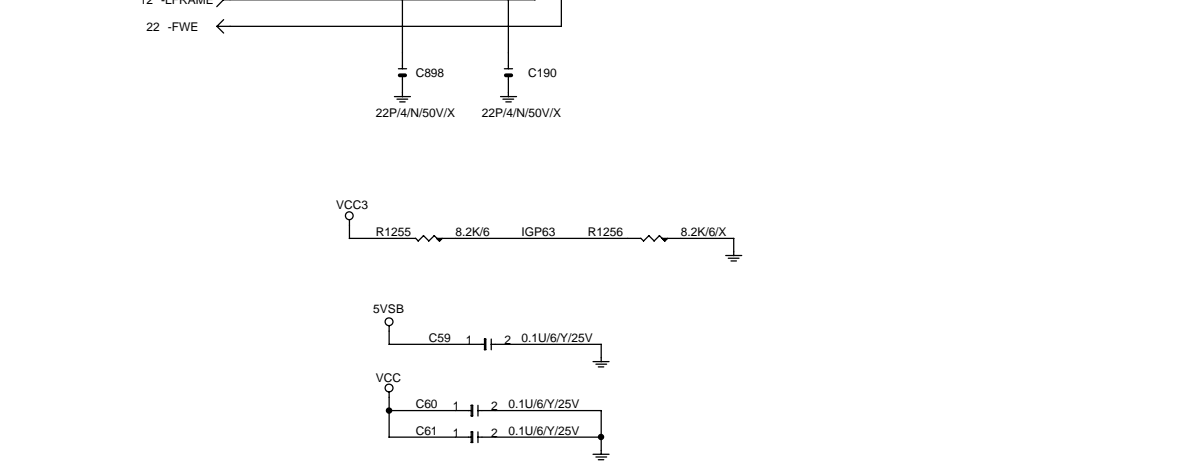
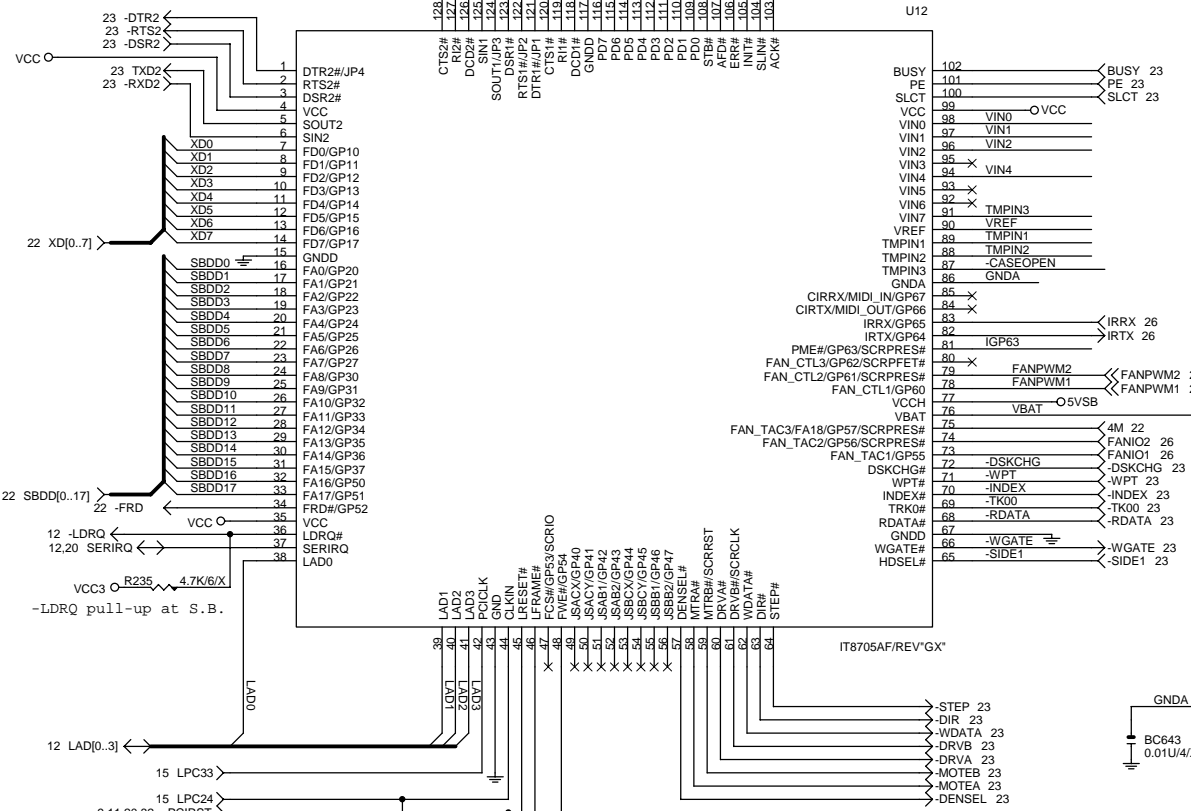
GIGABYTE  
PCI SLOT 1,2,3

Title	Document Number	Rev
	GIGABYTE	1.0
Date:	星期一, 九月 06, 2004	Sheet 19 of 34

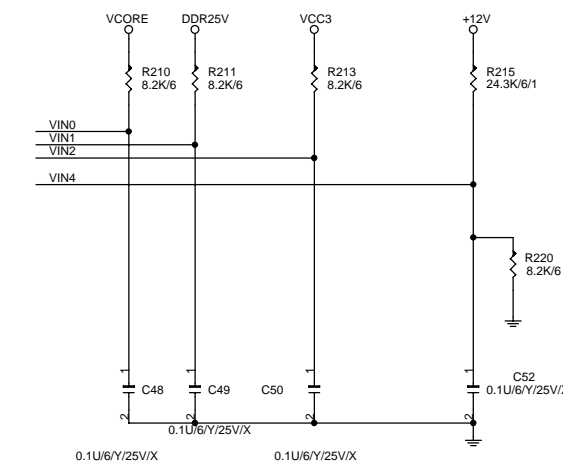




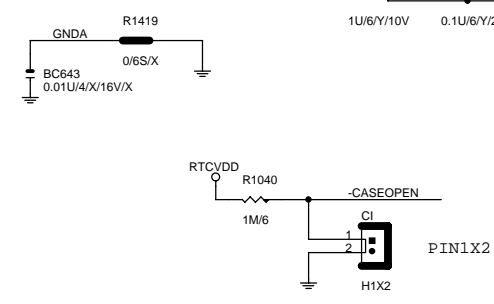
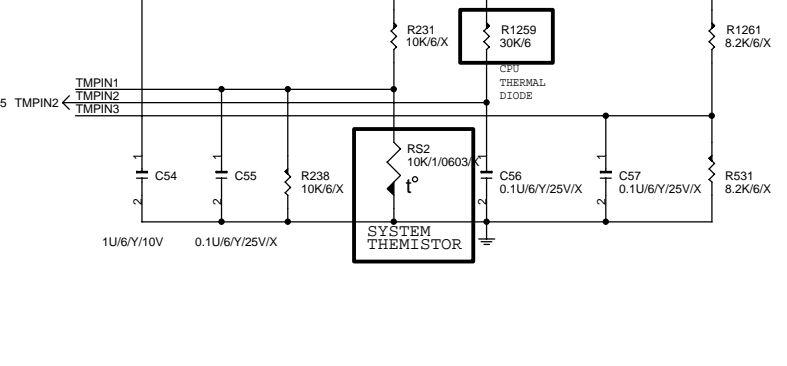
Flash Rom Strapping  
TXD2 only for 4Mb Flash



Voltage Sensing



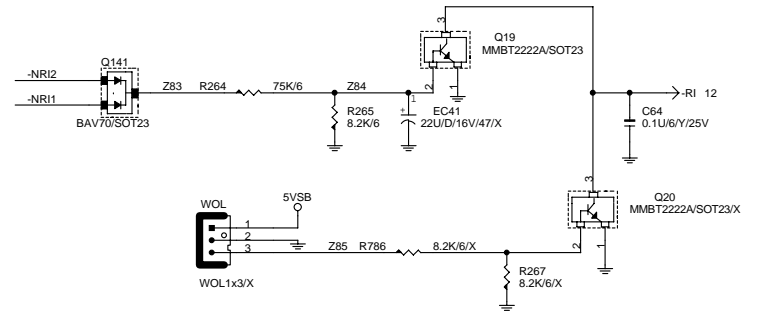
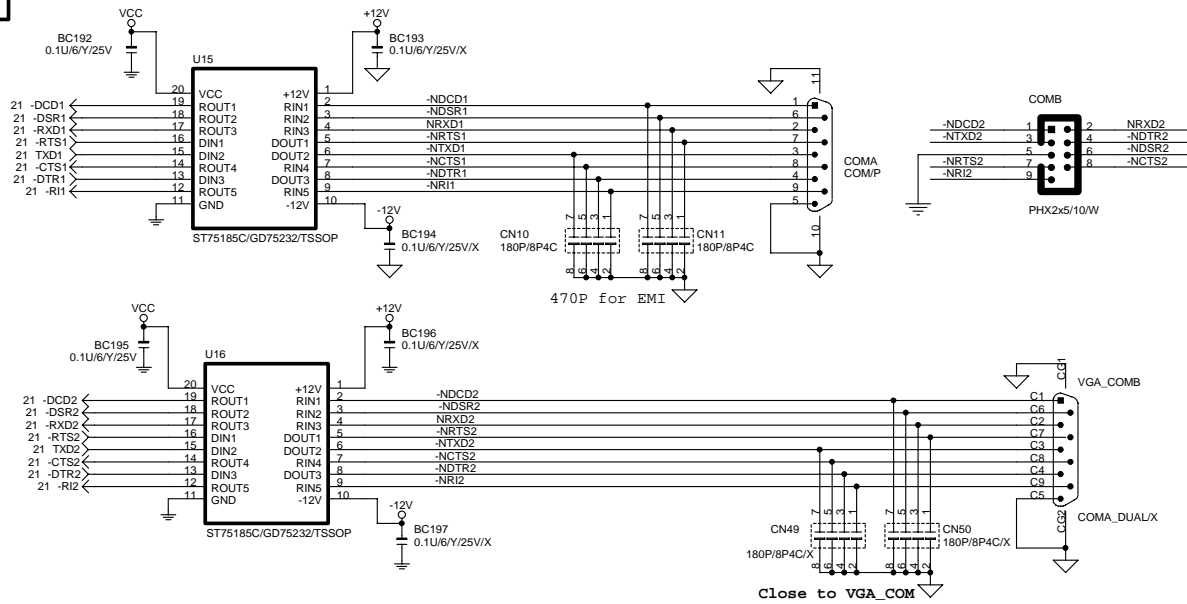
Temperature Sensing



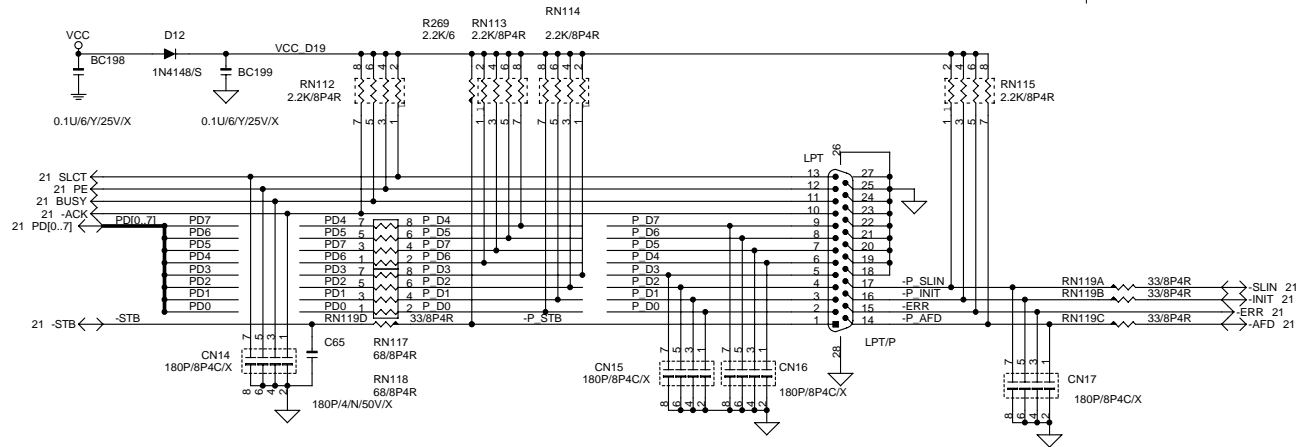
<b>GIGABYTE</b>		
<b>LPC I/O IT8705</b>		
Title	Document Number	Rev
	<b>GIGABYTE</b>	<b>1.0</b>
Date: 星期一, 九月 06, 2004	Sheet 21	of 34



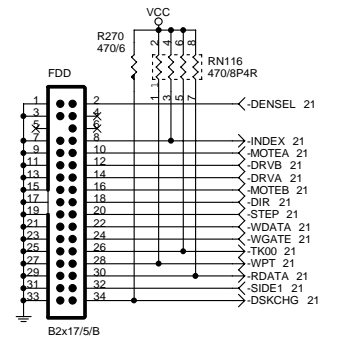
**COM A, B**



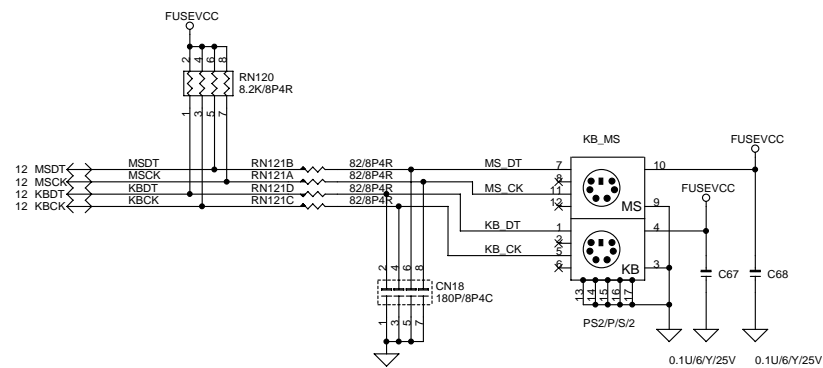
**LPT**



**FDD**



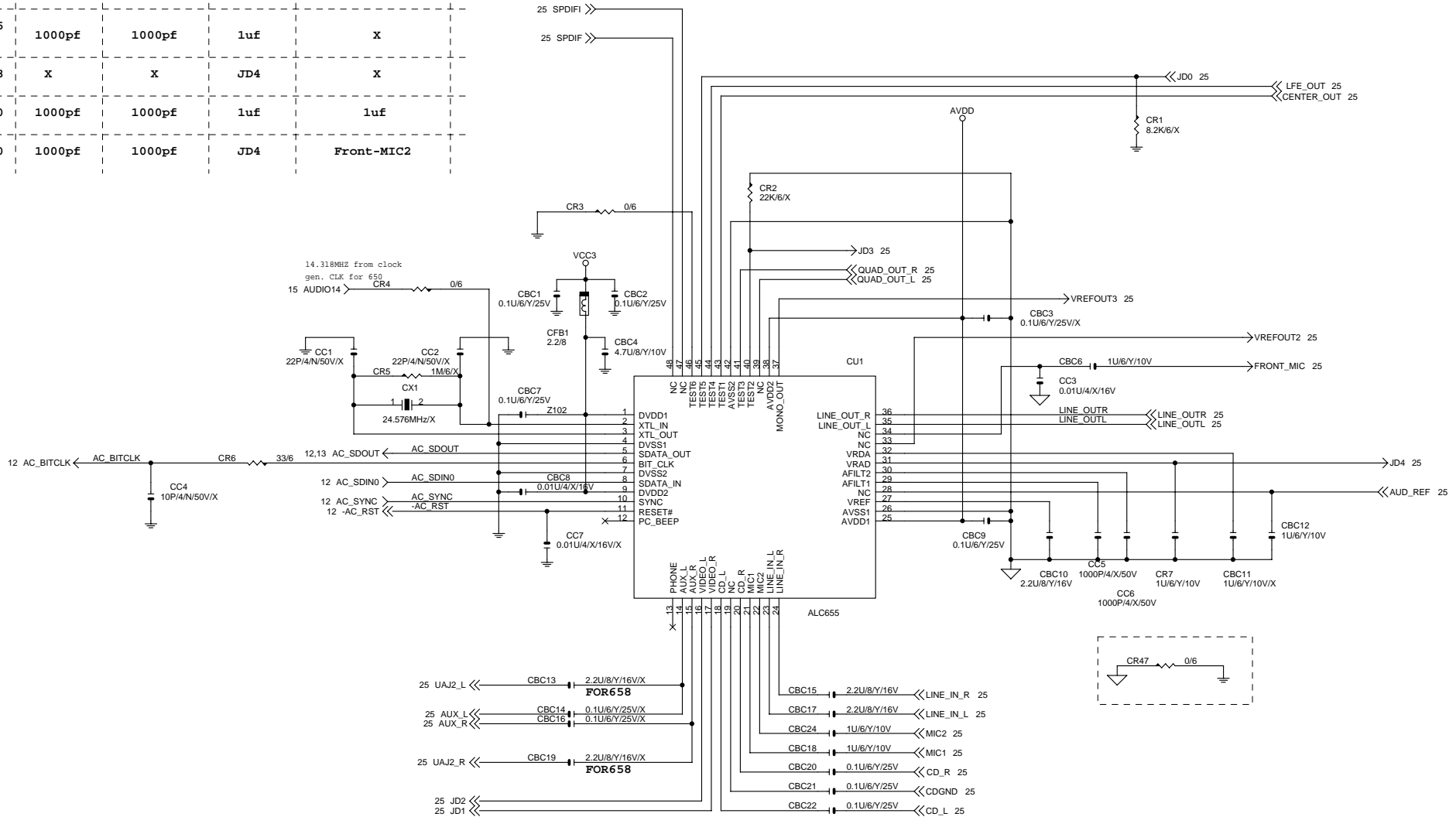
**KBC/PS2**



<b>GIGABYTE</b>		
Title <b>COM,PRT,FDD,KB,IR</b>		
Size Custom	Document Number <b>GIGABYTE</b>	Rev <b>1.0</b>
Date: 星期二, 九月 06, 2004	Sheet 23	of 34

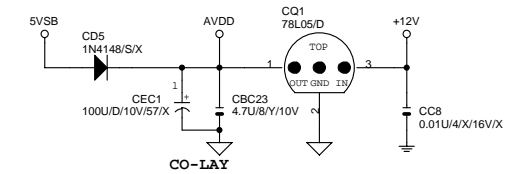
# Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2



## Arrangement of Jack detection Pin:

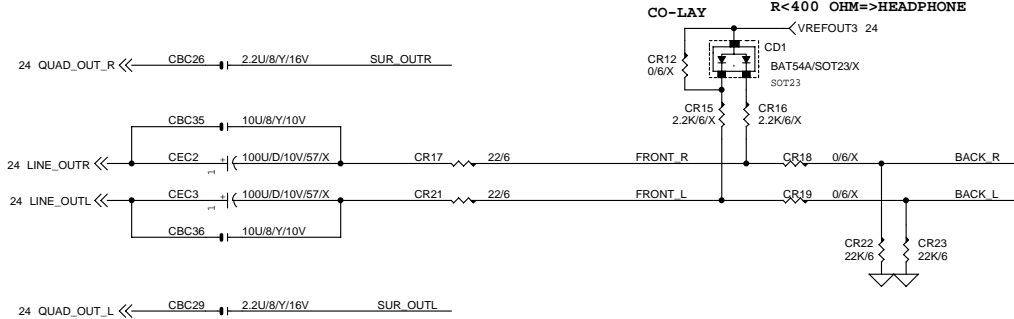
	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT	for LINE-IN	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT External pull high is needed	for LINE-IN External pull high is needed	for SurrBack Out



GIGABYTE			
Title			
<b>ALC655/658/850</b>			
Size	Document Number	Rev	
Custom	<b>GIGABYTE</b>	<b>1.0</b>	
Date:	星期一, 九月 06, 2004	Sheet	24 of 34

**LINE OUT**

JDO,JD2,GPI00 為偵測DEVICE INPUT 時由LOW TO HIGH Edge trigger(pop manual)



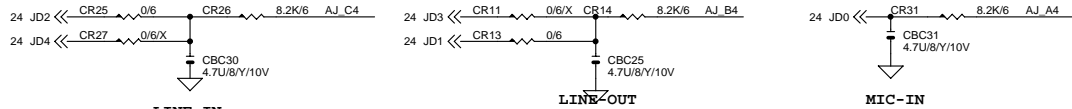
1/2(3.14)RC=1/2(3.14)8.2K\*4.7U=4.3HZ以上AC 信號全部衰減 TO 0V 不會造成JDO 誤動作(無device 時play wav)

**MIC**

**MICROPHONE IN SENSING(當OUTPUT)**  
 R>4K OHM=>POWER SPEAKER  
 4K OHM>R>400 OHM=>MICROPHONE  
 R<400 OHM=>HEADPHONE

**MICROPHONE IN SENSING(當INPUT)(利用vref 偏壓 與CR43,CR32 並聯求出阻抗)**  
 7.1k ohm>R>2.3k ohm==>microphone in  
 R<2.3k ohm or R>7.1k ohm==>unknown device

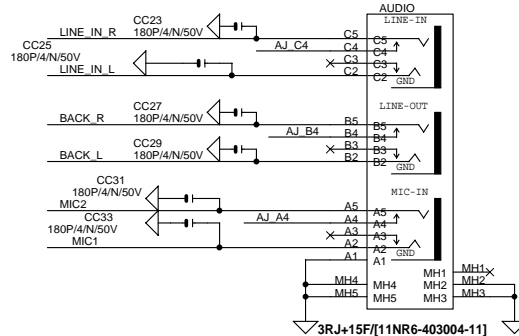
**AC97 JACK**



LINE-IN

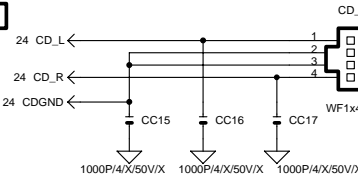
LINE-OUT

MIC-IN

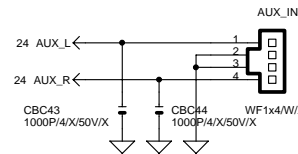


3RJ-15F/[11NR6-403004-11]

**CD IN**



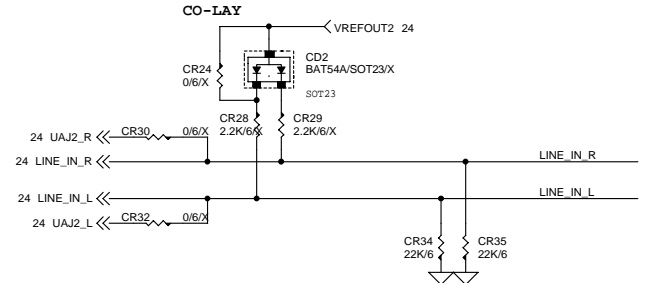
**AUX IN**



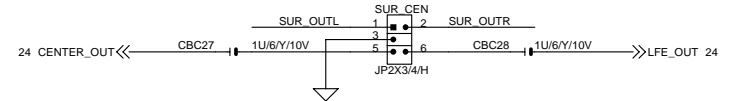
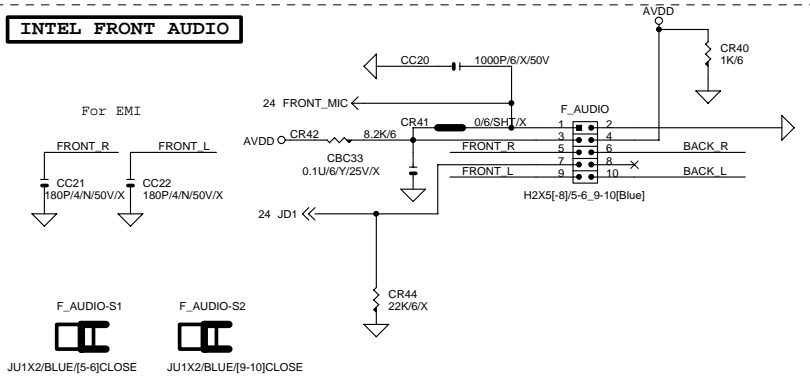
**LINE-IN**

**LINE IN SENSING(當OUTPUT)**  
 R>4K OHM=>POWER SPEAKER  
 4K OHM>R>400 OHM=>MICROPHONE  
 R<400 OHM=>HEADPHONE

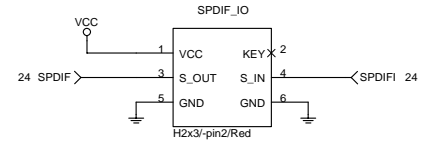
**LINE IN SENSING(當INPUT)**  
 swing of input signal>-40dbv(10mv)==>line in device active  
 swing of input signal<-40dbv(10mv)==>unknown line in device



**INTEL FRONT AUDIO**



**SPDIF/SPDIF\_IN**



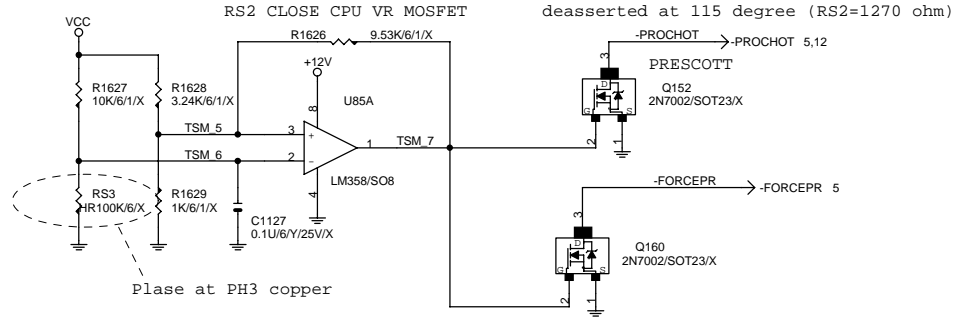
**GIGABYTE**

Title			<b>AUDIO OUTPUT, GAME PORT</b>		
Size	Document Number		Rev		
Custom	<b>GIGABYTE</b>		<b>1.0</b>		
Date:	日期: 九月 06, 2004	Sheet	25	of	34

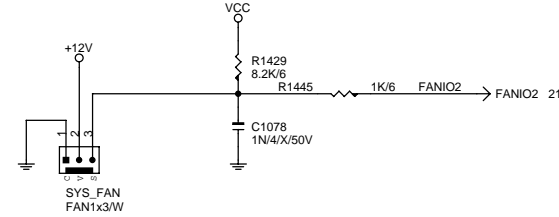
# PROCESSOR HOT

U-ATX PROCESSOR HOT NO POP

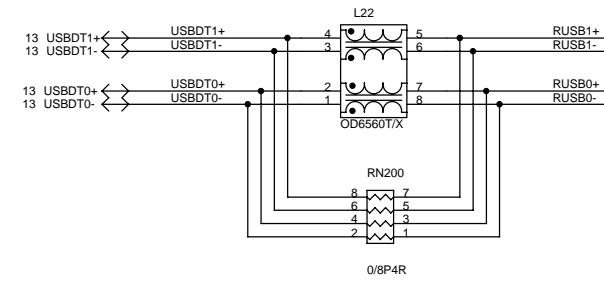
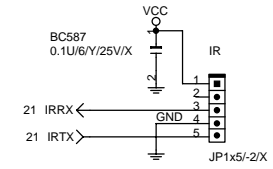
asserted at 130 degree (RS2=720 ohm)  
deasserted at 115 degree (RS2=1270 ohm)



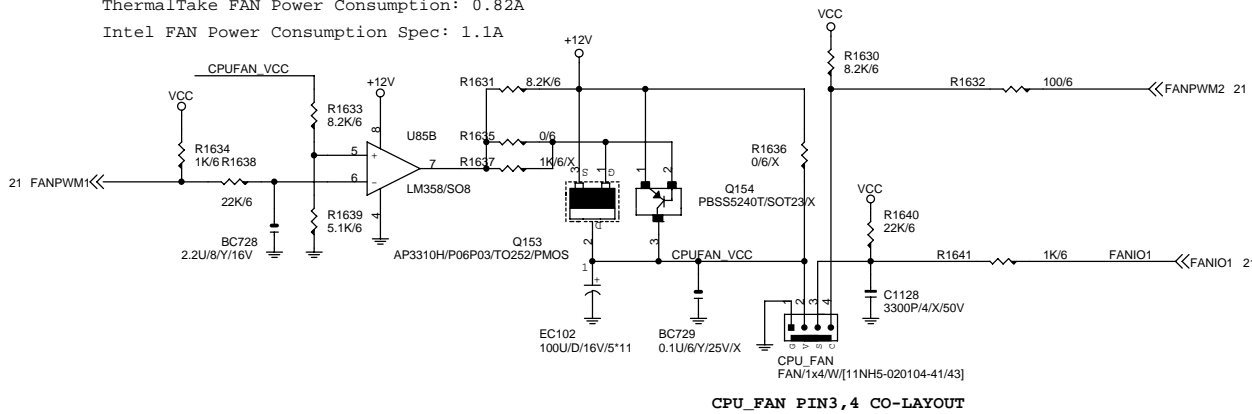
# SYSTEM FAN



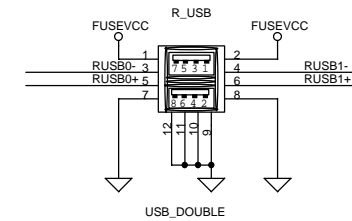
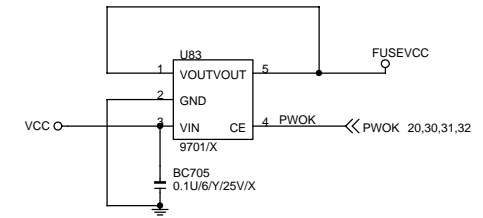
# IR CONNECTOR



ThermalTake FAN Power Consumption: 0.82A  
Intel FAN Power Consumption Spec: 1.1A

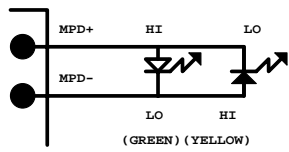


CPU\_FAN PIN3,4 CO-LAYOUT



Title		
GIGABYTE		
FAN, R_USB		
Size	Document Number	Rev
Custom	GIGABYTE	1.0
Date:	星期一, 九月 06, 2004	Sheet 26 of 34

**FRONT PANEL**



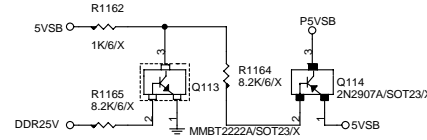
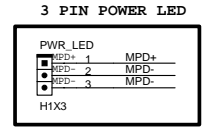
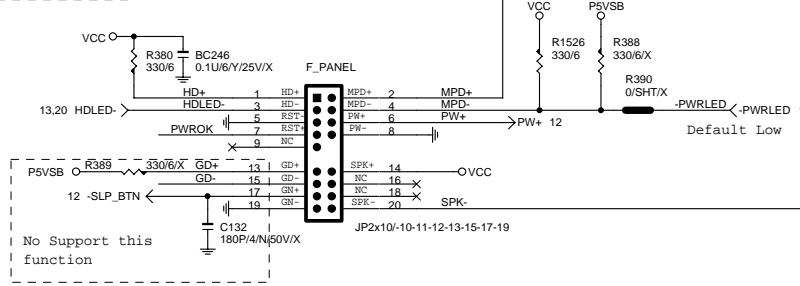
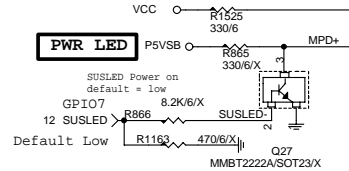
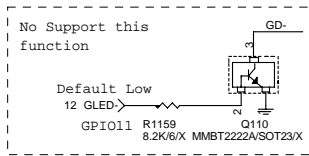
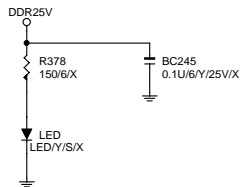
**States for a single-color power LED**

LED States	ACPI States	MPD+	MPD-
OFF	S1,S3,S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING

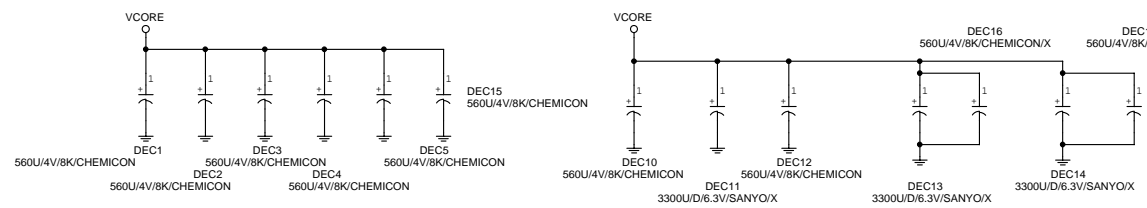
**States for a dual-color power LED**

LED States	ACPI States	MPD+	MPD-
OFF	S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING
Steady Yellow	S1,S3	LO	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING

	S0	S1	S3	S5
GPI011(GLED-)	0	1	1	0
GPI07(SUSLED)	0	B	B	0
ACPILED(Pin A15)	0	0	0	1



PWROK → PWROK 12,15,16,20,28



DD1 : 在HIGH SIDE 發生S-D SHORT 時(OVP), LOW SIDE MOSFET TURN ON, 讓VCORE 降壓, 同時V12 也會下降6-7V以下時, 造成PWM 無法提供POWER TO LOW SIDE TURN ON, 所以加DD1 延長PWM POWER 提供給LOW SIDE MOSFET TURN ON 保護CPU VOLTAGE 過高.

DR9, DC5 FOR V12 OVER 19V 以上, SPEC (18V)

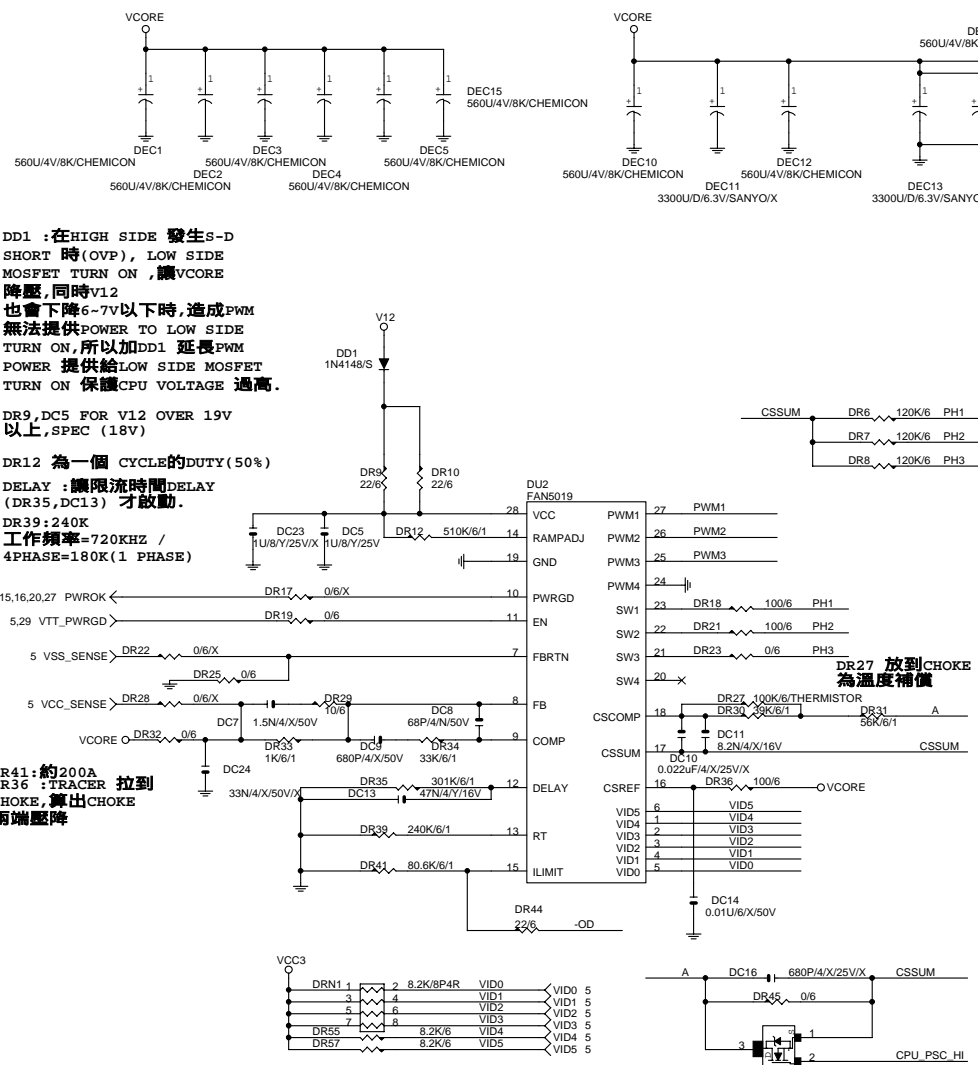
DR12 為一個 CYCLE 的 DUTY (50%) DELAY : 讓限流時間 DELAY (DR35, DC13) 才啟動.

DR39 : 240K 工作頻率 = 720KHZ / 4PHASE = 180K (1 PHASE)

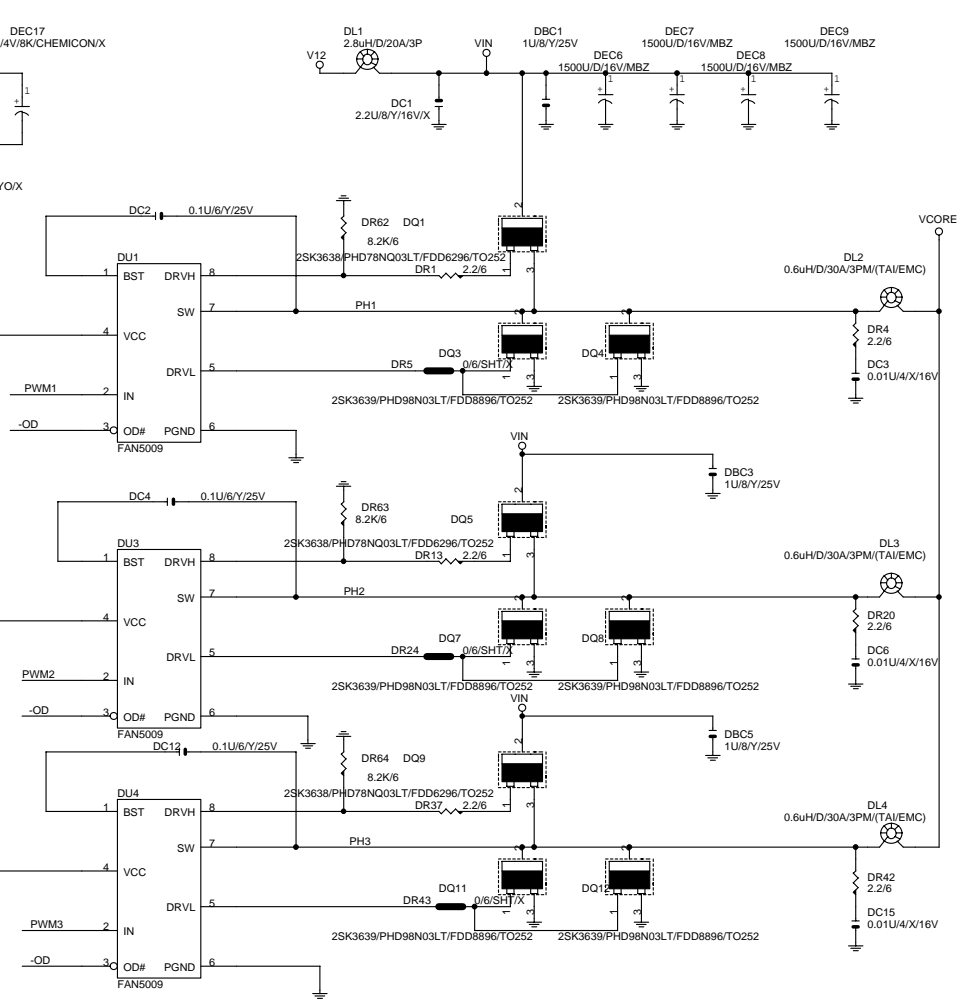
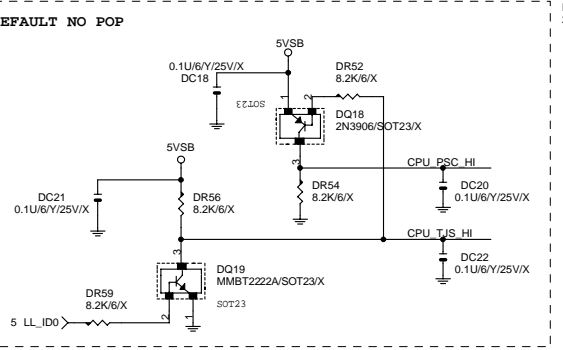
12, 15, 16, 20, 27 PWROK < DR17 0/6/X > 5.29 VTT\_PWRGD < DR19 0/6 >

5 VSS\_SENSE < DR22 0/6/X > 5 VCC\_SENSE < DR28 0/6/X >

DR41 : 約 200A DR36 : TRACER 拉到 CHOKE, 算出 CHOKE 兩端壓降

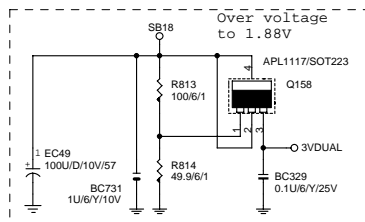


DR27 放到 CHOKE 為溫度補償



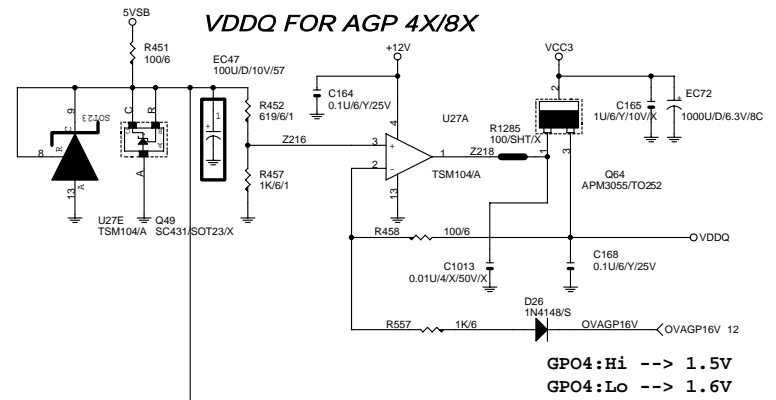
<b>GIGABYTE</b>		
VRD 10.1		
Size	Document Number	Rev
Custom	<b>GIGABYTE</b>	<b>1.0</b>
Date:	星期一, 九月 06, 2004	Sheet 28 of 34

### 18VDUAL FOR SB & NB



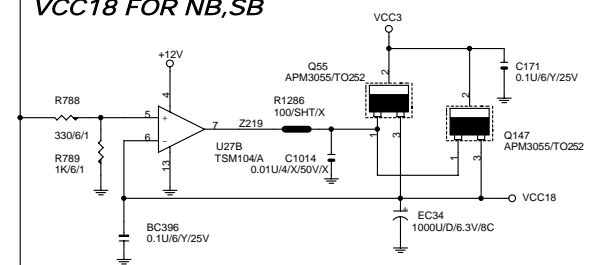
18VDUAL: USB 2.0 unplug, 50mA, each USB 2.0 device add (32~41mA). Maximum load (USB2.0 device\*8) is 327mA.

### VDDQ FOR AGP 4X/8X

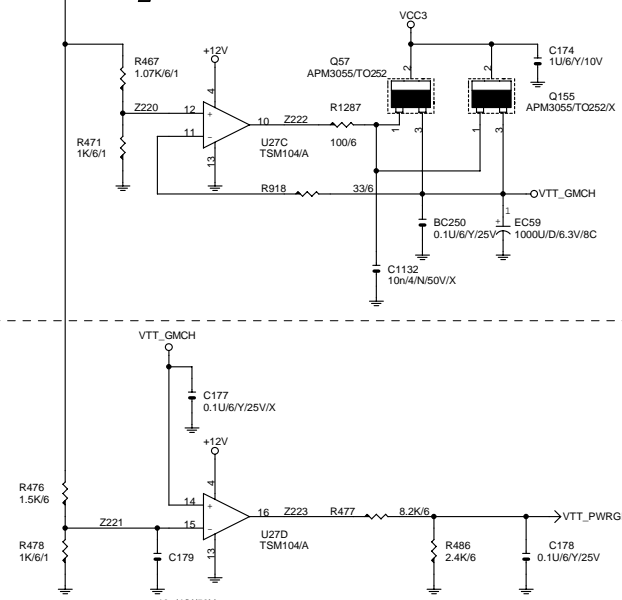


GPO4:Hi --> 1.5V  
GPO4:Lo --> 1.6V

### VCC18 FOR NB,SB



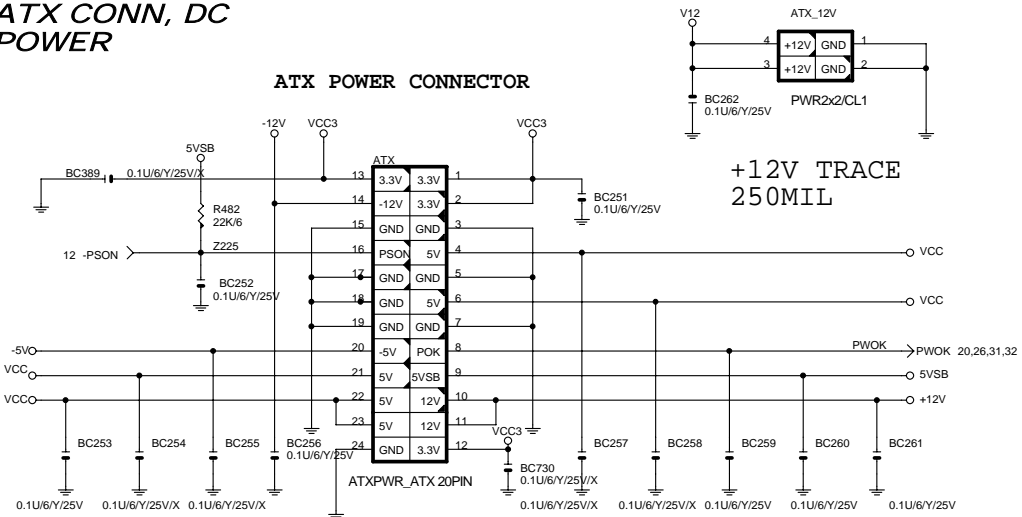
### VTT\_GMCHVID FOR 775 CPU



<b>GIGABYTE</b>			
Title <b>VDDQ, VCCVID, 3VDUAL</b>			
Size	Document Number		Rev
Custom		<b>GIGABYTE</b>	<b>1.0</b>
Date:	星期一, 九月 06, 2004	Sheet	29 of 34

# ATX CONN, DC POWER

## ATX POWER CONNECTOR



ITEM	DESCRIPTION	STATUS	Default
GPIO0	Non Use		Hi
GPIO1	Non Use		Hi
GPIO4	Non Use		Hi
GPIO2	Non Use		Hi
GPIO3	Green Button	Hi:Normal, Lo:Into Green mode	Hi
GPIO5	REQ5		
GPIO6	GNT5		
GPIO7	Non Use		Hi
GPIO11	Non Use		Hi
GPIO18	Wake On Ring	Hi:Normal, Lo:Ring Power On	Hi
GPIO9	Case Open	Hi:Case Open, Lo:Normal	Lo
GPIO10	Clear Caseopen status	Hi:Clear Caseopen Status, Lo:Normal	Lo
GPIO13	Non Use		Hi
GPIO12	Non Use		Hi
GPIO14	Primary Down	Lo:CODEC Only	Lo
GPIO15	KB Data		Hi
GPIO16	KB CLK		Hi
GPIO17	MS Data		Hi
GPIO18	MS CLK		Hi

### States for a single-color power LED

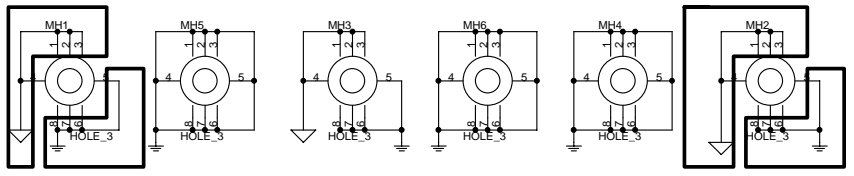
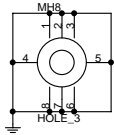
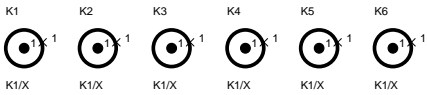
LED States	ACPI States	BIOS			
		MPD+	MPD-	GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING

### States for a dual-color power LED

LED States	ACPI States	BIOS			
		MPD+	MPD-	GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING
Steady Yellow	S1,S3	LO	HI	HI	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING	HI	BLINKING

### States for green LED

LED States	ACPI States	BIOS	
		GLEP+	GPIO11
ON	S1,S3	HI	HI
OFF	S0,S5	LO	LO



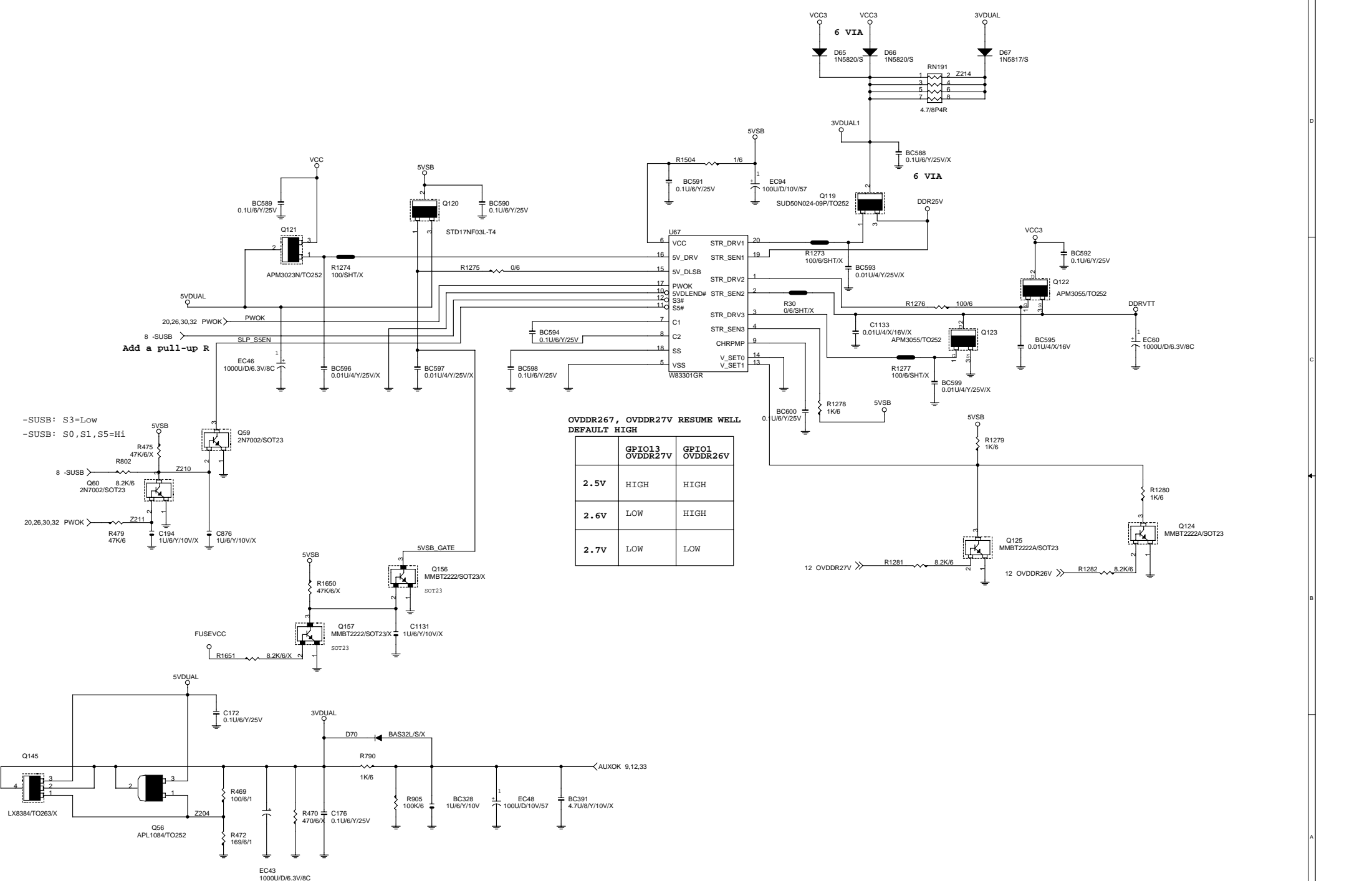
EMI (VCC.GND CUT HOLE PLANE)

EMI (VCC.LGND CUT HOLE PLANE)

### BIOS REQUEST

SINGLE	DUAL	INTEL LED DEFINED				GIGABYTE LED DEFINED				SINGLE	DUAL
		GPIO7	ACPILED	GPIO11		GPIO7	ACPILED	GPIO11			
GREEN	GREEN	S0	LO	LO	LO	S0	LO	LO	LO	GREEN	GREEN
OFF	YELLOW	S1	HI	HI	HI	S1	LO	BLINKING	HI	G(BLINK)	G(BLINK)
OFF	YELLOW	S3	HI	HI	HI	S3	HI	HI	HI	OFF	YELLOW
OFF	OFF	S4/S5	LO	HI/NC	LO	S4/S5	LO	HI/NC	LO	OFF	OFF

<b>GIGABYTE</b>		
<b>ATX, GPIO LIST</b>		
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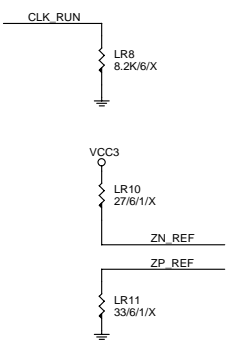
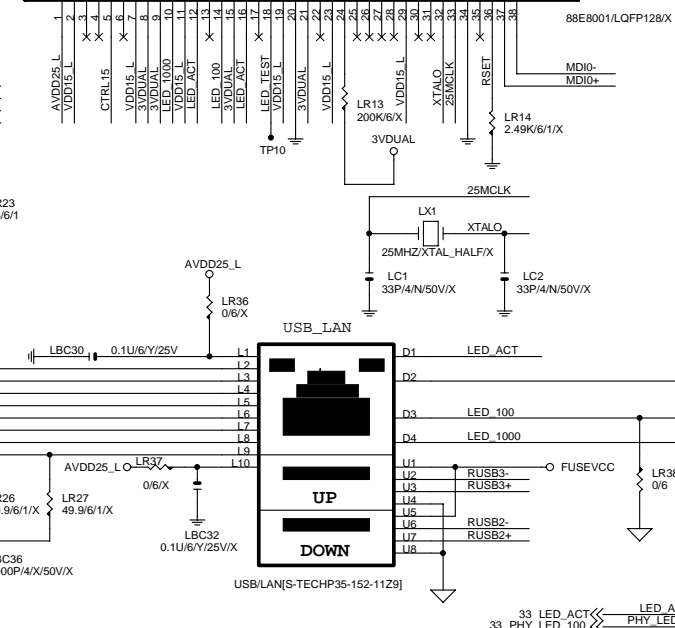
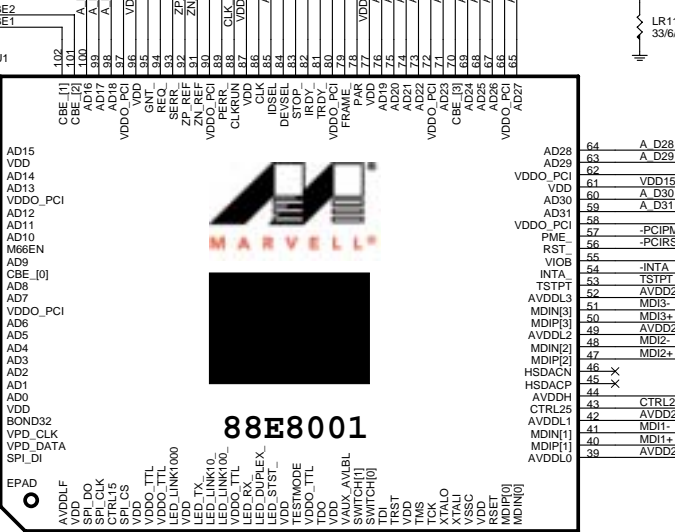
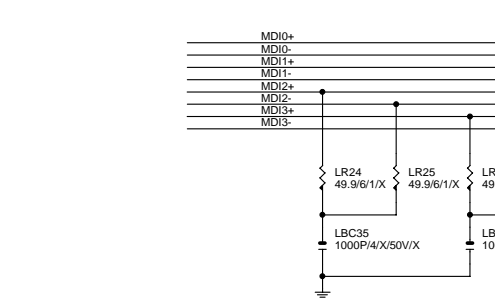
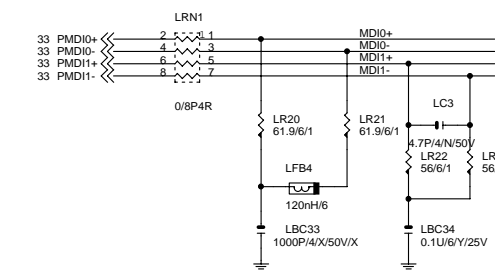
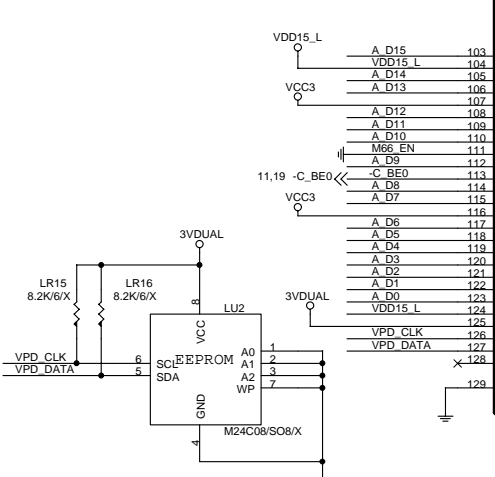
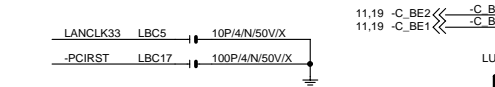


11.19 A\_D0[31] << A\_D0[31]

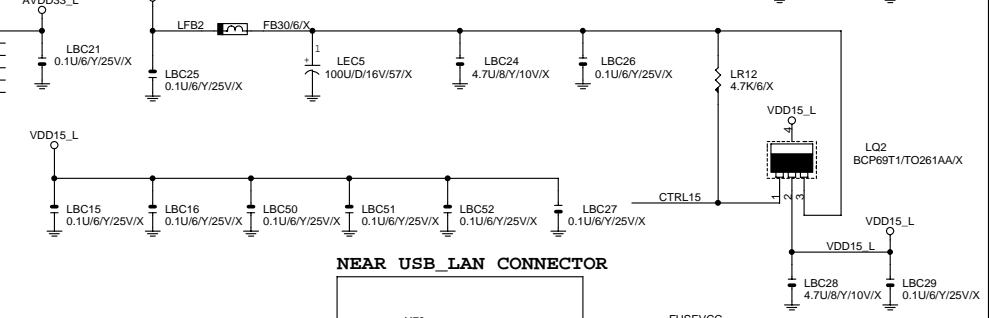
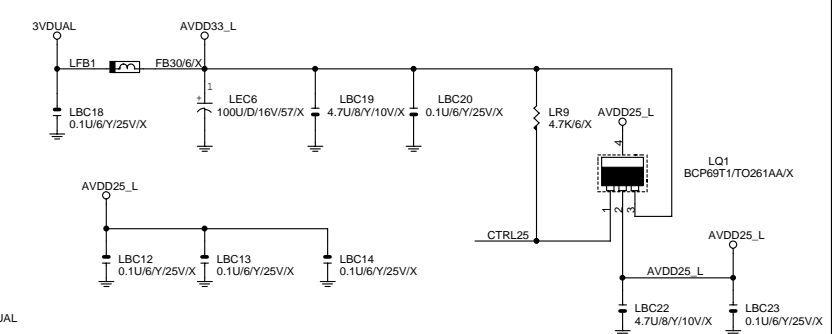
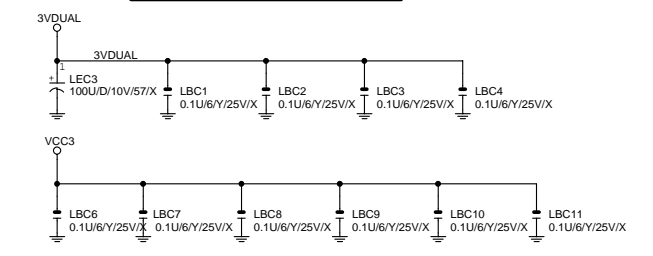
- 11.19 -C\_BE3 << -C\_BE3
- 11.19 -PAR << -PAR
- 11.19 -FRAME << -FRAME
- 11.19 -TRDY << -TRDY
- 11.19 -IRDY << -IRDY
- 11.19 -STOP << -STOP
- 11.19 -STOR << -STOR
- 11.19 -DEVSEL << -DEVSEL
- 15 LANCLK33 << LANCLK33
- 19 -PERR << -SERR
- 11.19 -SER<< -REQ5
- 12.19 -REQ<< -GNT5

### # Layout Check 注意事項

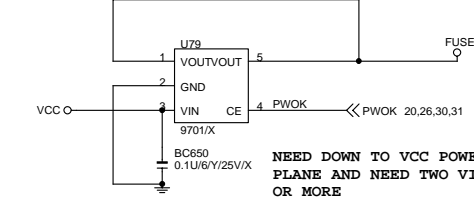
1. LU1 Pin129 需下內層GND, 至少打 22 VIA
2. 3VDUAL, VCC3, VDD15\_L, AVDD25\_L 至少走20mil寬, 並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線, TRACE 愈短愈好, 線寬12mil
4. MDI正負0-3, TRACE 8:7:8, 每對之間保持 40mil



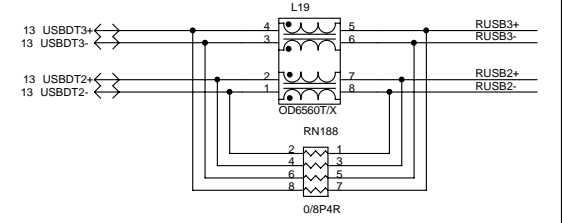
### POWER DECOUPLING CAP.



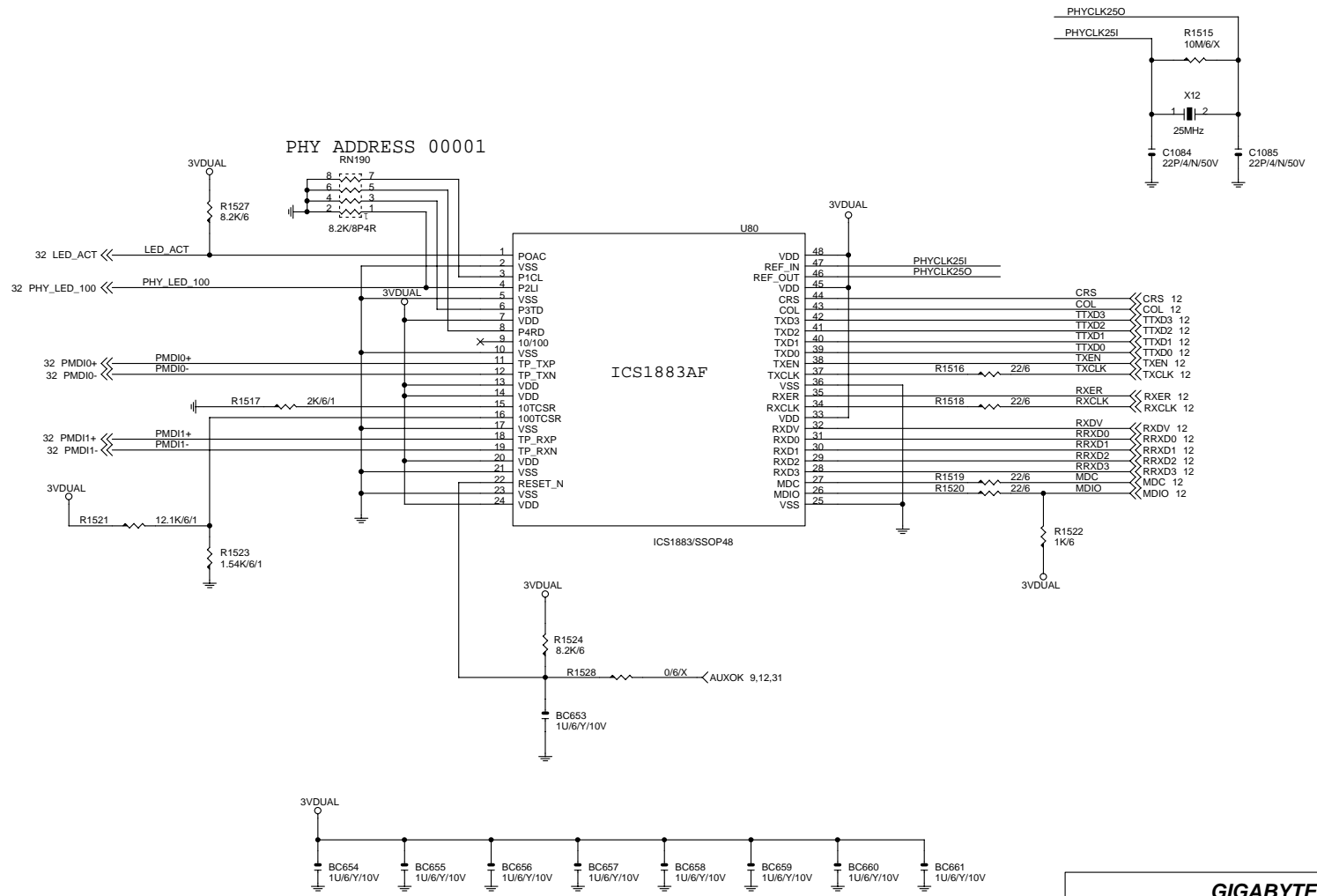
### NEAR USB LAN CONNECTOR



NEED DOWN TO VCC POWER PLANE AND NEED TWO VIA OR MORE



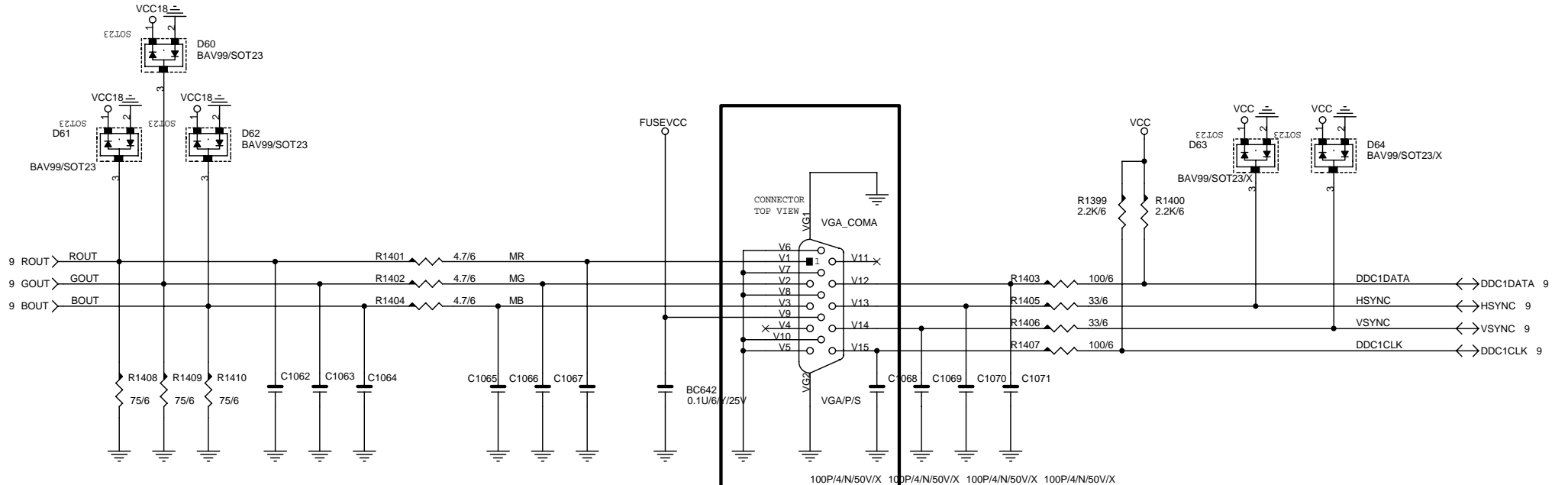
<b>GIGABYTE</b>		
<b>MARVELL 88E8001</b>		
Title	Document Number	Rev
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<b>GIGABYTE</b>		
<b>Title</b>		
<b>1394PHY &amp; CONN</b>		
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Custom	<b>GIGABYTE</b>	<b>1.0</b>
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# VGA CONNECTOR 1

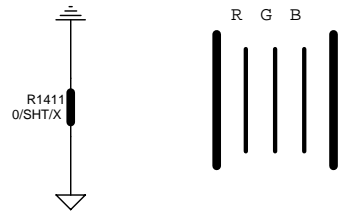
SIS 648 (FX) NO POP



PLEASE PLACE THESE COMPONENTS AS NEAR VGA CONNECT AS POSSIBLE

22P/4/N/50V 22P/4/N/50V 22P/4/N/50V 10P/4/N/50V 10P/4/N/50V 10P/4/N/50V

## DUAL LAYOUT (VGA/COM)



REV 0.2 VGA GND GUARD

<b>GIGABYTE</b>		
Title <b>VGA CONNECTOR</b>		
Size B	Document Number <b>GIGABYTE</b>	Rev <b>1.0</b>
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