

# GIGABYTE GA-8LD533 Schematics

Revision 1.0

SHEET

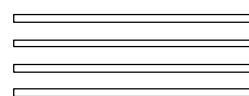
TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	SYSTEM BLOCK DIAGRAM
04	P4_478A
05	P4_478B
06	P4_478C
07	GMCH-A(845GL)CPU,DDR INTERFACE U1
08	GMCH-A(845GL)DDR,VGA INTERFACE
09	GMCH-A(845GL)POWER INTERFACE
10	DDR SERIAL TERMINATION
11	DDR1,2
12	VTT_DDR TERMMINATOR
13	ICH4-1 (HUB,PCI,CNR,AC97,USB) U12
14	ICH4-2
15	FWH (FLASH ROM)
16	CLOCK GENERATOR(ICS950211AF) U13
17	PCI1 & PCI2 SLOT
18	PCI3 SLOT
19	LPC I/O IR(ITE 8712 VER:GX) U14
20	IDE1, 2 CONNECTOR
21	PS/2 KB & MOUSE & F_USB
22	FLOPPY, COM & LPT & WOR & WOL CONNECTOR
23	FAN & H/W MONITOR ,CASE OPEN

SHEET

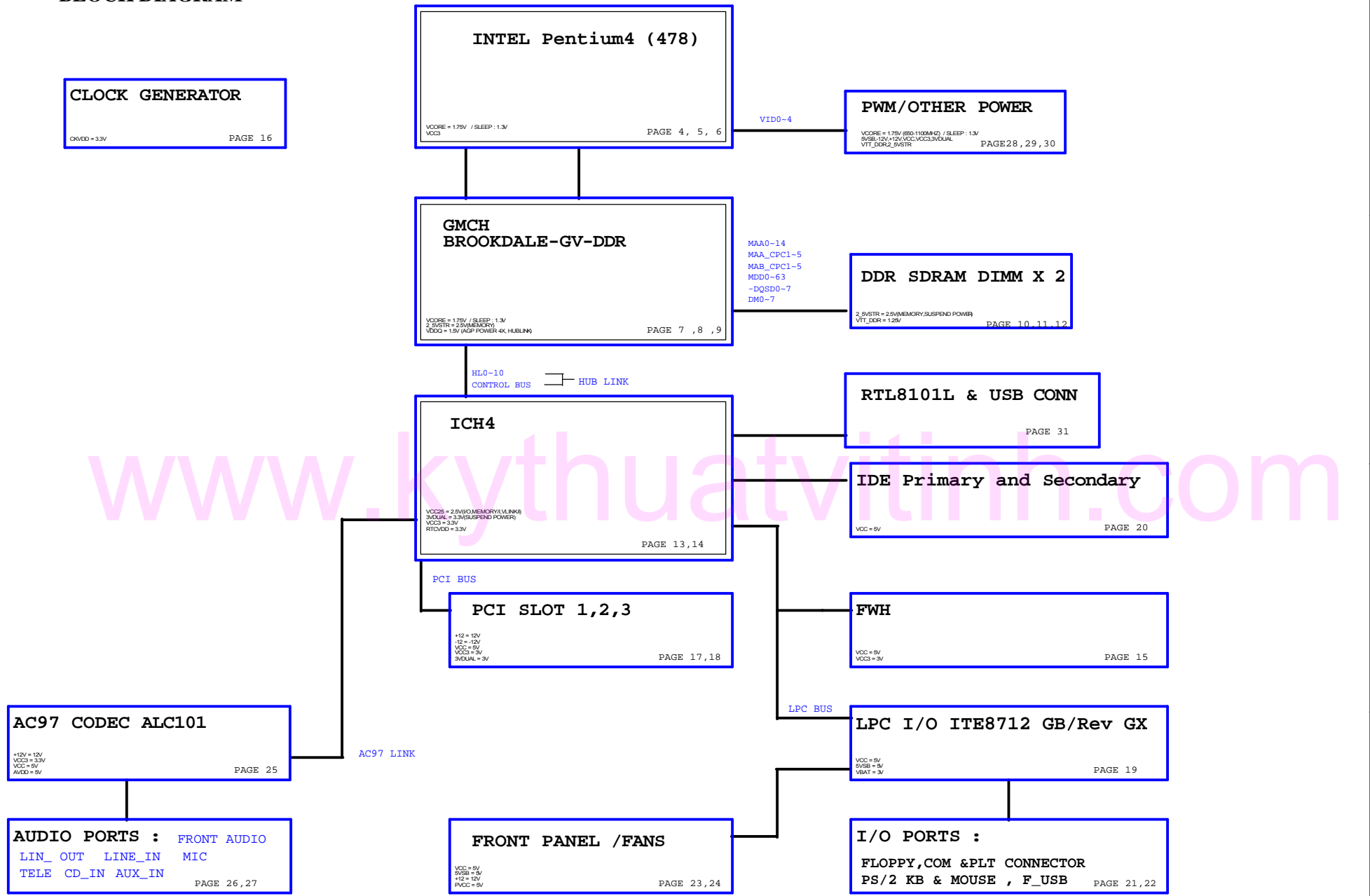
TITLE

24	FRONT PANEL,LED
25	AC97 CODEC <b>REALTEK ALC101</b>
26	LINE OUT & FRONT AUDIO CONN
27	LINE IN,MIC,CDIN,AUX(CD-IN2) GAME PORT
28	MISC. PWR & ATX POWER ( <b>3VDUAL, VDDQ</b> )
29	VCORE PWM(HIP6302+6602A)
30	DDR POWER ( <b>5VDUAL,2_5VSTR,VTT_DDR</b> )
31	RTL8101L Transformer
32	GPIO PIN LIST
33	PCI ROUNTING

		COMPONENT SIDE (1 oz. Copper) VCC SIDE (2 oz. Copper) GND SIDE (1 oz. Copper) SOLDER SIDE (1 oz. Copper)
<b>GIGABYTE</b>		
Title <b>COVER SHEET</b>		
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# BLOCK DIAGRAM



**CLOCK GENERATOR**  
 CRVDD = 3.3V  
 PAGE 16

**INTEL Pentium4 (478)**  
 V<sub>CORE</sub> = 1.75V / SLEEP: 1.3V  
 V<sub>CC3</sub>  
 PAGE 4, 5, 6

**PWM/OTHER POWER**  
 V<sub>CORE</sub> = 1.75V (650-1100MHz) / SLEEP: 1.3V  
 5VSB: 1.0V / +12V / V<sub>CC3</sub> / 5V<sub>DUAL</sub>  
 V<sub>TT\_DDR2\_5VSTR</sub>  
 PAGE 28, 29, 30

**GMCH BROOKDALE-GV-DDR**  
 V<sub>CORE</sub> = 1.75V / SLEEP: 1.3V  
 2.5VSTR = 2.5V (MEMORY SUSPEND POWER)  
 V<sub>DDQ</sub> = 1.5V (AGP POWER 4X, HUBLINK)  
 PAGE 7, 8, 9

**DDR SDRAM DIMM X 2**  
 2.5VSTR = 2.5V (MEMORY SUSPEND POWER)  
 V<sub>TT\_DDR</sub> = 1.25V  
 PAGE 10, 11, 12

**ICH4**  
 V<sub>CC25</sub> = 2.5V (IO MEMORY LINK)  
 5V<sub>DUAL</sub> = 2.5V (SUSPEND POWER)  
 V<sub>CC3</sub> = 3.3V  
 RTV<sub>DDQ</sub> = 3.3V  
 PAGE 13, 14

**RTL8101L & USB CONN**  
 PAGE 31

**IDE Primary and Secondary**  
 V<sub>CC</sub> = 5V  
 PAGE 20

**PCI SLOT 1,2,3**  
 +12 = 12V  
 -12 = 12V  
 V<sub>CC</sub> = 5V  
 V<sub>CC3</sub> = 3V  
 3V<sub>DUAL</sub> = 3V  
 PAGE 17, 18

**FWH**  
 V<sub>CC</sub> = 5V  
 V<sub>CC3</sub> = 3V  
 PAGE 15

**AC97 CODEC ALC101**  
 +12V = 12V  
 V<sub>CC3</sub> = 3.3V  
 V<sub>CC</sub> = 5V  
 AV<sub>DD</sub> = 5V  
 PAGE 25

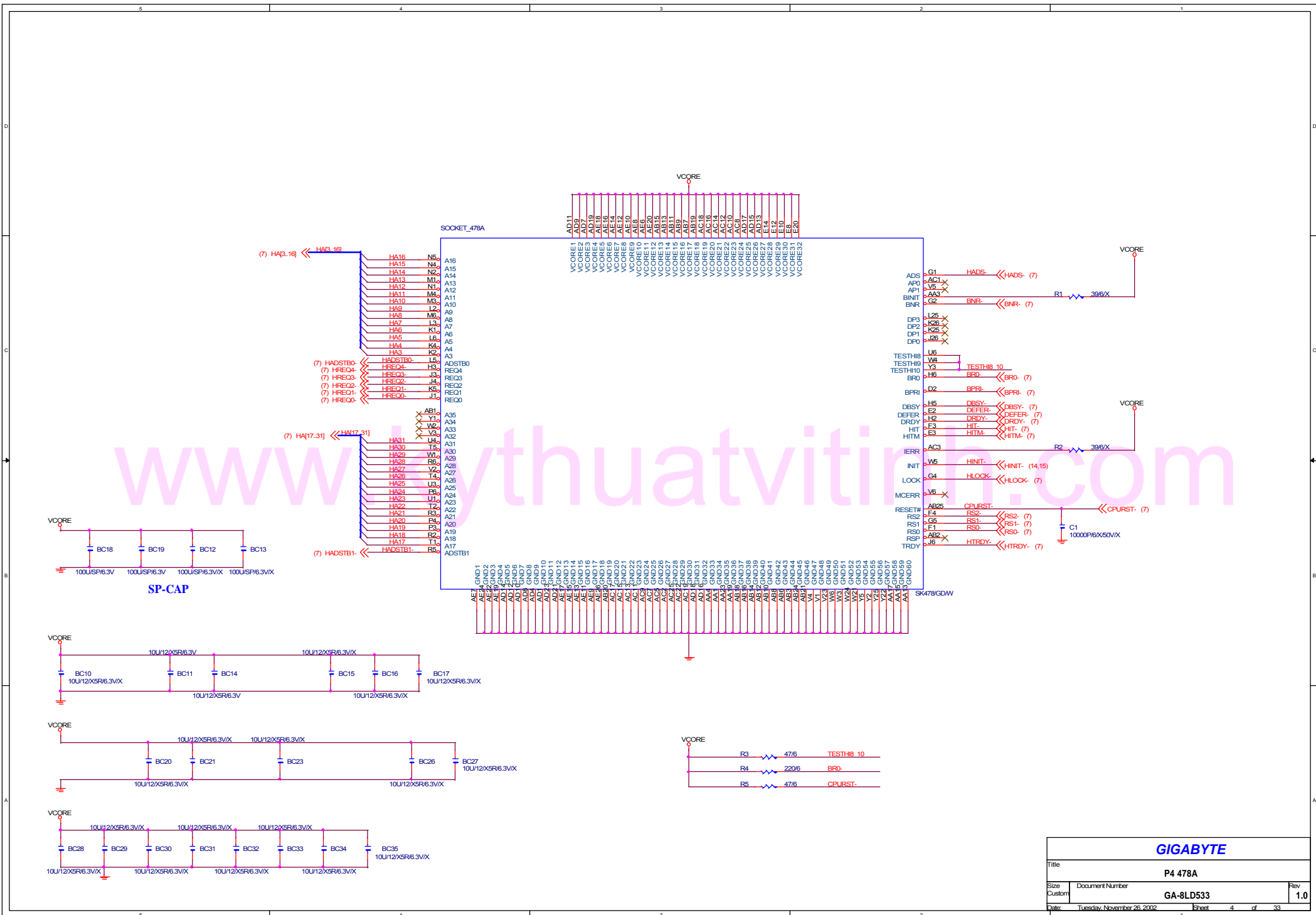
**AUDIO PORTS :** FRONT AUDIO  
 LIN\_OUT LINE\_IN MIC  
 TELE\_CD\_IN AUX\_IN  
 PAGE 26, 27

**FRONT PANEL /FANS**  
 V<sub>CC</sub> = 5V  
 5V<sub>SB</sub> = 5V  
 +12 = 12V  
 V<sub>CC</sub> = 5V  
 PAGE 23, 24

**LPC I/O ITE8712 GB/Rev GX**  
 V<sub>CC</sub> = 5V  
 5V<sub>SB</sub> = 5V  
 V<sub>BAT</sub> = 3V  
 PAGE 19

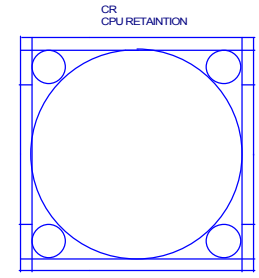
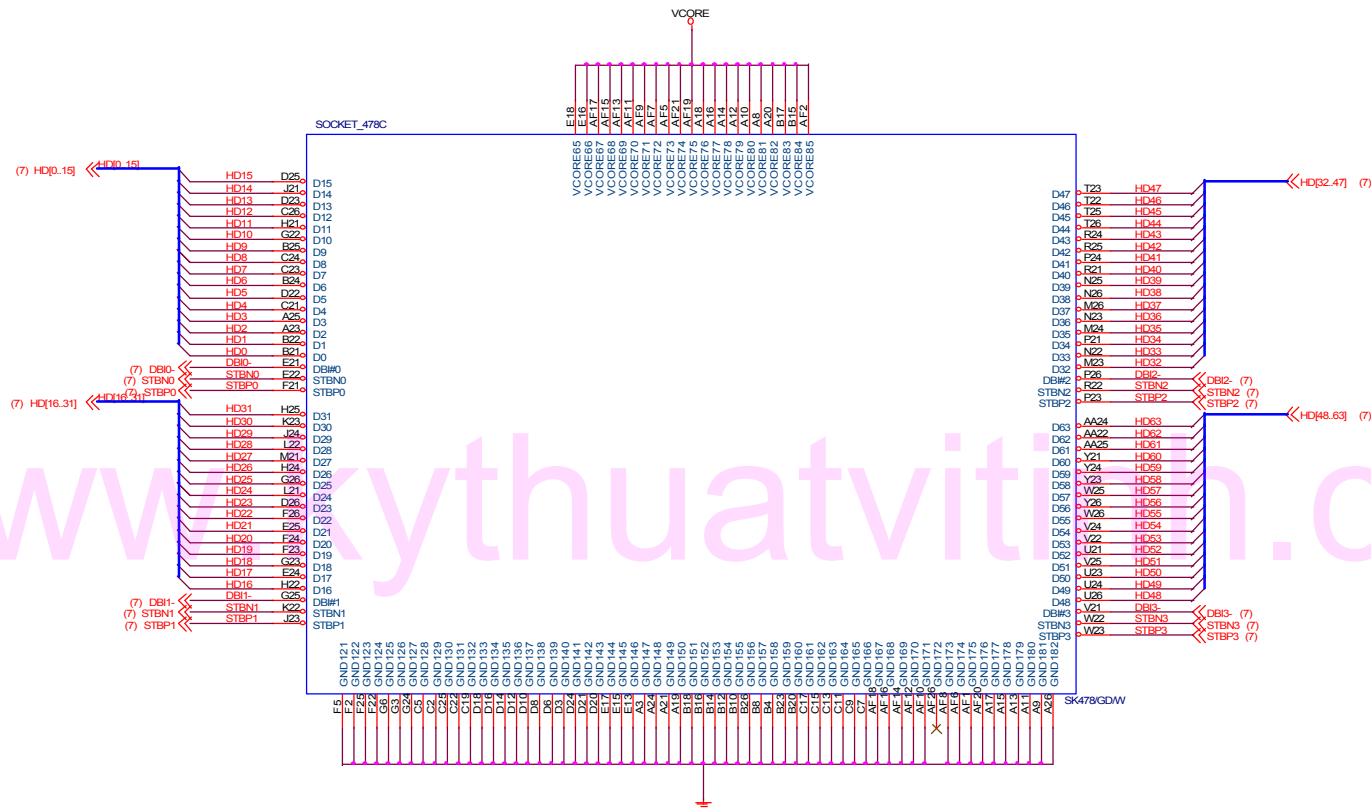
**I/O PORTS :**  
 FLOPPY, COM & PLT CONNECTOR  
 PS/2 KB & MOUSE , F\_USB  
 PAGE 21, 22

<b>GIGABYTE</b>			
<b>BOM &amp; PCB MODIFY HISTORY</b>			
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<b>GIGABYTE</b>		
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P4 478A		
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<b>GIGABYTE</b>		
Title <b>P4 478C</b>		
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(11,12) MD[0..63] << MD[0..63] (8)

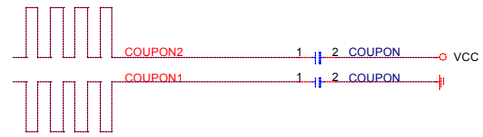
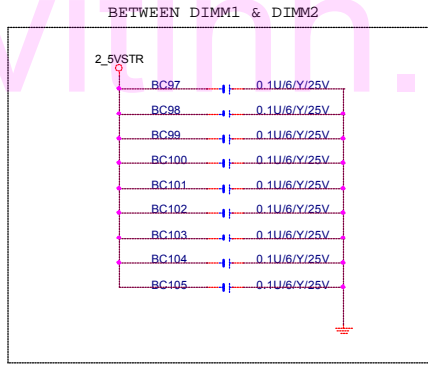
(11,12) DM[0..7] >> DM[0..7] (8)

(11,12) -DQS[0..7] << -DQS[0..7] (8)

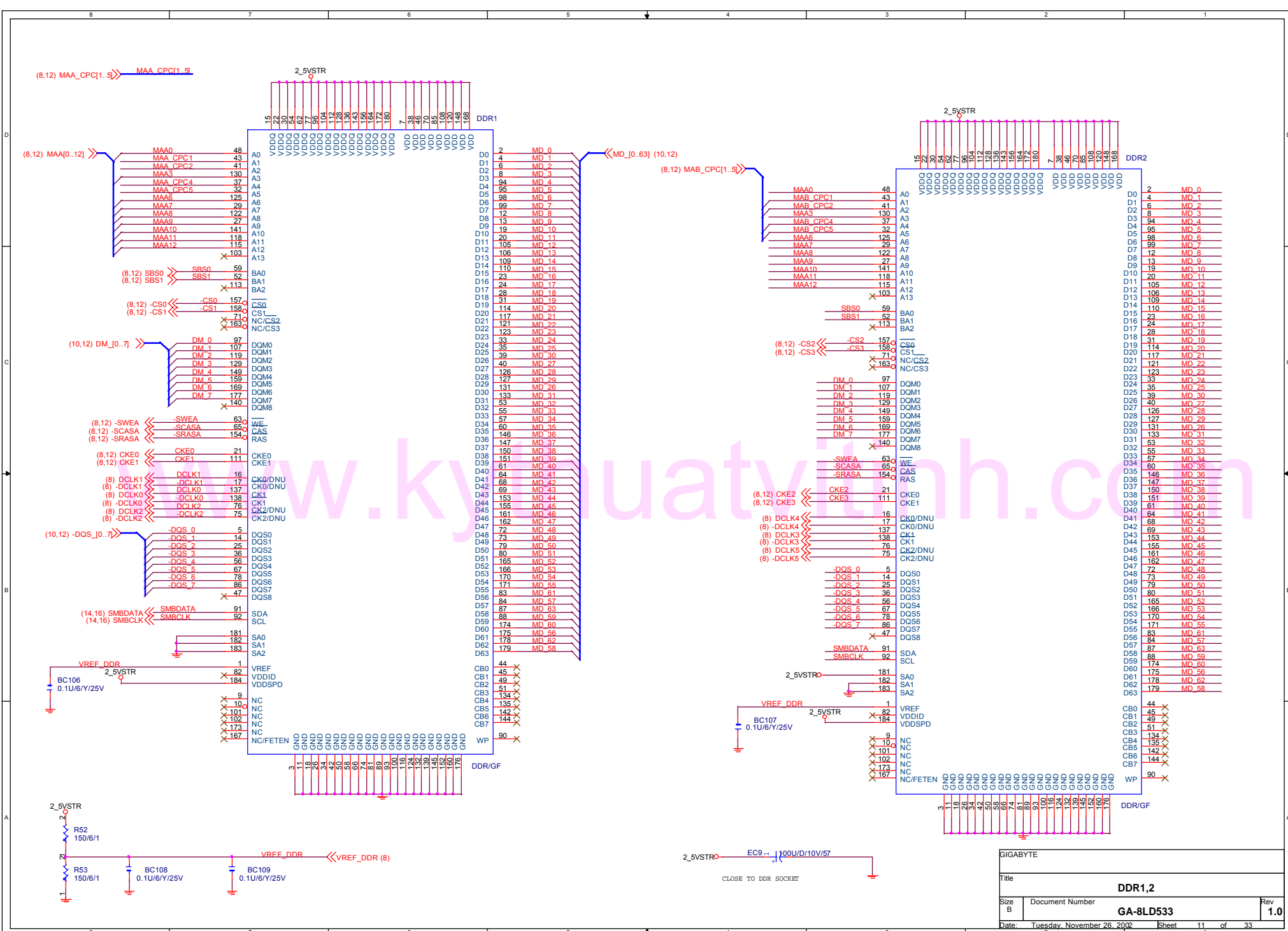
DM_0	RN3	1	20/8P4R/X	DM0
-DQS_0		3	4	-DQS0
MD_2		5	6	MD2
MD_6		7	8	MD6
MD_0	RN5	1	20/8P4R/X	MD0
MD_4		3	4	MD4
MD_5		5	6	MD5
MD_1		7	8	MD1
MD_12	RN6	1	20/8P4R/X	MD12
MD_13		3	4	MD13
-DQS_1		5	6	-DQS1
DM_1		7	8	DM1
MD_14	RN7	1	20/8P4R/X	MD14
MD_15		3	4	MD15
MD_10		5	6	MD10
MD_11		7	8	MD11
-DQS_2	RN9	1	20/8P4R/X	-DQS2
DM_2		3	4	DM2
MD_18		5	6	MD18
MD_22		7	8	MD22
MD_29	RN11	1	20/8P4R/X	MD29
MD_25		3	4	MD25
-DQS_3		5	6	-DQS3
DM_3		7	8	DM3
MD_26	RN12	1	20/8P4R/X	MD26
MD_30		3	4	MD30
MD_27		5	6	MD27
MD_31		7	8	MD31
MD_32	RN13	1	20/8P4R/X	MD32
MD_36		3	4	MD36
MD_33		5	6	MD33
MD_37		7	8	MD37
MD_39	RN14	1	20/8P4R/X	MD39
MD_35		3	4	MD35
MD_40		5	6	MD40
MD_44		7	8	MD44
-DQS_4	RN15	1	20/8P4R/X	-DQS4
DM_4		3	4	DM4
MD_34		5	6	MD34
MD_38		7	8	MD38
MD_45	RN16	1	20/8P4R/X	MD45
MD_41		3	4	MD41
MD_5		5	6	MD5
-DQS_5		7	8	-DQS5
MD_48	RN17	1	20/8P4R/X	MD48
MD_49		3	4	MD49
MD_52		5	6	MD52
MD_53		7	8	MD53
MD_50	RN18	1	20/8P4R/X	MD50
MD_51		3	4	MD51
MD_60		5	6	MD60
MD_61		7	8	MD61
DM_6	RN19	1	20/8P4R/X	DM6
-DQS_6		3	4	-DQS6
MD_54		5	6	MD54
MD_55		7	8	MD55
MD_56	RN20	1	20/8P4R/X	MD56
MD_57		3	4	MD57
DM_7		5	6	DM7
-DQS_7		7	8	-DQS7
MD_62	RN21	1	20/8P4R/X	MD62
MD_58		3	4	MD58
MD_63		5	6	MD63
MD_59		7	8	MD59

MD_20	RN2	1	20/8P4R/X	MD20
MD_16		3	4	MD16
MD_17		5	6	MD17
MD_21		7	8	MD21
MD_42	RN4	1	20/8P4R/X	MD42
MD_46		3	4	MD46
MD_43		5	6	MD43
MD_47		7	8	MD47

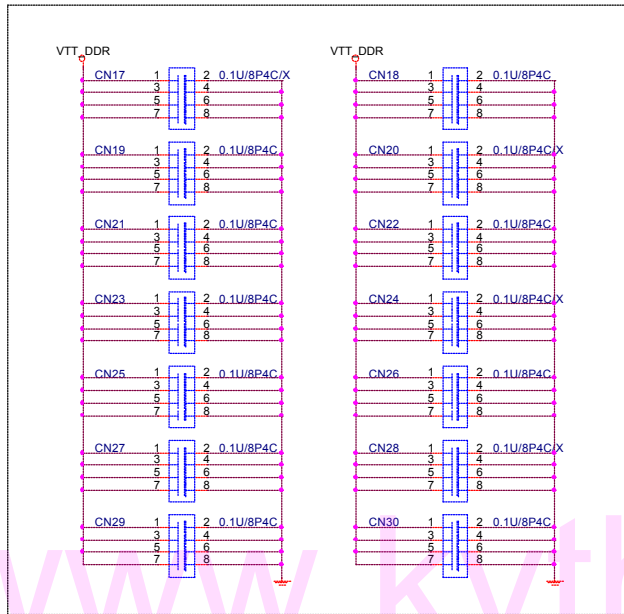
MD_7	RN8	1	20/8P4R/X	MD7
MD_3		3	4	MD3
MD_8		5	6	MD8
MD_9		7	8	MD9
MD_19	RN10	1	20/8P4R/X	MD19
MD_23		3	4	MD23
MD_24		5	6	MD24
MD_28		7	8	MD28



GIGABYTE	
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DDR SERIAL TERM.	
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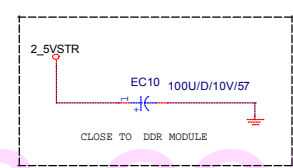
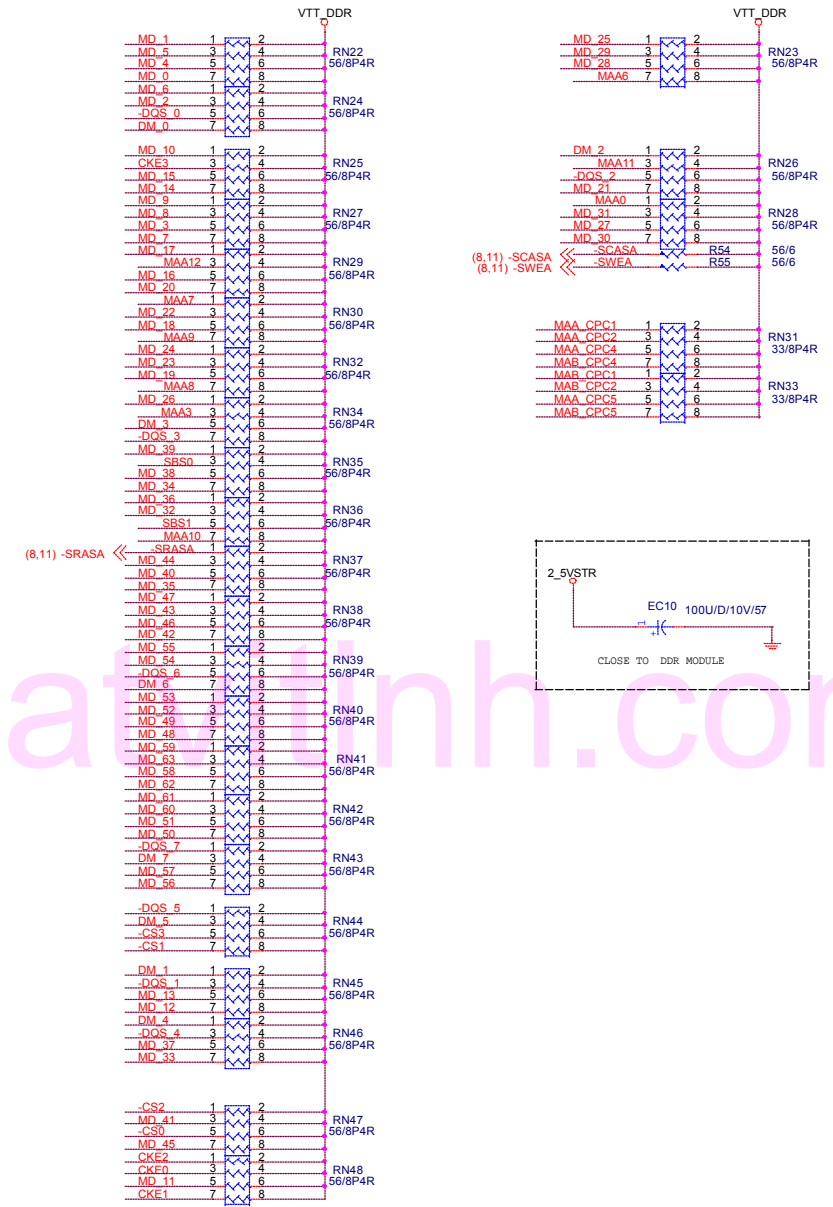


GIGABYTE	
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DDR1,2	
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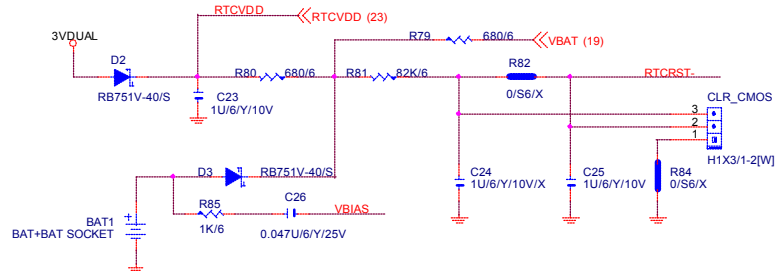
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- (10,11) DM[0..7] << MD [0..7]
- (10,11) -DQS[0..7] << -DQS [0..7]
- (8,11) MAA[0..12] << MAA[0..12]
- (8,11) -CS[0..3] << -CS[0..3]
- (8,11) CKE[0..3] << CKE[0..3]
- (8,11) SBS[0..1] << SBS[0..1]
- (8,11) MAA\_CPC[1..5] << MAA\_CPC[1..5]
- (8,11) MAB\_CPC[1..5] << MAB\_CPC[1..5]

CLOSE TO DDR TERMINATOR(1 CAP. FOR 2 R-PACKS)

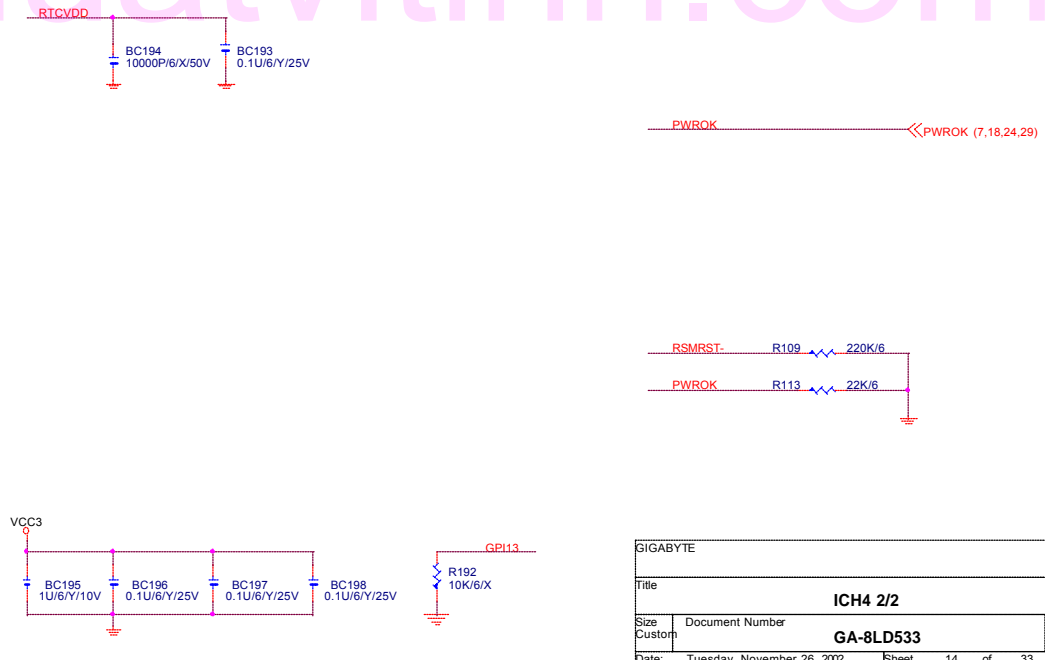
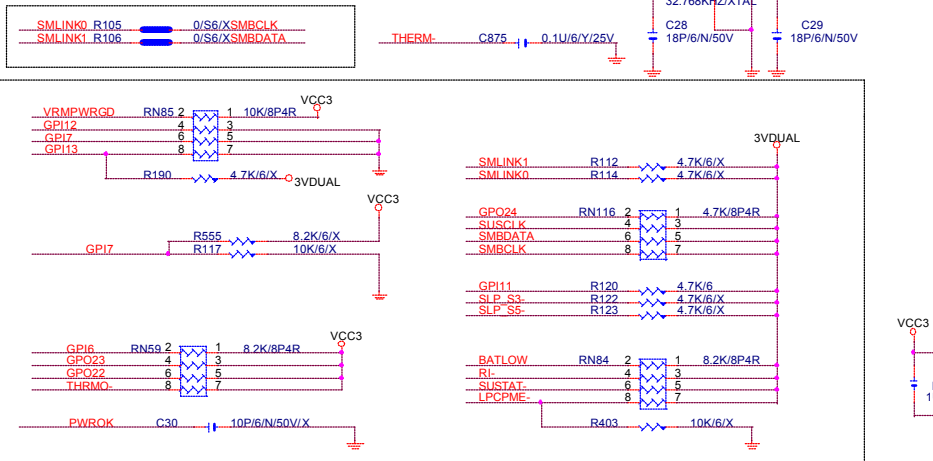
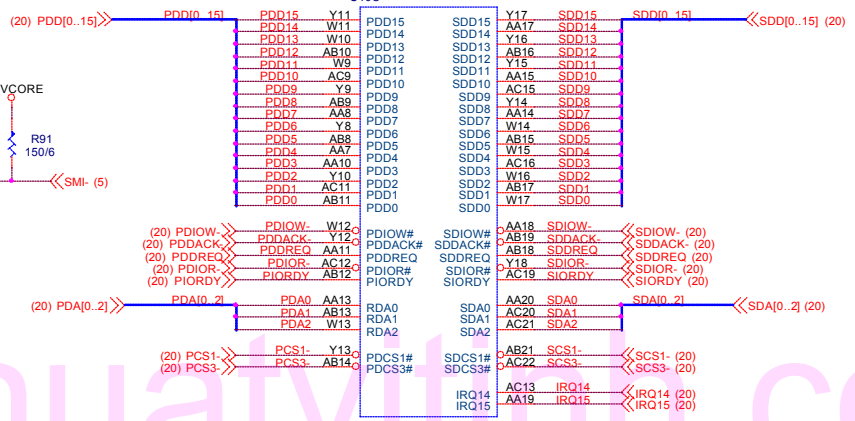
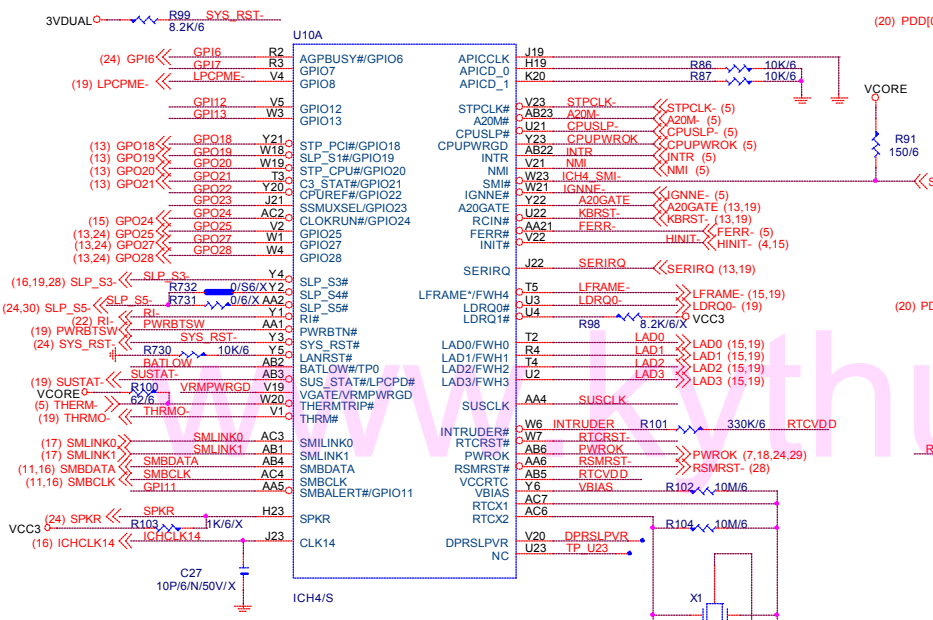


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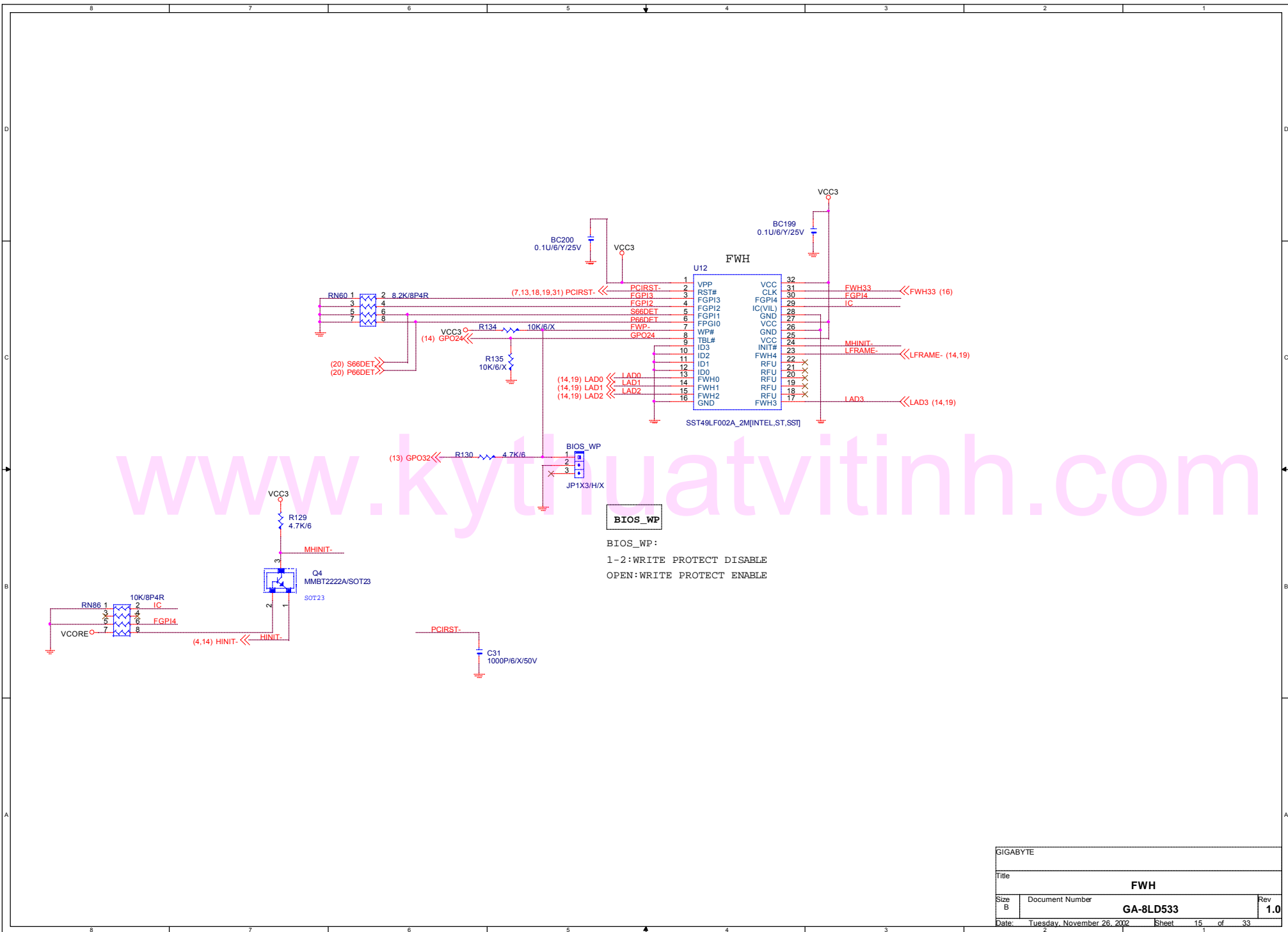




	CLR_CMOS
1-2	ENABLE (CLEAR CMOS)
2-3	NORMAL

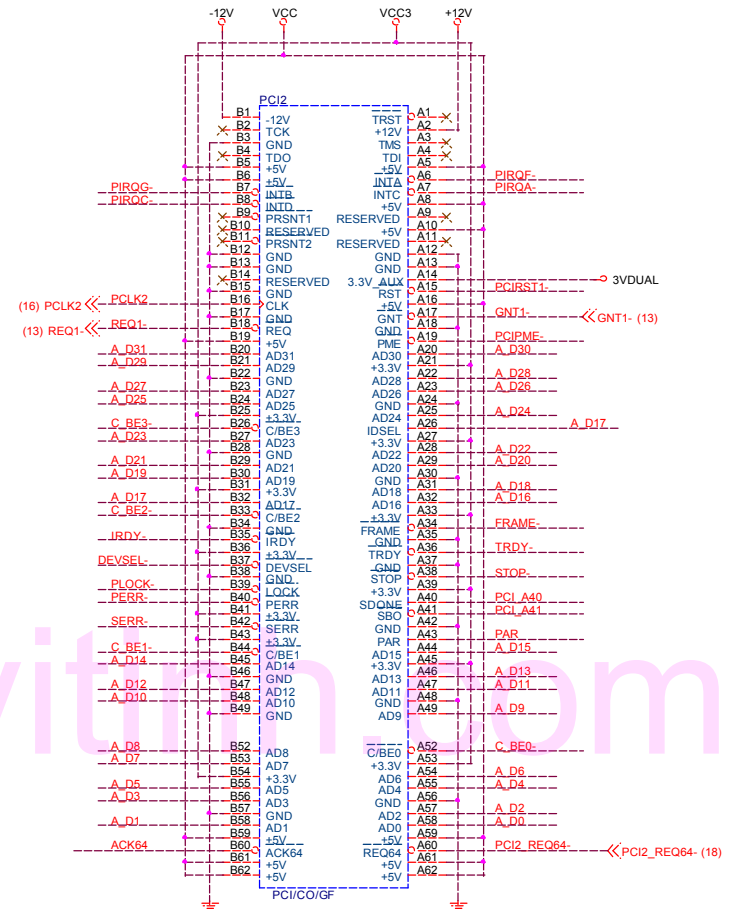
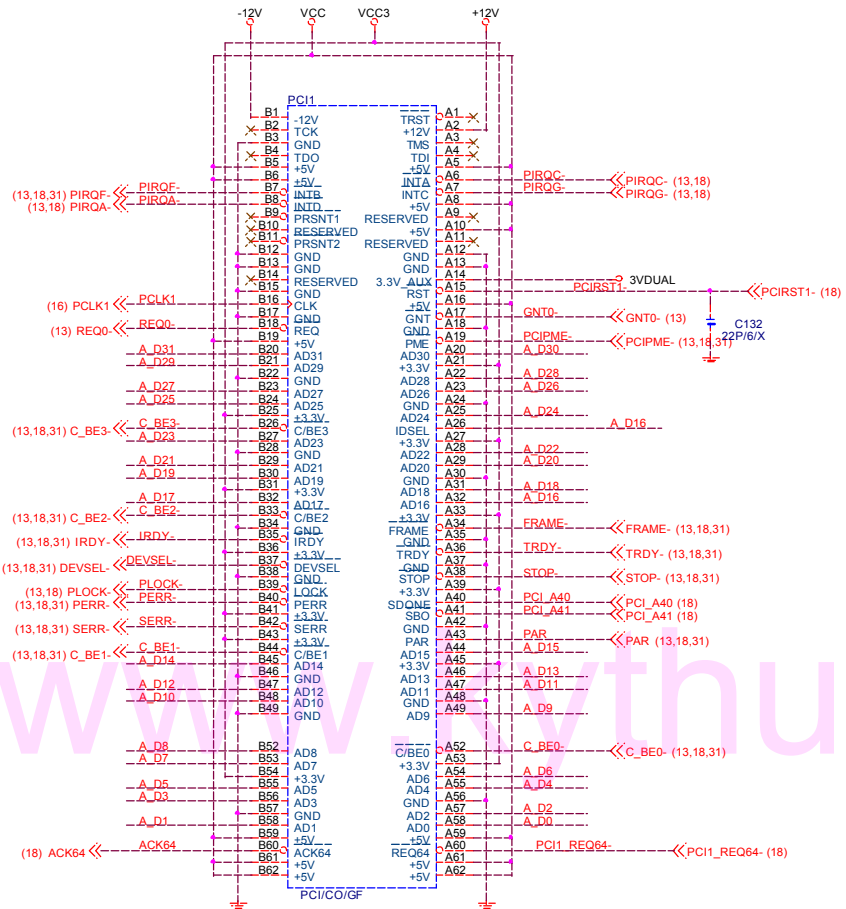


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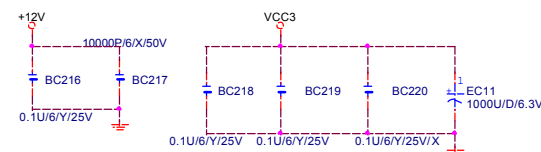
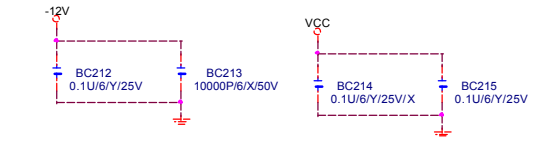
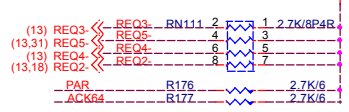
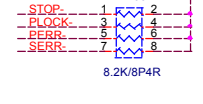
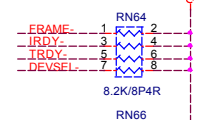
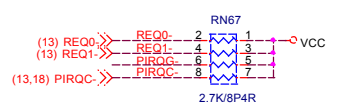
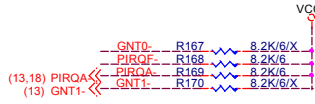
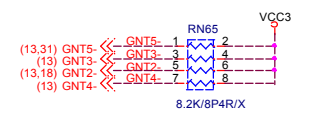
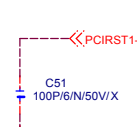


GIGABYTE			
Title			
<b>FWH</b>			
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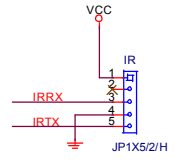
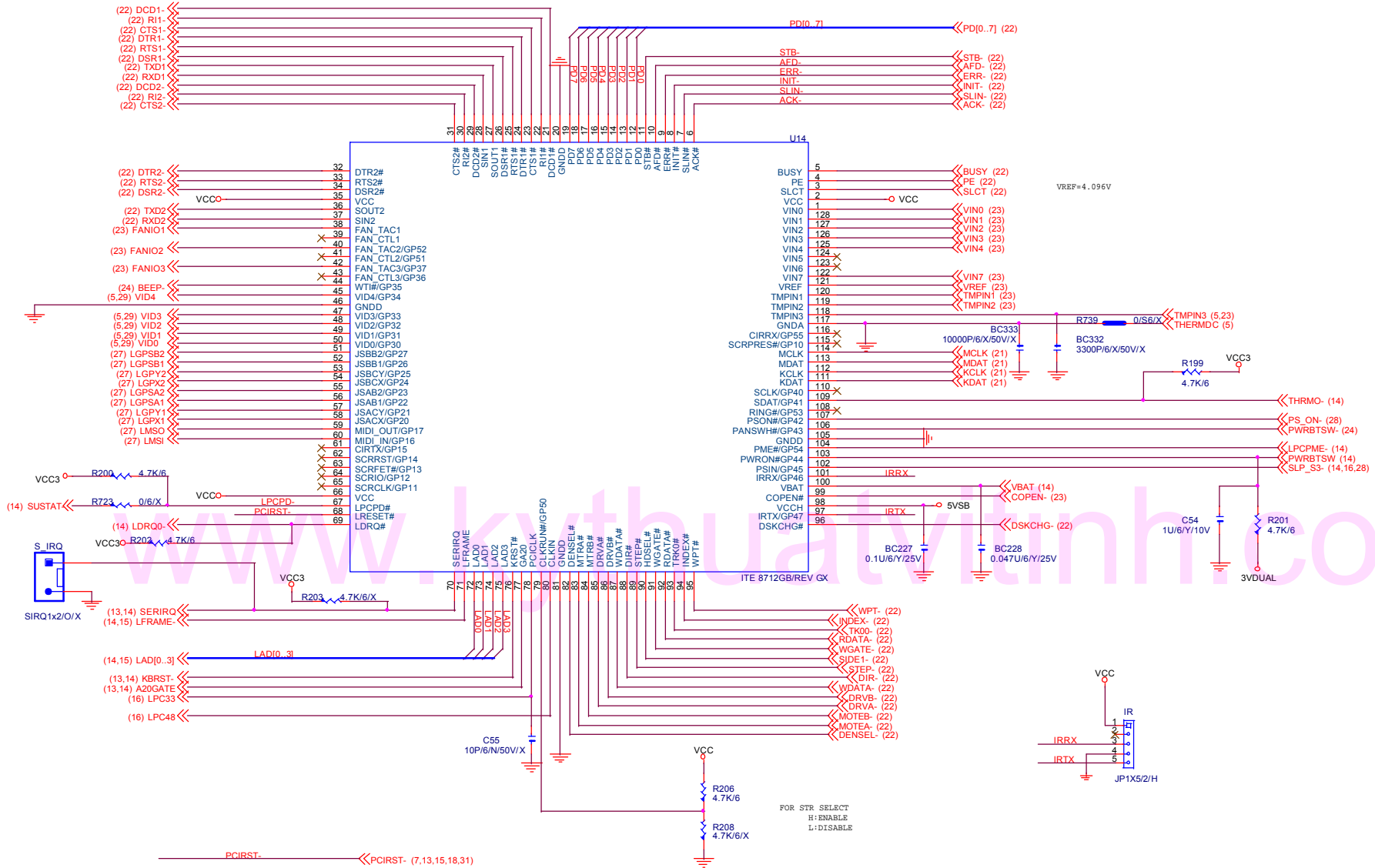
(13,18,31) A\_D[0..31] << A\_D[0..31]



GIGABYTE			
Title <b>PCI SLOT 1/2</b>			
Size B	Document Number	<b>GA-8LD533</b>	Rev <b>1.0</b>
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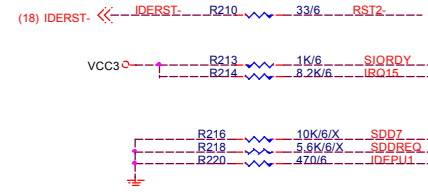
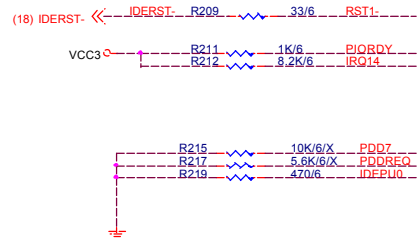
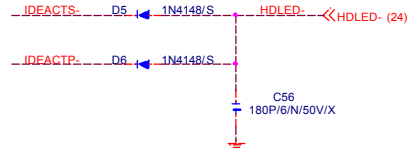






FOR STR SELECT  
H:ENABLE  
L:DISABLE

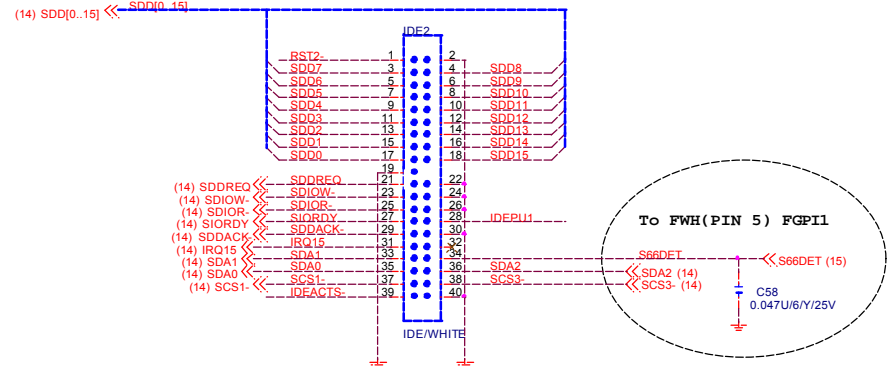
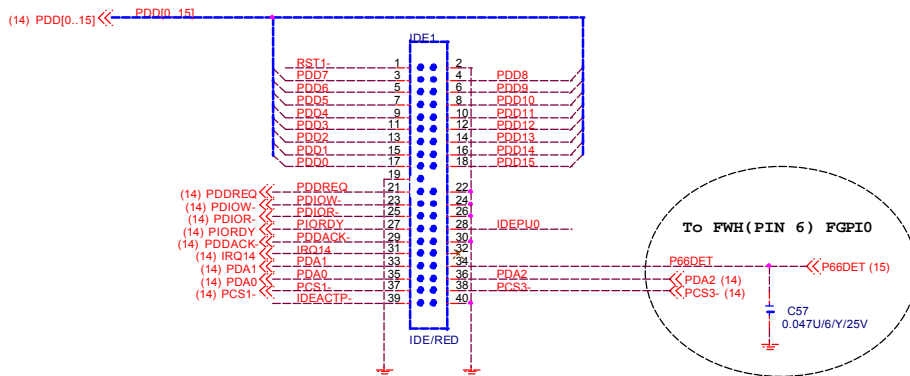
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Title <b>ITE 8712 LPC IO/GBT</b>	
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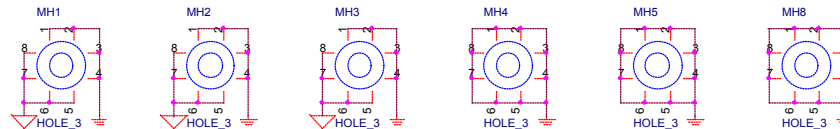
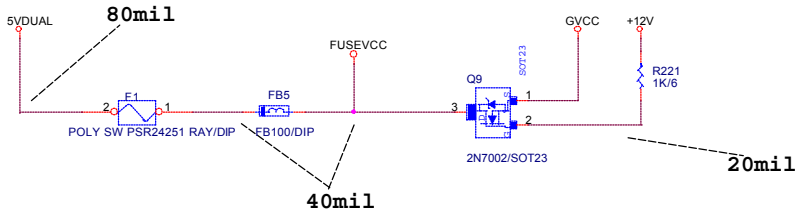
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PRIMARY IDE CONNECTOR

SECONDARY IDE CONNECTOR

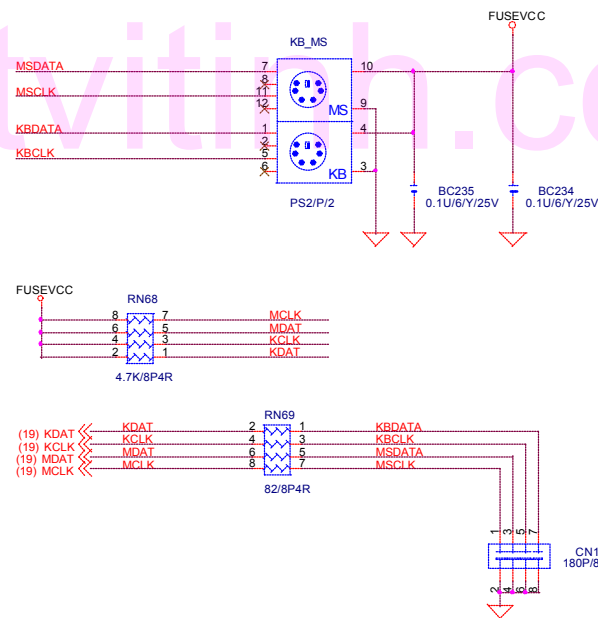
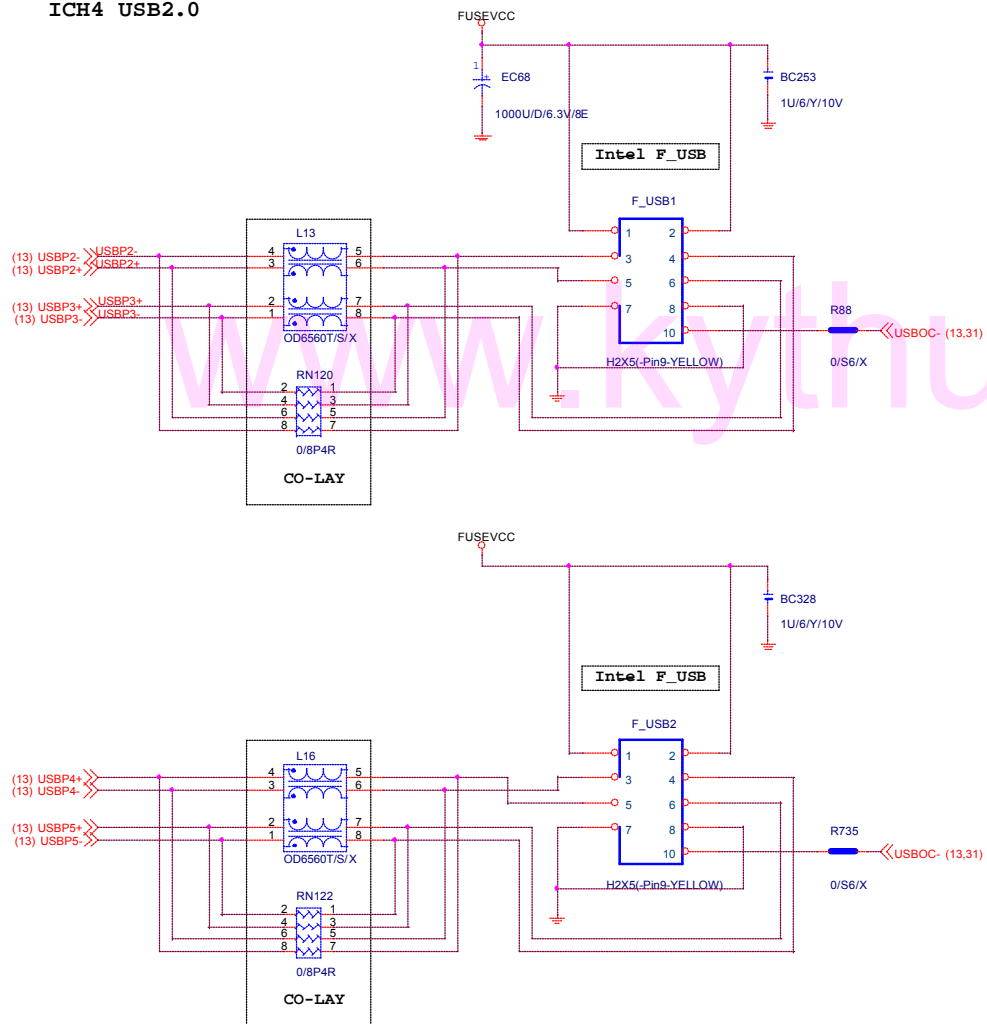


GIGABYTE			
Title			
<b>IDE CONNECTOR</b>			
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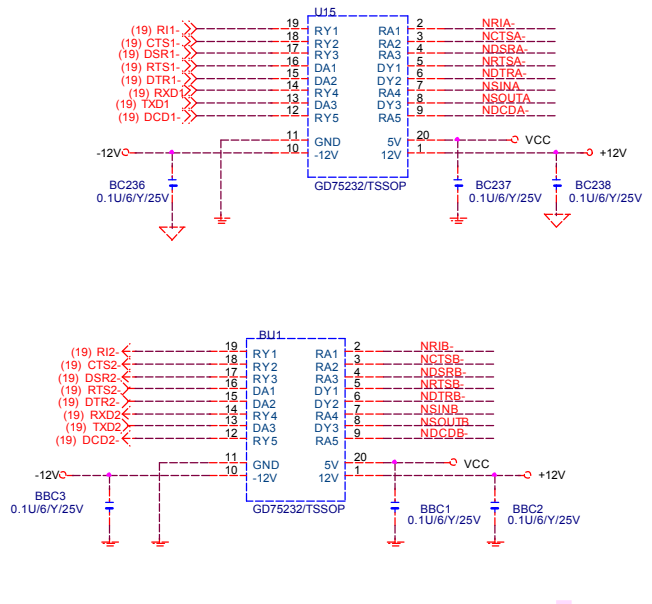
**FRONT USB CONN**

**ICH4 USB2.0**

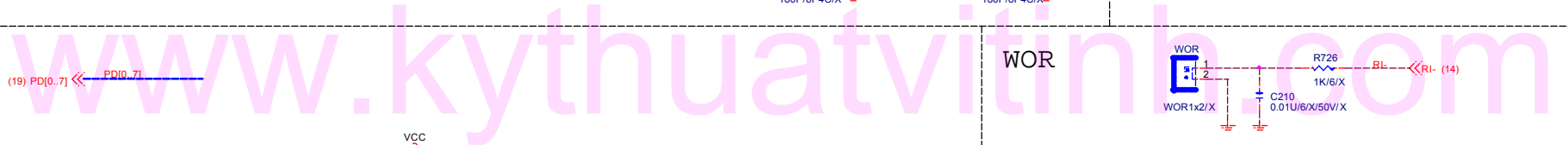
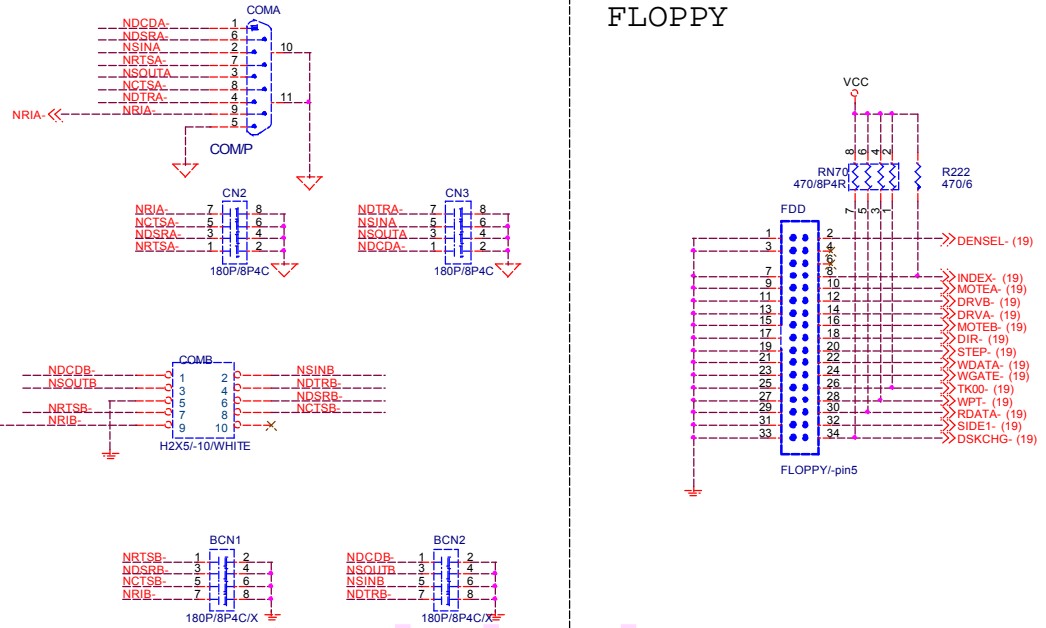


GIGABYTE		
Title		
<b>KB &amp; PS2 MOUSE &amp; IR</b>		
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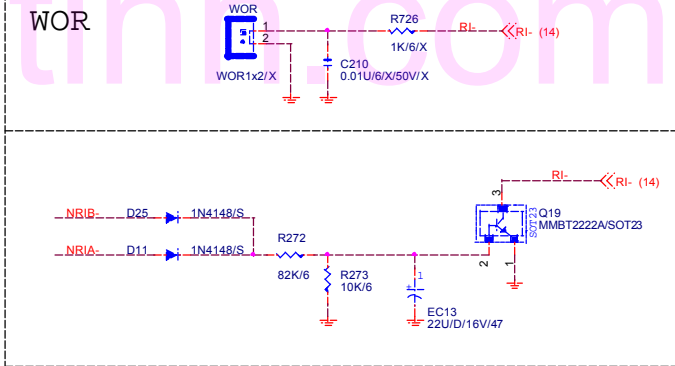
# COMA



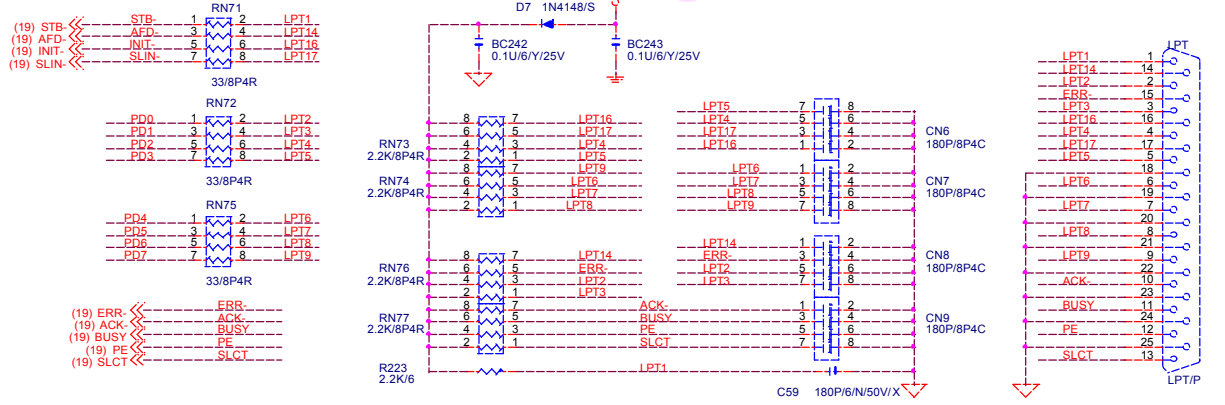
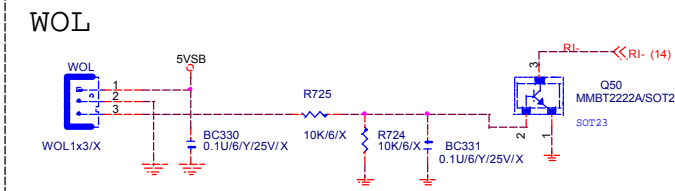
# FLOPPY



# WOR

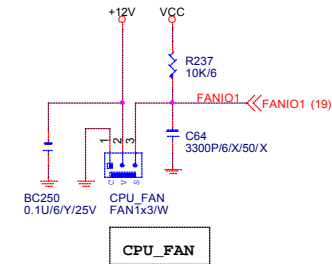
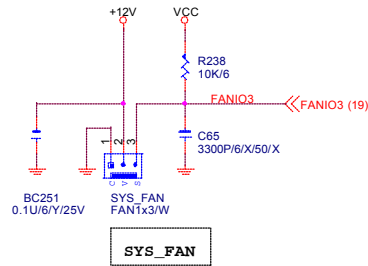
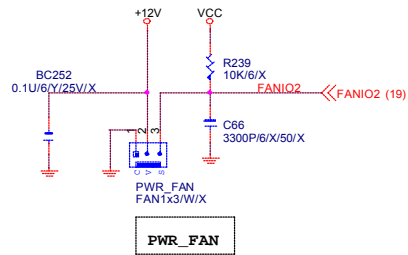
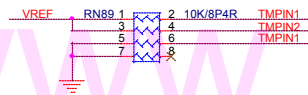
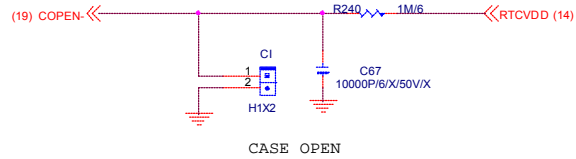
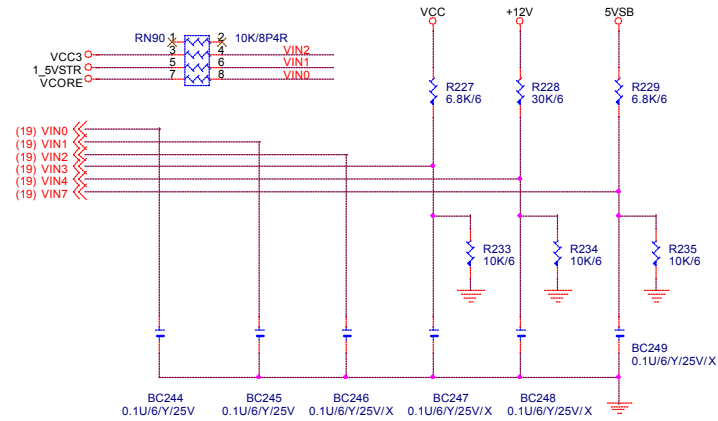
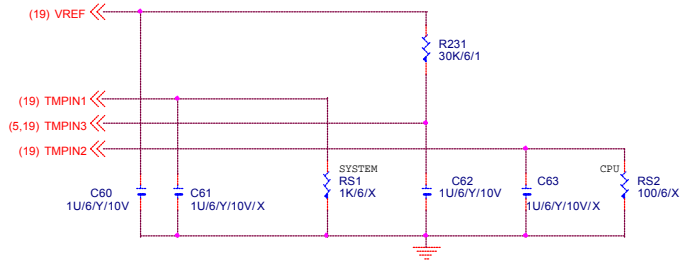


# WOL



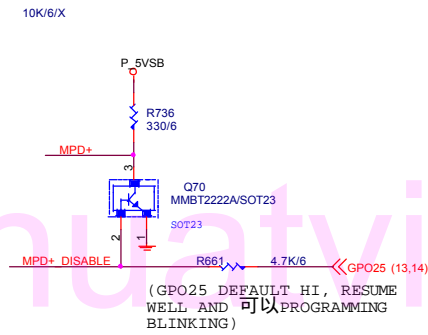
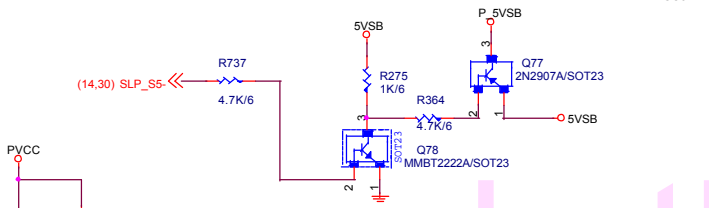
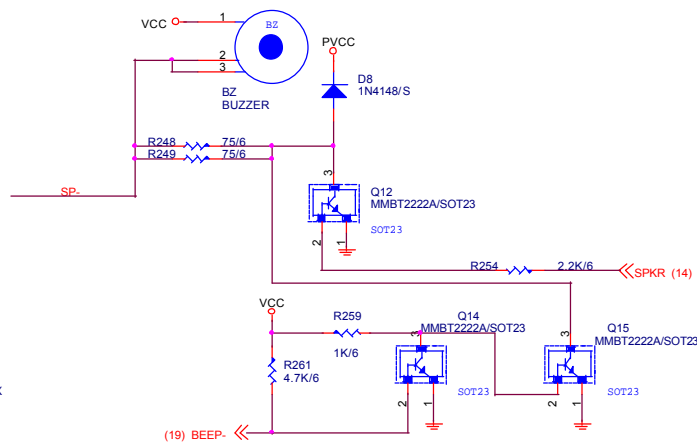
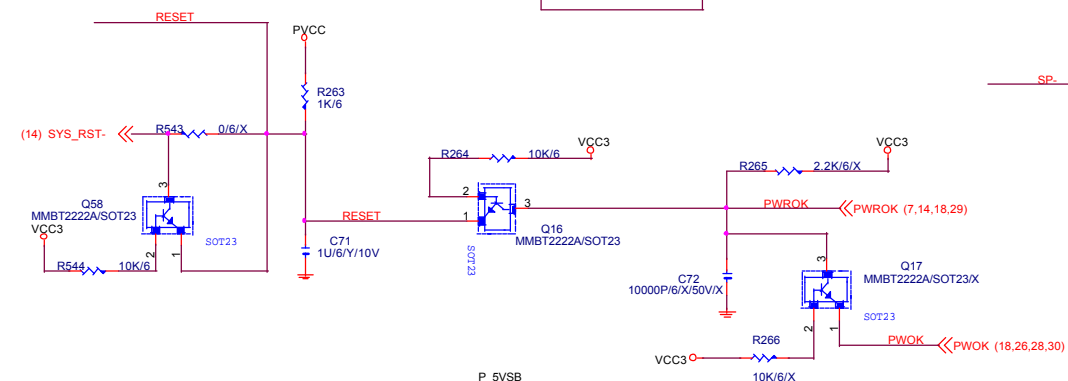
GIGABYTE			
Title <b>COM &amp; WOR &amp; WOL &amp; LPT PORT &amp; FLOOPY</b>			
Size B	Document Number	<b>GA-8LD533</b>	Rev <b>1.0</b>
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# Hardware Monitor circuits

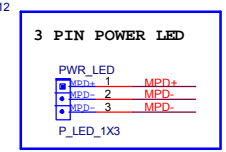
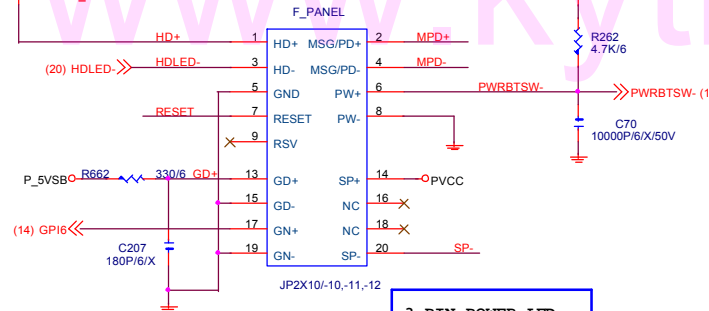


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GIGABYTE	
Title	
FAN/ HW MONITOR	
Size B	Document Number
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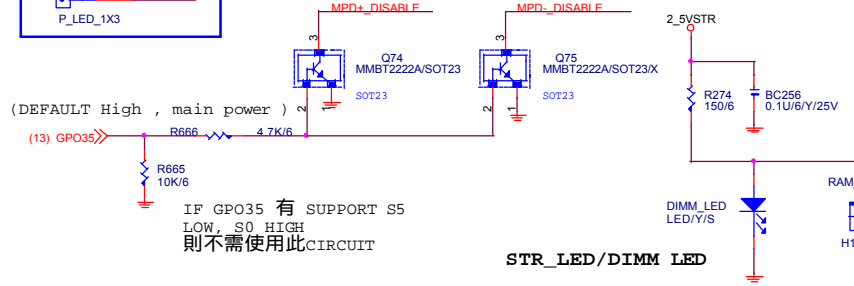
**INTEL FRONT PANEL**



(GPO28 DEFAULT HIGH, RESUME WELL)  
States for green LED

LED States	ACPI States	GPO28
ON	S1, S3	0
OFF	S0, S5	1

IF GPO35 有 SUPPORT S5  
LOW, S0 HIGH  
則不需使用此CIRCUIT



STR\_LED/DIMM\_LED

States for a single-color power LED

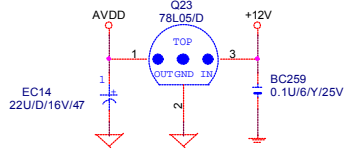
LED States	ACPI States	GPO25	GPO27	GPO35
OFF	S1, S3, S5	1	1	N01
Steady Green	S0	0	1	0
Blinking Green	S0(message waiting	0	B	0

N01 GPO35 只需在  
S1 PROGRAMMING  
LOW

States for a dual-color power LED

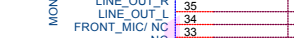
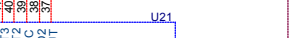
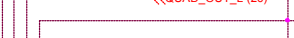
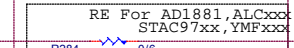
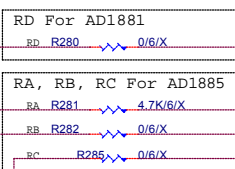
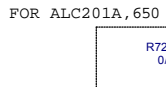
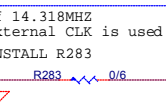
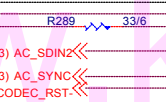
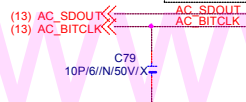
LED States	ACPI States	GPO25	GPO27	GPO35
OFF	S5	1	1	X
Steady Green	S0	0	1	0
Blinking Green	S0(message waiting	0	B	0
Steady Yellow	S1, S3	1	0	N01
Blinking Yellow	S1, S3(message waiting)	1	B	N01

AVDD

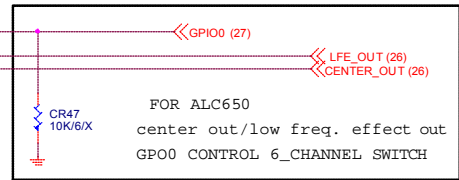


FOR 101 DEFAULT  
FOR 650 DESIGN DEFAULT 由  
CLOCK GEN 来

FOR 650 DESIGN DEFAULT  
不上 CRYSTAL



FOR ALC650 C850要上

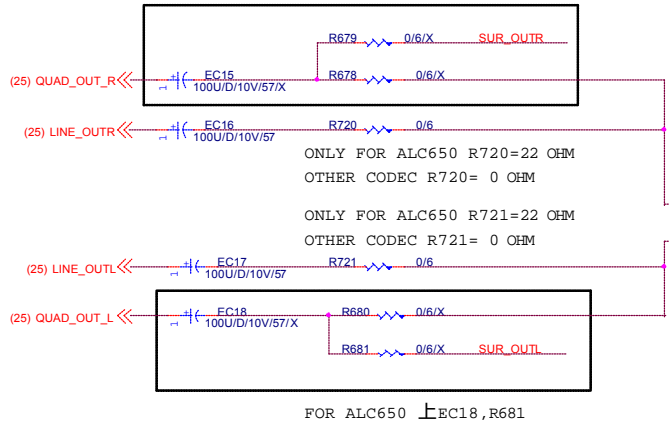


FOR ALC650  
center out/low freq. effect out  
GPO0 CONTROL 6\_CHANNEL SWITCH

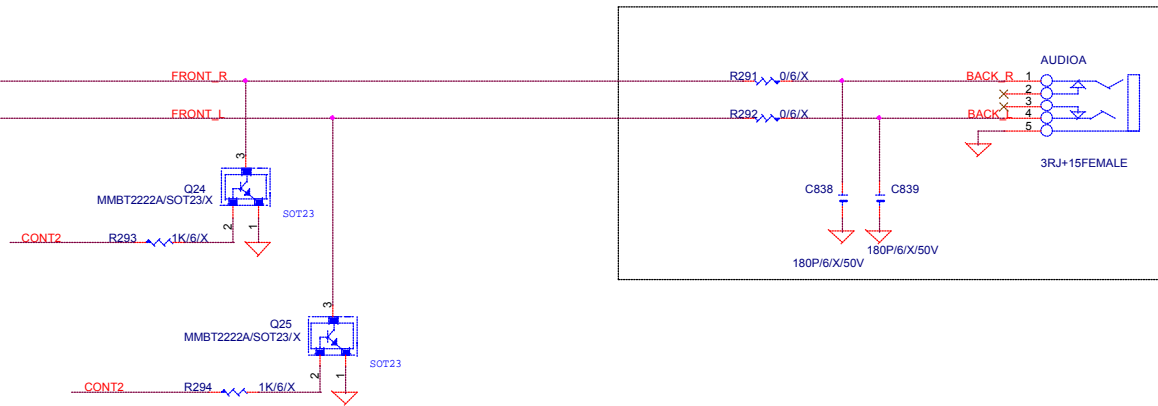
FOR ALC650  
surround out left/right  
channel

GIGABYTE			
Title			
AC97 CODEC			
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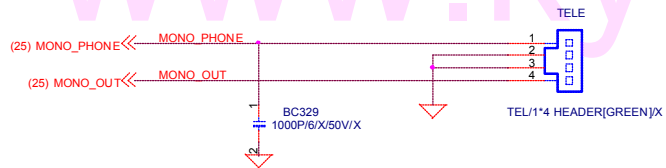
FOR ALC650  $\uparrow$  EC15, R679



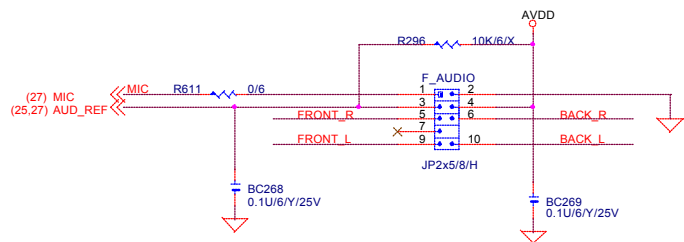
### LINE-OUT



### TELE

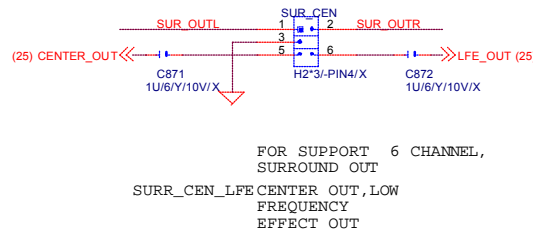


### INTEL FRONT AUDIO



### ANTI-POP

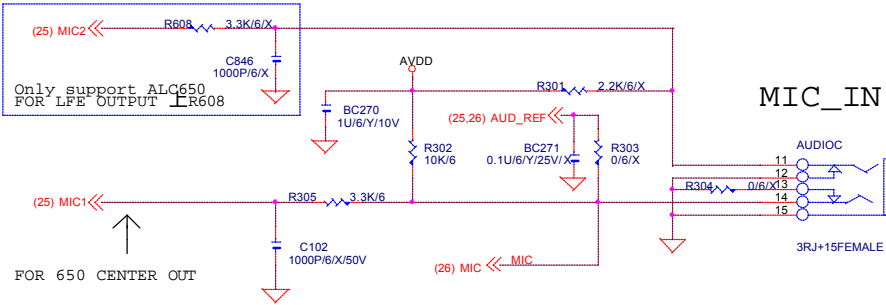
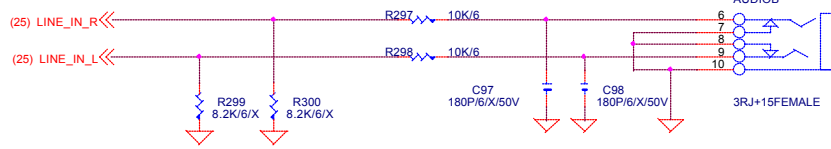
DEFAULT NO POP



GIGABYTE

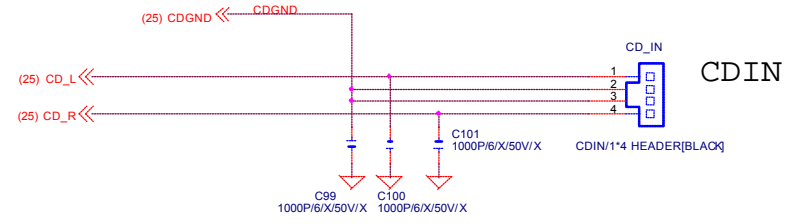
Title			LJACK LINE OUT
Size B	Document Number	GA-8LD533	
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### LINE-IN

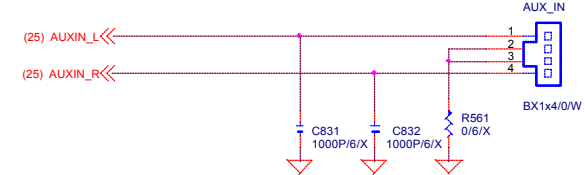


FOR 650 CENTER OUT

### MIC\_IN



### CDIN

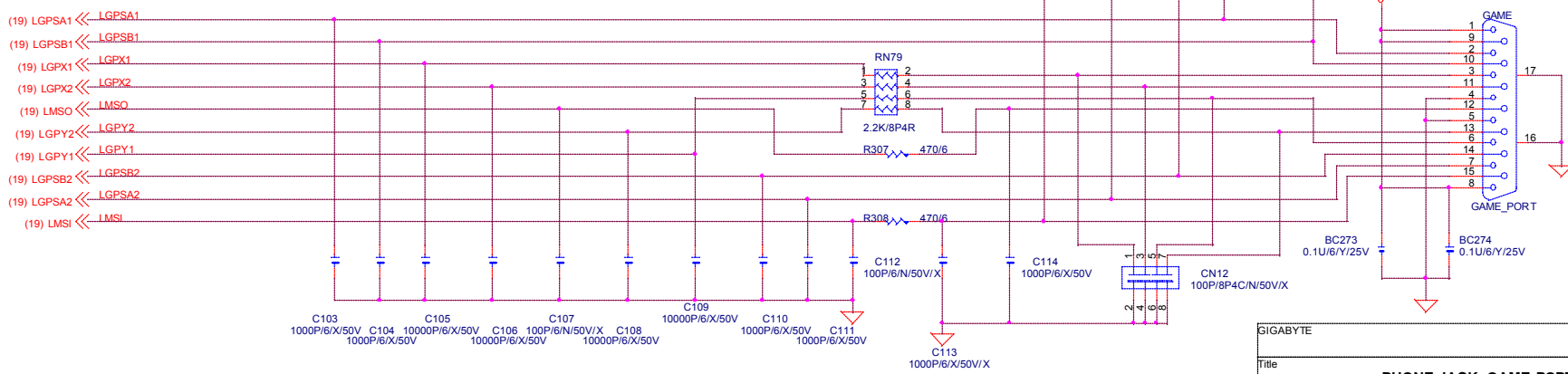


### AUX\_IN

### SPDIF

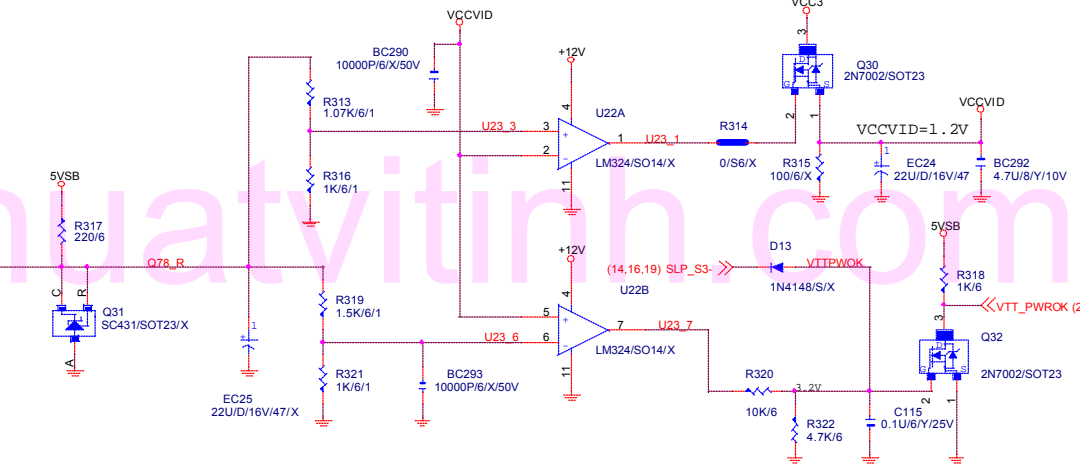
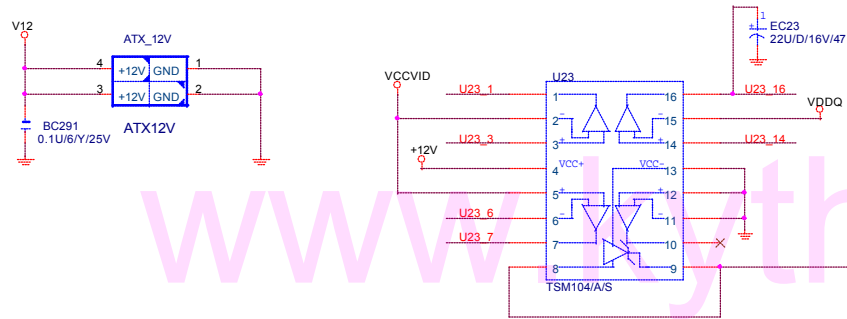
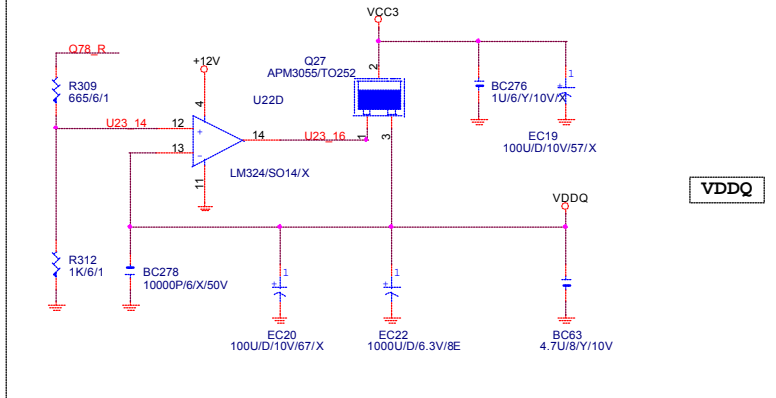
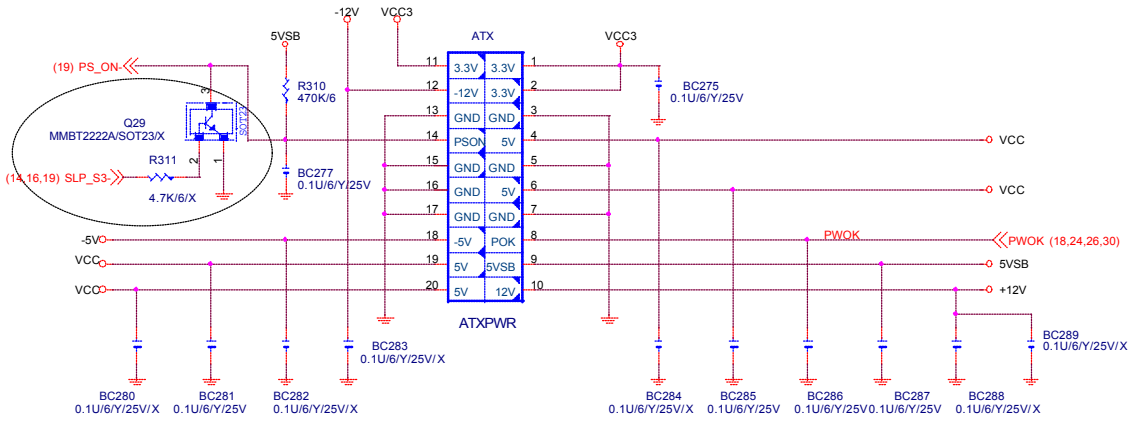


### ITE GAME\_PORT



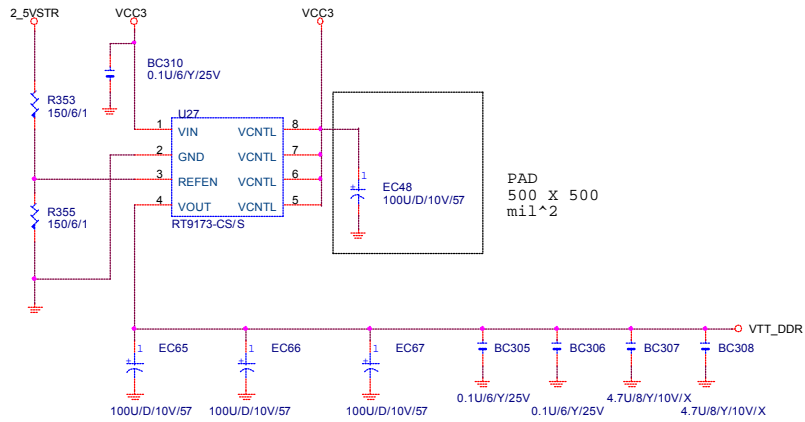
GIGABYTE		
Title <b>PHONE JACK, GAME PORT</b>		
Size B	Document Number <b>GA-8LD533</b>	Rev <b>1.0</b>
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### ATX POWER CONNECTOR

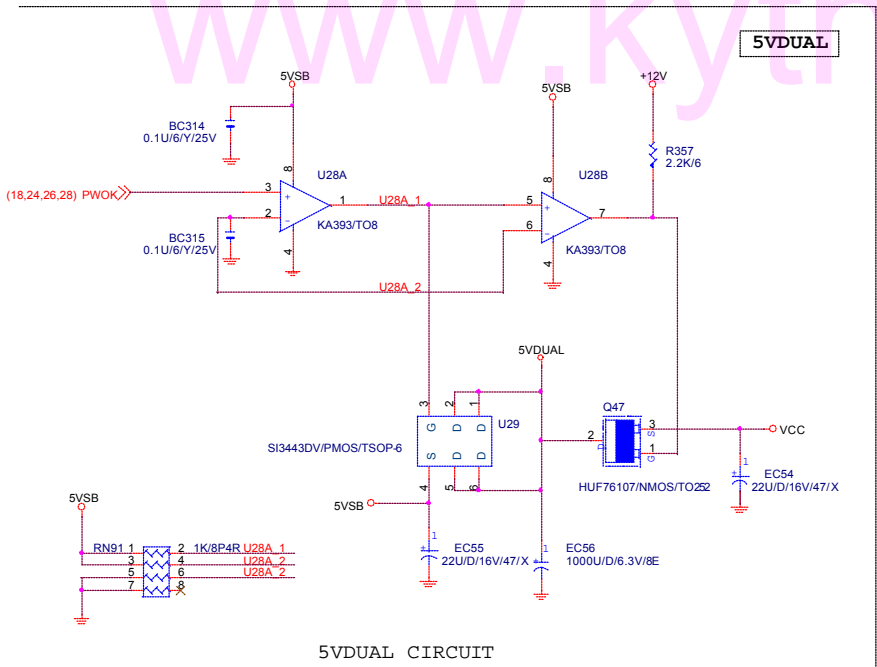




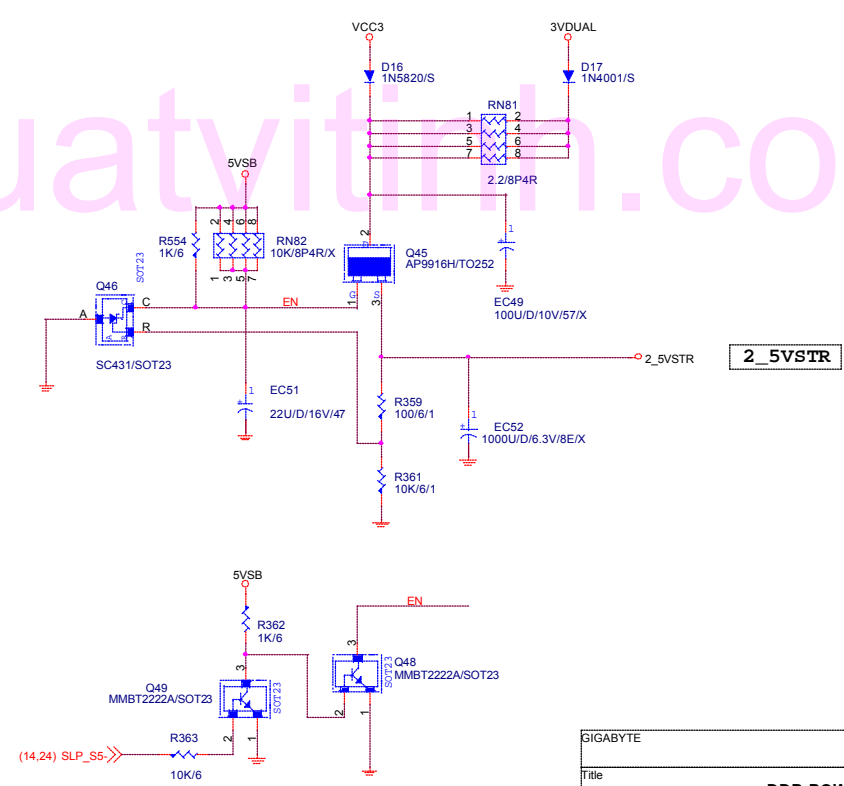
1.25V VTT\_DDR LINEAR SOLUTION



VTT\_DDR



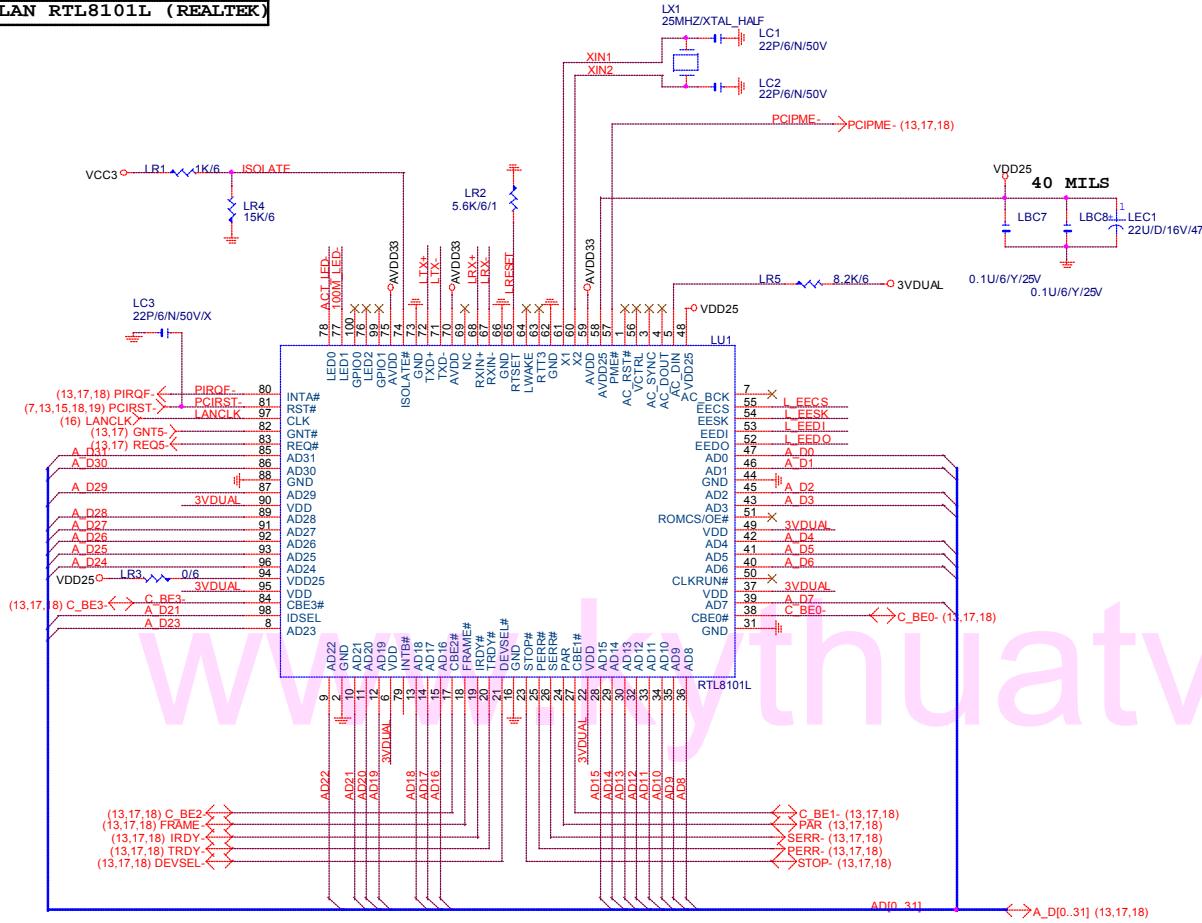
5VDUAL CIRCUIT



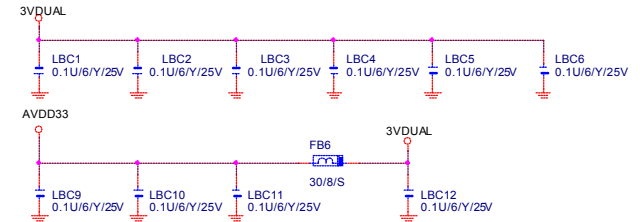
2\_5VSTR

GIGABYTE		
Title		
<b>DDR POWER</b>		
Size B	Document Number	Rev
	<b>GA-8LD533</b>	<b>1.0</b>
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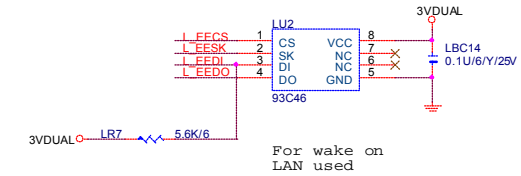
**LAN RTL8101L (REALTEK)**



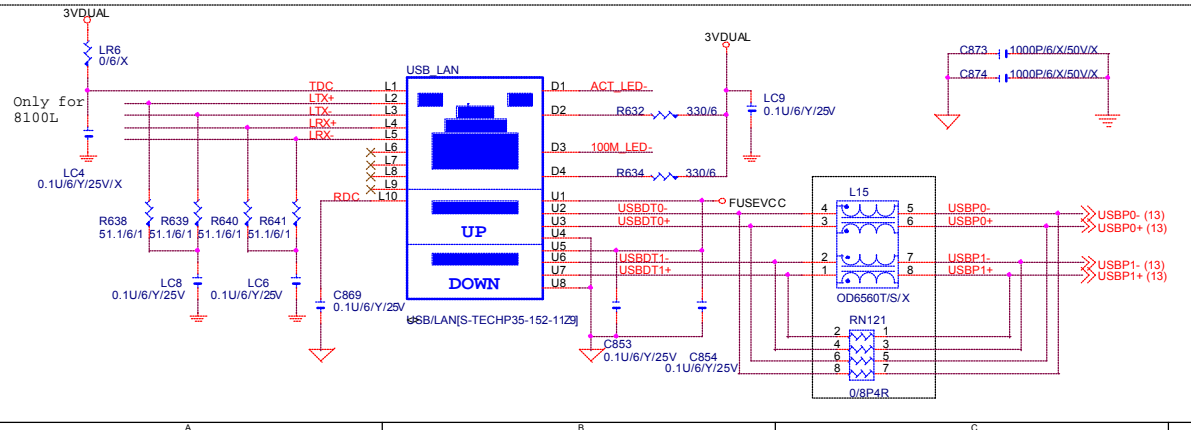
**POWER DECOUPLING CAP.**



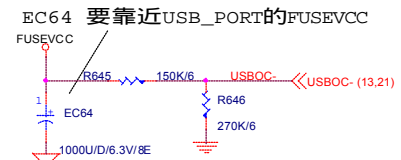
**LAN EEPROM**



**8101L NOTE:**



**模組化線路**



GIGABYTE CORP.		
Title	LAN RTL8101L	
Size	Document Number	Rev
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# GIGABYTE GA-8LD533 GPIO LIST

Revision 1.0

SHEET

TITLE

GPI		
PIRQB-		PULL 8.2K TO VCC3
PIRQD-		PULL 8.2K TO VCC3
PIRQE-		PULL 8.2K TO VCC3
PIRQH-		PULL 8.2K TO VCC3
GPI6		PULL 8.2K TO VCC3 (GREEN_BUTTON)
GPI7		NOT IMPLEMENTED
GPI8		PULL 8.2K TO 3VDUAL, LPC PME.
GPI9	NA	NOT IMPLEMENTED
GPI10	NA	NOT IMPLEMENTED
GPI11		PULL 4.7K TO 3VDUAL (SMBALERT)
GPI12		PULL DOWN 10K.
GPI13		PULL DOWN 10K, CNR_PRIMARY
GPI14	NA	NOT IMPLEMENTED
GPI15	NA	NOT IMPLEMENTED

SHEET

TITLE

GPO		
GPO18		PULL 8.2K TO VCC3
GPO19		PULL 8.2K TO VCC3
GPO20		PULL 8.2K TO VCC3
GPO21		PULL 8.2K TO VCC3
GPO22		PULL 8.2K TO VCC3
GPO23		PULL 8.2K TO VCC3
GPO24		PULL 1K TO 3VDUAL (TOP BLOCK)
GPO25		PULL 4.7K TO 3VDUAL, BIOS WRITE PROTECT.
GPO26		NOT IMPLEMENTED
GPO27		PULL 8.2K TO 3VDUAL, LAN 100/10 DETECT.
GPO28		PULL 8.2K TO 3VDUAL

<b>GIGABYTE</b>		
Title		
GPIO LIST		
Size	Document Number	Rev
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# GIGABYTE GA-8LD533 PCI ROUNTING LIST

Revision 1.0

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT
PCI SLOT1	16	C,F,G,A	PCLK1	REQ0-	GNT0-
PCI SLOT2	17	F,G,A,C	PCLK2	REQ1-	GNT1-
PCI SLOT3	18	G,A,C,F	PCLK3	REQ2-	GNT2-
	19				
	20				
	21				
	26				
	28				
	23				
	NA				

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<b>GIGABYTE</b>		
Title <b>PCI ROUNT LIST</b>		
Size Custom	Document Number <b>GA-8LD533</b>	Rev <b>1.0</b>
Date: Tuesday, November 26, 2002	Sheet 33	of 33