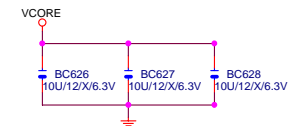
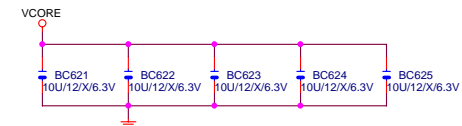
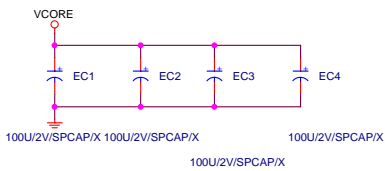


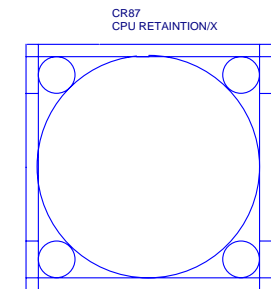
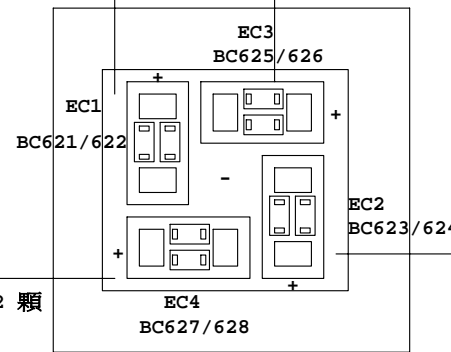
SP-CAP X 4PCS



上100U/2V/SPCAP 上10U/12/X/6.3V X2 顆

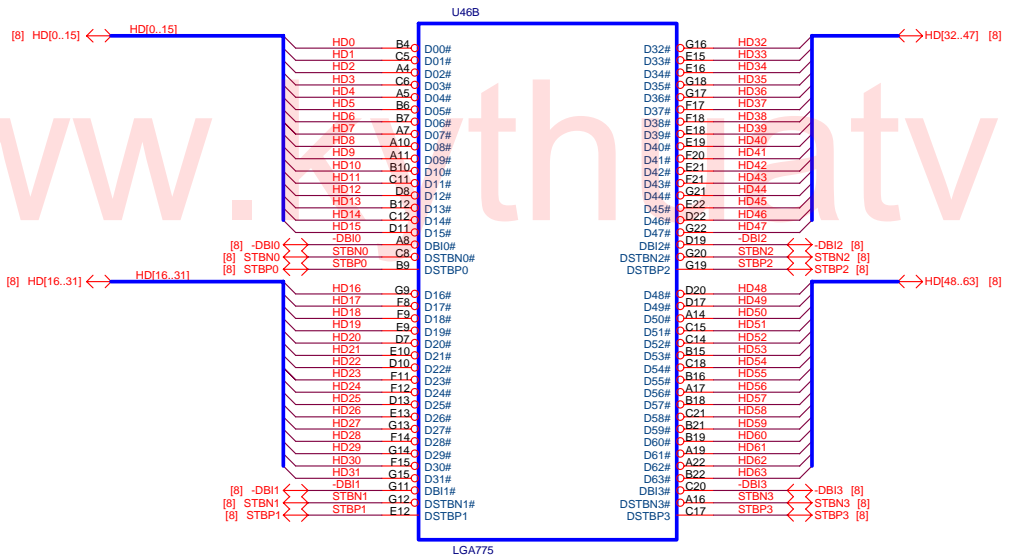
上10U/12/X/6.3V X2 顆

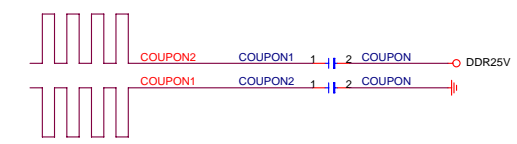
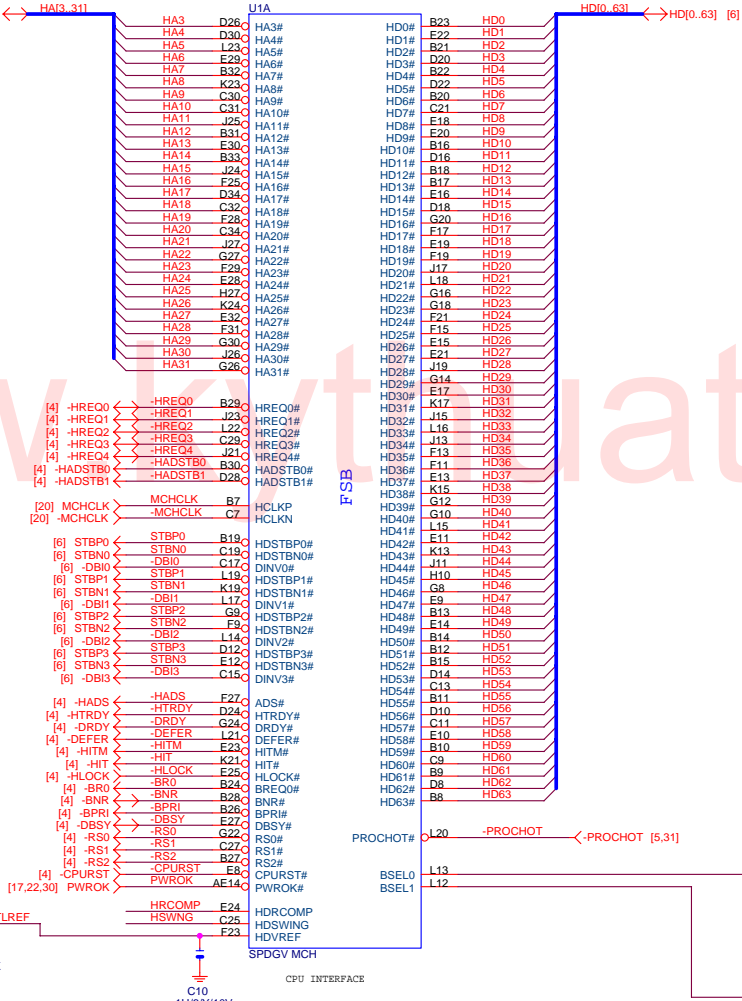
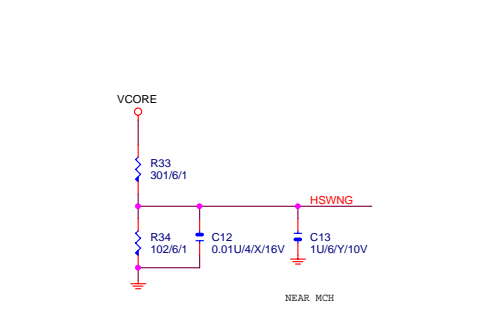
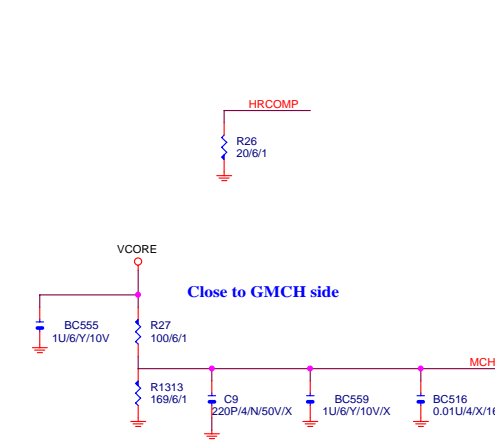
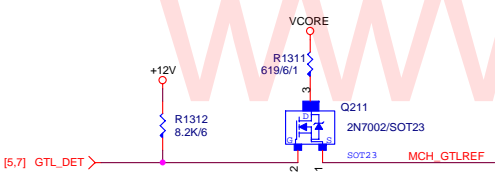
上100U/2V/SPCAP



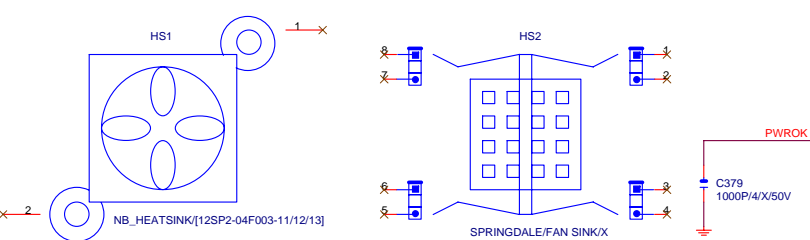
GIGABYTE			
Title P4_LGA775-A			
Size Custom	Document Number	GA-8I865GVM-775 Rev 1.0	
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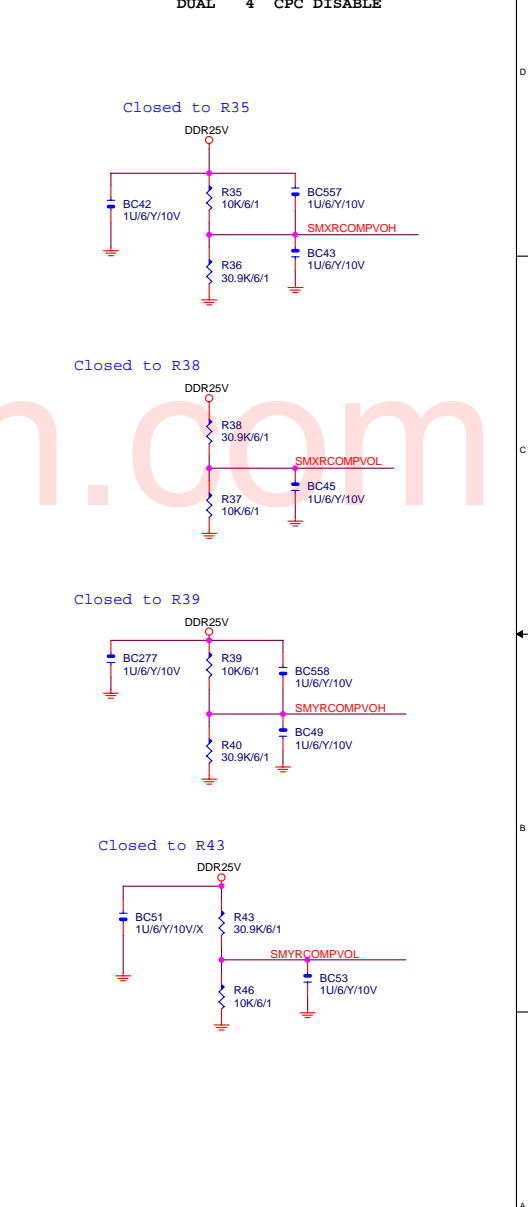
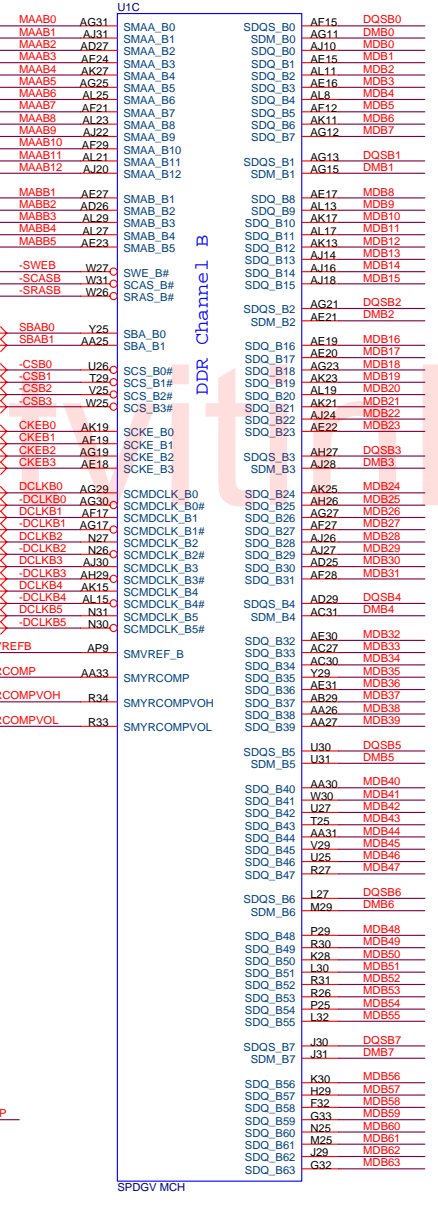
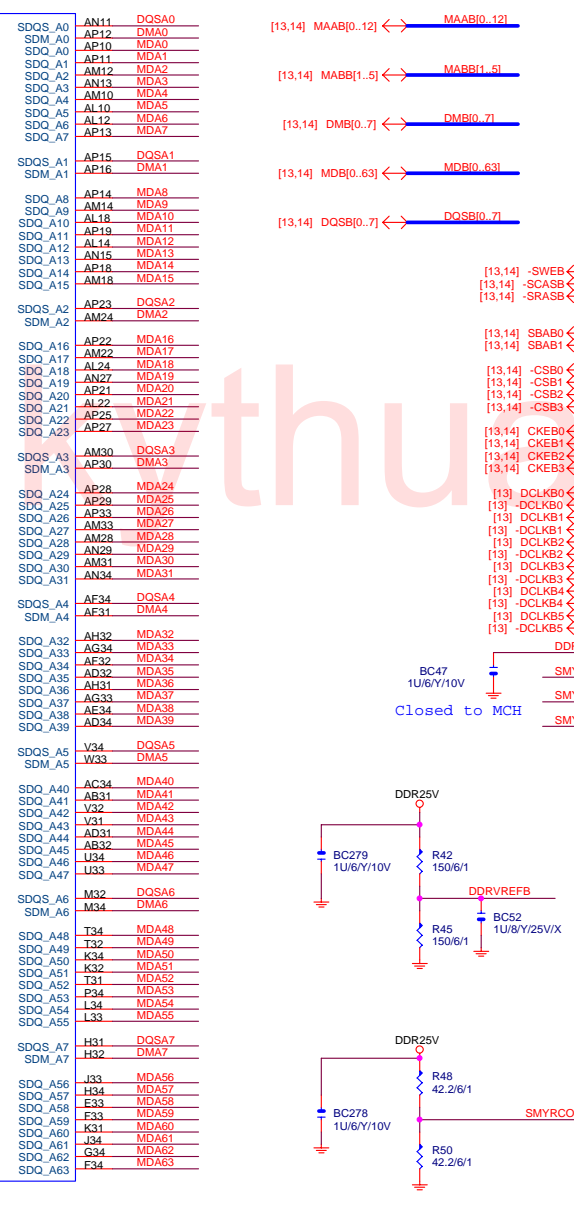
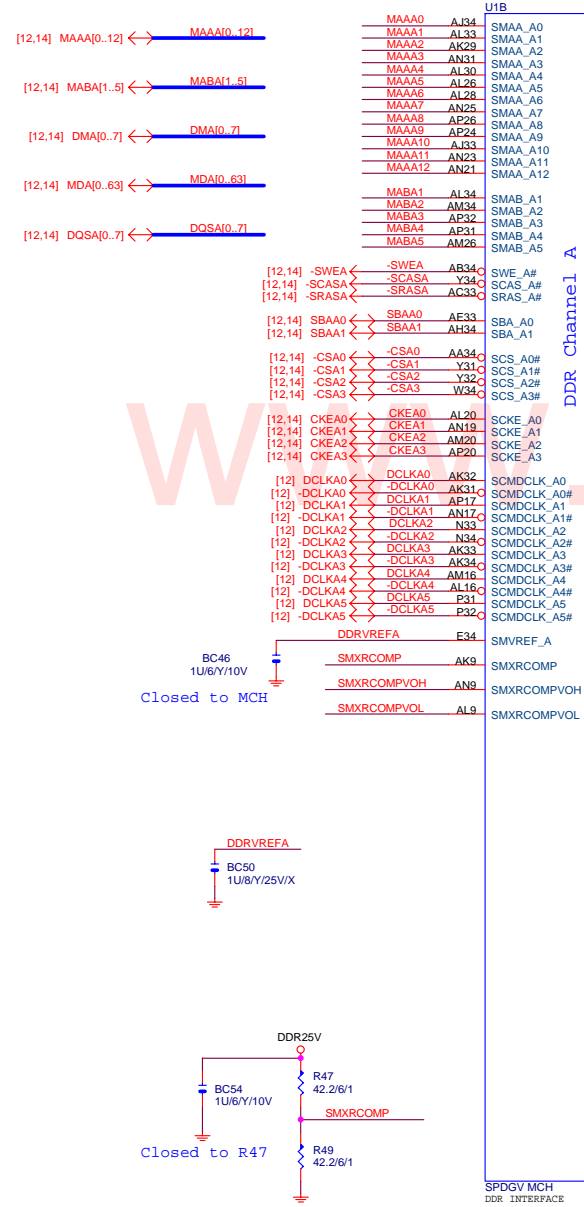


N. B HEATSINK

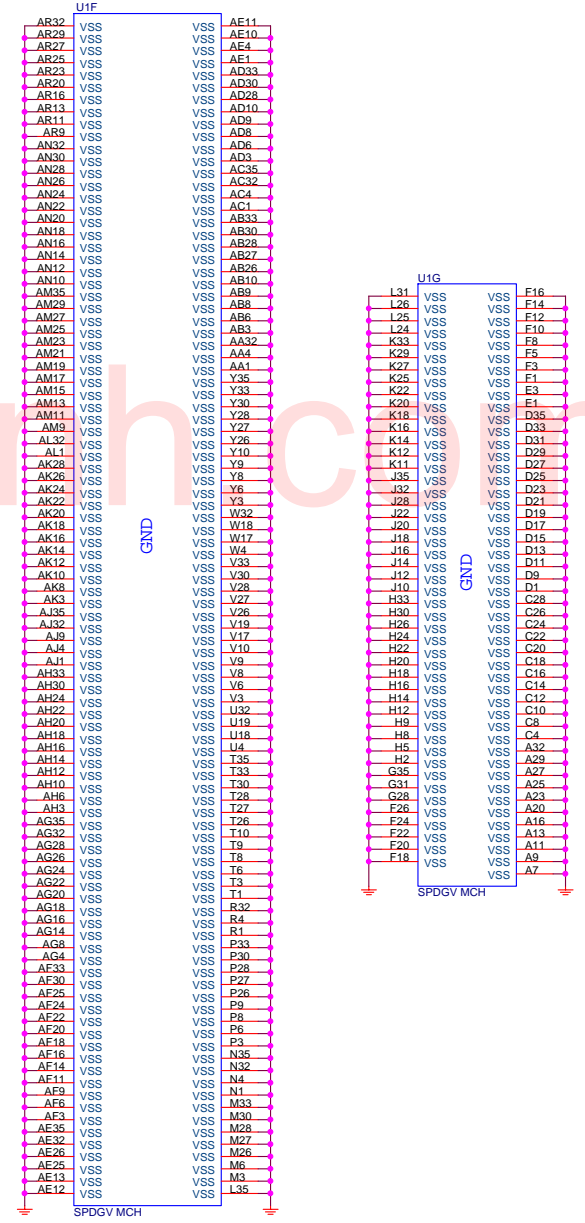
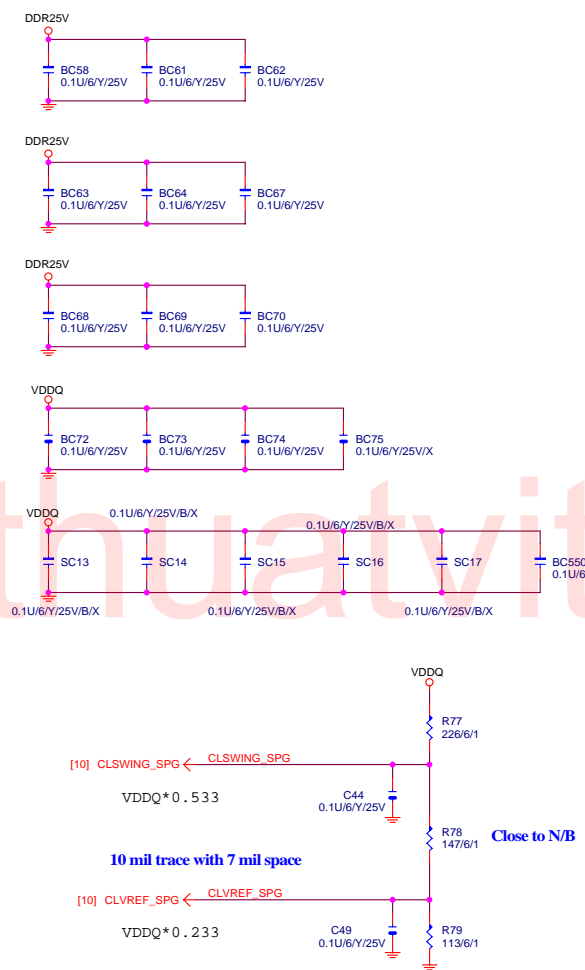
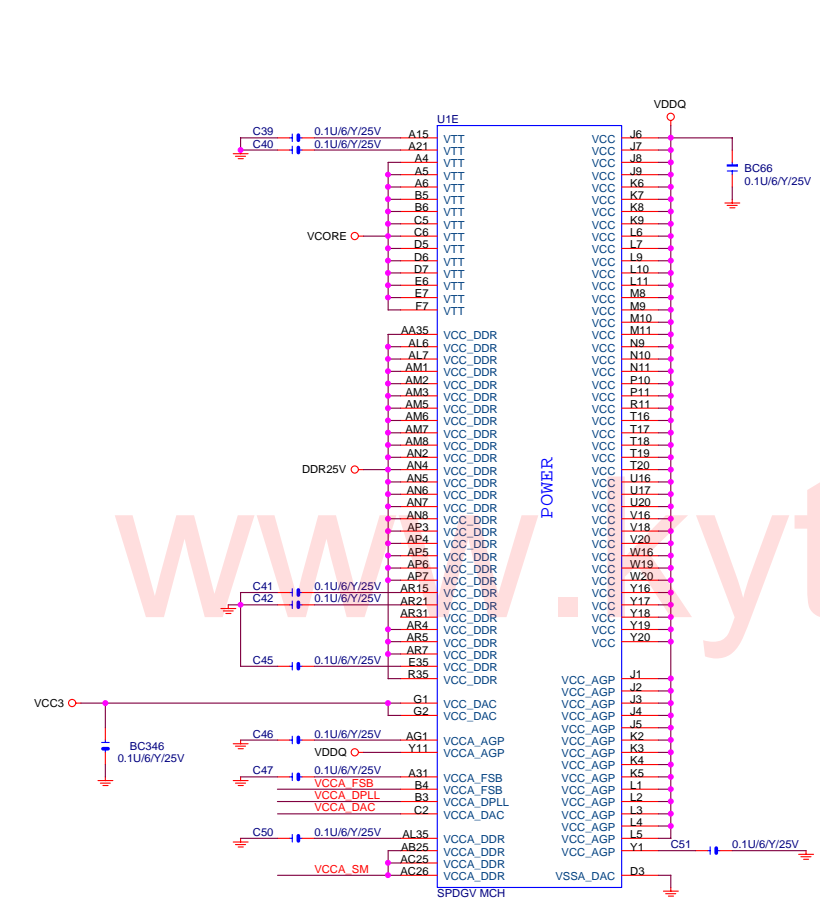


Title			SPRINGDALE HOST		
Size	Document Number		Rev		
Custom	GA-81865GVM-775		1.0		
Date:		Sheet	8	of	38

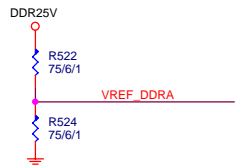
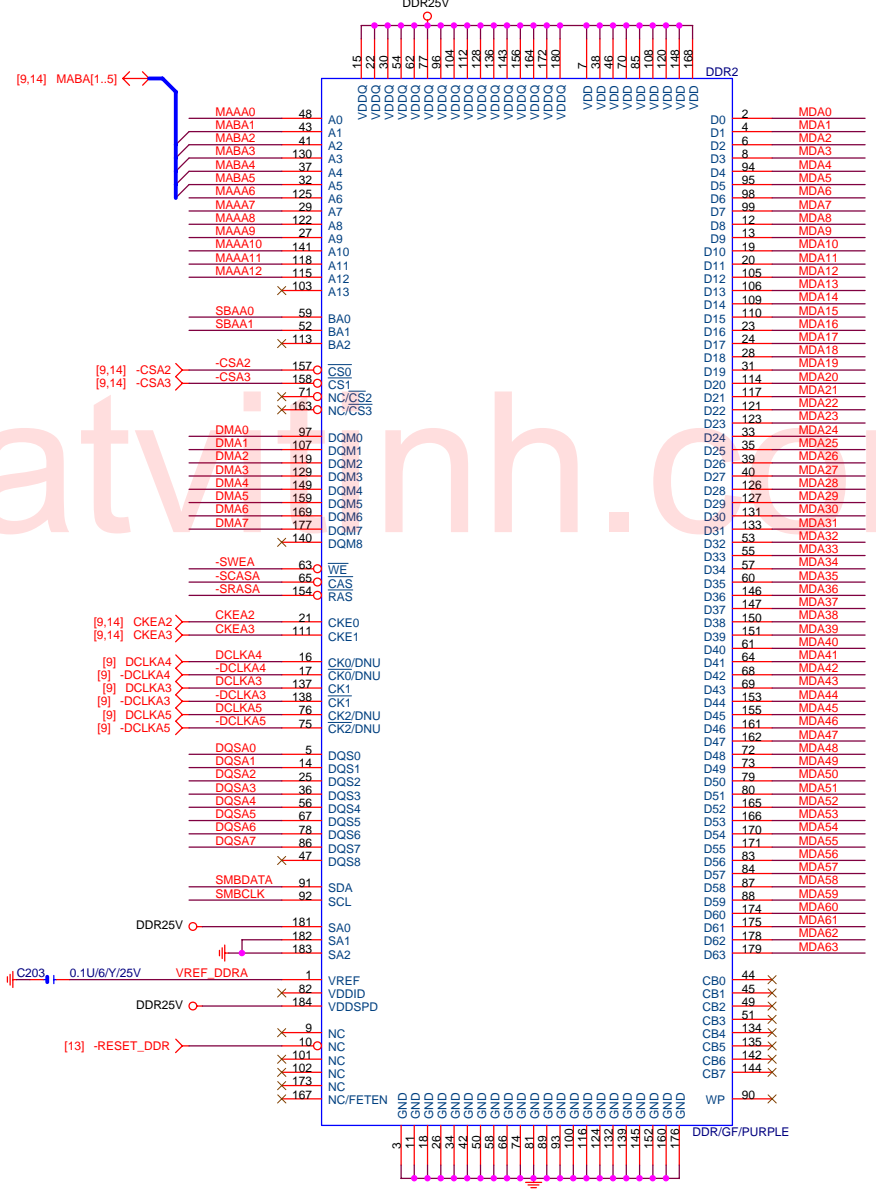
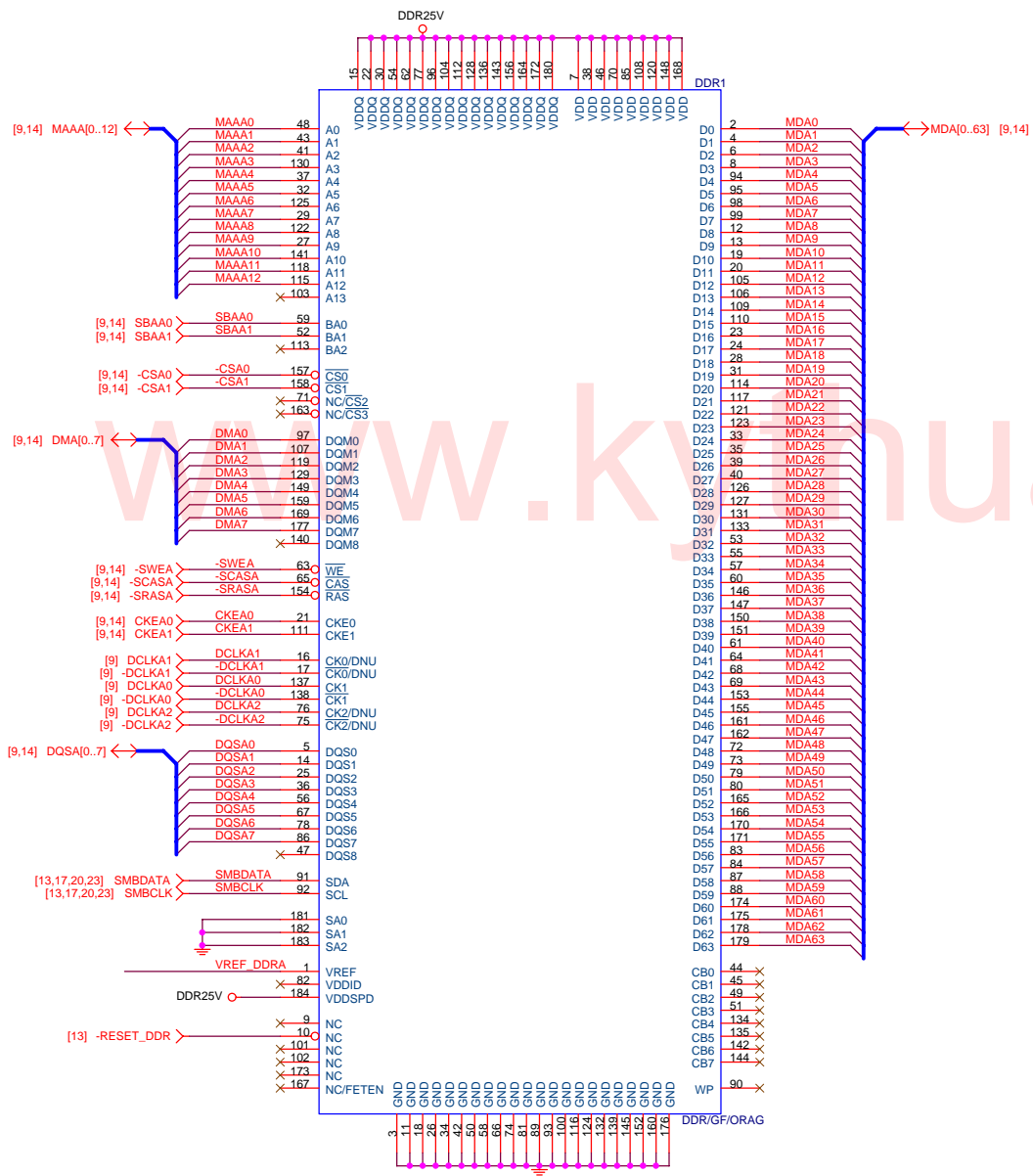
DDR 400 1-2-3-4 CPC DISABLE
 DDR 333 SIGNAL 1 CPC ENABLE
 2 CPC DISABLE
 DUAL 2 CPC ENABLE
 DUAL 4 CPC DISABLE



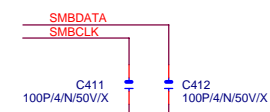
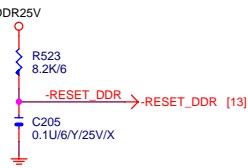
Title			SPRINGDALE DDR		
Size	Document Number		Rev		
Custom	GA-81865GVM-775		1.0		
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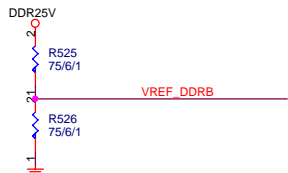
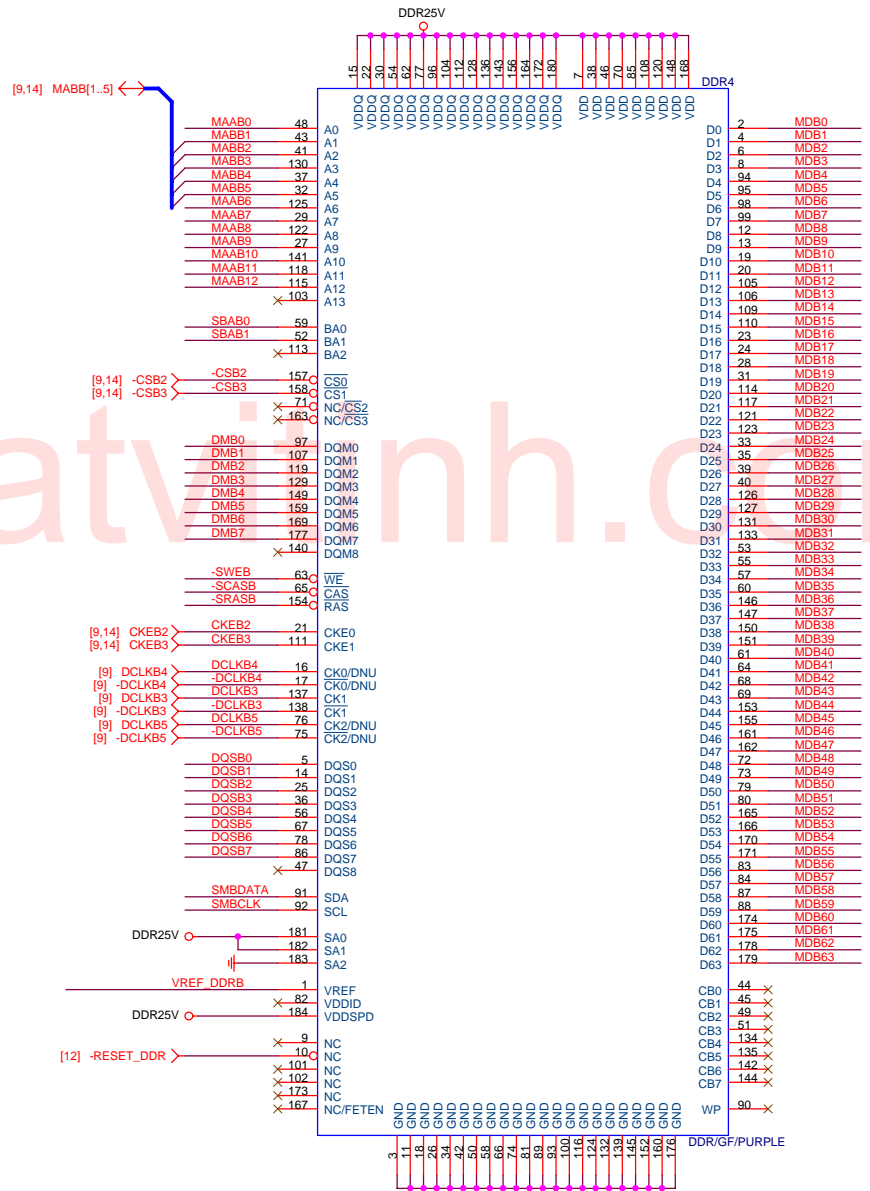
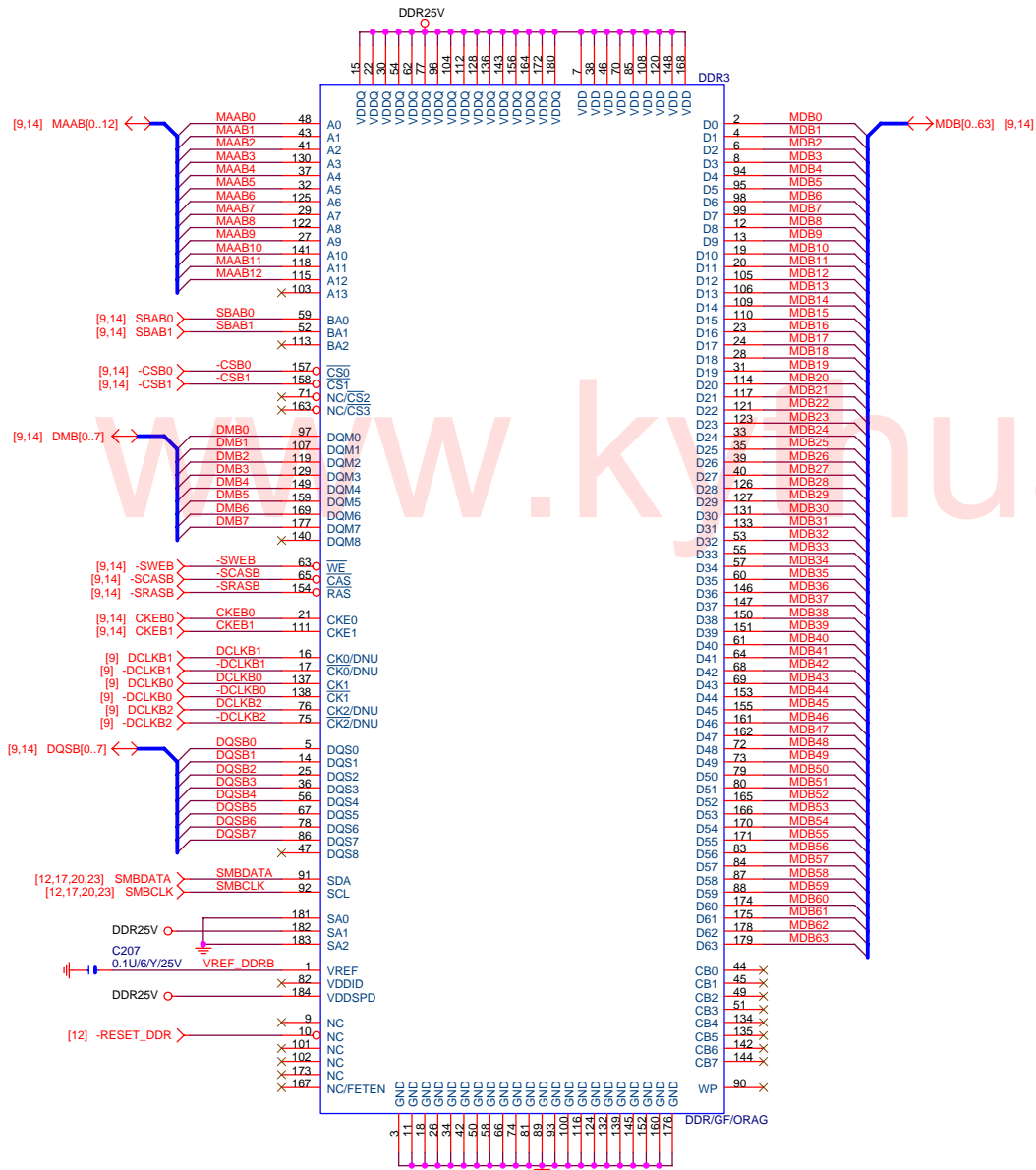
Title			SPRINGDALE PWR		
Size	Document Number		Rev		
Custom	GA-81865GVM-775		1.0		
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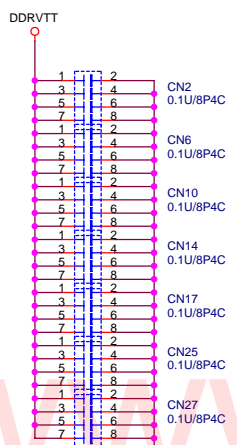
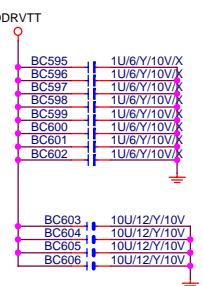
For Register DDR Support



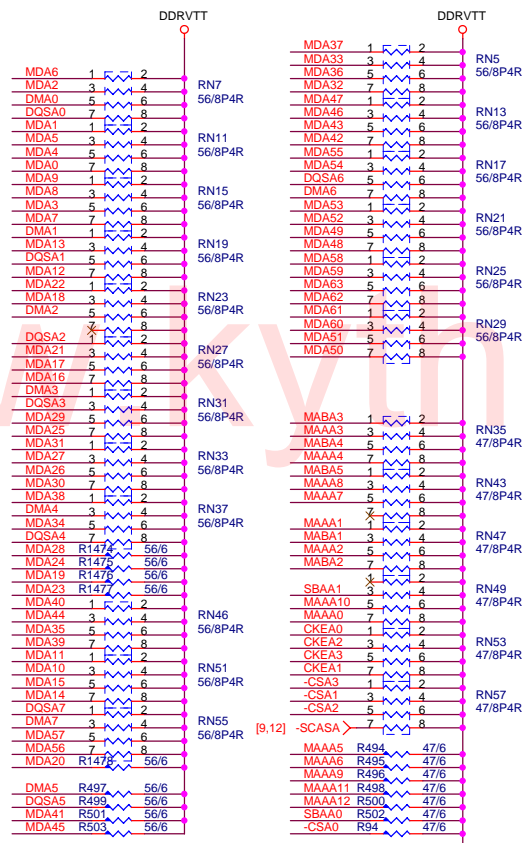
GIGABYTE		
Title		
DDR1,2 CHANNEL A		
Size	Document Number	Rev
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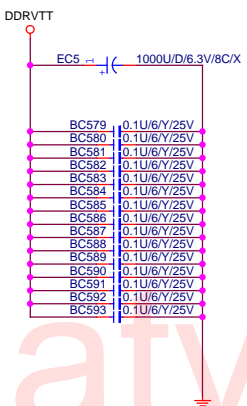
DDRVTT Decouple



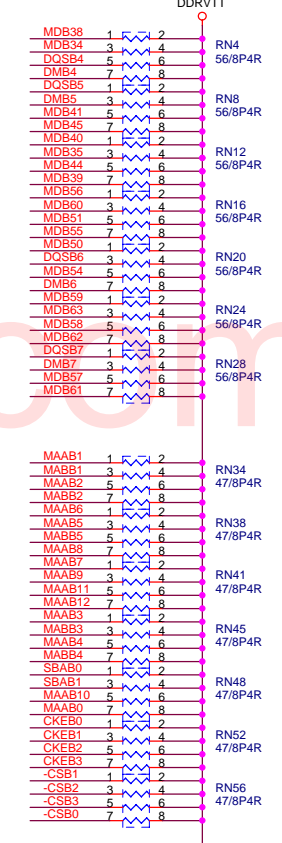
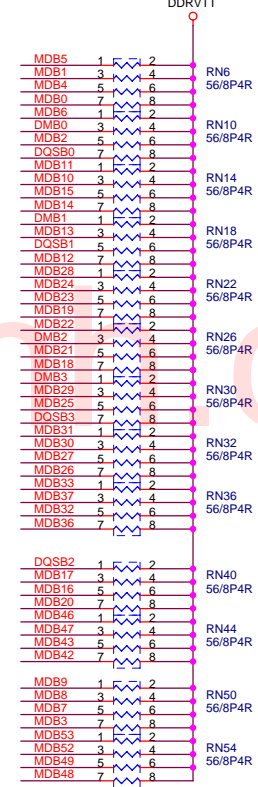
DDR TERMINATION CHANNEL A



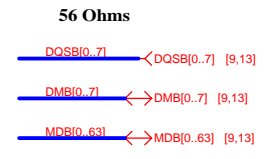
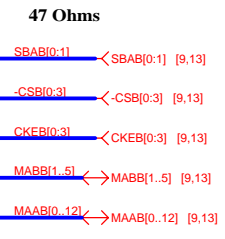
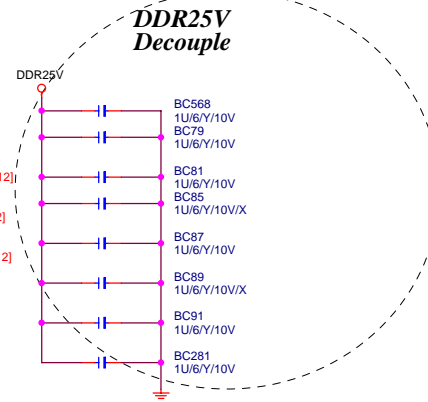
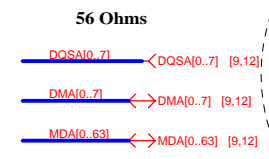
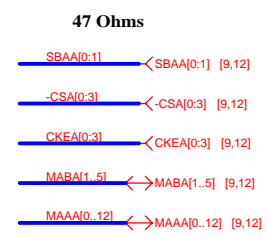
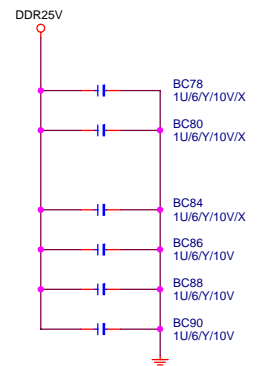
DDRVTT Decouple



DDRVTT Decouple CHANNEL B



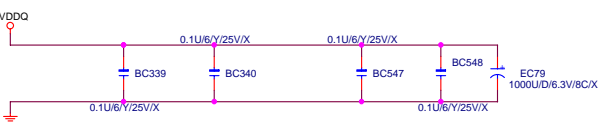
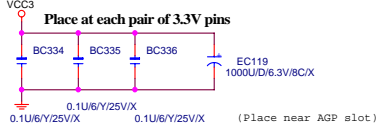
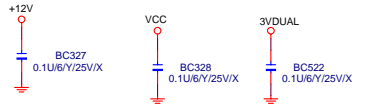
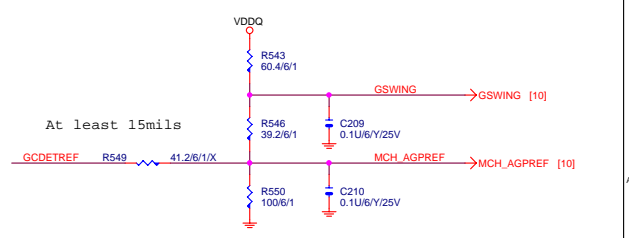
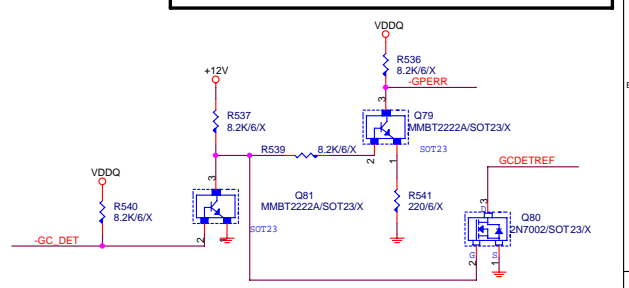
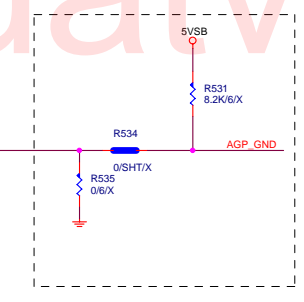
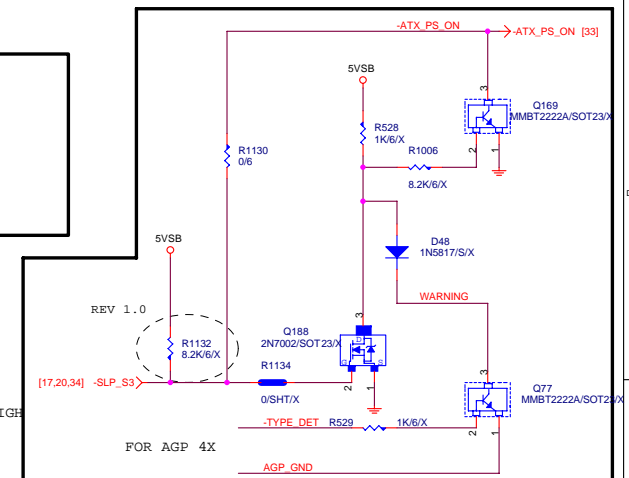
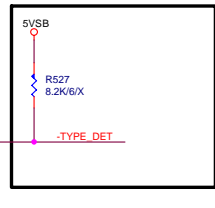
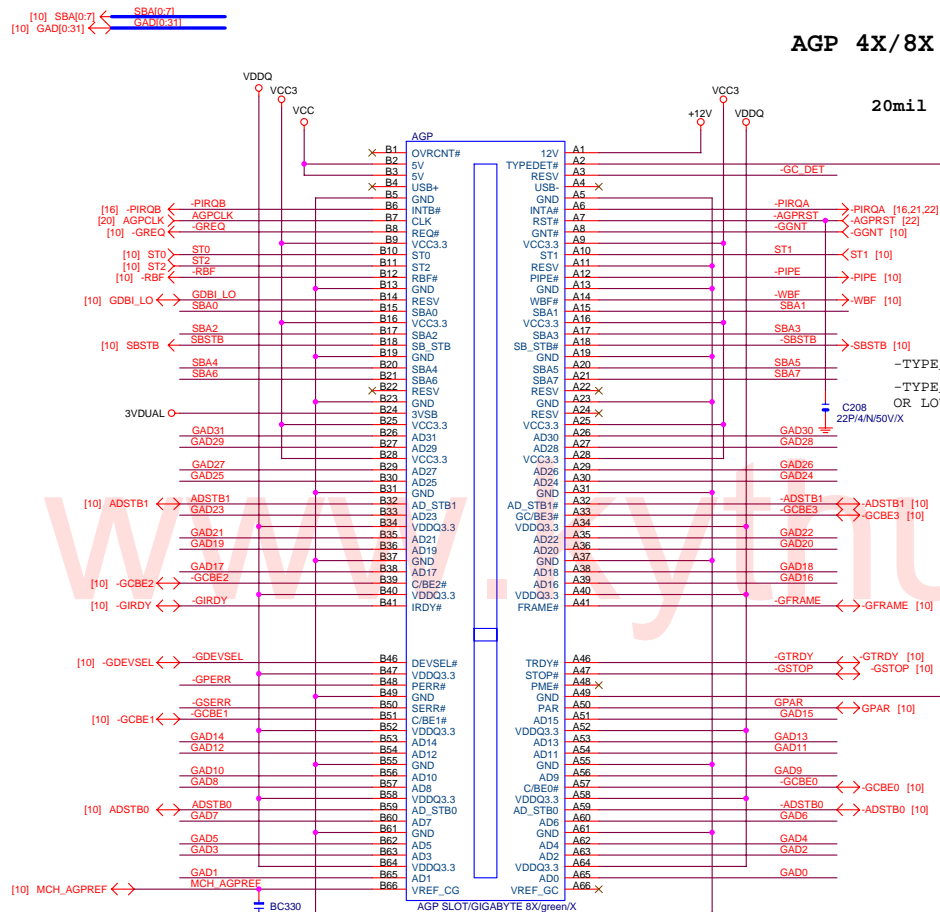
DDR25V Decouple



GIGABYTE			
Title DDR TERMINATION			
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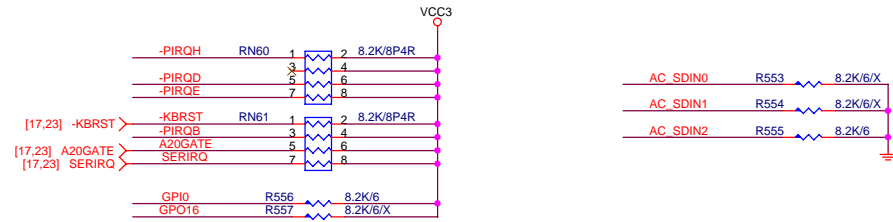
AGP 4X/8X

20mil

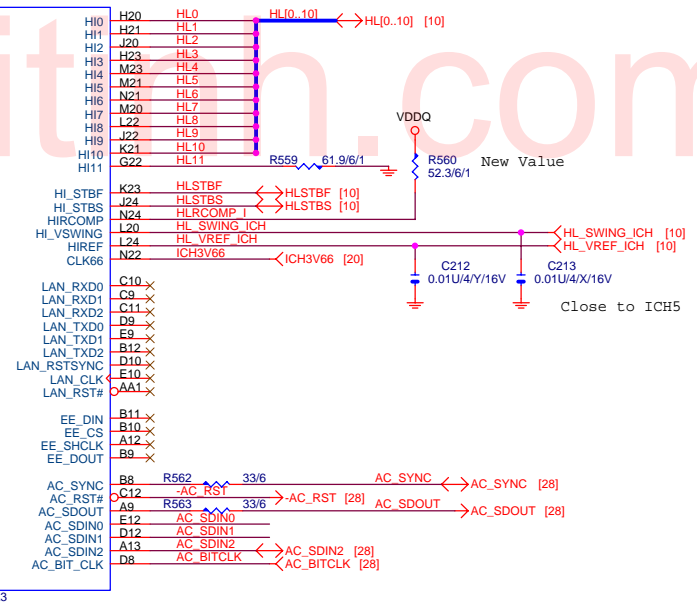
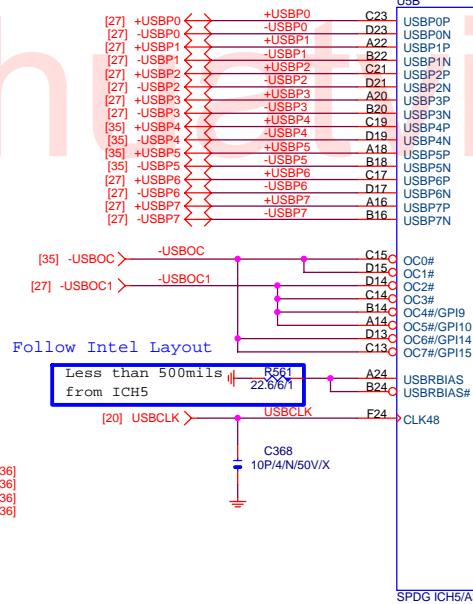
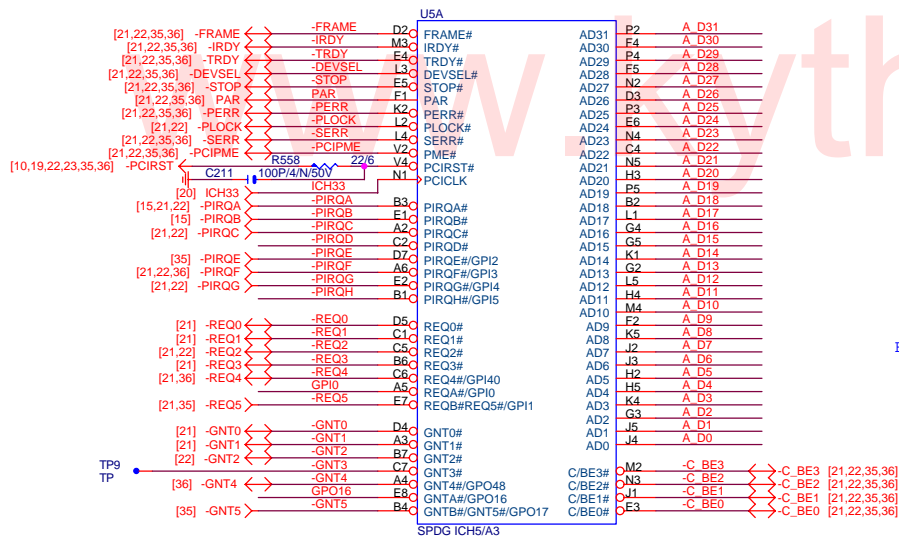


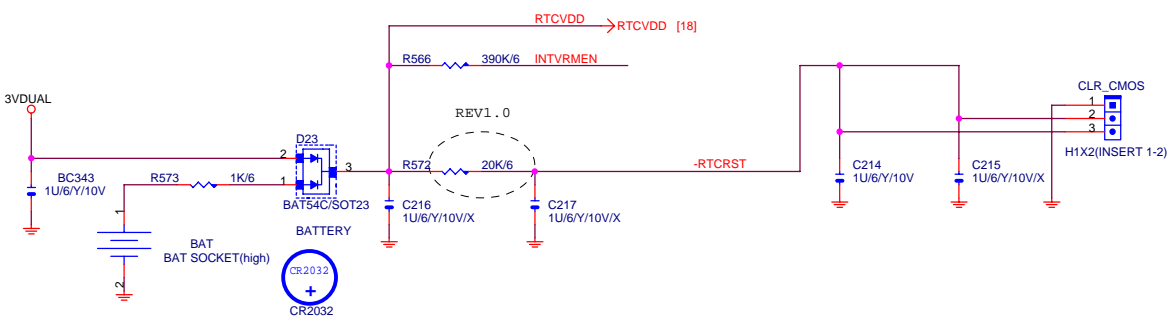
Place 1 at each pair of VDDQ pins
Place an additional for spread from A14 - A33

GIGABYTE		
File		
AGP SLOT		
Size	Document Number	Rev
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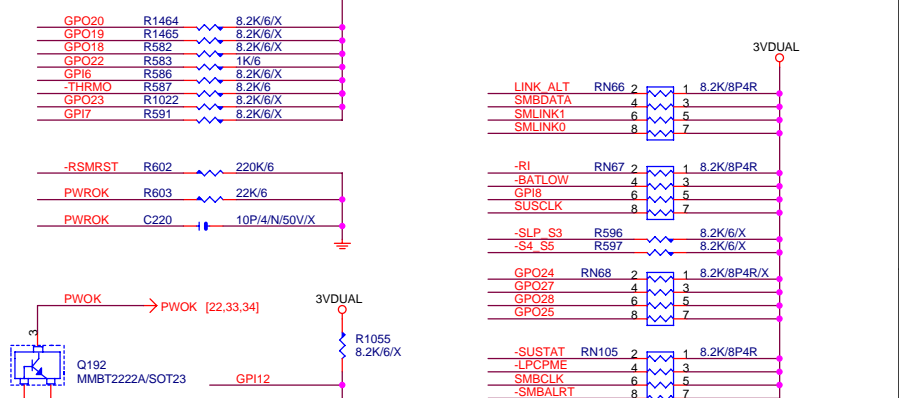
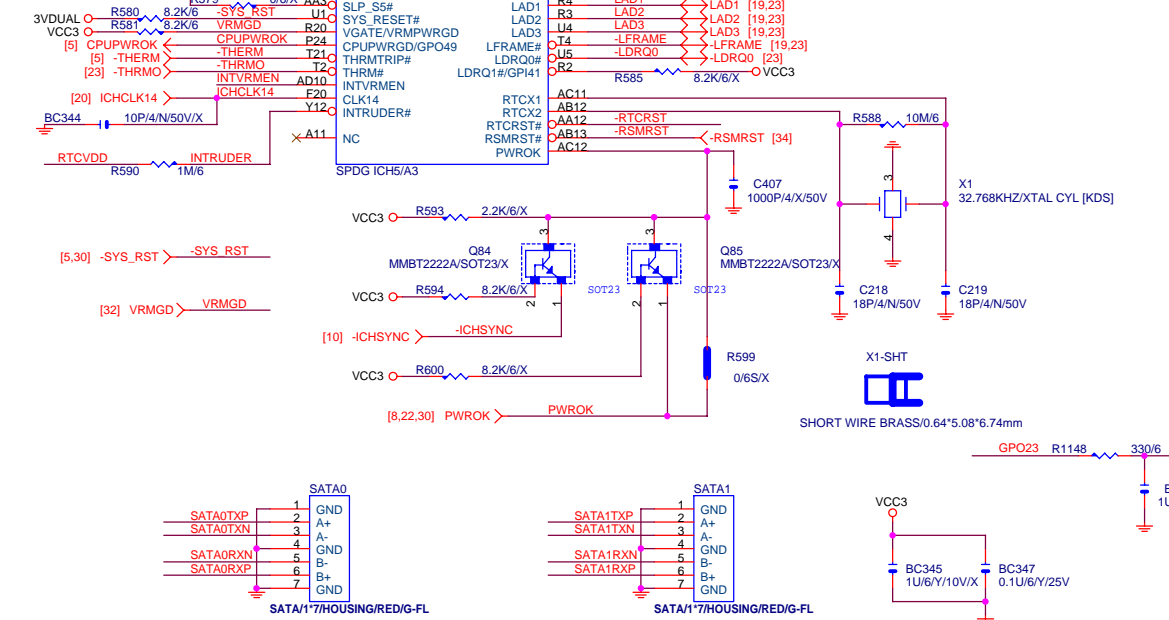
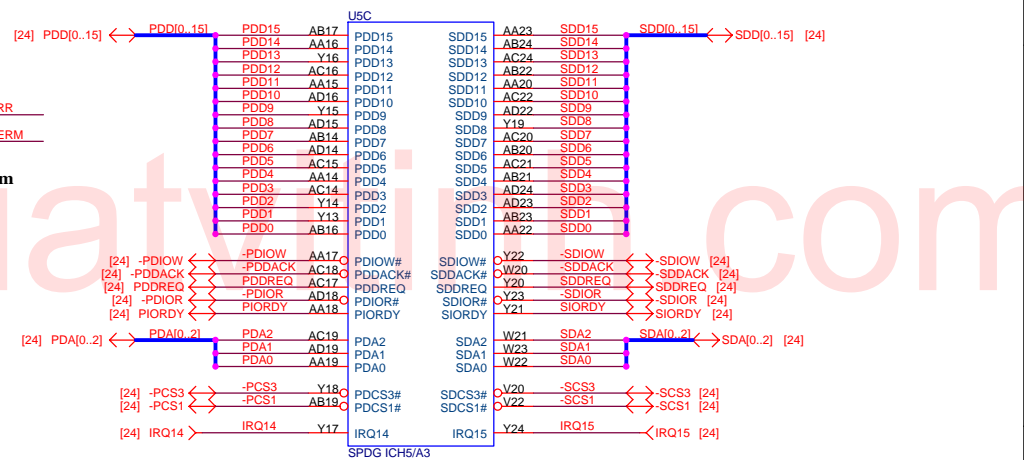
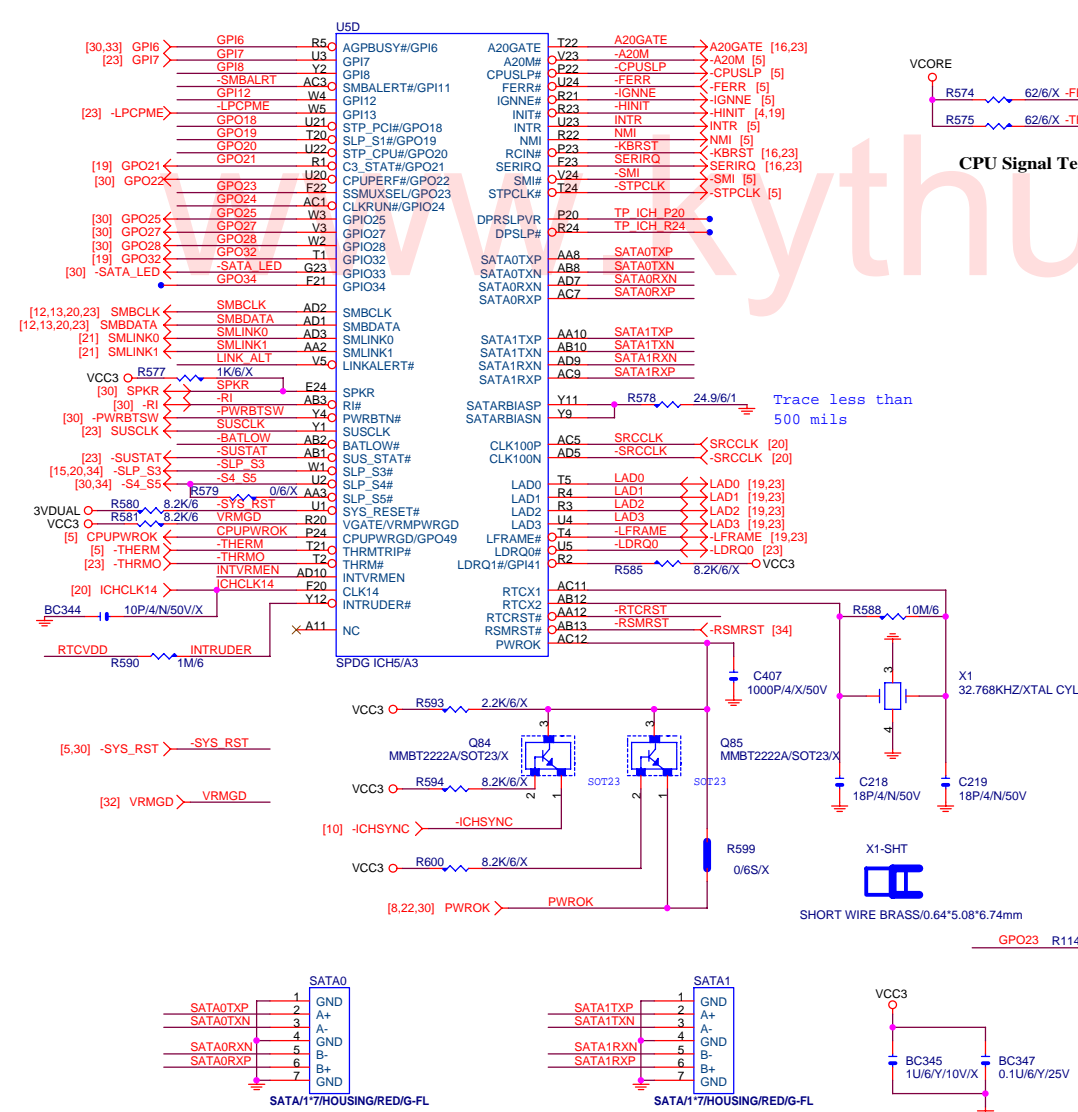


A_D[0..31] ↔ A_D[0..31] [21,22,35,36]



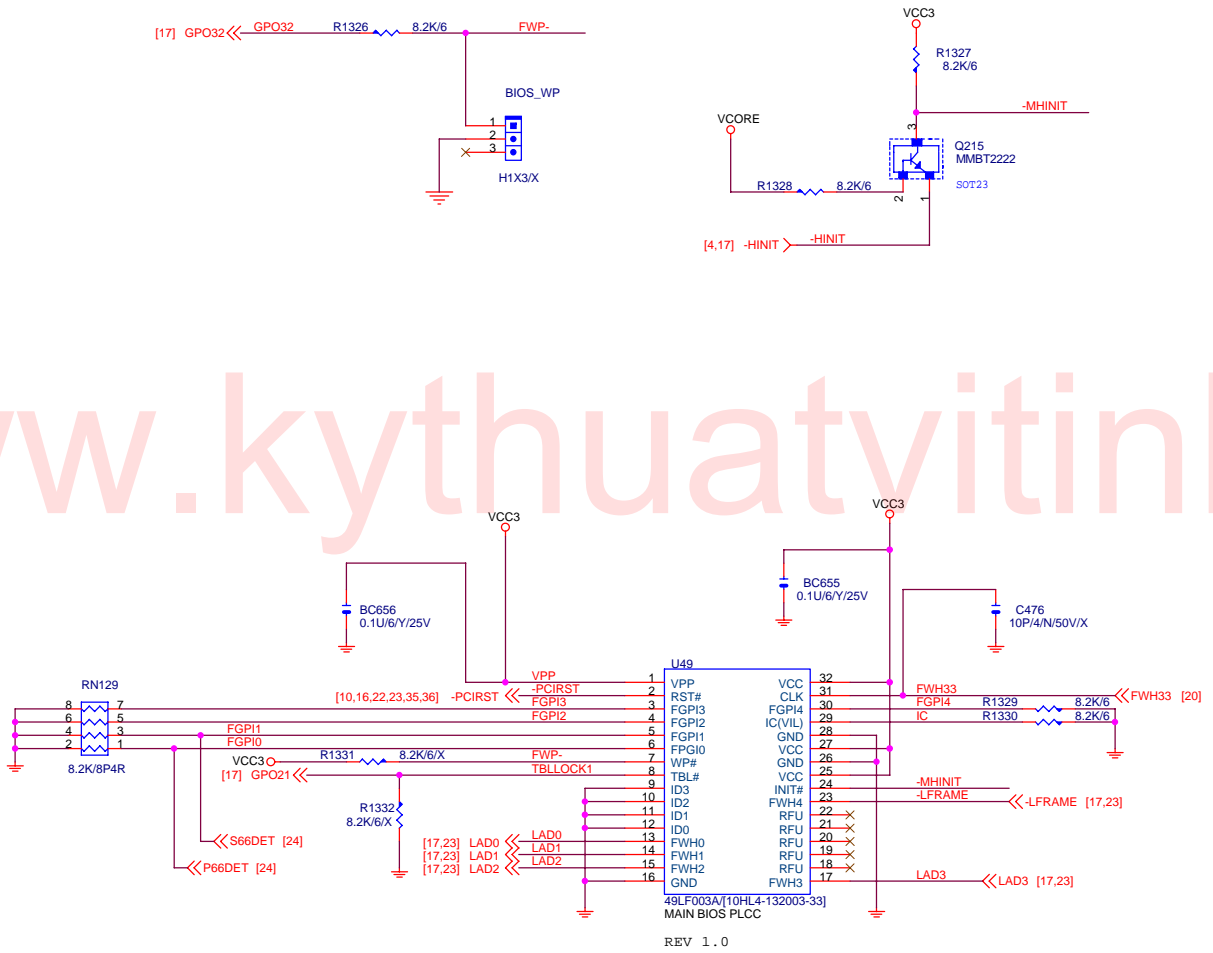


CLR_CMOS: 1-2	
SHORT	CLEAR CMOS
OPEN	NORMAL



GIGABYTE	
Title: ICH5 IDE, GPIO, SATA, CTRL	
Size: Custom	Document Number: GA-81865GVM-775
Date:	Rev: 1.0

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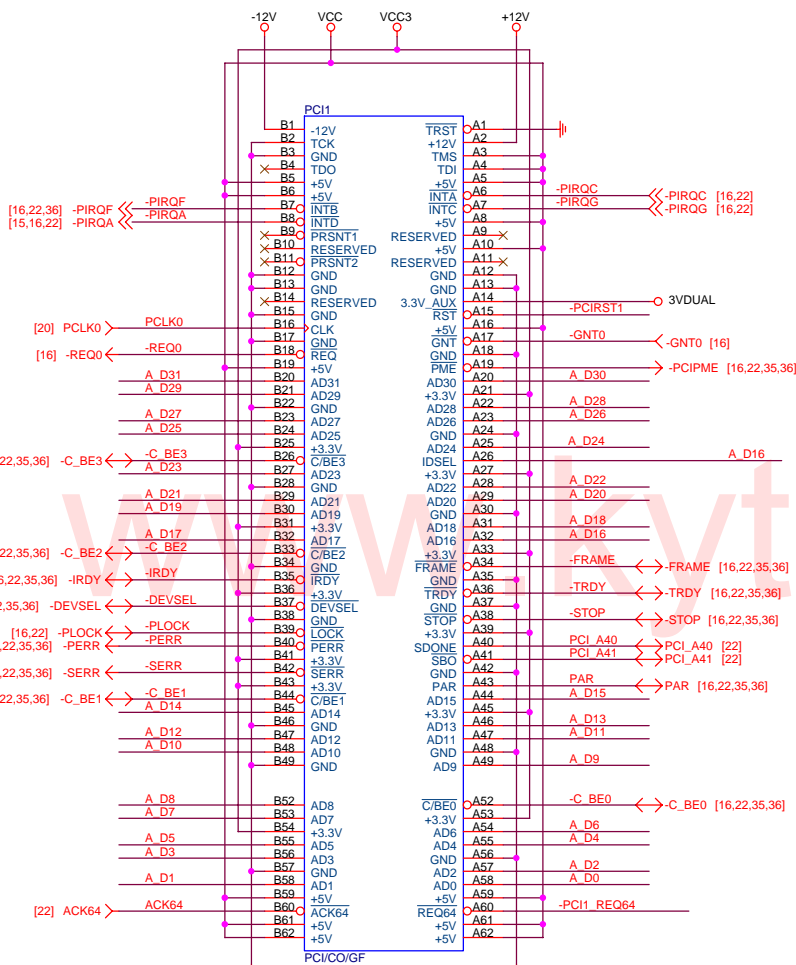


REV 1.0

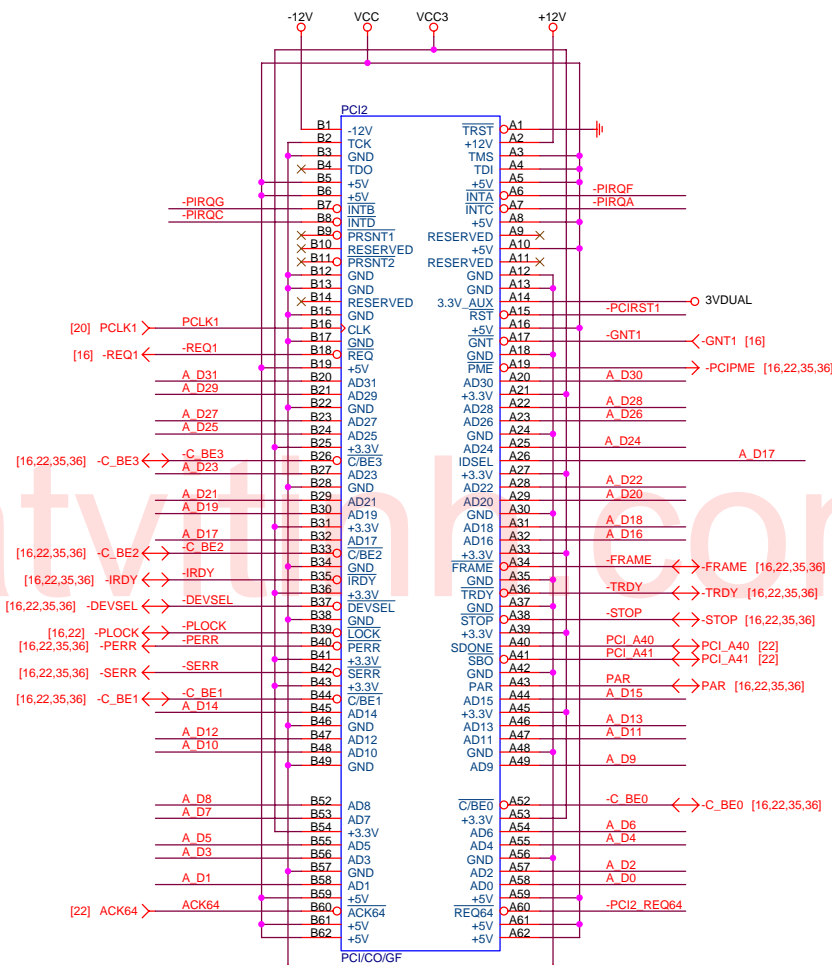
ADD WINBOUD FWH SEC. SOURCE



GIGABYTE		
Title		
FWH		
Size B	Document Number	Rev
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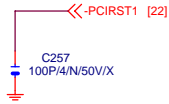


AD_16/-REQ0,-GNT0/-PIRQC,F,G,A

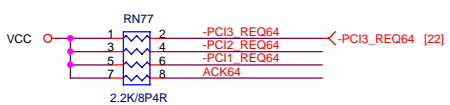


AD_17/-REQ1,-GNT1/-PIRQF,G,A,C

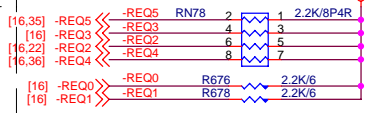
[16,22,35,36] A_D[0..31] << A D0..31



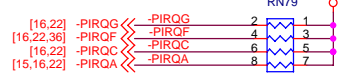
[17] SMLINK0 << R675 0/6/X PCI_A40
[17] SMLINK1 << R677 0/6/X PCI_A41



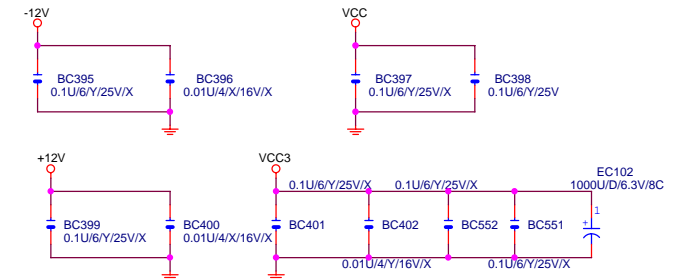
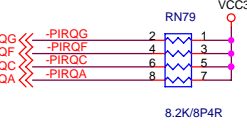
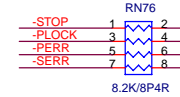
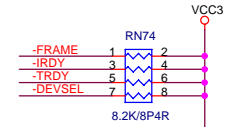
VCC << R1441 2.2K/6 PAR



[16,35] -REQ5 << -REQ5 RN78 2.2K/8P4R
[16] -REQ3 << -REQ3 4
[16,22] -REQ2 << -REQ2 6
[16,36] -REQ4 << -REQ4 8
[16] -REQ0 << -REQ0 R676 2.2K/6
[16] -REQ1 << -REQ1 R678 2.2K/6

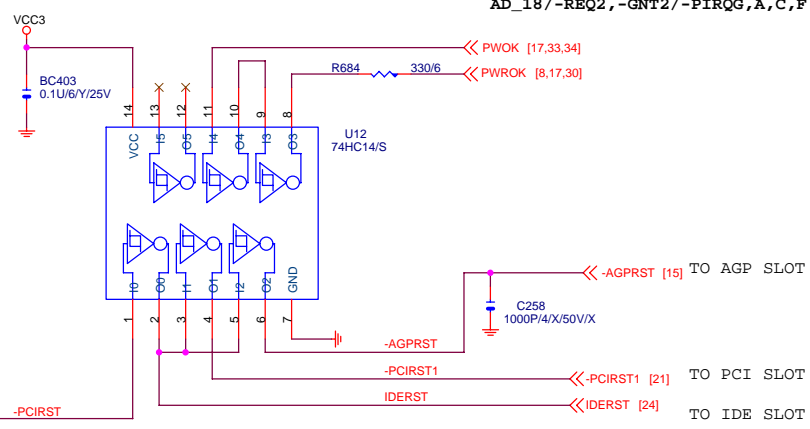
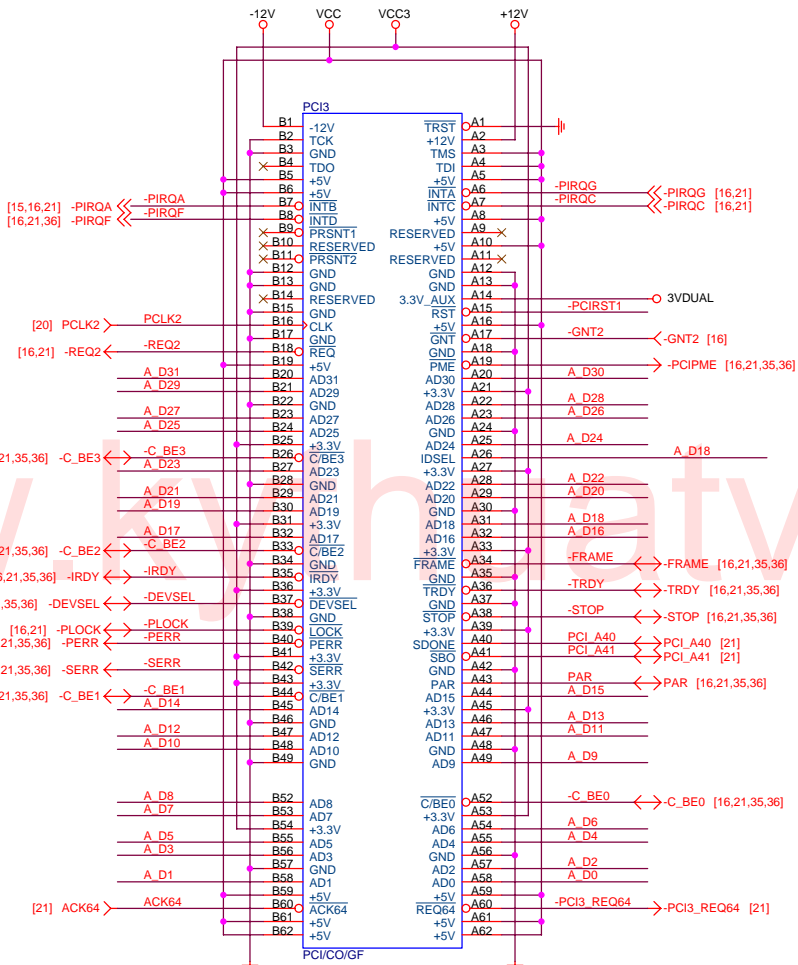


[16,22] -PIRQF << -PIRQF RN79 8.2K/8P4R
[16,22,36] -PIRQF << -PIRQF 4
[16,22] -PIRQC << -PIRQC 6
[15,16,22] -PIRQA << -PIRQA 8



GIGABYTE			
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[16,21,35,36] A_D[0..31] << A_D[0..31]



[10,16,19,23,35,36] -PCIRST << FROM ICH5

<< PWOK [17,33,34]

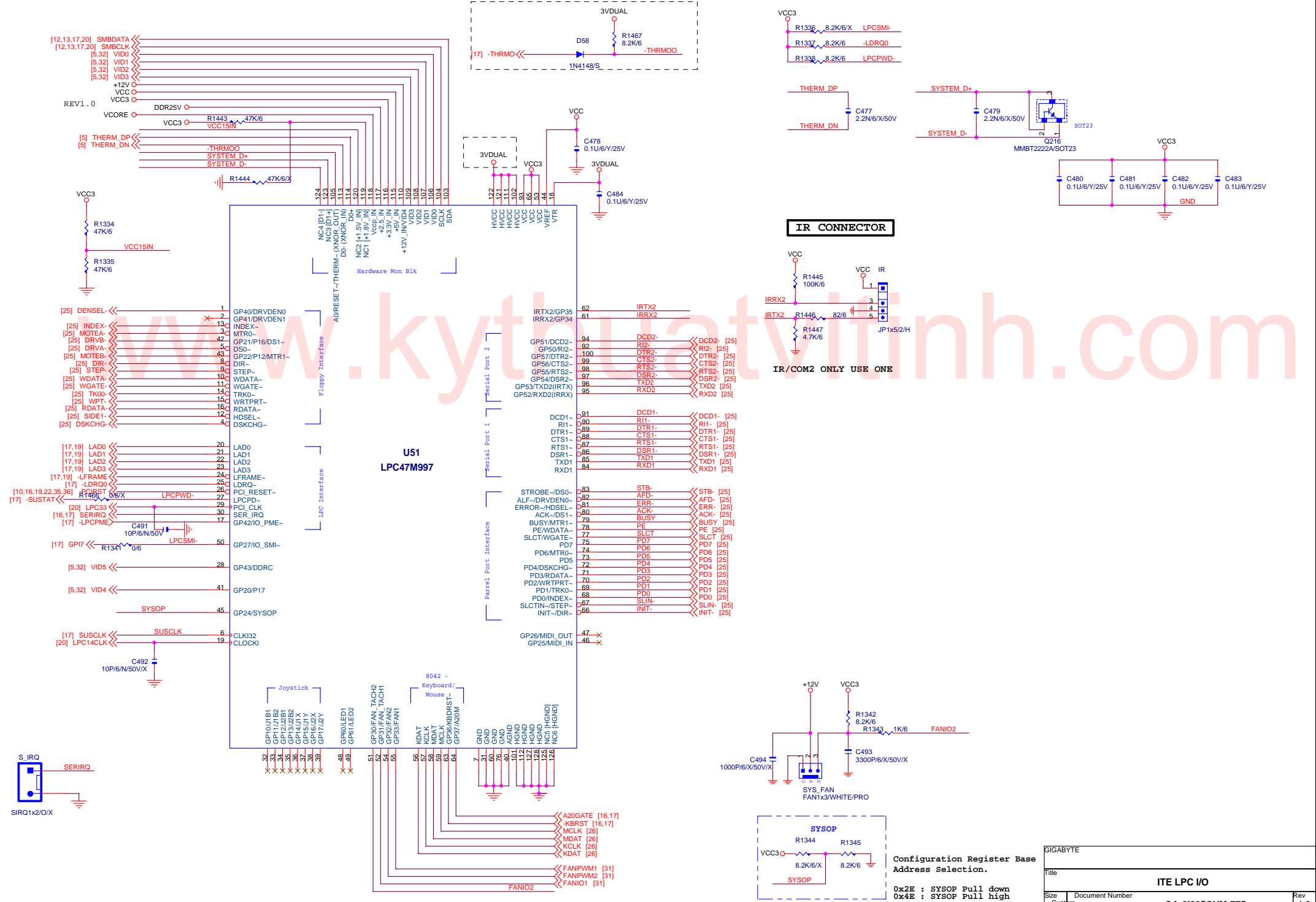
<< PWROK [8,17,30]

<< -AGPRST [15] TO AGP SLOT

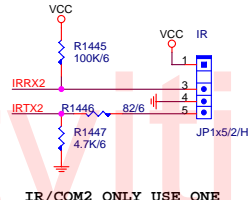
<< -PCIRST1 [21] TO PCI SLOT

<< -IDERST [24] TO IDE SLOT

GIGABYTE		
Title		
PCI SLOT 3		
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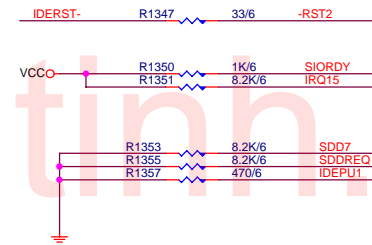
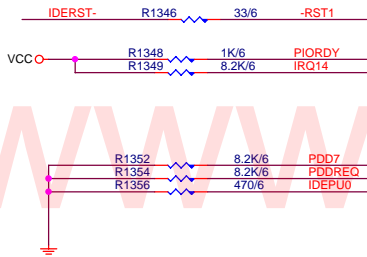
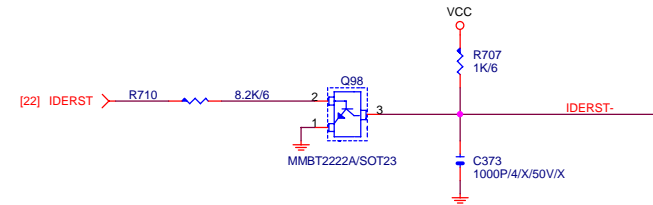
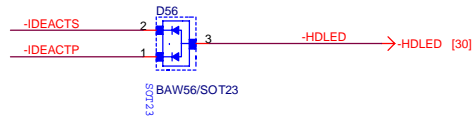
IR CONNECTOR



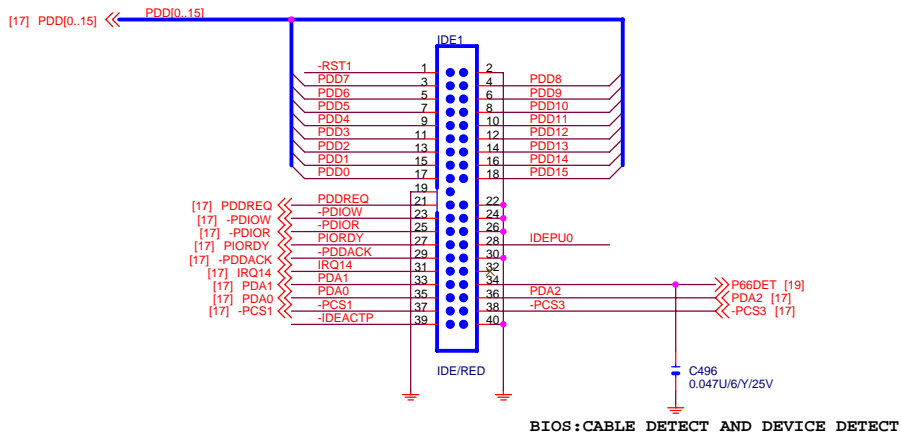
IR/COM2 ONLY USE ONE

Configuration Register Base Address Selection.
 0x2E : SYSOP Pull down
 0x4E : SYSOP Pull high

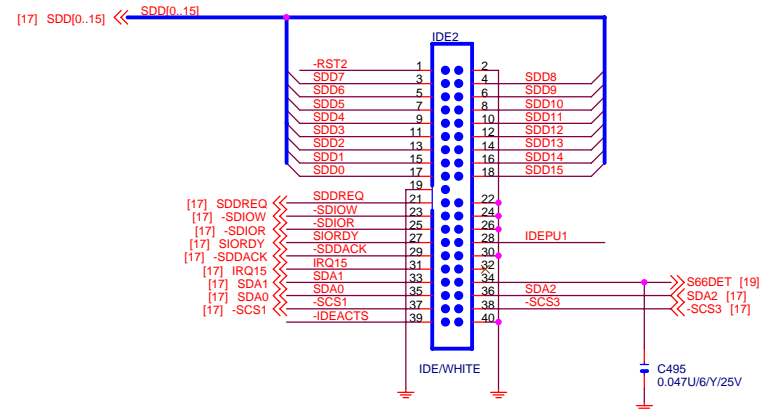
GIGABYTE		
Title		
ITE LPC I/O		
Size	Document Number	Rev
Custom	GA-8I865GVM-775	1.0
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PRIMARY IDE CONNECTOR

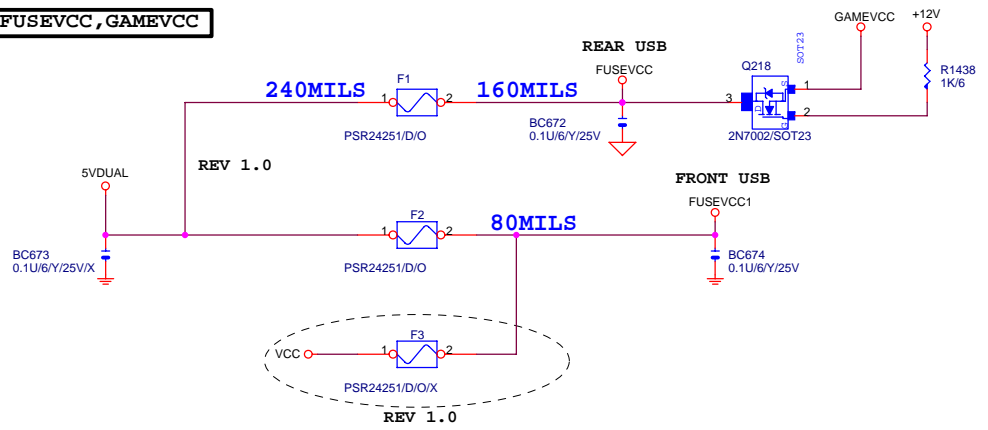


SECONDARY IDE CONNECTOR

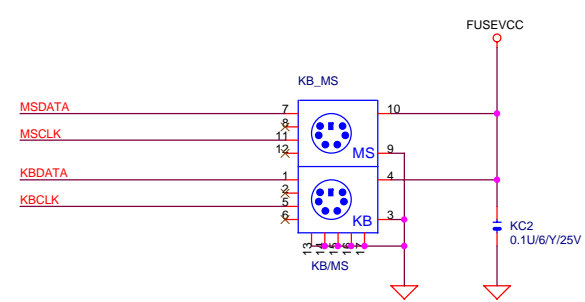
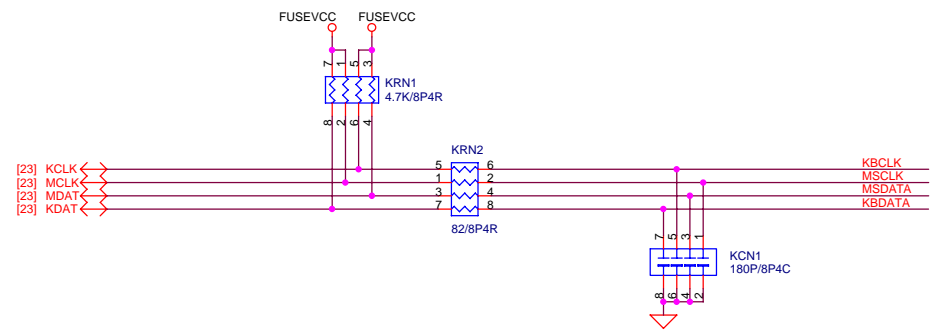


GIGABYTE			
Title			
IDE CONNECTOR			
Size	Document Number	Rev	
B		GA-81865GVM-775	
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		1	1.0

FUSEVCC, GAMEVCC

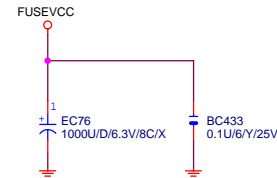
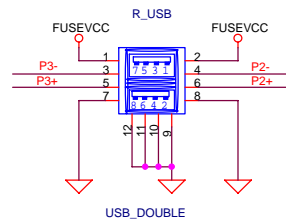
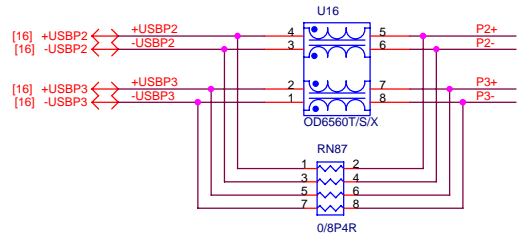


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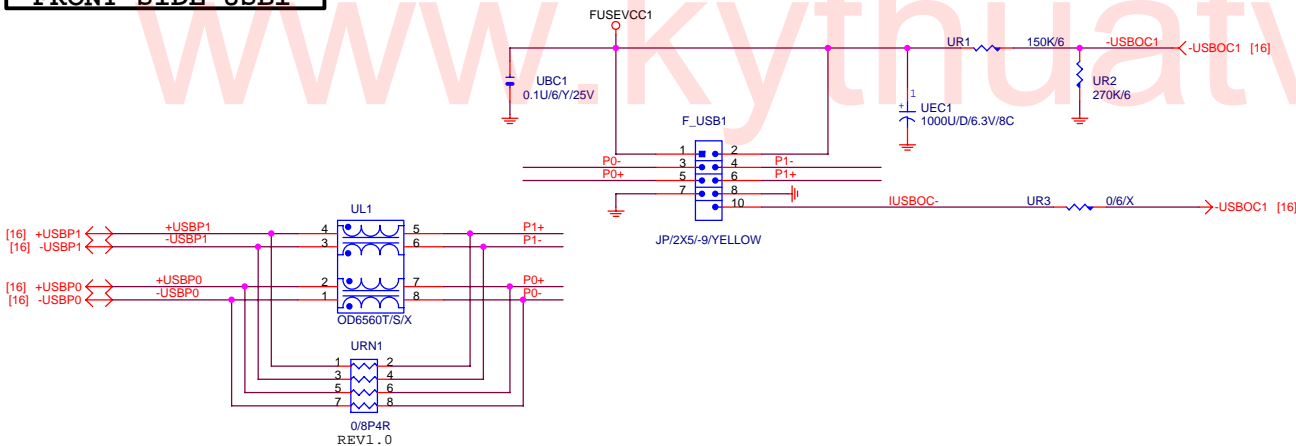


GIGABYTE			
Title			
KB & PS2 MOUSE & IR			
Size	Document Number	GA-8I865GVM-775	Rev
B			1.0
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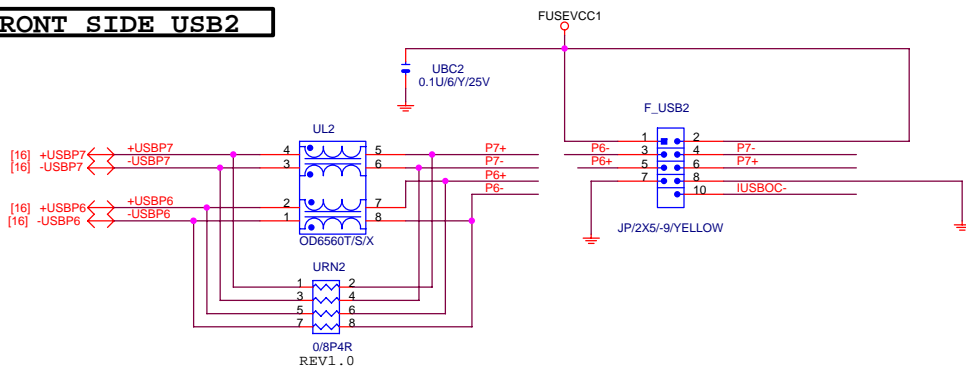
REAR USB



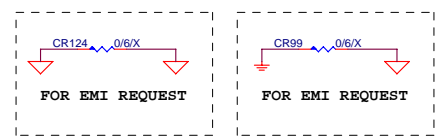
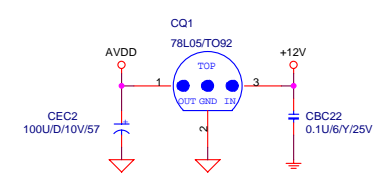
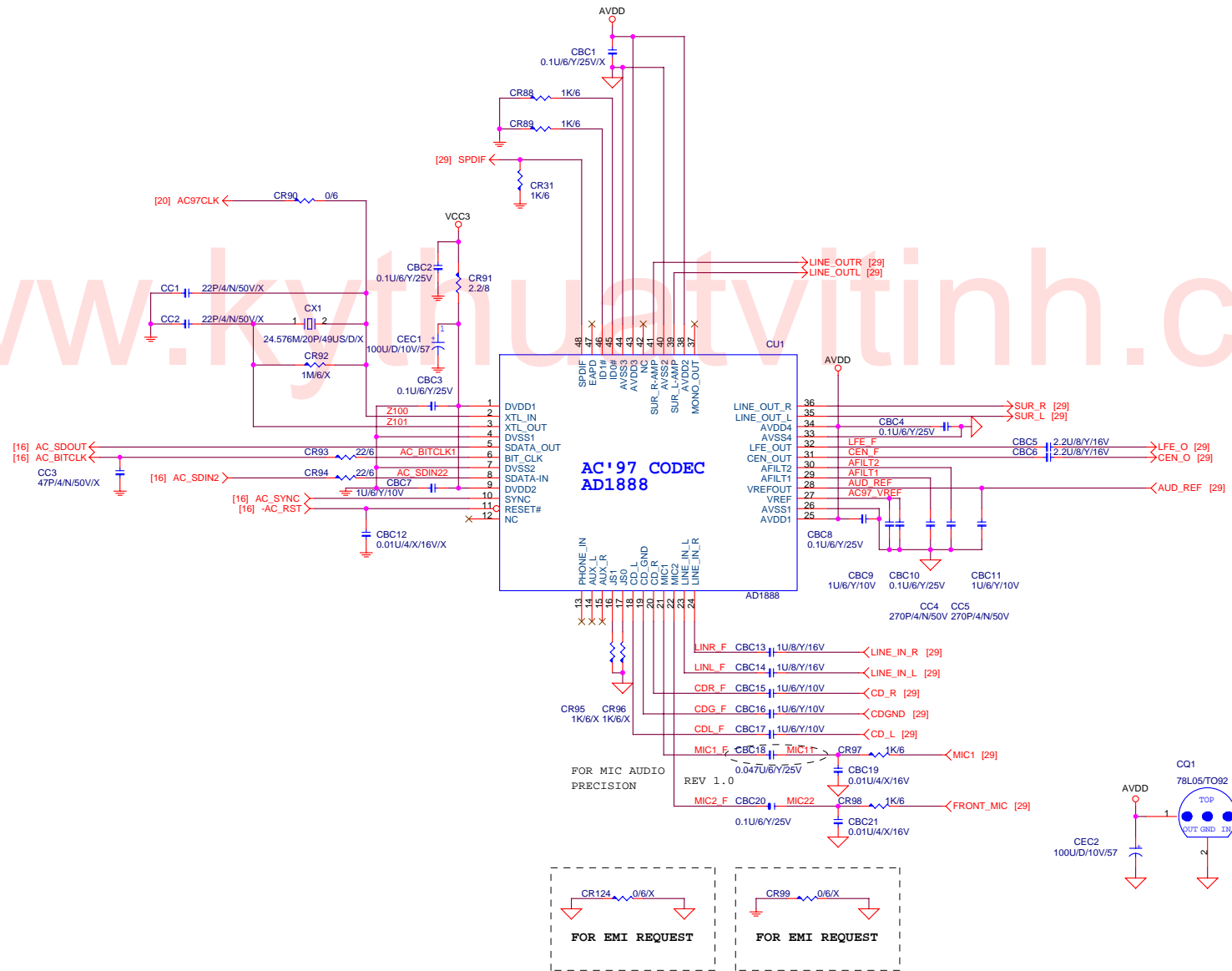
FRONT SIDE USB1



FRONT SIDE USB2

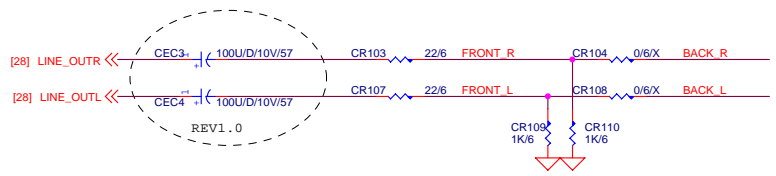


GIGABYTE			
Title			
ICH USB PORT			
Size B	Document Number	GA-81865GVM-775	Rev 1.0
Date:		Sheet 27 of 38	

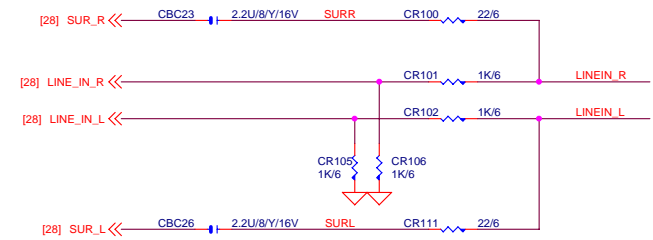


GIGABYTE		
Title AC97-ADI1888		
Size Custom	Document Number GA-81865GVM-775	Rev 1.0
Date: Friday, October 08, 2004	Sheet 28	of 38

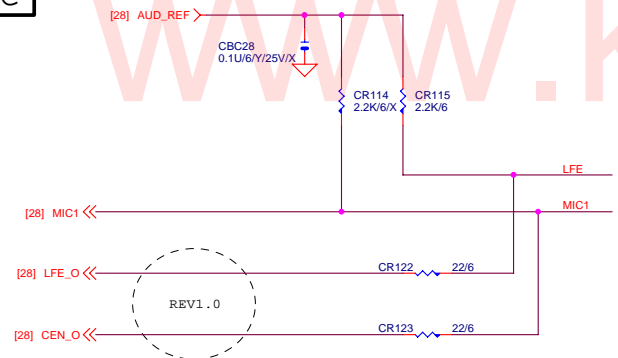
LINE OUT



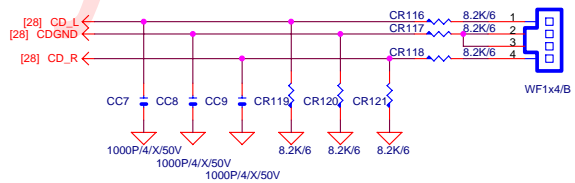
LINE-IN



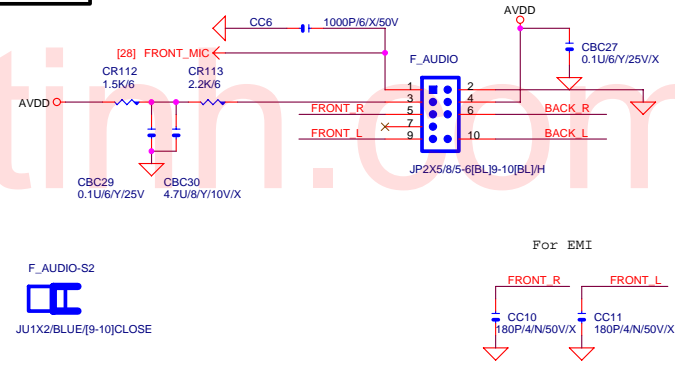
MIC



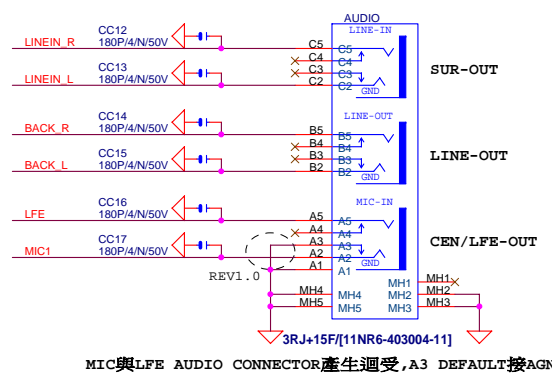
CD IN



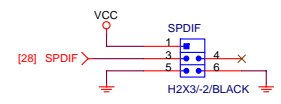
INTEL FRONT AUDIO



AC97 JACK

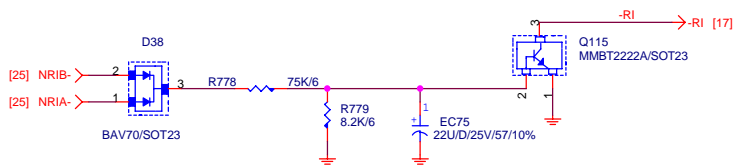
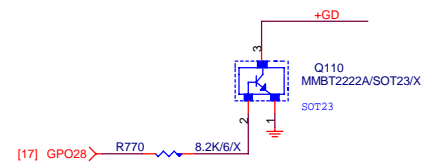
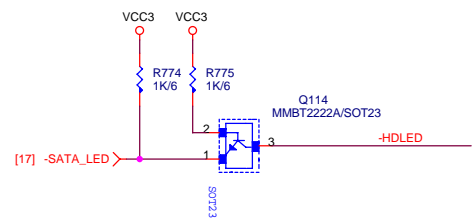
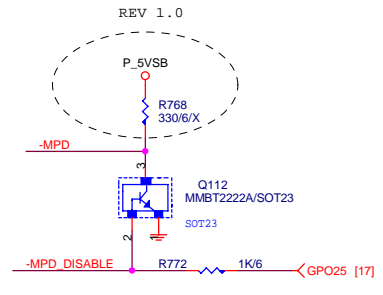
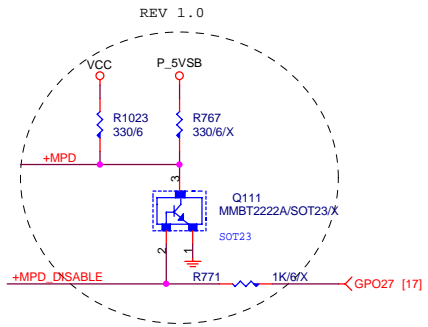
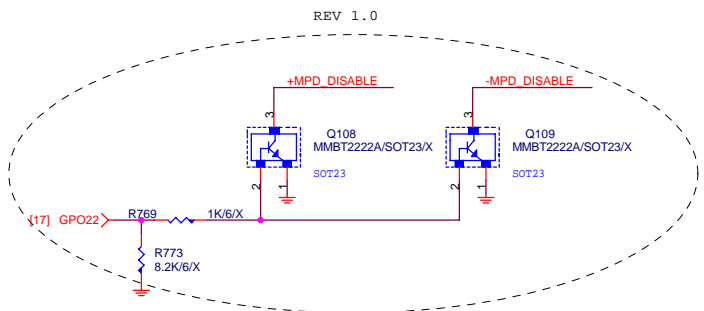
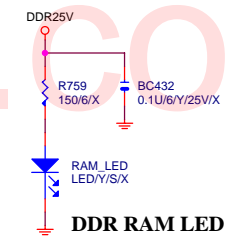
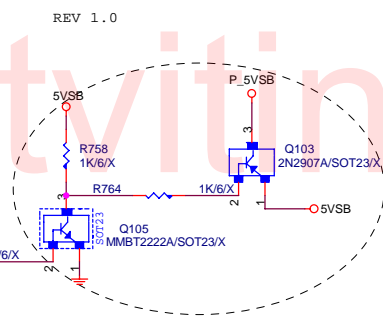
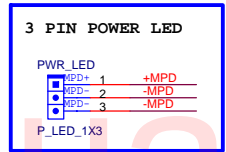
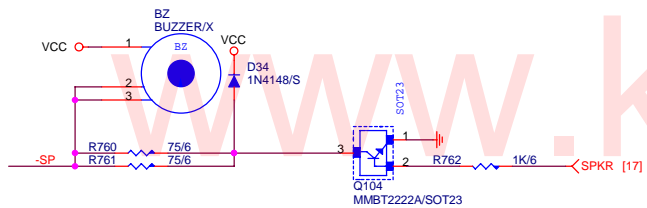
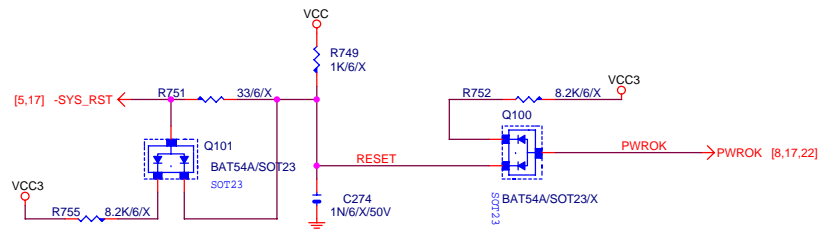
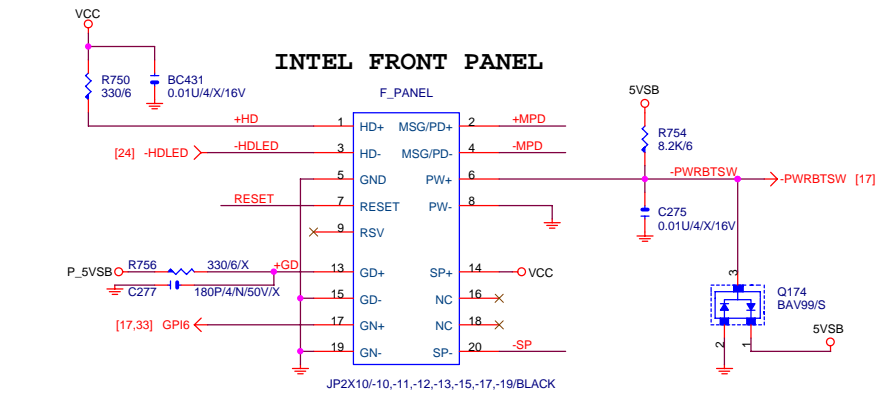


SPDIF

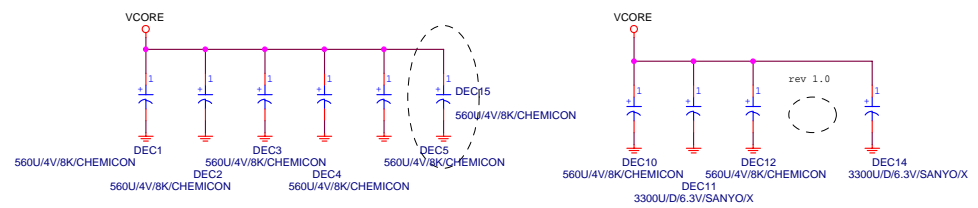


MIC與LFE AUDIO CONNECTOR 產生迴受, A3 DEFAULT 接AGND

GIGABYTE		
AUDIO OUTPUT, GAME PORT		
Size Custom	Document Number	Rev
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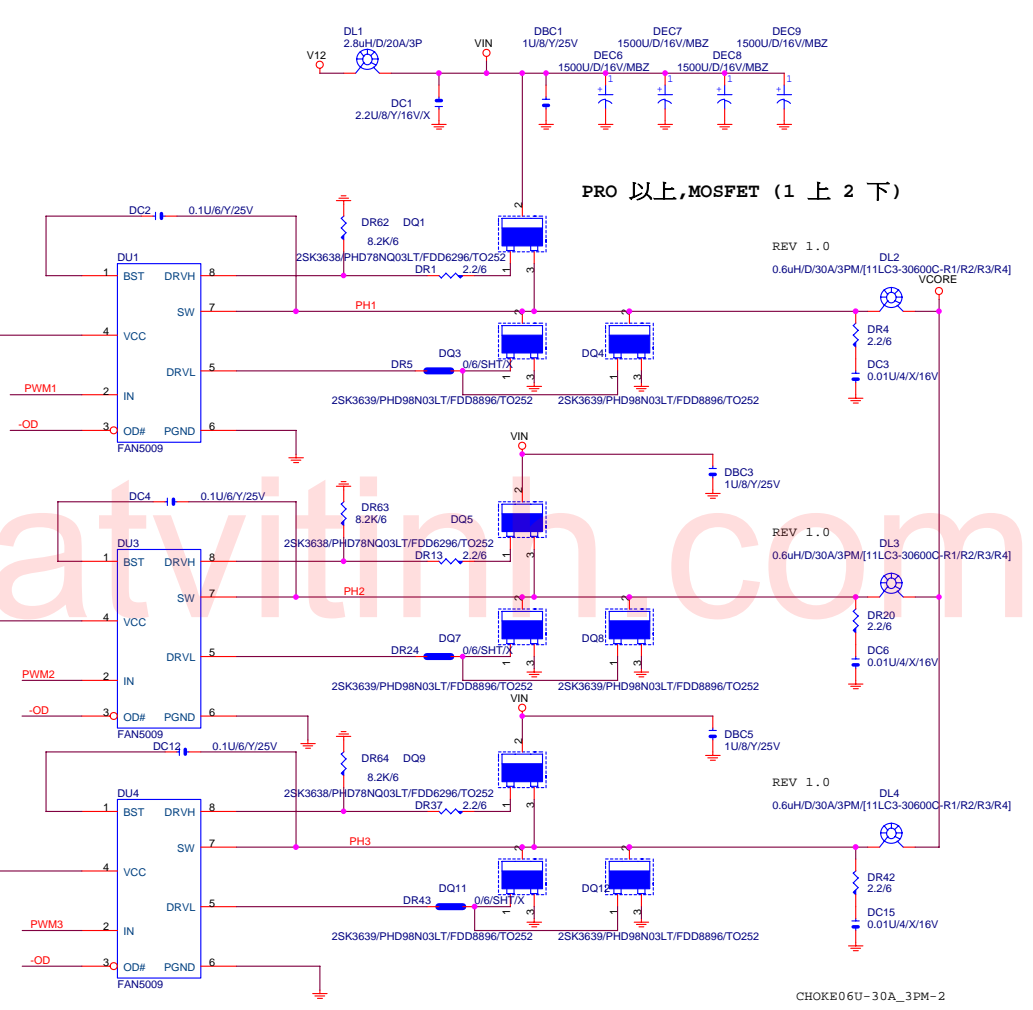
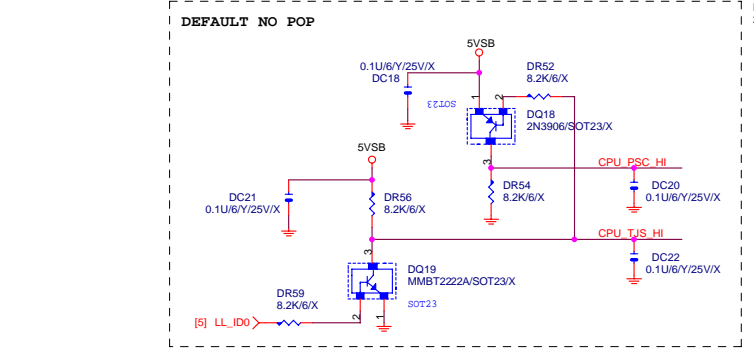
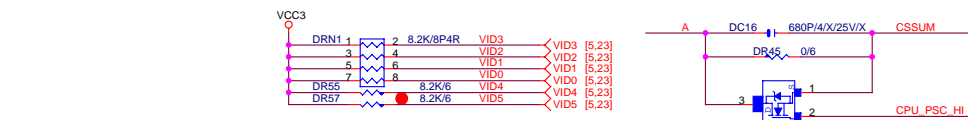
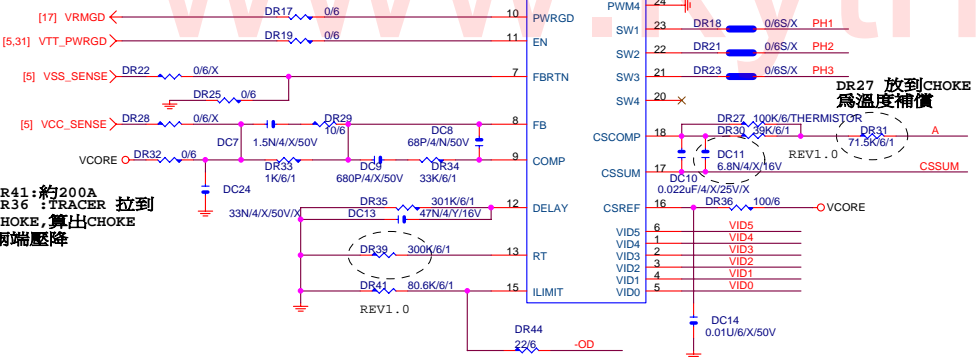


GIGABYTE			
Title			
PANEL & STR LED & RI			
Size B	Document Number	GA-81865GVM-775	
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		1	Rev 1.0



DD1 :在HIGH SIDE 發生S-D SHORT 時(OVP), LOW SIDE MOSFET TURN ON ,讓Vcore 降壓,同時V12 也會下降6-7V以下時,造成PWM 無法提供POWER TO LOW SIDE TURN ON,所以加DD1 延長POWER 提供給LOW SIDE MOSFET TURN ON 保護CPU VOLTAGE 過高.

DR9,DC5 FOR V12 OVER 19V 以上,SPEC (18V)
 DR12 為一個 CYCLE的DUTY(50%)
 DELAY :讓限流時間DELAY (DR35,DC13) 才啟動.
 DR39:240K
 工作頻率=720KHZ / 4PHASE=180K(1 PHASE)



PRO 以上,MOSFET (1 上 2 下)

REV 1.0
 DL2 0.6uH/D/30A/3PM(11LC3-30600C-R1/R2/R3/R4)

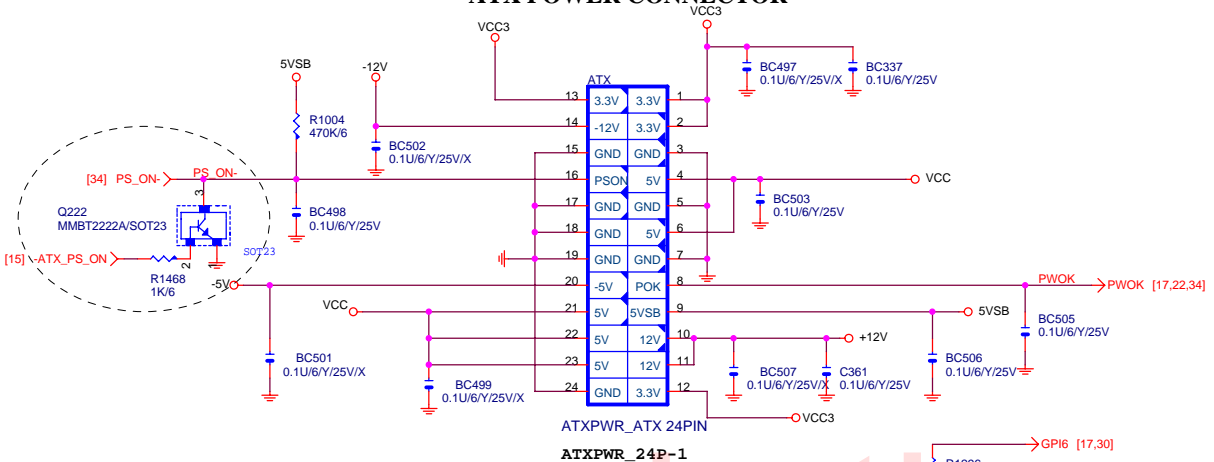
REV 1.0
 DL3 0.6uH/D/30A/3PM(11LC3-30600C-R1/R2/R3/R4)

REV 1.0
 DL4 0.6uH/D/30A/3PM(11LC3-30600C-R1/R2/R3/R4)

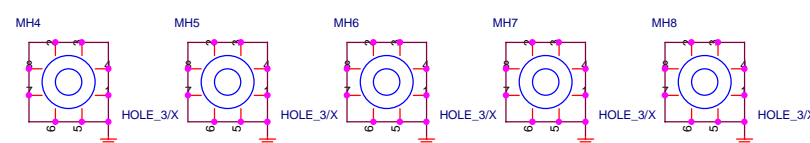
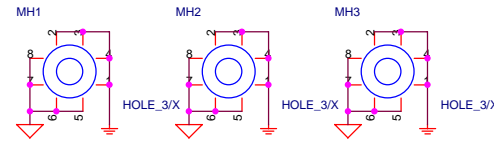
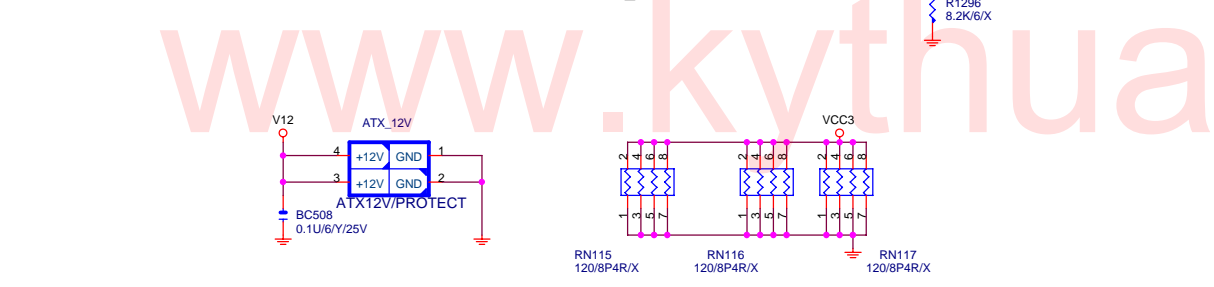
CHOKE06U-30A_3PM-2

GIGABYTE			
Title VRD 10.1			
Size	Document Number	GA-8I865GVM-775	
Custom			Rev 1.0
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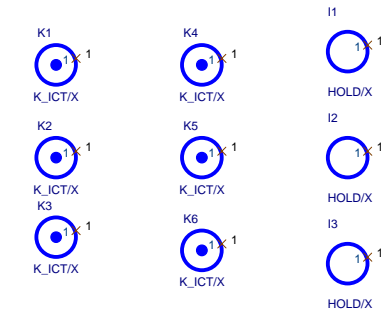
ATX POWER CONNECTOR



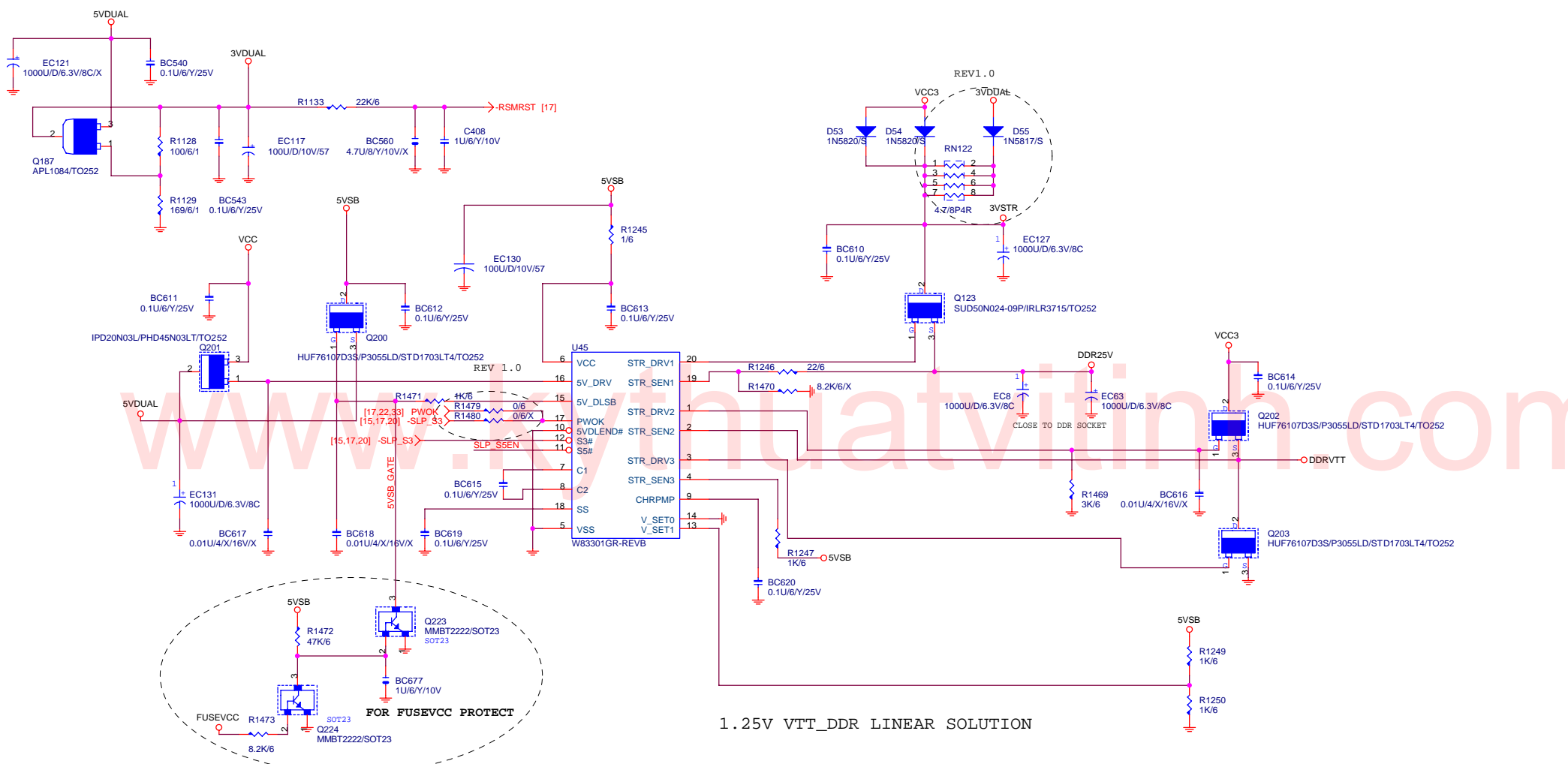
ATXPWR_ATX 24PIN
ATXPWR_24P-1



(08/12) HOLE_3-2



GIGABYTE			
Title			
Misc. PWR & ATX CONN.			
Size B	Document Number	GA-81865GVM-775	Rev 1.0
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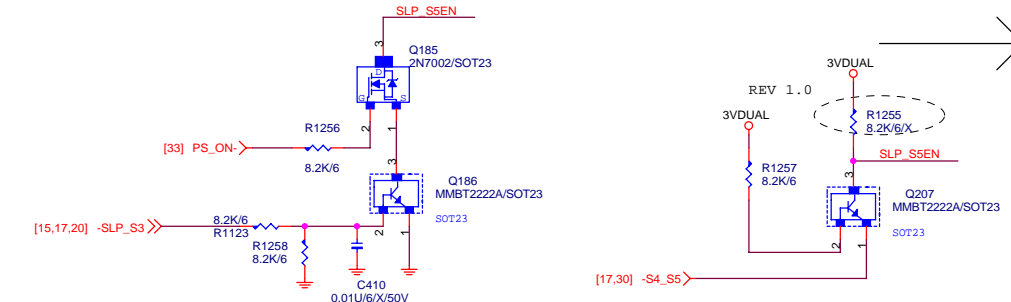


1.25V VTT_DDR LINEAR SOLUTION

DDR25_OV1,DDR25_OV2,DDR25_OV3 RESUME WELL DEFAULT HIGH

	DDR25_OV2	DDR25_OV1	DDR25_OV3	V_SET0	V_SET1
2.5V	HIGH	HIGH	HIGH	0V	0V
2.6V	LOW	HIGH	HIGH	0V	2.5V
2.7V	LOW	LOW	HIGH	0V	5V
2.8V	HIGH	HIGH	LOW	2.5V	0V

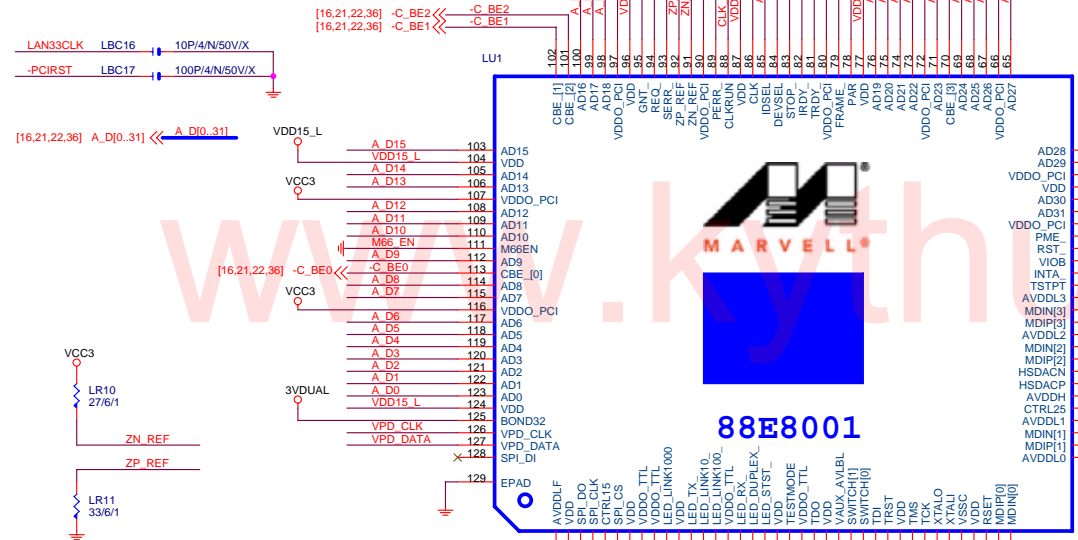
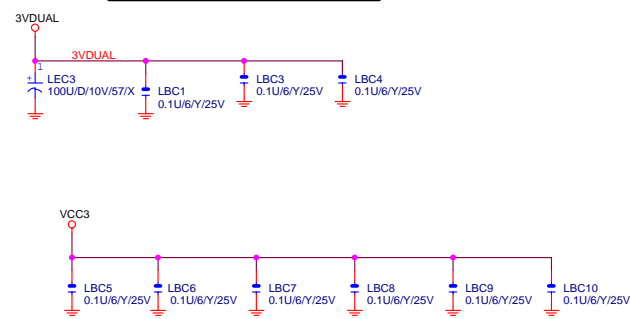
FOR 2.8V BIOS PROGRAMMING
 時須先PROGRAMMING
 2.5V後再PROGRAMMING 2.8V



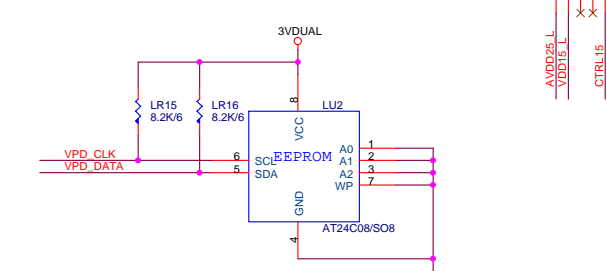
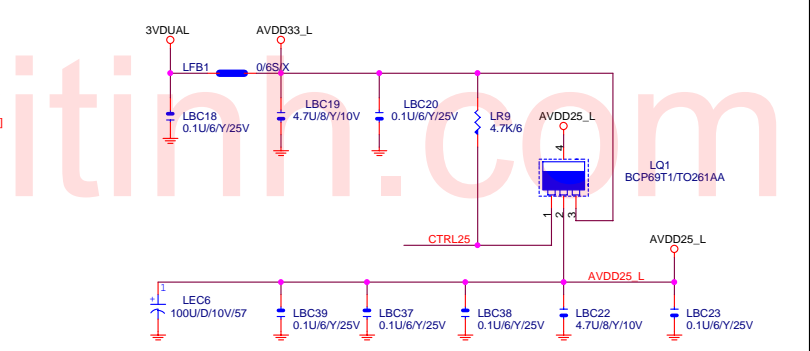
[16,21,22,36] -C BE3<< -C BE3
 [16,21,22,36] PAR -PAR
 [16,21,22,36] -FRAME -FRAME
 [16,21,22,36] -TRDY -TRDY
 [16,21,22,36] -IRDY -IRDY
 [16,21,22,36] -STOP -STOP
 [16,21,22,36] -STOR -STOR
 [16,21,22,36] -DEVSEL -DEVSEL
 [20] LAN33CLK LAN33CLK
 [16,21,22,36] -PERR -PERR
 [16,21,22,36] -SERR -SERR
 [16,21] -REQ0 -REQ0
 [16] -GNT5 -GNT5

- # Layout Check 注意事項
1. LU1 PIN129 需下內層GND, 至少打 22 VIA
 2. 3VDUAL, VCC3, VDD15_L, AVDD25_L 至少走20mil寬, 並且電容擺設每兩pin至少放一顆Bypass Cap.
 3. X'TAL 25MHz 兩訊號線, TRACE 愈短愈好, 線寬12mil
 4. MDI正負0-3, TRACE 8:7:8, 每對之間保持 40mil

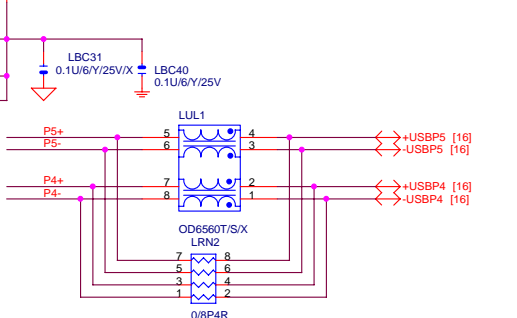
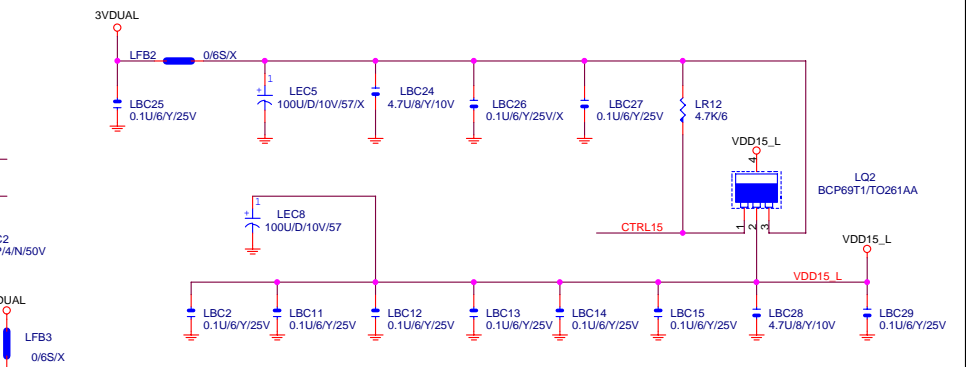
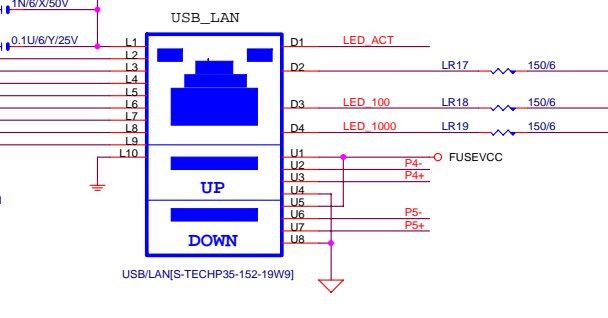
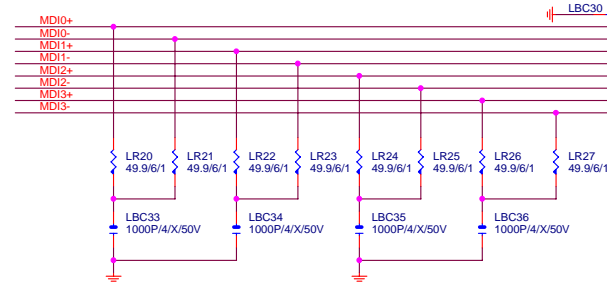
POWER DECOUPLING CAP.



AD28 .64 A D28
 AD29 .65 A D29
 VDDO_PCI .62
 VDD .61 VDD15_L
 VDD .60 A D30
 VDD .59 A D31
 VDDO_PCI .57 -PCIPME
 PME .56 -PCIRST
 RST .55
 VIOB .54 -PIROE
 INTA .53
 TSPT .52 X
 AVDDL3 .51
 MDIN[3] .50 MDI3+
 MDIP[3] .49 AVDD25_L
 AVDDL2 .48 MDI2+
 MDIN[2] .47 MDI2+
 MDIP[2] .46
 HSDACN .45 X
 AVDDH .44 X
 HSDACP .43 CTRL25
 AVDDL1 .42 AVDD25_L
 MDIN[1] .41 MDI1+
 MDIP[1] .40 MDI1+
 AVDDL0 .39 AVDD25_L



PIN L1, L10 TRACER 40MIL



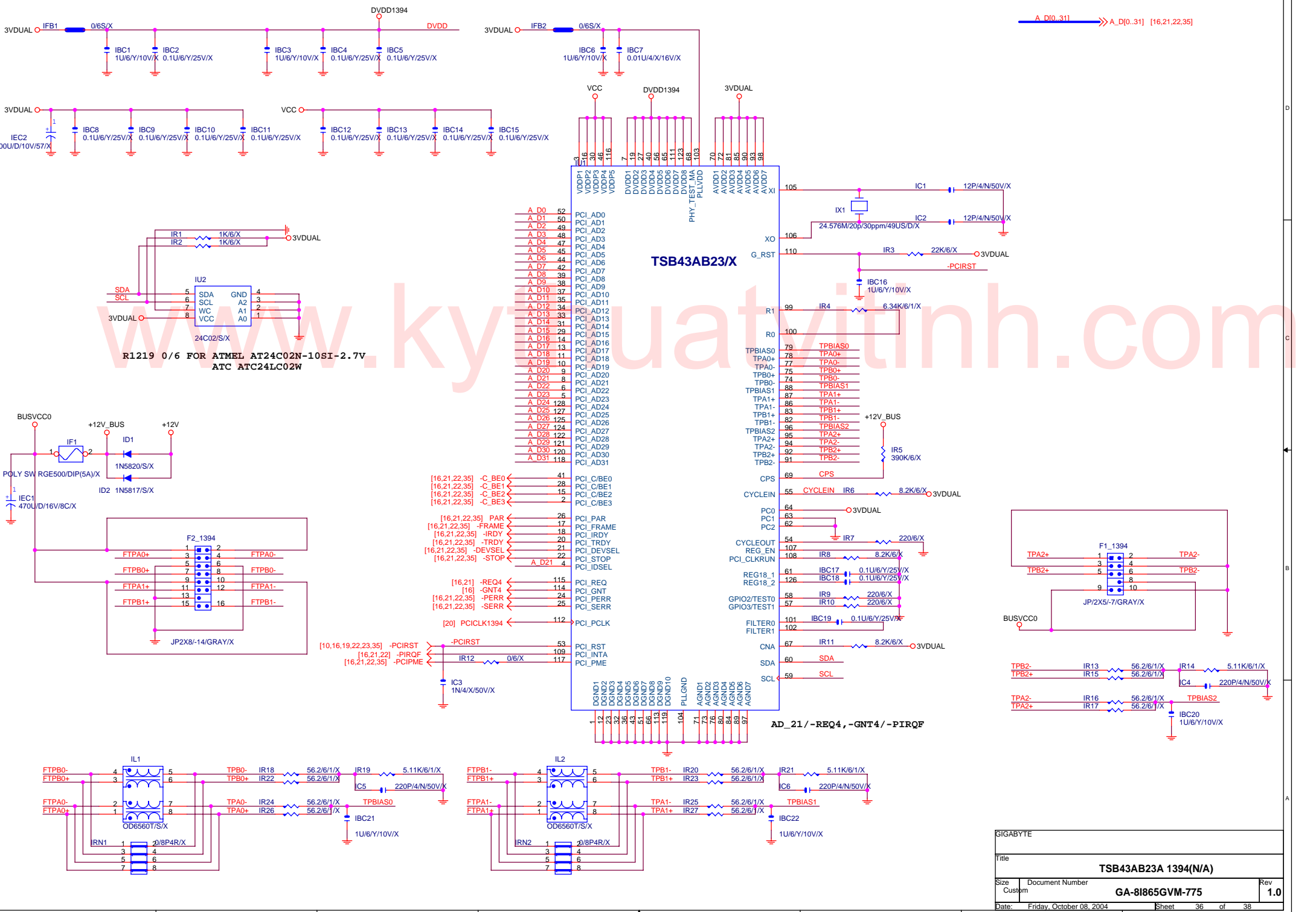
GIGABYTE

MARVELL 88E8001

GA-81865GVM-775

Rev 1.0

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TSB43AB23/X

A D0	52	PCI_AD0
A D1	50	PCI_AD1
A D2	49	PCI_AD2
A D3	48	PCI_AD3
A D4	47	PCI_AD4
A D5	44	PCI_AD5
A D6	44	PCI_AD6
A D7	42	PCI_AD7
A D8	39	PCI_AD8
A D9	38	PCI_AD9
A D10	37	PCI_AD10
A D11	35	PCI_AD11
A D12	34	PCI_AD12
A D13	33	PCI_AD13
A D14	31	PCI_AD14
A D15	29	PCI_AD15
A D16	14	PCI_AD16
A D17	13	PCI_AD17
A D18	11	PCI_AD18
A D19	10	PCI_AD19
A D20	9	PCI_AD20
A D21	8	PCI_AD21
A D22	6	PCI_AD22
A D23	5	PCI_AD23
A D24	128	PCI_AD24
A D25	127	PCI_AD25
A D26	125	PCI_AD26
A D27	124	PCI_AD27
A D28	122	PCI_AD28
A D29	121	PCI_AD29
A D30	120	PCI_AD30
A D31	118	PCI_AD31
41	PCI_C/BE0	
28	PCI_C/BE1	
15	PCI_C/BE2	
2	PCI_C/BE3	
26	PCI_PAR	
17	PCI_FRAME	
18	PCI_IRDY	
20	PCI_TRDY	
21	PCI_DEVSEL	
22	PCI_STOP	
4	PCI_IDSEL	
115	PCI_REQ	
114	PCI_GNT	
24	PCI_PERR	
25	PCI_SERR	
112	PCI_PCLK	
53	PCI_RST	
109	PCI_INTA	
117	PCI_PME	
12	DGND1	
23	DGND2	
36	DGND3	
43	DGND4	
51	DGND5	
66	DGND6	
77	DGND7	
83	DGND8	
84	DGND9	
89	DGND10	
104	PLLGND	
71	AGND1	
72	AGND2	
73	AGND3	
74	AGND4	
78	AGND5	
80	AGND6	
84	AGND7	
88	AGND8	
89	AGND9	
97	AGND10	

GIGABYTE		
Title		
TSB43AB23A 1394(N/A)		
Size	Document Number	Rev
Custom	GA-81865GVM-775	1.0
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GIGABYTE GA-8I865GVM-775 PCI ROUNTING LIST

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT
PCI SLOT1	16	C,F,G,A	PCLK0	-REQ0	-GNT0
PCI SLOT2	17	F,G,A,C	PCLK1	-REQ1	-GNT1
PCI SLOT3	18	G,A,C,F	PCLK2	-REQ2	-GNT2
TI 1394	21	F	PCICLK1394	-REQ4	-GNT4
LAN (Marvell)	25	E	LANCLK33	-REQ5	-GNT5

GIGABYTE		
Title PCI ROUNT LIST		
Size Custom	Document Number GA-8I865GVM-775	Rev 1.0
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