

GA-6VEML REV 1.0 (VT8601T + VT82C686B)

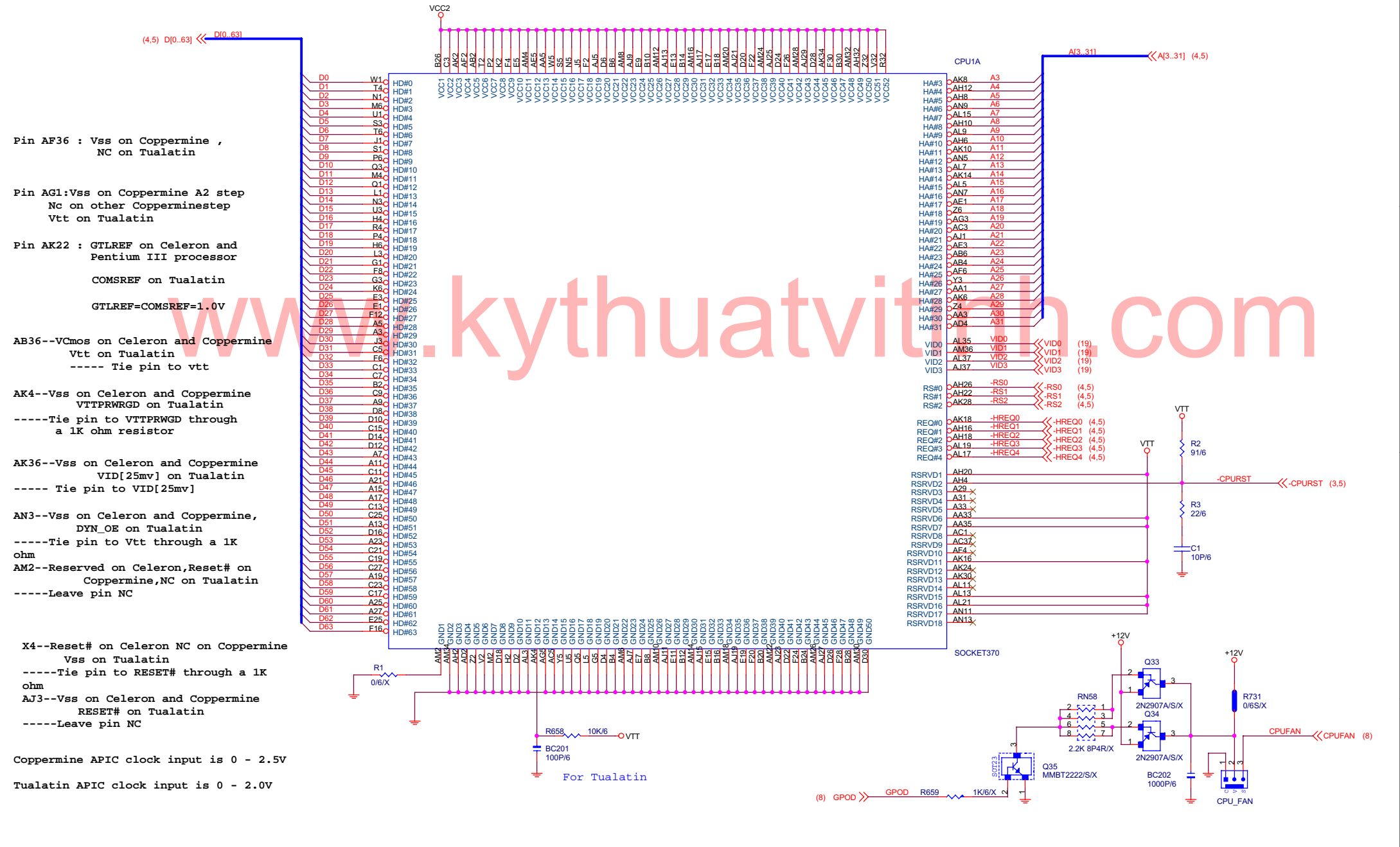
TITLE

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Pin AF36 : Vss on Coppermine ,
NC on Tualatin

Pin AG1:Vss on Coppermine A2 step
Nc on other Copperminestep
Vtt on Tualatin

Pin AK22 : GTLREF on Celeron and
Pentium III processor

COMSREF on Tualatin

GTLREF=COMSREF=1.0V

AB36--Vcmos on Celeron and Coppermine
Vtt on Tualatin
----- Tie pin to vtt

AK4--Vss on Celeron and Coppermine
VITPRWRGD on Tualatin
-----Tie pin to VITPRWRGD through
a 1K ohm resistor

AK36--Vss on Celeron and Coppermine
VID[25mv] on Tualatin
----- Tie pin to VID[25mv]

AN3--Vss on Celeron and Coppermine,
DYN_OE on Tualatin
-----Tie pin to Vtt through a 1K
ohm

AM2--Reserved on Celeron,Reset# on
Coppermine,NC on Tualatin
-----Leave pin NC

X4--Reset# on Celeron NC on Coppermine
Vss on Tualatin
-----Tie pin to RESET# through a 1K
ohm

AJ3--Vss on Celeron and Coppermine
RESET# on Tualatin
-----Leave pin NC

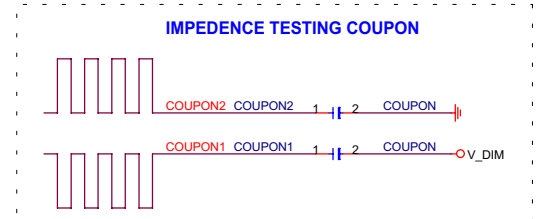
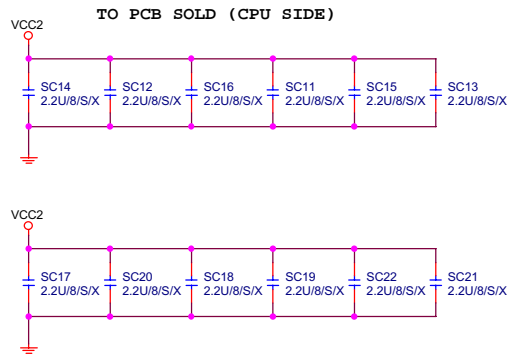
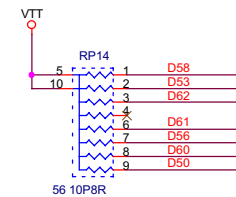
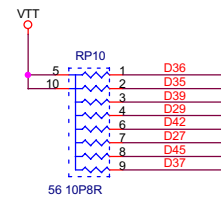
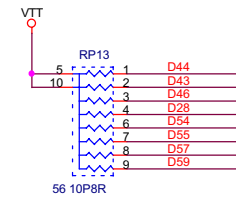
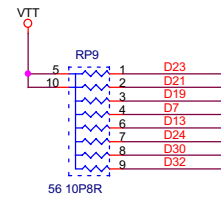
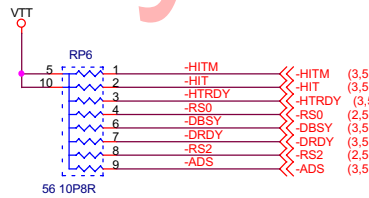
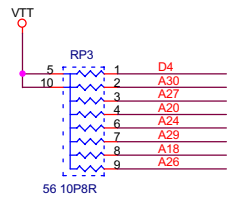
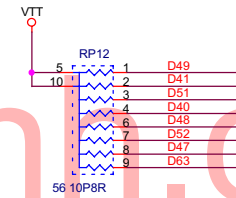
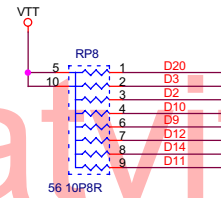
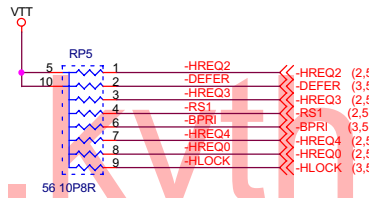
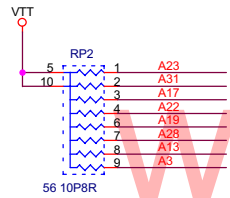
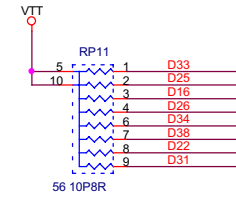
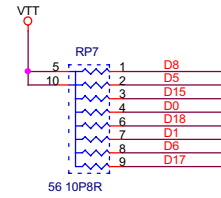
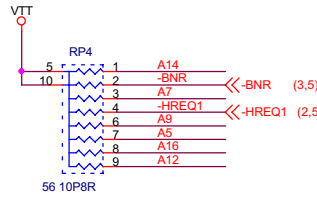
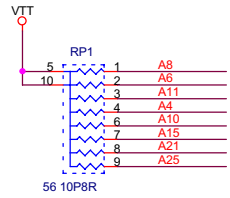
Coppermine APIC clock input is 0 - 2.5V
Tualatin APIC clock input is 0 - 2.0V

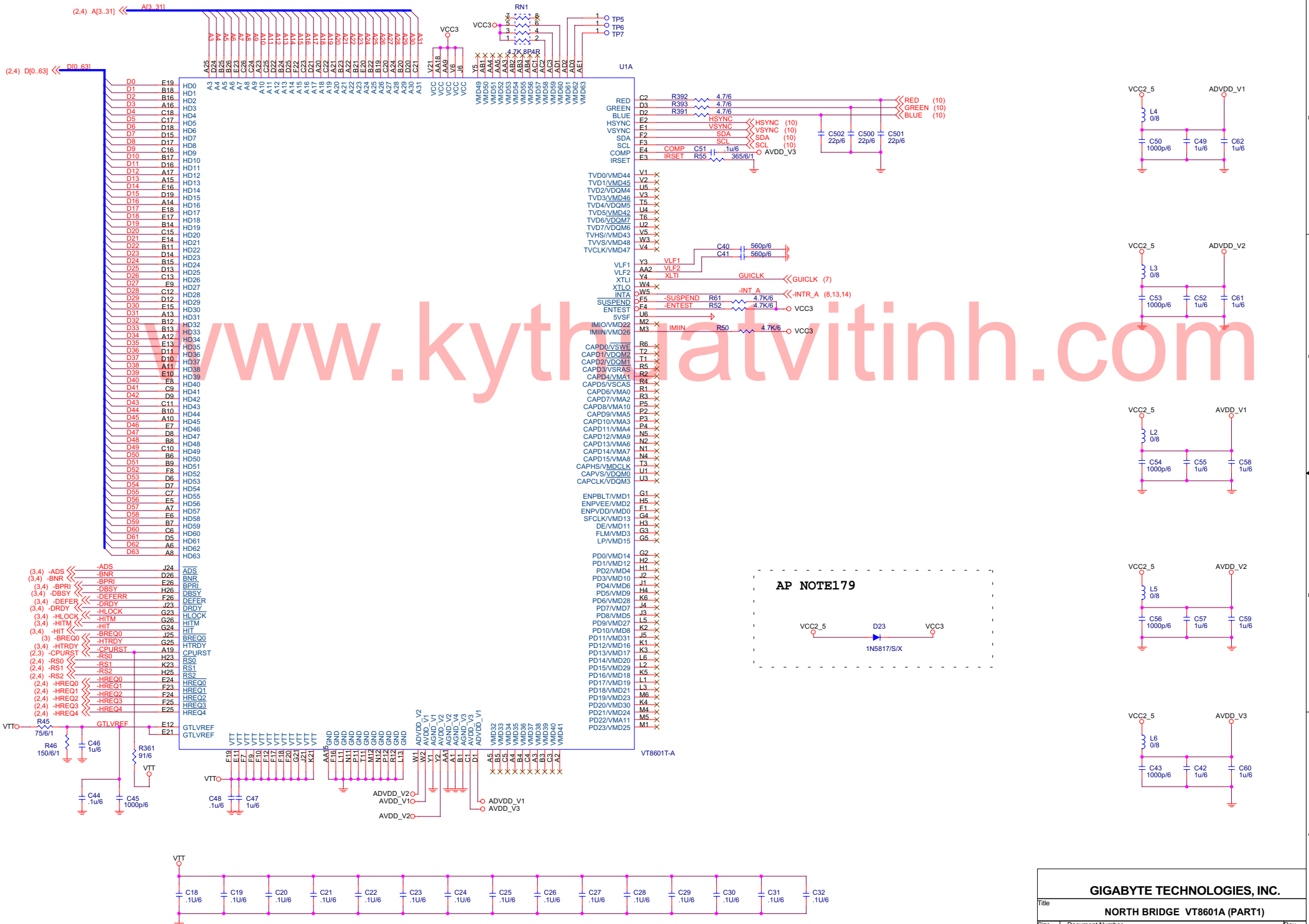
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SOCKET 370			
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GTL Termination

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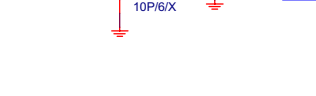
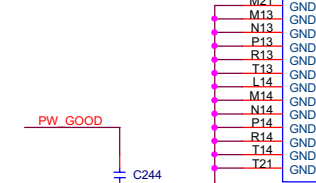
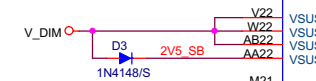
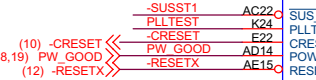
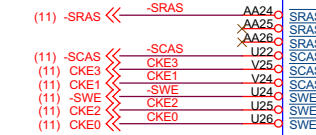
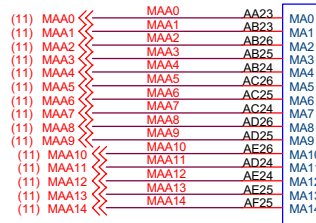
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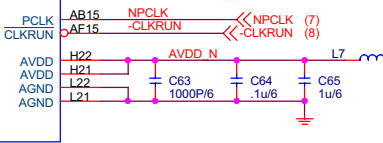
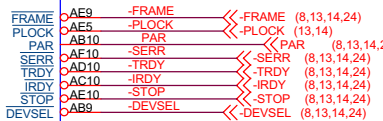
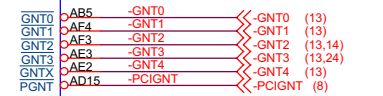
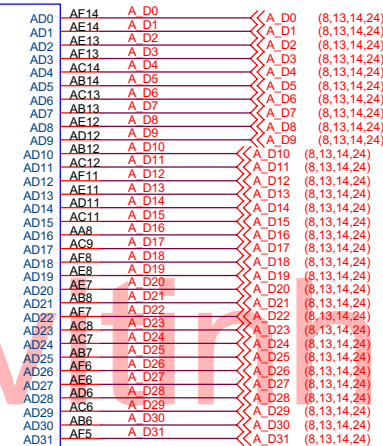


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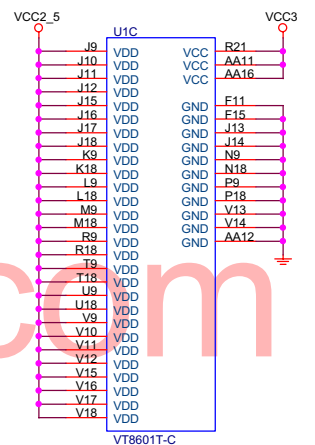
(11) MD[0:63] <<



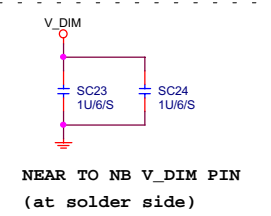
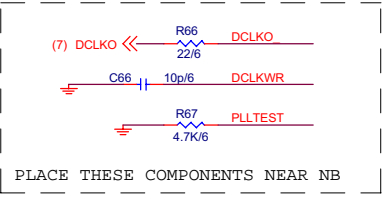
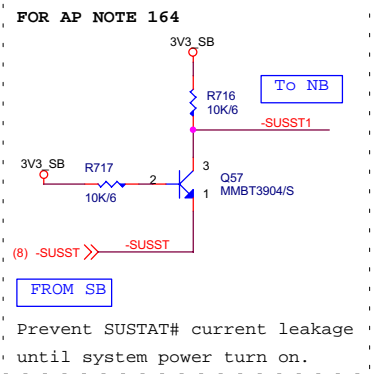
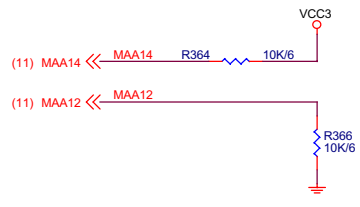
U1B



VT8601T-B

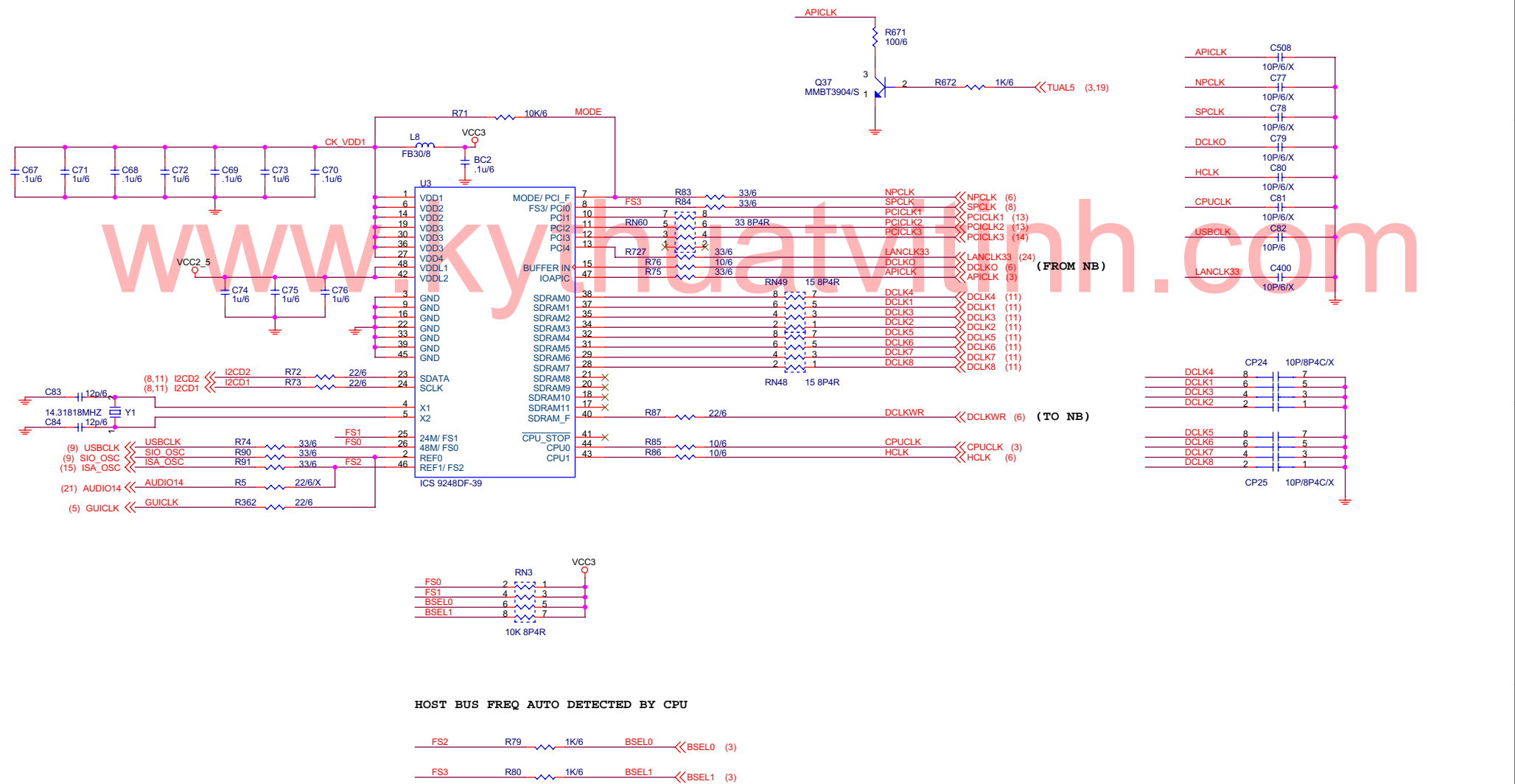


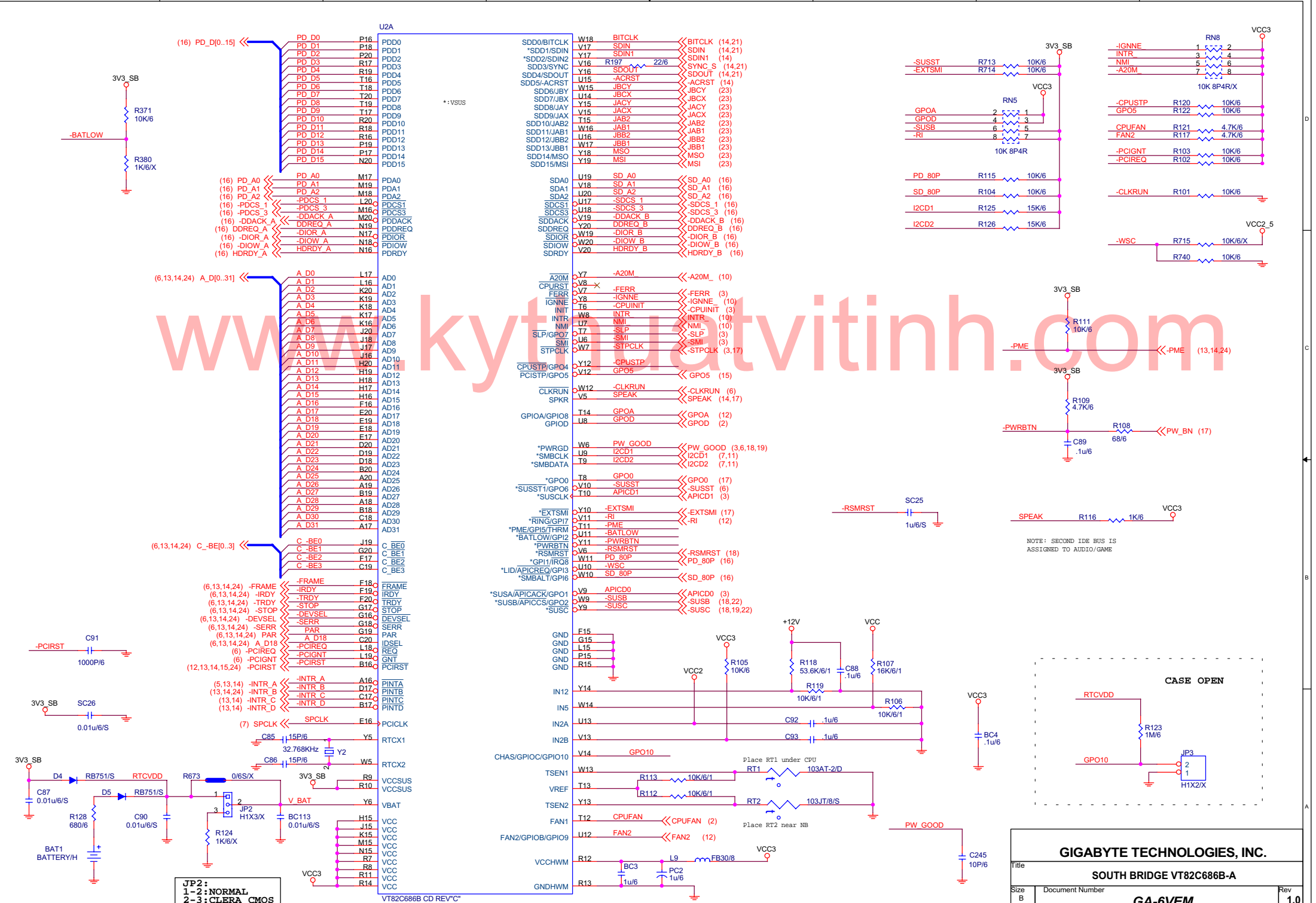
VT8601T-C



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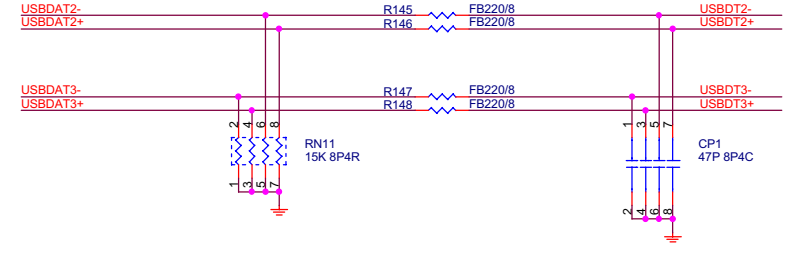
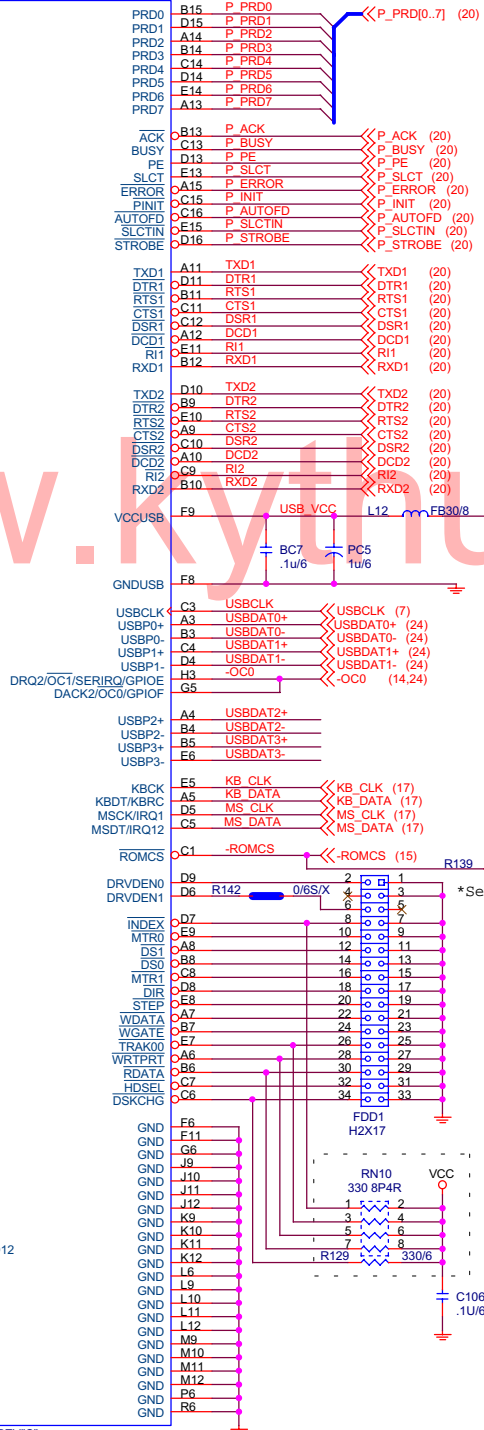
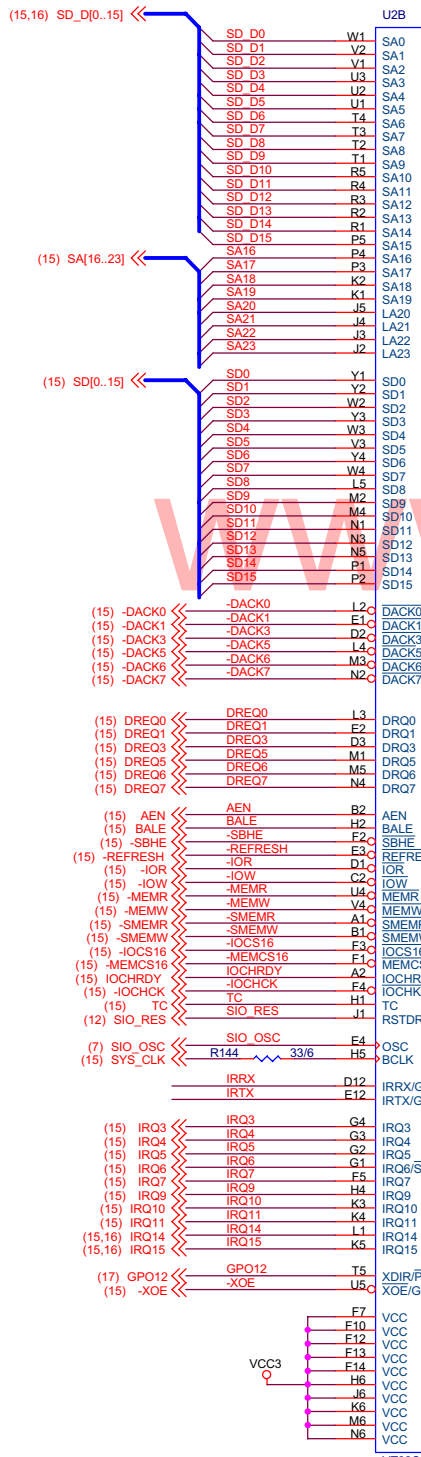


JP2 :
 1-2 : NORMAL
 2-3 : CLERA CMOS

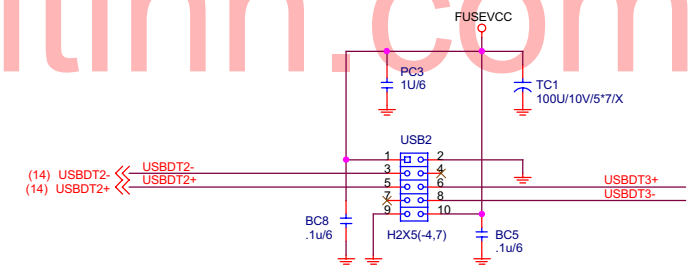
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SOUTH BRIDGE VT82C686B-A

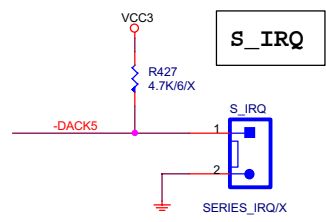
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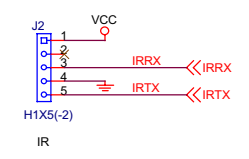
USB2



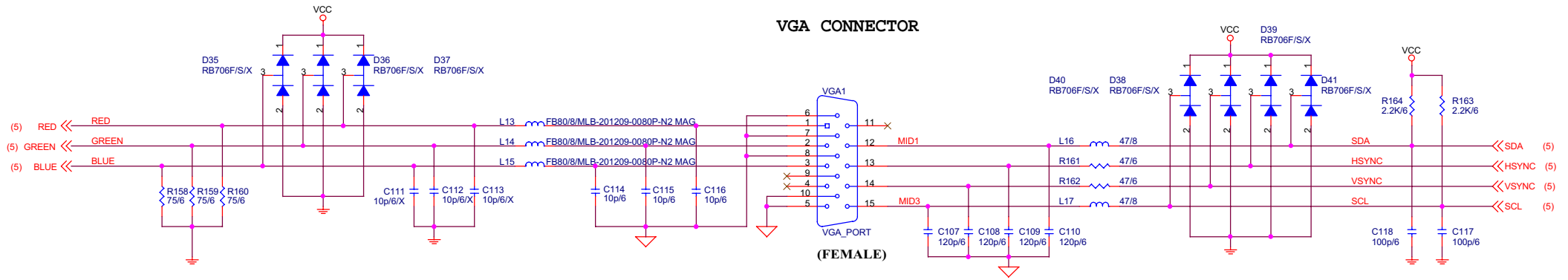
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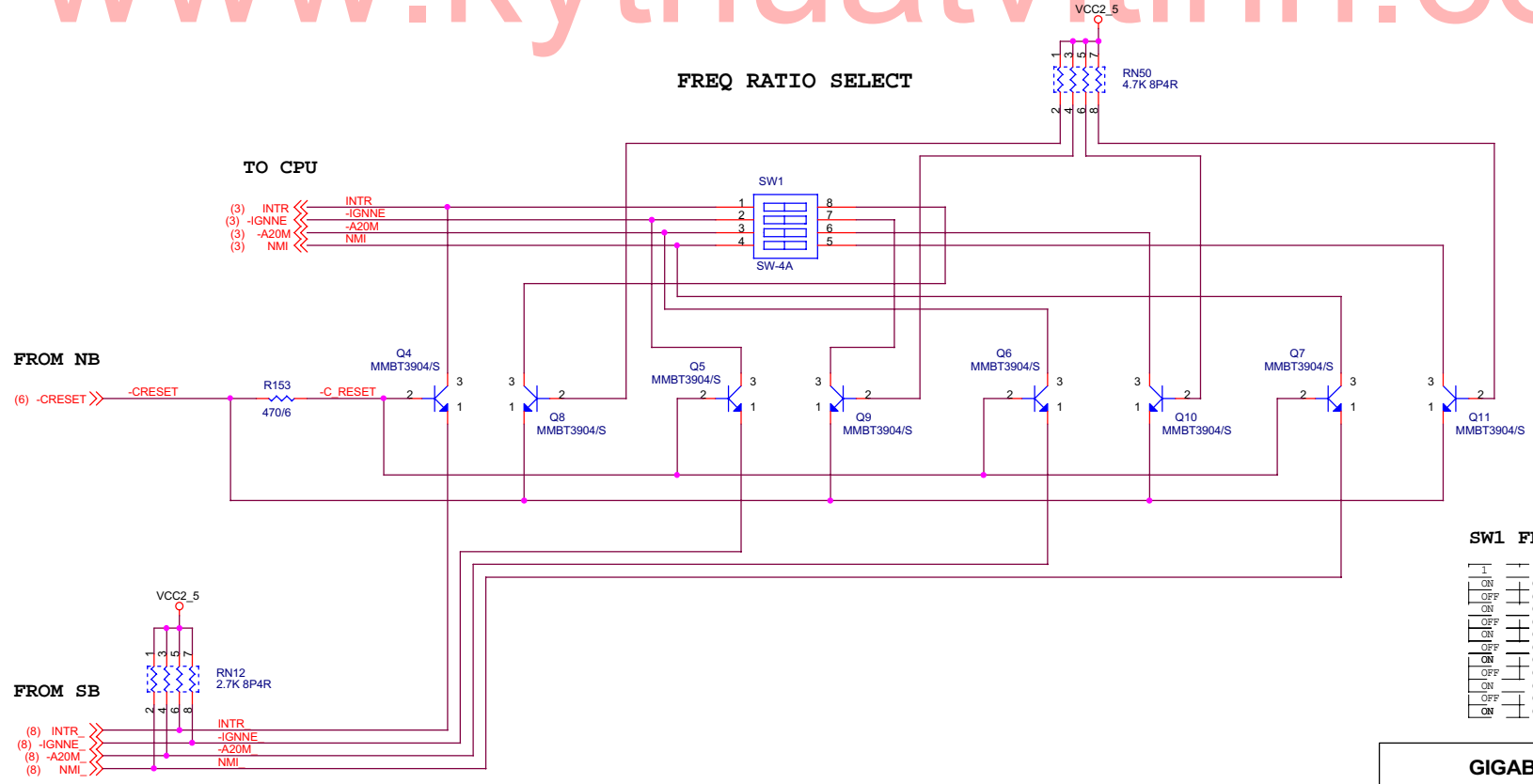
IR



GIGABYTE TECHNOLOGIES, INC.		
Title: SOUTH BRIDGE VT82C686B-B & USB & IR		
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SW1 FREQ RATIO LIST

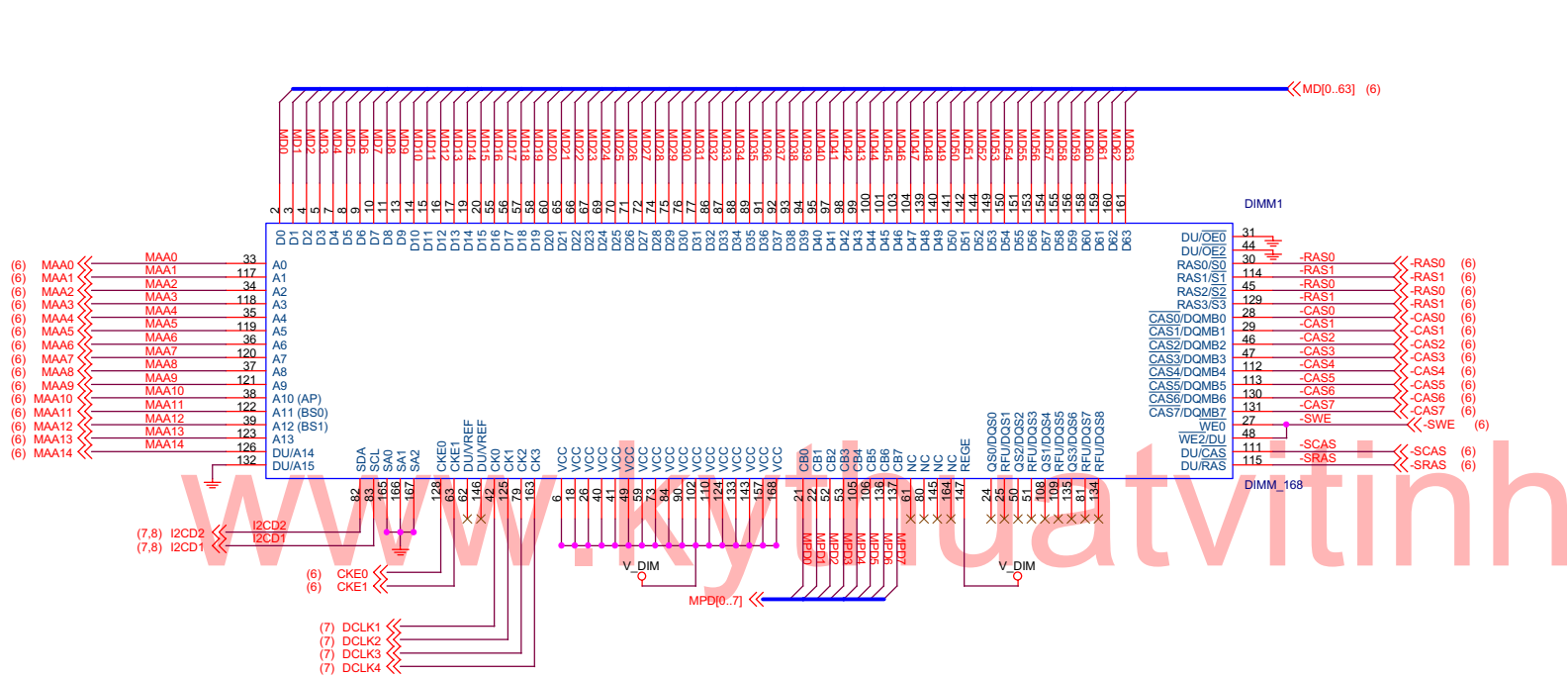
1	2	3	4	CLR	RATIO
ON	OFF	ON	ON	X3	
OFF	OFF	ON	ON	X3.5	
ON	ON	OFF	ON	X4	
OFF	ON	OFF	ON	X4.5	
ON	OFF	OFF	ON	X5	
OFF	OFF	OFF	ON	X5.5	
ON	ON	ON	OFF	X6	
OFF	ON	ON	OFF	X6.5	
ON	OFF	ON	OFF	X7	
OFF	OFF	ON	OFF	X7.5	
ON	ON	OFF	OFF	X8	

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Title: **VGA PORT & FREQ RATIO**

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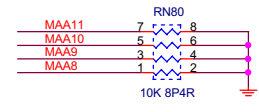
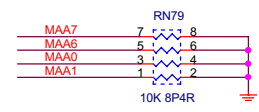
MA1	8601	oCLOCK	DELAY
LO	LO	0	
LO	HI	1	
HI	LO	2	
HI	HI	3	

8601:MA13 , 8603:MA6	
GTL	i/O BUFFER PULLUP
HI	DISABLE
LO	ENABLE

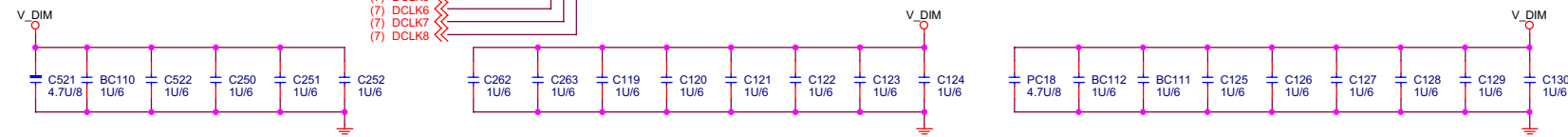
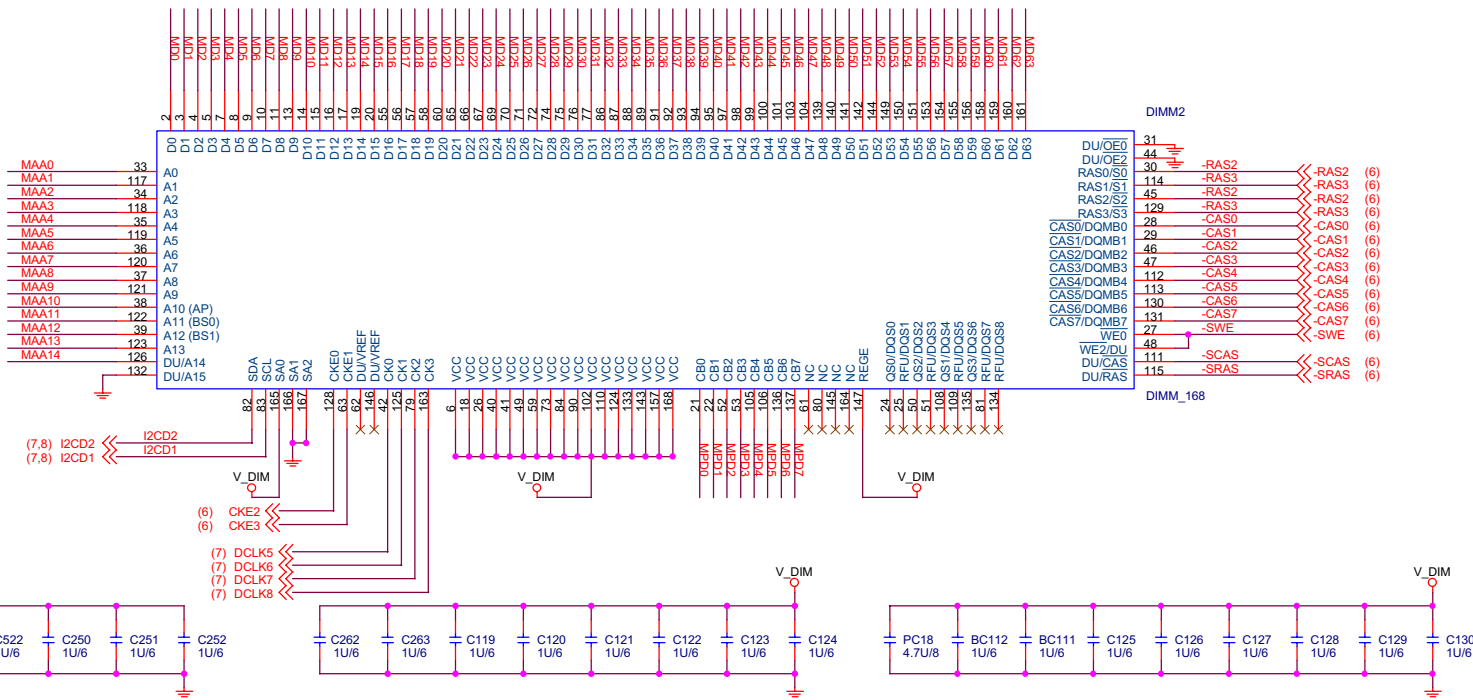
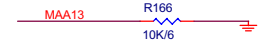
MA8	8601	GRAPHIC MODE
LO	LO	NORMAL
LO	HI	Graphic
HI	X	NB+Graphic

8601		8603	
MA10	MA9	NB/CLOCK DELAY	MA9
LO	LO	0	HI
LO	HI	1	LO
HI	LO	2	LO
HI	HI	3	LO
		DCLK, ECLK	SELECT
			EXTERNAL
			INTERNAL

8601 & 8603	
MA7	GRAPHIC TEST MODE
HI	TEST MODE
LO	NORMAL MODE



8601 & 8603	
MA11	IOO LENGTH
HI	1
LO	4

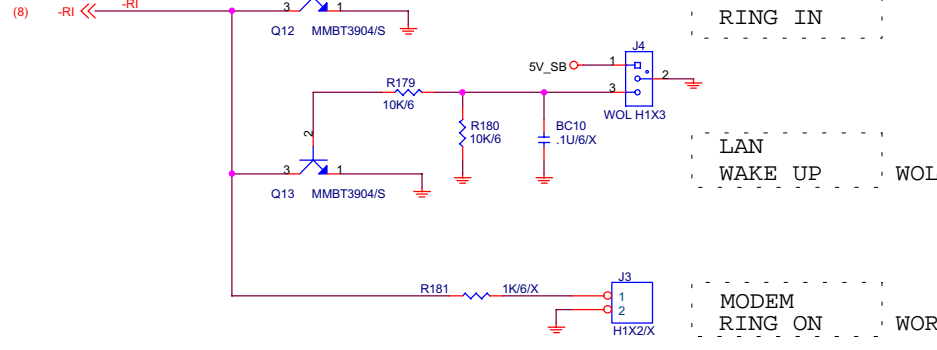
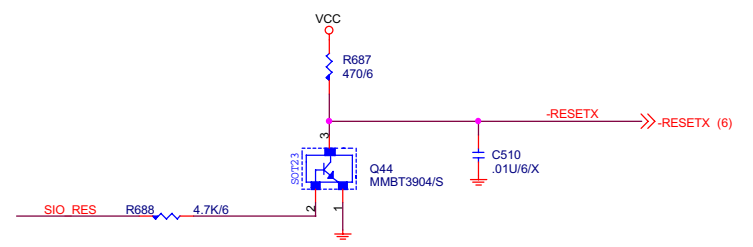
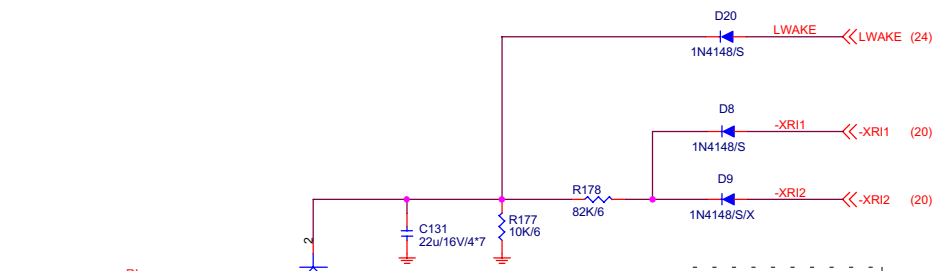
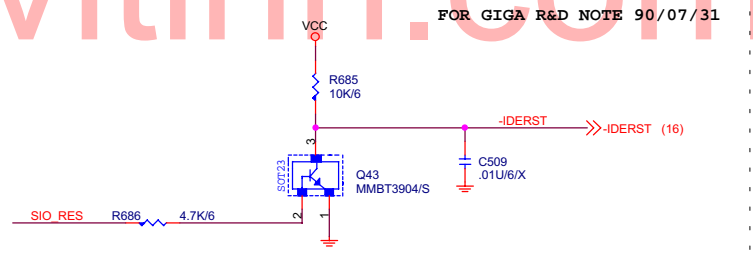
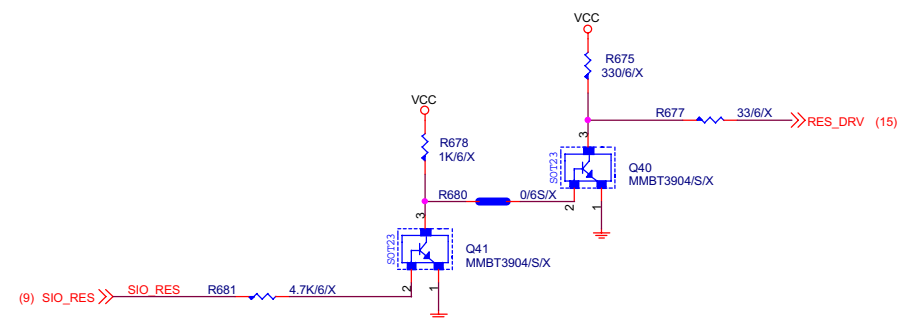
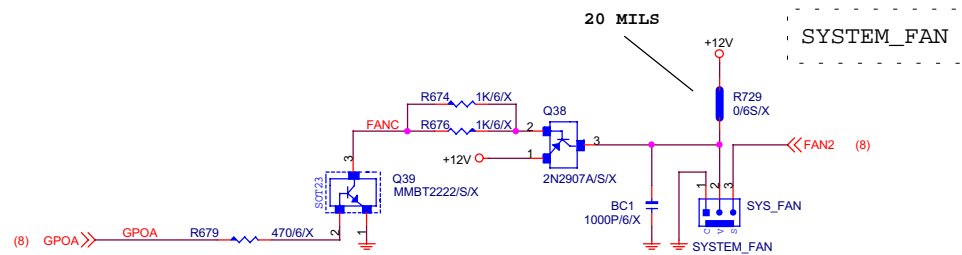


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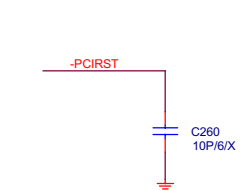
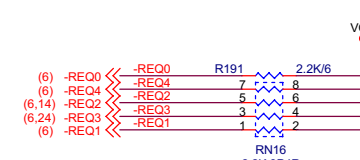
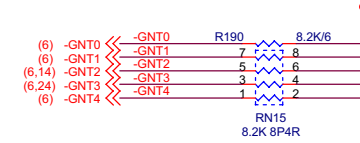
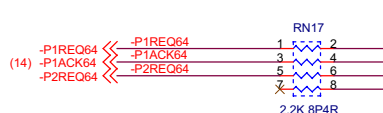
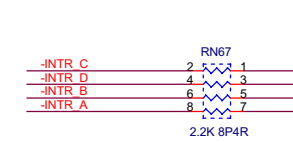
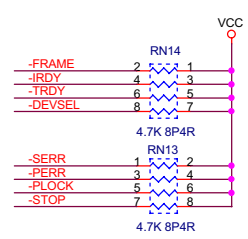
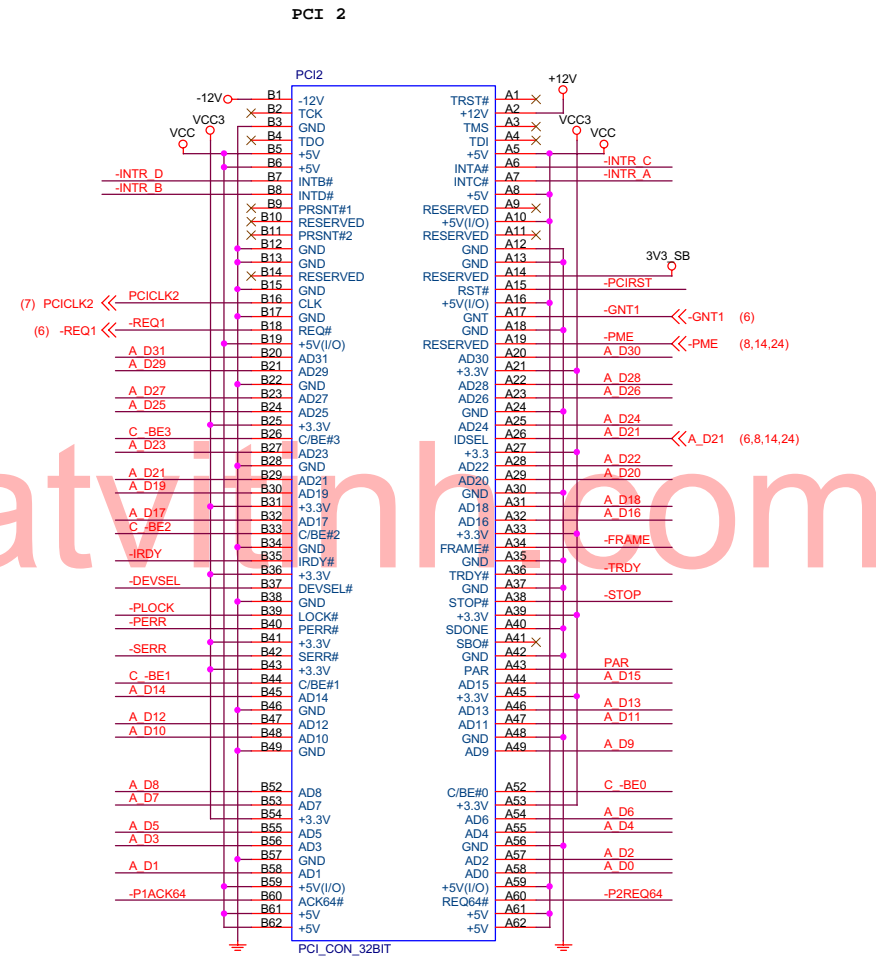
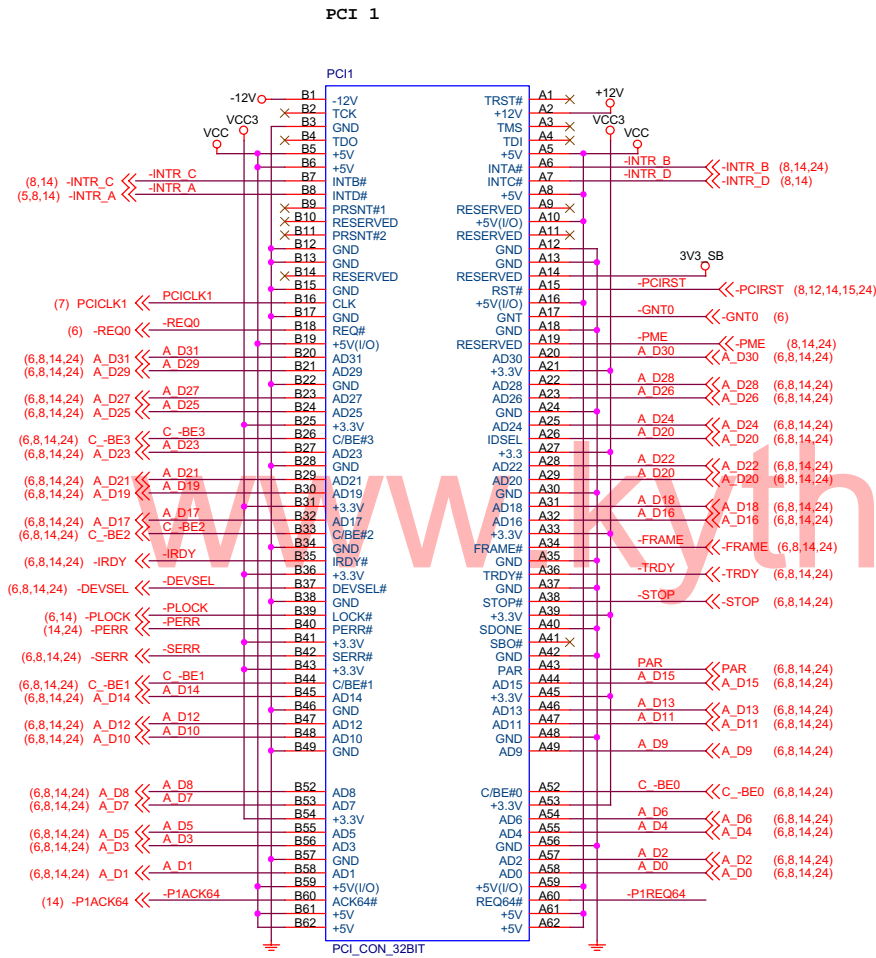
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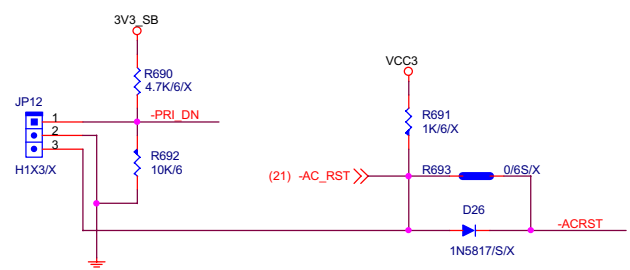
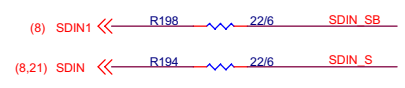
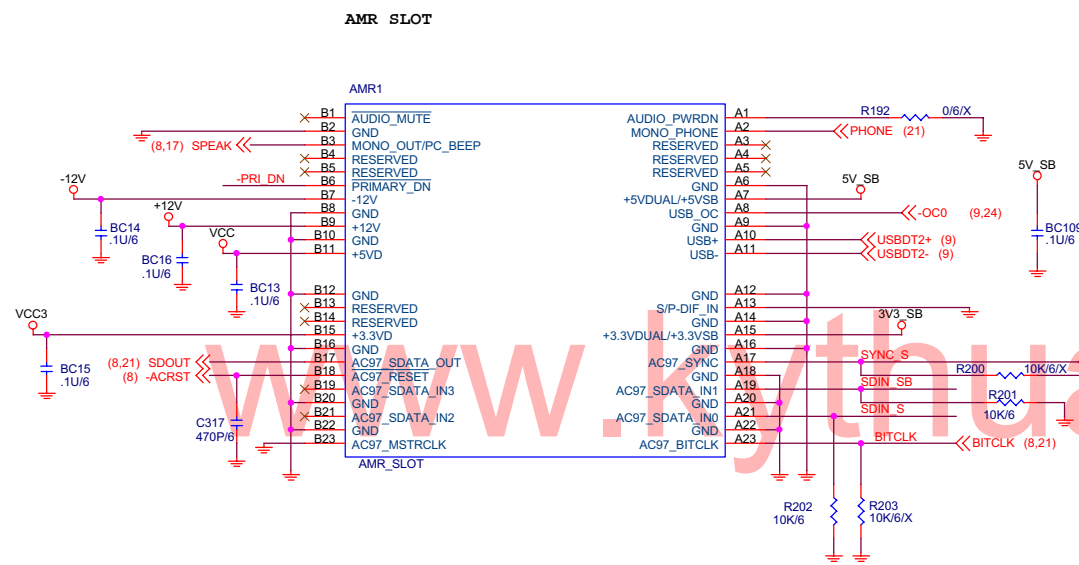
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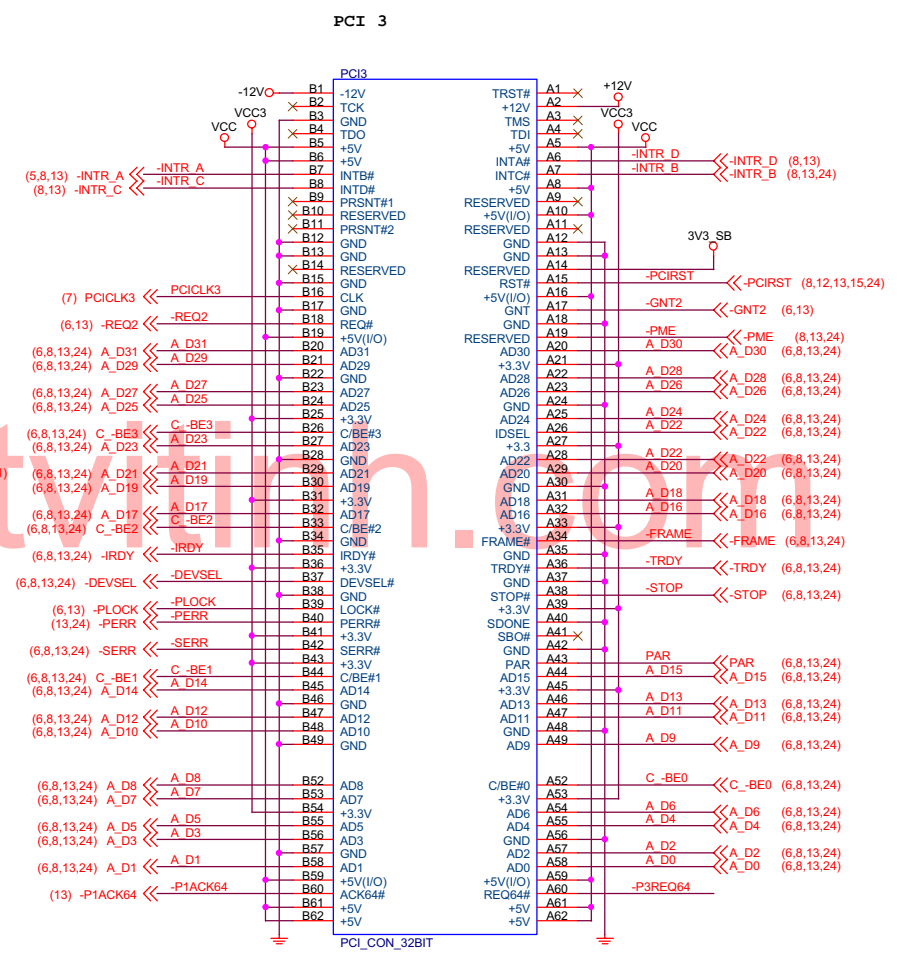
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JP12: AMR SELECT	
1-2	SECONDARY (DEFAULT)
2-3	PRIMARY



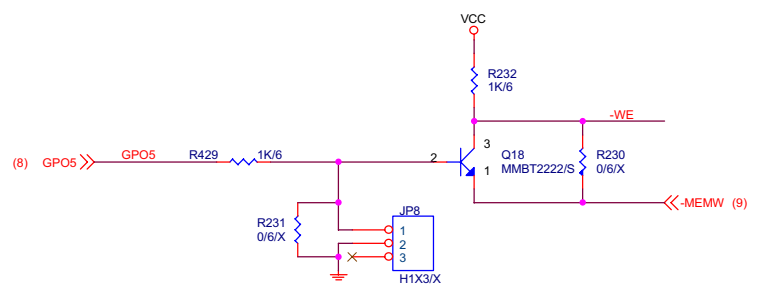
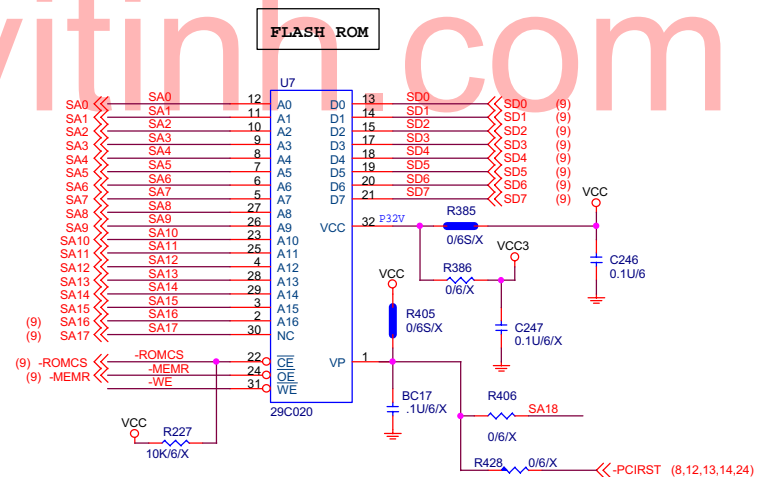
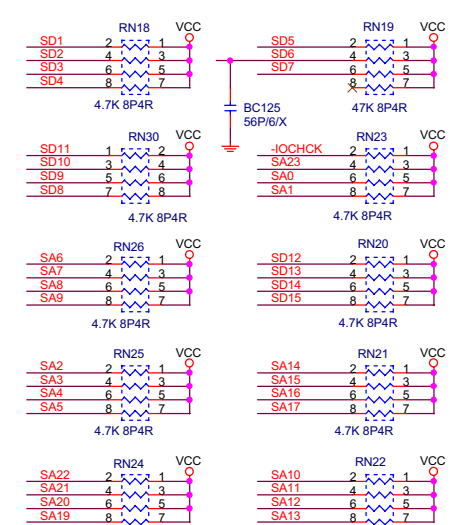
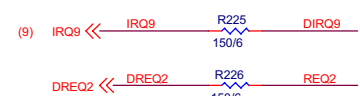
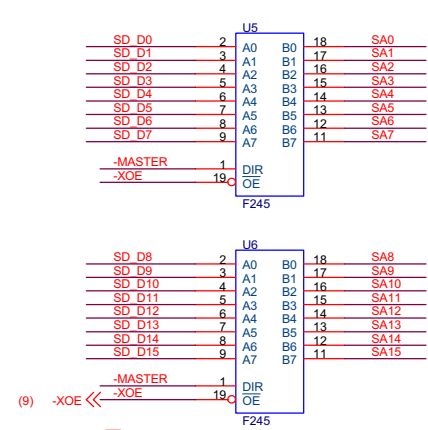
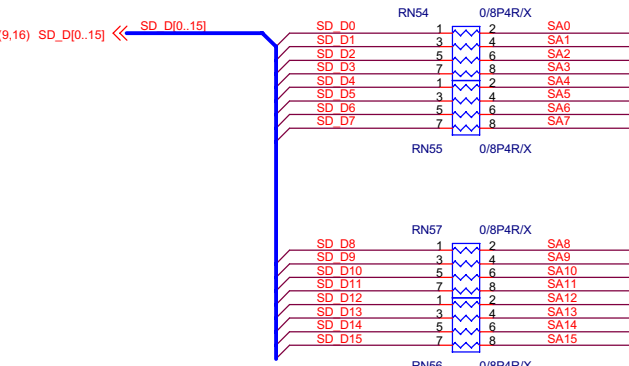
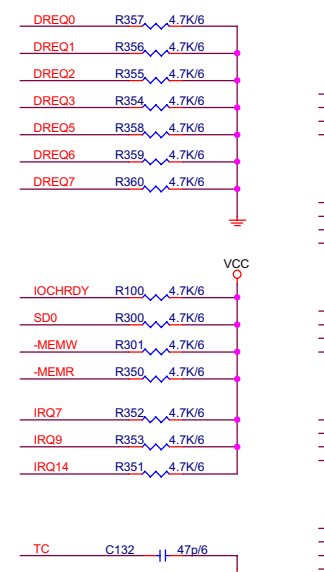
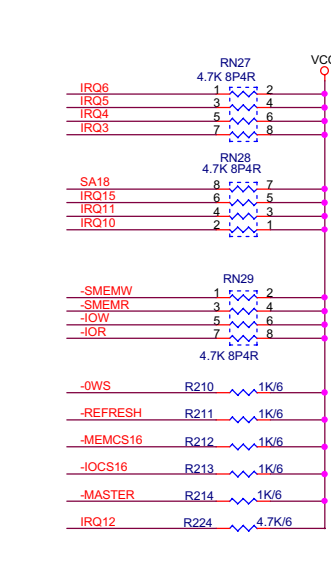
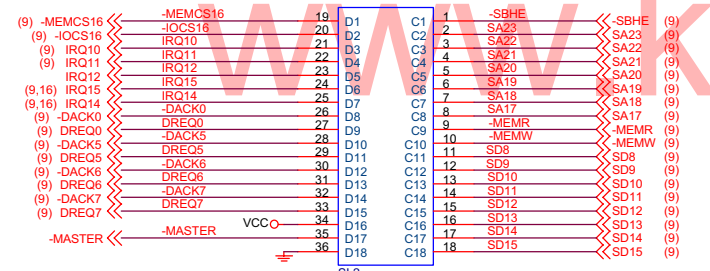
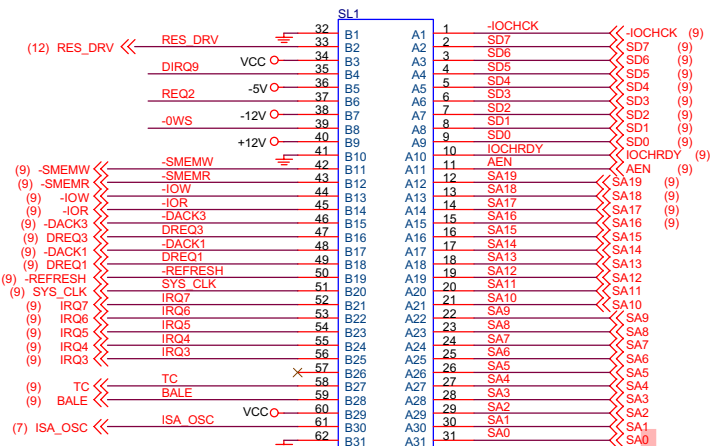
GIGABYTE TECHNOLOGIES, INC.

Title: **AMR SLOT & PCI3**

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ISA SLOT



JP8: BIOS WRITE PROTECT

1-2	ENABLE (WRITE PROTECT ENABLE)
2-3	AUTO (WRITE PROTECT DISABLE) (CONTROL BY BIOS)

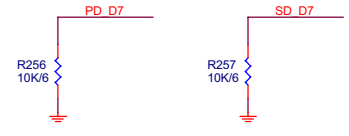
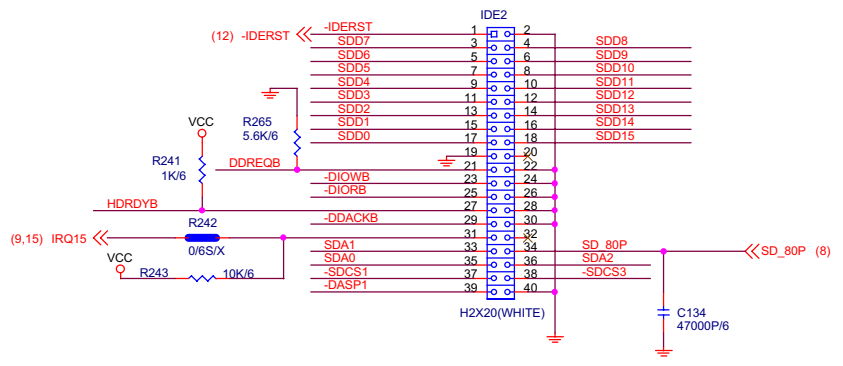
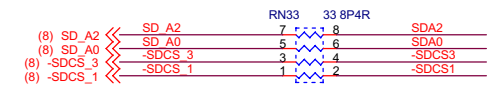
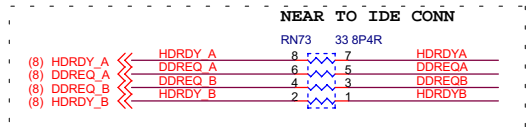
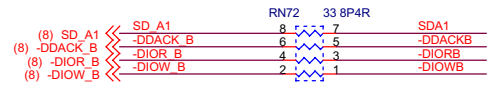
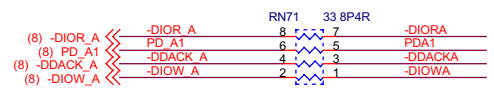
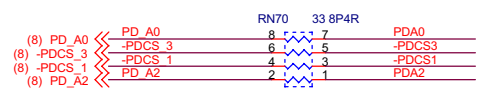
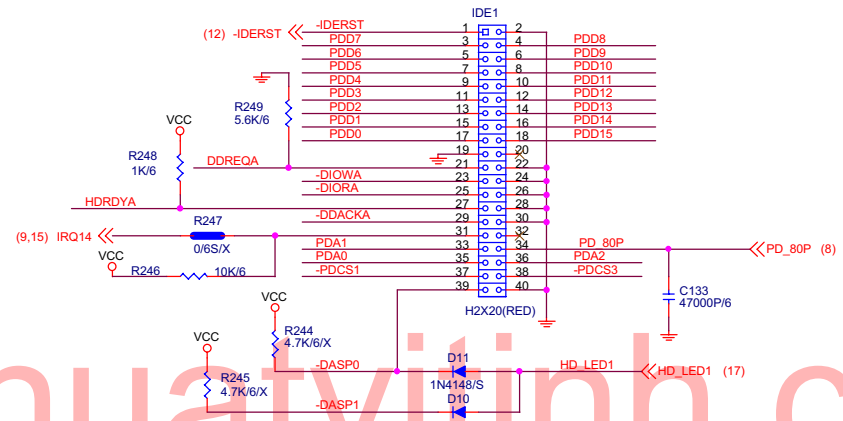
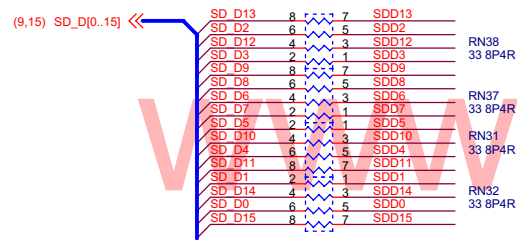
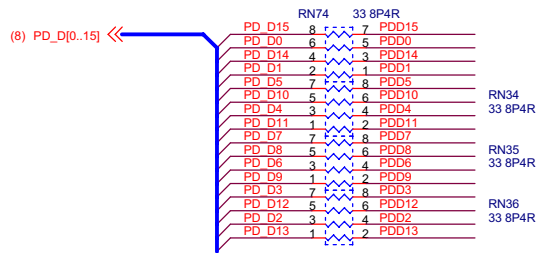
DEFAULT (SHORT 2-3)

GIGABYTE TECHNOLOGIES, INC.

Title: **ISA SLOT & BIOS**

Size B Document Number: **GA-6VEML** Rev: **1.0**

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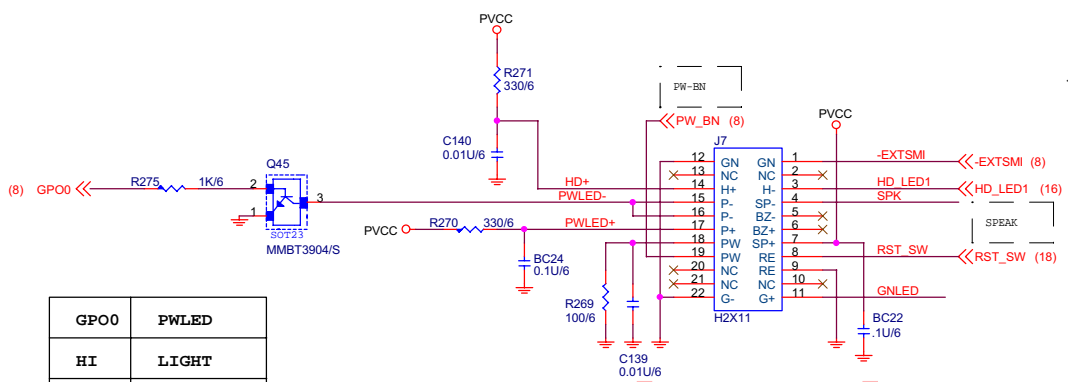


GIGABYTE TECHNOLOGIES, INC.

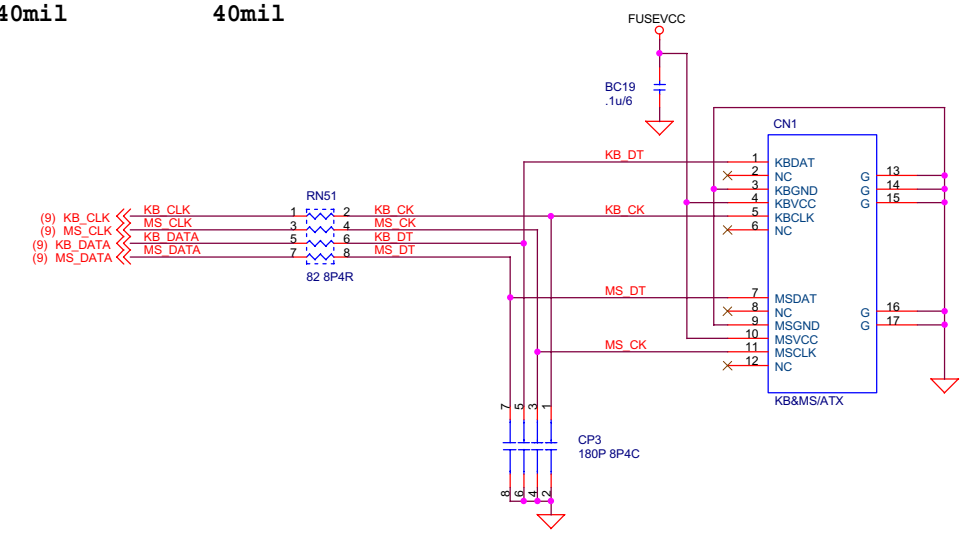
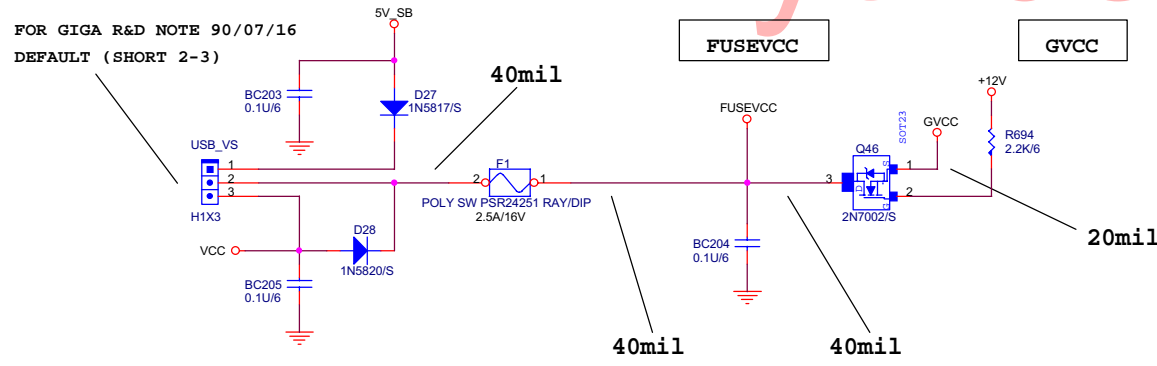
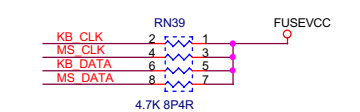
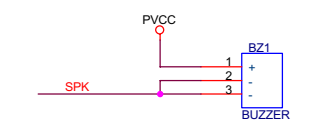
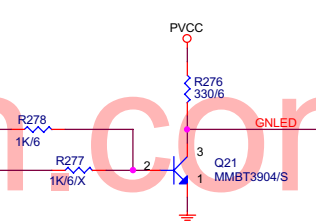
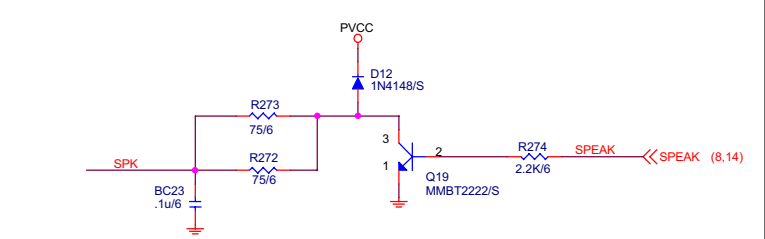
Title: IDE1 & IDE2

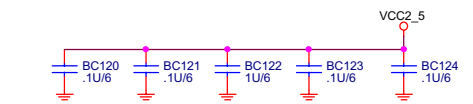
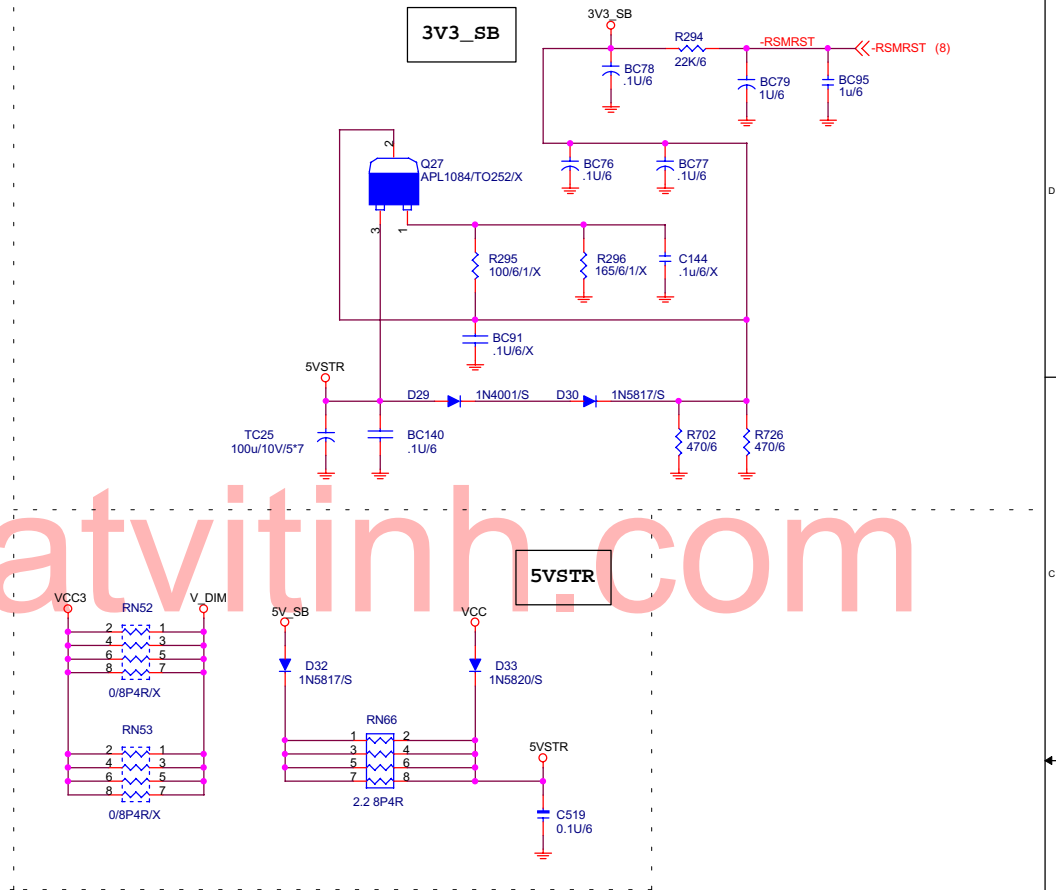
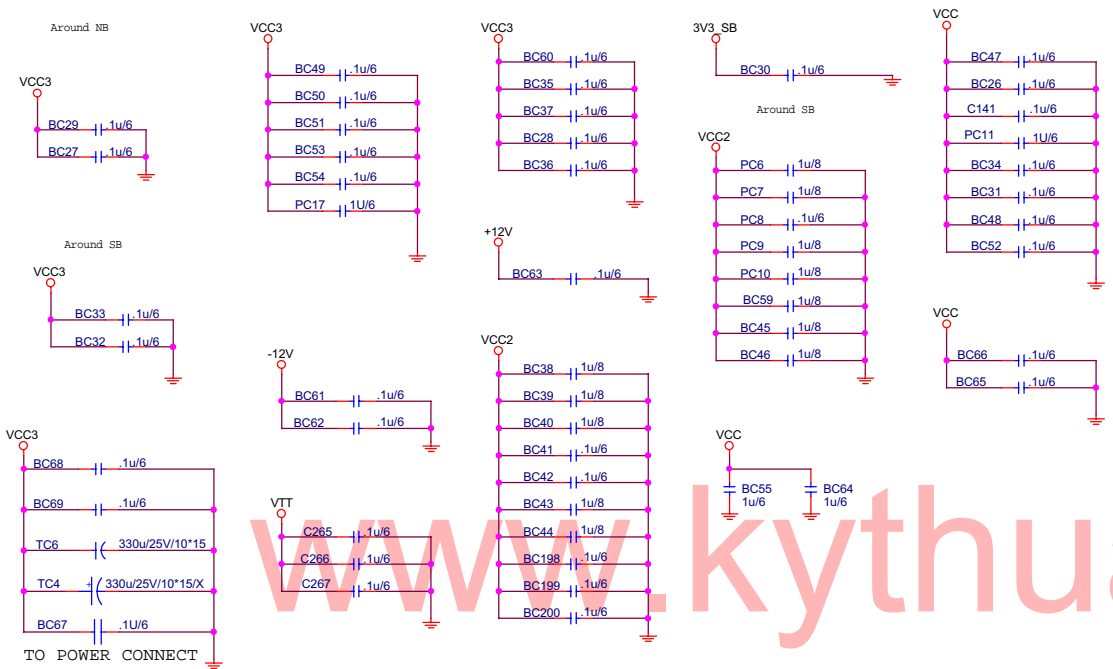
Size B Document Number **GA-6VEML** Rev 1.0

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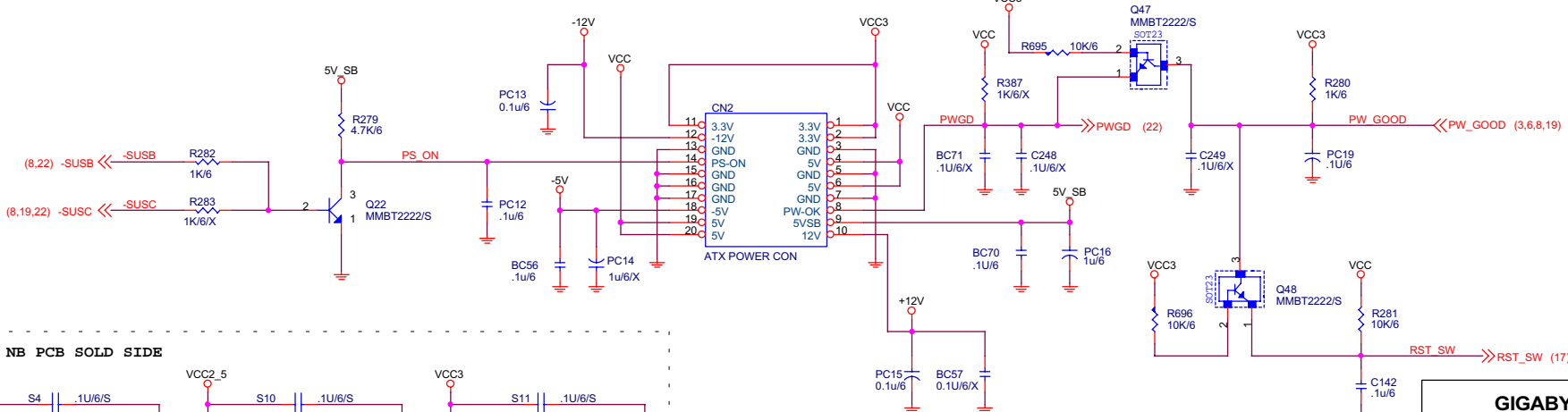


GPO0	PWLED
HI	LIGHT
LO	NOT LIGHT

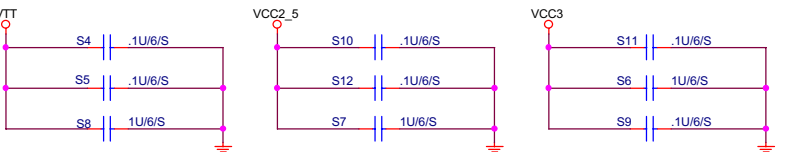




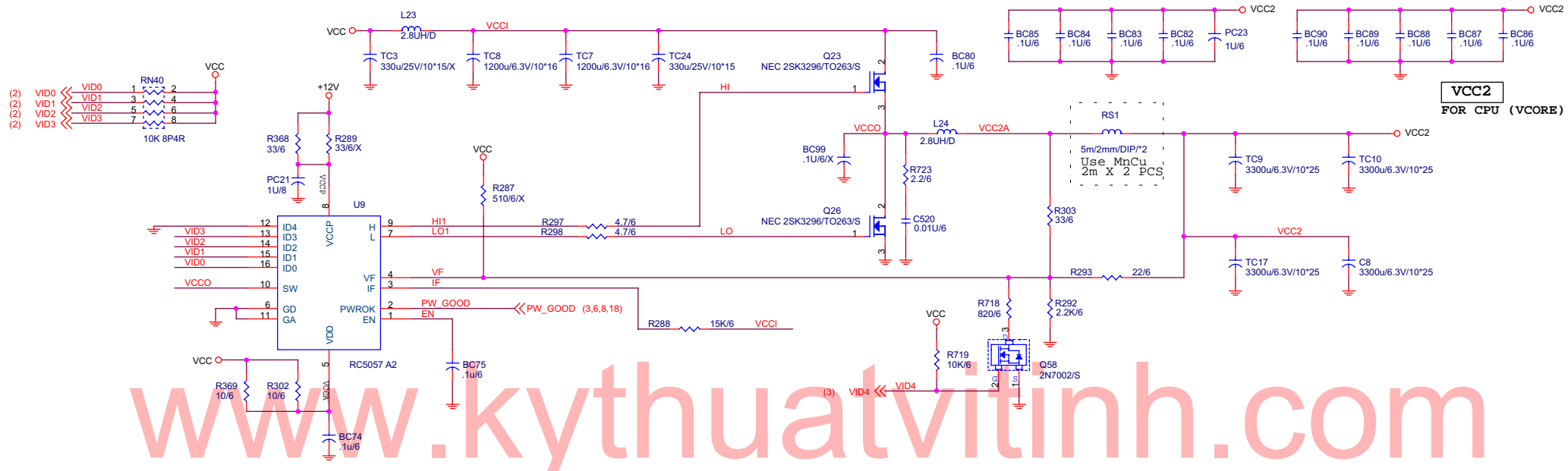
ATX POWER CONN



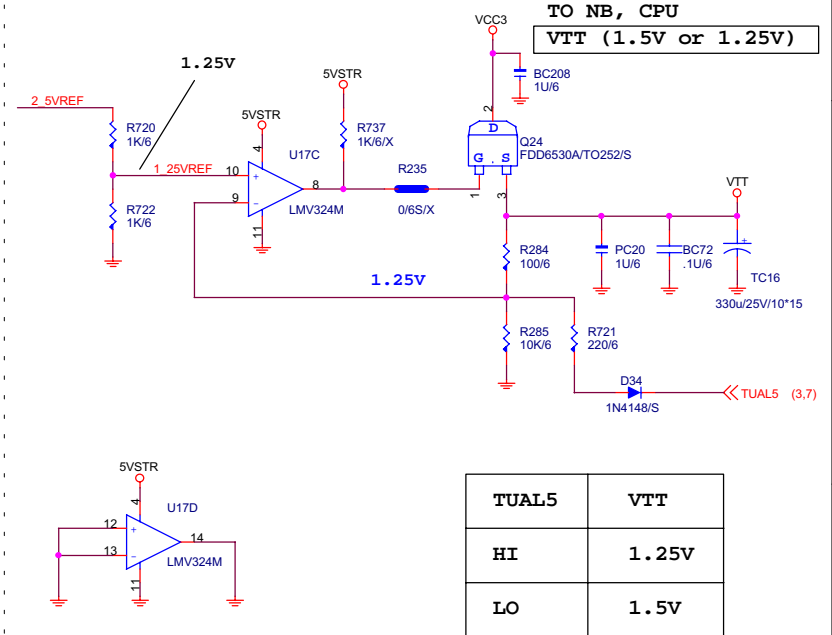
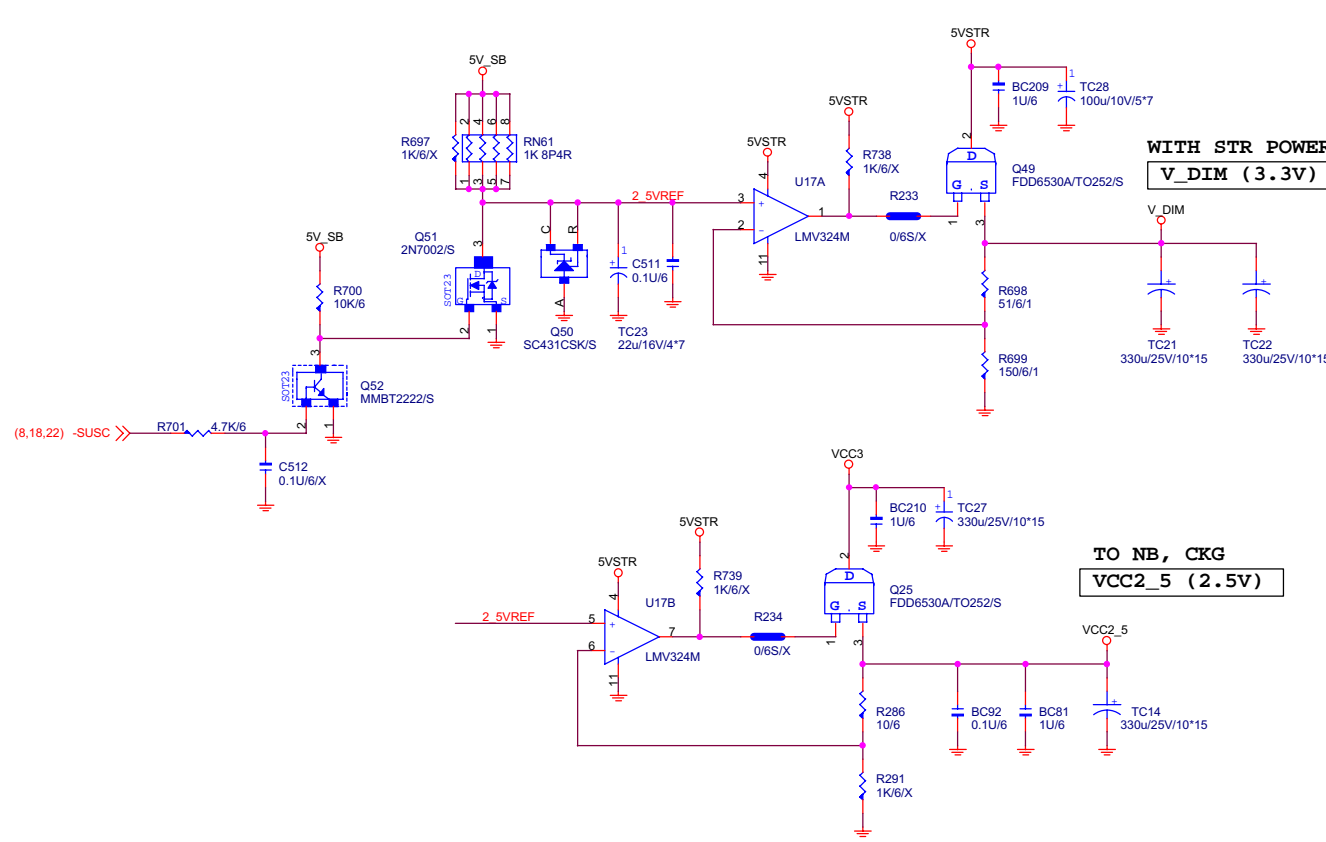
TO NB PCB SOLD SIDE



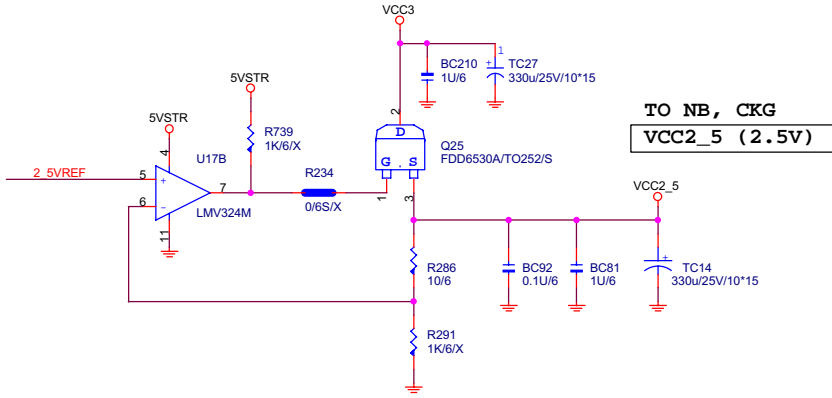
GIGABYTE TECHNOLOGIA, INC.		
Title	POWER CONNECTOR & BYPASS CAPACITORS	
Size	Document Number	Rev
B	GA-6VEML	1.0
Date:	Friday, September 07, 2001	Sheet 18 of 26

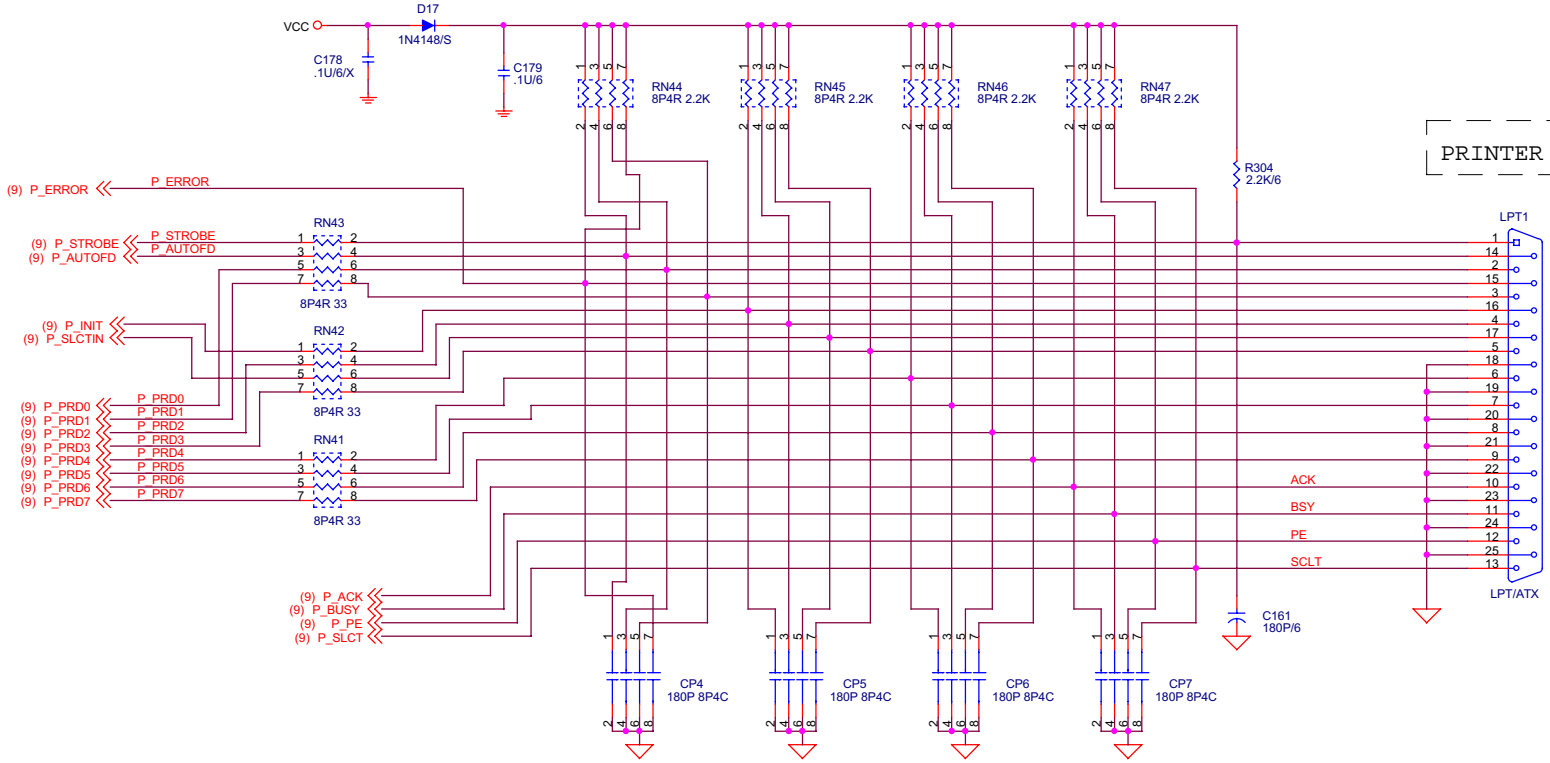
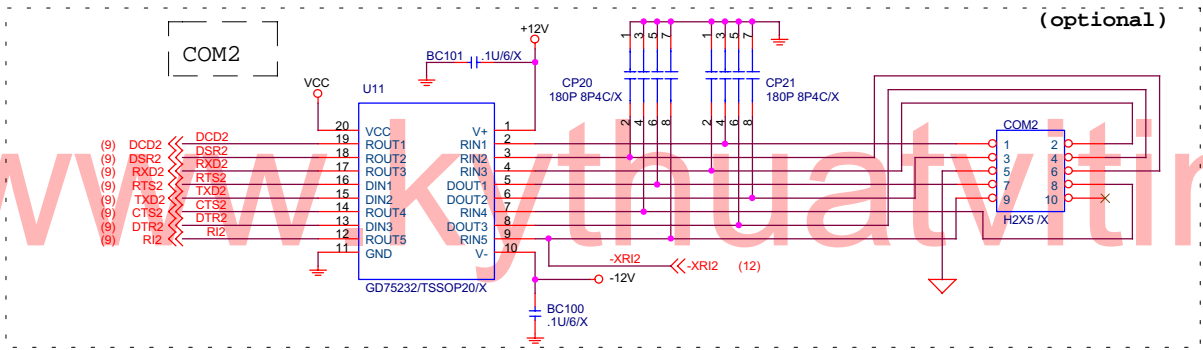
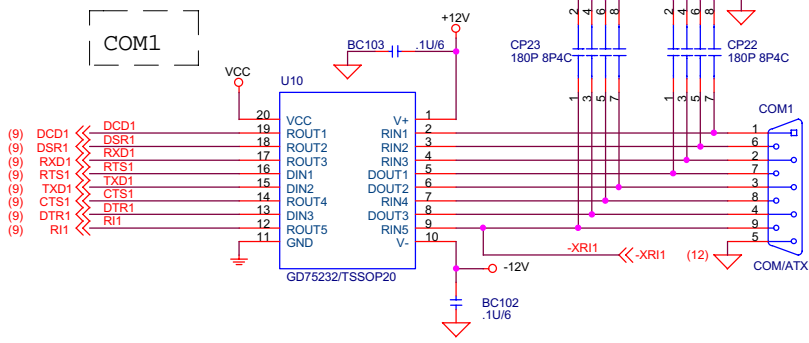


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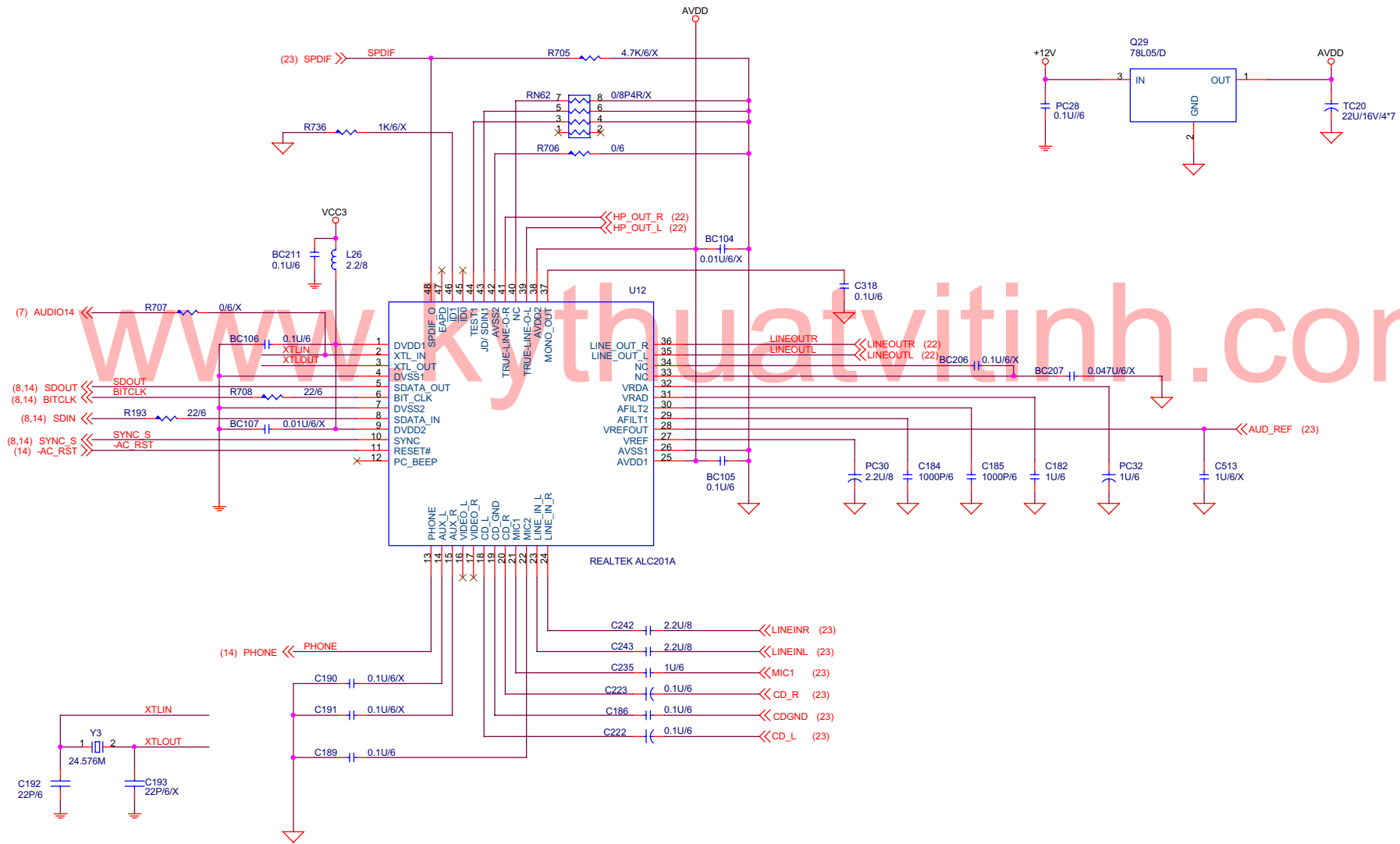
TUAL5	VTT
HI	1.25V
LO	1.5V



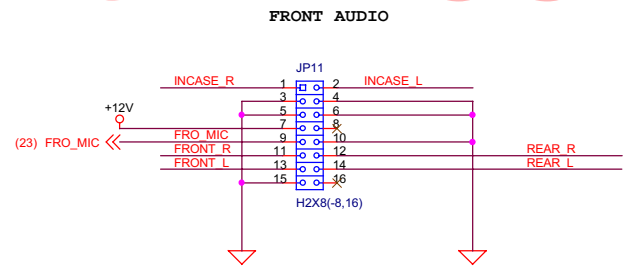
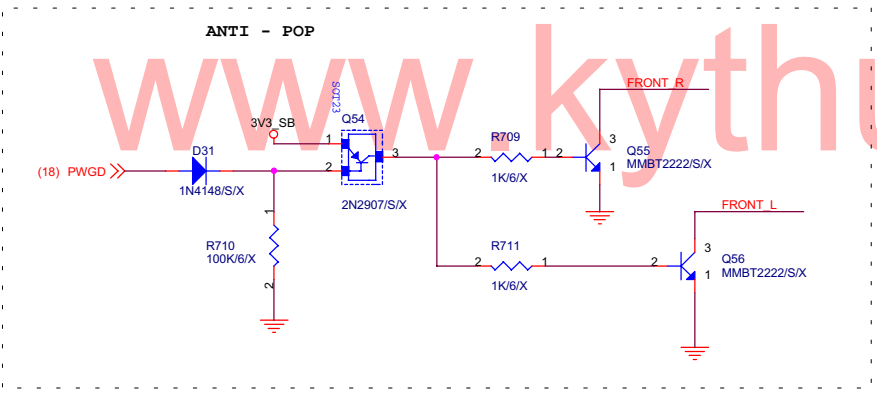
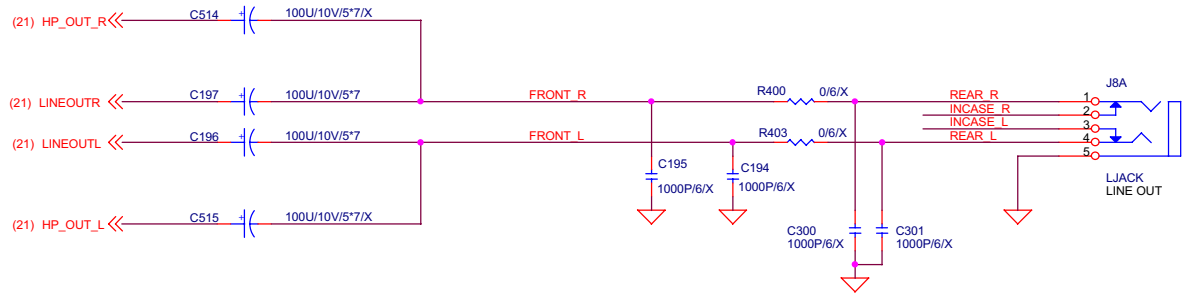


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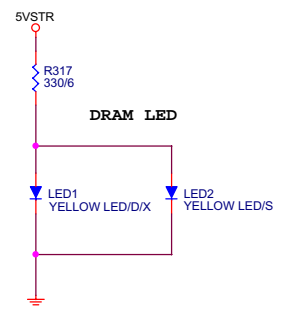
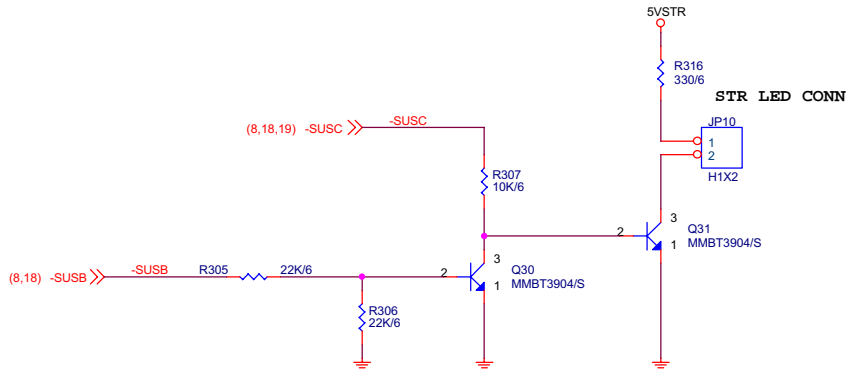
GIGABYTE TECHNOLOGIES, INC.		
Title PRINTER & COM PORT		
Size B	Document Number GA-6VEML	Rev 1.0
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GIGABYTE TECHNOLOGIES, INC.		
Title CODEC		
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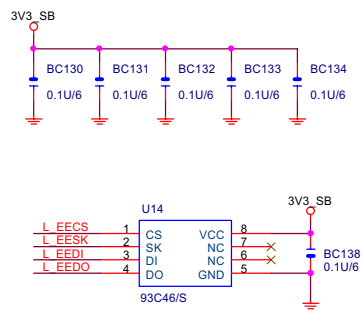
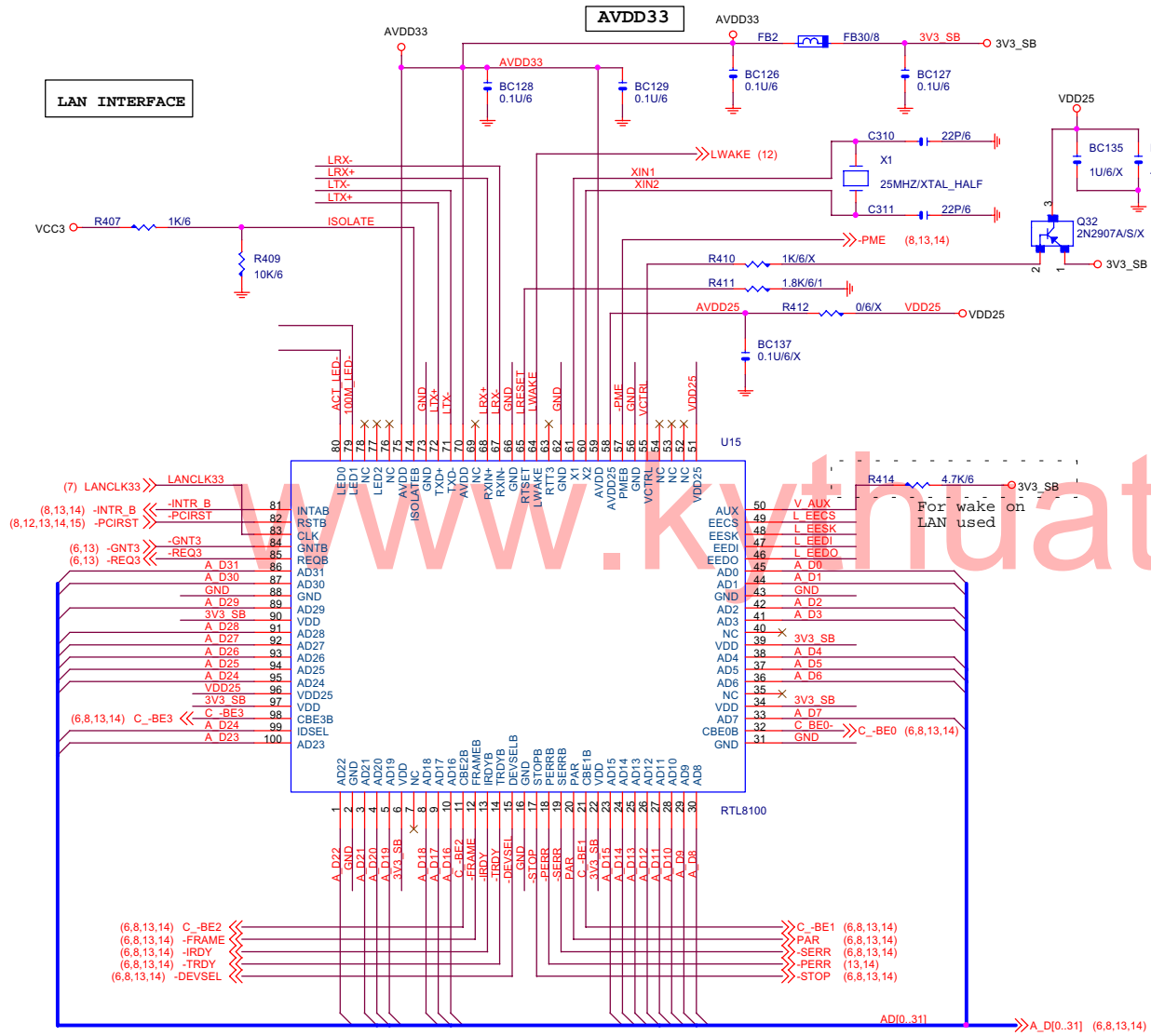


Front AUDIO:
11-12:CLOSE
13-14:CLOSE

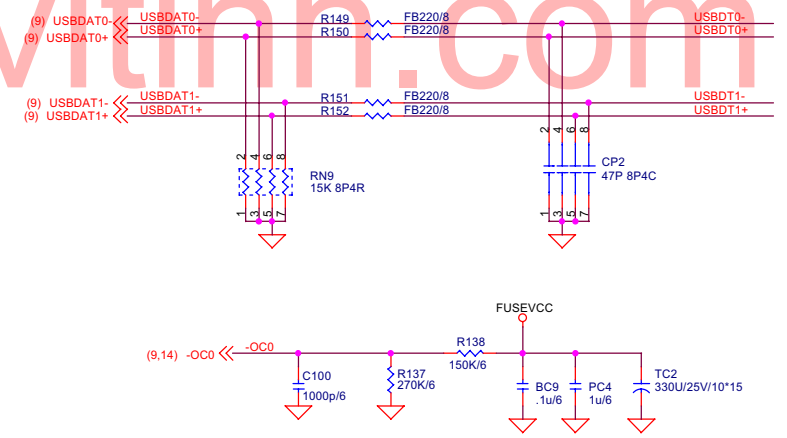


GIGABYTE TECHNOLOGIES, INC.		
Title L/JACK LINE OUT & STR LED		
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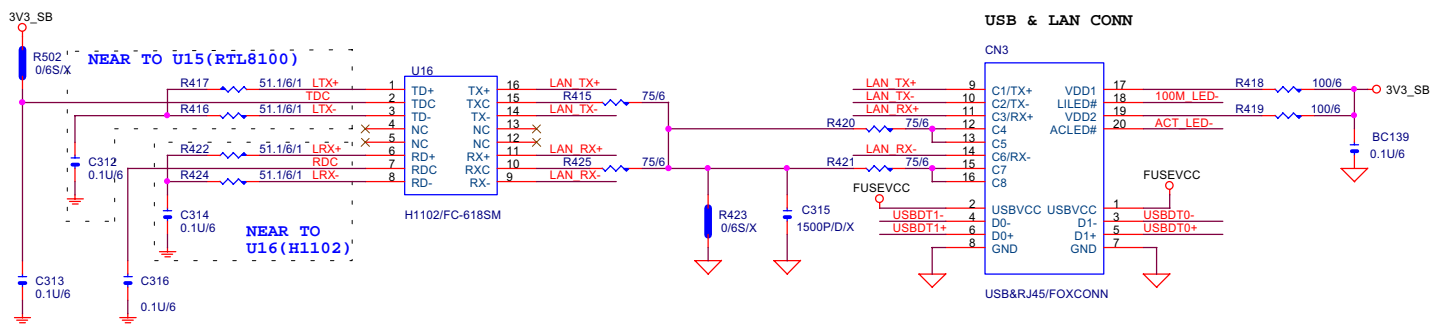
LAN INTERFACE



USB CIRCUIT



USB & LAN CONN



8100/8100B NOTE:
 Pin 65 pull-down (5.9K for 8100B)
 Pin 65 pull-down (1.8K for 8100)
 R502 remove pull-down (1.8K for 8100B)
 R502:0/6 pull-down (1.8K for 8100)

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File LAN REALTEK 8100B		
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GIGABYTE GA-6VEML GPIO LIST

Revision 1.0

PIN	GPI	CHIPSET POWER	
F4	GPI0/ <u>-IOCHCK</u>	VCC3	PULL 4.7K TO VCC3 (ISA SLOT)
W11	GPI1/ <u>IRQ8/ PD_80P</u>	3V3_SB	PULL 10K TO 3V3_SB (IDE1)
U11	GPI2/ <u>-BATLOW</u>	3V3_SB	PULL 10K TO 3V3_SB
U10	GPI3/ <u>LID / -WSC</u>	3V3_SB	PULL 10K TO VCC2_5
G1	GPI4/ <u>-SLPBTN/ IRQ6</u>	VCC3	PULL 4.7K TO VCC (ISA SLOT)
T11	GPI5/ <u>THRM / -PME</u>	3V3_SB	PULL 10K TO 3V3_SB (TO PCI SLOT, RTL8100)
W10	GPI6/ <u>-SMBALT/SD_80P</u>	3V3_SB	PULL 10K TO 3V3_SB (IDE2)
* V11	GPI7/ <u>-RI</u>	3V3_SB	PULL 10K TO 3V3_SB (WOL, WOR)
* T14	GPI08/ <u>GPOWE/GPOA</u>	VCC3	PULL 10K TO VCC3 (SYS_FAN CONTROL ON/OFF)
* U12	GPI09/ <u>GPIOB/FAN2</u>	VCC3	PULL 4.7K TO VCC3 (FAN2) (TO SYS_FAN SENSOR PIN)
* V14	GPI010/ <u>GPIOC/CHAS</u>	VCC3	PULL 1M TO RTCVDD (CASE OPEN)
* U8	GPI011/ <u>-MCCS/GPOD</u>	VCC3	PULL 10K TO VCC3 (CPU_FAN CONTROL ON/OFF)
	GPI12	VCC3	NOT IMPLEMENTED
	GPI13	VCC3	NOT IMPLEMENTED
	GPI14 (N/A)		NOT IMPLEMENTED
	GPI15 (N/A)		NOT IMPLEMENTED
L3	GPI16/ <u>DREQ0</u>	VCC3	PULL DOWN 4.7K (ISA SLOT)
E2	GPI17/ <u>DREQ1</u>	VCC3	PULL DOWN 4.7K (ISA SLOT)
D3	GPI18/ <u>DREQ3</u>	VCC3	PULL DOWN 4.7K (ISA SLOT)
M1	GPI19/ <u>DREQ5</u>	VCC3	PULL DOWN 4.7K (ISA SLOT)
M5	GPI20/ <u>DREQ6</u>	VCC3	PULL DOWN 4.7K (ISA SLOT)
N4	GPI21/ <u>DREQ7</u>	VCC3	PULL DOWN 4.7K (ISA SLOT)
W15	GPI22/ <u>JBCY</u>	VCC3	(TO GAME PORT OF JOYSTICK)
U14	GPI23/ <u>JBCX</u>	VCC3	(TO GAME PORT OF JOYSTICK)

PIN	GPO	CHIPSET POWER	
T8	GPO0/ <u>(H)/SLOWCLK</u>	3V3_SB	TTL output, Default High level (PWLED ON/OFF)
V9	GPO1/ <u>-SUSA/APICD0(H)</u>	3V3_SB	PULL 150 TO VCMOS (TO CPU)
W9	GPO2/ <u>-APICCS/-SUSB(H)</u>	3V3_SB	PULL 10K TO 3V3_SB (ATX POWER ON/OFF, STR LED)
V10	GPO3/ <u>-SUSST(H)</u>	3V3_SB	PULL 10K TO 3V3_SB TO NB (-SUSST1)
Y12	GPO4/ <u>-CPUSTP(L)</u>	VCC3	PULL 10K TO VCC3
V12	GPO5/ <u>-PCISTP(L)</u>	VCC3	PULL 10K TO VCC3 (BIOS WRITE PROTECT CONTROL)
	GPO6	VCC3	NOT IMPLEMENTED
* T7	GPO7/ <u>-SLP(OD)</u>	VCC3	PULL 150 TO VCMOS (TO CPU)
* T14	GPI08/ <u>GPOWE/GPOA</u>	VCC3	PULL 10K TO VCC3 (SYS_FAN CONTROL ON/OFF)
* U12	GPI09/ <u>GPIOB/FAN2</u>	VCC3	PULL 4.7K TO VCC3 (FAN2) (TO SYS_FAN SENSOR PIN)
* V14	GPI010/ <u>GPIOC/CHAS/GPO10</u>	VCC3	PULL 1M TO RTCVDD (CASE OPEN)
* U8	GPI011/ <u>-MCCS/GPOD</u>	VCC3	PULL 10K TO VCC3 (CPU_FAN CONTROL ON/OFF)
T5	GPO12/ <u>(H)/XDIR/-PCSO</u>	VCC3	GREEN LED ON/OFF CONTROL
U5	GPO13/ <u>-MCCS/-XOE(L)</u>	VCC3	F245 (ISA ADDR/DATA BUS CONTROL)
E12	GPO14/ <u>IRTX(L)</u>	VCC3	TO IR CONN (IRTX)
D12	GPO15/ <u>IRRX(L)</u>	VCC3	TO IR CONN (IRRX)
L2	GPO16/ <u>-DACK0</u>	VCC3	TO ISA SLOT
E1	GPO17/ <u>-DACK1</u>	VCC3	TO ISA SLOT
D2	GPO18/ <u>-DACK3</u>	VCC3	TO ISA SLOT
L4	GPO19/ <u>-DACK5</u>	VCC3	TO ISA SLOT
M3	GPO20/ <u>-DACK6</u>	VCC3	TO ISA SLOT
N2	GPO21/ <u>-DACK7</u>	VCC3	TO ISA SLOT
Y15	GPO22/ <u>JACY</u>	VCC3	TO GAME PORT OF JOYSTICK
V15	GPO23/ <u>JACX</u>	VCC3	TO GAME PORT OF JOYSTICK
H3	GPO24/ <u>DRQ2/SERIRQ/-OC0(H)</u>	VCC3	TO AMR SLOT, USB FUSEVCC

PS: '*' MEAN OPEN DRAIN SIGNAL, NEED EXTERNAL PULL UP.

GIGABYTE TECHNOLOGIES, INC.

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