

# GIGABYTE 8VM800M Schematics





Revision 1.01

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	P4_478A
05	P4_478B
06	P4_478C
07	P4M800_1_CPU
08	P4M800_2_DDR
09	P4M800_3_AGP_VLINK
10	P4M800_4_VGA
11	DDR1 & DDR2
12	VTT_DDR TERMINATOR
13	VT8237R+_ PCI, USB
14	VT8237R+_ IDE SATA GPIO
15	VT8237R+_ VLINK LPC MII
16	AGP SLOT
17	PCI1 & PCI2 SLOT
18	PCI3 SLOT
19	LPC I/O (IT8705)
20	IDE CONNECTOR
21	PS/2 KB & MS F_USB
22	BIOS, FDD, COM, LPT
23	FAN & H/W MONITOR

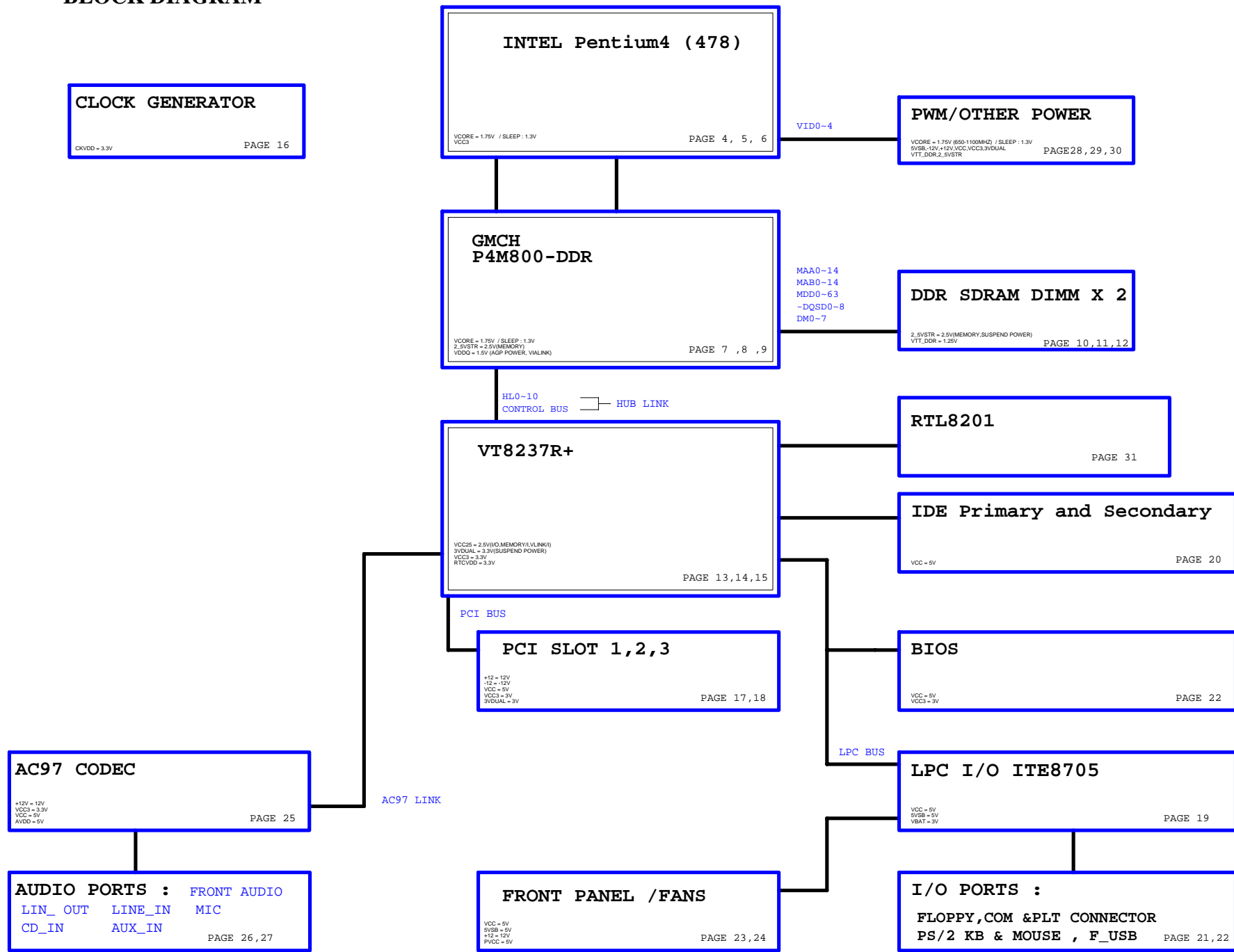
SHEET TITLE

24	FRONT PANEL
25	ALC653 CODEC
26	AUDIO JACK
27	CLOCK GEN. RTM862-520
28	ATX & StandBy Power
29	VCORE PWM (FAN5018B)
30	Discrete Power
31	RTL8201CL & USB_LAN
32	GPIO LIST

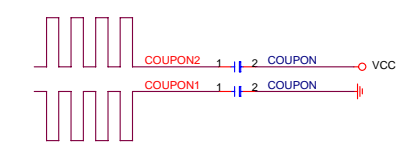
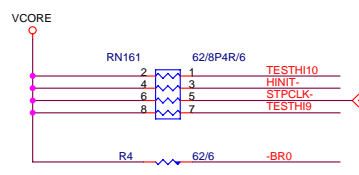
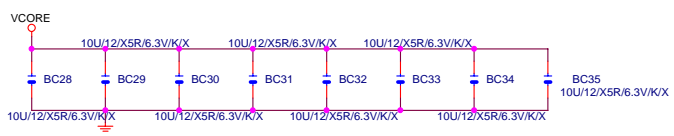
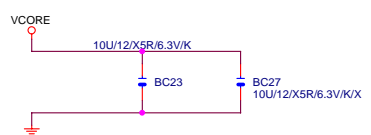
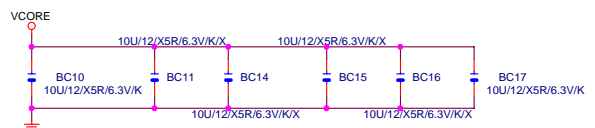
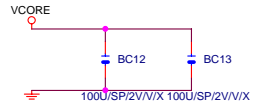
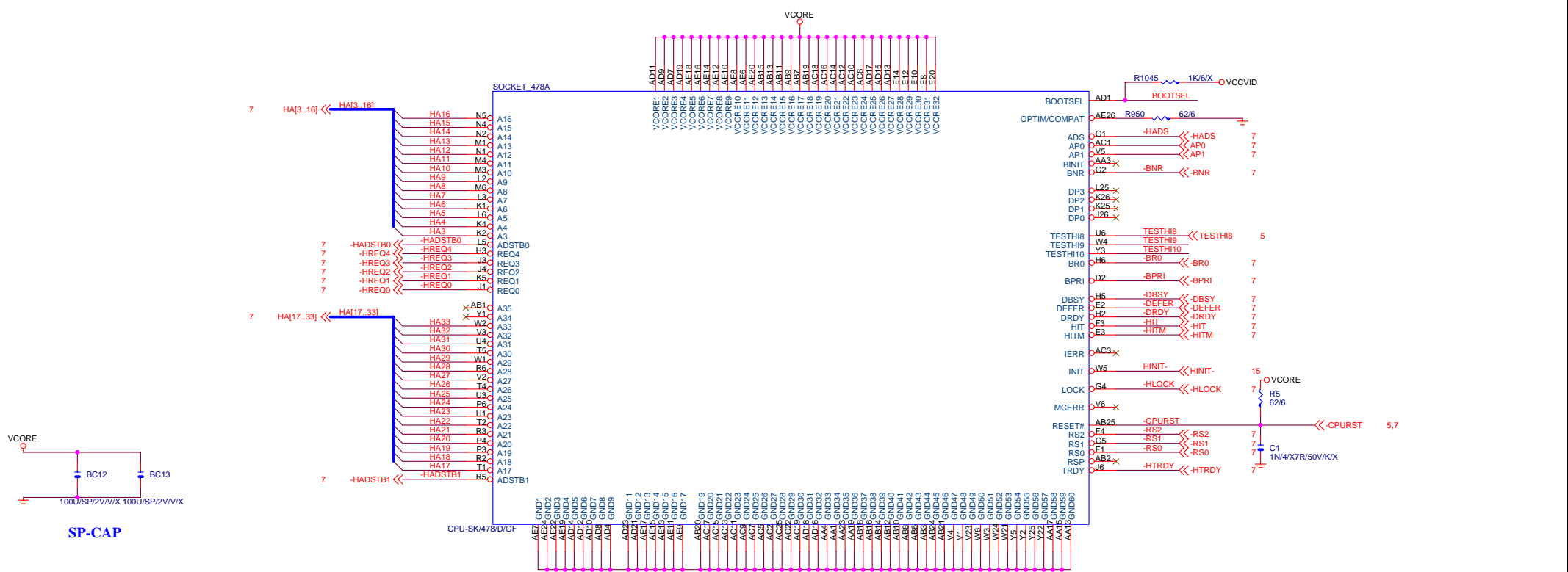
 COMPONENT SIDE (1 oz. Copper)		
 VCC SIDE (1 oz. Copper)		
 GND SIDE (1 oz. Copper)		
 SOLDER SIDE (1 oz. Copper)		
<b>GIGABYTE</b>		
Title <b>COVER SHEET</b>		
Size Custom	Document Number <b>8VM800M</b>	Rev <b>1.01</b>
Date: Thursday, November 03, 2005	Sheet 1	of 32



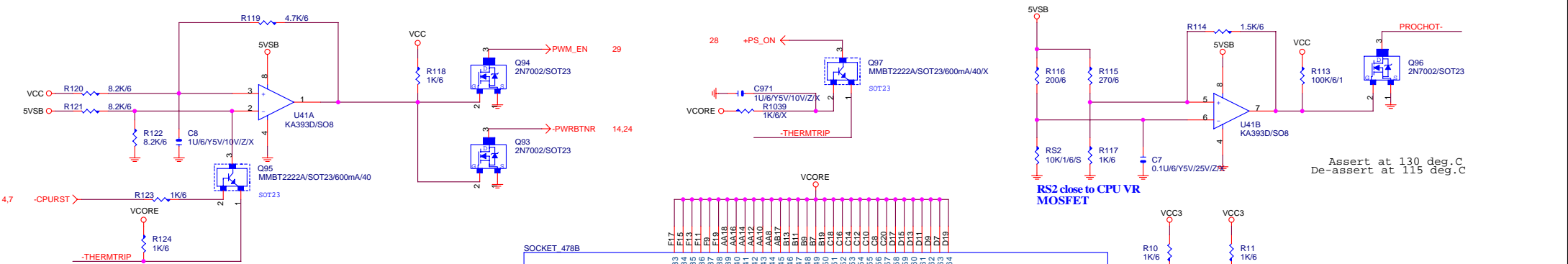
# BLOCK DIAGRAM



<b>GIGABYTE</b>			
<b>BOM &amp; PCB MODIFY HISTORY</b>			
File			
Size	Document Number	Rev	
Custom	<b>8VM800M</b>	<b>1.01</b>	
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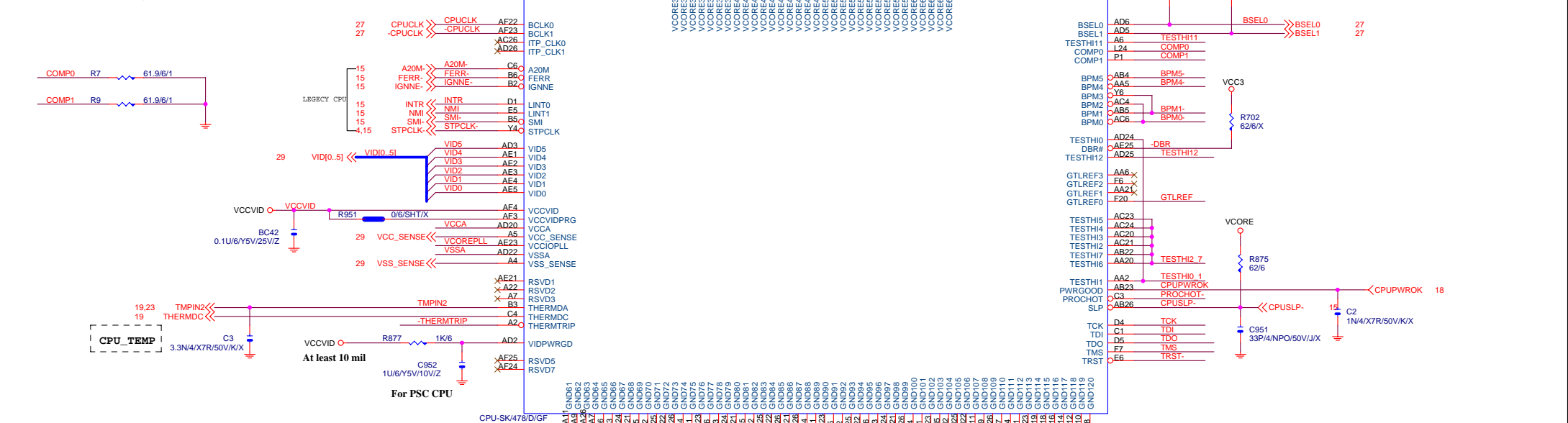


<b>GIGABYTE</b>		
<b>P4 478A</b>		
Title	Document Number	Rev
	<b>8VM800M</b>	<b>1.01</b>
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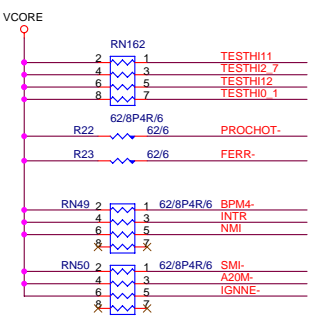
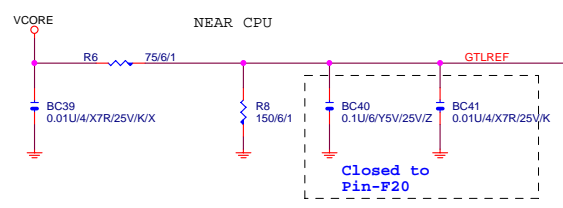
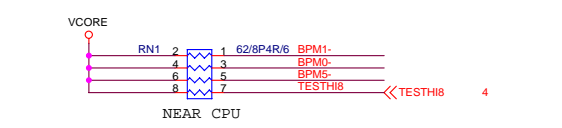
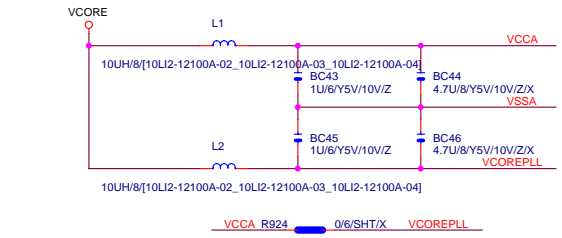


RS2 close to CPU VR MOSFET

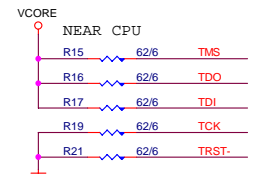
Assert at 130 deg.C  
De-assert at 115 deg.C



At least 10 mil  
For PSC CPU

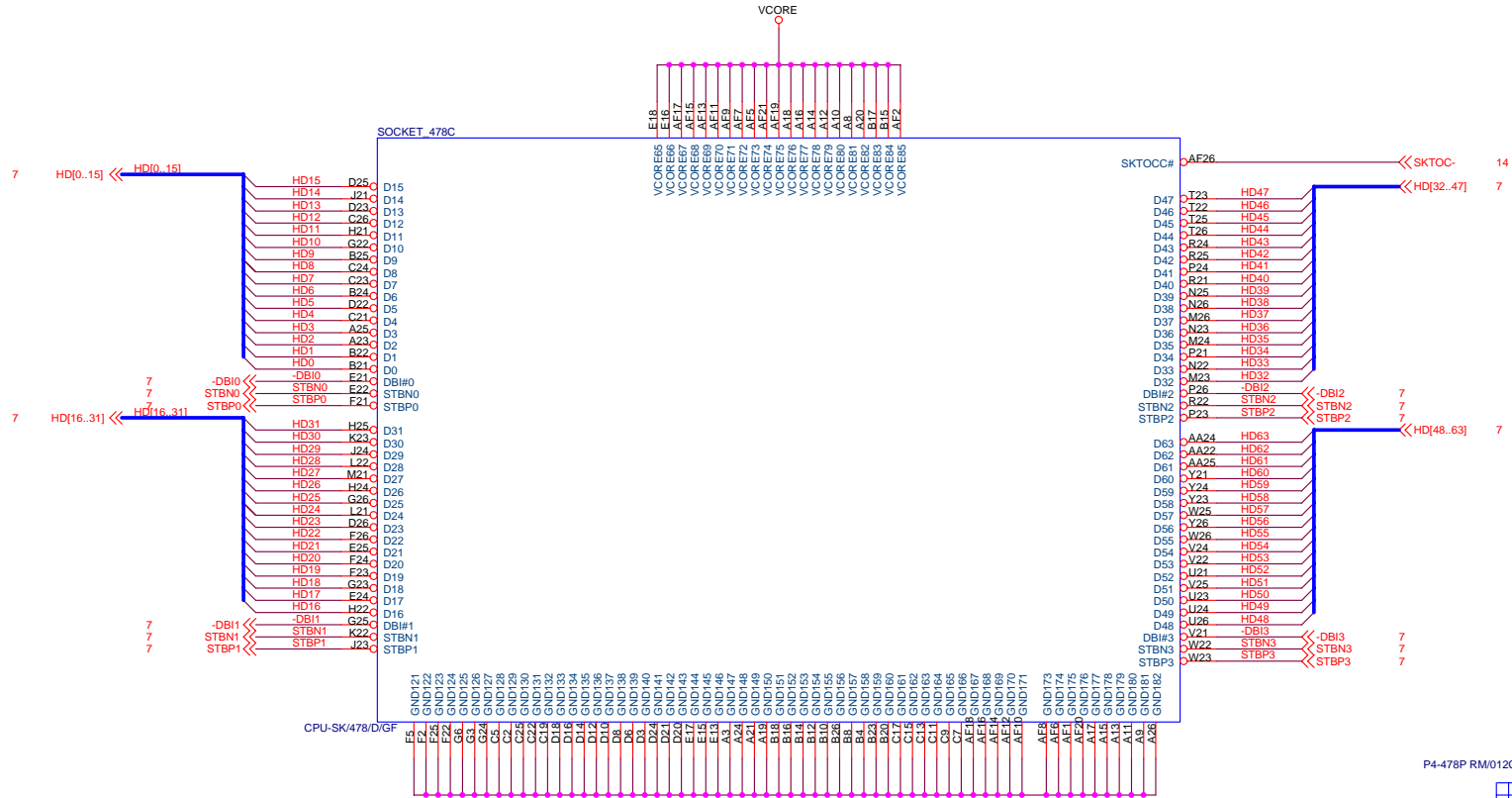


BSEL1	BSEL0	FSB
0	0	400MHz
0	1	533MHz
1	0	800MHz

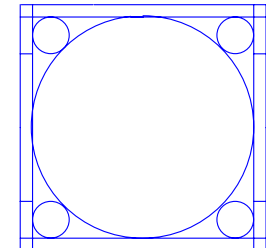


**GIGABYTE**

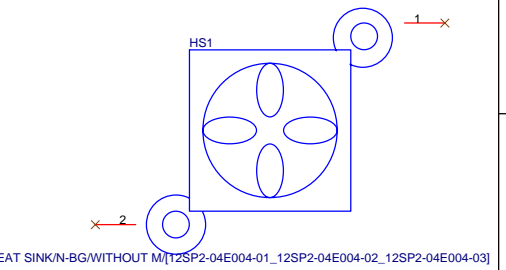
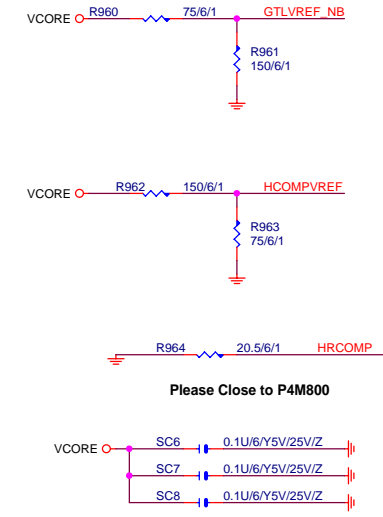
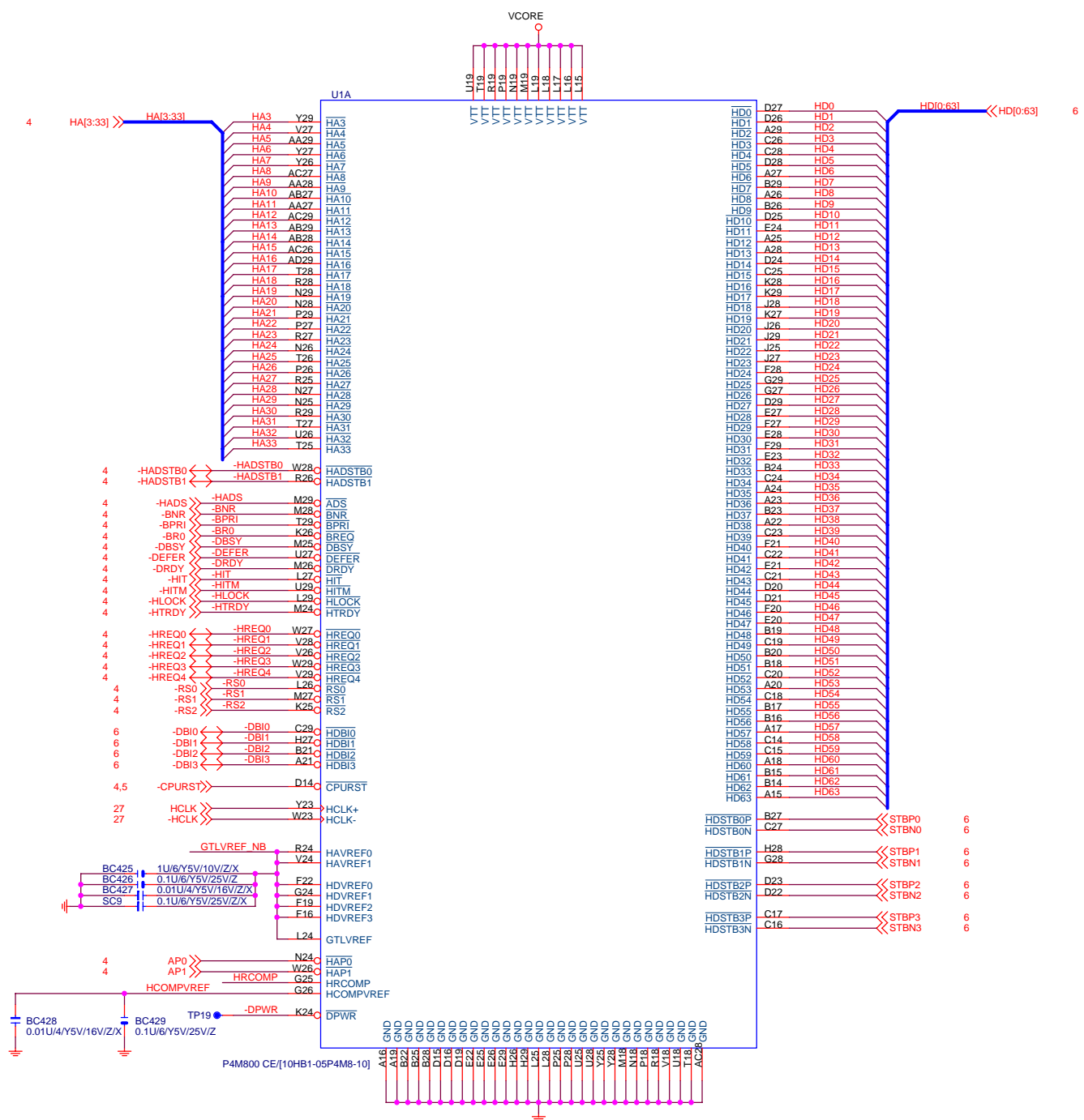
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Size	Document Number	Rev	
Custom	<b>8VM800M</b>	<b>1.01</b>	
Date:	Thursday, November 03, 2005	Sheet	5 of 32



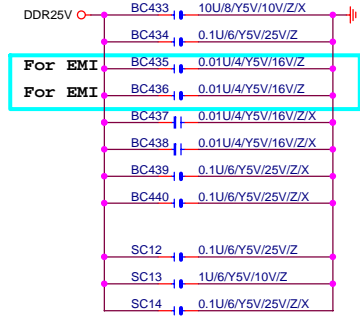
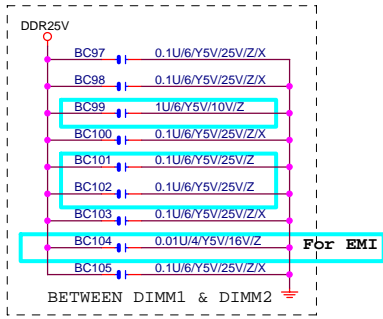
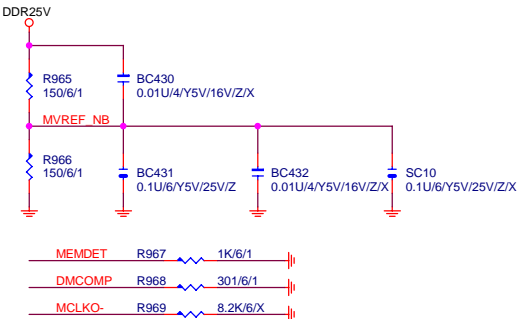
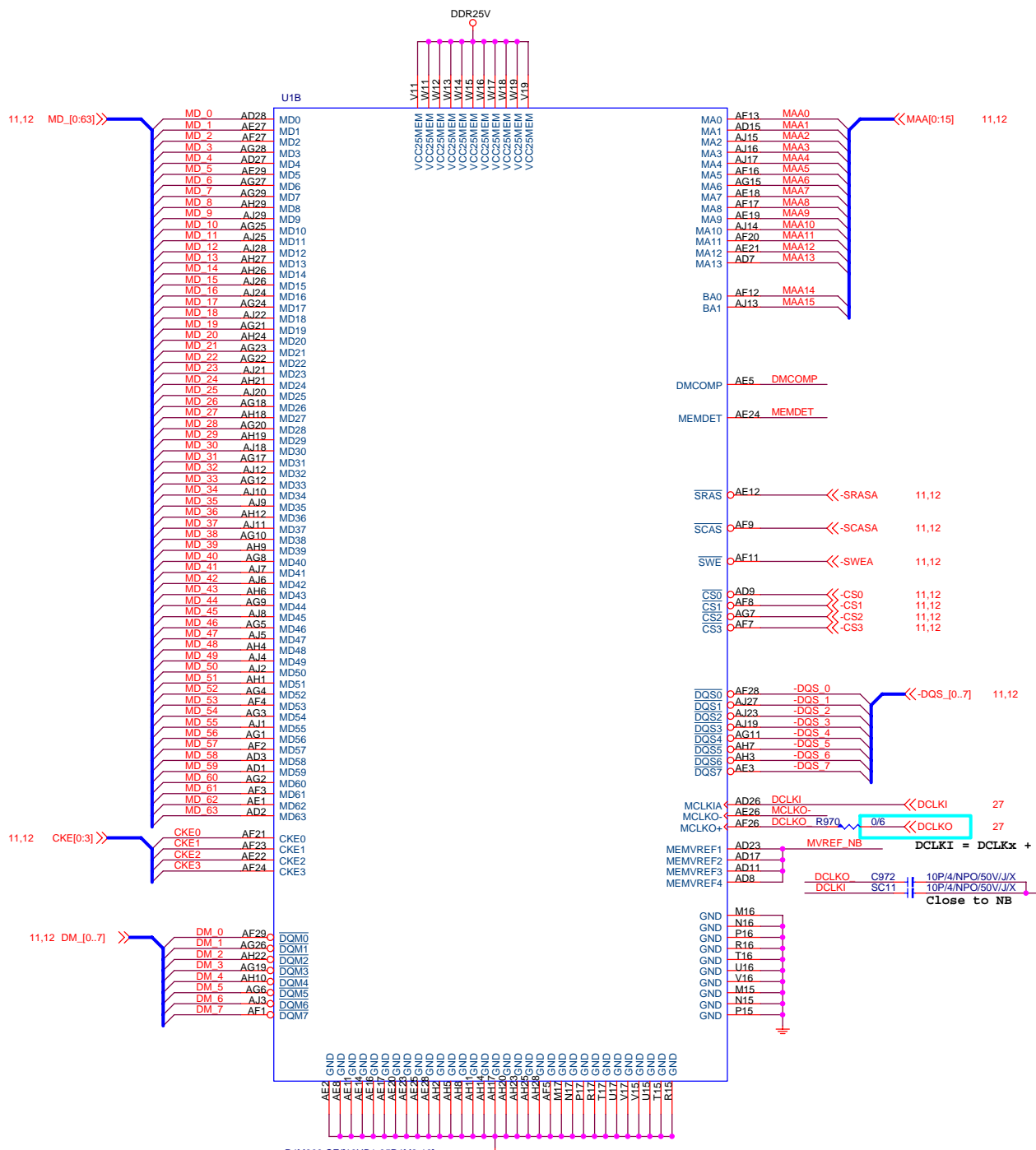
CR  
P4-478P RM/012C(YELLOW)[12KRC-040003-31\_12KRC-040003-32\_12KRC-040003-33]



<b>GIGABYTE</b>		
Title <b>P4 478C</b>		
Size Custom	Document Number <b>8VM800M</b>	Rev <b>1.01</b>
Date:	Thursday, November 03, 2005	Sheet 6 of 32



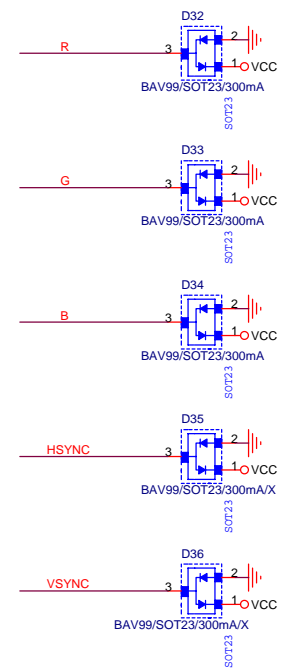
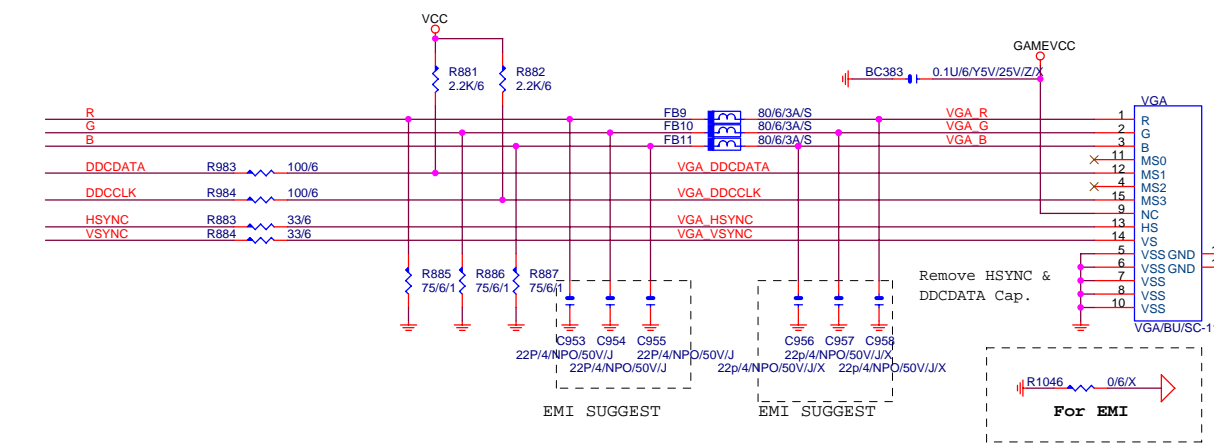
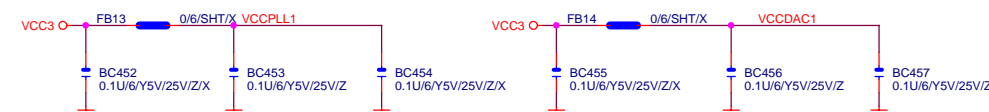
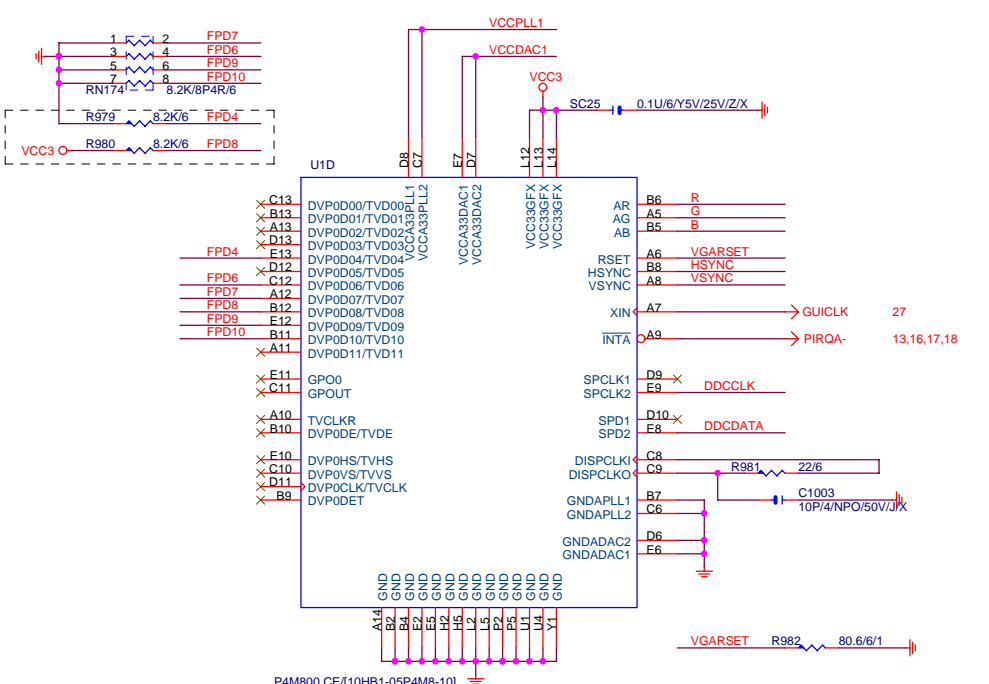
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Title <b>P4M800 1 CPU</b>		
Size C	Document Number <b>8VM800M</b>	Rev <b>1.01</b>
Date:	Thursday, November 03, 2005	Sheet 7 of 32



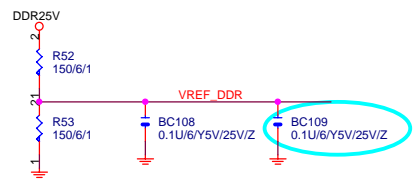
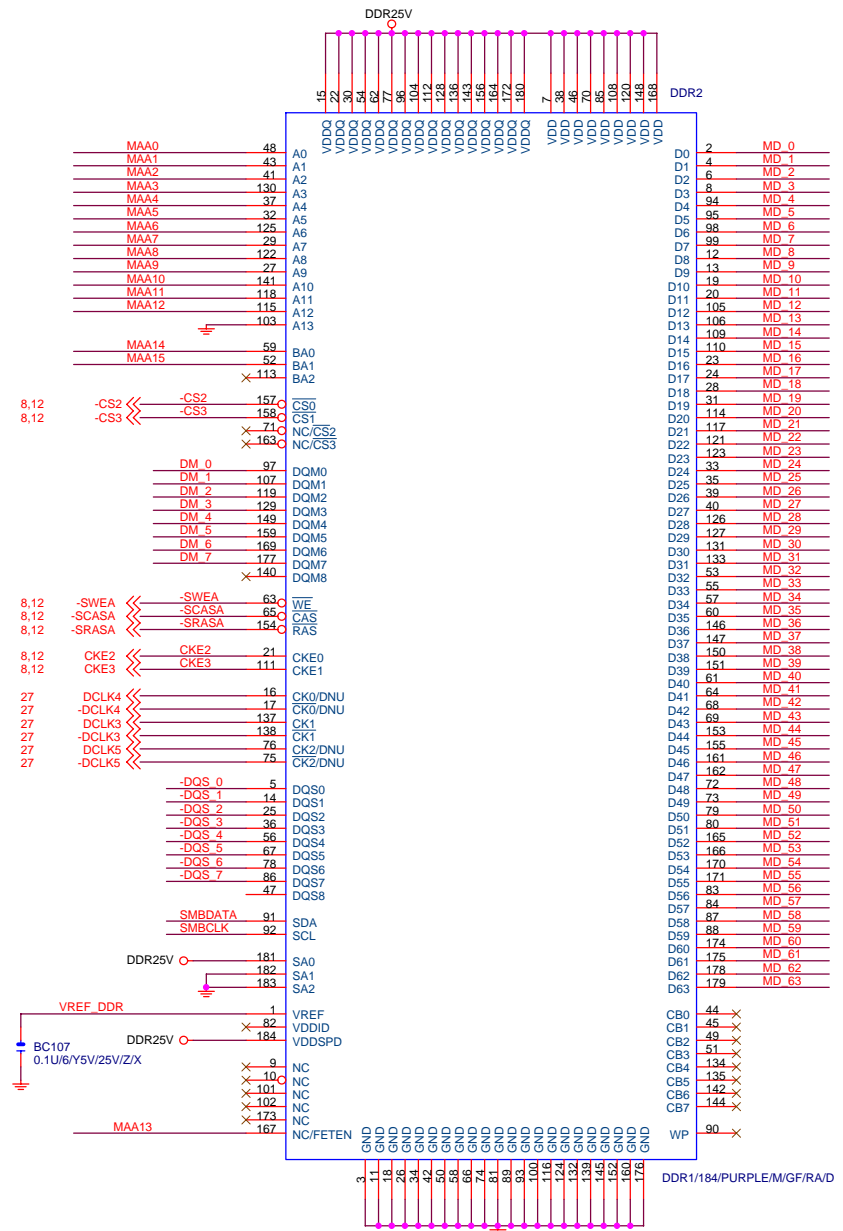
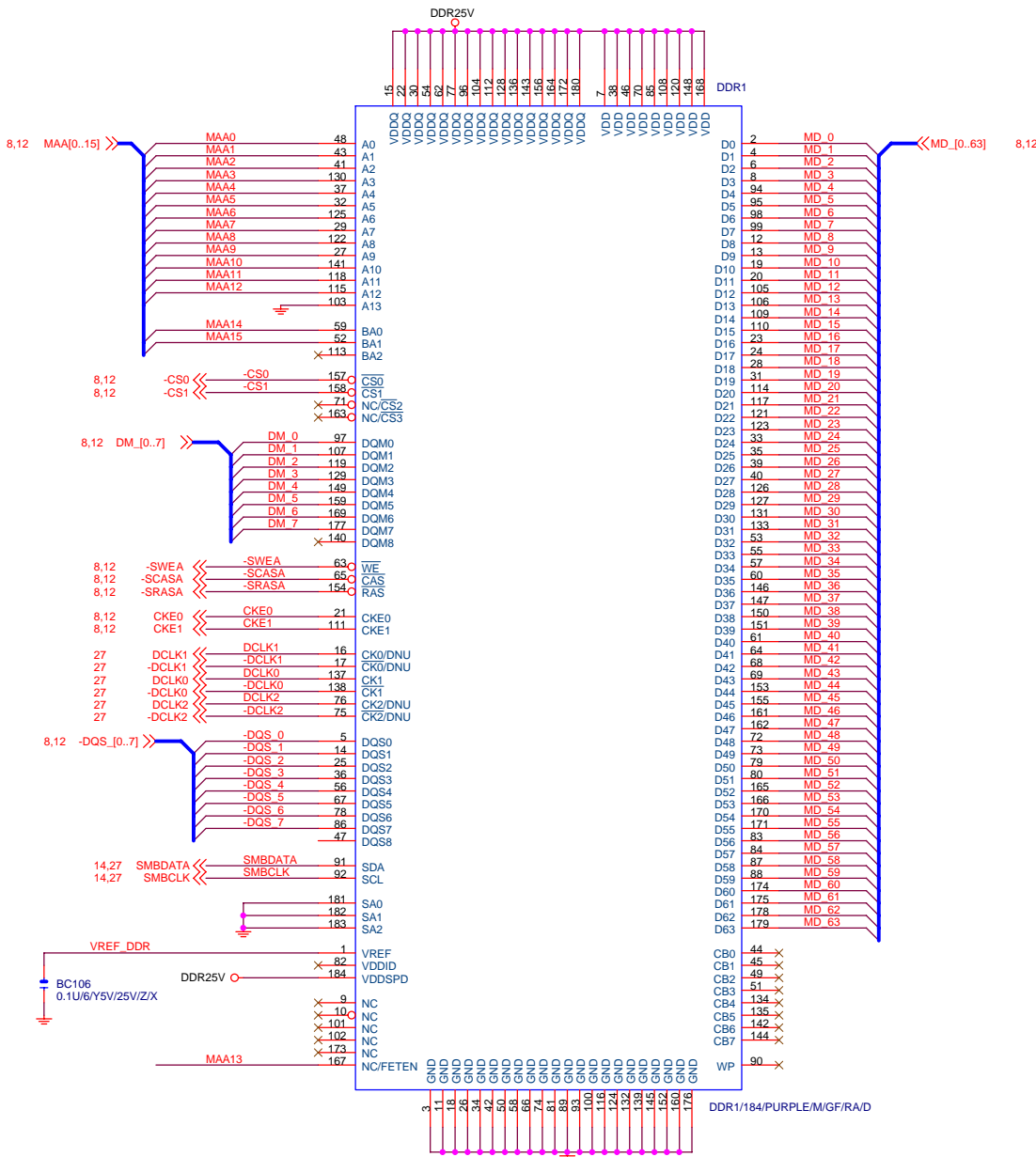
P4M800 CE(10HB1-05P4M8-10)

<b>GIGABYTE</b>		
Title <b>P4M800 2 DDR</b>		
Size C	Document Number <b>8VM800M</b>	Rev <b>1.01</b>
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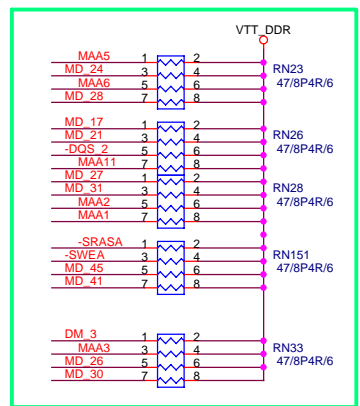
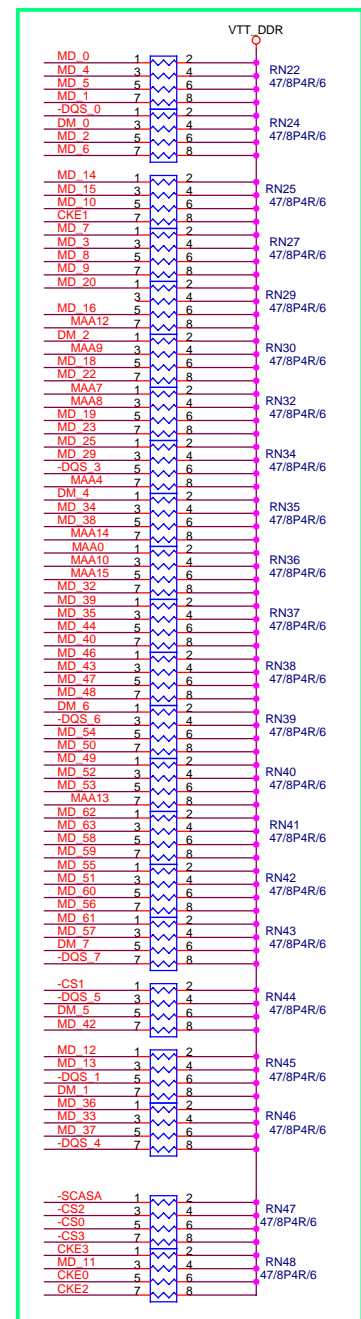
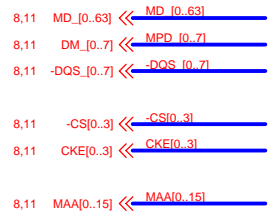
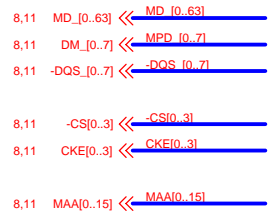
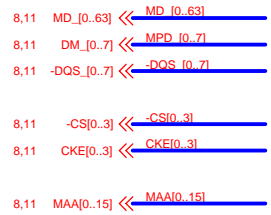
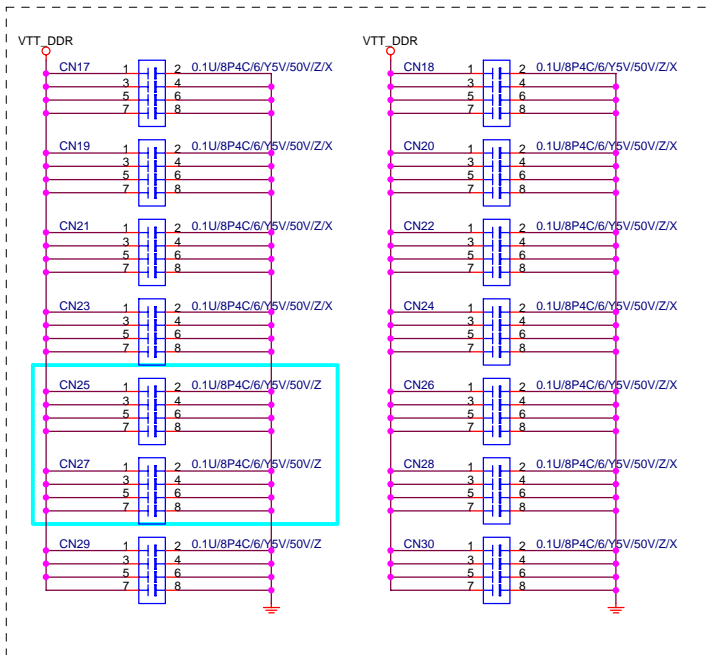




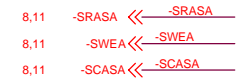
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Title <b>P4M800_4_VGA</b>		
Size C	Document Number <b>8VM800M</b>	Rev <b>1.01</b>
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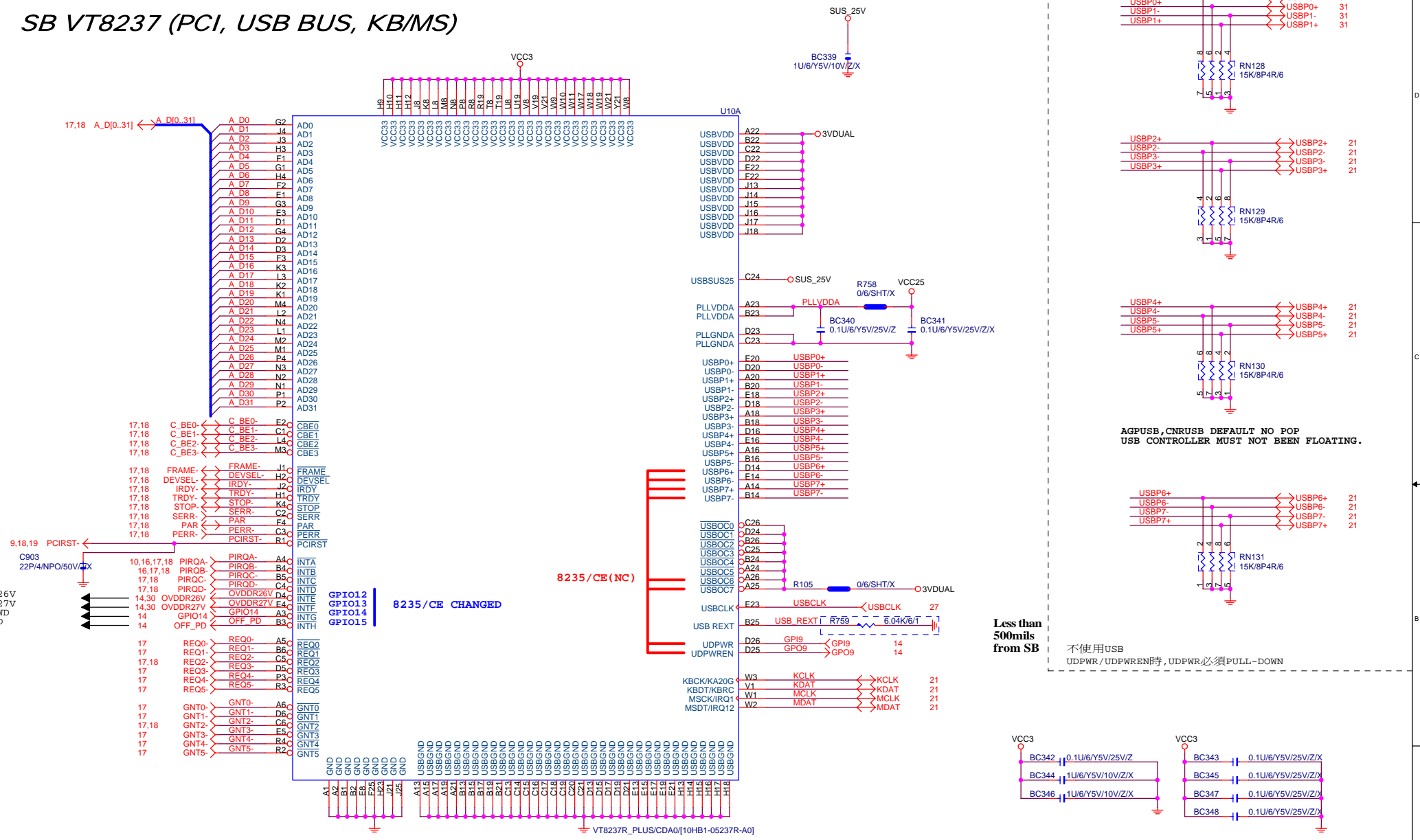
<b>GIGABYTE</b>		
Title <b>DDR1,2</b>		
Size B	Document Number <b>8VM800M</b>	Rev <b>1.01</b>
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VIA recommend 33 ohm



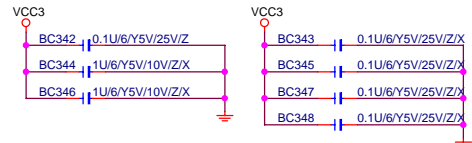
# SB VT8237 (PCI, USB BUS, KB/MS)



AGPUSB, CNRUSB DEFAULT NO POP  
USB CONTROLLER MUST NOT BEEN FLOATING.

Less than 500mils from SB

不使用USB  
UDPWR / UDPWREN時, UDPWR必須PULL-DOWN



<b>GIGABYTE</b>		
Title <b>8237R+(PCI, USB BUS, KB/MS)</b>		
Size B	Document Number <b>8VM800M</b>	Rev <b>1.01</b>
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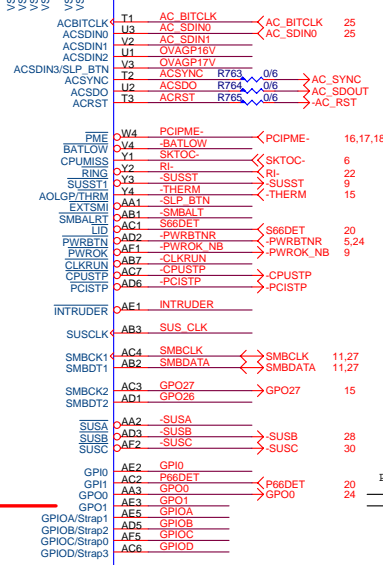
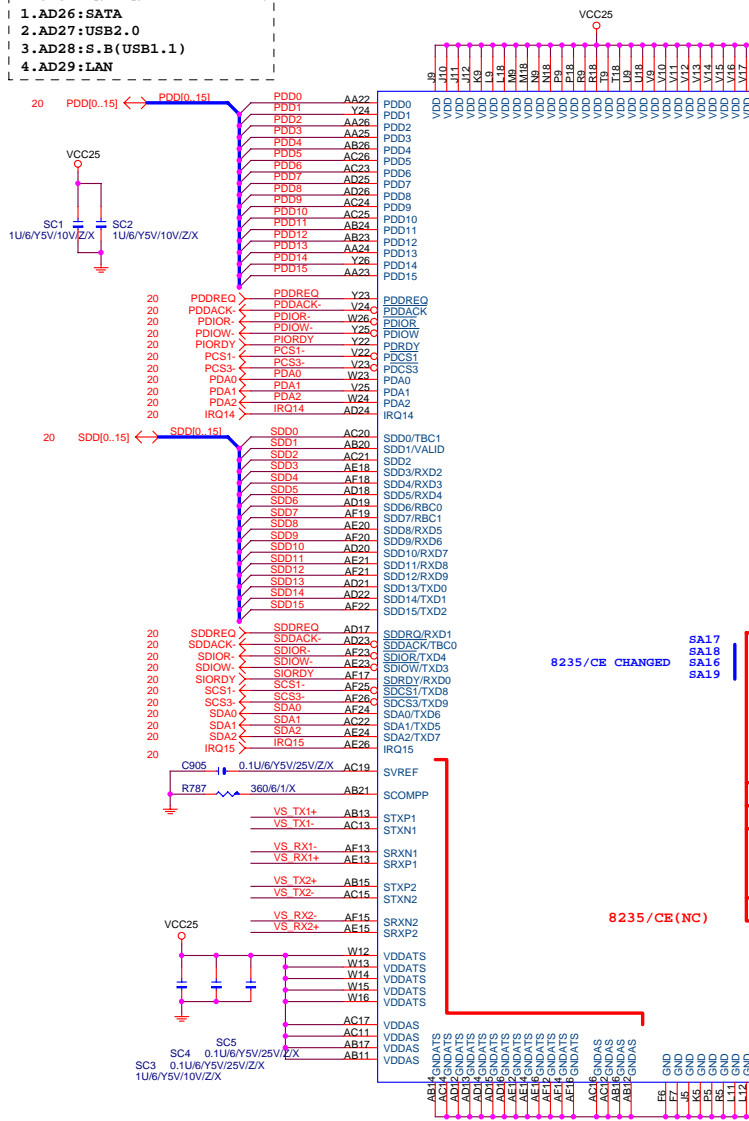
BIOS WRITE PROTECT

# SB VT8237 (SATA, IDE, AC97, POWER MANAGEMENT, PGIO)

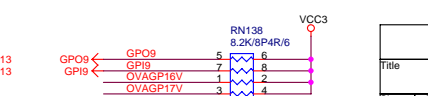
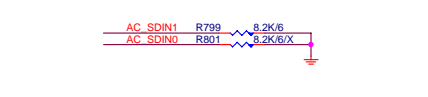
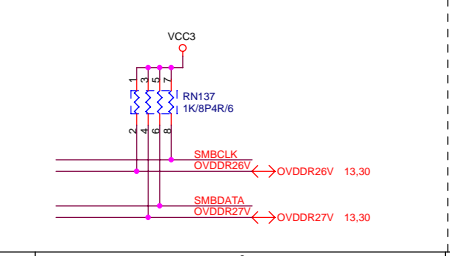
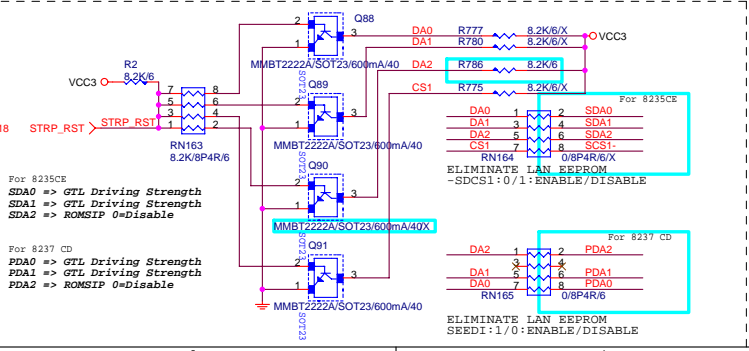
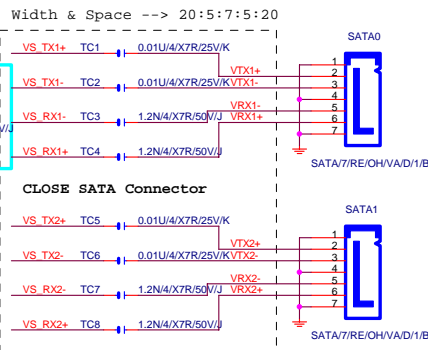
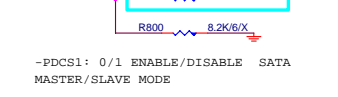
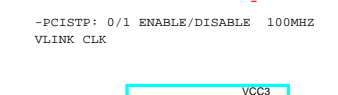
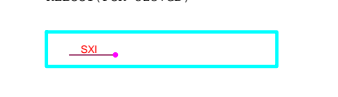
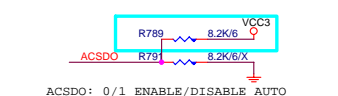
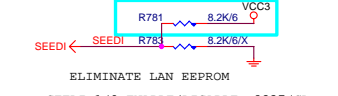
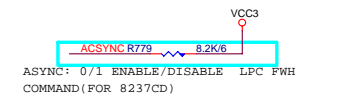
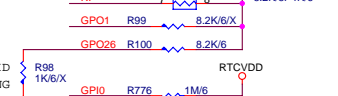
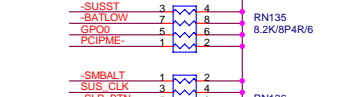
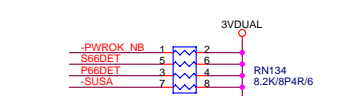
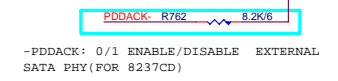
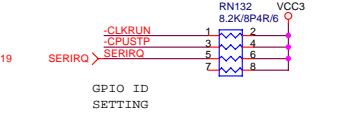
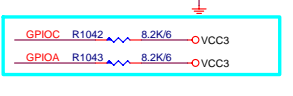
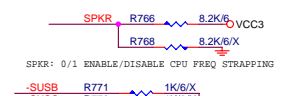
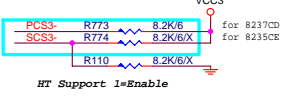
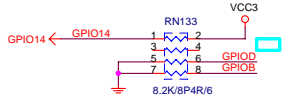
- VT8237 INTERNAL IDSEL LIST:**
- 1.AD26:SATA
  - 2.AD27:USB2.0
  - 3.AD28:S.B(USB1.1)
  - 4.AD29:LAN

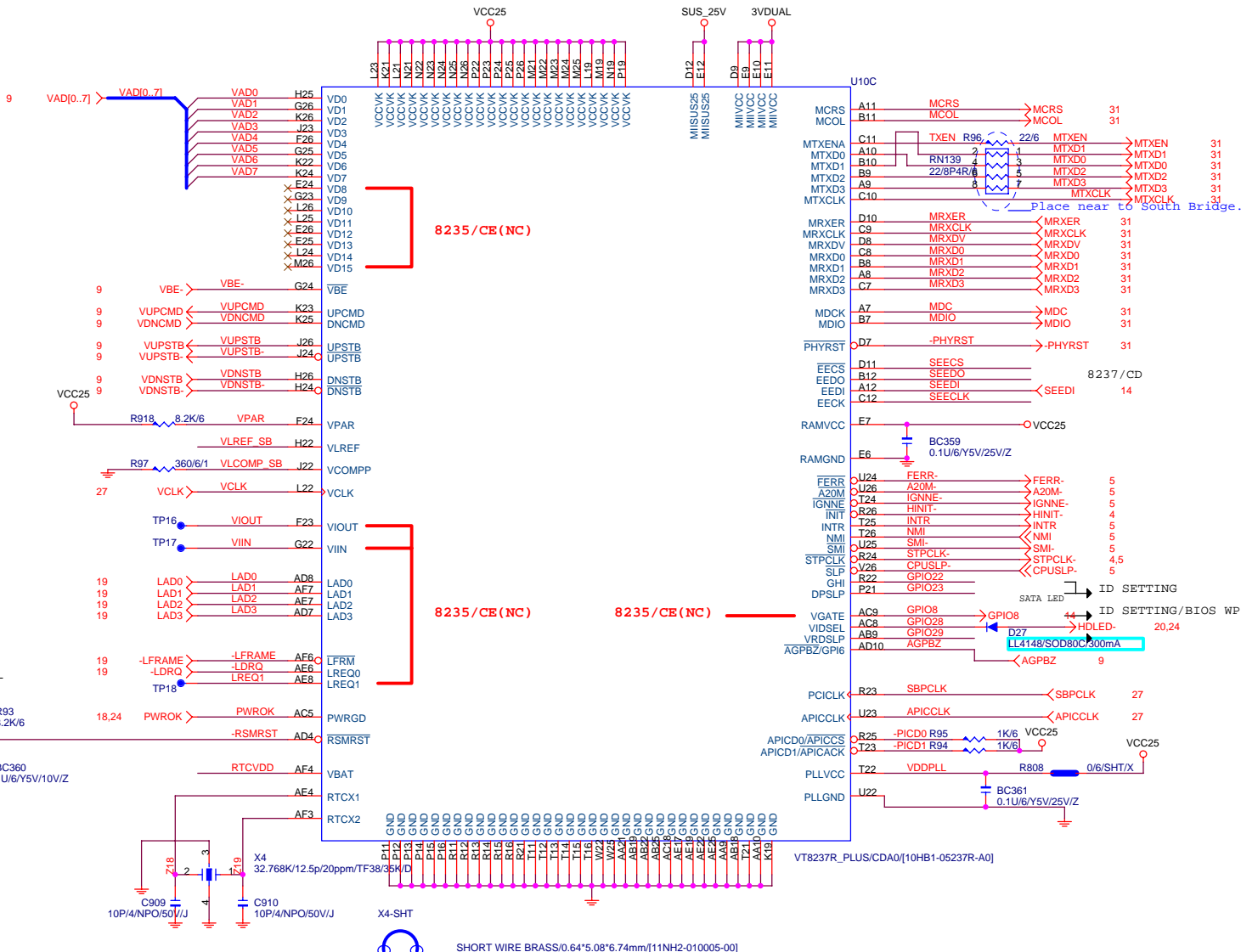
P/SDA1	P/SDA0	GTL Driving Strength
0	0	WEAK
0	1	MIDDLE WEAK
1	0	STRONG
1	1	STRONGEST

**GPIOB**  
0 ---> IOQ=12  
1 ---> IOQ=1

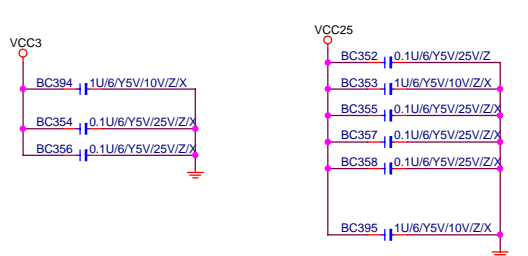


**GPIOD = GTL Pull 0** --> Enable  
**1** --> Disable





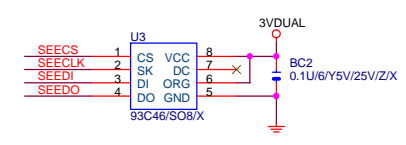
### Decoupling capacitors



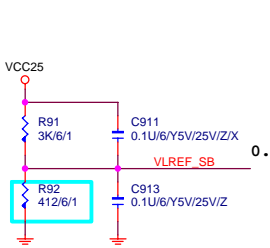
### Internal MAC P.U



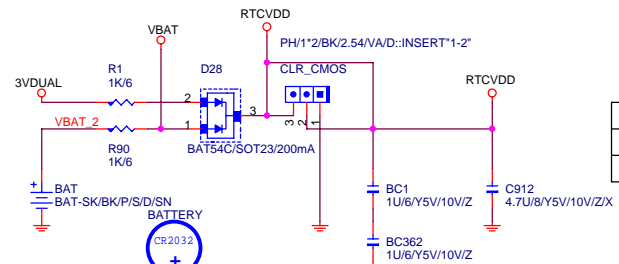
### LAN EEPROM



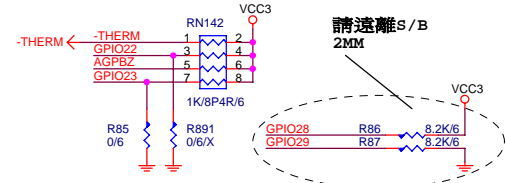
FOR 8233A-CE  
The voltage level of  
VLREF\_SB is 0.9V  
0.625V FOR  
8235-CD



0.3V



CLR_CMOS 1-2	
SHORT	CLEAR CMOS
OPEN	NORMAL (Default)



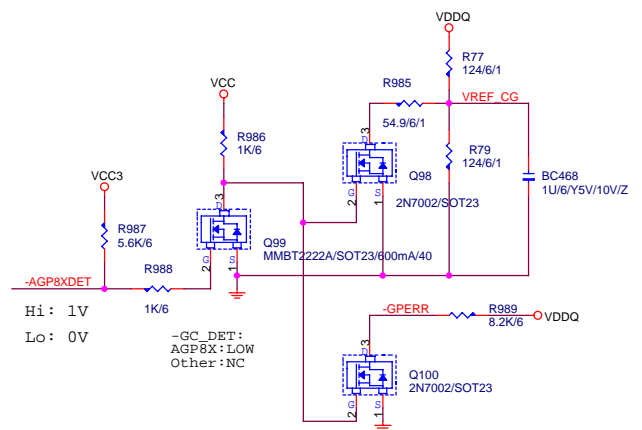
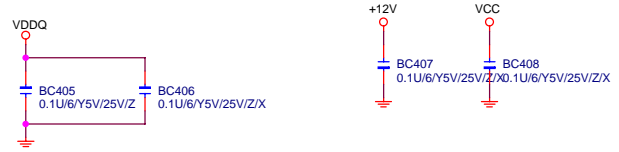
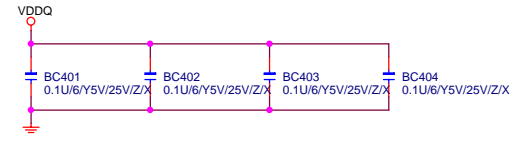
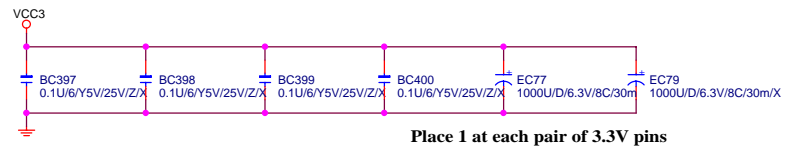
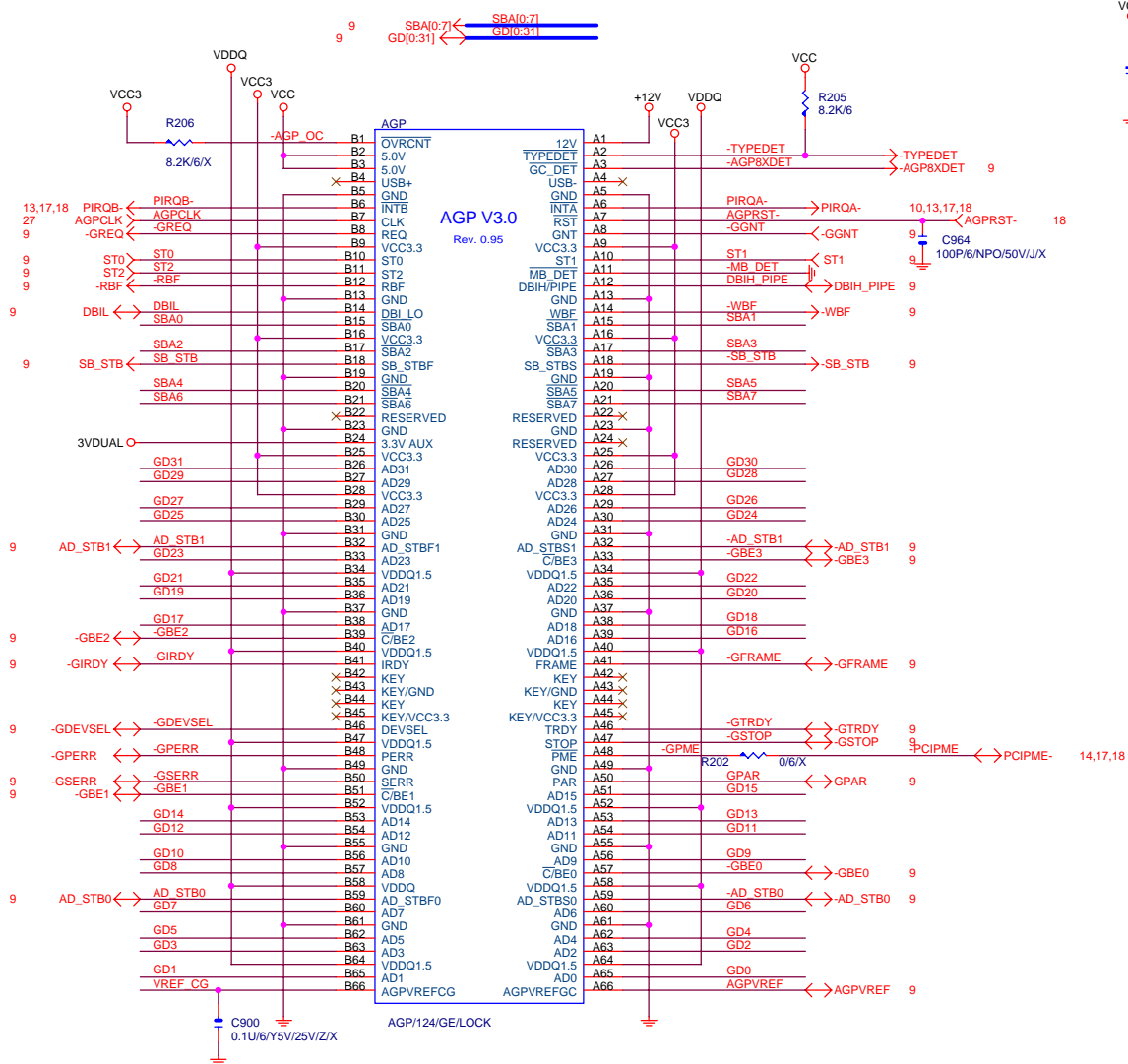
請遠離S/B  
2MM

**GIGABYTE**

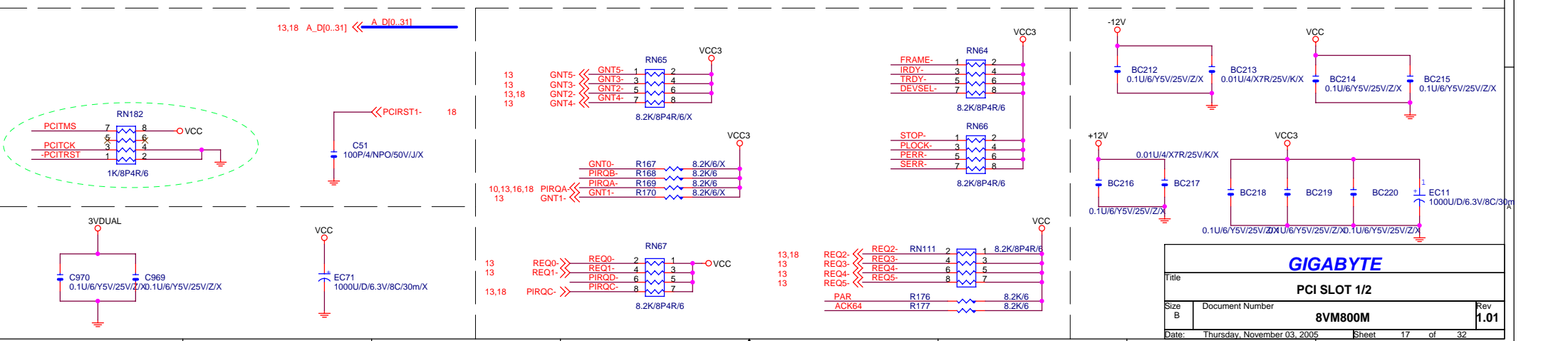
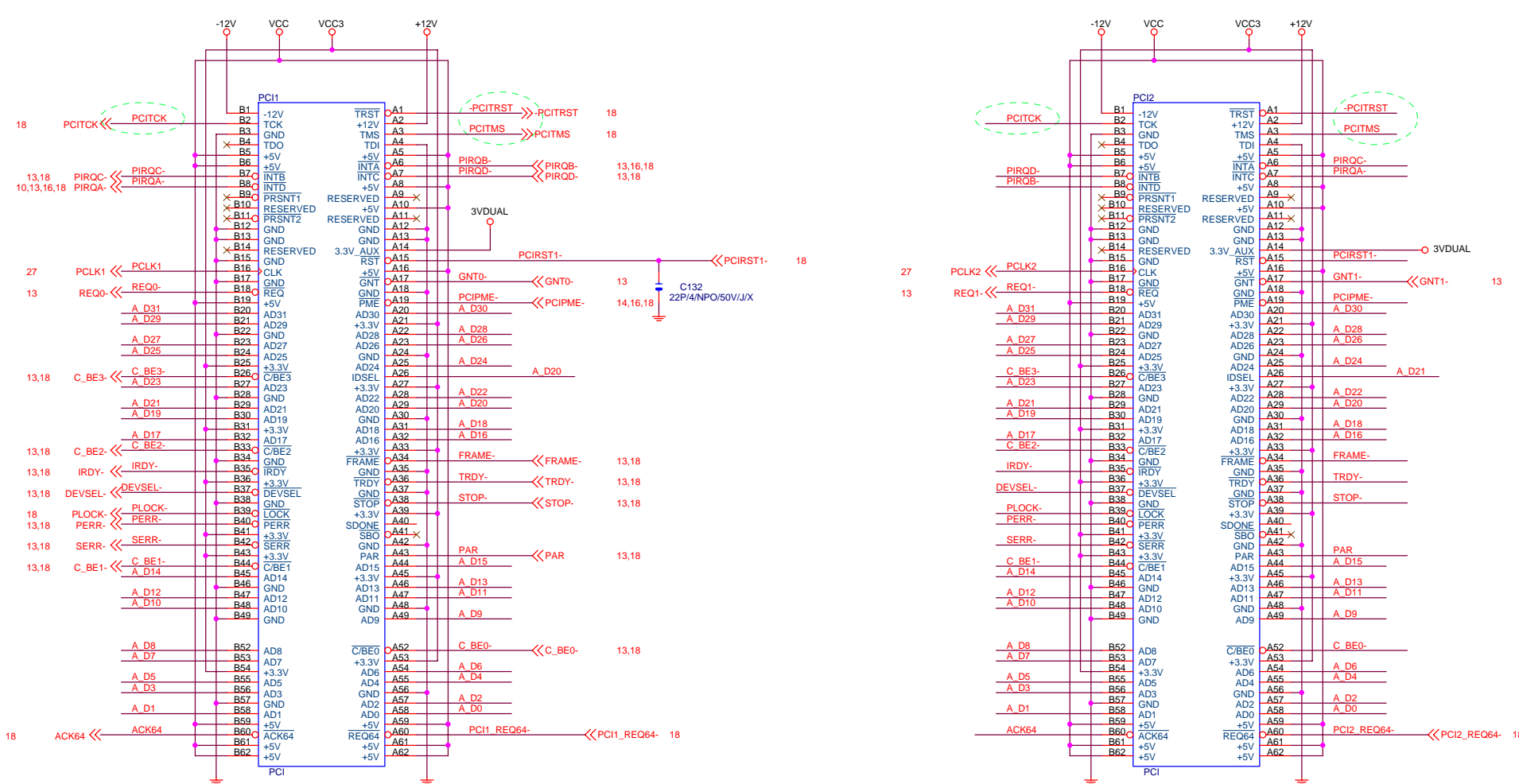
Title: **8237+(Vlink, CPU, LPC, LAN, I2C)**

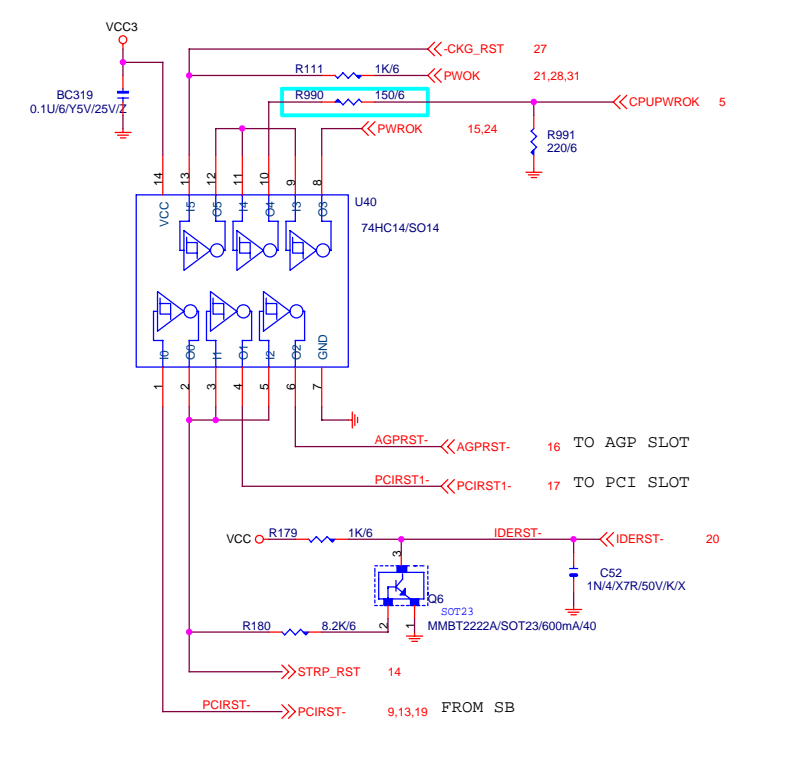
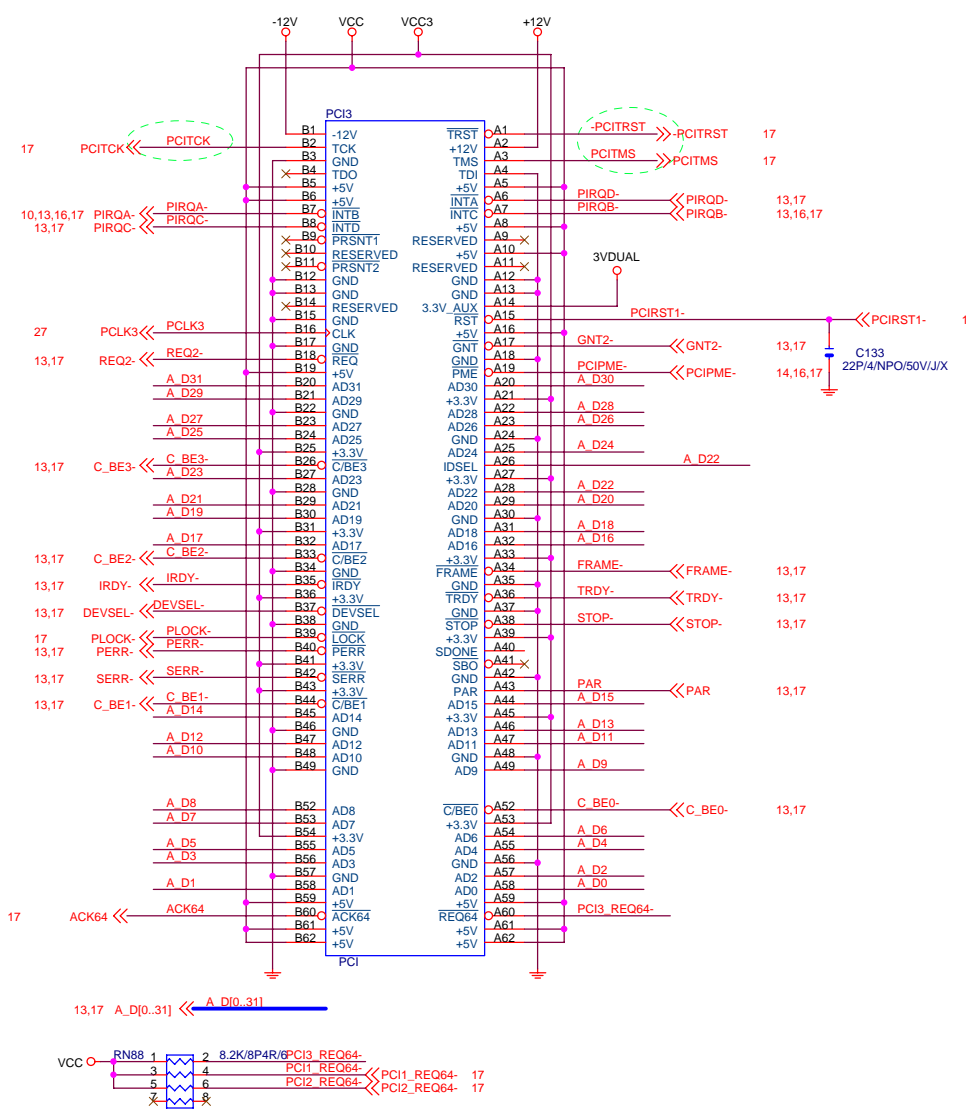
Size B Document Number: **8VM800M** Rev: **1.01**

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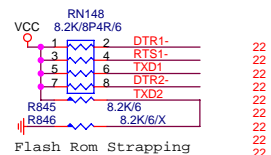


<b>GIGABYTE</b>		
<b>AGP SLOT</b>		
Title		
Size B	Document Number	Rev
	<b>8VM800M</b>	<b>1.01</b>
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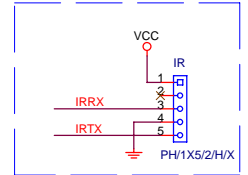
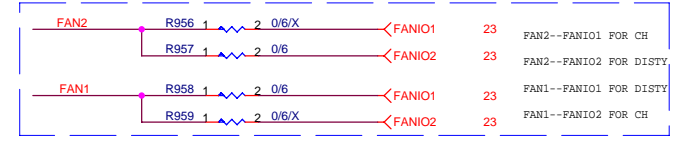
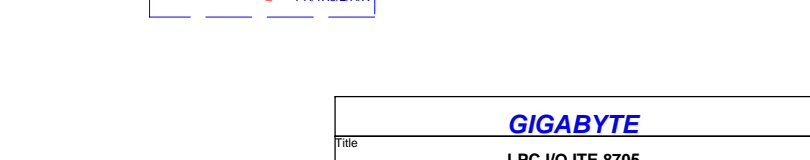
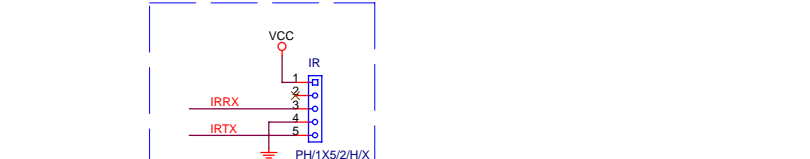
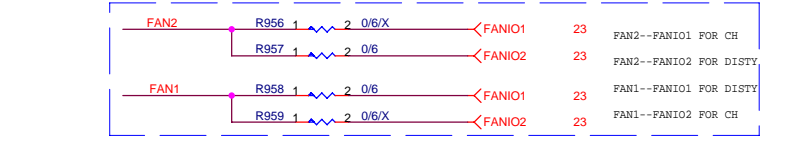
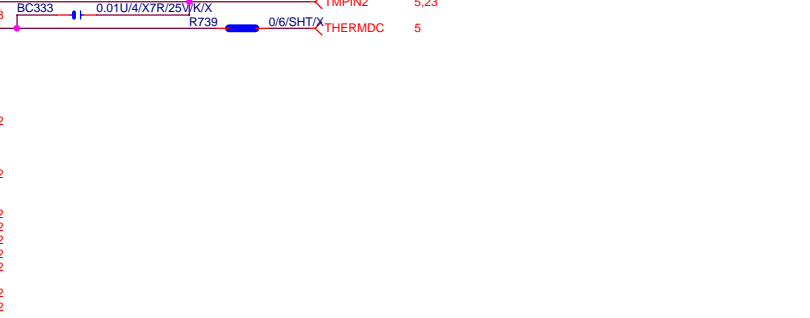
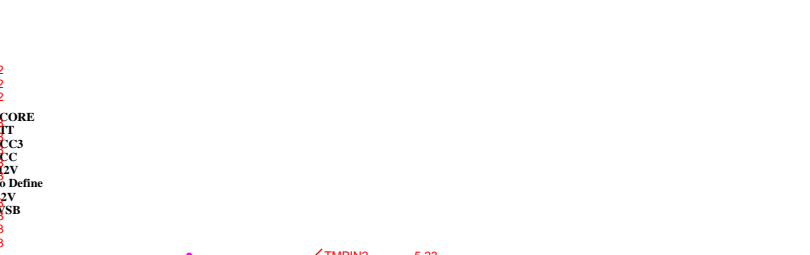
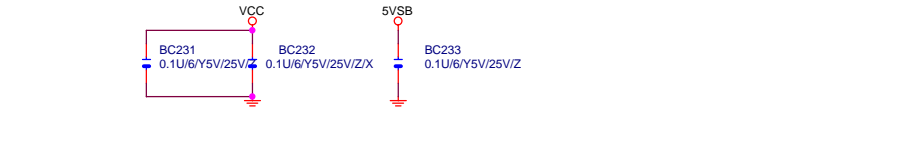
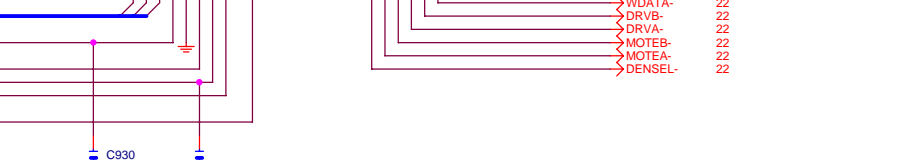
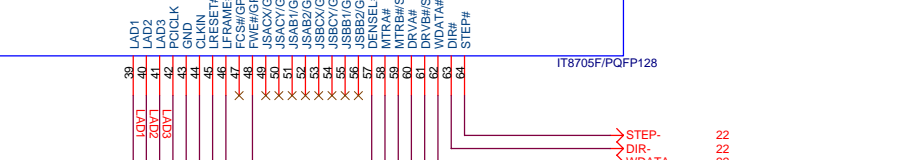
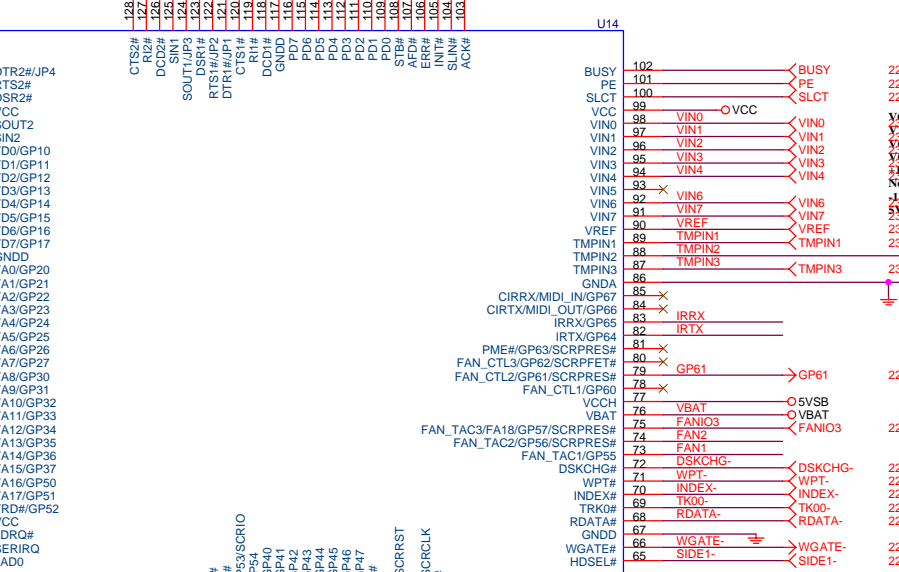
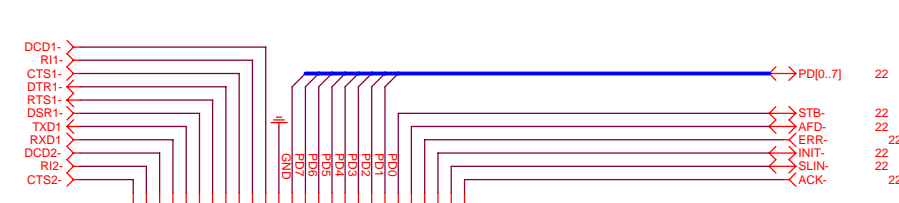
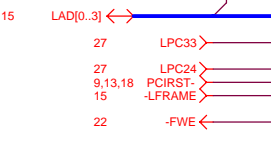
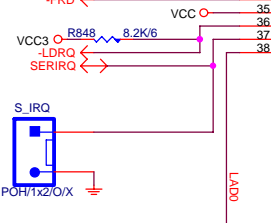
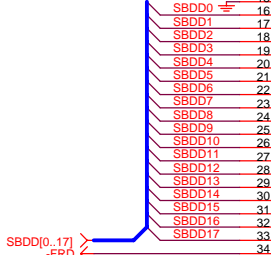
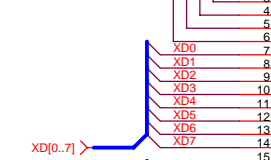
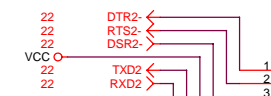


<b>GIGABYTE</b>		
<b>PCI SLOT 3</b>		
Title		
Size B	Document Number	Rev
	<b>8VM800M</b>	<b>1.01</b>
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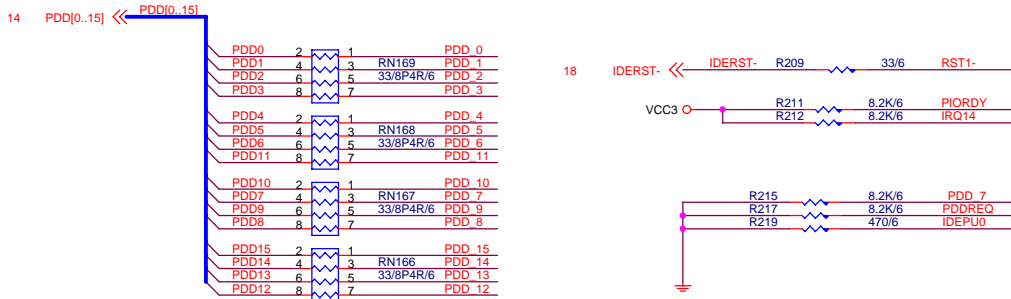
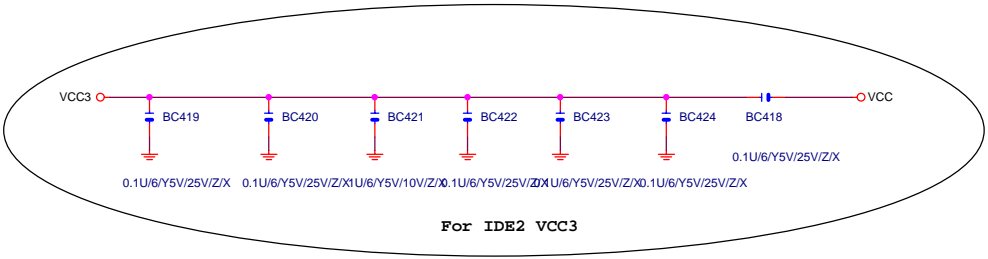
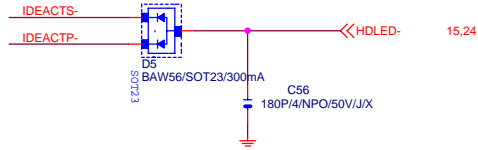


Flash Rom Strapping

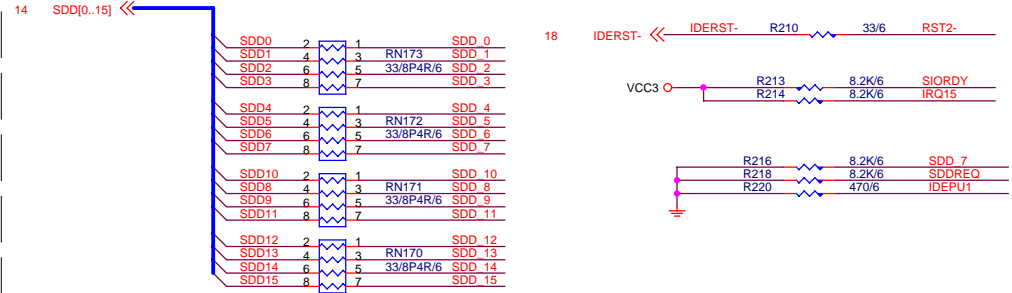
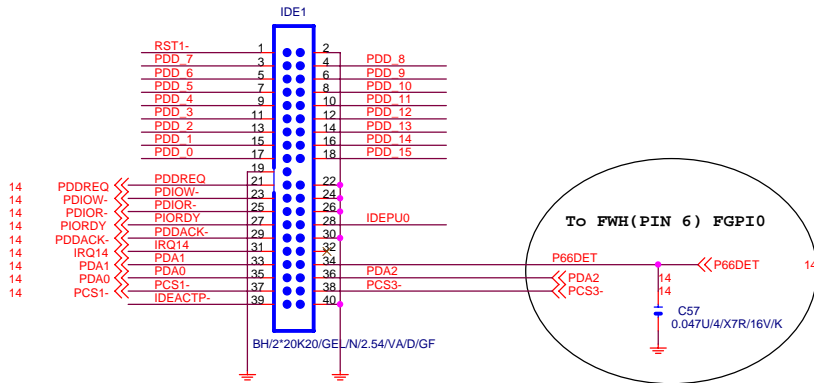
TXD2 only for 4Mb Flash  
2Mb:Low, 4Mb:Hi.



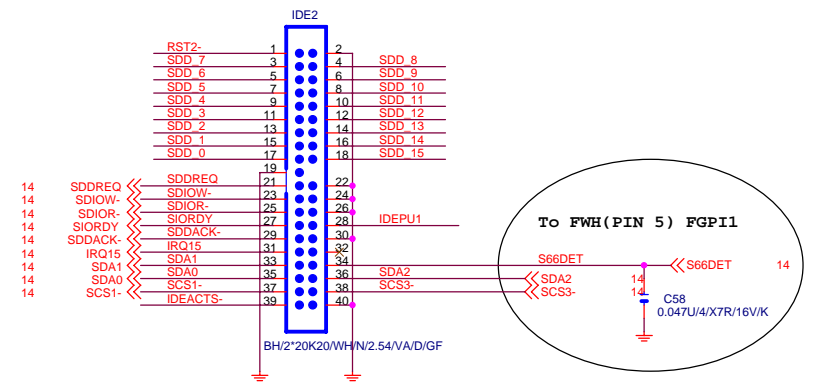
<b>GIGABYTE</b>		
<b>LPC I/O ITE 8705</b>		
Title	Document Number	
Size B	<b>8VM800M</b>	
Date: Thursday, November 03, 2005	Sheet 19	of 32
	2	1



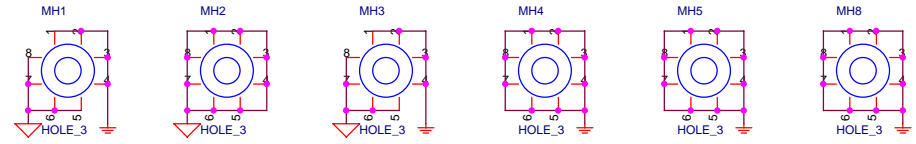
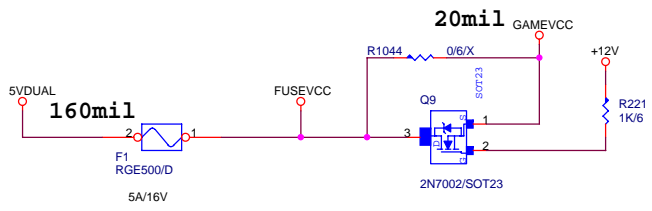
PRIMARY IDE CONNECTOR



SECONDARY IDE CONNECTOR

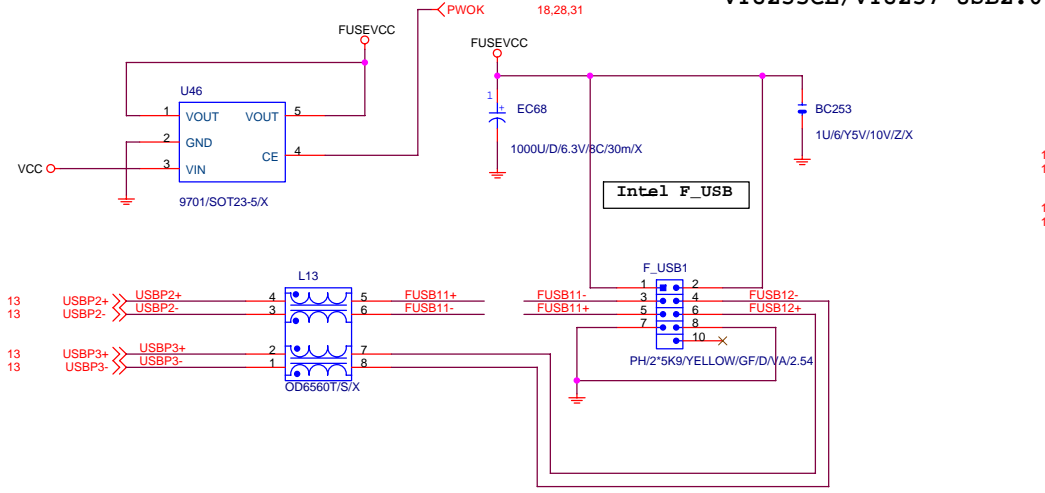


<b>GIGABYTE</b>		
<b>IDE CONNECTOR</b>		
Title	Document Number	
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	Rev	1.01



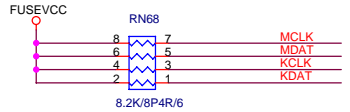
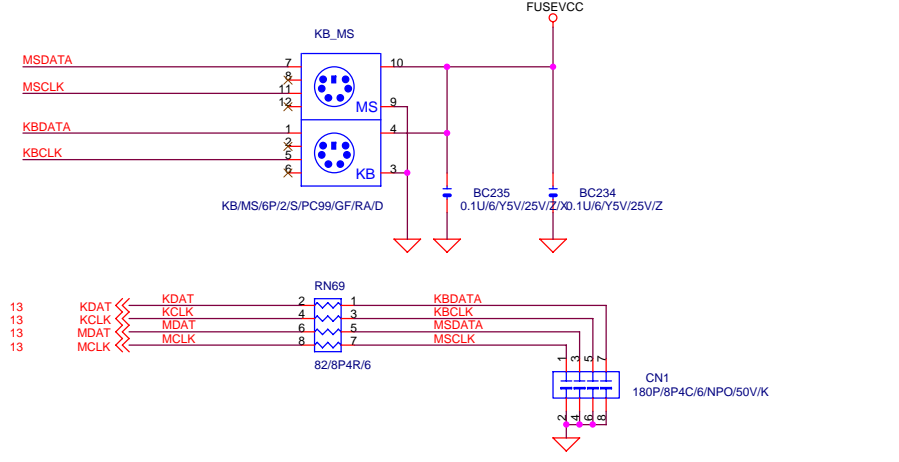
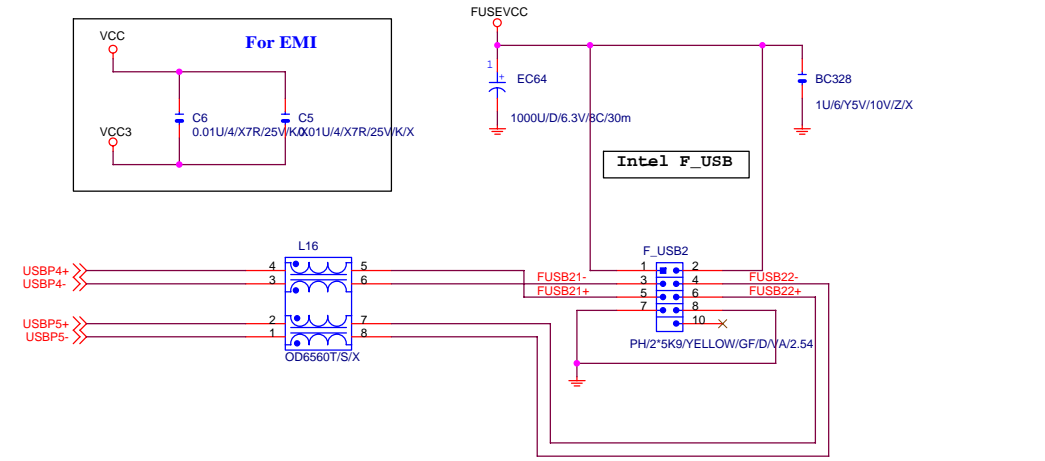
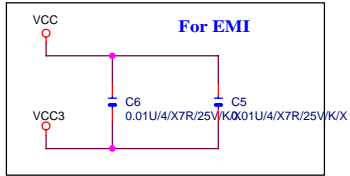
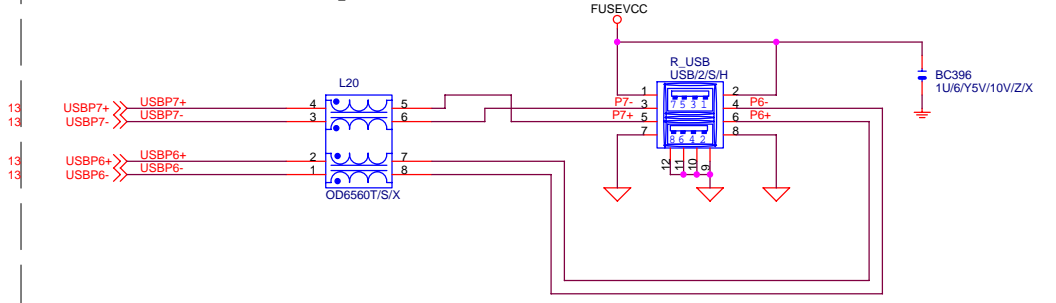
**FRONT USB CONN**

VT8235CE/VT8237 USB2.0



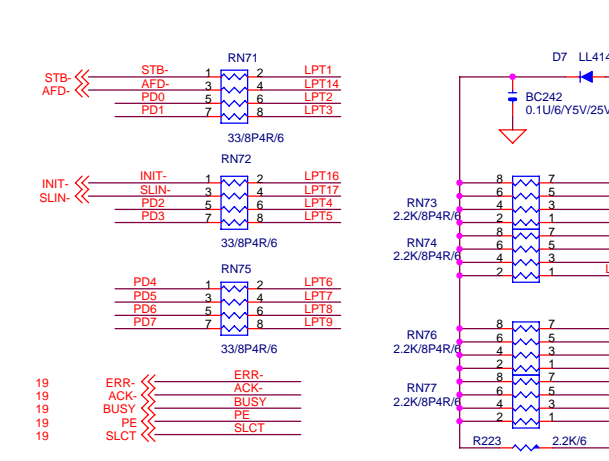
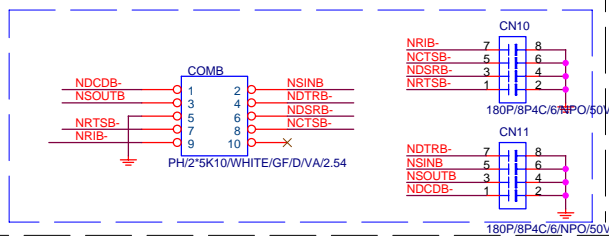
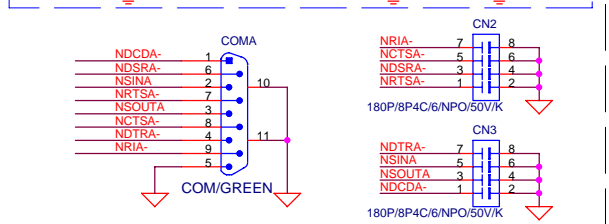
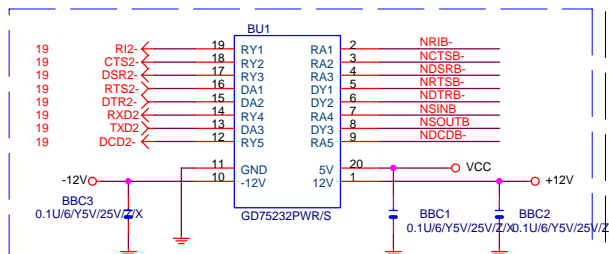
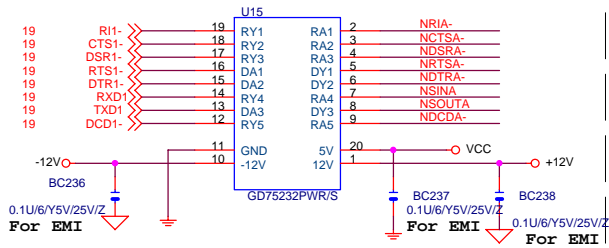
**REAR USB CONN**

VT8237 & CH BOM Only

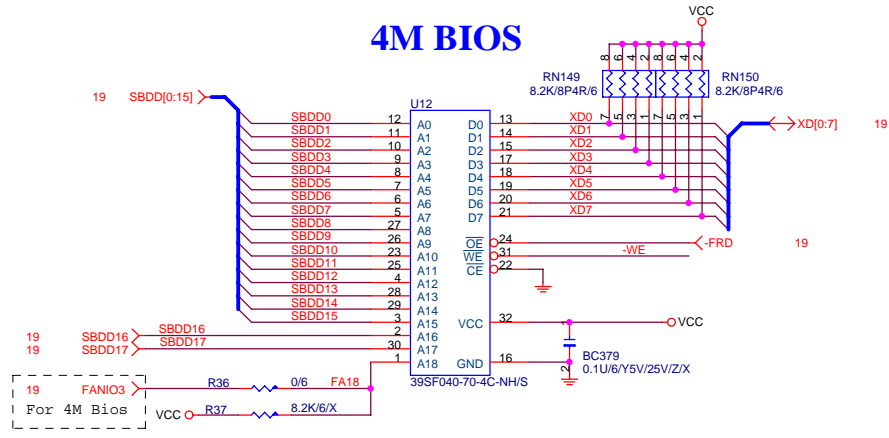


<b>GIGABYTE</b>		
<b>KB &amp; PS2 MOUSE &amp; IR</b>		
Title	Document Number	Rev
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# COMA

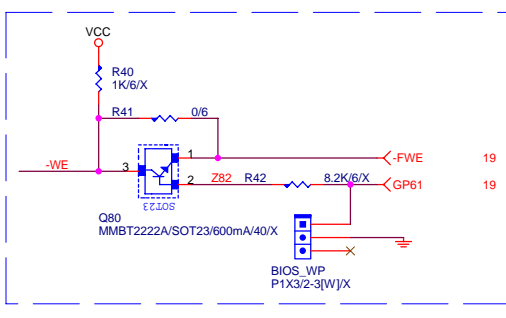


# 4M BIOS

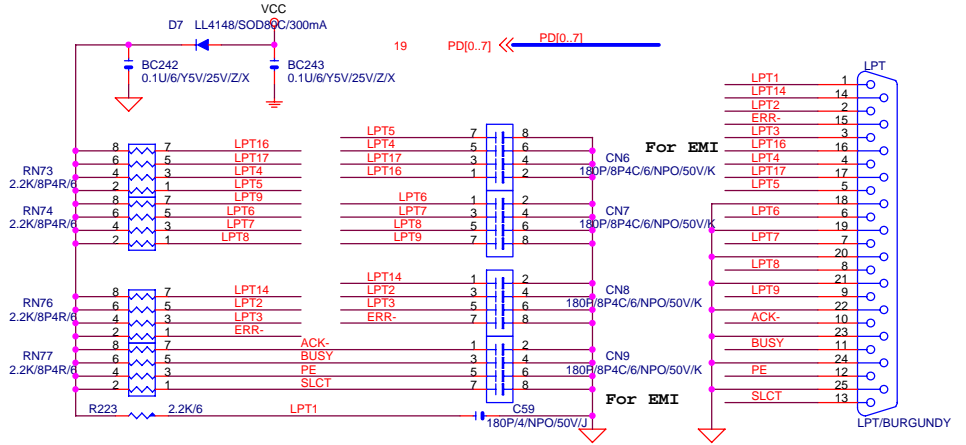
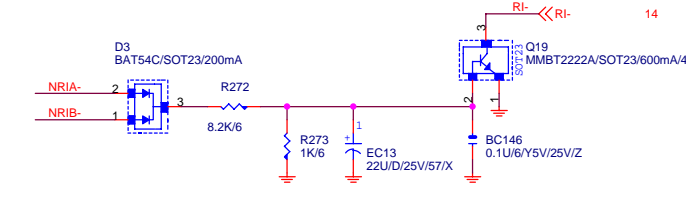
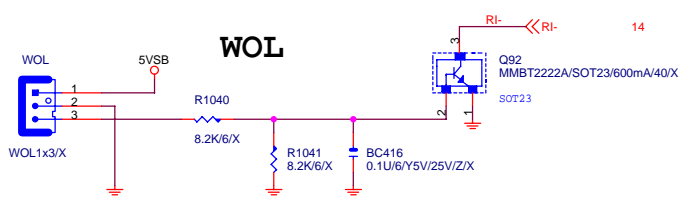
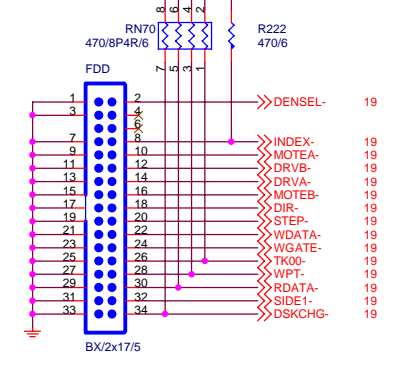


BIOS\_WP: BIOS WRITE PROTECT

PIN	BIOS_WP
1-2	WRITE PROTECT
2-3	WRITE ENABLE (default)



# FLOPPY

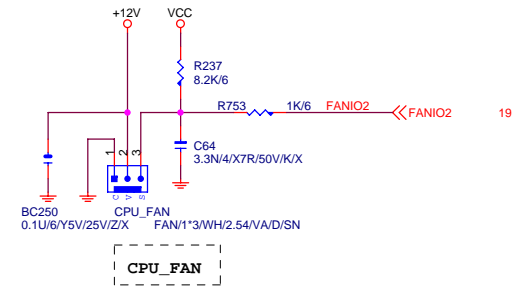
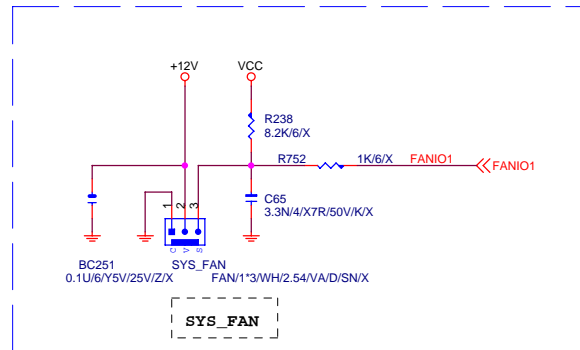
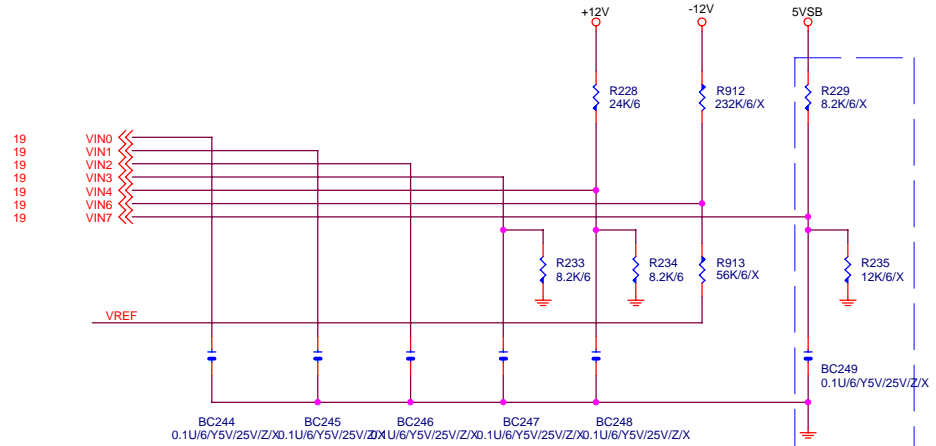
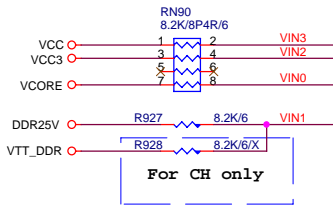
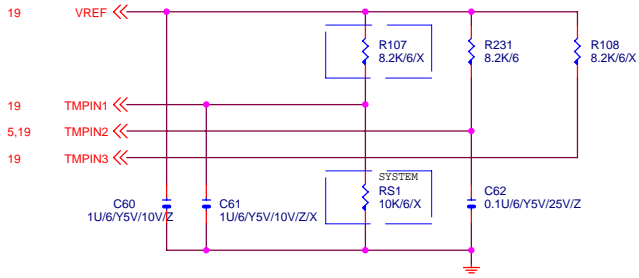


**GIGABYTE**

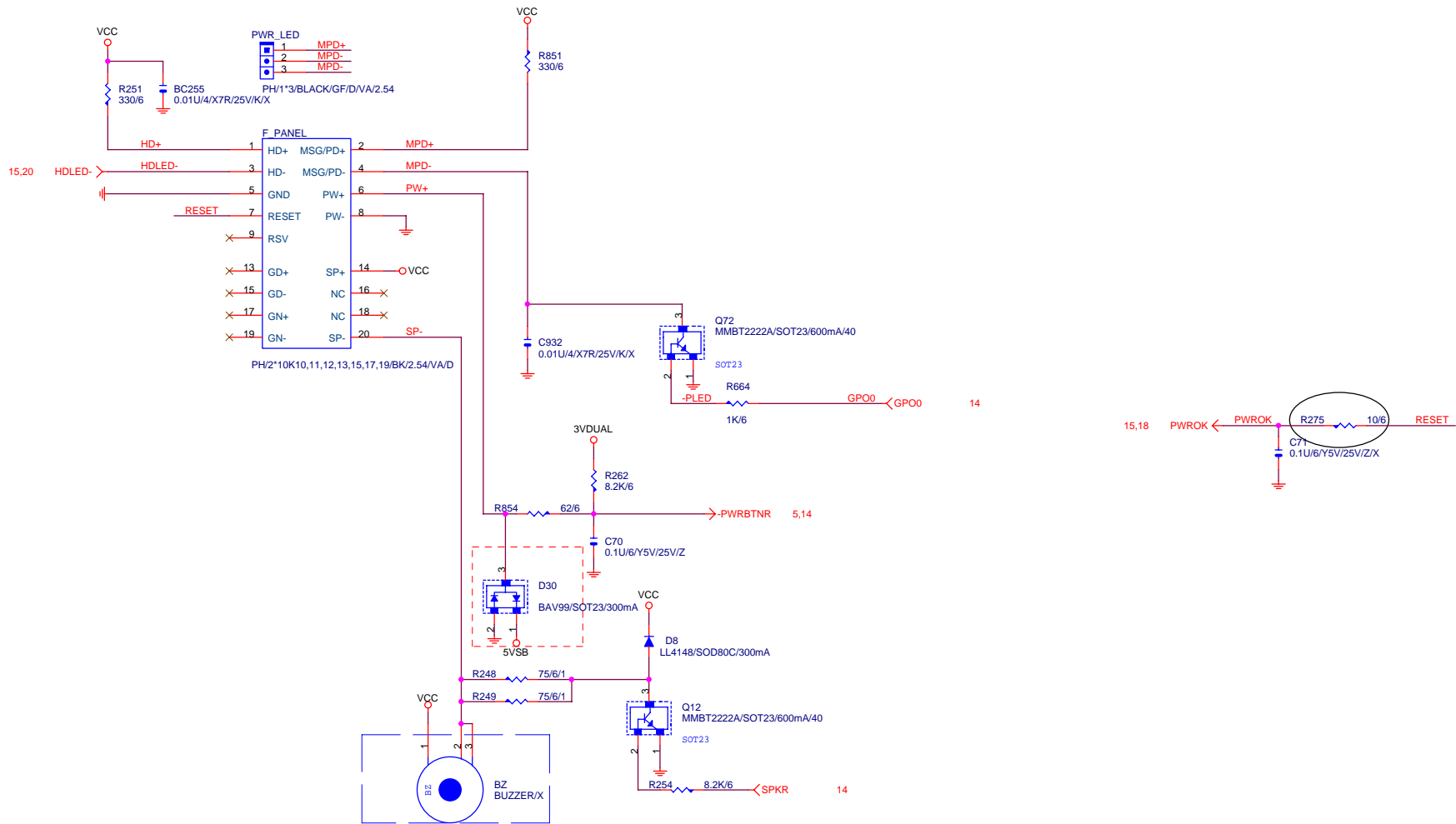
**BIOS, COM, WOR, WOL, LPT, FDD**

Title	BIOS, COM, WOR, WOL, LPT, FDD	
Size	Document Number	Rev
B	8VM800M	1.01
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# Hardware Monitor circuits



<b>GIGABYTE</b>		
Title <b>FAN/ HW MONITOR</b>		
Size B	Document Number <b>8VM800M</b>	Rev <b>1.01</b>
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**States for a single-color power LED**

LED States	ACPI States	GP025	GP027	GP035
OFF	S1,S3,S5	1	1	NO1
Steady Green	S0	0	1	0
Blinking Green	S0(message waiting)	0	B	0

NO1 GP035 只需在  
S1 PROGRAMMING  
← LOW

**States for a dual-color power LED**

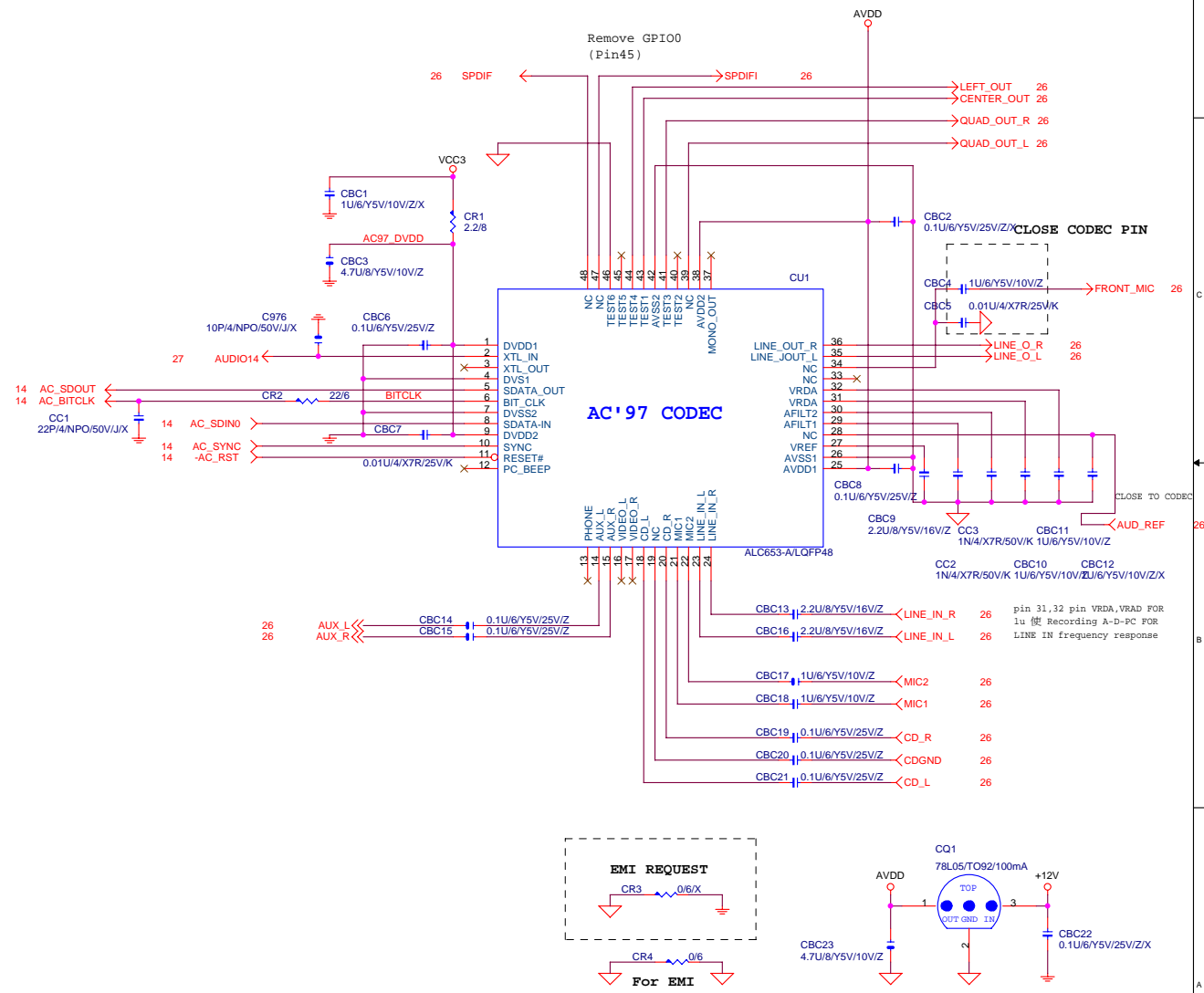
LED States	ACPI States	GP025	GP027	GP035
OFF	S5	1	1	X
Steady Green	S0	0	1	0
Blinking Green	S0(message waiting)	0	B	0
Steady Yellow	S1,S3	1	0	NO1
Blinking Yellow	S1,S3(message waiting)	1	B	NO1

**States for green LED**

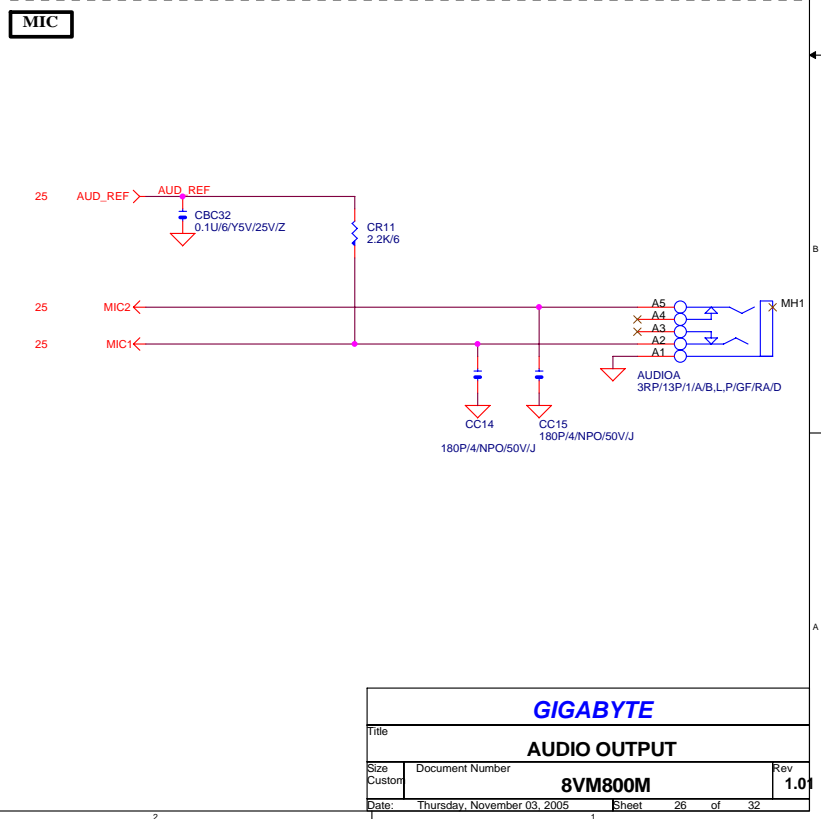
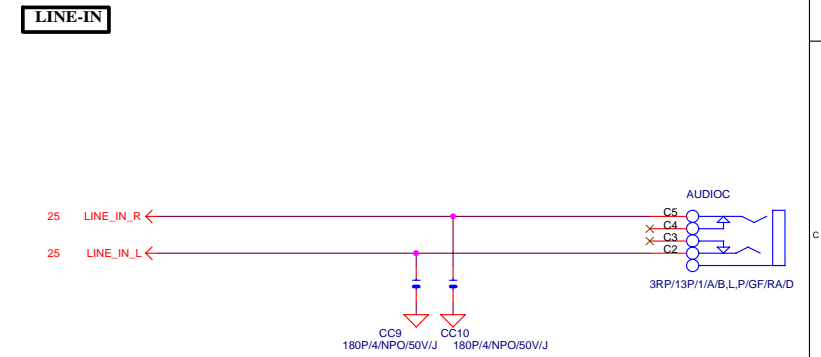
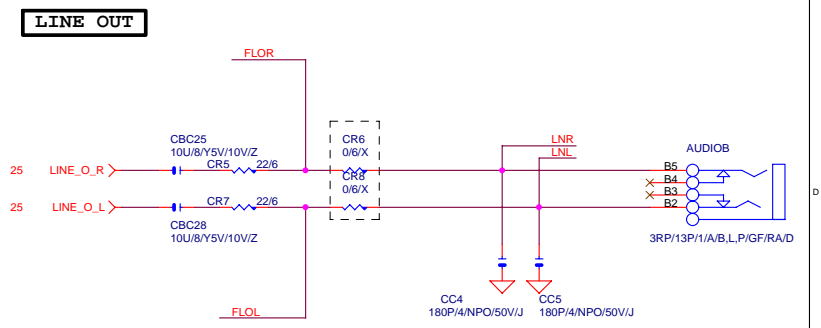
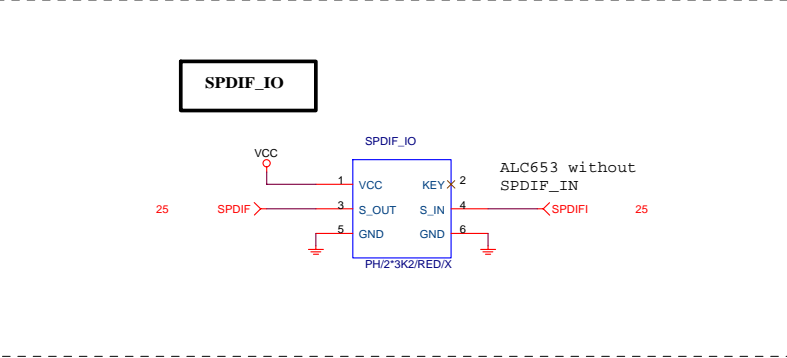
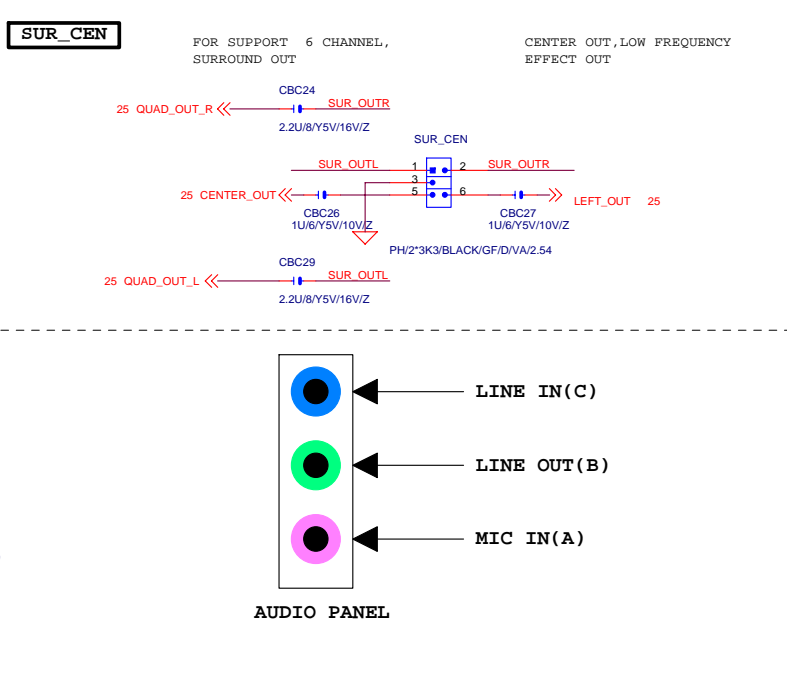
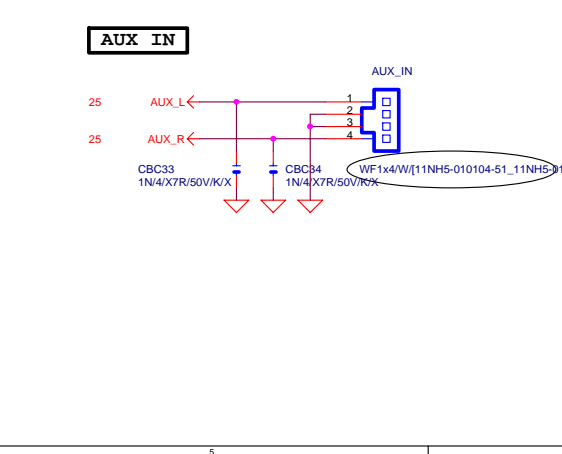
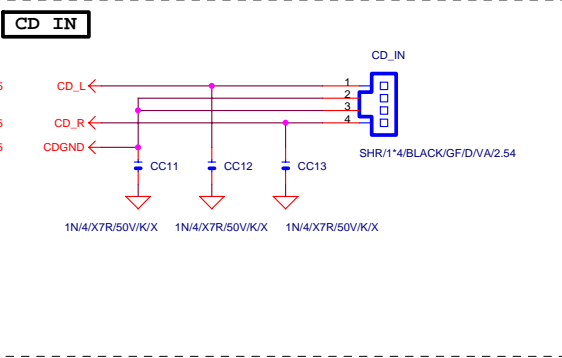
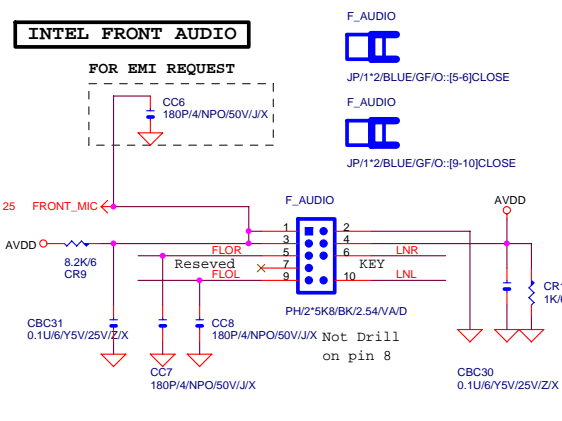
LED States	ACPI States	GP028
ON	S1,S3	0
OFF	S0,S5	1

(GP028 DEFAULT HIGH, RESUME WELL)

<b>GIGABYTE</b>		
<b>PANEL &amp; STR LED</b>		
Title		
Size B	Document Number	Rev
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Date:	Thursday, November 03, 2005	Sheet 24 of 32

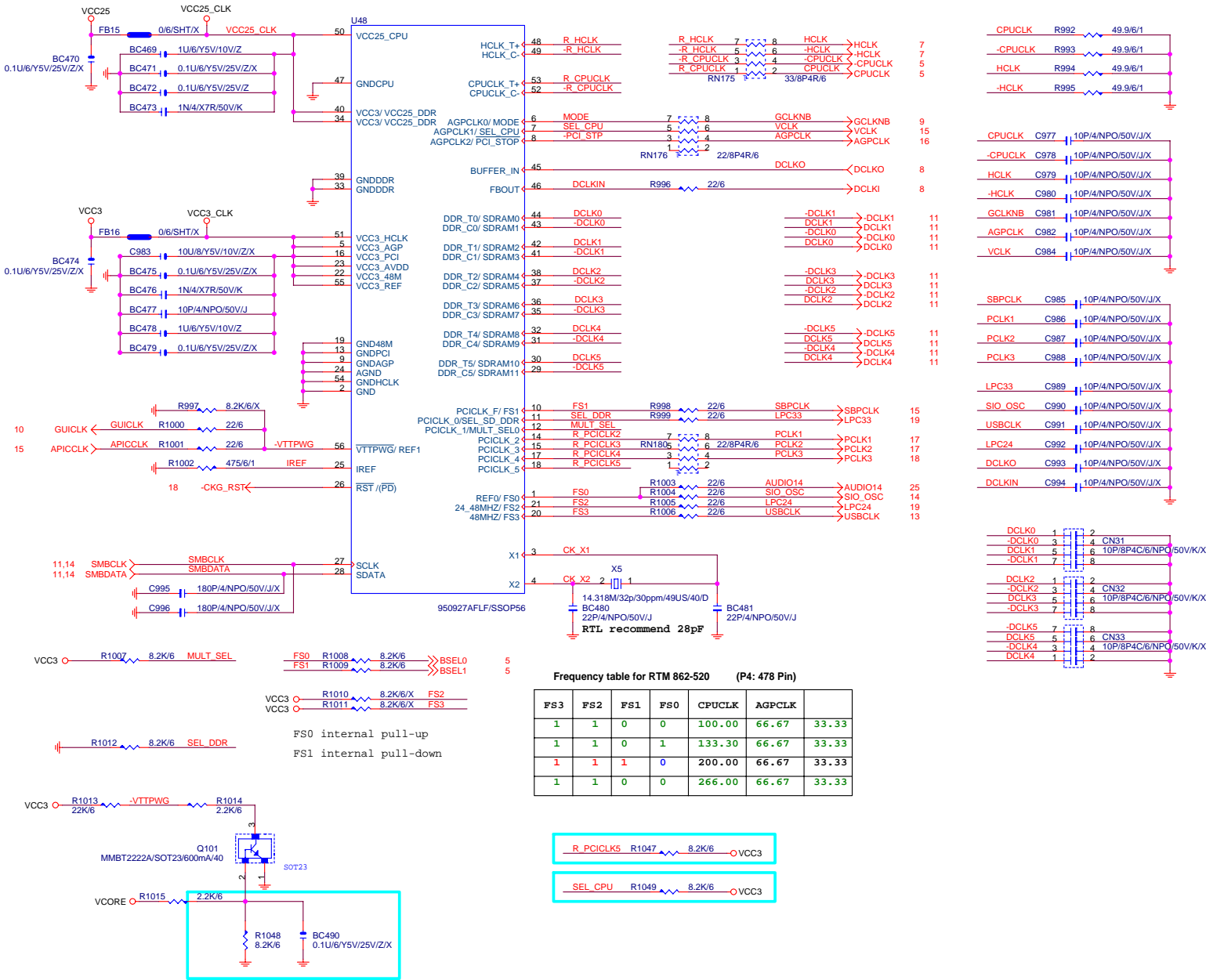


<b>GIGABYTE</b>		
<b>AUDIO (ALC655)</b>		
Title		
Size	Document Number	Rev
Custom	<b>8VM800M</b>	<b>1.01</b>
Date:	Thursday, November 03, 2005	Sheet 26 of 32

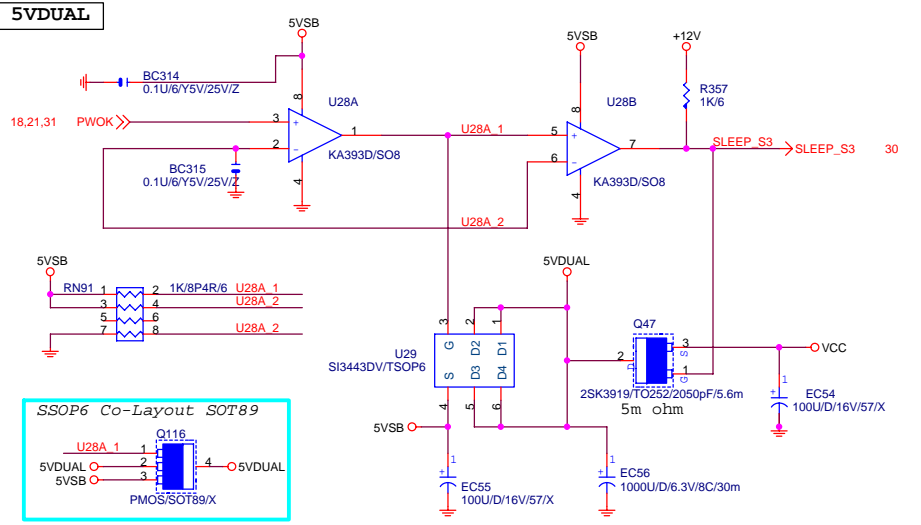
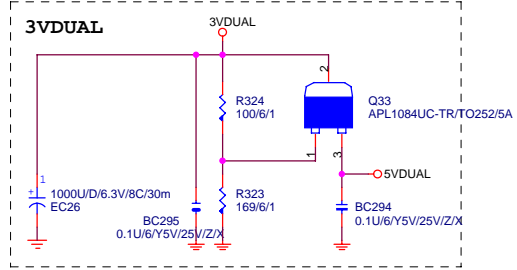
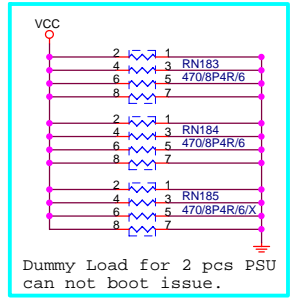
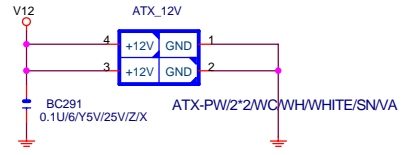
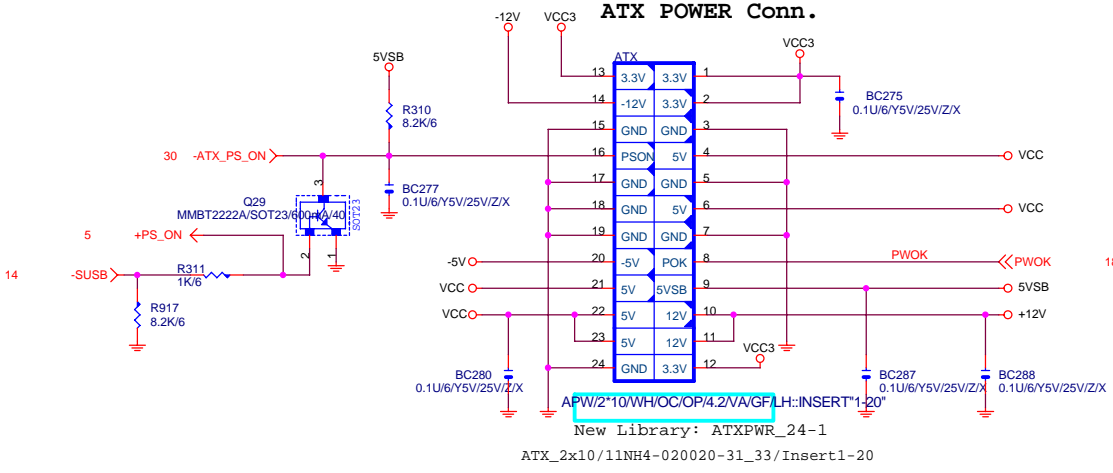


<b>GIGABYTE</b>		
<b>AUDIO OUTPUT</b>		
Title	Document Number	Rev
	<b>8VM800M</b>	<b>1.01</b>
Date:	Thursday, November 03, 2005	Sheet 26 of 32

# CLOCK GENERATOR

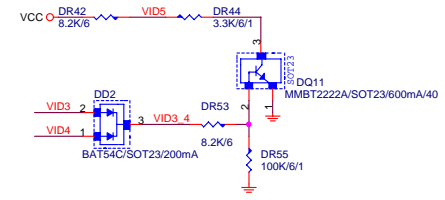
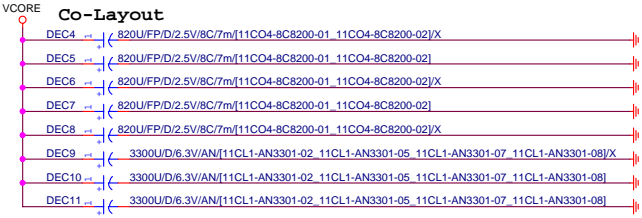
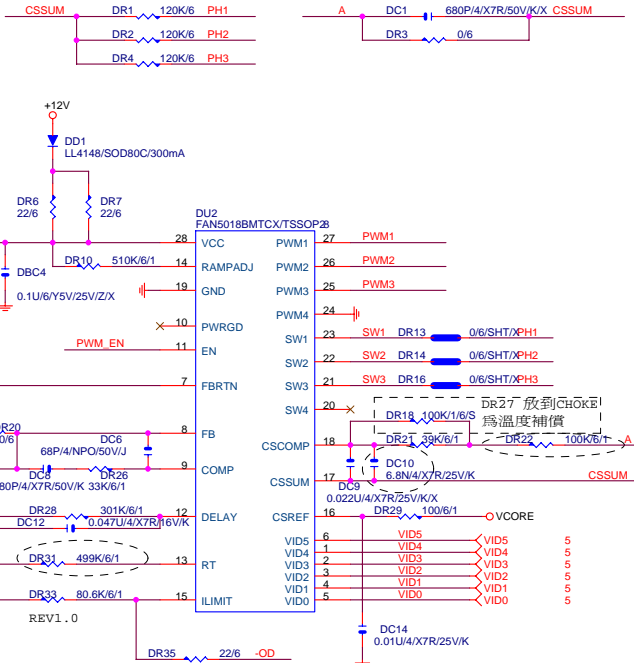


### ATX POWER Conn.

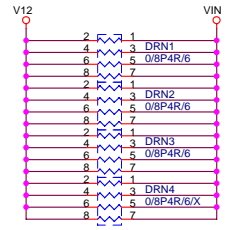
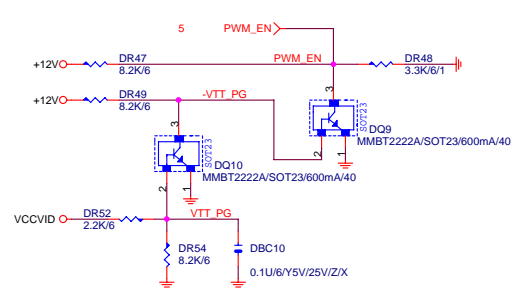
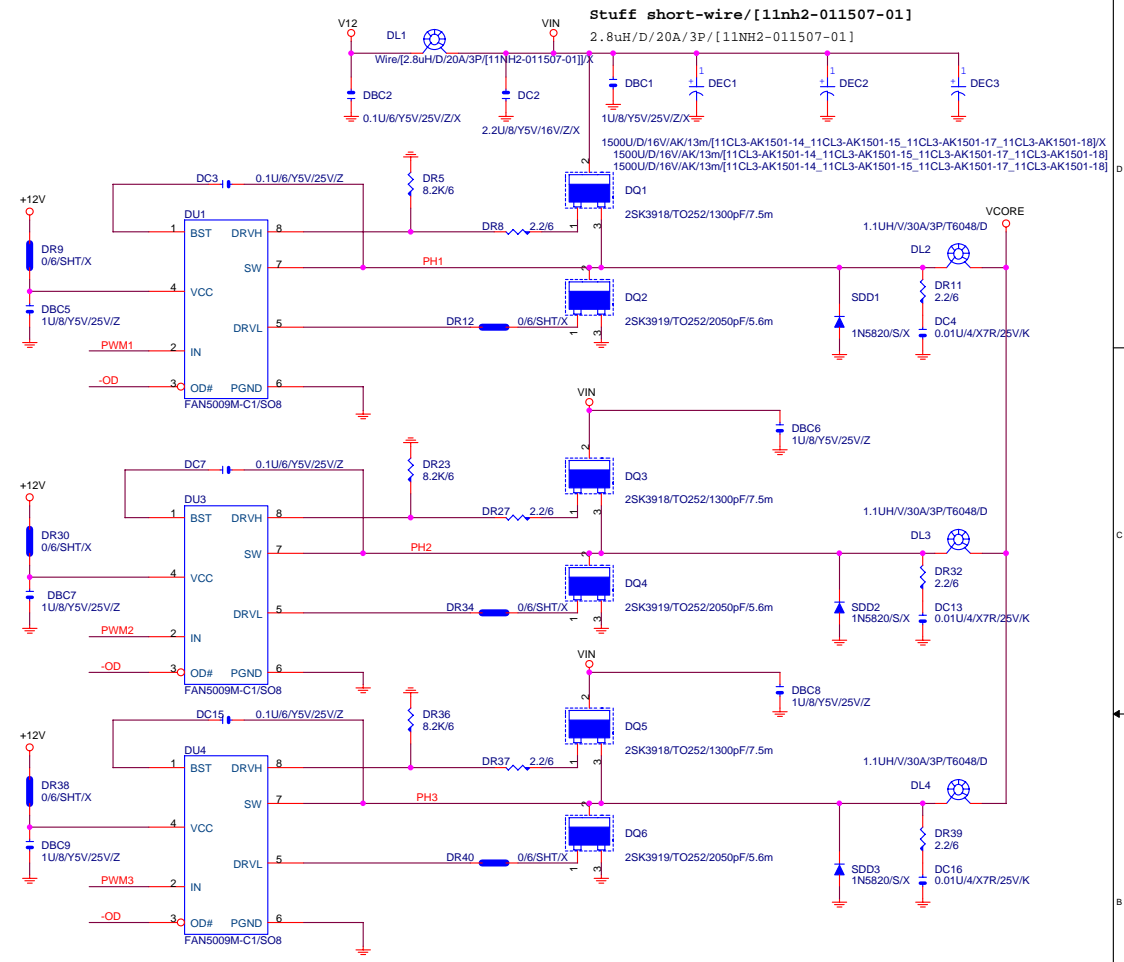
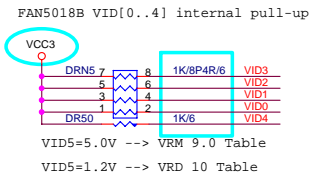


<b>GIGABYTE</b>			
Title <b>Misc. PWR &amp; ATX CONN.</b>			
Size B	Document Number <b>8VM800M</b>	Rev <b>1.01</b>	
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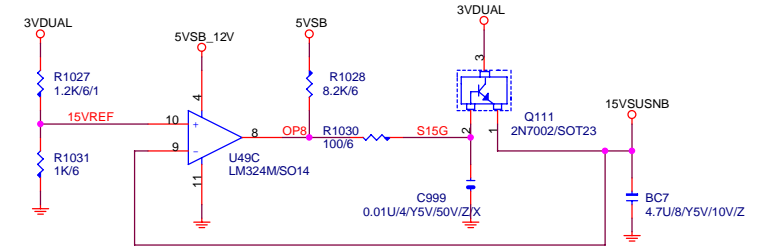
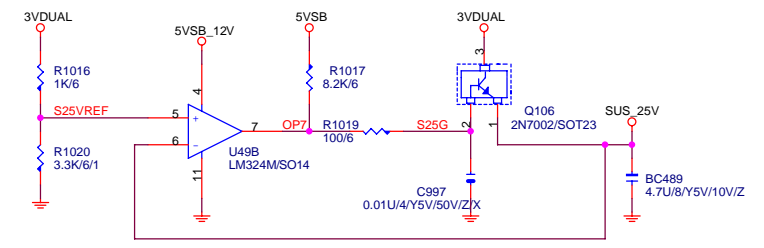
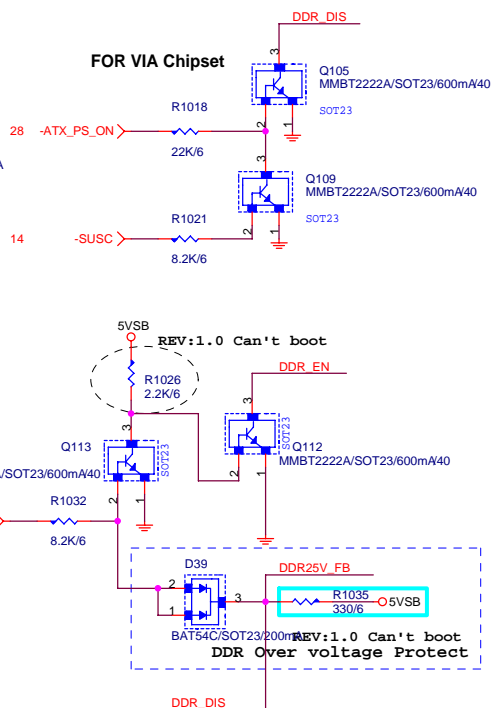
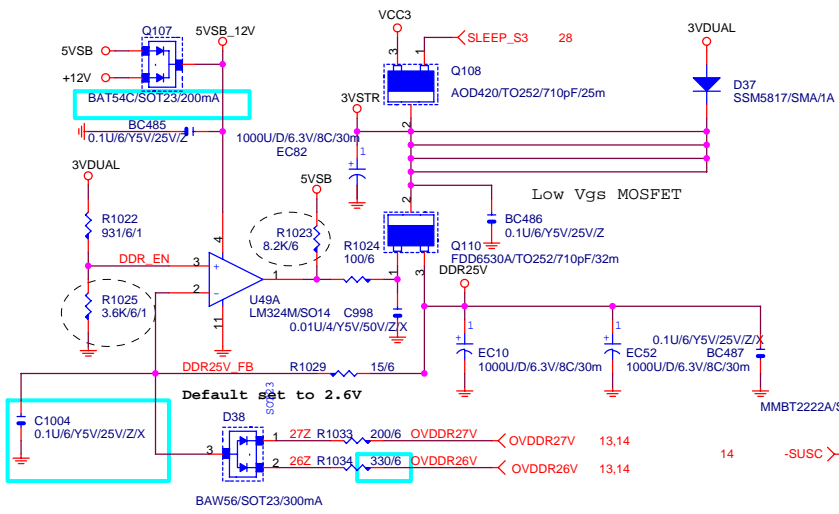
DD1 : 在HIGH SIDE 發生S-D SHORT 時(OVP), LOW SIDE MOSFET TURN ON, 讓VCORE 降壓, 同時V12 也會下降6~7V以下時, 造成PWM 無法提供POWER TO LOW SIDE TURN ON, 所以加DD1 延長PWM POWER 提供給LOW SIDE MOSFET TURN ON 保護CPU VOLTAGE 過高  
 DR9, DC5 FOR V12 OVER 19V 以上, SPEC (18V)  
 DR12 為一個 CYCLE的DUTY (50%)  
 DELAY : 限流時間DELAY (DR35, DC13) 才啓動.  
 DR39: 240K  
 工作頻率=720KHZ / 4PHASE=180K(1 PHASE)



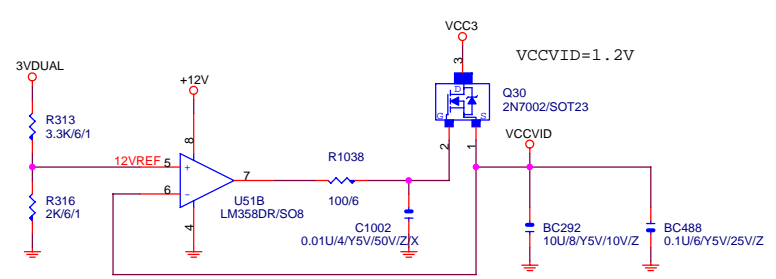
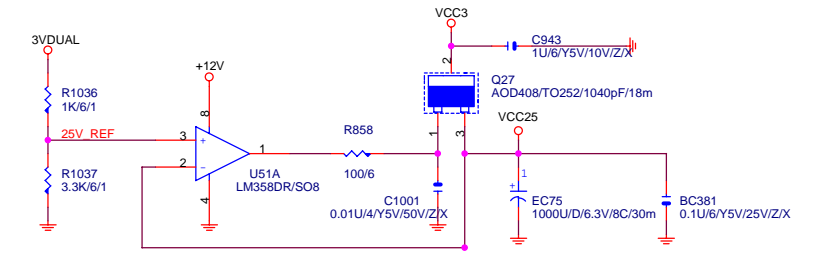
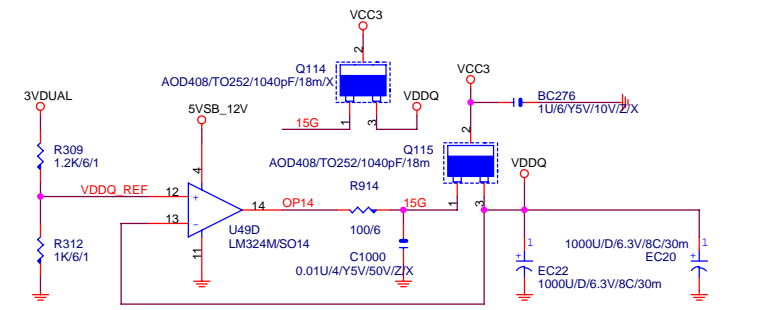
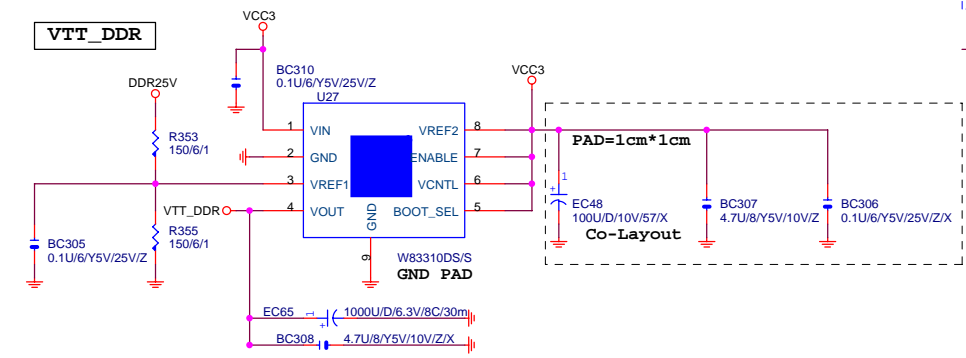
	VID3+VID4	BOOTSEL
Willamette	0	0
Northwood	1	0
Prescott	1	1



# DDR25V=2.6V FOR DDR DIMM & NB

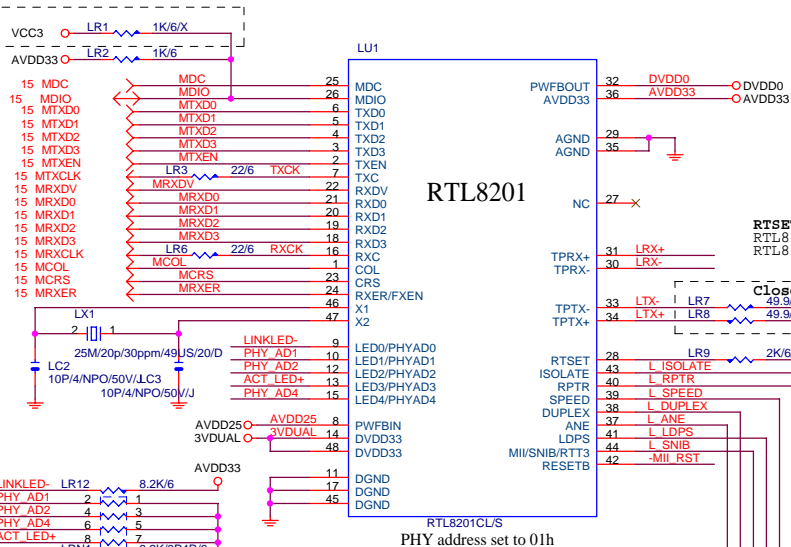


## VTT\_DDR



<b>GIGABYTE</b>			
<b>DDR POWER &amp; AVDD25V &amp; SUS_25V</b>			
Title	Document Number		Rev
	<b>8VM800M</b>		<b>1.01</b>
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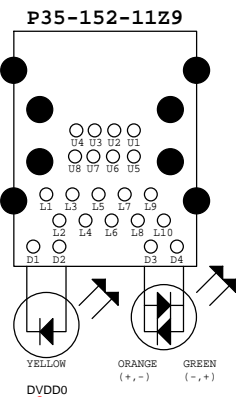
MDIO nvidia recommend  
pull-up to VCC3



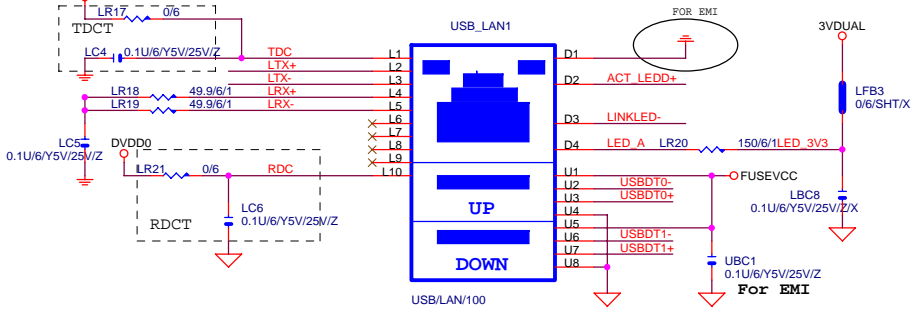
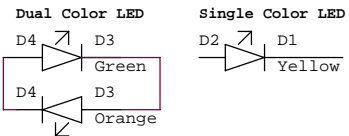
PHY Addr --> 00001

RTL8139C+ should configure to MDux = 0, MLink=1  
MDupActiveState = 0 MLinkActiveState = 1

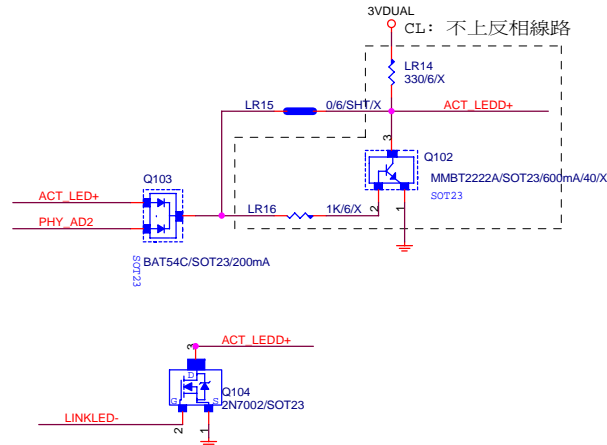
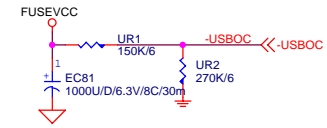
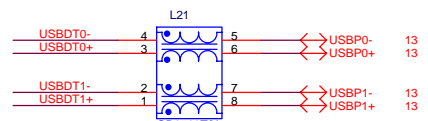
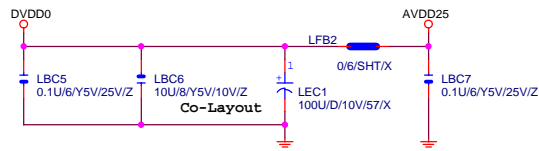
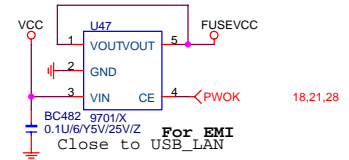
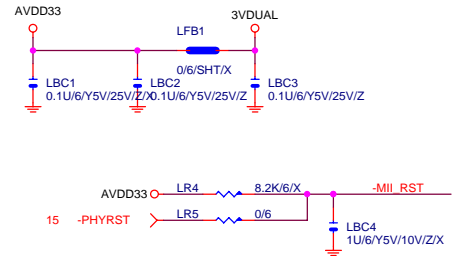
Enable: N-way, Full duplex, 100Mbps, Link Down Power Saving  
Disable: Isolate, Repeater Mode



Link(Speed)	Link to Hub	Active (Data Transmit)
10Mb	Green (ON)	Yellow (Blink)
100Mb	Green (ON)	Yellow (Blink)
1Gb	--	--

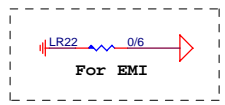


RTL8201	BL	CL
TDCT	NC	PULL HIGH 0 OHM & 0.1uF TO GND
RDCT	0.1uF	PULL HIGH 0 OHM & 0.1uF TO GND



Place decoupling capacitor DC1-DC5 as close as possible to each power pin

BLOCK A : The components inside BLOCK A are reserved for RTL8201B(.25u version). In RTL8201B, DVDD0 and AVDD0 will be fed 2.5V produced by BLOCK A which is functional as linear regulator and L3, R6 will be removed. In order to be layout-compatible between RTL8201 and RTL8201B, please reserve the component space and pads in your layout for future extension.



**GIGABYTE**

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