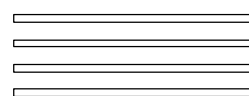


8SR533 Schematics

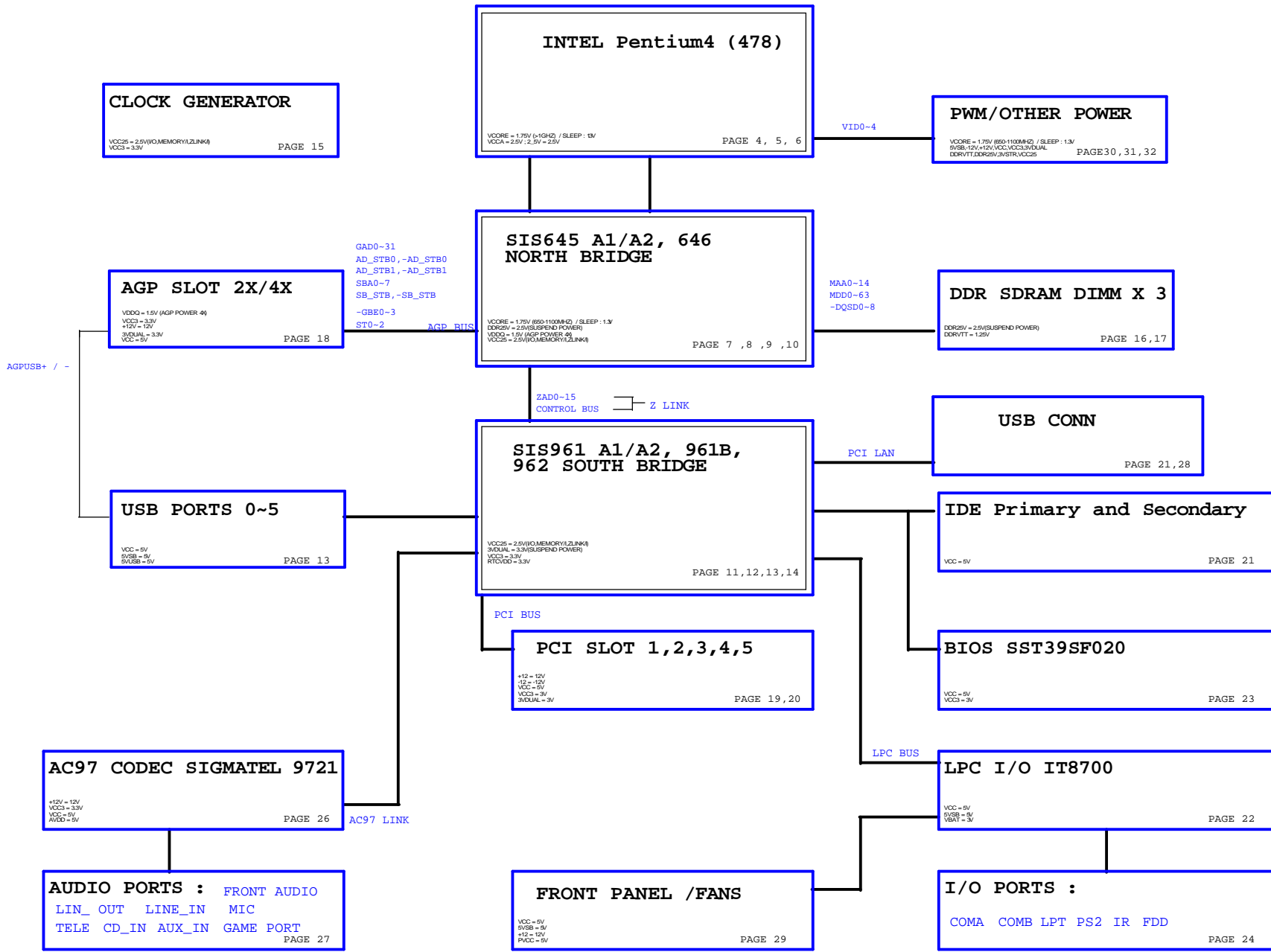
Revision 2.0

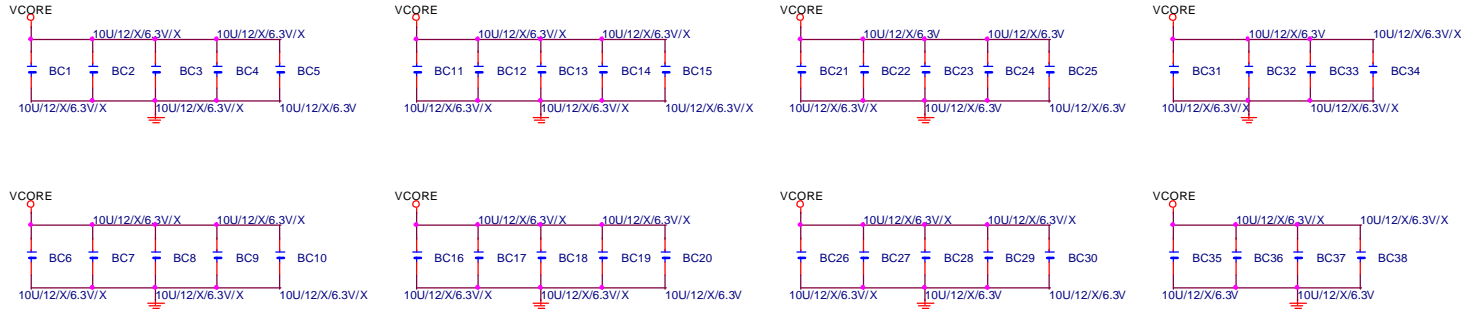
SHEET	TITLE
1	COVER SHEET
2	BOM & PCB MODIFY HISTORY
3	BLOCK DIAGRAM
4,5,6	INTEL CPU_WMT_478
7-10	SIS645 (NORTH BRIDGE) HOST; DDR; AGP,HYPER ZIP
11-14	SIS961 (SOUTH BRIDGE)
15	CLOCK GENERATOR (ICS952001)
16,17	DDR SDRAM DIMMS 1,2,3
18	AGP SLOT
19,20	PCI SLOT 1,2,3,4,5,6
21	IDE,FRONT USB,PCIRST#
22	LPCIO_IT8705
23	BIOS
24	COM,PRT,FDD,KB/MS,IR
25	AUDIO (CT5880)/AC 97
26	AUDIO JACK,GAME PORT
27	FAN, SMB PORT
28	PANEL,STR LED,FANS ,CPU GN
29	VCORE PHASE PWM HIP 6302 + 6602
30	DDR POWER,3VDUAL,VDDQ DC POWER
31	ATX CONN, GPIO LIST
32	RTL8100BL

PCB Size: 304*200 mm

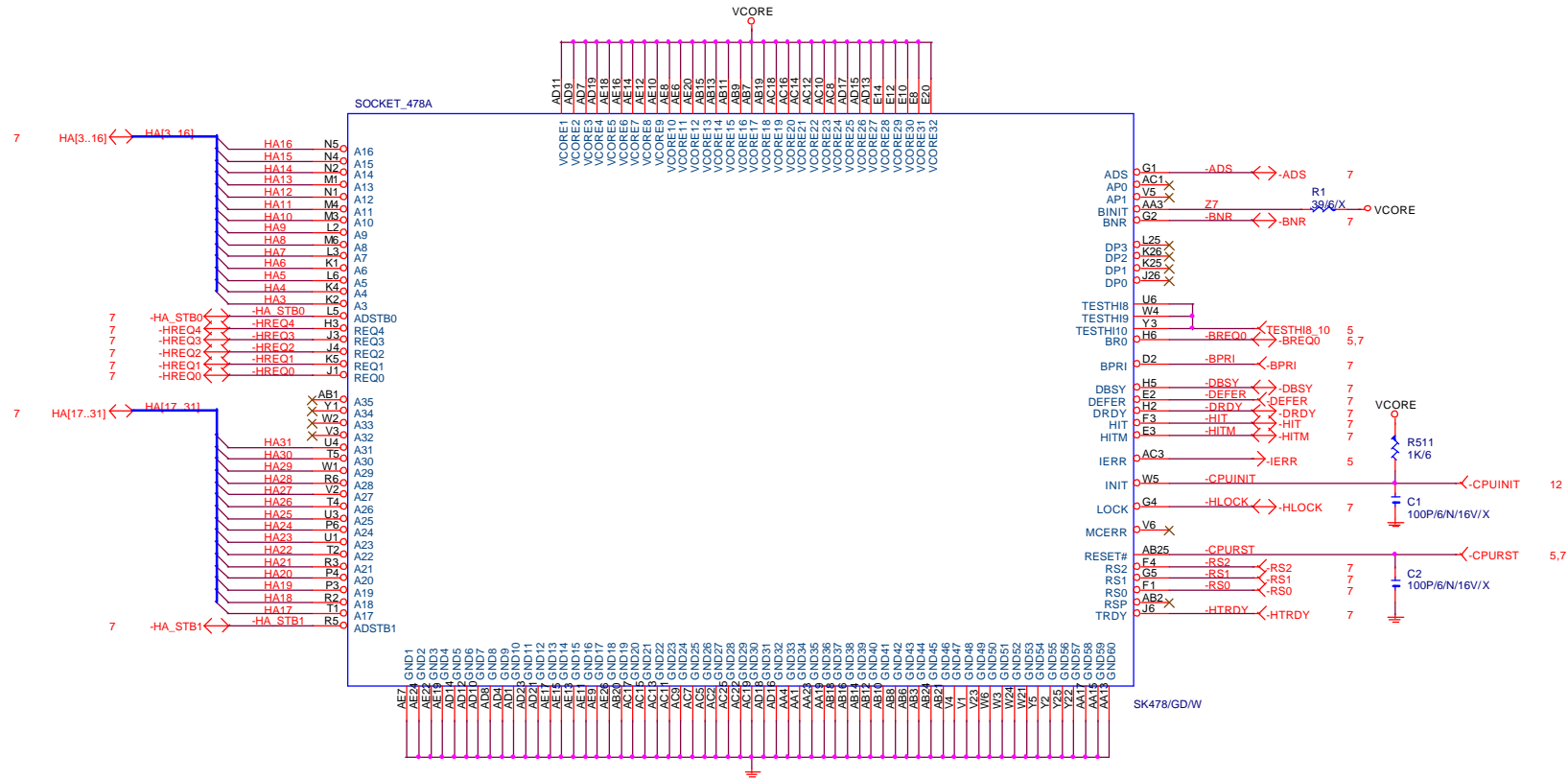
		
GIGABYTE		
COVER SHEET		
Size Custom	Document Number	Rev
	GA-8SR533	2.0
Date: Tuesday, July 02, 2002	Sheet 1 of 33	

8SR533 BLOCK DIAGRAM

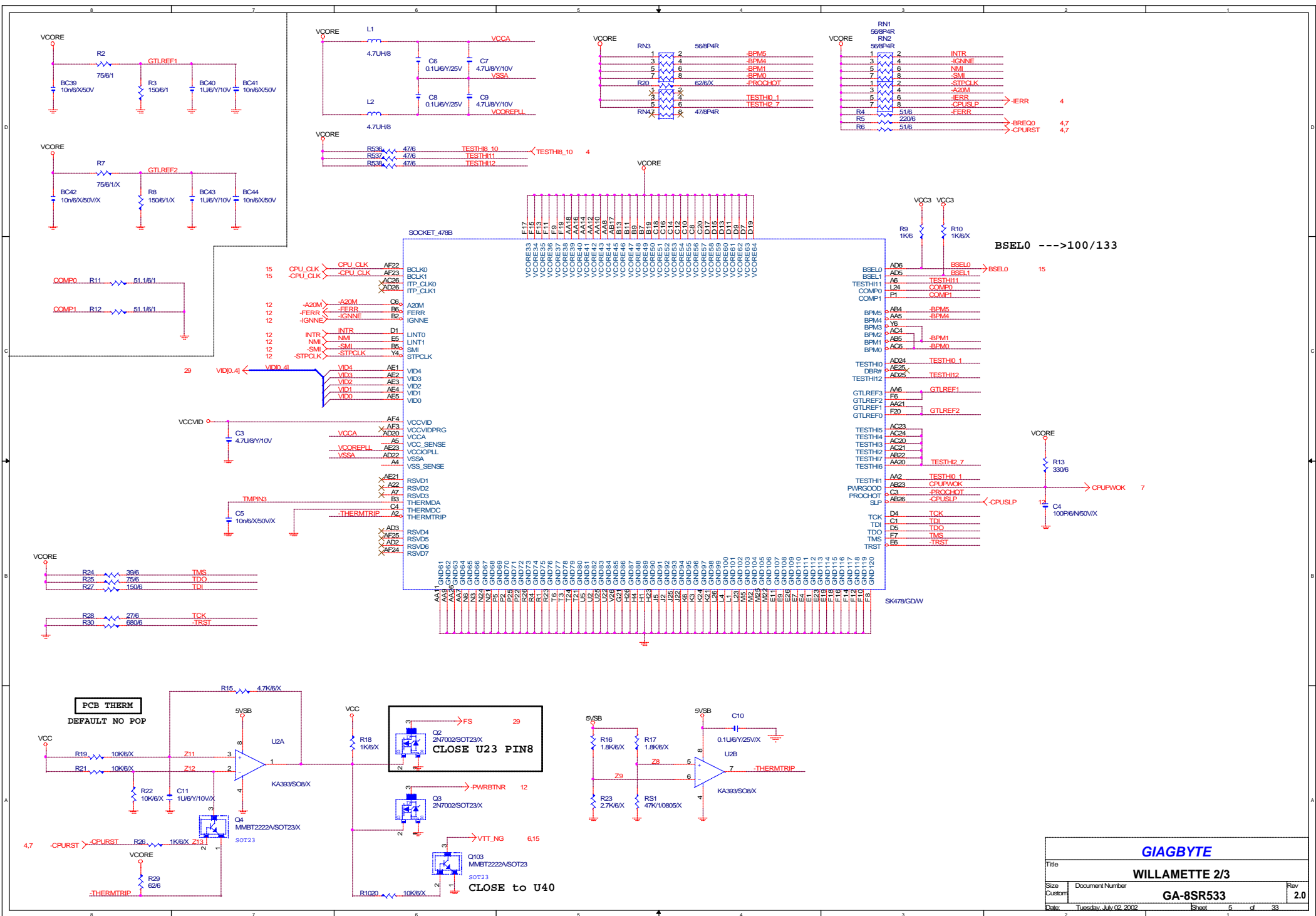




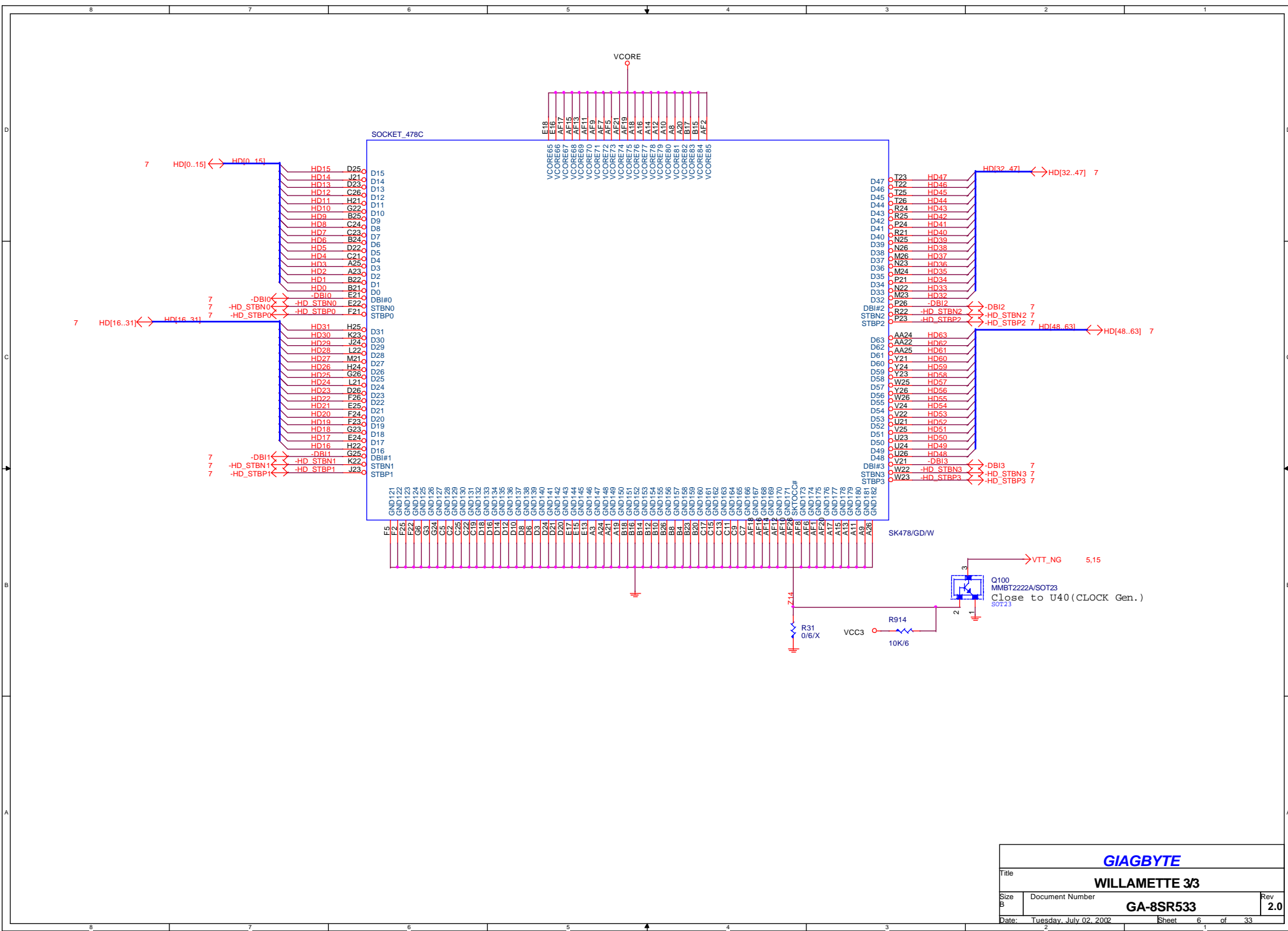
上11顆10U/X5R電容



GIAGBYTE		
Title		
WILLAMETTE 1/3		
Size	Document Number	Rev
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GIAGBYTE		
Title WILLAMETTE 2/3		
Size Custom	Document Number GA-8SR533	Rev 2.0
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GIAGBYTE		
Title		
WILLAMETTE 3/3		
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B	GA-8SR533	2.0
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SIS 645 A1/A2 , 646
共用

AGP

645-1

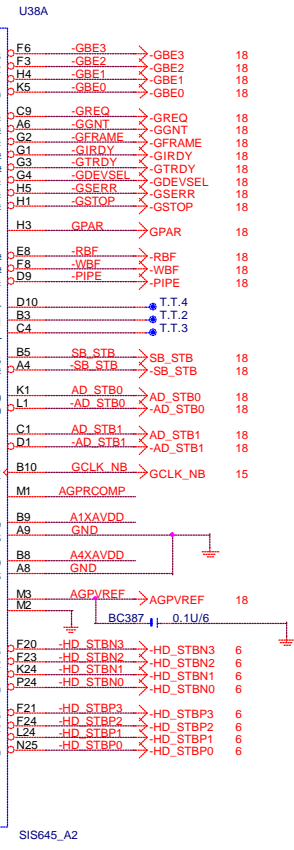
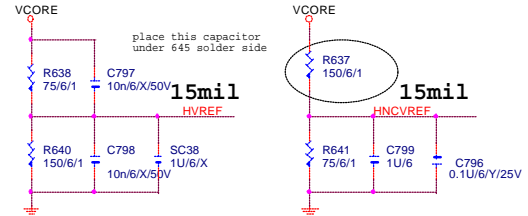
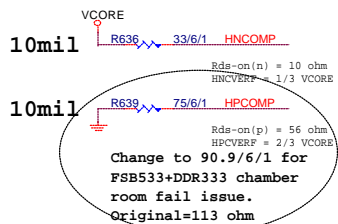
HOST

- DB[0..3] <-> -DB[0..3] 6
- HD[0..63] <-> HD[0..63] 6
- HA[3..31] <-> HA[3..31] 4
- GD[0..31] <-> GD[0..31] 18
- SBA[0..7] <-> SBA[0..7] 18
- ST[0..2] <-> ST[0..2] 18

- 15 HCLK <-> HCLK AJ26 CPUCCLK
- 15 -HCLK <-> -HCLK AH26 CPUCCLK#
- 4 -HLOCK <-> -HLOCK U24 HLOCK#
- 4 -DEFER <-> -DEFER U26 DEFER#
- 4 -HTRDY <-> -HTRDY V28 HTRDY#
- 4,5 -CPURST <-> -CPURST C20 CPURST#
- 5 -CPUPWOK <-> -CPUPWOK D19 CPUPWOK#
- 4 -BPRI <-> -BPRI T27 BPRI#
- 4,5 -BREQ0 <-> -BREQ0 U25 BREQ0#
- 4 -RS2 <-> -RS2 T24 RS#2
- 4 -RS1 <-> -RS1 T26 RS#1
- 4 -RS0 <-> -RS0 U29 RS#0
- 4 -ADS <-> -ADS V28 ADS#
- 4 -HITM <-> -HITM T28 HITM#
- 4 -HIT <-> -HIT U28 HIT#
- 4 -DRDY <-> -DRDY W26 DRDY#
- 4 -DBSY <-> -DBSY V24 DBSY#
- 4 -BNR <-> -BNR V27 BNR#
- 4 -HREQ4 <-> -HREQ4 W28 HREQ#4
- 4 -HREQ3 <-> -HREQ3 W29 HREQ#3
- 4 -HREQ2 <-> -HREQ2 W24 HREQ#2
- 4 -HREQ1 <-> -HREQ1 W25 HREQ#1
- 4 -HREQ0 <-> -HREQ0 Y27 HREQ#0
- 4 -HA_STB1 <-> -HA_STB1 AD24 HASTB#1
- 4 -HA_STB0 <-> -HA_STB0 AA24 HASTB#0

- HA31 AF26 HA#31
- HA30 AE25 HA#30
- HA29 AH28 HA#29
- HA28 AD28 HA#28
- HA27 AG29 HA#27
- HA26 AE26 HA#26
- HA25 AF28 HA#25
- HA24 AC24 HA#24
- HA23 AG28 HA#23
- HA22 AE29 HA#22
- HA21 AD28 HA#21
- HA20 AC25 HA#20
- HA19 AD27 HA#19
- HA18 AE26 HA#18
- HA17 AF27 HA#17
- HA16 AB24 HA#16
- HA15 AB26 HA#15
- HA14 AC28 HA#14
- HA13 AC26 HA#13
- HA12 AC29 HA#12
- HA11 AA26 HA#11
- HA10 AB28 HA#10
- HA9 AB27 HA#9
- HA8 AA25 HA#8
- HA7 AA29 HA#7
- HA6 AA28 HA#6
- HA5 Y26 HA#5
- HA4 Y24 HA#4
- HA3 Y28 HA#3

- HD#63 HD#63
- HD#62 HD#62
- HD#61 HD#61
- HD#60 HD#60
- HD#59 HD#59
- HD#58 HD#58
- HD#57 HD#57
- HD#56 HD#56
- HD#55 HD#55
- HD#54 HD#54
- HD#53 HD#53
- HD#52 HD#52
- HD#51 HD#51
- HD#50 HD#50
- HD#49 HD#49
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- HD#47 HD#47
- HD#46 HD#46
- HD#45 HD#45
- HD#44 HD#44
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- HD#32 HD#32
- HD#31 HD#31
- HD#30 HD#30
- HD#29 HD#29
- HD#28 HD#28
- HD#27 HD#27
- HD#26 HD#26
- HD#25 HD#25
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- HD#16 HD#16
- HD#15 HD#15
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- HD#13 HD#13
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- HD#11 HD#11
- HD#10 HD#10
- HD#9 HD#9
- HD#8 HD#8
- HD#7 HD#7
- HD#6 HD#6
- HD#5 HD#5
- HD#4 HD#4
- HD#3 HD#3
- HD#2 HD#2
- HD#1 HD#1
- HD#0 HD#0
- DB#3 DB#3
- DB#2 DB#2
- DB#1 DB#1
- DB#0 DB#0



NOTE: This page is for universal PCB design(suitable for both 645 or 650)

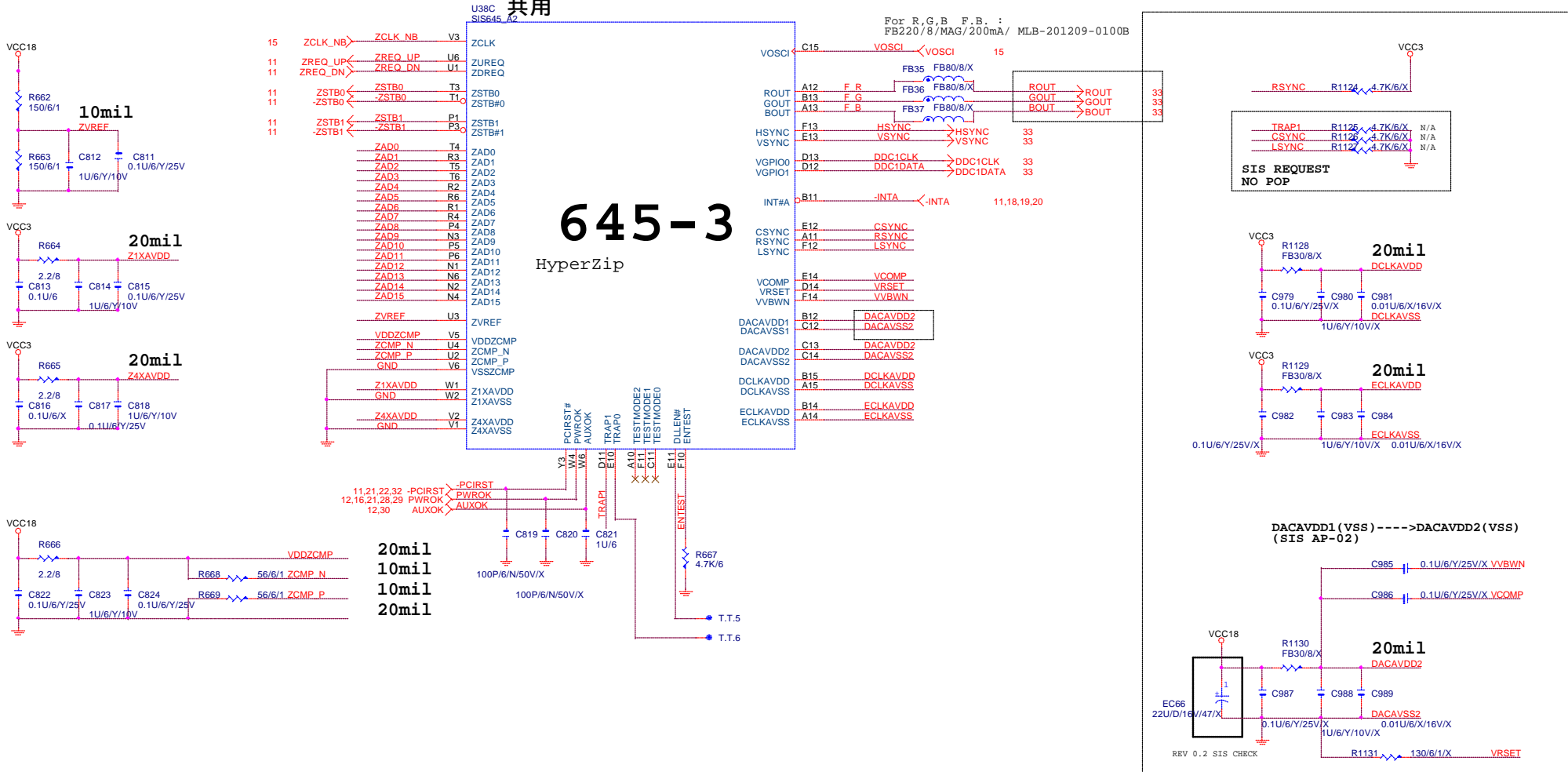
NB Hardware Trap Table			
	0	1	Default
DLENN	enable PLL	disable PLL	0
DRAM_SPL	SDR	DDR	1(DDR)
TRAP0	normal	NB debug mode	0
TRAP1	TV selection, NTSC/PAL(0/1)		
CSYNC	enable VB		0
RSYNC	enable VGA interrupt		1
LSYNC	enable panel link		0

embedded pull-low (30-50K Ohm)
yes
yes
yes

SIS 645 A1/A2 , 646
共用

645-3
HyperZip

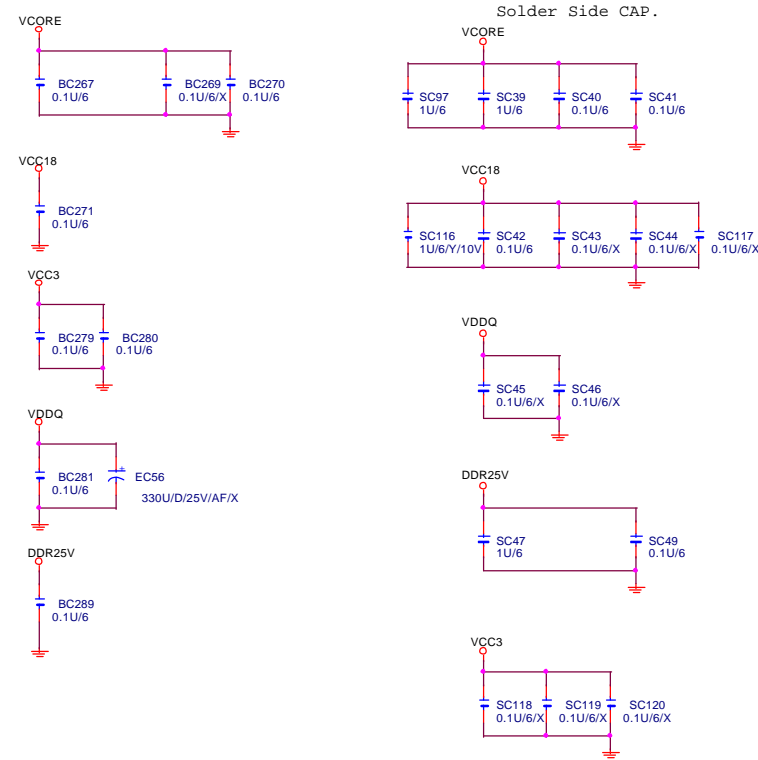
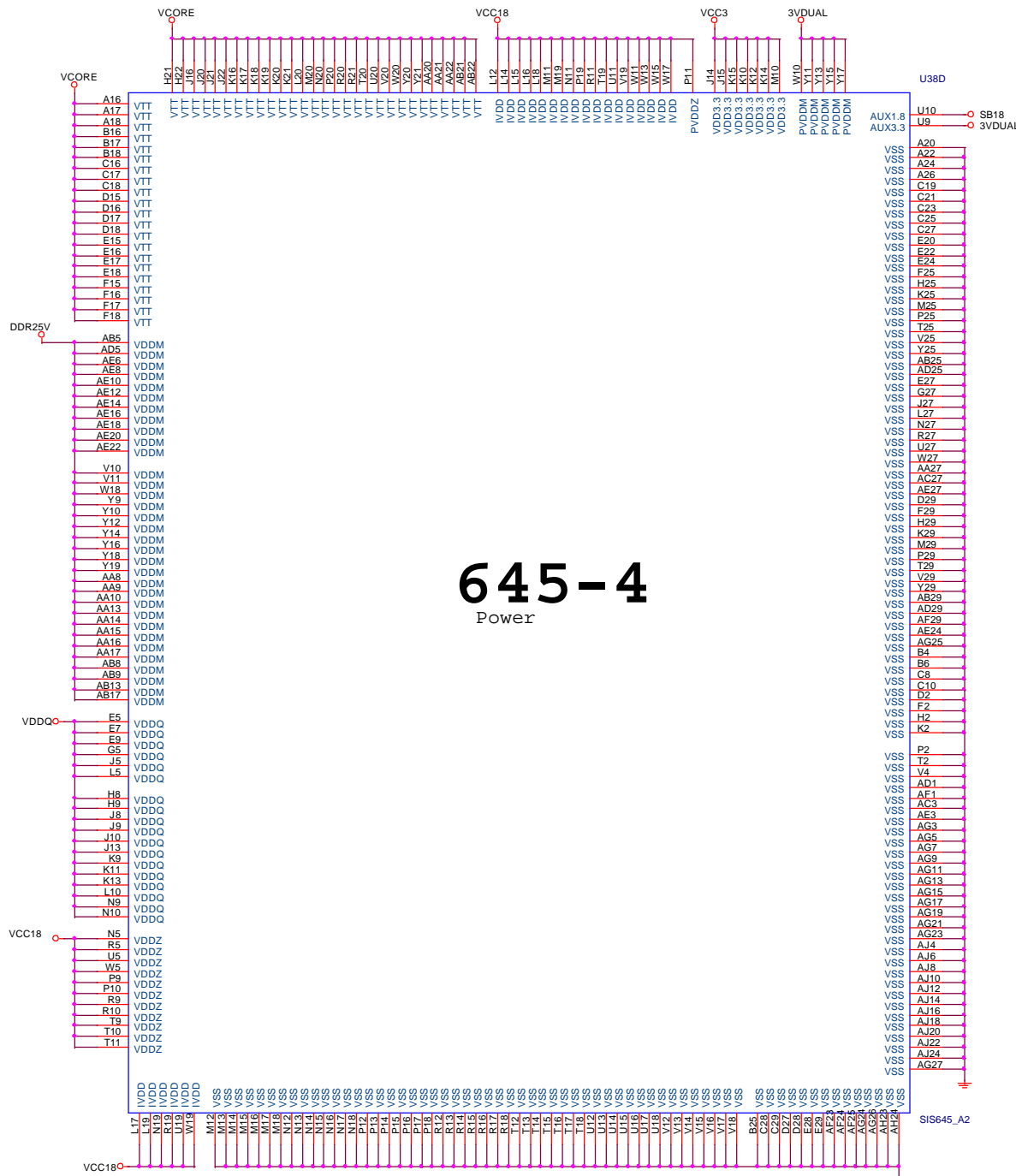
For R,G,B F.B. :
FB220/8/MAG/200mA/ MLB-201209-0100B



GIGABYTE		
Title SIS645(HYPER ZIP)		
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645-4

Power



SIS 645 A1/A2 , 646
共用

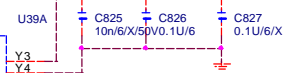
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Title SIS645(PWR)		
Size Custom	Document Number GA-8SR533	Rev 2.0
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PDD0_15] <-> PDD[0..15] 21
 SDD0_15] <-> SDD[0..15] 21
 -REQ0_4] <-> REQ[0..4] 19,20
 -GNT0_4] <-> GNT[0..4] 19,20
 -C_BE0_3] <-> C_BE[0..3] 19,20,32
 AD0_31] <-> AD[0..31] 19,20,32
 ZAD0_15] <-> ZAD[0..15] 9

SIS 961 A1/A2 , 961B, 962

AD31 HI2
 AD30 HI1
 AD29 HI1
 AD28 HI1
 AD27 HI1
 AD26 HI1
 AD25 HI1
 AD24 HI1
 AD23 HI1
 AD22 HI1
 AD21 HI1
 AD19 HI1
 AD18 HI1
 AD17 HI1
 AD16 HI1
 AD15 HI1
 AD14 HI1
 AD13 HI1
 AD12 HI1
 AD11 HI1
 AD10 HI1
 AD9 HI1
 AD8 HI1
 AD7 HI1
 AD6 HI1
 AD5 HI1
 AD4 HI1
 AD3 HI1
 AD2 HI1
 AD1 HI1
 AD0 HI1

20mil
VCC18



PCI

F1 PREQ#4
 F2 PREQ#3
 E1 PREQ#2
 H5 PREQ#1
 F3 PREQ#0
 H3 PGNT#4
 G1 PGNT#3
 G2 PGNT#2
 G3 PGNT#1
 H4 PGNT#0
 K3 C/BE#3
 M4 C/BE#2
 P1 C/BE#1
 R4 C/BE#0
 E3 INT#A
 F4 INT#B
 E2 INT#C
 G4 INT#D
 M3 FRAME#
 M1 IRDY#
 M2 TRDY#
 N4 STOP#
 M5 SERR#
 N3 PAR
 M1 DEVSEL#
 N2 PLOCK#
 Y2 PCICLK_SB
 C3 PCIRST#

IDE

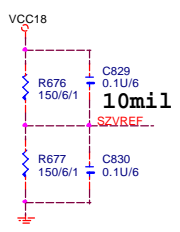
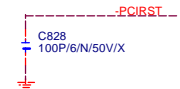
961A-1

V20 ZCLK
 N19 ZSTB0
 N20 ZSTB0#
 K20 ZSTB1
 K19 ZSTB1#
 N16 ZUREQ
 N17 ZDREQ

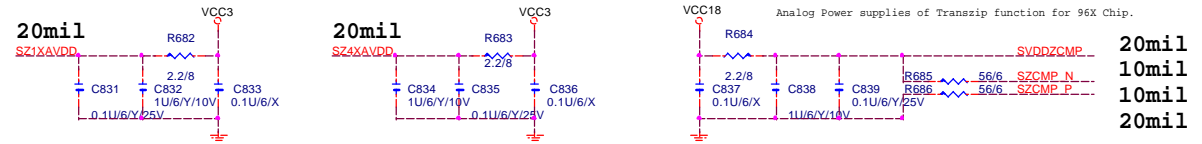
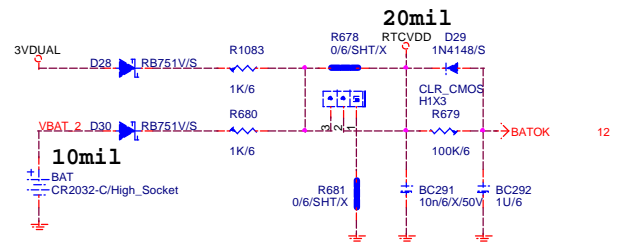
HyperZip

R19 VDDZCMP
 N18 ZCMP_N
 R18 ZCMP_P
 P18 VSSZCMP
 U20 Z1XAVDD
 U19 Z1XAVSS
 T20 Z4XAVDD
 T19 Z4XAVSS
 R20 ZVREF
 P20 ZVSSREF

IDEAVDD Y3
 IDEAVSS Y4
 W10 PIORDY
 V10 PDDREQ
 Y11 IRQ14
 U12 P66DET
 V11 PDIOR
 Y9 PDIOV
 Y10 PDDACK
 T11 PDA2
 U11 PDA1
 W11 PDA0
 T12 PDCS3
 V12 PDCS1
 W17 SIORDY
 Y17 SDDREQ
 T16 IRQ15
 U17 S66DET
 T14 SDIOR
 W16 SDIOV
 V16 SRPCK
 Y18 SDA2
 T15 SDA1
 V17 SDA0
 U16 SDCS3
 W18 SDCS1
 U10 PDD0
 V9 PDD1
 W8 PDD2
 T9 PDD3
 Y7 PDD4
 V7 PDD5
 Y6 PDD6
 Y5 PDD7
 W6 PDD8
 U8 PDD9
 W7 PDD10
 V8 PDD11
 U9 PDD12
 Y8 PDD13
 T10 PDD14
 W9 PDD15
 Y16 SDD0
 V15 SDD1
 U14 SDD2
 W14 SDD3
 Y13 SDD4
 T13 SDD5
 Y13 SDD6
 Y12 SDD7
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 Y14 SDD11
 V14 SDD12
 W15 SDD13
 Y15 SDD14
 U15 SDD15



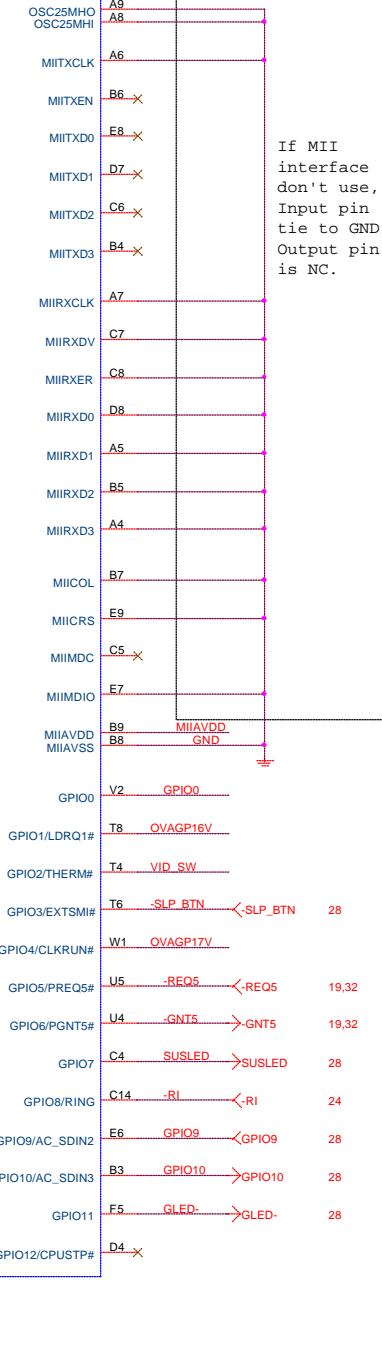
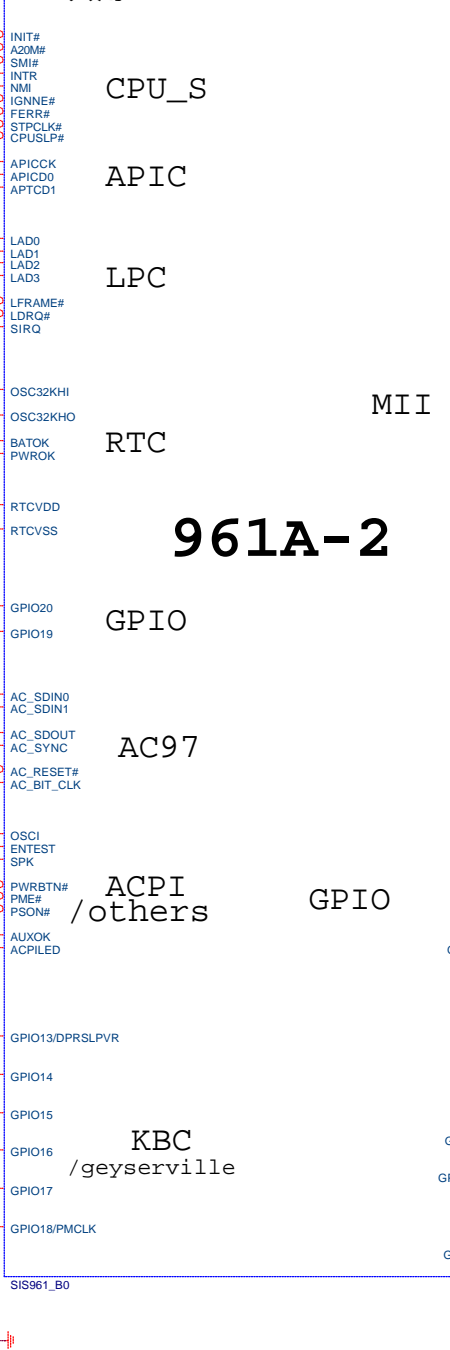
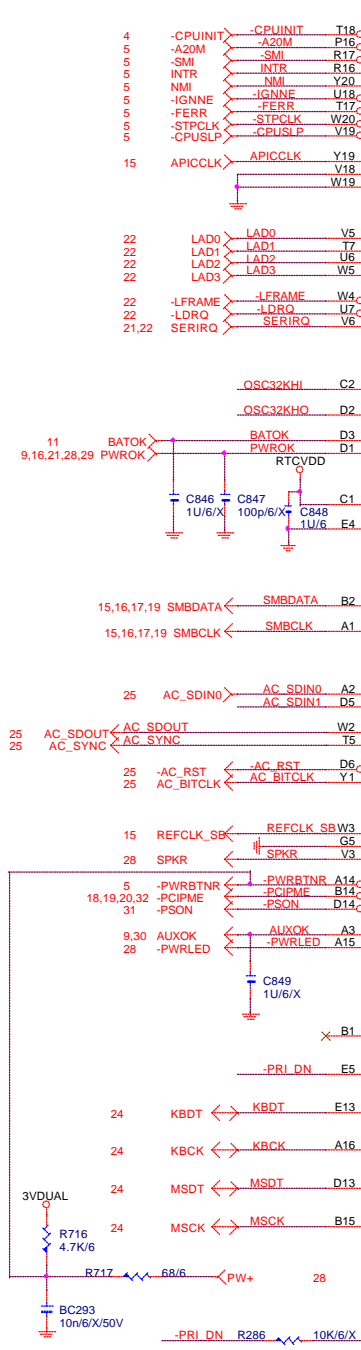
CLR_CMOS CLEAR COMS JUMPER	
1-2	Enable
2-3	Disable (Default)



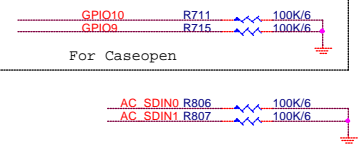
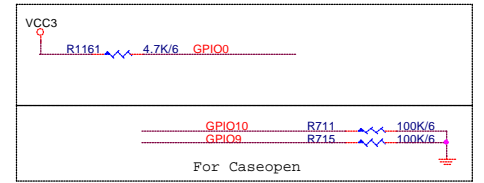
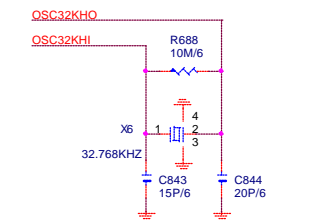
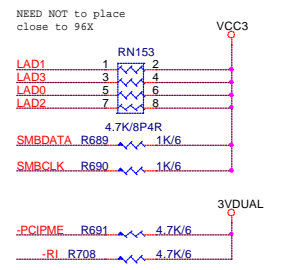
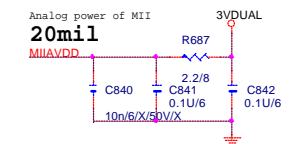
GIGABYTE		
SIS961A(HP ZIP,PCI,IDE)		
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SIS 961 A1/A2 , 961B, 962

共用



If MII interface don't use, Input pin tie to GND. Output pin is NC.



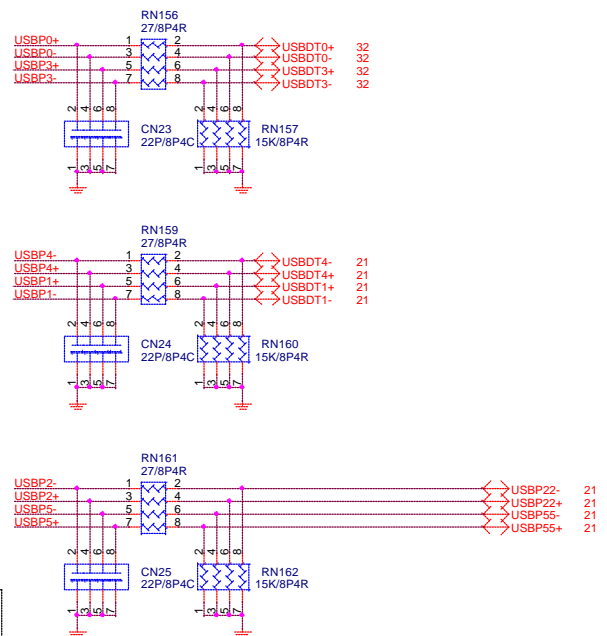
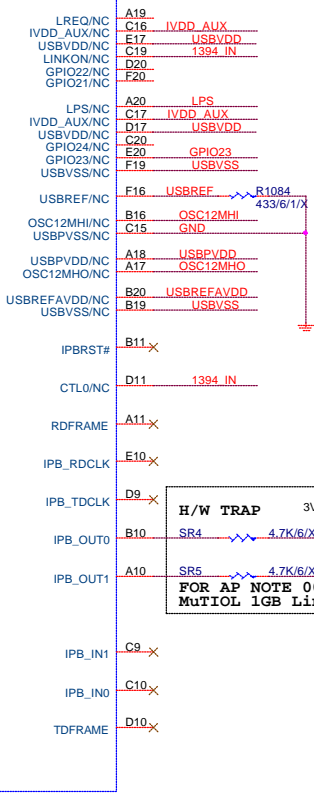
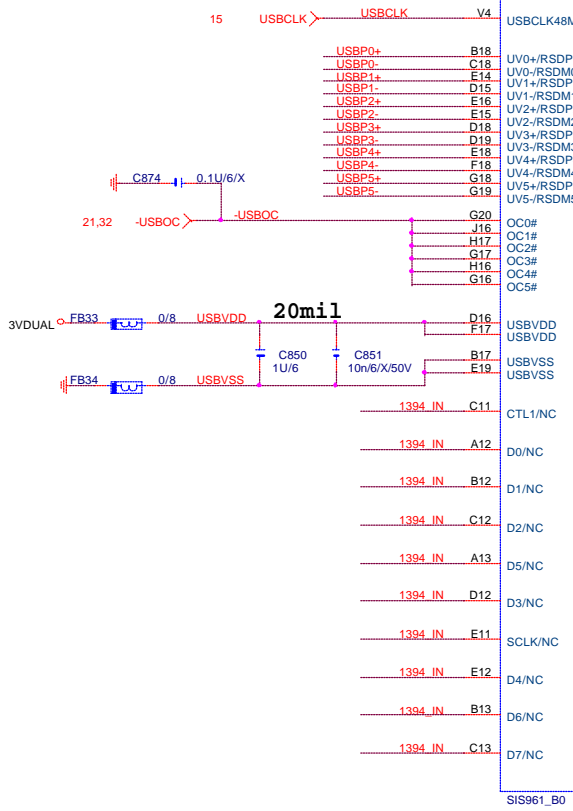
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Title SIS961A(CPU,LPC,RTC,AC97,GPIO,ACPI,KBC)			
Size Custom	Document Number GA-8SR533	Rev 2.0	
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SIS 961 A1/A2 , 961B, 962

共用

961A-3

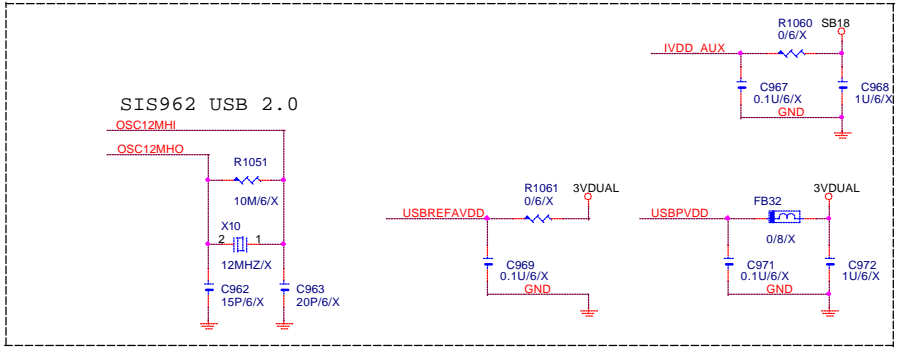
USB



H/W TRAP
FOR AP NOTE 003 SiS
MuTIOL LGB Link

FOR SIS962 USB2.0
RN156, RN159, RN161=0/8P4R
CN23, CN24, CN25=N/A
RN157, RN160, RN162=N/A

FOR SIS961 USB1.1
RN156, RN159, RN161=27/8P4R
CN23, CN24, CN25=22P
RN157, RN160, RN162=15K



GPIO23 R1156 4.7K/6/X 3VDUAL
R1157 4.7K/6

All of 1394 pin:
Output pin(LPS, LREQ) can be open.
All input pin connect together
and pull-down to gnd.

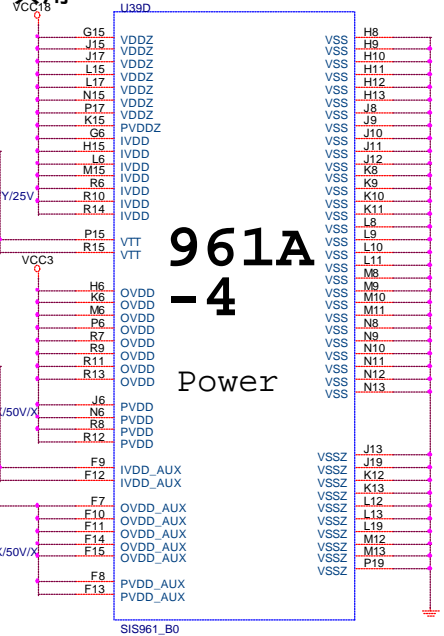
LPS R1154 4.7K/6/X
1394 IN R1064 4.7K/6

For SIS961B, 962

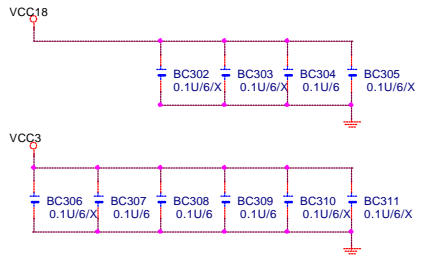
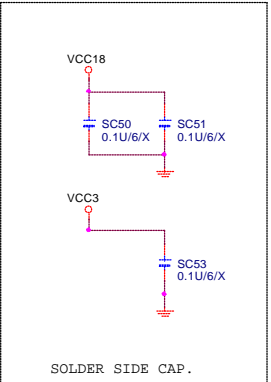
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SIS961A(USB)		
Title	SIS961A(USB)	
Size	Document Number	Rev
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SIS 961 A1/A2 , 961B, 962

共用
VCC18

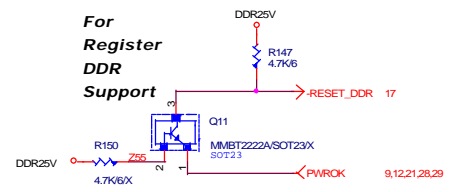
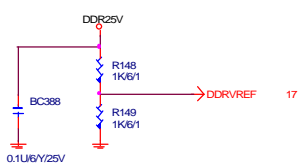
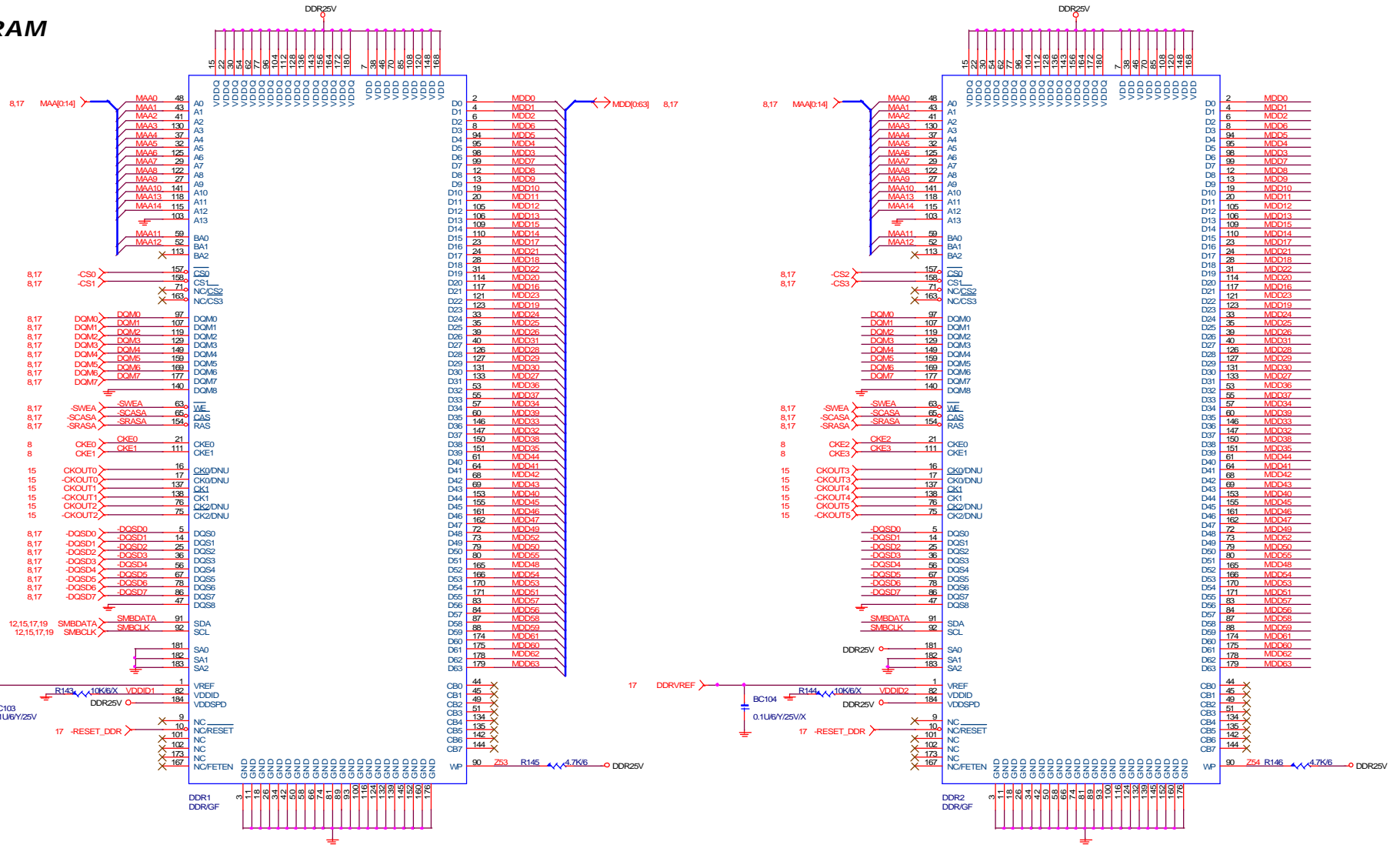


961A
-4
Power



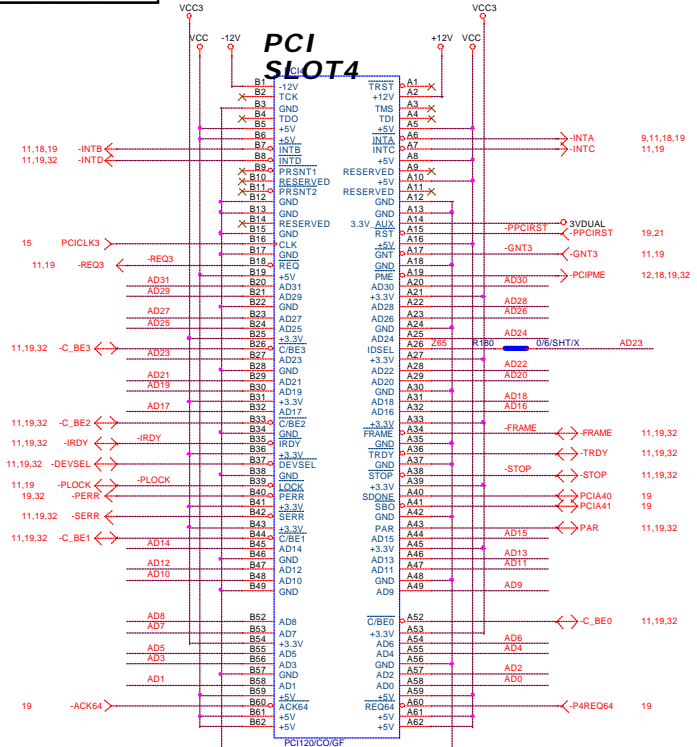
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Title SIS961A(PWR)		
Size Custom	Document Number GA-8SR533	Rev 2.0
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DDR SDRAM 1,2

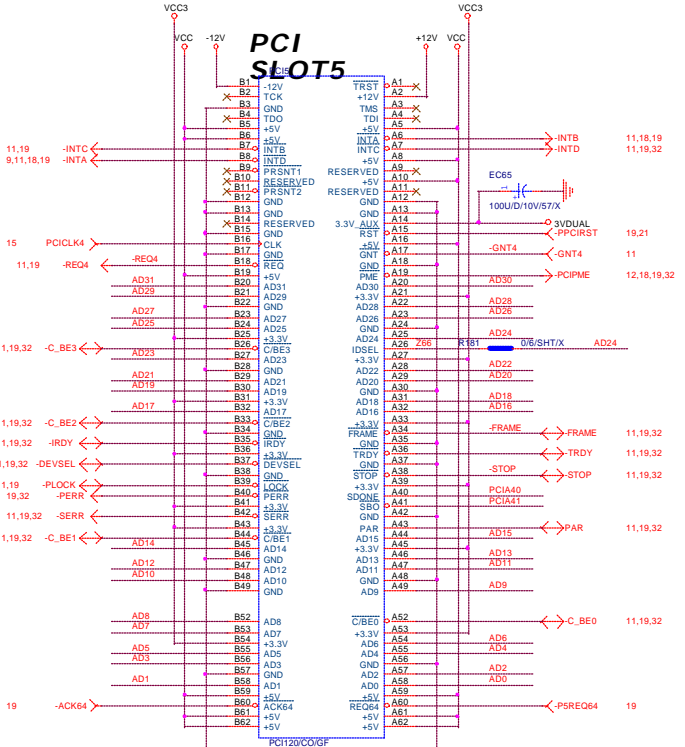


GIGABYTE		
DDR UNBUFFERED 1,2		
Title	Document Number	Rev
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PCI SLOT 4,5,6



IDSEL(A23)
(A)

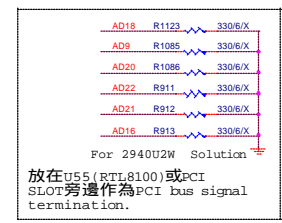


IDSEL(A24)
(B)

-PPCIRST
Close PCI Slot5
C44
100pF/N50V/X

-PCIRST PCIRST 9,11,21,22,32

PCI的走線要盡量 避免走"Γ"型。



放在U55(RTL8100)或PCI SLOT旁邊作為PCI bus signal termination.

	INTA#	IDSEL	REQX-
PCI1	BCDA	AD20	REQ0
PCI2	CDAB	AD21	REQ1
PCI3	DABC	AD22	REQ2
PCI4	ABCD	AD23	REQ3
PCI5	BCDA	AD24	REQ4
RTL8100	D	AD26	REQ5

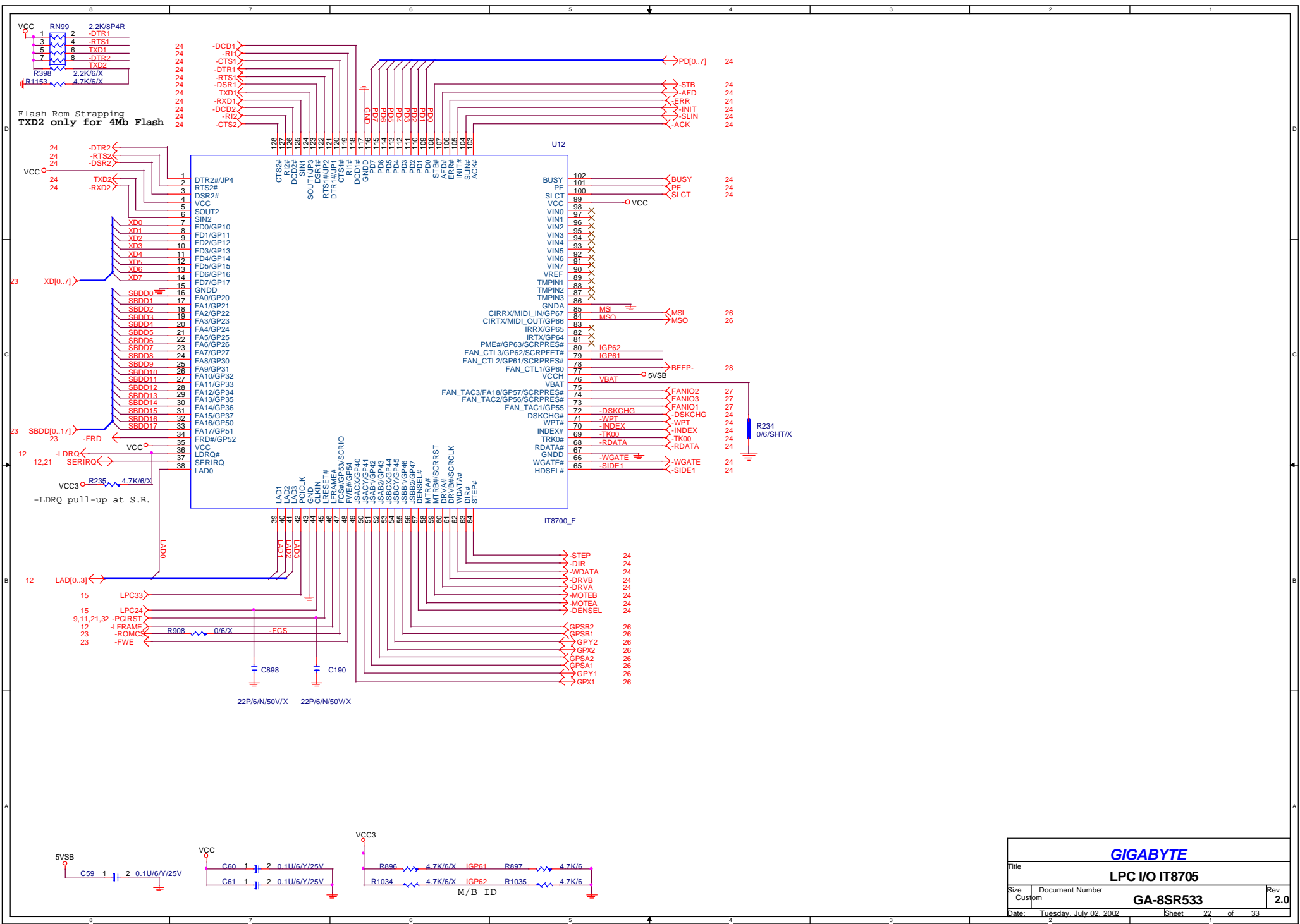
GIGABYTE

File: **PCI SLOT 4,5**

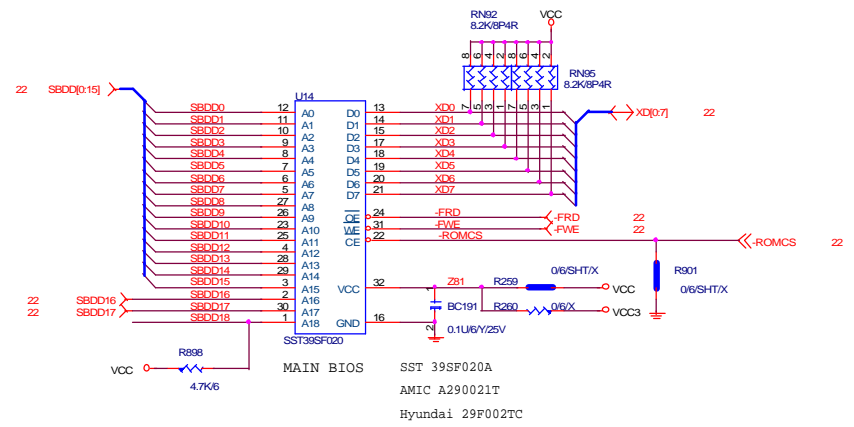
Size: Document Number **GA-8SR533** Rev **2.0**

Custom: **GA-8SR533**

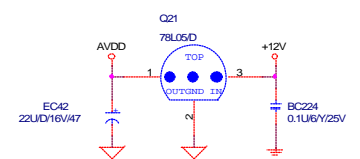
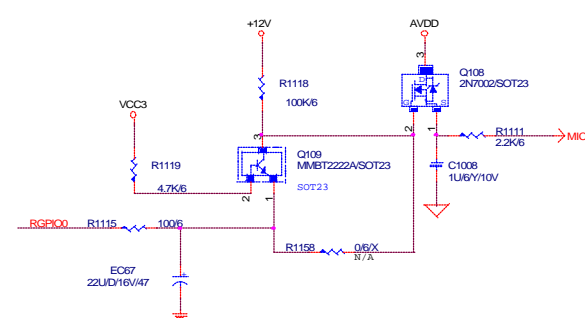
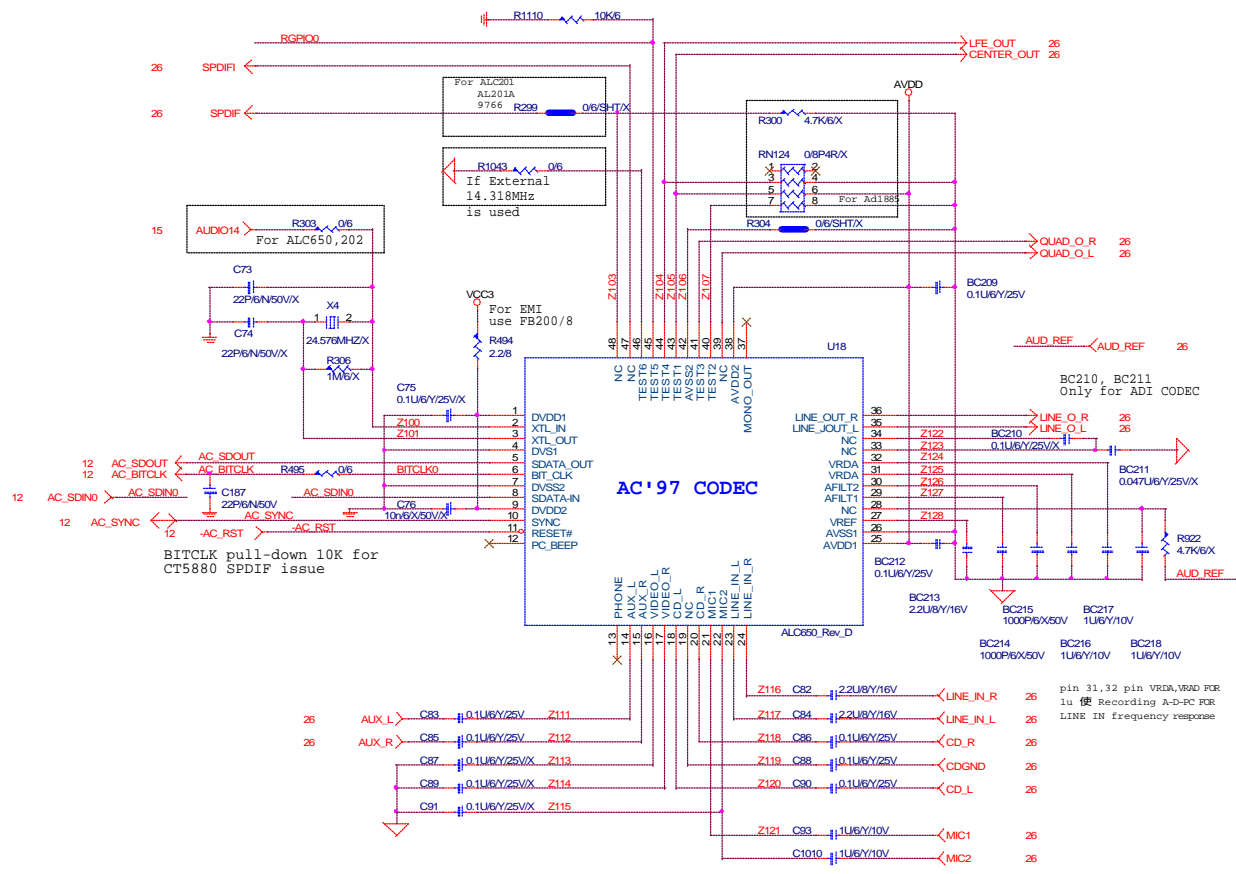
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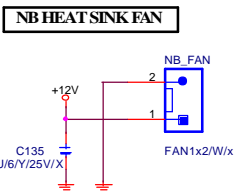
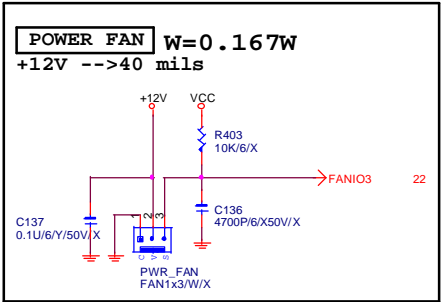
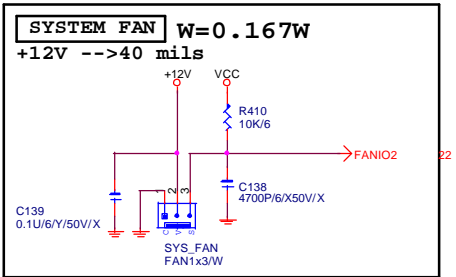
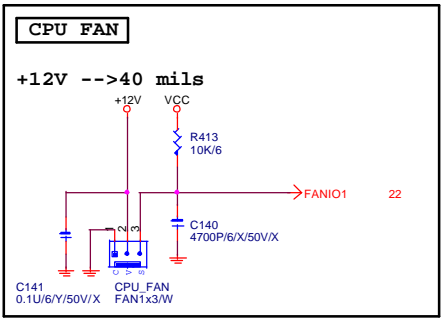
GIGABYTE		
Title		
LPC I/O IT8705		
Size	Document Number	Rev
Custom	GA-8SR533	2.0
Date:	Tuesday, July 02, 2002	Sheet 22 of 33



GIGABYTE		
Title		
Flash ROM		
Size	Document Number	Rev
Custom	GA-8SR533	2.0
Date:	Tuesday, July 02, 2002	Sheet 23 of 33

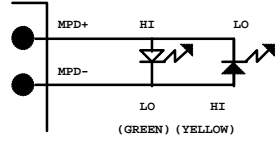


Title			GIGABYTE		
Size			AUDIO (CREATIVE CT5880)		
Custom	Document Number	GA-8SR533		Rev	2.0
Date:	Tuesday, May 02, 2002	Sheet	25	of	33



GIGABYTE			
FAN			
Size Custom	Document Number	GA-8SR533	Rev 2.0
Date:	Tuesday, July 02, 2002	Sheet 27	of 33

FRONT PANEL



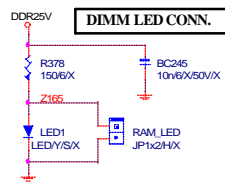
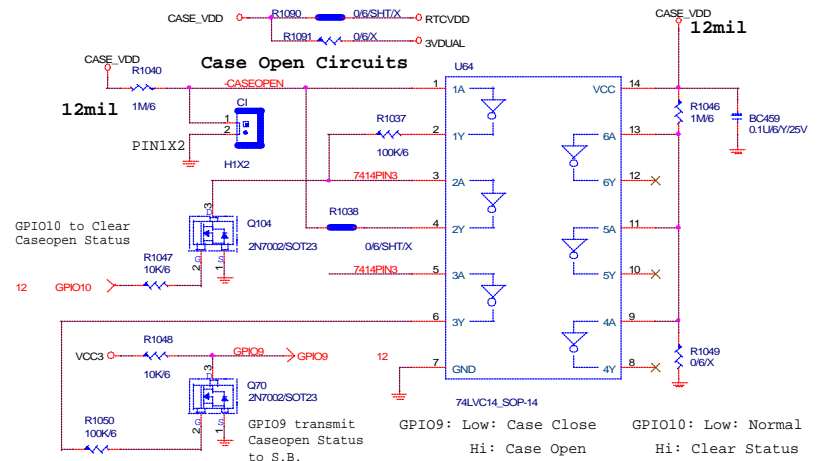
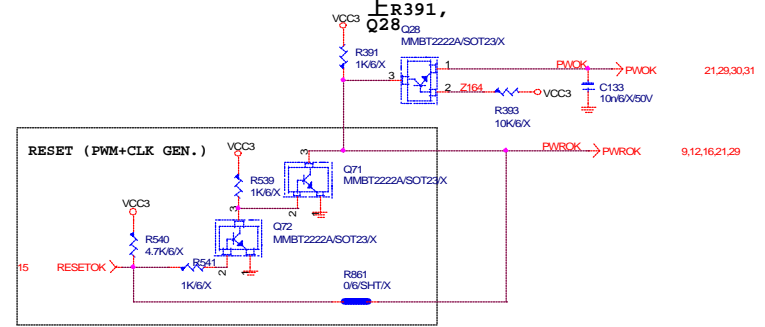
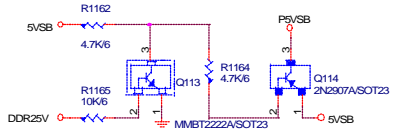
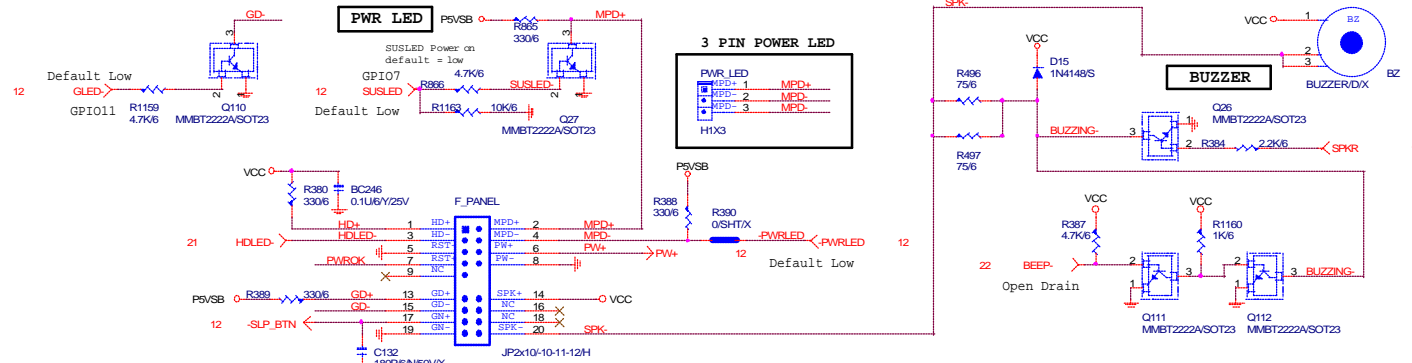
States for a single-color power LED

LED States	ACPI States	MPD+	MPD-
OFF	S1,S3,S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING

States for a dual-color power LED

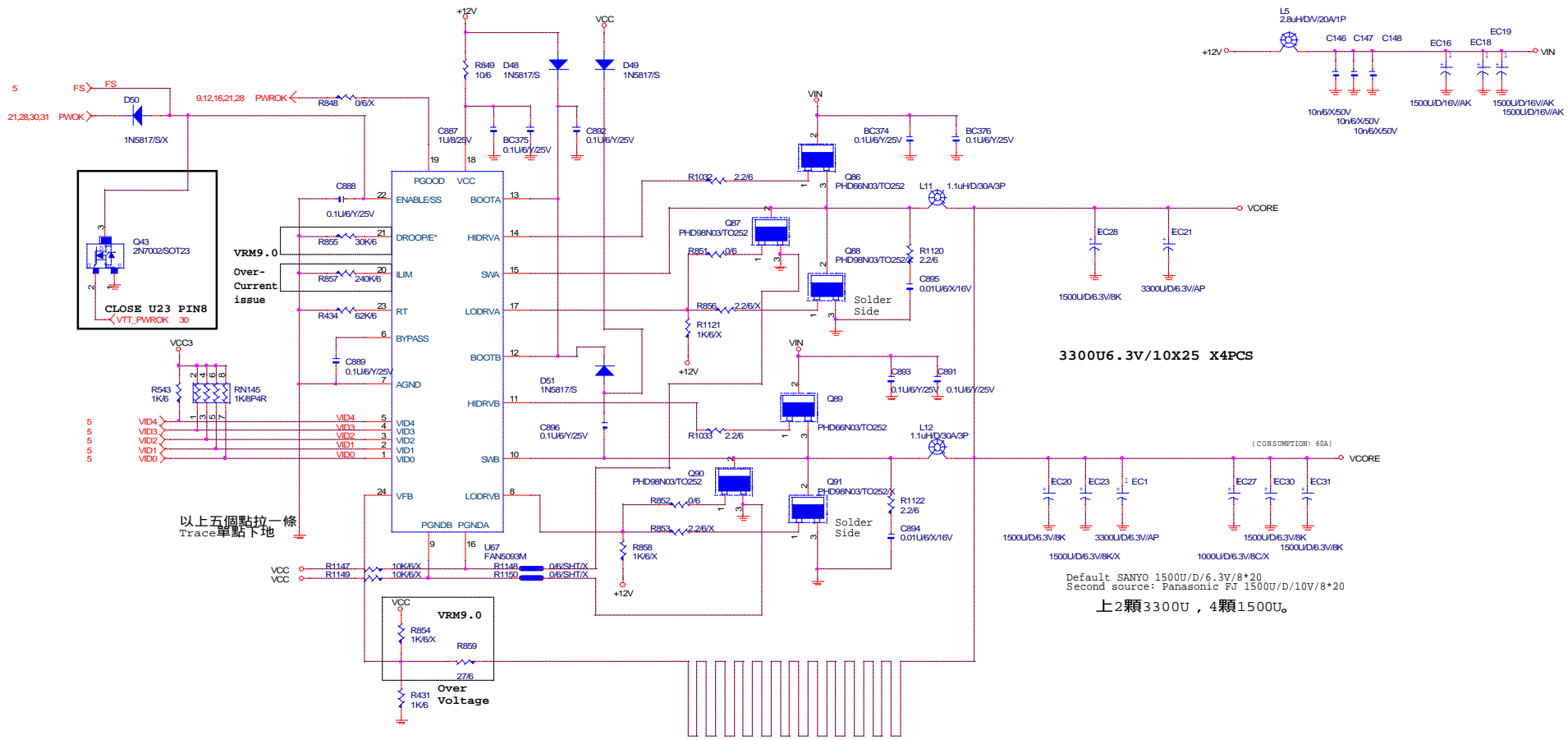
LED States	ACPI States	MPD+	MPD-
OFF	S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING
Steady Yellow	S1,S3	LO	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING

	S0	S1	S3	S5
GPIO11(GLED-)	0	1	1	0
GPIO7(SUSLED)	0	B	B	0
ACPILED(Pin A15)	0	0	0	1



74LVC14:
10TC1-140014-01
10TC1-120014-01
10TC1-120014-02

GIGABYTE		
PANEL, STR LED		
Title		
Size	Document Number	Rev
Custom	GA-8SR533	2.0
Date	Tuesday, May 02, 2002	Sheet 28 of 33

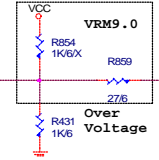
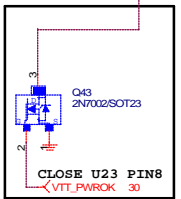


3300U6.3V/10X25 X4PCS

(CONSUMPTION: 60A)

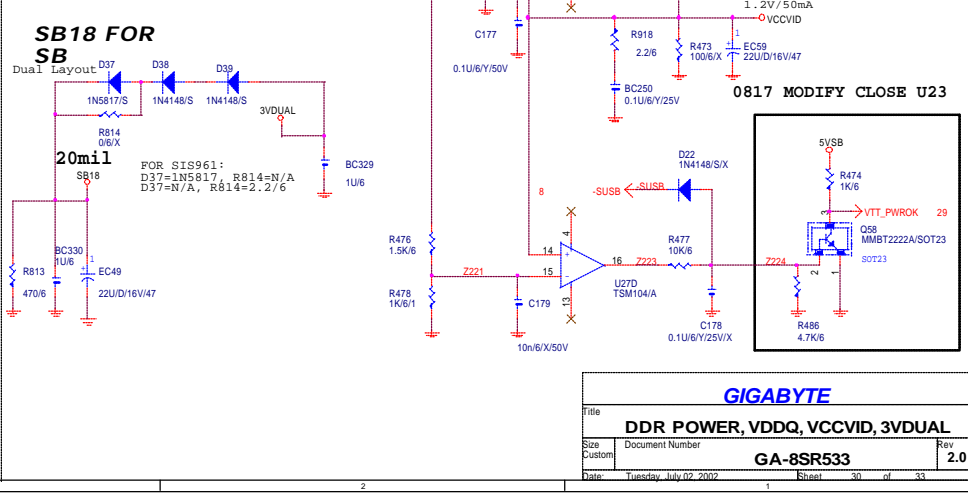
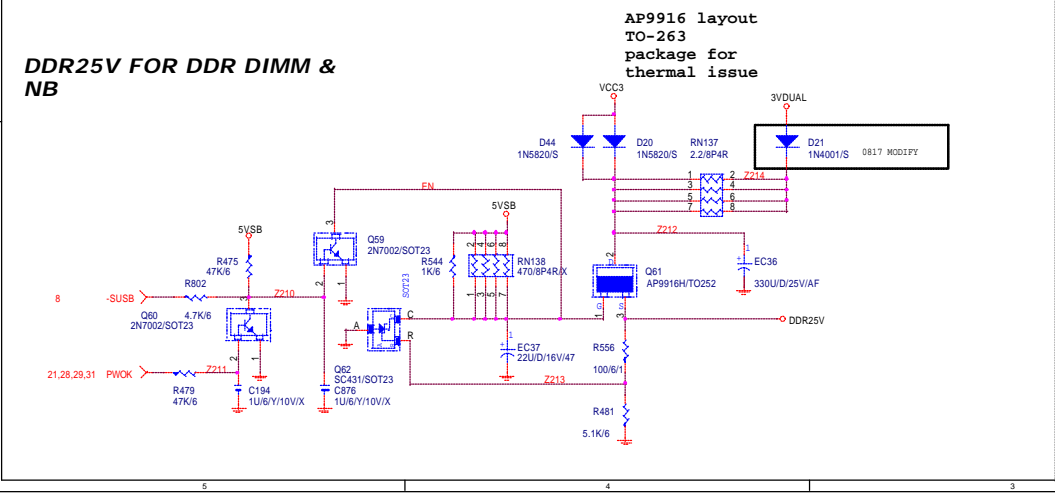
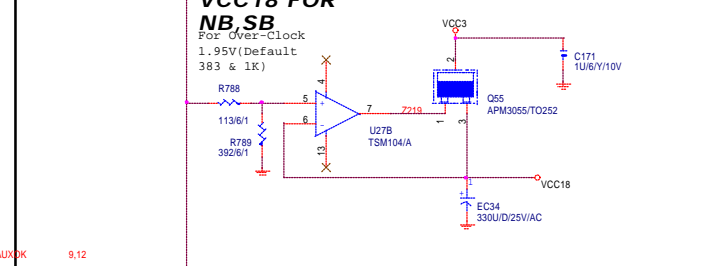
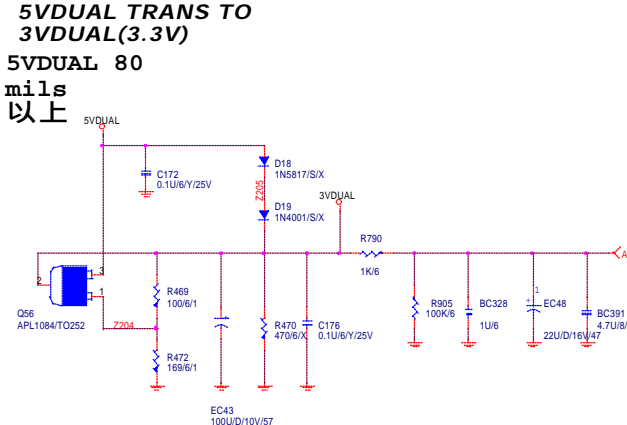
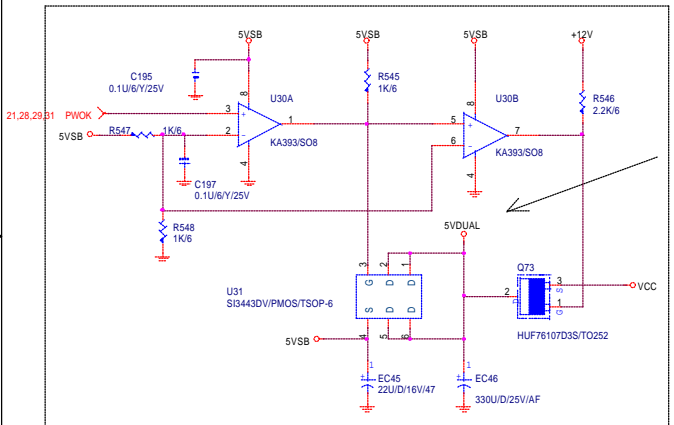
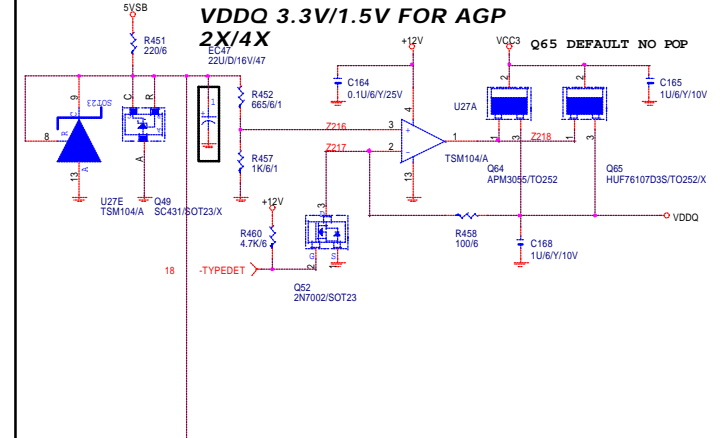
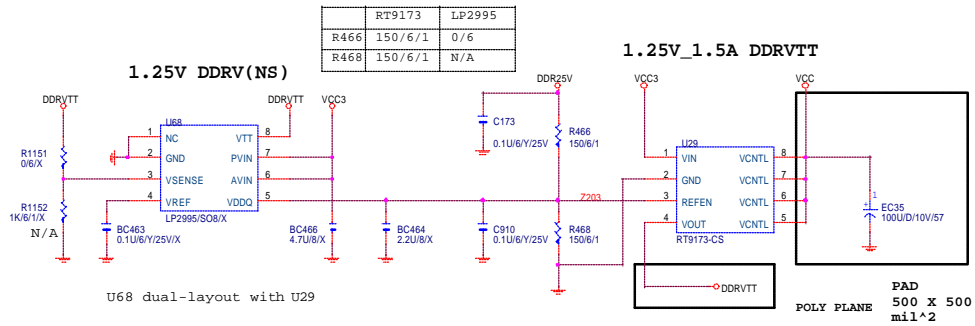
Default SANYO 1500U/D/6.3V/8*20
 Second source: Panasonic FJ 1500U/D/10V/8*20
 上2顆3300U, 4顆1500U.

以上五個點拉一條
 Trace單點下地



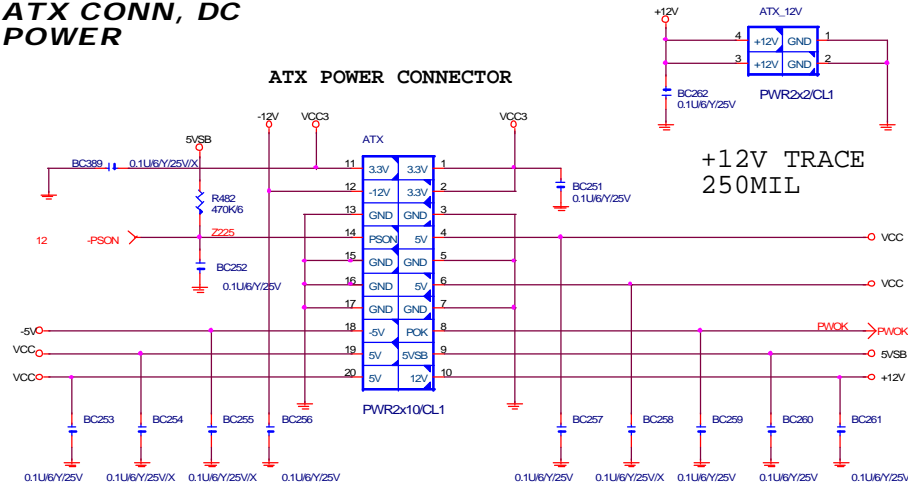
GIGABYTE		
Title VCORE (PWM FAN5093M)		
Size Custom	Document Number GA-8SR533	Rev 0.2
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1.25V DDRVTT LINEAR SOLUTION



ATX CONN, DC POWER

ATX POWER CONNECTOR



21,28,29,30

8SRXL South Bridge GPIO LIST			
ITEM	DESCRIPTION	STATUS	Default
GP00	Non Use		Hi
GP01	Non Use		Hi
GP04	Non Use		Hi
GP02	Non Use		Hi
GP03	Green Button	Hi:Normal, Lo:Into Green mode	Hi
GPIO5	REQ5		
GPIO6	GNT5		
GP07	Non Use		Hi
GP011	Non Use		Hi
GPI8	Wake On Ring	Hi:Normal, Lo:Ring Power On	Hi
GPI9	Case Open	Hi:Case Open, Lo:Normal	Lo
GPI10	Clear Caseopen status	Hi:Clear Caseopen Status, Lo:Normal	Lo
GPI13	Non Use		Hi
GP012	Non Use		Hi
GPI14	Primary Down	Lo:CODEC Only	Lo
GPIO15	KB Data		Hi
GPIO16	KB Clk		Hi
GPIO17	MS Data		Hi
GPIO18	MS Clk		Hi

States for a single-color power LED

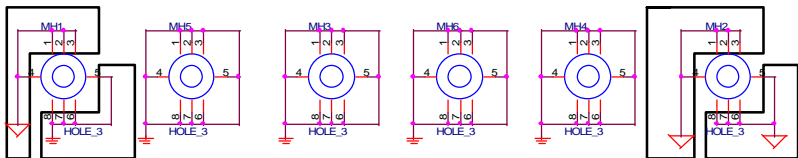
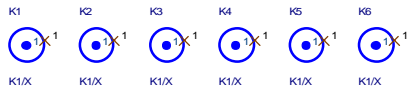
LED States	ACPI States	MPD+	MPD-	BIOS	
				GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING

States for a dual-color power LED

LED States	ACPI States	MPD+	MPD-	BIOS	
				GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING
Steady Yellow	S1,S3	LO	HI	HI	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING	HI	BLINKING

States for green LED

LED States	ACPI States	GLLED-	BIOS
			GPIO11
ON	S1,S3	HI	HI
OFF	S0,S5	LO	LO



EMI (VCC.GND CUT HOLE PLANE)

EMI (VCC.LGND CUT HOLE PLANE)

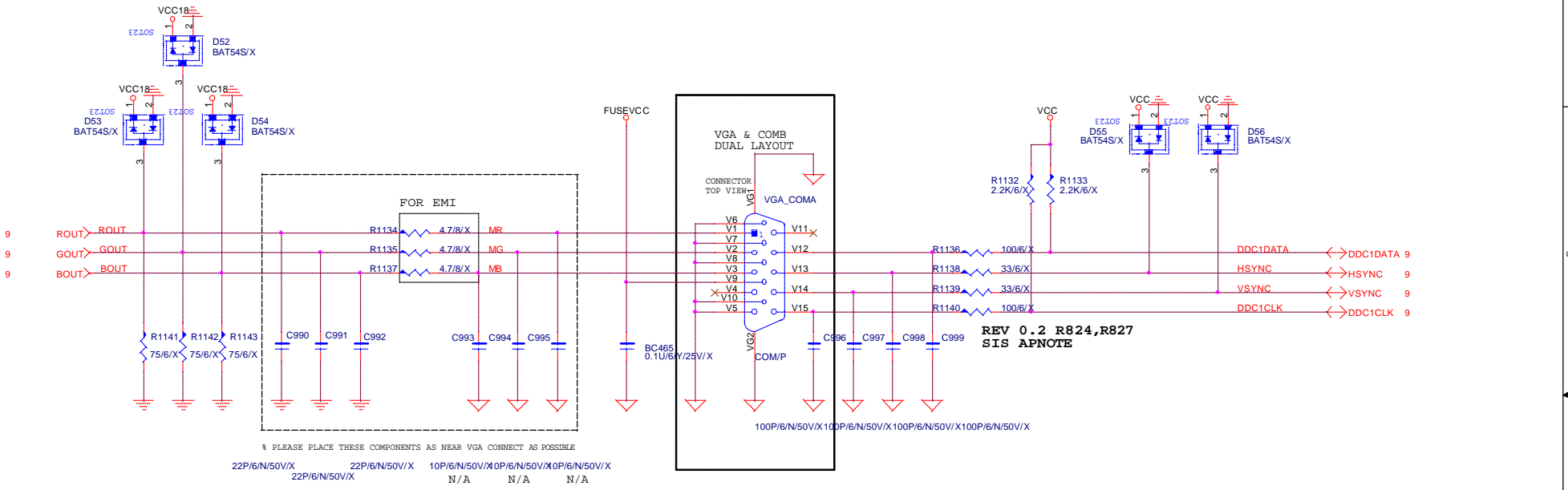
BIOS REQUEST

SINGLE	DUAL	INTEL LED DEFINED				GIGABYTE LED DEFINED				SINGLE	DUAL
		GPIO7	ACPILED	GPIO11		GPIO7	ACPILED	GPIO11			
GREEN	GREEN	S0	LO	LO	LO	S0	LO	LO	LO	GREEN	GREEN
OFF	YELLOW	S1	HI	HI	HI	S1	LO	BLINKING	HI	(BLINK)	(BLINK)
OFF	YELLOW	S3	HI	HI	HI	S3	HI	HI	HI	OFF	YELLOW
OFF	OFF	S4/S5	LO	HI/NC	LO	S4/S5	LO	HI/NC	LO	OFF	OFF

GIGABYTE

Title			ATX, GPIO LIST		
Size	Document Number	Rev			
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Date	Tuesday, May 02, 2002	Sheet	31	of 33	

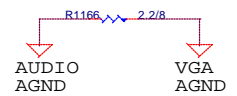
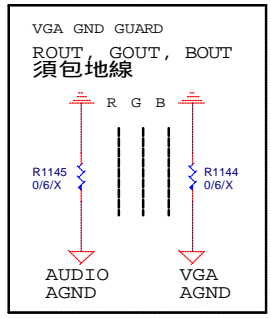
VGA CONNECTOR 1



REV 0.2 R824,R827
SIS APNOTE

PLEASE PLACE THESE COMPONENTS AS NEAR VGA CONNECT AS POSSIBLE

22P/6/N/50V/X	22P/6/N/50V/X	10P/6/N/50V/X	10P/6/N/50V/X	10P/6/N/50V/X	10P/6/N/50V/X
22P/6/N/50V/X		N/A	N/A	N/A	



R1166: For Recording Noise issue
For ST9721: 2.2/8 (EMI Recommend FB30)
For ALC650: 0/8

GIGABYTE		
VGA CONNECTOR		
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