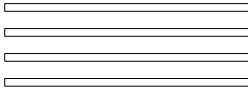


8SIMLH-P Schematics

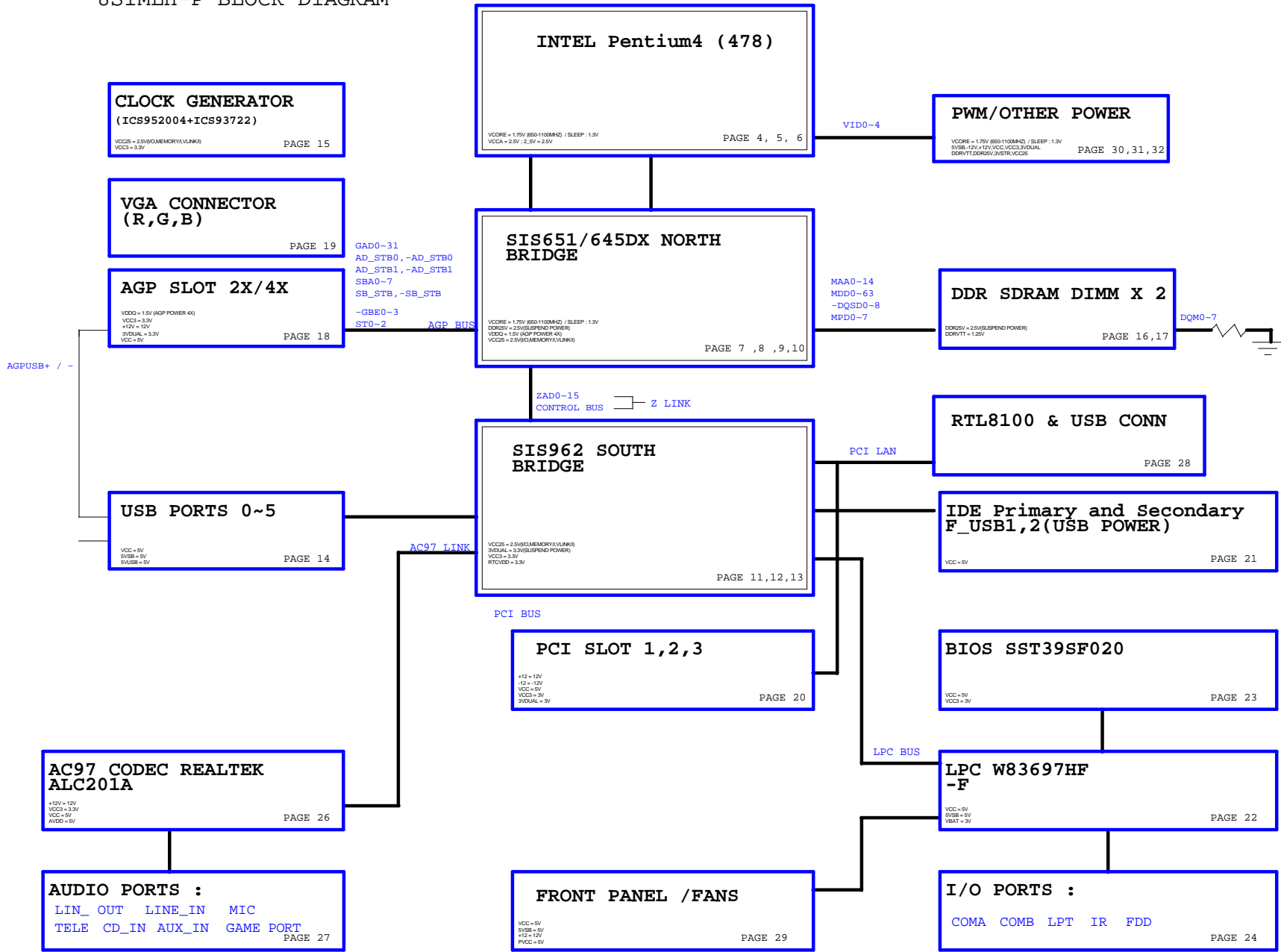
Revision 4.0

Dte: 92/09/18

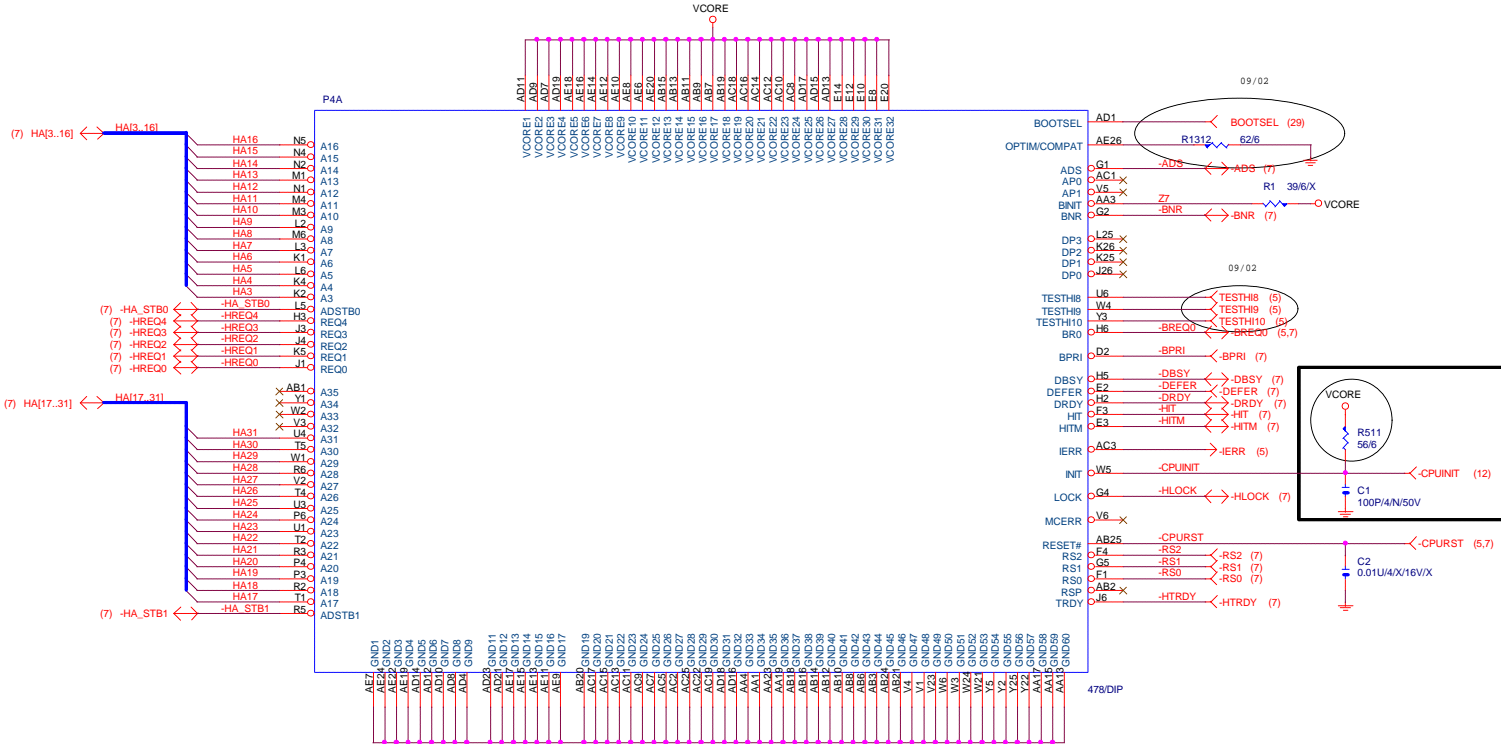
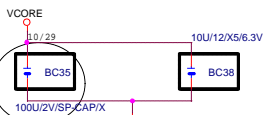
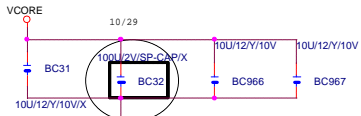
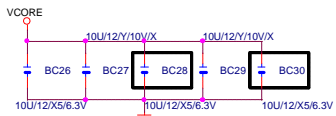
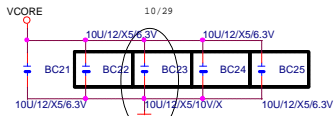
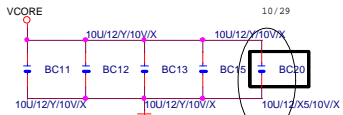
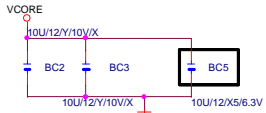
SHEET	TITLE
1	COVER SHEET
2	BOM & PCB MODIFY HISTORY
3	BLOCK DIAGRAM
4,5,6	INTEL CPU_WMT_478
7-10	SIS651/645DX (NORTH BRIDGE) HOST; DDR; AGP, HYPER ZIP
11-14	962 (SOUTH BRIDGE)
15	CKG(ICS952004) + CKBF (ICS93722)
16,17	DDR SDRAM DIMMS 1,2 & DDR TERMINATION
18	AGP SLOT
19	VGA Connector
20	PCI SLOT 1-3
21	IDE, USB
22	Winbond W83697HF
23	BIOS
24	COM, PRT, FDD, KB/MS, IR
25	CNR SLOT
26	AUDIO AC 97 CODEC
27	AUDIO JACK, GAME PORT
28	RTL8100B & USB CONNECTOR
29	PANEL, STR LED, FANS, CPU GN
30	VCORE PHASE PWM HIP 6301 + 6601
31	ALL POWER CIRCUIT
32	ATX & ATX12V CONN
33	GPIO Connection
34	TEST POINT

		COMPONENT SIDE (1 oz. Copper) GND SIDE (1 oz. Copper) VCC SIDE (1 oz. Copper) SOLDER SIDE (1 oz. Copper)
GIGABYTE		
Title: COVER SHEET		
Size: Custom	Document Number: GA-8SIMLH-P	Rev: 4.0
Date: 星期三, 十二月 03, 2003	Sheet 1 of 32	

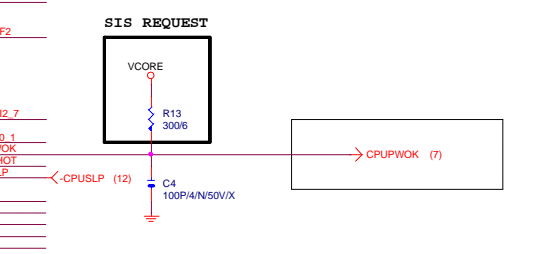
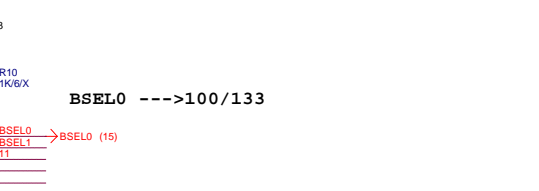
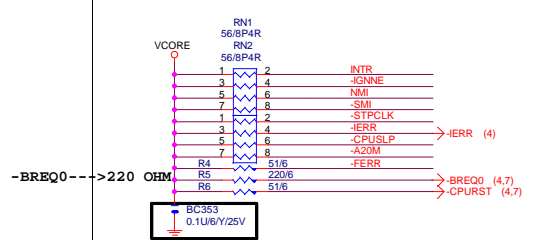
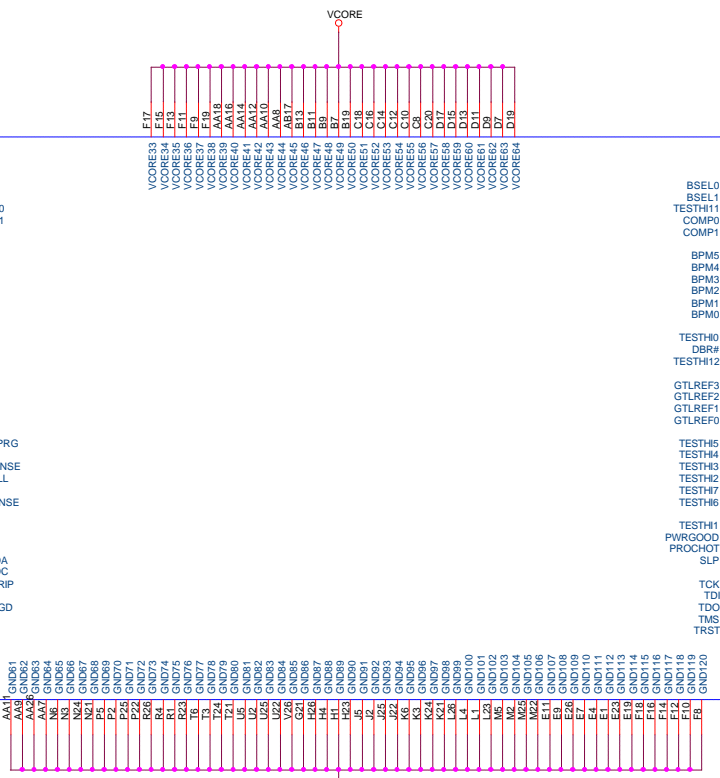
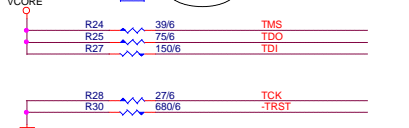
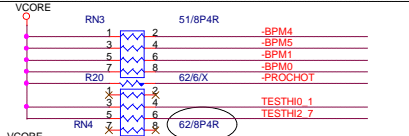
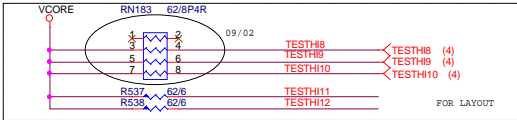
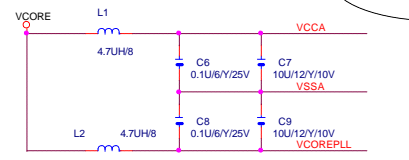
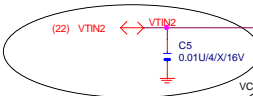
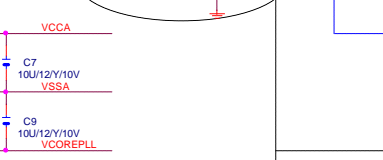
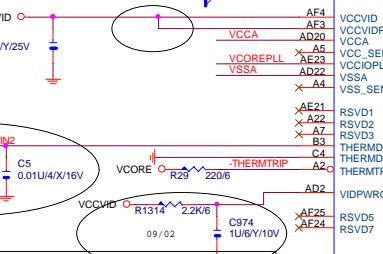
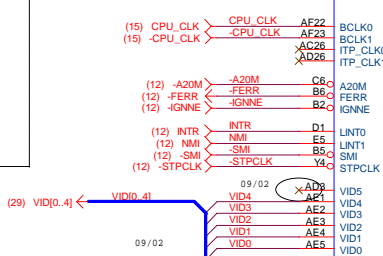
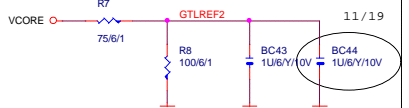
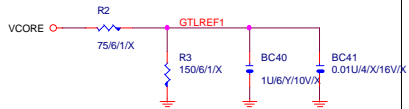
8SIMLH-P BLOCK DIAGRAM



(X5R) X11 1206(10U) NOTE:GIGA



GIGABYTE		
WILLIAMATE 478A		
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Size		WILLIAMATE 478B	
Custom	Document Number	GA-8SIMLHP	
Date:	Rev	Rev	4.0
日期: 2003.03.12	Sheet	5	of 32

D

D

C

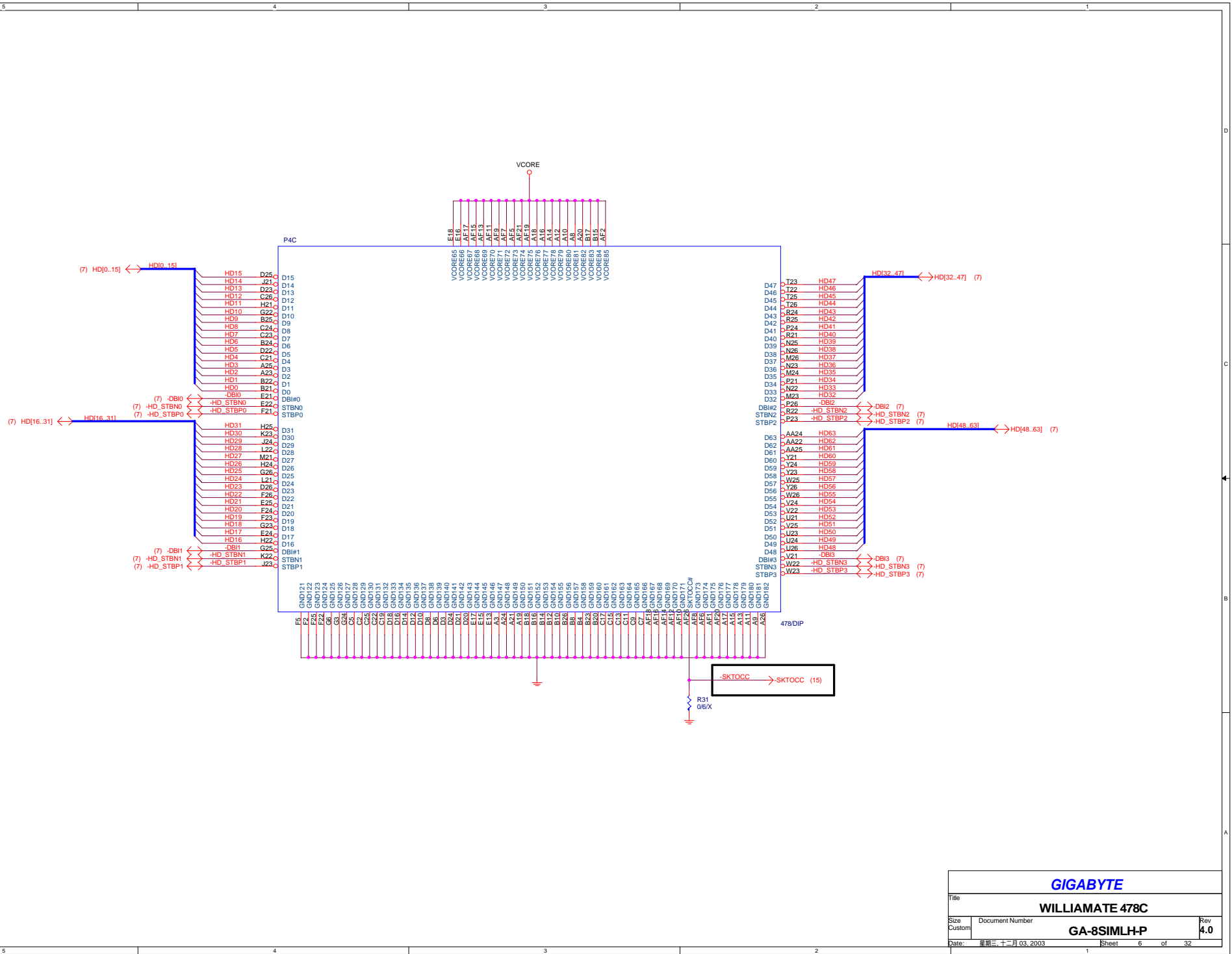
C

B

B

A

A



GIGABYTE			
WILLIAMATE 478C			
Title	Document Number		
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-DBI0..31 → DBI[0..31] (6)
 HDI0..631 → HD[0..631] (6)
 HAI3..311 → HA[3..311] (4)
 GD10..311 → GD[0..311] (18)
 SBA10..71 → SBA[0..71] (18)
 STI0..21 → STI[0..21] (18)

(15) HCLK → HCLK A126 CPUCCLK
 (15) -HCLK → -HCLK AH28 CPUCCLK#
 (4) -HLOCK → -HLOCK U24 HLOCK#
 (4) -DEFER → -DEFER U26 DEFER#
 (4) -HTRDY → -HTRDY V26 HTRDY#
 (4.5) -CPURST → -CPURST C20 CPURST#
 (5) CPUFWOK → CPUFWOK D19 CPUFWOK#
 (4) -BPR1 → -BPR1 T27 BPR#
 (4.5) -BREQ0 → -BREQ0 U25 BREQ0#
 (4) -RS2 → -RS2 T24 RS#2
 (4) -RS1 → -RS1 T26 RS#1
 (4) -RS0 → -RS0 U29 RS#0
 (4) -ADS → -ADS V28 ADS#
 (4) -HITM → -HITM T28 HITM#
 (4) -HIT → -HIT U28 HIT#
 (4) -DRDY → -DRDY W26 DRDY#
 (4) -DBSY → -DBSY V24 DBSY#
 (4) -BNR → -BNR V27 BNR#
 (4) -HREQ4 → -HREQ4 W28 HREQ#4
 (4) -HREQ3 → -HREQ3 W29 HREQ#3
 (4) -HREQ2 → -HREQ2 W24 HREQ#2
 (4) -HREQ1 → -HREQ1 W25 HREQ#1
 (4) -HREQ0 → -HREQ0 Y27 HREQ#0
 (4) -HA_STB1 → -HA_STB1 AD24 HASTB#1
 (4) -HA_STB0 → -HA_STB0 AA24 HASTB#0

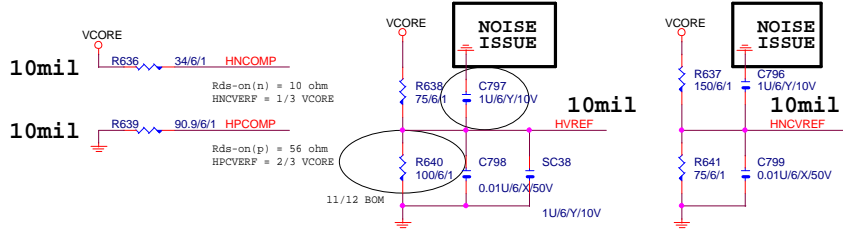
HA31 AF26 HA#31
 HA30 AE25 HA#30
 HA29 AH28 HA#29
 HA28 AD26 HA#28
 HA27 AG29 HA#27
 HA26 AE26 HA#26
 HA25 AF28 HA#25
 HA24 AC24 HA#24
 HA23 AG28 HA#23
 HA22 AE29 HA#22
 HA21 AD28 HA#21
 HA20 AC25 HA#20
 HA19 AD27 HA#19
 HA18 AE26 HA#18
 HA17 AF27 HA#17
 HA16 AB24 HA#16
 HA15 AB26 HA#15
 HA14 AC28 HA#14
 HA13 AC26 HA#13
 HA12 AC29 HA#12
 HA11 AA26 HA#11
 HA10 AB28 HA#10
 HA9 AB27 HA#9
 HA8 AA25 HA#8
 HA7 AA29 HA#7
 HA6 AA28 HA#6
 HA5 Y26 HA#5
 HA4 Y24 HA#4
 HA3 Y28 HA#3

HOST

651/645DX-1

AGP

HDI#63 DBI#63
 HDI#62 DBI#62
 HDI#61 DBI#61
 HDI#60 DBI#60
 HDI#59 DBI#59
 HDI#58 DBI#58
 HDI#57 DBI#57
 HDI#56 DBI#56
 HDI#55 DBI#55
 HDI#54 DBI#54
 HDI#53 DBI#53
 HDI#52 DBI#52
 HDI#51 DBI#51
 HDI#50 DBI#50
 HDI#49 DBI#49
 HDI#48 DBI#48
 HDI#47 DBI#47
 HDI#46 DBI#46
 HDI#45 DBI#45
 HDI#44 DBI#44
 HDI#43 DBI#43
 HDI#42 DBI#42
 HDI#41 DBI#41
 HDI#40 DBI#40
 HDI#39 DBI#39
 HDI#38 DBI#38
 HDI#37 DBI#37
 HDI#36 DBI#36
 HDI#35 DBI#35
 HDI#34 DBI#34
 HDI#33 DBI#33
 HDI#32 DBI#32
 HDI#31 DBI#31
 HDI#30 DBI#30
 HDI#29 DBI#29
 HDI#28 DBI#28
 HDI#27 DBI#27
 HDI#26 DBI#26
 HDI#25 DBI#25
 HDI#24 DBI#24
 HDI#23 DBI#23
 HDI#22 DBI#22
 HDI#21 DBI#21
 HDI#20 DBI#20
 HDI#19 DBI#19
 HDI#18 DBI#18
 HDI#17 DBI#17
 HDI#16 DBI#16
 HDI#15 DBI#15
 HDI#14 DBI#14
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 HDI#12 DBI#12
 HDI#11 DBI#11
 HDI#10 DBI#10
 HDI#9 DBI#9
 HDI#8 DBI#8
 HDI#7 DBI#7
 HDI#6 DBI#6
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 HDI#2 DBI#2
 HDI#1 DBI#1
 HDI#0 DBI#0

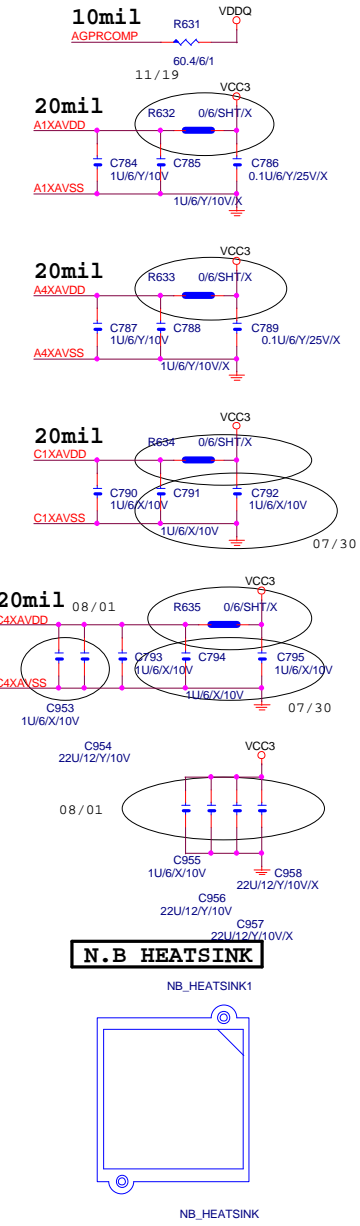


VREF C-CAP PULL-UP MEASURE NOISE WORST.

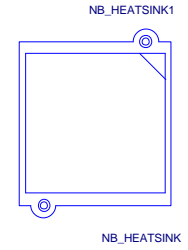
U38A

AC/BE#3 CF → -GBE3 → GBE3 (18)
 AC/BE#2 CH4 → -GBE2 → GBE2 (18)
 AC/BE#1 CK5 → -GBE0 → GBE0 (18)
 AREQ# C9 → -GREQ → GREQ (18)
 AGNT# CA6 → -GGNT → GGNT (18)
 AFRAME# CG2 → -GFRAME → GFRAME (18)
 AIRDY# CG1 → -GIRDY → GIRDY (18)
 ATRDY# CG3 → -GTRDY → GTRDY (18)
 ADEVSEL# CH4 → -GDEVSEL → GDEVSEL (18)
 ASERR# CH5 → -GSERR → GSERR (18)
 ASTOP# CH1 → -GSTOP → GSTOP (18)
 APAR H3 → GPAR → GPAR (18)
 RBF# CF8 → -RBF → RBF (18)
 WBF# CD9 → -WBF → WBF (18)
 PIPE# C10 → -PIPE → PIPE (18)
 AGP8XDET D10 → TP8
 ADBH B3 → TP9
 ADBL C4 → TP10
 SB_STB B5 → SB_STB → SB_STB (18)
 SB_STB# CA4 → -SB_STB → -SB_STB (18)
 AD_STB0 K1 → AD_STB0 → AD_STB0 (18)
 AD_STB# L1 → -AD_STB0 → -AD_STB0 (18)
 AD_STB1 C1 → AD_STB1 → AD_STB1 (18)
 AD_STB# D1 → -AD_STB1 → -AD_STB1 (18)
 AGPCLK B10 → GCLK_NB → GCLK_NB (15)
 AGPRCOMP M1 → AGPRCOMP
 A1XAVDD B9 → A1XAVDD
 A1XAVSS A9 → A1XAVSS
 A4XAVDD B8 → A4XAVDD
 A4XAVSS A8 → A4XAVSS
 AGPVREF M3 → AGPVREF → AGPVREF (18)
 AGPVSSREF M2
 HDSTBN#3 F20 → -HD_STBN3 → -HD_STBN3 (6)
 HDSTBN#2 C23 → -HD_STBN2 → -HD_STBN2 (6)
 HDSTBN#1 K24 → -HD_STBN1 → -HD_STBN1 (6)
 HDSTBN#0 C24 → -HD_STBN0 → -HD_STBN0 (6)
 HDSTBP#3 F21 → -HD_STBP3 → -HD_STBP3 (6)
 HDSTBP#2 C24 → -HD_STBP2 → -HD_STBP2 (6)
 HDSTBP#1 L24 → -HD_STBP1 → -HD_STBP1 (6)
 HDSTBP#0 C25 → -HD_STBP0 → -HD_STBP0 (6)

SIS651/B0



N.B HEATSINK



GIGABYTE		
SIS651/645DX(HOST/AGP)		
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- MDDI0_631 ←→ MDDI[0:63] (16,17)
- DOMI0_71 → DOM[0..7] (16,17)
- MAAI0_141 → MAA[0..14] (16,17)
- CSI0_31 → CS[0..3] (16,17)
- CKEI0_51 → CKE[0..5] (16)
- DQSDI0_71 → -DQSD[0..7] (16,17)

DDR MD DAMPING

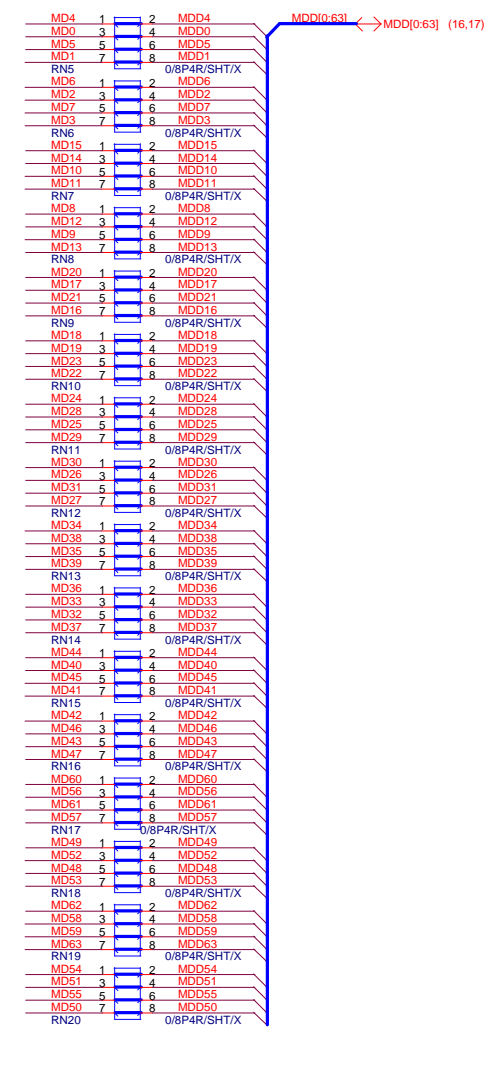
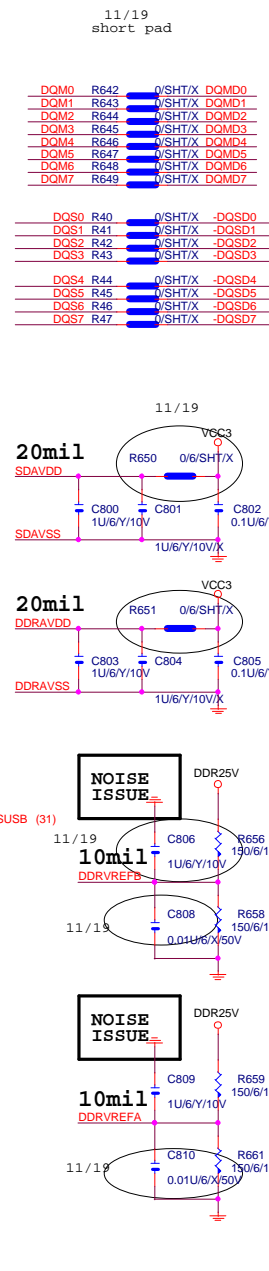
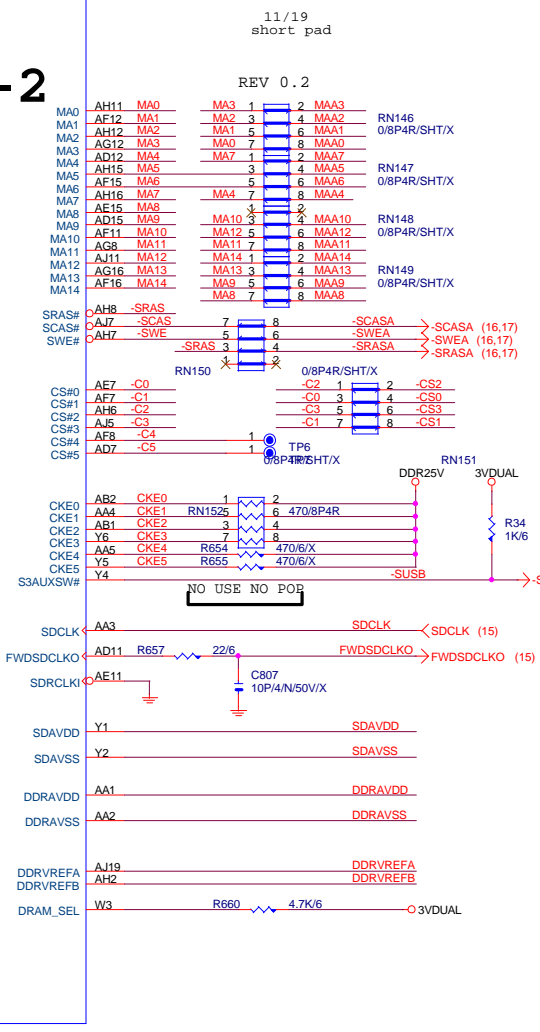
Near DIMM 1

MD0	AJ23	MD0
MD1	AG22	MD1
MD2	AH21	MD2
MD3	AJ21	MD3
MD4	AD23	MD4
MD5	AE23	MD5
MD6	AF22	MD6
MD7	AF21	MD7
DOMD0	AD22	MD7
DQS0	AH22	DOM0
MD8	AD21	MD8
MD9	AG20	MD9
MD10	AE19	MD10
MD11	AF18	MD11
MD12	AE21	MD12
MD13	AD20	MD13
MD14	AD19	MD14
MD15	AH19	MD15
DOMD1	AF20	MD15
DQS1	AH20	DOM1
MD16	AF18	MD16
MD17	AG18	MD17
MD18	AH17	MD18
MD19	AD16	MD19
MD20	AD18	MD19
MD21	AD17	MD20
MD22	AF17	MD21
MD23	AJ17	MD22
DOMD2	AJ17	MD23
DQS2	AH18	DOM2
MD24	AD14	MD24
MD25	AG14	MD25
MD26	AJ13	MD26
MD27	AE13	MD27
MD28	AJ15	MD27
MD29	AF14	MD29
MD30	AD13	MD30
MD31	AF13	MD31
DOMD3	AH13	MD31
DQS3	AH14	DOM3
MD32	AD10	MD32
MD33	AH10	MD33
MD34	AE9	MD34
MD35	AD8	MD35
MD36	AG10	MD36
MD37	AF10	MD37
MD38	AH9	MD38
MD39	AF9	MD39
DOMD4	AD9	MD39
DQS4	AJ9	DOM4
MD40	AH5	MD40
MD41	AG4	MD41
MD42	AE5	MD42
MD43	AH3	MD43
MD44	AG6	MD44
MD45	AF6	MD45
MD46	AF5	MD46
MD47	AF4	MD47
DOMD5	AH4	MD47
DQS5	AJ3	DOM5
MD48	AE4	MD48
MD49	AD6	MD49
MD50	AE5	MD50
MD51	AC5	MD51
MD52	AG2	MD52
MD53	AG1	MD53
MD54	AF3	MD54
MD55	AC6	MD55
DOMD6	AD4	MD55
DQS6	AF2	DOM6
MD56	AB6	MD56
MD57	AD3	MD57
MD58	AE6	MD58
MD59	AB3	MD59
MD60	AC4	MD60
MD61	AE1	MD61
MD62	AD2	MD62
MD63	AC1	MD63
DOMD7	AB4	MD63
DQS7	AC2	DOM7
		DQS7/CSB#7

651
645DX-2

U38B

SIS651/B0



VREF C-CAP PULL-UP MEASURE NOISE WORST.

GIGABYTE		
Title		
SIS651/645DX(DDR)		
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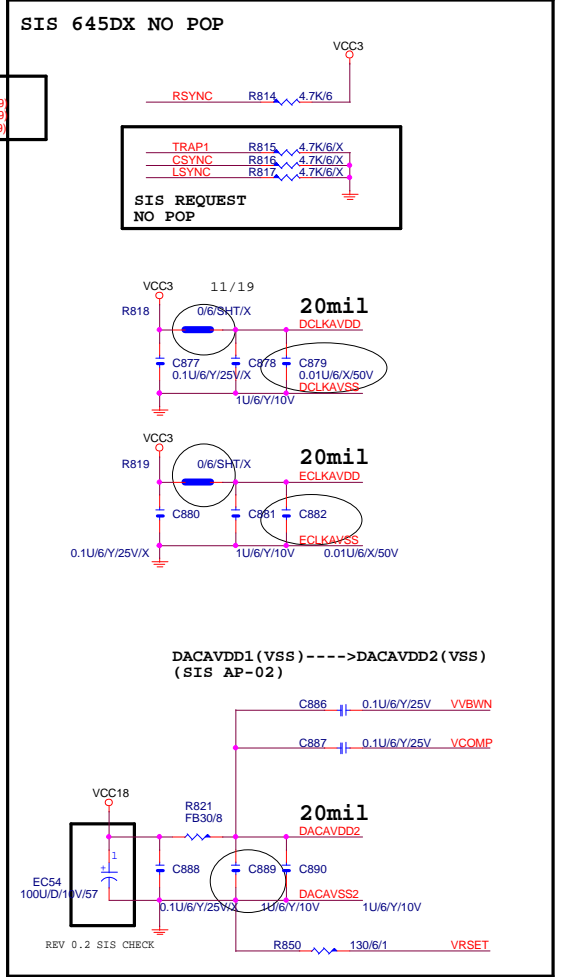
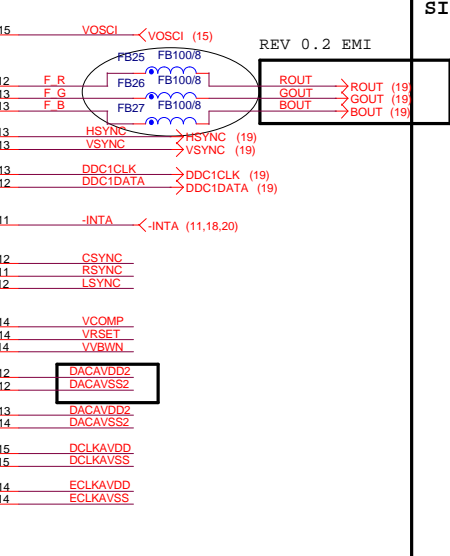
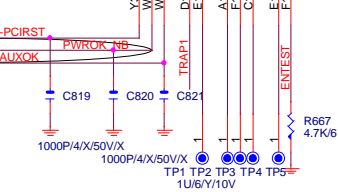
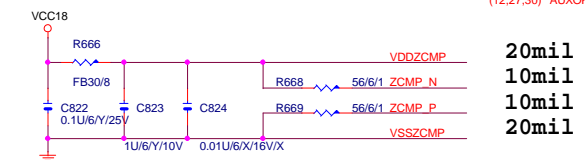
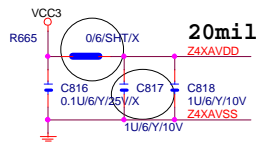
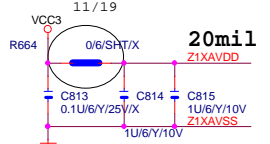
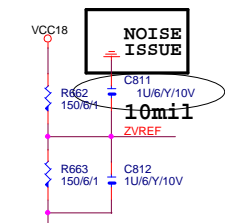
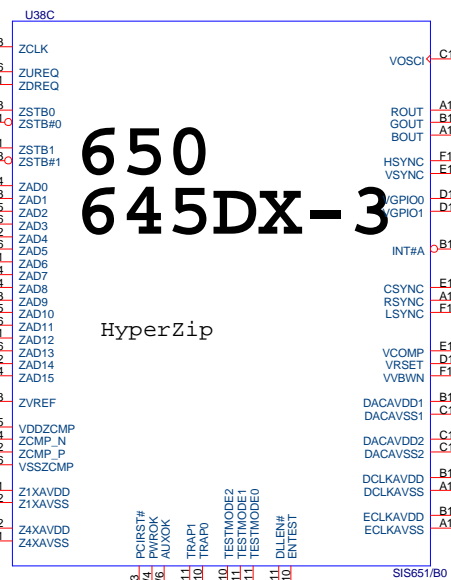
NOTE: This page is for universal PCB design(suitable for both 645 or 650)

NB Hardware Trap Table

	0	1	Default	embedded pull-low (30-50K Ohm)
DLEN#	enable PLL	disable PLL	0	yes
DRAM_SEL	SDR	DDR	1(DDR)	yes
TRAP0	normal	NB debug mode	0	yes
TRAP1	TV selection, NTSC/PAL(0/1)		0	
CSYNC	enable VB		0	
RSYNC	enable VGA interrupt		1	
LSYNC	enable panel link		0	

650 645DX-3

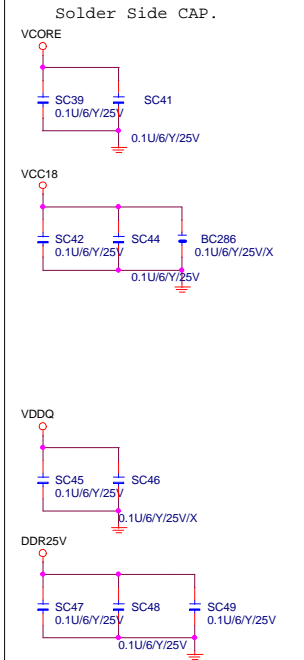
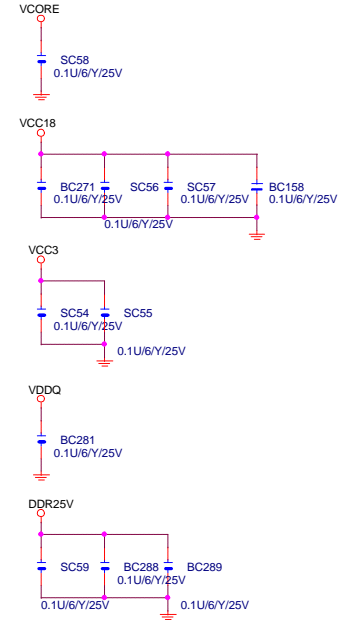
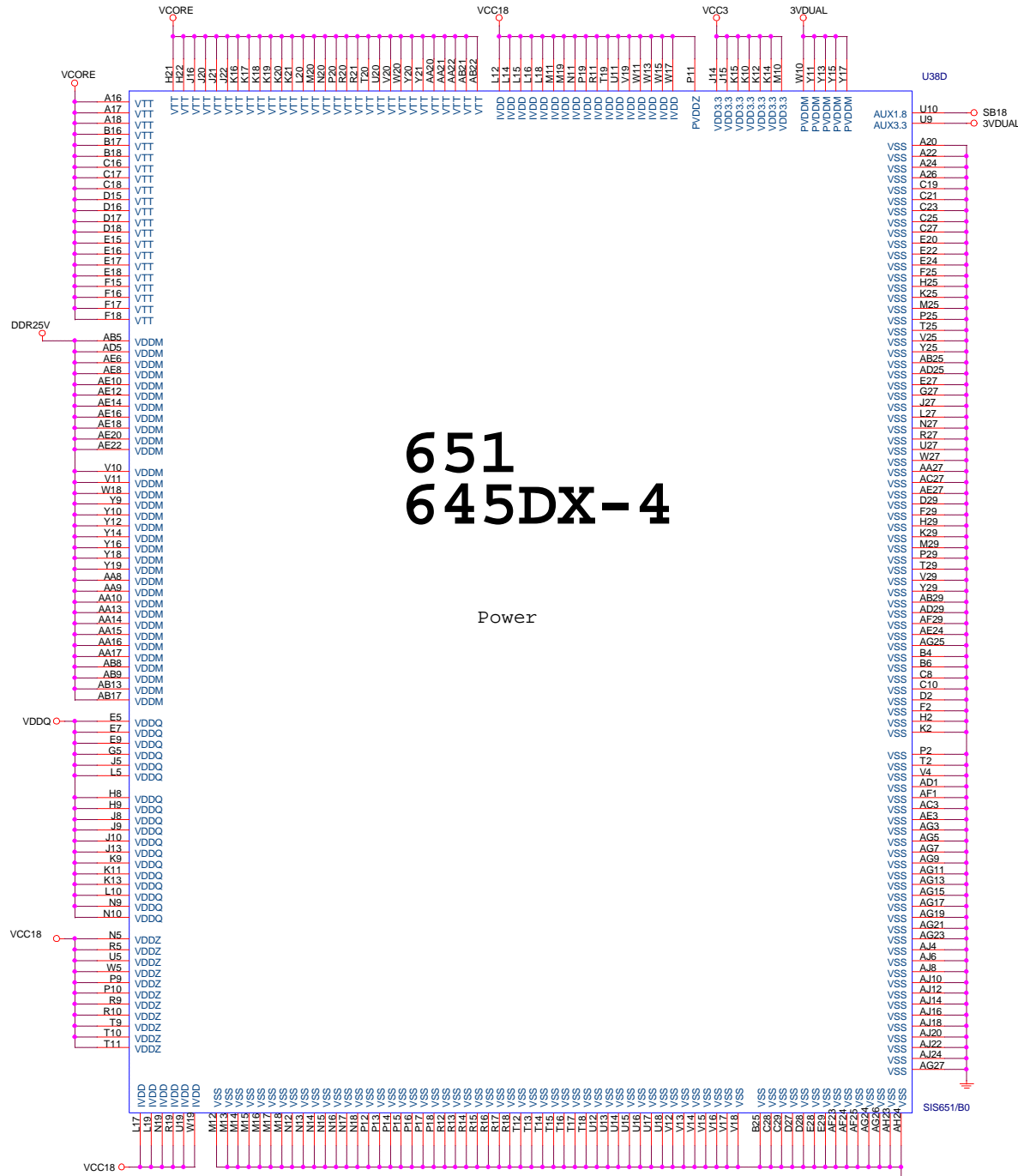
HyperZip



GIGABYTE		
Title SIS651/645DX(HYPER ZIP)		
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651 645DX-4

Power



GIGABYTE		
Title SIS651/645DX(PWR)		
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PDD0_15L <-> PDD[0..15] (21)
 SDD0_15L <-> SDD[0..15] (21)
 -REQ0_4I <-> -REQ[0..4] (20)
 -GNT0_3I <-> -GNT[0..3] (20)
 -C_BE0_3I <-> -C_BE[0..3] (20)
 AD0_31I <-> AD[0..31] (20)

-REQ4 F1 PREQ#4
 -REQ3 F2 PREQ#3
 -REQ2 E1 PREQ#2
 -REQ1 H5 PREQ#1
 -REQ0 F3 PREQ#0
 -GNT3 H3 PGNT#4
 -GNT2 G1 PGNT#3
 -GNT1 G2 PGNT#2
 -GNT0 H4 PGNT#1
 -GNT0 H4 PGNT#0
 -C_BE3 K3 C/BE#3
 -C_BE2 M4 C/BE#2
 -C_BE1 P1 C/BE#1
 -C_BE0 R4 C/BE#0
 (9,18,20) -INTA E3 INT#A
 (18,20) -INTB F4 INT#B
 (20) -INTC E2 INT#C
 (20) -INTD G4 INT#D
 (20) -FRAME M3 FRAME#
 (20) -IRDY M1 IRDY#
 (20) -TRDY M2 TRDY#
 (20) -STOP N4 STOP#
 (20) -SERR M5 SERR#
 (20) PAR N3 PAR
 (20) -DEVSEL N1 DEVSEL#
 (20) -PLOCK N2 PLOCK#
 (15) PCLK_SB Y2 PCICLK
 (9,21,22) -PCIRST R671 PCIRST#
 (15) ZCLK_SB Z2 ZCLK
 (9) ZSTB0 N19 ZSTB0
 (9) -ZSTB0 N20 ZSTB0#
 (9) ZSTB1 K20 ZSTB1
 (9) -ZSTB1 K19 ZSTB1#
 (9) ZREQ_UP N16 ZUREQ
 (9) ZREQ_DN N17 ZDREQ
 -SVDDZCMP R19 VDDZCMP
 -SZCMP_N N18 ZCMP_N
 -SZCMP_P R18 ZCMP_P
 -SVSSZCMP P18 VSSZCMP
 -SZ1XAVDD U20 Z1XAVDD
 -SZ1XAVSS U19 Z1XAVSS
 -SZ4XAVDD T20 Z4XAVDD
 -SZ4XAVSS T19 Z4XAVSS
 -SZVREF R20 ZVREF
 -ZVSSREF P20 ZVSSREF

AD31
 AD30
 AD29
 AD28
 AD27
 AD26
 AD25
 AD24
 AD23
 AD22
 AD21
 AD20
 AD19
 AD18
 AD17
 AD16
 AD15
 AD14
 AD13
 AD12
 AD11
 AD10
 AD9
 AD8
 AD7
 AD6
 AD5
 AD4
 AD3
 AD2
 AD1
 AD0

PCI

IDE

962/961B

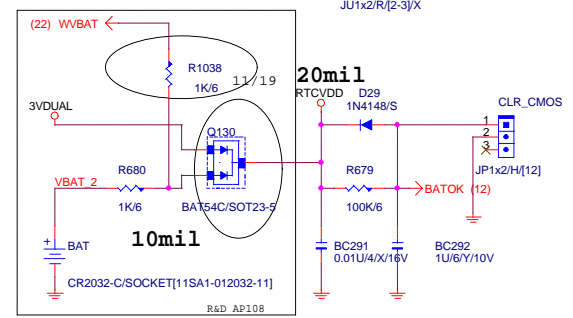
HyperZip

ZAD0
 ZAD1
 ZAD2
 ZAD3
 ZAD4
 ZAD5
 ZAD6
 ZAD7
 ZAD8
 ZAD9
 ZAD10
 ZAD11
 ZAD12
 ZAD13
 ZAD14
 ZAD15
 M18
 M17
 M16
 M15
 M14
 M13
 M12
 M11
 M10
 M9
 M8
 M7
 M6
 M5
 M4
 M3
 M2
 M1

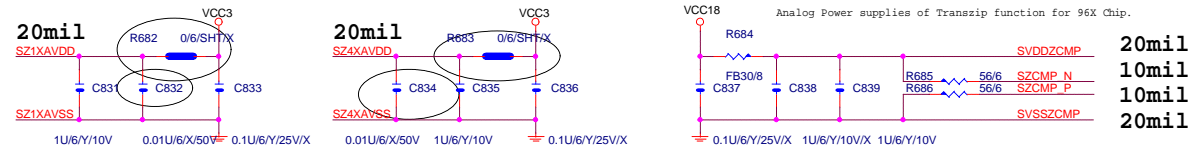
(9) ZAD[0..15] <-> ZAD[0..15]

IDEAVDD
 IDEAVSS
 ICHRDYA
 IDREQA
 IIRQA
 CBLIDA
 IIOR#A
 IIOW#A
 IDACK#A
 IDSA#A
 IDSA#A
 IDSA#A
 IDECSA#1
 IDECSA#0
 ICHRDYB
 IDREQB
 IIRQB
 CBLIDB
 IIOR#B
 IIOW#B
 IDACK#B
 IDSA#B
 IDSA#B
 IDSA#B
 IDECSB#1
 IDECSB#0
 IDA0
 IDA1
 IDA2
 IDA3
 IDA4
 IDA5
 IDA6
 IDA7
 IDA8
 IDA9
 IDA10
 IDA11
 IDA12
 IDA13
 IDA14
 IDA15
 IDB0
 IDB1
 IDB2
 IDB3
 IDB4
 IDB5
 IDB6
 IDB7
 IDB8
 IDB9
 IDB10
 IDB11
 IDB12
 IDB13
 IDB14
 IDB15
 U39A
 C826
 C827
 VCC18
 1U/6Y/10V/X
 0.1U/6Y/25V/X
 W10 PIORDY <-> PIORDY (21)
 V10 PDDREQ <-> PDDREQ (21)
 Y11 IRQ14 <-> IRQ14 (21)
 U12 P66DET <-> P66DET (21)
 Y11 -PDIOR <-> -PDIOR (21)
 Y9 -PDLOW <-> -PDLOW (21)
 Y10 -PDDACK <-> -PDDACK (21)
 T11 PDA2 <-> PDA2 (21)
 U11 PDA1 <-> PDA1 (21)
 W11 PDA0 <-> PDA0 (21)
 T12 -PDCS3 <-> -PDCS3 (21)
 V12 -PDCS1 <-> -PDCS1 (21)
 W17 SIORDY <-> SIORDY (21)
 Y17 SDDREQ <-> SDDREQ (21)
 T16 IRQ15 <-> IRQ15 (21)
 U17 S66DET <-> S66DET (21)
 T14 -SDIOR <-> -SDIOR (21)
 W16 -SDLOW <-> -SDLOW (21)
 V16 -SDDACK <-> -SDDACK (21)
 Y18 SDA2 <-> SDA2 (21)
 T15 SDA1 <-> SDA1 (21)
 V17 SDA0 <-> SDA0 (21)
 U16 -SDCS3 <-> -SDCS3 (21)
 W18 -SDCS1 <-> -SDCS1 (21)
 U10 PDD0
 V9 PDD1
 W8 PDD2
 T9 PDD3
 Y7 PDD4
 V7 PDD5
 Y6 PDD6
 Y5 PDD7
 W6 PDD8
 U8 PDD9
 W7 PDD10
 V8 PDD11
 U8 PDD12
 Y8 PDD13
 T10 PDD14
 W9 PDD15
 Y16 SDD0
 V15 SDD1
 U14 SDD2
 W14 SDD3
 V13 SDD4
 T13 SDD5
 Y13 SDD6
 Y12 SDD7
 W12 SDD8
 W13 SDD9
 U13 SDD10
 Y14 SDD11
 V14 SDD12
 W15 SDD13
 Y15 SDD14
 U15 SDD15

CLR_CMOS	CLEAR COMS JUMPER
1-2	Enable
2-3	Normal (Default)

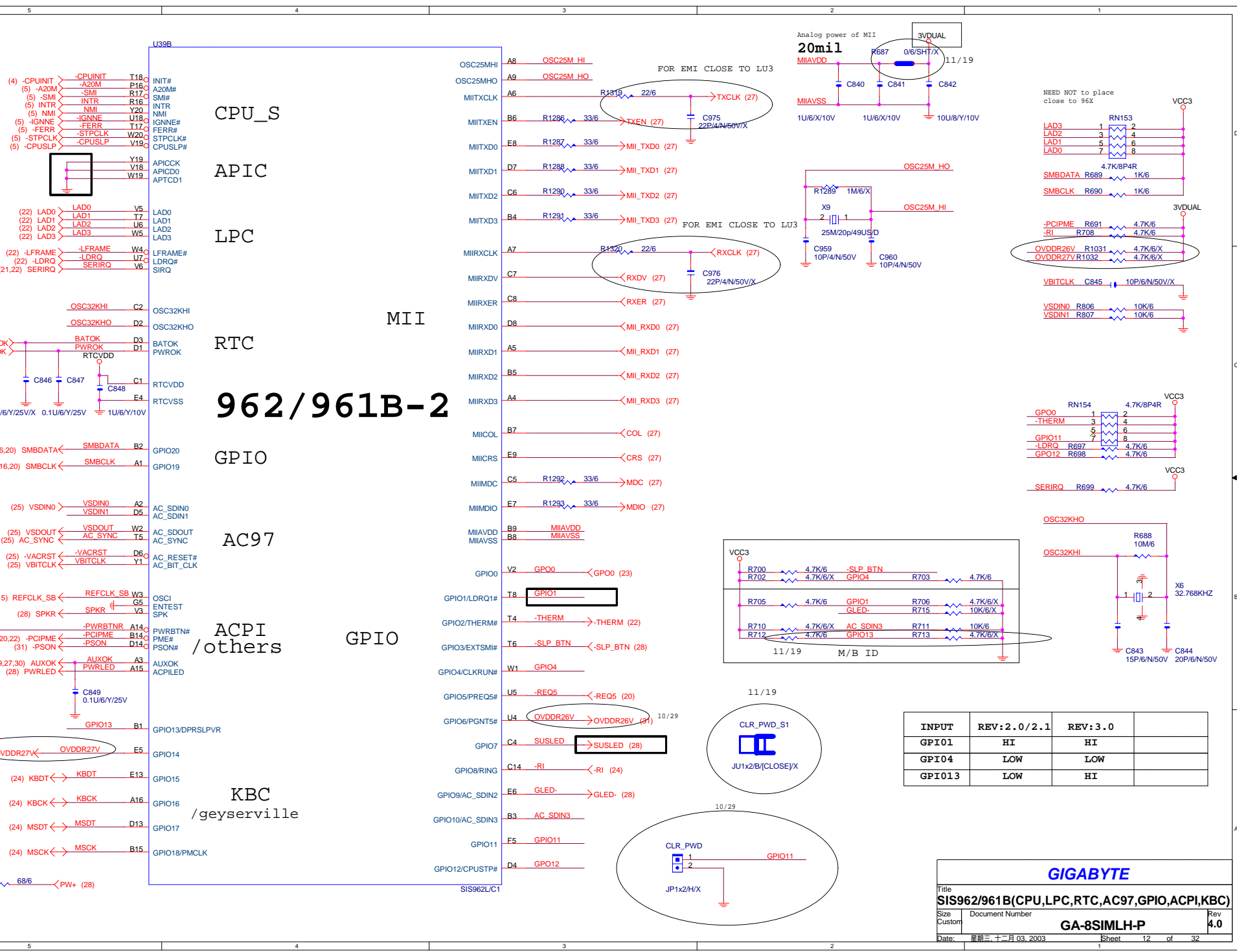


Analog Power supplies of Transzip function for 96X Chip.



NF REQUEST CLR_CMOS

GIGABYTE		
SIS962(HP ZIP,PCI,IDE)		
Title		
Size Custom	Document Number	Rev 4.0
GA-8SIMLH-P		
Date: 星期三, 十二月 03, 2003	Sheet 11	of 32



CPU_S

APIC

LPC

MII

RTC

962/961B-2

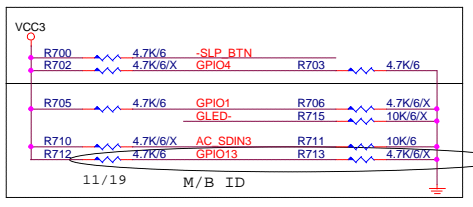
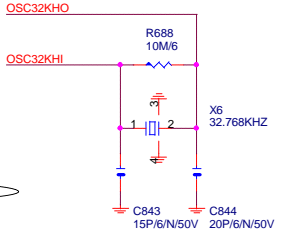
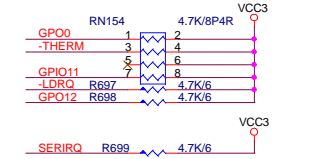
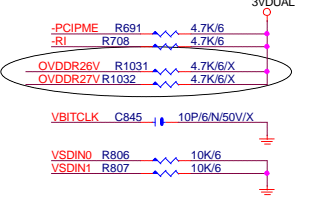
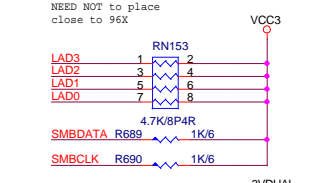
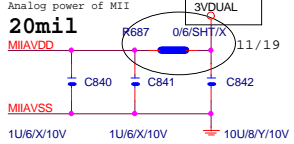
GPIO

AC97

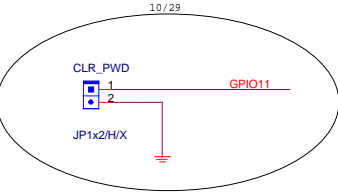
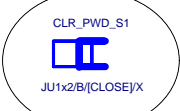
ACPI / others

GPIO

KBC / geyserville



INPUT	REV: 2.0/2.1	REV: 3.0	
GPIO1	HI	HI	
GPIO4	LOW	LOW	
GPIO13	LOW	HI	

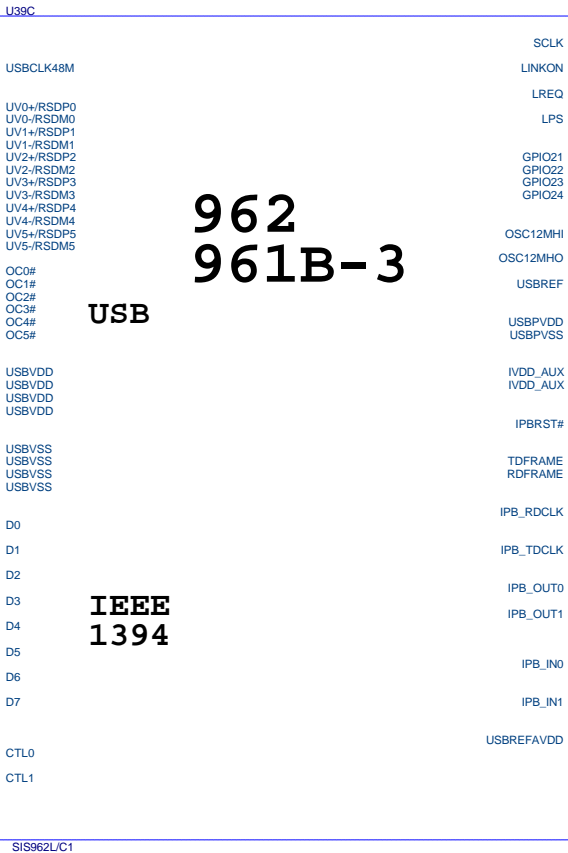


GIGABYTE

Title
SIS962/961B(CPU,LPC,RTC,AC97,GPIO,ACPI,KBC)

Size Custom
GA-8SIMLH-P

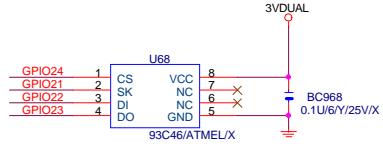
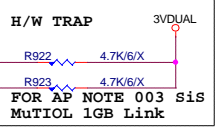
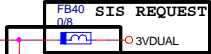
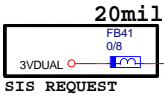
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962 961B-3

USB

IEEE 1394



10/29
 USBDO- <-> USBDO- (27)
 USBDO+ <-> USBDO+ (27)
 USBDT3- <-> USBDT3- (27)
 USBDT3+ <-> USBDT3+ (27)

SUPPORT SIS962 ONLY POP 0/8P4R(USB2.0)

10/29
 USBDT1- <-> USBDT1- (21)
 USBDT1+ <-> USBDT1+ (21)
 USBDT4- <-> USBDT4- (21)
 USBDT4+ <-> USBDT4+ (21)

SUPPORT SIS962 ONLY POP 0/8P4R(USB2.0)

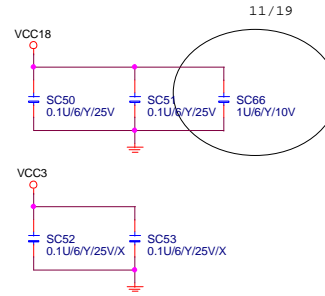
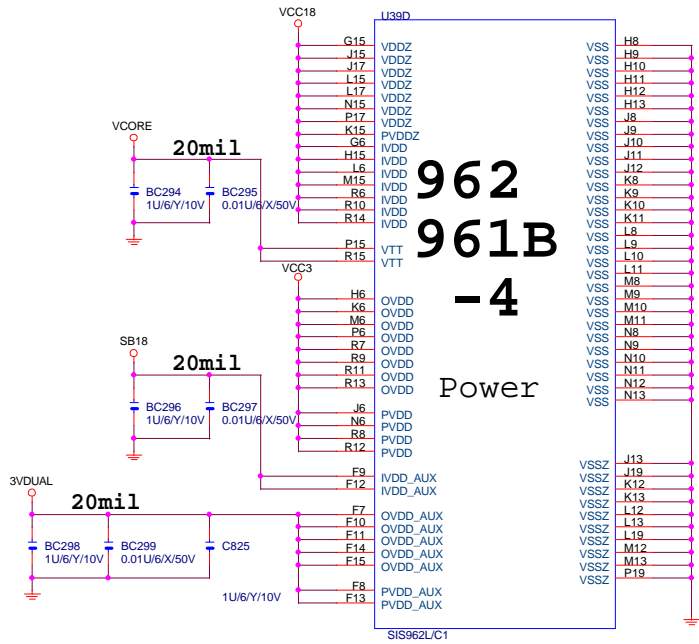
SUPPORT SIS962 ONLY POP 0/8P4R(USB2.0)

10/29
 USBDT2- <-> USBDT2- (21)
 USBDT2+ <-> USBDT2+ (21)
 USBDT5- <-> USBDT5- (21)
 USBDT5+ <-> USBDT5+ (21)

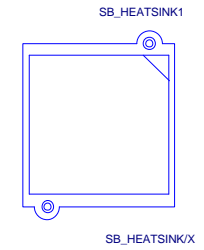
SUPPORT SIS962 ONLY POP 0/8P4R(USB2.0)

SUPPORT SIS962 ONLY POP 0/8P4R(USB2.0)
 AGPUSB,CNRUSB DEFAULT NO POP
 NOTE: POP CN3 15K/8P4R---->USB PULL DOWN
 USB CONTROLLER MUST NOT BEEN FLOATING.

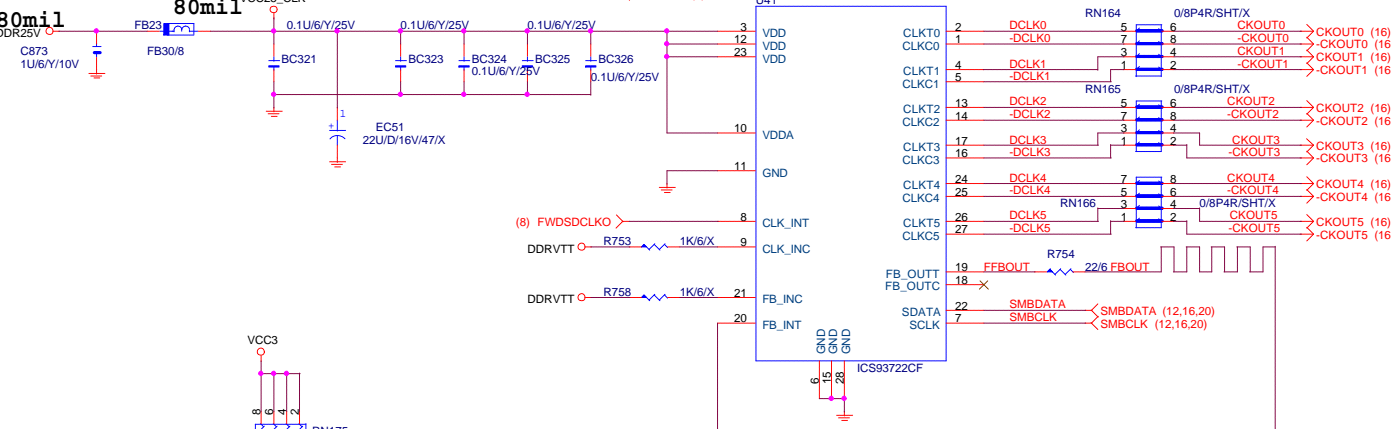
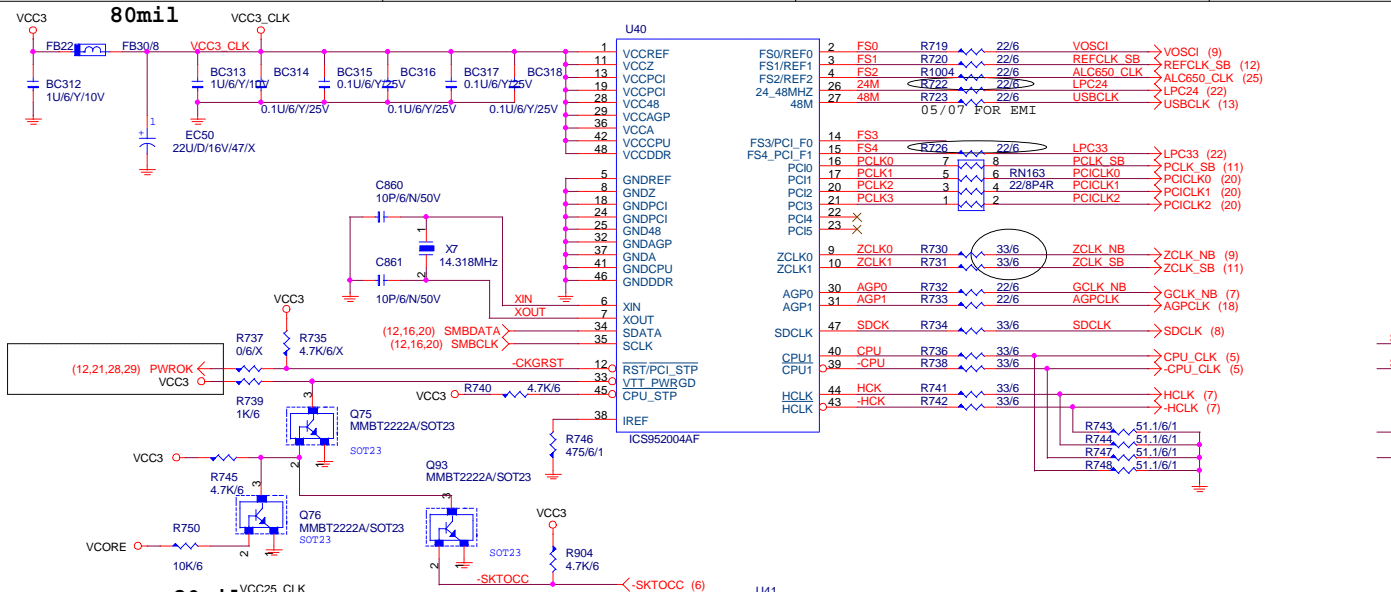
GIGABYTE		
Title SIS962/961B(USB20,1394)		
Size Custom	Document Number GA-8SIMLH-P	Rev 4.0
Date:	星期三, 十二月 03, 2003	Sheet 13 of 32



S.B HEATSINK

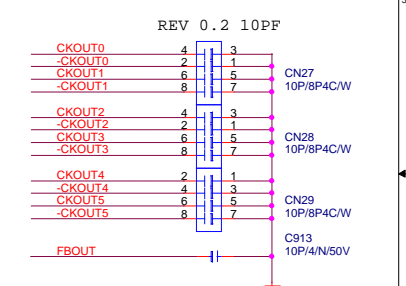
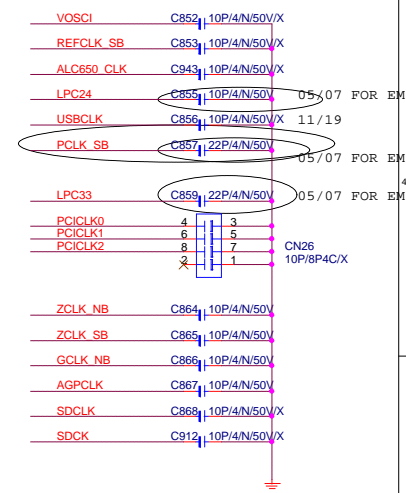
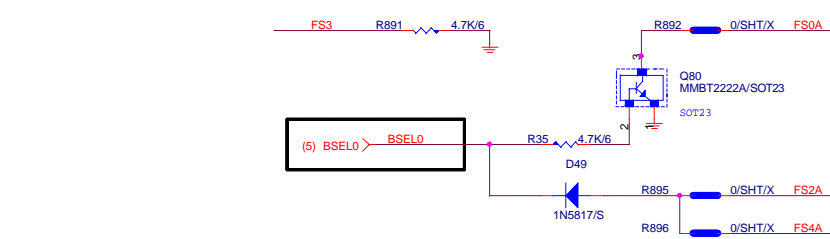


GIGABYTE		
Title		
SIS962/961B(PWR)		
Size	Document Number	Rev
Custom	GA-8SIMLH-P	4.0
Date:	星期三, 十二月 03, 2003	Sheet 14 of 32



ICS952001/2004						
CPU	DDR	FS0	FS1	FS2	FS3	FS4
100	133	1	1	0	0	0
133	133	0	1	1	0	1

DEFAULT SETUP AUTO(100/133)



REV 0.2 10PF
DCLK +/----->0 ohm ADD CAP 10PF (clear glitch)

GIGABYTE

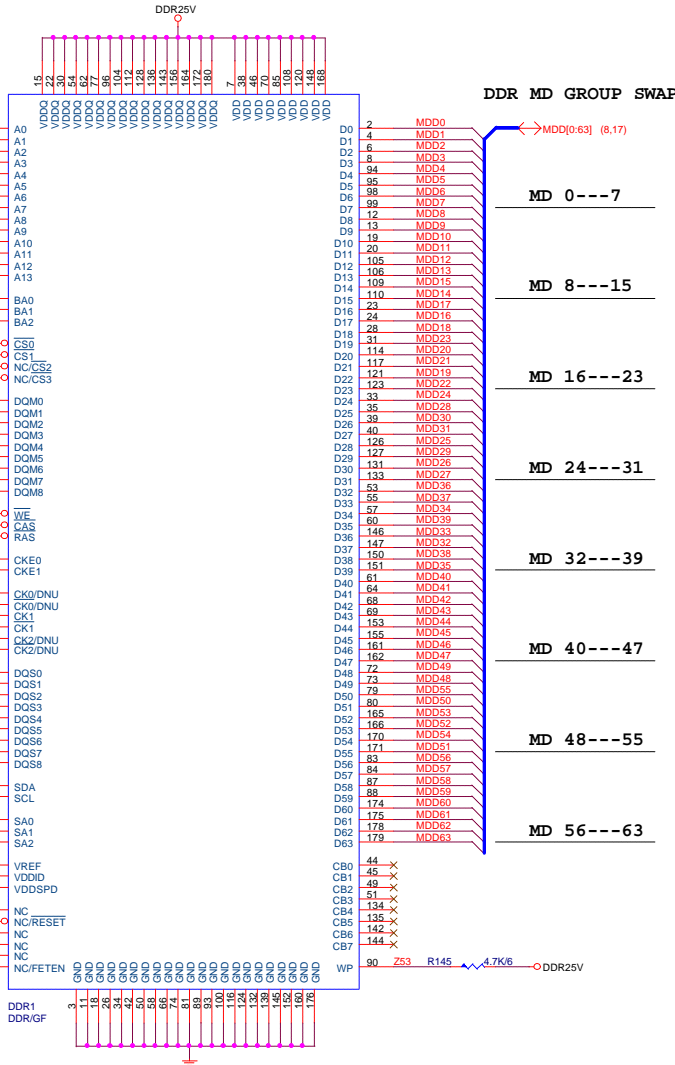
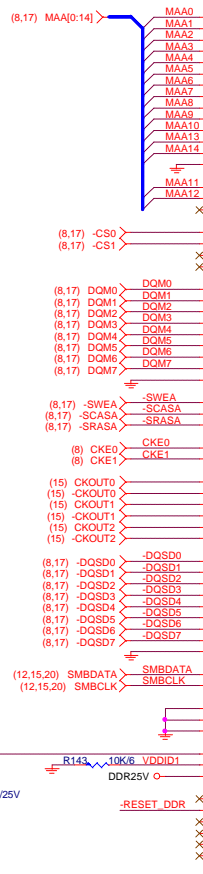
Title
CLOCK GEN + DDR BUFFER

Size Custom Document Number **GA-8SIMLH-P** Rev **4.0**

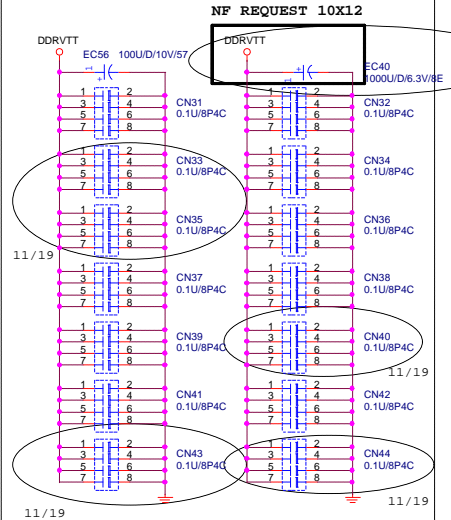
Date: 星期三, 十二月 03, 2003 Sheet 15 of 32

DDR SDRAM 1,2

SIS ONLY MAA



DDRVTT Decouple

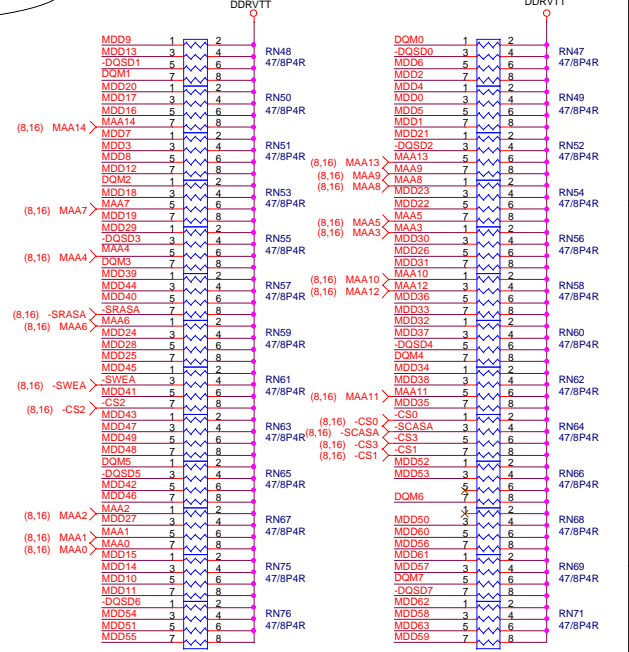


R&D NOTE 109 (0.1U/8P4C X9PCS)

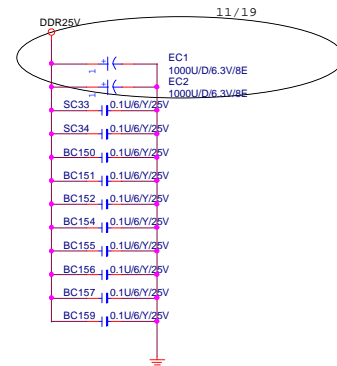
NOTE: Place these decoupling capacitors close to VTT_MEM termination resistors. (one decoupling capacitor for each two R-packs)

DDR TERMINATION

REV 0.2 DDR DIMM ISSUE
33-->47 OHM

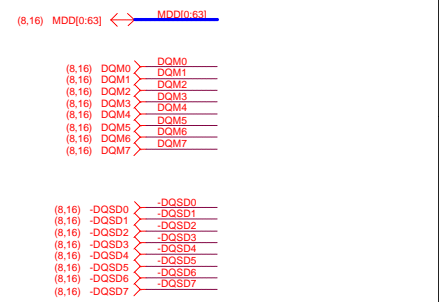
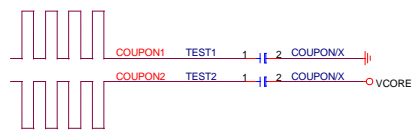


DDR25V Decouple

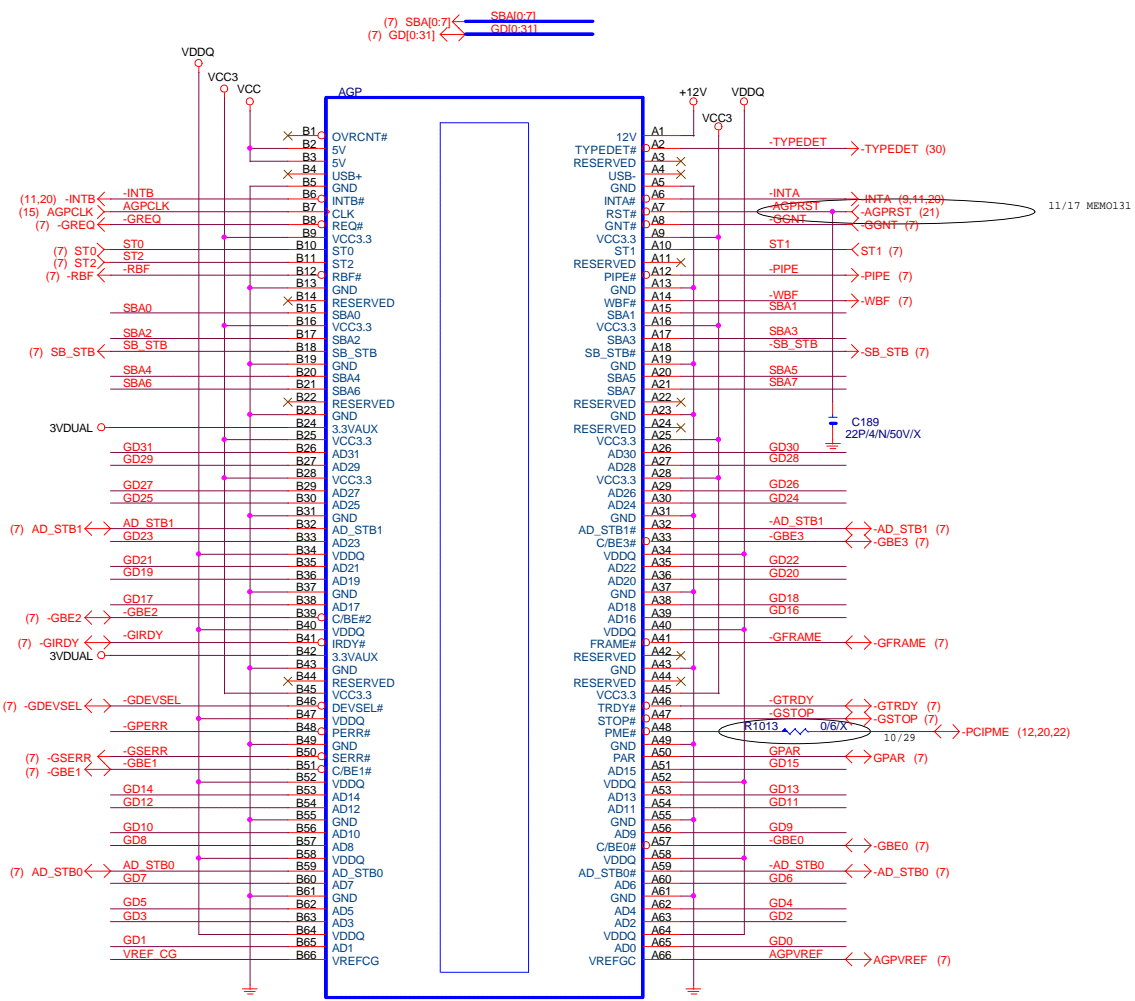


NOTE: Place Dretribute 4 pcs per DDR module.

IMPEDENCE TESTING COUPON

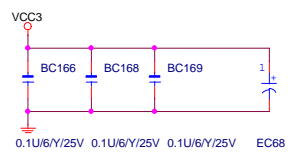


Title		
GIGABYTE		
DDR UNBUFFERED 3		
Size	Document Number	Rev
Custom	GA-8SIMLHP	4.0
Date:	星期二, 2003年03月12日	Sheet 17 of 32

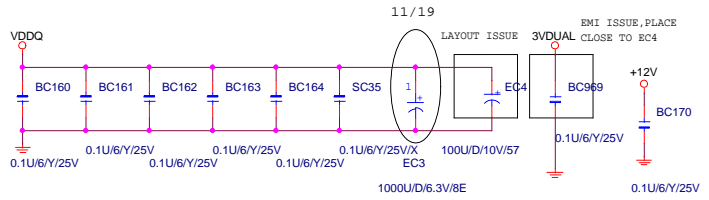


UAGP132/CO/GF
REV 0.2 AGP BOM MODIFY
11AC1-05R124-11

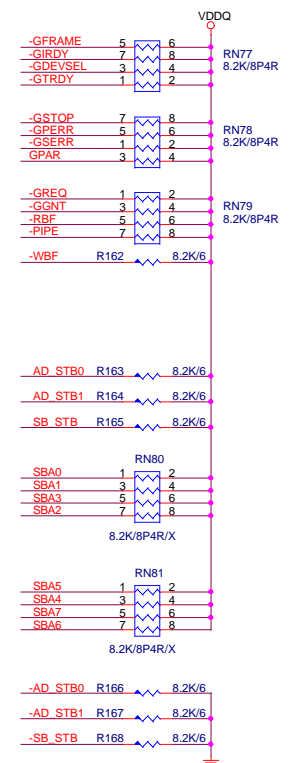
AGP SLOT (AGP-N)



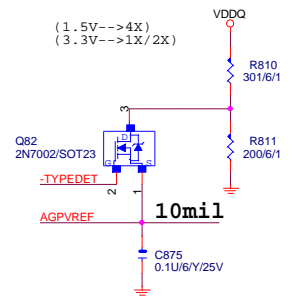
Place 1 at each pair of 3.3V pins
Decoupling capacitors
(Place near AGP slot)



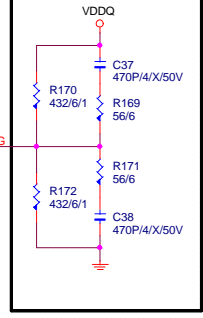
Place 1 at each pair of VDDQ pins
Place an additional for spread from A14 - A31



SWITCH CIRCUIT FOR VDDQ



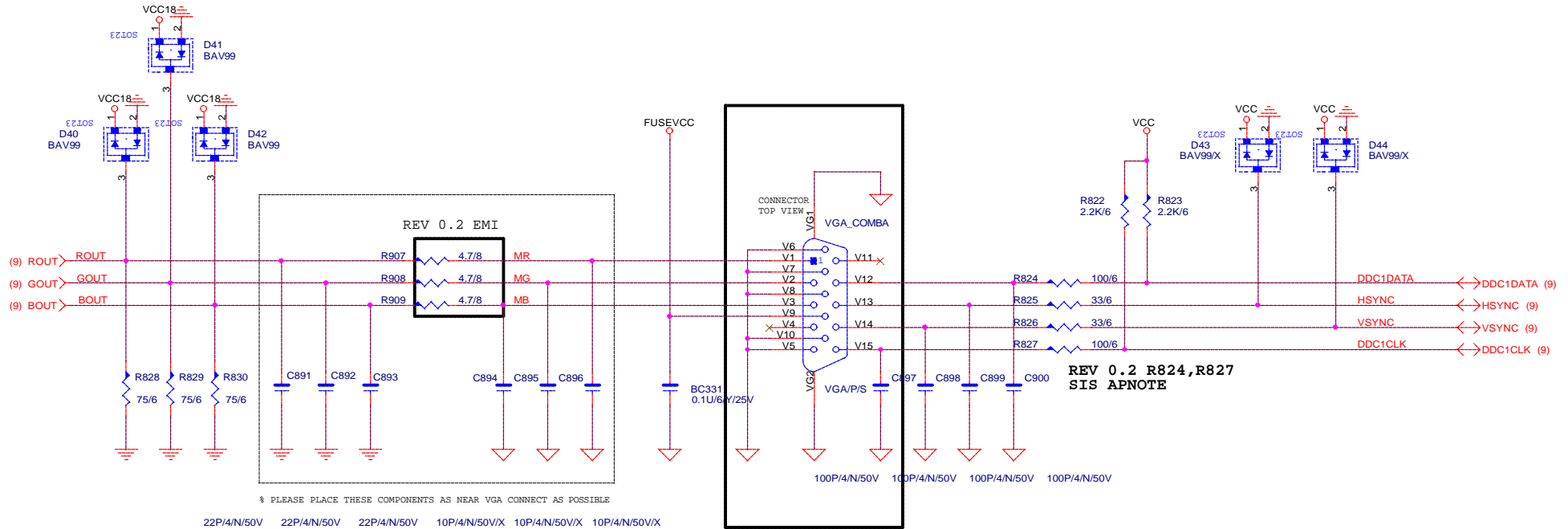
SIS DESIGN



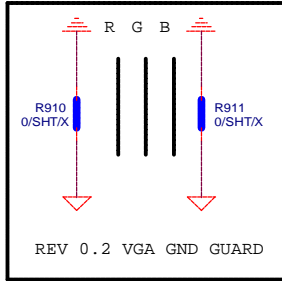
GIGABYTE		
AGP SLOT		
Title	AGP SLOT	
Size	Document Number	Rev
Custom	GA-8SIMLH-P	4.0
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VGA CONNECTOR 1

SIS 645DX NO POP



DUAL LAYOUT (VGA/COM)



**REV 0.2 R824, R827
SIS APNOTE**

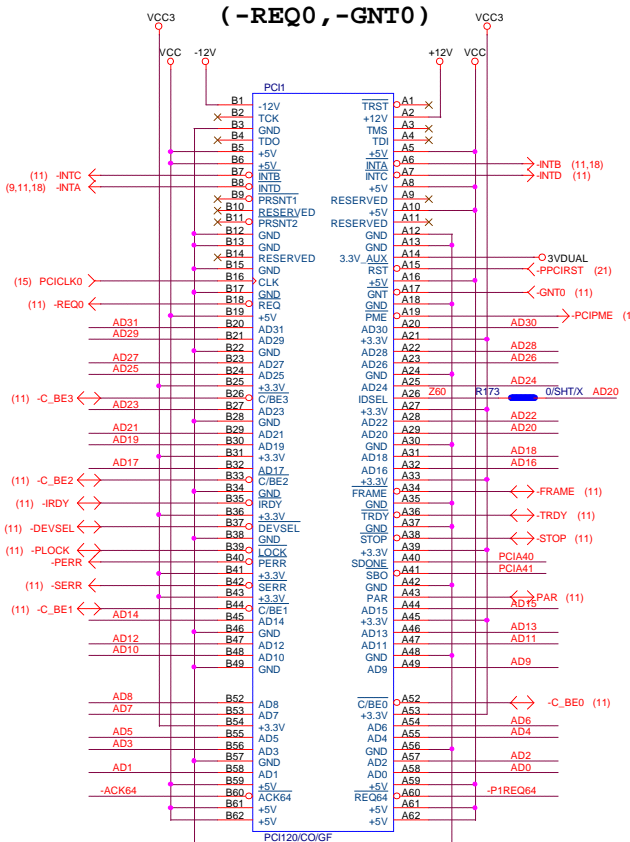
GIGABYTE		
Title VGA CONNECTOR		
Size B	Document Number GA-8SIMLH-P	Rev 4.0
Date: 星期三, 十二月 03, 2003	Sheet 19	of 32

PCI SLOT 1,2,3

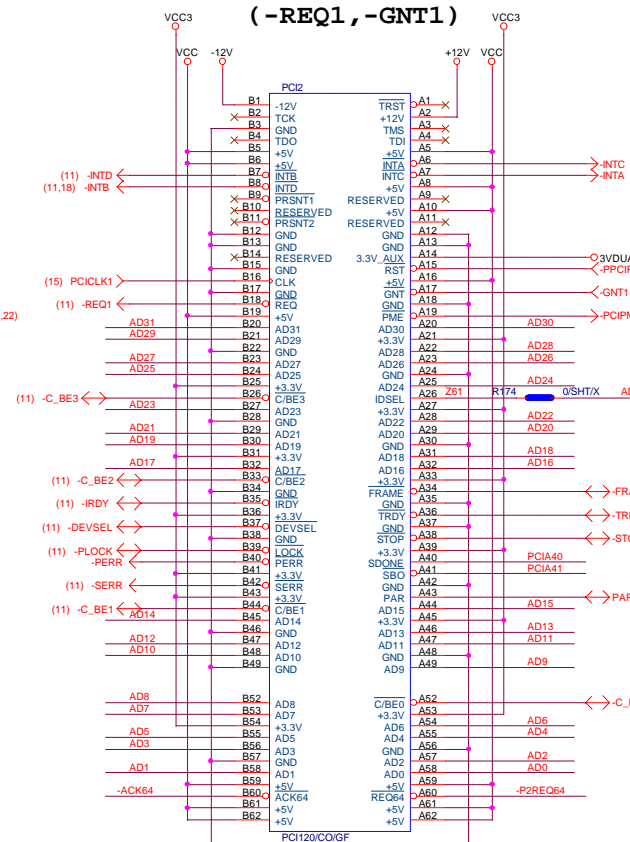
PCI SLOT1
(-REQ0, -GNT0)

PCI SLOT2
(-REQ1, -GNT1)

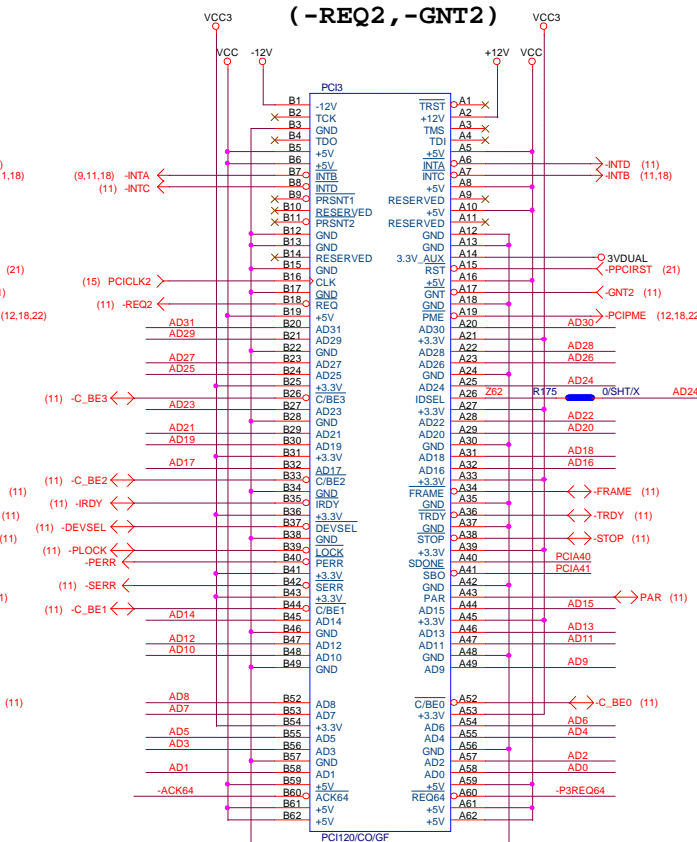
PCI SLOT3
(-REQ2, -GNT2)



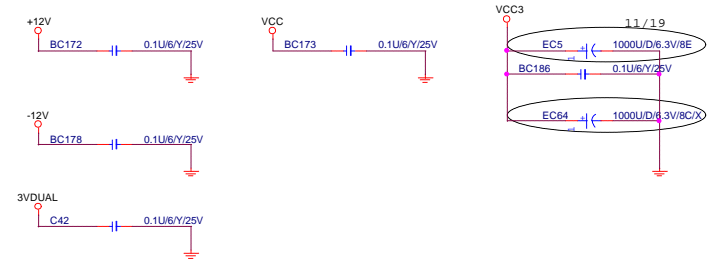
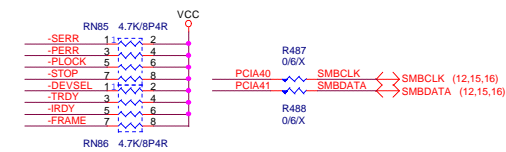
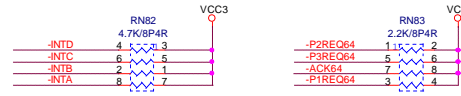
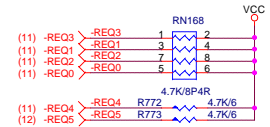
SIS-IDSEL(A20)
(B)



SIS-IDSEL(A22)
(C)

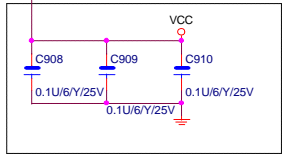
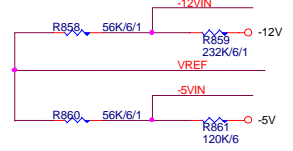
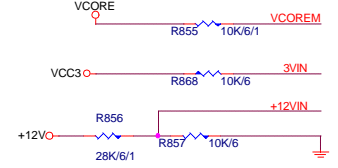
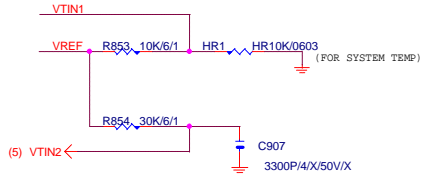
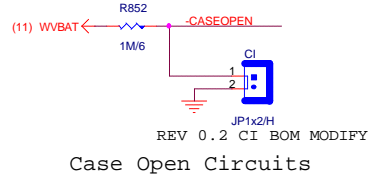
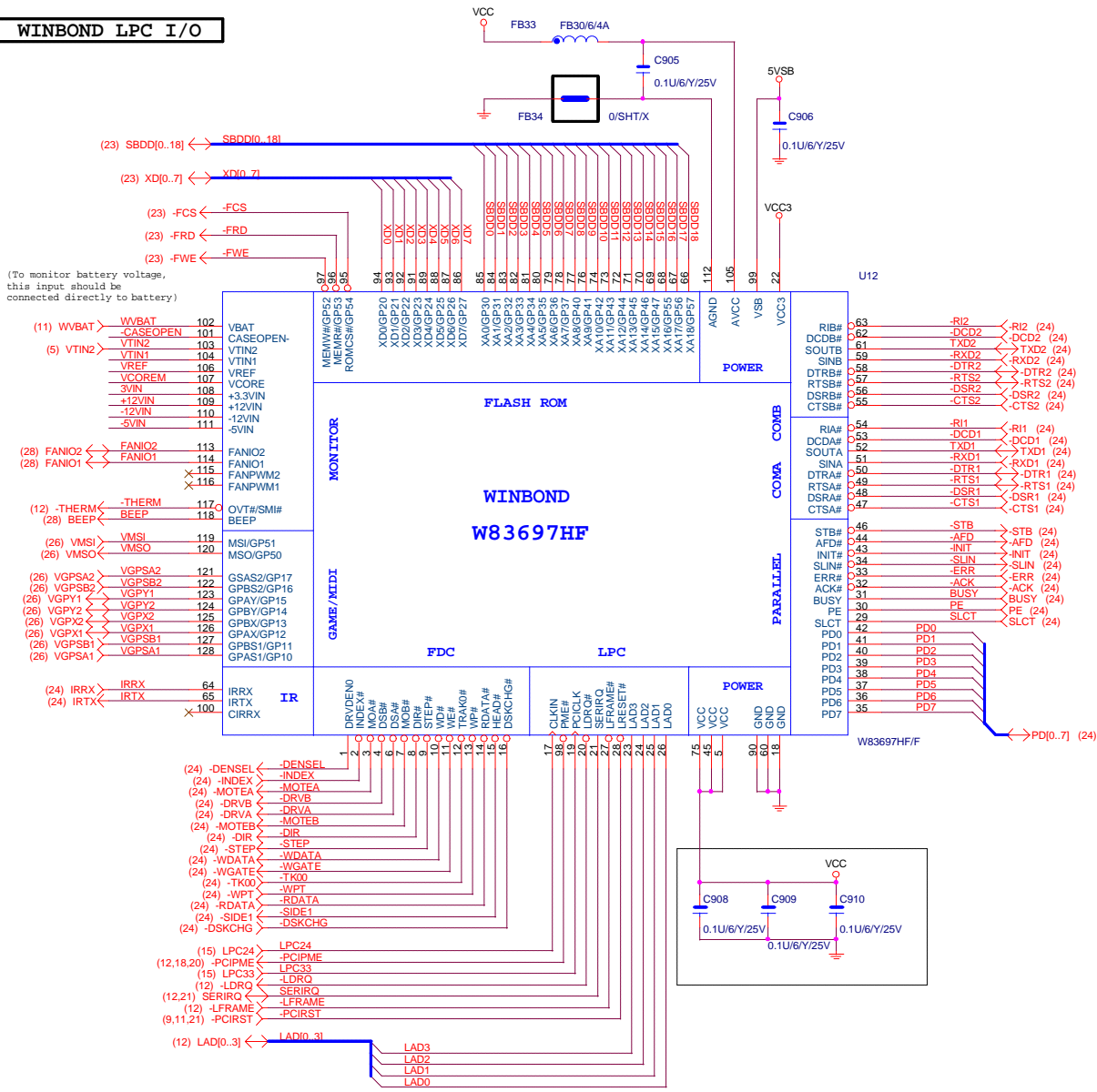


SIS-IDSEL(A24)
(D)

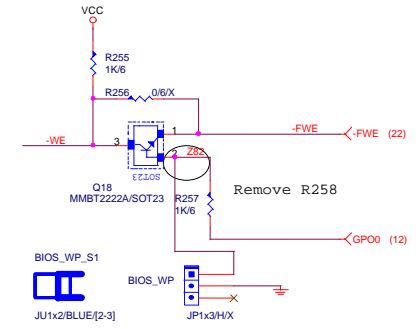
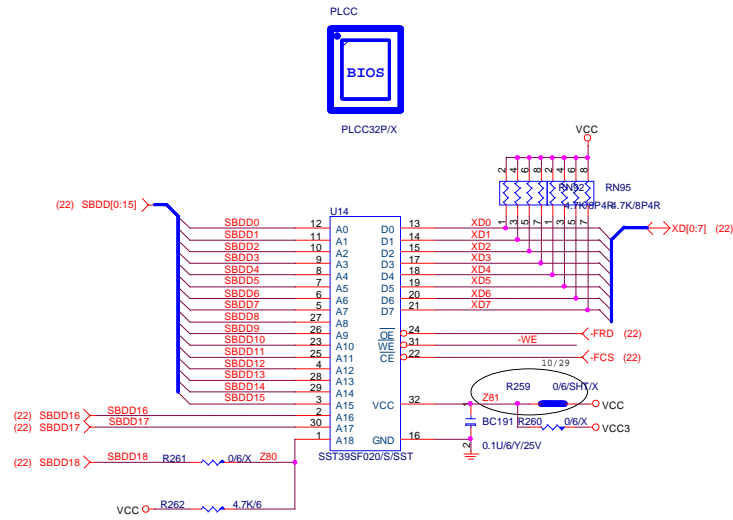


GIGABYTE			
PCI SLOT 1,2,3			
Size	Document Number	Rev	
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WINBOND LPC I/O

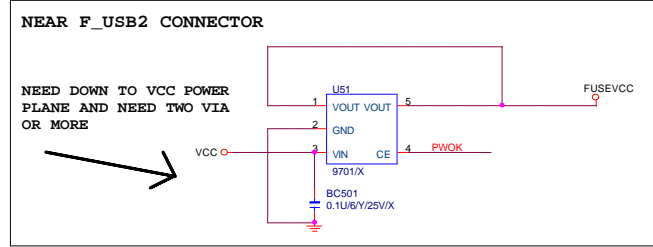
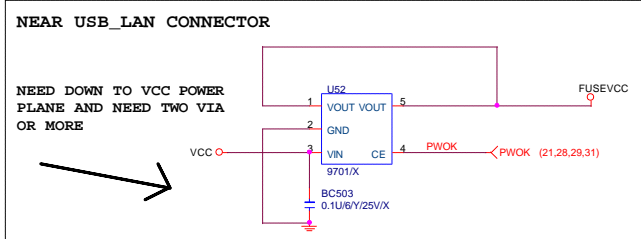
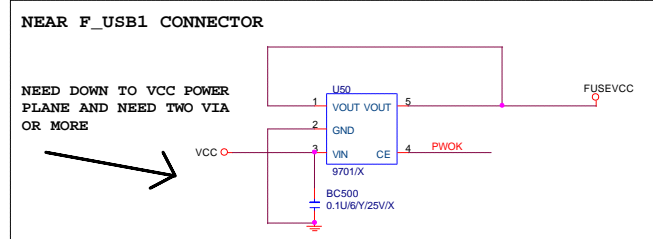


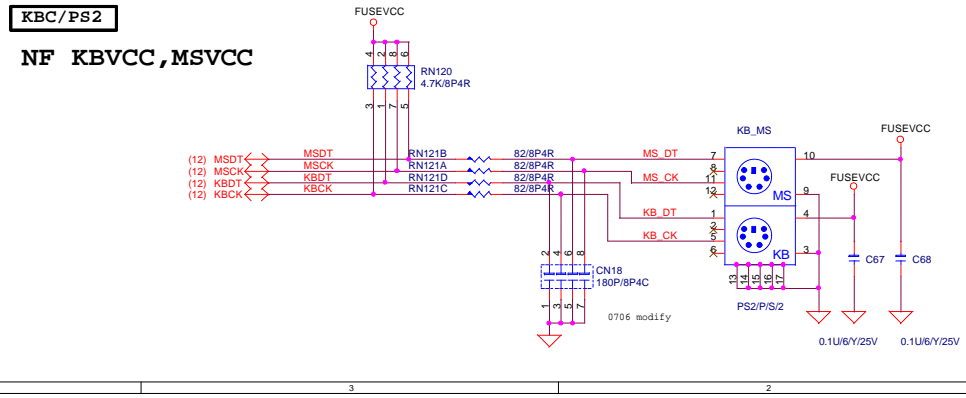
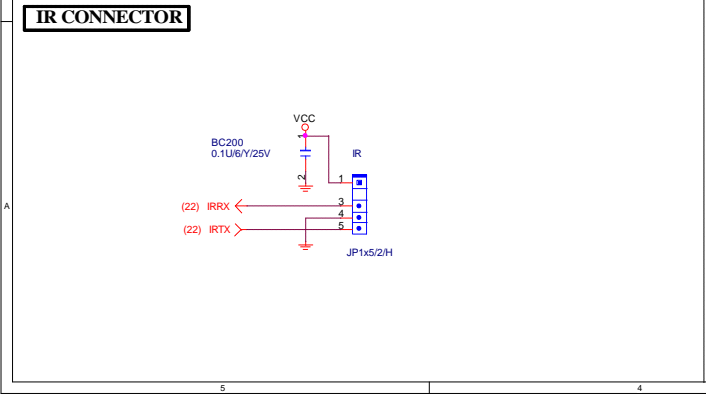
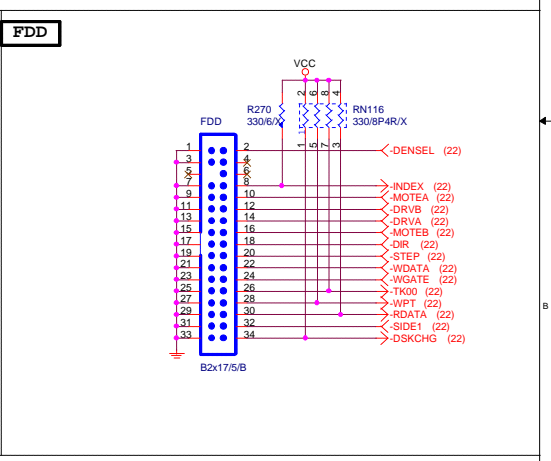
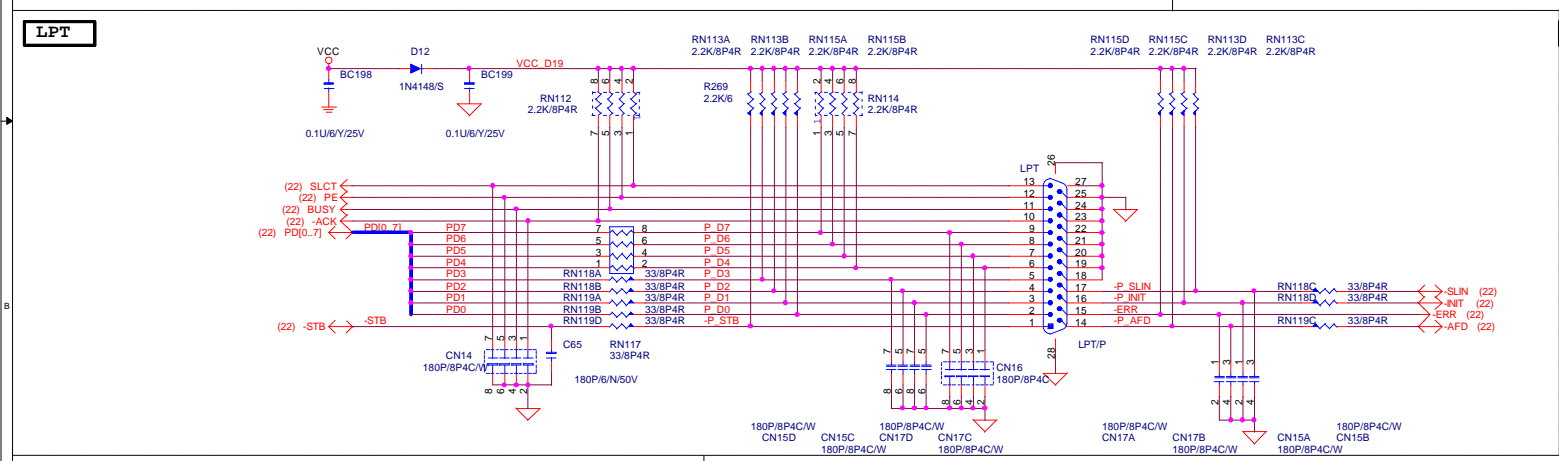
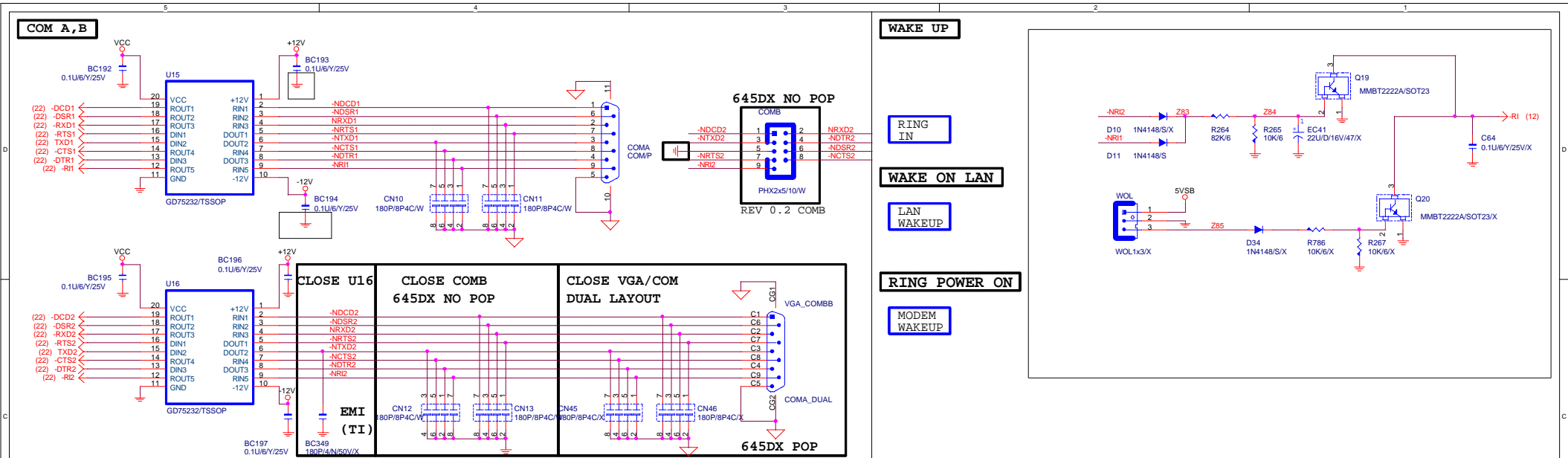
GIGABYTE		
Title		
LPC W83697		
Size	Document Number	Rev
Custom	GA-8SIMLH-P	4.0
Date:	星期三, 三月 03, 2003	Sheet 22 of 32

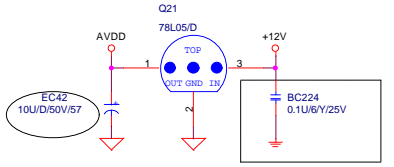
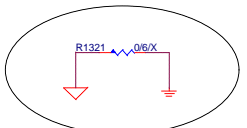
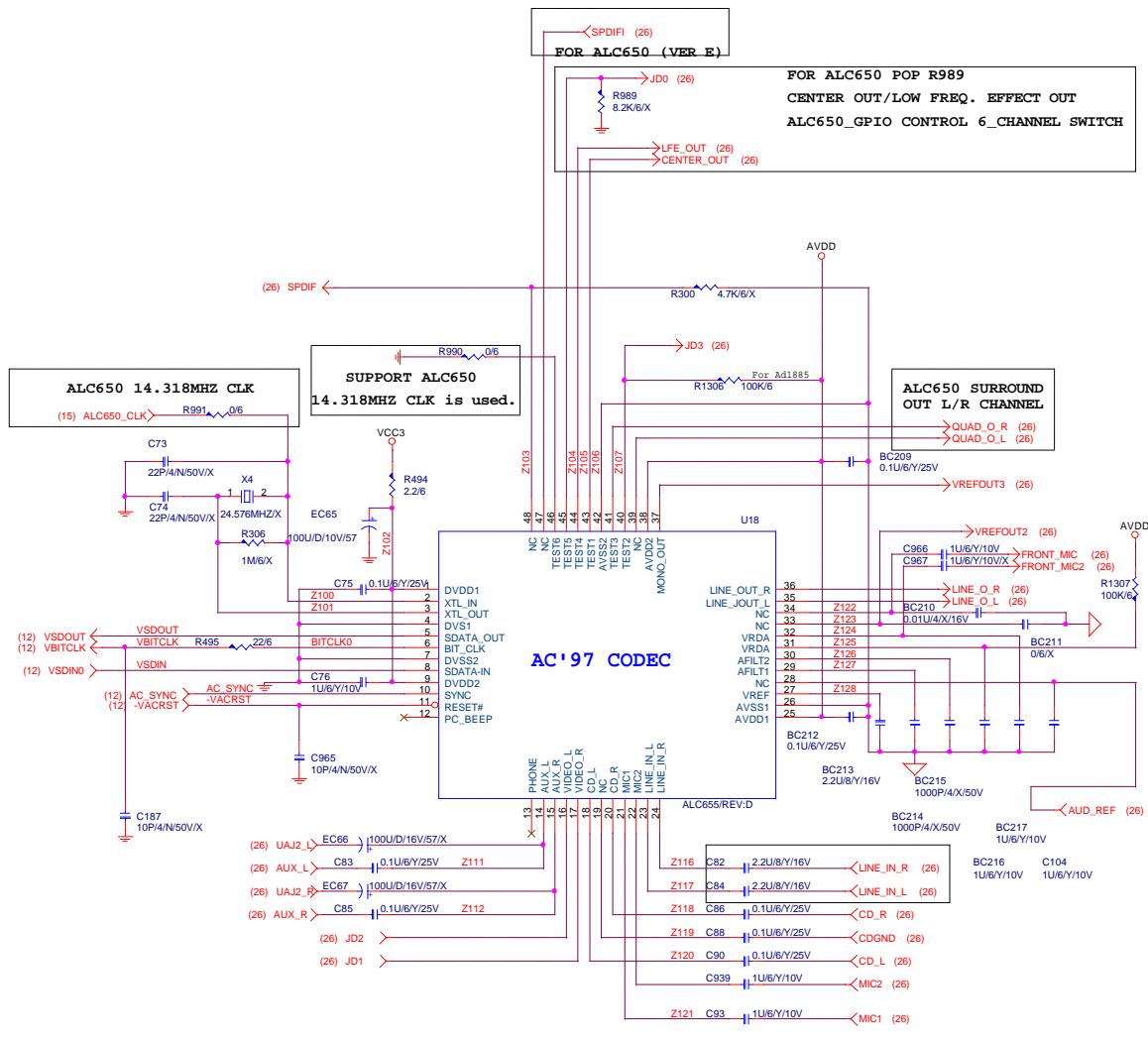


BIOS_WP: BIOS WRITE PROTECT

PIN	BIOS_WP
1-2	WRITE PROTECT
2-3	WRITE ENABLE (default)





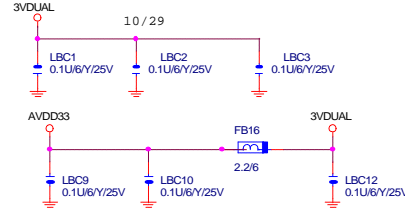
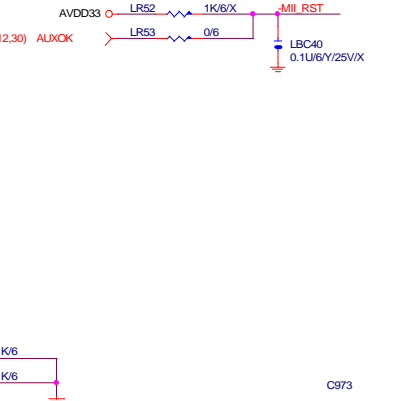
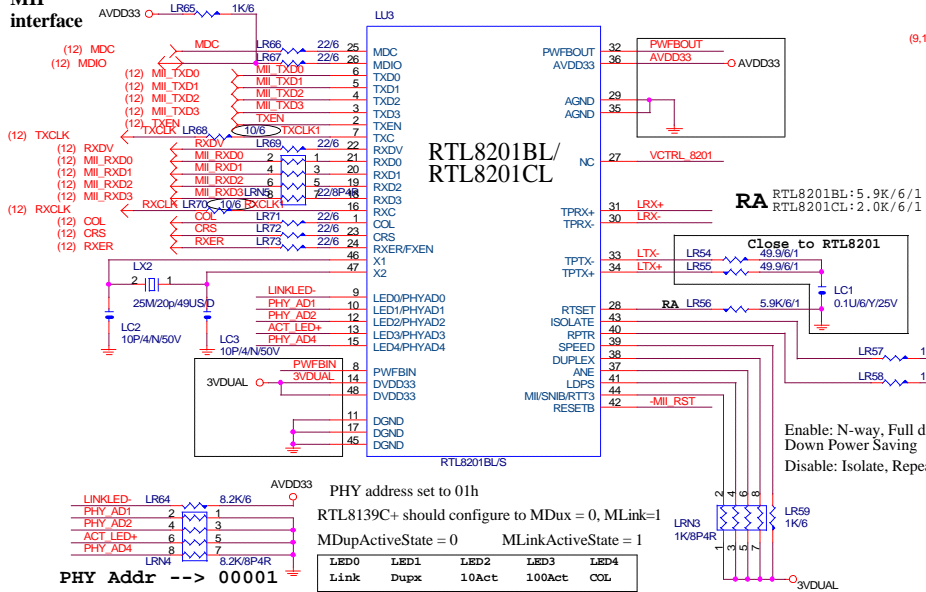


NF	SIGMATEL9756
Disti	ALC201A

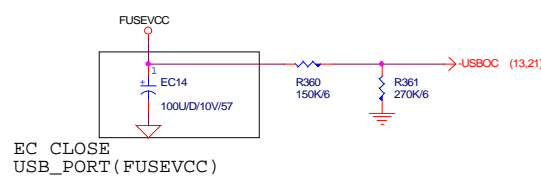
GIGABYTE	
AUDIO (AC97 CODEC)	
Title	Rev
Size	4.0
Custom	Document Number
GA-8SIMLHP	
Date:	Sheet 25 of 32

Connect to MII interface

RTL8201BL/ RTL8201CL Co-Layout



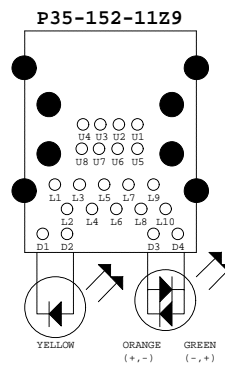
USB2.0 REAR USBX2



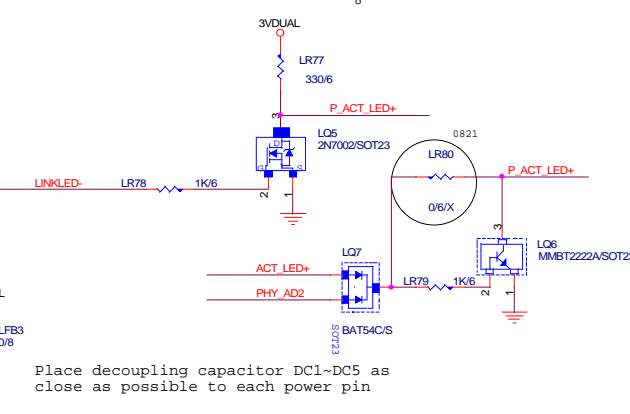
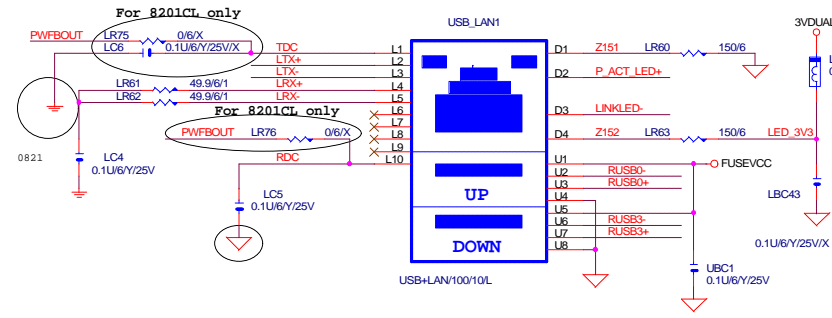
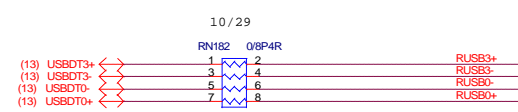
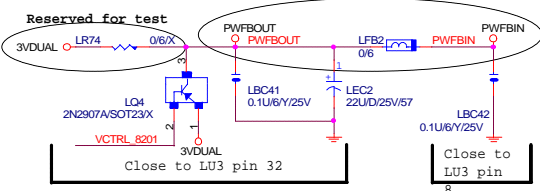
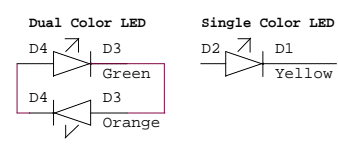
PHY address set to 01h
RTL8139C+ should configure to MDux = 0, MLink=1
MDupActiveState = 0 MLinkActiveState = 1

LED0 Link	LED1 Dupx	LED2 10Act	LED3 100Act	LED4 COL
-----------	-----------	------------	-------------	----------

PHY Addr --> 00001

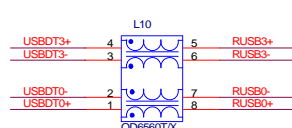


Link (Speed)	(Link to Hub)	Data Active	Transmit
10Mb	Green (ON)	Yellow	(Blink)
100Mb	Green (ON)	Yellow	(Blink)
1Gb	--	--	--

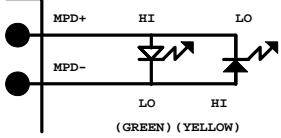


Place decoupling capacitor DC1-DC5 as close as possible to each power pin

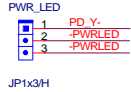
BLOCK A : The components inside BLOCK A are reserved for RTL8201B(.25u version). In RTL8201B, DVDD0 and AVDD0 will be fed 2.5V produced by BLOCK A which is functional as linear regulator and L3, R6 will be removed. In order to be layout-compatible between RTL8201 and RTL8201B, please reserve the component space and pads in your layout for future extension.



FRONT PANEL



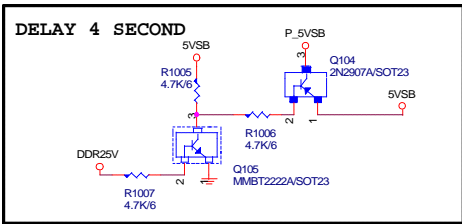
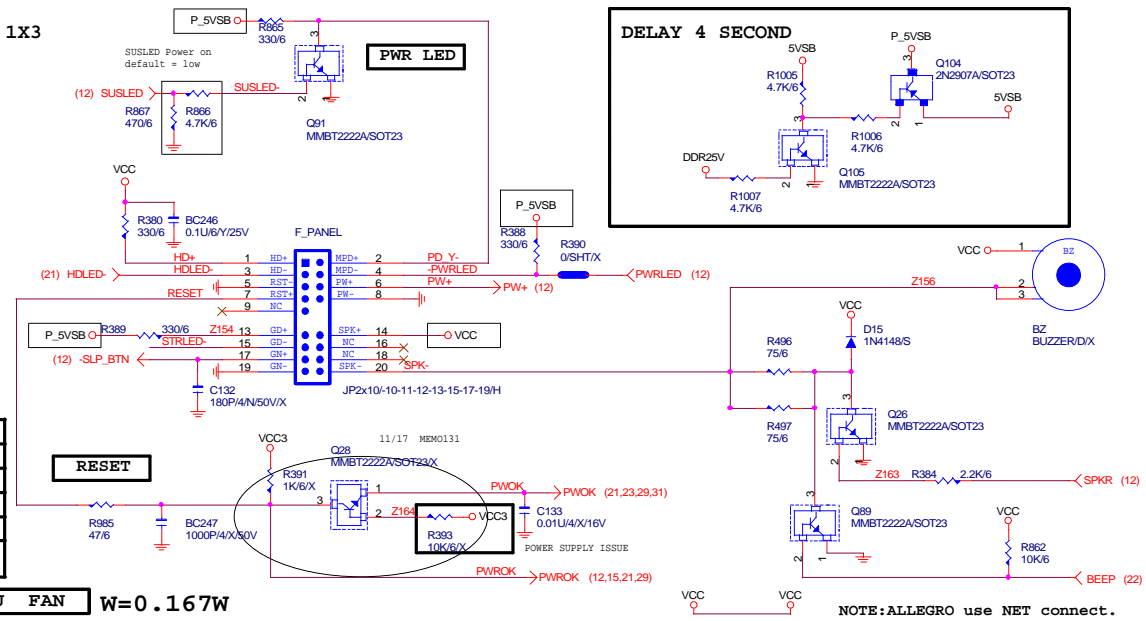
**PWR_LED FOR DISTI PIN 1X3
LED USED**



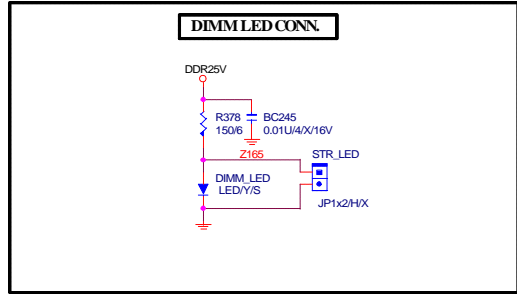
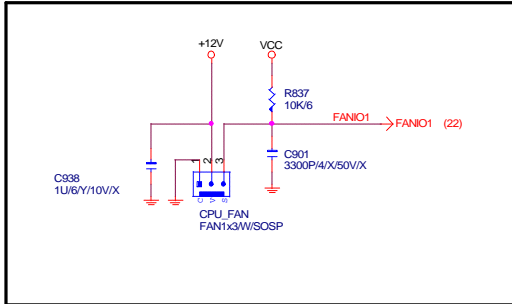
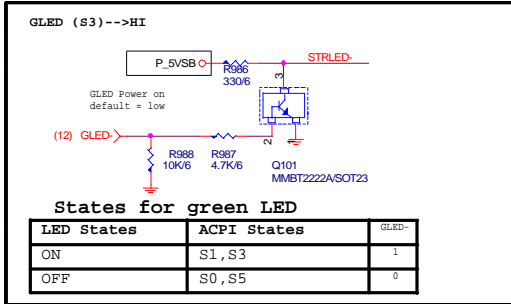
LED States	ACPI States	MPD+	MPD-
OFF	S1,S3,S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING

States for a dual-color power LED

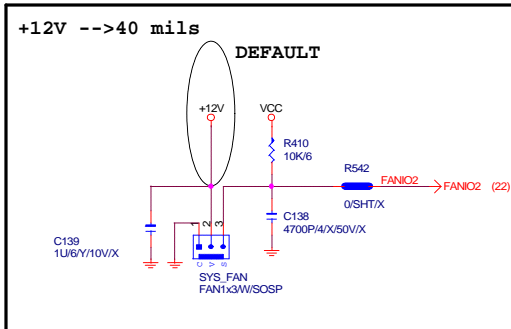
LED States	ACPI States	MPD+	MPD-
OFF	S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING
Steady Yellow	S1,S3	LO	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING



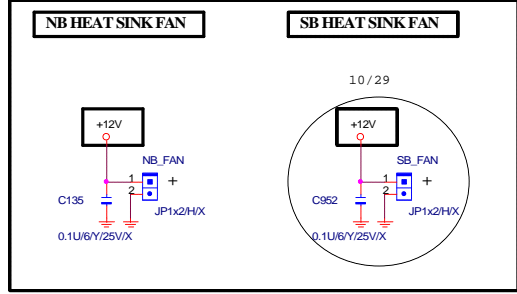
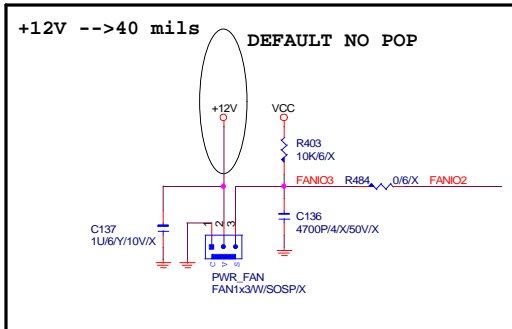
CPU FAN W=0.167W

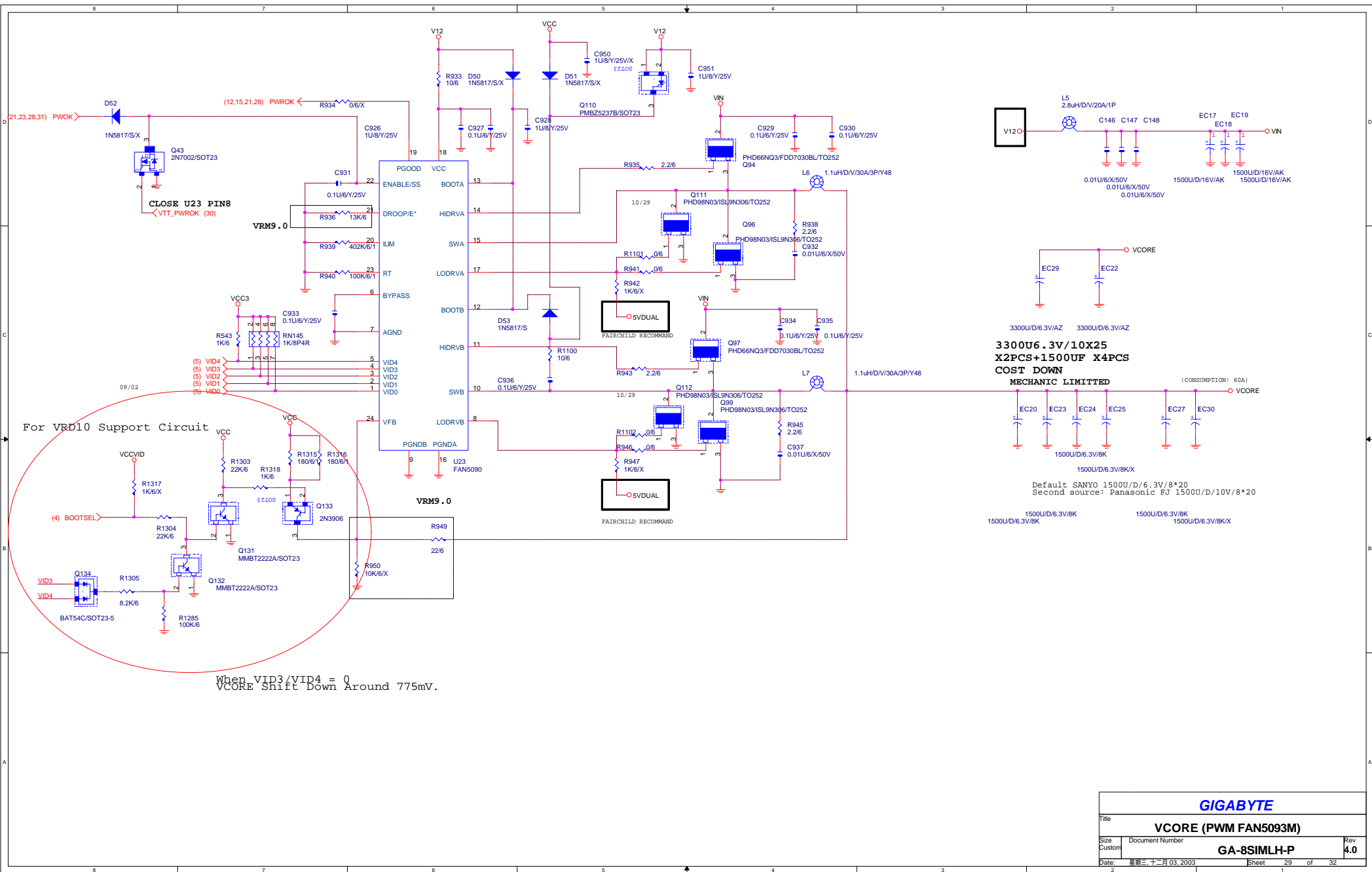


SYSTEM FAN W=0.167W



POWER FAN W=0.167W

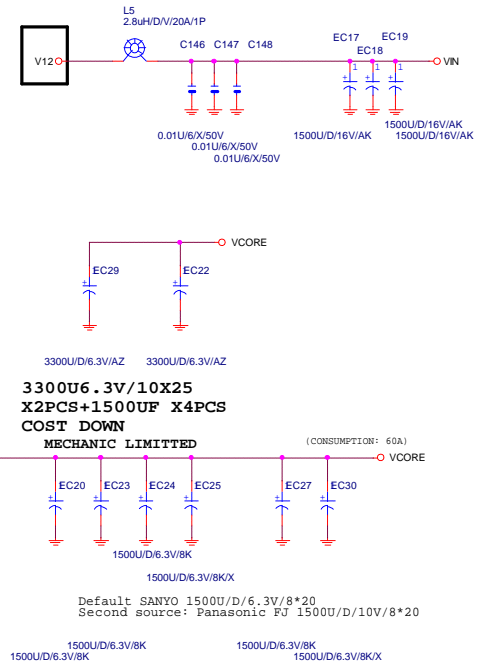




For VRD10 Support Circuit

(4) BOOTSEL

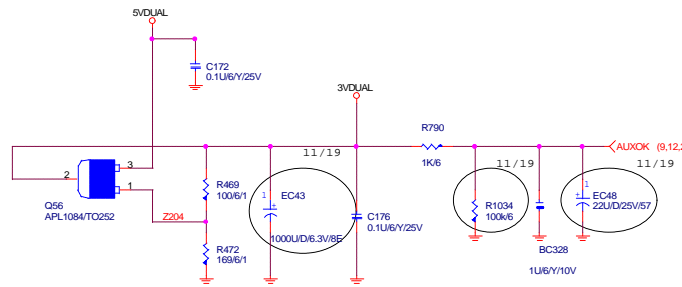
When VID3/VID4 = 0
Vcore Shift Down Around 775mV.



GIGABYTE		
Title Vcore (PWM FAN5093M)		
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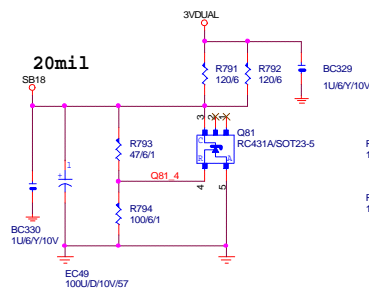
5VDUAL TRANS TO 3VDUAL(3.3V)

5VDUAL 80 mils ABOVE

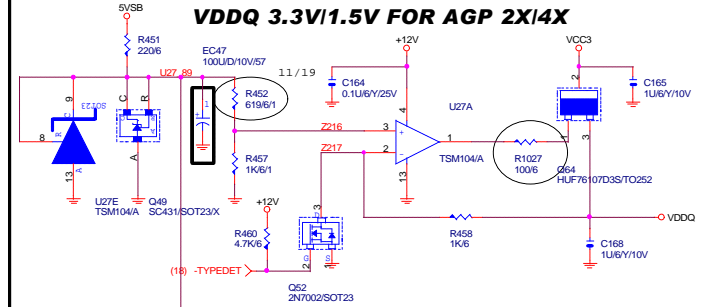


SB18 FOR SB

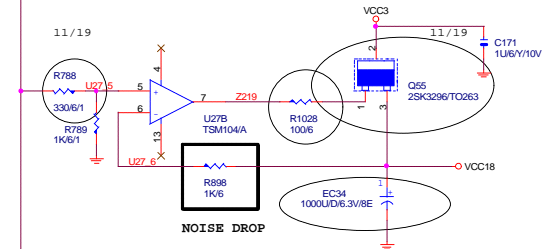
20mil



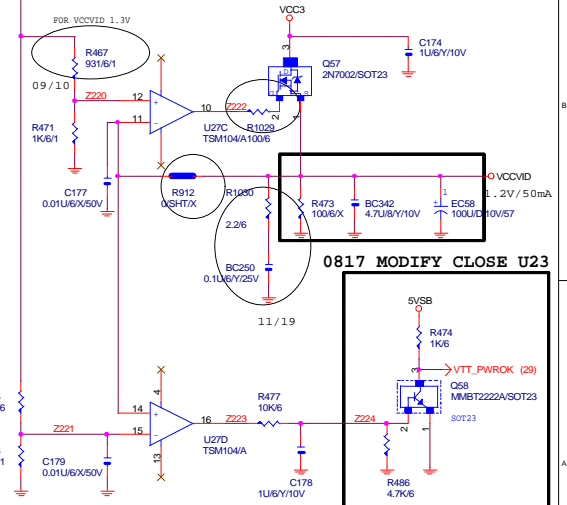
VDDQ 3.3V/1.5V FOR AGP 2X/4X



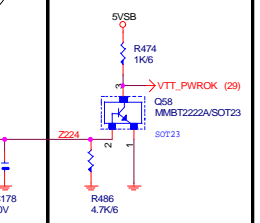
VCC18 FOR NB,SB



VCCVID FOR NORTHWOOD CPU



0817 MODIFY CLOSE U23



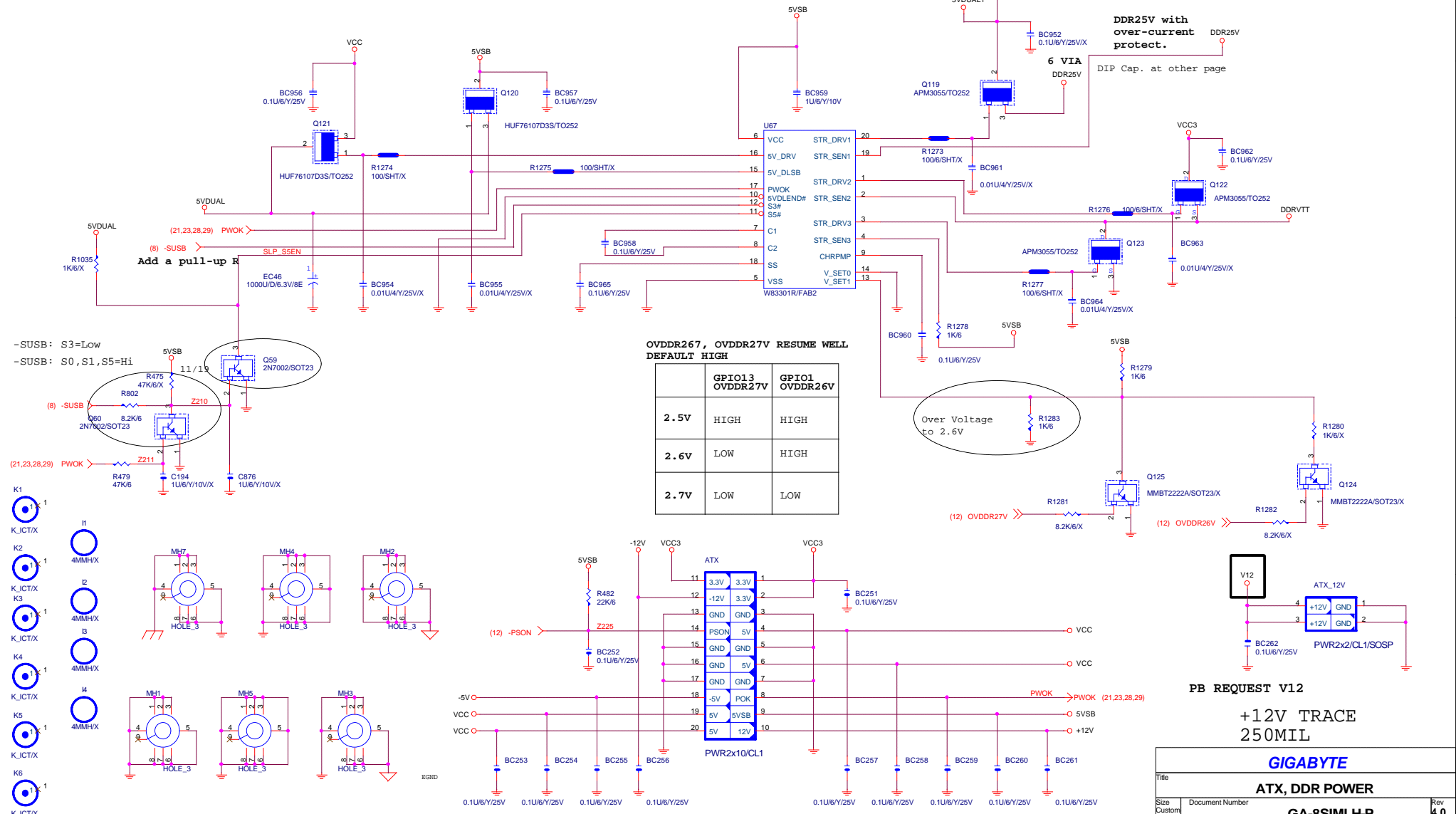
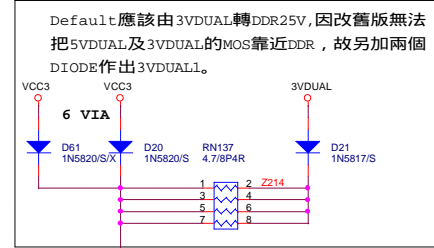
GIGABYTE

DC POWER

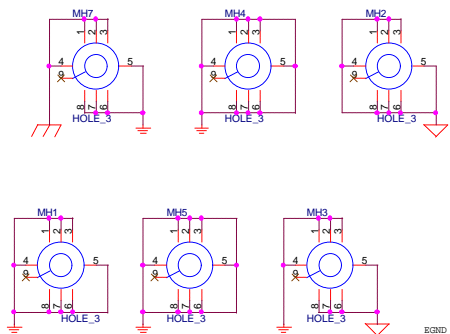
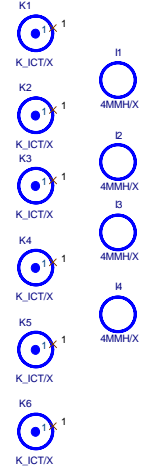
Title		
DC POWER		
Size	Document Number	Rev
Custom	GA-8SIMLH-P	4.0
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ATX CON, DDR POWER

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-SUSB: S3=Low
-SUSB: S0, S1, S5=Hi



ATX POWER CONNECTOR

PB REQUEST V12

+12V TRACE 250MIL

GIGABYTE

ATX, DDR POWER

GA-8SIMLHP

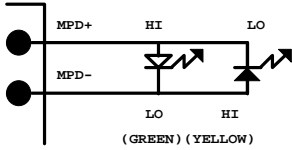
Rev 4.0

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LO:Normal

RTL8100L ON-BOARD			
-REQ0	PCI1	IDSEL(A20)--B	
-REQ1	PCI2	IDSEL(A22)--C	
-REQ2	PCI3	IDSEL(A24)--D	
-REQ3	RTL8100L	IDSEL(A27)--B	

8SRXL South Bridge GPIO LIST					
ITEM	DESCRIPTION	I/O	STATUS	Default	
GPIO0	Bios Write Protect	O	Hi:Write Enable, Lo:Write Protect	Hi	
GPIO1	N/A		PULL-UP	Hi	
GPIO2	THERM#			Hi	
GPIO3	Green Button	O	Hi:Normal, Lo:Into Green mode	Hi	
GPIO4	CLKRUN#		PULL-DOWN	Lo	
GPIO5	N/A		PULL-UP	Hi	
GPIO6	DDR OVER VOLTAGE	O		Hi	
GPIO7	SUSLED	O	AS LIKE DEFINED...	Lo	
GPIO8	Wake On Ring	I	Hi:Normal, Lo:Ring Power On	Hi	
GPIO9	GLED	I	AS LIKE DEFINED...	Lo	
GPIO10	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo	
GPIO11	N/A		PULL-UP	Hi	
GPIO12	N/A		PULL-UP	Hi	
GPIO13	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo	
GPIO14	DDR OVER VOLTAGE	I		Lo	
GPIO15	KB Data	I/OD			
GPIO16	KB Clk	I/OD			
GPIO17	MS Data	I/OD			
GPIO18	MS Clk	I/OD			



States for a single-color power LED

LED States	ACPI States	MPD+	MPD-	BIOS	
				GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING

States for a dual-color power LED

LED States	ACPI States	MPD+	MPD-	BIOS	
				GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING
Steady Yellow	S1,S3	LO	HI	HI	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING	HI	BLINKING

States for green LED

LED States	ACPI States	GLED-	BIOS
			GPIO9
ON	S1,S3	HI	HI
OFF	S0,S5	LO	LO

BIOS REQUEST

SINGLE	DUAL	INTEL LED DEFINED				GIGABYTE LED DEFINED				SINGLE	DUAL
		GPIO7	ACPILED	GPIO9		GPIO7	ACPILED	GPIO9			
GREEN	GREEN	S0	LO	LO	LO	S0	LO	LO	LO	GREEN	GREEN
OFF	YELLOW	S1	HI	HI	HI	S1	LO	BLINKING	HI	G(BLINK)	G(BLINK)
OFF	YELLOW	S3	HI	HI	HI	S3	HI	HI	HI	OFF	YELLOW
OFF	OFF	S4/S5	LO	HI/NC	LO	S4/S5	LO	HI/NC	LO	OFF	OFF

GIGABYTE

Title			
GPIO, REQ/GNT Table			
Size Custom	Document Number	GA-8SIMLH-P	Rev 4.0
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