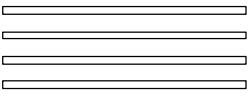


# 8SIMLH Schematics

Revision 3.02

SHEET	TITLE
1	COVER SHEET
2	BOM & PCB MODIFY HISTORY
3	BLOCK DIAGRAM
4,5,6	INTEL CPU_WMT_478
7-10	SIS651/645DX (NORTH BRIDGE) HOST; DDR; AGP,HYPER ZIP
11-14	962 (SOUTH BRIDGE)
15	CKG(ICS952004) + CKBF (ICS93722)
16,17	DDR SDRAM DIMMS 1,2 & DDR TERMINATION
18	AGP SLOT
19	VGA Connector
20	PCI SLOT 1-3
21	IDE,USB
22	Winbond W83697HF
23	BIOS
24	COM,PRT,FDD,KB/MS,IR
25	CNR SLOT
26	AUDIO AC 97 CODEC
27	AUDIO JACK,GAME PORT
28	RTL8100B & USB CONNECTOR
29	PANEL,STR LED,FANS ,CPU GN
30	VCORE PHASE PWM HIP 6301 + 6601
31	ALL POWER CIRCUIT
32	ATX & ATX12V CONN
33	GPIO Connection
34	TEST POINT

		COMPONENT SIDE (1 oz. Copper) GND SIDE (1 oz. Copper) VCC SIDE (1 oz. Copper) SOLDER SIDE (1 oz. Copper)
<b>GIGABYTE</b>		
Title <b>COVER SHEET</b>		
Size Custom	Document Number <b>GA-8SIMLH</b>	Rev <b>3.02</b>
Date: Monday, January 13, 2008		Sheet 1 of 32

# Model Name: 8SIMLH

Version:3.02

## Component value change history

AUTOBOM  
2002/06/04

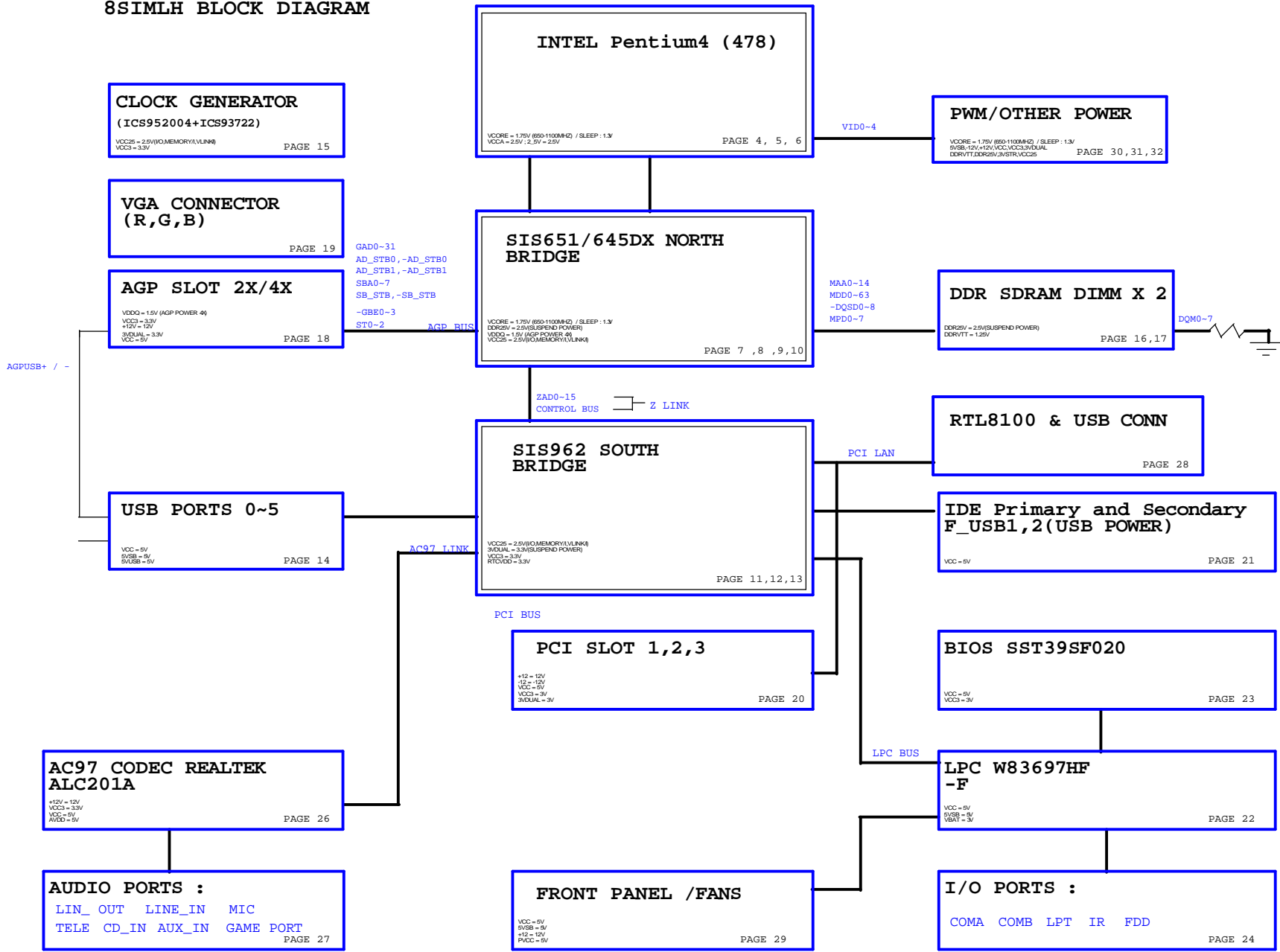
Date	Change Item	Reason
02/04	LAYOUT PLACEMENT	DEL 1394 CONNECTOR(LAYOUT ISSUE) SWAP NET
02/05	LAYOUT LIB	COIL-8P---->COIL-8P_SHORT
02/06	VGA/COM DUAL LAYOUT	
	DDRVTT (R&D 109)	DDRVTT DECOUPLING X14 PCS (0.1U/8P4C CAP)
02/06-1	LAYOUT LIB MODIFY	USB2.0 CHOKE (NO SHORT) AGP SLOT-->AGP_N
02/19	NET SWAP	BC345-->SC60 (COMP-->SOLDER SIDE)
02/20	EMI ISSUE	CLOSE U16(75232) -NTXD2 ADD CAP 180P/6(BC349)
02/21	LAYOUT ISSUE	BC344-->SC61 (COMP-->SOLDER SIDE) SWAP NET
	LIB MODIFY	MOSFET LIB TO263,252 CO LAYOUT(Q_TO263-252)
04/22	BOM MODIFY	AC97 CODEC ---->ALC650
	PCB REV1.9	PWM 2 PHASE FAN5093M/C(VOCRE CAP COST DOWN) INTEL F_PANEL+F_USB1,2,F_AUDIO DDRVTT CAP 0.1U/8P4C X9PCS
04/23	PCB MODIFY	reduced PCB size(COST DOWN)
04/29		DEL MH6,ADD CAP MIC FOR EMI
05/08	PCB MODIFY	rename to GA-8SIMLH
	BOM MODIFY	SIS651+SIS962
05/13	BOM MODIFY	cost down CAP & FB ALC650 change to ST9721
05/21	PCB MODIFY	DEL BC218 ,ADD R1011 FOR F_MIC TEXT MODIFY
	BOM MODIFY	PCB CHANGE TO REV:2.0 1
06/04	BOM MODIFY	R867 10k/6 change to 470/6 R921 324/1/6 change to 487/1/6 ADD CN14,15,16,17 180P/8P4C ADD C944,C65 180P/N/50V/6
08/04	BOM MODIFY	IDE ,PANEL,USB FDD,SMBUS,22U TO 100U

## Circuit or PCB layout change for next version

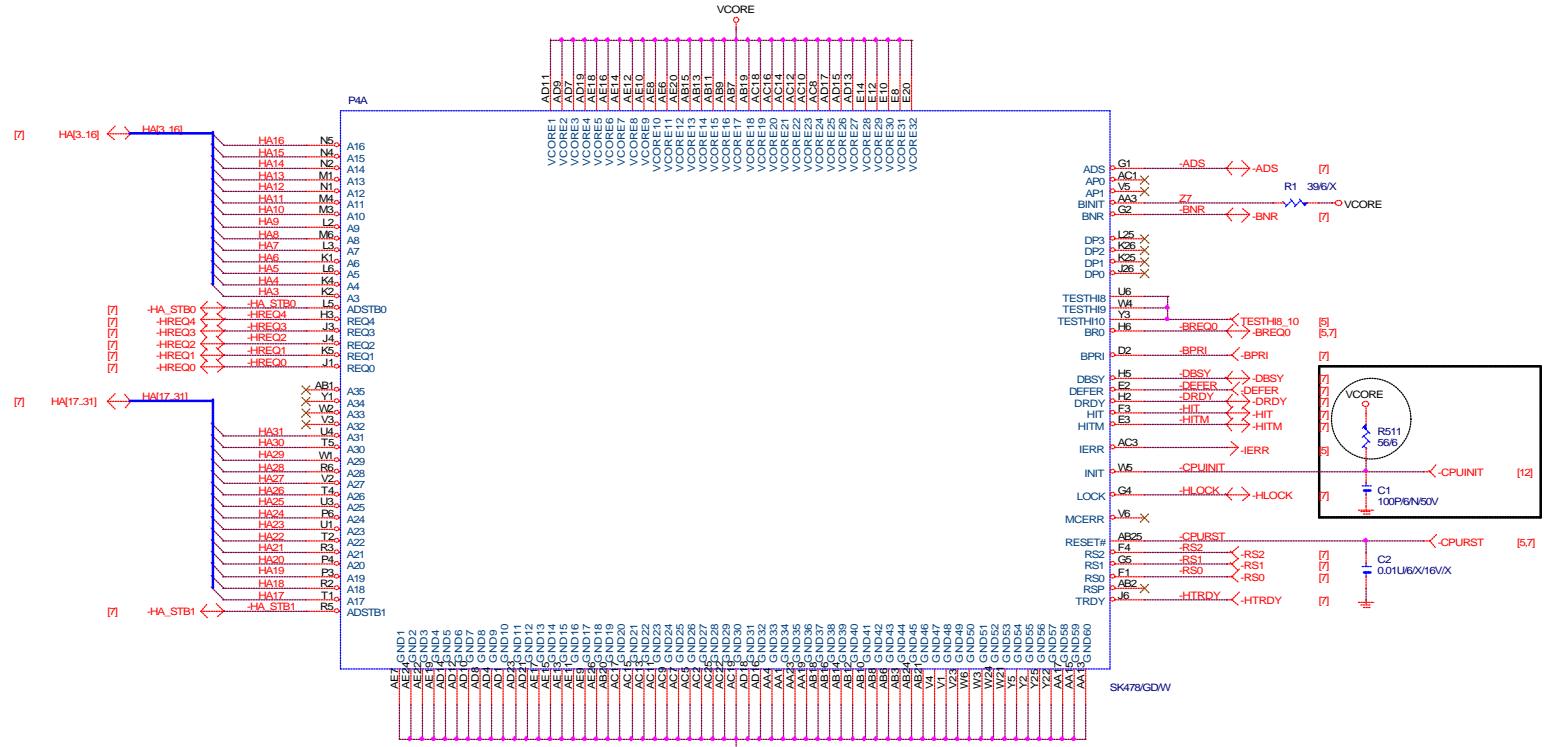
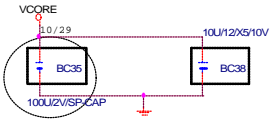
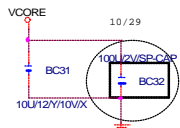
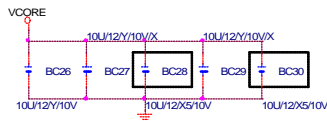
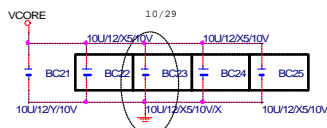
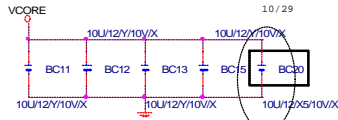
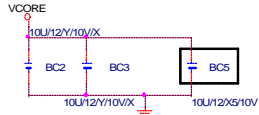
Date	Change Item	Reason
08/06	BOM MODIFY	U39 change to SIS962L REV:A2
08/12	BOM MODIFY	DEL R948 1K/6 ADD R950 470/6 R949 10/6 change to 22/6
08/13	BOM MODIFY	EC1,2,3,5,34,40,46 330U/25V change to 1200U/6.3V EC54 22U change to 100U
	BOM MODIFY	R939 200K/6 change to 240K/6 ST9721 change to ALC101
	PCB MODIFY	REV:2.01 CHANGE TO2.1
09/12	BOM MODIFY	EC37 100U change to 22U
10/14	BOM MODIFY	R935,R943 2.2 ohm Change to 4.7 ohm
10/28	BOM MODIFY	U12 ADD W83697HF/UB FOR MEMO change
11/15	PCB MODIFY	PCB size ADD 0.5 cm(SPEC change)
12/09	PCB MODIFY	PCB text modify
12/09	BOM MODIFY	DEL BC20,23 ADD BC21,BC26 10U/12 C110,C111 ADD 1K ohm C182 add 150 ohm R8 75/6/1 change to 100/6/1 PCB change to REV:3.01
12/26	PCB MODIFY	ADD HT SUPPORT REV:3.02

<b>GIGABYTE</b>		
Title <b>BOM &amp; PCB MODIFY HISTORY</b>		
Size Custom	Document Number	Rev
	<b>GA-8SIMLH</b>	<b>3.02</b>
Date: Monday, January 13, 2003	Sheet	2 of 32

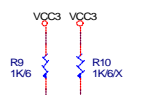
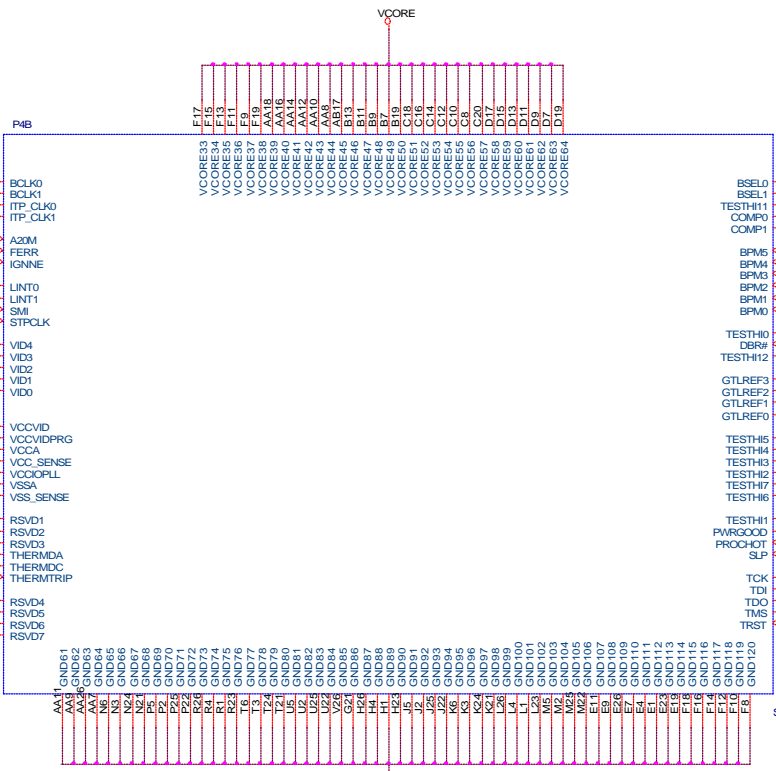
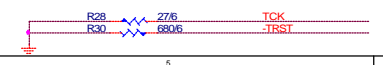
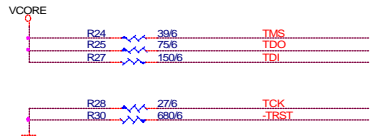
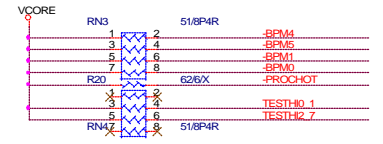
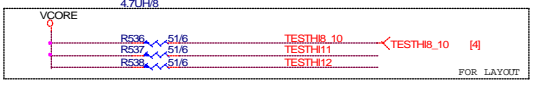
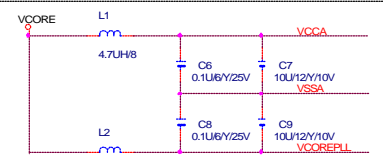
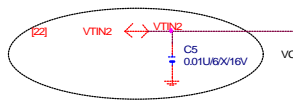
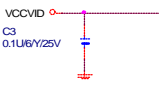
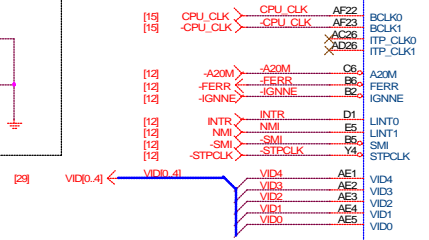
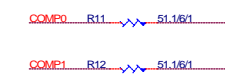
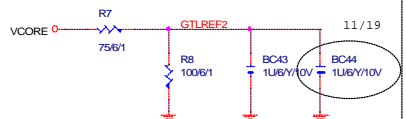
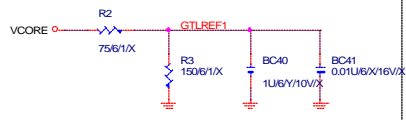
8SIMLH BLOCK DIAGRAM



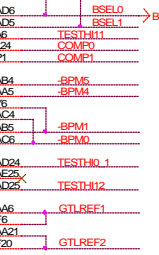
(X5R) X11 1206(10U) NOTE-GIGA



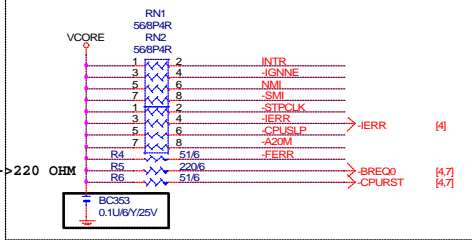
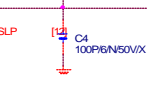
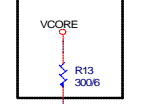
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Title <b>WILLIAMATE 478A</b>		
Size Custom	Document Number <b>GA-8SIMLH</b>	Rev <b>3.02</b>
Date Monday, January 13, 2003	Sheet 4 of 32	



BSELO ---->100/133



SIS REQUEST



<b>GIGABYTE</b>		
<b>WILLIAMATE 478B</b>		
Title		
Size	Document Number	Rev
Custom	<b>GA-8SIMLH</b>	<b>3.02</b>
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DB[0..3] <-> DB[0..3] [6]  
 HD[0..63] <-> HD[0..63] [6]  
 HA[3..31] <-> HA[3..31] [4]  
 GD[0..31] <-> GD[0..31] [18]  
 SBA[0..7] <-> SBA[0..7] [18]  
 ST[0..2] <-> ST[0..2] [18]

[15] HCLK -HCLK AJ26 CPUCCLK  
 [15] -HCLK -HCLK AH26 CPUCCLK#  
 [4] -HLOCK -HLOCK U24 HLOCK#  
 [4] -DEFER -DEFER U26 DEFER#  
 [4] -HTRDY -HTRDY V28 HTRDY#  
 [4,5] -CPURST -CPURST C20 CPURST#  
 [5] CPUPWOK CPUPWOK D19 CPUPWOK#  
 [4] -BPR1 -BPR1 T27 BPR1#  
 [4,5] -BREQ0 -BREQ0 U25 BREQ0#  
 [4] -RS2 -RS2 T24 RS2#  
 [4] -RS1 -RS1 T26 RS1#  
 [4] -RS0 -RS0 U29 RS0#  
 [4] -ADS -ADS V28 ADS#  
 [4] -HITM -HITM U28 HITM#  
 [4] -HIT -HIT# HIT#  
 [4] -DRDY -DRDY W26 DRDY#  
 [4] -DBSY -DBSY V24 DBSY#  
 [4] -BNR -BNR V27 BNR#  
 [4] -HREQ4 -HREQ4 W28 HREQ#4  
 [4] -HREQ3 -HREQ3 W29 HREQ#3  
 [4] -HREQ2 -HREQ2 W24 HREQ#2  
 [4] -HREQ1 -HREQ1 W25 HREQ#1  
 [4] -HREQ0 -HREQ0 Y27 HREQ#0  
 [4] -HA\_STB1 -HA\_STB1 AD24 HASTB#1  
 [4] -HA\_STB0 -HA\_STB0 AA24 HASTB#0

HA31 AF26 HA#31  
 HA30 AE25 HA#30  
 HA29 AH28 HA#29  
 HA28 AD26 HA#28  
 HA27 AG29 HA#27  
 HA26 AE26 HA#26  
 HA25 AF28 HA#25  
 HA24 AC24 HA#24  
 HA23 AG28 HA#23  
 HA22 AE29 HA#22  
 HA21 AD28 HA#21  
 HA20 AC25 HA#20  
 HA19 AD27 HA#19  
 HA18 AE26 HA#18  
 HA17 AF27 HA#17  
 HA16 AB24 HA#16  
 HA15 AB26 HA#15  
 HA14 AC28 HA#14  
 HA13 AC26 HA#13  
 HA12 AC29 HA#12  
 HA11 AA26 HA#11  
 HA10 AB28 HA#10  
 HA9 AB27 HA#9  
 HA8 AA25 HA#8  
 HA7 AA29 HA#7  
 HA6 AA28 HA#6  
 HA5 Y26 HA#5  
 HA4 Y24 HA#4  
 HA3 Y28 HA#3

AH5 C1XAVSS  
 AH6 C1XAVDD  
 AH7 C1XAVDD  
 CA1XAVSS  
 CA2XAVSS  
 CA3XAVDD  
 CA4XAVDD  
 U1 HVREF  
 U2 HVREF1  
 U3 HVREF2  
 U4 HVREF3  
 U5 HVREF4

B0 HPCOMP  
 B1 HPCOMP  
 B2 HPCOMP  
 B3 HPCOMP  
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 B5 HPCOMP  
 B6 HPCOMP  
 B7 HPCOMP  
 B8 HPCOMP  
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 B10 HPCOMP  
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 B20 HPCOMP

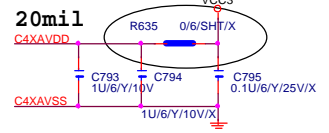
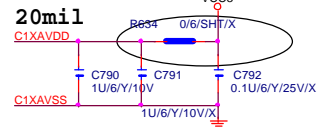
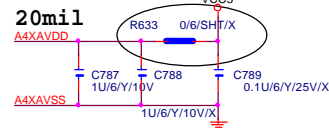
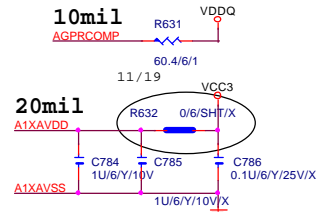
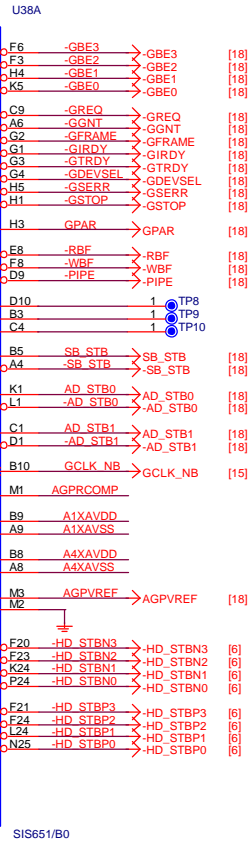
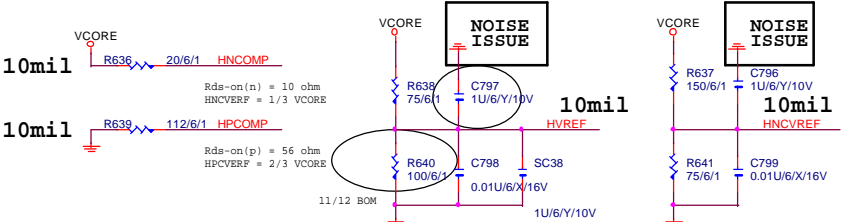
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 ST100 ST100

AGP

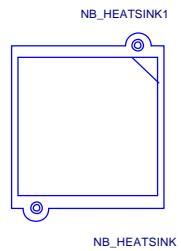
651/645DX-1

HOST

HD#63 HD#63  
 HD#62 HD#62  
 HD#61 HD#61  
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 HD#0 HD#0



N.B HEATSINK



<b>GIGABYTE</b>		
<b>SIS651/645DX(HOST/AGP)</b>		
Title	Document Number	Rev
	<b>GA-8SIMLH</b>	<b>3.02</b>
Date:	Monday, January 13, 2003	Sheet 7 of 32

place this capacitor under 650 solder side

MDDI[0:63] ↔ MDD[0:63] [16,17]  
 DQM[0..7] → DQM[0..7] [16,17]  
 MAA[0..14] → MAA[0..14] [16,17]  
 -CS[0..3] → -CS[0..3] [16,17]  
 CKE[0..5] → CKE[0..5] [16]  
 -DQSDI[0..7] → -DQSD[0..7] [16,17]

11/19  
short pad

# DDR MD DAMPING

Near DIMM 1

11/19  
short pad

MDDI[0:63] ↔ MDD[0:63] [16,17]

U38R

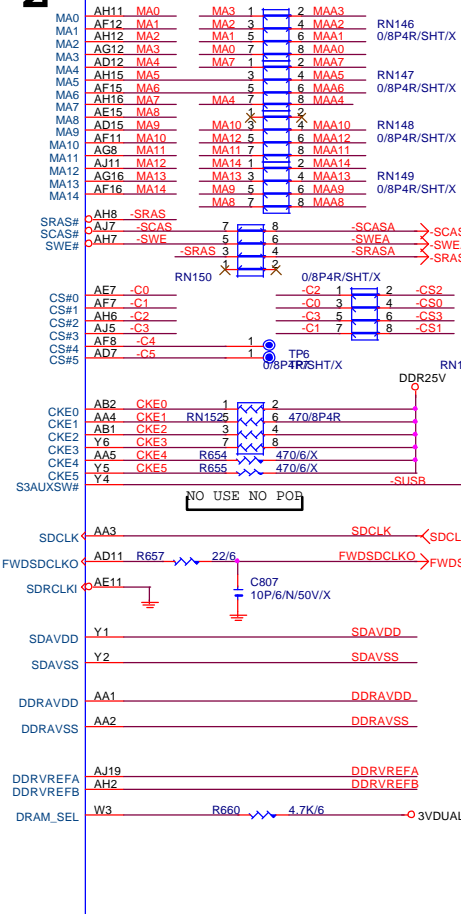
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MD2	AH21	MD2
MD3	AJ21	MD3
MD4	AD23	MD4
MD5	AE23	MD5
MD6	AF22	MD6
MD7	AF21	MD7
DCMD0	AD22	MD7
DQS0	AH22	DQM0
MD8	AD21	DQS0/CSB#0
MD9	AG20	MD8
MD10	AE19	MD9
MD11	AF19	MD10
MD12	AE21	MD11
MD13	AD20	MD12
MD14	AD19	MD13
MD15	AH19	MD14
DCMD1	AF20	MD15
DQS1	AH20	DQM1
MD16	AF18	DQS1/CSB#1
MD17	AG18	MD16
MD18	AH17	MD17
MD19	AD16	MD18
MD20	AD18	MD19
MD21	AD17	MD20
MD22	AF17	MD21
MD23	AJ17	MD22
DCMD2	AE17	MD23
DQS2	AH18	DQM2
MD24	AD14	DQS2/CSB#2
MD25	AG14	MD24
MD26	AJ13	MD25
MD27	AE13	MD26
MD28	AJ15	MD27
MD29	AF14	MD28
MD30	AD13	MD29
MD31	AF13	MD30
DCMD3	AH13	MD31
DQS3	AH14	DQM3
MD32	AD10	DQS3/CSB#3
MD33	AH10	MD32
MD34	AE9	MD33
MD35	AD8	MD34
MD36	AG10	MD35
MD37	AF10	MD36
MD38	AH9	MD37
MD39	AF9	MD38
DCMD4	AD9	MD39
DQS4	AJ9	DQM4
MD40	AH5	DQS4/CSB#4
MD41	AG4	MD40
MD42	AE5	MD41
MD43	AH3	MD42
MD44	AG6	MD43
MD45	AF6	MD44
MD46	AF5	MD45
MD47	AF4	MD46
DCMD5	AH4	MD47
DQS5	AJ3	DQM5
MD48	AE4	DQS5/CSB#5
MD49	AD6	MD48
MD50	AE2	MD49
MD51	AC5	MD50
MD52	AG2	MD51
MD53	AG1	MD52
MD54	AF3	MD53
MD55	AC6	MD54
DCMD6	AD4	MD55
DQS6	AF2	DQM6
MD56	AB6	DQS6/CSB#6
MD57	AD3	MD56
MD58	AA6	MD57
MD59	AB3	MD58
MD60	AC4	MD59
MD61	AE1	MD60
MD62	AD2	MD61
MD63	AC1	MD62
DCMD7	AB4	MD63
DQS7	AC2	DQM7
		DQS7/CSB#7

SIS651/B0

## 651 645DX-2

11/19  
short pad

REV 0.2



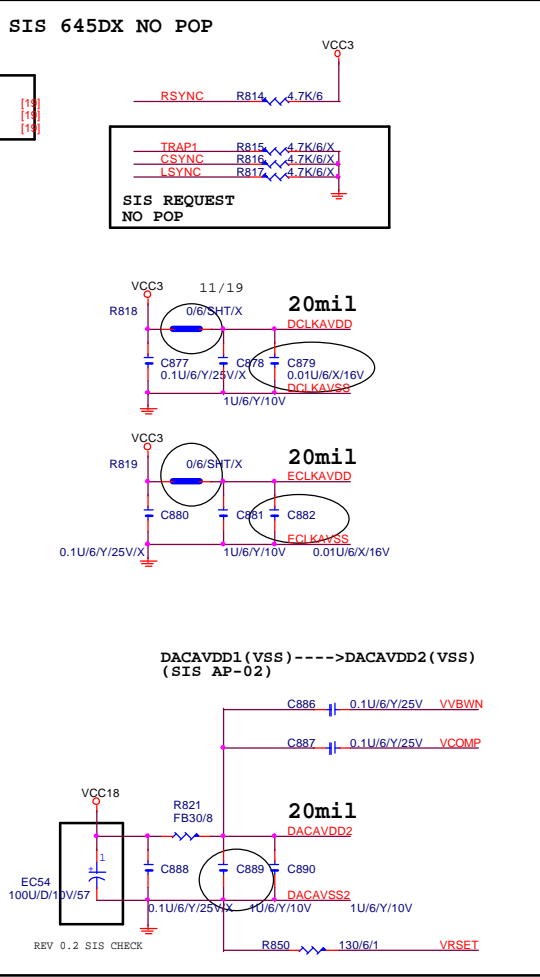
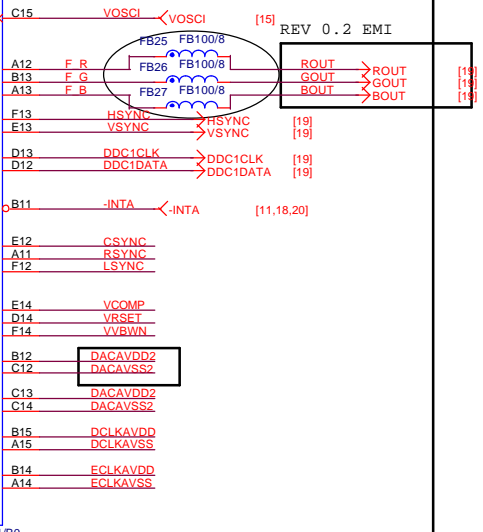
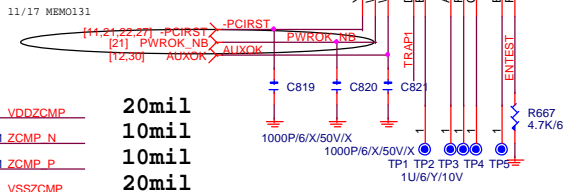
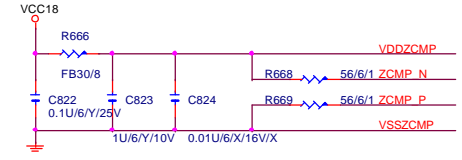
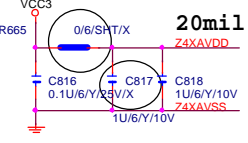
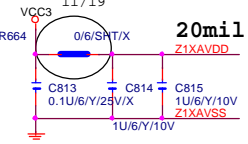
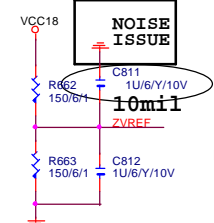
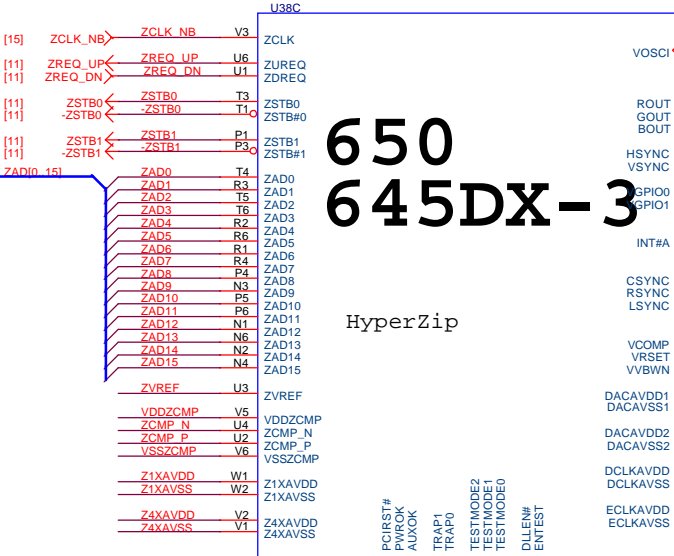
NOTE: This page is for universal PCB design( suitable for both 645 or 650)

NB Hardware Trap Table			
DLE#	0	1	Default
enable PLL	enable PLL	disable PLL	0
DRAM SET	SDR	DDR	1 (DDR)
TRAP0	normal	NB debug mode	0
TRAP1	TV selection, NTSC/PAL(0/1)		0
CSYNC	enable VB		0
RSYNC	enable VGA interrupt		1
LSYNC	enable panel link		0

embedded pull-low (30~50K Ohm)  
yes  
yes  
yes

# 650 645DX-3

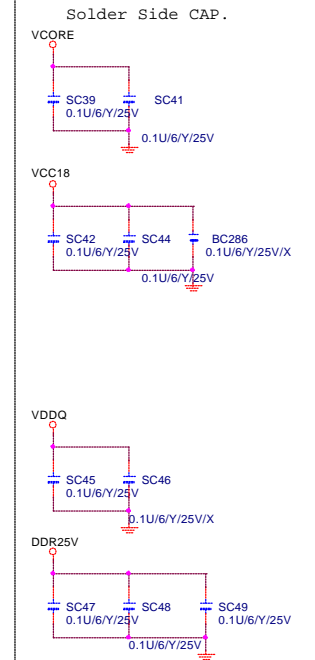
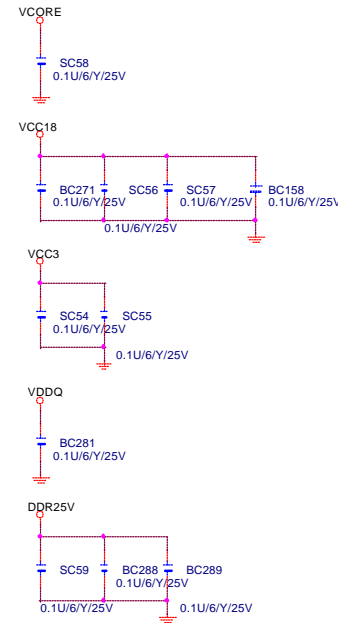
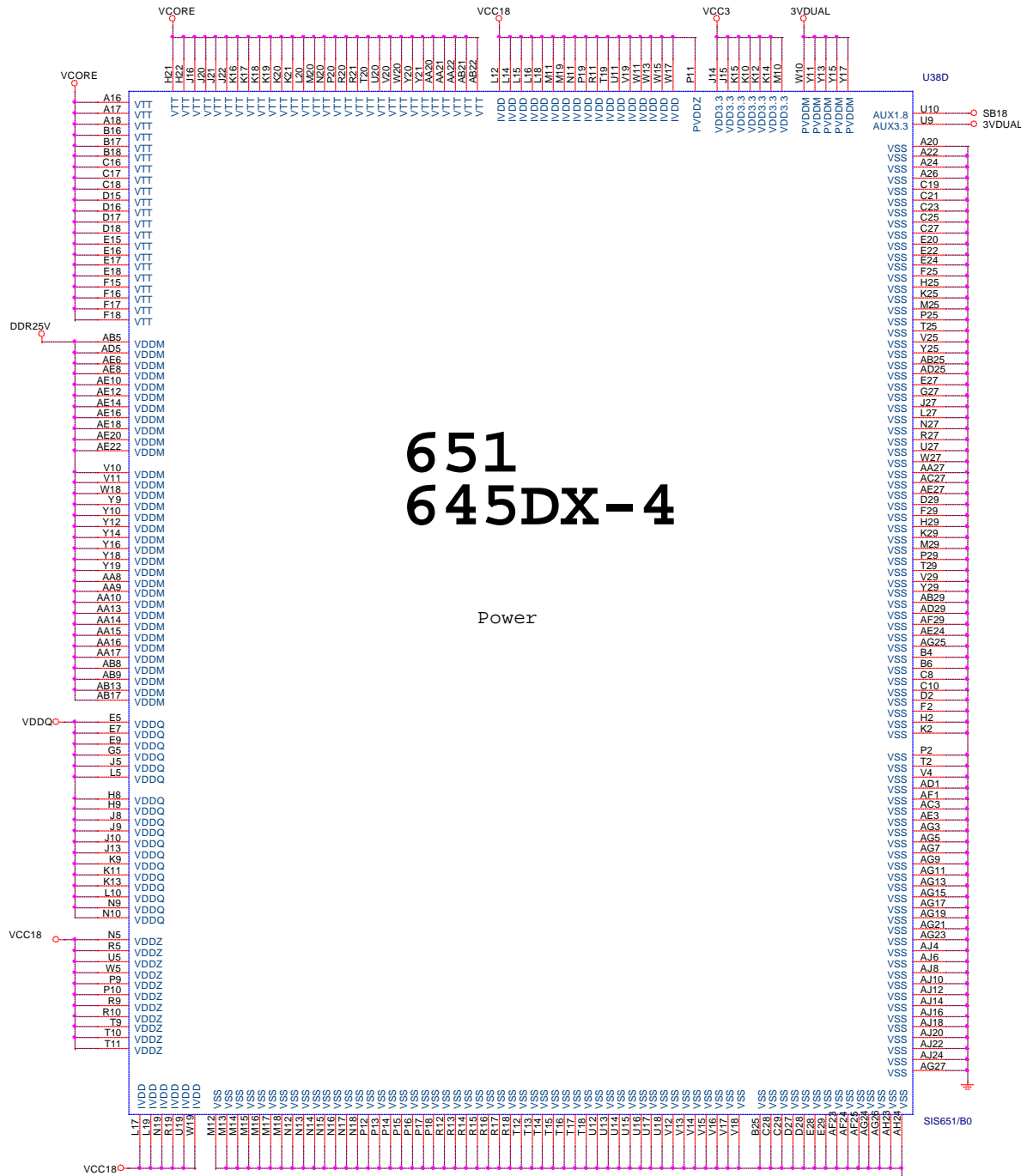
HyperZip



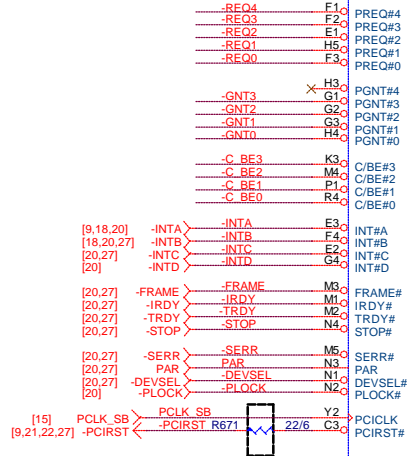
<b>GIGABYTE</b>		
Title <b>SIS651/645DX(HYPER ZIP)</b>		
Size Custom	Document Number <b>GA-8SIMLH</b>	Rev <b>3.02</b>
Date: Monday, January 13, 2003	Sheet 9	of 32

# 651 645DX-4

Power



<b>GIGABYTE</b>		
Title <b>SIS651/645DX(PWR)</b>		
Size Custom	Document Number <b>GA-8SIMLH</b>	Rev <b>3.02</b>
Date: Monday, January 13, 2003	Sheet 10 of 32	

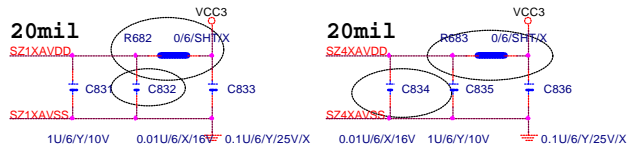
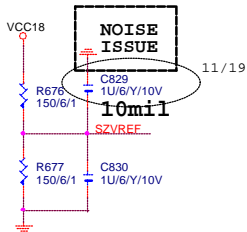
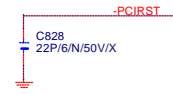
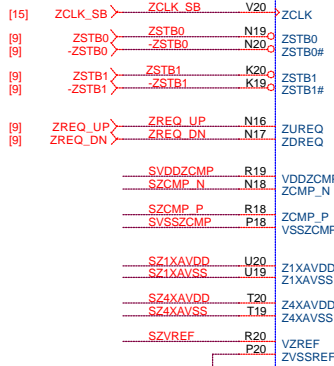


PCI

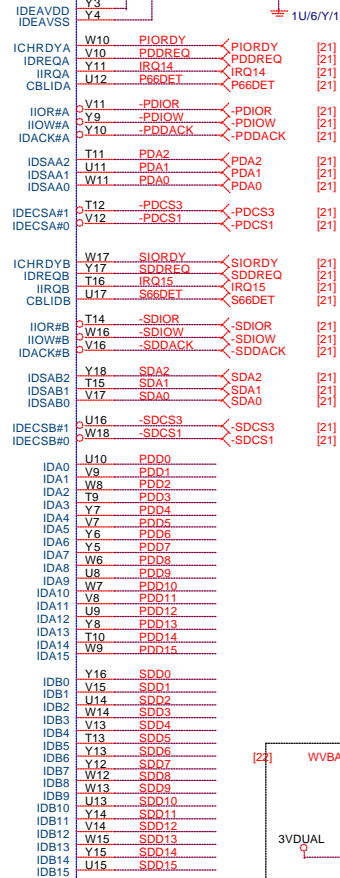
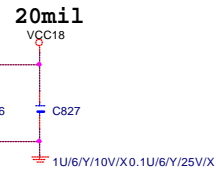
IDE

# 962/961B

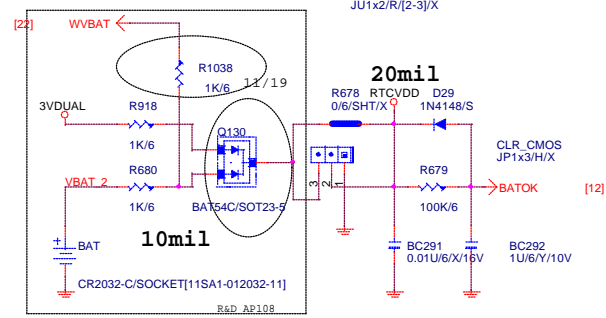
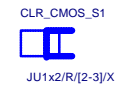
HyperZip



Analog Power supplies of Transzip function for 96X Chip.



CLR_CMOS	CLEAR COMS JUMPER
1-2	Enable
2-3	Normal (Default)



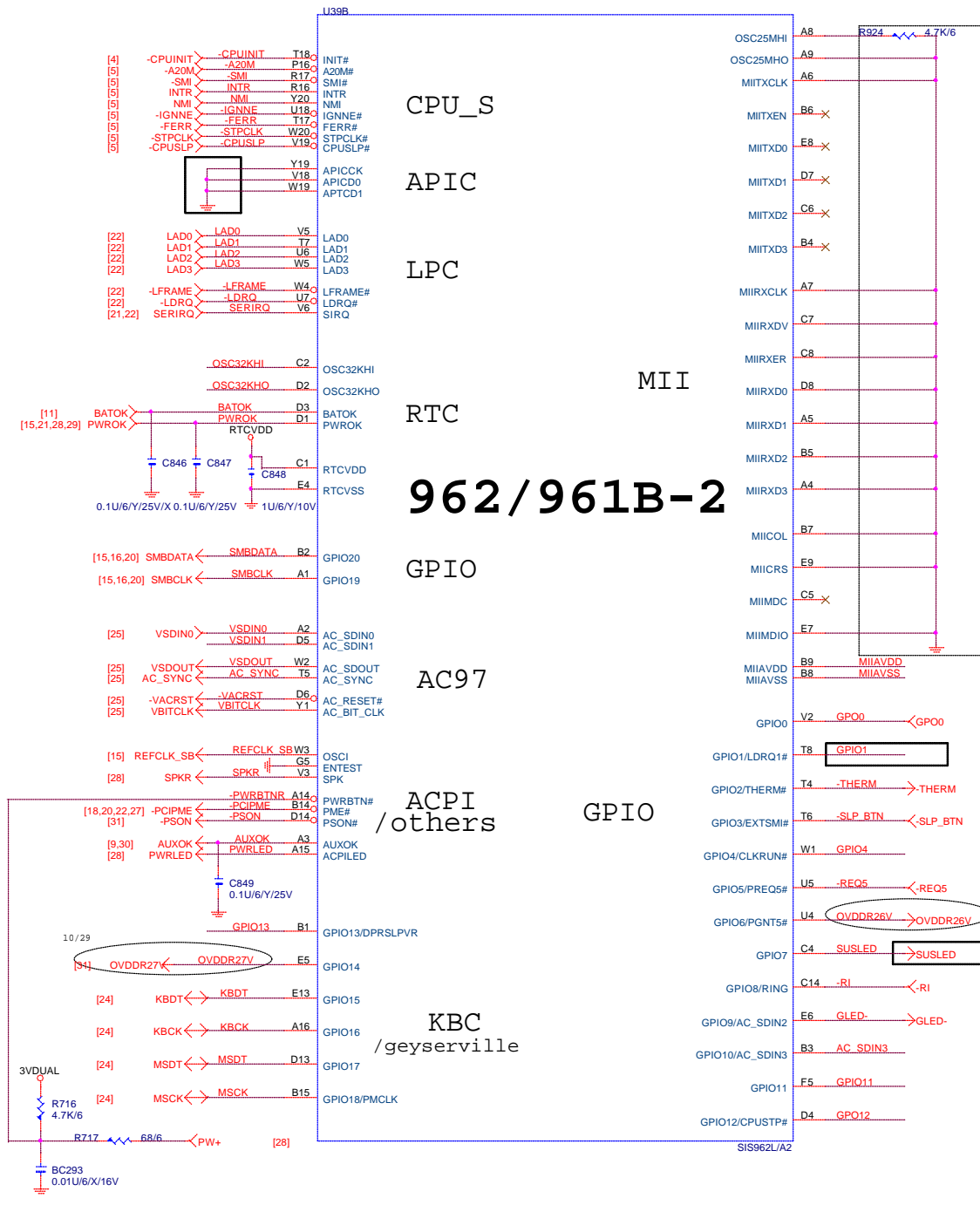
NF REQUEST CLR\_CMOS

**GIGABYTE**

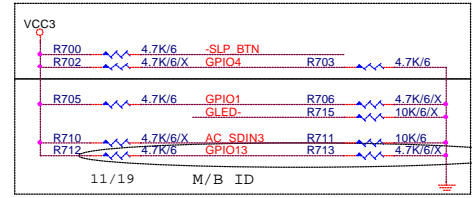
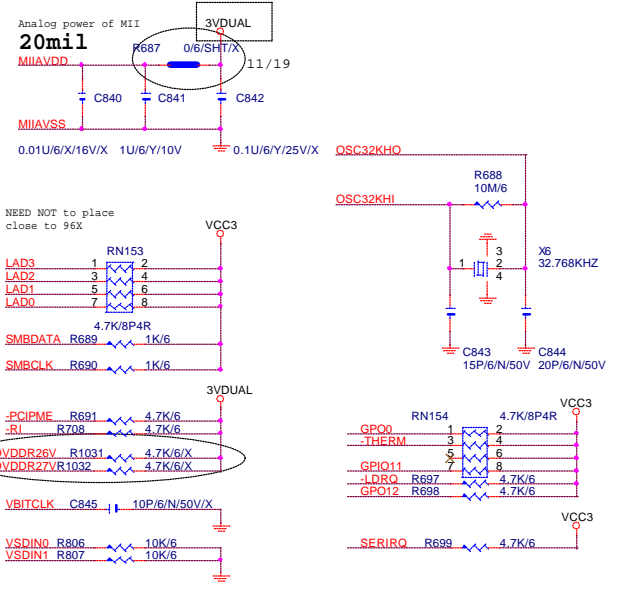
Title: **SIS962(HP ZIP,PCI,IDE)**

Size: Custom Document Number: **GA-8SIMLH** Rev: **3.02**

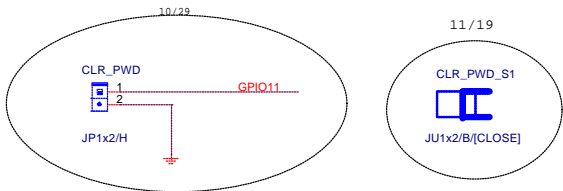
Date: Monday, January 13, 2003 Sheet 11 of 32

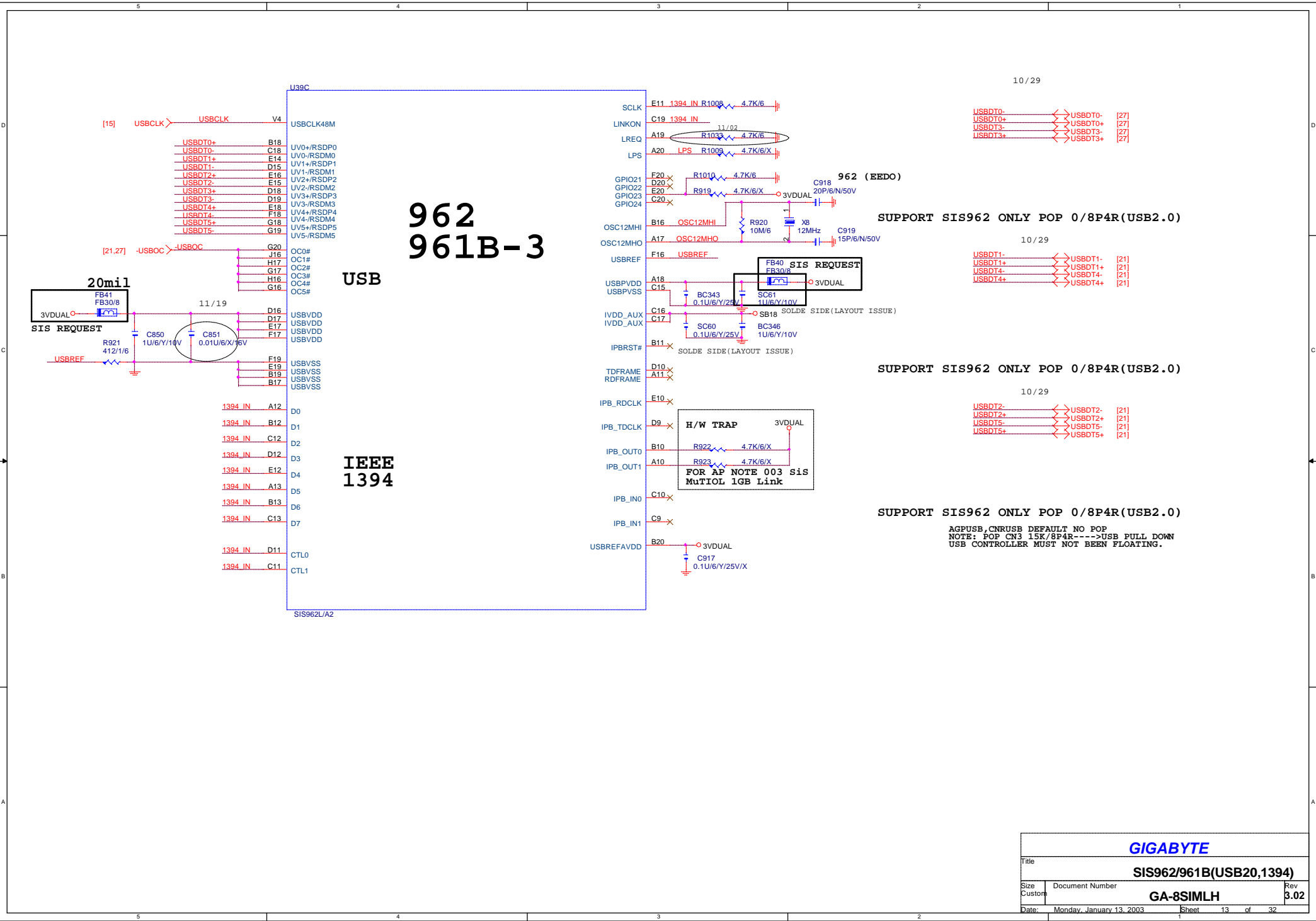


If MII interface don't use, Input pin tie to GND. Output pin is NC.

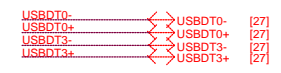


INPUT	REV: 2.0 / 2.1	REV: 3.0
GPIO1	HI	HI
GPIO4	LOW	LOW
GPIO13	LOW	HI





10/29

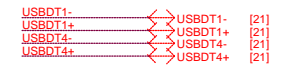


**962  
961B-3**

**USB**

**SUPPORT SIS962 ONLY POP 0/8P4R(USB2.0)**

10/29



**IEEE  
1394**

**SUPPORT SIS962 ONLY POP 0/8P4R(USB2.0)**

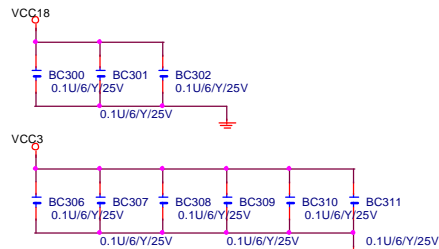
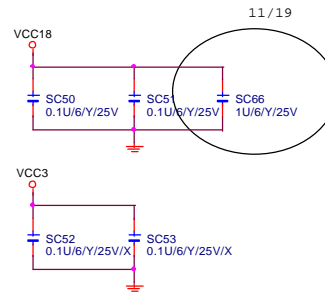
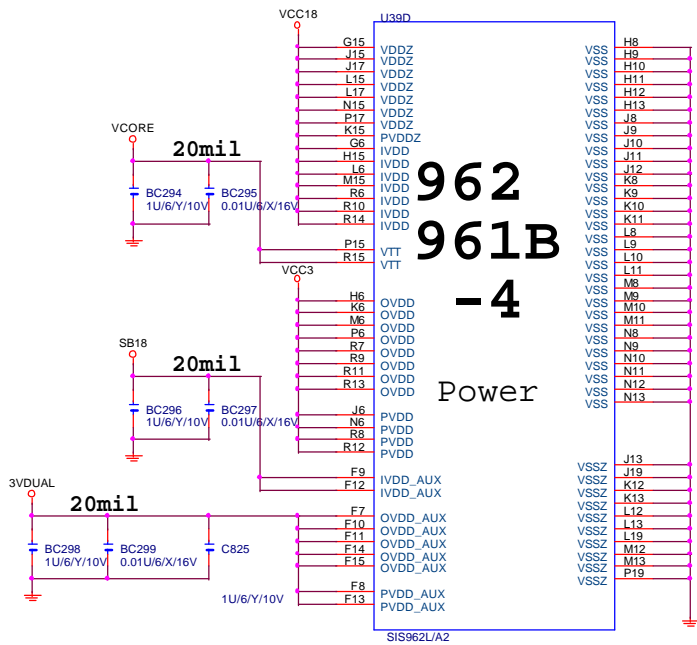
10/29



**SUPPORT SIS962 ONLY POP 0/8P4R(USB2.0)**

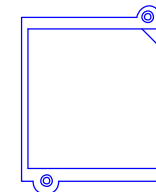
AGPUSB,CNRUSB DEFAULT NO POP  
NOTE: POP CN3 15K/8P4R--->USB PULL DOWN  
USB CONTROLLER MUST NOT BEEN FLOATING.

<b>GIGABYTE</b>		
Title <b>SIS962/961B(USB20,1394)</b>		
Size Custom	Document Number <b>GA-8SIMLH</b>	Rev <b>3.02</b>
Date:	Monday, January 13, 2003	Sheet 13 of 32



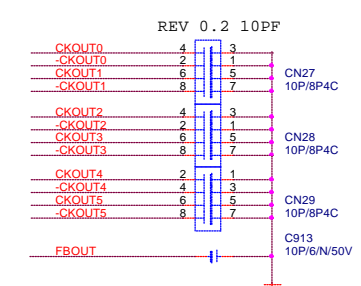
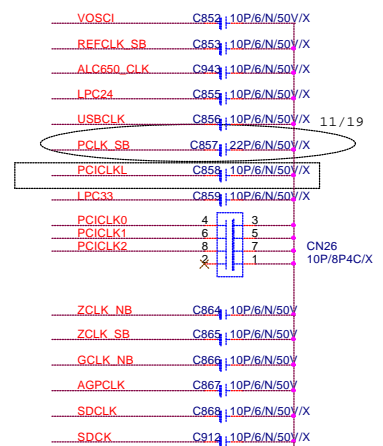
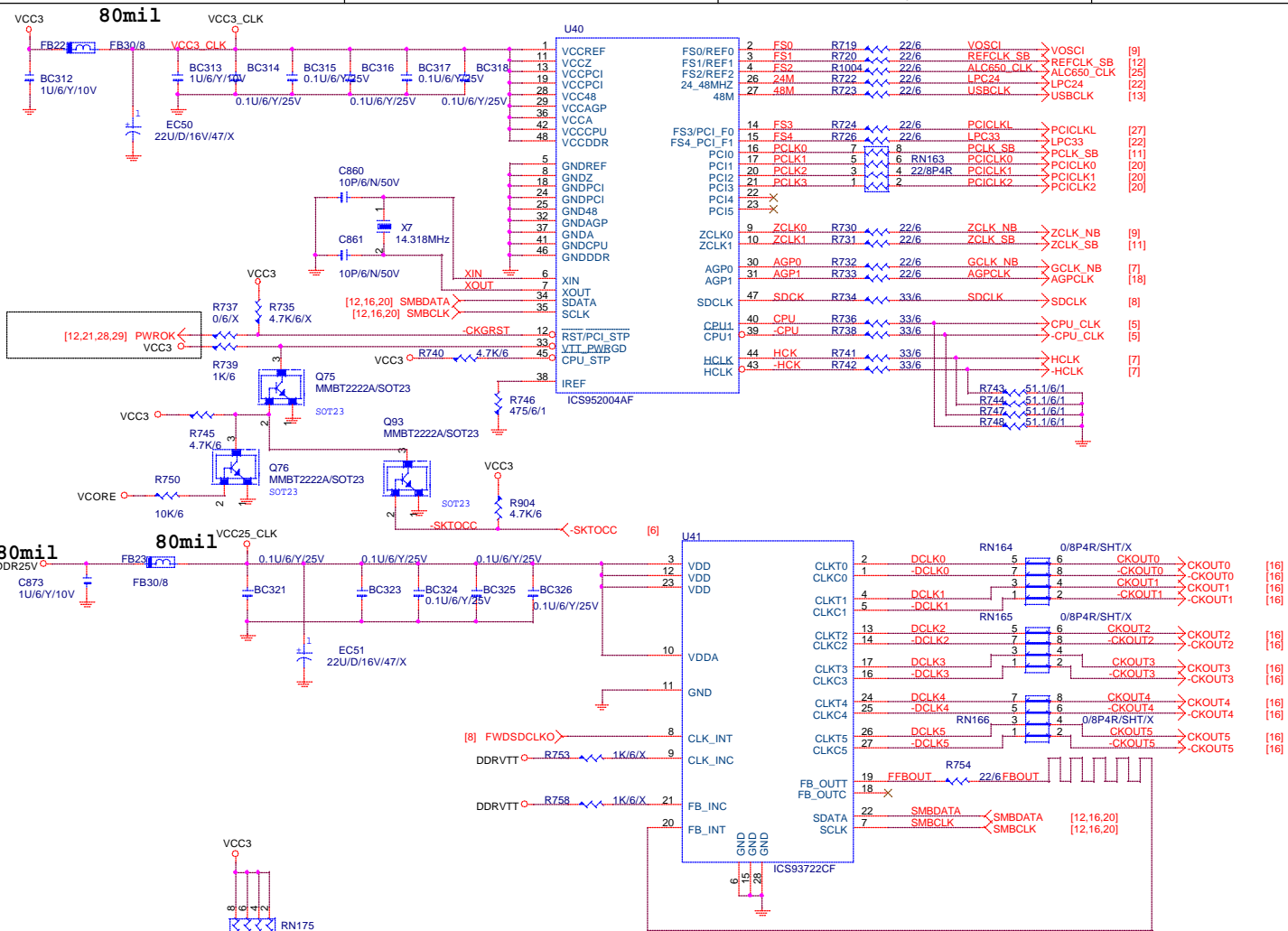
**S.B HEATSINK**

SB\_HEATSINK1



SB\_HEATSINK/X

<b>GIGABYTE</b>		
Title <b>SIS962/961B(PWR)</b>		
Size Custom	Document Number <b>GA-8SIMLH</b>	Rev <b>3.02</b>
Date: Monday, January 13, 2003	Sheet 14	of 32

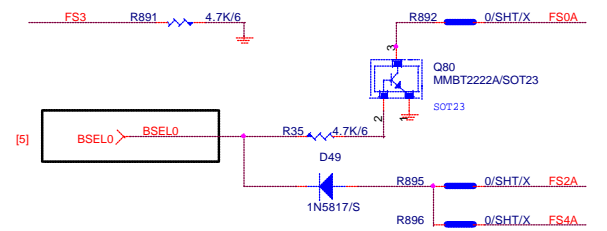


REV 0.2 10PF  
 CKOUT0 4 3  
 -CKOUT0 2 1  
 CKOUT1 6 5  
 -CKOUT1 8 7  
 CN27 10P/8P4C  
 CKOUT2 4 3  
 -CKOUT2 2 1  
 CKOUT3 6 5  
 -CKOUT3 8 7  
 CN28 10P/8P4C  
 CKOUT4 2 1  
 -CKOUT4 4 3  
 CKOUT5 6 5  
 -CKOUT5 8 7  
 CN29 10P/8P4C  
 FBOUT C913 10P/6/N/50V

DCLK +/----->0 ohm ADD CAP 10PF (clear glitch)

ICS952001/2004						
CPU	DDR	FS0	FS1	FS2	FS3	FS4
100	133	1	1	0	0	0
133	133	0	1	1	0	1

DEFAULT SETUP AUTO(100/133)



**GIGABYTE**

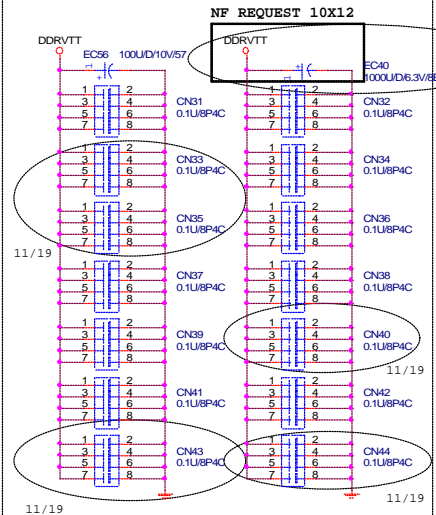
Title  
**CLOCK GEN + DDR BUFFER**

Size	Document Number	Rev
Custom	<b>GA-8SIMLH</b>	<b>3.02</b>

Date: Monday, January 13, 2003 Sheet 15 of 32



### DDRVTT Decouple

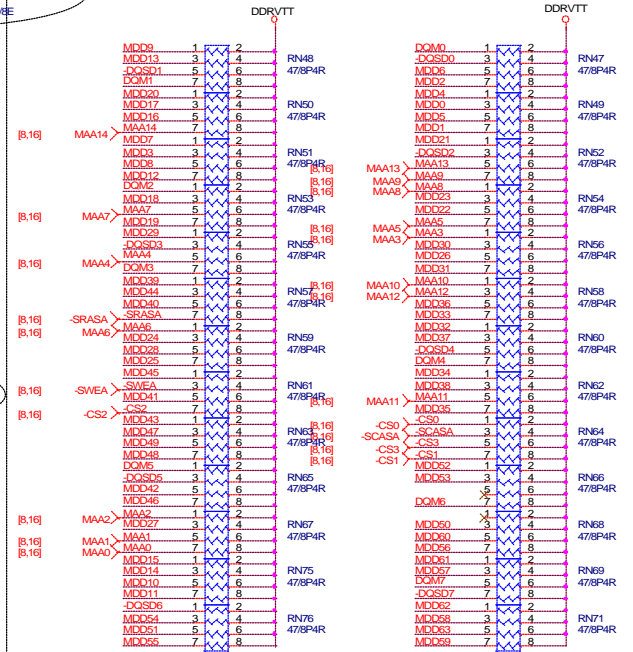


R&D NOTE 109 (0.1U/8P4C X9PCS)

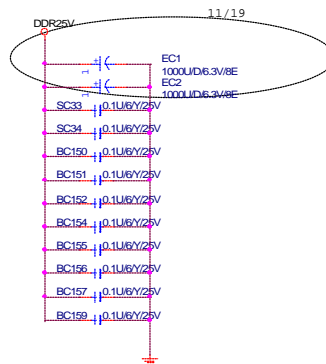
NOTE: Place these decoupling capacitors close to VTT\_MEM termination resistors. (one decoupling capacitor for each two R-packs)

### DDR TERMINATION

REV 0.2 DDR DIMM ISSUE 33-->47 OHM

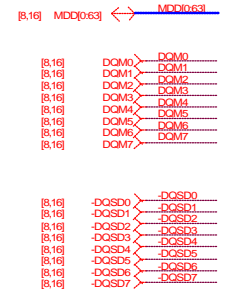
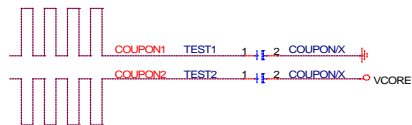


### DDR25V Decouple



NOTE: Place Distribute 4 pcs per DDR module.

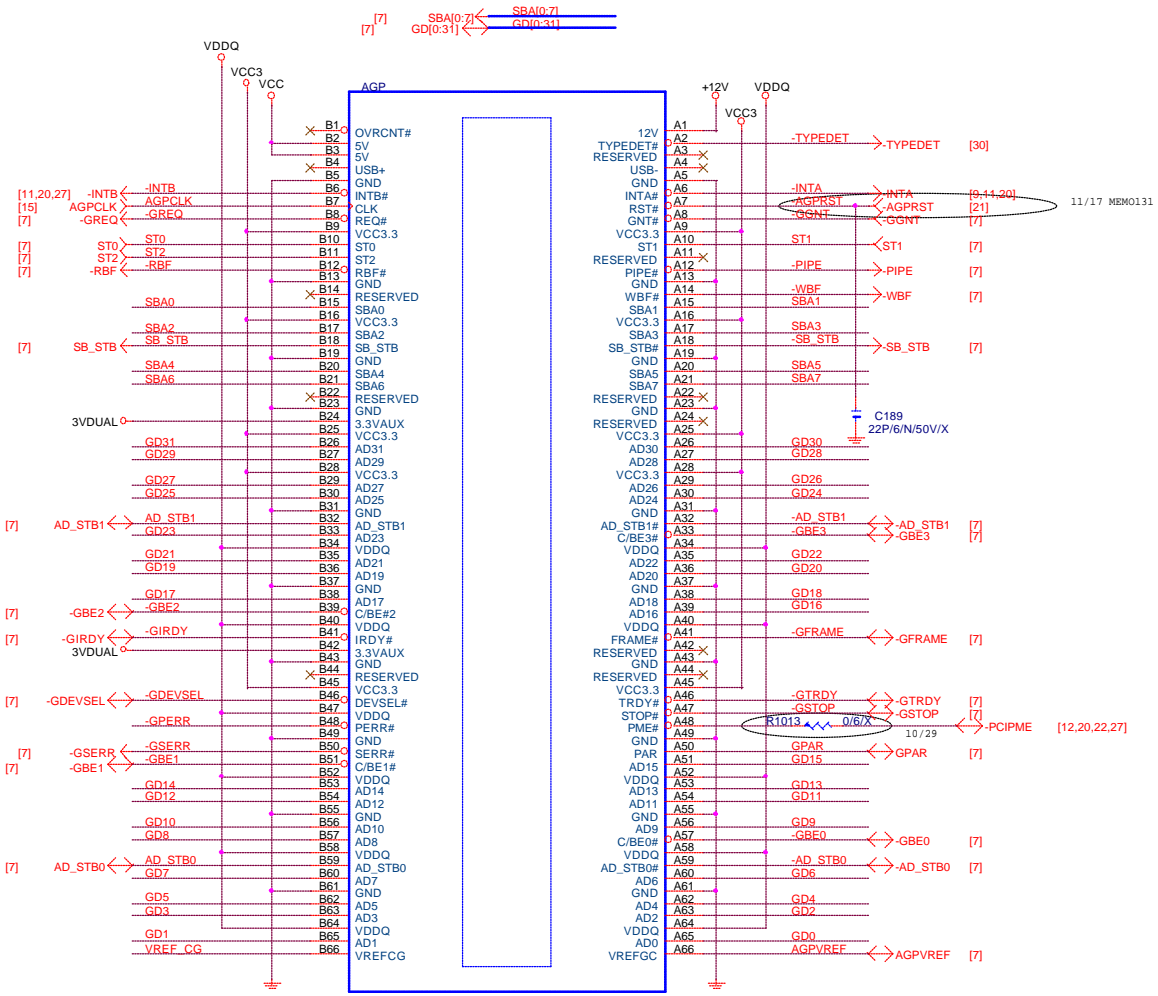
### IMPEDANCE TESTING COUPON



**GIGABYTE**

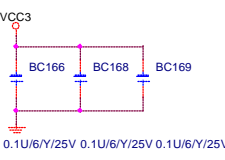
**DDR UNBUFFERED 3**

Title		Rev
Size		3.02
Custom	Document Number	
<b>GA-8SIMLH</b>		
Date:	Monday, January 13, 2003	Sheet 17 of 32



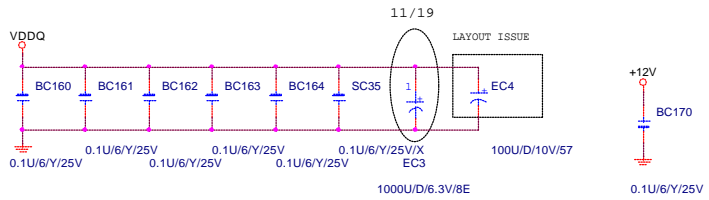
UAGP132/CO/GF  
REV 0.2 AGP BOM MODIFY  
11AC1-05R124-11

**AGP SLOT (AGP-N)**



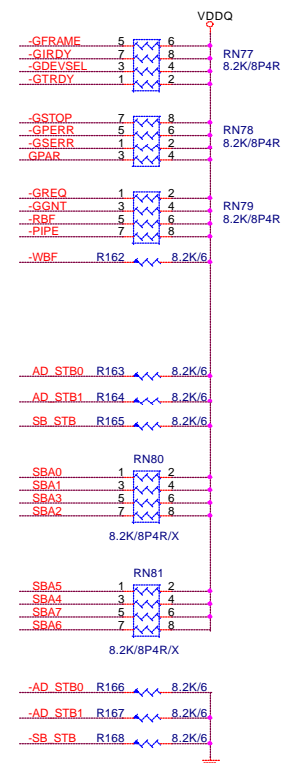
Place 1 at each pair of 3.3V pins

Decoupling capacitors  
(Place near AGP slot)

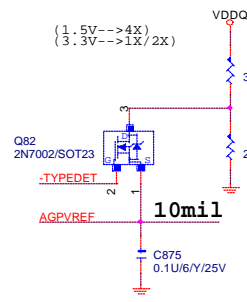


Place 1 at each pair of VDDQ pins

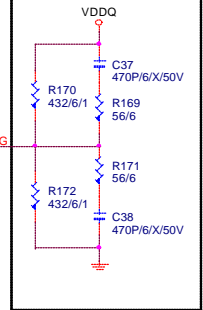
Place an additional for spread from A14 - A33



**SWITCH CIRCUIT FOR VDDQ**



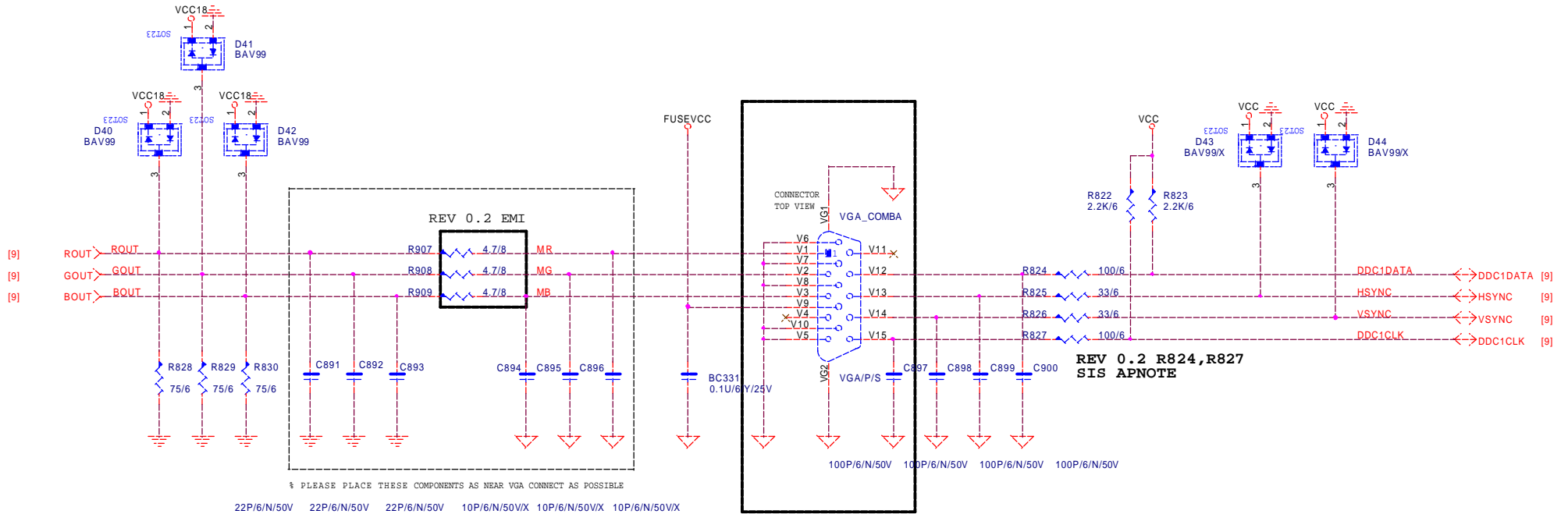
**SIS DESIGN**



<b>GIGABYTE</b>		
<b>AGP SLOT</b>		
Title	AGP SLOT	
Size	Document Number	Rev
Custom	<b>GA-8SIMLH</b>	<b>3.02</b>
Date:	Monday, January 13, 2003	Sheet 18 of 32

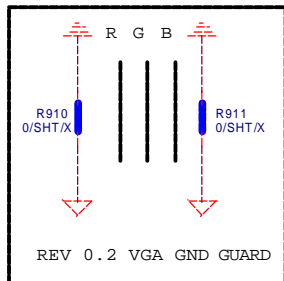
# VGA CONNECTOR 1

SIS 645DX NO POP



REV 0.2 R824, R827  
SIS APNOTE

## DUAL LAYOUT (VGA/COM)

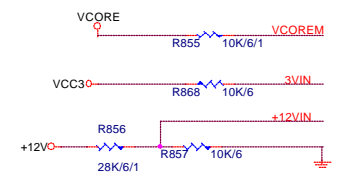
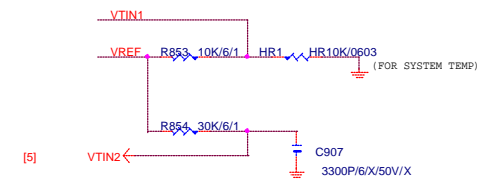
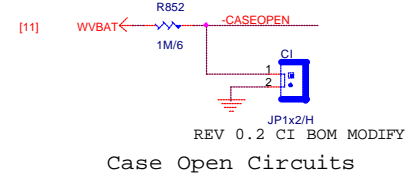
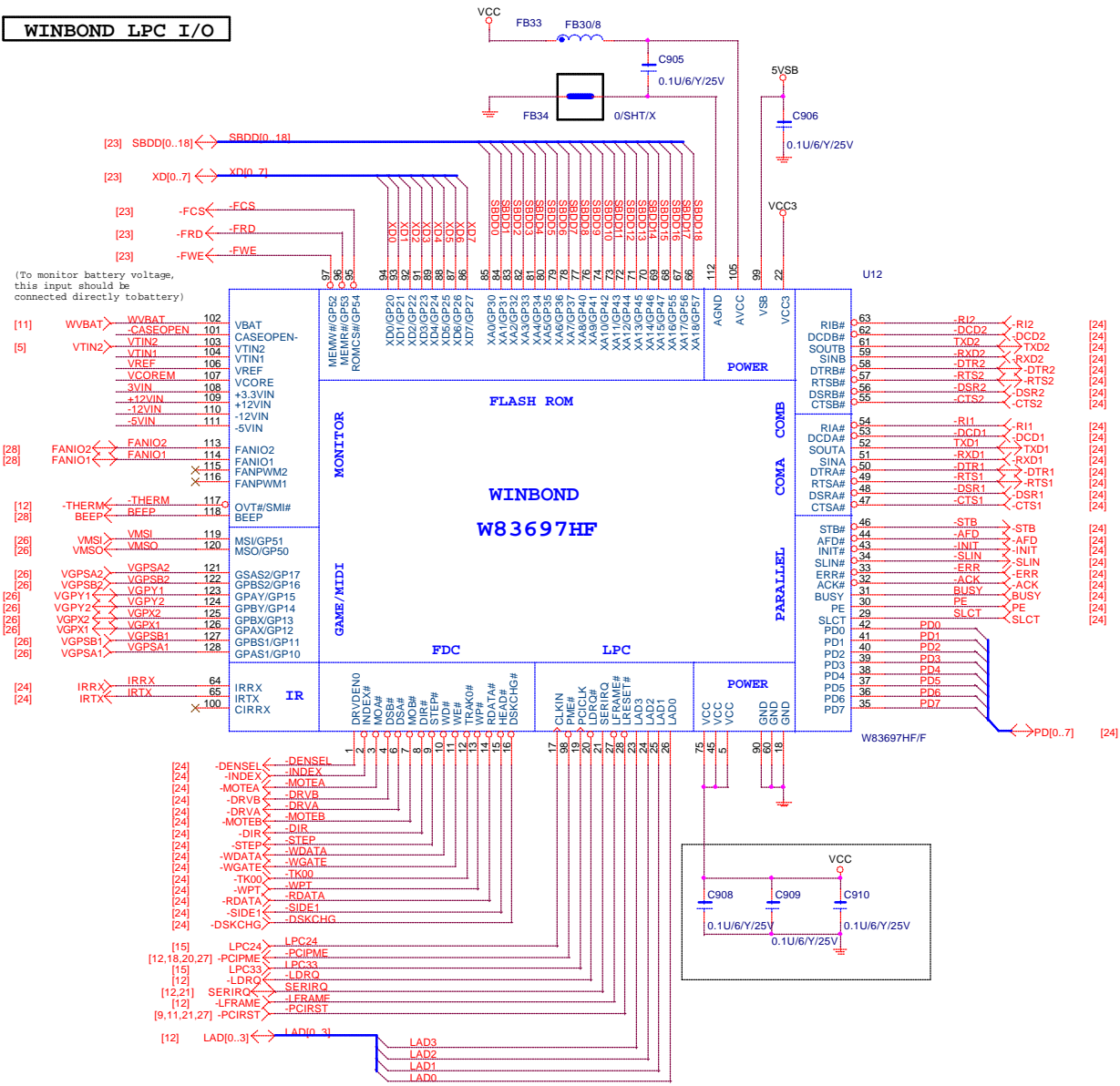


<b>GIGABYTE</b>		
Title <b>VGA CONNECTOR</b>		
Size P	Document Number <b>GA-8SIMLH</b>	Rev <b>3.02</b>
Date: Monday, January 13, 2003	Sheet 19	of 32

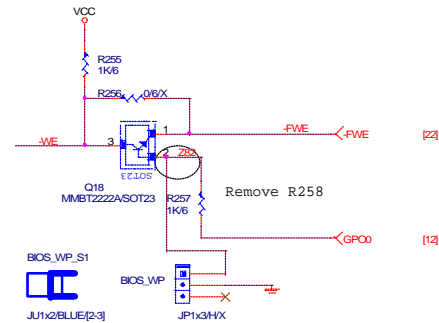
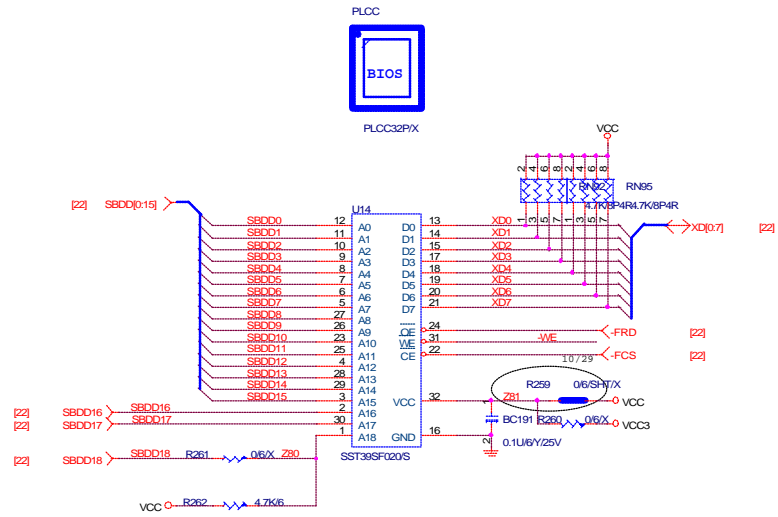




**WINBOND LPC I/O**

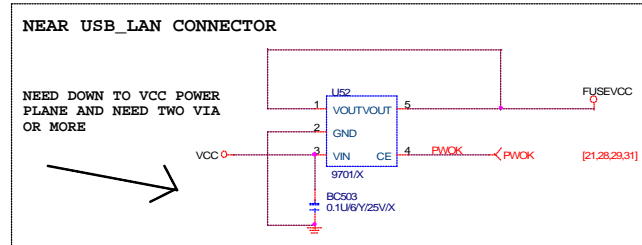
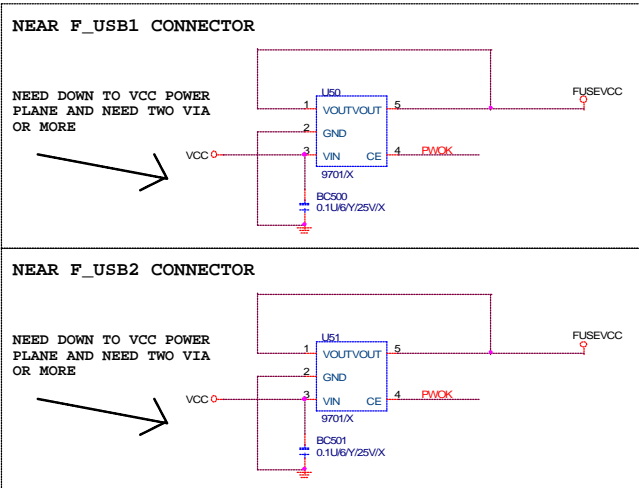


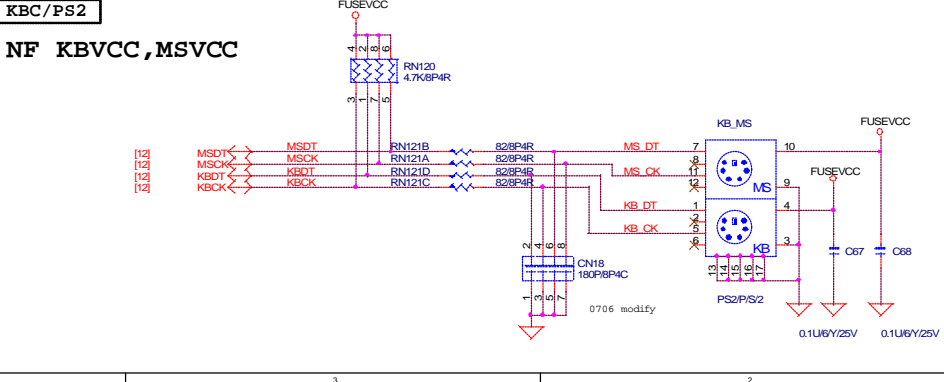
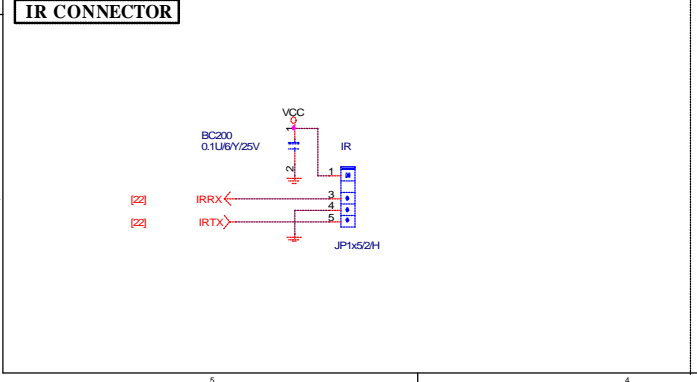
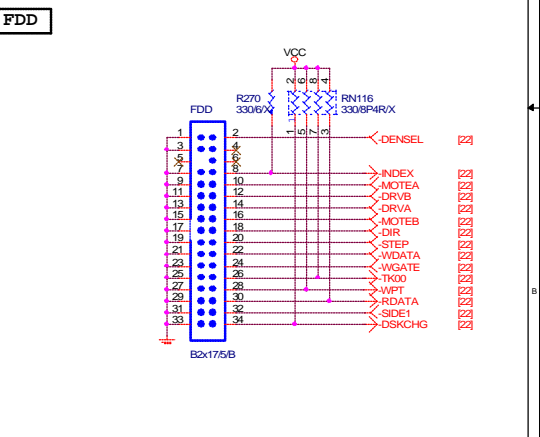
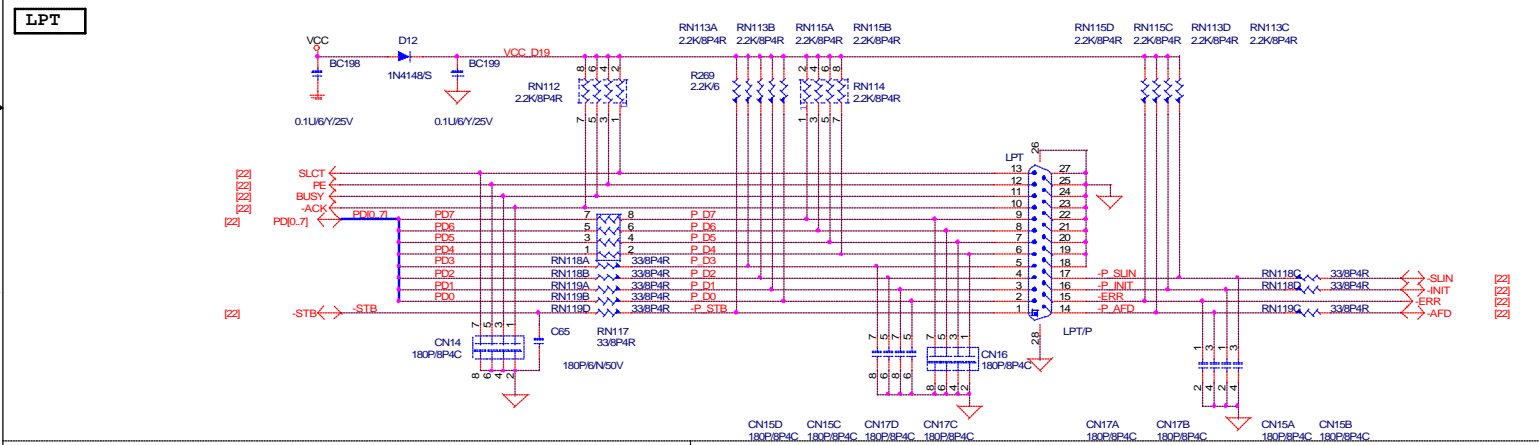
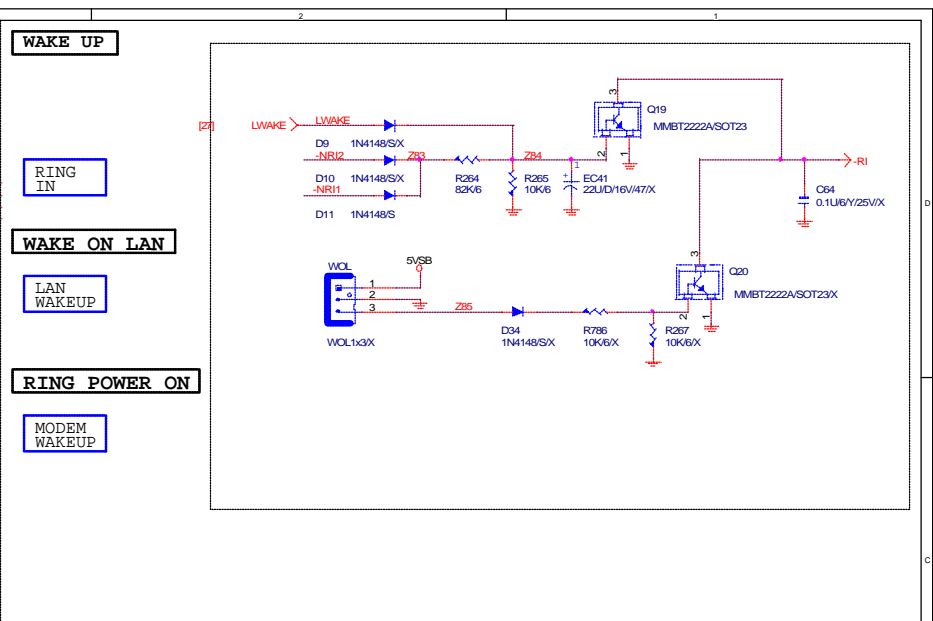
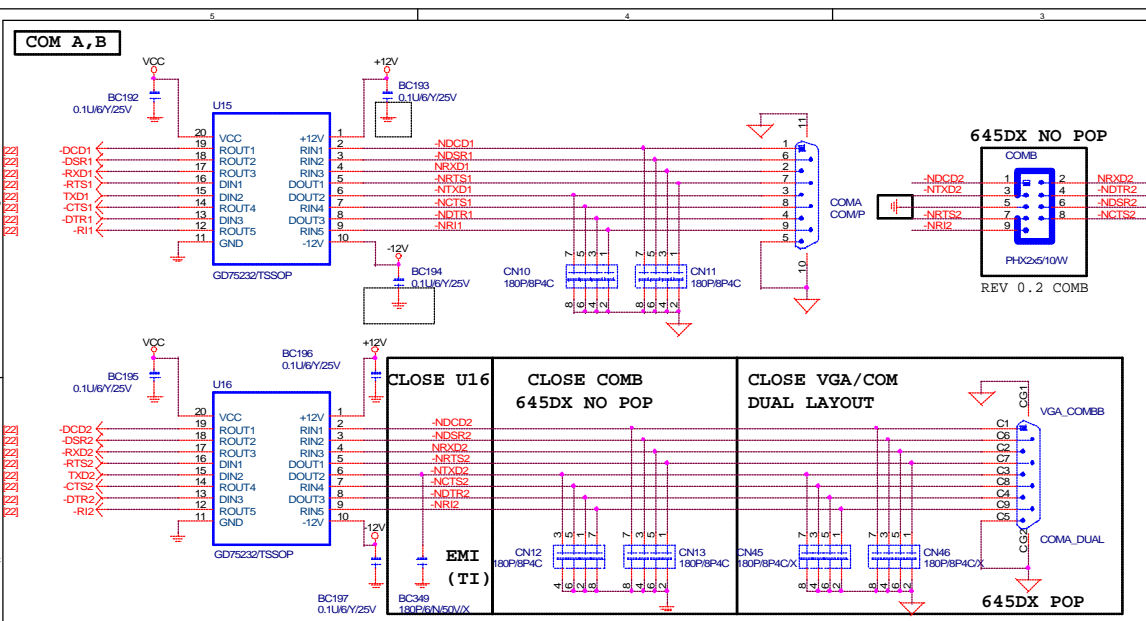
<b>GIGABYTE</b>		
Title <b>LPC W83697</b>		
Size Custom	Document Number <b>GA-8SIMLH</b>	Rev <b>3.02</b>
Date: Monday, January 13, 2003	Sheet 22	of 32

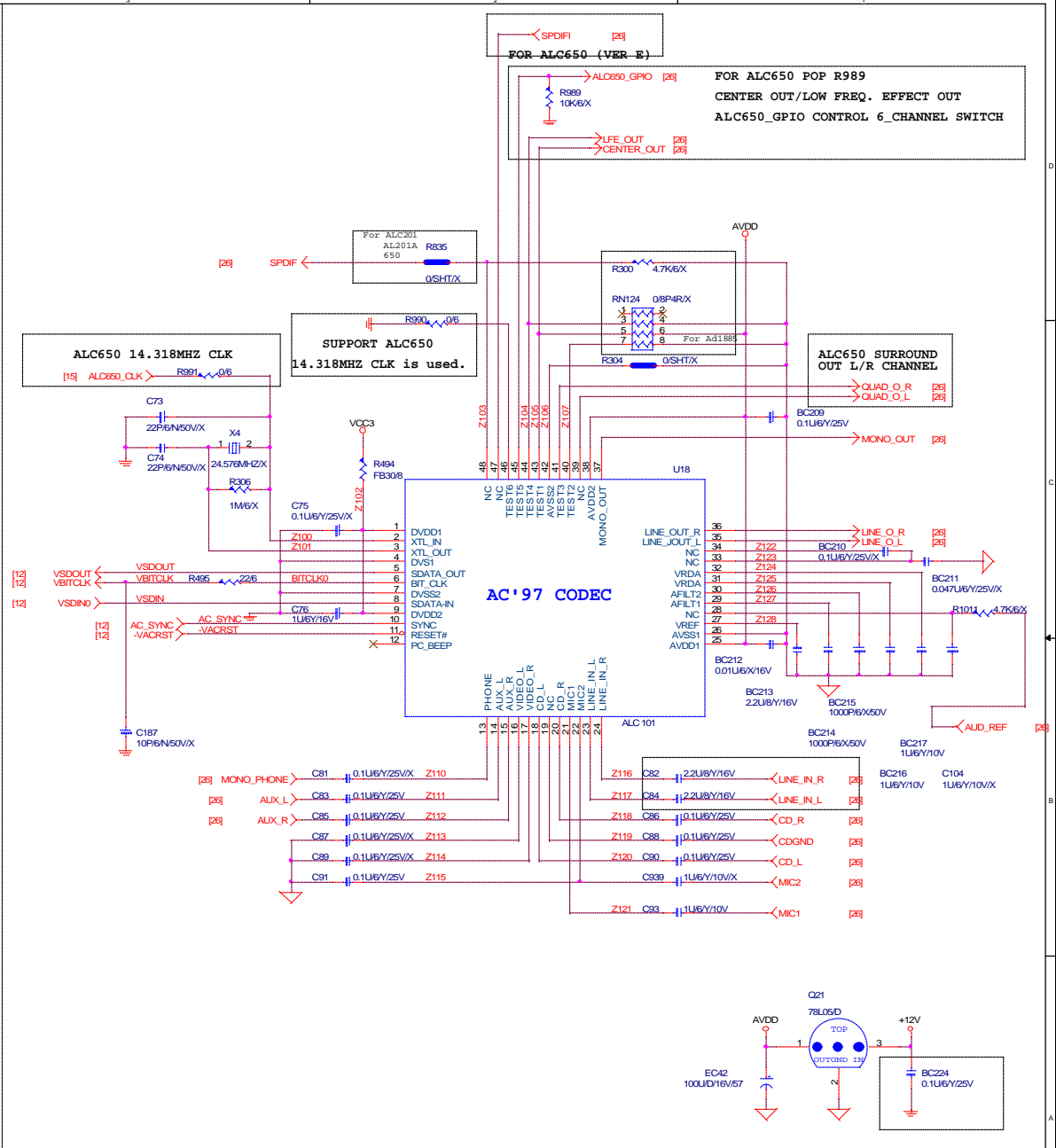


BIOS\_WP: BIOS WRITE PROTECT

PIN	BIOS_WP
1-2	WRITE PROTECT
2-3	WRITE ENABLE (default)







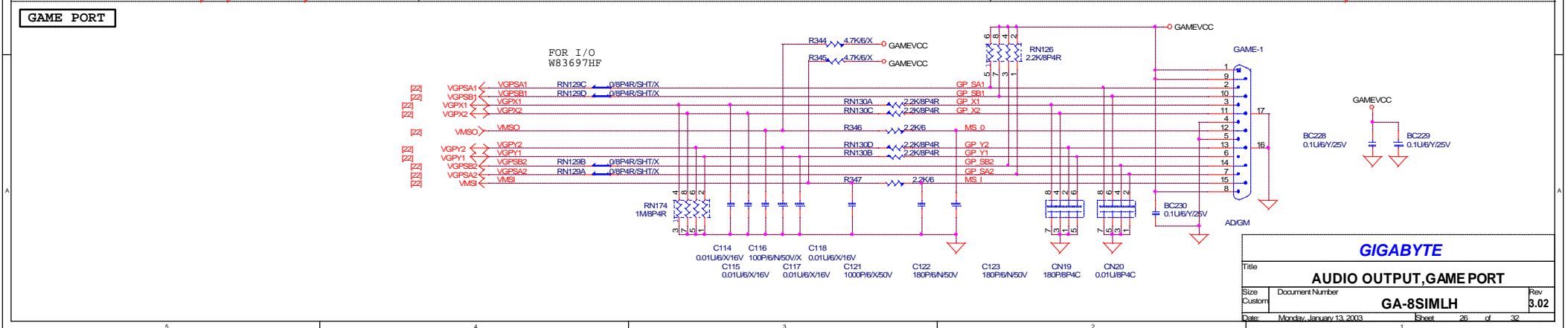
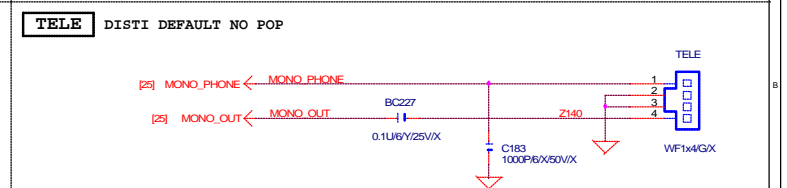
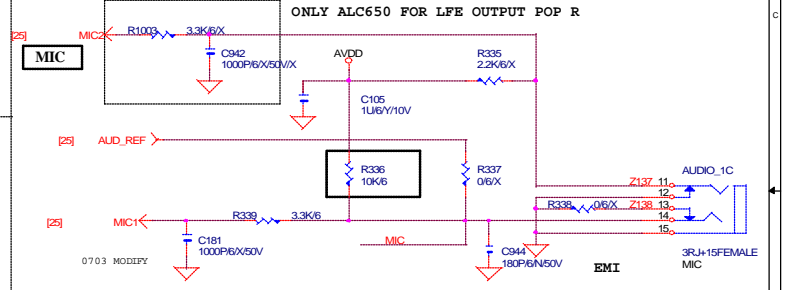
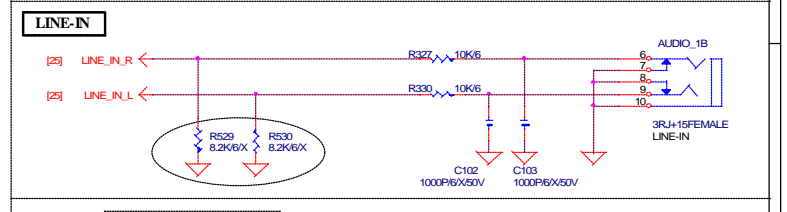
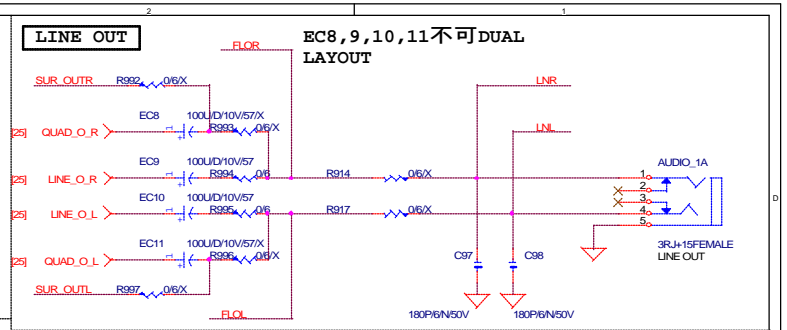
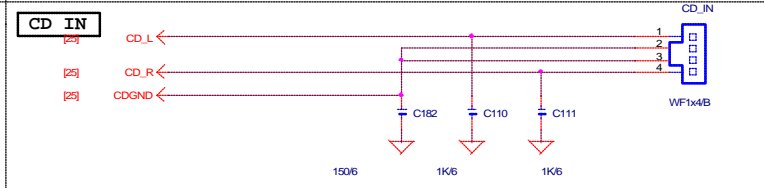
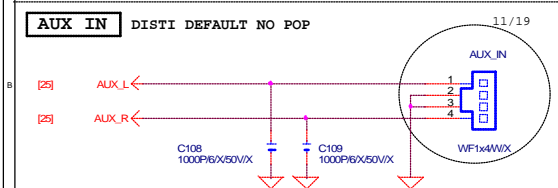
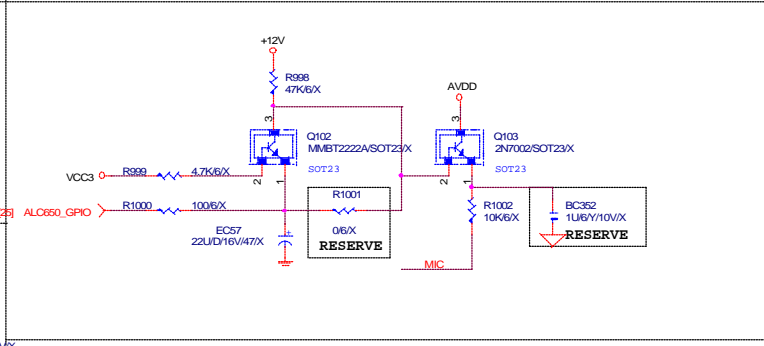
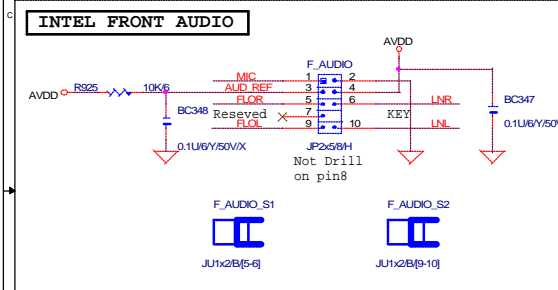
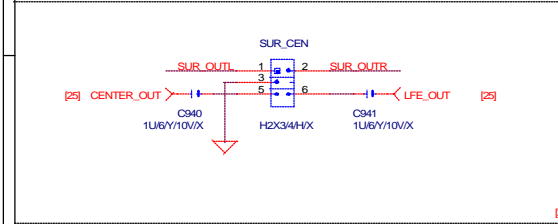
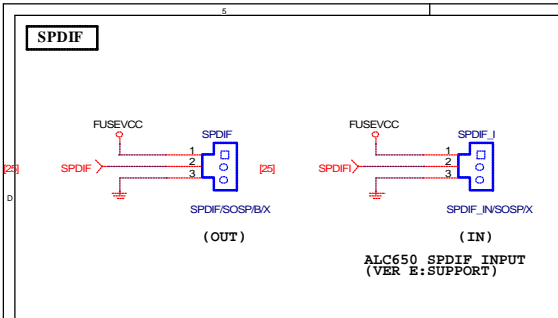
NF	SIGMATEL9756
Disti	ALC201A

**GIGABYTE**

**AUDIO (AC97 CODEC)**

Size	Document Number	Rev
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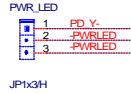
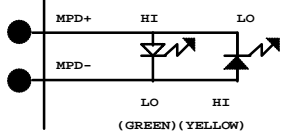
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**FRONT PANEL**

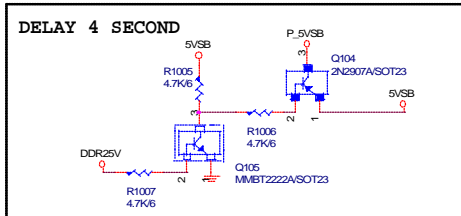
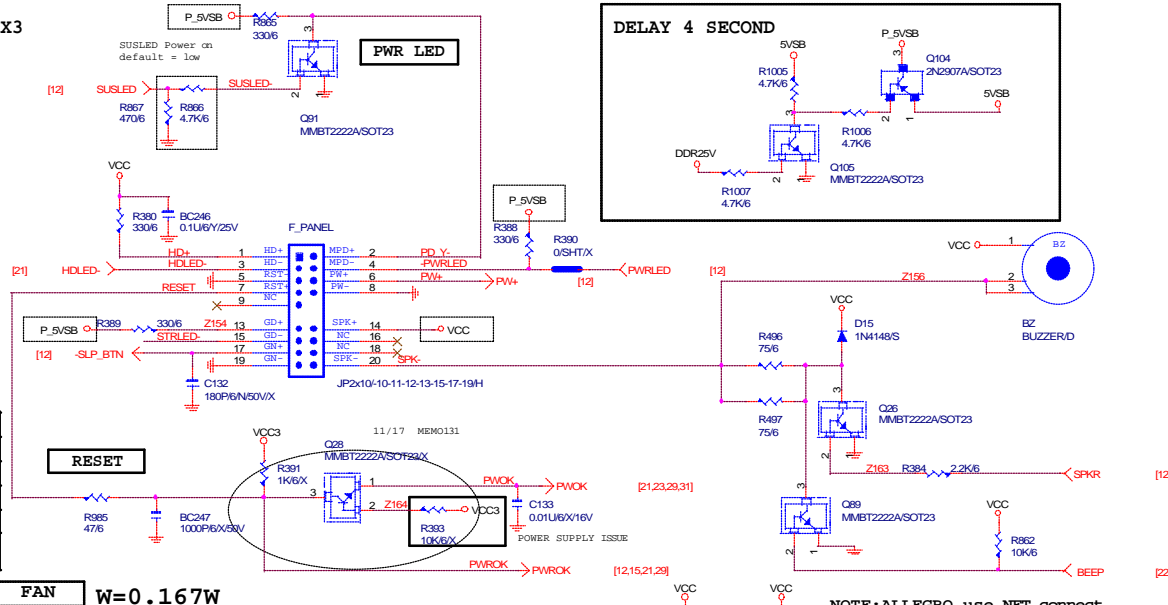
**PWR\_LED FOR DISTI PIN 1X3  
LED USED**



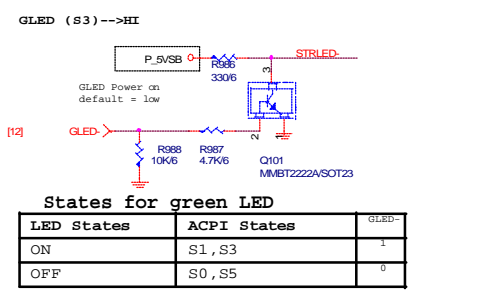
LED States	ACPI States	MPD+	MPD-
OFF	S1,S3,S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING

**States for a dual-color power LED**

LED States	ACPI States	MPD+	MPD-
OFF	S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING
Steady Yellow	S1,S3	LO	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING

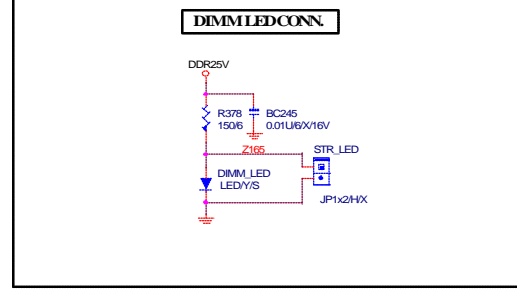
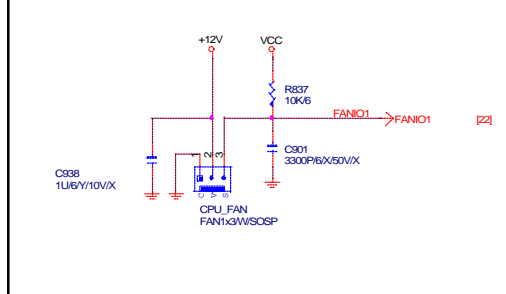


**CPU FAN W=0.167W**

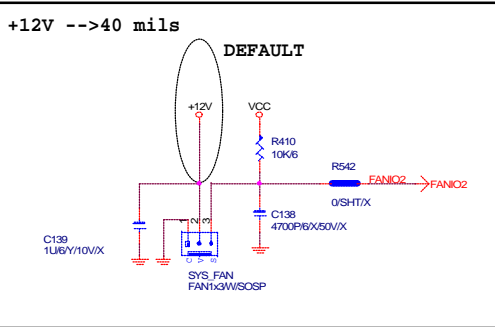


**States for green LED**

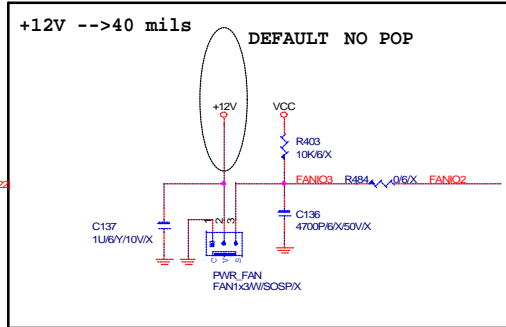
LED States	ACPI States	GLED-
ON	S1, S3	1
OFF	S0, S5	0



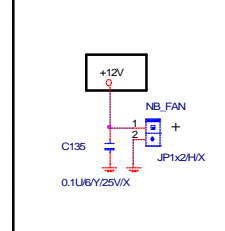
**SYSTEM FAN W=0.167W**



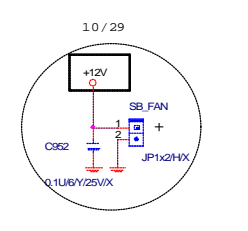
**POWER FAN W=0.167W**



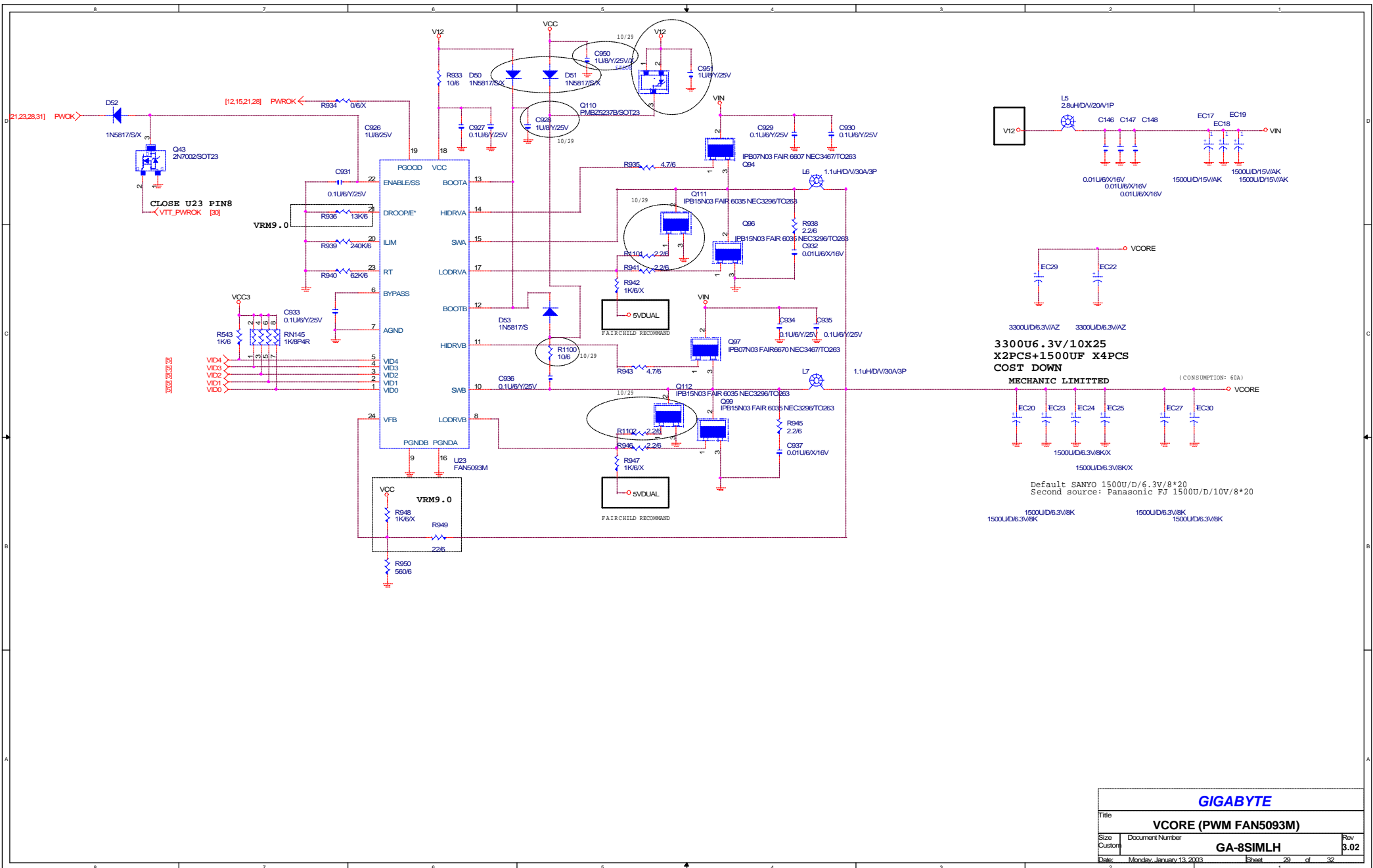
**NB HEATSINKFAN**



**SB HEAT SINK FAN**



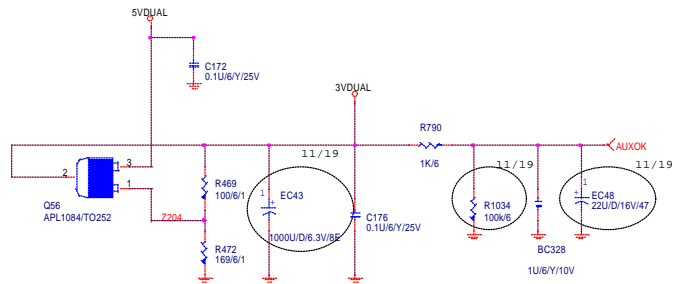
<b>GIGABYTE</b>		
<b>PANEL, STR LED &amp; FANS</b>		
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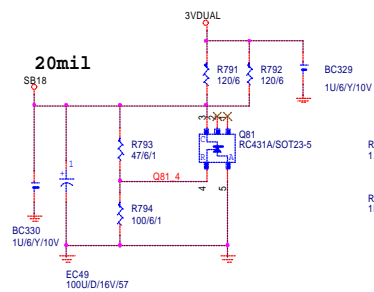
<b>GIGABYTE</b>		
Title		
<b>VCORE (PWM FAN5093M)</b>		
Size	Document Number	Rev
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**5VDUAL TRANS TO 3VDUAL(3.3V)**

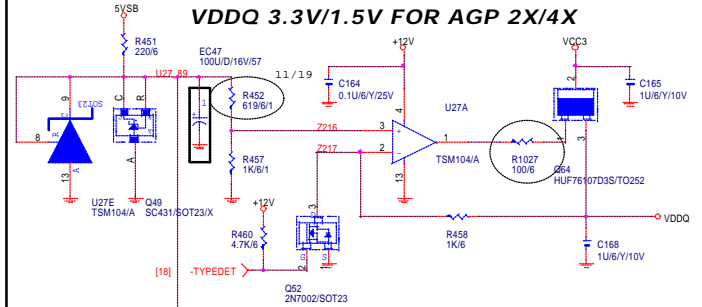
5VDUAL 80 mils ABOVE



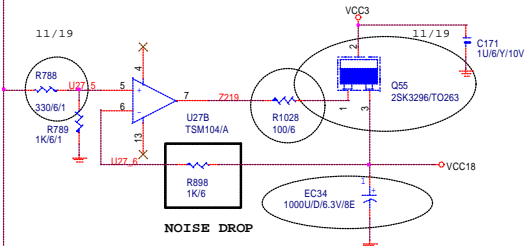
**SB18 FOR SB**



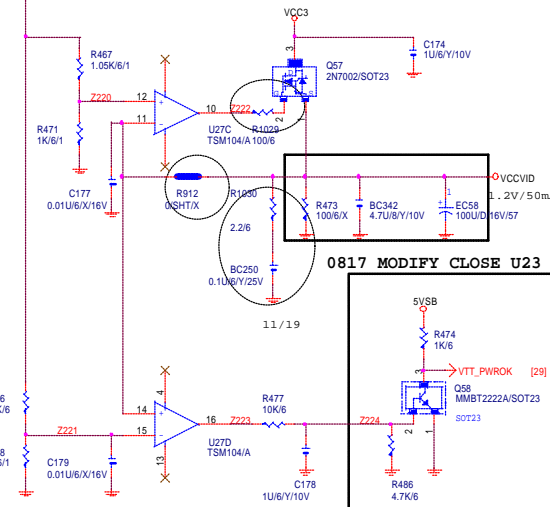
**VDDQ 3.3V/1.5V FOR AGP 2X/4X**



**VCC18 FOR NB,SB**



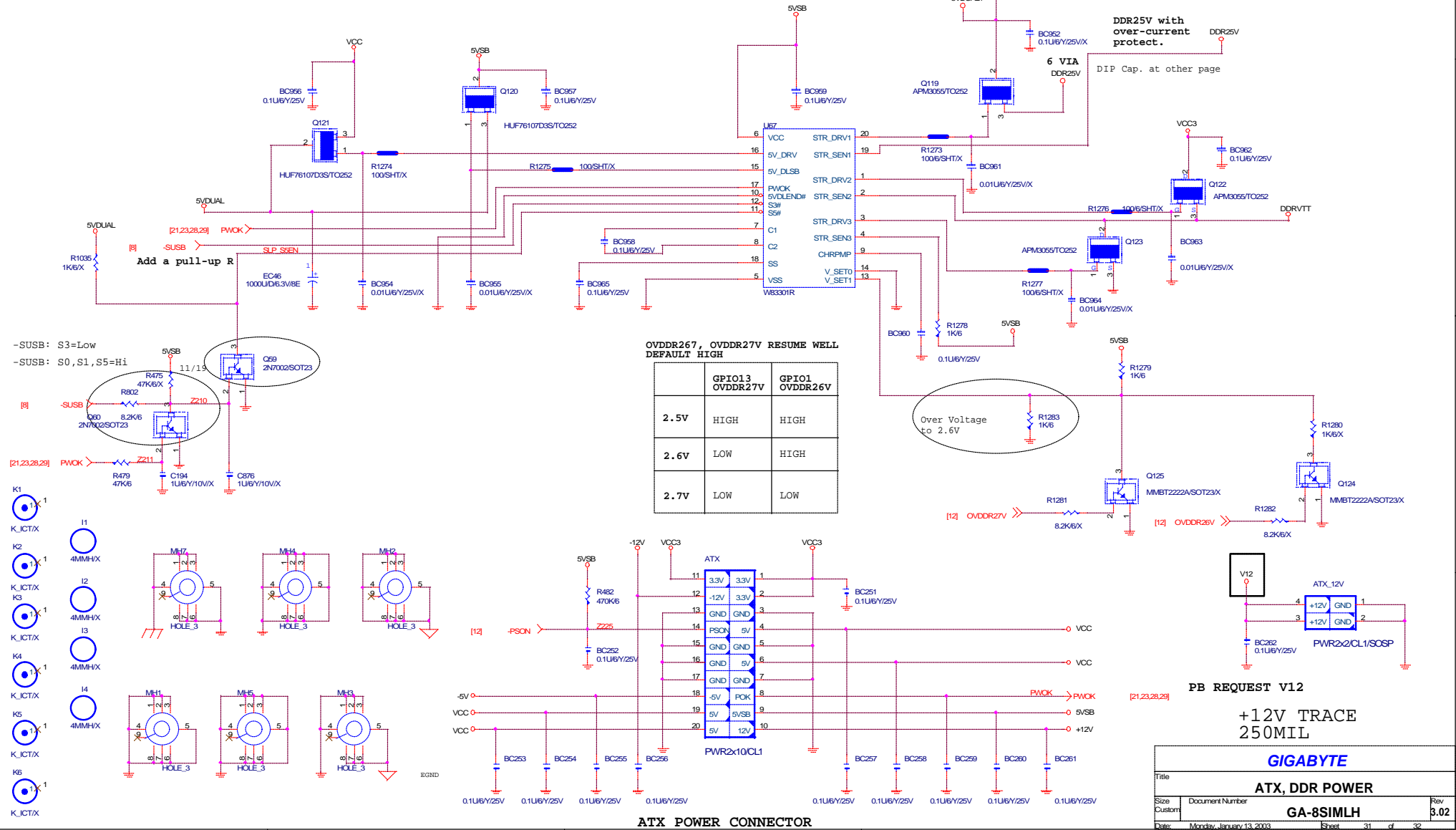
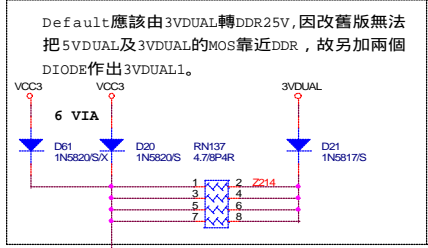
**VCCVID FOR NORTHWOOD CPU**



<b>GIGABYTE</b>		
<b>DC POWER</b>		
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# ATX CON, DDR POWER

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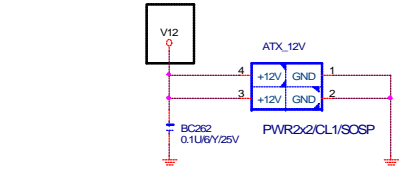
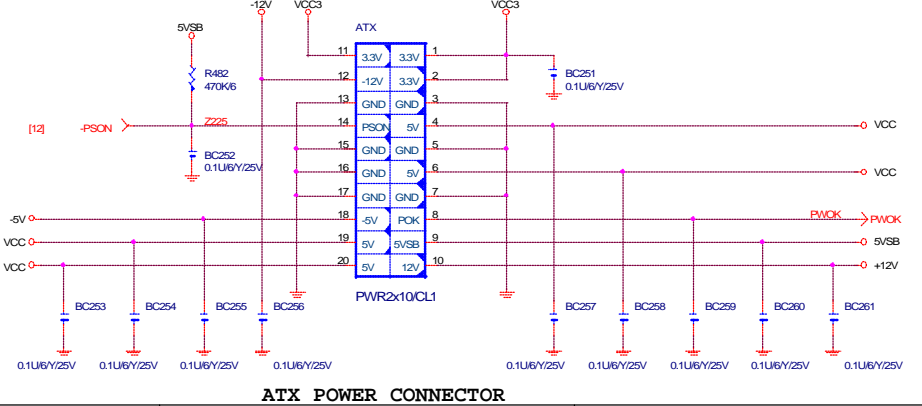
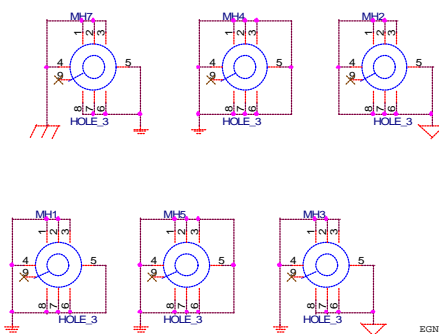
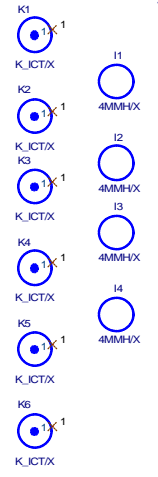
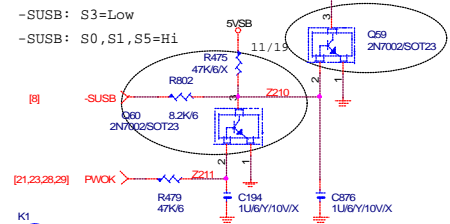


DDR25V with over-current protect.  
DIP Cap. at other page

OVDDR267, OVDDR27V RESUME WELL DEFAULT HIGH

	GPIO13 OVDDR27V	GPIO10 OVDDR26V
2.5V	HIGH	HIGH
2.6V	LOW	HIGH
2.7V	LOW	LOW

Over Voltage to 2.6V



PB REQUEST V12  
+12V TRACE  
250MIL

**GIGABYTE**

Title: **ATX, DDR POWER**

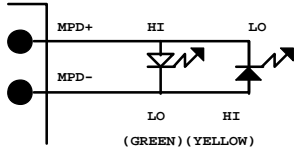
Size Custom | Document Number: **GA-8SIMLH** | Rev: **3.02**

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LO:Normal

RTL8100L ON-BOARD		
-REQ0	PCI1	IDSEL(A20)--B
-REQ1	PCI2	IDSEL(A22)--C
-REQ2	PCI3	IDSEL(A24)--D
-REQ3	RTL8100L	IDSEL(A27)--B

8SRXL South Bridge GPIO LIST				
ITEM	DESCRIPTION	I/O	STATUS	Default
GPIO0	Bios Write Protect	O	Hi:Write Enable, Lo:Write Protect	Hi
GPIO1	N/A		PULL-UP	Hi
GPIO2	THERM#			Hi
GPIO3	Green Button	O	Hi:Normal, Lo:Into Green mode	Hi
GPIO4	CLKRUN#		PULL-DOWN	Lo
GPIO5	N/A		PULL-UP	Hi
GPIO6	DDR OVER VOLTAGE	O		Hi
GPIO7	SUSLED	O	AS LIKE DEFINED...	Lo
GPIO8	Wake On Ring	I	Hi:Normal, Lo:Ring Power On	Hi
GPIO9	GLED	I	AS LIKE DEFINED...	Lo
GPIO10	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo
GPIO11	N/A		PULL-UP	Hi
GPIO12	N/A		PULL-UP	Hi
GPIO13	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo
GPIO14	DDR OVER VOLTAGE	I		Lo
GPIO15	KB Data	I/OD		
GPIO16	KB Clk	I/OD		
GPIO17	MS Data	I/OD		
GPIO18	MS Clk	I/OD		



States for a single-color power LED

LED States	ACPI States	MPD+	MPD-	BIOS	
				GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING

BIOS REQUEST

SINGLE	DUAL	INTEL LED DEFINED				GIGABYTE LED DEFINED				SINGLE	DUAL
		GPIO7	ACPILED	GPIO9		GPIO7	ACPILED	GPIO9			
GREEN	GREEN	S0	LO	LO	LO	S0	LO	LO	LO	GREEN	GREEN
OFF	YELLOW	S1	HI	HI	HI	S1	LO	BLINKING	HI	G(BLINK)	G(BLINK)
OFF	YELLOW	S3	HI	HI	HI	S3	HI	HI	HI	OFF	YELLOW
OFF	OFF	S4/S5	LO	HI/NC	LO	S4/S5	LO	HI/NC	LO	OFF	OFF

States for a dual-color power LED

LED States	ACPI States	MPD+	MPD-	BIOS	
				GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING
Steady Yellow	S1,S3	LO	HI	HI	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING	HI	BLINKING

States for green LED

LED States	ACPI States	GLED-	BIOS
			GPIO9
ON	S1,S3	HI	HI
OFF	S0,S5	LO	LO

**GIGABYTE**

Title			<b>GPIO, REQ/GNT Table</b>		
Size	Document Number	Rev			
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