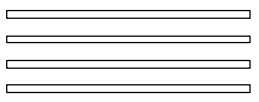
8SIMLH Schematics

Revision 2.1

SHEET	TITLE
1	COVER SHEET
2	BOM & PCB MODIFY HISTORY
3	BLOCK DIAGRAM
4,5,6	INTEL CPU_WMT_478
7-10	SIS651/645DX (NORTH BRIDGE) HOST; DDR; AGP,HYPER ZIP
11-14	962 (SOUTH BIRDGE)
15	CKG(ICS952004) + CKBF (ICS93722)
16,17	DDR SDRAM DIMMS 1,2 & DDR TERMINATION
18	AGP SLOT
19	VGA Connector
20	PCI SLOT 1-3
21	IDE,USB
22	Winbond W83697HF
23	BIOS
24	COM,PRT,FDD,KB/MS,IR
25	CNR SLOT
26	AUDIO AC 97 CODEC
27	AUDIO JACK,GAME PORT
28	RTL8100B & USB CONNECTOR
29	PANEL,STR LED,FANS ,CPU GN
30	VCORE PHASE PWM HIP 6301 + 6601
31	ALL POWER CIRCUIT
32	ATX & ATX12V CONN
33	GPIO Connecttion
34	TEST POINT



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Title: COVER SHEET

Size	Document Number	Rev
Custom	GA-8SIMLH	2.1

Date: Thursday, September 12, 2002 Sheet 1 of 32

Model Name: 8SIMLH

Version:2.0

Component value change history

AUTOBOM
2002/06/04

Date	Change Item	Reason
02/04	LAYOUT PLACEMENT	DEL 1394 CONNECTOR(LAYOUT ISSUE)
		SWAP NET
02/05	LAYOUT LIB	COIL-8P---->COIL-8P_SHORT
02/06	VGA/COM DUAL LAYOUT	
	DDRVTT (R&D 109)	DDRVTT DECOUPLING X14 PCS (0.1U/8P4C CAP)
02/06-1	LAYOUT LIB MODIFY	USB2.0 CHOKE (NO SHORT)
		AGP SLOT-->AGP_N
02/19	NET SWAP	BC345-->SC60(COMP-->SOLDER SIDE)
02/20	EMI ISSUE	CLOSE U16(75232) -NTXD2 ADD CAP 180P/6(BC349)
02/21	LAYOUT ISSUE	BC344-->SC61(COMP-->SOLDER SIDE)
		SWAP NET
	LIB MODIFY	MOSFET LIB TO263,252 CO LAYOUT(Q_TO263-252)
04/22	BOM MODIFY	AC97 CODEC --->ALC650
	PCB REV1.9	PWM 2 PHASE FAN5093M/C(VOCRE CAP COST DOWN)
		INTEL F_PANEL+F_USB1,2,F_AUDIO
		DDRVTT CAP 0.1U/8P4C X9PCS
04/23	PCB MODIFY	reduced PCB size(COST DOWN)
04/29		DEL MH6,ADD CAP MIC FOR EMI
05/08	PCB MODIFY	rename to GA-8SIMLH
	BOM MODIFY	SIS651+SIS962
05/13	BOM MODIFY	cost down CAP & FB
		ALC650 change to ST9721
05/21	PCB MODIFY	DEL BC218 ,ADD R1011 FOR F_MIC
		TEXT MODIFY
	BOM MODIFY	PCB CHANGE TO REV:2.0 1
06/04	BOM MODIFY	R867 10k/6 change to 470/6
		R921 324/1/6 change to 487/1/6
		ADD CN14,15,16,17 180P/8P4C
		ADD C944,C65 180P/N/50V/6
08/04	BOM MODIFY	IDE,PANEL,USB
		FDD,SMBUS,22U TO 100U

Circuit or PCB layout change for next version

Date	Change Item	Reason
08/06	BOM MODIFY	U39 change to SIS962L REV:A2
08/12	BOM MODIFY	DEL R948 1K/6 ADD R950 470/6 R949 10/6 change to 22/6
		EC1,2,3,5,34,40,46 330U/25V change to 1200U/6.3V
08/13	BOM MODIFY	EC54 22U change to 100U
	BOM MODIFY	R939 200K/6 change to 240K/6 ST9721 change to ALC101
	PCB MODIFY	REV:2.01 CHANGE TO2.1
09/12	BOM MODIFY	EC37 100U change to 22U

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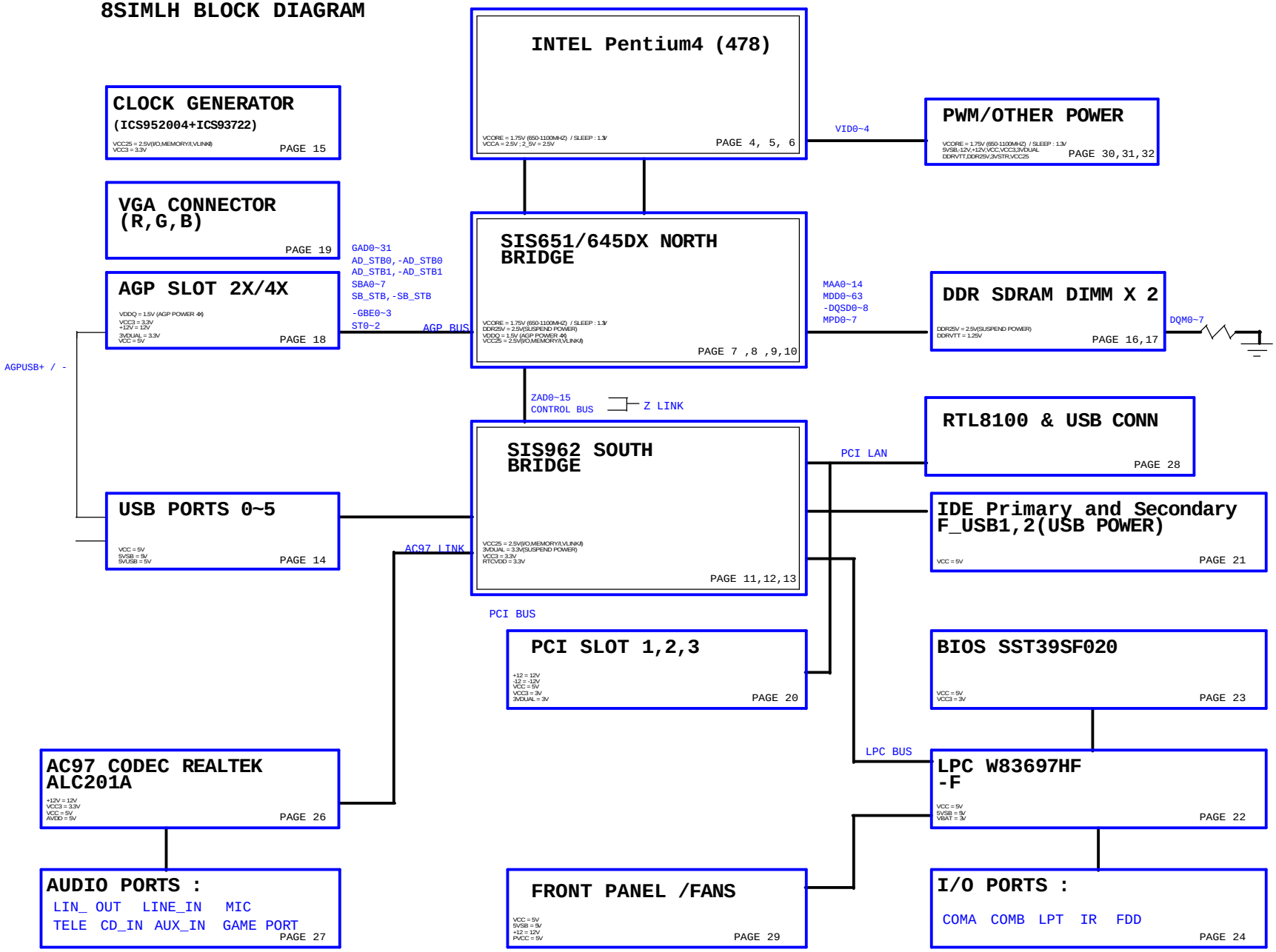
Title	BOM & PCB MODIFY HISTORY	
Size: Custom	Document Number: GA-8SIMLH	Rev: 2.0
Date: Thursday, September 12, 2002	Sheet 2 of 32	

8SIMLH BLOCK DIAGRAM



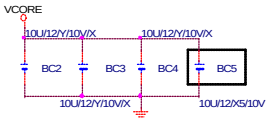
GIGABYTE

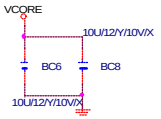
Title: BLOCK DIAGRAM

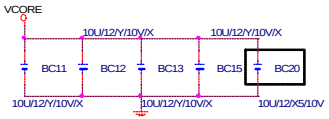
Size: A3 | Document Number: GA-8SIMLH | Rev: 2.1

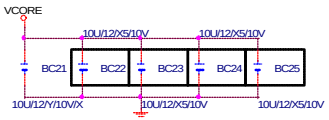
Date: Thursday, September 12, 2002 | Sheet 3 of 32

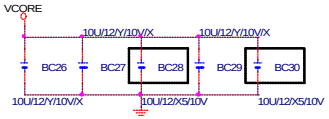
(X5R) X11 1206(10U) NOTE:GIGA

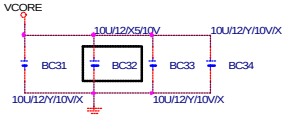


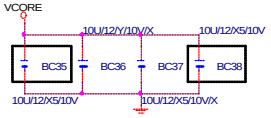


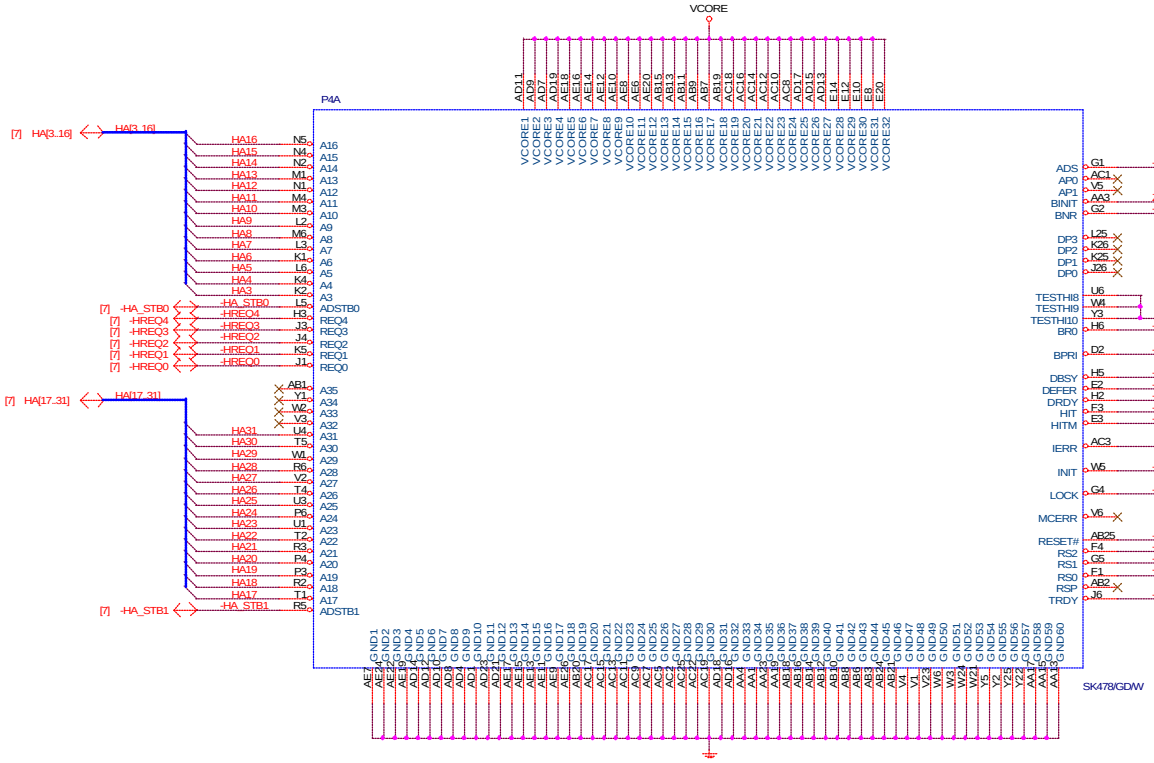












GIGABYTE		
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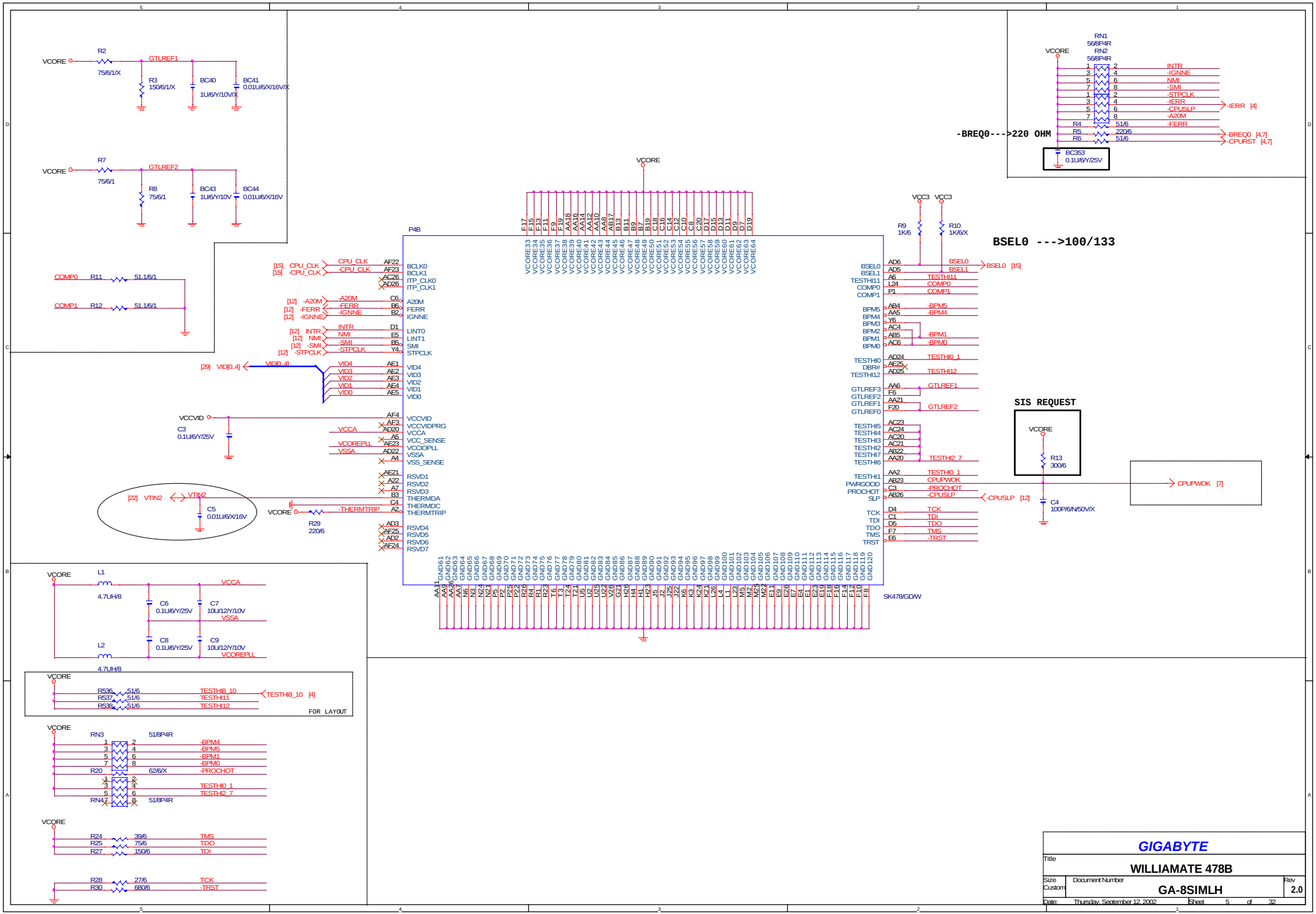
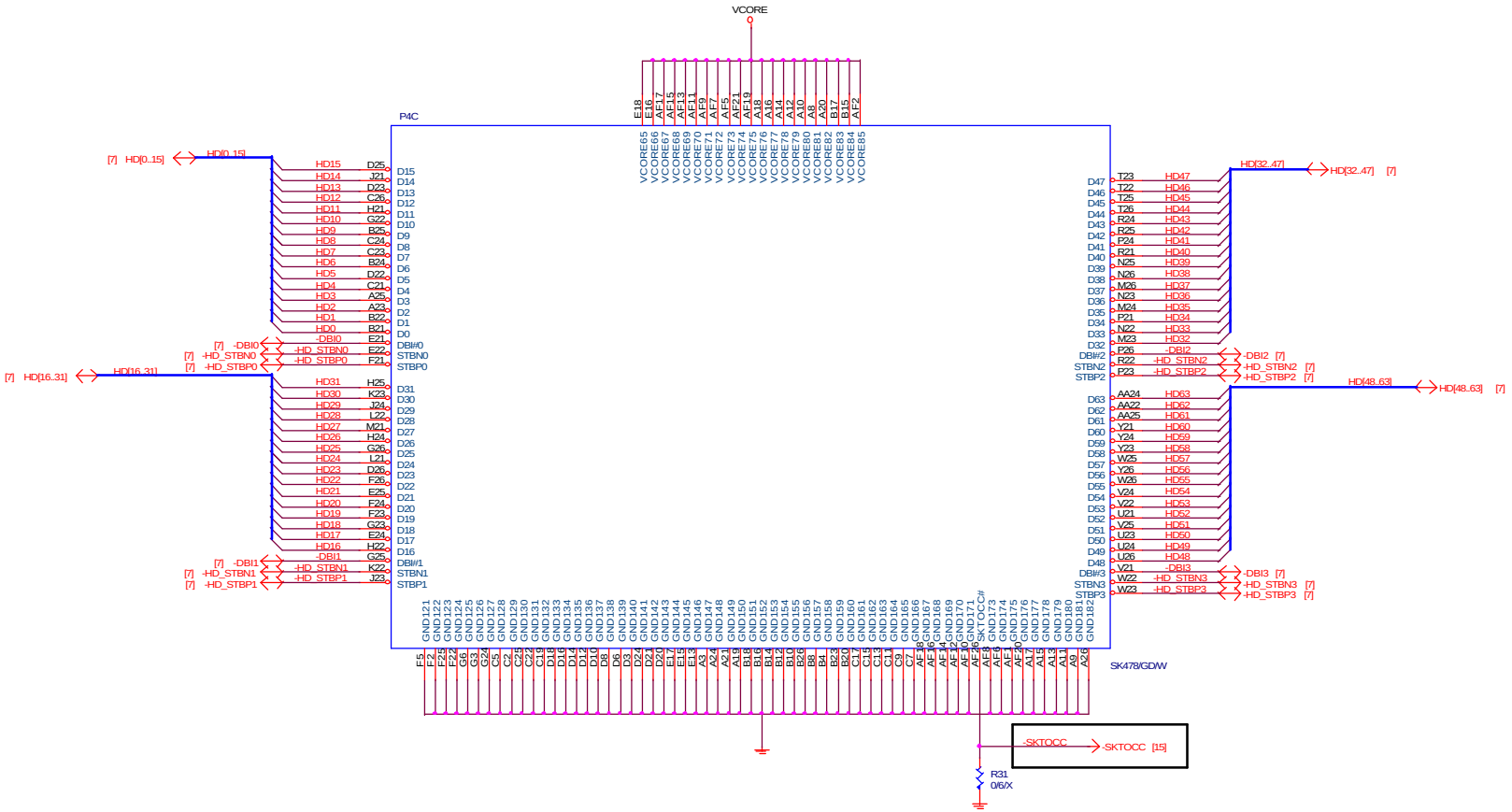
Size: Custom	Document Number: GA-8SIMLH	Rev: 2.0
Date: Thursday, September 12, 2002	Sheet 4 of 32	


VCORE
R2
75/6/1/X
GTLREF1
R3
150/6/1/X
BC40
1U/6/Y/10V/X
BC41
0.01U/6/X/16V/X
R7
75/6/1
GTLREF2
R8
75/6/1
BC43
1U/6/Y/10V
BC44
0.01U/6/X/16V
COMP0
R11
51.1/6/1
COMP1
R12
51.1/6/1
P4B
CPU_CLK
-CPU_CLK
BCLK0
BCLK1
ITP_CLK0
ITP_CLK1
A20M
FERR
IGNNE
INTR
NMI
SMI
STPCLK
LINT0
LINT1
VID[0.4]
VID4
VID3
VID2
VID1
VID0
VCCVID
VCCVIDPRG
VCCA
VCC_SENSE
VCCIOPLL
VSSA
VSS_SENSE
RSVD1
RSVD2
RSVD3
THERMDA
THERMDC
THERMTRIP
RSVD4
RSVD5
RSVD6
RSVD7
VTIN2
C5
0.01U/6/X/16V
R29
220/6
C3
0.1U/6/Y/25V
L1
4.7UH/8
C6
0.1U/6/Y/25V
C7
10U/12/Y/10V
VSSA
C8
0.1U/6/Y/25V
C9
10U/12/Y/10V
VCOREPLL
L2
4.7UH/8
R536
R537
R538
51/6
TESTHI8_10
TESTHI11
TESTHI12
FOR LAYOUT
RN3
51/8P4R
R20
62/6/X
RN47
51/8P4R
R24
R25
R27
39/6
75/6
150/6
TMS
TDO
TDI
R28
R30
27/6
680/6
TCK
-TRST
VCC3
R9
1K/6
R10
1K/6/X
BSEL0 --->100/133
BSEL0 [15]
BSEL1
TESTHI11
COMP0
COMP1
BPM5
BPM4
BPM3
BPM2
BPM1
BPM0
TESTHI0
DBR#
TESTHI12
GTLREF3
GTLREF2
GTLREF1
GTLREF0
TESTHI5
TESTHI4
TESTHI3
TESTHI2
TESTHI7
TESTHI6
TESTHI1
PWRGOOD
PROCHOT
SLP
TESTHI0_1
CPUPWOK
-PROCHOT
-CPUSLP [12]
TESTHI2_7
TCK
TDI
TDO
TMS
-TRST
SK478/GDW
SIS REQUEST
R13
300/6
C4
100P/6/N/50V/X
CPUPWOK [7]
RN1
56/8P4R
RN2
56/8P4R
INTR
-IGNNE
NMI
-SMI
-STPCLK
-IERR
-CPUSLP
-A20M
-FERR
-IERR [4]
-BREQ0 [4,7]
-CPURST [4,7]
-BREQ0--->220 OHM
R4
R5
R6
51/6
220/6
51/6
BC353
0.1U/6/Y/25V
GIGABYTE
WILLIAMATE 478B
GA-8SIMLH
2.0
Thursday, September 12, 2002
5
32



GIGABYTE			
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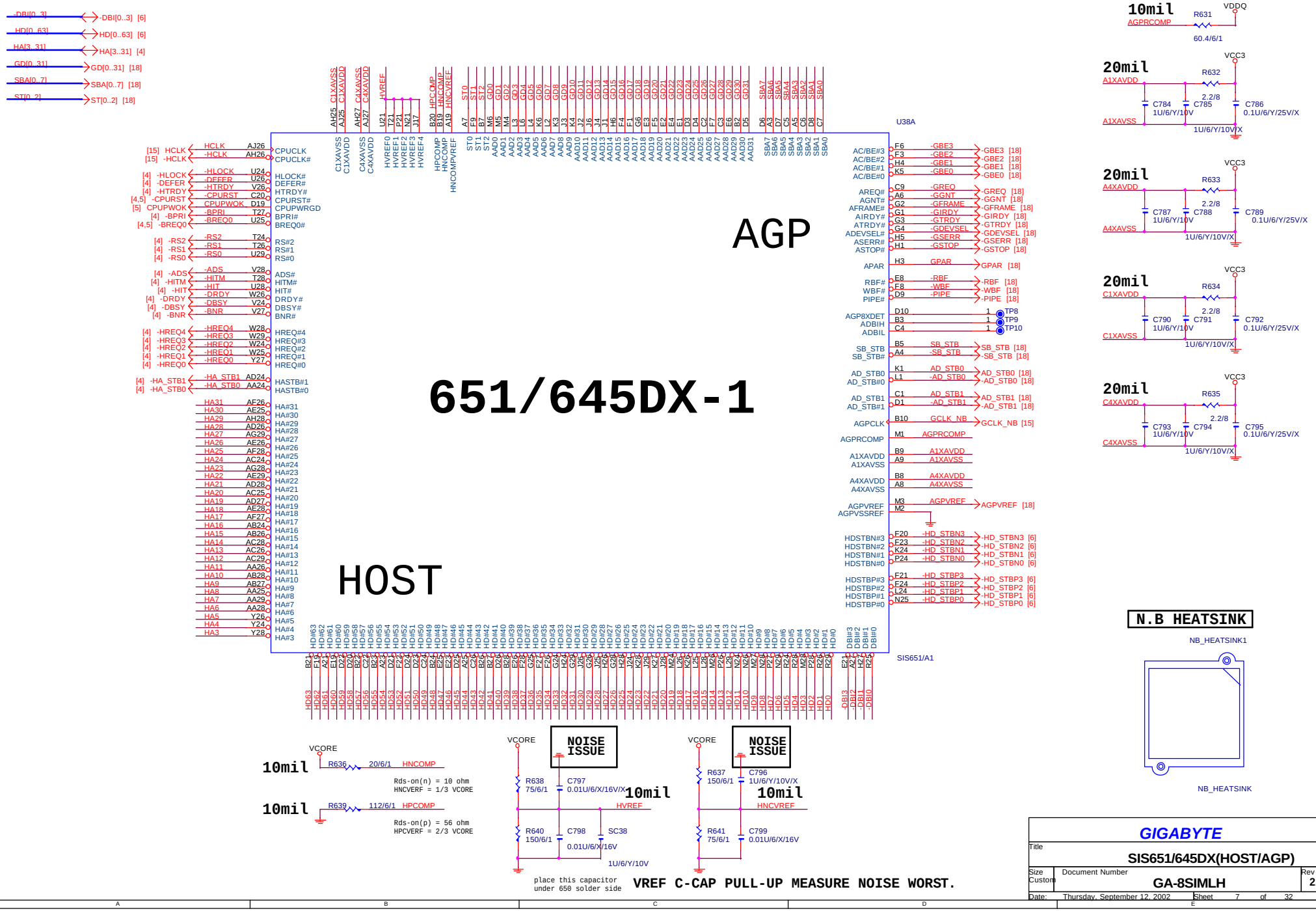
Size: Custom	Document Number: GA-8SIMLH		Rev: 2.0
Date: Thursday, September 12, 2002	Sheet 6 of 32		


651/645DX-1
AGP
HOST
U38A
SIS651/A1
-DBI[0..3] [6]
HD[0..63] [6]
HA[3..31] [4]
GD[0..31] [18]
SBA[0..7] [18]
ST[0..2] [18]
HCLK
-HCLK
CPUCLK
CPUCLK#
-HLOCK
-DEFER
-HTRDY
-CPURST
CPUPWOK
-BPRI
-BREQ0
HLOCK#
DEFER#
HTRDY#
CPURST#
CPUPWRGD
BPRI#
BREQ0#
-RS2
-RS1
-RS0
RS#2
RS#1
RS#0
-ADS
-HITM
-HIT
-DRDY
-DBSY
-BNR
ADS#
HITM#
HIT#
DRDY#
DBSY#
BNR#
-HREQ4
-HREQ3
-HREQ2
-HREQ1
-HREQ0
HREQ#4
HREQ#3
HREQ#2
HREQ#1
HREQ#0
-HA_STB1
-HA_STB0
HASTB#1
HASTB#0
C1XAVSS
C1XAVDD
C4XAVSS
C4XAVDD
HVREF
HPCOMP
HNCOMP
HNCOMPVREF
ST0
ST1
ST2
AGPCLK
AGPRCOMP
A1XAVDD
A1XAVSS
A4XAVDD
A4XAVSS
AGPVREF
AGPVSSREF
-GBE3
-GBE2
-GBE1
-GBE0
-GREQ
-GGNT
-GFRAME
-GIRDY
-GTRDY
-GDEVSEL
-GSERR
-GSTOP
GPAR
-RBF
-WBF
-PIPE
-SB_STB
-AD_STB0
-AD_STB1
GCLK_NB
-HD_STBN3
-HD_STBN2
-HD_STBN1
-HD_STBN0
-HD_STBP3
-HD_STBP2
-HD_STBP1
-HD_STBP0
10mil
R631
AGPRCOMP
VDDQ
60.4/6/1
20mil
R632
R633
R634
R635
A1XAVDD
A4XAVDD
C1XAVDD
C4XAVDD
A1XAVSS
A4XAVSS
C1XAVSS
C4XAVSS
C784
C785
C786
C787
C788
C789
C790
C791
C792
C793
C794
C795
1U/6/Y/10V
2.2/8
0.1U/6/Y/25V/X
1U/6/Y/10V/X
VCC3
N.B HEATSINK
NB_HEATSINK1
NB_HEATSINK
VCORE
R636
20/6/1
HNCOMP
Rds-on(n) = 10 ohm
HNCVERF = 1/3 VCORE
R639
112/6/1
HPCOMP
Rds-on(p) = 56 ohm
HPCVERF = 2/3 VCORE
NOISE ISSUE
R638
75/6/1
C797
0.01U/6/X/16V/X
HVREF
R640
150/6/1
C798
SC38
0.01U/6/X/16V
1U/6/Y/10V
R637
150/6/1
C796
1U/6/Y/10V/X
HNCVREF
R641
75/6/1
C799
0.01U/6/X/16V
place this capacitor
under 650 solder side
VREF C-CAP PULL-UP MEASURE NOISE WORST.
GIGABYTE
Title
SIS651/645DX(HOST/AGP)
Size
Custom
Document Number
GA-8SIMLH
Rev
2.0
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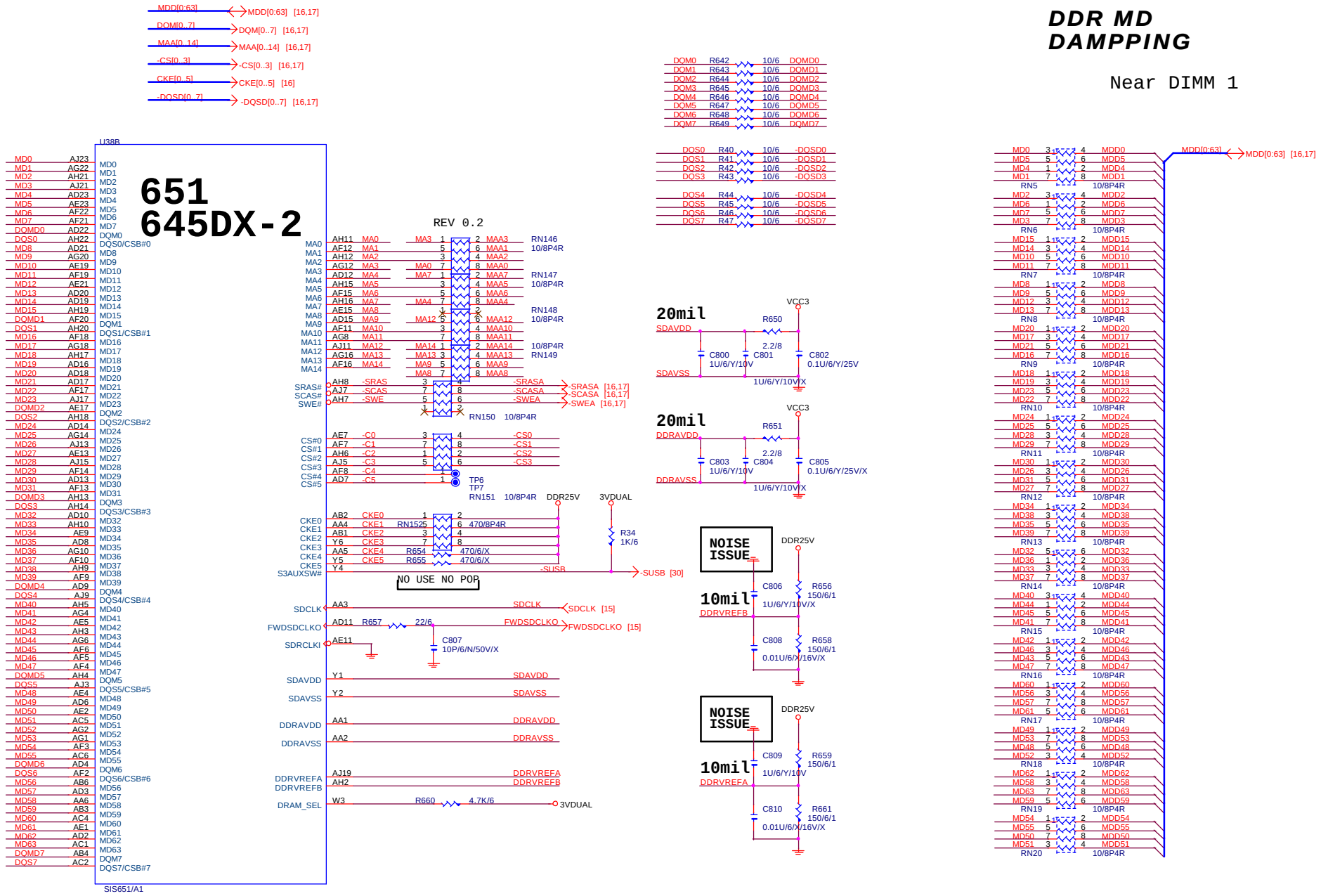
DDR MD DAMPPING

Near DIMM 1



VREF C-CAP PULL-UP MEASURE NOISE WORST.

GIGABYTE			
Title: SIS651/645DX(DDR)			
Size: Custom	Document Number: GA-8SIMLH	Rev: 2.0	
Date: Thursday, September 12, 2002	Sheet 8 of 32		

NOTE: This page is for universal PCB design(suitable for both 645 or 650)

NB Hardware Trap Table

	0	1	Default	embedded pull-low (30~50K Ohm)
DLLEN#	enable PLL	disable PLL	0	yes
DRAM_SEL	SDR	DDR	1(DDR)	yes
TRAP0	normal	NB debug mode	0	yes
TRAP1	TV selection, NTSC/PAL(0/1)		0	
CSYNC	enable VB		0	
RSYNC	enable VGA interrupt		1	
LSYNC	enable panel link		0	

650
645DX-3

HyperZip

U38C

SIS651/A1

NOISE ISSUE

10mil

20mil

REV 0.2 EMI

SIS 645DX NO POP

SIS REQUEST
NO POP

DACAVDD1(VSS)---->DACAVDD2(VSS)
(SIS AP-02)

REV 0.2 SIS CHECK

Title	SIS651/645DX(HYPER ZIP)
Size: Custom	Document Number: GA-8SIMLH
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Date:	Thursday, September 12, 2002
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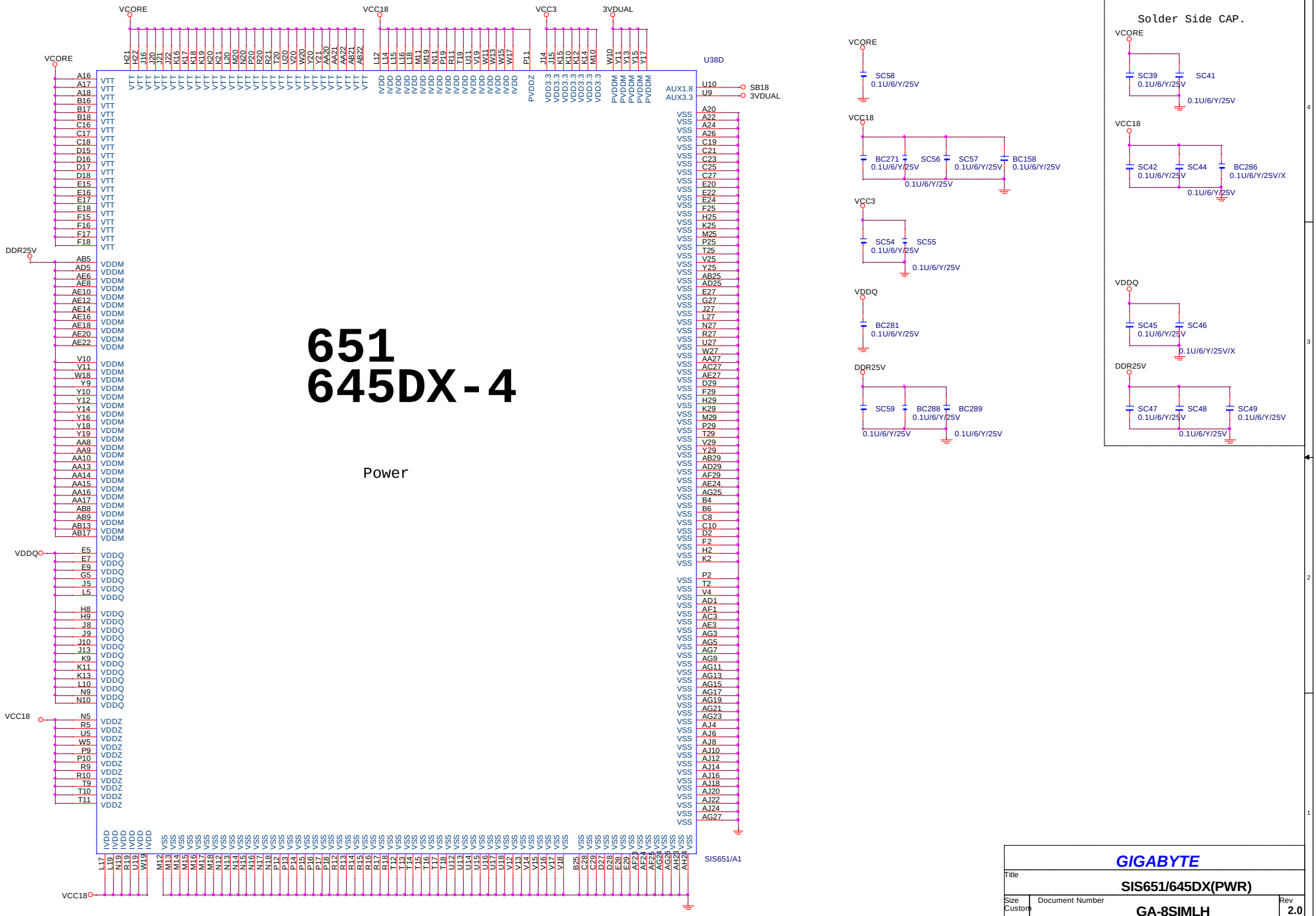
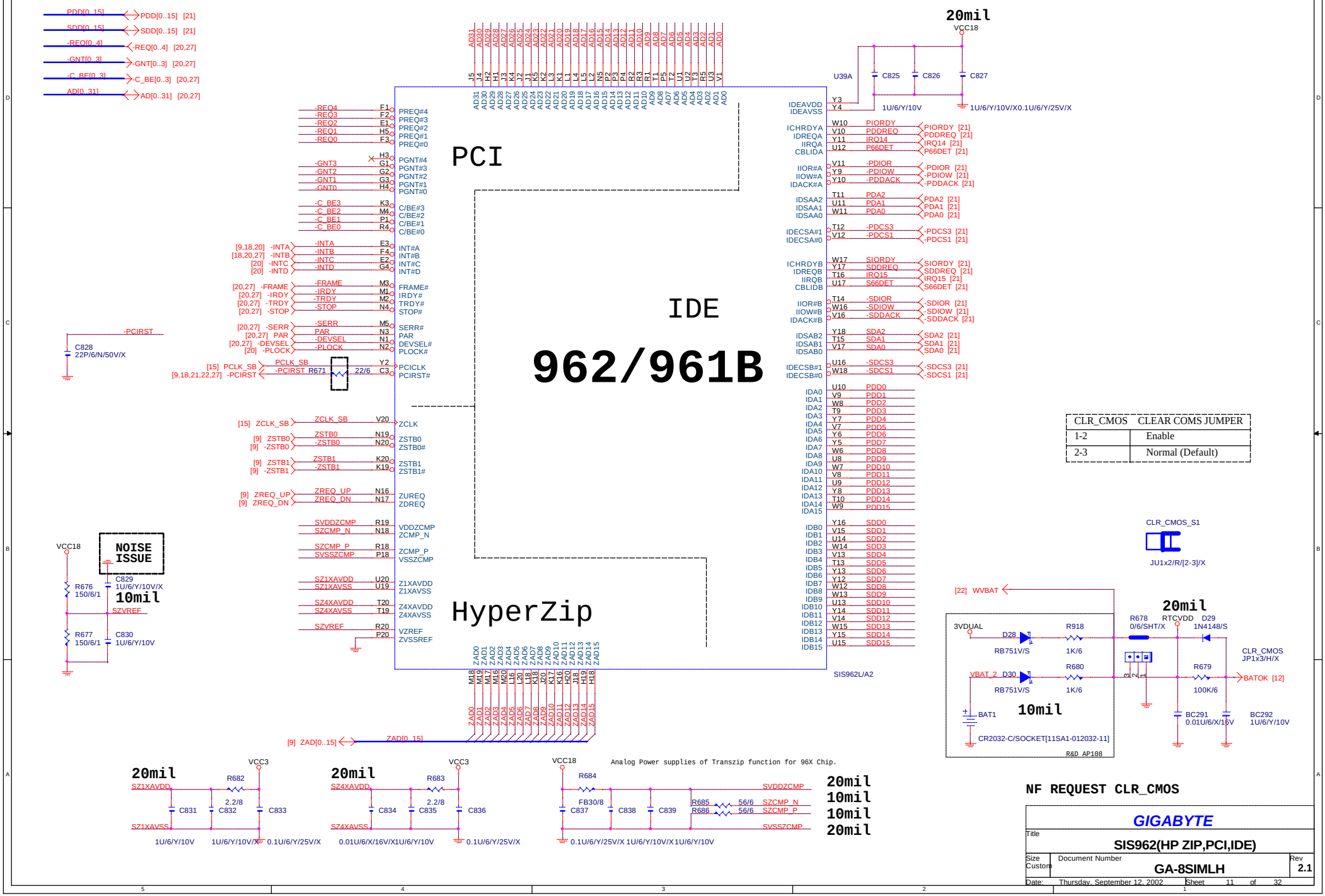


GIGABYTE

Title	SIS651/645DX(PWR)	
Size: Custom	Document Number: GA-8SIMLH	Rev: 2.0
Date: Thursday, September 12, 2002	Sheet 10 of 32	


PCI
IDE
962/961B
HyperZip
SIS962L/A2
PDD[0..15] [21]
SDD[0..15] [21]
-REQ[0..4] [20,27]
-GNT[0..3] [20,27]
-C_BE[0..3] [20,27]
AD[0..31] [20,27]
20mil
VCC18
U39A
C825
C826
C827
1U/6/Y/10V
1U/6/Y/10V/X0.1U/6/Y/25V/X
IDEAVDD
IDEAVSS
ICHRDYA
IDREQA
IIRQA
CBLIDA
IIOR#A
IIOW#A
IDACK#A
IDSAA2
IDSAA1
IDSAA0
IDECSA#1
IDECSA#0
ICHRDYB
IDREQB
IIRQB
CBLIDB
IIOR#B
IIOW#B
IDACK#B
IDSAB2
IDSAB1
IDSAB0
IDECSB#1
IDECSB#0
IDA0
IDA1
IDA2
IDA3
IDA4
IDA5
IDA6
IDA7
IDA8
IDA9
IDA10
IDA11
IDA12
IDA13
IDA14
IDA15
IDB0
IDB1
IDB2
IDB3
IDB4
IDB5
IDB6
IDB7
IDB8
IDB9
IDB10
IDB11
IDB12
IDB13
IDB14
IDB15
-PCIRST
C828
22P/6N/50V/X
PCLK_SB
-PCIRST_R671
22/6
ZCLK_SB
ZSTB0
-ZSTB0
ZSTB1
-ZSTB1
ZREQ_UP
ZREQ_DN
SVDDZCMP
SZCMP_N
SZCMP_P
SVSSZCMP
SZ1XAVDD
SZ1XAVSS
SZ4XAVDD
SZ4XAVSS
SZVREF
ZAD[0..15]
CLR_CMOS
CLEAR COMS JUMPER
1-2
Enable
2-3
Normal (Default)
CLR_CMOS_S1
JU1x2/R/[2-3]/X
NOISE ISSUE
R676
150/6/1
C829
1U/6/Y/10V/X
10mil
R677
150/6/1
C830
1U/6/Y/10V
[22] WVBAT
3VDUAL
D28
RB751V/S
R918
1K/6
VBAT_2
D30
RB751V/S
R680
1K/6
BAT1
CR2032-C/SOCKET[11SA1-012032-11]
R678
0/6/SHT/X
RTCVDD
D29
1N4148/S
R679
100K/6
CLR_CMOS
JP1x3/H/X
BATOK [12]
BC291
0.01U/6/X/16V
BC292
1U/6/Y/10V
R&D AP108
20mil
VCC3
R682
SZ1XAVDD
C831
2.2/8
C832
C833
SZ1XAVSS
1U/6/Y/10V
1U/6/Y/10V/X
0.1U/6/Y/25V/X
R683
SZ4XAVDD
C834
2.2/8
C835
C836
SZ4XAVSS
0.01U/6/X/16V/X
1U/6/Y/10V
0.1U/6/Y/25V/X
Analog Power supplies of Transzip function for 96X Chip.
R684
FB30/8
C837
C838
C839
R685
56/6
SZCMP_N
R686
56/6
SZCMP_P
SVDDZCMP
SVSSZCMP
0.1U/6/Y/25V/X
1U/6/Y/10V/X
1U/6/Y/10V
20mil
10mil
10mil
20mil
NF REQUEST CLR_CMOS
GIGABYTE
Title
SIS962(HP ZIP,PCI,IDE)
Size
Custom
Document Number
GA-8SIMLH
Rev
2.1
Date:
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of
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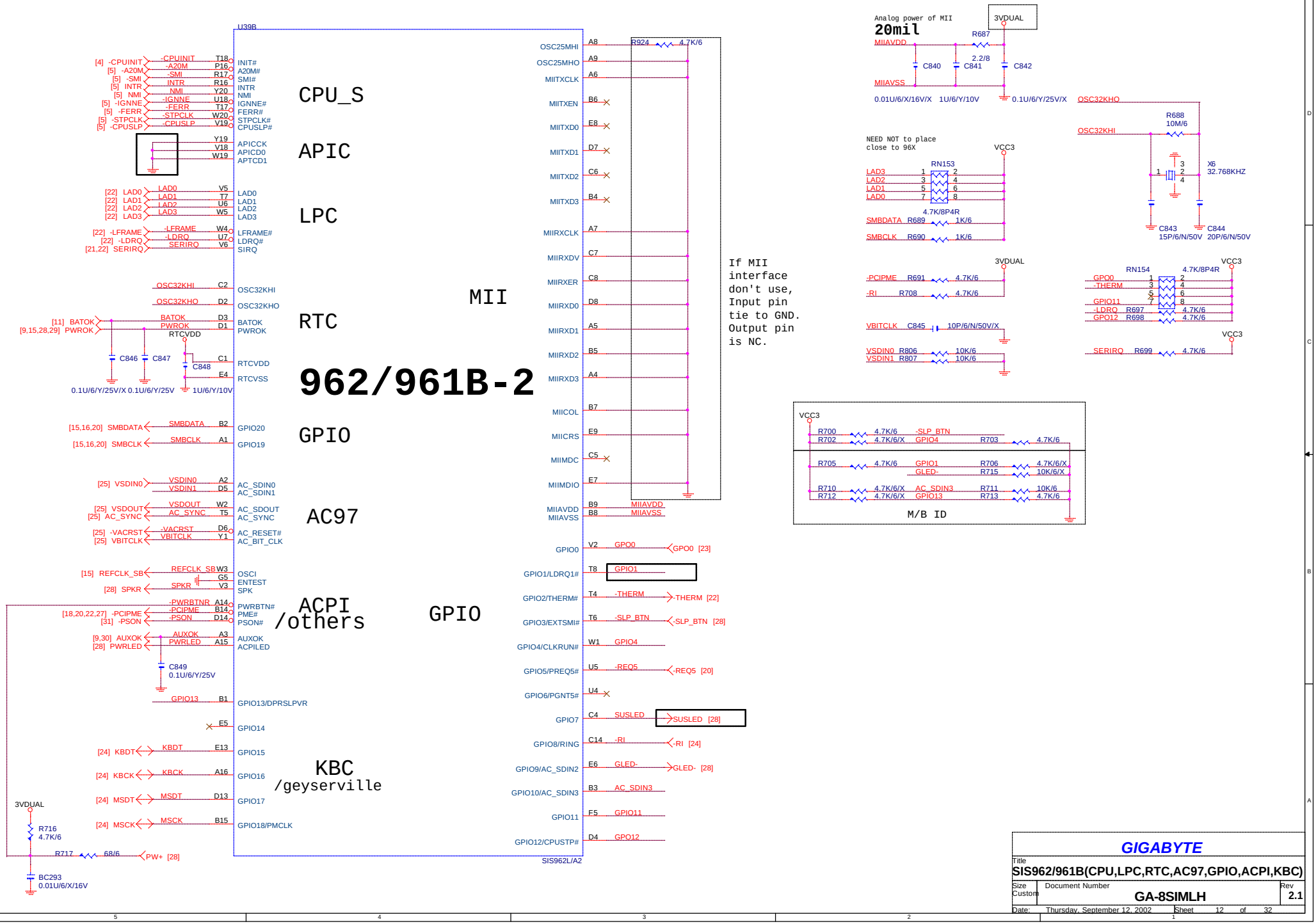
CPU_S
APIC
LPC
MII
RTC
962/961B-2
GPIO
AC97
ACPI
/others
GPIO
KBC
/geyserville
If MII interface don't use, Input pin tie to GND. Output pin is NC.
M/B ID
GIGABYTE
SIS962/961B(CPU,LPC,RTC,AC97,GPIO,ACPI,KBC)
GA-8SIMLH
2.1
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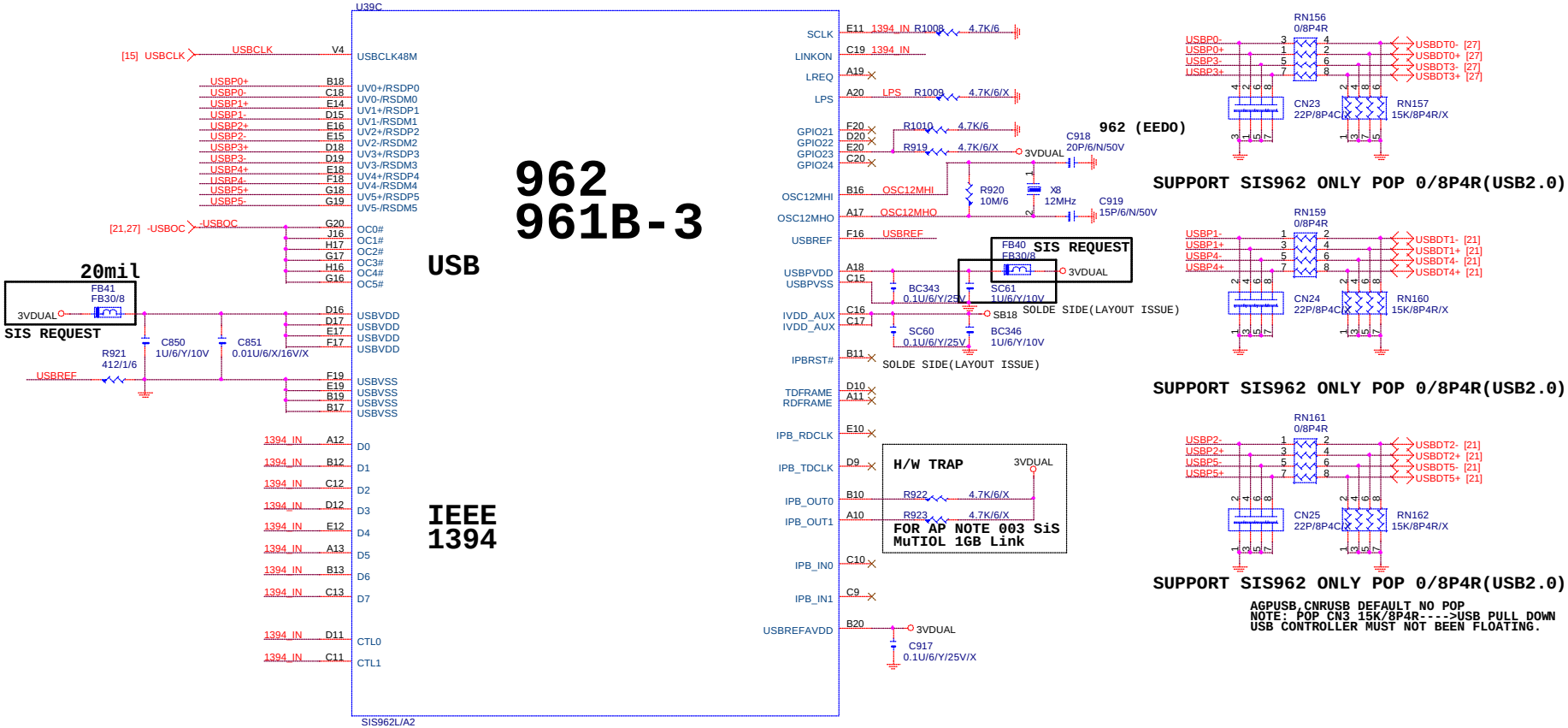
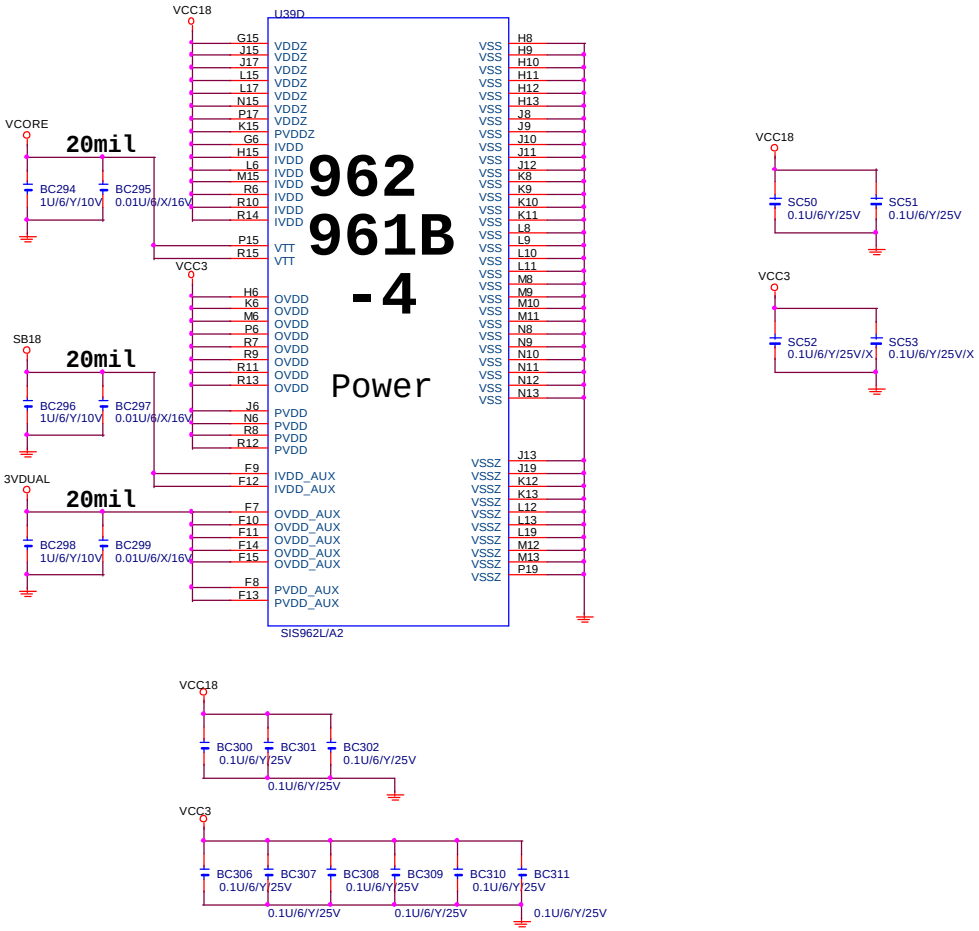
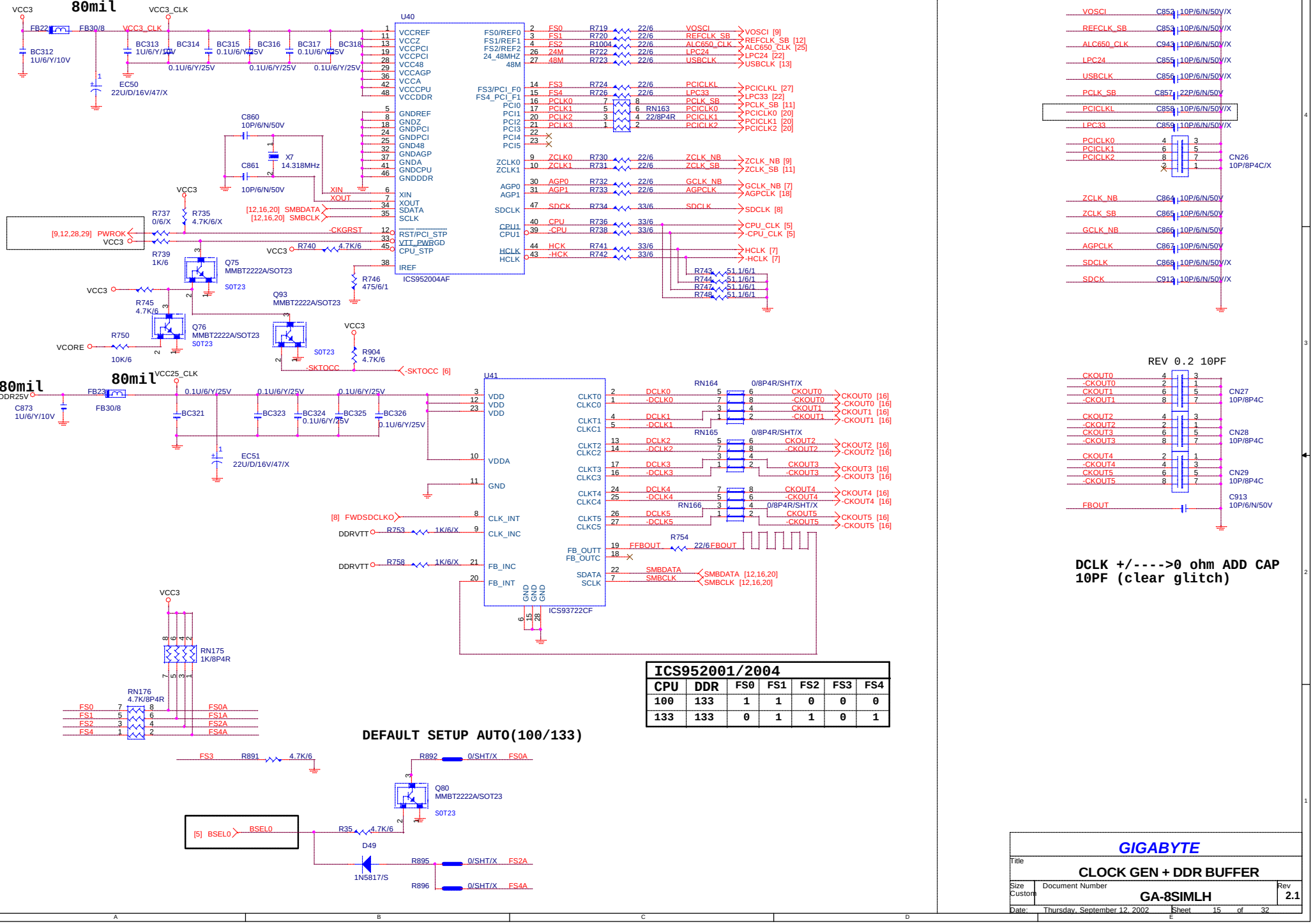


GIGABYTE			
Title	SIS962/961B(USB20,1394)		
Size: Custom	Document Number: GA-8SIMLH	Rev: 2.0	
Date: Thursday, September 12, 2002	Sheet 13 of 32		



GIGABYTE		
Title: SIS962/961B(PWR)		
Size: Custom	Document Number: GA-8SIMLH	Rev: 2.0
Date: Thursday, September 12, 2002	Sheet 14 of 32	



ICS952001/2004						
CPU	DDR	FS0	FS1	FS2	FS3	FS4
100	133	1	1	0	0	0
133	133	0	1	1	0	1

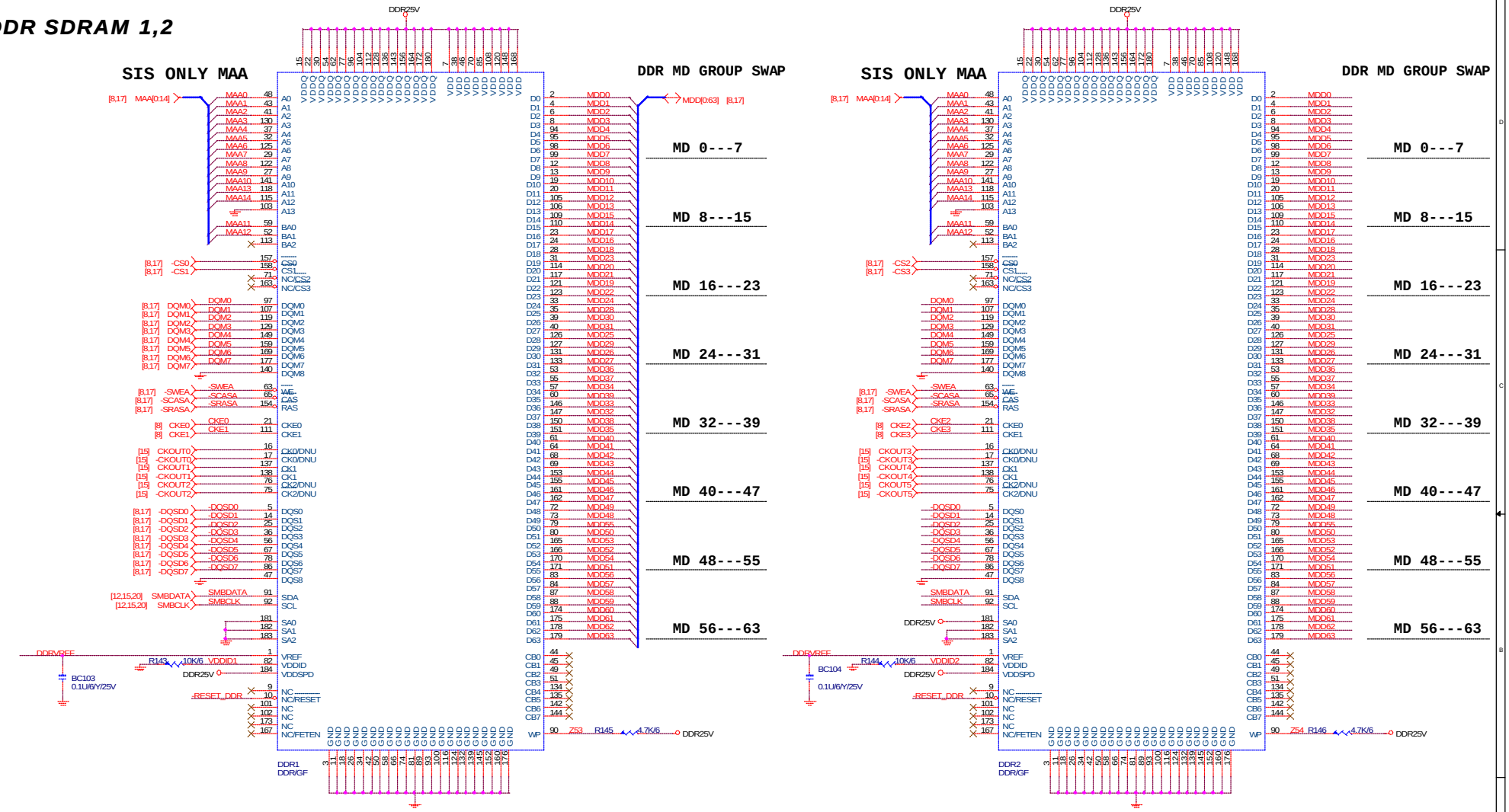
GIGABYTE

Title: CLOCK GEN + DDR BUFFER

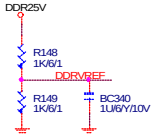
Size: Custom | Document Number: GA-8SIMLH | Rev: 2.1

Date: Thursday, September 12, 2002 | Sheet 15 of 32

DDR SDRAM 1,2



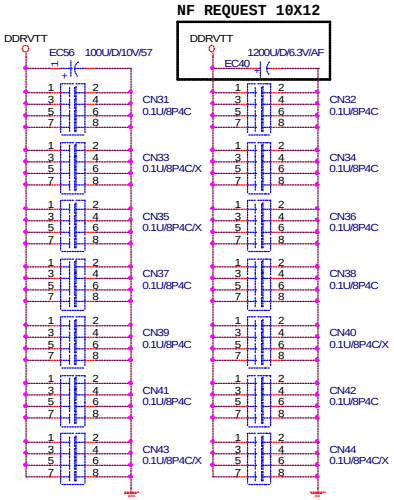
For Register DDR Support



GIGABYTE

Title: DDR UNBUFFERED 1,2		
Size: Custom	Document Number: GA-8SIMLH	Rev: 2.0
Date: Thursday, September 12, 2002	Sheet 16 of 32	

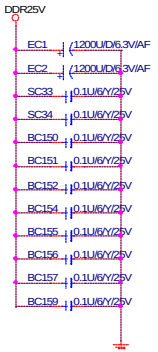
DDRVTT Decouple



R&D NOTE 109 (0.1U/8P4C X9PCS)

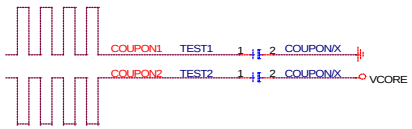
NOTE: Place these decoupling capacitors close to VTT_MEM termination resistors. (one decoupling coapcitor for each two R-packs)

DDR25V Decouple



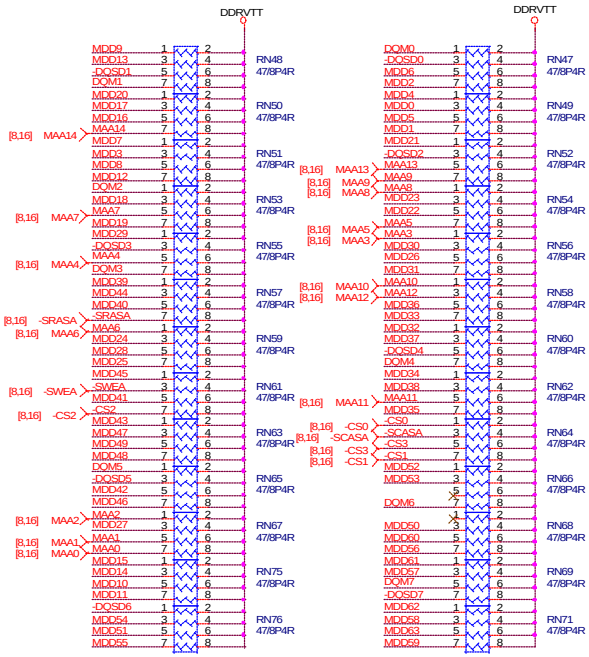
NOTE: Place Detribute 4 pcs per DDR module.

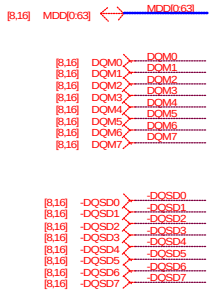
IMPEDENCE TESTING COUPON



DDR TERMINATION

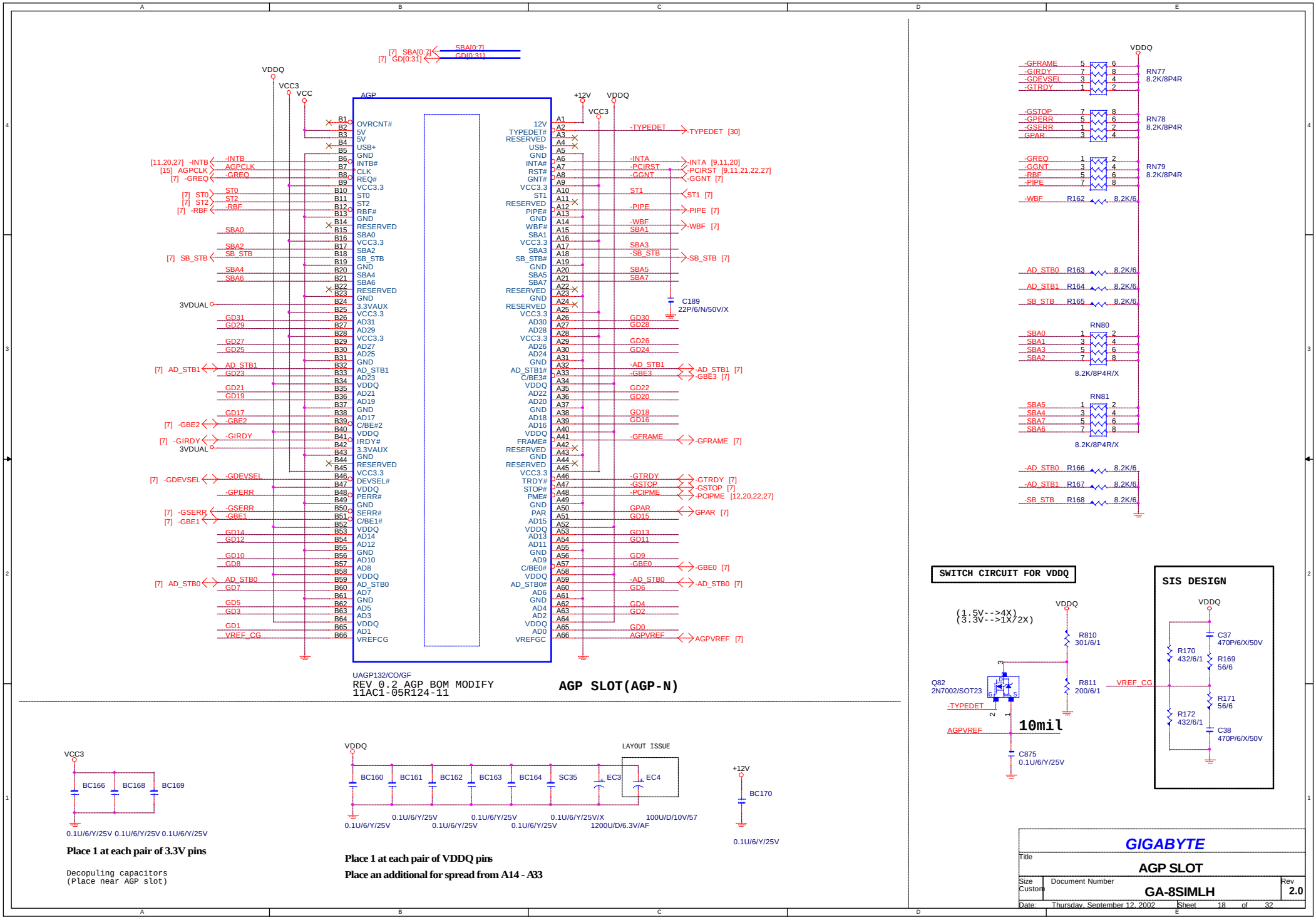
REV 0.2 DDR DIMM ISSUE
33-->47 OHM





GIGABYTE

Title	DDR UNBUFFERED 3	
Size: Custom	Document Number: GA-8SIMLH	Rev: 2.0
Date: Thursday, September 12, 2002	Sheet 17 of 32	


[7] SBA[0:7]
[7] GD[0:31]
SBA[0:7]
GD[0:31]
AGP
VDDQ
VCC3
VCC
+12V
3VDUAL
OVRCNT#
5V
USB+
GND
INTB#
CLK
REQ#
VCC3.3
ST0
ST2
RBF#
RESERVED
SBA0
SBA2
SB_STB
SBA4
SBA6
3.3VAUX
AD31
AD29
AD27
AD25
AD_STB1
AD23
AD21
AD19
AD17
C/BE#2
IRDY#
DEVSEL#
PERR#
SERR#
C/BE1#
AD14
AD12
AD10
AD8
AD_STB0
AD7
AD5
AD3
AD1
VREFCG
12V
TYPEDET#
USB-
INTA#
RST#
GNT#
ST1
PIPE#
WBF#
SBA1
SBA3
SB_STB#
SBA5
SBA7
AD30
AD28
AD26
AD24
AD_STB1#
C/BE3#
AD22
AD20
AD18
AD16
FRAME#
TRDY#
STOP#
PME#
PAR
AD15
AD13
AD11
AD9
C/BE0#
AD_STB0#
AD6
AD4
AD2
AD0
VREFGC
-TYPEDET
-INTA
-PCIRST
-GGNT
ST1
-PIPE
-WBF
SBA1
SBA3
-SB_STB
SBA5
SBA7
GD30
GD28
GD26
GD24
-AD_STB1
-GBE3
GD22
GD20
GD18
GD16
-GFRAME
-GTRDY
-GSTOP
-PCIPME
GPAR
GD15
GD13
GD11
GD9
-GBE0
-AD_STB0
GD6
GD4
GD2
GD0
AGPVREF
-INTB
AGPCLK
-GREQ
ST0
ST2
-RBF
SBA0
SBA2
SB_STB
SBA4
SBA6
3VDUAL
GD31
GD29
GD27
GD25
AD_STB1
GD23
GD21
GD19
GD17
-GBE2
-GIRDY
3VDUAL
-GDEVSEL
-GPERR
-GSERR
-GBE1
GD14
GD12
GD10
GD8
AD_STB0
GD7
GD5
GD3
GD1
VREF_CG
[11,20,27] -INTB
[15] AGPCLK
[7] -GREQ
[7] ST0
[7] ST2
[7] -RBF
[7] SB_STB
[7] AD_STB1
[7] -GBE2
[7] -GIRDY
[7] -GDEVSEL
[7] -GSERR
[7] -GBE1
[7] AD_STB0
-TYPEDET [30]
-INTA [9,11,20]
-PCIRST [9,11,21,22,27]
-GGNT [7]
ST1 [7]
-PIPE [7]
-WBF [7]
-SB_STB [7]
-AD_STB1 [7]
-GBE3 [7]
-GFRAME [7]
-GTRDY [7]
-GSTOP [7]
-PCIPME [12,20,22,27]
GPAR [7]
-GBE0 [7]
-AD_STB0 [7]
AGPVREF [7]
C189
22P/6/N/50V/X
UAGP132/CO/GF
REV 0.2 AGP_BOM MODIFY
11AC1-05R124-11
AGP SLOT(AGP-N)
VDDQ
-GFRAME
-GIRDY
-GDEVSEL
-GTRDY
RN77
8.2K/8P4R
-GSTOP
-GPERR
-GSERR
GPAR
RN78
8.2K/8P4R
-GREQ
-GGNT
-RBF
-PIPE
RN79
8.2K/8P4R
-WBF
R162
8.2K/6
AD_STB0
R163
AD_STB1
R164
SB_STB
R165
RN80
SBA0
SBA1
SBA3
SBA2
8.2K/8P4R/X
RN81
SBA5
SBA4
SBA7
SBA6
8.2K/8P4R/X
-AD_STB0
R166
-AD_STB1
R167
-SB_STB
R168
SWITCH CIRCUIT FOR VDDQ
(1.5V-->4X)
(3.3V-->1X/2X)
R810
301/6/1
R811
200/6/1
Q82
2N7002/SOT23
-TYPEDET
AGPVREF
10mil
C875
0.1U/6/Y/25V
VREF_CG
SIS DESIGN
C37
470P/6/X/50V
R170
432/6/1
R169
56/6
R171
56/6
R172
432/6/1
C38
470P/6/X/50V
VCC3
BC166
BC168
BC169
0.1U/6/Y/25V 0.1U/6/Y/25V 0.1U/6/Y/25V
Place 1 at each pair of 3.3V pins
Decoupling capacitors
(Place near AGP slot)
VDDQ
LAYOUT ISSUE
BC160
BC161
BC162
BC163
BC164
SC35
EC3
EC4
0.1U/6/Y/25V
0.1U/6/Y/25V
0.1U/6/Y/25V
0.1U/6/Y/25V
0.1U/6/Y/25V
0.1U/6/Y/25V/X
100U/D/10V/57
1200U/D/6.3V/AF
Place 1 at each pair of VDDQ pins
Place an additional for spread from A14 - A33
+12V
BC170
0.1U/6/Y/25V
GIGABYTE
Title
AGP SLOT
Size
Custom
Document Number
GA-8SIMLH
Rev
2.0
Date: Thursday, September 12, 2002
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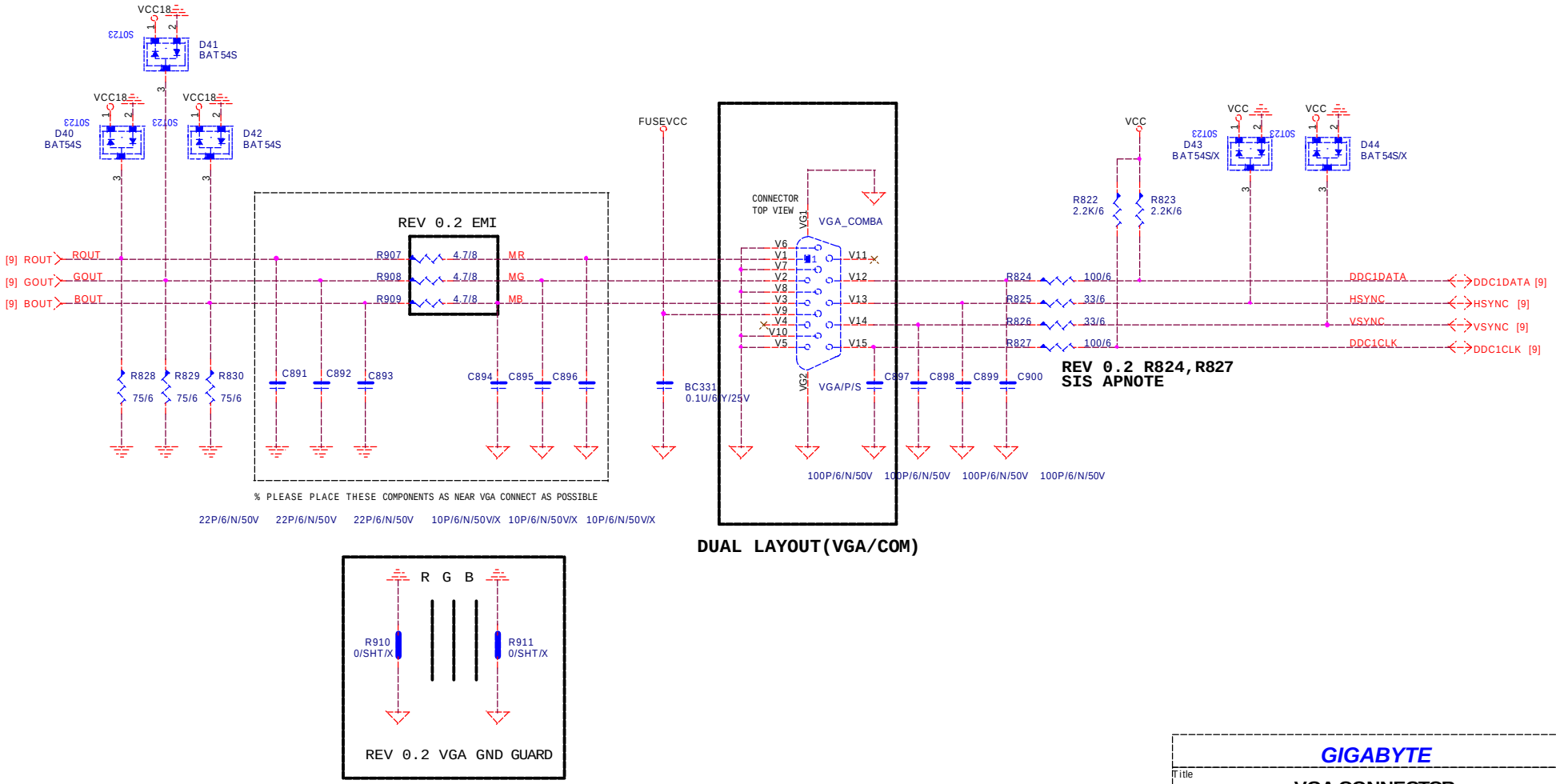
VGA CONNECTOR 1

SIS 645DX NO POP

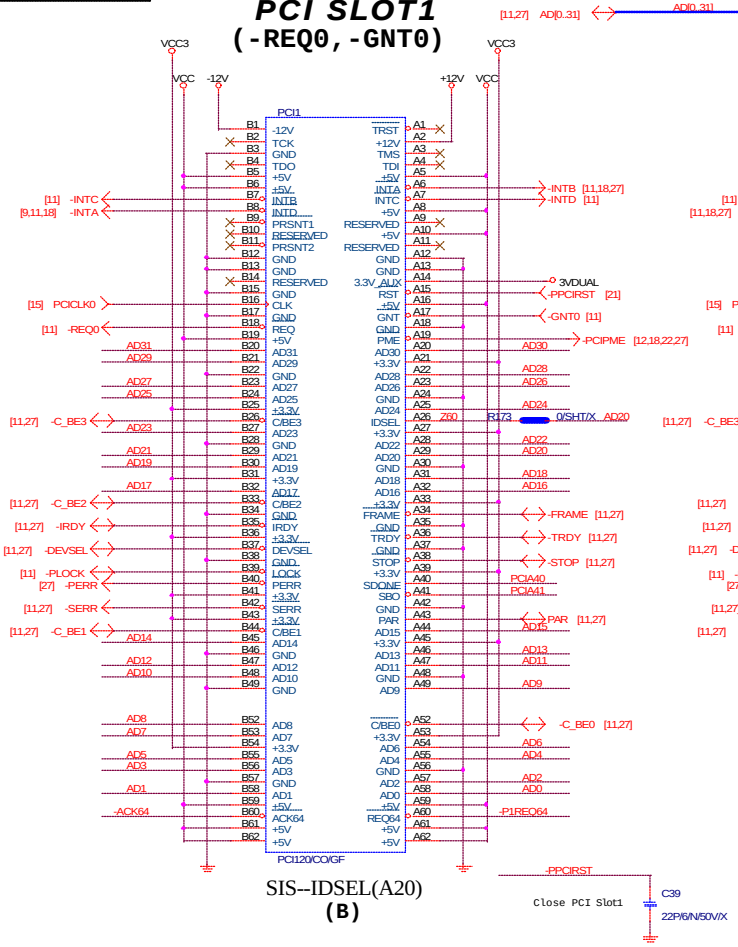


DUAL LAYOUT(VGA/COM)

GIGABYTE		
Title: VGA CONNECTOR		
Size: B	Document Number: GA-8SIMLH	Rev: 2.0
Date: Thursday, September 12, 2002	Sheet 19 of 32	

PCI SLOT 1,2,3

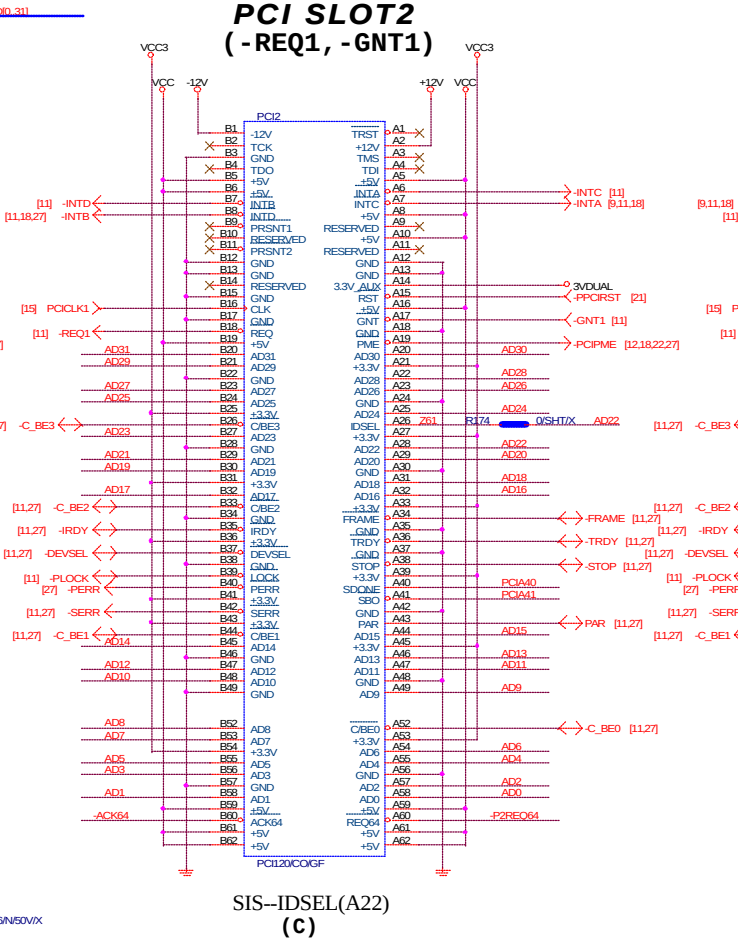
PCI SLOT1 (-REQ0,-GNT0)



SIS--IDSEL(A20)

(B)

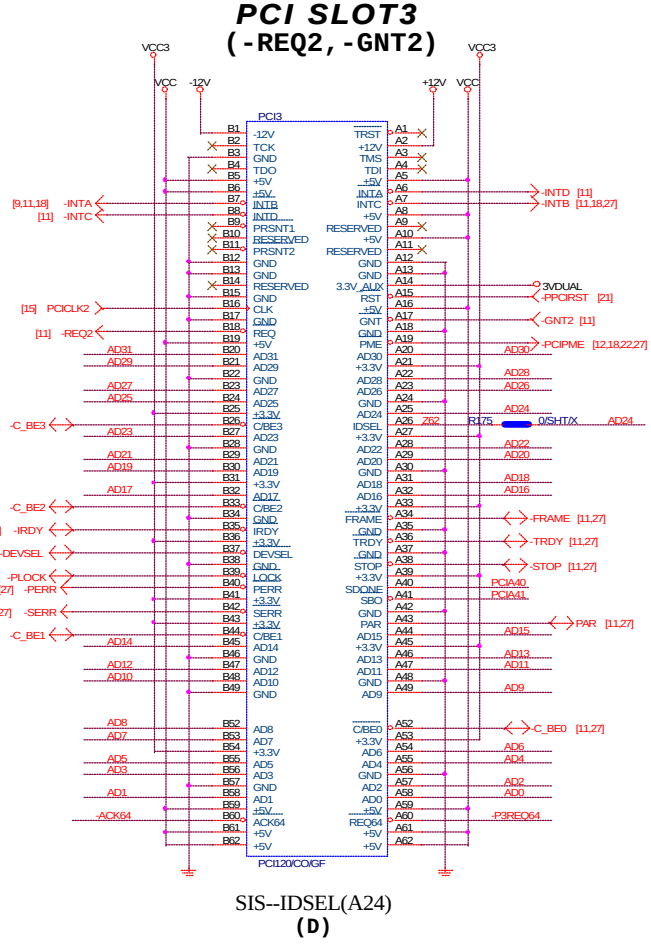
PCI SLOT2 (-REQ1,-GNT1)



SIS--IDSEL(A22)

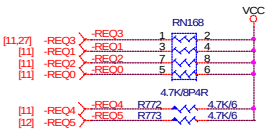
(C)

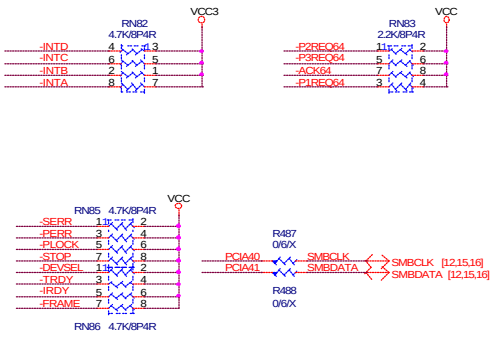
PCI SLOT3 (-REQ2,-GNT2)

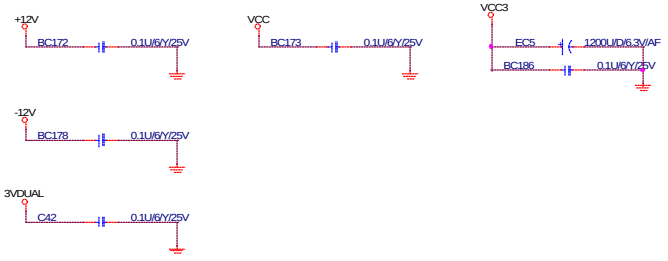


SIS--IDSEL(A24)

(D)



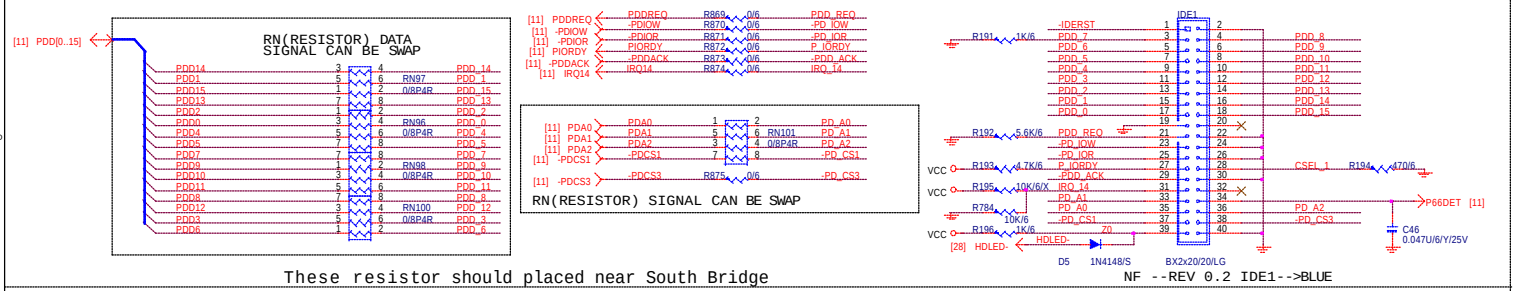




GIGABYTE

Title	PCI SLOT 1,2,3	
Size: Custom	Document Number: GA-8SIMLH	Rev: 2.0
Date: Thursday, September 12, 2002	Sheet 20 of 32	

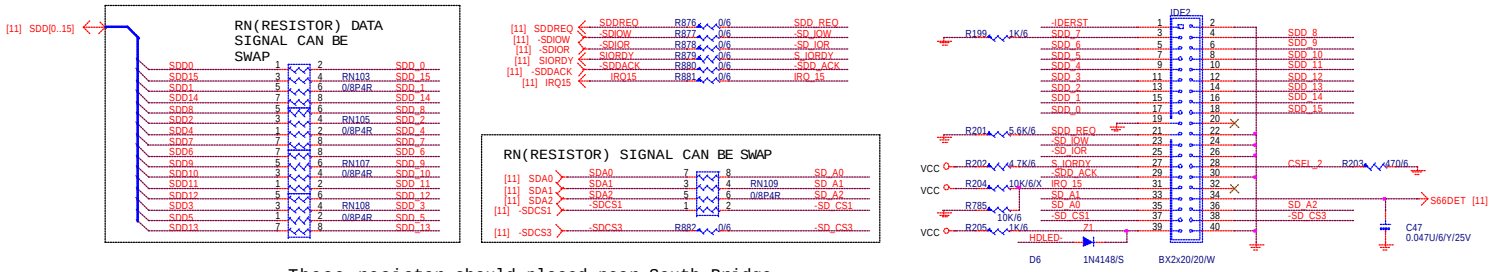
PRIMARY IDE



These resistor should placed near South Bridge

NF --REV 0.2 IDE1-->BLUE

SECONDARY IDE



These resistor should placed near South Bridge

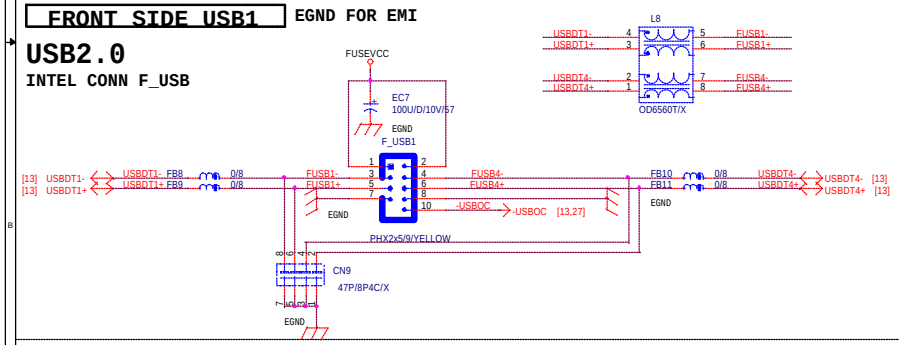
SIRQ

FRONT SIDE USB1

EGND FOR EMI

USB2.0

INTEL CONN F_USB

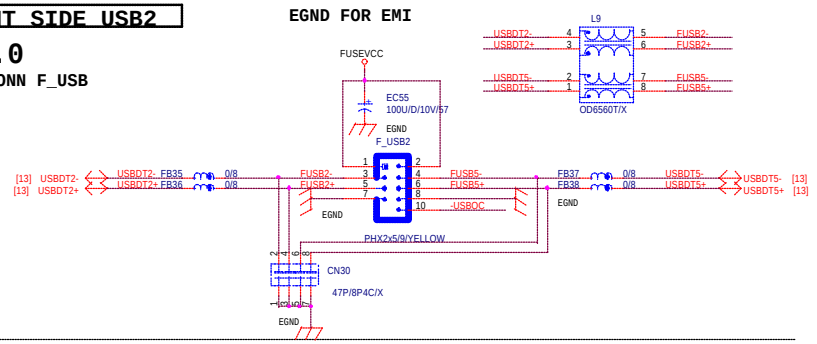


FRONT SIDE USB2

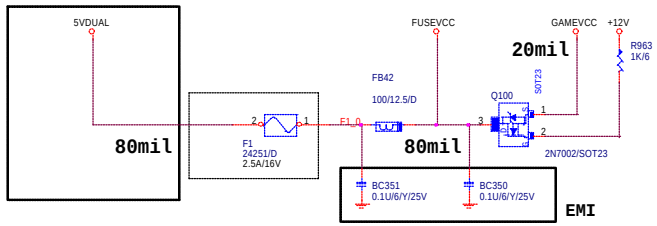
EGND FOR EMI

USB2.0

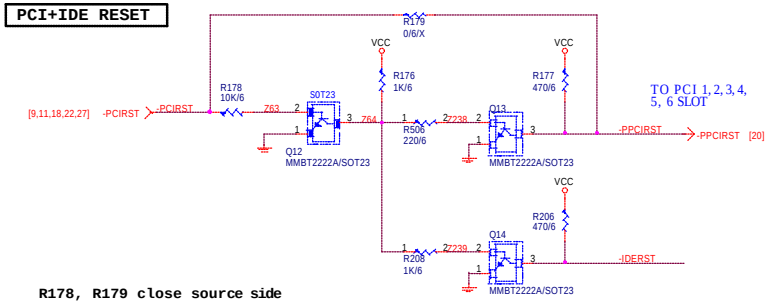
INTEL CONN F_USB



FUSEVCC,GAMEVCC



PCI+IDE RESET



R178, R179 close source side

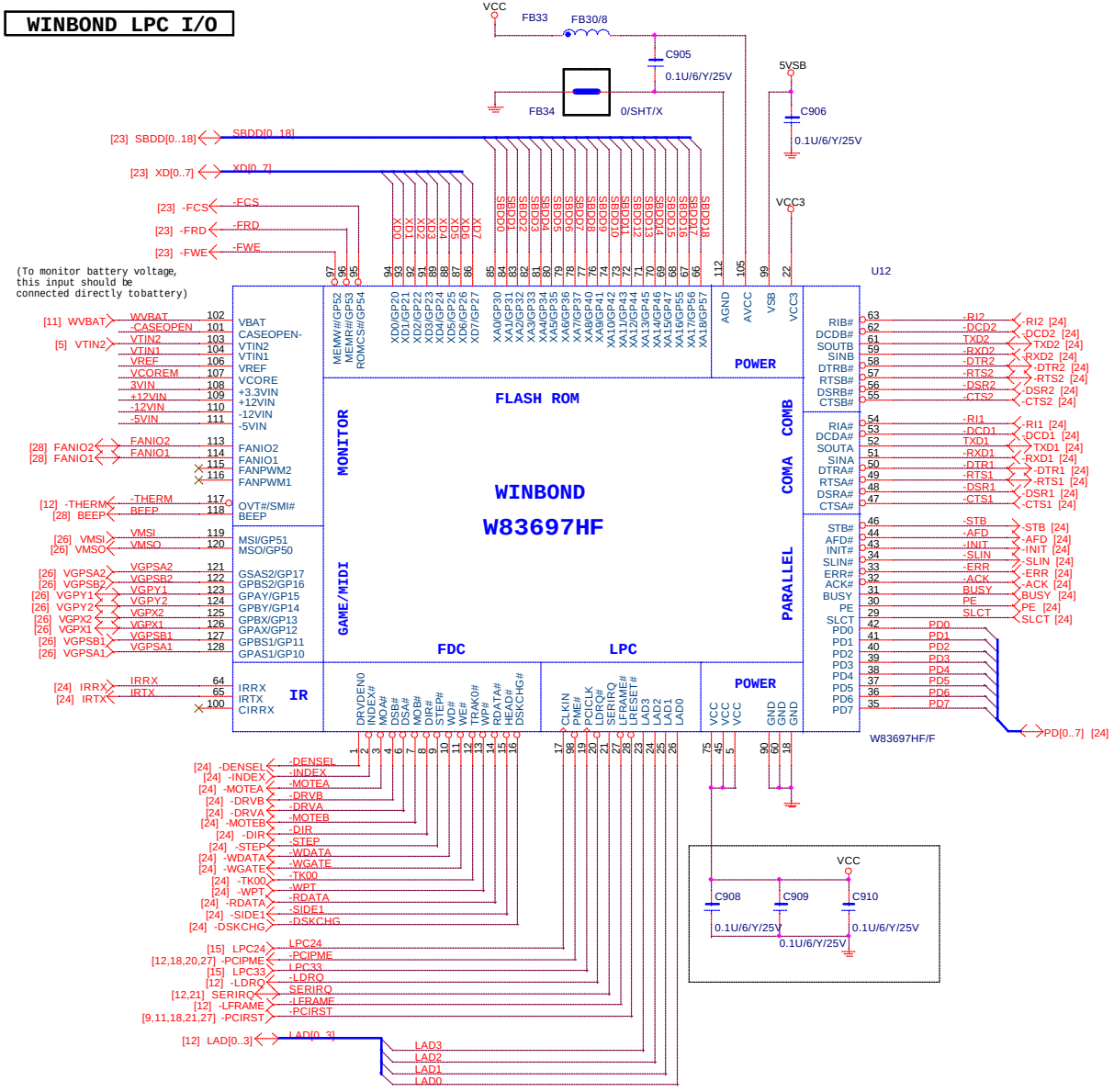
GIGABYTE

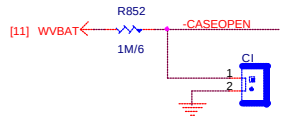
Title: IDE, USB

Size: Custom | Document Number: GA-8SIMLH | Rev: 2.0

Date: Thursday, September 12, 2002 | Sheet 21 of 32

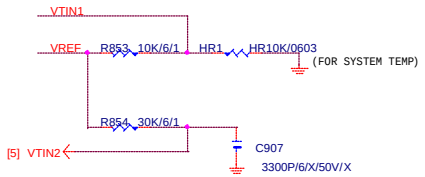
WINBOND LPC I/O



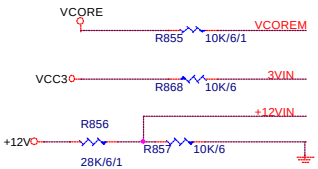


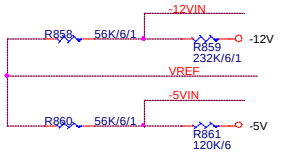
REV 0.2 CI BOM MODIFY

Case Open Circuits



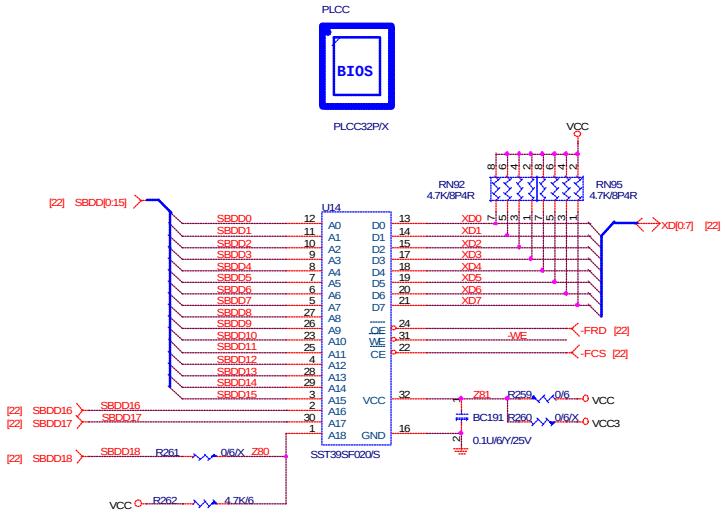
Thermal Monitoring

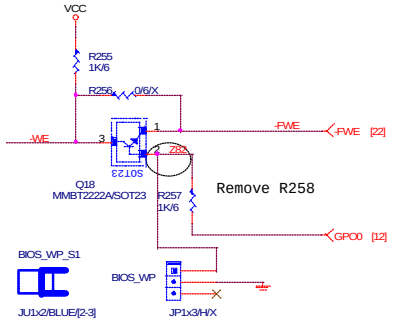




Voltage Monitoring

GIGABYTE		
Title: LPC W83697		
Size: Custom	Document Number: GA-8SIMLH	Rev: 2.0
Date: Thursday, September 12, 2002	Sheet 22 of 32	

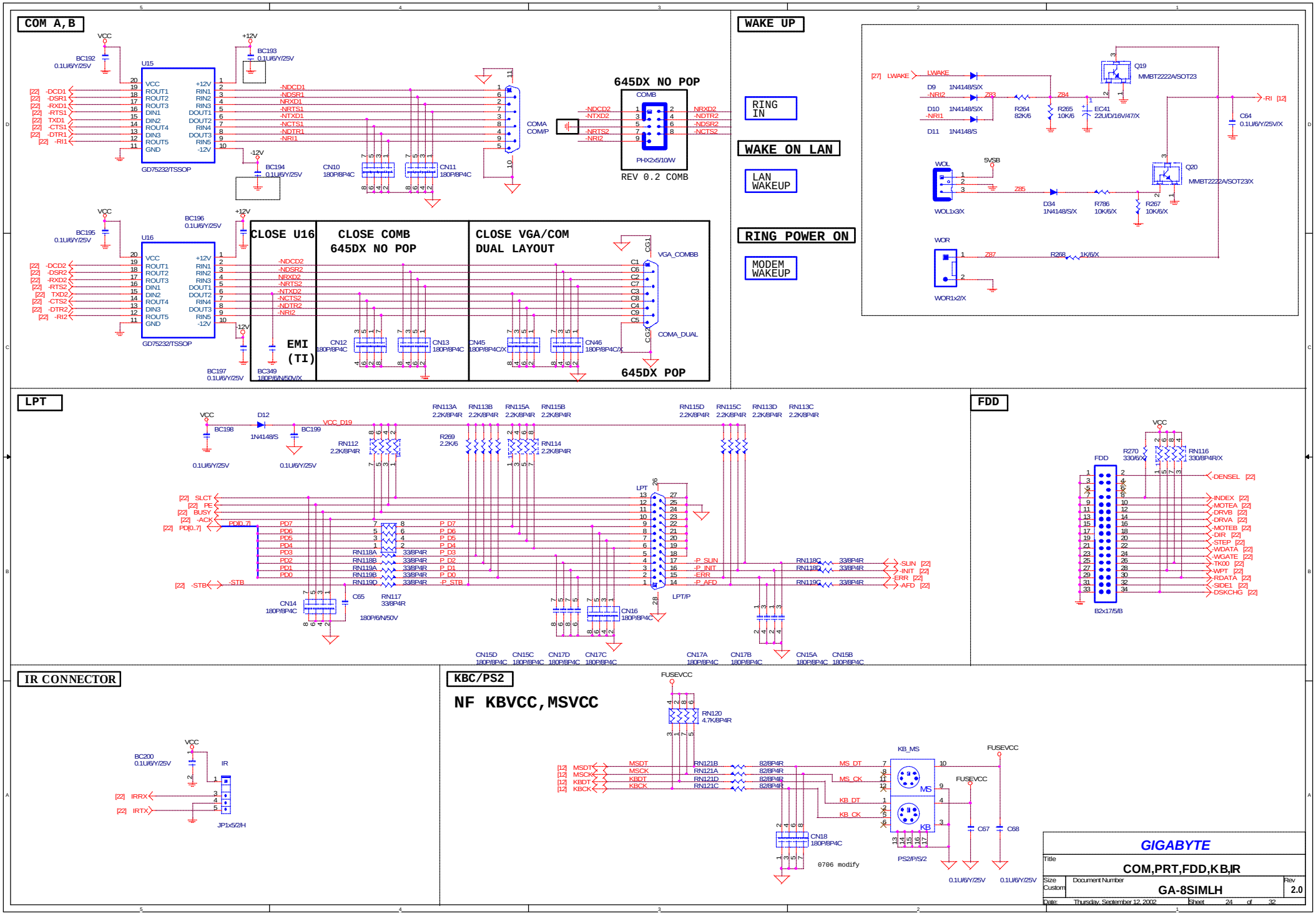


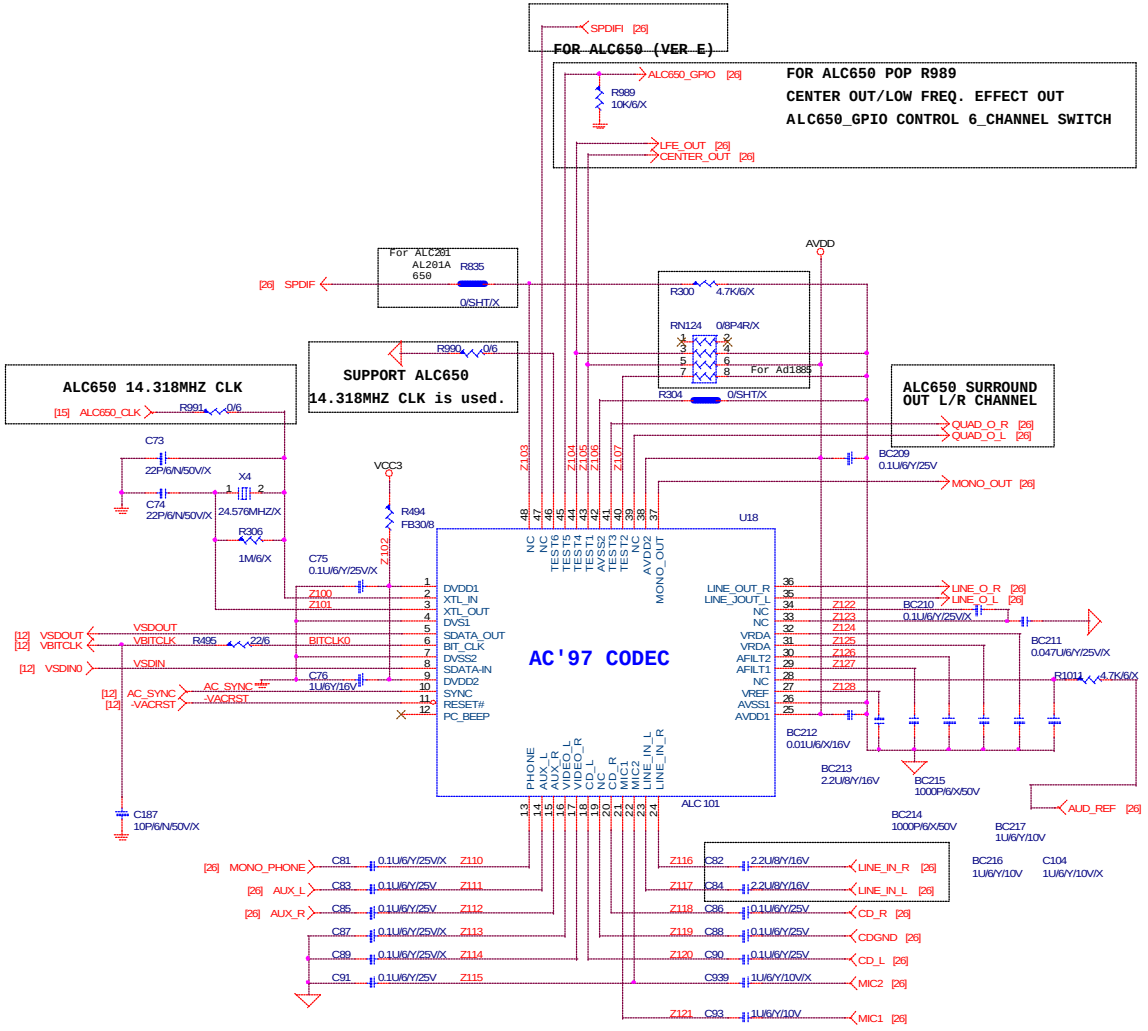


BIOS_WP: BIOS WRITE PROTECT

PIN	BIOS_WP	
1-2	WRITE PROTECT	
2-3	WRITE ENABLE	(default)

GIGABYTE		
Title: Flash ROM		
Size: Custom	Document Number: GA-8SIMLH	Rev: 2.1
Date: Thursday, September 12, 2002	Sheet 23 of 32	


COM A,B
GD75232/TSSOP
645DX NO POP
REV 0.2 COMB
CLOSE U16
CLOSE COMB
645DX NO POP
CLOSE VGA/COM
DUAL LAYOUT
EMI
(TI)
645DX POP
WAKE UP
RING
IN
WAKE ON LAN
LAN
WAKEUP
RING POWER ON
MODEM
WAKEUP
LPT
FDD
IR CONNECTOR
KBC/PS2
NF KBVCC,MSVCC
0706 modify
GIGABYTE
COM,PRT,FDD,KB,IR
GA-8SIMLH
2.0
Thursday, September 12, 2002



NF	SIGMATEL9756
Disti	ALC201A

GIGABYTE

Title: AUDIO (AC97 CODEC)

Size: Custom | Document Number: GA-8SIMLH | Rev: 2.0

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SPDIF

FUSEVCC, SPDIF, SPDIF/B/X, [25] SPDIF — (OUT)

FUSEVCC, SPDIF_I, SPDIF_IN/X, [25] SPDIFI — (IN)

ALC650 SPDIF INPUT
(VER E:SUPPORT)

POP NOISE

DISTI DEFAULT NO POP

[28,29,30,31] PWOK, D14 1N4148/S/X, R321 100K/6/X, Q23 2N2907A/SOT23/X, 3VDUAL, Z131, Z132, Z133, Z134, R313 1K/6/X, R322 1K/6/X, Q22 MMBT2222A/SOT23/X, Q24 MMBT2222A/SOT23/X, SOT23, FLOR, FLOL

LINE OUT

EC8,9,10,11不可DUAL LAYOUT

[25] QUAD_O_R, [25] LINE_O_R, [25] LINE_O_L, [25] QUAD_O_L, SUR_OUTR R992 0/6/X, SUR_OUTL R997 0/6/X, EC8 100U/D/10V/57/X, EC9 100U/D/10V/57, EC10 100U/D/10V/57, EC11 100U/D/10V/57/X, R993 0/6/X, R994 0/6, R995 0/6, R996 0/6/X, R914 0/6/X, R917 0/6/X, FLOR, FLOL, LNR, LNL, C97 180P/6/N/50V, C98 180P/6/N/50V, AUDIO_1A, 3RJ+15FEMALE LINE OUT

LINE-IN

[25] LINE_IN_R, [25] LINE_IN_L, R327 10K/6, R330 10K/6, R529 8.2K/6/X, R530 8.2K/6/X, C102 1000P/6/X/50V, C103 1000P/6/X/50V, AUDIO_1B, 3RJ+15FEMALE LINE-IN

SUR_CEN

SUR_OUTL, SUR_OUTR, [25] CENTER_OUT, LFE_OUT [25], C940 1U/6/Y/10V/X, C941 1U/6/Y/10V/X, H2X3/4/H/X

+12V, R998 47K/6/X, Q102 MMBT2222A/SOT23/X, Q103 2N7002/SOT23/X, SOT23, AVDD, VCC3, R999 4.7K/6/X, [25] ALC650_GPIO, R1000 100/6/X, EC57 22U/D/16V/47/X, R1001 0/6/X RESERVE, R1002 10K/6/X, BC352 1U/6/Y/10V/X RESERVE, MIC

INTEL FRONT AUDIO

AVDD, R925 10K/6, BC348 Reseved, BC347 0.1U/6/Y/50V/X, F_AUDIO, MIC, AUD_REF, FLOR, FLOL, LNR, LNL, KEY, JP2x5/8/H, Not Drill on pin8

F_AUDIO_S1, JU1x2/G/[5-6]

F_AUDIO_S2, JU1x2/G/[9-10]

MIC

ONLY ALC650 FOR LFE OUTPUT POP R

[25] MIC2, R1003 3.3K/6/X, C942 1000P/6/X/50V/X, AVDD, R335 2.2K/6/X, C105 1U/6/Y/10V, [25] AUD_REF, R336 10K/6, R337 0/6/X, [25] MIC1, R339 3.3K/6, C181 1000P/6/X/50V, 0703 MODIFY, MIC, C944 180P/6/N/50V, R338 0/6/X, Z137, Z138, AUDIO_1C, 3RJ+15FEMALE MIC, EMI

AUX IN

DISTI DEFAULT NO POP

[25] AUX_L, [25] AUX_R, AUX_IN, C108 1000P/6/X/50V/X, C109 1000P/6/X/50V/X, WF1x4/W

CD IN

[25] CD_L, [25] CD_R, [25] CDGND, CD_IN, C182 1000P/6/X/50V/X, C110 1000P/6/X/50V/X, C111 1000P/6/X/50V/X, WF1x4/B

TELE

DISTI DEFAULT NO POP

[25] MONO_PHONE, [25] MONO_OUT, BC227 0.1U/6/Y/25V/X, C183 1000P/6/X/50V/X, Z140, WF1x4/G/X

GAME PORT

FOR I/O W83697HF

[22] VGPSA1, VGPSB1, VGPX1, VGPX2, VMSO, VGPY2, VGPY1, VGPSB2, VGPSA2, VMSI, RN129C 0/8P4R/SHT/X, RN129D 0/8P4R/SHT/X, RN129B 0/8P4R/SHT/X, RN129A 0/8P4R/SHT/X, RN174 1M/8P4R

R344 4.7K/6/X, R345 4.7K/6/X, GAMEVCC, RN126 2.2K/8P4R, RN130A 2.2K/8P4R, RN130C 2.2K/8P4R, RN130D 2.2K/8P4R, RN130B 2.2K/8P4R, R346 2.2K/6, R347 2.2K/6, GP_SA1, GP_SB1, GP_X1, GP_X2, GP_Y2, GP_Y1, GP_SB2, GP_SA2, MS_0, MS_1

GAME-1, AD/GM, BC230 0.1U/6/Y/25V, BC228 0.1U/6/Y/25V, BC229 0.1U/6/Y/25V

C114 0.01U/6/X/16V, C115 0.01U/6/X/16V, C116 100P/6/N/50V/X, C117 0.01U/6/X/16V, C118 0.01U/6/X/16V, C121 1000P/6/X/50V, C122 180P/6/N/50V, C123 180P/6/N/50V, CN19 180P/8P4C, CN20 0.01U/8P4C

GIGABYTE

Title: AUDIO OUTPUT,GAME PORT

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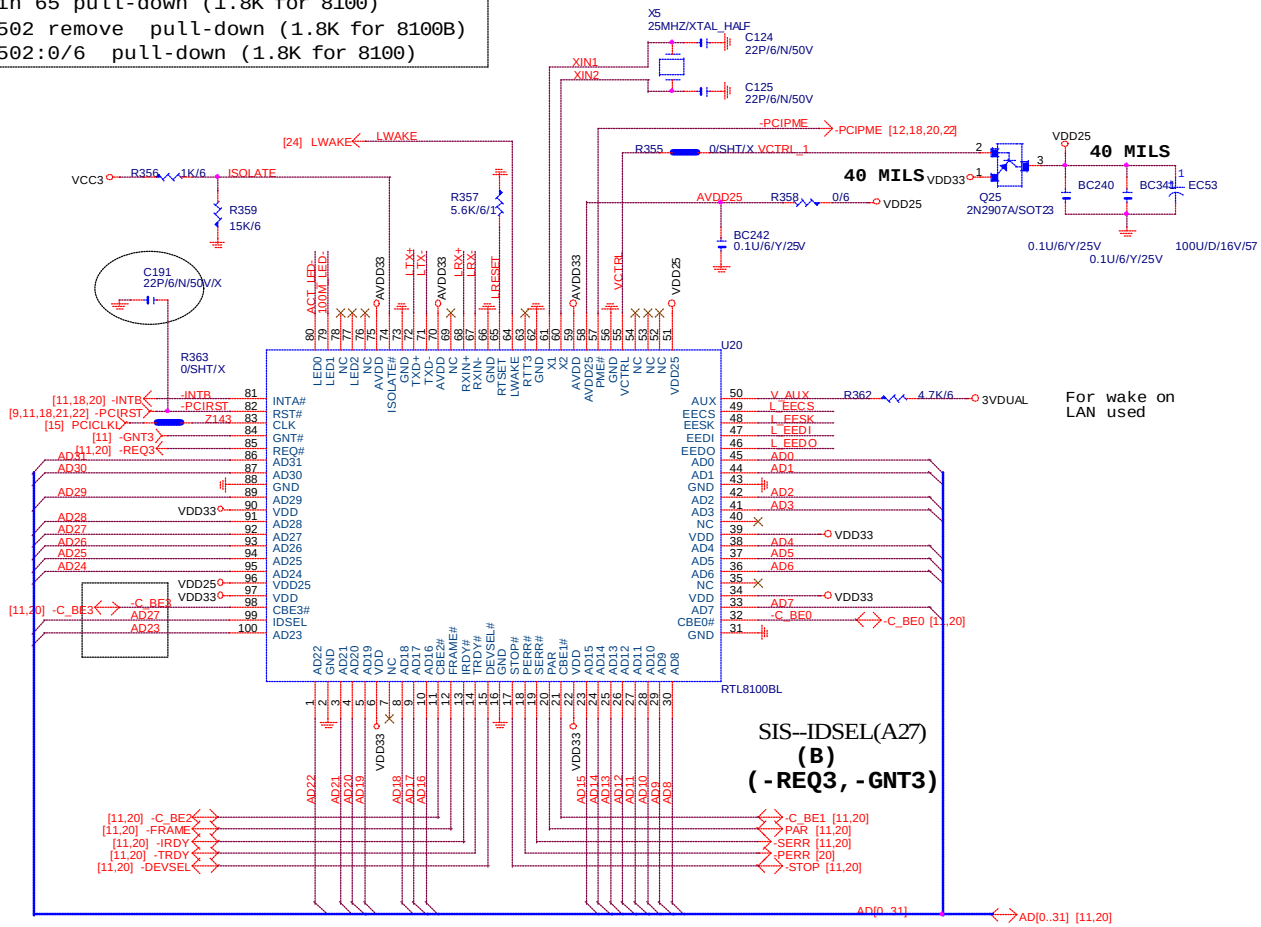
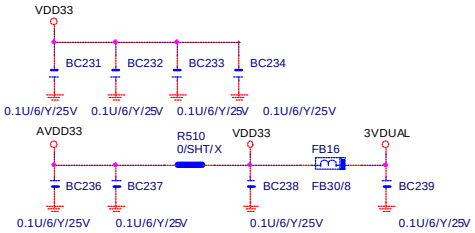
LAN RTL8100 (REALTEK)

8100/8100B NOTE:
Pin 65 pull-down (5.6K for 8100B)
Pin 65 pull-down (1.8K for 8100)
R502 remove pull-down (1.8K for 8100B)
R502:0/6 pull-down (1.8K for 8100)

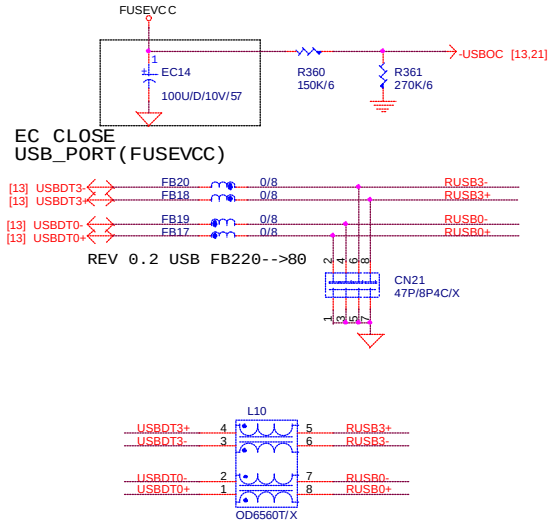


POWER DECOUPLING CAP.

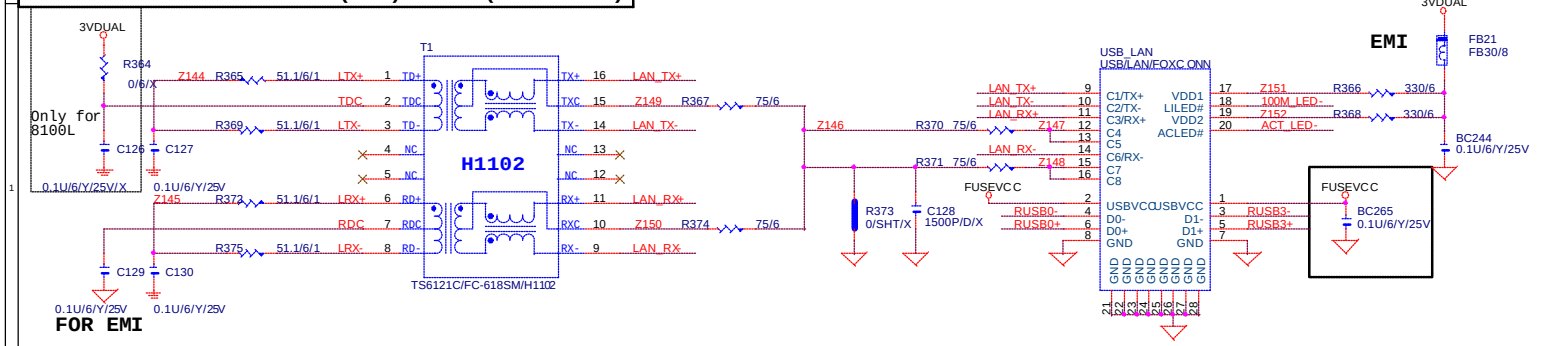


REAR USBX2

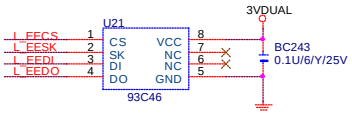
USB2.0



10/100M BASE TRANSFORMER(1:1)+FOXCON(RJ45+USBX2)



LAN EEPROM



GIGABYTE

Title	LAN RTL8100B	
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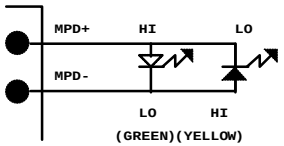
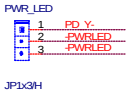
FRONT PANEL



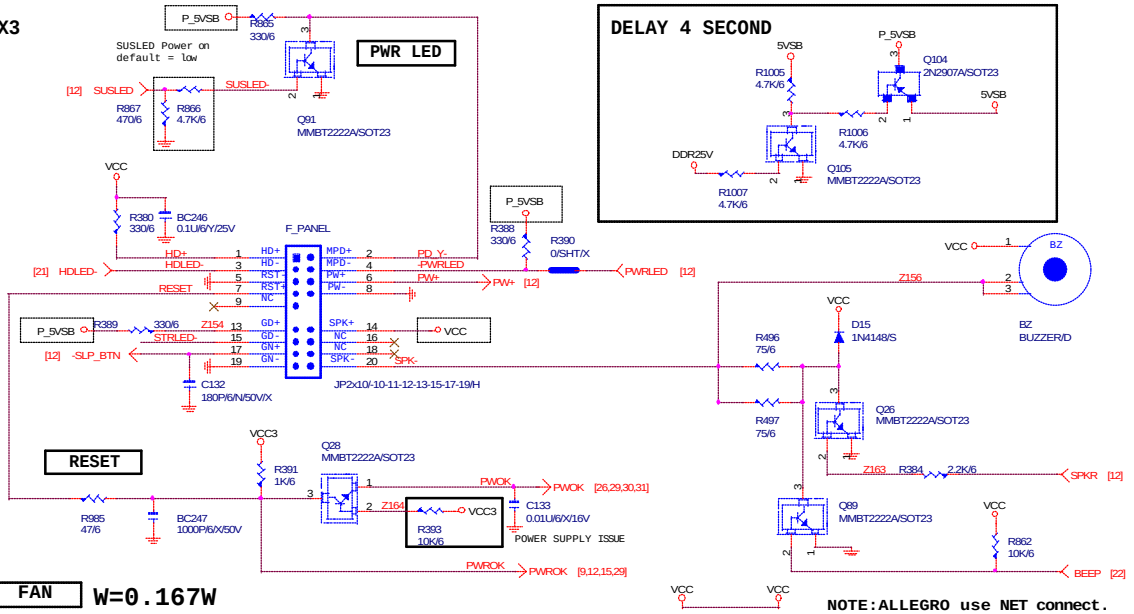
PWR_LED FOR DISTI PIN 1X3 LED USED



LED States	ACPI States	MPD+	MPD-
OFF	S1,S3,S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING

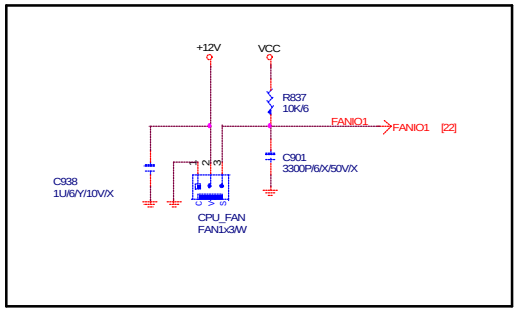
States for a dual-color power LED

LED States	ACPI States	MPD+	MPD-
OFF	S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING
Steady Yellow	S1,S3	LO	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING

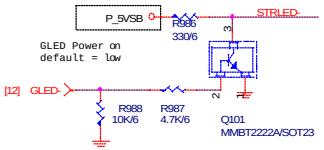


NOTE:ALLEGRO use NET connect.

CPU FAN W=0.167W



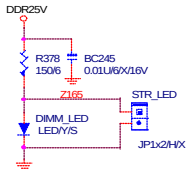
GLED (S3)-->HI



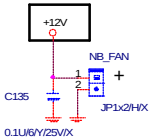
States for green LED

LED States	ACPI States	GLED-
ON	S1,S3	1
OFF	S0,S5	0

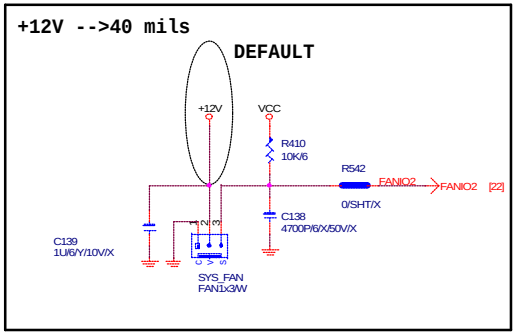
DIMM LED CONN.



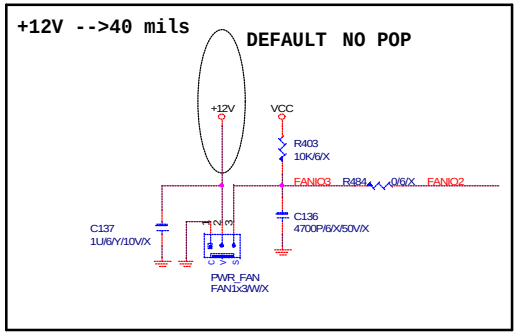
NB HEATSINK FAN



SYSTEM FAN W=0.167W



POWER FAN W=0.167W



GIGABYTE		
Title: PANEL, STR LED & FANS		
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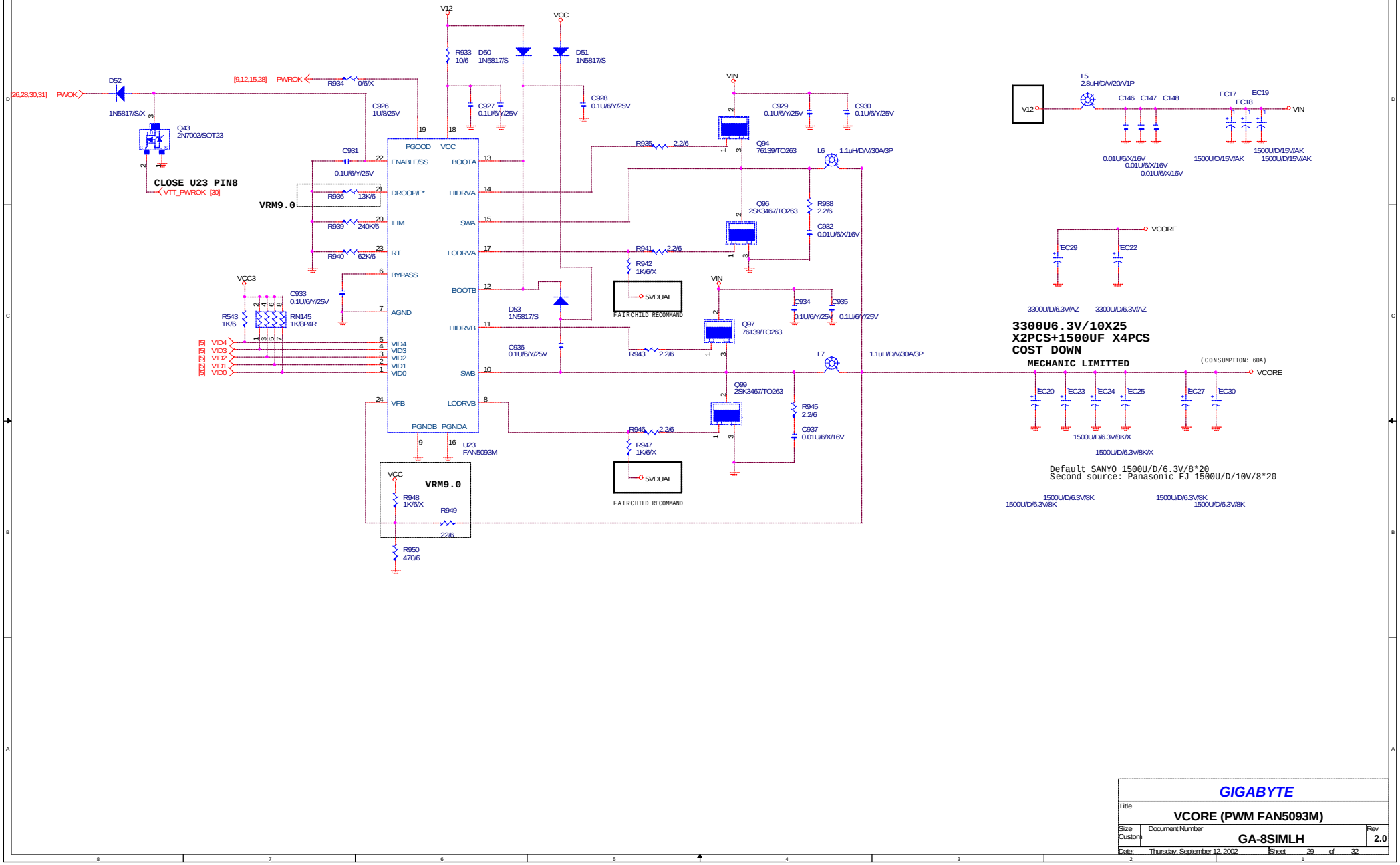

GIGABYTE		
Title: VCORE (PWM FAN5093M)		
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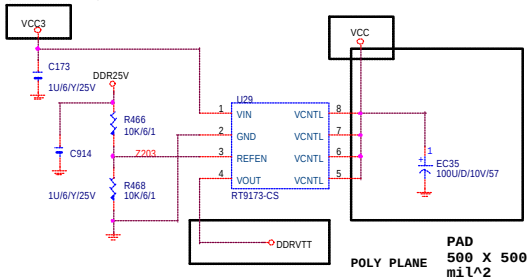
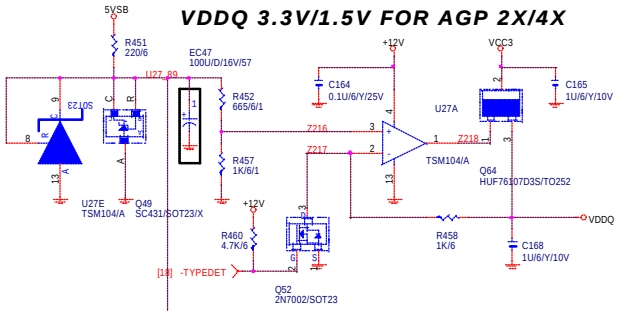
1.25V DDRVTT SWITCHING SOLUTION

SiS645, RT9173 application circuit have to modified.
Because SiS645 had problem in power on state.
If we used the typical circuit, and then there will had surge current during power on.
And then the 2.5Vdual will be failed, system can't boot normally

1. Vin of 9173 had change connect to Vcc3(3.3V from ATX)
2. Vctrl of 9173 had change connect to Vcc(5V from ATX)
3. REF/EN of 9173 remain connect to the resistor divider from 2.5Vdual.
(2.5/2=1.25V)

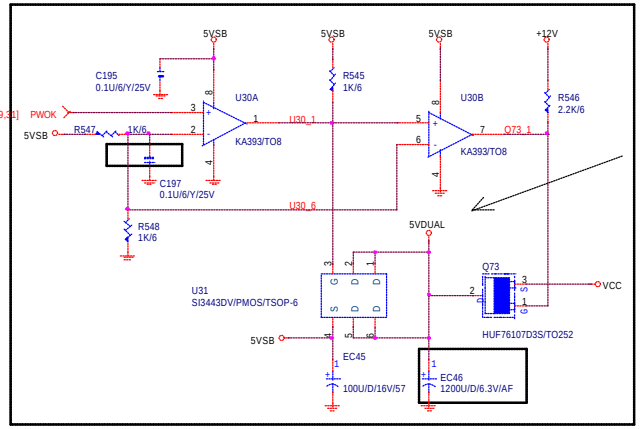


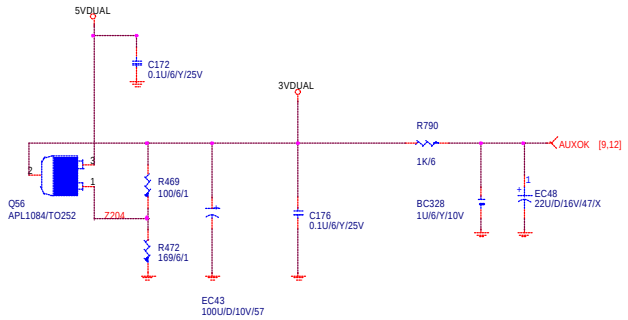
VDDQ 3.3V/1.5V FOR AGP 2X/4X



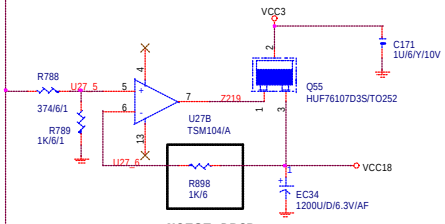
5VDUAL TRANS TO 3VDUAL(3.3V)

5VDUAL 80 mils ABOVE



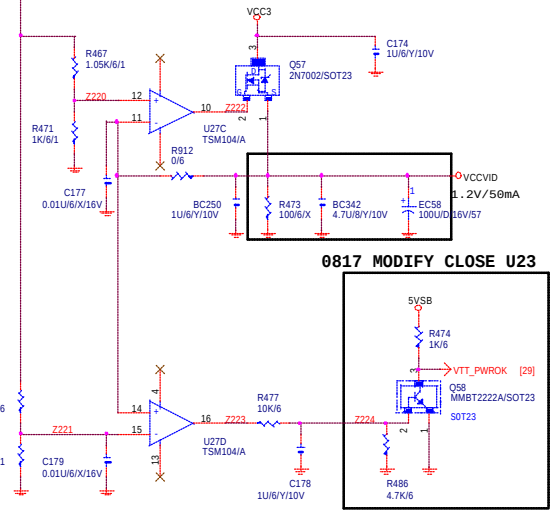


VCC18 FOR NB,SB



NOISE DROP

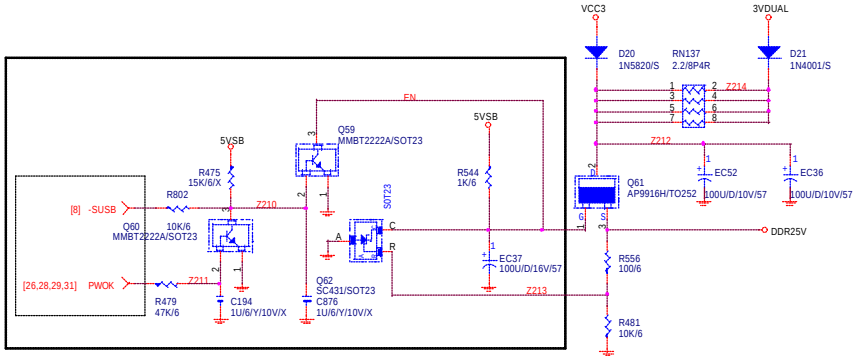
VCCVID FOR NORTHWOOD CPU



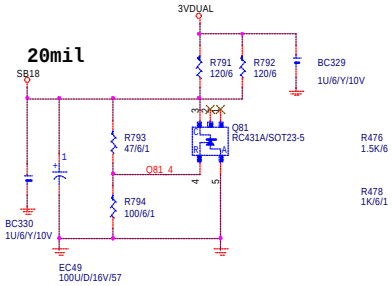
0817 MODIFY CLOSE U23

DDR25V FOR DDR DIMM & NB

AP9916 layout
TO-263 package
for thermal issue



SB18 FOR SB



GIGABYTE		
Title: DDR POWER		
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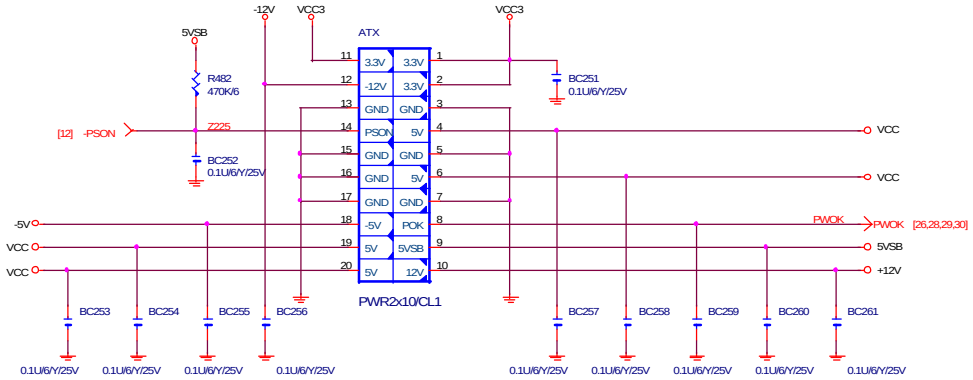
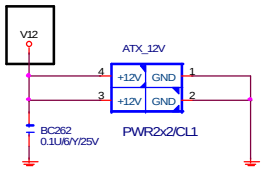
ATX CONN, DC POWER

K1 K_ICT/X — I1 4MMH/X
K2 K_ICT/X — I2 4MMH/X
K3 K_ICT/X — I3 4MMH/X
K4 K_ICT/X — I4 4MMH/X
K5 K_ICT/X
K6 K_ICT/X

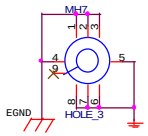
ATX POWER CONNECTOR

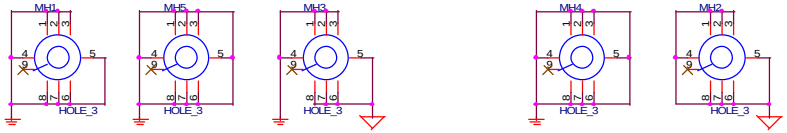




PB REQUEST V12

+12V TRACE
250MIL





GIGABYTE		
Title: ATX, DC POWER		
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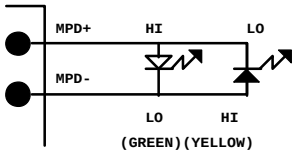
RTL8100L ON-BOARD		
	-REQ0 PCI1	**IDSEL(A20)--B**
	-REQ1 PCI2	**IDSEL(A22)--C**
	-REQ2 PCI3	**IDSEL(A24)--D**
	-REQ3 RTL8100L	**IDSEL(A27)--B**



8SRXL South Bridge GPIO LIST				
ITEM	DESCRIPTION	I/O	STATUS	Default
GPIO0	Bios Write Protect	O	Hi:Write Enable, Lo:Write Protect	Hi
GPIO1	N/A		PULL-UP	Hi
GPIO2	THERM#			Hi
GPIO3	Green Button	O	Hi:Normal, Lo:Into Green mode	Hi
GPIO4	CLKRUN#		PULL-DOWN	Lo
GPIO5	N/A		PULL-UP	Hi
GPIO6	CPU OVER VOLTAGE	O	Hi:Normal	Hi
GPIO7	SUSLED	O	**AS LIKE DEFINED...**	Lo
GPIO8	Wake On Ring	I	Hi:Normal, Lo:Ring Power On	Hi
GPIO9	GLED	I	**AS LIKE DEFINED...**	Lo
GPIO10	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo
GPIO11	N/A		PULL-UP	Hi
GPIO12	N/A		PULL-UP	Hi
GPIO13	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo
GPIO14	Primary Down	I	Lo:CODEC Only	Lo
GPIO15	KB Data	I/OD		
GPIO16	KB Clk	I/OD		
GPIO17	MS Data	I/OD		
GPIO18	MS Clk	I/OD		

States for a single-color power LED

				BIOS	
LED States	**ACPI States**	MPD+	MPD-	GPIO7	ACPILED
OFF	S5	HI	HI	**LO**	**HI/NC**
Steady Green	S0	HI	LO	**LO**	**LO**
Blinking Green	S0(message waiting)	HI	BLINKING	**LO**	**BLINKING**

States for a dual-color power LED

				BIOS	
LED States	**ACPI States**	MPD+	MPD-	GPIO7	ACPILED
OFF	S5	HI	HI	**LO**	**HI/NC**
Steady Green	S0	HI	LO	**LO**	**LO**
Blinking Green	S0(message waiting)	HI	BLINKING	**LO**	**BLINKING**
Steady Yellow	S1,S3	LO	HI	**HI**	**HI**
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING	**HI**	**BLINKING**

States for green LED

			BIOS
LED States	**ACPI States**	GLED-	GPIO9
ON	S1,S3	HI	**HI**
OFF	S0,S5	LO	**LO**

BIOS REQUEST

		INTEL LED DEFINED				GIGABYTE LED DEFINED					
SINGLE	**DUAL**		**GPIO7**	**ACPILED**	**GPIO9**		**GPIO7**	**ACPILED**	**GPIO9**	**SINGLE**	**DUAL**
GREEN	**GREEN**	**S0**	**LO**	**LO**	**LO**	**S0**	**LO**	**LO**	**LO**	**GREEN**	**GREEN**
OFF	**YELLOW**	**S1**	**HI**	**HI**	**HI**	**S1**	**LO**	**BLINKING**	**HI**	**G(BLINK)**	**G(BLINK)**
OFF	**YELLOW**	**S3**	**HI**	**HI**	**HI**	**S3**	**HI**	**HI**	**HI**	**OFF**	**YELLOW**
OFF	**OFF**	**S4/S5**	**LO**	**HI/NC**	**LO**	**S4/S5**	**LO**	**HI/NC**	**LO**	**OFF**	**OFF**

GIGABYTE

Title: **GPIO, REQ/GNT Table**

Size: Custom | Document Number: **GA-8SIMLH** | Rev: **2.0**

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