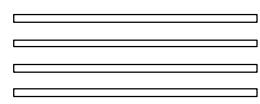


8SG667 Schematics

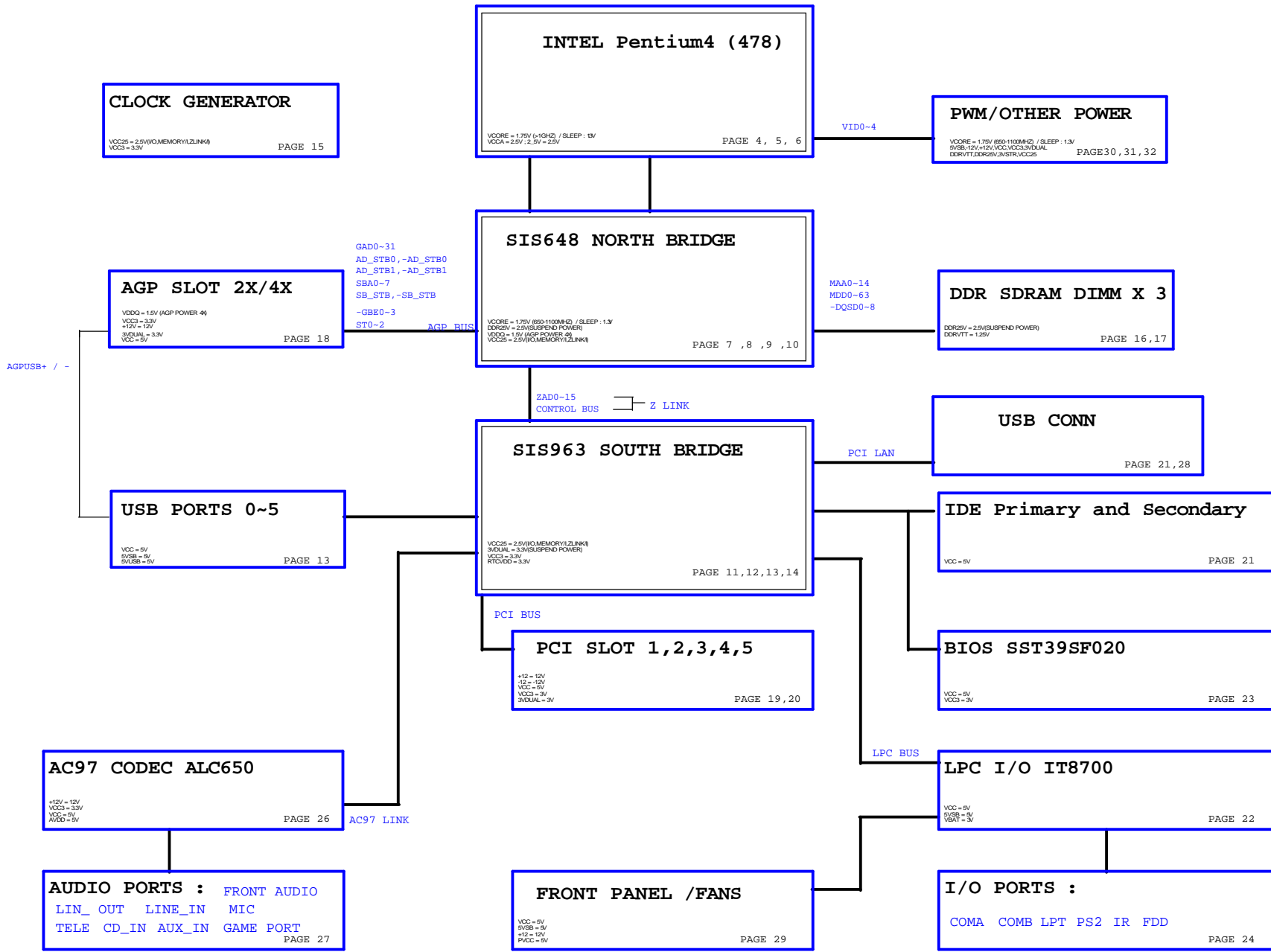
Revision 1.0

SHEET	TITLE
1	COVER SHEET
2	BOM & PCB MODIFY HISTORY
3	BLOCK DIAGRAM
4,5,6	INTEL CPU_WMT_478
7-10	SIS645 (NORTH BRIDGE) HOST; DDR; AGP,HYPER ZIP
11-14	SIS961 (SOUTH BRIDGE)
15	CLOCK GENERATOR (ICS952001)
16,17	DDR SDRAM DIMMS 1,2,3
18	AGP SLOT
19,20	PCI SLOT 1,2,3,4,5,6
21	IDE,FRONT USB,PCIRST#
22	LPCIO_IT8705
23	BIOS
24	COM,PRT,FDD,KB/MS,IR
25	AUDIO (CT5880)/AC 97
26	AUDIO JACK,GAME PORT
27	FAN, SMB PORT
28	PANEL,STR LED,FANS ,CPU GN
29	VCORE PHASE PWM HIP 6302 + 6602
30	DDR POWER,3VDUAL,VDDQ DC POWER
31	ATX CONN, GPIO LIST
32	RTL8100BL

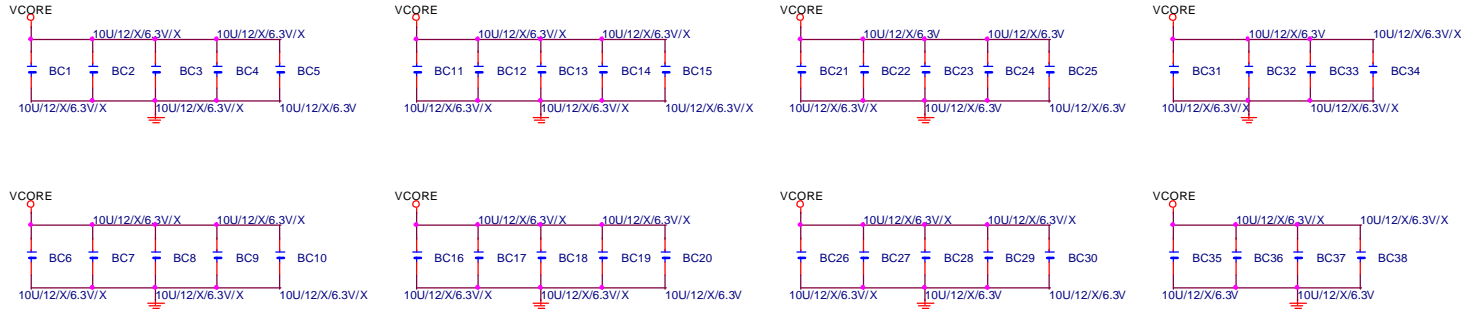
PCB Size: 304*200 mm

	
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COVER SHEET	
Size Custom	Document Number
GA-8SG667	
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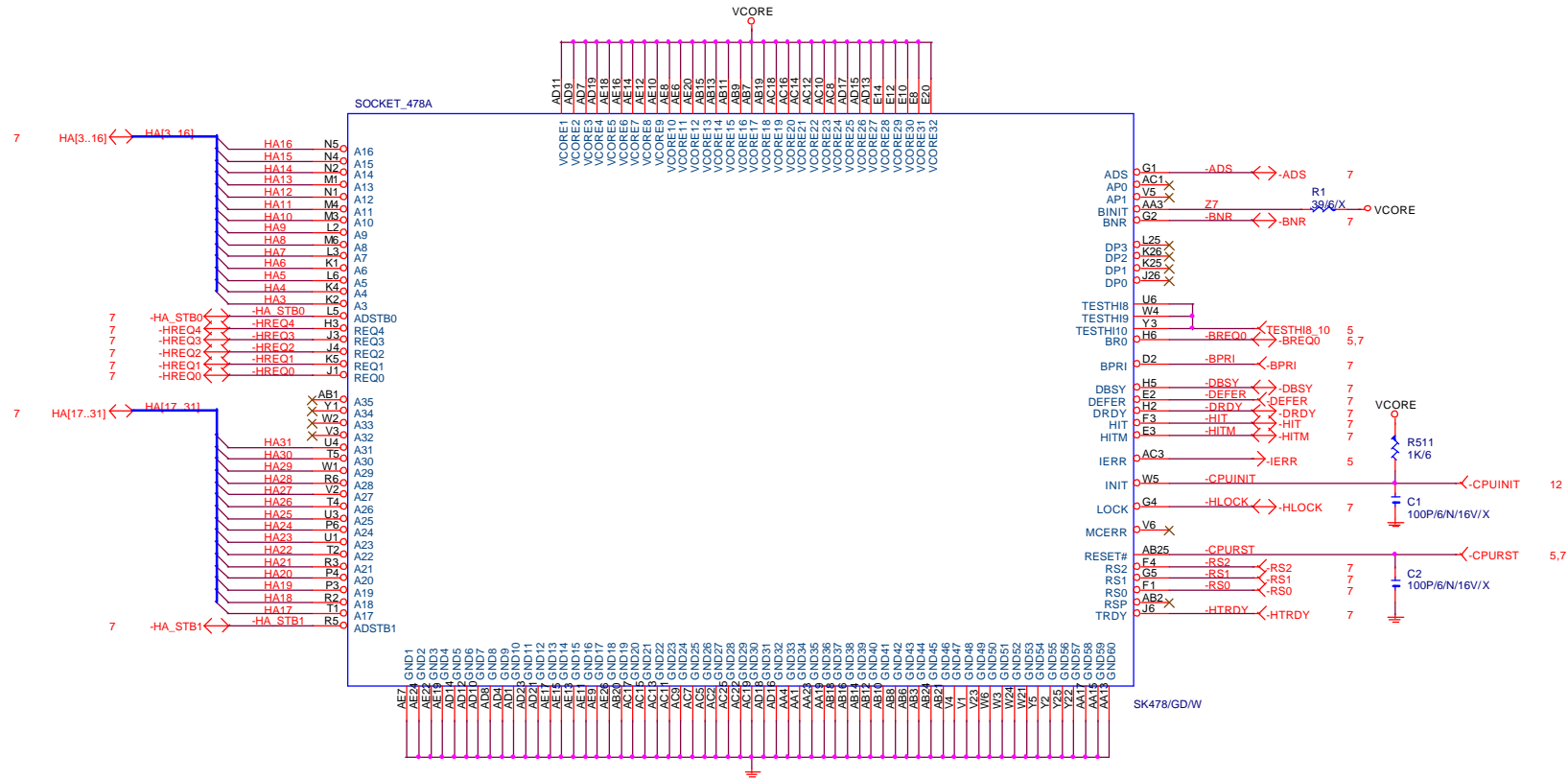
8SG667 BLOCK DIAGRAM



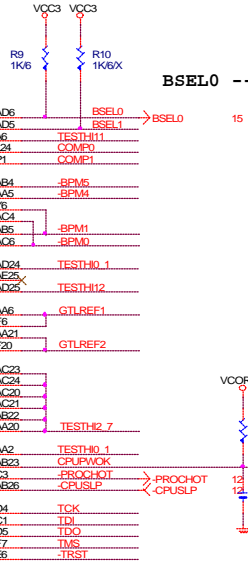
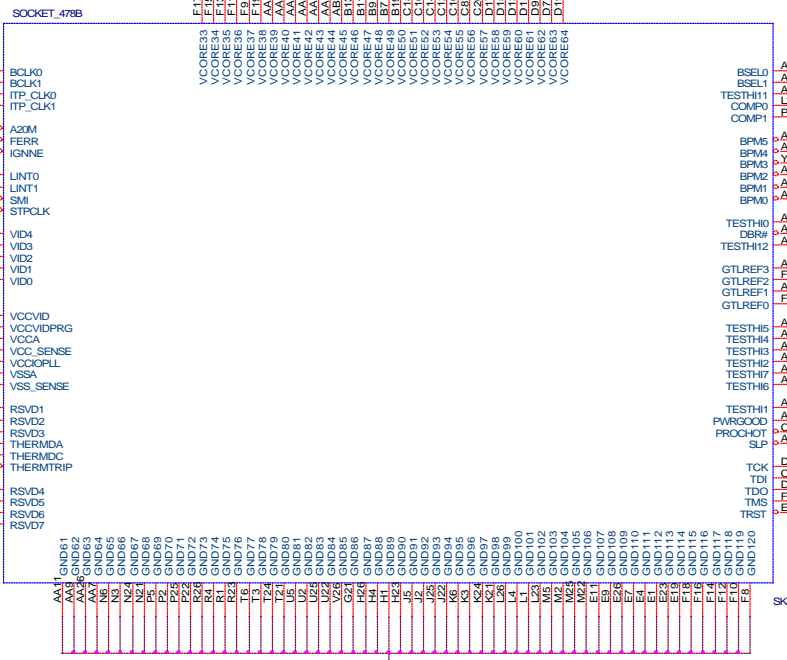
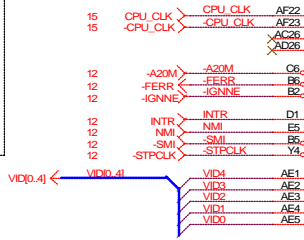
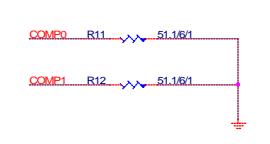
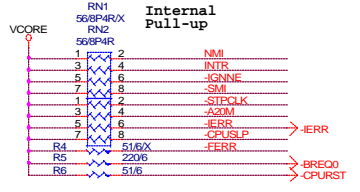
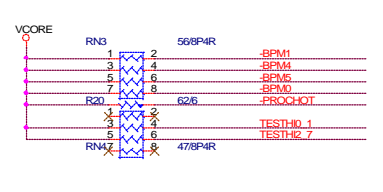
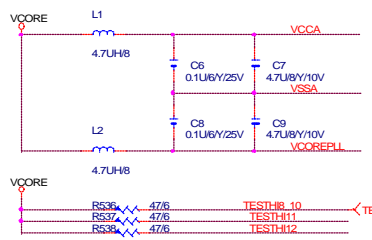
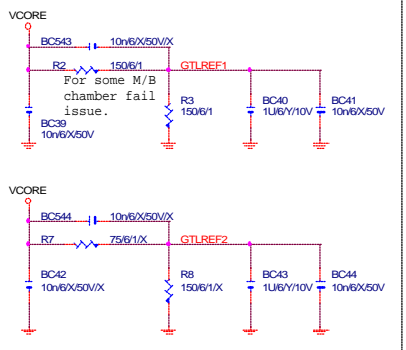
GIAGBYTE			
BLOCK DIAGRAM			
Doc Number	GA-8SG667		Rev 1.0
Date Created	Wednesday, September 10, 2003 12:24		Page 3 of 34



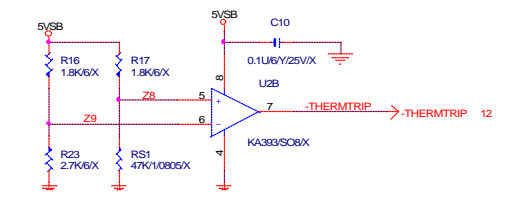
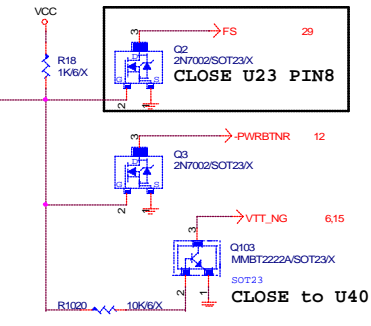
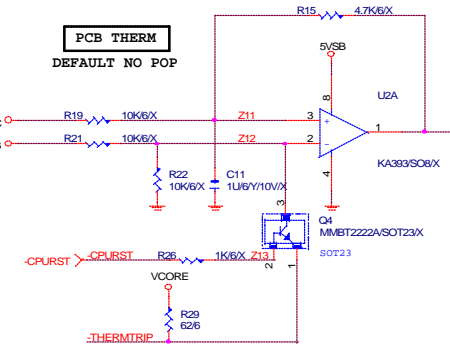
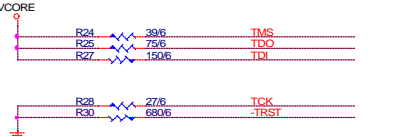
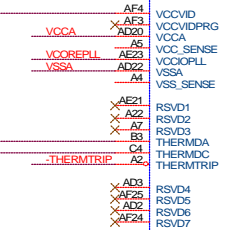
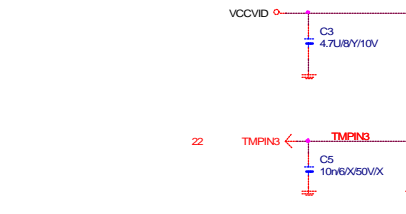
上11顆10U/X5R電容



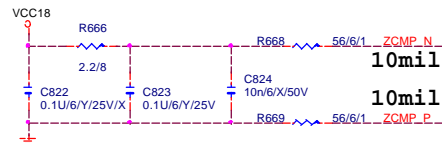
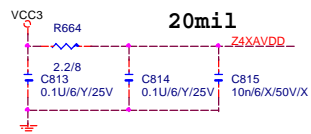
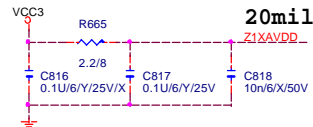
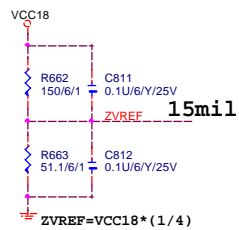
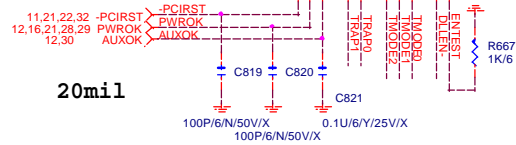
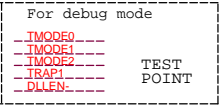
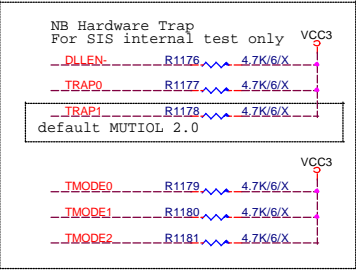
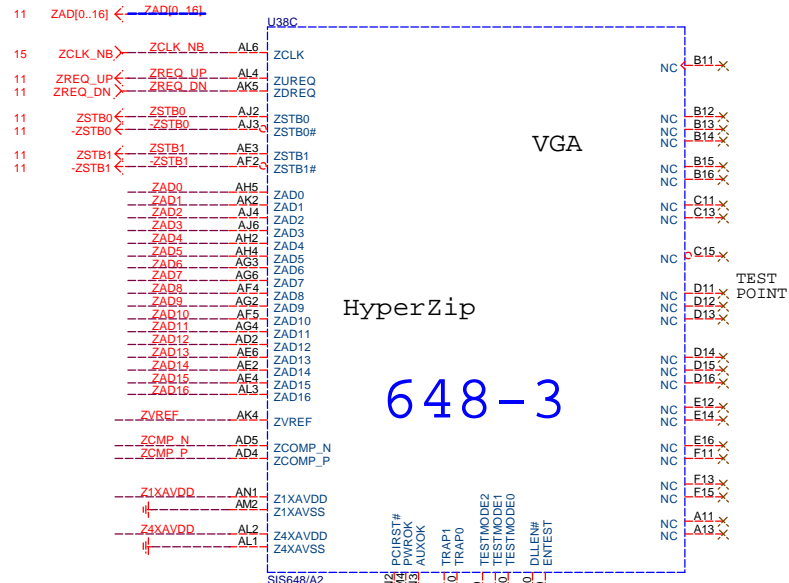
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Title		
WILLAMETTE 1/3		
Size	Document Number	Rev
B	GA-8SG667	1.0
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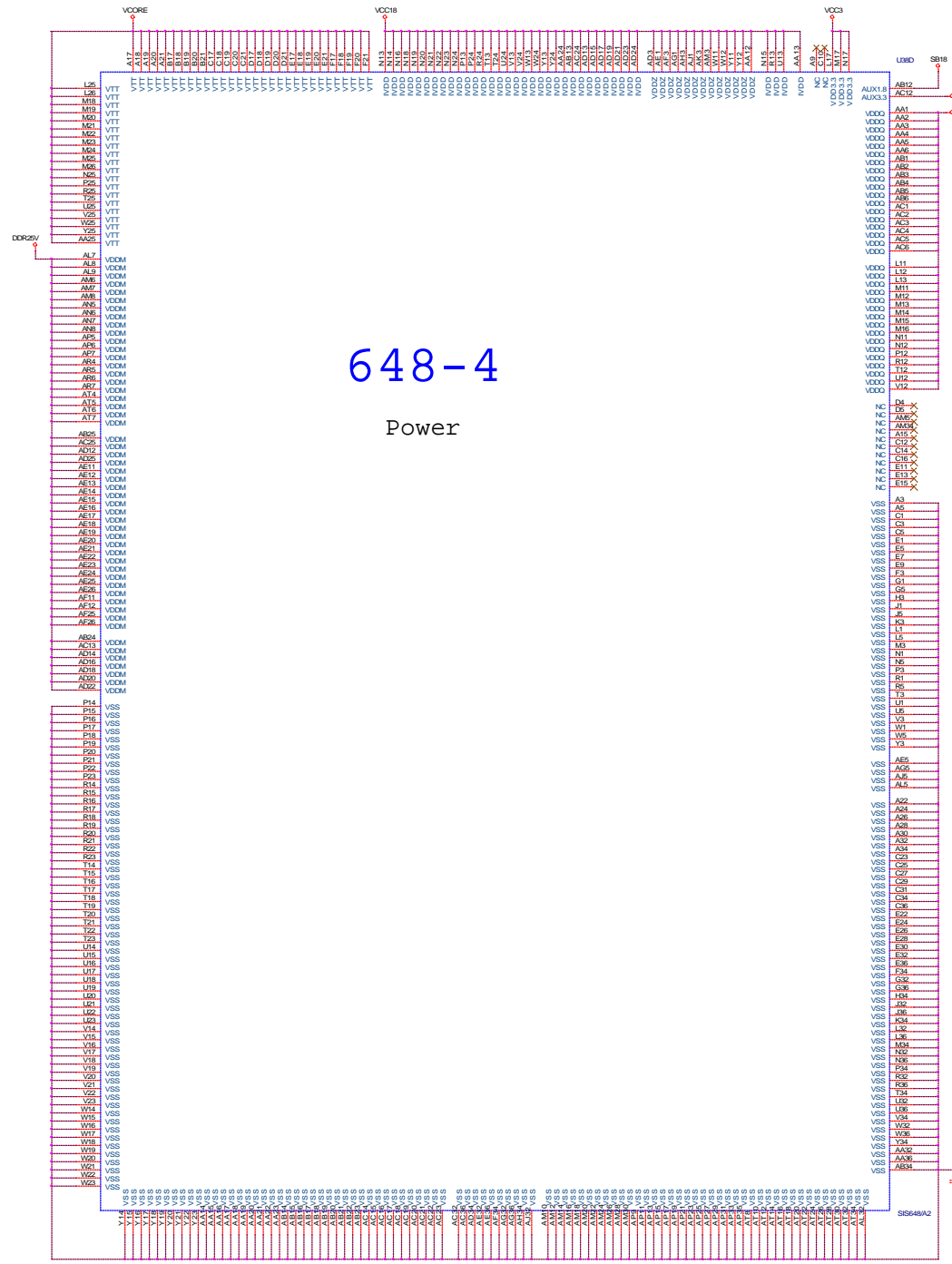


BSELO ---->100/133



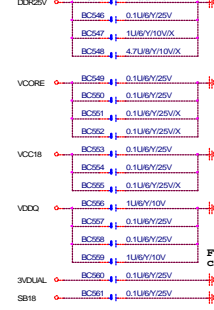
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Title		
WILLAMETTE 2/3		
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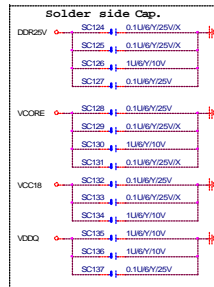


648-4 Power

Close to SIS648 chipset



For ATI(R300) chamber issue



For ATI(R300) chamber issue

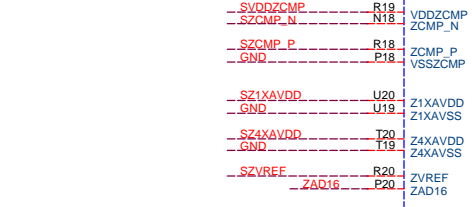
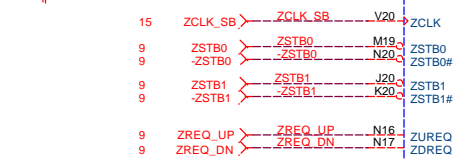
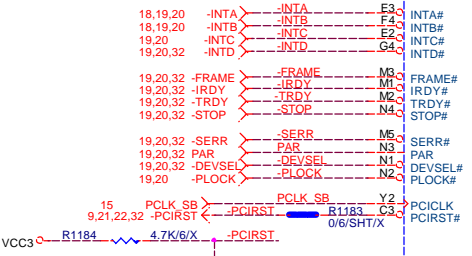
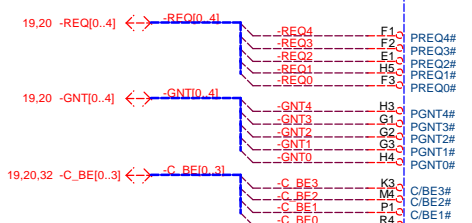
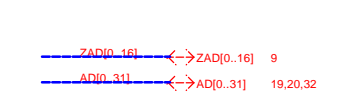
For ATI(R300) chamber issue

For ATI(R300) chamber issue

For ATI(R300) chamber issue

Place on SIS648 chipset
Solder side.

GIGABYTE		
SIS648-4(Power)		
File	Document Number	Rev
Customer	GA-8SG667	1.0
Date	Wednesday, September 04, 2002	Print 10 of 32

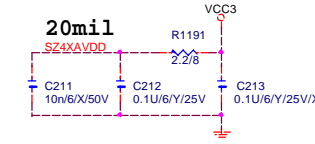
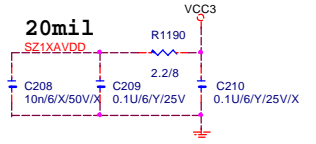
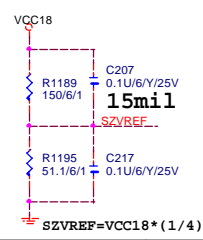
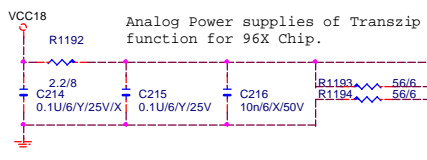
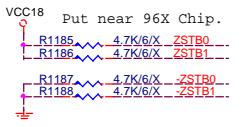
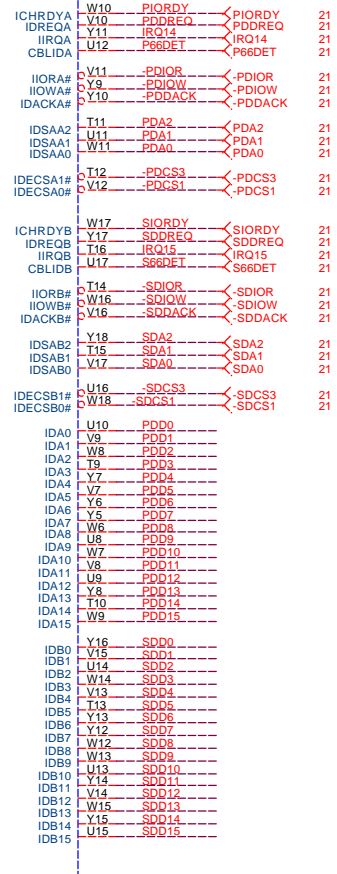
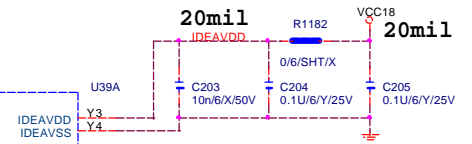
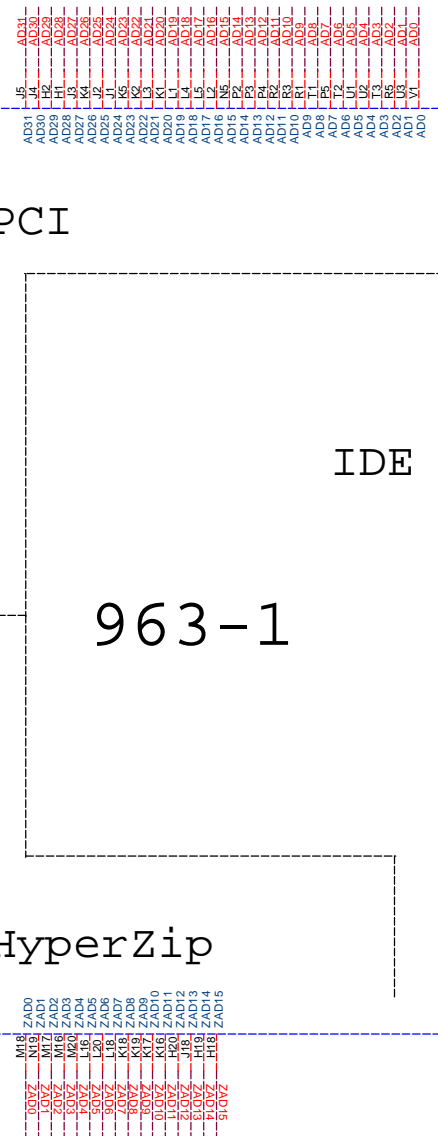


PCI

IDE

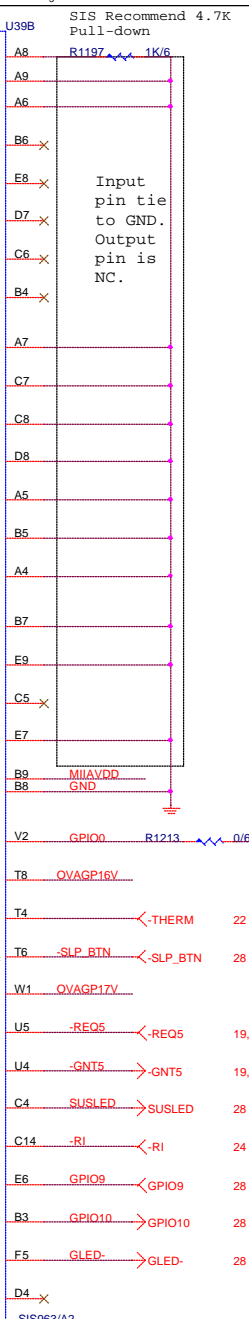
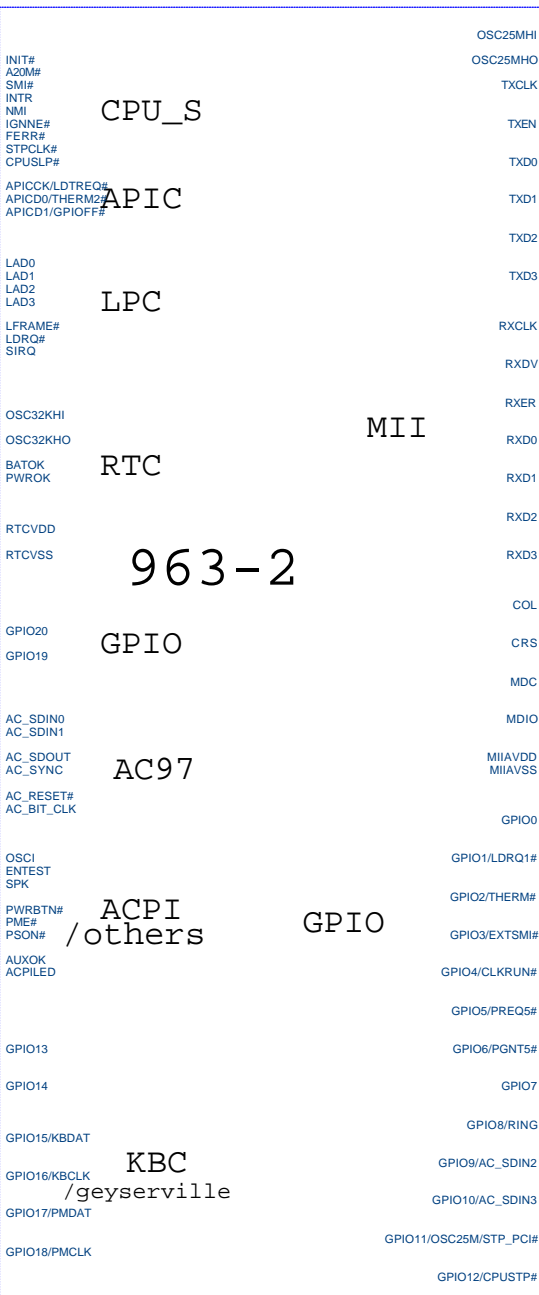
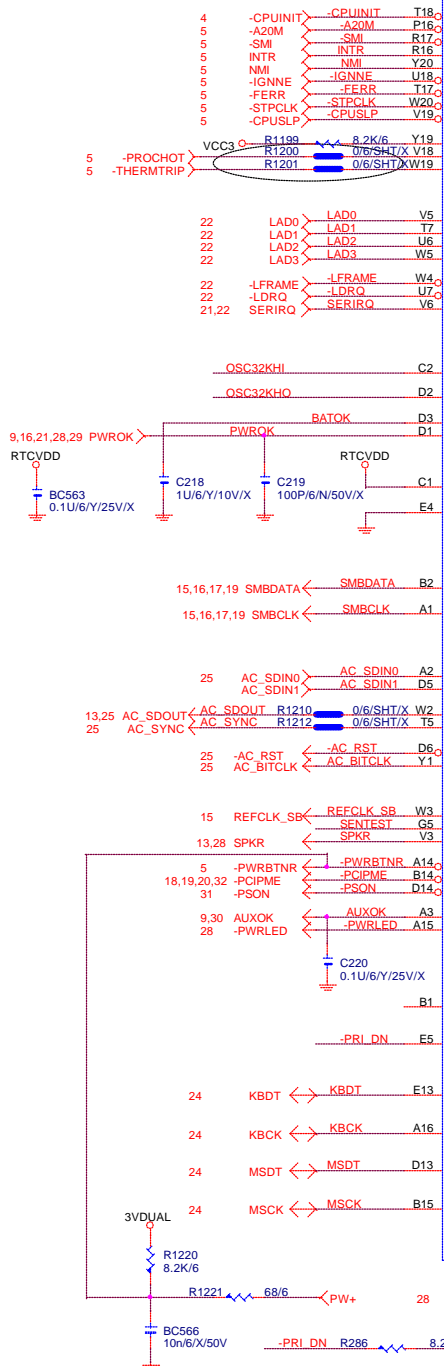
HyperZip

963-1



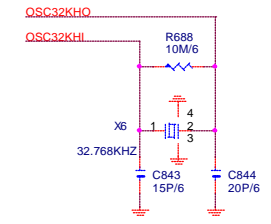
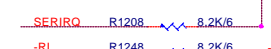
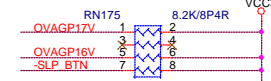
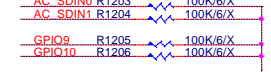
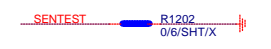
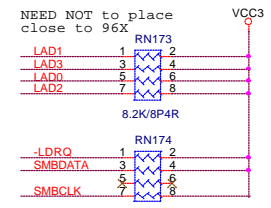
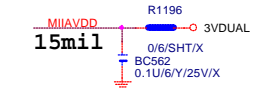
GIGABYTE		
SIS963-1(HP ZIP,PCI,IDE)		
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	GA-8SG667	1.0
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Programmable on-die pull-high strength for CPU_S:
(Infinite, 150, 110, 56 Ohm)

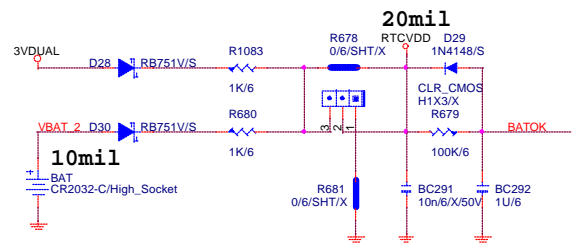


SIS Recommend 4.7K Pull-down

Input pin tie to GND. Output pin is NC.



CLR_CMOS	CLEAR COMS JUMPER
1-2	Enable
2-3	Disable (Default)

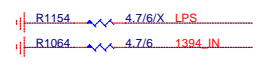
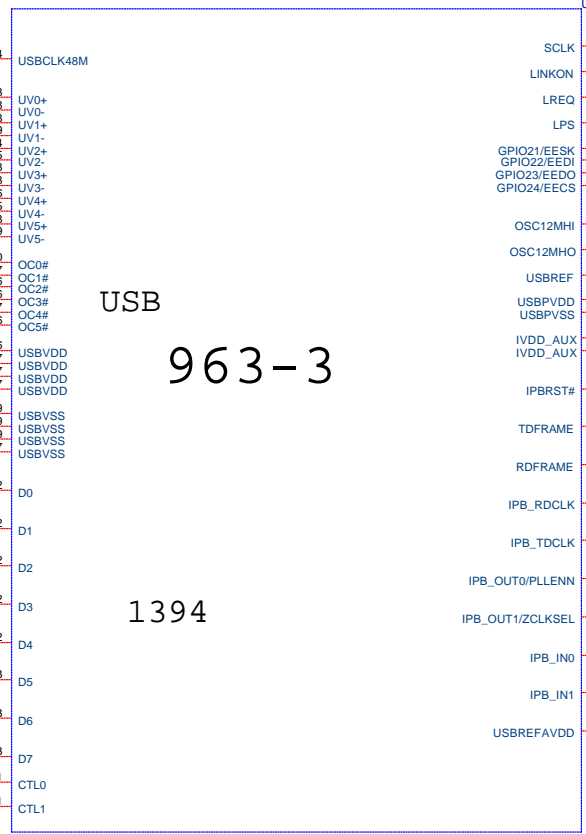
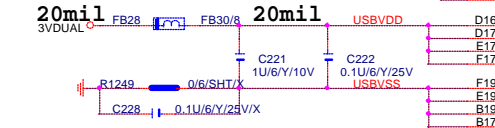
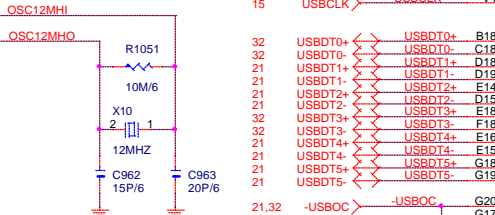


GIGABYTE

SIS963-2(LPC,MII,GPIO)

Title	SIS963-2(LPC,MII,GPIO)	
Size	Document Number	Rev
Custom	GA-8SG667	1.0
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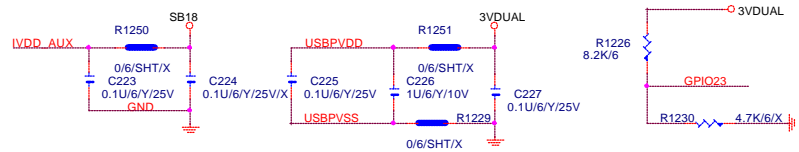
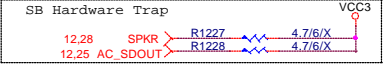
SIS962 USB 2.0



	0	1	Default	
SPKR(LPC address mapping)	disable	enable	R169 un-stuff	yes
AC_SDOOUT(Trap From)	ROM	PCI AD	R170 un-stuff	yes
SB debug mode	enable	disable		

embedded pull-low (30-50K Ohm)

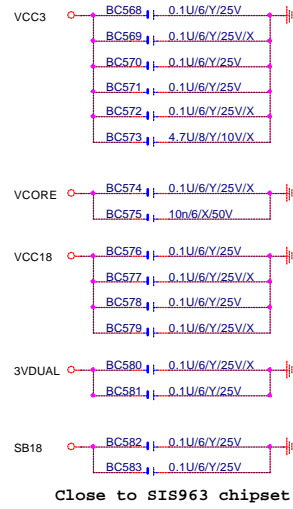
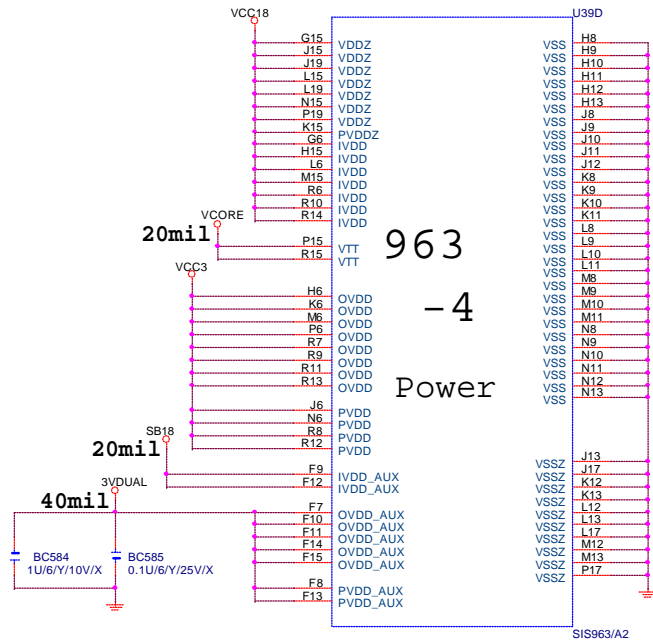
If 1394 do not use:
Output pin(LPS, LREQ) can be open.
All input pin pull-down to gnd.



GIGABYTE

SIS963-3(USB2.0)

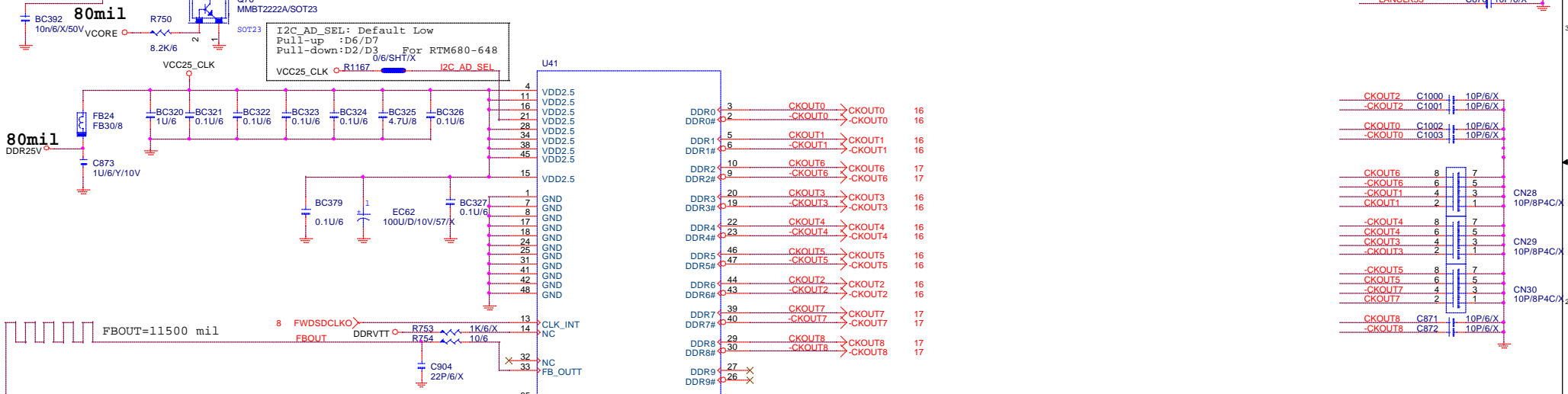
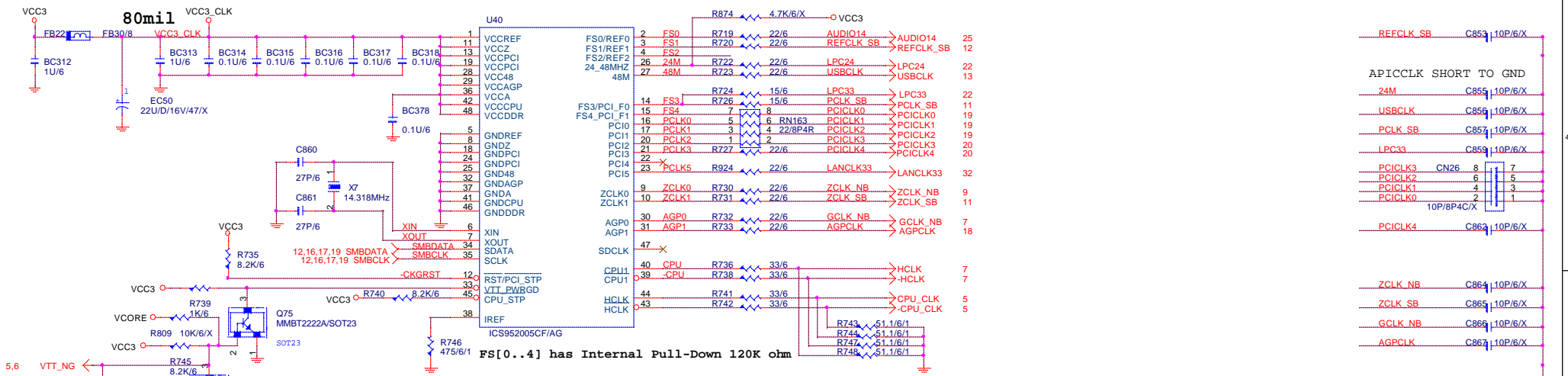
Title	SIS963-3(USB2.0)	
Size	Document Number	Rev
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Solder side Cap.

3VDUAL SC138 0.1U/6/Y/25V/X
SB18 SC139 0.1U/6/Y/25V/X
VCC18 SC140 0.1U/6/Y/25V/X
VCC3 SC141 0.1U/6/Y/25V/X

Place on SIS963 chipset
Solder side.



ICS952005

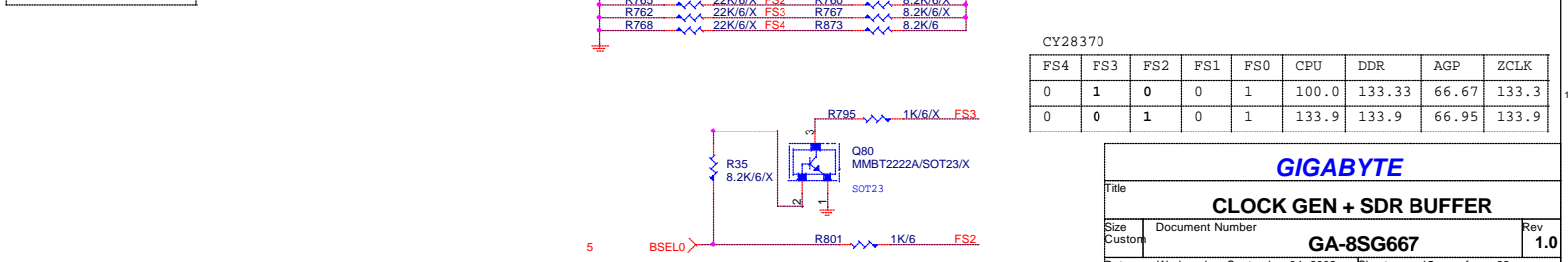
FS4	FS3	FS2	FS1	FS0	CPU	DDR	AGP	ZCLK
1	0	0	0	1	100.2	133.6	66.8	133.6
1	0	1	0	1	133.6	133.6	66.8	133.6

CY28370

FS4	FS3	FS2	FS1	FS0	CPU	DDR	AGP	ZCLK
0	1	0	0	1	100.0	133.33	66.67	133.3
0	0	1	0	1	133.9	133.9	66.95	133.9

ICS952005/CY28370 CLOCK BOM OPTION TABLE

H/W Strap	R763	R767	R873	R801	R35	Q80	R795
ICS952005	8.2K	N/A	8.2K	1K	N/A	N/A	N/A
100.2/133.6							
CY28370	8.2K	8.2K	N/A	1K	8.2K	MMBT	1K
100.0/133.9						2222	



GIGABYTE

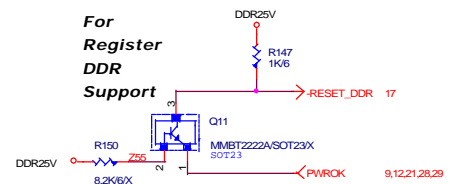
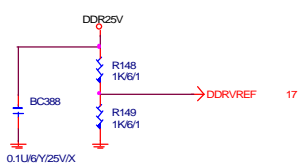
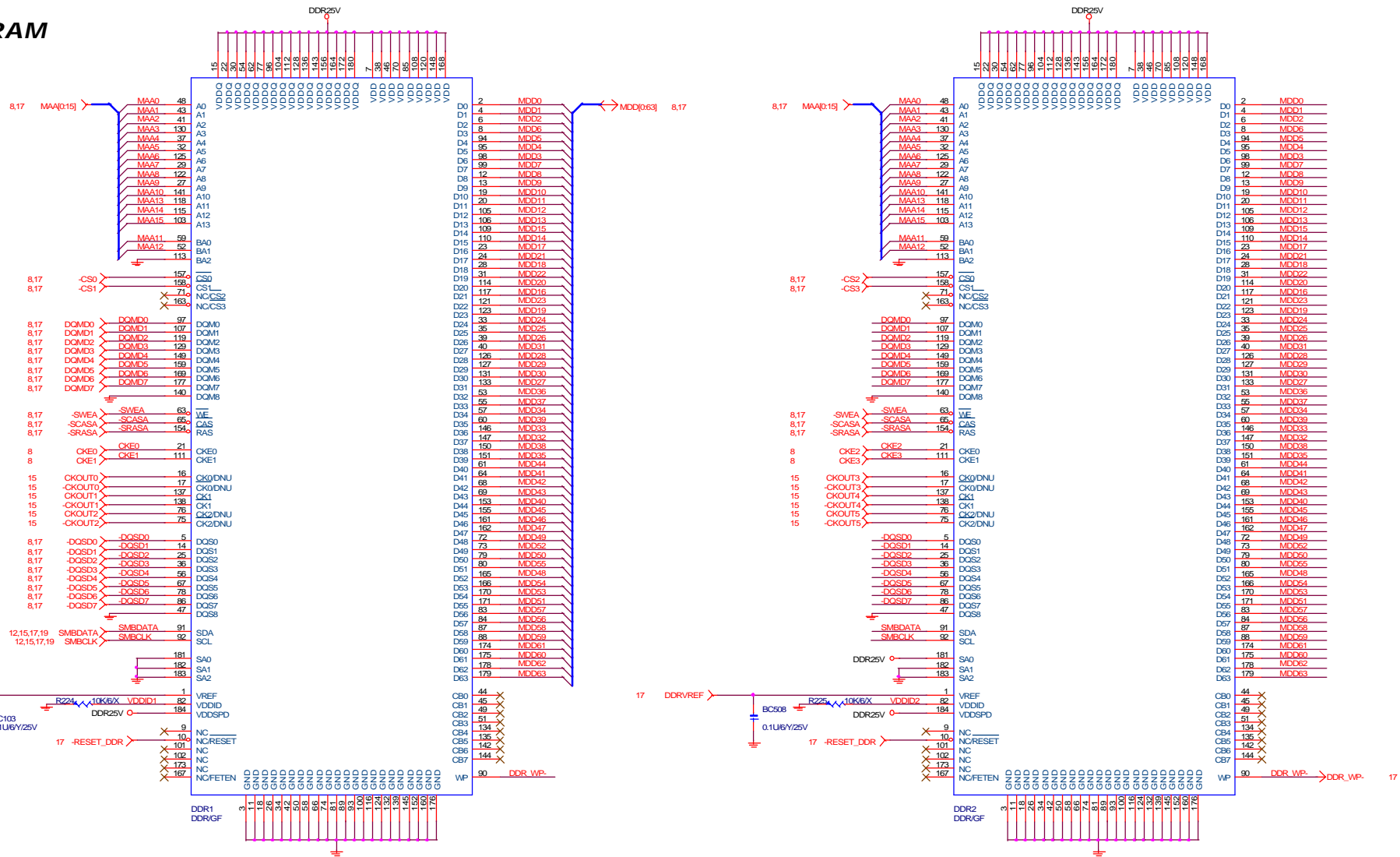
CLOCK GEN + SDR BUFFER

Title: **GA-8SG667**

Size: Custom Document Number: **GA-8SG667** Rev: **1.0**

Date: Wednesday, September 04, 2002 Sheet: 15 of 32

DDR SDRAM 1,2

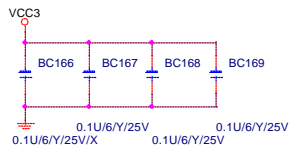
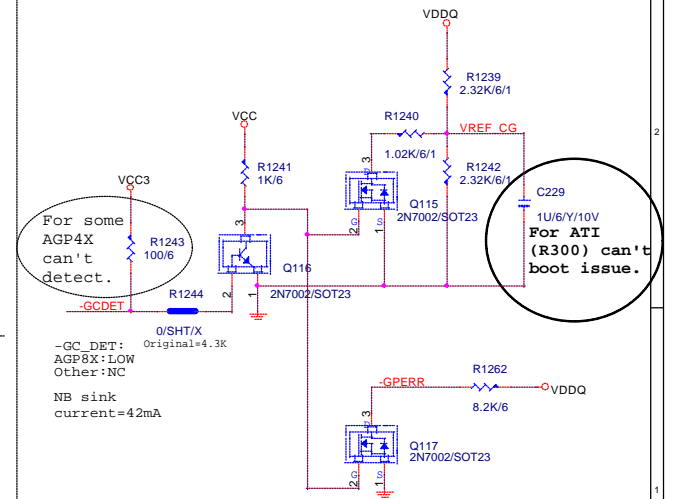
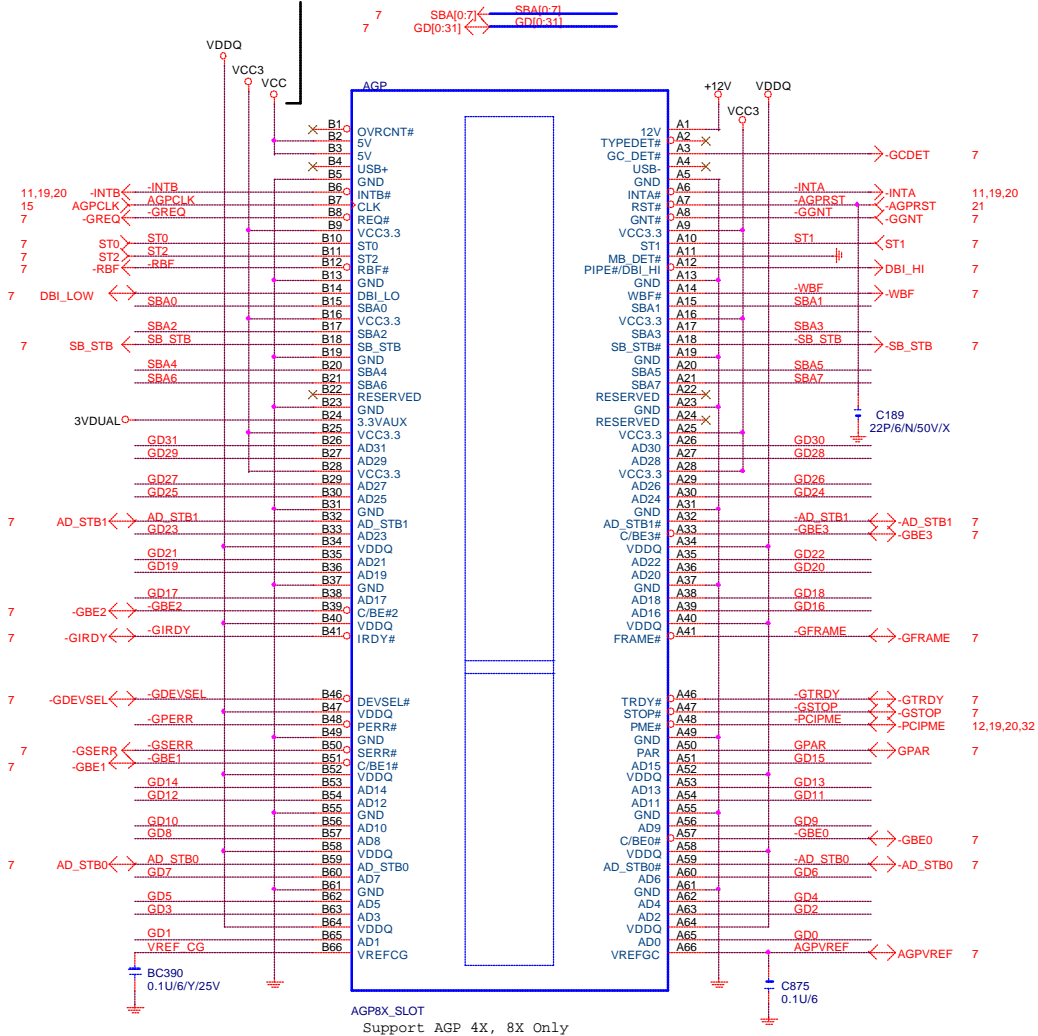


GIGABYTE

DDR UNBUFFERED 1,2

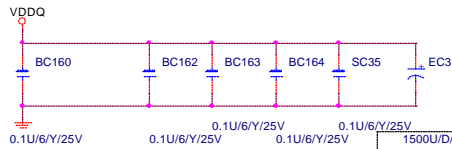
Title		Rev
DDR UNBUFFERED 1,2		1.0
Size	Document Number	
Custom	GA-8SG667	
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VCC : 80 mil



Place 1 at each pair of 3.3V pins

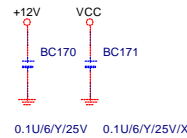
Decoupling capacitors
(Place near AGP slot)



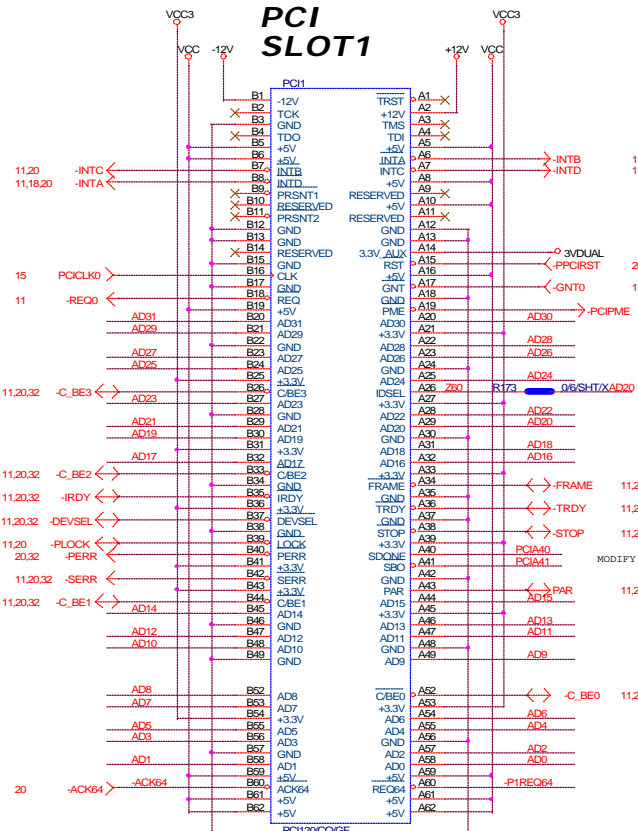
Place 1 at each pair of VDDQ pins

Place an additional for spread from A14 - A33

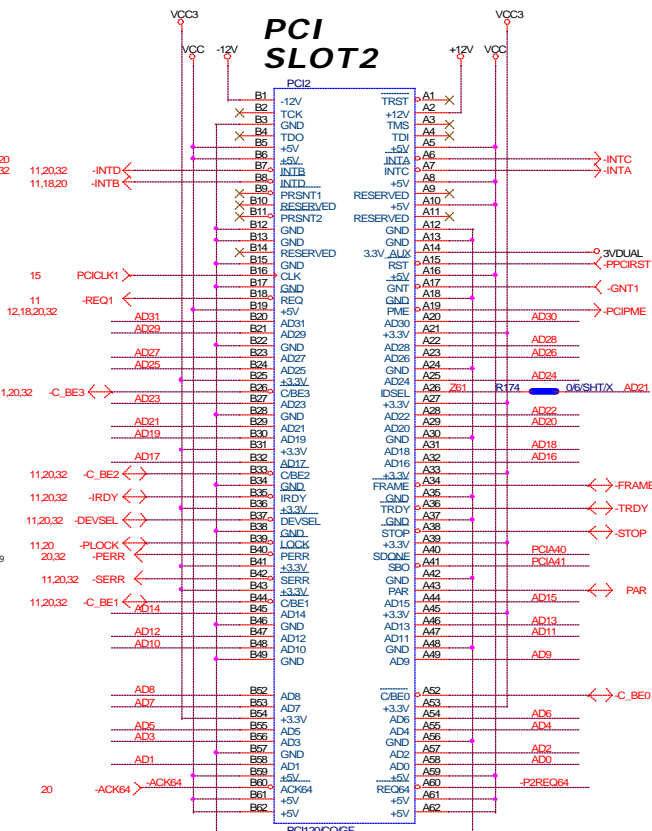
For ATI (R300) chamber issue



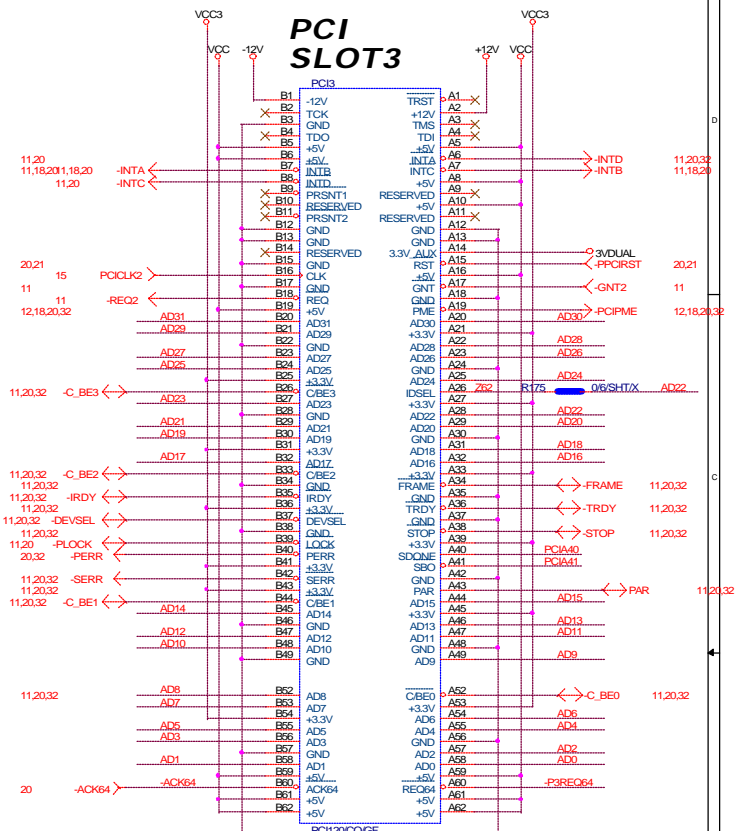
GIGABYTE		
AGP SLOT		
Title		
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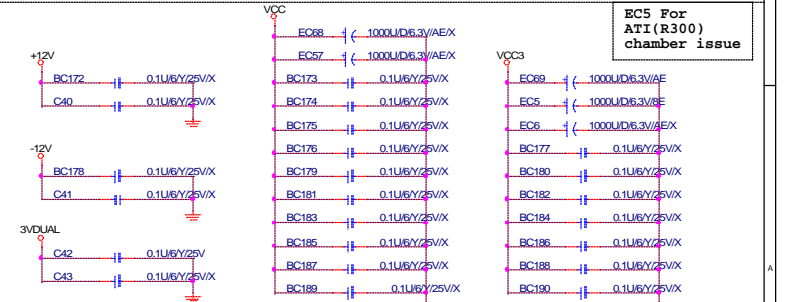
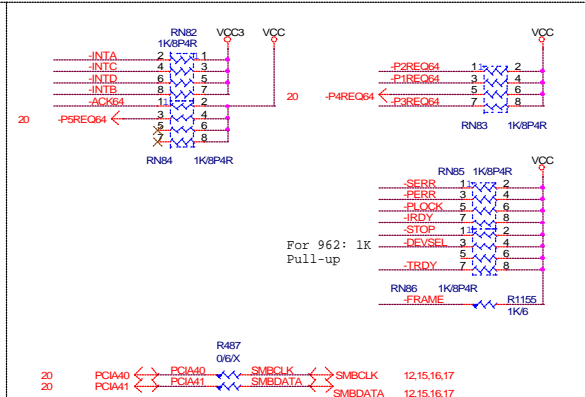
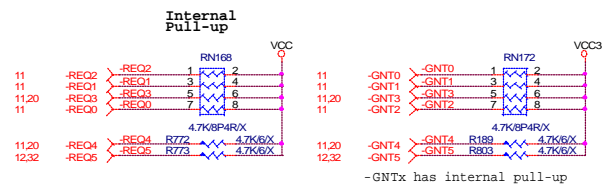
IDSEL(A20)
(B)



IDSEL(A21)
(C)



IDSEL(A22)
(D)



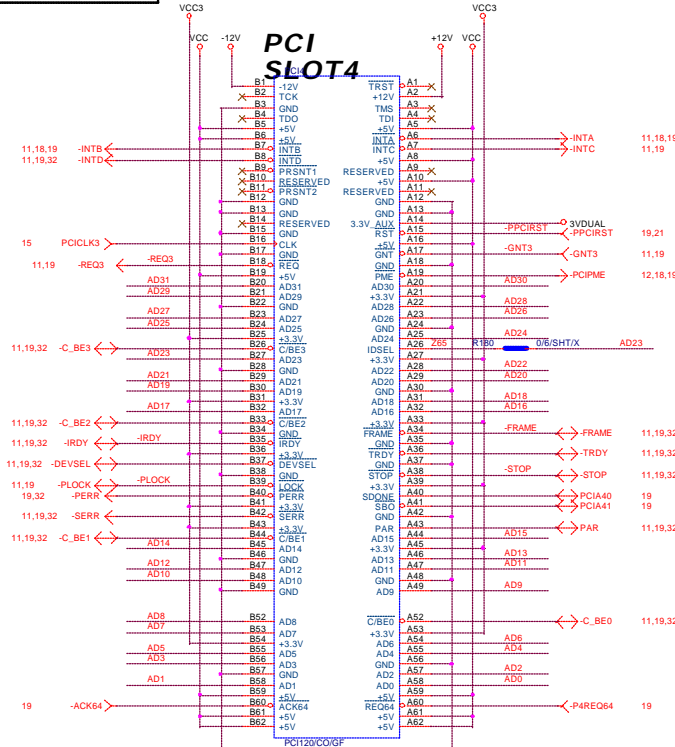
GIGABYTE

Title: **PCI SLOT 1,2,3**

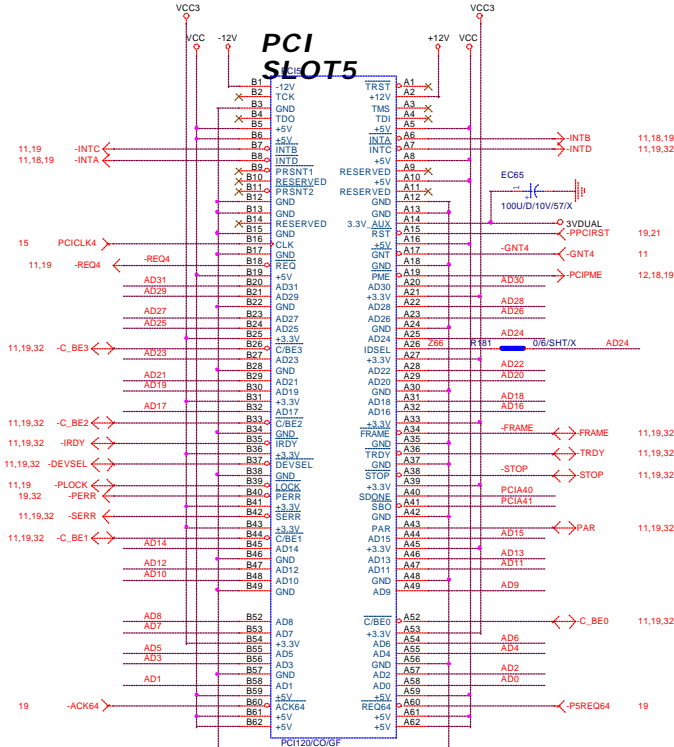
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PCI SLOT 4,5,6



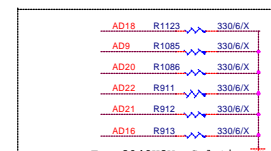
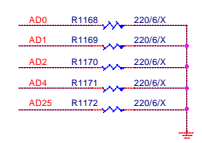
PCI120/CO/GF
IDSEL(A23)
(A)



PCI120/CO/GF
IDSEL(A24)
(B)

-PPCIRST
Close PCI Slot5
C44
100P/N50V/X

PCI的走線要盡量 避免走"Γ"型。



For 2940U2W Solution
放在U55(RTL8100)或PCI SLOT旁邊作為PCI bus signal termination.

	INTA#	IDSEL	REQX-
PCI1	BCDA	AD20	REQ0
PCI2	CDAB	AD21	REQ1
PCI3	DABC	AD22	REQ2
PCI4	ABCD	AD23	REQ3
PCI5	BCDA	AD24	REQ4
RTL8100	D	AD26	REQ5

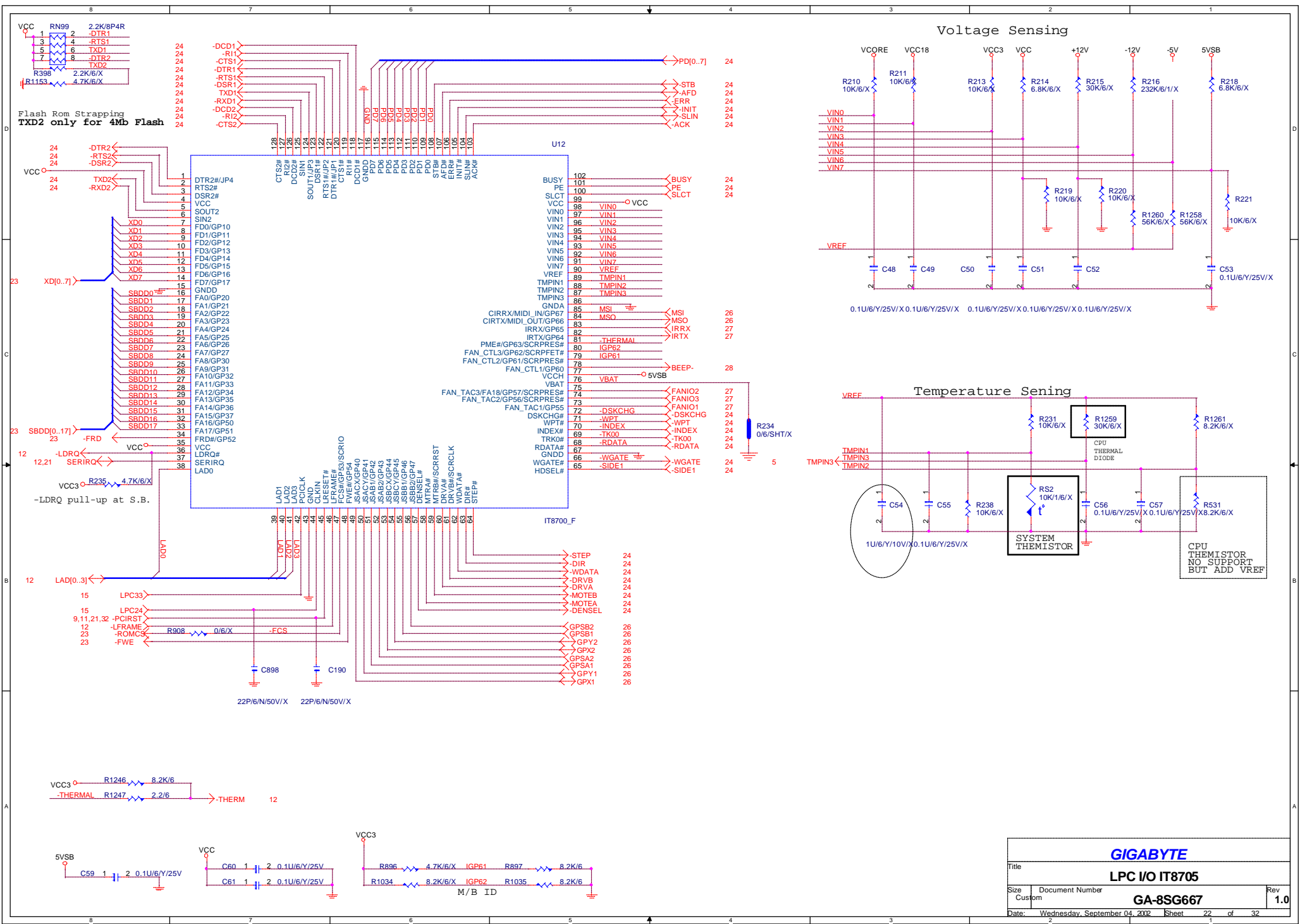
GIGABYTE

File: **PCI SLOT 4,5**

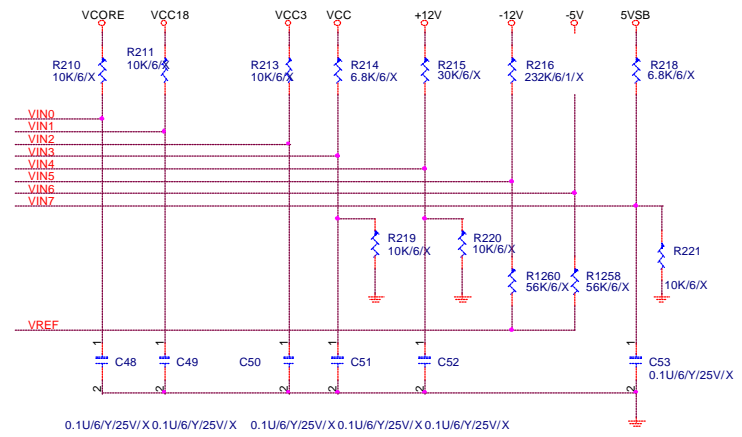
Size: Document Number **GA-8SG667** Rev **1.0**

Custom: **GA-8SG667**

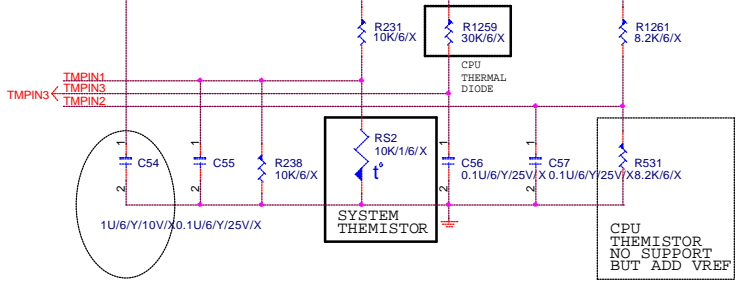
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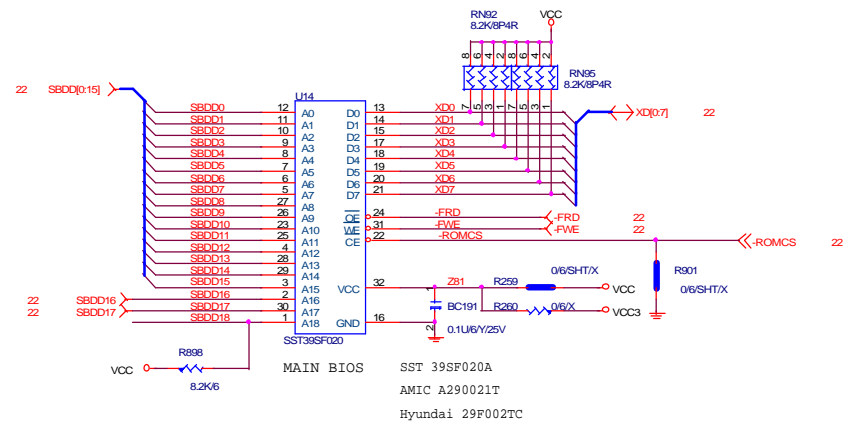
Voltage Sensing



Temperature Sensing

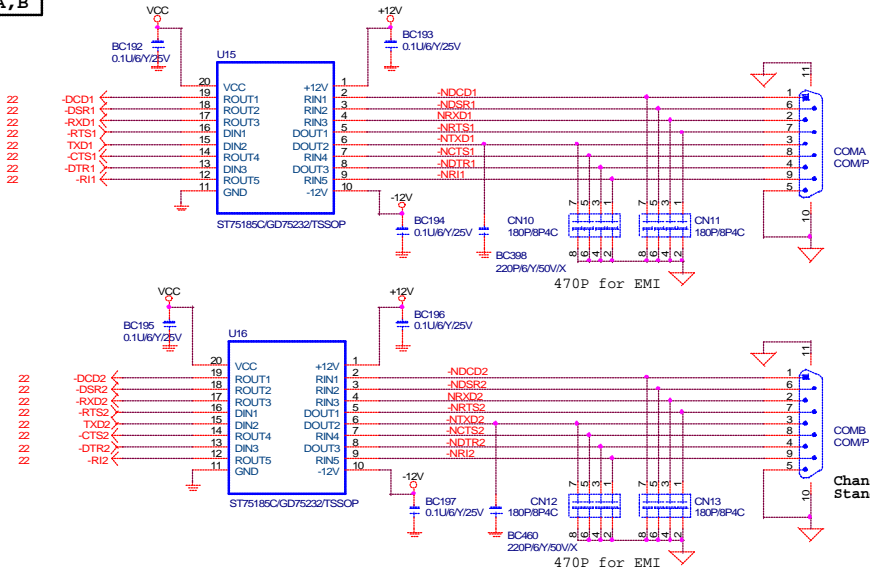


GIGABYTE			
LPC I/O IT8705			
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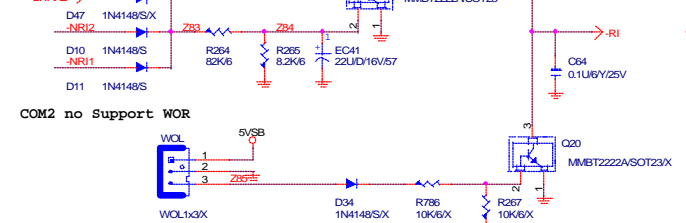
GIGABYTE		
Title Flash ROM		
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COM A, B

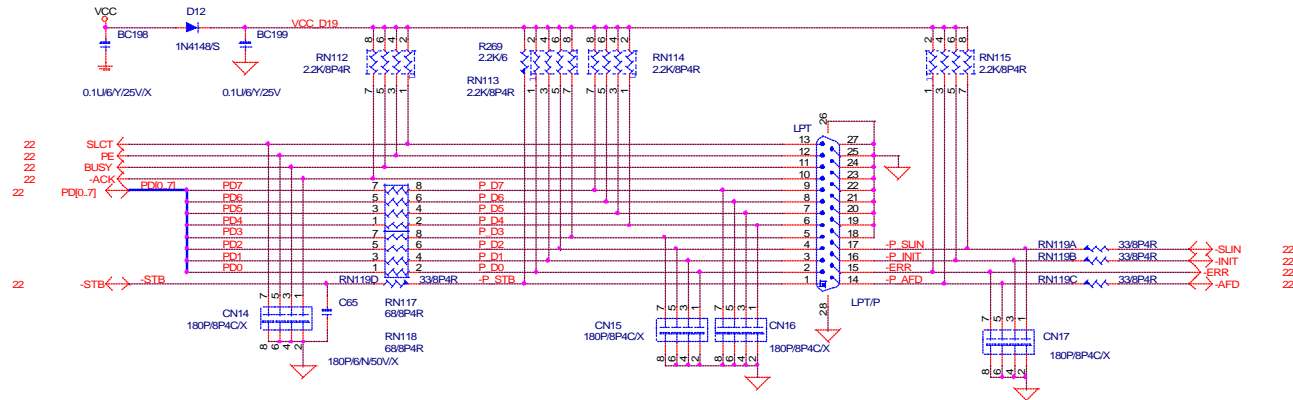


Change to Standard COM Port

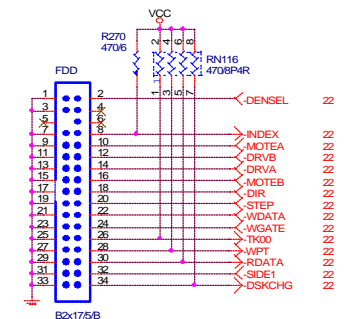
COM2 no Support WOR



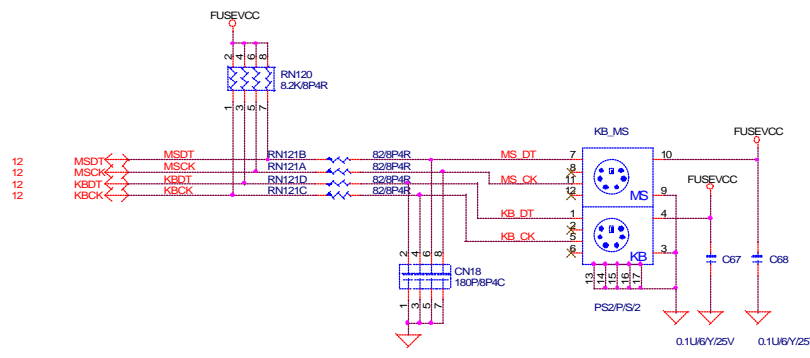
LPT



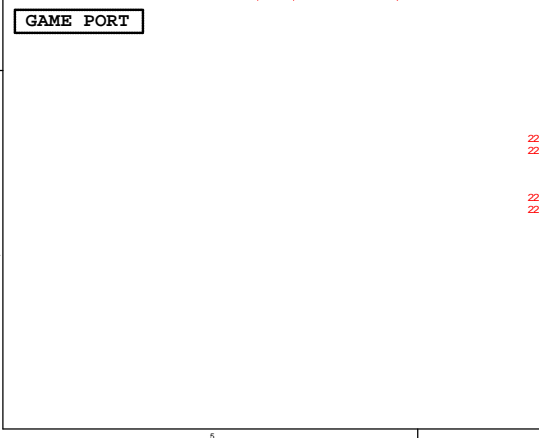
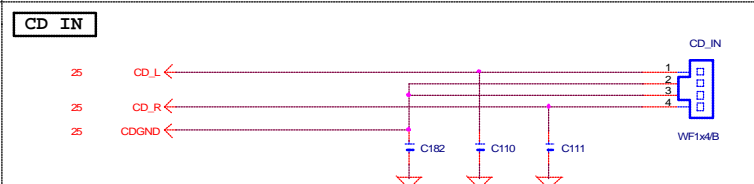
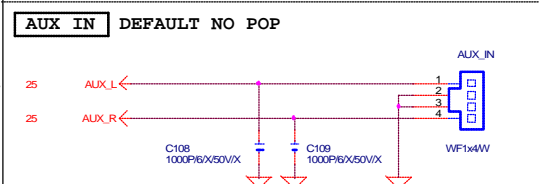
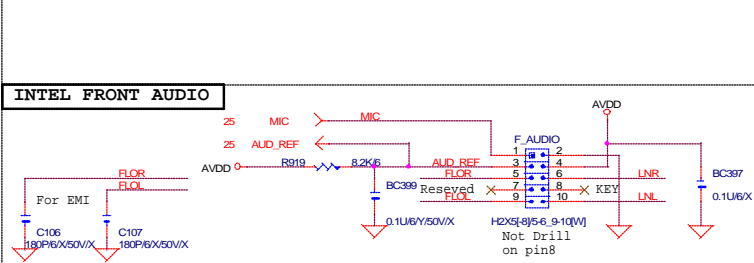
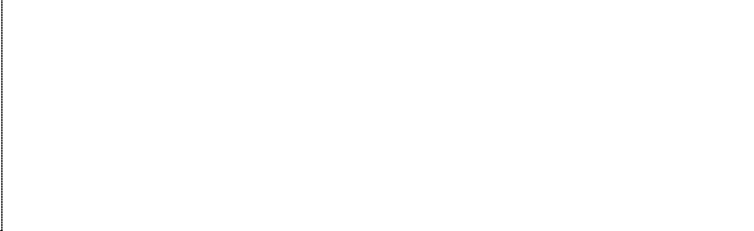
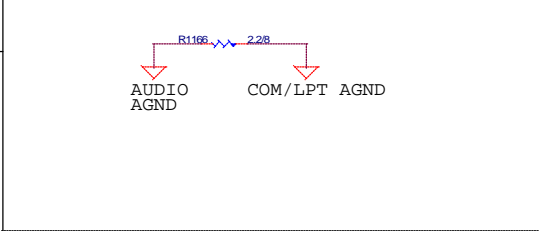
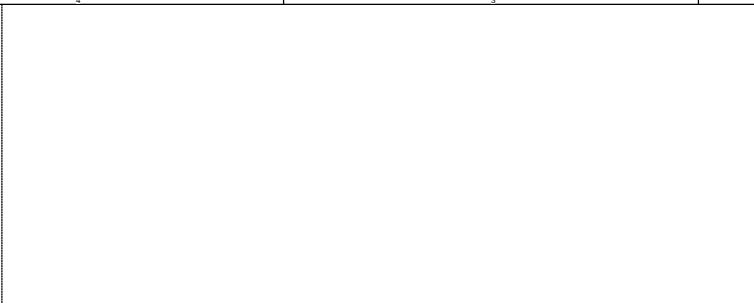
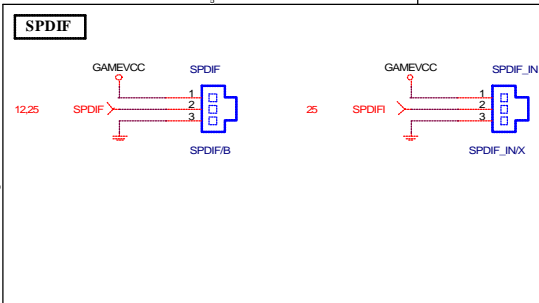
FDD

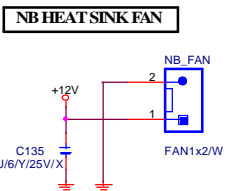
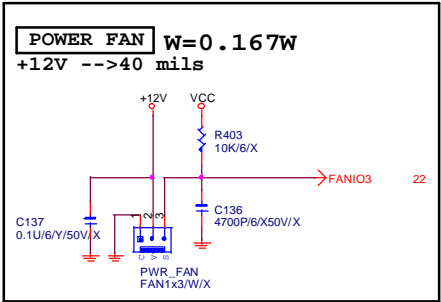
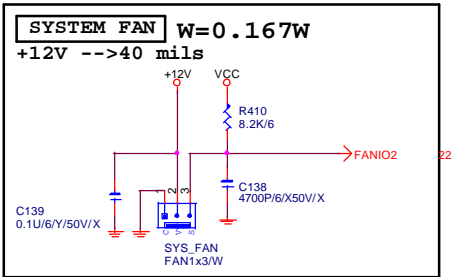
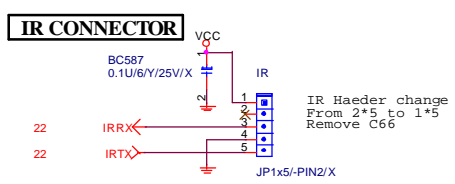
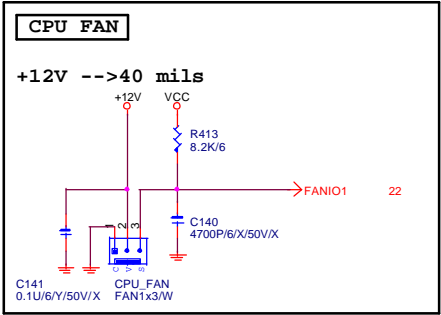


KBC/PS2



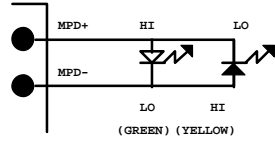
GIGABYTE		
Title COM,PRT,FDD,KB,IR		
Size Custom	Document Number GA-8SG667	Rev 1.0
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GIGABYTE		
Title FAN		
Size Custom	Document Number GA-8SG667	Rev 1.0
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FRONT PANEL



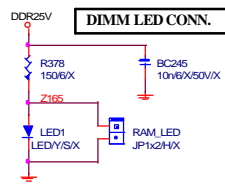
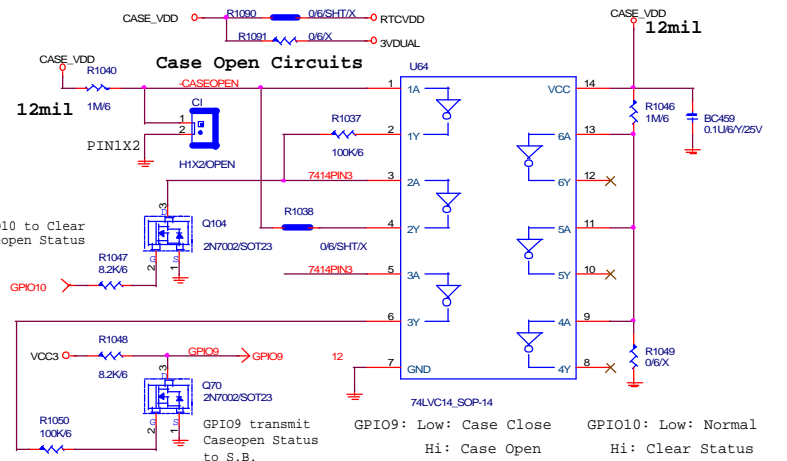
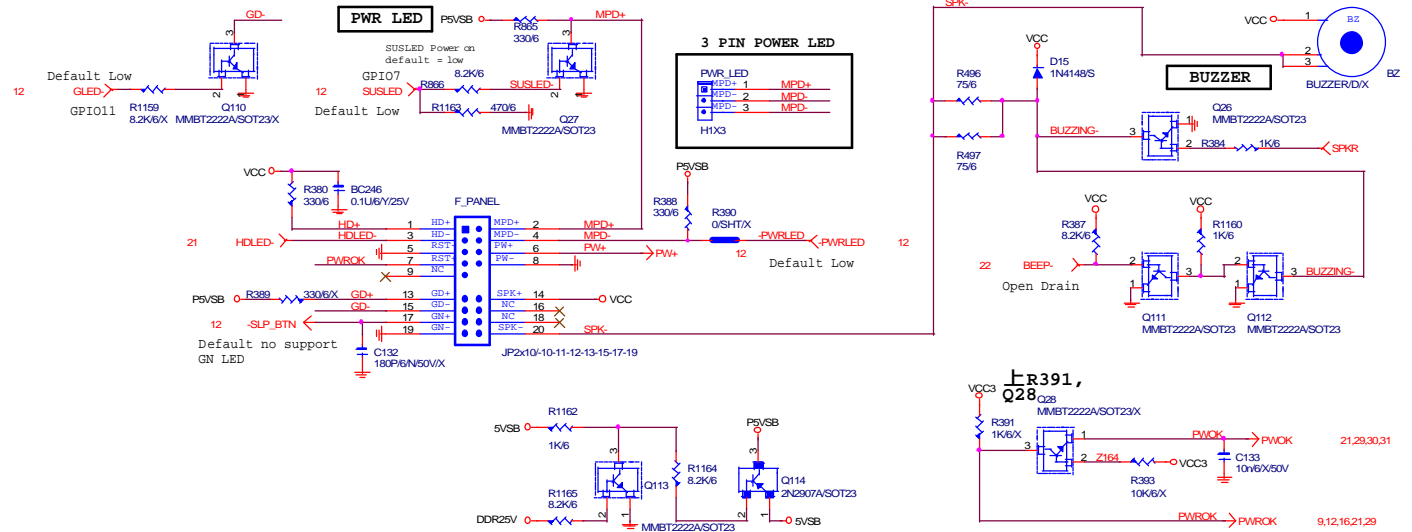
States for a single-color power LED

LED States	ACPI States	MPD+	MPD-
OFF	S1,S3,S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING

States for a dual-color power LED

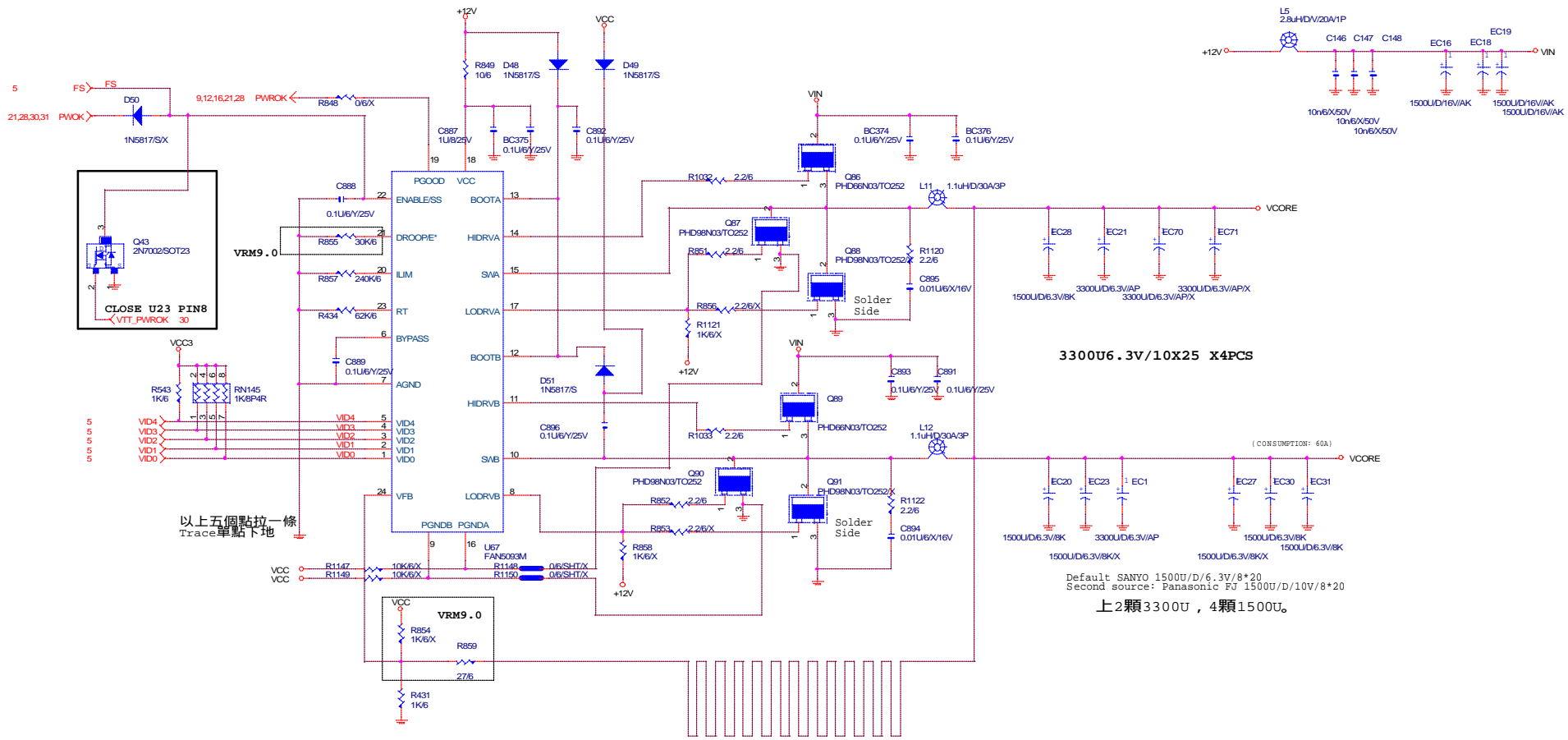
LED States	ACPI States	MPD+	MPD-
OFF	S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING
Steady Yellow	S1,S3	LO	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING

	S0	S1	S3	S5
GPIO11(GLED-)	0	1	1	0
GPIO7(SUSLED)	0	B	B	0
ACPILED(Pin A15)	0	0	0	1



74LVC14:
 10TC1-140014-01
 10TC1-120014-01
 10TC1-120014-02

GIGABYTE		
PANEL, STR LED		
Title		
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CLOSE U23 PIN8
VTT_PWRCK 30

以上五個點拉一條
Trace單點下地

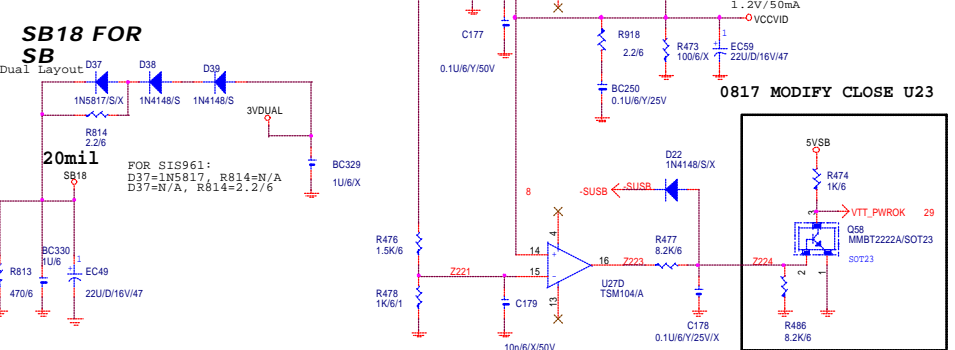
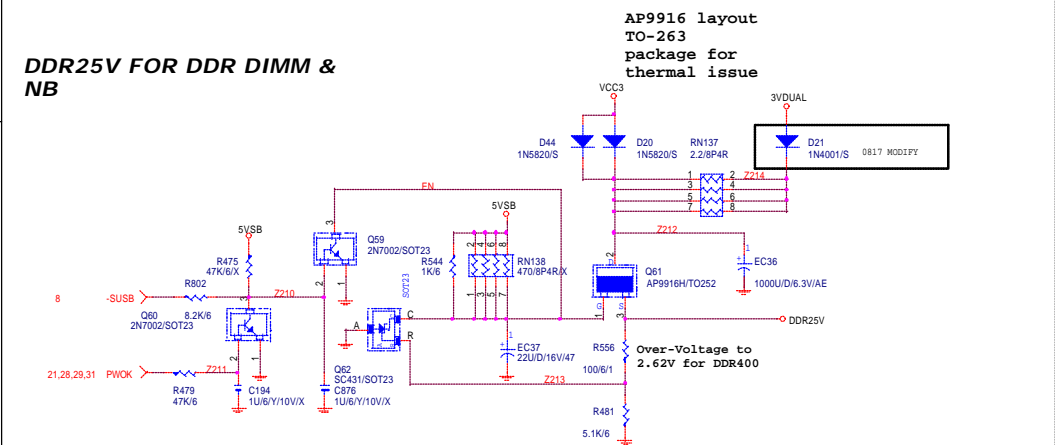
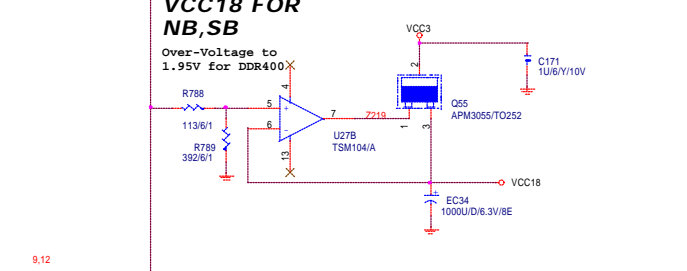
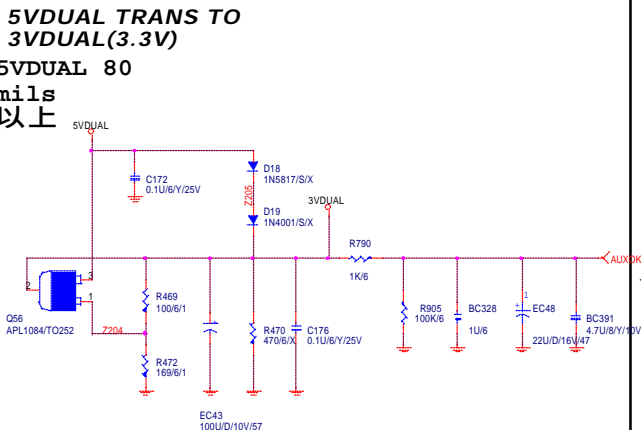
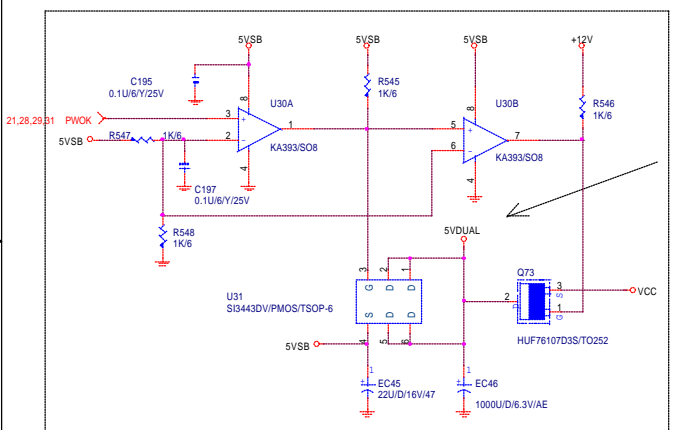
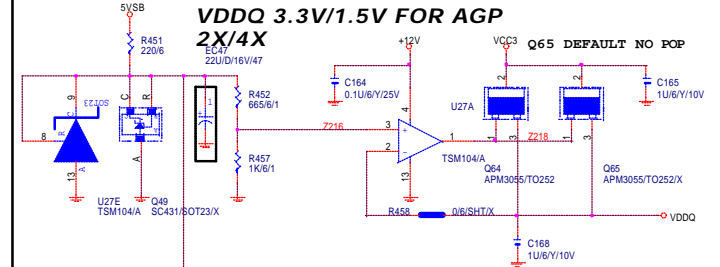
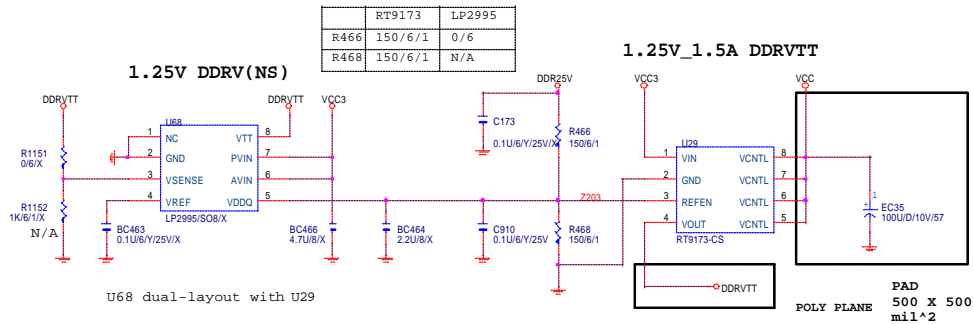
3300U6.3V/10X25 X4PCS

Default SANYO 1500U/D/6.3V/8*20
Second source: Panasonic FJ 1500U/D/10V/8*20
上2顆3300U, 4顆1500U.

TO-252 Hi-Side	TO-252 Lo-Side
PHD66N03(m ohm)	PHD98N03(m ohm)
IPD09N03LA(8.6m ohm)	IPD06N03LA(5.7m ohm)
2SK3638(8.5m ohm)	2SK3639(5.5m ohm)

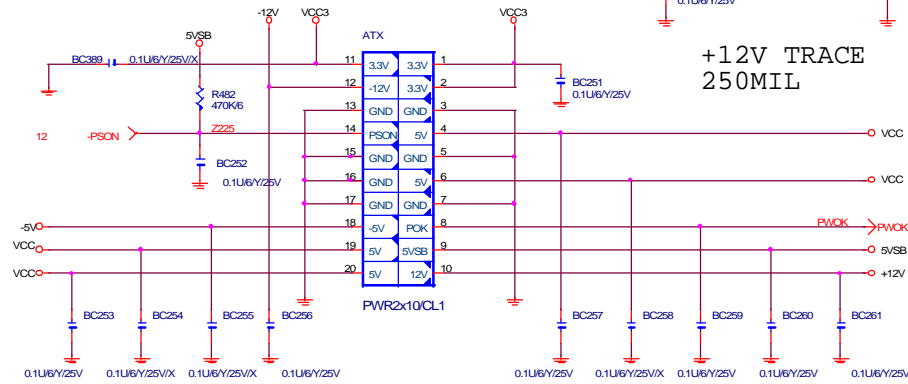
GIGABYTE		
VCORE (PWM FAN5093M)		
Title		
Size	Document Number	Rev
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1.25V DDRVTT LINEAR SOLUTION



ATX CONN, DC POWER

ATX POWER CONNECTOR



21,28,29,30

ITEM	DESCRIPTION	STATUS	Default
GP00	Non Use		Hi
GP01	Non Use		Hi
GP04	Non Use		Hi
GP02	Non Use		Hi
GP03	Green Button	Hi:Normal, Lo:Into Green mode	Hi
GPIO5	REQ5		
GPIO6	GNT5		
GP07	Non Use		Hi
GP011	Non Use		Hi
GP18	Wake On Ring	Hi:Normal, Lo:Ring Power On	Hi
GP19	Case Open	Hi:Case Open, Lo:Normal	Lo
GP110	Clear Caseopen status	Hi:Clear Caseopen Status, Lo:Normal	Lo
GP113	Non Use		Hi
GP012	Non Use		Hi
GP114	Primary Down	Lo:CODEC Only	Lo
GPIO15	KB Data		Hi
GPIO16	KB Clk		Hi
GPIO17	MS Data		Hi
GPIO18	MS Clk		Hi

States for a single-color power LED

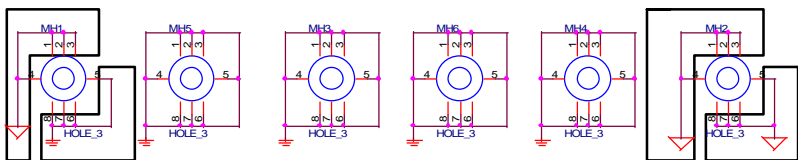
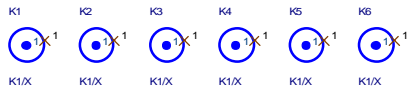
LED States	ACPI States	MPD+	MPD-	BIOS	
				GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING

States for a dual-color power LED

LED States	ACPI States	MPD+	MPD-	BIOS	
				GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING
Steady Yellow	S1,S3	LO	HI	HI	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING	HI	BLINKING

States for green LED

LED States	ACPI States	GLLED-	BIOS
			GPIO11
ON	S1,S3	HI	HI
OFF	S0,S5	LO	LO



EMI (VCC.GND CUT HOLE PLANE)

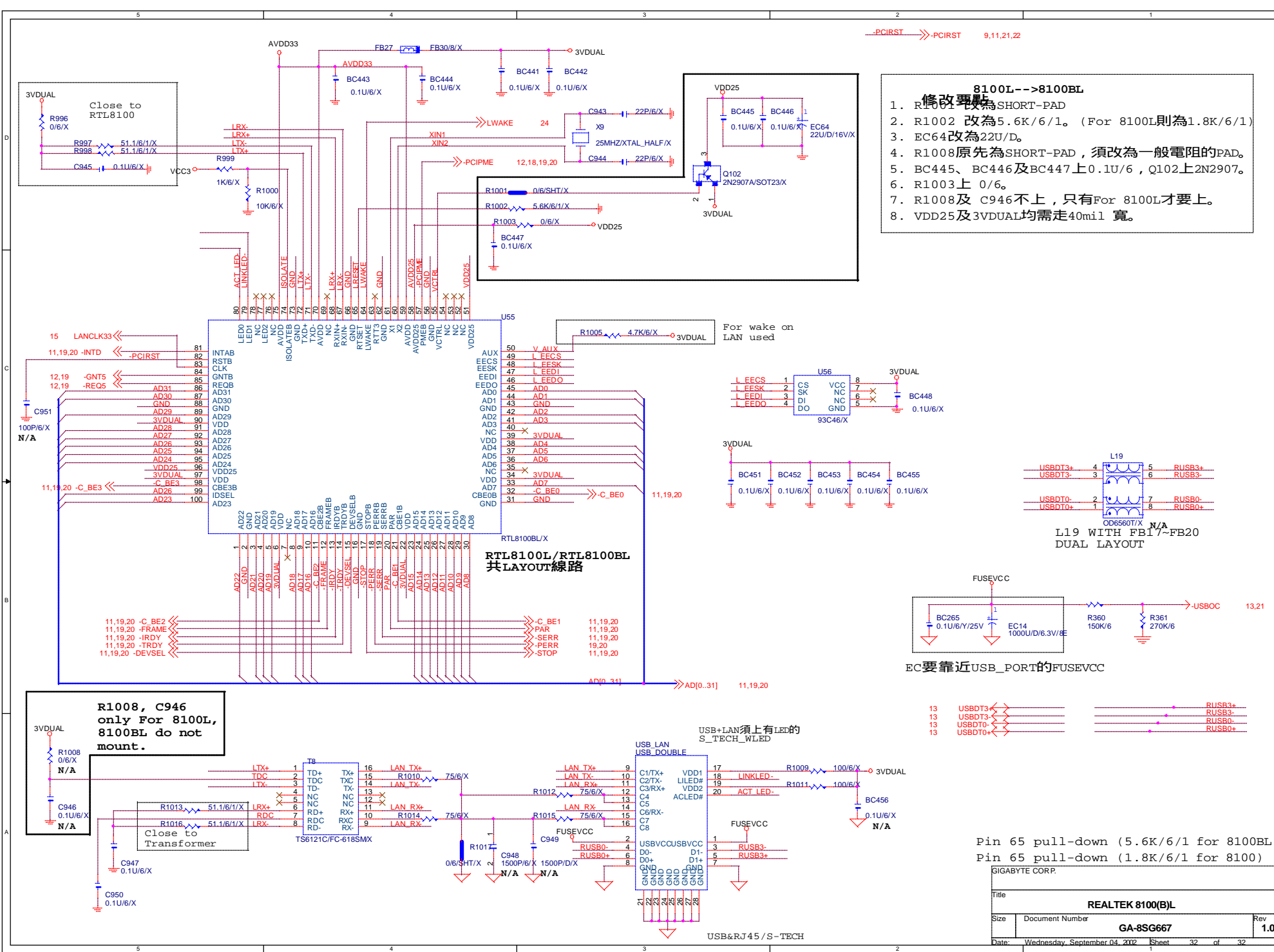
EMI (VCC.LGND CUT HOLE PLANE)

BIOS REQUEST

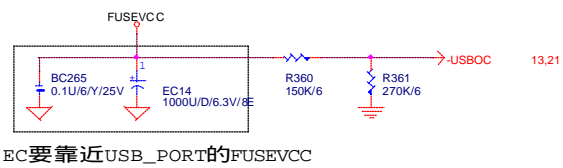
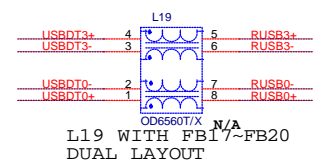
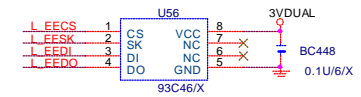
SINGLE	DUAL	INTEL LED DEFINED				GIGABYTE LED DEFINED				SINGLE	DUAL
		GPIO7	ACPILED	GPIO11		GPIO7	ACPILED	GPIO11			
GREEN	GREEN	S0	LO	LO	LO	S0	LO	LO	LO	GREEN	GREEN
OFF	YELLOW	S1	HI	HI	HI	S1	LO	BLINKING	HI	G(BLINK)	G(BLINK)
OFF	YELLOW	S3	HI	HI	HI	S3	HI	HI	HI	OFF	YELLOW
OFF	OFF	S4/S5	LO	HI/NC	LO	S4/S5	LO	HI/NC	LO	OFF	OFF

GIGABYTE

Title			ATX, GPIO LIST		
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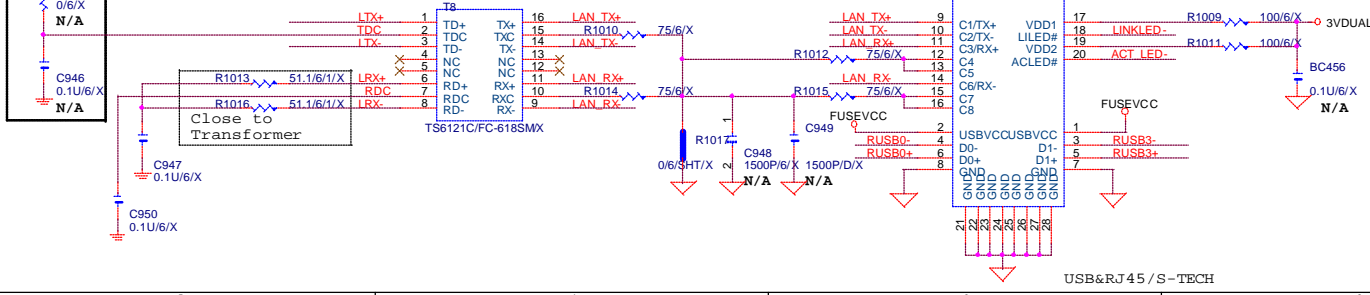
- 8100L-->8100BL**
1. R1001 改為 SHORT-PAD
 2. R1002 改為 5.6K/6/1。(For 8100L則為 1.8K/6/1)
 3. EC64 改為 22U/D.
 4. R1008 原先為 SHORT-PAD, 須改為一般電阻的 PAD.
 5. BC445、BC446 及 BC447 上 0.1U/6, Q102 上 2N2907.
 6. R1003 上 0/6.
 7. R1008 及 C946 不上, 只有 For 8100L 才要上.
 8. VDD25 及 3VDUAL 均需走 40mil 寬.



EC要靠近USB_PORT的FUSEVCC



R1008, C946 only For 8100L, 8100BL do not mount.



Pin 65 pull-down (5.6K/6/1 for 8100BL)
Pin 65 pull-down (1.8K/6/1 for 8100)

GIGABYTE CORP.		
Title		
REALTEK 8100(B)L		
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