

Model Name: 8N-SLI Royal Revision 1.02

SHEET TITLE

01	COVER SHEET
02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	P4_LGA775_A
05	P4_LGA775_B
06	P4_LGA775_C
07	P4_LGA775_D
08	Crush19 CPU
09	Crush19 PCI-Ex16 & x1
10	Crush19 HT Interface
11	Crush19 DDRII (CHa & CHb)
12	Crush19 Power & GND
13	MCP04 HT, PCI, IDE
14	MCP04 CPU, GPIO, AC97, LPC, RGMII
15	MCP04 USB, SATAII, Clock
16	MCP04 Power & GND
17	DDRII CHANNEL A 1-2
18	DDRII CHANNEL B 3-4
19	DDRII TERMINATION
20	PCI EXPRESS*16 SLOT
21	PCI EXPRESS*16-2 SLOT (8 Lanes)
22	PCI EXPRESS*1 SLOT 1, 2
23	NV-SLI Slot
24	PCI SLOT 1, 2 FWH
25	ITE 8712GB
26	H/W MONITOR & Caseopen
27	Prochot , FAN Control , Thermal Shdn

SHEET TITLE

28	IDE 1-2, FDD
29	FRONT USB
30	KB_PS2
31	AUDIO CODEC ALC850
32	AUDIO JACK 1 & 2
33	COM_LPT
34	FRONT PANEL
35	DUAL BIOS
36	DISCRETE POWER
37	MARVELL 88E8053 PCI-E LAN
38	MARVELL 88E8111 RGMII LAN
39	Promise PDC20779 SATAII
40	PDC20779 SATAII 4-5
41	TI 1394B-1
42	TI 1394B-2
43	ATX POWER CONN.
44	DPS-1
45	DPS-2
46	DPS-3

PCB Vendor: 智恩, 育富, 祥裕

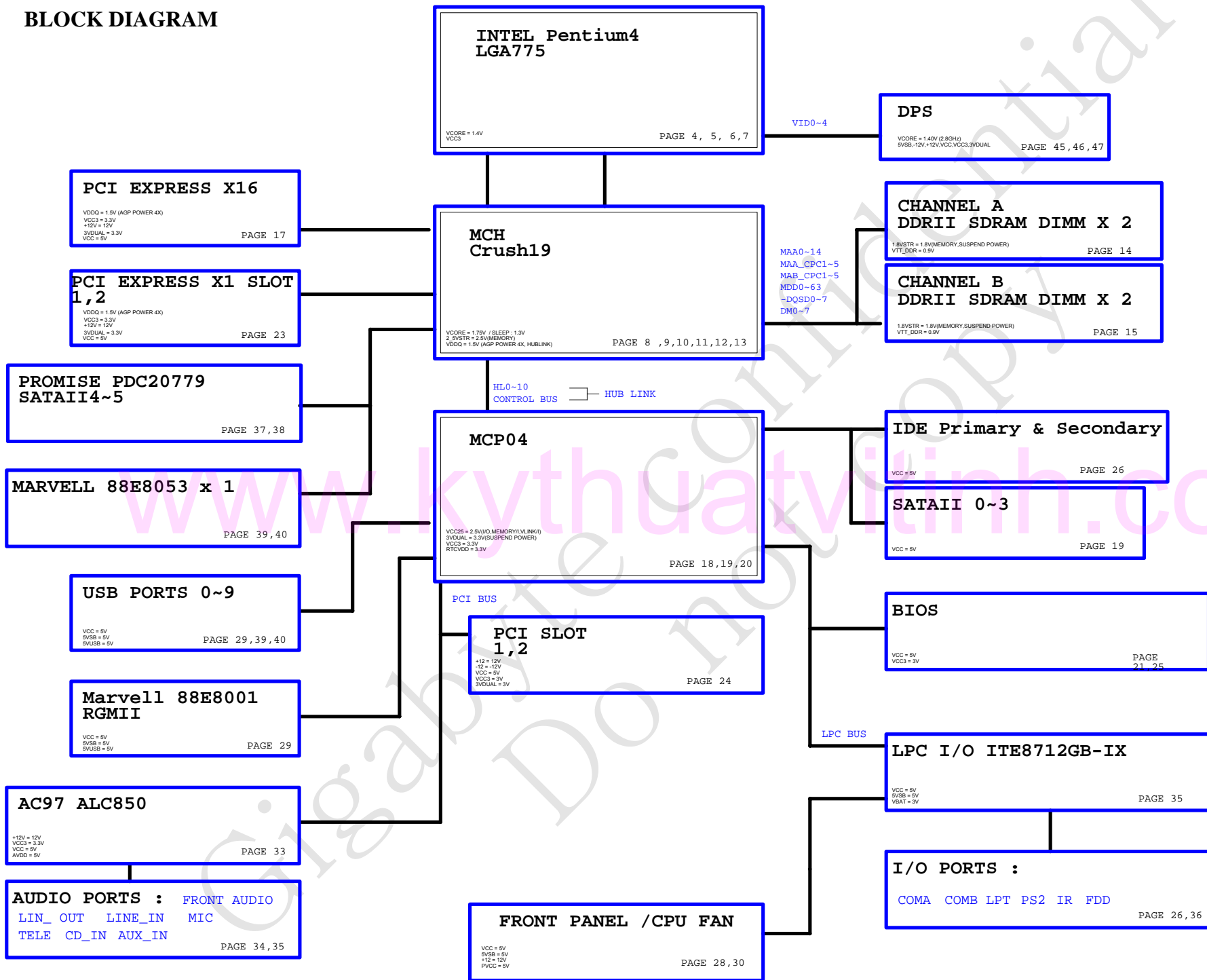
PCB Size: 304.80\*243.84 mm

PCB Stack: Top, VCC, INT1, INT2, GND, Bottom

**Gigabyte Technology**

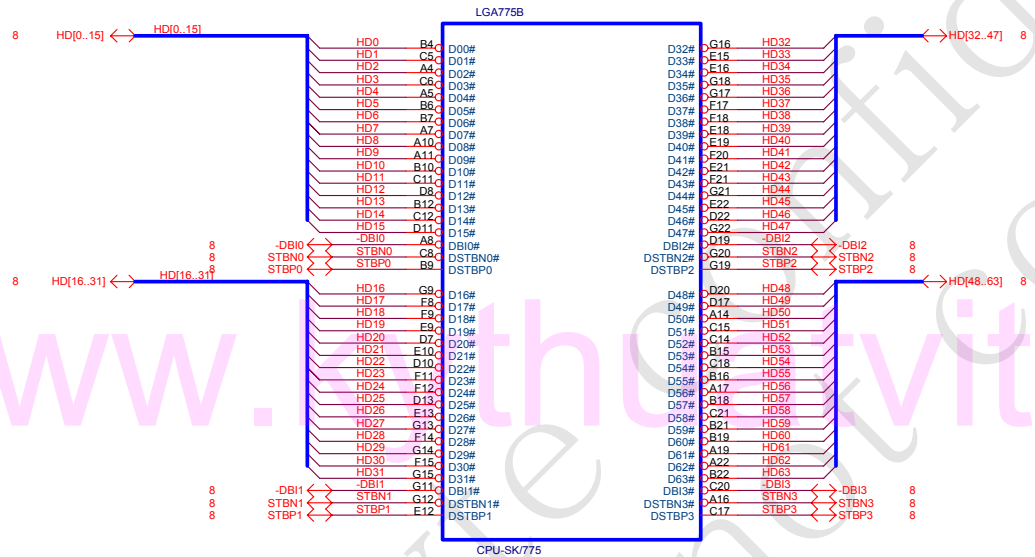
Title		Cover Sheet	
Size	Document Number	Rev	
Custom	8N-SLI Royal	1.02	
Date:	Thursday, May 19, 2005	Sheet	1 of 46

# BLOCK DIAGRAM



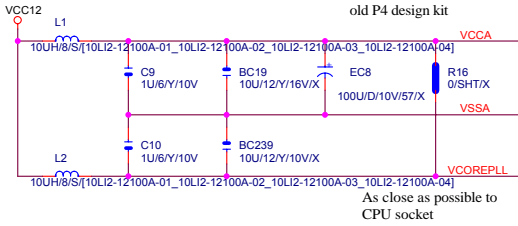




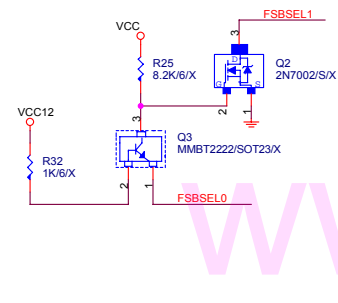


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**Note:**  
VCCA & VCOREPLL  
define doesn't same as  
old P4 design kit

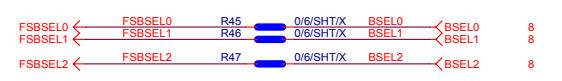
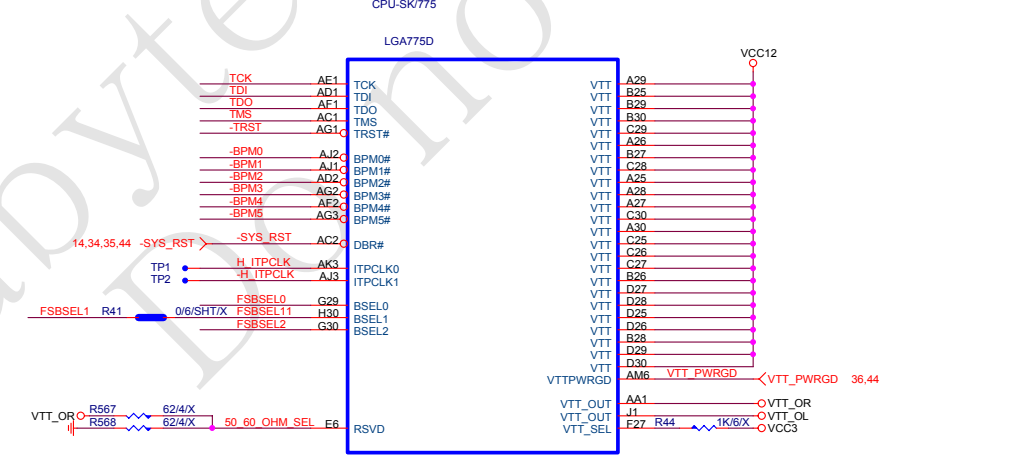
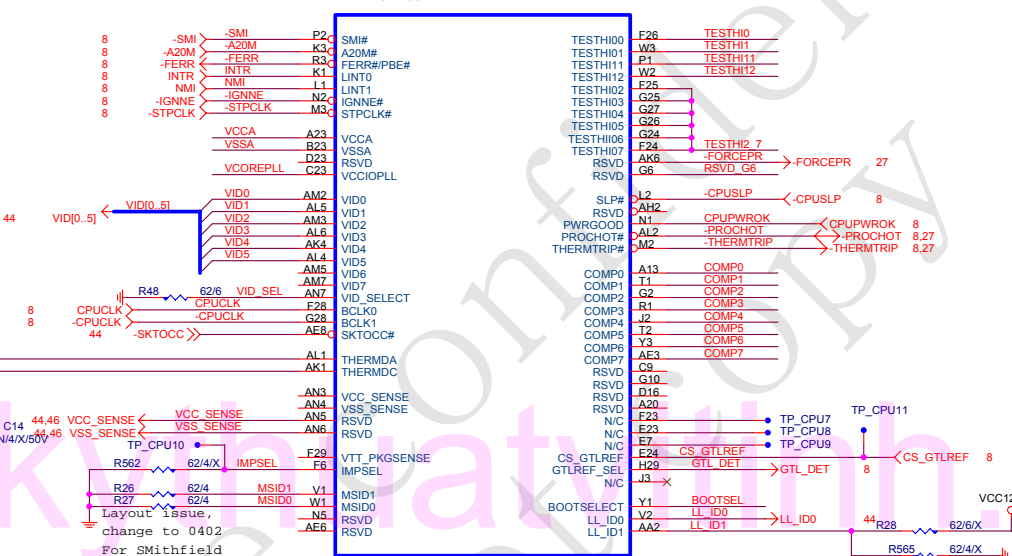
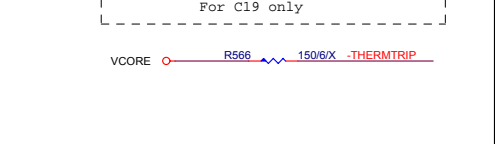
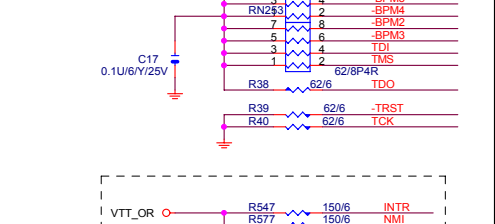
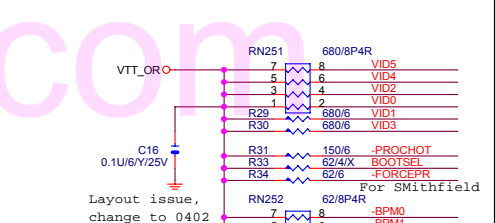
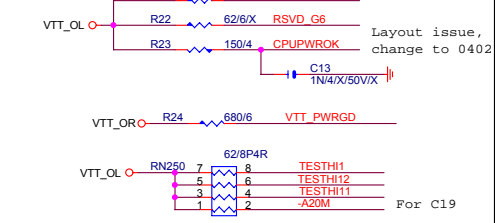
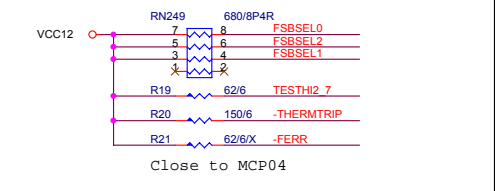
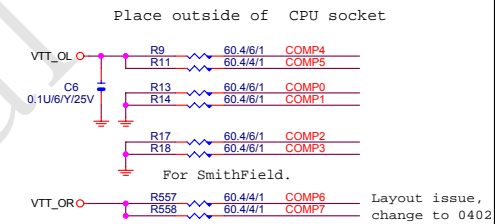
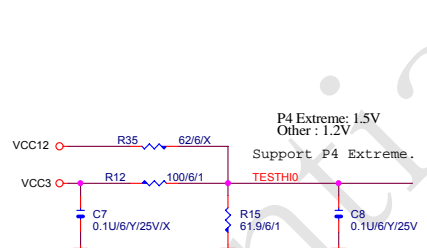
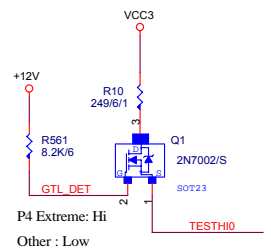


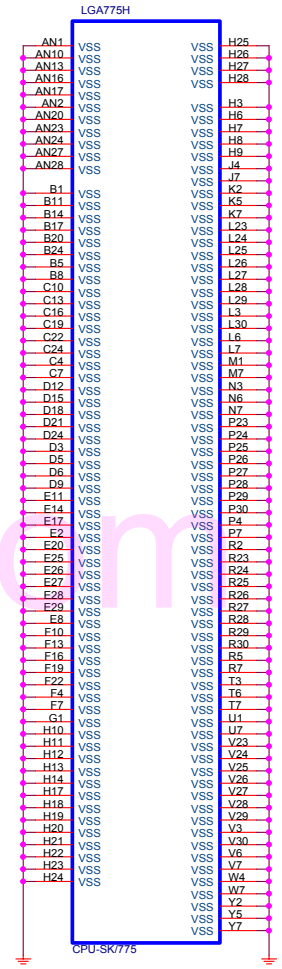
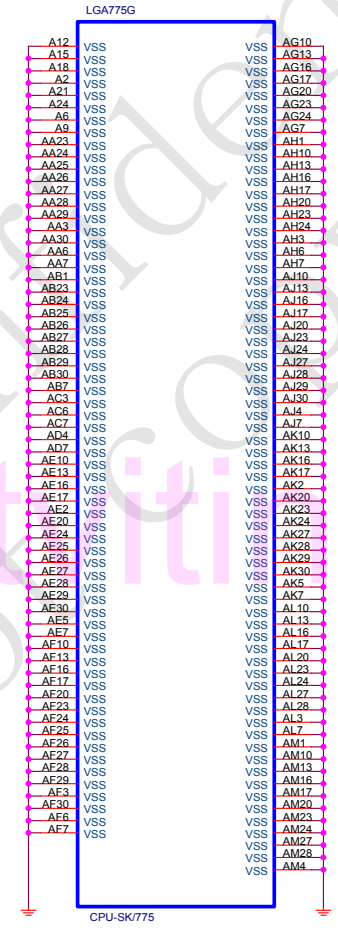
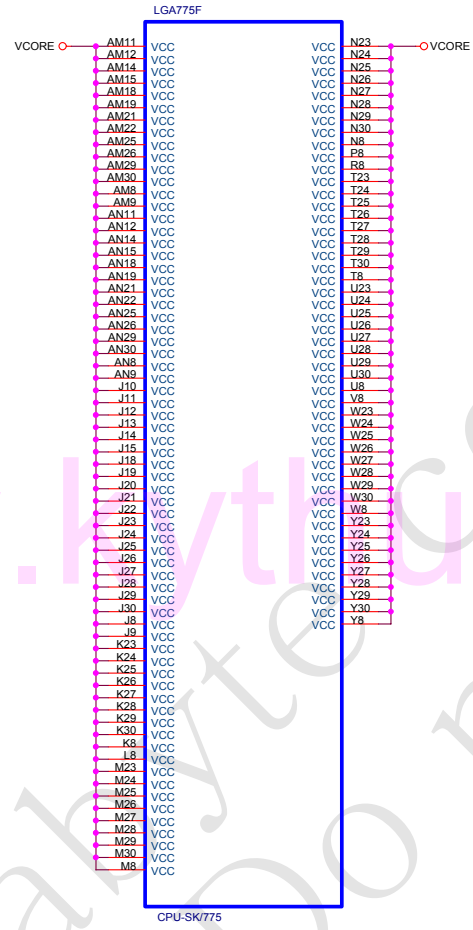
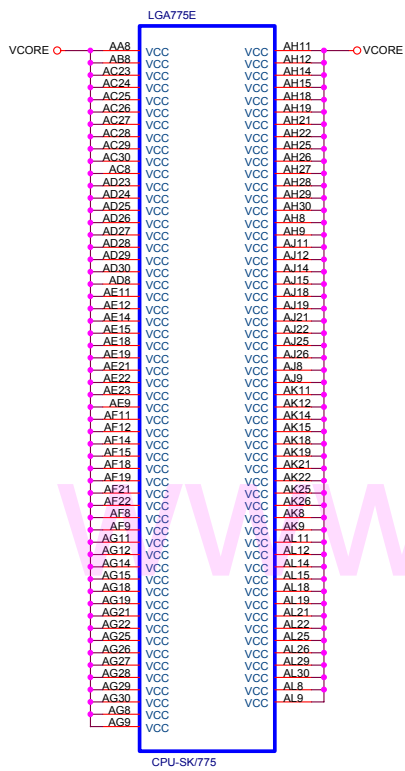
As close as possible to CPU socket  
Remove -CPUSLP cap



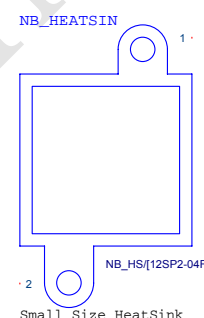
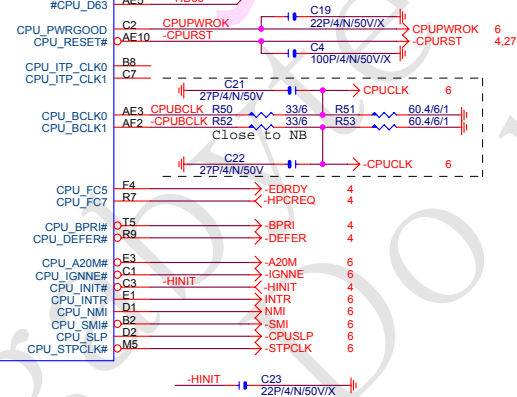
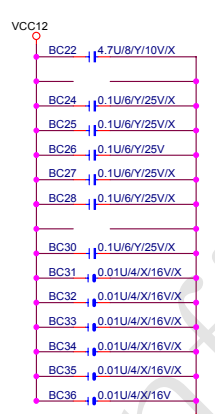
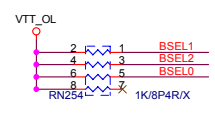
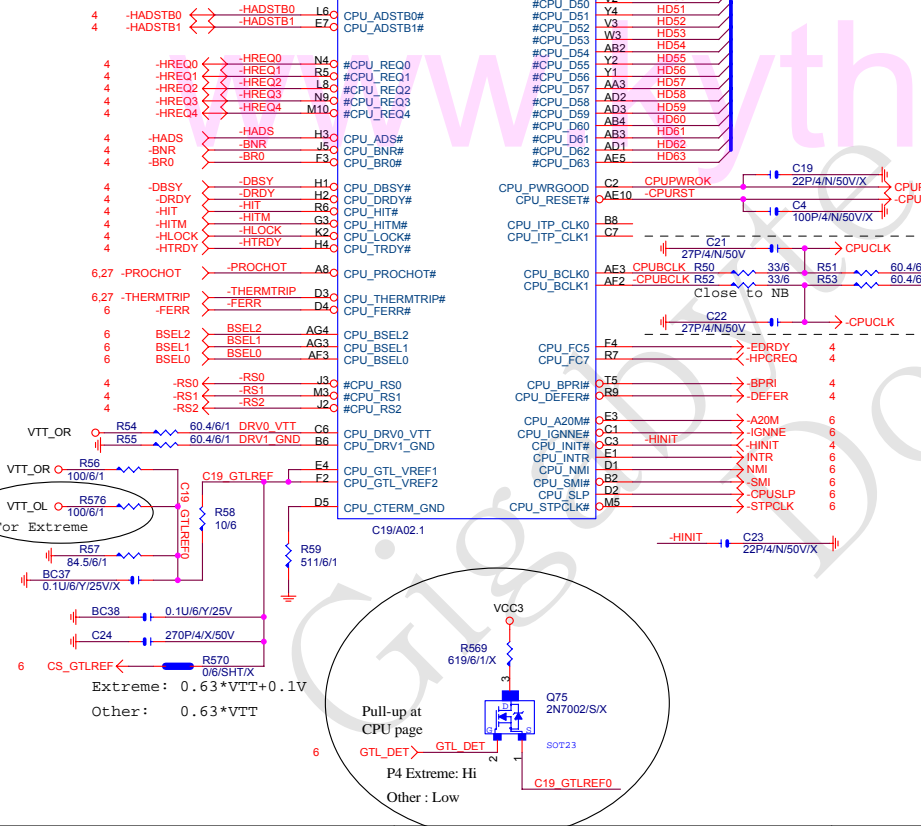
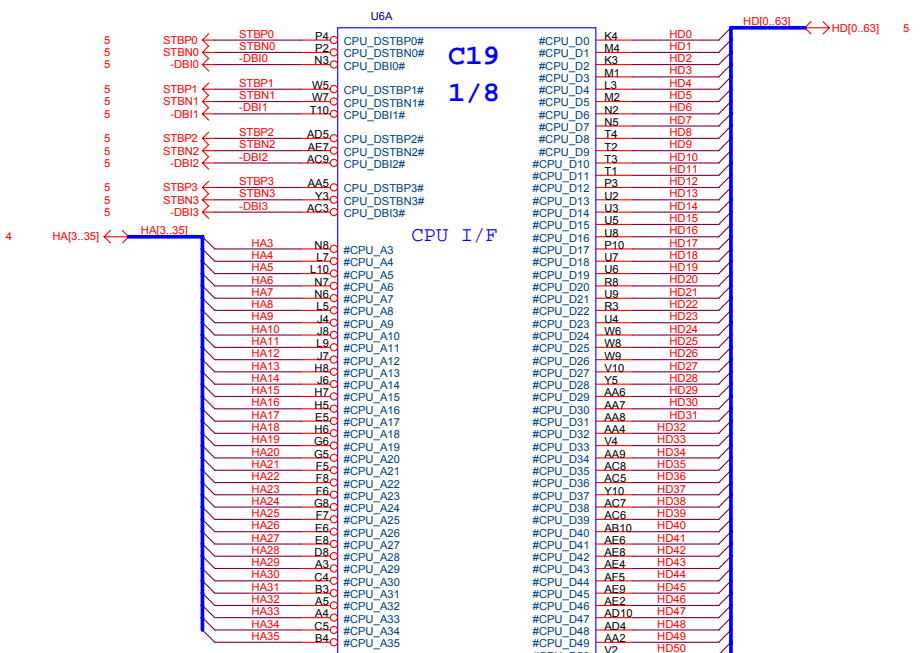
**CPU FSB**

FSBSEL2	FSBSEL1	FSBSEL0	Clock	
1	0	0	100MHz	X
0	0	1	133MHz	
0	1	1	166MHz	X
0	1	0	200MHz	
0	0	0	266MHz	

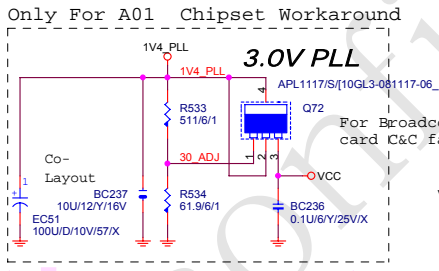
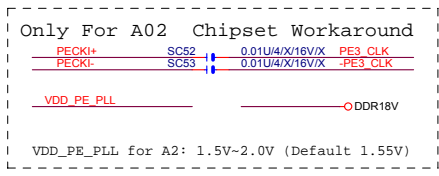
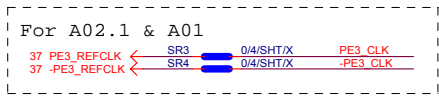
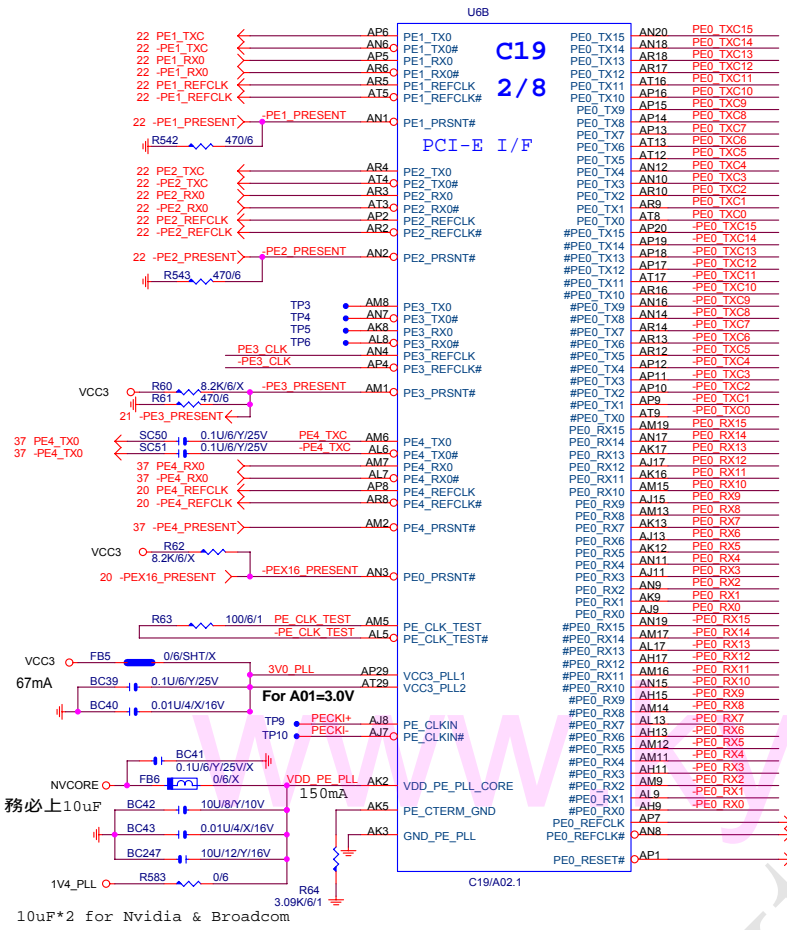




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<b>Gigabyte Technology</b>			
Title		<b>C19_CPU</b>	
Size	Document Number	<b>8N-SLI Royal</b>	
Custom			Rev <b>1.02</b>
Date:	Thursday, May 19, 2005	Sheet	8 of 46



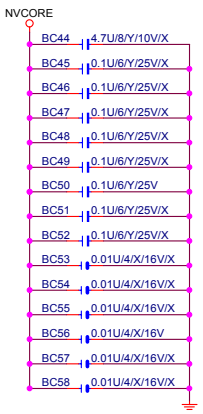
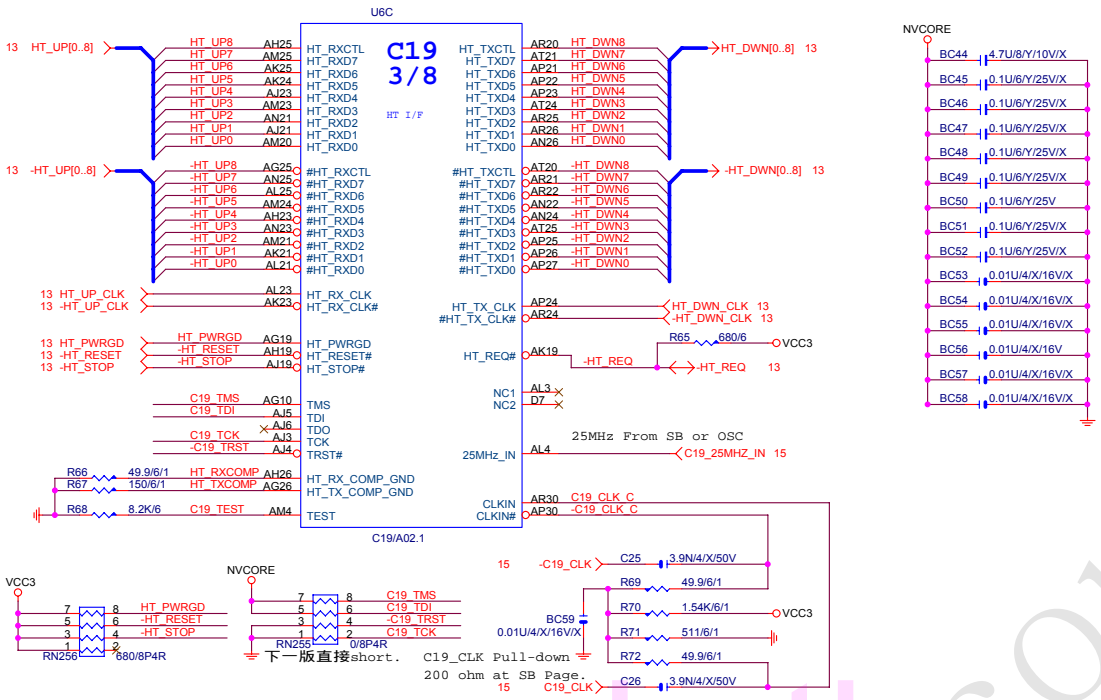
- PE0\_TXC[0..15] >>> PE0\_TXC[0..15] 23
- PE0\_TXC[0..15] >>> -PE0\_TXC[0..15] 23
- PE0\_RX[0..15] >>> PE0\_RX[0..15] 23
- PE0\_RX[0..15] >>> -PE0\_RX[0..15] 23
- PE0\_REFCLK 21
- PE0\_REFCLK 21
- PCI\_E\_RST 20,21,22,37

10uF\*2 for Nvidia & Broadcom

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Do not edit

<b>Gigabyte Technology</b>			
Title <b>C19_PCI-E</b>			
Size Custom	Document Number	<b>8N-SLI Royal</b>	
Date: Thursday, May 19, 2005	Sheet	9	of 46
			Rev <b>1.02</b>

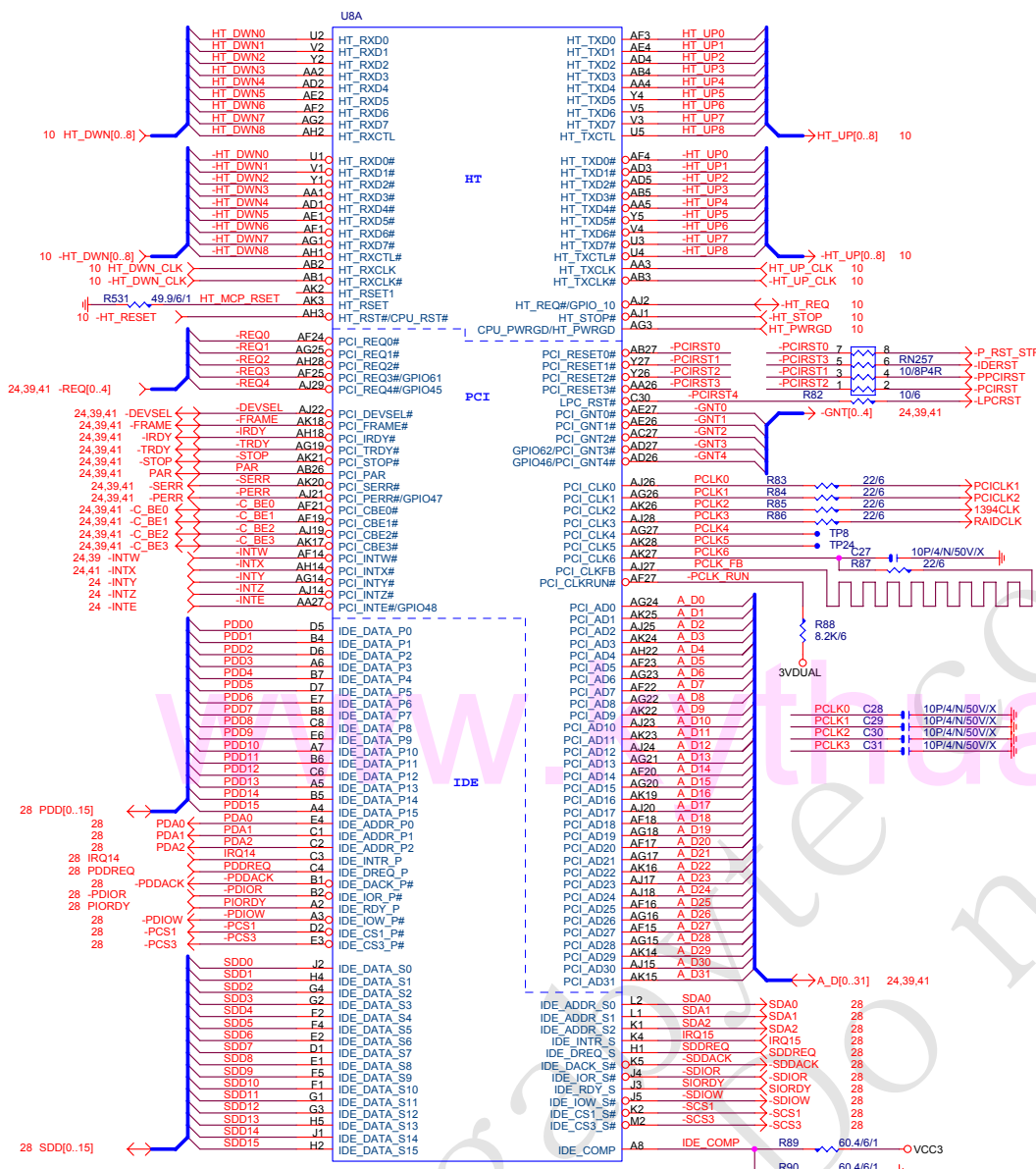


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<b>Gigabyte Technology</b>		
Title: C19_HT		
Size Custom	Document Number: 8N-SLI Royal	Rev: 1.02
Date: Thursday, May 19, 2005	Sheet: 10	of 46







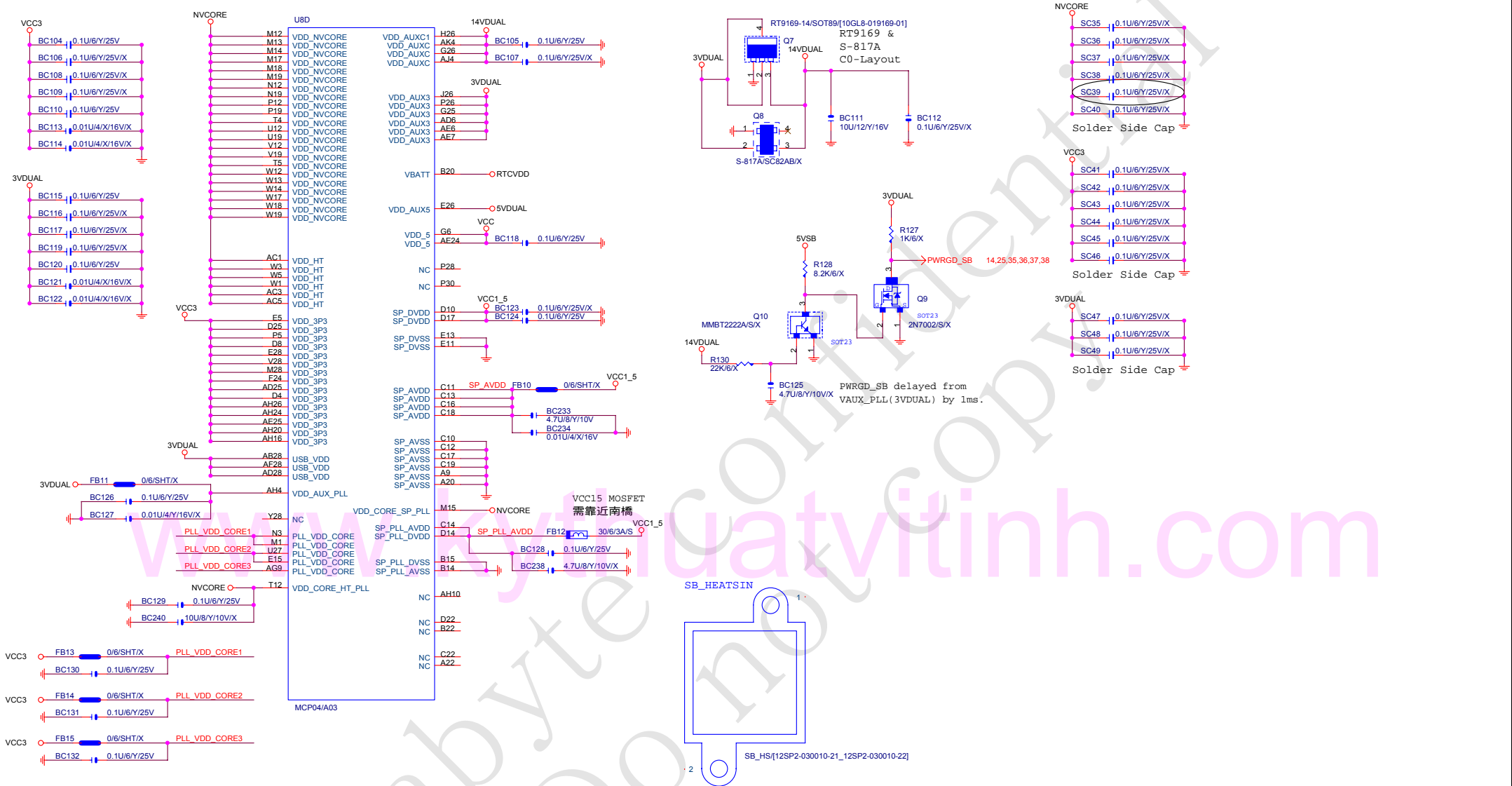
	IDSEL	INTA#	REQ#
PCI1	AD22	INTY	0
PCI2	AD23	INTZ	1
T11394B	AD28	INTX	3
PDC20779	AD24	INTW	2

Gigabyte Technology

Title			MCP04_HT_PCI_IDE
Size	Document Number	8N-SLI Royal	
Custom		Rev	1.02
Date:	Thursday, May 19, 2005	Sheet	13 of 46

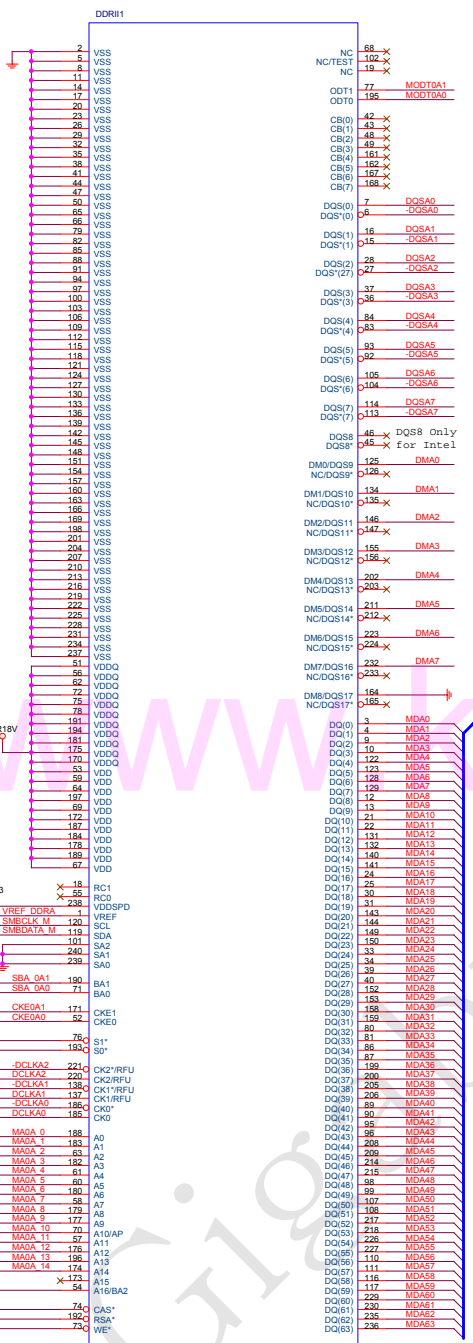






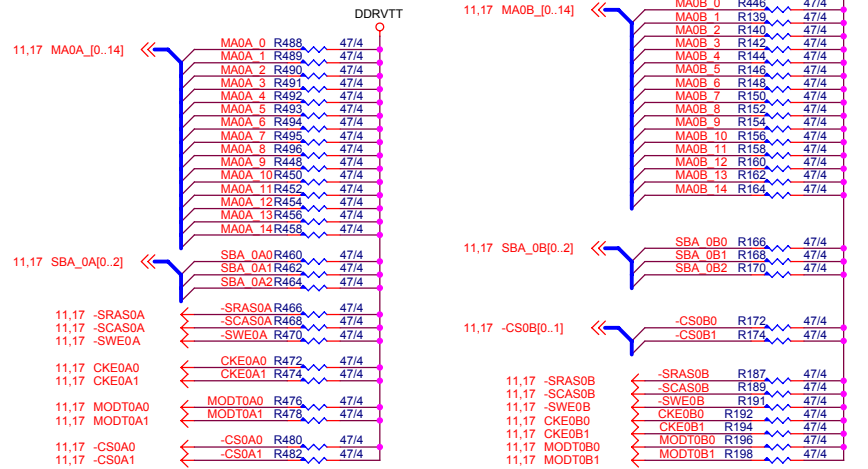
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<b>Gigabyte Technology</b>			
Title <b>MCP04_POWER_GND</b>			
Size	Document Number	<b>8N-SLI Royal</b>	Rev
			<b>1.02</b>
Date:	Thursday, May 19, 2005	Sheet	16 of 46

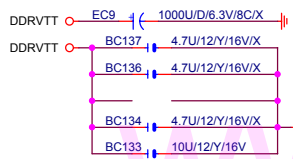




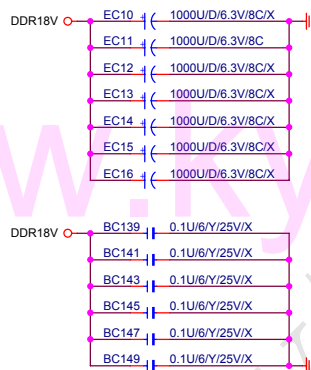
# DDR TERMINATION CHANNEL A



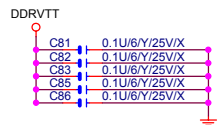
## DDRVTT Decouple



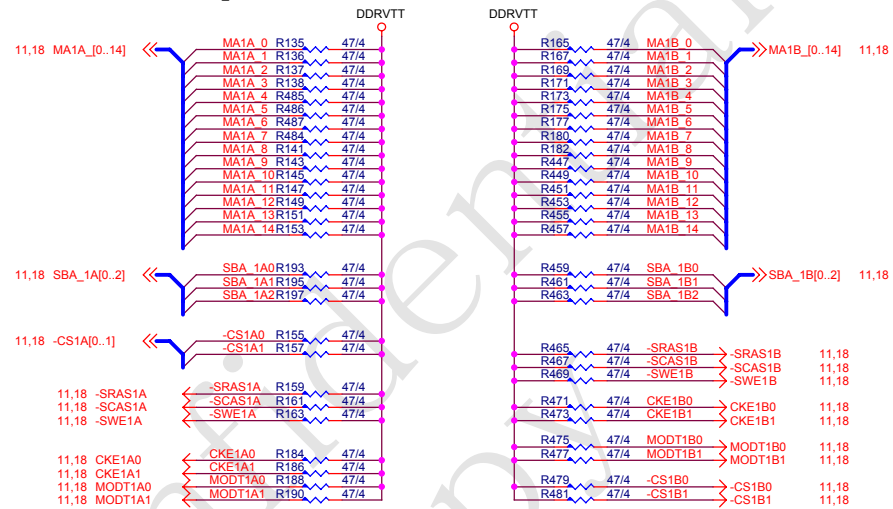
## DDR18V Decouple



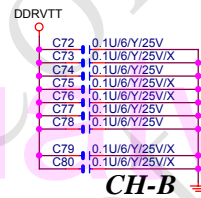
## CH-A



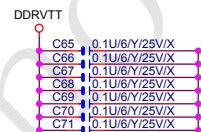
# DDRVTT Decouple CHANNEL B



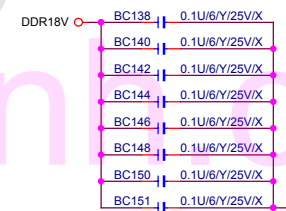
## DDRVTT Decouple

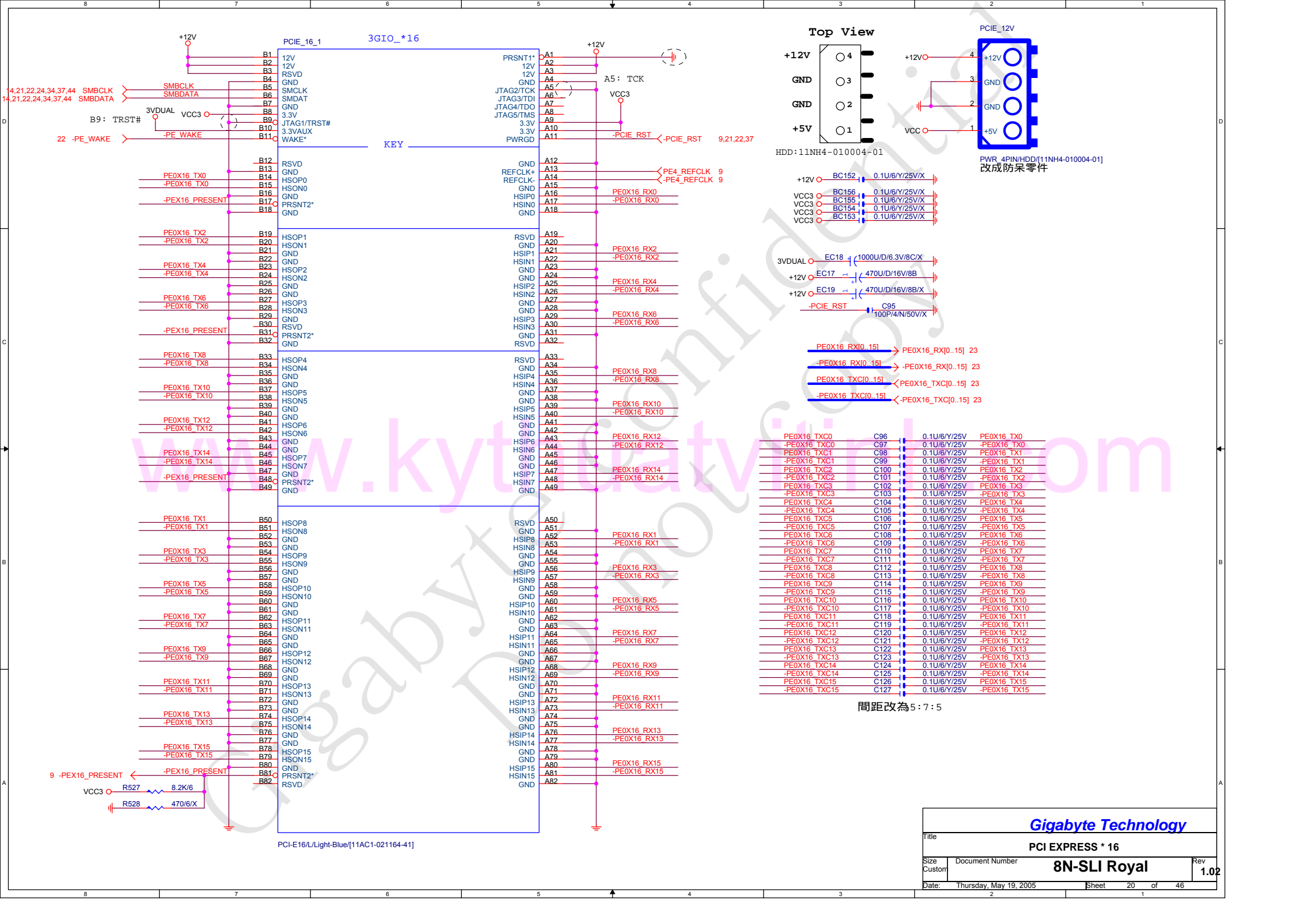


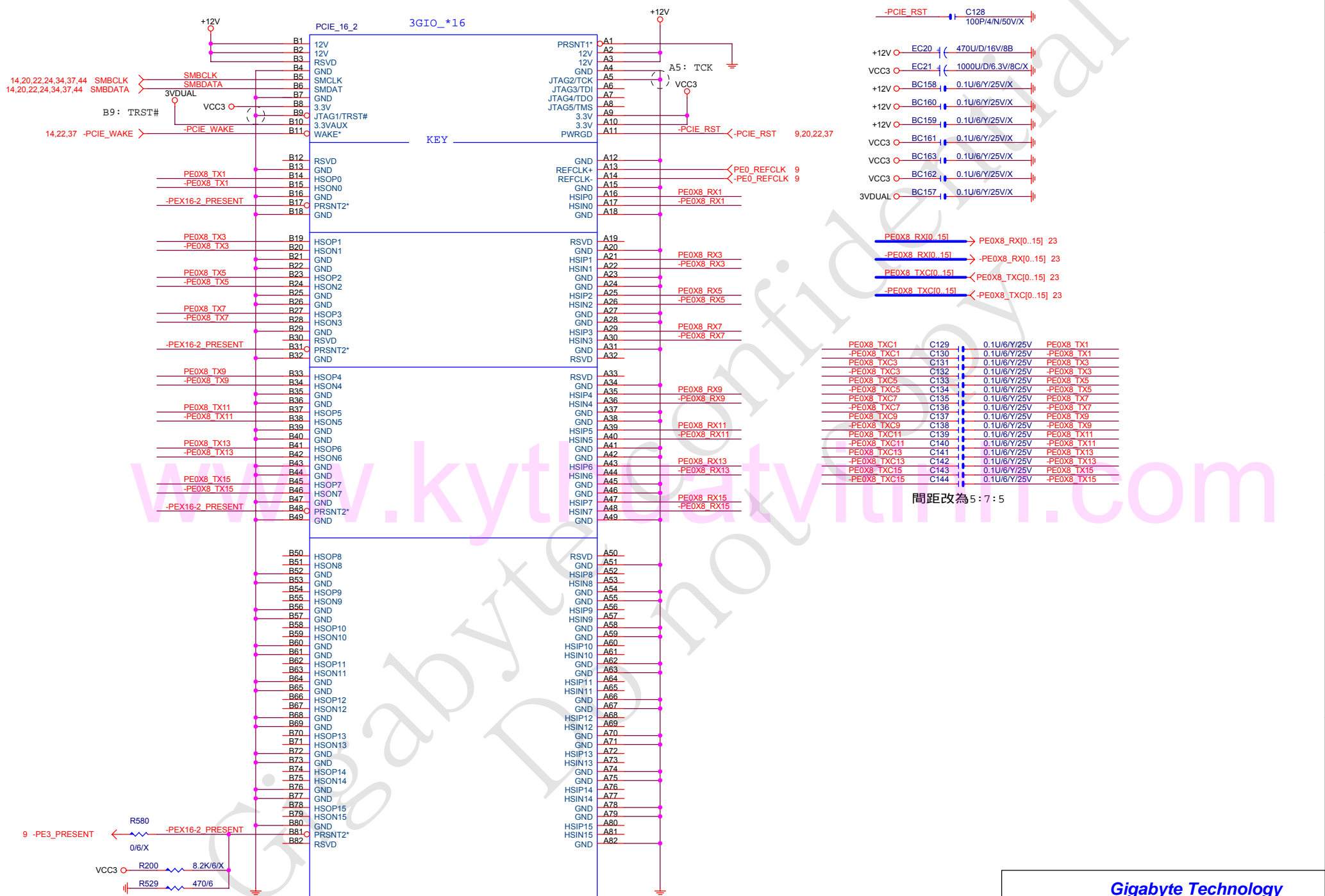
## CH-B



## DDR18V Decouple







- PCIE\_RST C128 100P/4N/50V/X
- +12V EC20 470U/D/16V/8B
- VCC3 EC21 1000U/D/6.3V/8C/X
- +12V BC158 0.1U/6/Y/25V/X
- +12V BC160 0.1U/6/Y/25V/X
- +12V BC159 0.1U/6/Y/25V/X
- VCC3 BC161 0.1U/6/Y/25V/X
- VCC3 BC163 0.1U/6/Y/25V/X
- VCC3 BC162 0.1U/6/Y/25V/X
- 3VDUAL BC157 0.1U/6/Y/25V/X

- PE0X8 RXI0..15I PE0X8\_RXI[0..15] 23
  - PE0X8 RXI0..15I -PE0X8\_RXI[0..15] 23
  - PE0X8 TXCI0..15I PE0X8\_TXCI[0..15] 23
  - PE0X8 TXCI0..15I -PE0X8\_TXCI[0..15] 23
- |              |      |              |             |
|--------------|------|--------------|-------------|
| PE0X8 TXC1   | C129 | 0.1U/6/Y/25V | PE0X8 TX1   |
| -PE0X8 TXC1  | C130 | 0.1U/6/Y/25V | -PE0X8 TX1  |
| PE0X8 TXC3   | C131 | 0.1U/6/Y/25V | PE0X8 TX3   |
| -PE0X8 TXC3  | C132 | 0.1U/6/Y/25V | -PE0X8 TX3  |
| PE0X8 TXC5   | C133 | 0.1U/6/Y/25V | PE0X8 TX5   |
| -PE0X8 TXC5  | C134 | 0.1U/6/Y/25V | -PE0X8 TX5  |
| PE0X8 TXC7   | C135 | 0.1U/6/Y/25V | PE0X8 TX7   |
| -PE0X8 TXC7  | C136 | 0.1U/6/Y/25V | -PE0X8 TX7  |
| PE0X8 TXC9   | C137 | 0.1U/6/Y/25V | PE0X8 TX9   |
| -PE0X8 TXC9  | C138 | 0.1U/6/Y/25V | -PE0X8 TX9  |
| PE0X8 TXC11  | C139 | 0.1U/6/Y/25V | PE0X8 TX11  |
| -PE0X8 TXC11 | C140 | 0.1U/6/Y/25V | -PE0X8 TX11 |
| PE0X8 TXC13  | C141 | 0.1U/6/Y/25V | PE0X8 TX13  |
| -PE0X8 TXC13 | C142 | 0.1U/6/Y/25V | -PE0X8 TX13 |
| PE0X8 TXC15  | C143 | 0.1U/6/Y/25V | PE0X8 TX15  |
| -PE0X8 TXC15 | C144 | 0.1U/6/Y/25V | -PE0X8 TX15 |

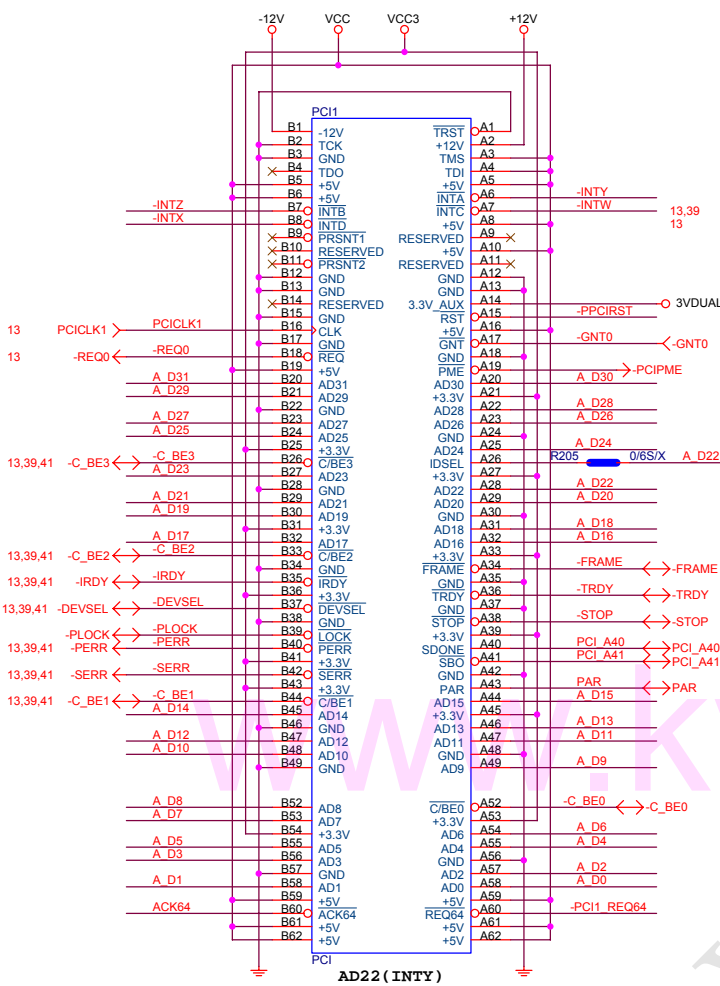
間距改為 5 : 7 : 5

PCI-E16/L/Black[11AC1-021164-21] only 8 Lanes  
Black

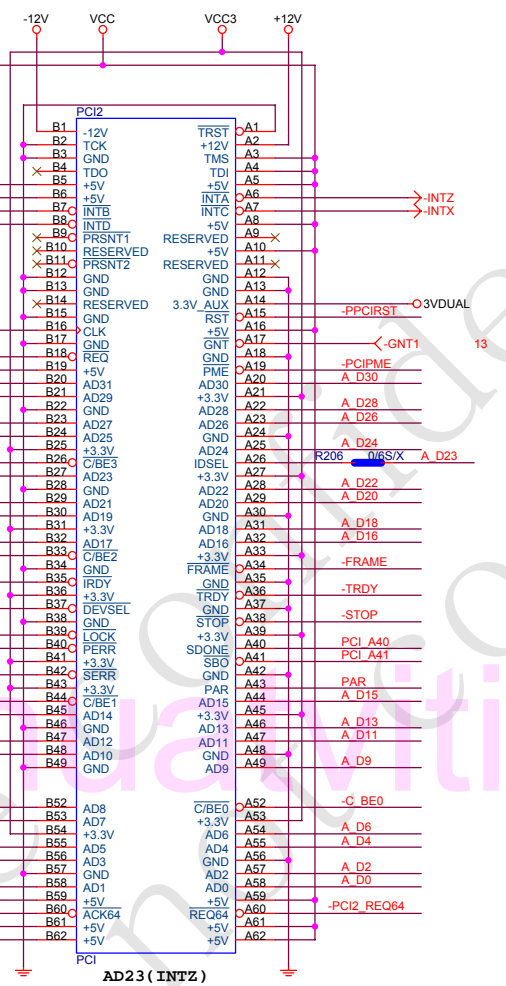
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Title: <b>PCI EXPRESS X 8</b>		
Size Custom	Document Number: <b>8N-SLI Royal</b>	Rev: <b>1.02</b>
Date: Thursday, May 19, 2005	Sheet 21	of 46



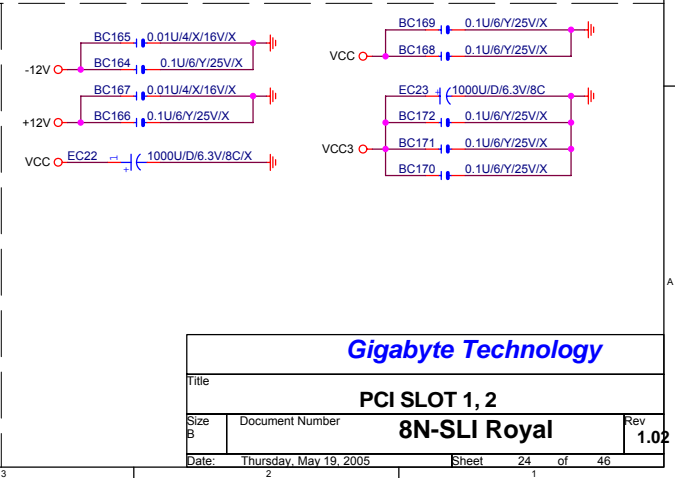
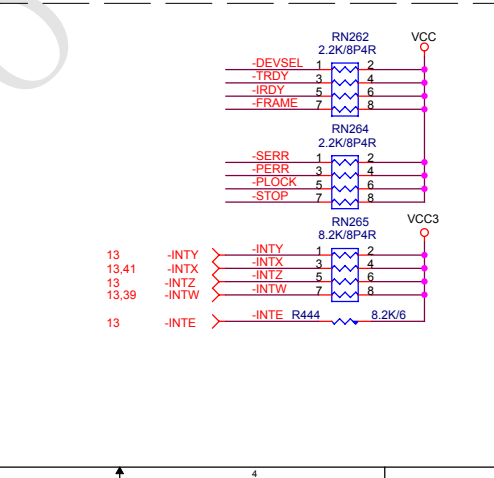
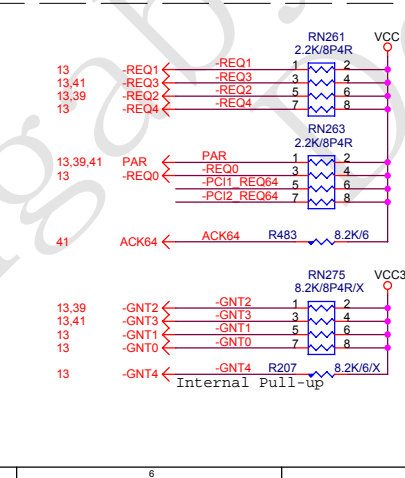
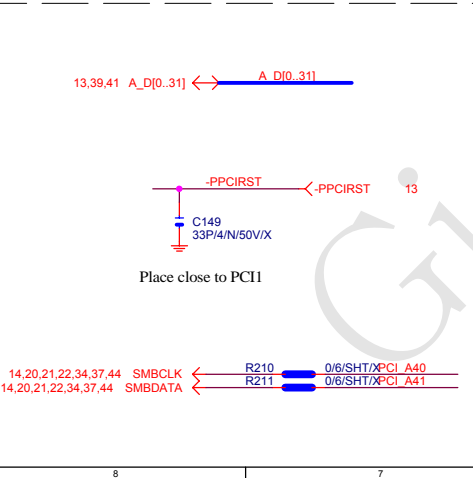




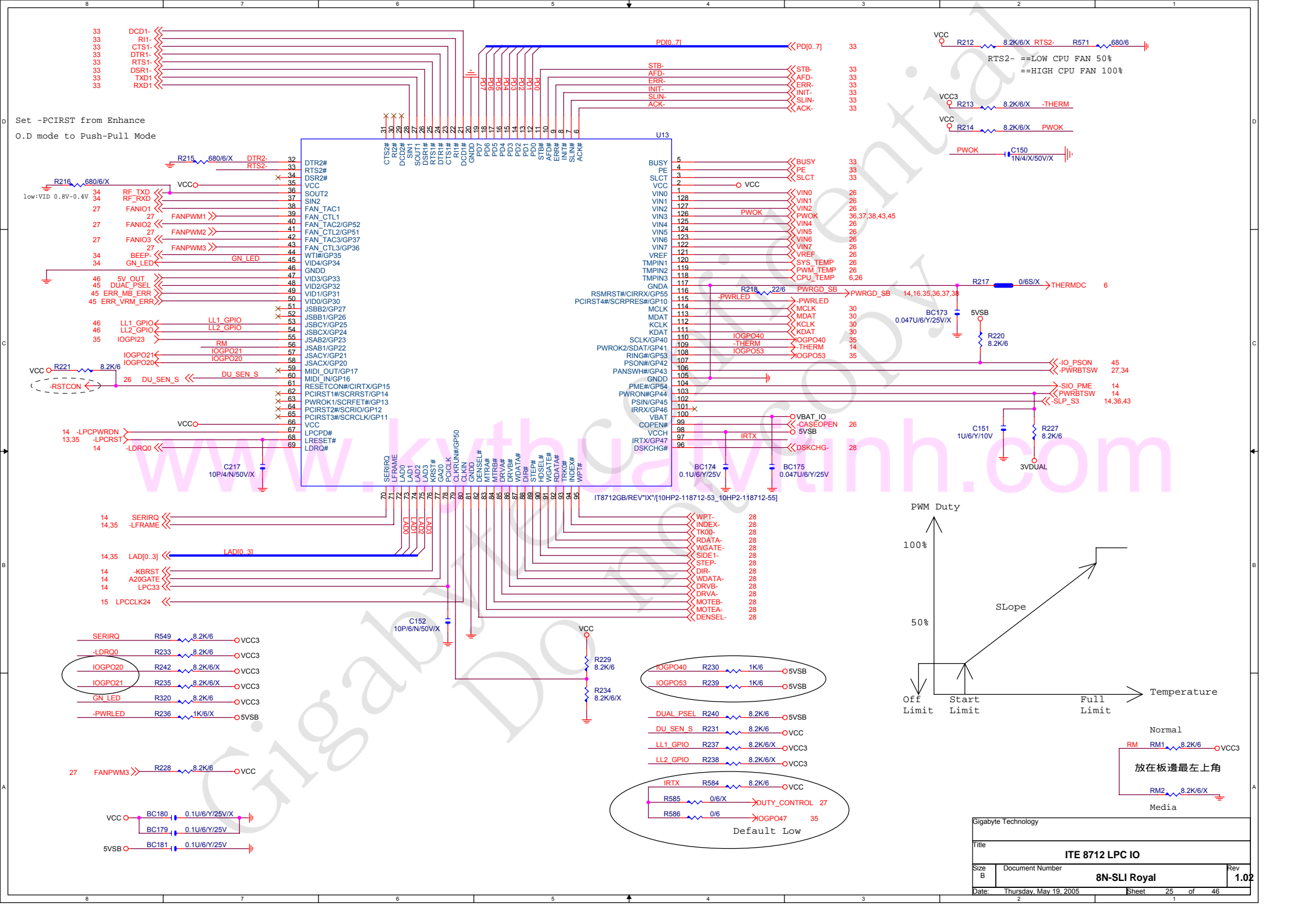
AD22 (INTY)



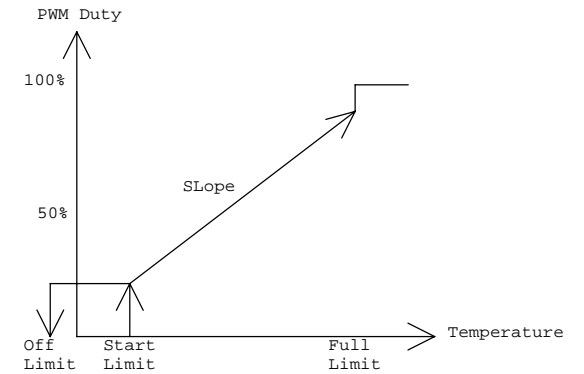
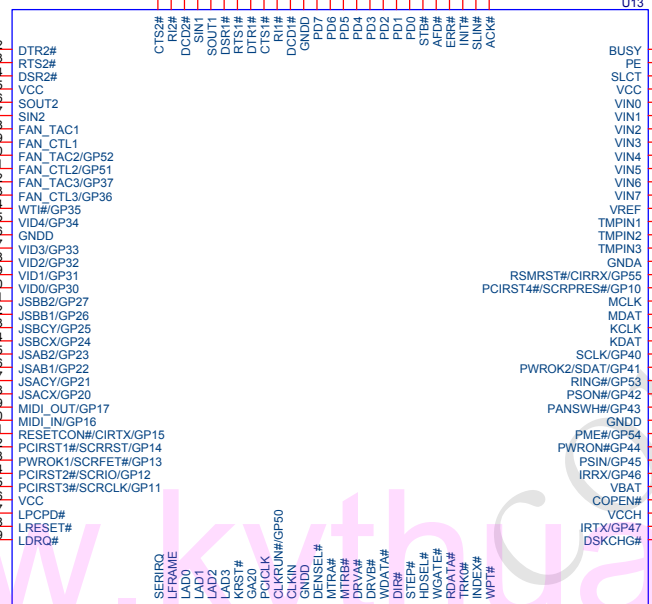
AD23 (INTZ)



<b>Gigabyte Technology</b>		
<b>PCI SLOT 1, 2</b>		
<b>8N-SLI Royal</b>		Rev <b>1.02</b>
Title	Document Number	Date: Thursday, May 19, 2005
Size B	Sheet 24	of 46

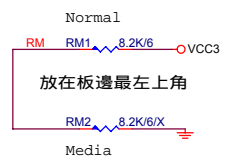


Set -PCIRST from Enhance  
O.D mode to Push-Pull Mode

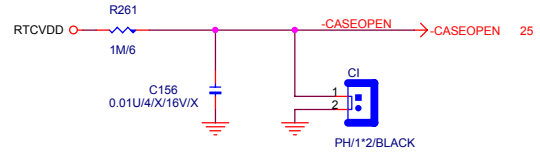
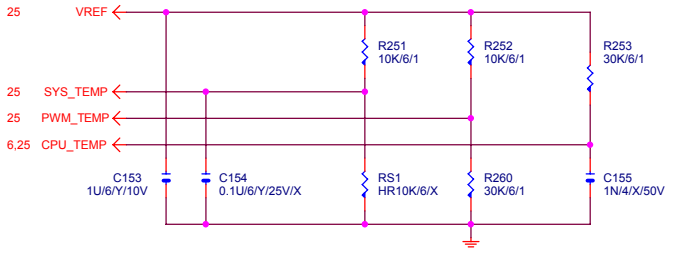


- SERIIRQ R549 8.2K/6 VCC3
- LDRQ0 R233 8.2K/6 VCC3
- IOGPO20 R242 8.2K/6/X VCC3
- IOGPO21 R235 8.2K/6/X VCC3
- GN\_LED R320 8.2K/6 VCC3
- PWRLED R236 1K/6/X 5VSB
- FANPWM3 R228 8.2K/6 VCC
- BC180 0.1U/6Y/25V VCC
- BC179 0.1U/6Y/25V VCC
- BC181 0.1U/6Y/25V 5VSB

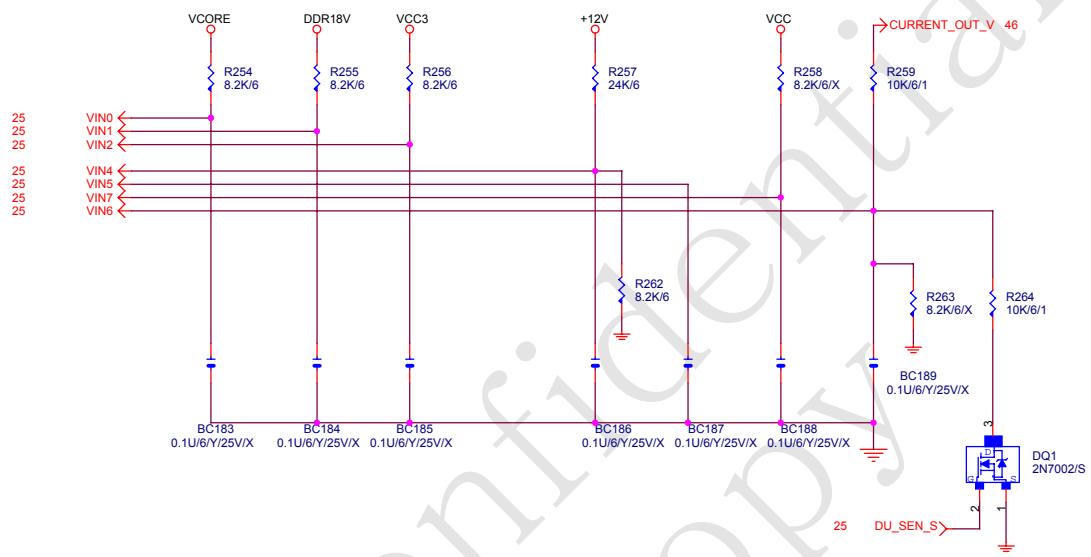
- IOGPO40 R230 1K/6 5VSB
- IOGPO53 R239 1K/6 5VSB
- DUAL\_PSEL R240 8.2K/6 5VSB
- DU\_SEN\_S R231 8.2K/6 VCC
- LL1\_GPIO R237 8.2K/6/X VCC3
- LL2\_GPIO R238 8.2K/6/X VCC3
- IRTX R584 8.2K/6 VCC
- R585 0/6/X DUTY\_CONTROL 27
- R586 0/6 IOGPO47 35



Gigabyte Technology			
Title			
ITE 8712 LPC IO			
Size B	Document Number	Rev 1.02	
8N-SLI Royal			
Date: Thursday, May 19, 2005	Sheet 25	of 46	



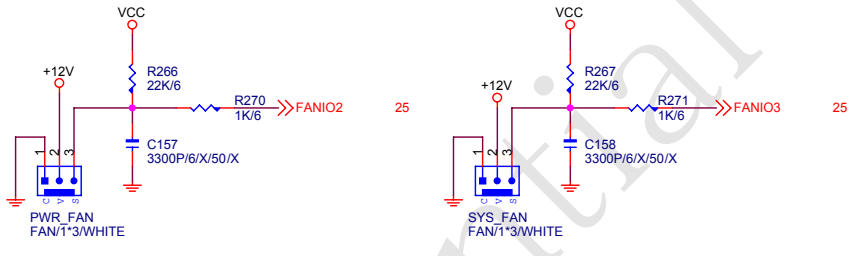
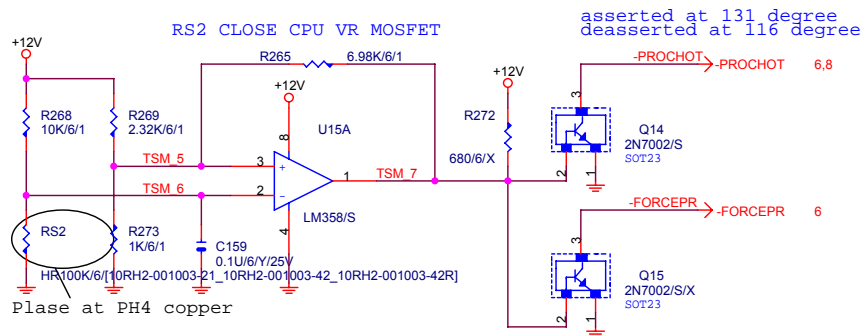
Case Open Circuits



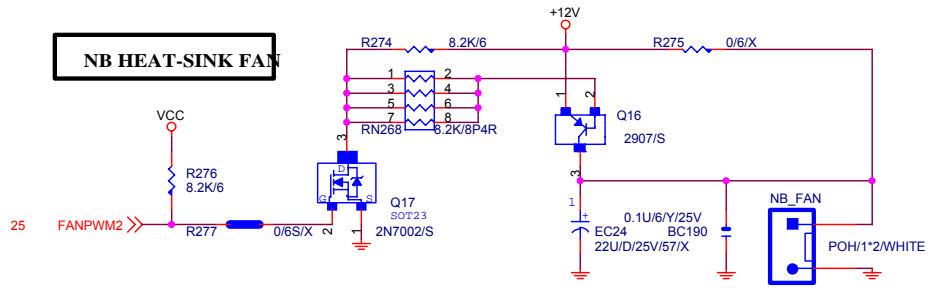
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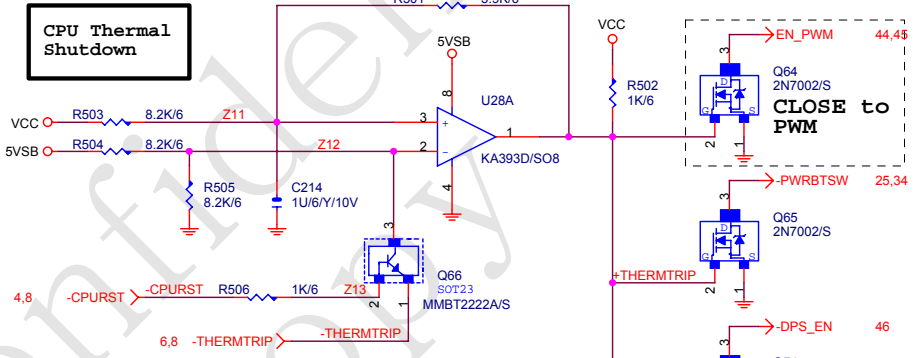
<b>Gigabyte Technology</b>		
Title		
<b>HARDWARE MONITOR</b>		
Size B	Document Number	Rev
	<b>8N-SLI Royal</b>	<b>1.02</b>
Date:	Thursday, May 19, 2005	Sheet 26 of 46



**NB HEAT-SINK FAN**



**CPU Thermal Shutdown**



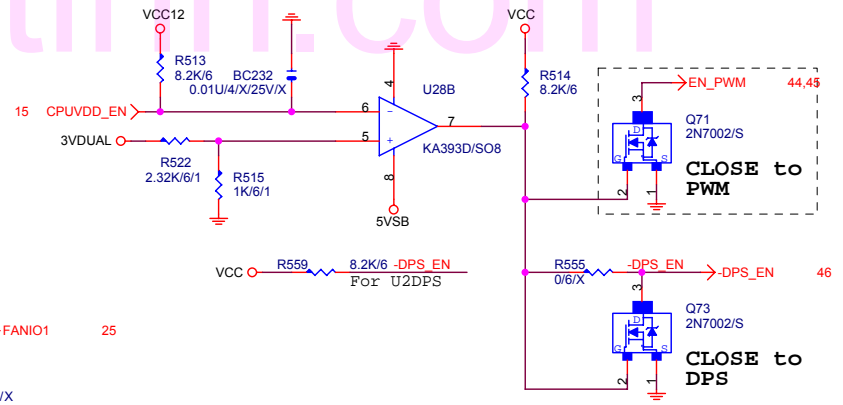
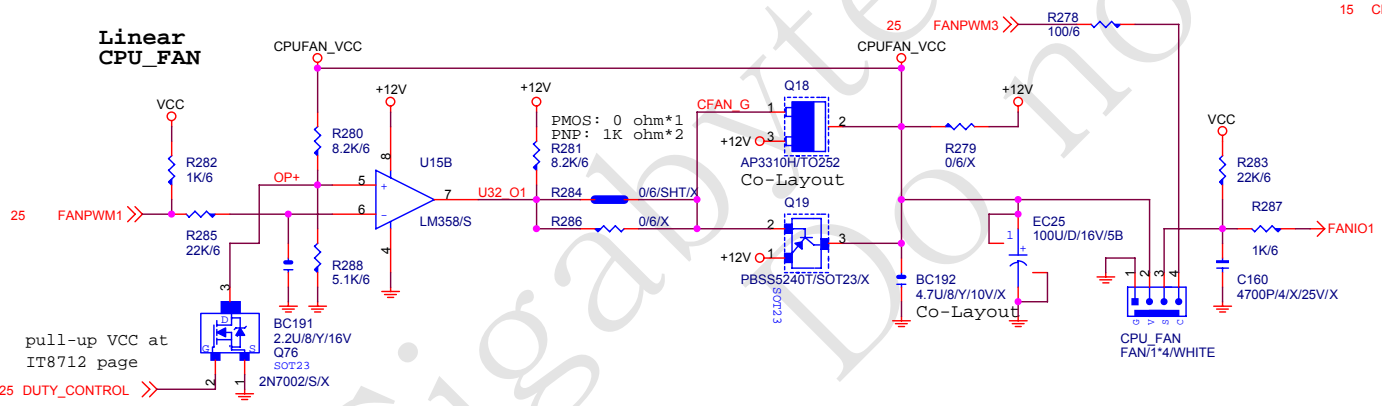
**Table1: 3 pin FAN**

Off Limit	-10 degree	0 PWM
Start Limit	20 degree	35 PWM
Full Limit	65 degree	127 PWM
Slope	2 PWM/degree	

**Table2: 4 pin FAN**

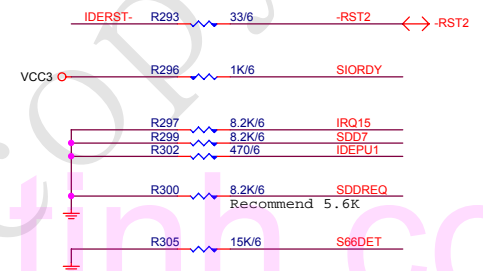
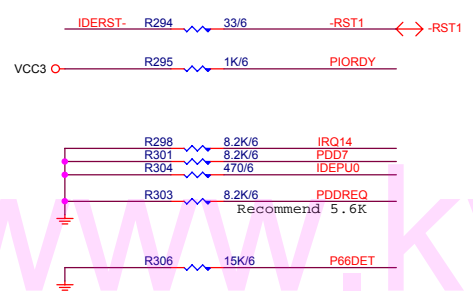
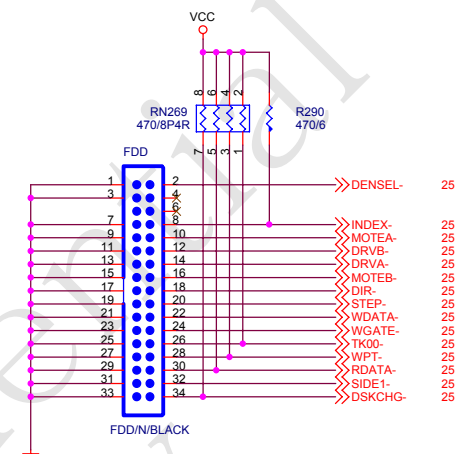
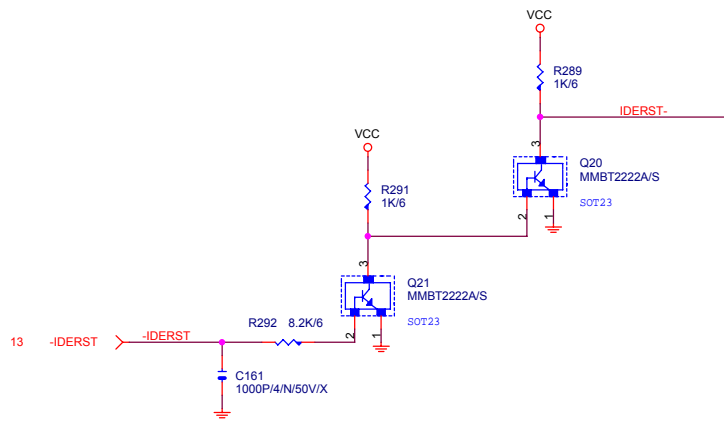
Off Limit	-10 degree	0 PWM
Start Limit	20 degree	35 PWM
Full Limit	65 degree	127 PWM
Slope	2 PWM/degree	

**Linear CPU\_FAN**

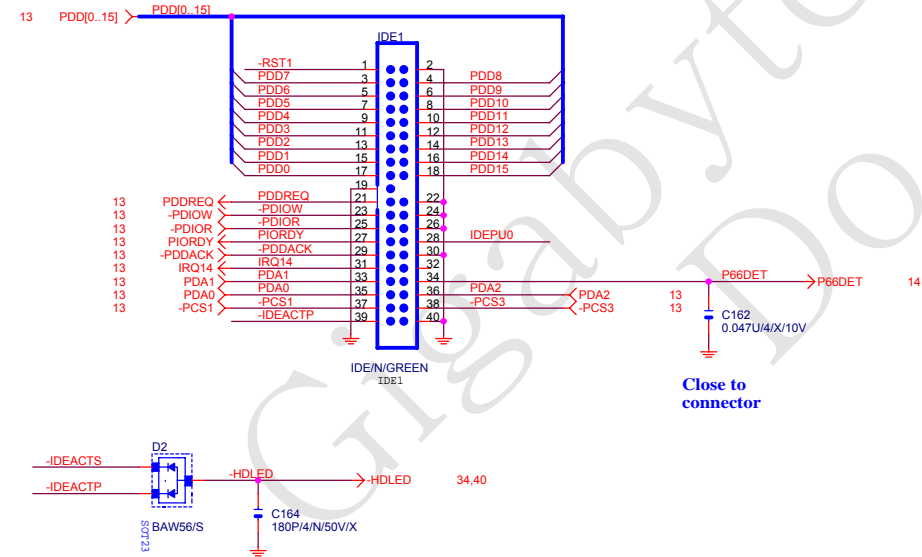


**Gigabyte Technology**

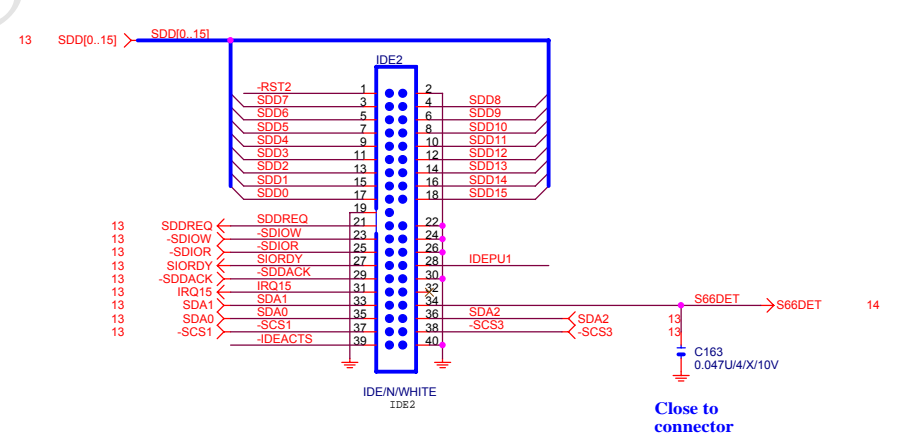
Title		<b>FAN CONTROL</b>	
Size	Document Number	<b>8N-SLI Royal</b>	
Date	Thursday, May 19, 2005	Sheet	27 of 46



**PRIMARY IDE CONNECTOR**

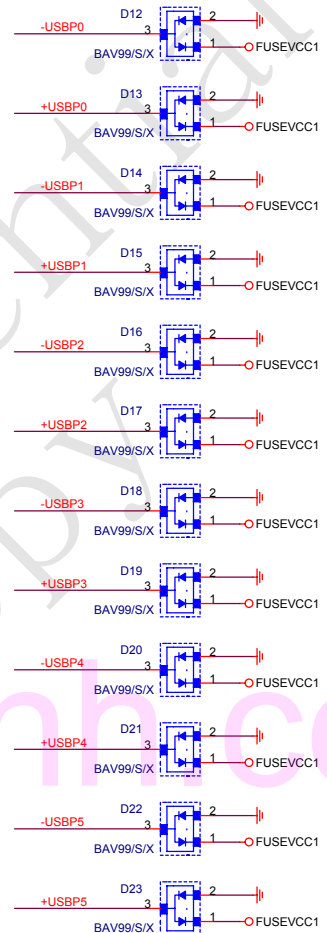
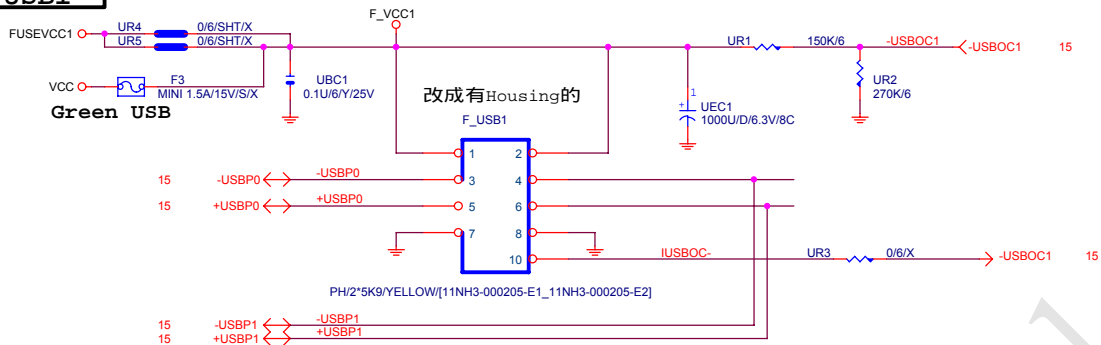


**SECONDARY IDE CONNECTOR**

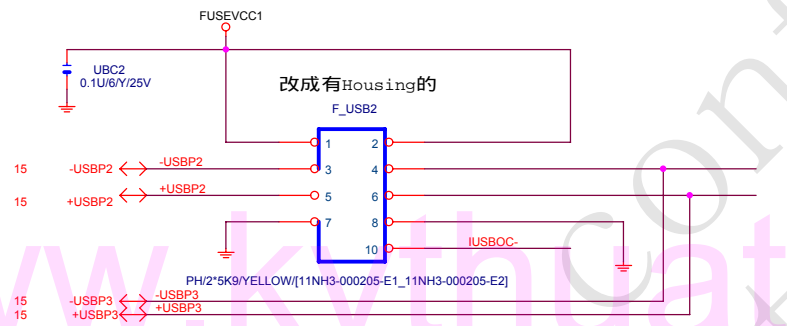


<b>Gigabyte Technology</b>		
<b>IDE CONNECTOR</b>		
Title	Document Number	Rev
	<b>8N-SLI Royal</b>	<b>1.02</b>
Date:	Sheet 28 of 46	

### FRONT SIDE USB1

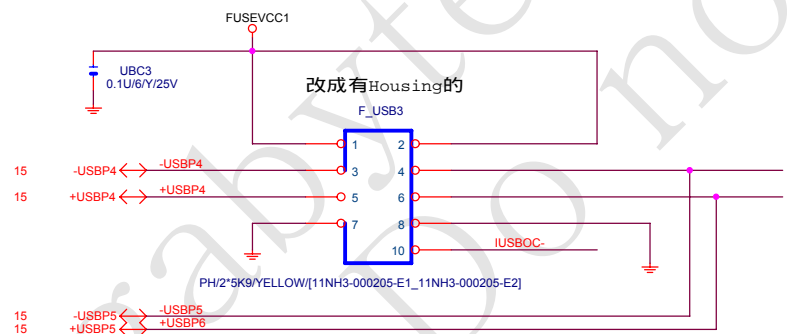


### FRONT SIDE USB2



For ESD issue.

### FRONT SIDE USB3

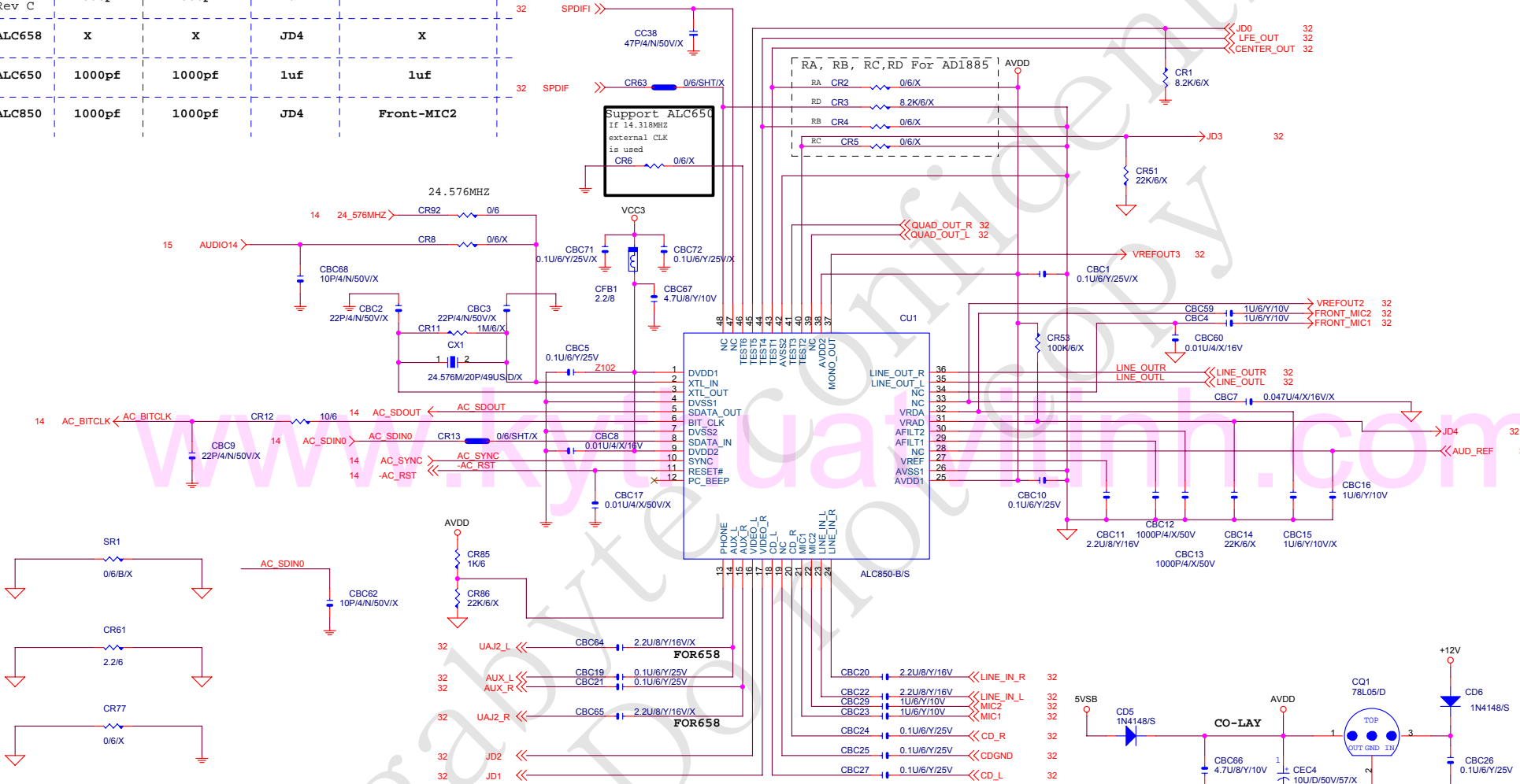


<b>Gigabyte Technology</b>			
Title			
<b>FRONT USB CONNECTOR</b>			
Size	Document Number	<b>8N-SLI Royal</b>	
B		Rev	1.02
Date:	Thursday, May 19, 2005	Sheet	29 of 46



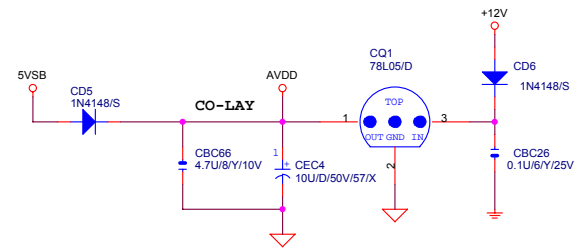
## Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pF	1000pF	1uF	Front-MIC2
ALC655 Rev C	1000pF	1000pF	1uF	X
ALC658	X	X	JD4	X
ALC650	1000pF	1000pF	1uF	1uF
ALC850	1000pF	1000pF	JD4	Front-MIC2

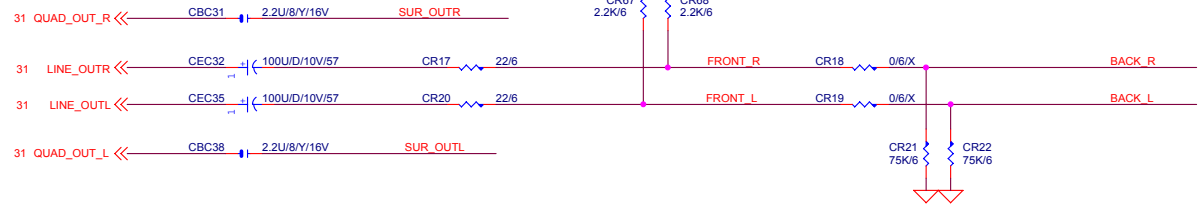


## Arrangement of Jack detection Pin:

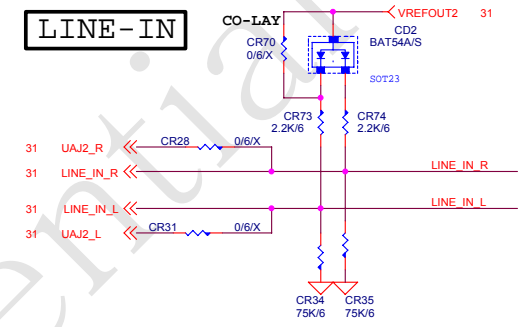
	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT External pull high is needed	for LINE-IN External pull high is needed	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out



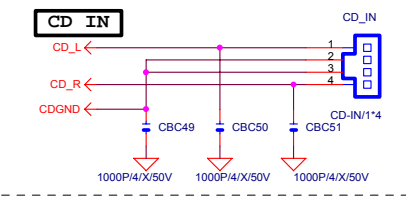
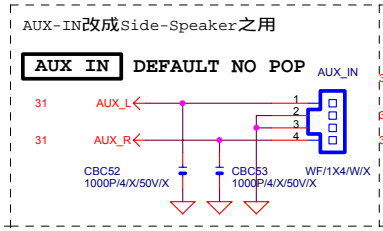
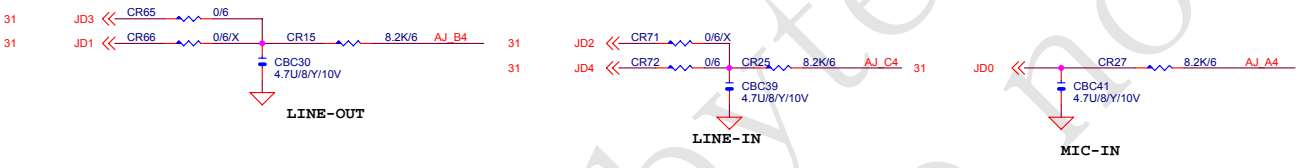
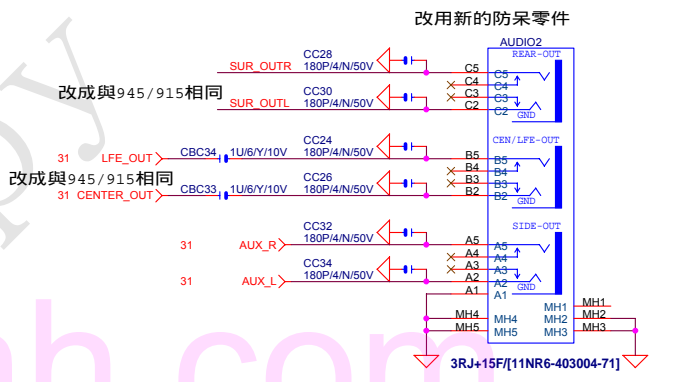
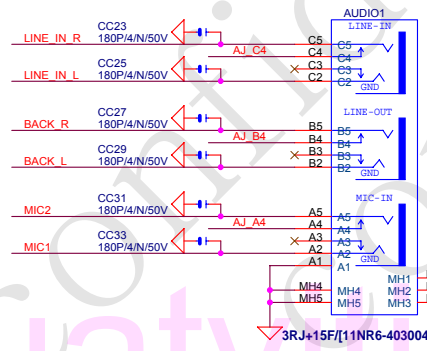
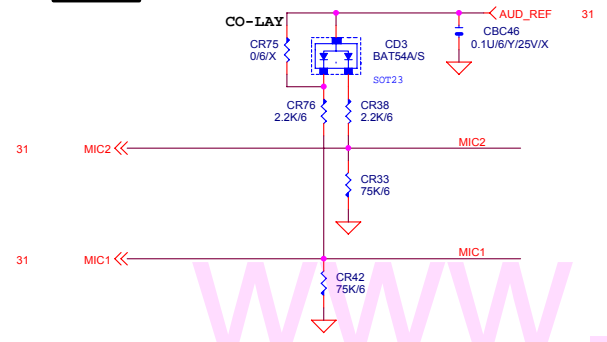
**LINE OUT**



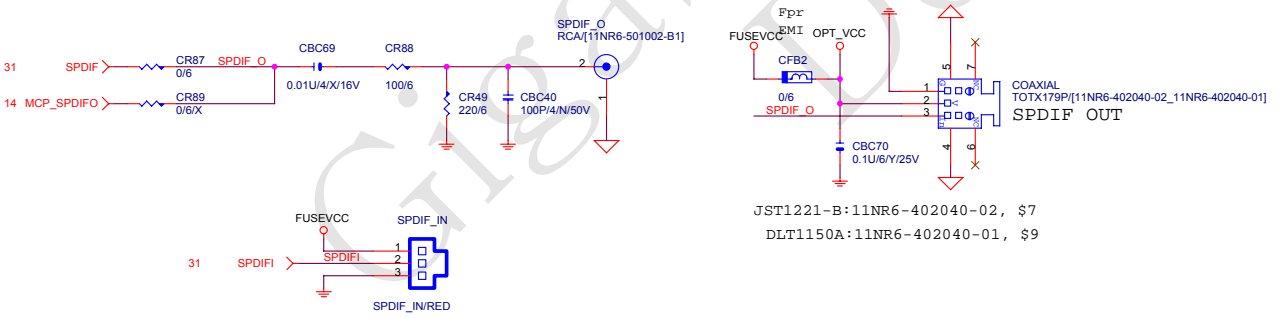
**LINE-IN**



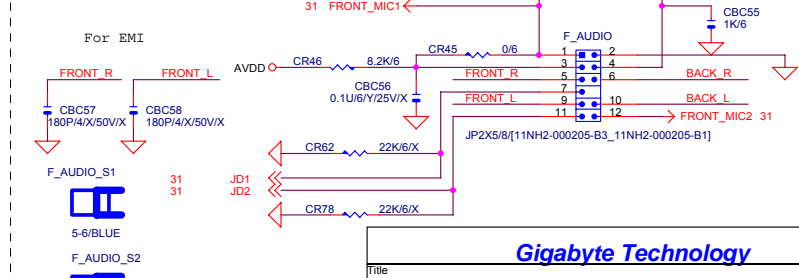
**MIC**



**SPDIF**



**INTEL FRONT AUDIO**

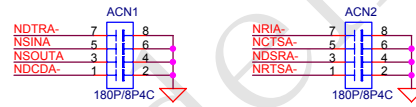
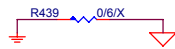
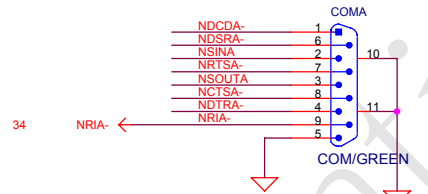
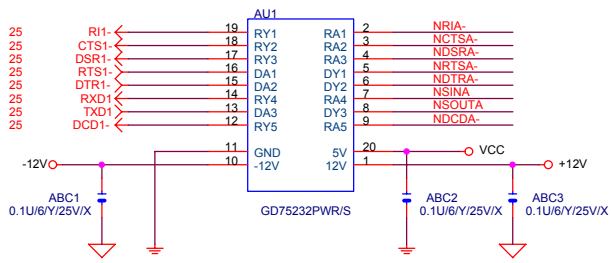


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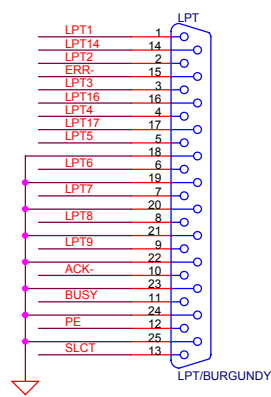
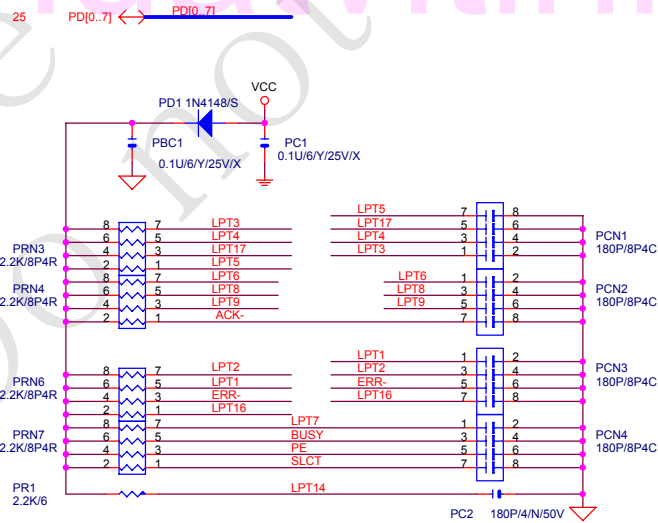
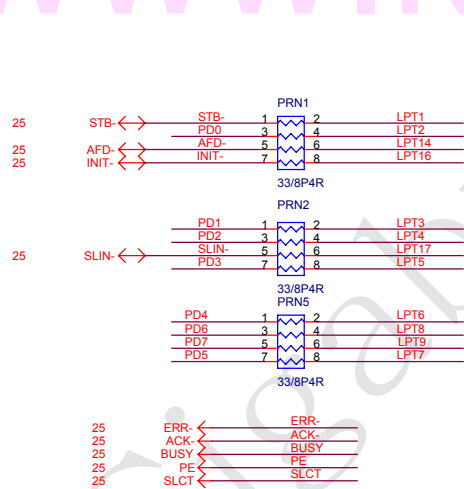
**AUDIO OUTPUT**

Title	Document Number	Rev
	<b>8N-SLI Royal</b>	<b>1.02</b>
Date: Thursday, May 19, 2005	Sheet	32 of 46

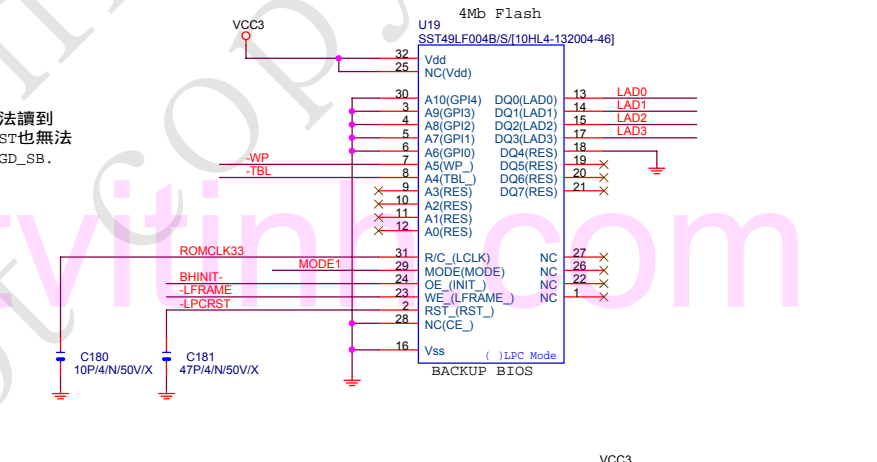
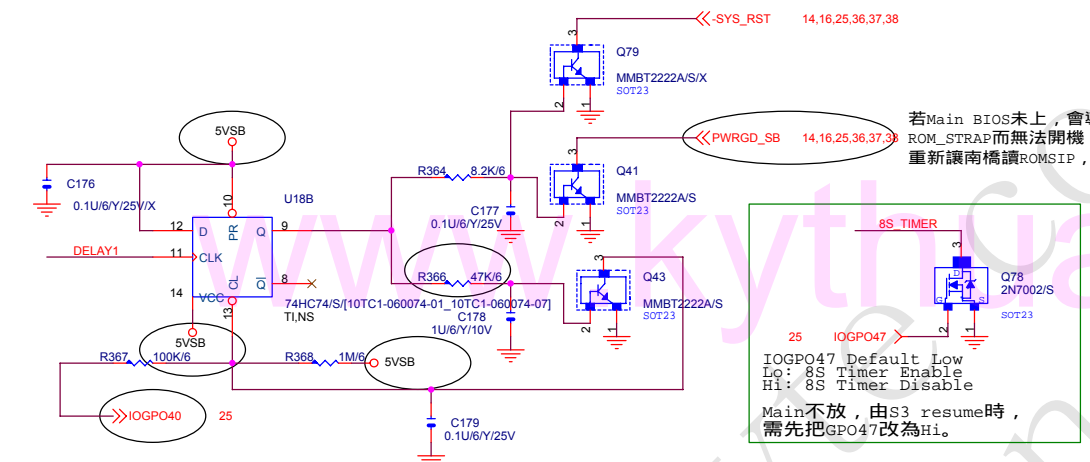
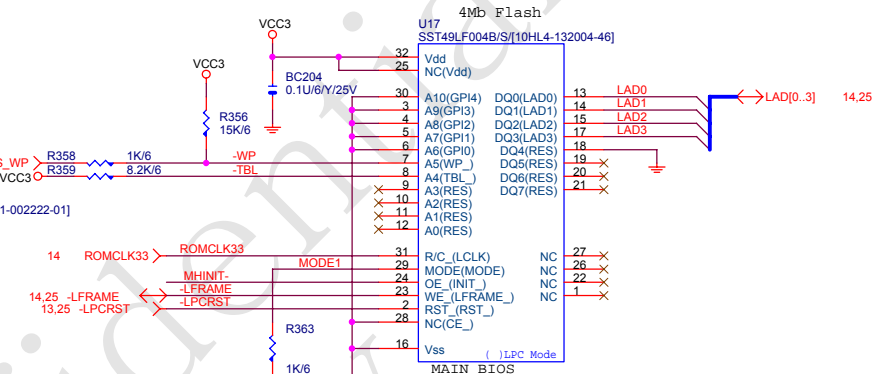
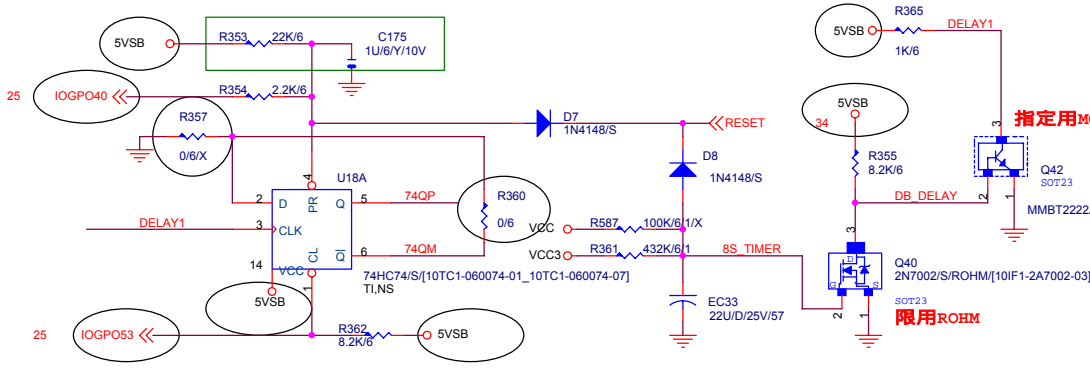
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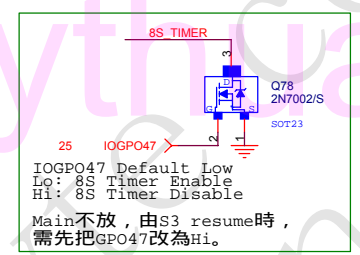
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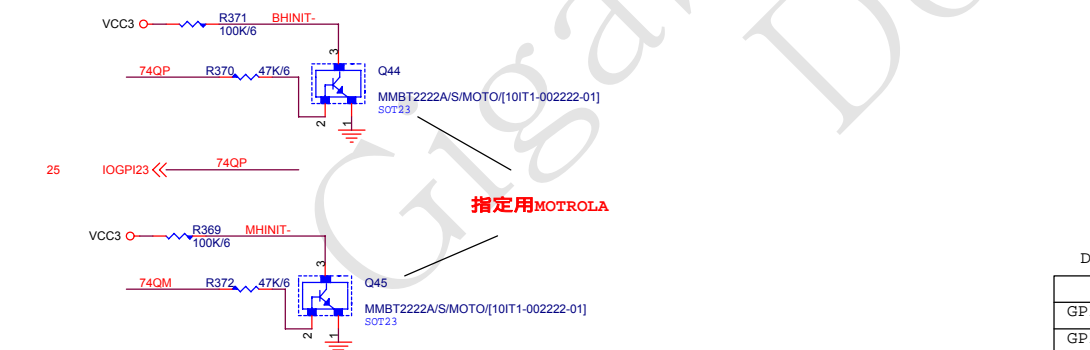


若Main BIOS未上，會導致開機無法讀到ROM\_STRAP而無法開機，拉-SYS\_RST也無法重新讓南橋讀ROMSIP，故改用PWRGD\_SB。



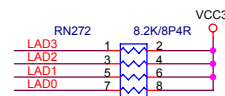
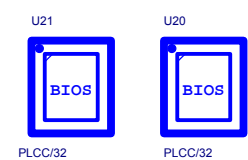
IOGPO47 Default Low  
Lo: 8S Timer Enable  
Hi: 8S Timer Disable  
Main不放，由S3 resume時，需先把GPO47改為Hi。

每次Power on先把GPO40 & GPO53 改為Hi。  
如果開機後發現被H/W切到Backup BIOS，則由S3 resume時需先把GPO47改為Hi。



DUAL BIOS SELECTION

	Main	Backup
GPI040	0	1
GPI053	1	0



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**DUAL BIOS**

Title: **8N-SLI Royal**

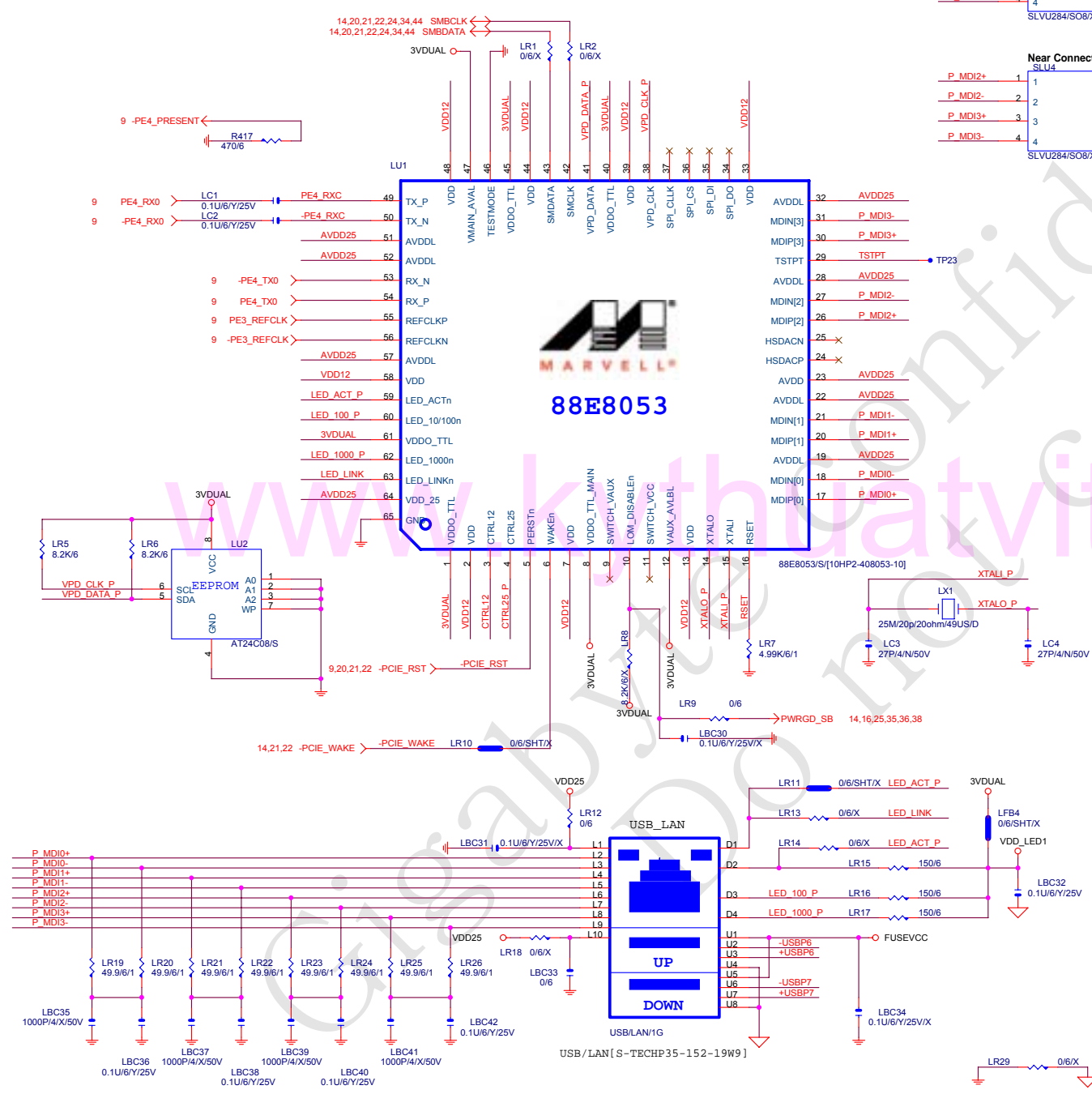
Size B: Document Number: **8N-SLI Royal** Rev: **1.02**

Date: Thursday, May 19, 2005 Sheet: 35 of 46

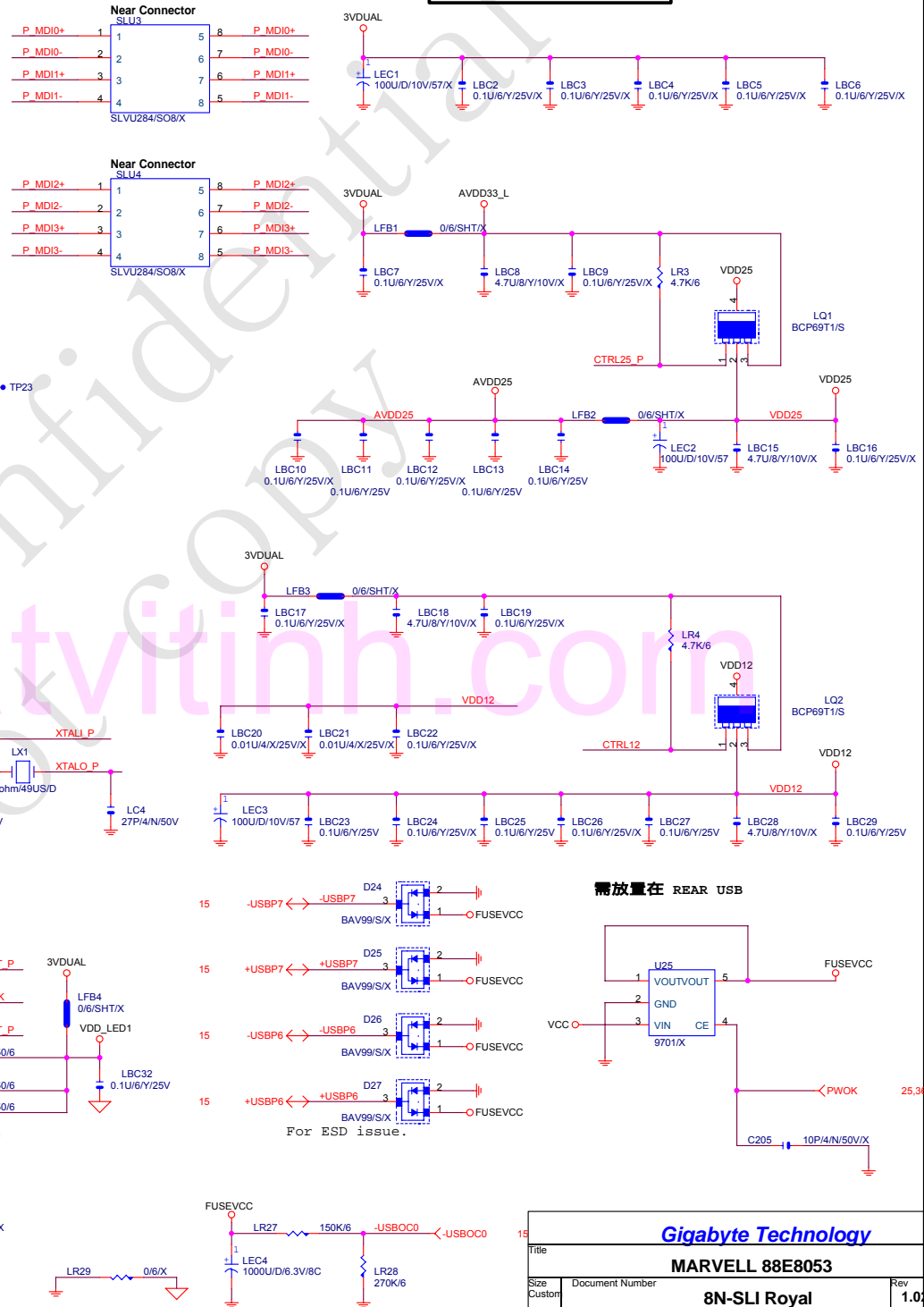


# Layout Check 注意事項

1. LU1 PIN65 需下內層GND,打12VIA
2. 3VDUAL, VCC3, VDD15\_L, AVDD25\_L 至少走20mil寬,並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線,TRACE 愈短愈好,線寬1.2mil
4. MDI正負0~3,TRACE 8:7:8, 每對之間保持 40mil



POWER DECOUPLING CAP.



需放置在 REAR USB

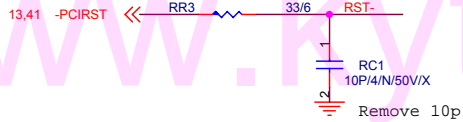
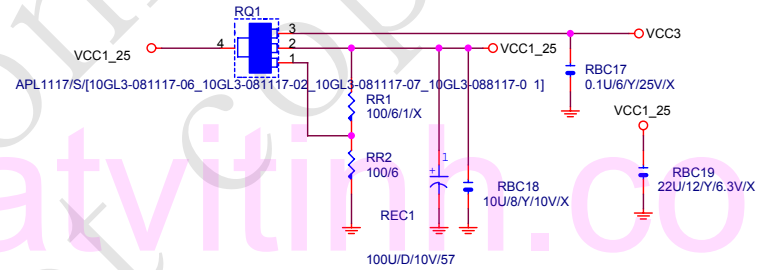
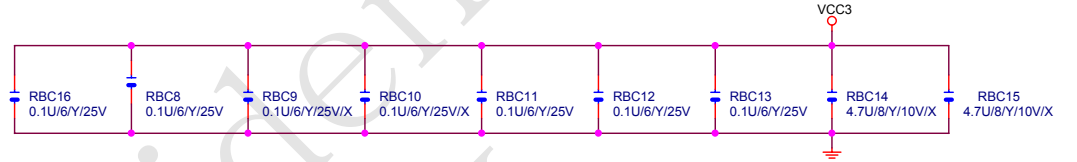
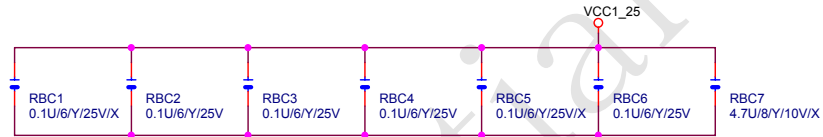
<b>Gigabyte Technology</b>		
<b>MARVELL 88E8053</b>		
Size Custom	Document Number	Rev
	<b>8N-SLI Royal</b>	<b>1.02</b>
Date:	Thursday, May 19, 2005	Sheet 37 of 46



A\_D[0..31] >> A\_D[0..31] 13,24,41

RU1A			
A_D0	50	BAD0	RESTN
A_D1	49	BAD1	
A_D2	48	BAD2	CLK
A_D3	46	BAD3	
A_D4	45	BAD4	INTA
A_D5	43	BAD5	
A_D6	42	BAD6	
A_D7	41	BAD7	PCIGNTN
A_D8	39	BAD8	PCIREQN
A_D9	38	BAD9	
A_D10	37	BAD10	IDSEL
A_D11	35	BAD11	
A_D12	34	BAD12	BFRAMEN
A_D13	33	BAD13	
A_D14	32	BAD14	
A_D15	30	BAD15	BIRDYN
A_D16	16	BAD16	BTRDYN
A_D17	15	BAD17	
A_D18	13	BAD18	BDEVSELN
A_D19	12	BAD19	
A_D20	10	BAD20	BSTOPN
A_D21	9	BAD21	PAR
A_D22	7	BAD22	
A_D23	6	BAD23	SERRN
A_D24	3	BAD24	PERRN
A_D25	2	BAD25	
A_D26	1	BAD26	
A_D27	128	BAD27	BCBE0N
A_D28	127	BAD28	BCBE1N
A_D29	125	BAD29	BCBE2N
A_D30	123	BAD30	BCBE3N
A_D31	122	BAD31	

PDC20779(10HP2-810779-10)

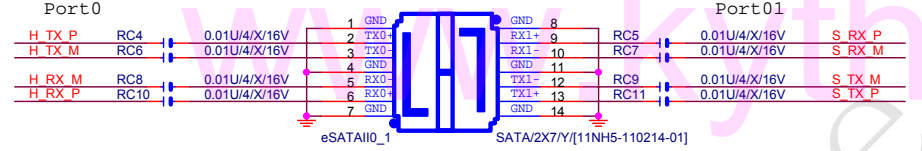
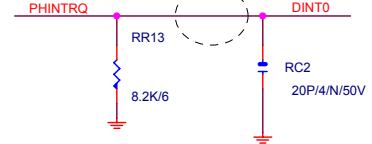
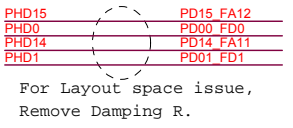
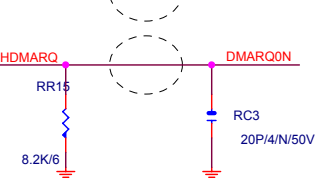
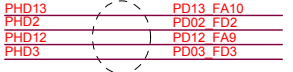
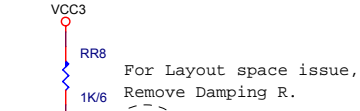
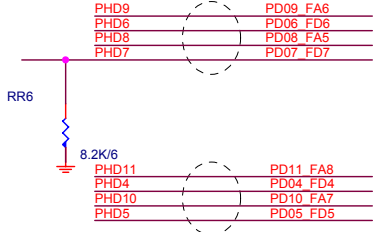
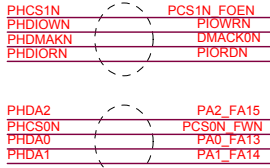
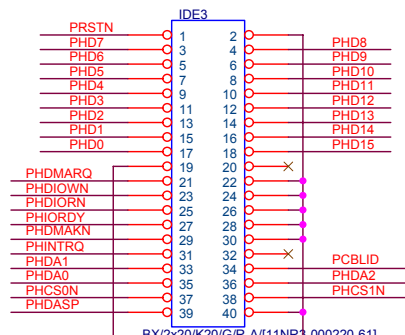


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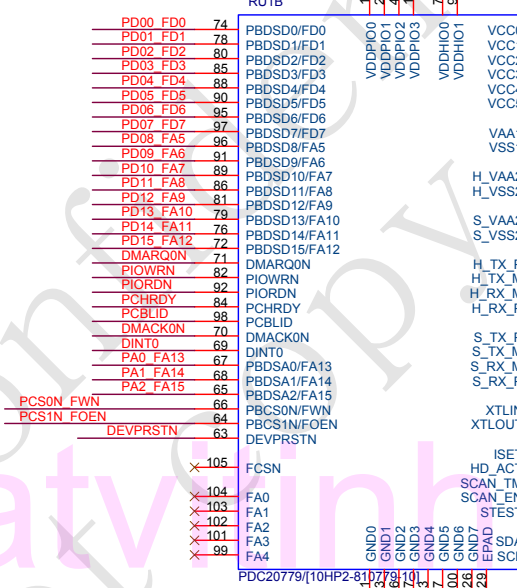
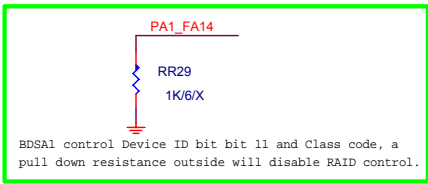
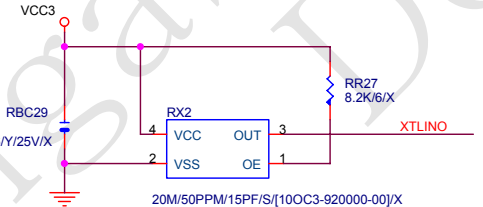
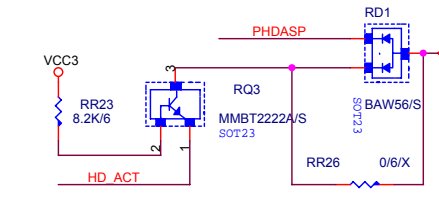
Gigabyte Technology

Title		PDC20779-PCI, POWER	
Size	Document Number	8N-SLI Royal	
Date:	Thursday, May 19, 2005	Sheet	39 of 46

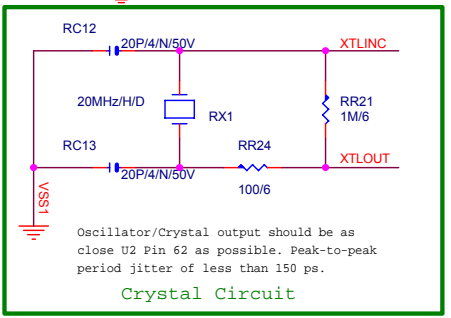
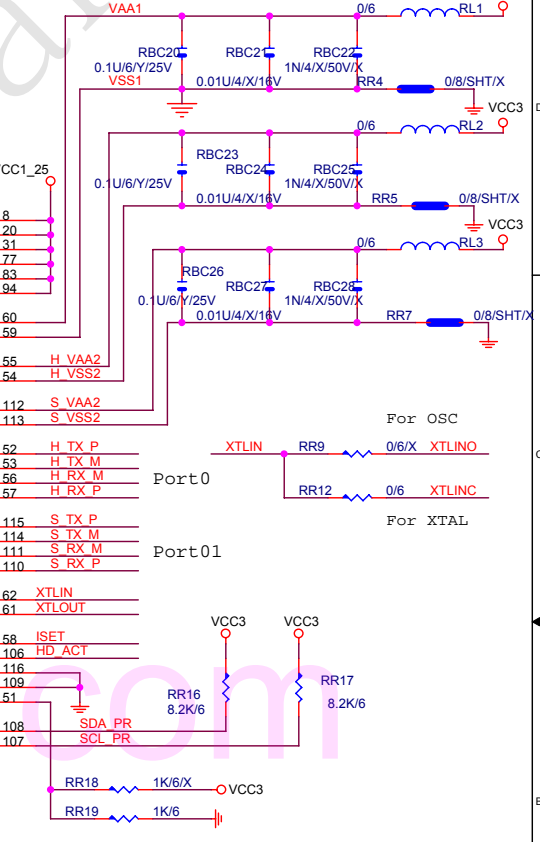
Rev 1.02



需個別標示出何者為eSATA0, eSATA1



Bead should be a "wide band choke" where the frequency is attenuated by 30dB or more between 1-650MHz. Noise levels on these pin should be less than 100mV.

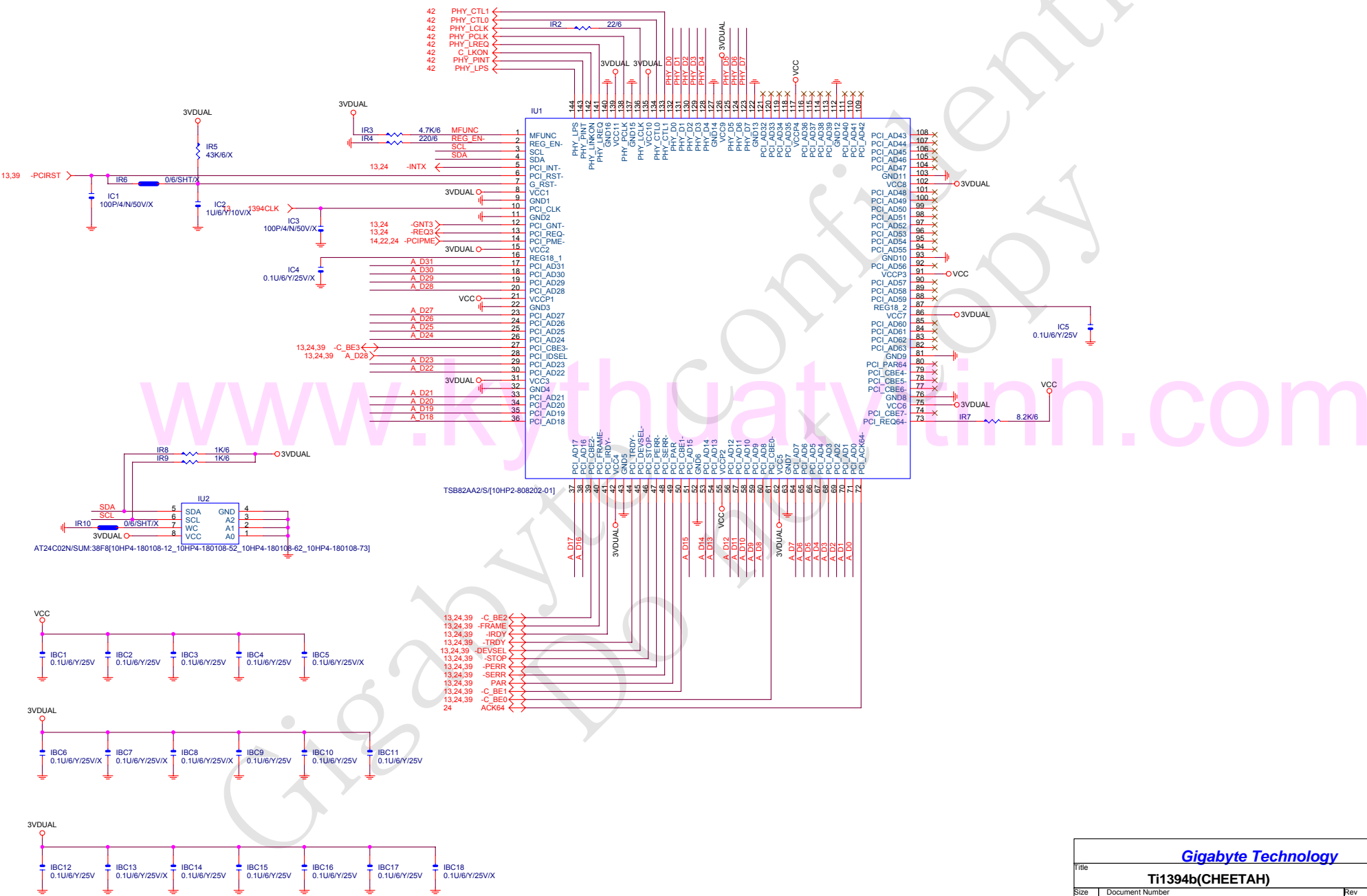


Oscillator/Crystal output should be as close U2 Pin 62 as possible. Peak-to-peak period jitter of less than 150 ps.

Gigabyte Technology		
Title: PDC20779 - SATA,IDE AND FLASH INTERFACE		
Size B	Document Number: 8N-SLI Royal	Rev: 1.02
Date: Thursday, May 19, 2005	Sheet: 40	of 46

13.24.39 A\_D0[.31] ← A\_D0[.31]

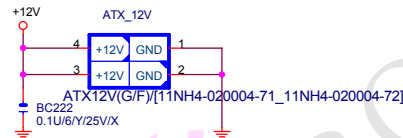
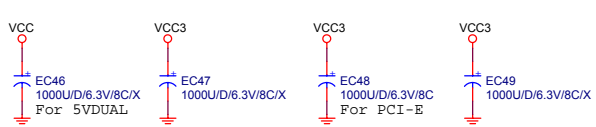
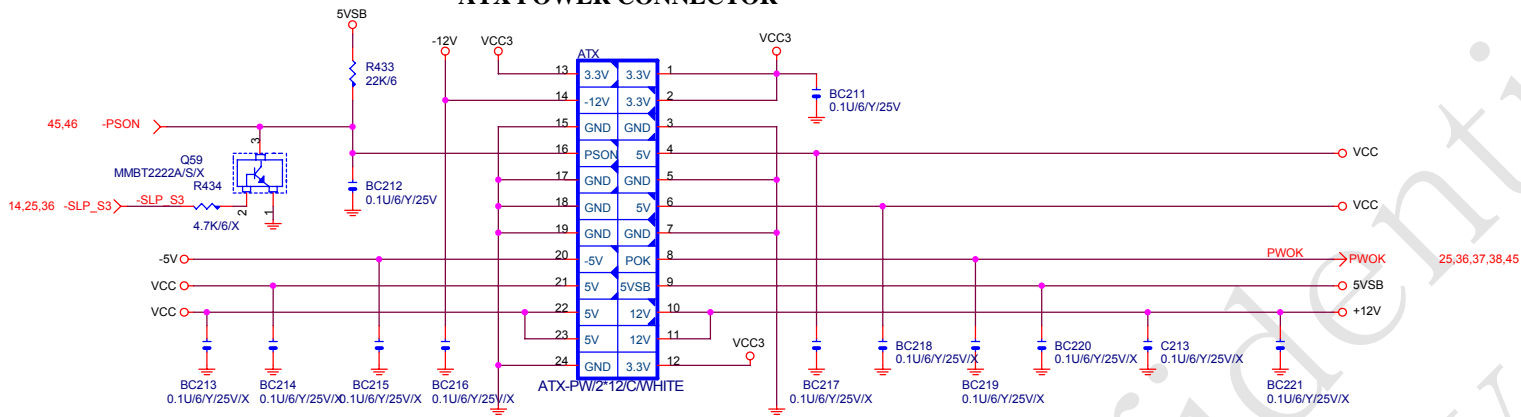
42 PHY\_D0[.7] ← PHY\_D0[.7]



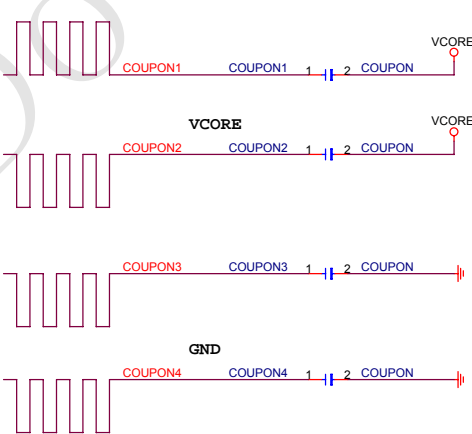
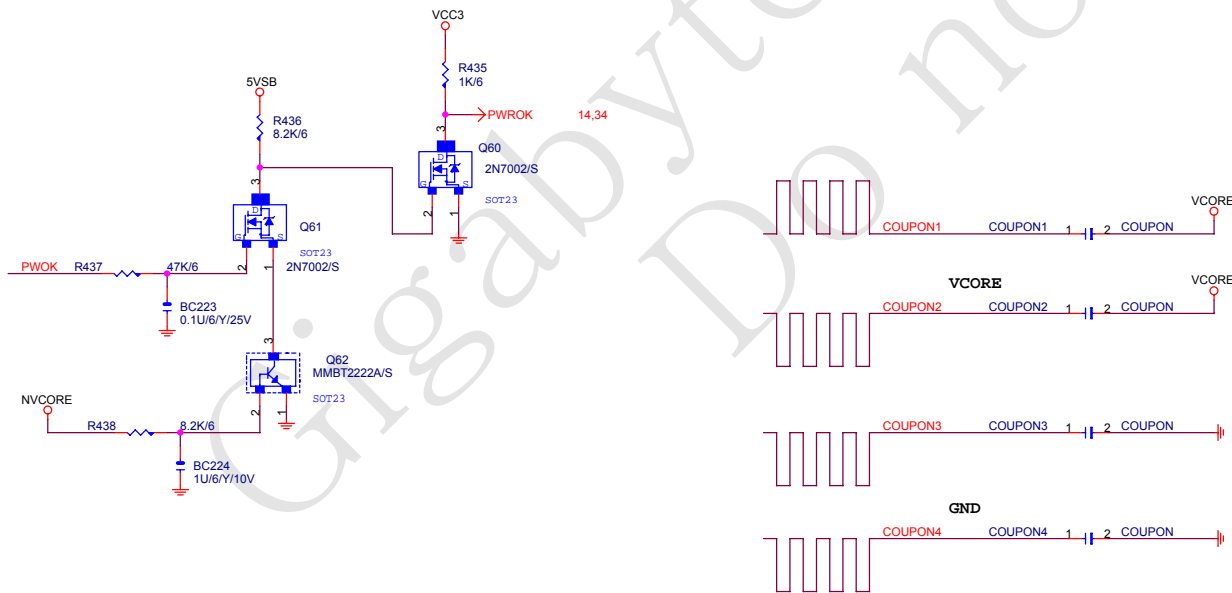
<b>Gigabyte Technology</b>		
<b>Ti1394b(CHEETAH)</b>		
Size Custom	Document Number <b>8N-SLI Royal</b>	Rev 1.02
Date Thursday, May 19, 2005	Sheet 41	of 46



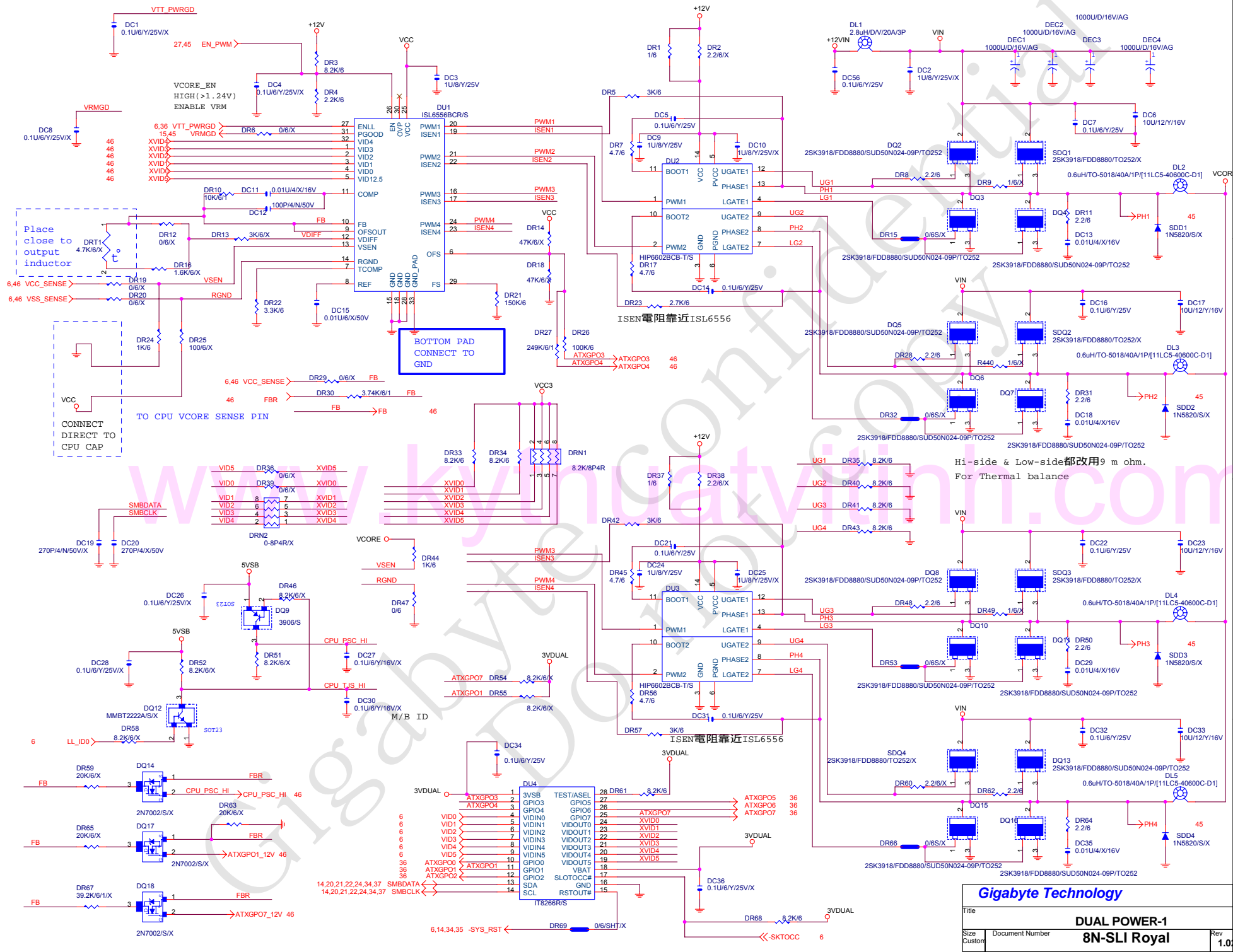
# ATX POWER CONNECTOR



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Size B	Document Number <b>8N-SLI Royal</b>
Date: Thursday, May 19, 2005	Rev <b>1.02</b>
Sheet 43 of 46	



<b>Gigabyte Technology</b>			
<b>DUAL POWER-1</b>			
Title	Document Number		
Size	8N-SLI Royal		
Custom	Rev 1.02		
Date	Thursday, May 19, 2005	Sheet	44 of 46



DUAL POWER

