Model Name: 8I915P Dual Graphic
Rev:1.02

SHEET	TITLE
01	COVER SHEET
02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	P4_LGA775_A
05	P4_LGA775_B
06	P4_LGA775_C
07	P4_LGA775_D
08	VCORE POWER
09	GMCH-GRANTSDALE_HOST
10	GMCH-GARNTSDALE_DDR
11	GMCH-GRANTSDALE_PCI E, DMI
12	GMCH-GRANTSDALE_INT VGA
13	GMCH-GRANTSDALE_GND
14	GMCH-GRANTSDALE_PWR
15	DDR CHANNEL A
16	DDR CHANNEL B
17	DDR TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH6 PCI, USB, DMI, LAN
20	ICH6 IDE, GPIO, SATA, CTRL
21	ICH6 PWR, GND
22	CLK_GEN/CK410M

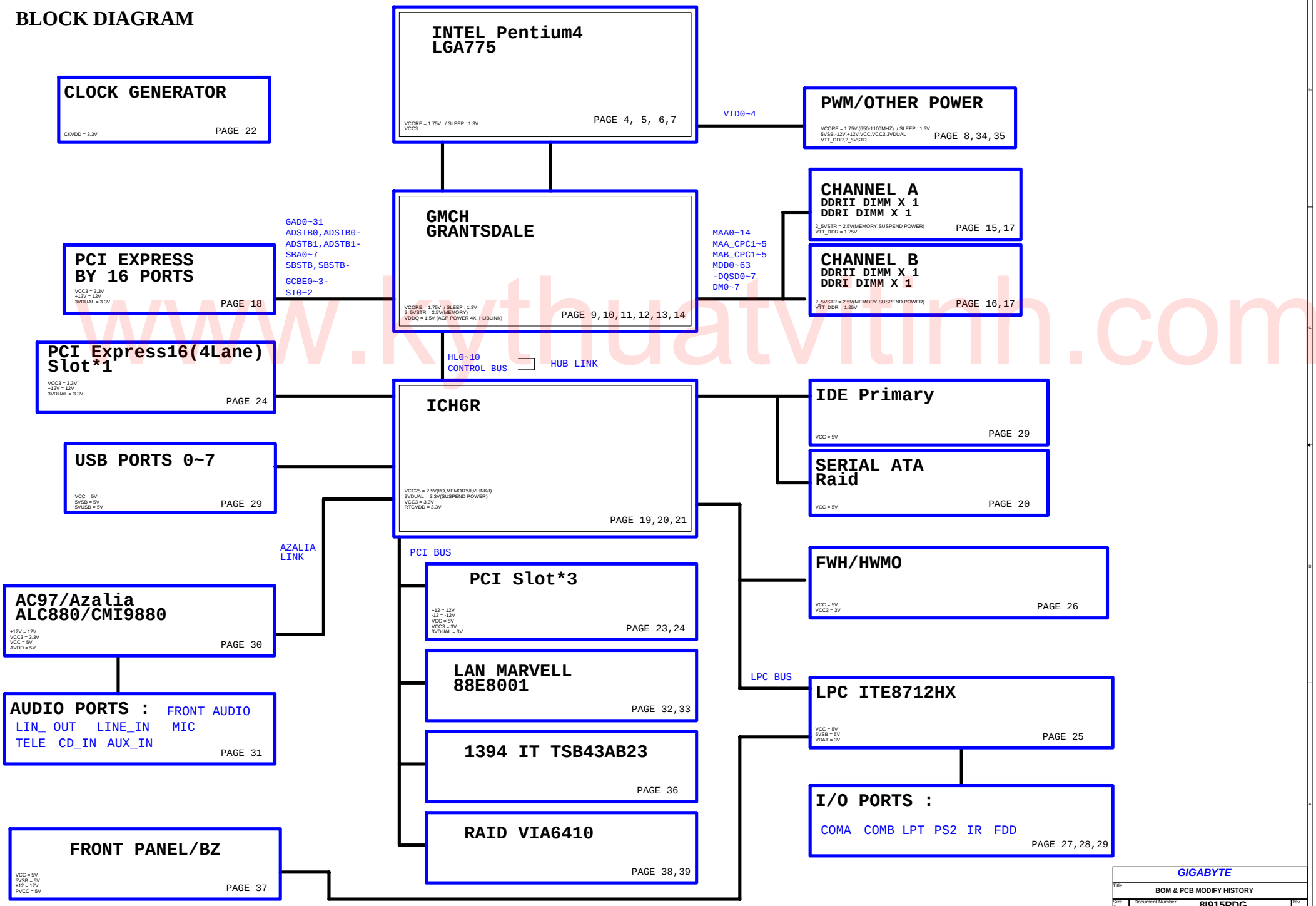
SHEET	TITLE
23	PCI SLOT
24	PCIE X1 /PCIE SLI SLOT
25	ITE8712 LPC I/O
26	HWMO/FAN
27	KB_MS/GAME
28	COM/LPT/FDD
29	(FRONT+REAR)USB/RING/IDE SATA LED
30	AZALIA CODEC ALC880/CMI9880
31	AUDIO JACK
32	MARVELL 88E8001
33	ATX,OTHERS POWER/DUAL BIOS
34	DISCRETE POWER
35	TI TSB43AB23 1394
36	FRONT PANEL
37	RAID VIA 6410
38	RAID IDE CONNECTOR
39	GPIO TABLE
40	GPIO/RESET TABLE

COMPONENT SIDE
1 oz. Copper)
OLDER SIDE
1 oz. Copper)

GIGABYTE

Size: Custom	Document Number	Title: Cover Sheet	Rev: 1.02
Date: Tuesday, January 04, 2005	Sheet 1 of 40	8I915PDG	

BLOCK DIAGRAM



GIGABYTE

Title	BOM & PCB MODIFY HISTORY	
Size: Custom	Document Number: 8I915PDG	Rev: 1.02
Date: Tuesday, January 04, 2005	Sheet 2 of 40	

Model Name: 8I915P Dual Graphic

Version: 1.02

Component value change history

2004/12/20

Data	Change Item	Reason
0.1 BOM 2004/11/19	First BOM release PCB 0.1	
1.0A BOM 2004/12/10	PCB 1.01 E-BOM release (Q SW)	
1.0B BOM 2004/12/16	PCB 1.01 P-BOM release (Q SW)	
1.0C BOM 2004/12/23	PCB 1.02 P-BOM release (DIP SW)	DIP SW MP
1.0D BOM 2005/01/05	R1147 2.2/6==>4.7/6	Dual BIOS issue

Circuit or PCB layout change for next version

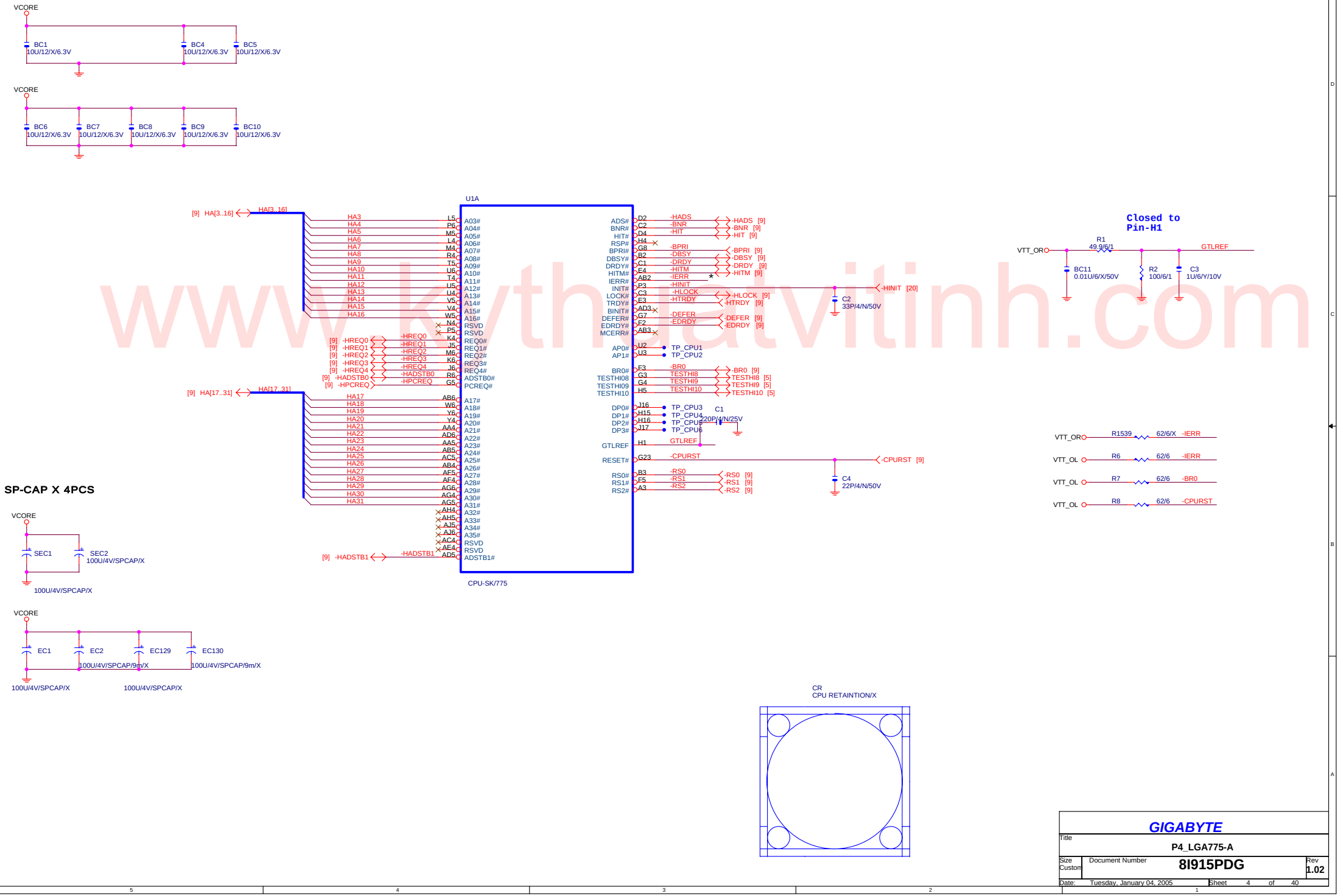
PAGE	Change Item	Reason

GIGABYTE

Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: 8I915PDG | Rev: 1.02

Date: Tuesday, January 04, 2005 | Sheet 3 of 40



GIGABYTE		
Title	P4_LGA775-A	
Size: Custom	Document Number: 8I915PDG	Rev: 1.02
Date: Tuesday, January 04, 2005	Sheet 4 of 40	

Note:

VCCA & VCOREPLL define doesn't same as old P4 design kit

Trace width doesn't less than 12 Mil

As close as possible to CPU socket

Place outside of CPU socket

Locate at ICH6 Side

U1C

CPU-SK/775

U1D

Title	P4_LGA775-B
Size	Custom
Document Number	8I915PDG
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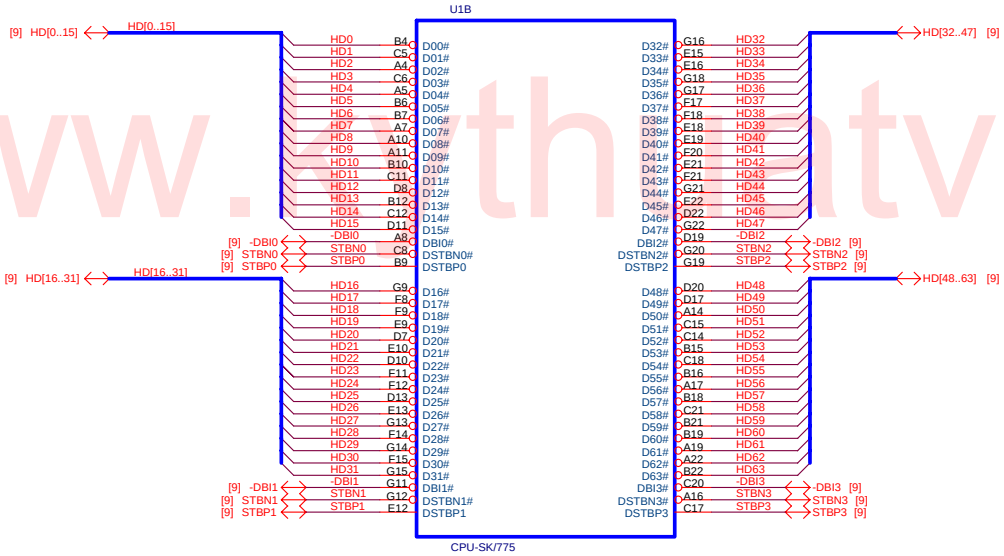
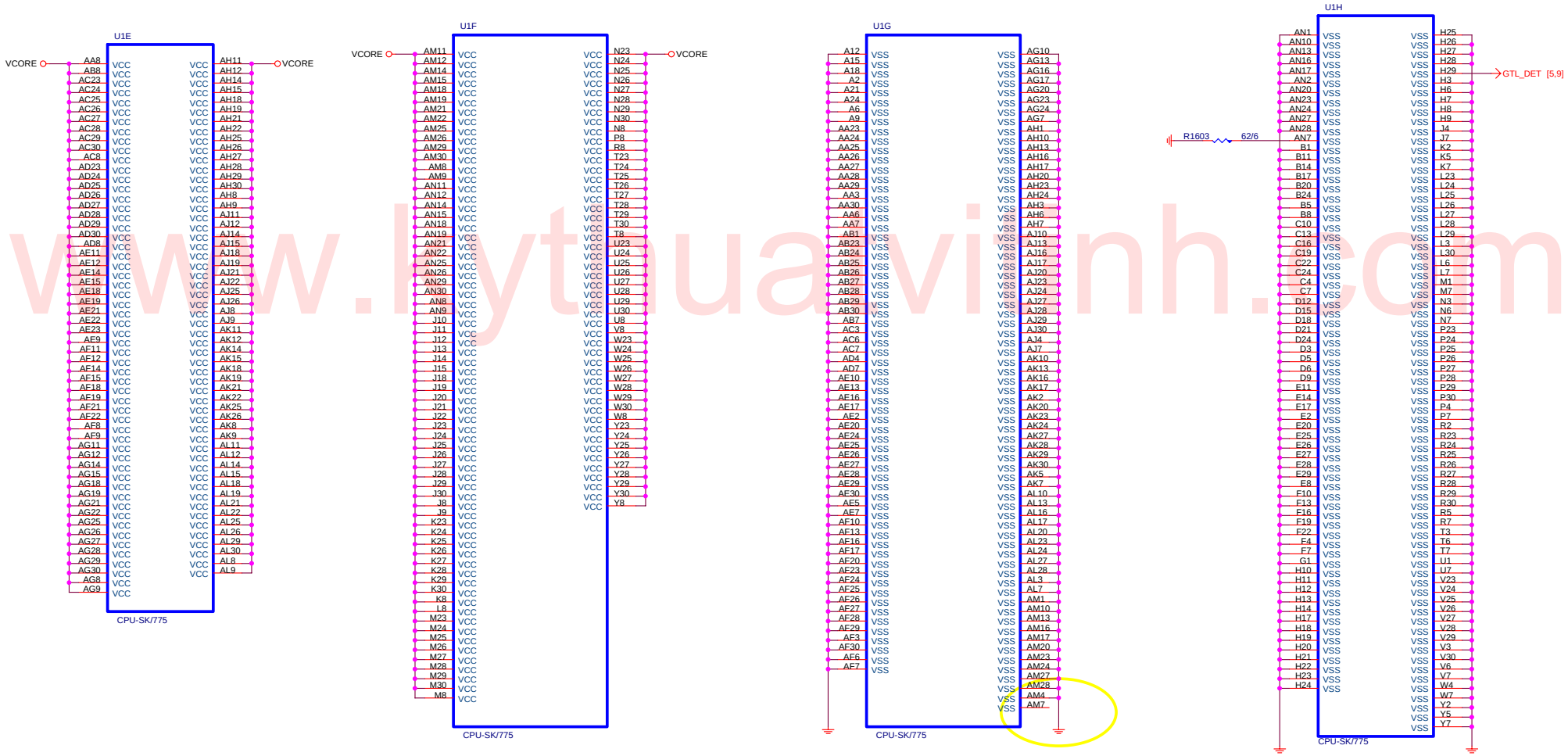
Date:	Tuesday, January 04, 2005
Sheet	5 of 40

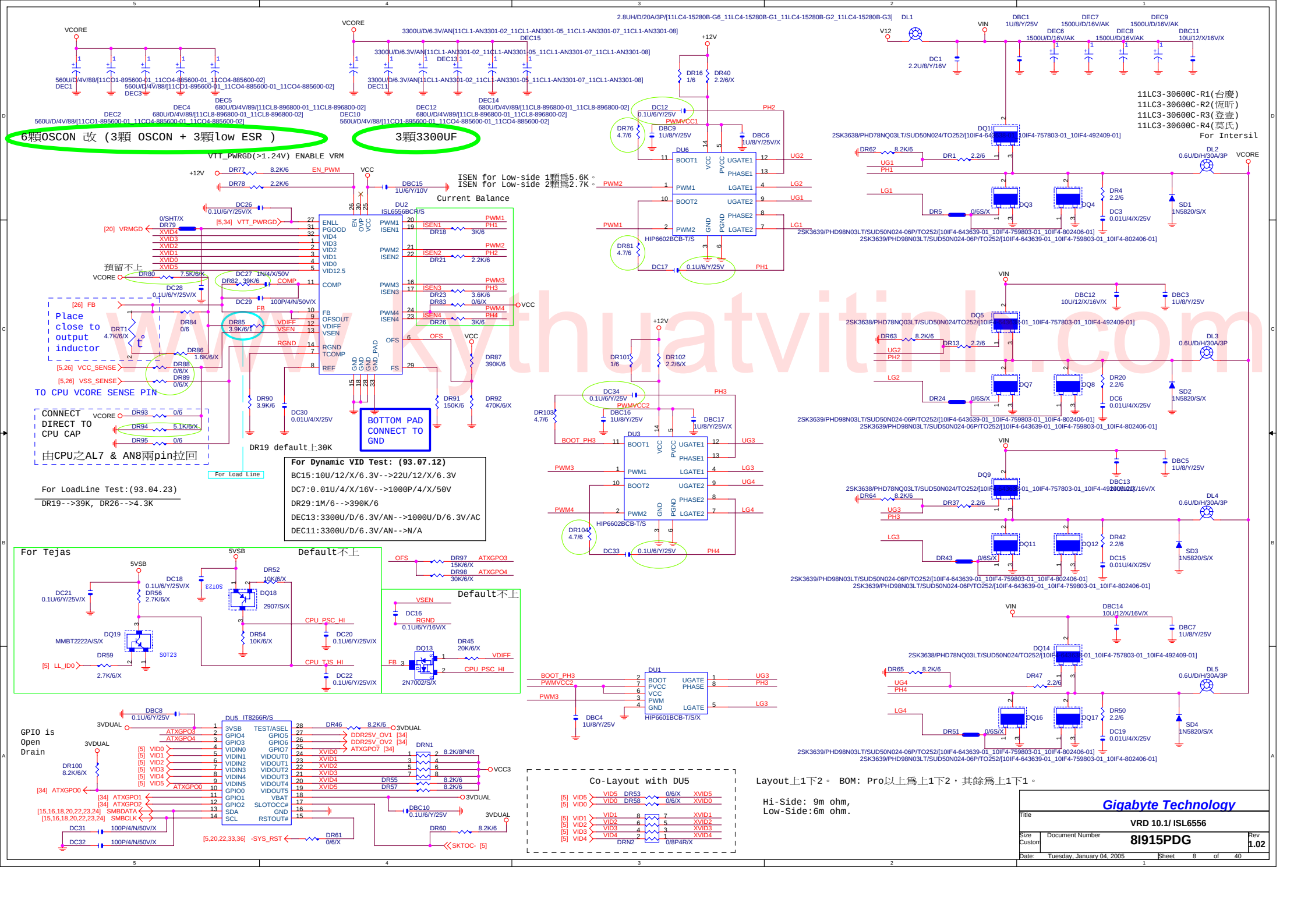


GIGABYTE

Title	P4_LGA775-C		
Size: Custom	Document Number: 8I915PDG		Rev: 1.02
Date: Tuesday, January 04, 2005	Sheet 6 of 40		



GIGABYTE			
Title	P4_LGA775-D		
Size: Custom	Document Number: 8I915PDG		Rev: 1.02
Date: Tuesday, January 04, 2005	Sheet 7 of 40		


6顆OSCON 改 (3顆 OSCON + 3顆low ESR)
3顆3300UF
VTT_PWRGD(>1.24V) ENABLE VRM
ISEN for Low-side 1顆爲5.6K。
ISEN for Low-side 2顆爲2.7K。
Current Balance
預留不上
Place close to output inductor
TO CPU VCORE SENSE PIN
CONNECT DIRECT TO CPU CAP
由CPU之AL7 & AN8兩pin拉回
For Load Line
BOTTOM PAD CONNECT TO GND
DR19 default上30K
For LoadLine Test:(93.04.23)
DR19-->39K, DR26-->4.3K
For Dynamic VID Test: (93.07.12)
BC15:10U/12/X/6.3V-->22U/12/X/6.3V
DC7:0.01U/4/X/16V-->1000P/4/X/50V
DR29:1M/6-->390K/6
DEC13:3300U/D/6.3V/AN-->1000U/D/6.3V/AC
DEC11:3300U/D/6.3V/AN-->N/A
For Tejas
Default不上
Default不上
GPIO is Open Drain
Co-Layout with DU5
Layout上1下2。 BOM: Pro以上爲上1下2，其餘爲上1下1。
Hi-Side: 9m ohm,
Low-Side:6m ohm.
11LC3-30600C-R1(台慶)
11LC3-30600C-R2(恆昕)
11LC3-30600C-R3(登壹)
11LC3-30600C-R4(莫氏)
For Intersil
Gigabyte Technology
VRD 10.1/ ISL6556
8I915PDG
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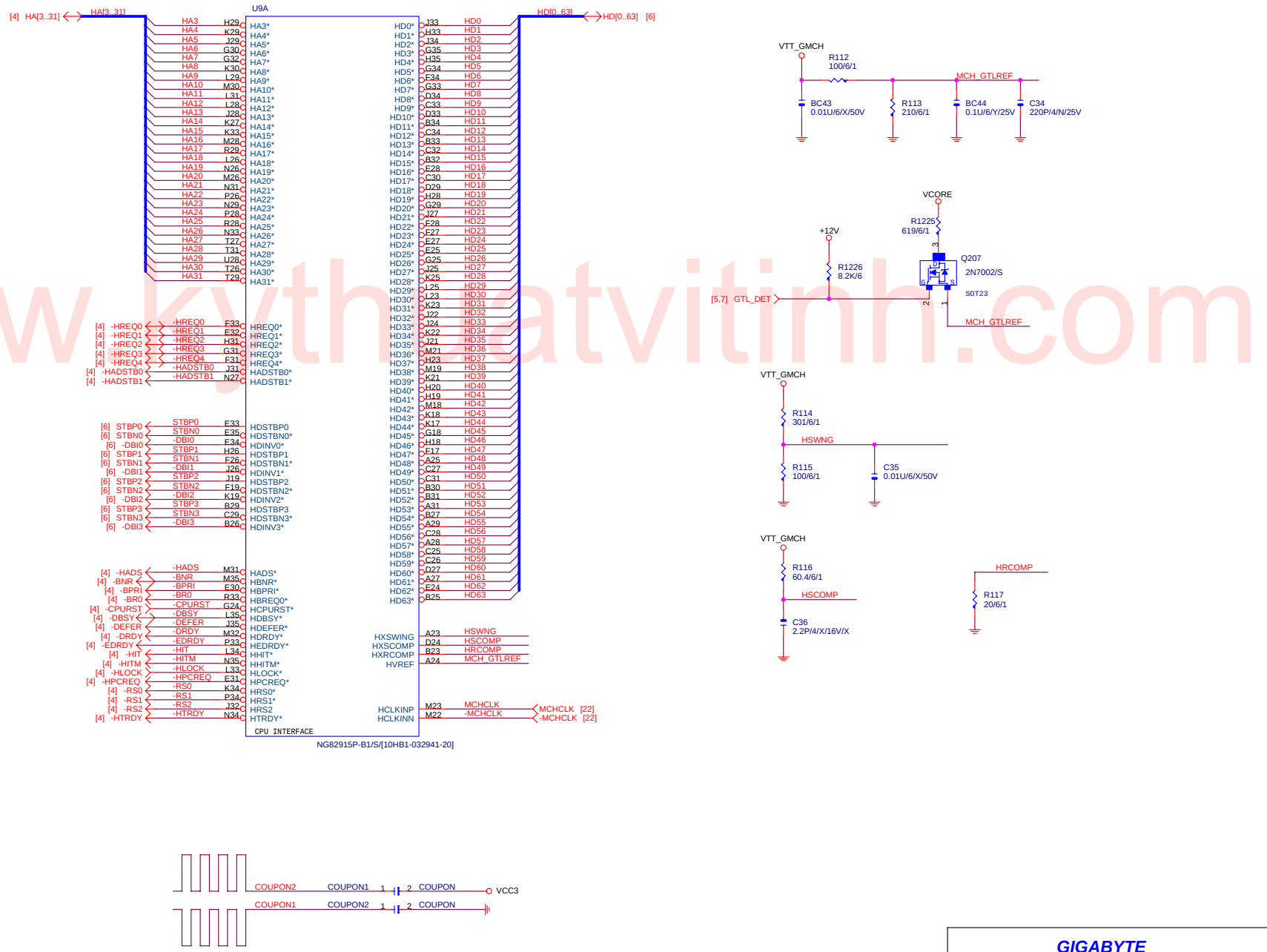
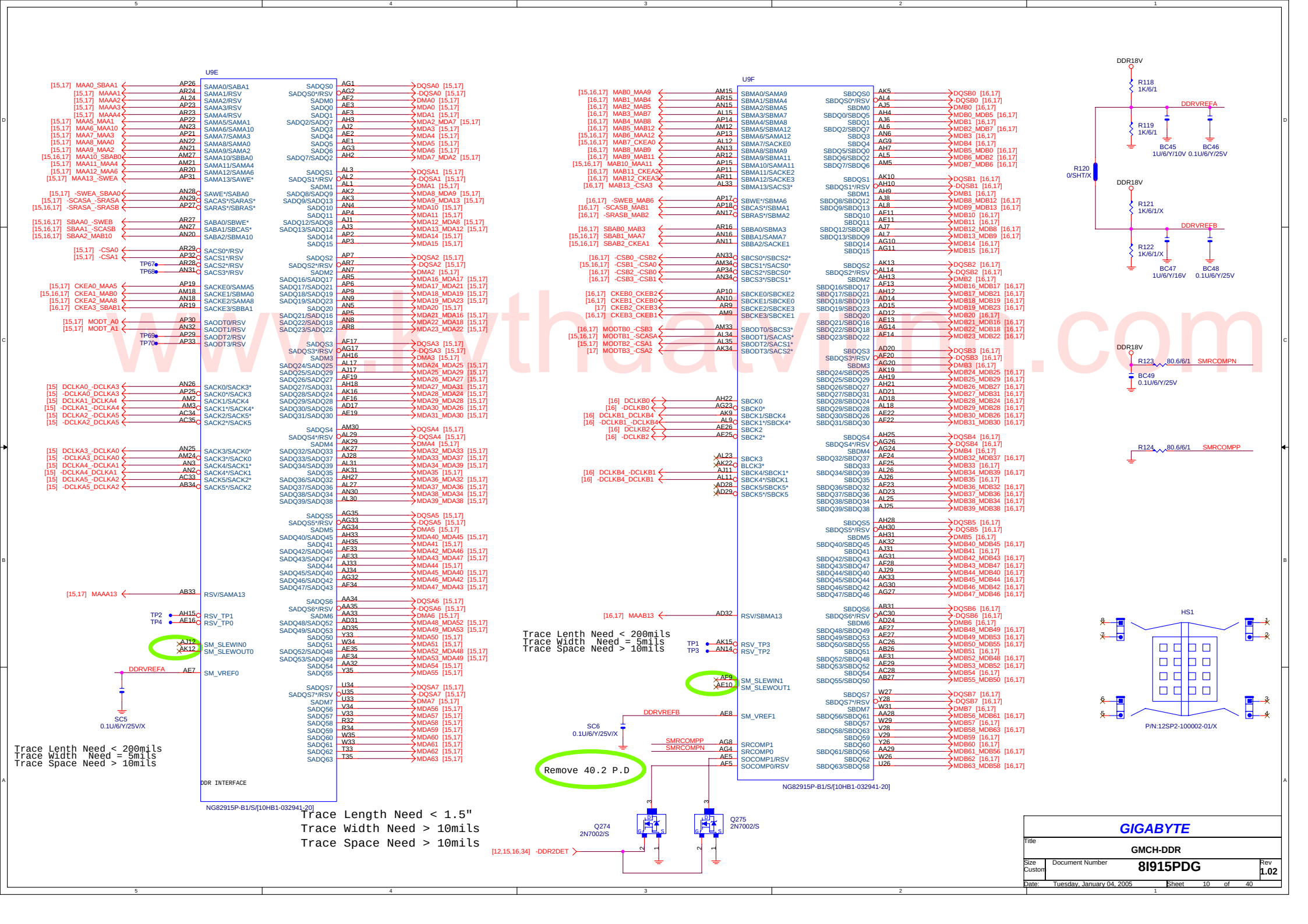


GIGABYTE			
Title	GMCH-HOST		
Size: Custom	Document Number: 8I915PDG		Rev: 1.02
Date: Tuesday, January 04, 2005	Sheet 9 of 40		


U9E
U9F
DDR INTERFACE
NG82915P-B1/S/[10HB1-032941-20]
Trace Lenth Need < 200mils
Trace Width Need = 5mils
Trace Space Need > 10mils
Trace Length Need < 1.5"
Trace Width Need > 10mils
Trace Space Need > 10mils
Remove 40.2 P.D
DDR18V
DDRVREFA
DDRVREFB
SMRCOMPN
SMRCOMPP
R118 1K/6/1
R119 1K/6/1
R120 0/SHT/X
R121 1K/6/1/X
R122 1K/6/1/X
R123 80.6/6/1
R124 80.6/6/1
BC45 1U/6Y/10V
BC46 0.1U/6Y/25V
BC47 1U/6Y/16V
BC48 0.1U/6Y/25V
BC49 0.1U/6Y/25V
SC5 0.1U/6Y/25V/X
SC6 0.1U/6Y/25V/X
Q274 2N7002/S
Q275 2N7002/S
HS1
P/N:12SP2-100002-01/X
GIGABYTE
Title
GMCH-DDR
Size Custom
Document Number 8I915PDG
Rev 1.02
Date: Tuesday, January 04, 2005
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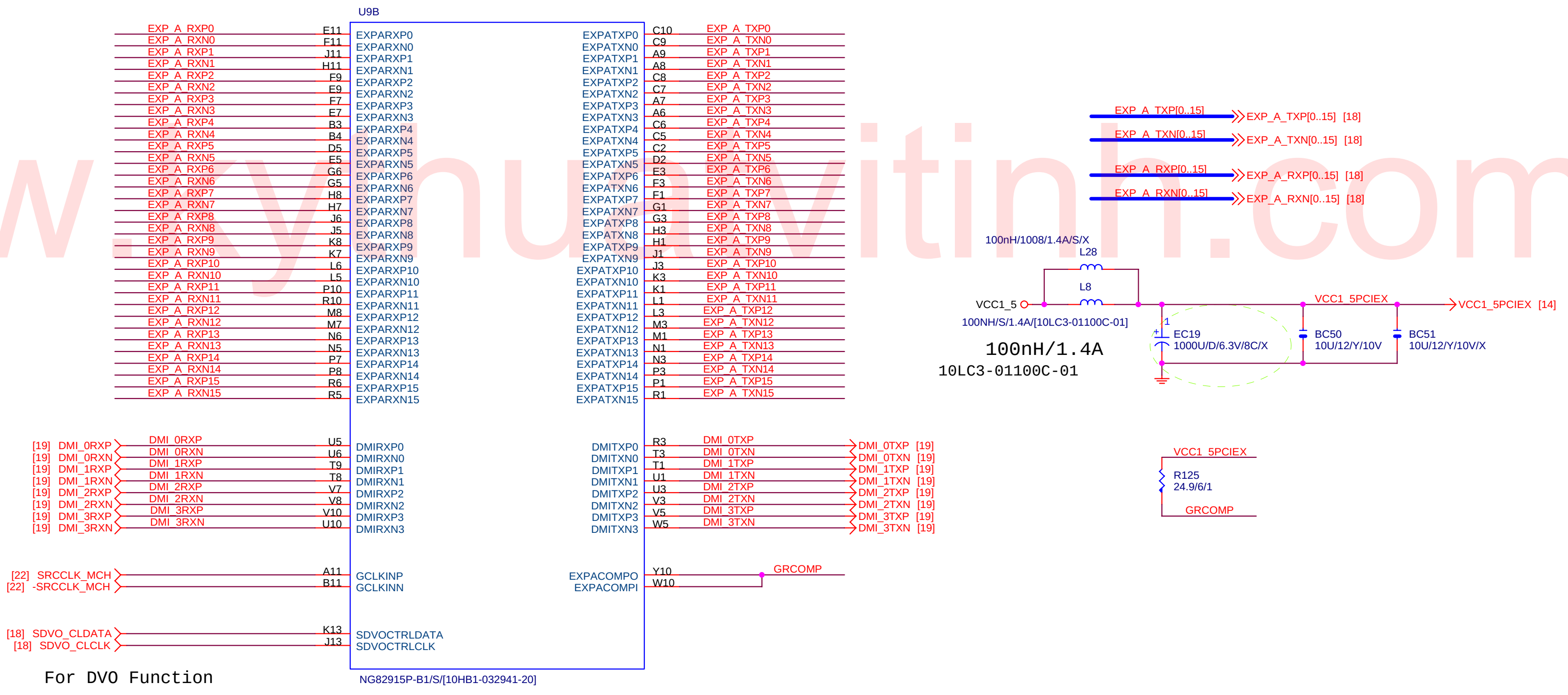
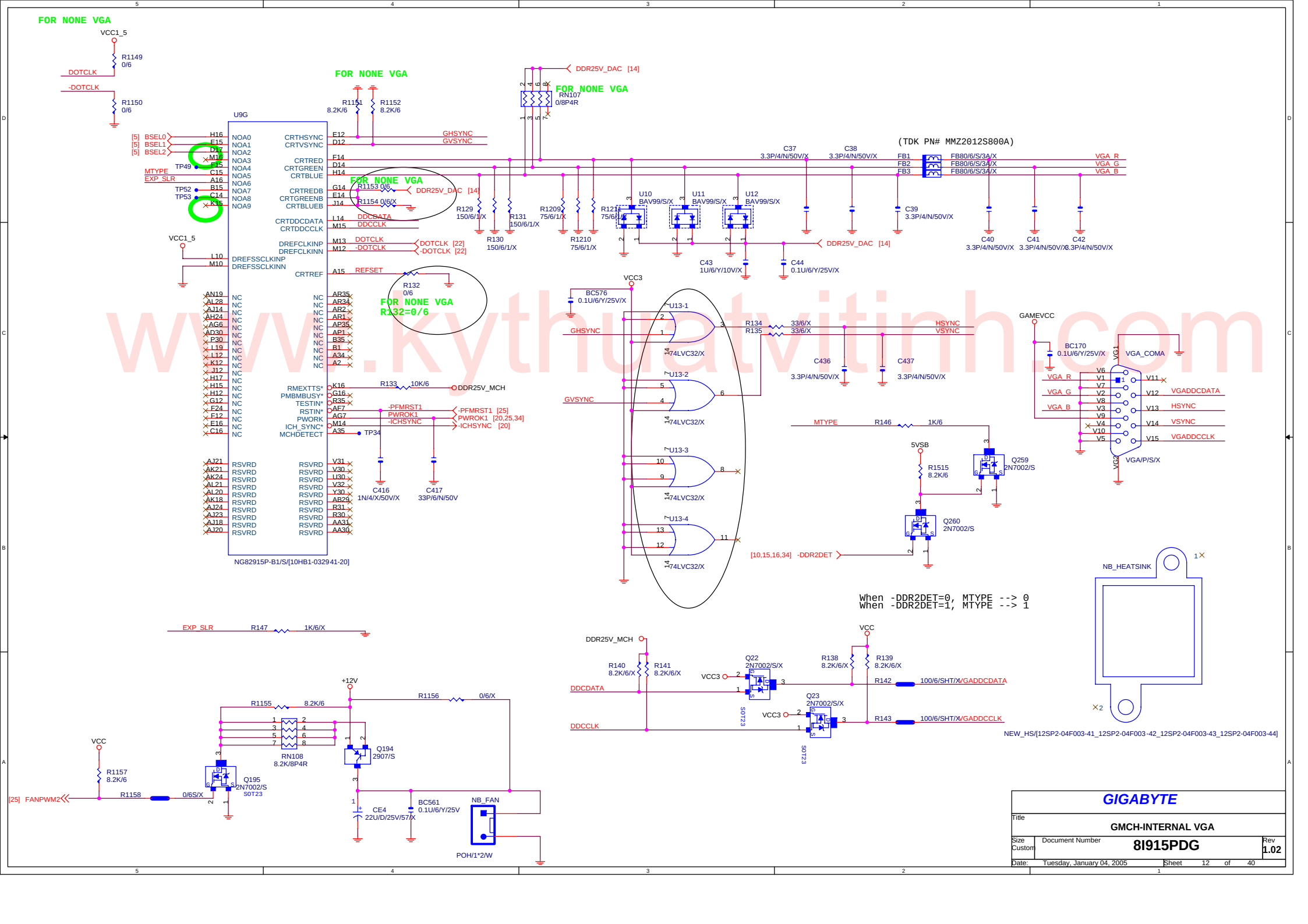


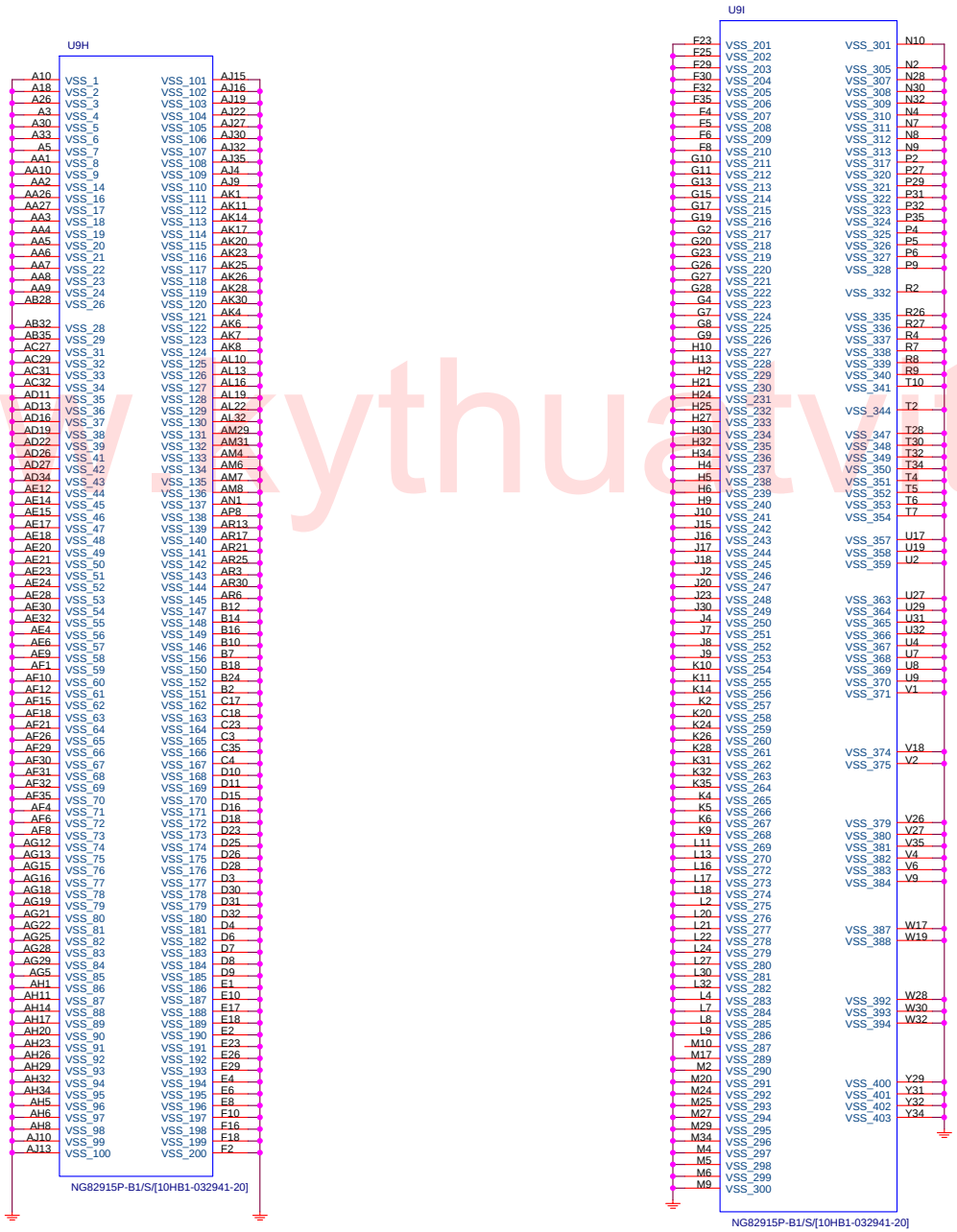
GIGABYTE

Title: GMCH-PCI E & DMI

Size	Document Number	Rev
Custom	8I915PDG	1.02

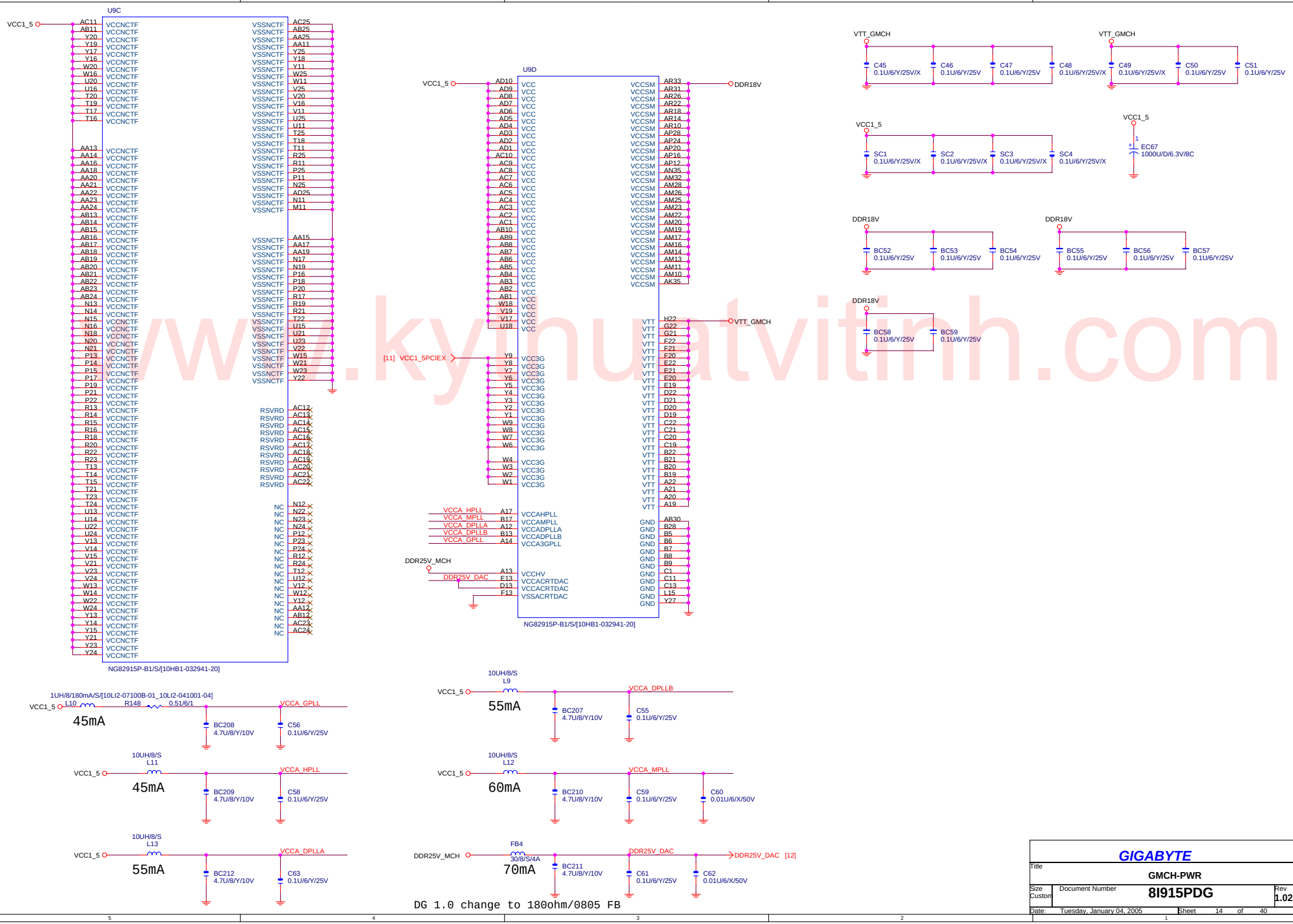
Date: Tuesday, January 04, 2005 Sheet 11 of 40

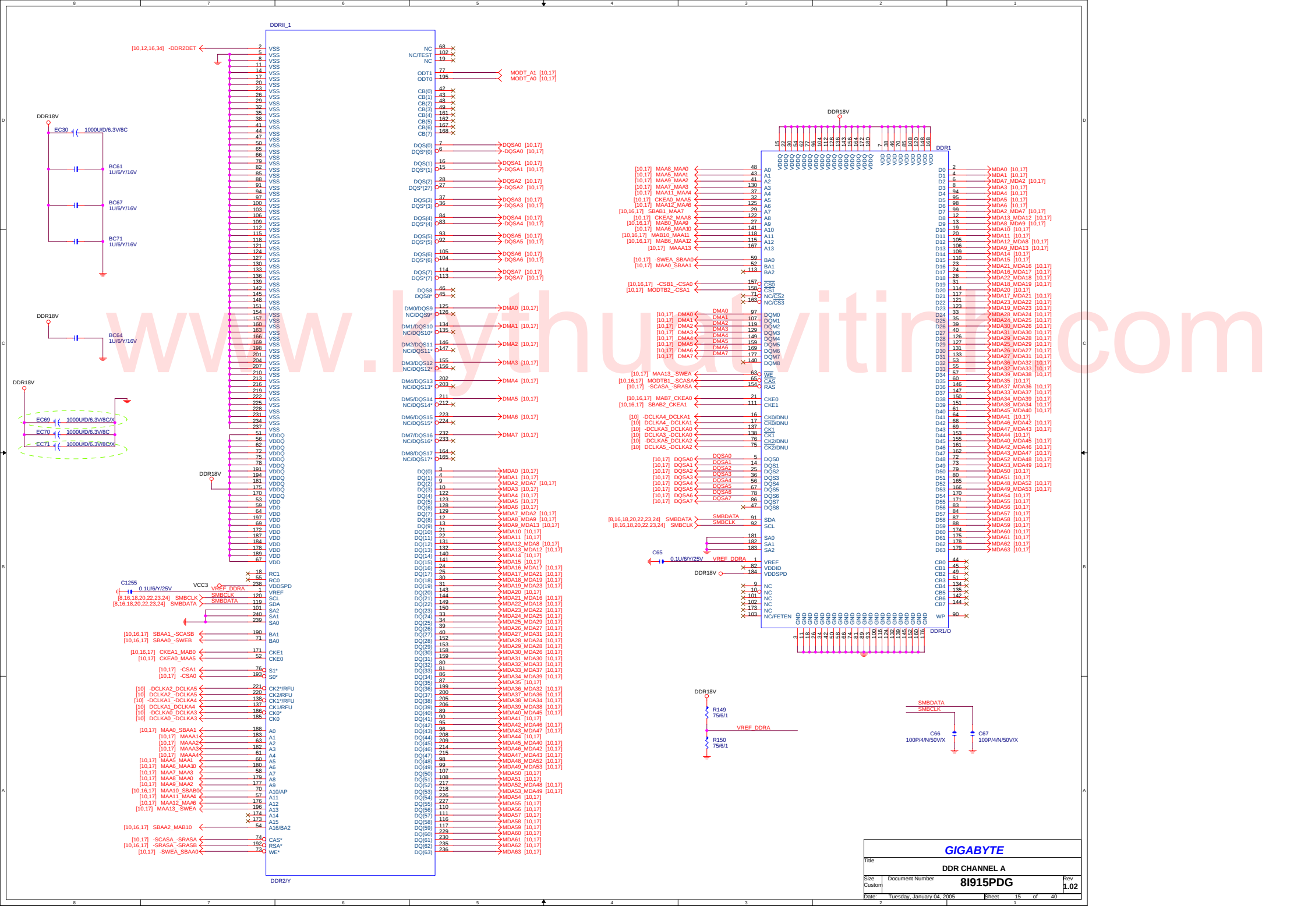


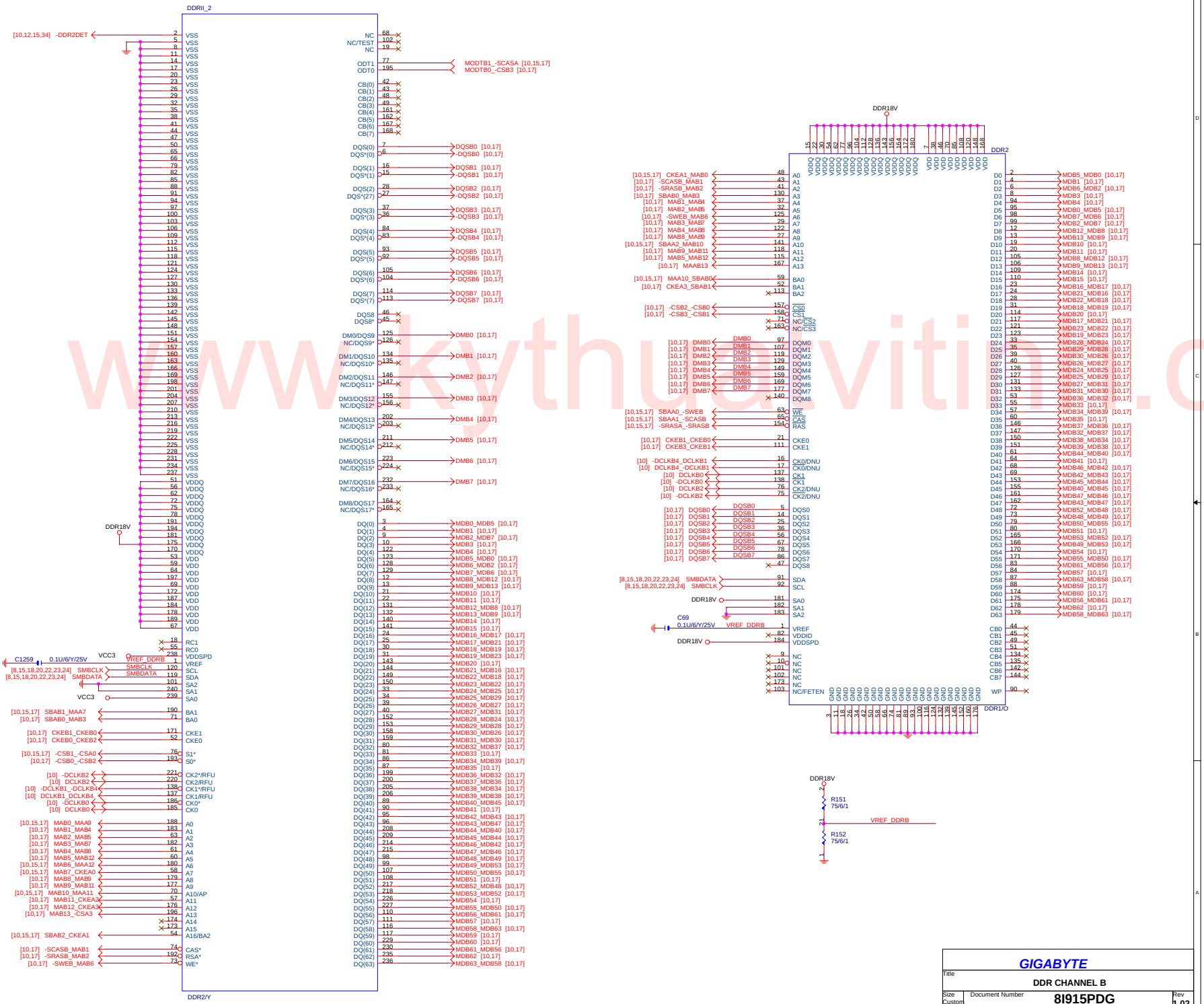


GIGABYTE

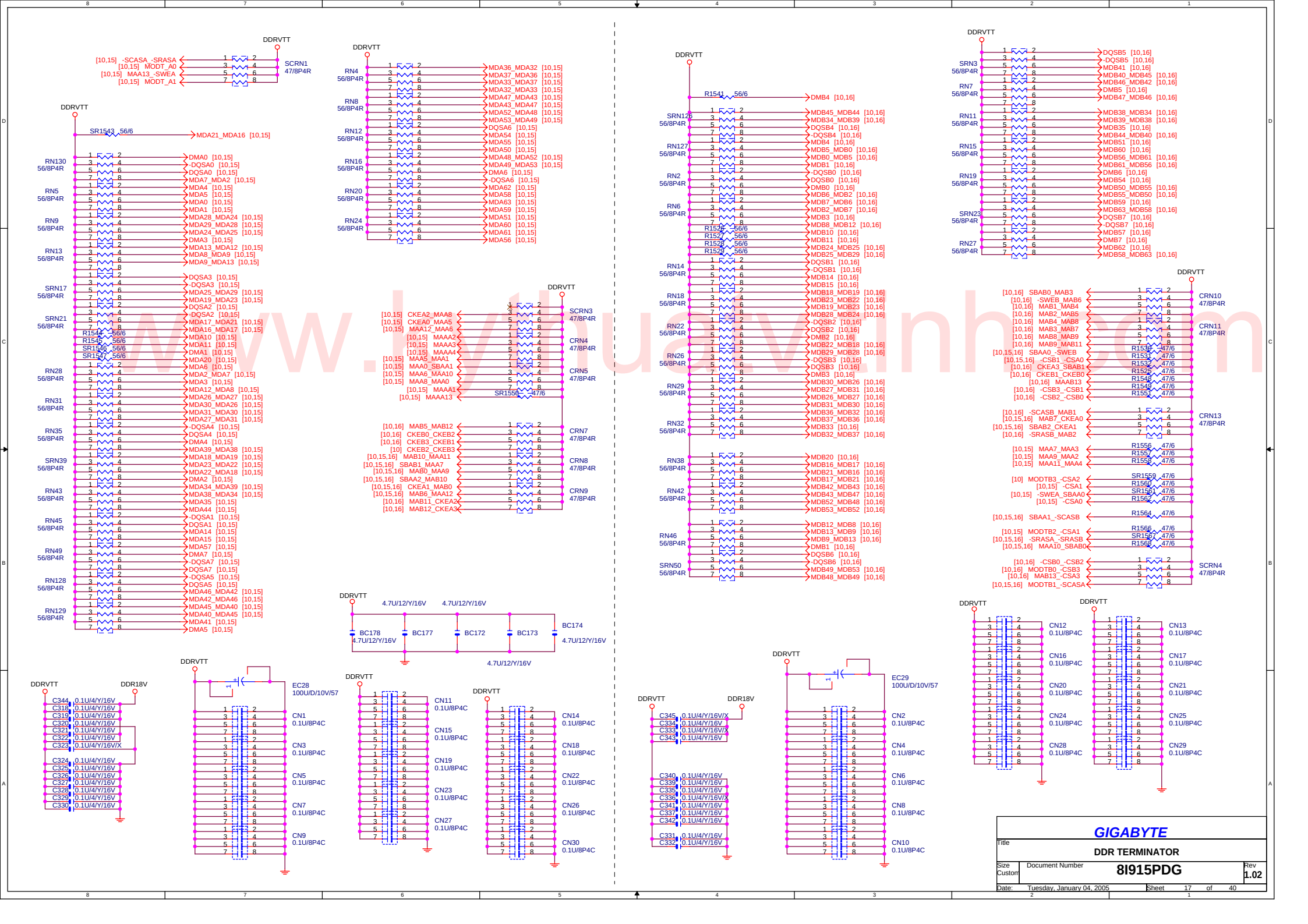
Title	GMCH-GND	
Size: Custom	Document Number: 8I915PDG	Rev: 1.02
Date: Tuesday, January 04, 2005	Sheet 13 of 40	

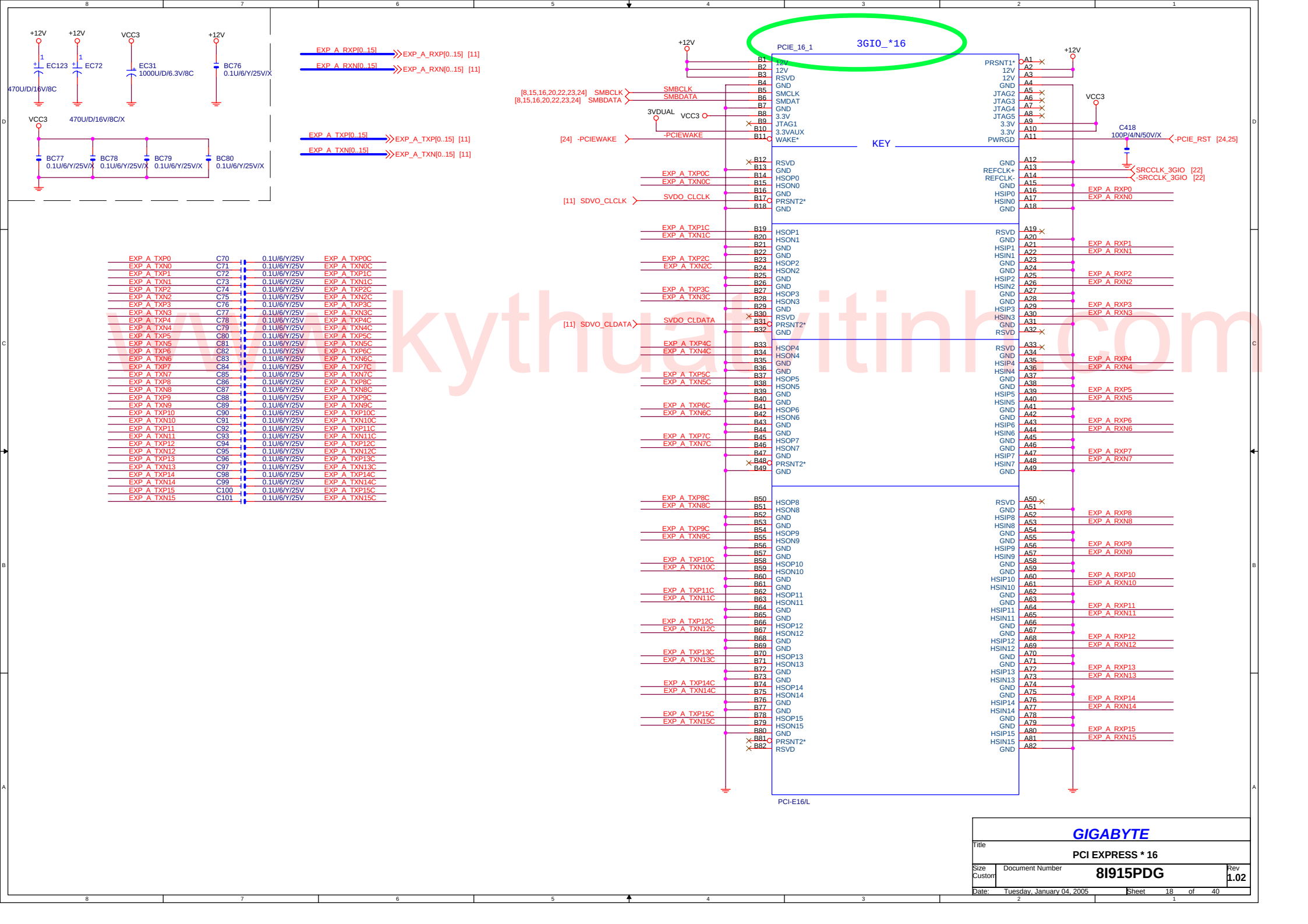


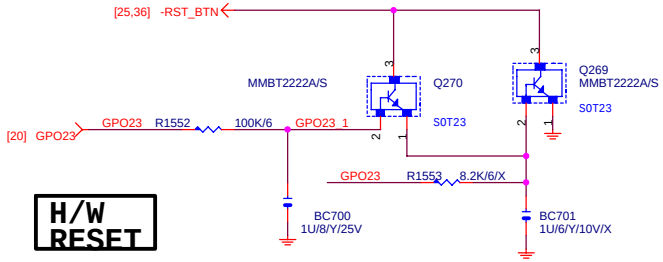




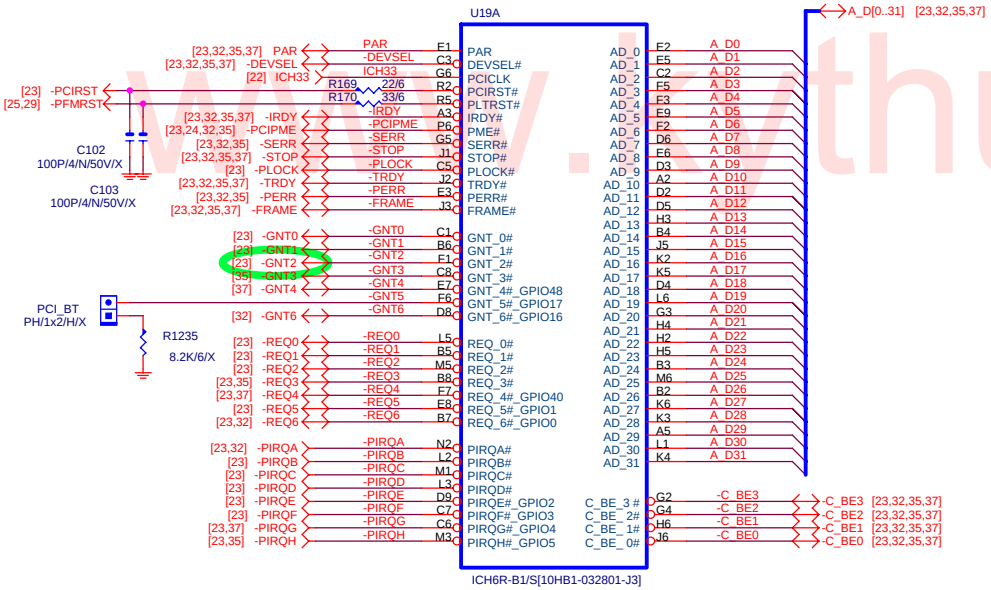
GIGABYTE		
Title	DDR CHANNEL B	
Size: Custom	Document Number: 8I915PDG	Rev: 1.02
Date: Tuesday, January 04, 2005	Sheet 16 of 40	

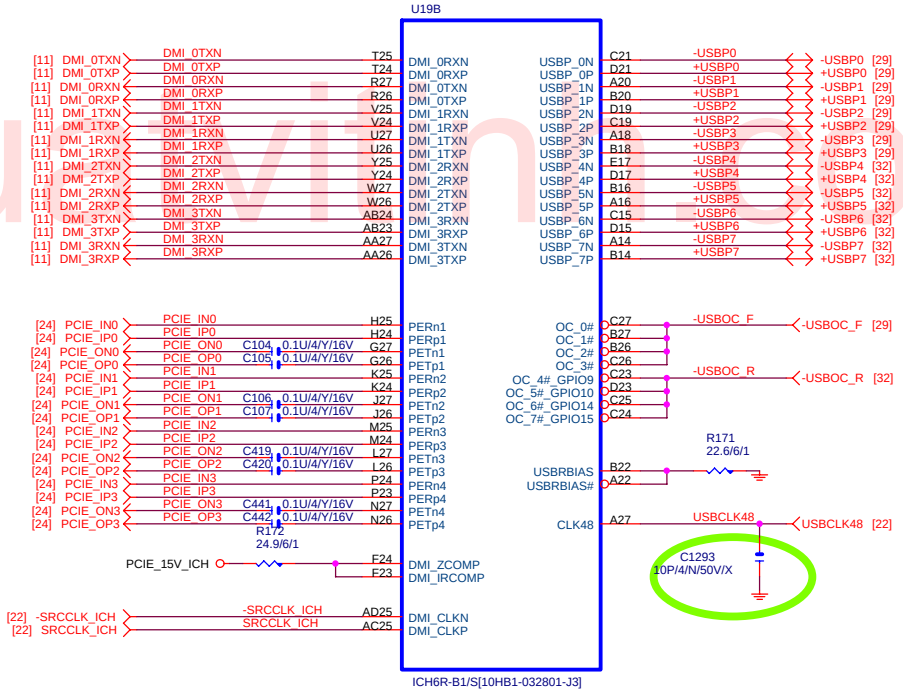


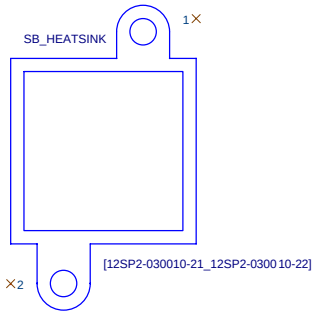




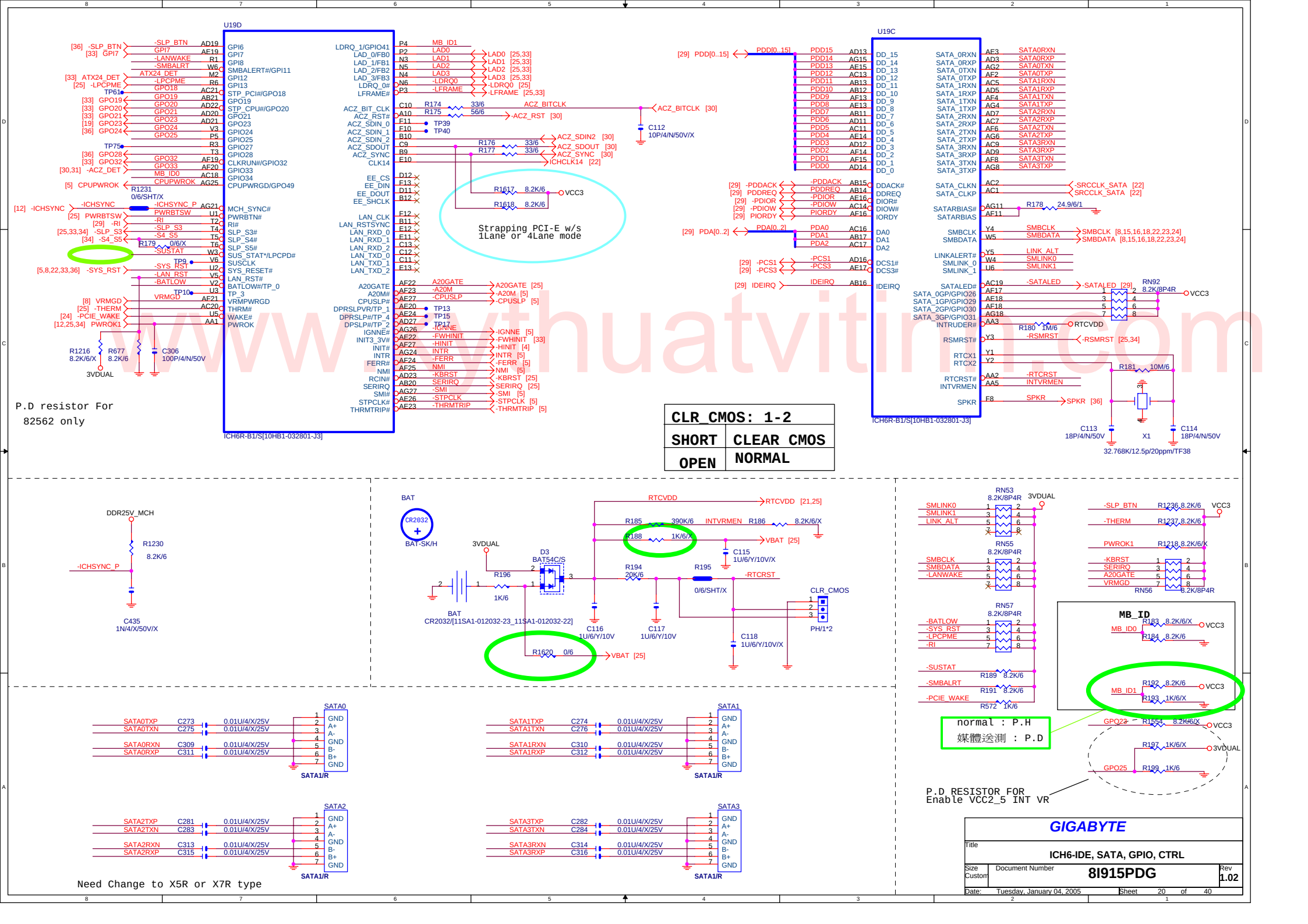
DMI Connection Note
GMCH TX Pin Need Connect to ICH6 RX Pin
ICH6 TX Pin Need Connect to GMCH RX Pin







GIGABYTE		
Title: ICH6-PCI, DMI, LAN, USB		
Size: B	Document Number: 8I915PDG	Rev: 1.02
Date: Tuesday, January 04, 2005	Sheet 19 of 40	


U19D
ICH6R-B1/S[10HB1-032801-J3]
U19C
ICH6R-B1/S[10HB1-032801-J3]
Strapping PCI-E w/s
1Lane or 4Lane mode
P.D resistor For
82562 only
CLR_CMOS: 1-2
SHORT CLEAR CMOS
OPEN NORMAL
BAT
BAT-SK/H
BAT
CR2032/[11SA1-012032-23_11SA1-012032-22]
SATA0
SATA1
SATA2
SATA3
SATA1/R
Need Change to X5R or X7R type
MB_ID
normal : P.H
媒體送測 : P.D
P.D RESISTOR FOR
Enable VCC2_5 INT VR
GIGABYTE
ICH6-IDE, SATA, GPIO, CTRL
8I915PDG
Rev 1.02
Tuesday, January 04, 2005
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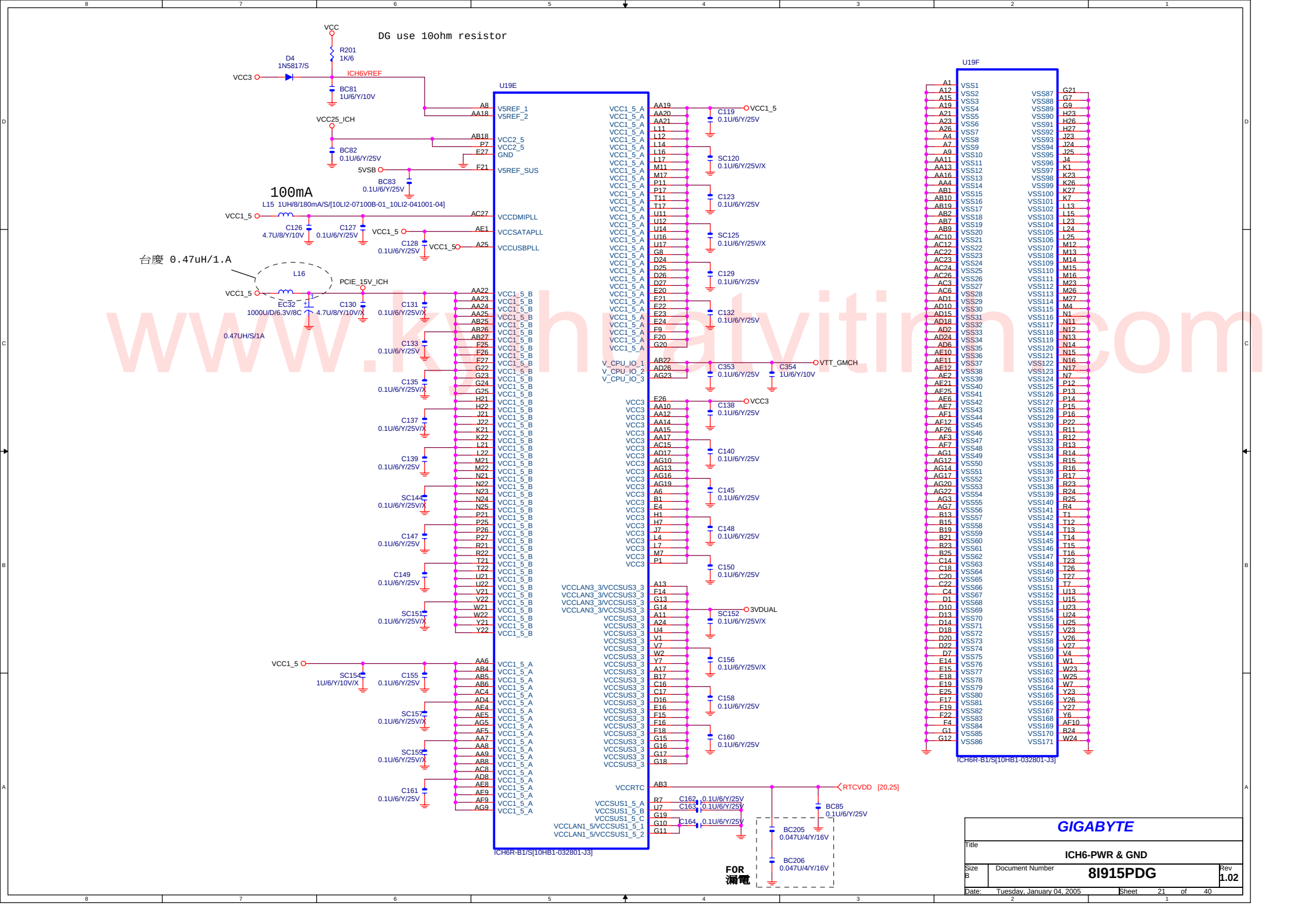
DG use 10ohm resistor
100mA
台慶 0.47uH/1.A
U19E
U19F
ICH6R-B1/S[10HB1-032801-J3]
GIGABYTE
Title
ICH6-PWR & GND
Size B
Document Number
8I915PDG
Rev 1.02
Date: Tuesday, January 04, 2005
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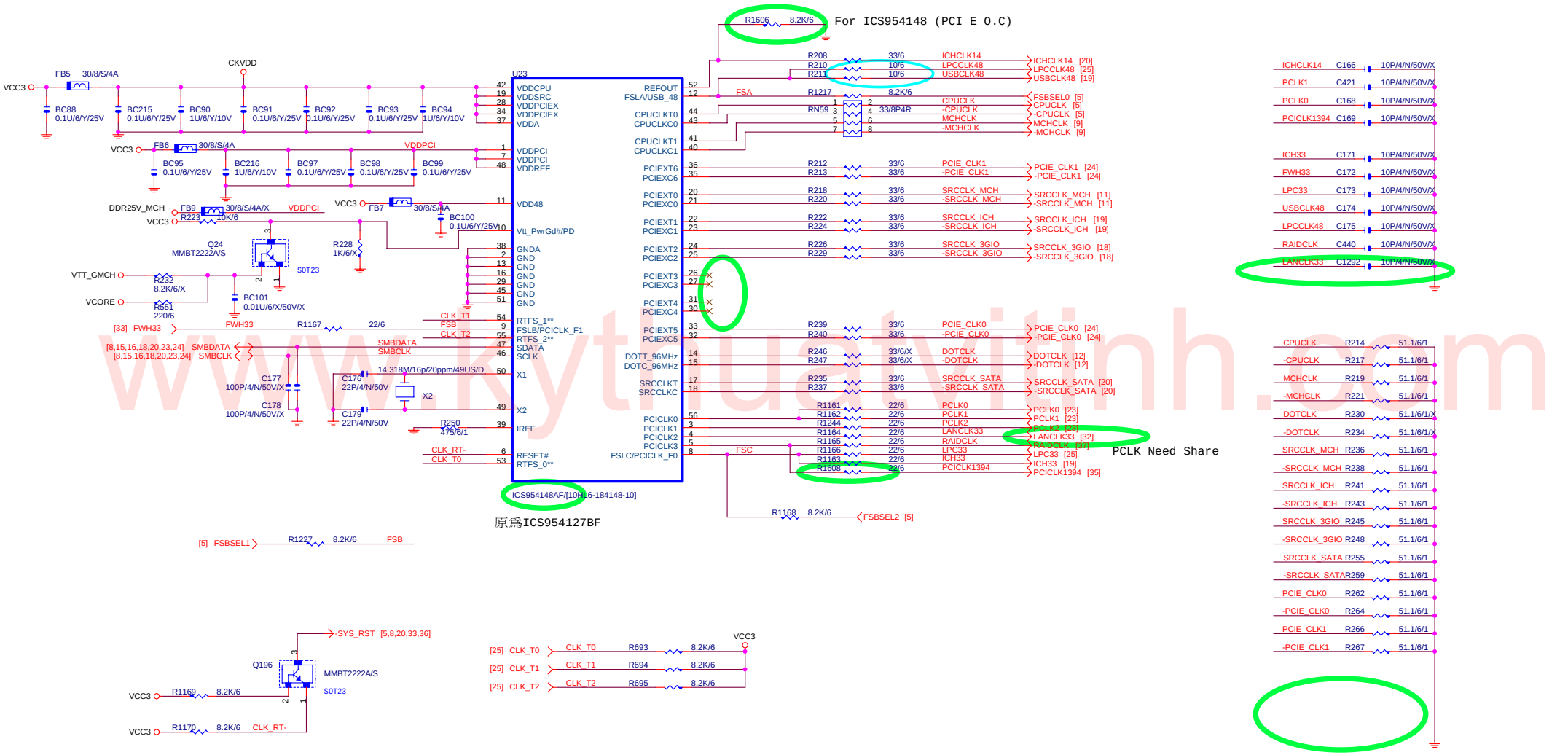
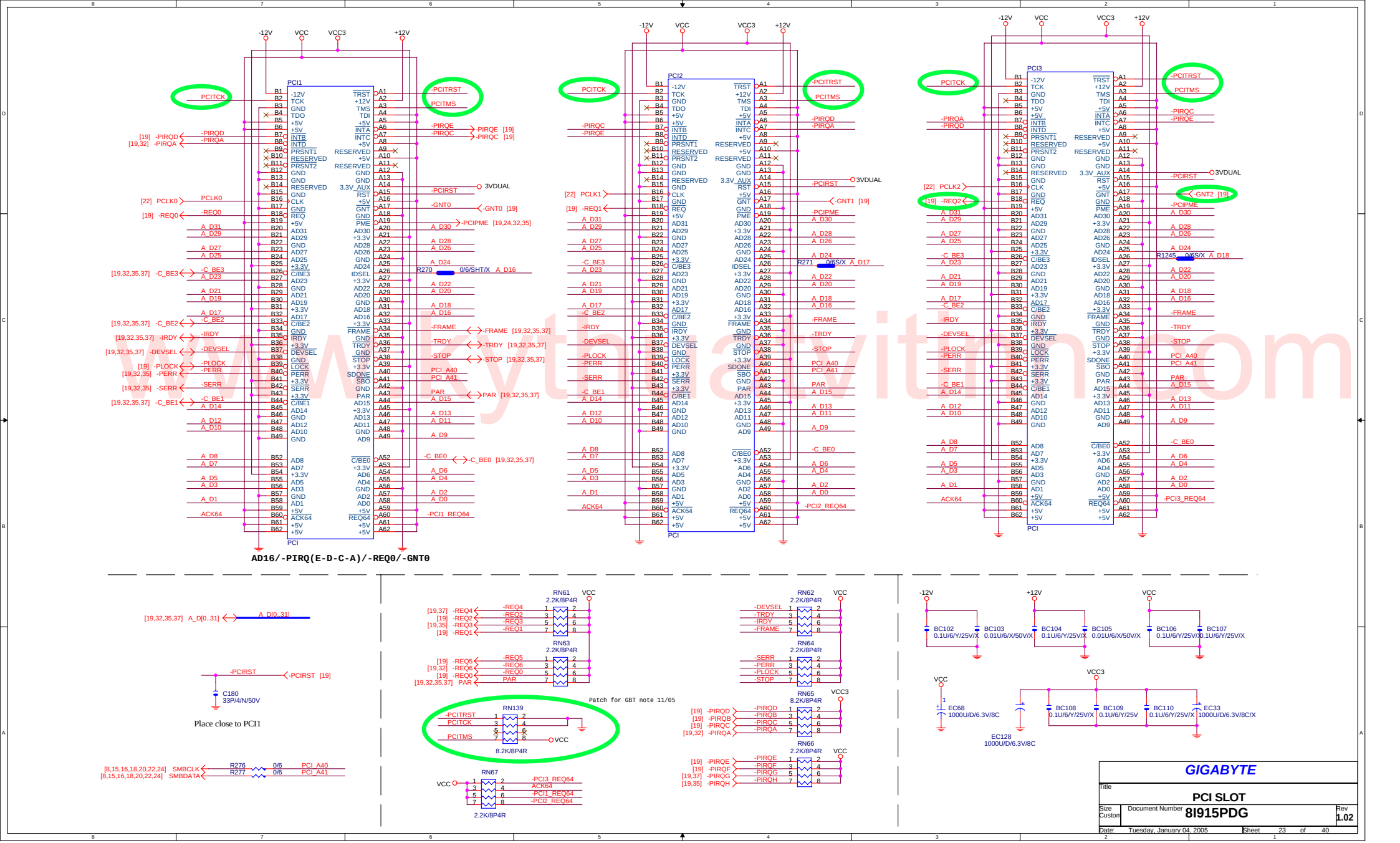
FOR 漏電

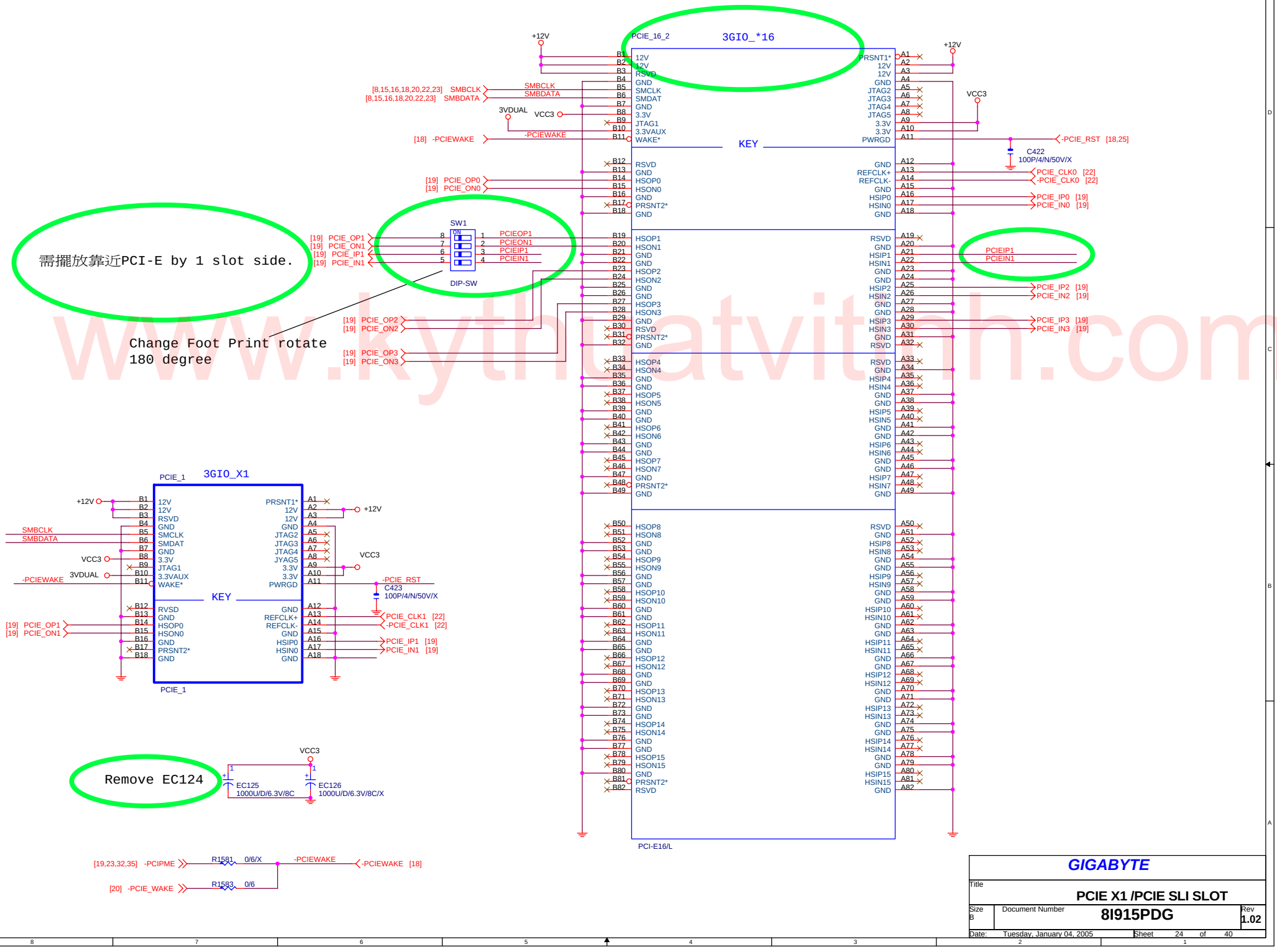


GIGABYTE			
Title	CK410M/GBT_CLK GEN		
Size: Custom	Document Number: 8I915PDG		Rev: 1.02
Date: Tuesday, January 04, 2005	Sheet 22 of 40		

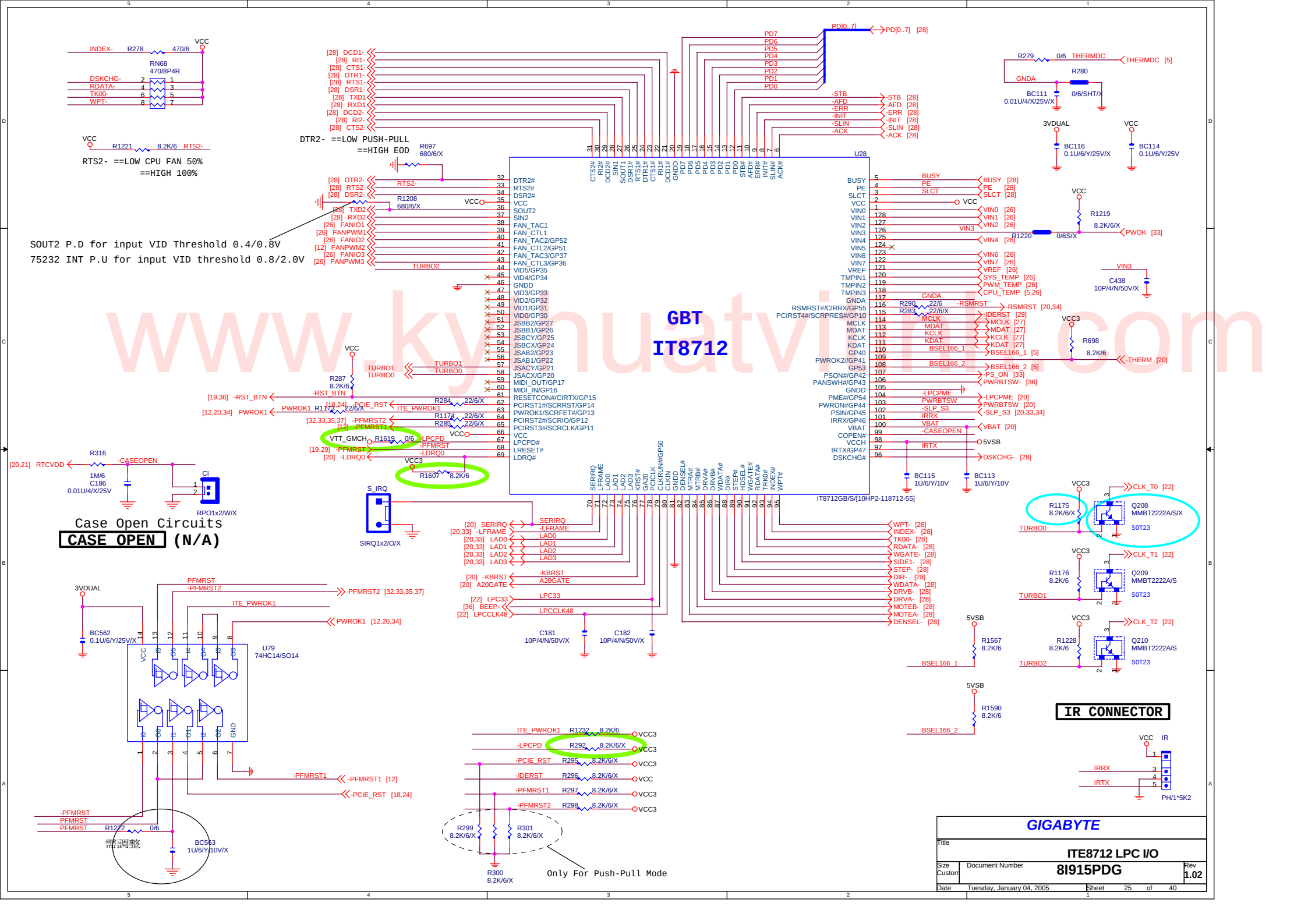


GIGABYTE

Title	PCI SLOT	
Size: Custom	Document Number: 8I915PDG	Rev: 1.02
Date: Tuesday, January 04, 2005	Sheet 23 of 40	



GIGABYTE		
Title	PCIE X1 /PCIE SLI SLOT	
Size B	Document Number 8I915PDG	Rev 1.02
Date: Tuesday, January 04, 2005	Sheet 24 of 40	


GBT
IT8712
SOUT2 P.D for input VID Threshold 0.4/0.8V
75232 INT P.U for input VID threshold 0.8/2.0V
DTR2- ==LOW PUSH-PULL
==HIGH EOD
RTS2- ==LOW CPU FAN 50%
==HIGH 100%
Case Open Circuits
CASE OPEN (N/A)
IR CONNECTOR
Only For Push-Pull Mode
U79
74HC14/SO14
IT8712GB/S/[10HP2-118712-55]
GIGABYTE
ITE8712 LPC I/O
8I915PDG
Rev 1.02
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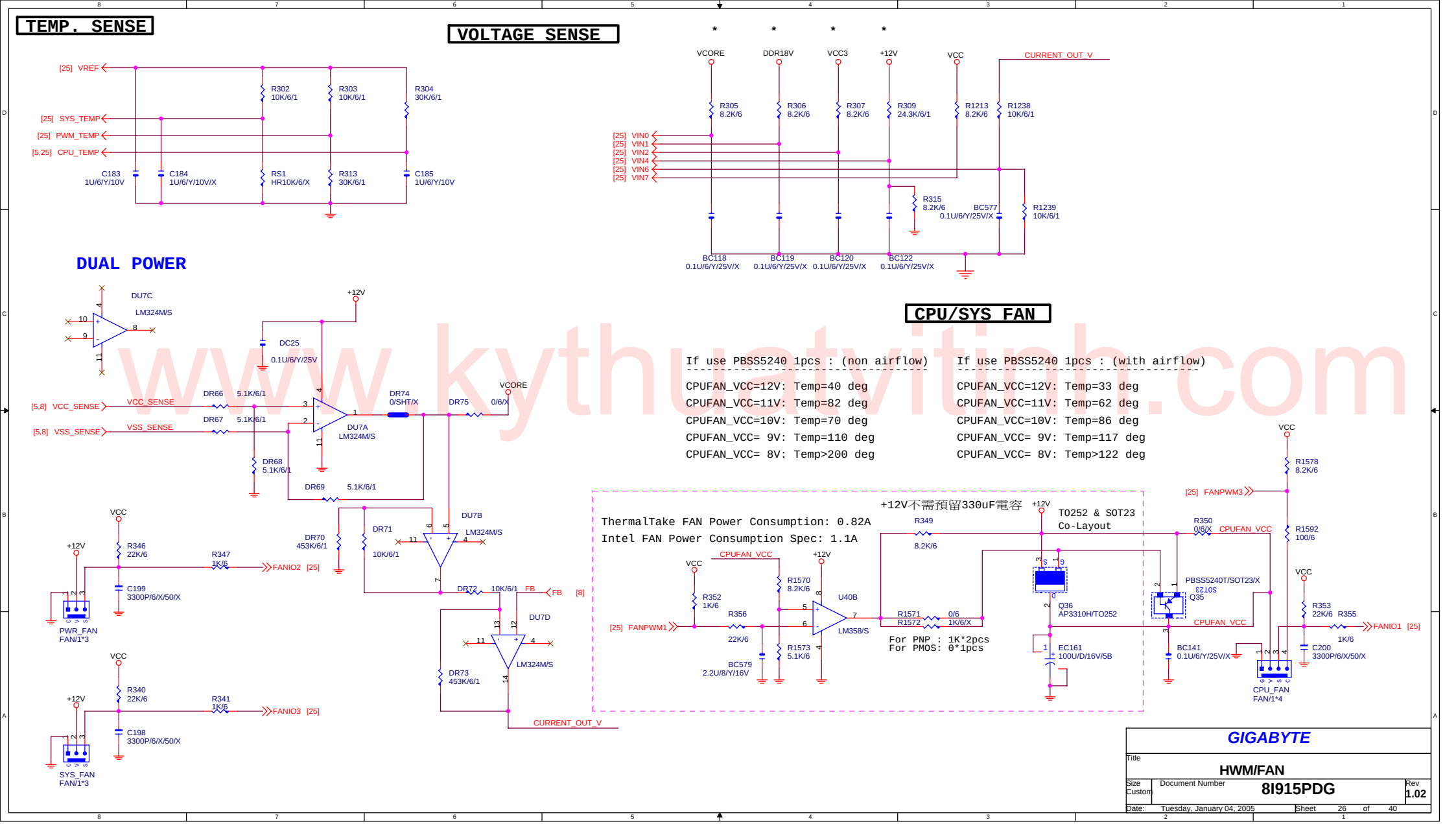
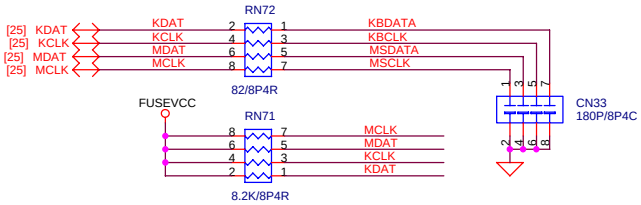
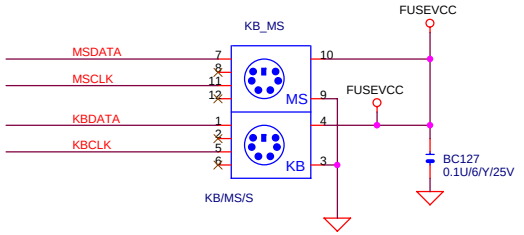
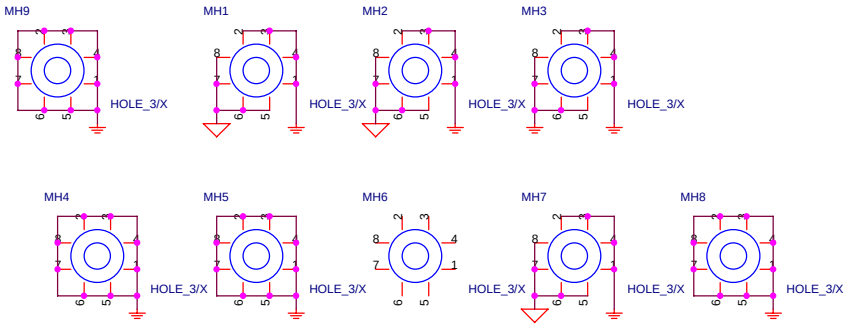


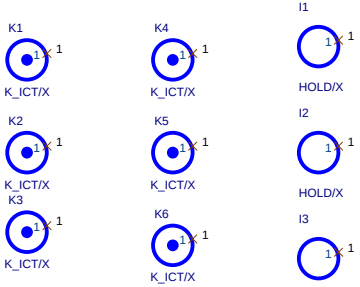
KB/MS





GAME PORT (N/A)





GIGABYTE		
Title: PS/2 KB & MS		
Size: B	Document Number: 8I915PDG	Rev: 1.02
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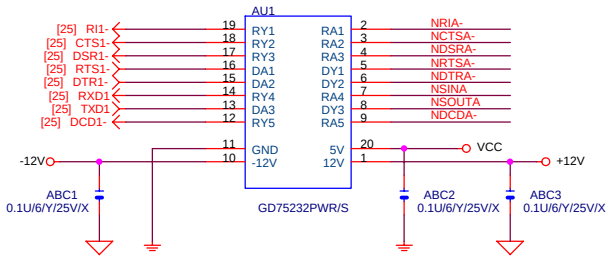
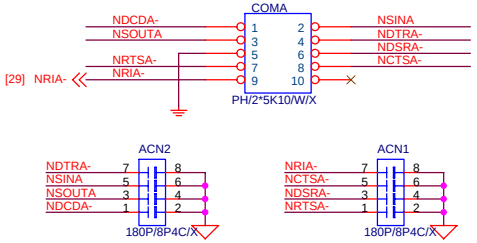
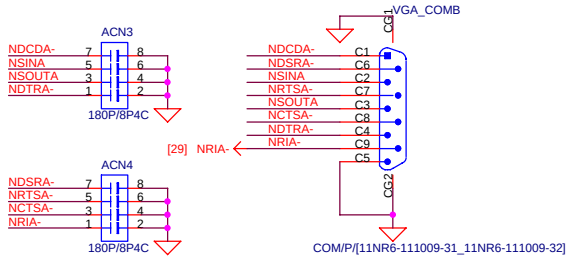
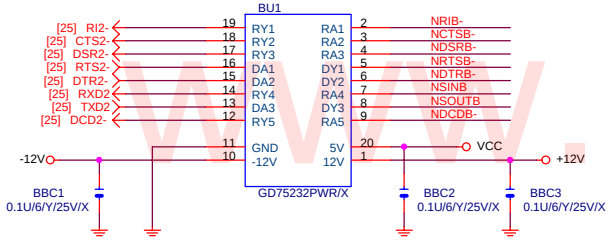
COMA/COMB



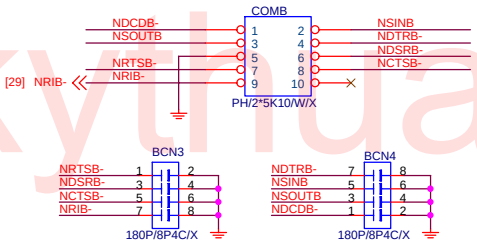
INTERNAL COMA





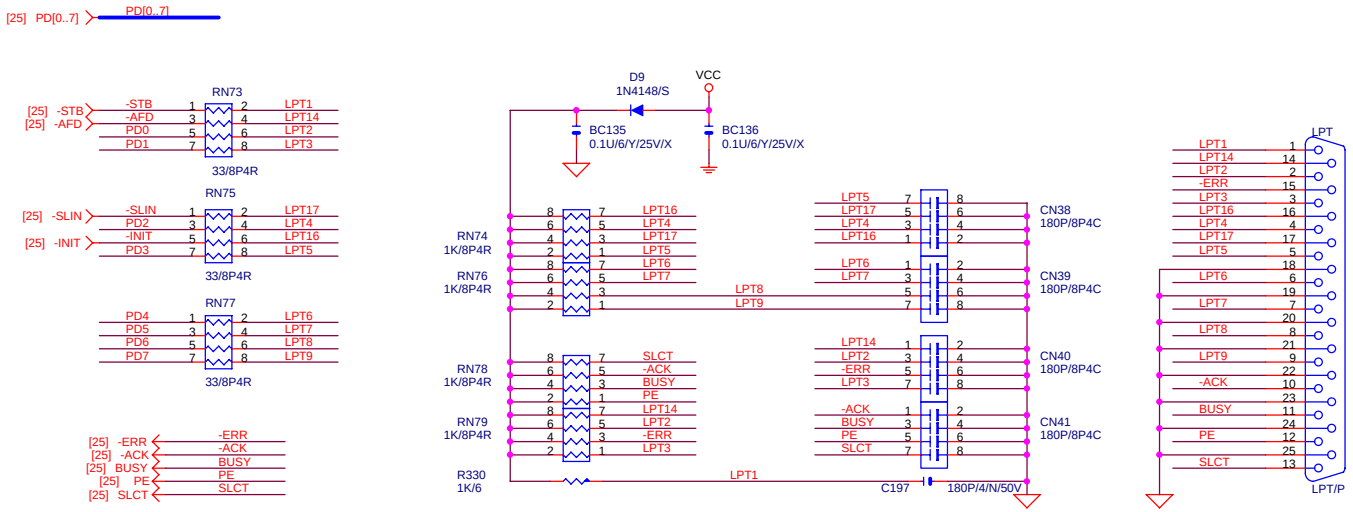


INTERNAL COMB

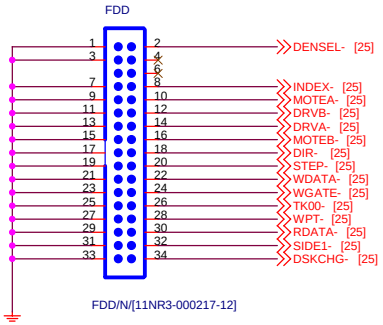


PLACE NEAR VGA_COM CONNECTOR

LPT



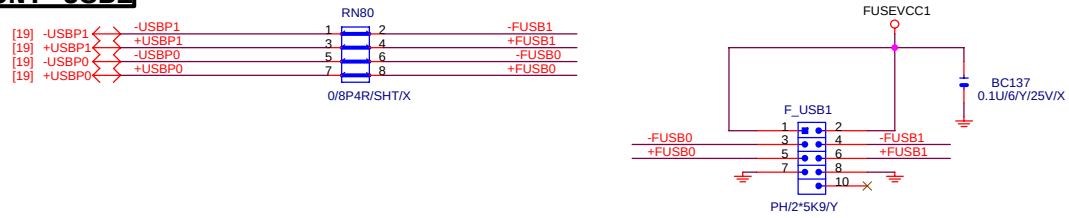
FLOPPY



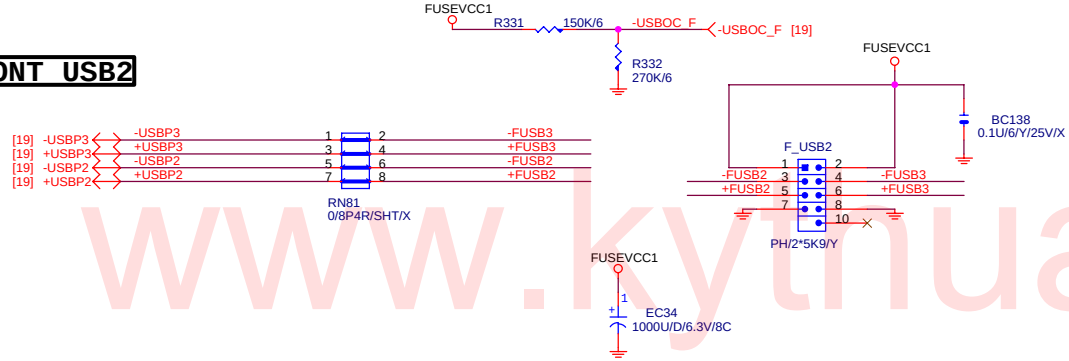
Right Angle Type

GIGABYTE		
Title: COM, LPT, FDD		
Size: B	Document Number: 8I915PDG	Rev: 1.02
Date: Tuesday, January 04, 2005	Sheet 28 of 40	

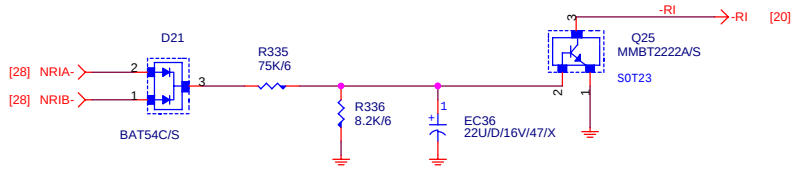
FRONT USB1



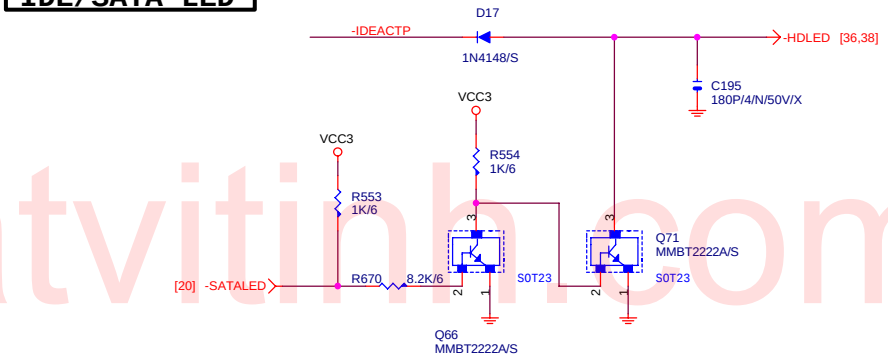
FRONT USB2



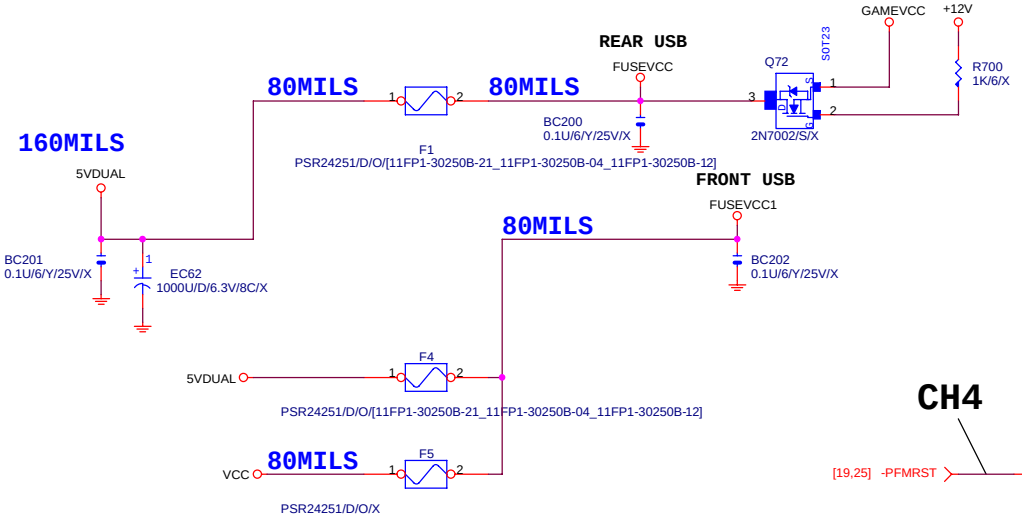
RING IN



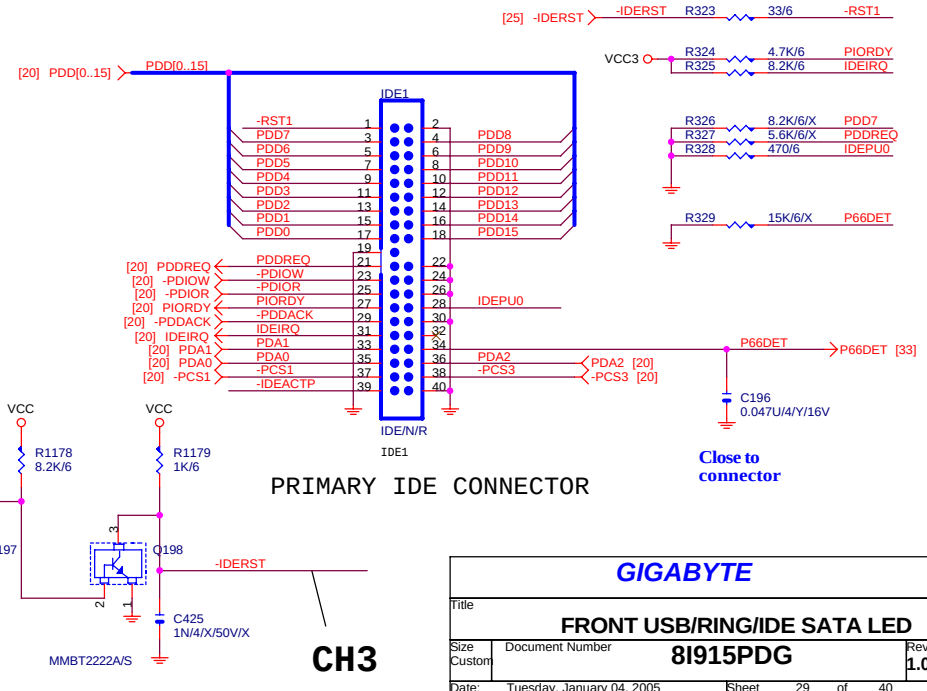
IDE/SATA LED



FUSEVCC,GAMEVCC



IDE



GIGABYTE

Title	FRONT USB/RING/IDE SATA LED	
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"$" means for ALC880 only
"*" means for CMI9880 only

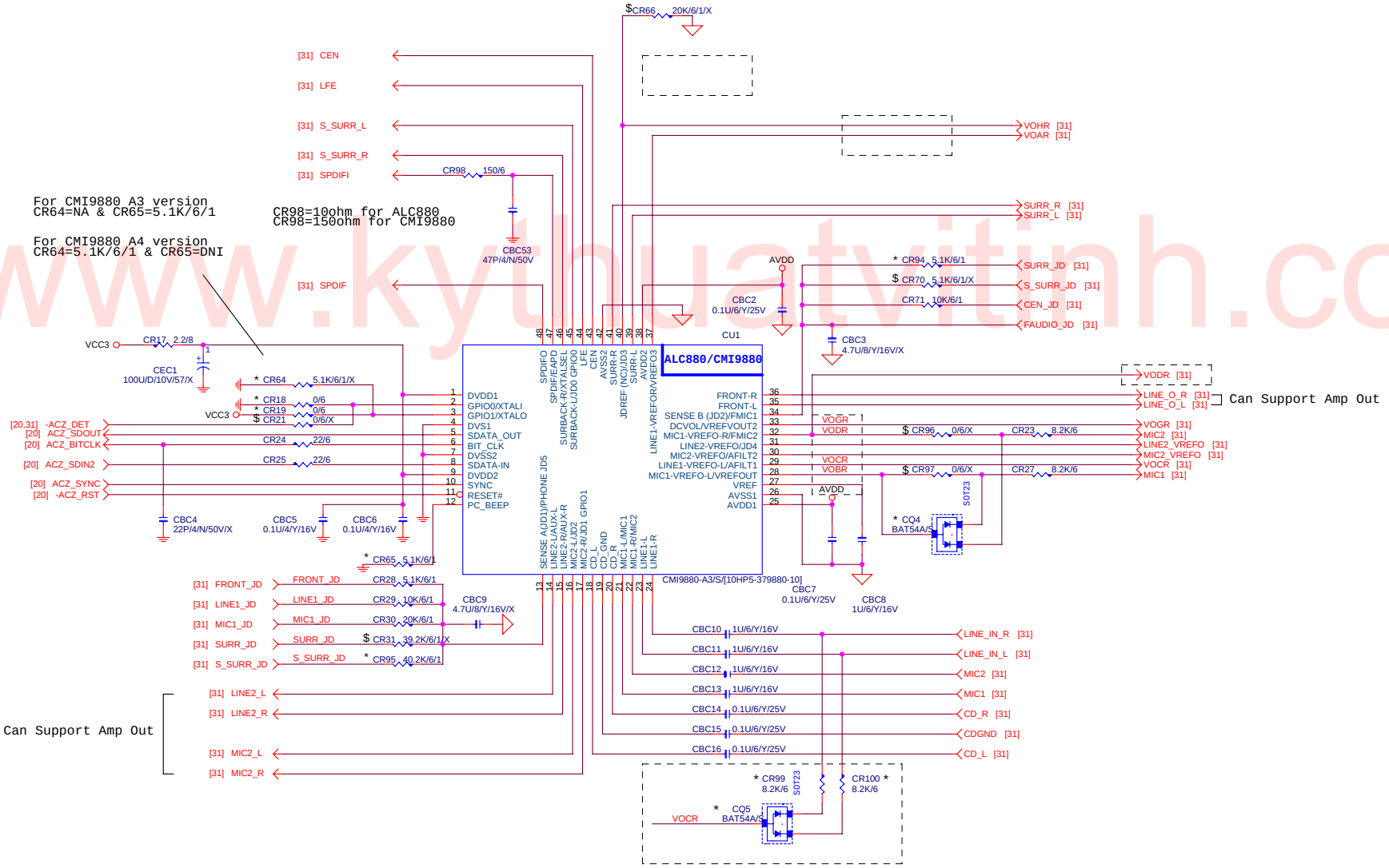
For CMI9880 A3 version
CR64=NA & CR65=5.1K/6/1

For CMI9880 A4 version
CR64=5.1K/6/1 & CR65=DNI

CR98=10ohm for ALC880
CR98=150ohm for CMI9880

Can Support Amp Out

Can Support Amp Out



GIGABYTE

Title: AZALIA CODEC ALC880/CMI9880

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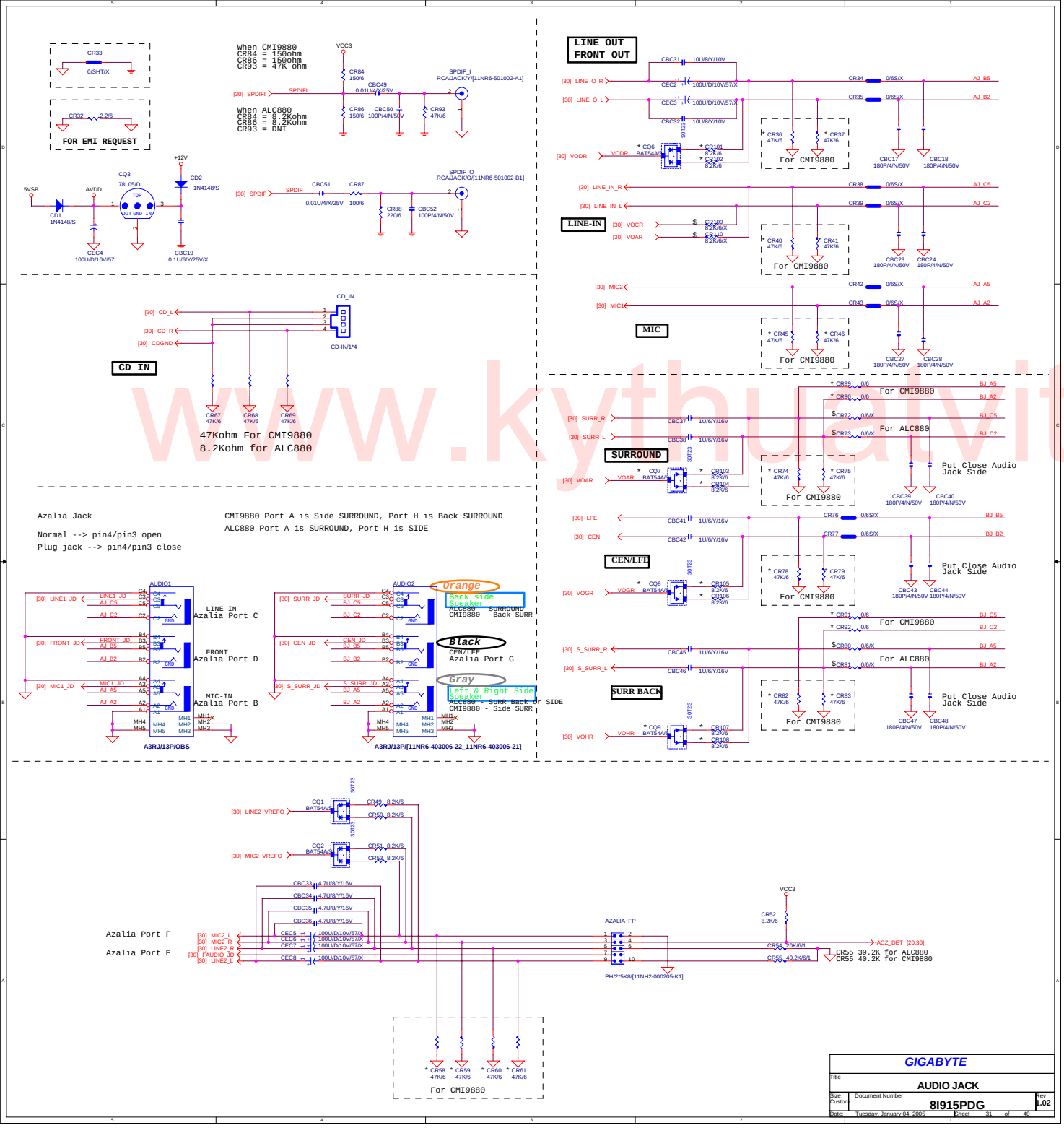

GIGABYTE			
Title: AUDIO JACK			
Size: Custom	Document Number: 8I915PDG		Rev: 1.02
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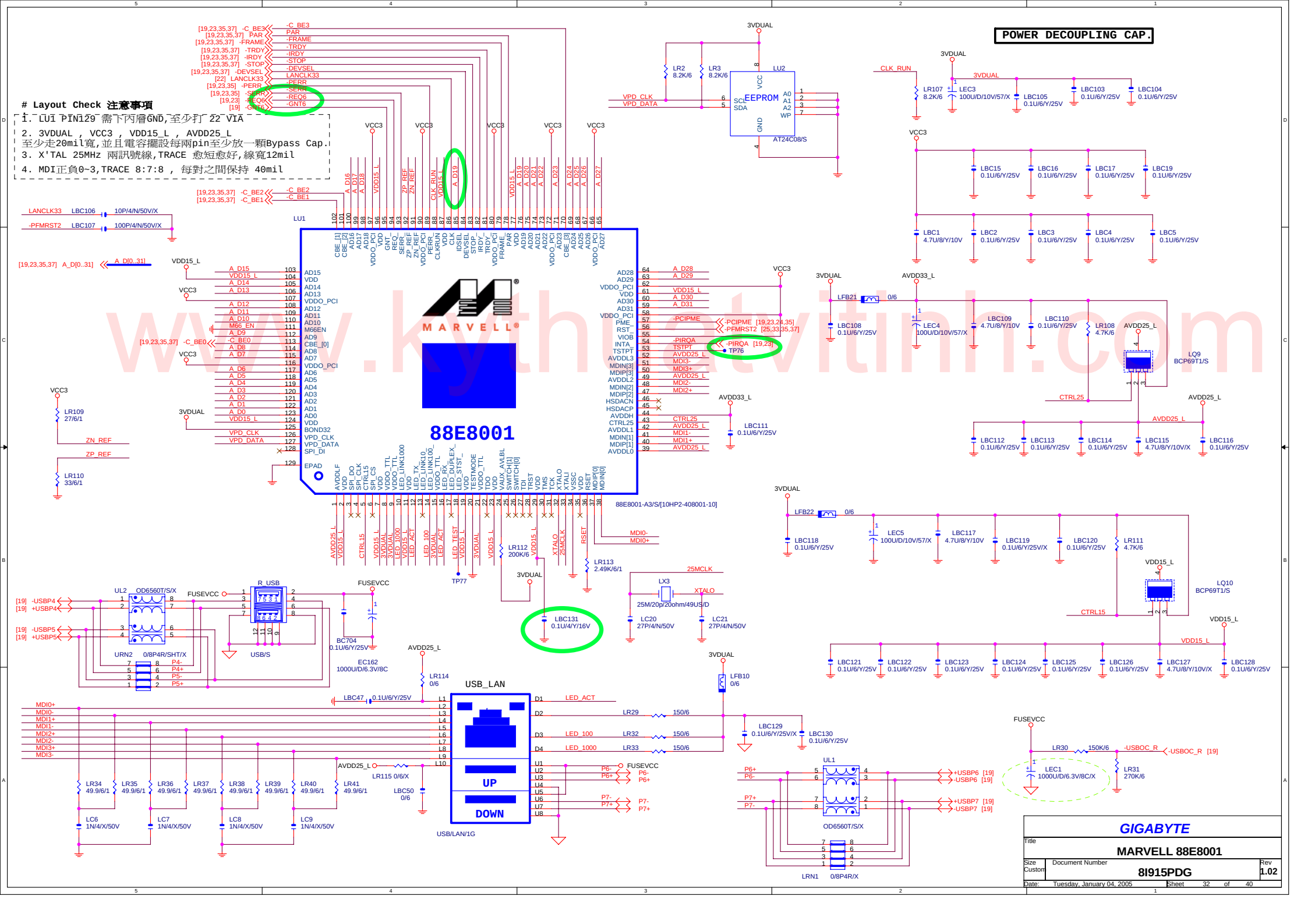
POWER DECOUPLING CAP.
Layout Check 注意事項
1. LU1 PIN129 需下內層GND,至少打 22 VIA
2. 3VDUAL , VCC3 , VDD15_L , AVDD25_L
至少走20mil寬,並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線,TRACE 愈短愈好,線寬12mil
4. MDI正負0~3,TRACE 8:7:8 , 每對之間保持 40mil
88E8001
MARVELL
EEPROM
AT24C08/S
USB_LAN
UP
DOWN
USB/S
GIGABYTE
MARVELL 88E8001
8I915PDG
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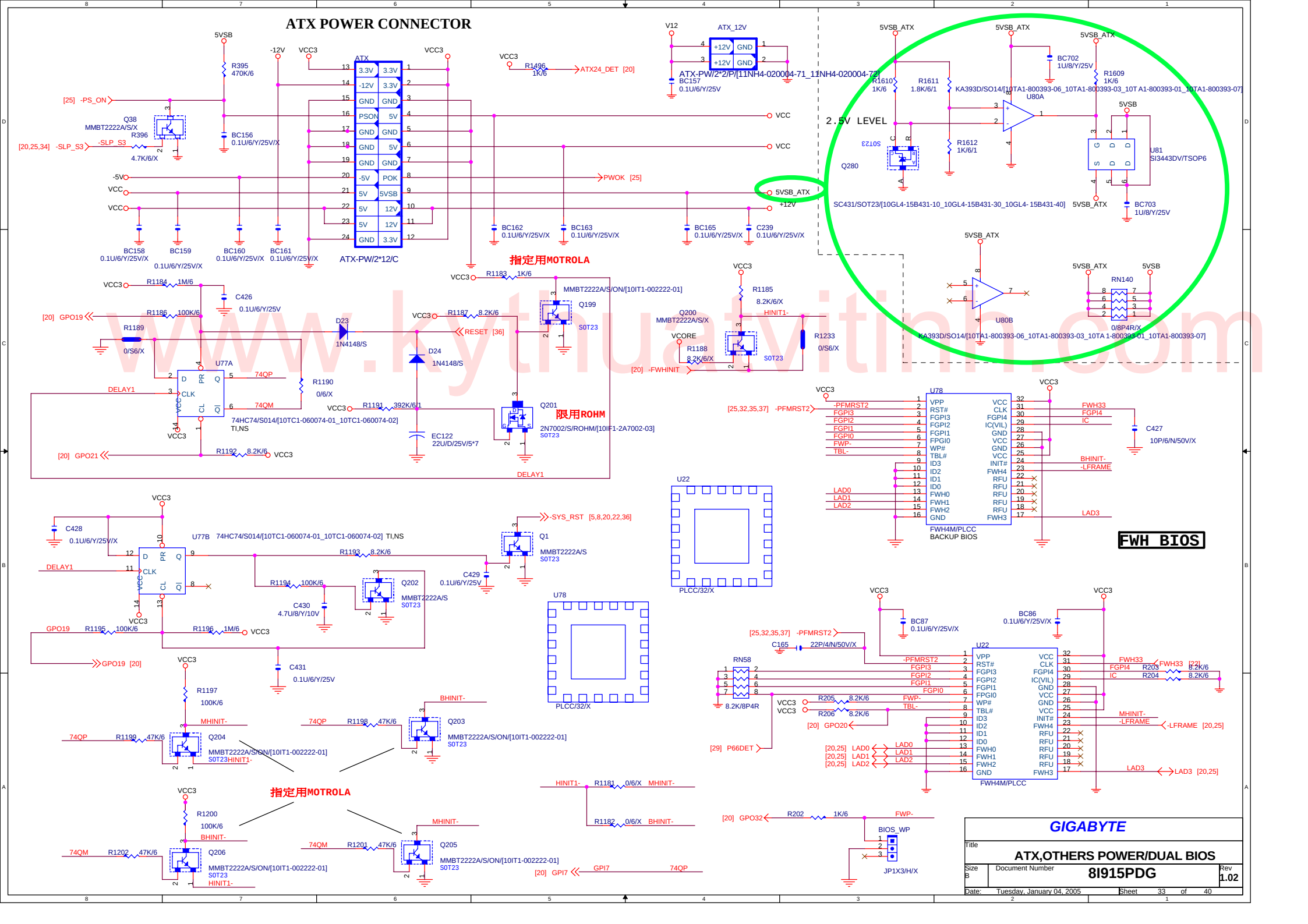

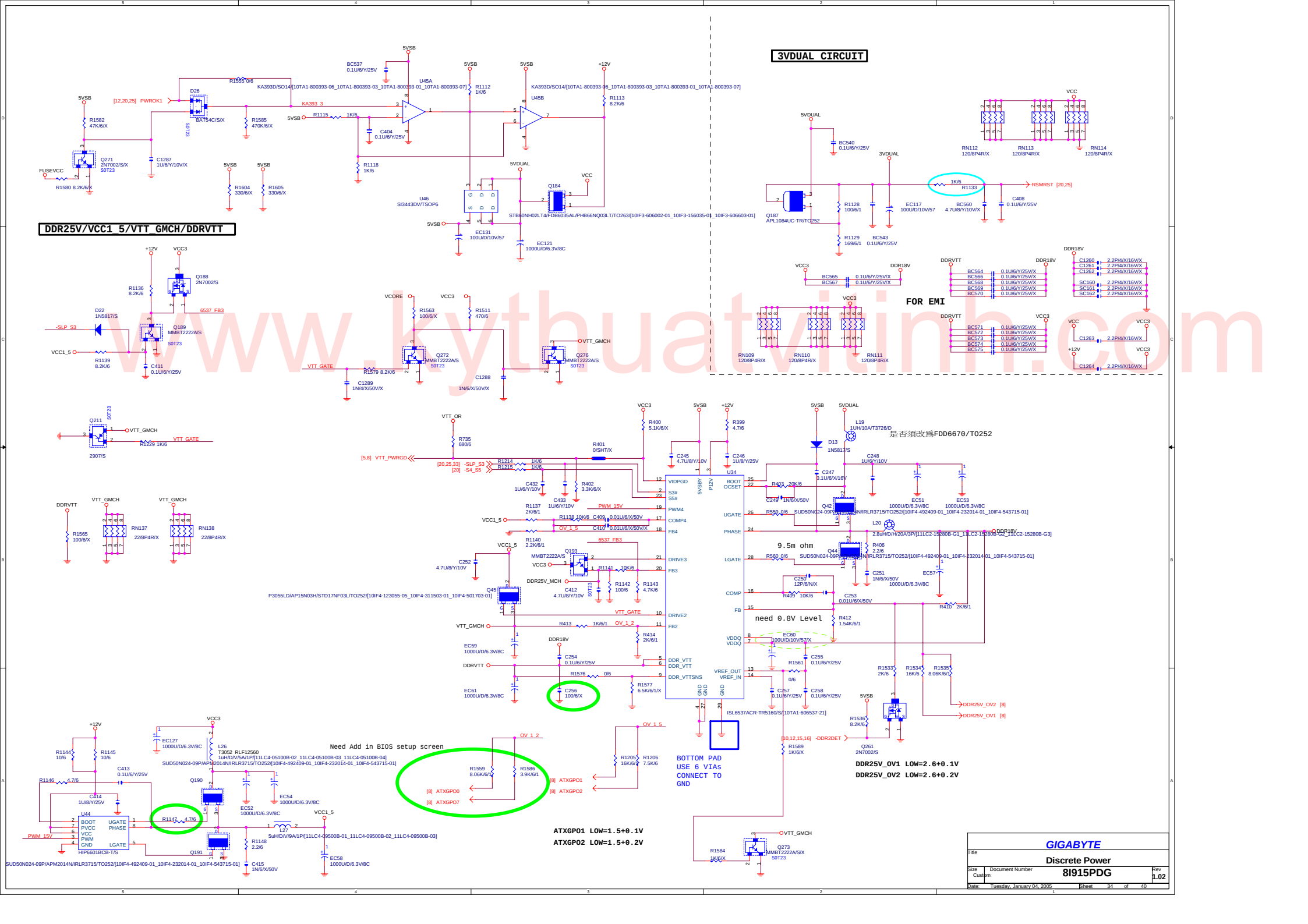
3VDUAL CIRCUIT
DDR25V/VCC1_5/VTT_GMCH/DDRVTT
FOR EMI
www.kythuatvitinh.com
Need Add in BIOS setup screen
BOTTOM PAD USE 6 VIAS CONNECT TO GND
是否须改为FDD6670/TO252
9.5m ohm
need 0.8V Level
ATXGPO1 LOW=1.5+0.1V
ATXGPO2 LOW=1.5+0.2V
DDR25V_OV1 LOW=2.6+0.1V
DDR25V_OV2 LOW=2.6+0.2V
GIGABYTE
Discrete Power
8I915PDG
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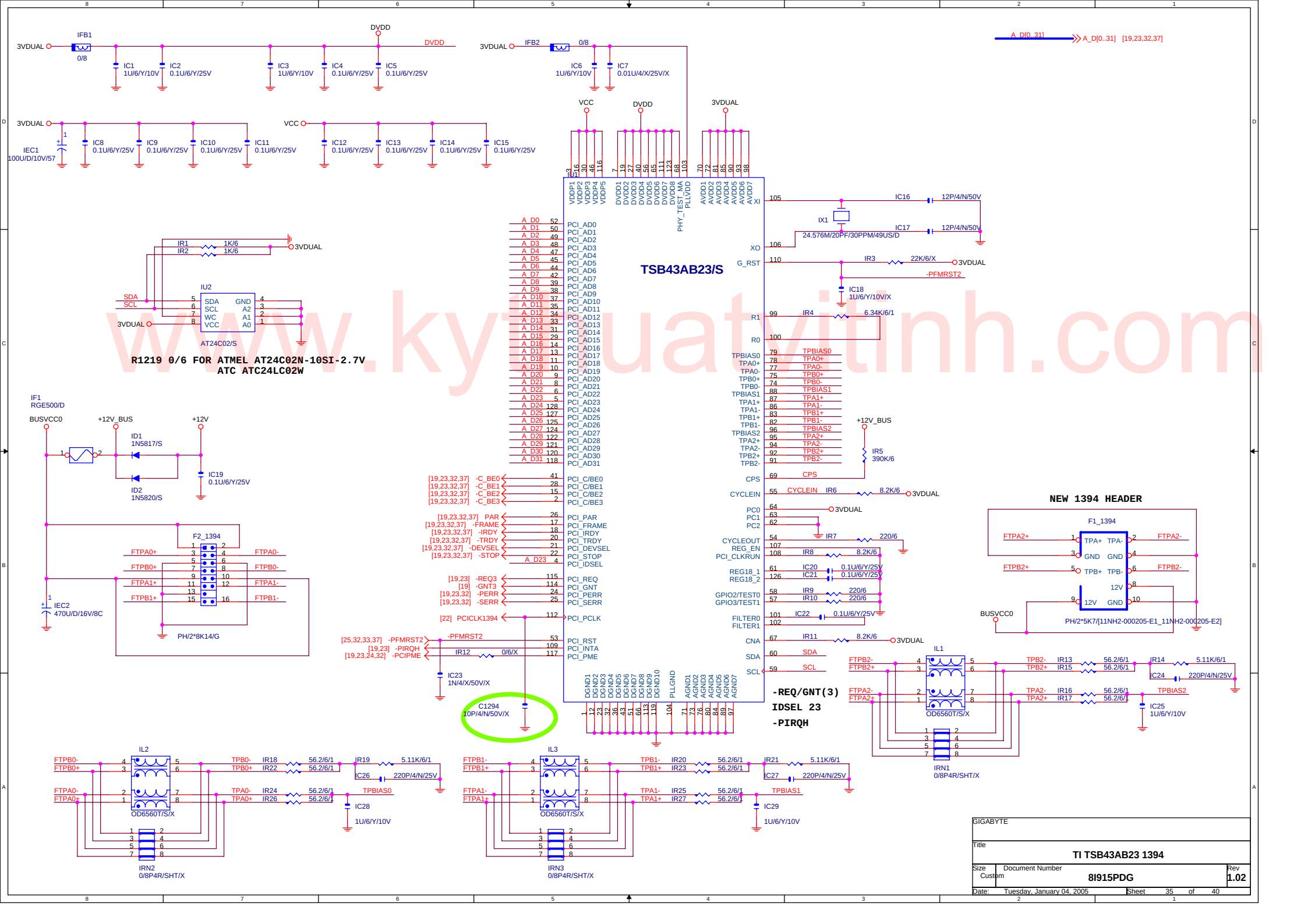
TSB43AB23/S
R1219 0/6 FOR ATMEL AT24C02N-10SI-2.7V
ATC ATC24LC02W
NEW 1394 HEADER
-REQ/GNT(3)
IDSEL 23
-PIRQH
A_D[0..31]
A_D[0..31] [19,23,32,37]
GIGABYTE
TI TSB43AB23 1394
8I915PDG
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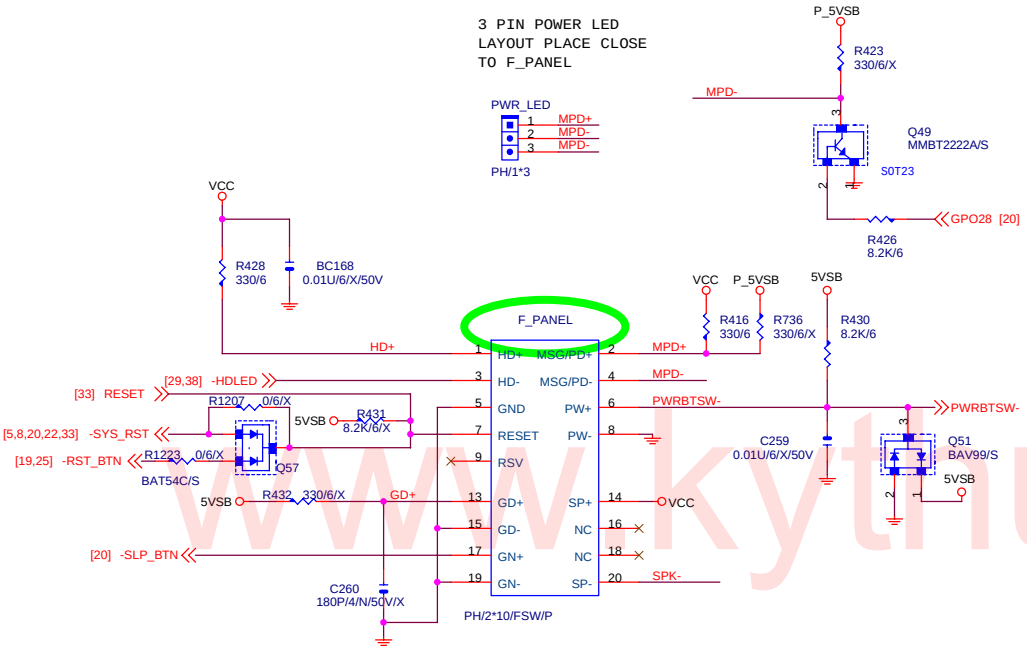
INTEL FRONT PANEL



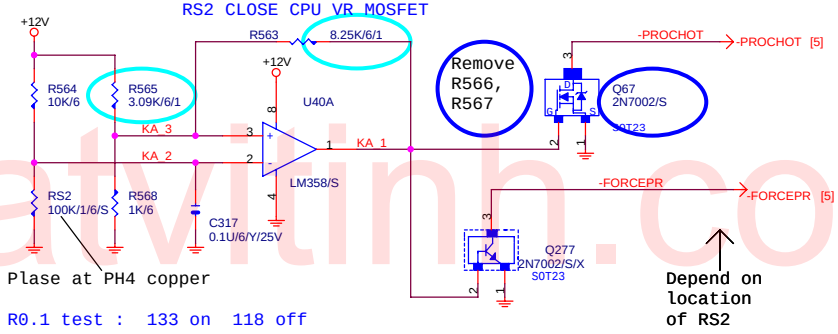
PROCESSOR HOT (N/A)

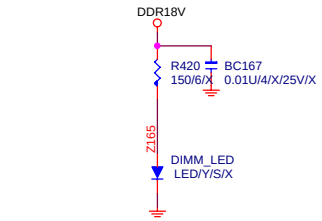
如果要用2N7002需注意OP output
Hi時的電壓是否遠大於2V。

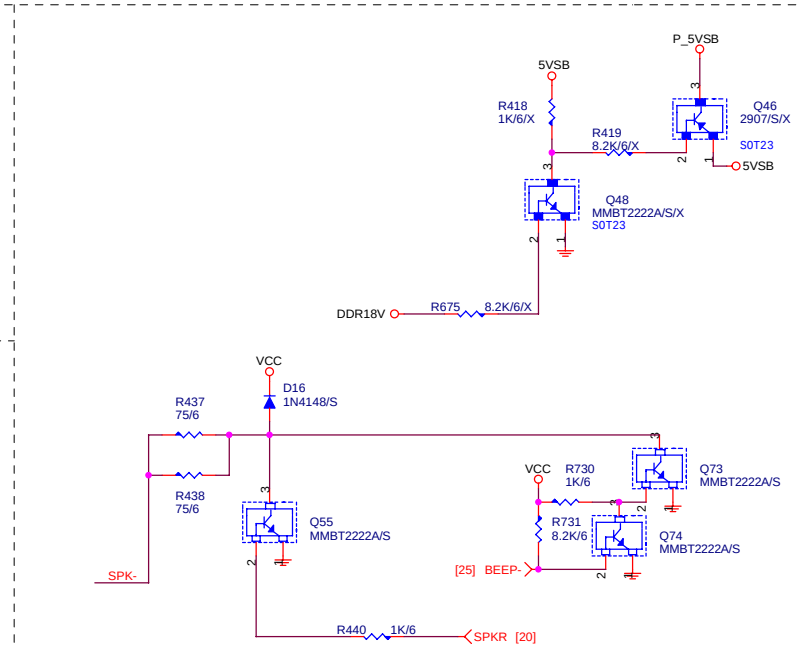
asserted at 130 degree (RS2=720 ohm)
deasserted at 115 degree (RS2=1270 ohm)

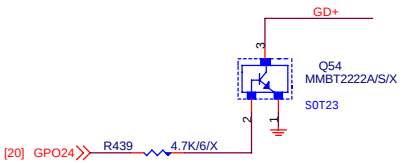
KA393改爲LM358，電源pin改接+12V，Prochot#溫度需重新調整之。

RS2 CLOSE CPU VR MOSFET









States for green LED NO1 GPO22 only S1 PROGRAMMING LOW

LED States	ACPI States	GPO28
ON	S1,S3	0
OFF	S0,S5	1

(GPO22 DEFAULT HIGH, main power)

States for a single-color power LED

LED States	ACPI States	GPO25	GPO27	GPO24
OFF	S1,S3,S5	1	1	NO1
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	B	1

LED States	ACPI States	GPO25	GPO27	GPO22
OFF	S5	1	1	X
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	B	1
Steady Yellow	S1,S3	1	0	NO1
Blinking Yellow	S1,S3(message waiting)	1	B	NO1

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Title: FRONT PANEL

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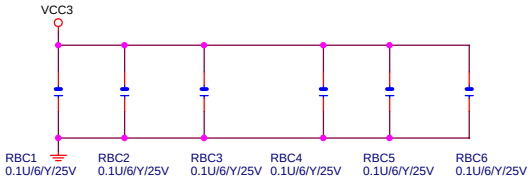
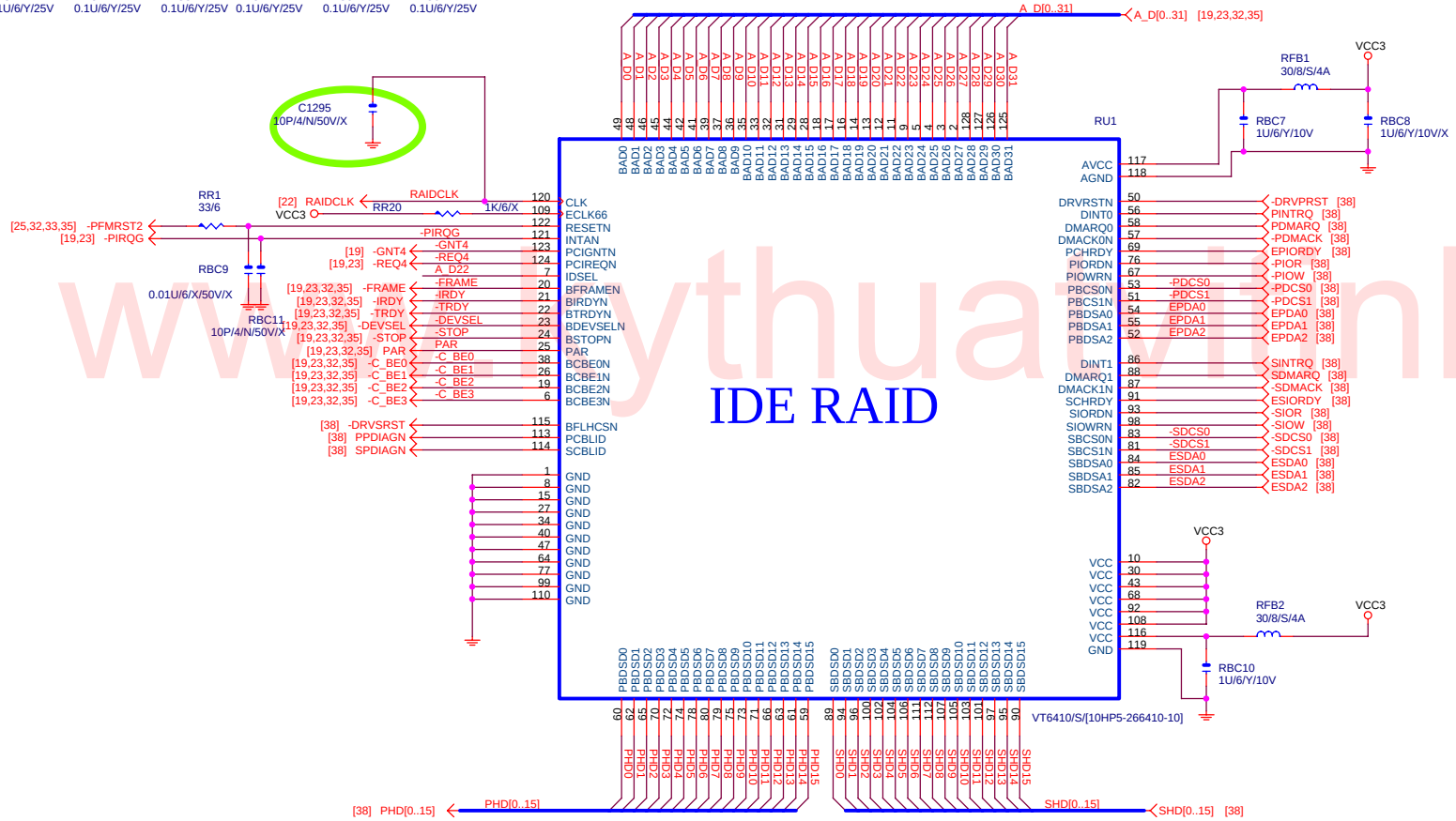
ALL INPUT PIN MUST HAVE 0.1 CAPACITOR





IDE RAID

GIGABYTE			
Title: RAID VIA 6410			
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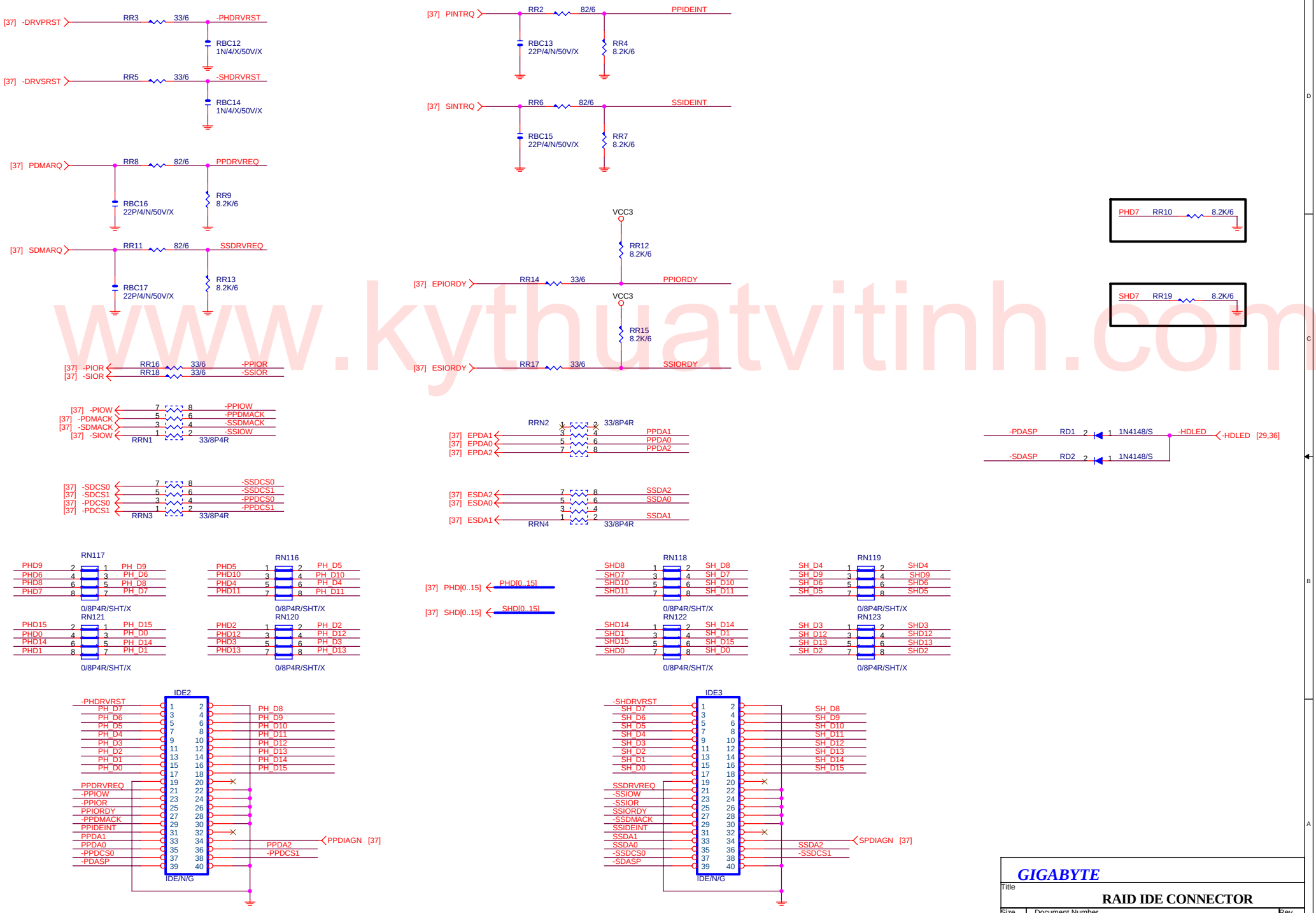

GIGABYTE

Title: RAID IDE CONNECTOR

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GPI26

INTEL ICH6 GPIO Implementation

紅字表示CPI/O 同PIN

GPI PIN

Pin Name	Pin Type	Power Well			GPIO Application
GPI[0]	Input	V5REF	-REQ[6]	(P.U VCC)	-REQ[6]
GPI[1]	Input	V5REF	-REQ[5]	(P.U VCC)	Reserved
GPI[5:2]	Input	V5REF	-PIRQ[H:E]	(P.U VCC)	PCI/LAN/NA/1394
GPI[6]	Input	VCC3	GPI[6]	(P.U VCC3)	-SLP_BTN
GPI[7]	Input	VCC3	GPI[7]	(NA)	DUALBIOS_INPUT
GPI[8]	Input	3VDUAL	GPI[8]	(P.U 3VDUAL)	-LANWAKE
GPI[10:9]	Input	3VDUAL	0C_4/5	(P.U 5VDUAL分壓)	-USBOC_R
GPI[11]	Input	3VDUAL	-SMBALERT	(P.U 3VDUAL)	-SMBALRT
GPI[12]	Input	VCC3	GPI[12]	(P.U VCC3)	ATX24_DET
GPI[13]	Input	3VDUAL	GPI[13]	(P.U 3VDUAL)	-LPCPME
GPI[15:14]	Input	3VDUAL	0C_6/7	(P.U 5VDUAL分壓)	-USBOC_R
GPO[16]	OUTPUT	VCC3	-GNT[6]	(integrated VCC3)	Reserved
GPO[17]	OUTPUT	VCC3	-GNT[5]	(integrated VCC3)	Reserved
GPO[18]	OUTPUT	VCC3	GPO[18]	(P.U VCC3)	LANRST-
GPO[19]	OUTPUT	VCC3	GPO[19]	(P.U VCC3)	DUAL_BIOS_OUTPUT
GPO[20]	OUTPUT	VCC3	GPO[20]	(P.U VCC3)	TBL-
GPO[21]	OUTPUT	VCC3	GPO[21]	(P.U VCC3)	DUAL_BIOS_OUTPUT
GPO[22]	Not Implemented		Not Implemented		Not Implemented
GPO[23]	OUTPUT	VCC3	GPO[23]	(P.U VCC3)	LANRST-
GPO[24]	IN/OUT	3VDUAL	GPO[24]	(NA)	GREEN_LED
GPO[25]	IN/OUT	3VDUAL	vcc_25vregulator	(NA)	Reserved
GPI[26]	Input	VCC3	SATA[0]GP	(P.U VCC3)	SATA[0]GP
GPIO[27]	IN/OUT	3VDUAL	GPIO[27]	(NA)	Reserved
GPIO[28]	IN/OUT	3VDUAL	GPO[28]	(NA)	PWD_LED
GPI[29]	Input	VCC3	SATA_1GP	(P.U VCC3)	SATA_1GP
GPI[30]	Input	VCC3	SATA_2GP	(P.U VCC3)	SATA_2GP
GPI[31]	Input	VCC3	SATA_3GP	(P.U VCC3)	SATA_3GP
GPIO[32]	IN/OUT	VCC3	GPO[32]	(NA)	FWP-
GPIO[33]	IN/OUT	VCC3	GPI[33]	(P.U VCC3)	-ACZ_DET
GPIO[34]	IN/OUT	VCC3	GPIO[34]	(P.U VCC3)	MB_ID0
GPI[40]	Input	V5REF	-REQ[4]	(P.U VCC)	-REQ[4]
GPI[41]	Input	VCC3	GPI[41]	(P.U VCC3)	MB_ID1
GPO[48]	OUTPUT	VCC3	-GNT[4]	(integrated VCC3)	Reserved
GPO[49]	OD O	V_CPU_IO	CPUPWROK	(P.U VTT_OR)	CPUPWROK
GP1O[35-39,42-47]	NOT IMPLEMENTED		NOT IMPLEMENTED		

GPO PIN

Pin Name	Pin Number	Power Well	Pin Type			GPIO Application

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Title	GPIO TABLE	
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ICH6 GPIO Table:

NAME	PWR LANE	USAGE	NAME	PWR LANE	USAGE
GPI0	V5REF	M/B ID (-REQ6)	GPI41	VCC3	M/B ID
GPI1	V5REF	-REQ5	GPO48	VCC3	-GNT4
GPI2	V5REF	-PIRQE	GPO49	V-CPUIO	CPUPWOK
GPI3	V5REF	-PIRQF			
GPI4	V5REF	-PIRQG			
GPI5	V5REF	-PIRQH			
GPI6	VCC3	-SLP_BTN			
GPI7	VCC3	DUAL BIOS			
GPI8	3VDAUL	-LANWAKE			
GPI9	3VDAUL	-USBOC4			
GPI10	3VDAUL	-USBOC5			
GPI11	3VDAUL	-SMBALT			
GPI12	VCC3	ATX_DET			
GPI13	3VDAUL	-LPCPME			
GPI14	3VDAUL	-USBOC6			
GPI15	3VDAUL	-USBOC7			
GPO16	VCC3	CPU OV1 (-GNT6)			
GPO17	VCC3	-GNT5			
GPO18	VCC3	CPU OV2			
GPO19	VCC3	DUAL BIOS			
GPO20	VCC3	BIOS T-BLOCK			
GPO21	VCC3	DUAL BIOS			
GPO23	VCC3	DDR OV0			
GPIO24	3VDAUL	GREEN LED			
GPIO25	3VDAUL	DDR OV1			
GPI26	VCC3	SATA_GP0			
GPIO27	3VDAUL	+PWRLED			
GPIO28	3VDAUL	-PWRLED			
GPI29	VCC3	SATA GP1			
GPI30	VCC3	SATA GP2			
GPI31	VCC3	SATA GP3			
GPIO32	VCC3	BIOS WP			
GPIO33	VCC3	AZALIA DET			
GPIO34	VCC3	M/B ID			
GPI40	V5REF	-REQ4			

PWROK/RESET Table:

ITE8712BHX PIN	NET NAME	TARGET
PIN62/-PCIRST1	-PCIE_RST	1. PCI-E * 1 Slot1 2. PCI-E * 1 Slot2 3. PCI-E * 1 Slot3 4. PCI-E * 16 Slot
PIN64/-PCIRST2	-PFMRST2	1. Onboard PCI Lan 2. Onboard 1394 Chip 3. OnBoard FWH
PIN65/-PCIRST3	-PFMRST1	1. Onboard PCI-E Lan 2. Onboard SATA Chip 3. GMCH
PIN115/-PCIRST4	-PFMRST_ -IDERST	Reserved For IDE
PIN63/PWROK1	PWROK1	1. GMCH 2. ICH6 3. 5VDUAL SWITCH 4. DPS CONTROL
PIN109/PWROK2	-THERM	1. ICH6

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Title	GPIO/RESET TABLE	
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