

Model Name: 8I915G DUO

REV1.4

SHEET	TITLE
01	COVER SHEET
02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	P4_LGA775_A
05	P4_LGA775_B
06	P4_LGA775_C
07	P4_LGA775_D
08	VCORE POWER
09	GMCH-GRANTS DALE_HOST
10	GMCH-GARNTSDALE_DDR
11	GMCH-GRANTS DALE_PCI E, DMI
12	GMCH-GRANTS DALE_INT VGA
13	GMCH-GRANTS DALE_GND
14	GMCH-GRANTS DALE_PWR
15	DDR CHANNEL A
16	DDR CHANNEL B
17	DDR TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH6 PCI, USB, DMI, LAN
20	ICH6 IDE, GPIO, SATA, CTRL
21	ICH6 VCC, GND
22	CLK GEN

SHEET	TITLE
23	PCI SLOT
24	PCI EXPRESS*1 SLOT
25	ITE8712HX
26	HWMO/FAN/FWH BIOS
27	KB_MS/GAME
28	COM/LPT/FDD
29	(FRONT+REAR)USB/RING/IDE
30	AZALIA CODEC ALC880/CMI9880
31	AUDIO JACK
32	LAN BCM5705E/5751
33	LAN BCM5751
34	ATX POWER CONN.
35	ALL POWER
36	1394 TSB43AB23
37	FRONT PANEL/BZ
38	RAID VIA6410
39	RAID IDE CONNECTOR
40	GPIO TABLE
41	RESET TABLE

 COMPONENT SIDE
 (1 oz. Copper)
 VCC SIDE
 (1 oz. Copper)
 GND SIDE
 (1 oz. Copper)
 SOLDER SIDE
 (1 oz. Copper)

GIGABYTE		
Cover Sheet		
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BLOCK DIAGRAM

**INTEL Pentium4
LGA775**

VCCORE = 1.75V / SLEEP: 1.3V
VCC3

PAGE 4, 5, 6, 7

PWM/OTHER POWER

VCCORE = 1.75V (650-1100MHZ) / SLEEP: 1.3V
5VSB-12V,+12V,VCC,VCC3,DUAL
VTT_DDR2-5VSTR

PAGE 8, 34, 35

CHANNEL A
DDRII DIMM X 1
DDRI DIMM X 1

2.5VSTR = 2.5V(MEMORY,SUSPEND POWER)
VTT_DDR = 1.25V

PAGE 15, 17

CHANNEL B
DDRII DIMM X 1
DDRI DIMM X 1

2.5VSTR = 2.5V(MEMORY,SUSPEND POWER)
VTT_DDR = 1.25V

PAGE 16, 17

**GMCH
GRANTS DALE**

VCCORE = 1.75V / SLEEP: 1.3V
2.5VSTR = 2.5V(MEMORY)
VDDQ = 1.5V (AGP POWER 4X, HUBLINK)

PAGE 9, 10, 11, 12, 13, 14

MAA0-14
MAA_CPC1-5
MAB_CPC1-5
MDD0-63
-DQSD0-7
DM0-7

GAD0-31
ADSTB0,ADSTB0-
ADSTB1,ADSTB1-
SBA0-7
SBSTB,SBSTB-
GCBE0-3-
ST0-2

CLOCK GENERATOR

CKVDD = 3.3V

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**PCI EXPRESS
BY 16 PORTS**

VCC3 = 1.5V (ASP POWER 4X)
VCC3 = 3.3V
+12V = 12V
3VDUAL = 3.3V
VCC = 5V

PAGE 18

USB PORTS 0~7


VCC = 5V
5VSB = 5V
5VUSB = 5V

PAGE 29

ICH6

VCC25 = 2.5V(I/O, MEMORY, VLINK)
3DUAL = 3.3V(SUSPEND POWER)
VCC3 = 3.3V
RTCVDD = 3.3V

PAGE 19, 20, 21

HLO-10
CONTROL BUS  HUB LINK

IDE Primary

VCC = 5V

PAGE 29

SERIAL ATA

VCC = 5V

PAGE 20

FWH/HWMO

VCC = 5V
VCC3 = 3V

PAGE 26

LPC ITE8712HX

VCC = 5V
5VSB = 5V
VBAT = 3V

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I/O PORTS :
COMA COMB LPT PS2 IR FDD

PAGE 27, 28, 29

AZALIA
LINK

PCI BUS

LPC BUS

**AC97/Azalia
ALC880/CMI9880**

+12V = 12V
VCC3 = 3.3V
VCC = 5V
AVDD = 5V

PAGE 30

AUDIO PORTS : FRONT AUDIO
LIN_ OUT LINE_IN MIC
TELE CD_IN AUX_IN

PAGE 31

FRONT PANEL/BZ

VCC = 5V
5VSB = 5V
+12V = 12V
PVCC = 5V

PAGE 37

**PCI SLOT
PCI EXPRESS SLOT**

+12 = 12V
+12 = 12V
VCC = 5V
VCC3 = 3V
3VDUAL = 3V

PAGE 23, 24

LAN BCM5721/5751

PAGE 32, 33

1394 IT TSB43AB23

PAGE 36

RAID VIA6410

PAGE 38, 39

Model Name: 8I915G DUO

Version: 1.4

Component value change history

2004/05/19

Data	Change Item	Reason
0317	ADD 2ND SOURCE	*** 更換 *** 新舊線路中 元件值不同 *** L10由 10H/8/180mA/S(10L12-07100B-01/10L12-041001-04)變為 10H/8/180mA/S(10L12-07100B-01/10L12-041001-04) L15由 10H/8/180mA/S(10L12-07100B-01/10L12-041001-04)變為 10H/8/180mA/S(10L12-07100B-01/10L12-041001-04) Q190由 SUD50N024-09P/APM2014N/IRLR3715/TO252變為 10IF4-083918-01R_10IF4-492409-01R_10IF4-098880-10R/TO252 Q191由 SUD50N024-09P/APM2014N/IRLR3715/TO252變為 10IF4-083918-01R_10IF4-492409-01R_10IF4-098880-10R/TO252 Q42由 SUD50N024-09P/TO252變為 10IF4-083918-01R_10IF4-492409-01R_10IF4-098880-10R/TO252 Q44由 SUD50N024-09P/TO252變為 10IF4-083918-01R_10IF4-492409-01R_10IF4-098880-10R/TO252
	LIB CHANGE	*** 更換 *** 新舊線路中 元件值不同 *** DL2由 0.6uH/D/30A/5018/3PW/(TAI/EMC)變為 0.6uH/TO-5018/40A/1P/[11LC5-40600C-D1] DL3由 0.6uH/D/30A/5018/3PW/(TAI/EMC)變為 0.6uH/TO-5018/40A/1P/[11LC5-40600C-D1] DL4由 0.6uH/D/30A/5018/3PW/(TAI/EMC)變為 0.6uH/TO-5018/40A/1P/[11LC5-40600C-D1] DL5由 0.6uH/D/30A/5018/3PW/(TAI/EMC)變為 0.6uH/TO-5018/40A/1P/[11LC5-40600C-D1] L1由 10UH/8/100mA/S(10L12-00100A-01/03)變為 10UH//120M/8/S/[10L12-12100A-01_10L12-12100A-02_10L12-12100A-03] L2由 10UH/8/100mA/S(10L12-00100A-01/03)變為 10UH//120M/8/S/[10L12-12100A-01_10L12-12100A-02_10L12-12100A-03]
0401	Q187 ADD 2ND SOURCE	10GL6-501085-01R
0407	N/B VERSION CHANGE TO C2	10HB1-032940-61

Circuit or PCB layout change for next version

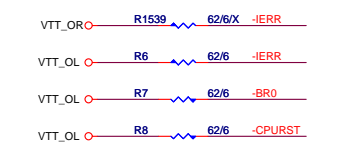
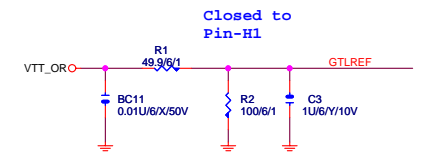
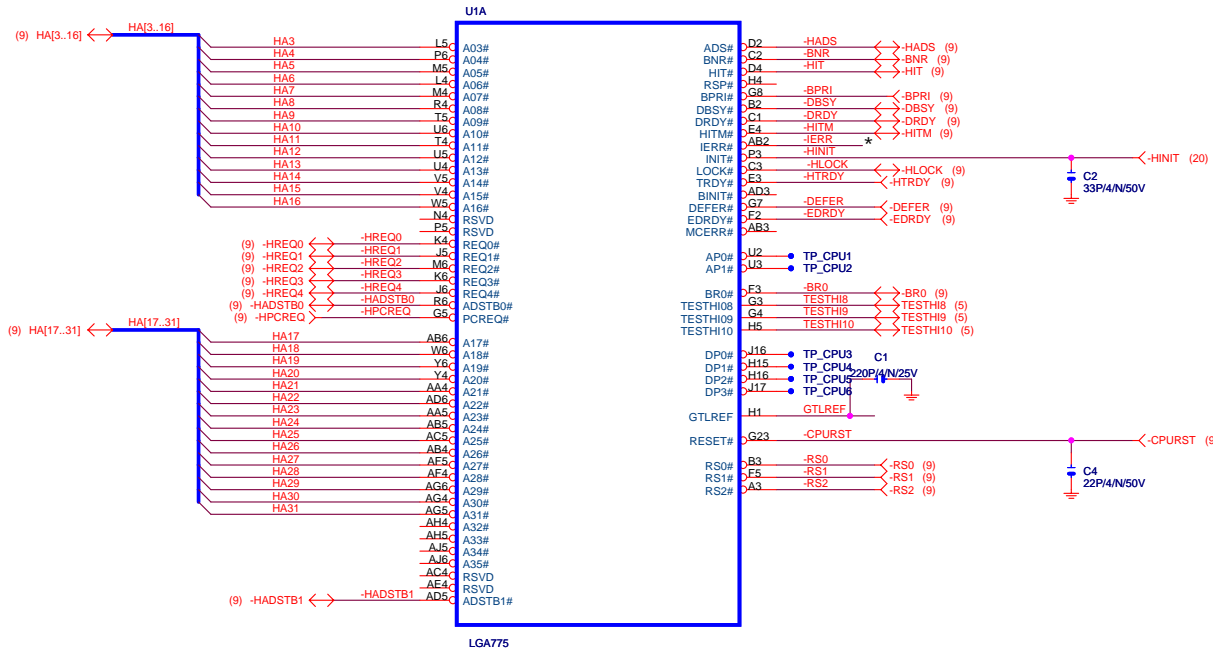
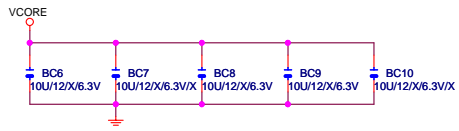
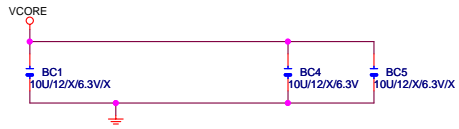
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0317	LIB CHANGE	

GIGABYTE

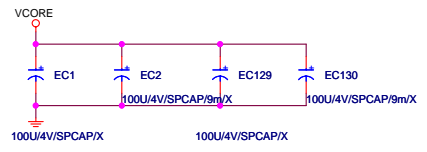
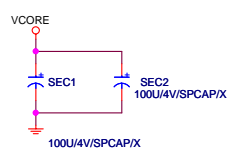
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Size Custom: Document Number **8I915G DUO** Rev **1.4**

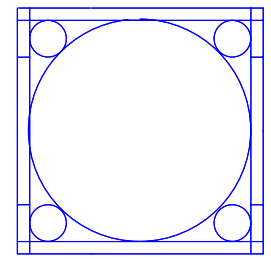
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SP-CAP X 4PCS

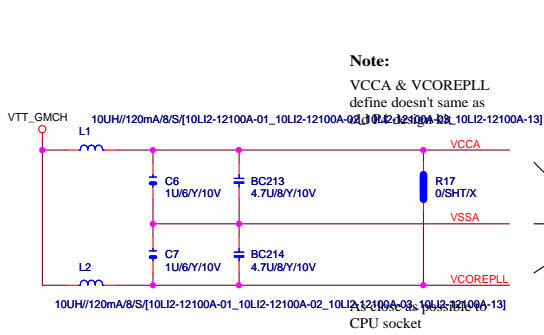


CR CPU RETAINION/X

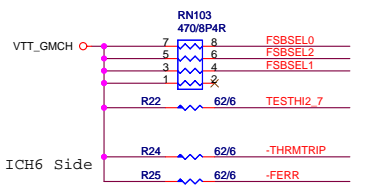
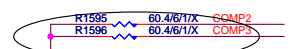
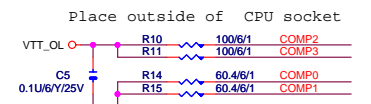
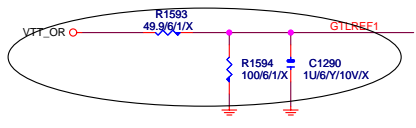
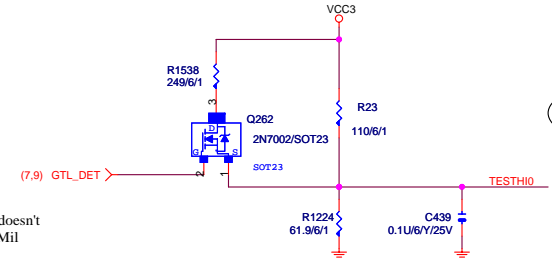
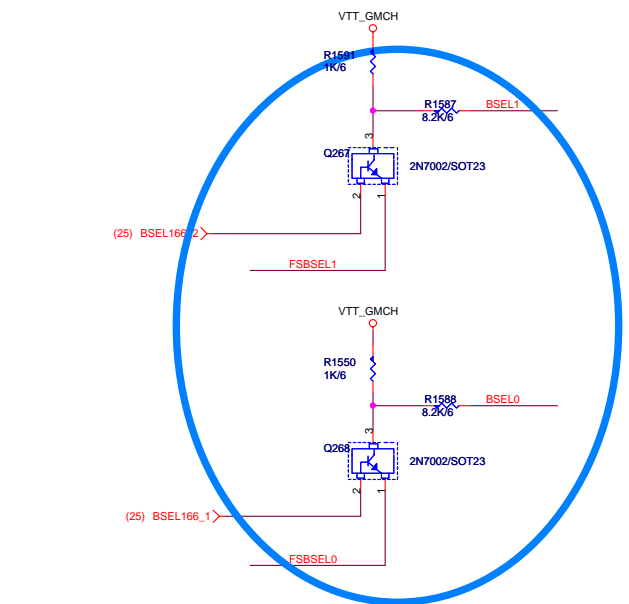
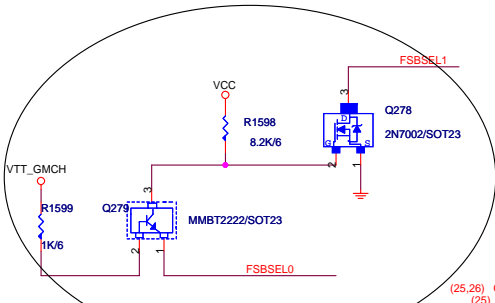


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Size Custom	Document Number	8I915G DUO	
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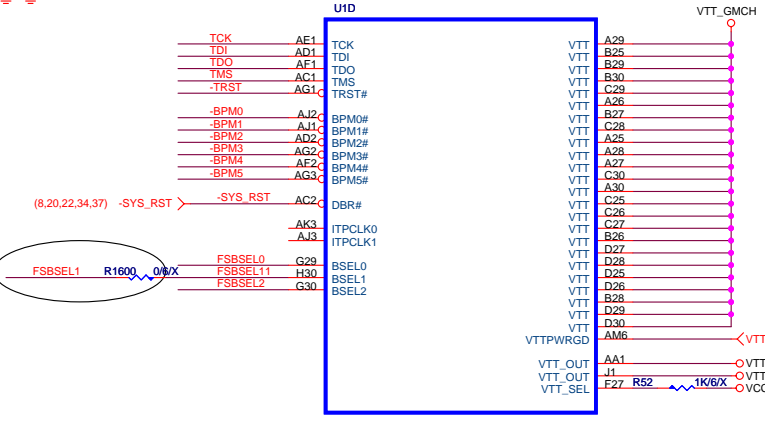
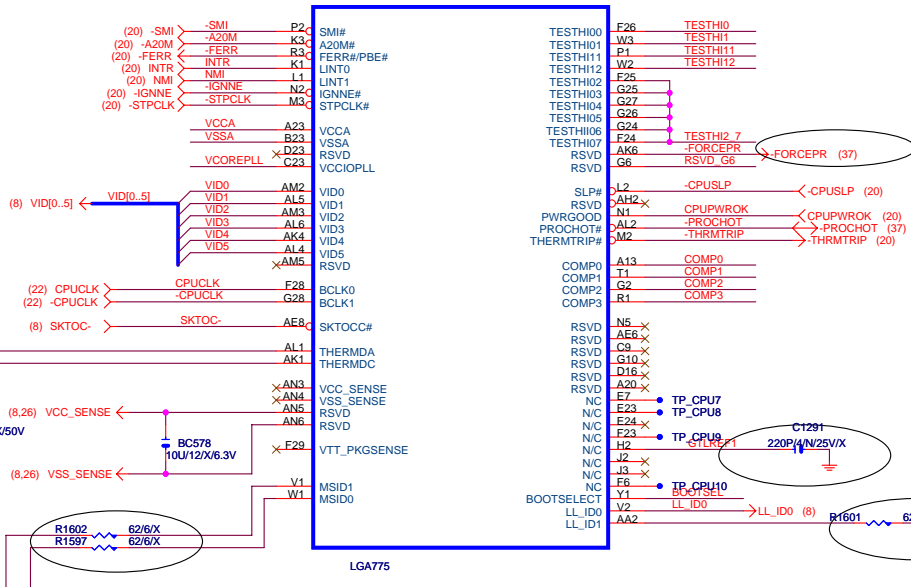
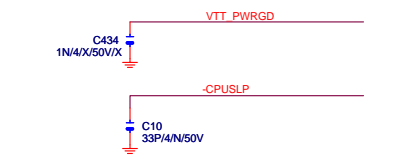
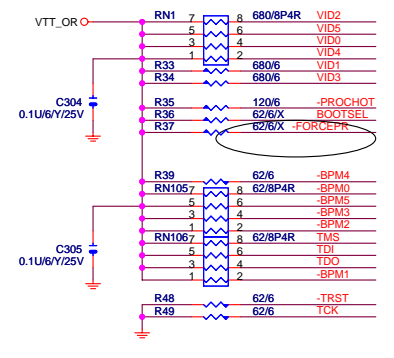
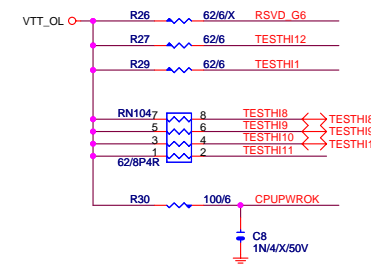
Note:
VCCA & VCOREPLL
define doesn't same as
CPU socket



Trace width doesn't
less than 12 Mil



Locate at ICH6 Side

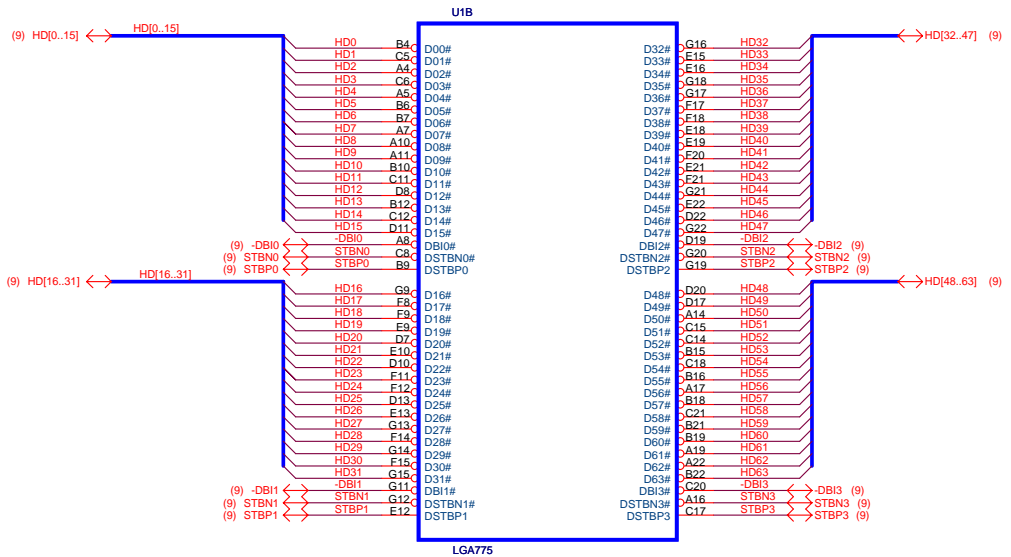


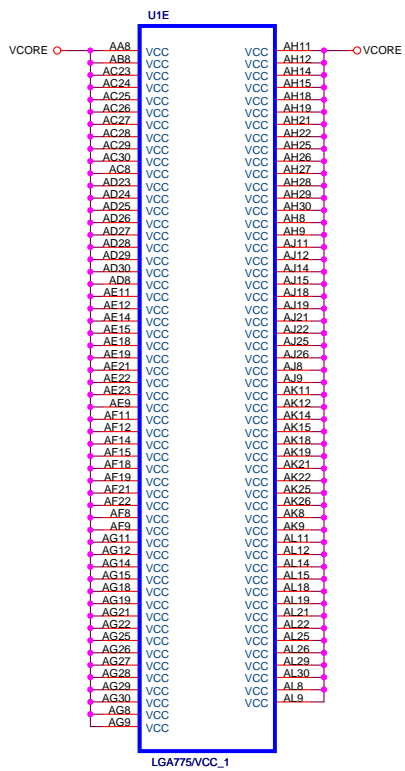
GIGABYTE

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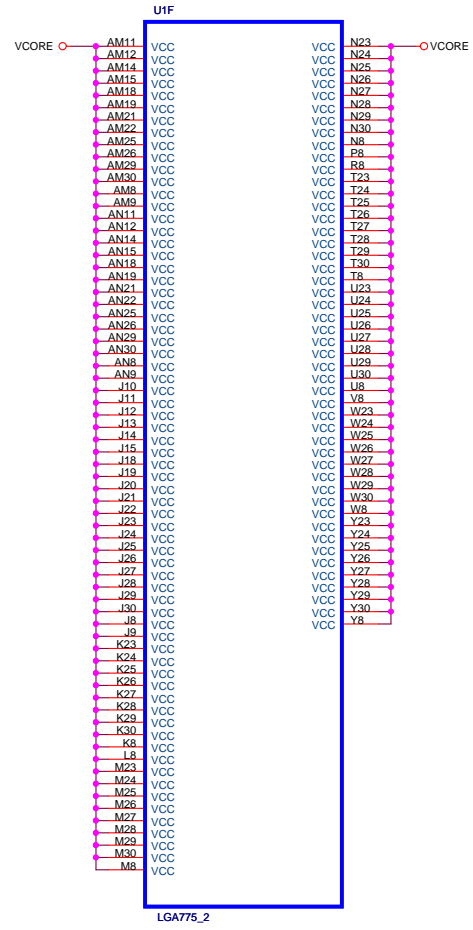
Size Custom: Document Number **81915G DUO** Rev **1.4**

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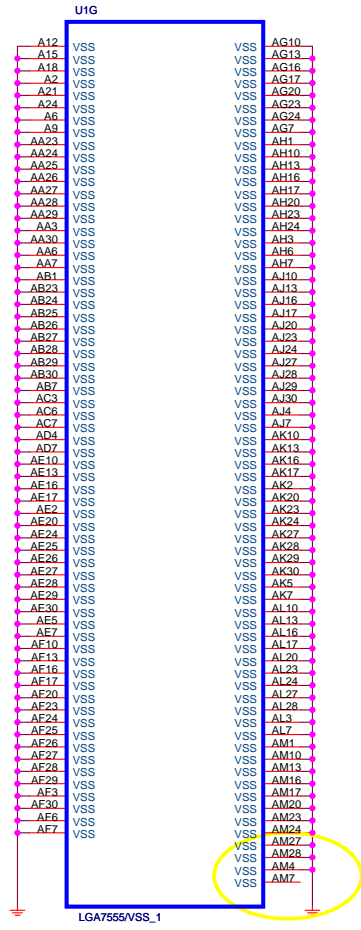




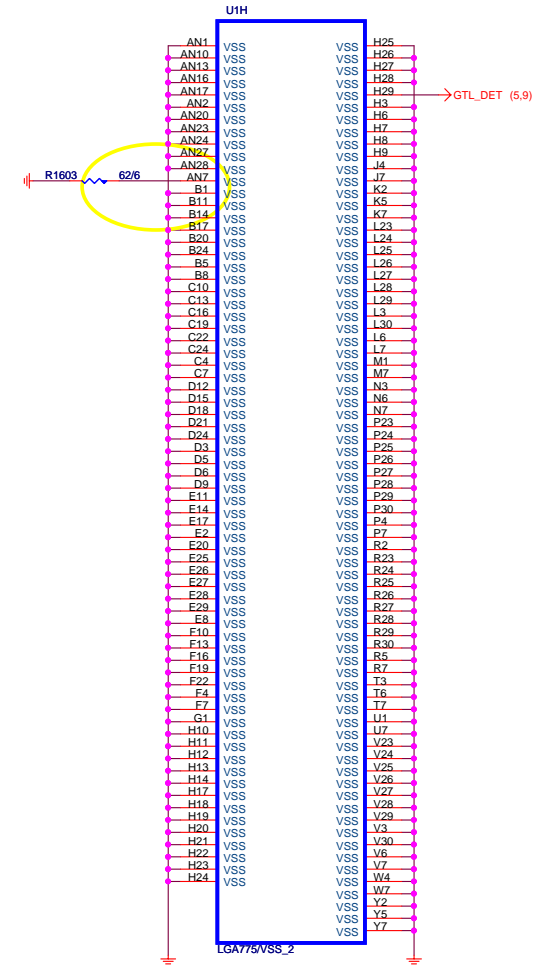
LGA775VCC_1



LGA775_2



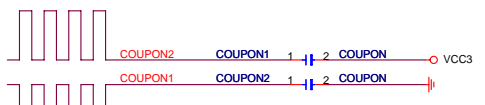
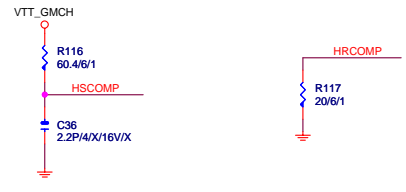
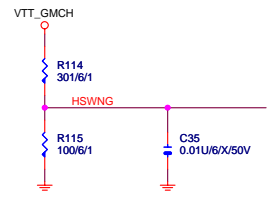
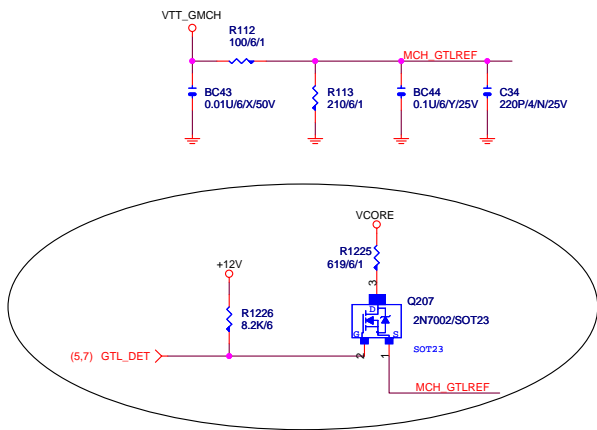
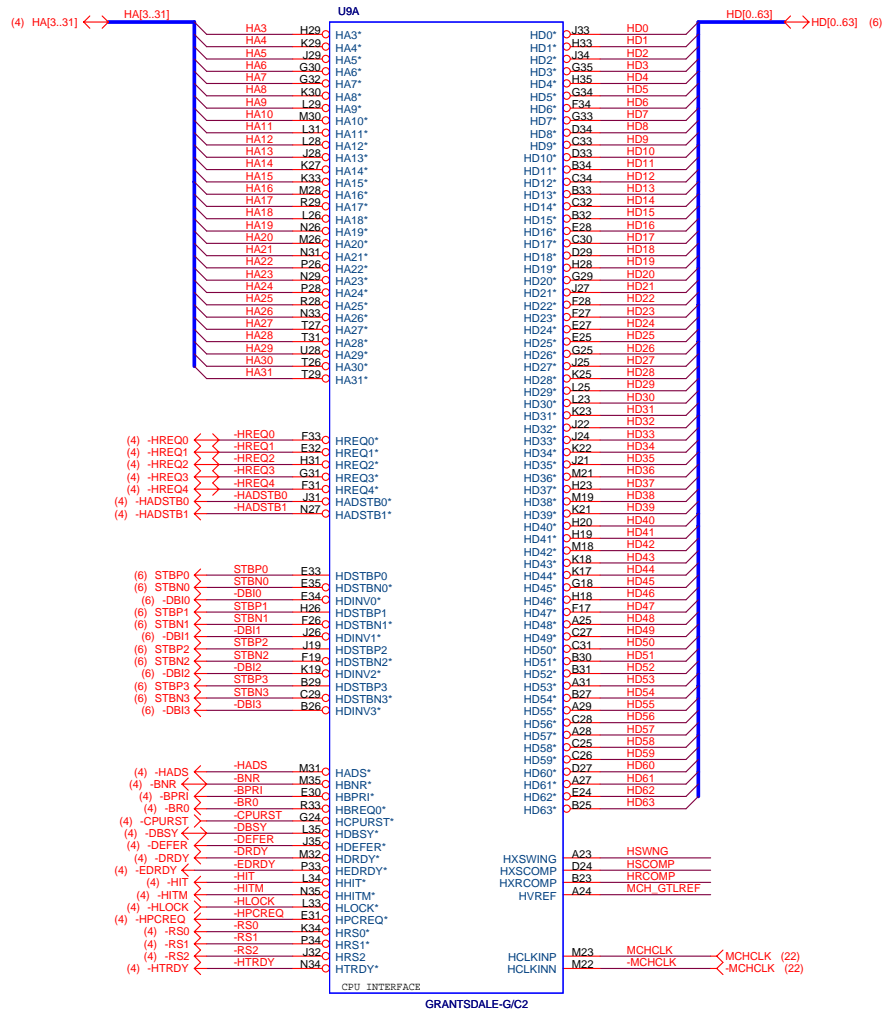
LGA755VSS_1



LGA775VSS_2

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Title			
P4_LGA775-D			
Size	Document Number	81915G DUO	
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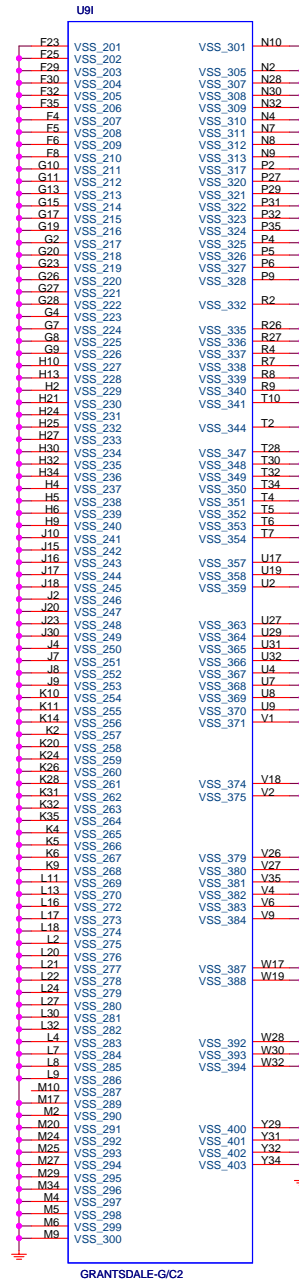
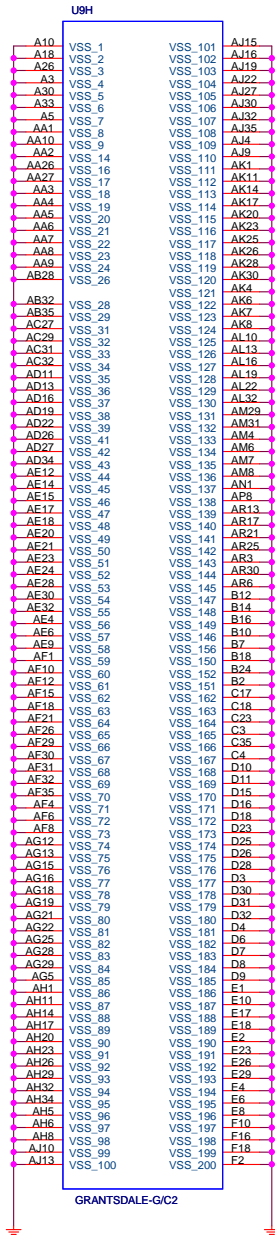


GIGABYTE			
Title GMCH-HOST			
Size Custom	Document Number 8I915G DUO	Rev 1.4	
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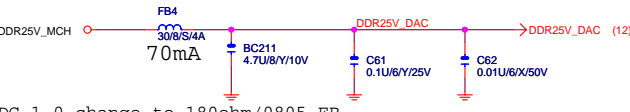
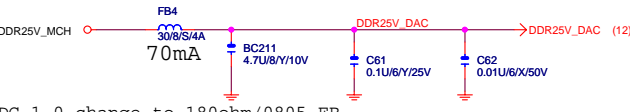
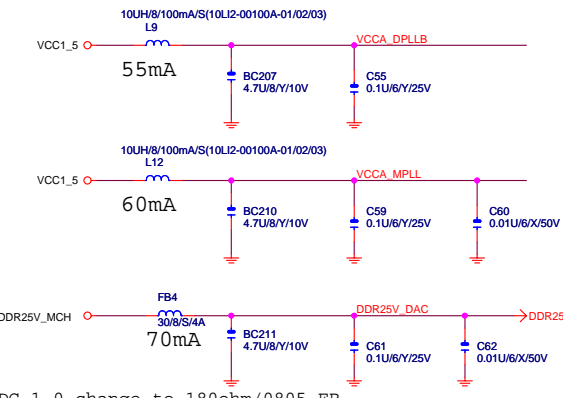
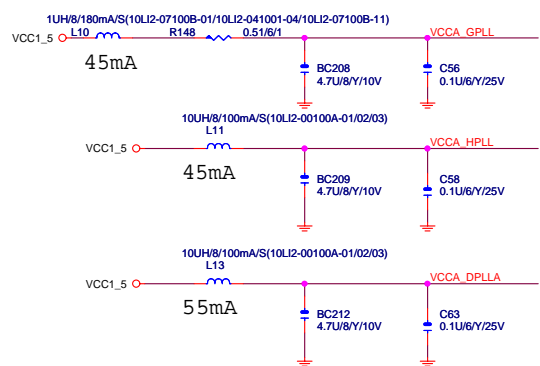
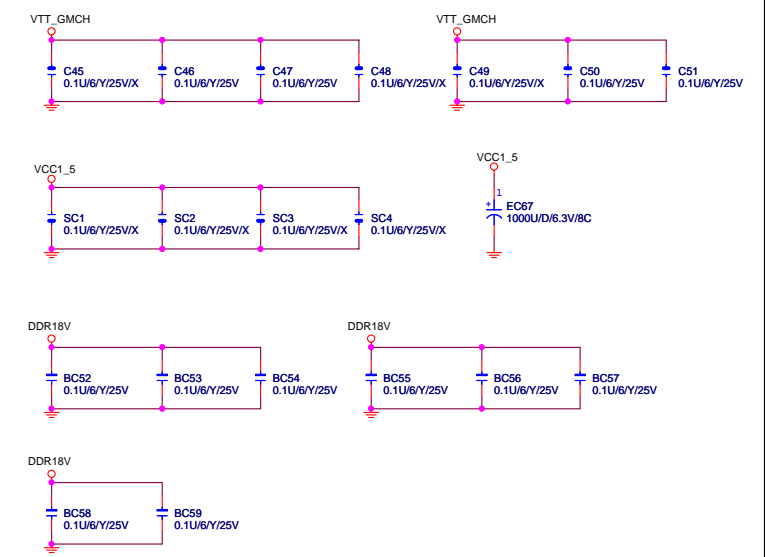
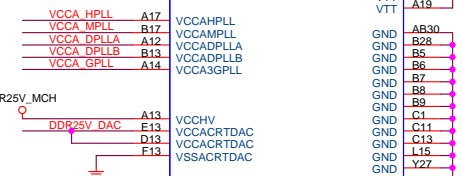
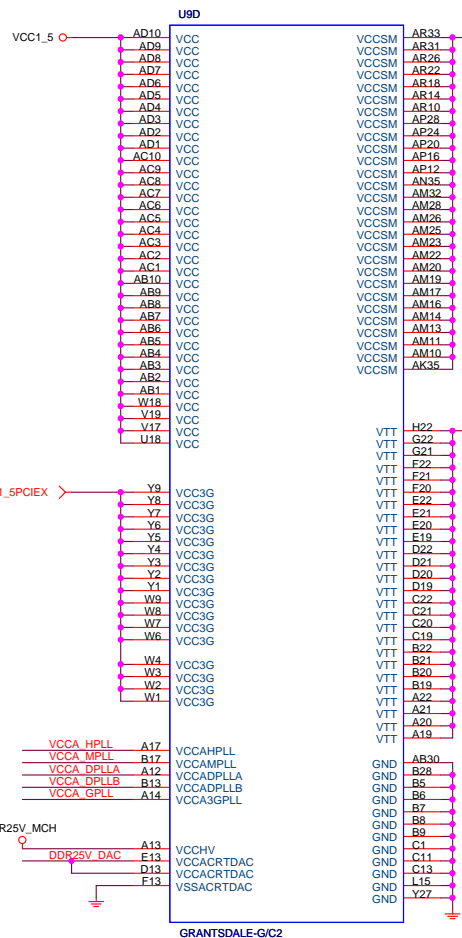


For DVO Function

GIGABYTE		
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Size Custom	Document Number 8I915G DUO	Rev 1.4
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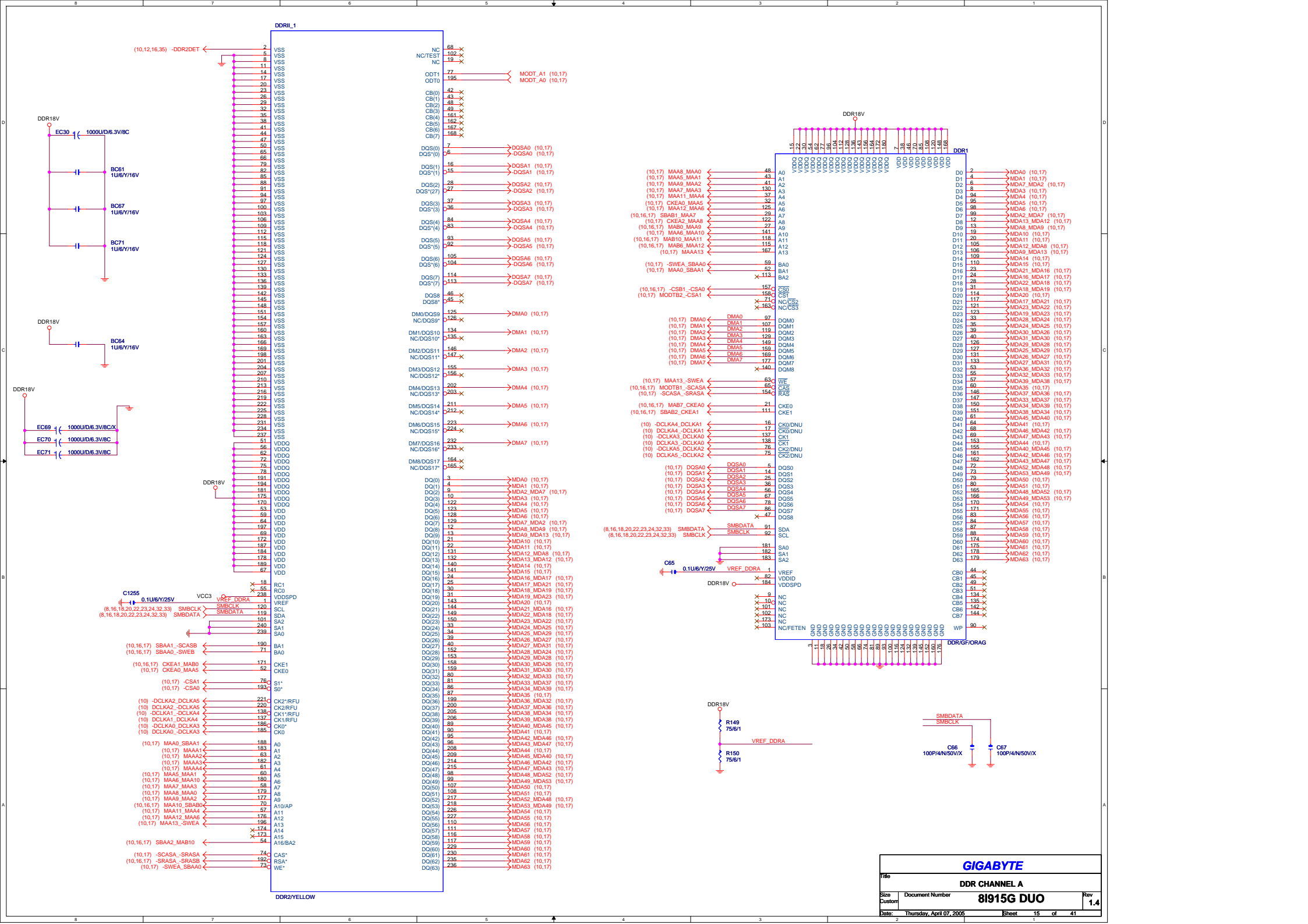


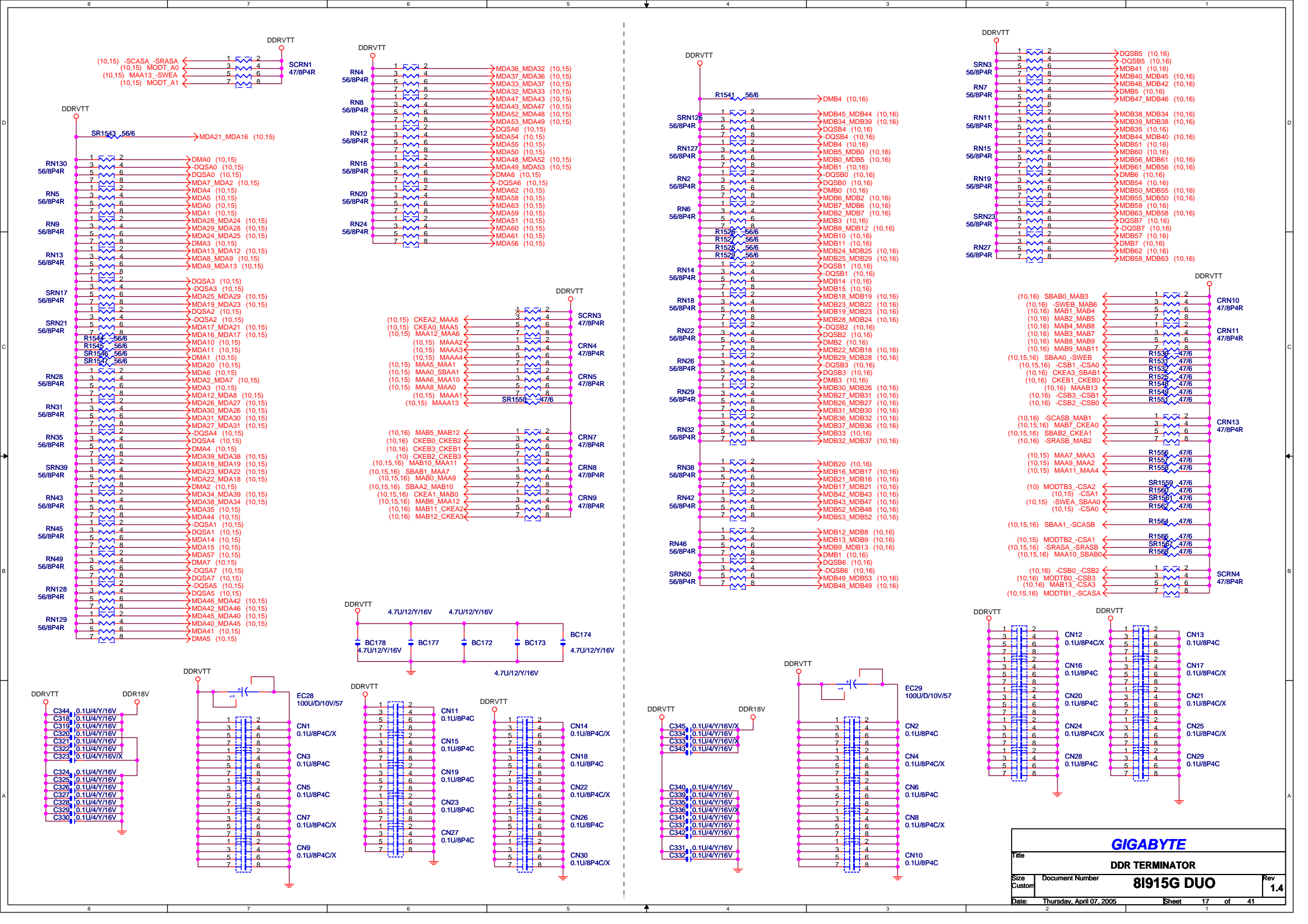
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Size Custom	Document Number	81915G DUO	
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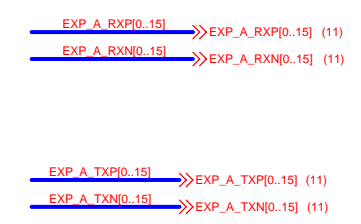
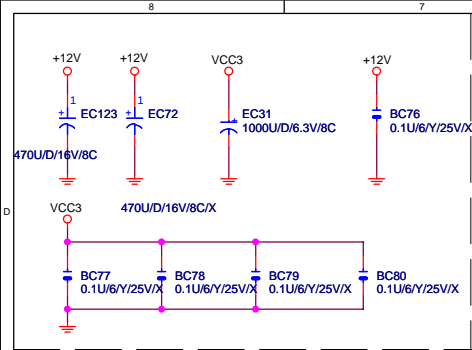


DG 1.0 change to 180ohm/0805 FB

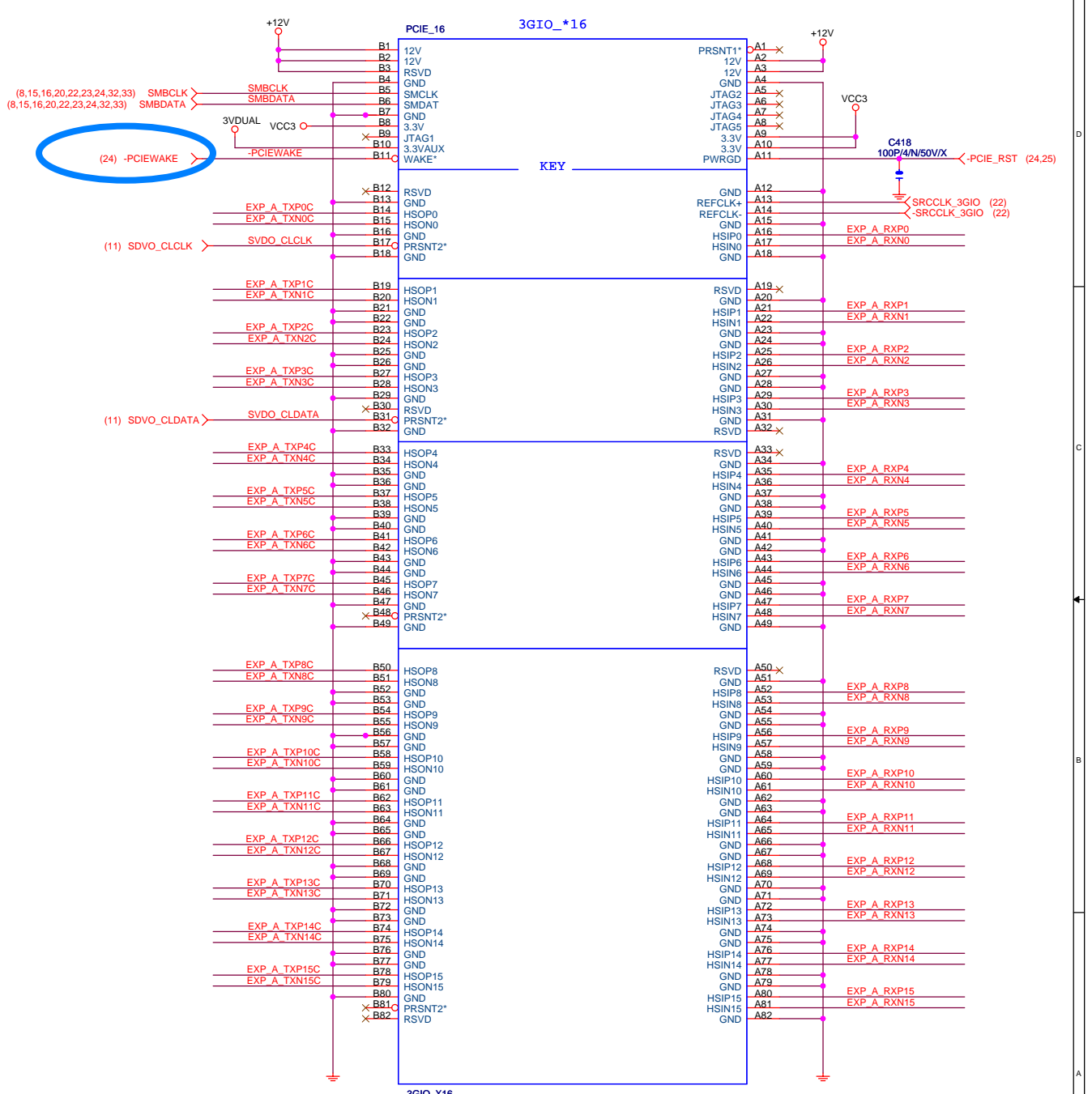
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Title	GMCH-PWR		
Size Custom	Document Number	81915G DUO	
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EXP_A_TXP0	C70	0.1U/6/Y/25V	EXP_A_TXP0C
EXP_A_TXN0	C71	0.1U/6/Y/25V	EXP_A_TXN0C
EXP_A_TXP1	C72	0.1U/6/Y/25V	EXP_A_TXP1C
EXP_A_TXN1	C73	0.1U/6/Y/25V	EXP_A_TXN1C
EXP_A_TXP2	C74	0.1U/6/Y/25V	EXP_A_TXP2C
EXP_A_TXN2	C75	0.1U/6/Y/25V	EXP_A_TXN2C
EXP_A_TXP3	C76	0.1U/6/Y/25V	EXP_A_TXP3C
EXP_A_TXN3	C77	0.1U/6/Y/25V	EXP_A_TXN3C
EXP_A_TXP4	C78	0.1U/6/Y/25V	EXP_A_TXP4C
EXP_A_TXN4	C79	0.1U/6/Y/25V	EXP_A_TXN4C
EXP_A_TXP5	C80	0.1U/6/Y/25V	EXP_A_TXP5C
EXP_A_TXN5	C81	0.1U/6/Y/25V	EXP_A_TXN5C
EXP_A_TXP6	C82	0.1U/6/Y/25V	EXP_A_TXP6C
EXP_A_TXN6	C83	0.1U/6/Y/25V	EXP_A_TXN6C
EXP_A_TXP7	C84	0.1U/6/Y/25V	EXP_A_TXP7C
EXP_A_TXN7	C85	0.1U/6/Y/25V	EXP_A_TXN7C
EXP_A_TXP8	C86	0.1U/6/Y/25V	EXP_A_TXP8C
EXP_A_TXN8	C87	0.1U/6/Y/25V	EXP_A_TXN8C
EXP_A_TXP9	C88	0.1U/6/Y/25V	EXP_A_TXP9C
EXP_A_TXN9	C89	0.1U/6/Y/25V	EXP_A_TXN9C
EXP_A_TXP10	C90	0.1U/6/Y/25V	EXP_A_TXP10C
EXP_A_TXN10	C91	0.1U/6/Y/25V	EXP_A_TXN10C
EXP_A_TXP11	C92	0.1U/6/Y/25V	EXP_A_TXP11C
EXP_A_TXN11	C93	0.1U/6/Y/25V	EXP_A_TXN11C
EXP_A_TXP12	C94	0.1U/6/Y/25V	EXP_A_TXP12C
EXP_A_TXN12	C95	0.1U/6/Y/25V	EXP_A_TXN12C
EXP_A_TXP13	C96	0.1U/6/Y/25V	EXP_A_TXP13C
EXP_A_TXN13	C97	0.1U/6/Y/25V	EXP_A_TXN13C
EXP_A_TXP14	C98	0.1U/6/Y/25V	EXP_A_TXP14C
EXP_A_TXN14	C99	0.1U/6/Y/25V	EXP_A_TXN14C
EXP_A_TXP15	C100	0.1U/6/Y/25V	EXP_A_TXP15C
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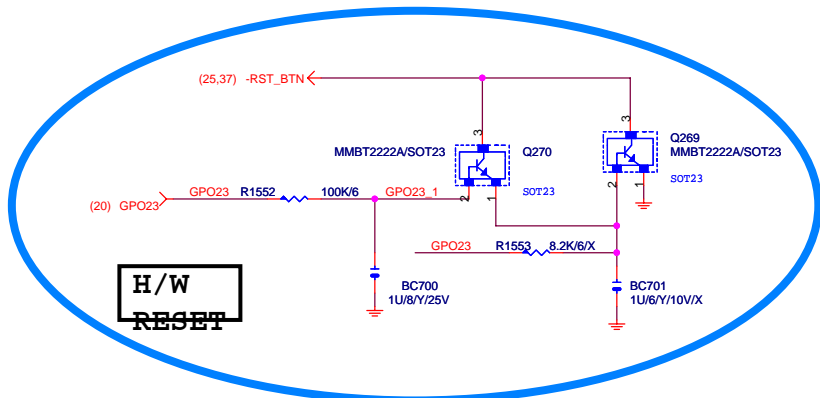


GIGABYTE

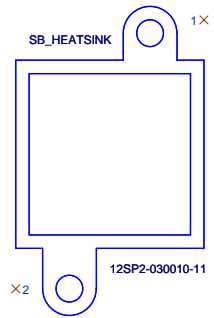
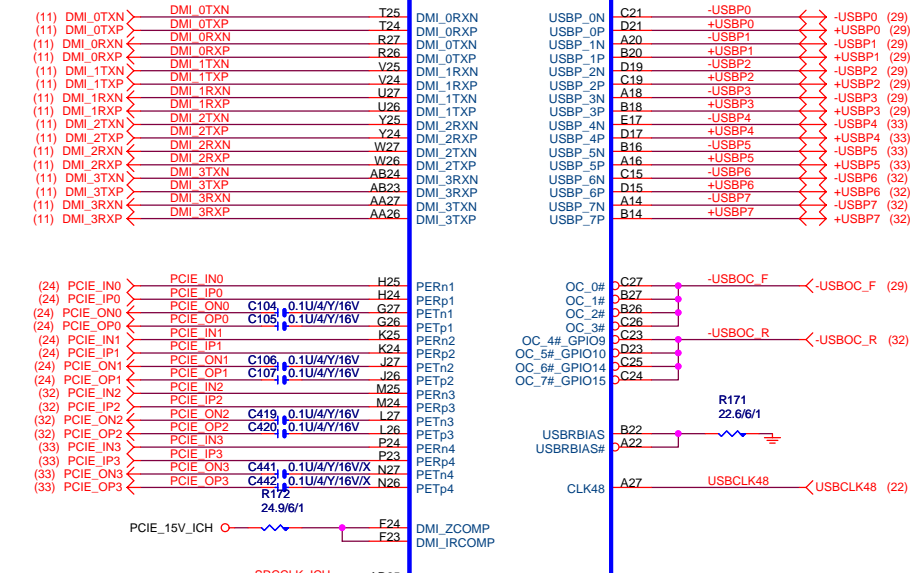
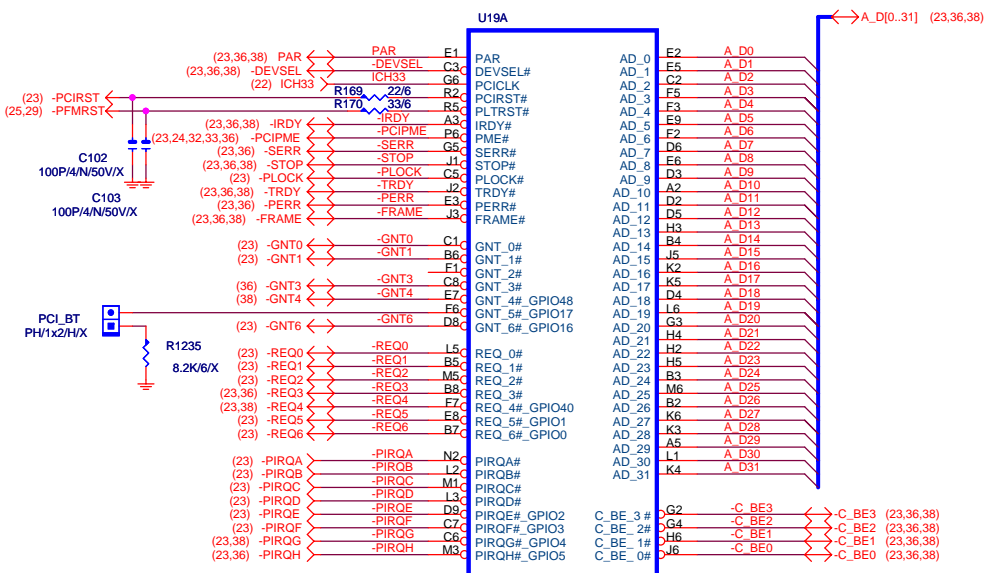
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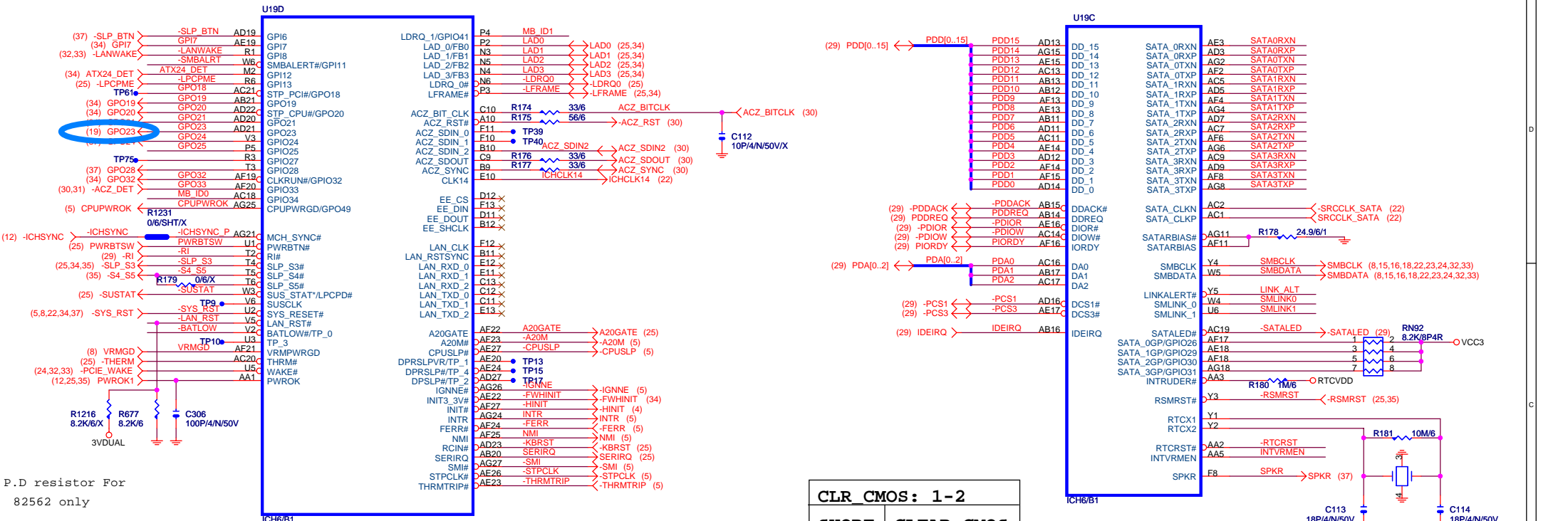
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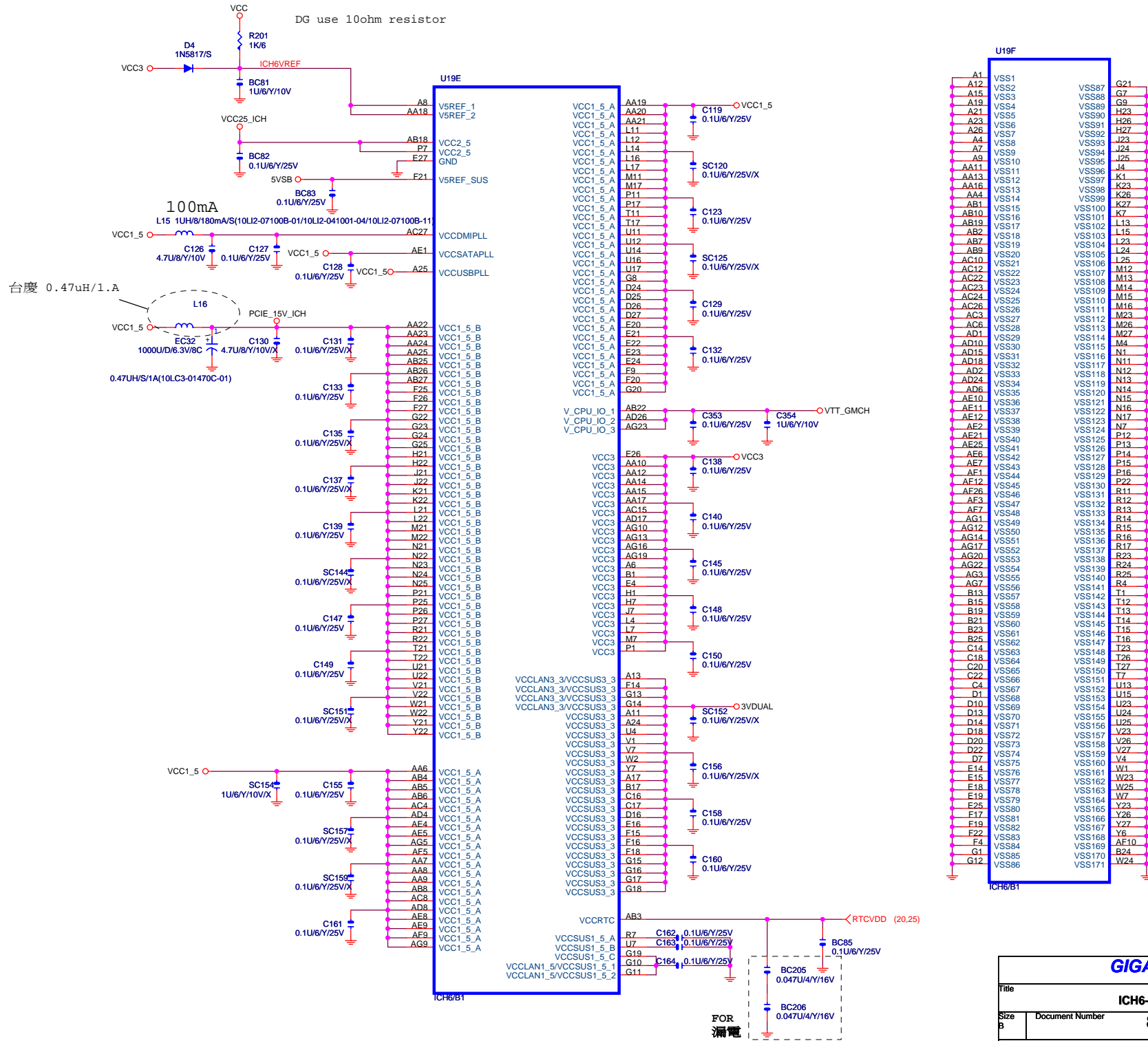
Date: Thursday, April 07, 2005 Sheet: 18 of 41



DMI Connection Note
 GMCH TX Pin Need Connect to ICH6 RX Pin
 ICH6 TX Pin Need Connect to GMCH RX Pin



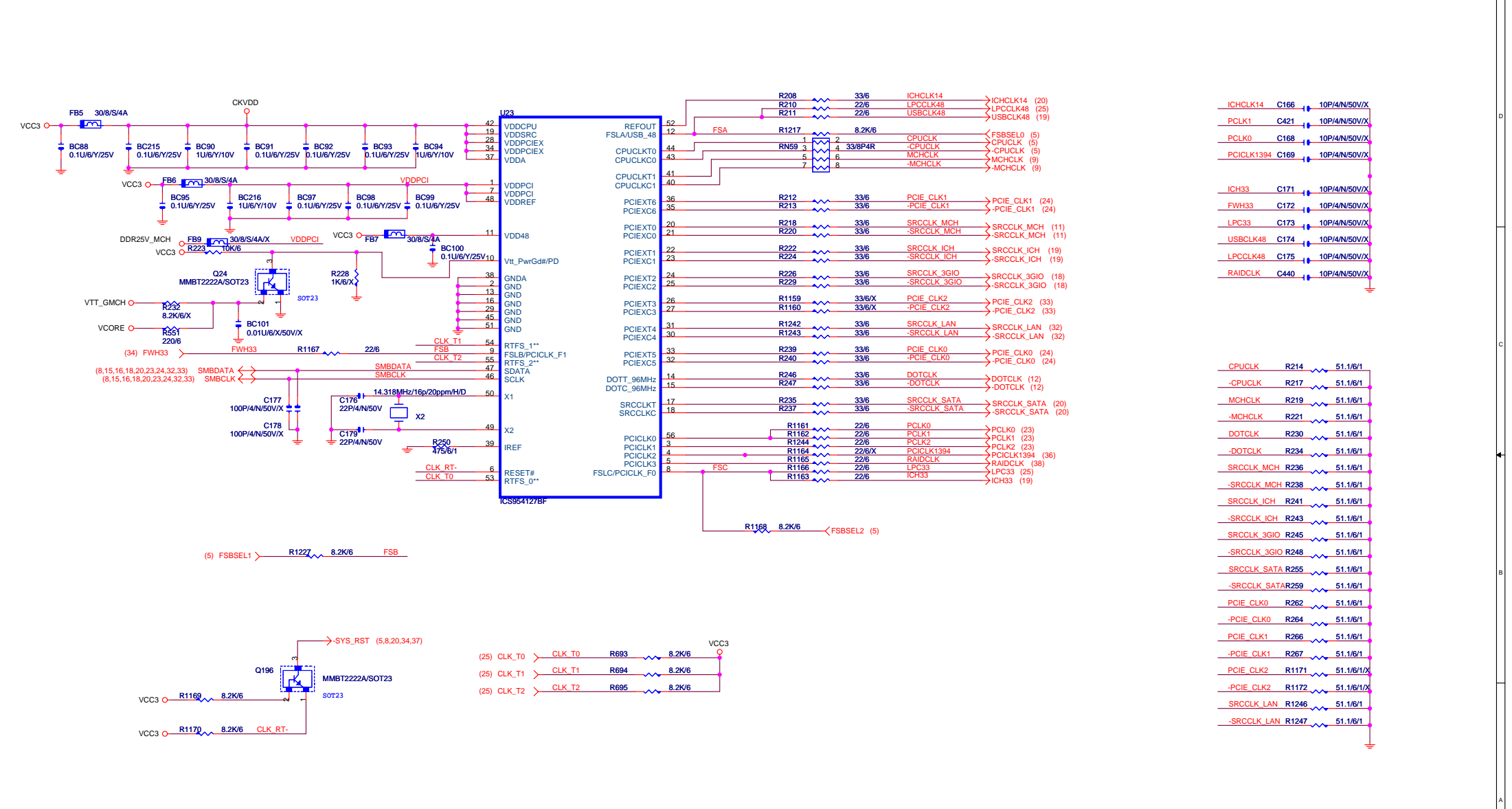




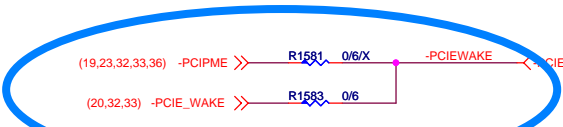
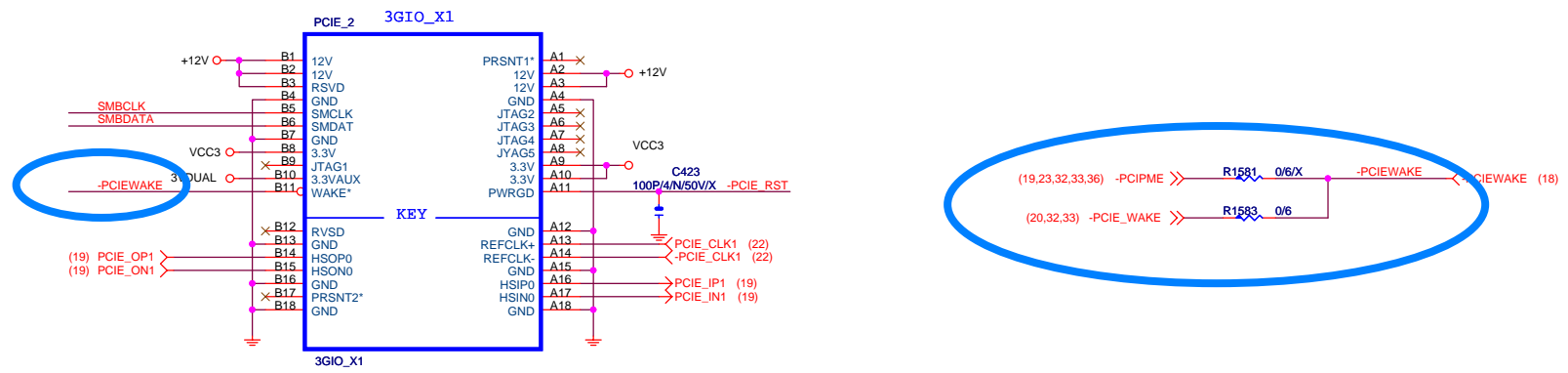
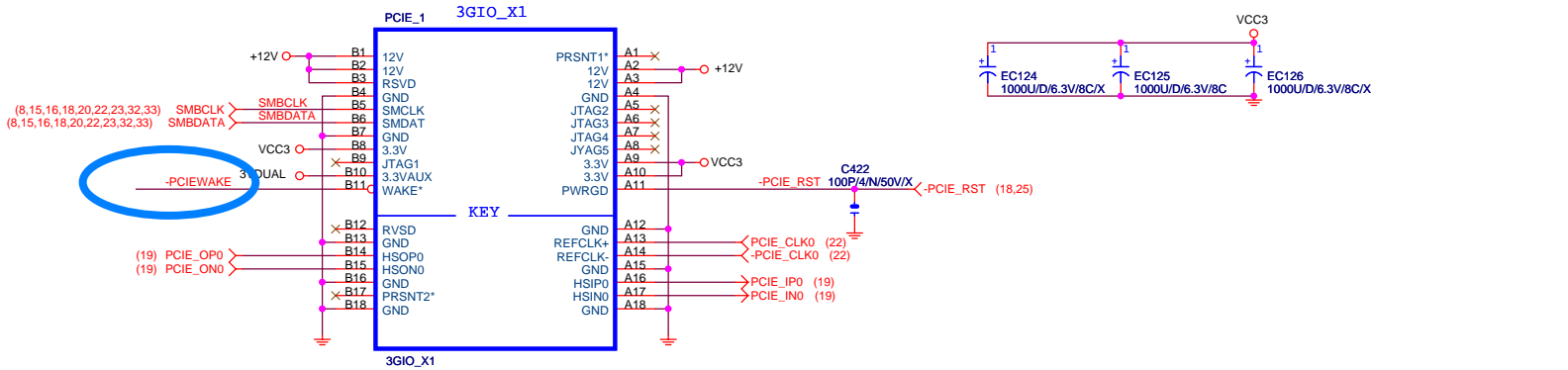
GIGABYTE

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Size	Document Number	8I915G DUO	
Date	Thursday, April 07, 2005	Sheet	21 of 41
		Rev	1.4

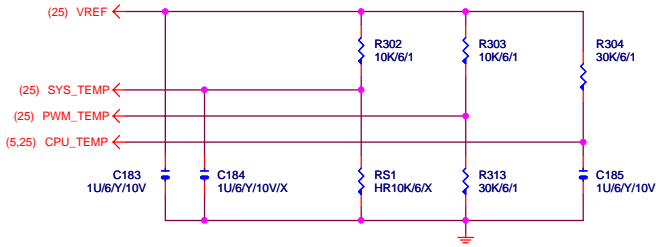
FOR 漏電



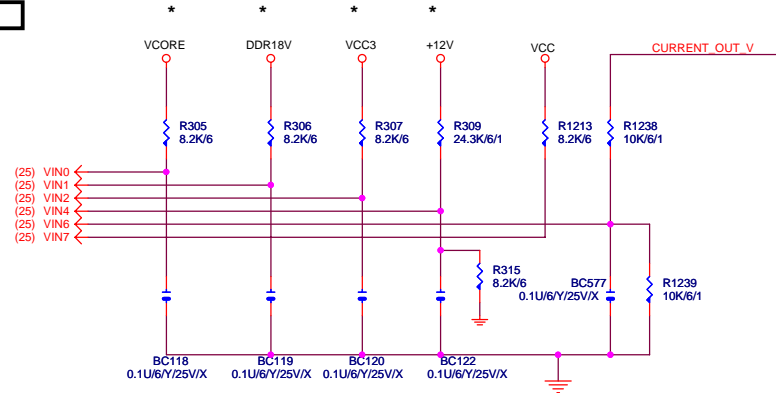
GIGABYTE			
CK410M/GBT_CLK_GEN			
Title		Rev	
CK410M/GBT_CLK_GEN		1.4	
Size	Document Number		
Custom	8915G DUO		
Date:	Thursday, April 07, 2005	Sheet	22 of 41



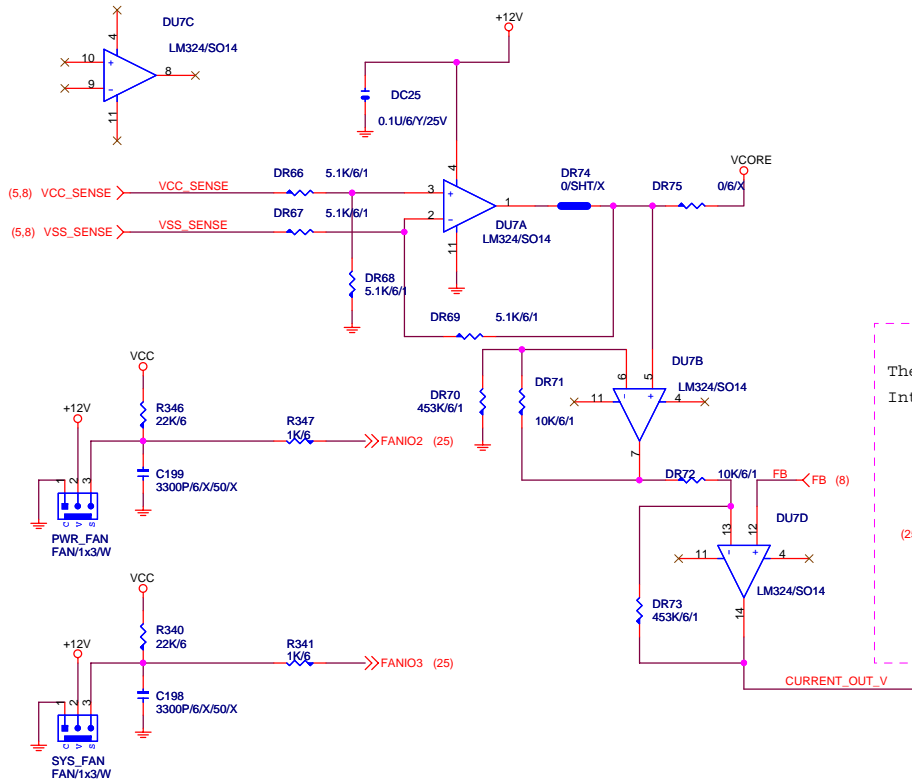
TEMP. SENSE



VOLTAGE SENSE

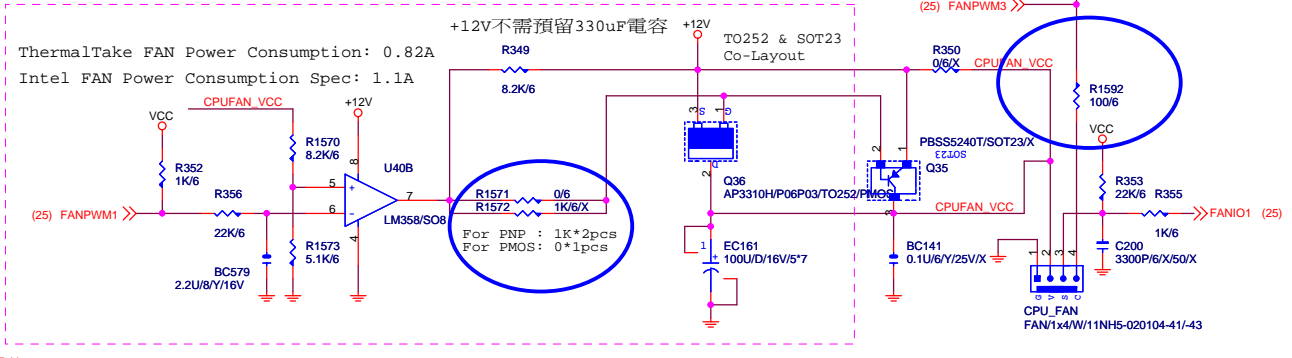


DUAL POWER



CPU/SYS FAN

Configuration	Temp
CPUFAN_VCC=12V: (non airflow)	Temp=40 deg
CPUFAN_VCC=11V: (non airflow)	Temp=82 deg
CPUFAN_VCC=10V: (non airflow)	Temp=70 deg
CPUFAN_VCC=9V: (non airflow)	Temp=110 deg
CPUFAN_VCC=8V: (non airflow)	Temp>200 deg
CPUFAN_VCC=12V: (with airflow)	Temp=33 deg
CPUFAN_VCC=11V: (with airflow)	Temp=62 deg
CPUFAN_VCC=10V: (with airflow)	Temp=86 deg
CPUFAN_VCC=9V: (with airflow)	Temp=117 deg
CPUFAN_VCC=8V: (with airflow)	Temp>122 deg

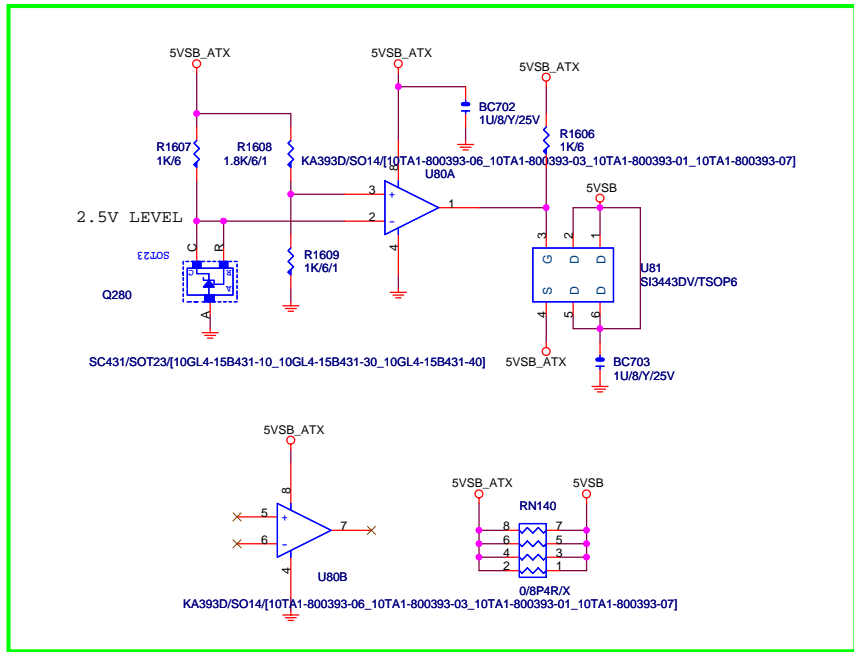
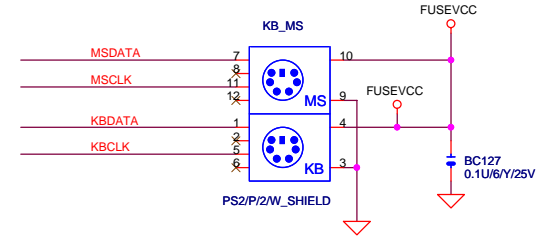
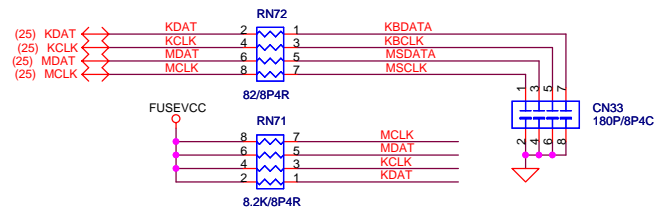


GIGABYTE

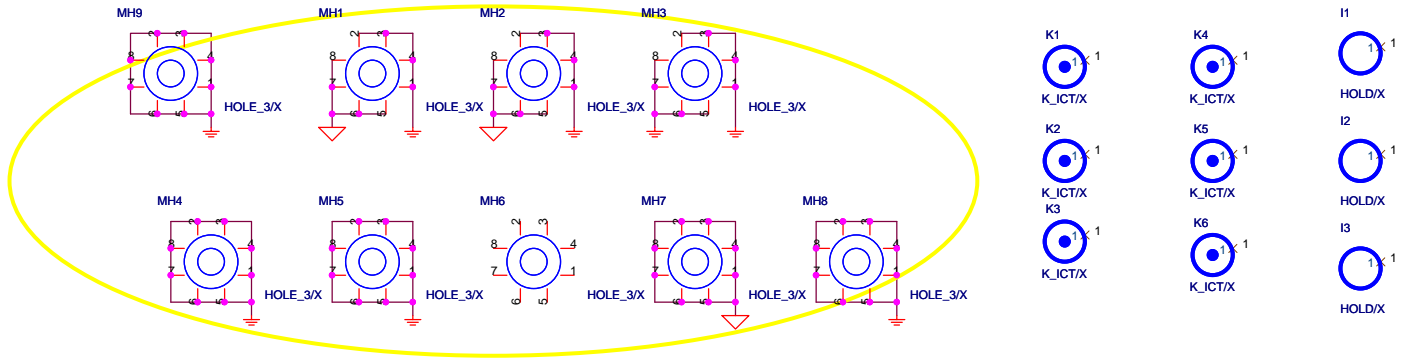
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Size: Custom Document Number: **8I915G DUO** Rev: **1.4**

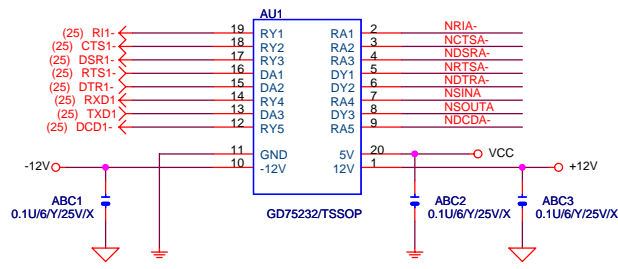
Date: Thursday, April 07, 2005 Sheet: 26 of 41



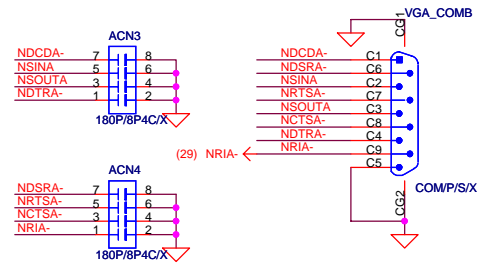
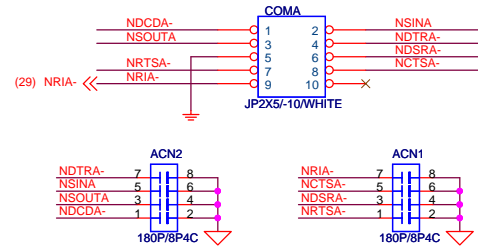
Stand by power
regulator
protection



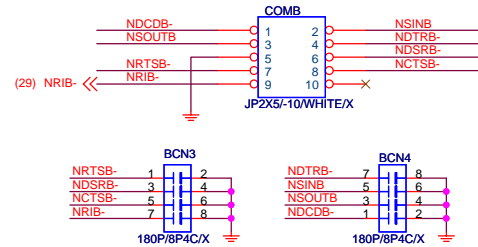
COMA / COMB



INTERNAL COMA



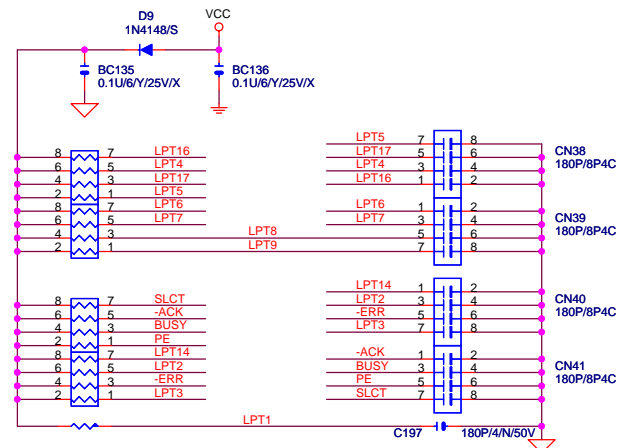
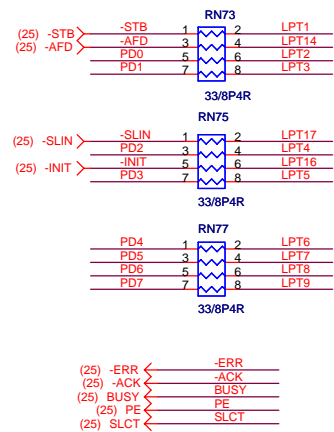
INTERNAL COMB



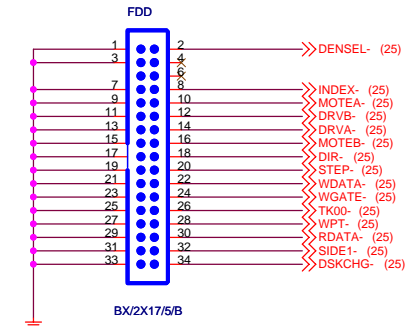
PLACE NEAR VGA_COM CONNECTOR

LPT

(25) PD[0..7] PD[0..7]

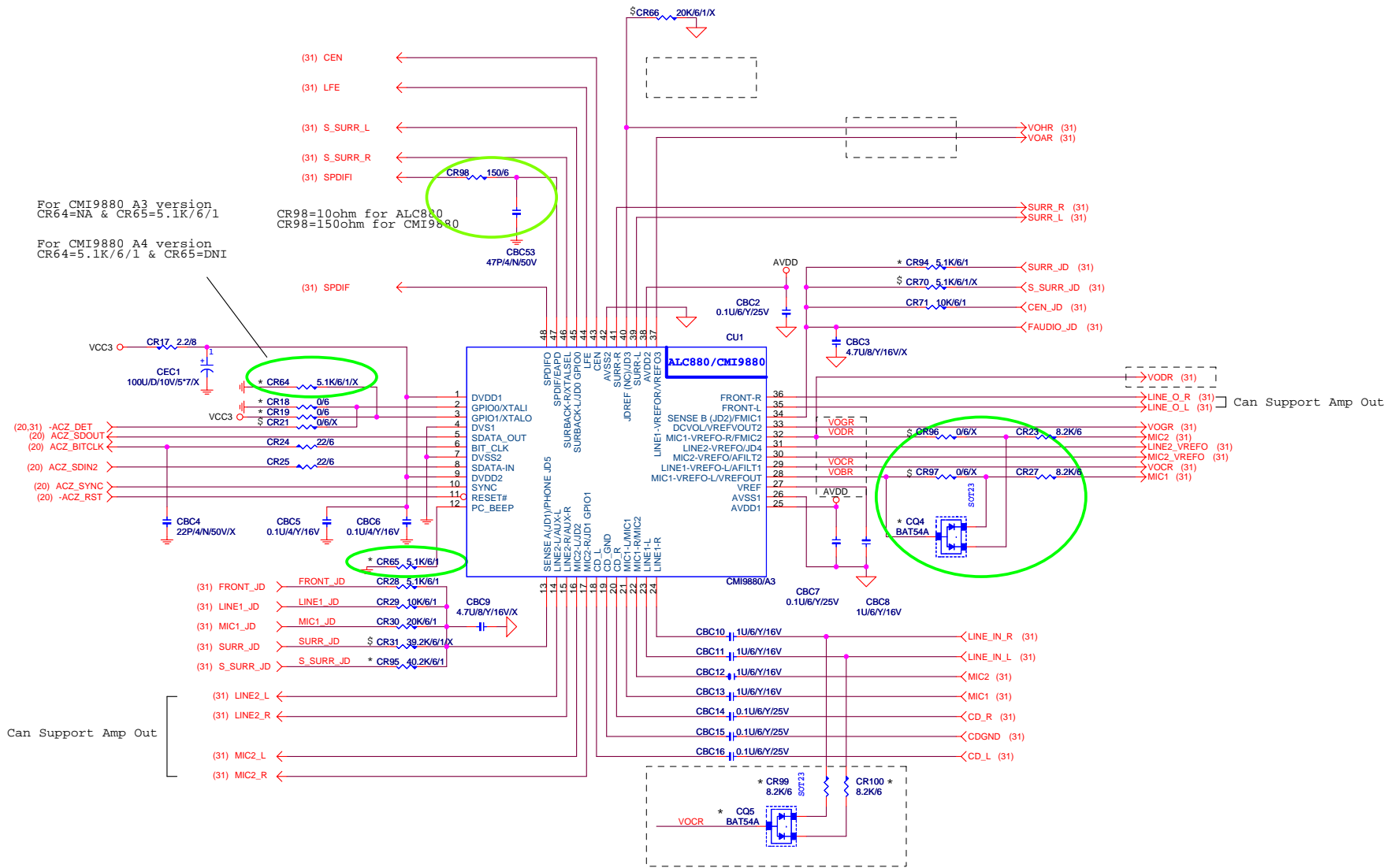


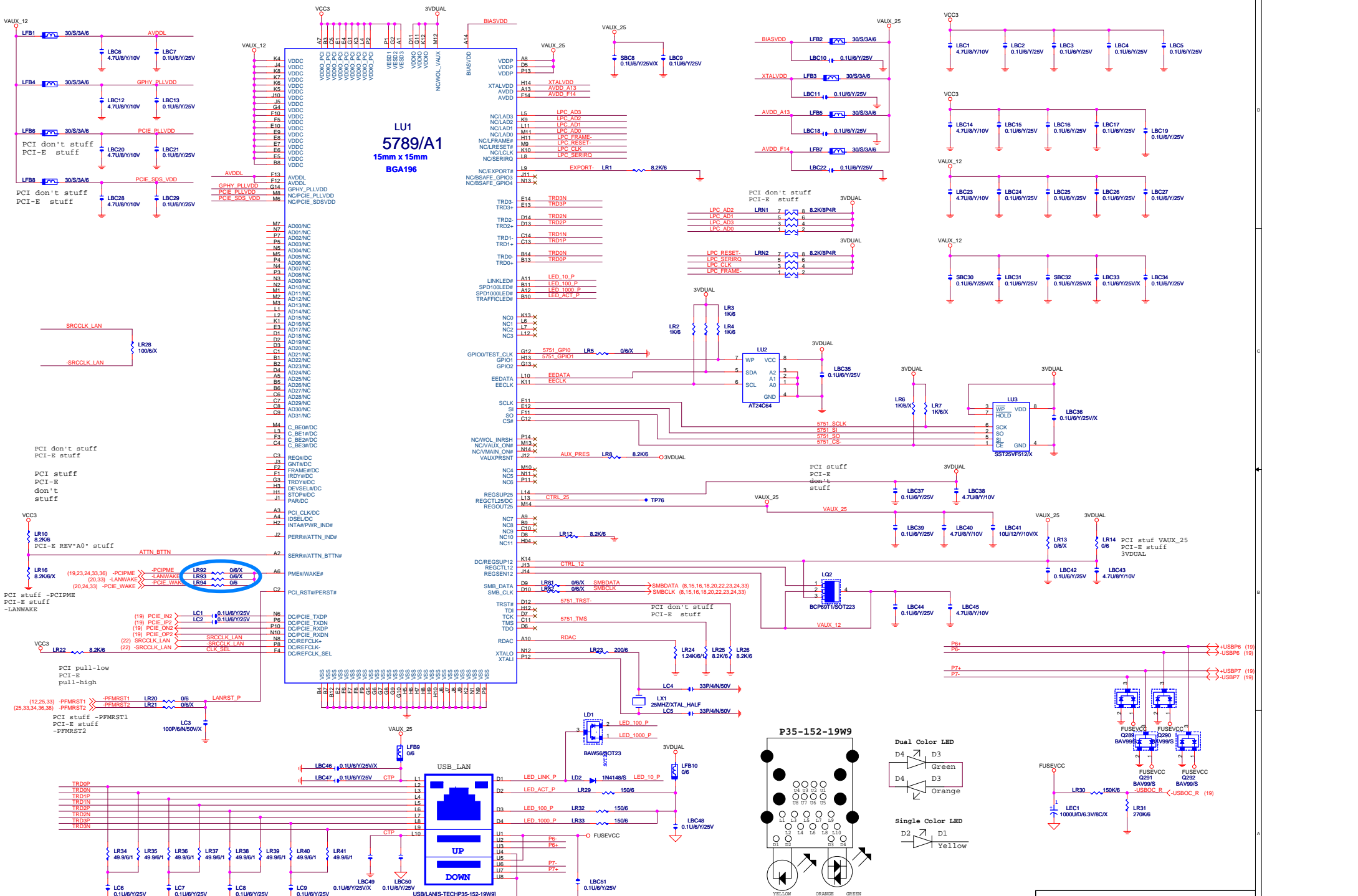
FLOPPY



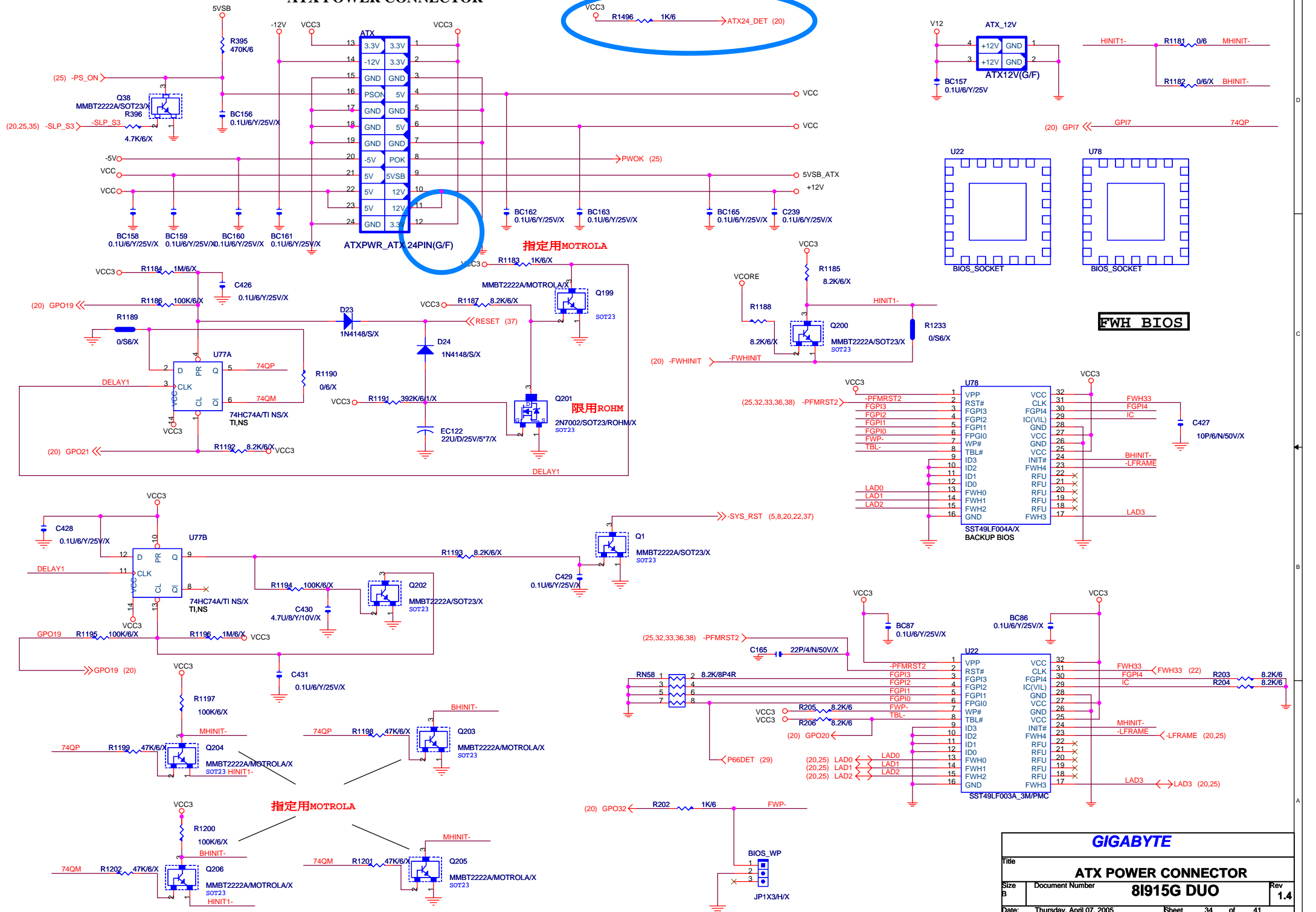
GIGABYTE		
Title		
COM, LPT, FDD		
Size B	Document Number	Rev
	81915G DUO	1.4
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"\$" means for ALC880 only
 "*" means for CMI9880 only

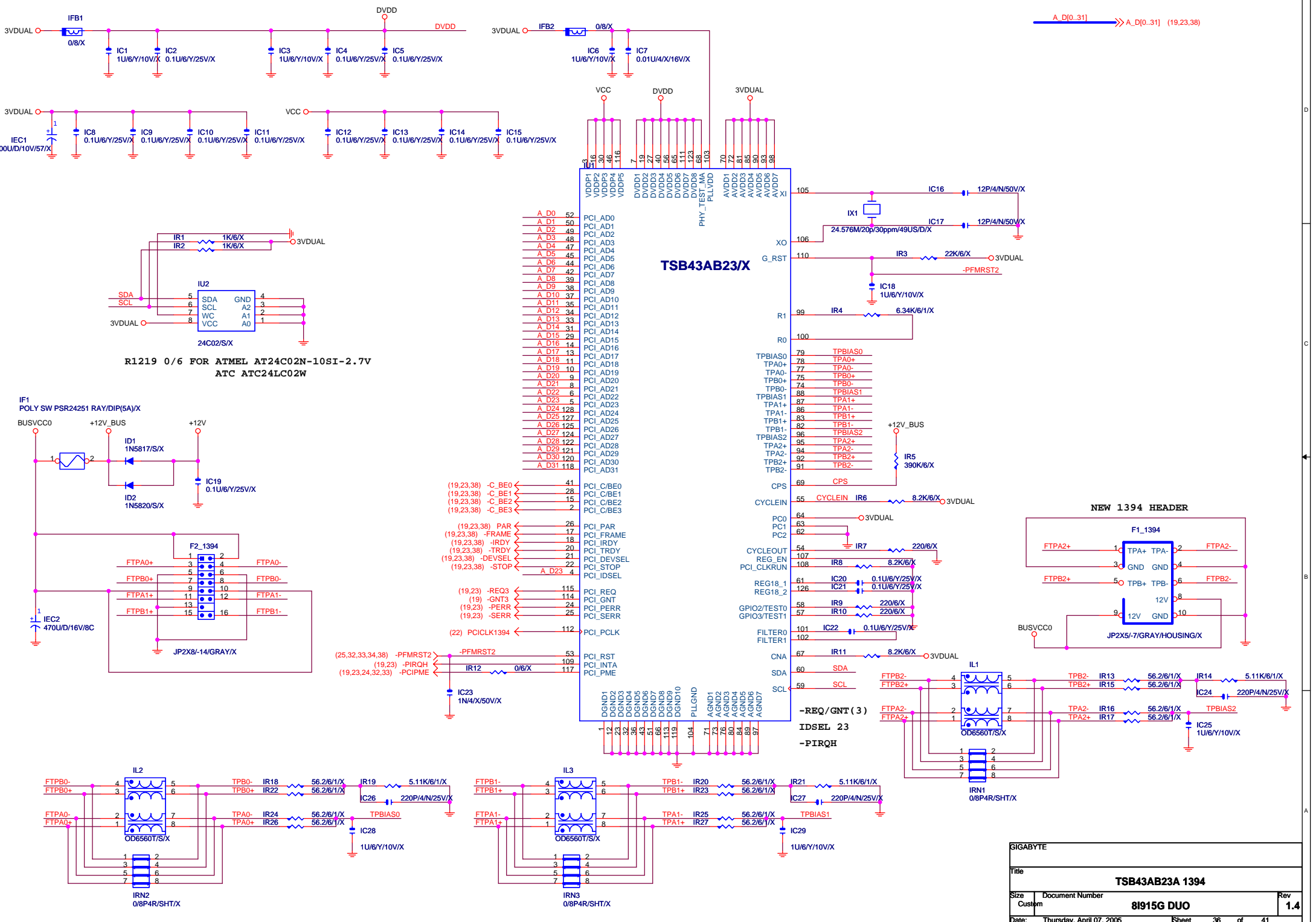




ATX POWER CONNECTOR



GIGABYTE		
ATX POWER CONNECTOR		
Title	81915G DUO	
Size B	Document Number	Rev 1.4
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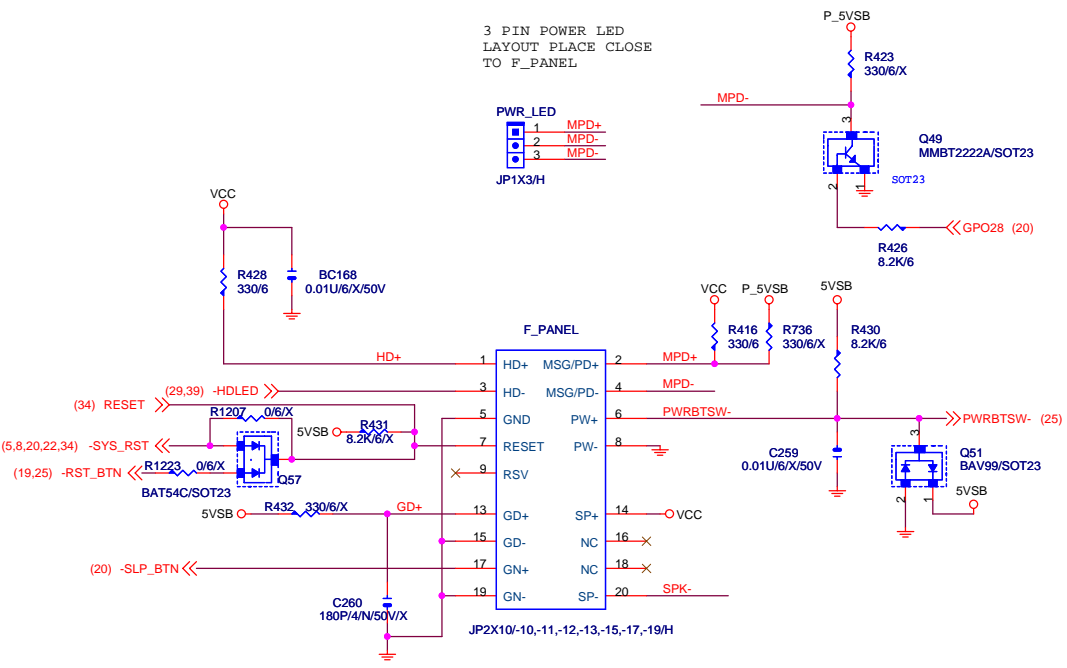
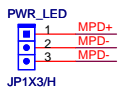
TSB43AB23/X

A D0	52	PCI_AD0
A D1	50	PCI_AD1
A D2	49	PCI_AD2
A D3	48	PCI_AD3
A D4	47	PCI_AD4
A D5	45	PCI_AD5
A D6	44	PCI_AD6
A D7	42	PCI_AD7
A D8	39	PCI_AD8
A D9	38	PCI_AD9
A D10	37	PCI_AD10
A D11	35	PCI_AD11
A D12	34	PCI_AD12
A D13	33	PCI_AD13
A D14	31	PCI_AD14
A D15	29	PCI_AD15
A D16	14	PCI_AD16
A D17	13	PCI_AD17
A D18	11	PCI_AD18
A D19	10	PCI_AD19
A D20	9	PCI_AD20
A D21	8	PCI_AD21
A D22	6	PCI_AD22
A D23	5	PCI_AD23
A D24	128	PCI_AD24
A D25	127	PCI_AD25
A D26	125	PCI_AD26
A D27	124	PCI_AD27
A D28	122	PCI_AD28
A D29	121	PCI_AD29
A D30	120	PCI_AD30
A D31	118	PCI_AD31

(19,23,38) -C_BE0	41	PCI_C/BE0
(19,23,38) -C_BE1	28	PCI_C/BE1
(19,23,38) -C_BE2	15	PCI_C/BE2
(19,23,38) -C_BE3	2	PCI_C/BE3
(19,23,38) PAR	26	PCI_PAR
(19,23,38) -FRAME	17	PCI_FRAME
(19,23,38) -IRDY	18	PCI_IRDY
(19,23,38) -TRDY	20	PCI_TRDY
(19,23,38) -DEVSEL	22	PCI_DEVSEL
(19,23,38) -STOP	22	PCI_STOP
(19,23) -REQ3	115	PCI_REQ
(19) -GNT3	114	PCI_GNT
(19,23) -PERR	24	PCI_PERR
(19,23) -SERR	25	PCI_SERR
(22) PCICLK1394	112	PCI_PCLK
(25,32,33,34,38) -PFMRST2	53	PCI_RST
(19,23) -PIRQH	109	PCI_INTA
(19,23,24,32,33) -PCIPME	117	PCI_PME

INTEL FRONT PANEL

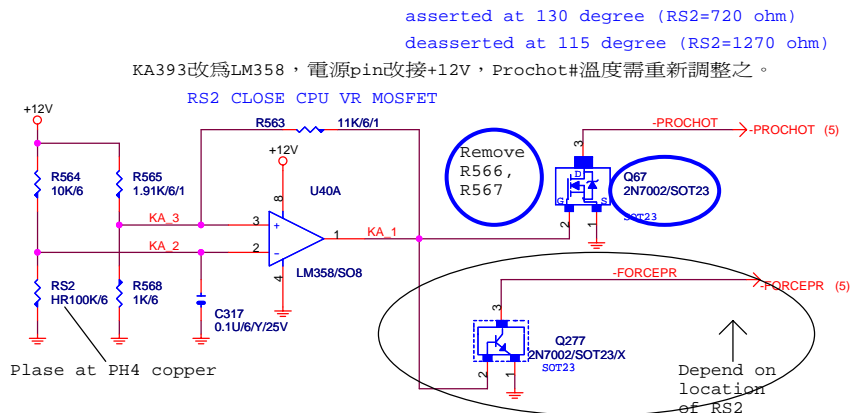
3 PIN POWER LED
LAYOUT PLACE CLOSE
TO F_PANEL



PROCESSOR HOT

(N/A)

如果要用2N7002需注意OP output
Hi時的電壓是否遠大於2V。



asserted at 130 degree (RS2=720 ohm)
deasserted at 115 degree (RS2=1270 ohm)

KA393改為LM358，電源pin改接+12V，Prochot#溫度需重新調整之。

RS2 CLOSE CPU VR MOSFET

States for green LED NO1 GPO22 only S1 PROGRAMMING LOW

LED States	ACPI States	GPO28
ON	S1, S3	0
OFF	S0, S5	1

(GPO22 DEFAULT HIGH, main power)

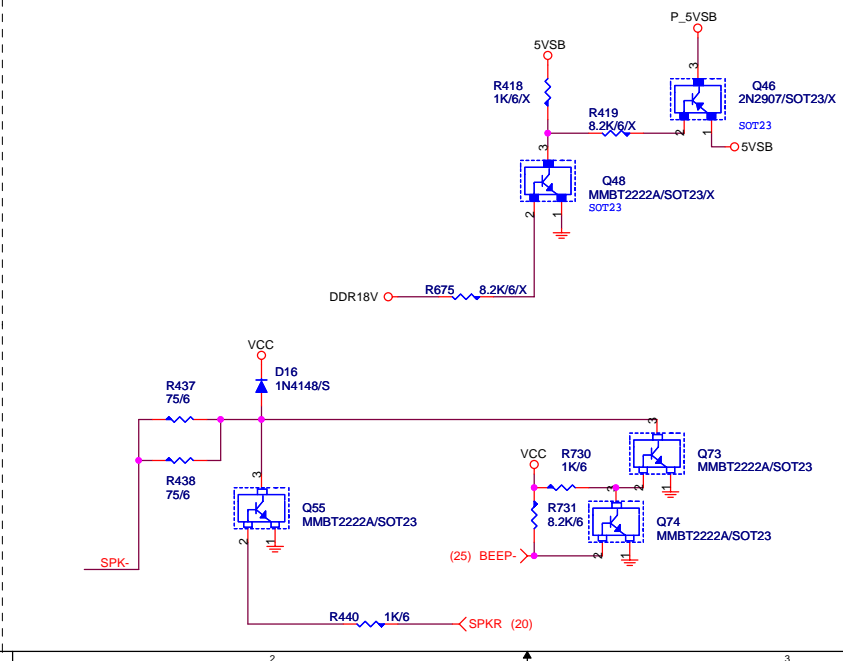
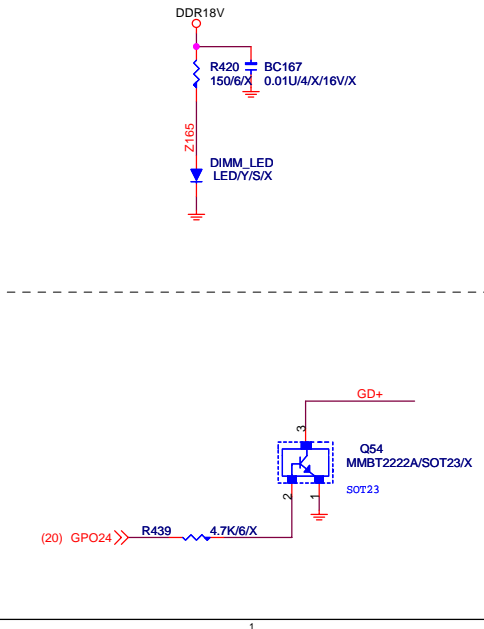
States for a single-color power LED

LED States	ACPI States	GPO25	GPO27	GPO24
OFF	S1, S3, S5	1	1	NO1
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	B	1

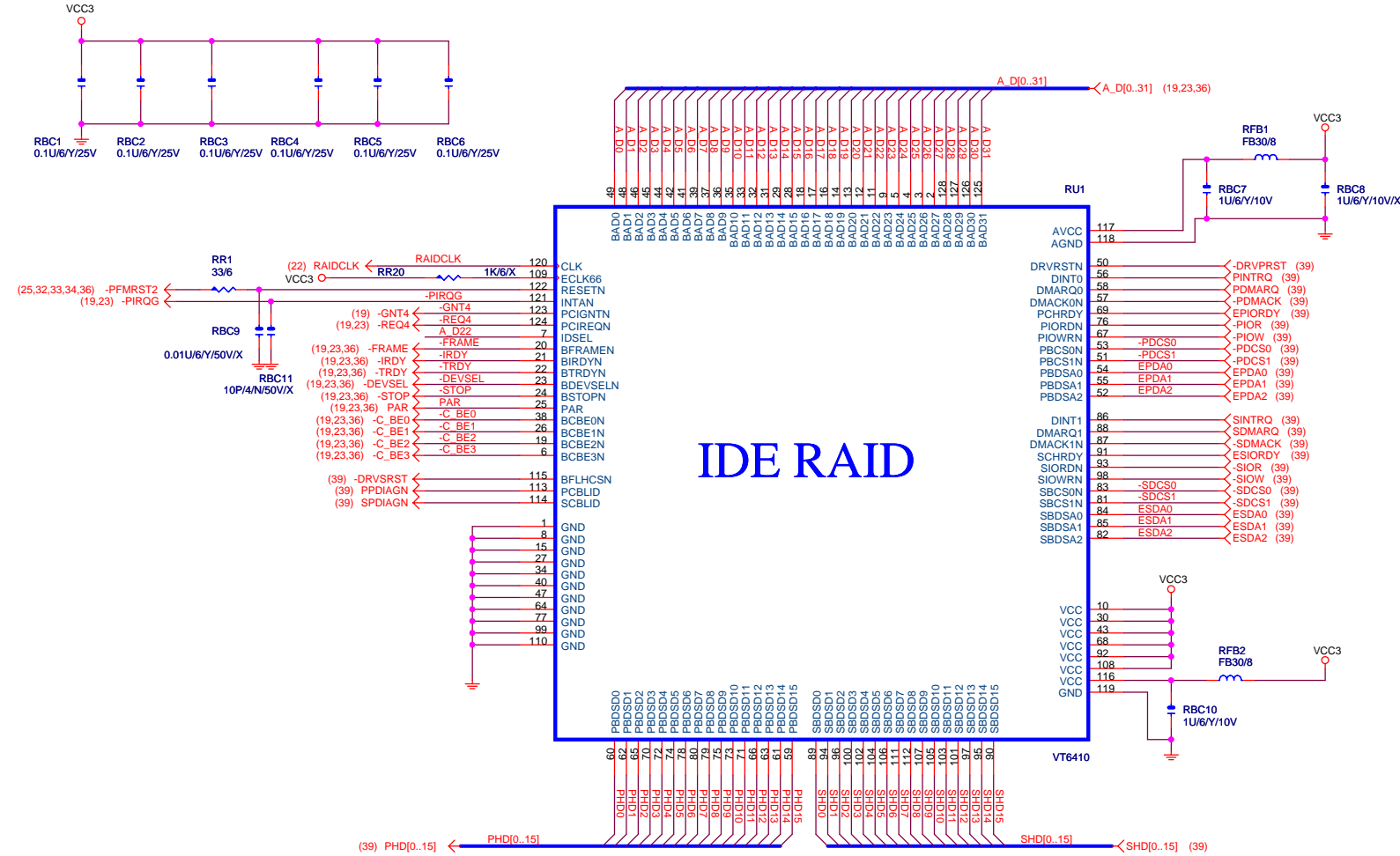
LED States	ACPI States	GPO25	GPO27	GPO22
OFF	S5	1	1	X
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	B	1
Steady Yellow	S1, S3	1	0	NO1
Blinking Yellow	S1, S3(message waiting)	1	B	NO1

GIGABYTE

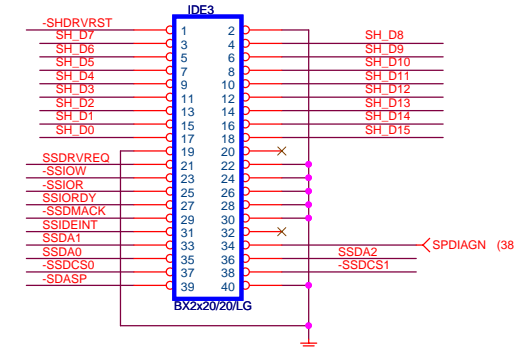
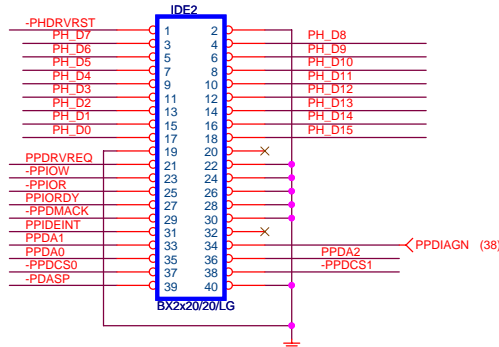
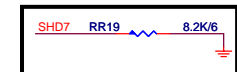
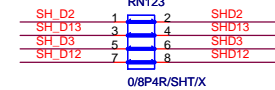
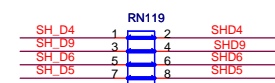
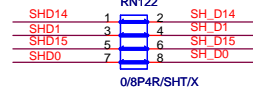
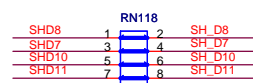
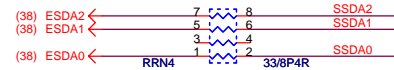
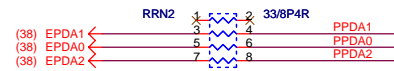
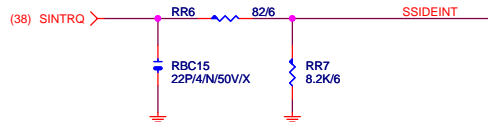
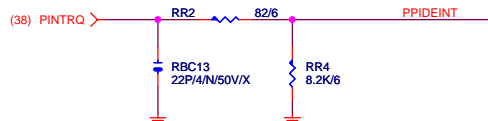
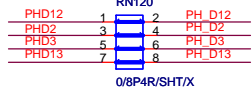
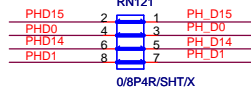
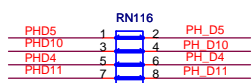
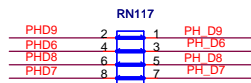
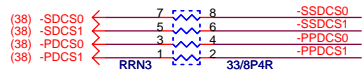
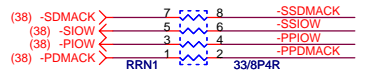
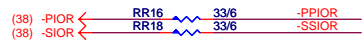
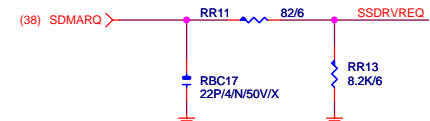
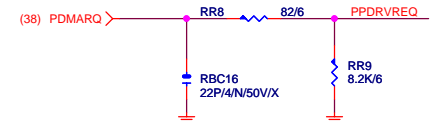
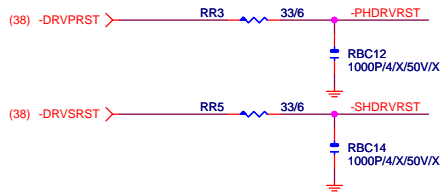
Title: **FRONT PANEL**
 Size Custom: Document Number: **8I915G DUO** Rev: **1.4**
 Date: Thursday, April 07, 2005 Sheet 37 of 41



ALL INPUT PIN MUST HAVE 0.1 CAPACITOR



IDE RAID



ICH6 GPIO Table:

NAME	PWR LANE	USAGE	NAME	PWR LANE	USAGE
GPI0	V5REF	M/B ID (-REQ6)	GPI41	VCC3	M/B ID
GPI1	V5REF	-REQ5	GPO48	VCC3	-GNT4
GPI2	V5REF	-PIRQE	GPO49	V-CPUIO	CPUPWOK
GPI3	V5REF	-PIRQF			
GPI4	V5REF	-PIRQG			
GPI5	V5REF	-PIRQH			
GPI6	VCC3	-SLP BTN			
GPI7	VCC3	DUAL BIOS			
GPI8	3VDAUL	-LANWAKE			
GPI9	3VDAUL	-USBOC4			
GPI10	3VDAUL	-USBOC5			
GPI11	3VDAUL	-SMBALT			
GPI12	VCC3	ATX DET			
GPI13	3VDAUL	-LPCPME			
GPI14	3VDAUL	-USBOC6			
GPI15	3VDAUL	-USBOC7			
GPO16	VCC3	CPU OV1 (-GNT6)			
GPO17	VCC3	-GNT5			
GPO18	VCC3	CPU OV2			
GPO19	VCC3	DUAL BIOS			
GPO20	VCC3	BIOS T-BLOCK			
GPO21	VCC3	DUAL BIOS			
GPO23	VCC3	DDR OV0			
GPIO24	3VDAUL	GREEN LED			
GPIO25	3VDAUL	DDR OV1			
GPI26	VCC3	SATA GP0			
GPIO27	3VDAUL	+PWRLED			
GPIO28	3VDAUL	-PWRLED			
GPI29	VCC3	SATA GP1			
GPI30	VCC3	SATA GP2			
GPI31	VCC3	SATA GP3			
GPIO32	VCC3	BIOS WP			
GPIO33	VCC3	AZALIA DET			
GPIO34	VCC3	M/B ID			
GPI40	V5REF	-REQ4			

PWROK/RESET Table:

ITE8712BHX PIN	NET NAME	TARGET
PIN62/-PCIRST1	-PCIE_RST	1. PCI-E * 1 Slot1 2. PCI-E * 1 Slot2 3. PCI-E * 1 Slot3 4. PCI-E * 16 Slot
PIN64/-PCIRST2	-PFMRST2	1. Onboard PCI Lan 2. Onboard 1394 Chip 3. OnBoard FWH
PIN65/-PCIRST3	-PFMRST1	1. Onboard PCI-E Lan 2. Onboard SATA Chip 3. GMCH
PIN115/-PCIRST4	-PFMRST_ -IDERST	Reserved For IDE
PIN63/PWROK1	PWROK1	1. GMCH 2. ICH6 3. 5VDUAL SWITCH 4. DPS CONTROL
PIN109/PWROK2	-THERM	1. ICH6

GIGABYTE THCNOLOGIES , INC.

Title			GPIO/RESET TABLE		
Size	Document Number	8I915G DUO			Rev
Custom					1.4
Date:	Thursday, April 07, 2005	Sheet	41	of	41