

Compal Confidential

Schematic Document

Crestline_GM/PM+NB8M-GS & ICH8M

2007 / 1 / 2 Rev:0.4

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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	Cover Sheet
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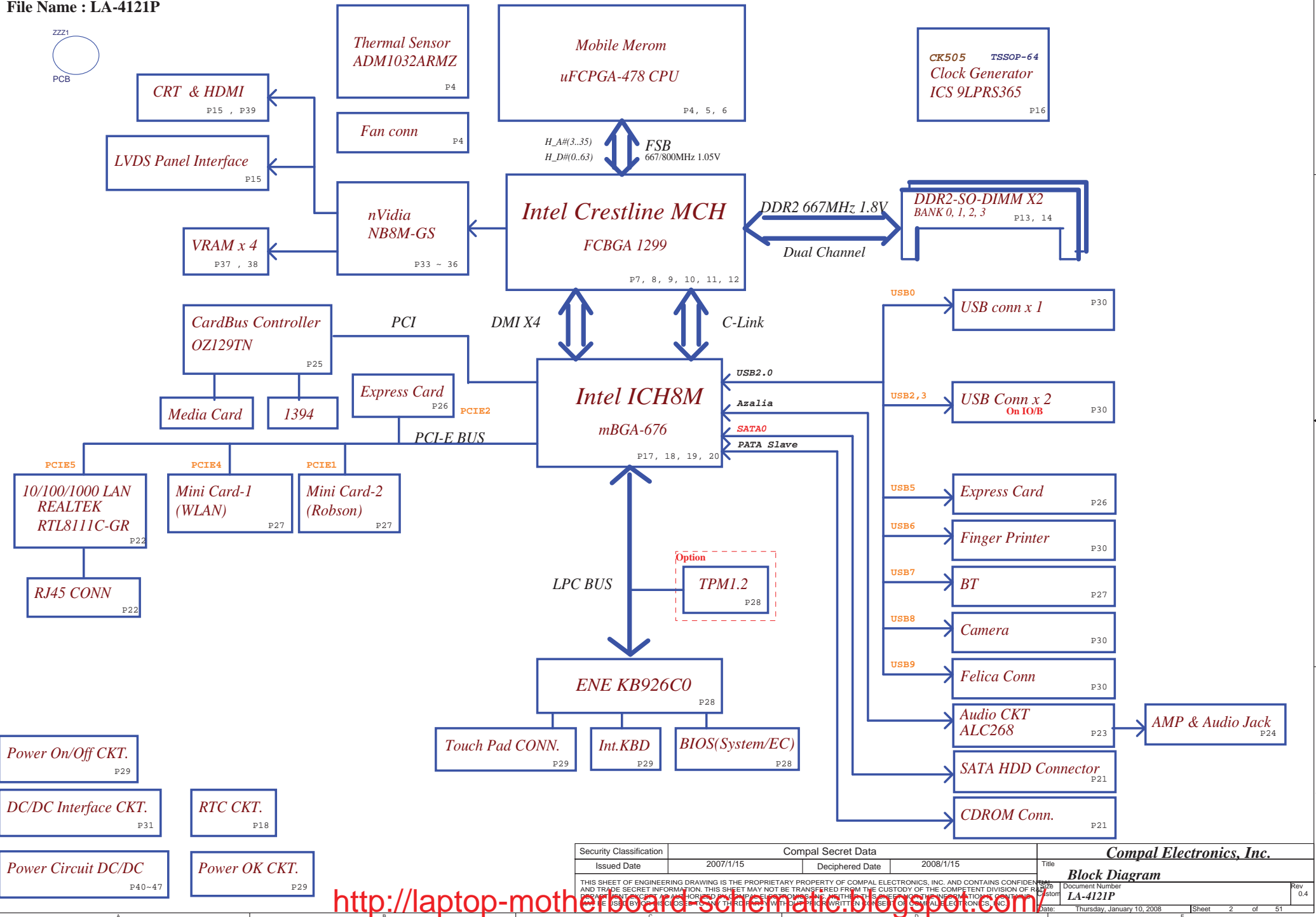
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Project Code: ANRJAL3000 (JAL30)

File Name : LA-4121P

JAL30 UMA/Discrete



O MEANS ON X MEANS OFF

State \ Power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.8VS +1.5VS +1.25VS +1.2VS +0.9VS +CPU_CORE +VGA_CORE +VCCP	CLOCK
S0	O	O	O	O	O
S3	O	O	O	X	O
S5 S4/AC	O	O	X	X	O
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

O MEANS ON

X MEANS OFF

S3 : STR

S4 : STD

S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD21	0	PIRQE/PIRQF/PIRQG

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b?	ADM1032	4D
EEPROM(24C16/02)	1010 000X b?		
(24C04)	1011 000Xb?		

EC SM Bus2 address

Device	Address
ADM1032	4D

ICH7 SM Bus address

Device	Address
Clock Generator (ICS ICS9LPR310)	1101 001Xb?
DDRII DIMM0	1001 000Xb?
DDRII DIMM2	1001 010Xb?

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

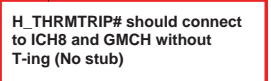
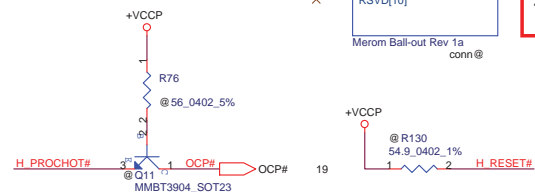
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	
4	
5	
6	
7	

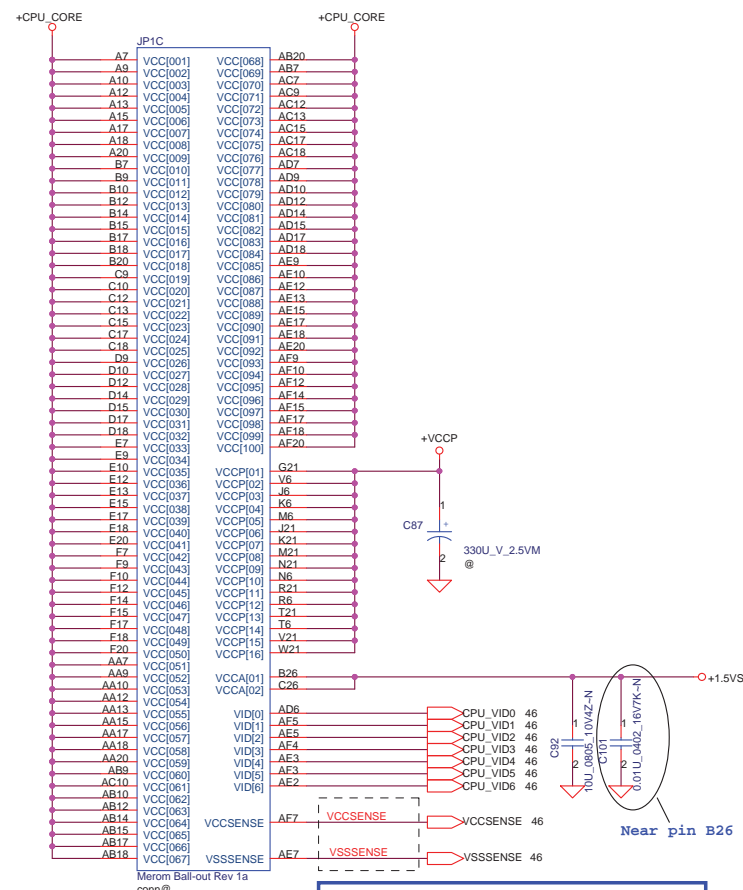
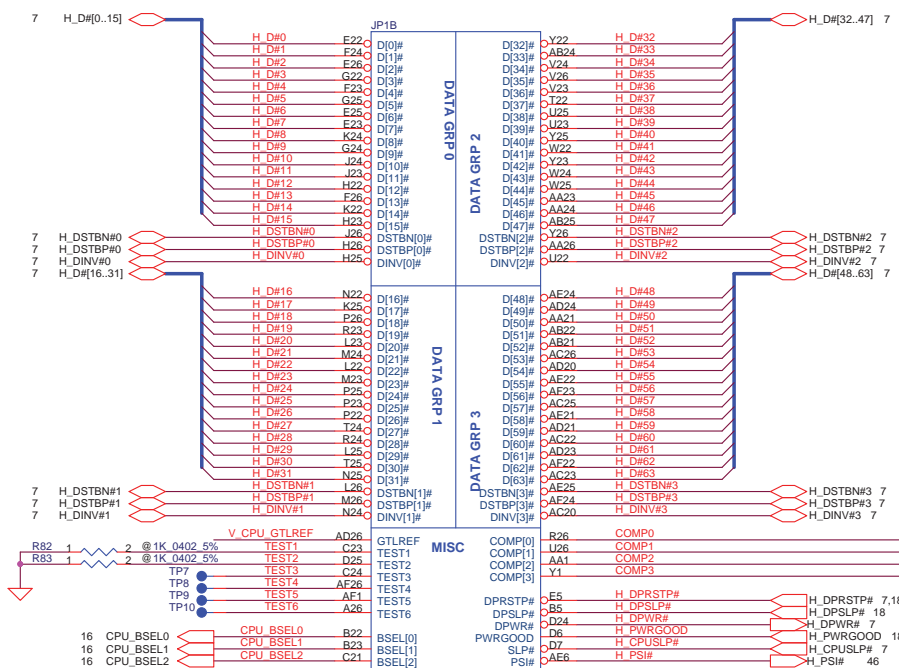
BTO Option Table

[illegible]

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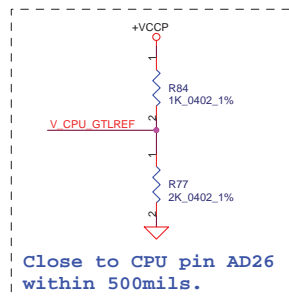
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layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

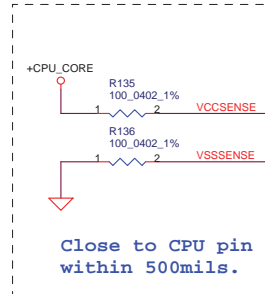
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0



Close to CPU pin AD26 within 500mils.

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.

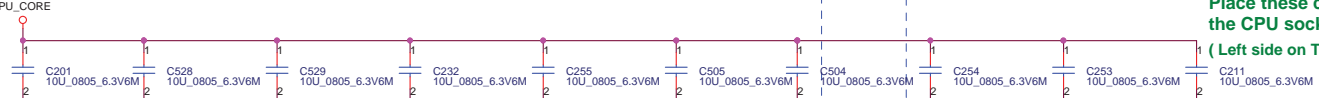


Close to CPU pin within 500mils.

High Frequency Decoupling 10uF 0805 X5R -> 85 degree.

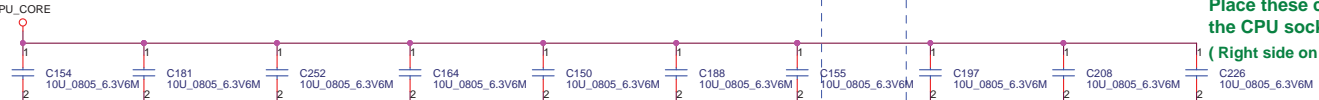
A4	JP1D	VSS[001]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V22
C8	VSS[018]	VSS[099]	V25
C11	VSS[019]	VSS[100]	W1
C14	VSS[020]	VSS[101]	W4
C16	VSS[021]	VSS[102]	W23
C19	VSS[022]	VSS[103]	W26
C2	VSS[023]	VSS[104]	Y3
C22	VSS[024]	VSS[105]	Y6
C25	VSS[025]	VSS[106]	Y21
D1	VSS[026]	VSS[107]	Y24
D4	VSS[027]	VSS[108]	AA2
D8	VSS[028]	VSS[109]	AA5
D11	VSS[029]	VSS[110]	AA8
D13	VSS[030]	VSS[111]	AA11
D16	VSS[031]	VSS[112]	AA14
D19	VSS[032]	VSS[113]	AA16
D23	VSS[033]	VSS[114]	AA19
D26	VSS[034]	VSS[115]	AA22
E3	VSS[035]	VSS[116]	AA25
E6	VSS[036]	VSS[117]	AB1
E8	VSS[037]	VSS[118]	AB4
E11	VSS[038]	VSS[119]	AB8
E14	VSS[039]	VSS[120]	AB11
E16	VSS[040]	VSS[121]	AB13
E19	VSS[041]	VSS[122]	AB16
E21	VSS[042]	VSS[123]	AB19
E24	VSS[043]	VSS[124]	AB23
F5	VSS[044]	VSS[125]	AB26
F8	VSS[045]	VSS[126]	AC3
F11	VSS[046]	VSS[127]	AC6
F13	VSS[047]	VSS[128]	AC8
F16	VSS[048]	VSS[129]	AC11
F19	VSS[049]	VSS[130]	AC14
F2	VSS[050]	VSS[131]	AC16
F22	VSS[051]	VSS[132]	AC19
F25	VSS[052]	VSS[133]	AC21
G4	VSS[053]	VSS[134]	AC24
G1	VSS[054]	VSS[135]	AD2
G23	VSS[055]	VSS[136]	AD5
G26	VSS[056]	VSS[137]	AD8
H3	VSS[057]	VSS[138]	AD11
H6	VSS[058]	VSS[139]	AD13
H21	VSS[059]	VSS[140]	AD16
H24	VSS[060]	VSS[141]	AD19
J2	VSS[061]	VSS[142]	AD22
J5	VSS[062]	VSS[143]	AD25
J22	VSS[063]	VSS[144]	AE1
J25	VSS[064]	VSS[145]	AE4
K1	VSS[065]	VSS[146]	AE8
K4	VSS[066]	VSS[147]	AE11
K23	VSS[067]	VSS[148]	AE14
K26	VSS[068]	VSS[149]	AE16
L3	VSS[069]	VSS[150]	AE19
L6	VSS[070]	VSS[151]	AE23
L24	VSS[071]	VSS[152]	AE26
M2	VSS[072]	VSS[153]	A2
M5	VSS[073]	VSS[154]	AF6
M22	VSS[074]	VSS[155]	AF8
M25	VSS[075]	VSS[156]	AF11
N1	VSS[076]	VSS[157]	AF13
N4	VSS[077]	VSS[158]	AF16
N23	VSS[078]	VSS[159]	AF19
N26	VSS[079]	VSS[160]	AF21
P3	VSS[080]	VSS[161]	A25
	VSS[081]	VSS[162]	AF25
		VSS[163]	

Place these caps inside
the CPU socket cavity.
(Left side on Top).



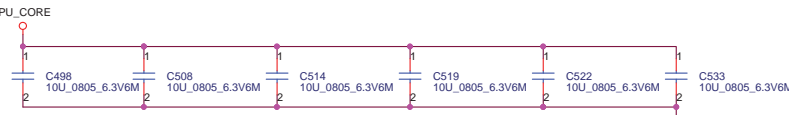
Place these caps inside
the CPU socket.
(Left side on Top).

Place these caps inside
the CPU socket cavity.
(Right side on Top side).

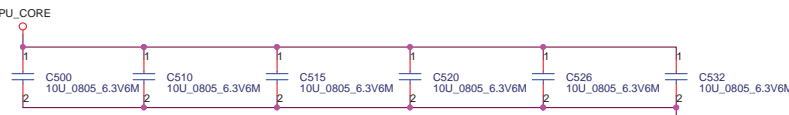


Place these caps inside
the CPU socket.
(Right side on Top).

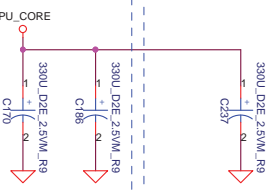
Place these caps inside
the CPU socket cavity.
(Left side on Bottom).



Place these caps inside
the CPU socket cavity.
(Right side on Bottom).



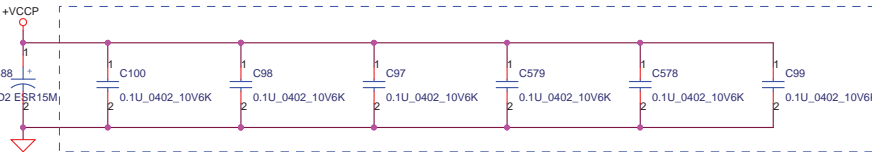
Place these caps inside
the CPU socket.
(Left side on Top).



Place these caps inside
the CPU socket.
(Right side on Top side).

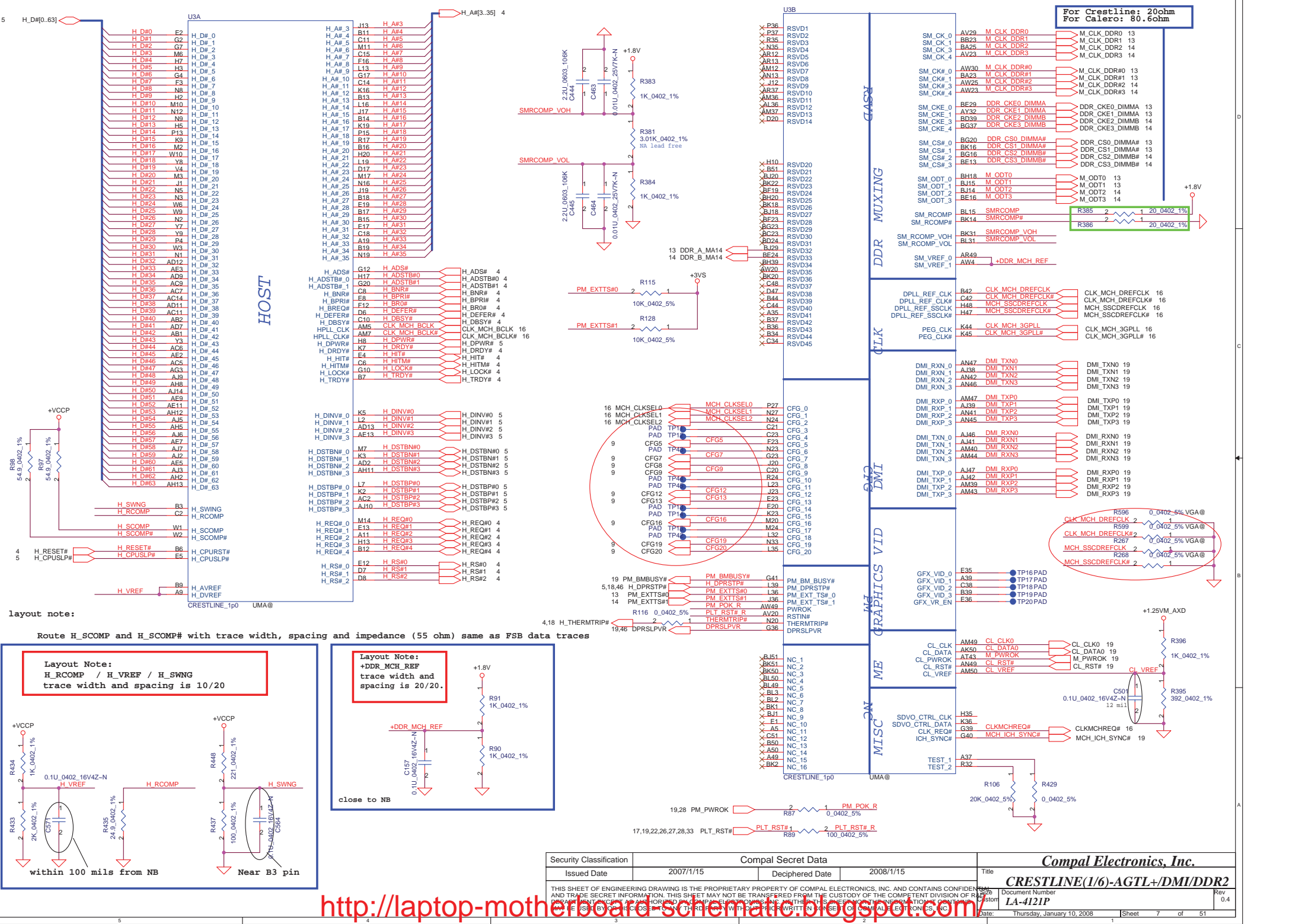
ESR <= 1.5m ohm
Capacitor > 880 uF

Place these outside of
socket cavity on L8
(North side Secondary)

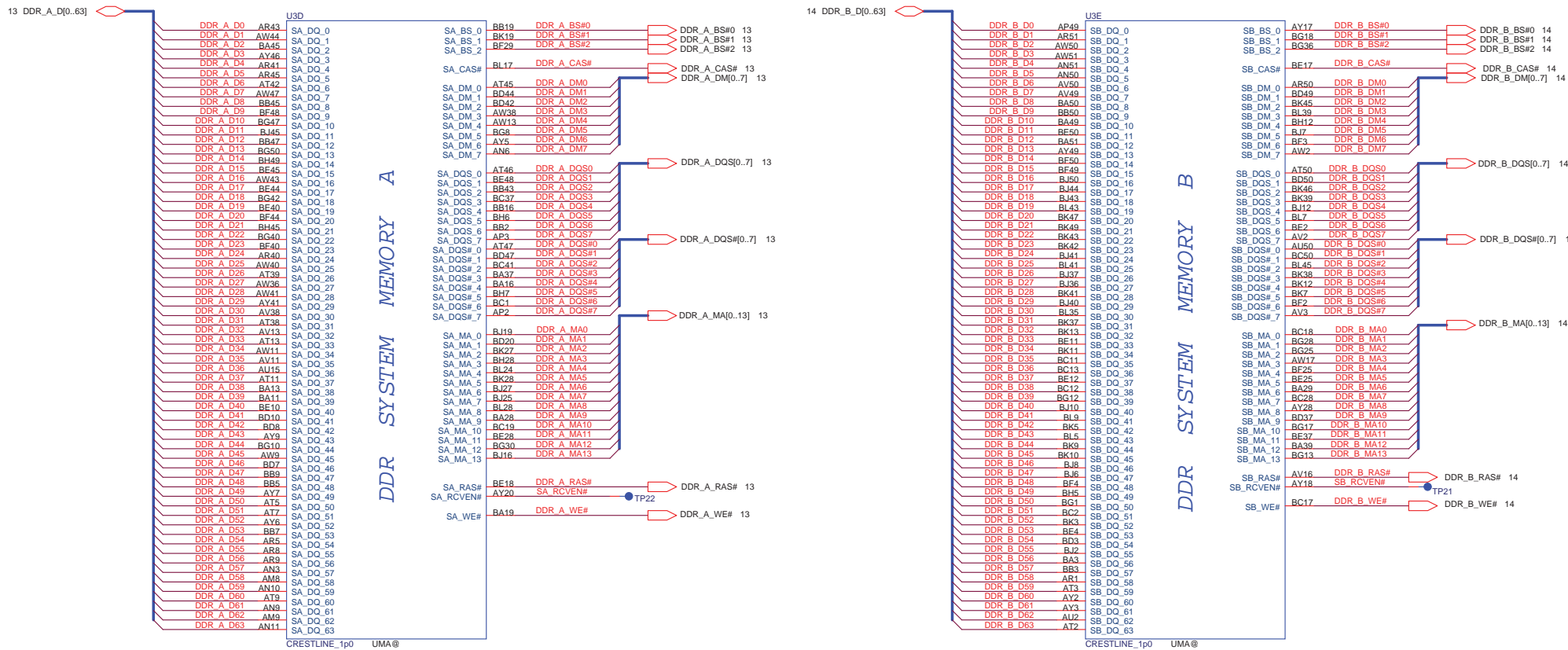


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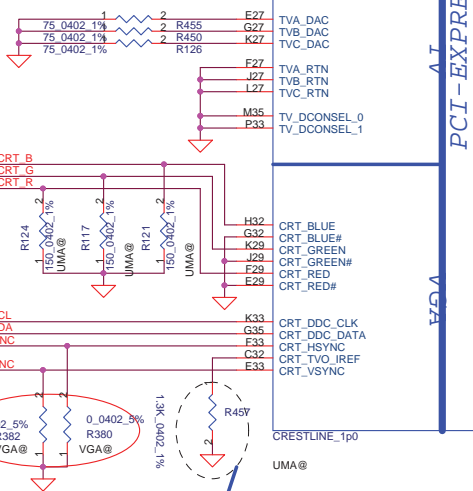
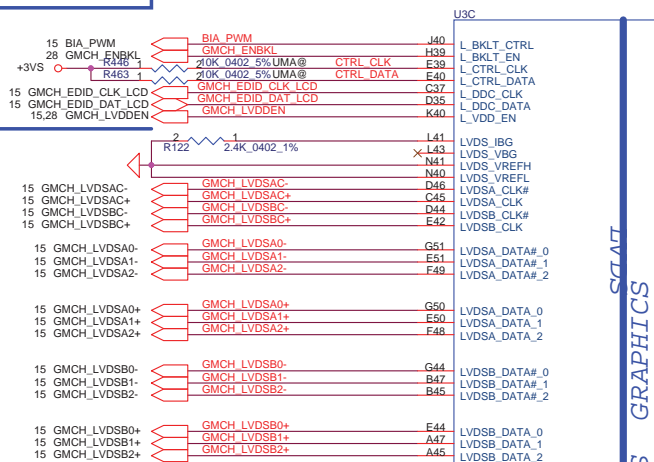
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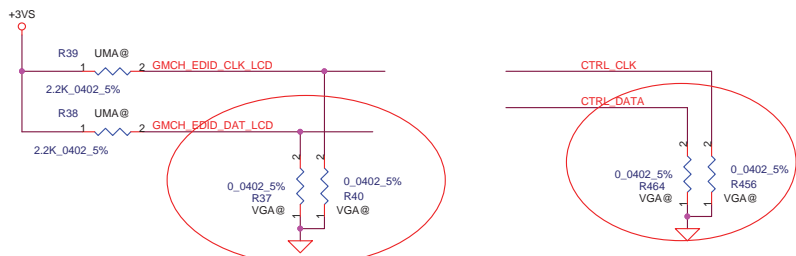
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```
For Crestline:2.4kohm
For Calero: 1.5Kohm
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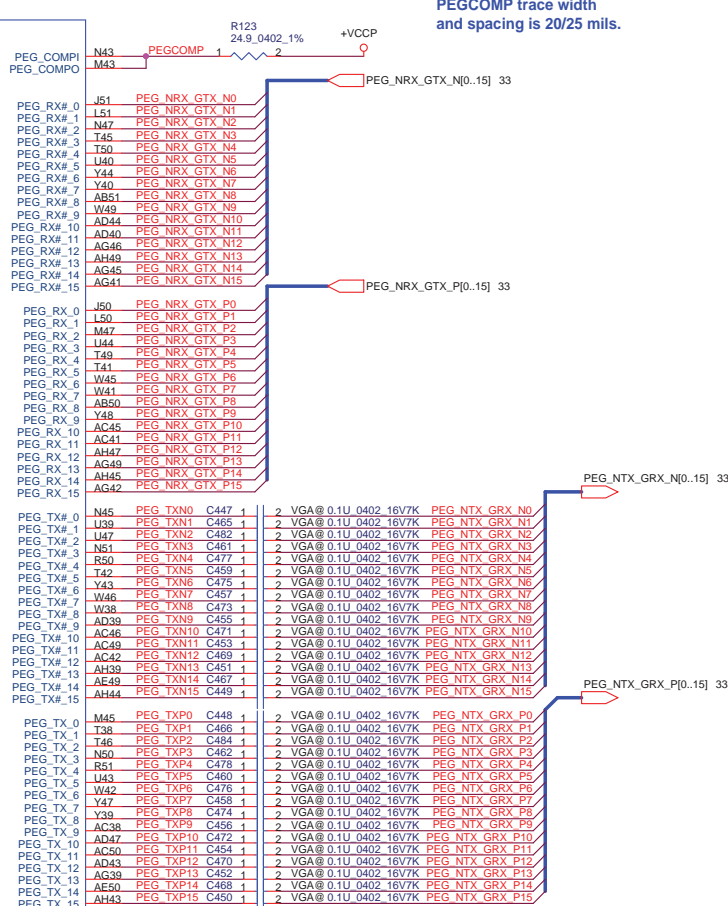


For Crestline: 1.3kohm
For Calero: 255ohm



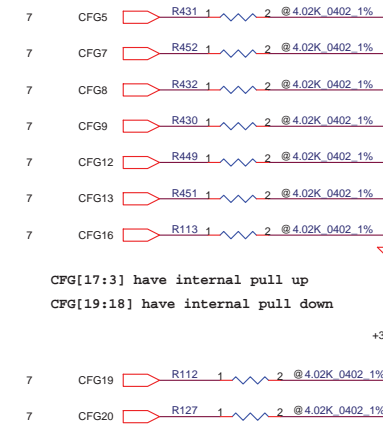
Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

PEGCOMP trace width
and spacing is 20/25 mils.

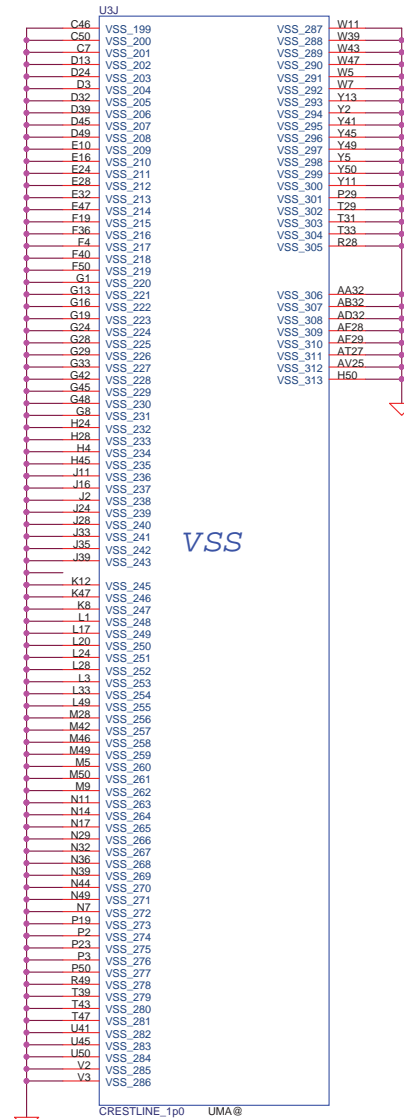
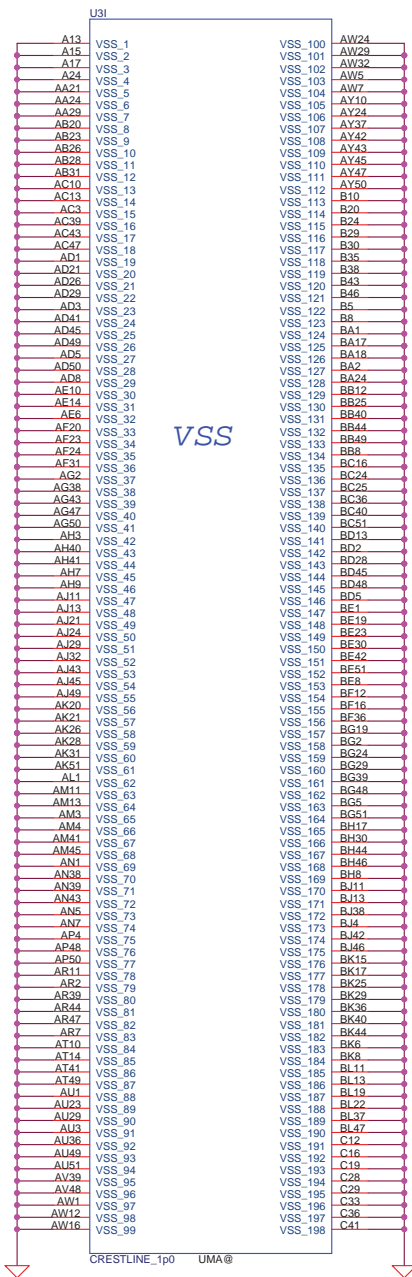


Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

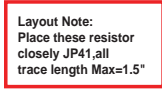
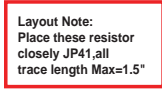
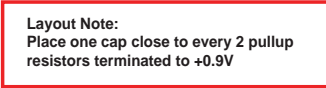
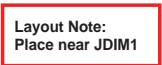


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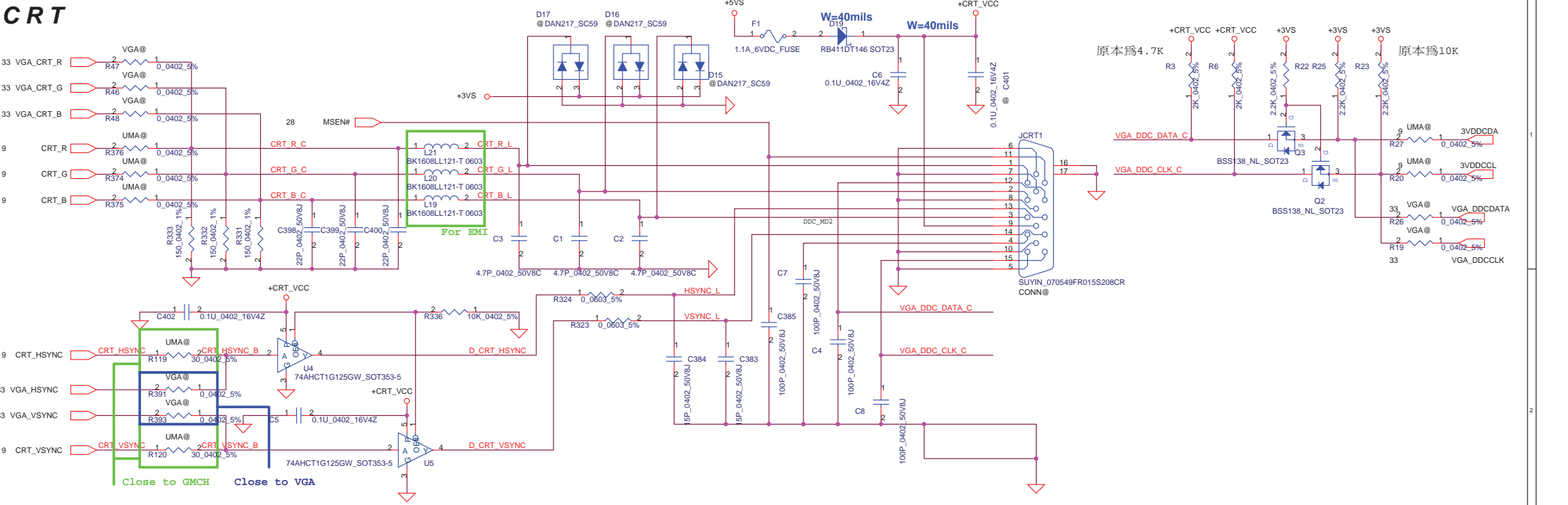
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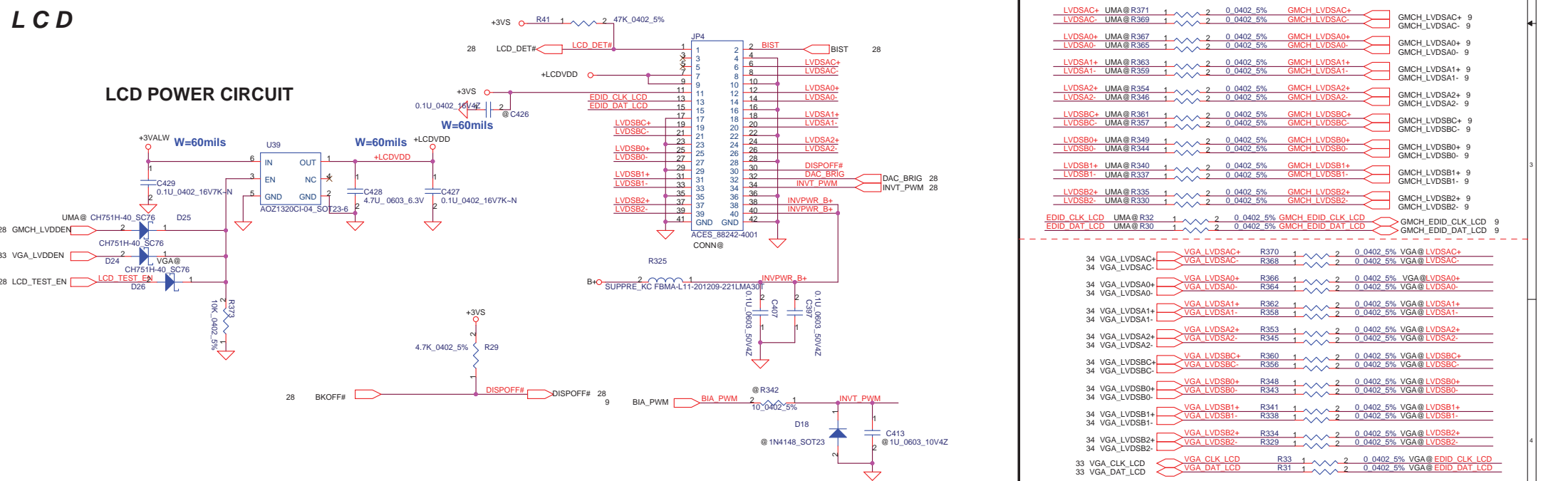


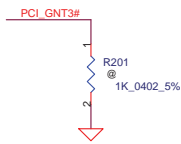
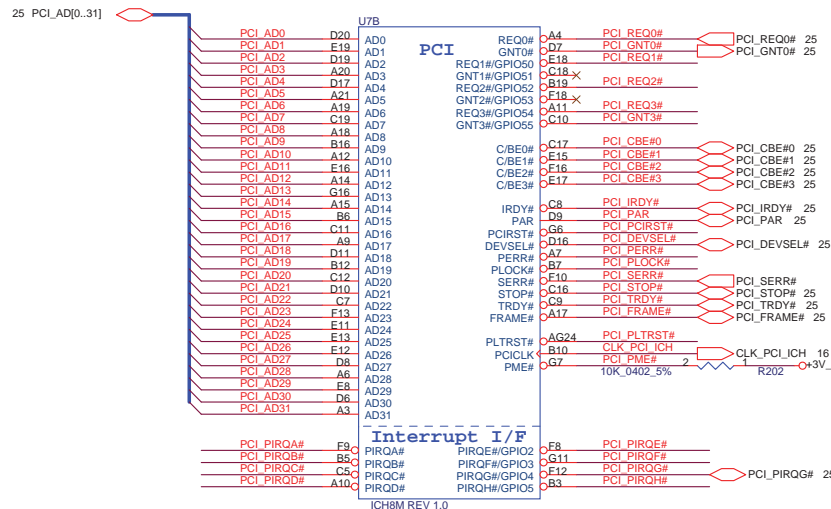
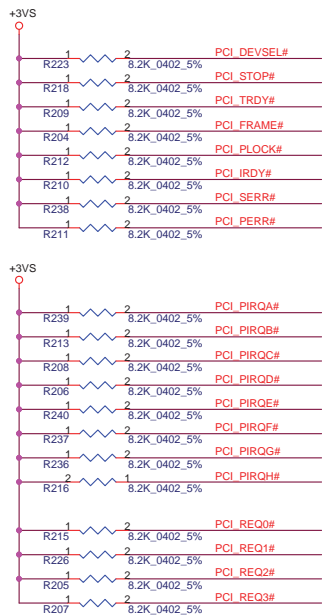
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CRT

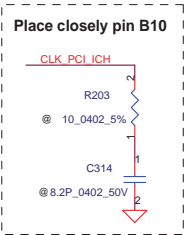


LCD

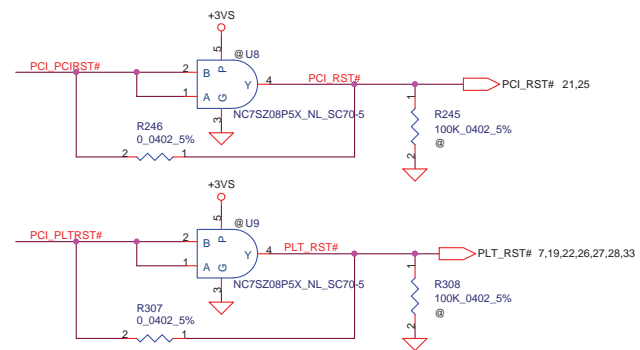
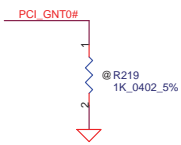


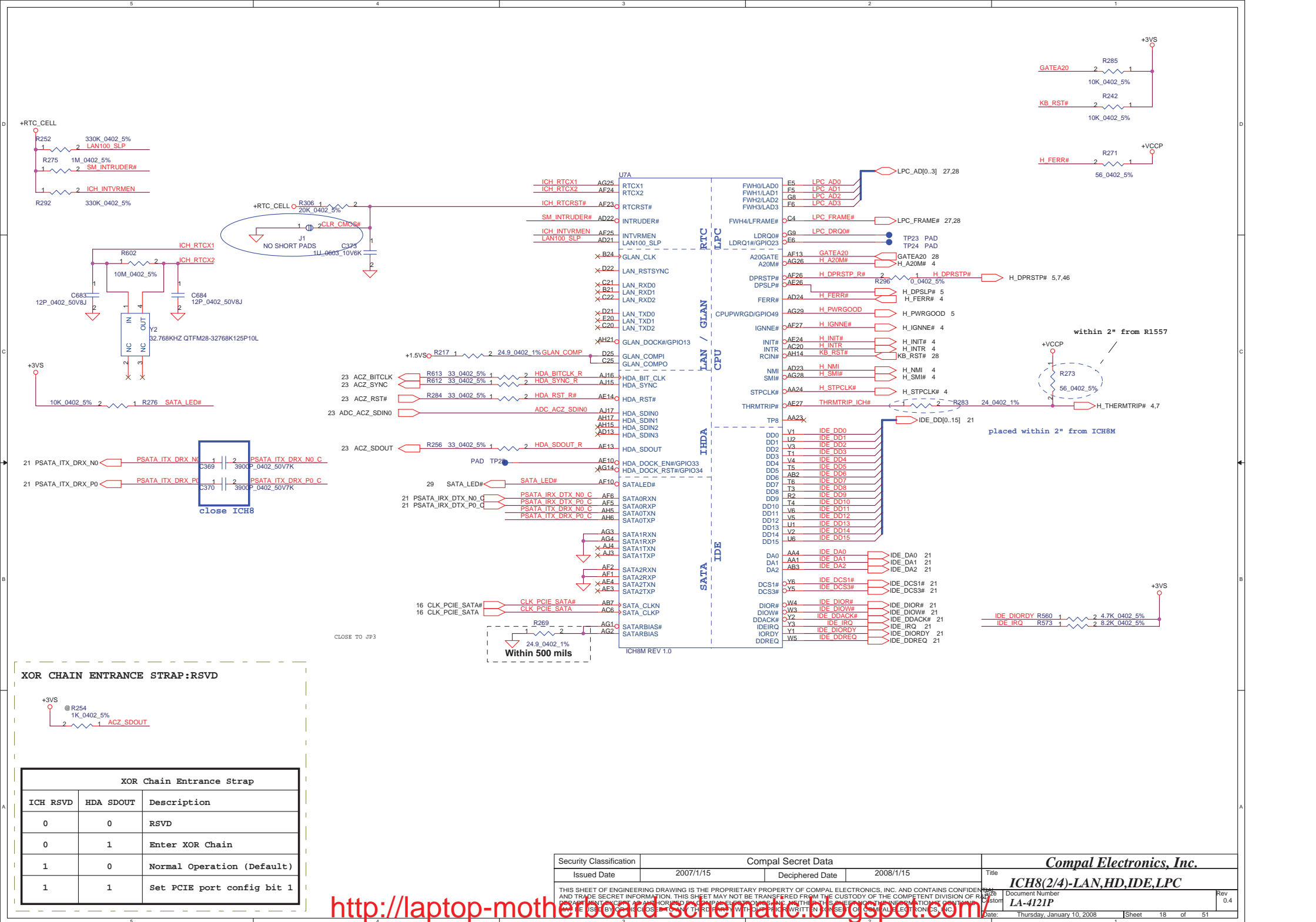


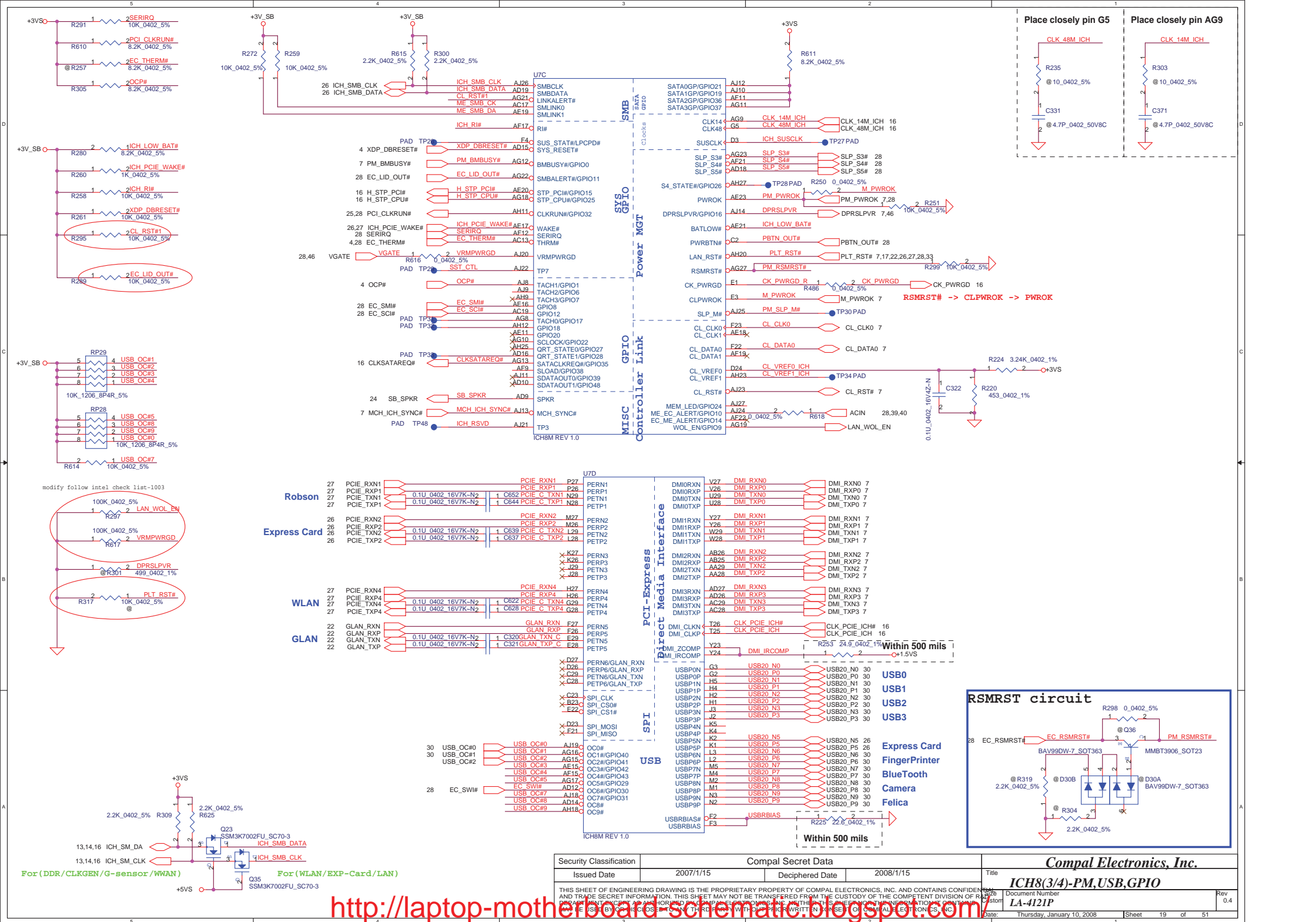
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*

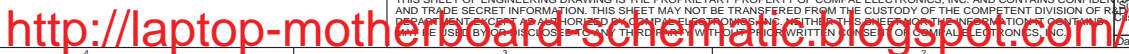


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS
0	1	SPI
1	1	LPC *(Default)

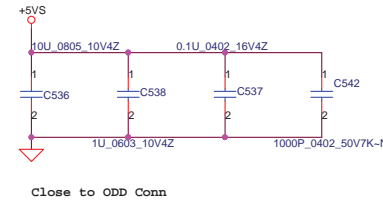
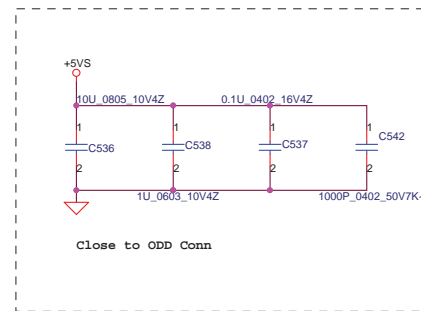






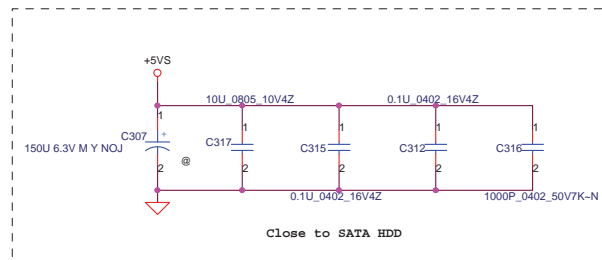


SATA HDD CONN



Close to ODD Conn

```
If CDR0M is Slave
    then SD_CSEL= Floating
else SD_CSEL= Low
```

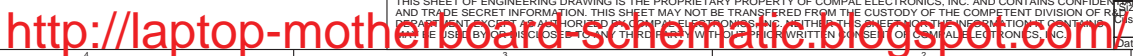


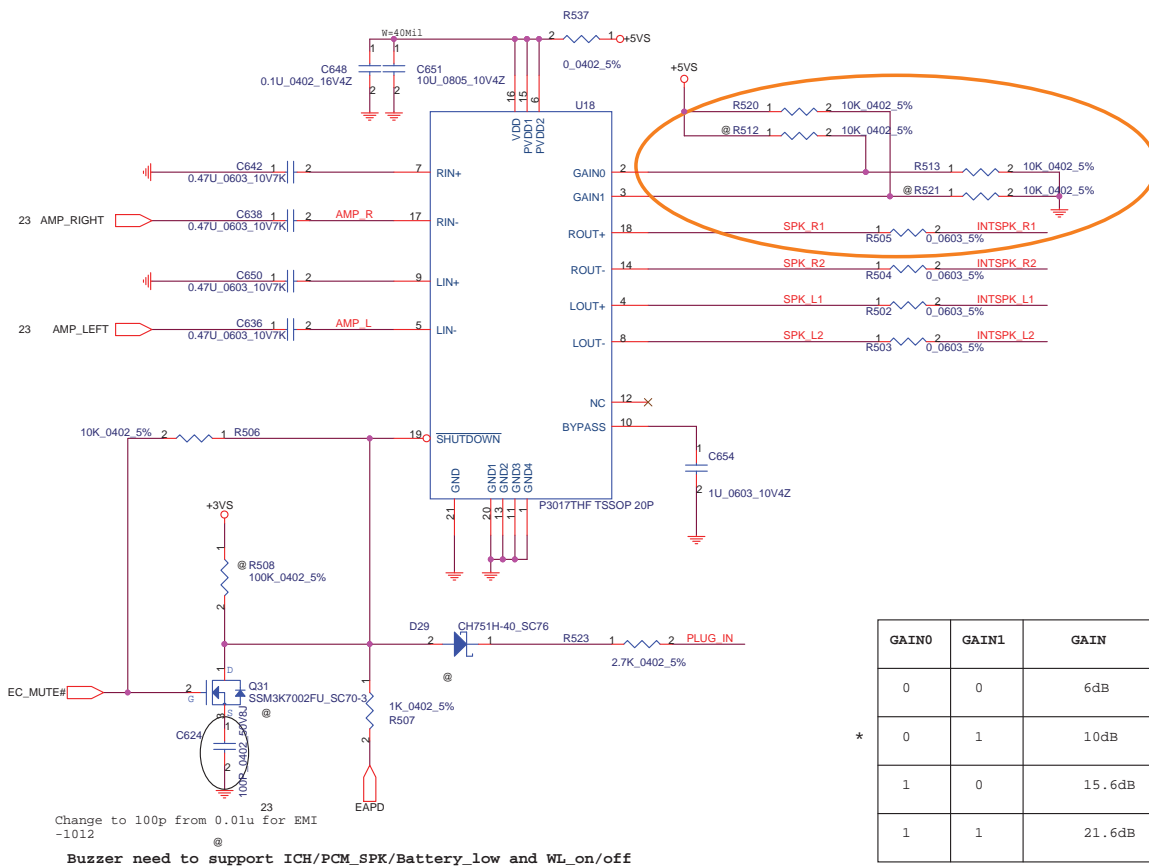
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then SD_CSEL= Floating
else SD_CSEL= Low

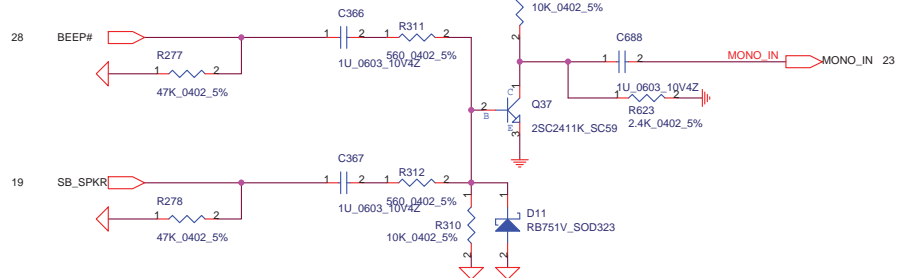
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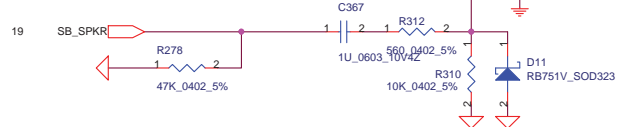




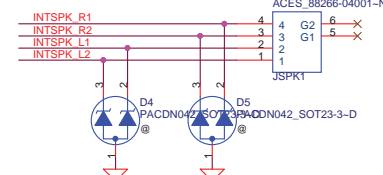
EC Beep



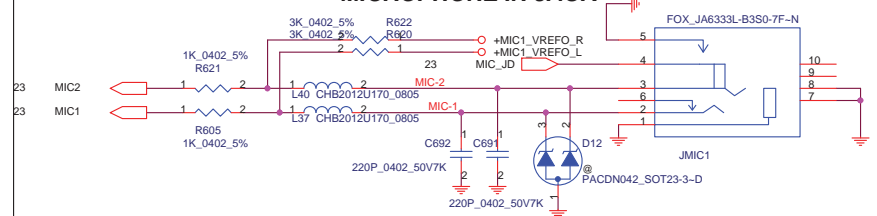
ICH Beep



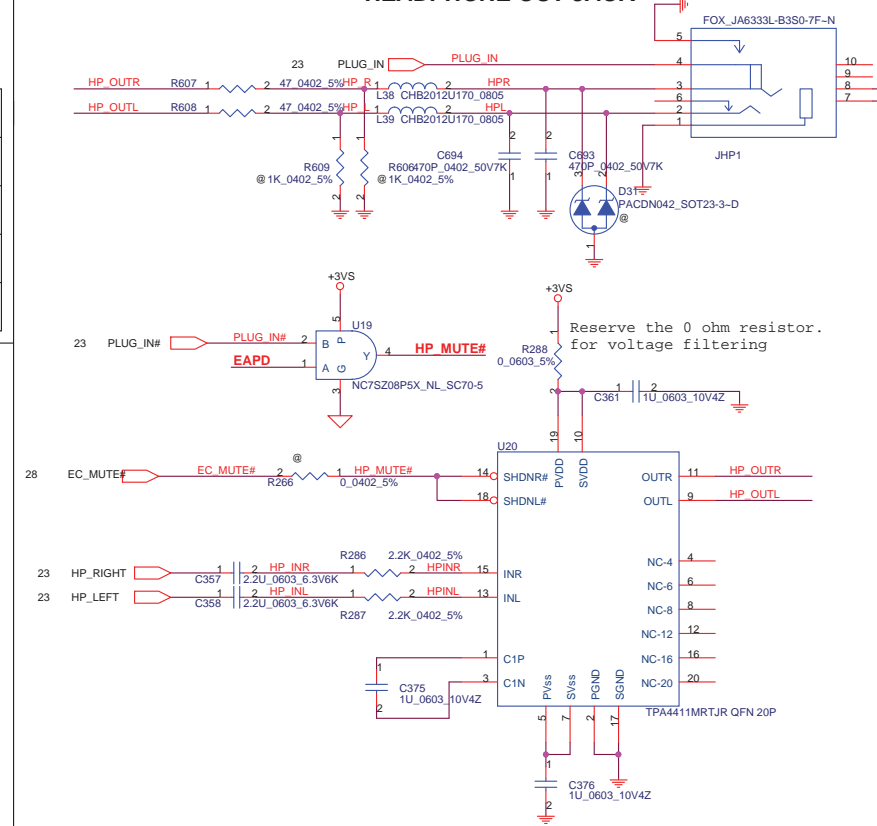
Speaker Connector



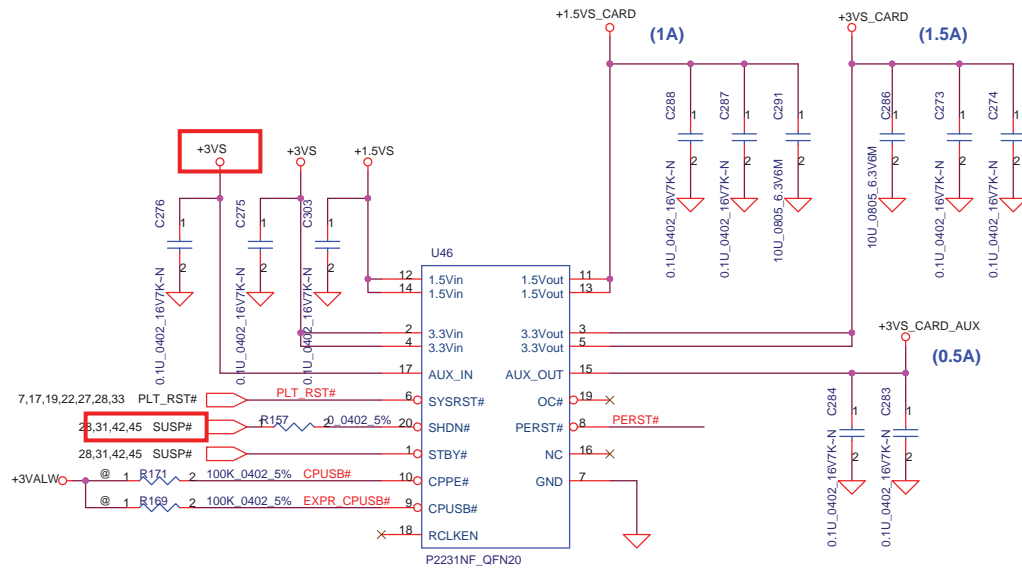
MICROPHONE IN JACK



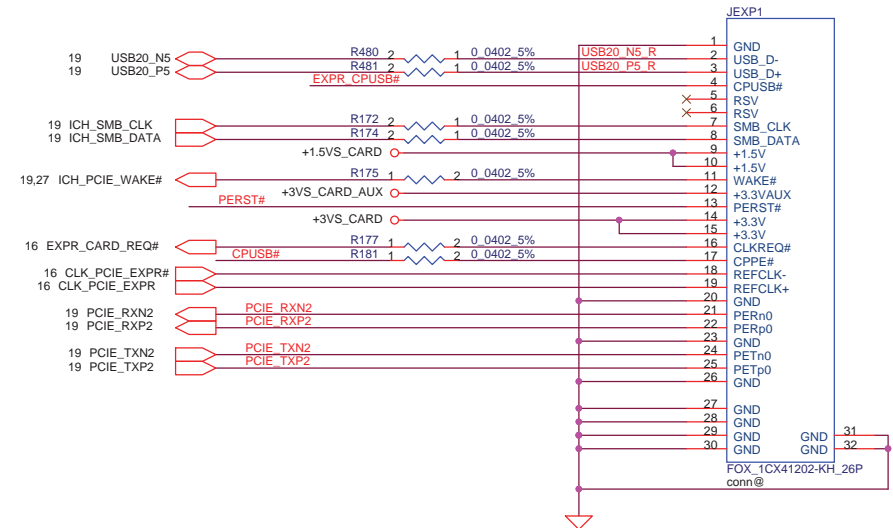
HEADPHONE OUT JACK



Express Card Power Switch



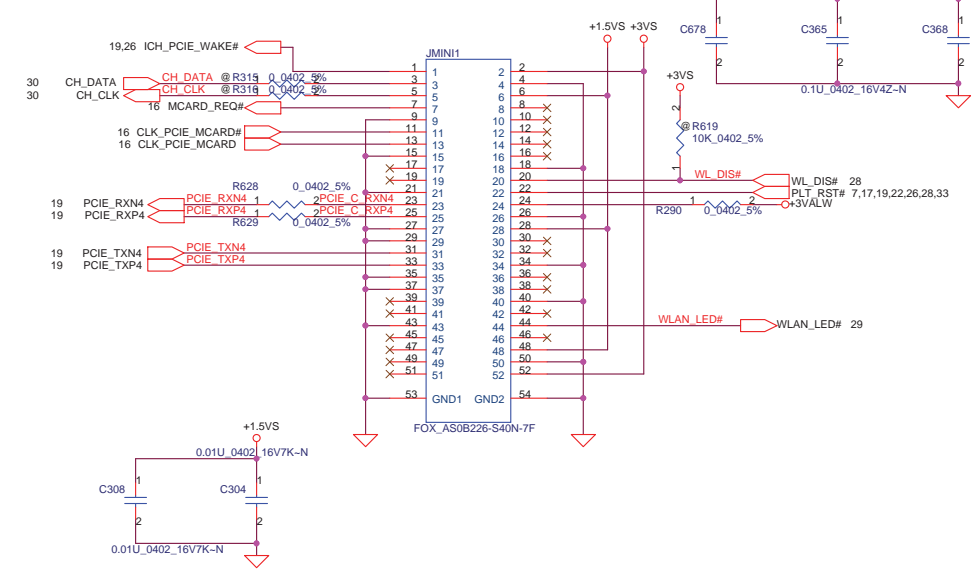
Express Card



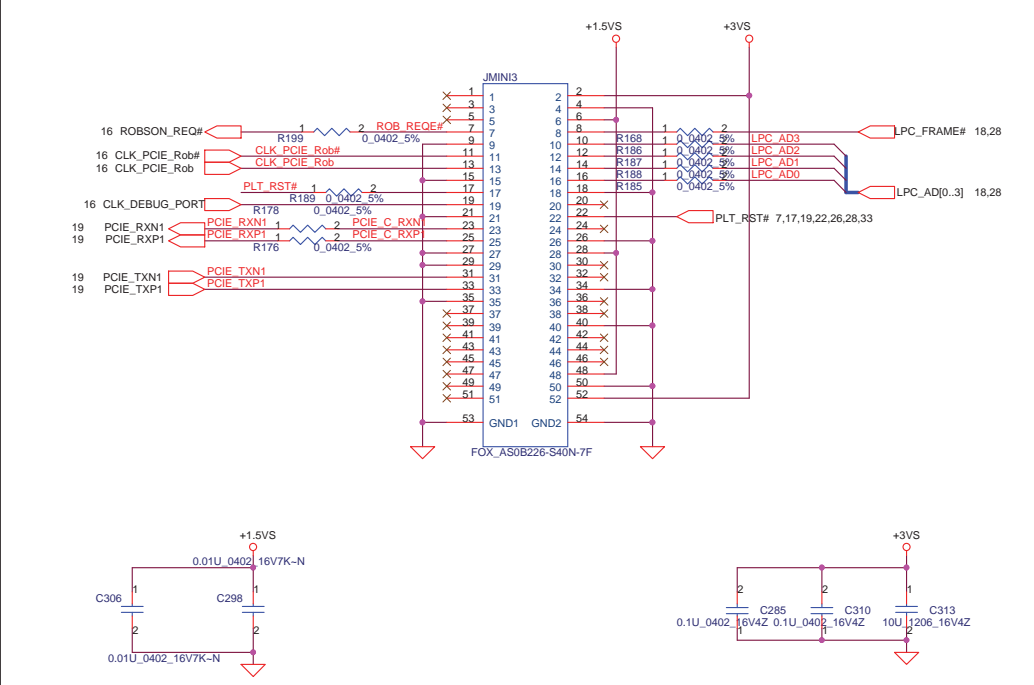
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Issued Date				2007/1/15				Deciphered Date			
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				Document Number				LA-4121P			
				Date				Thursday, January 10, 2008			
				Sheet				26 of 51			
				Rev				0.4			

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Mini-Express Card---WLAN



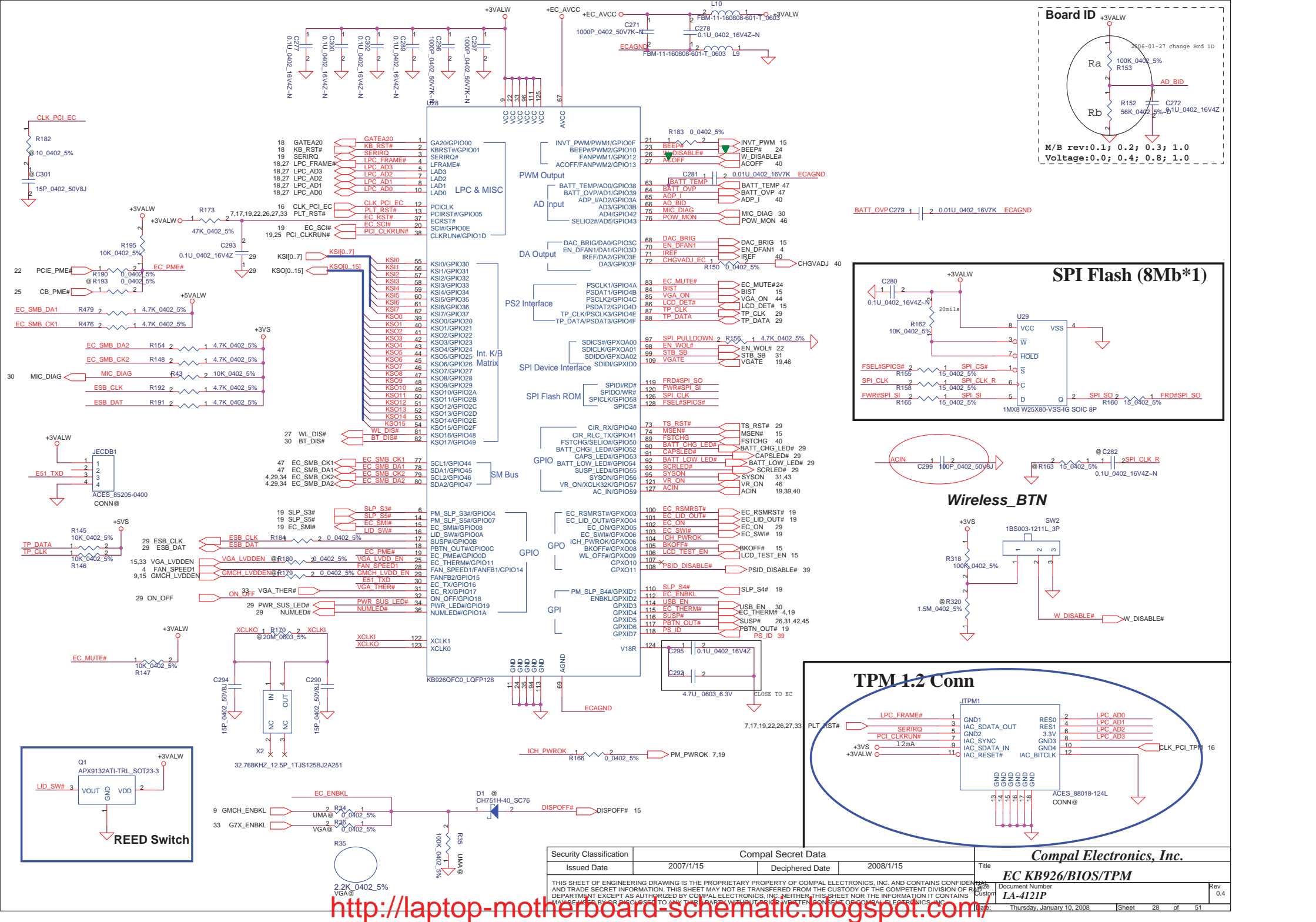
Robson

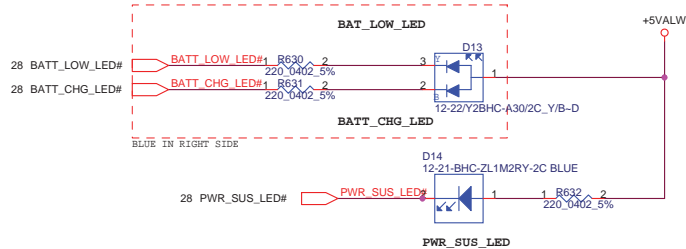
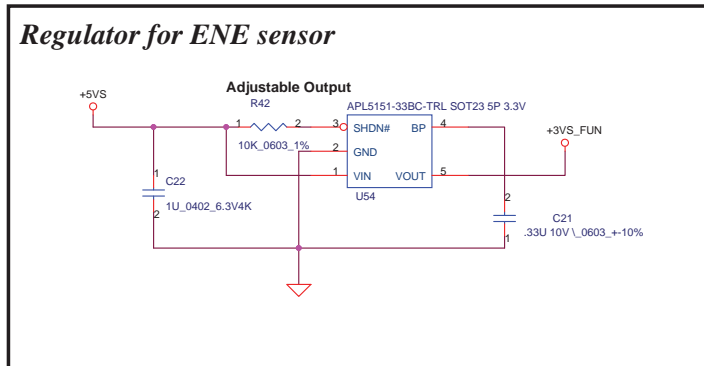
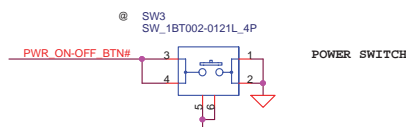
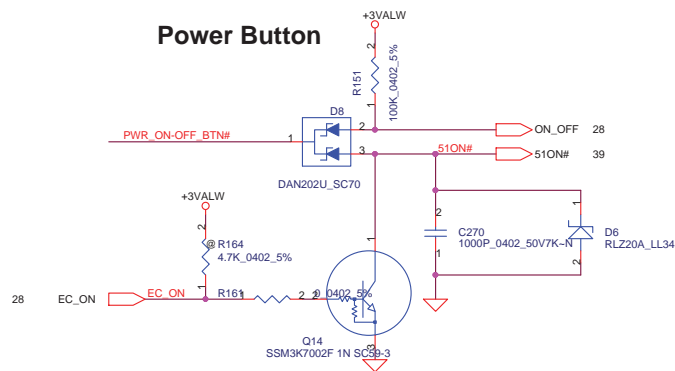


Mini-Express Card---WWAN

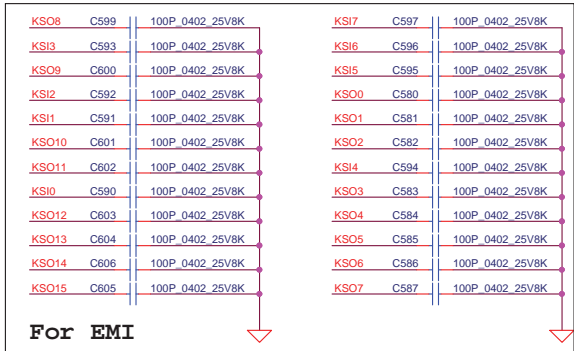
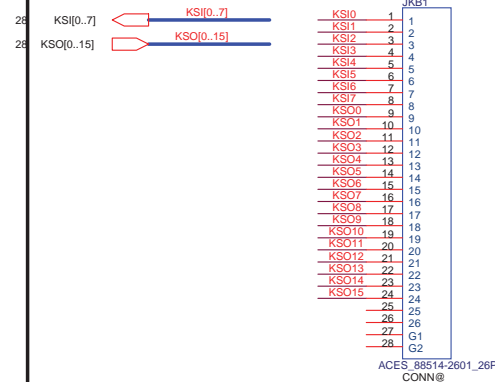
Mini-Express Card---Bluetooth

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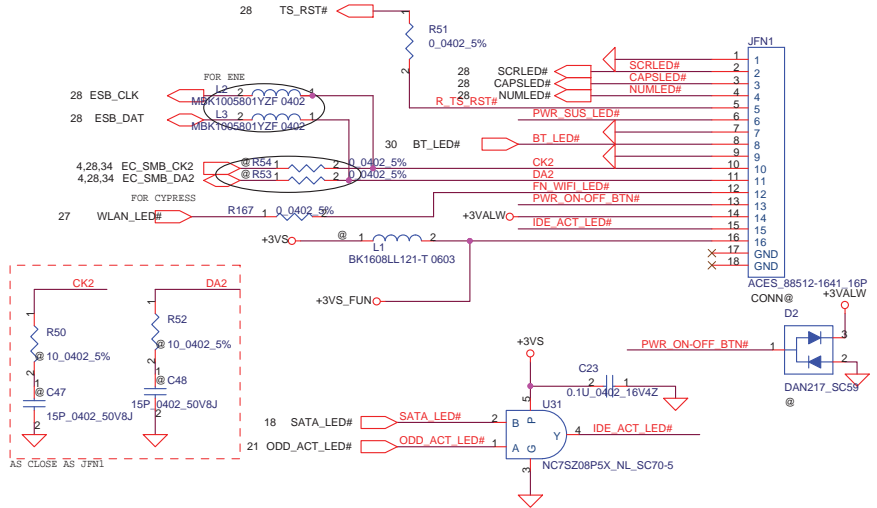




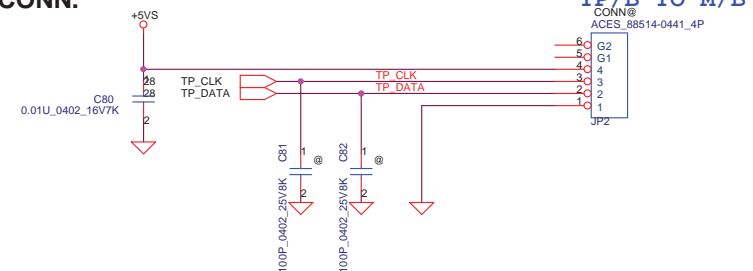
INT_KBD CONN.

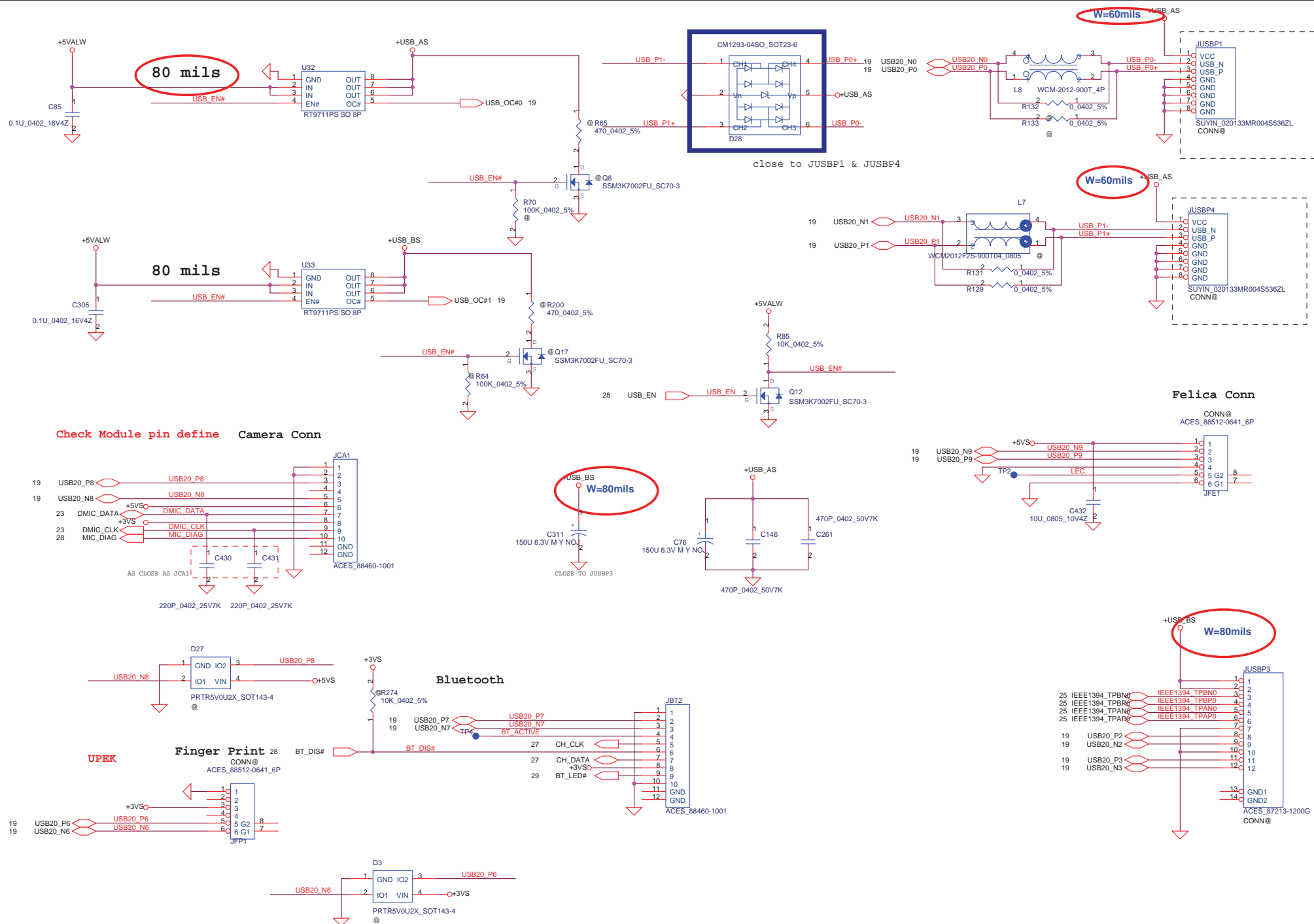


Function/B CONN.

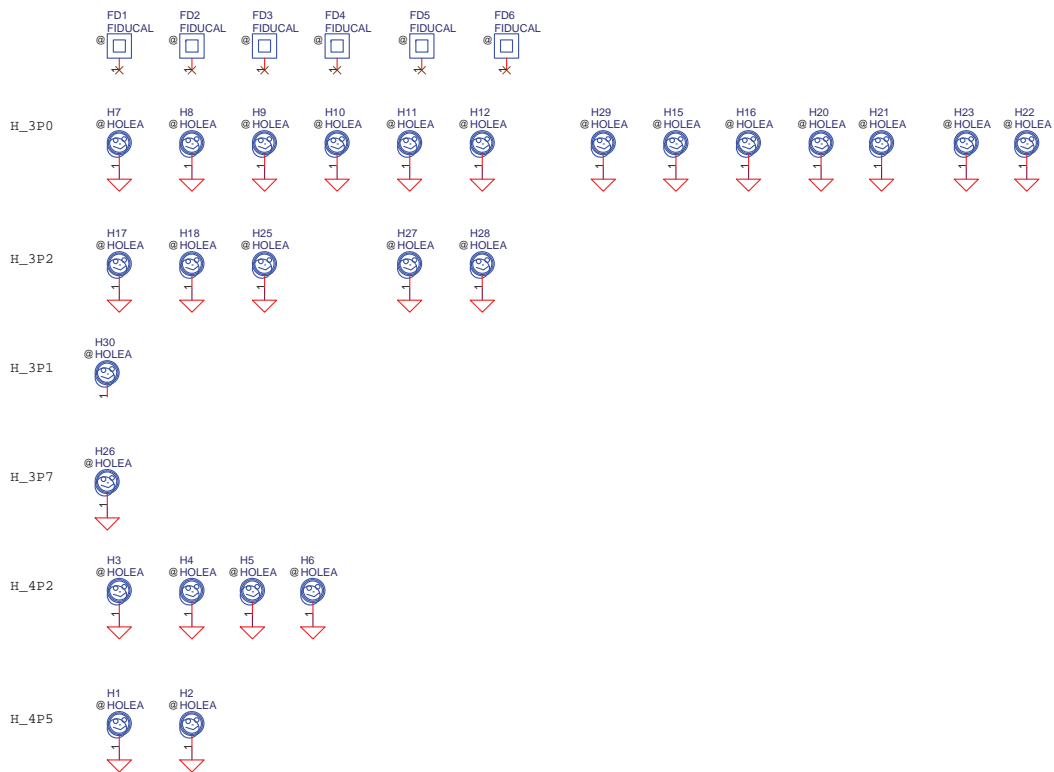


Touch PAD/B CONN.

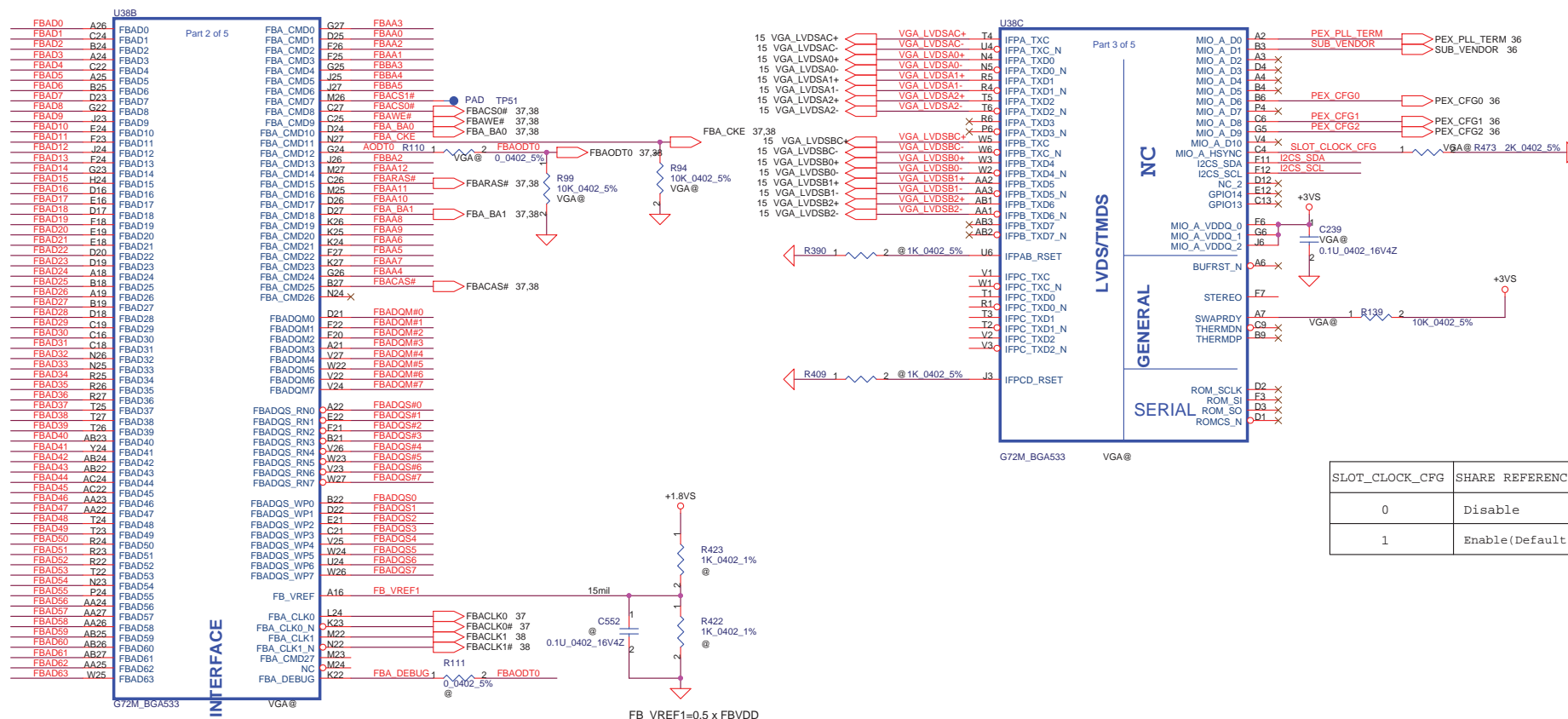




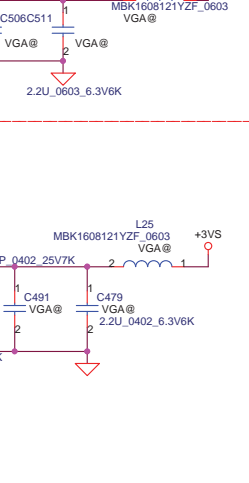
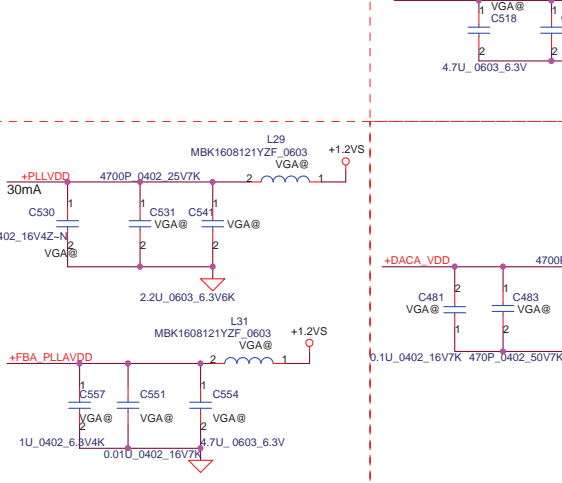
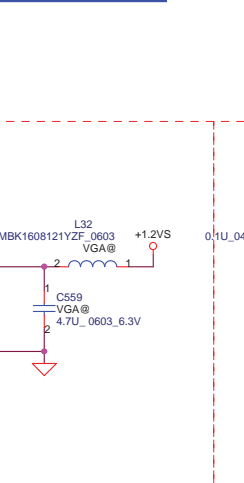
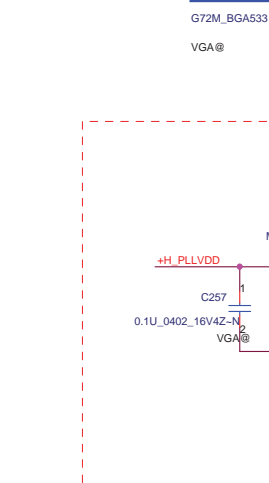
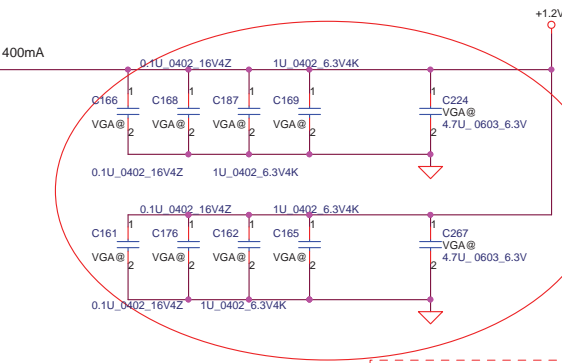
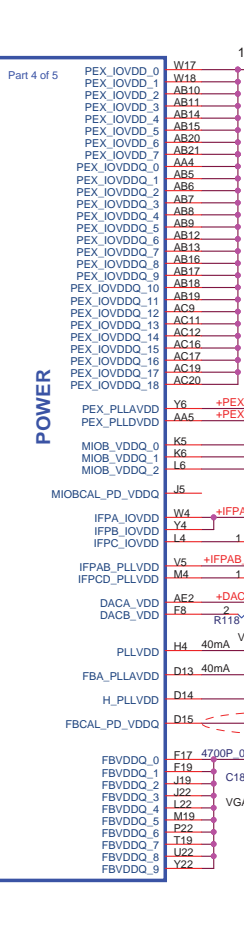
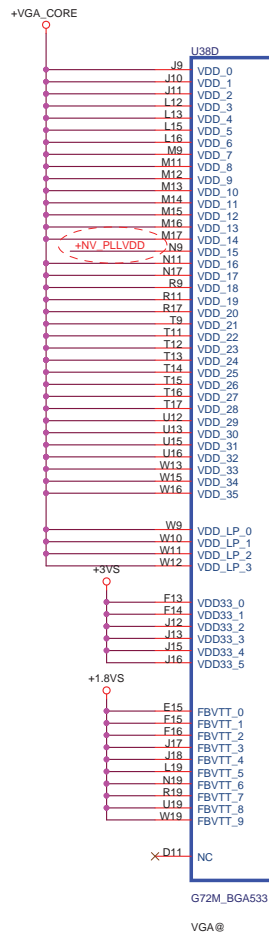
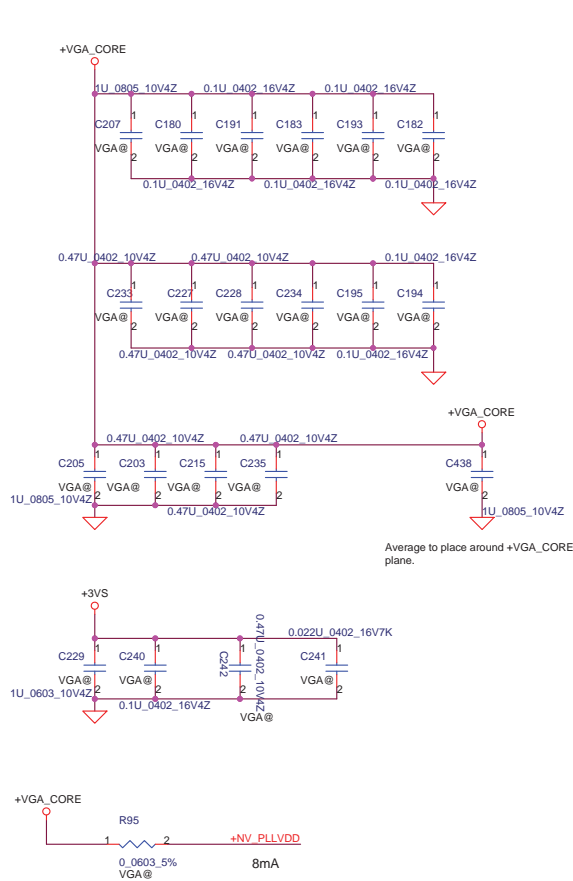
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				Rev	0.4
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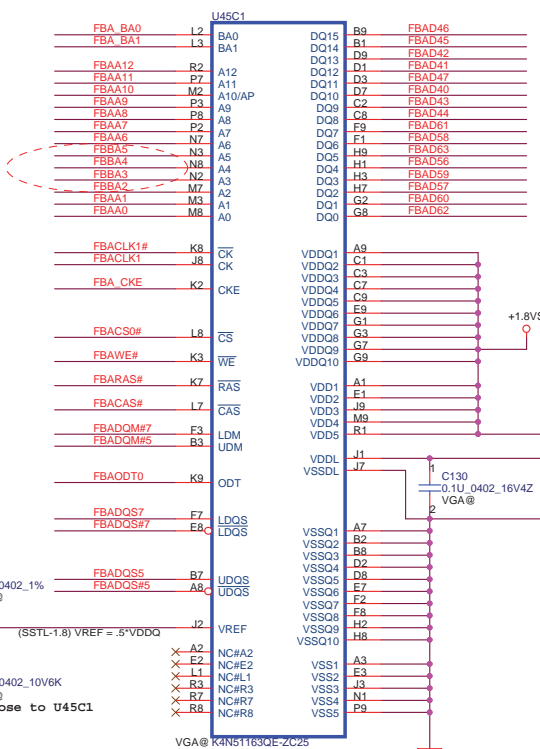
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Date: Thursday, January 10, 2008		Sheet 32 of 51			



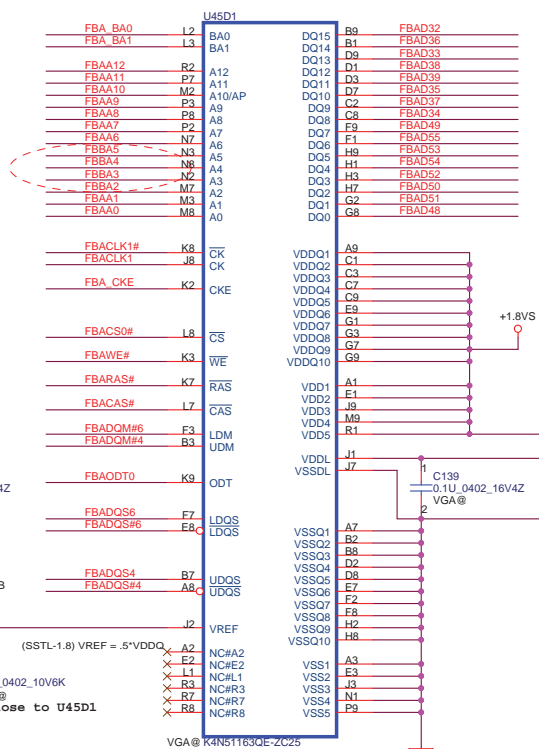
SLOT_CLOCK_CFG	SHARE REFERENCE CLOCK
0	Disable
1	Enable(Default)



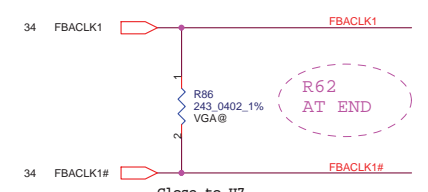
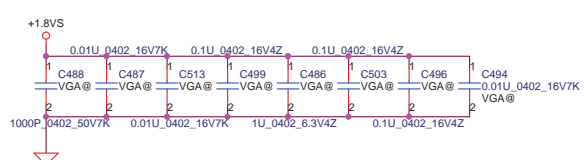
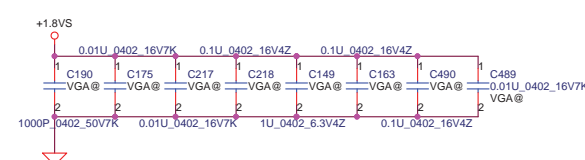
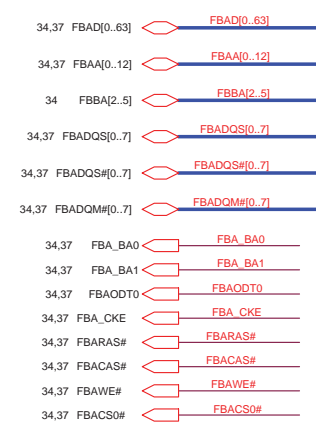
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2006/07/10				2007/07/10				NB8M-GS Power			
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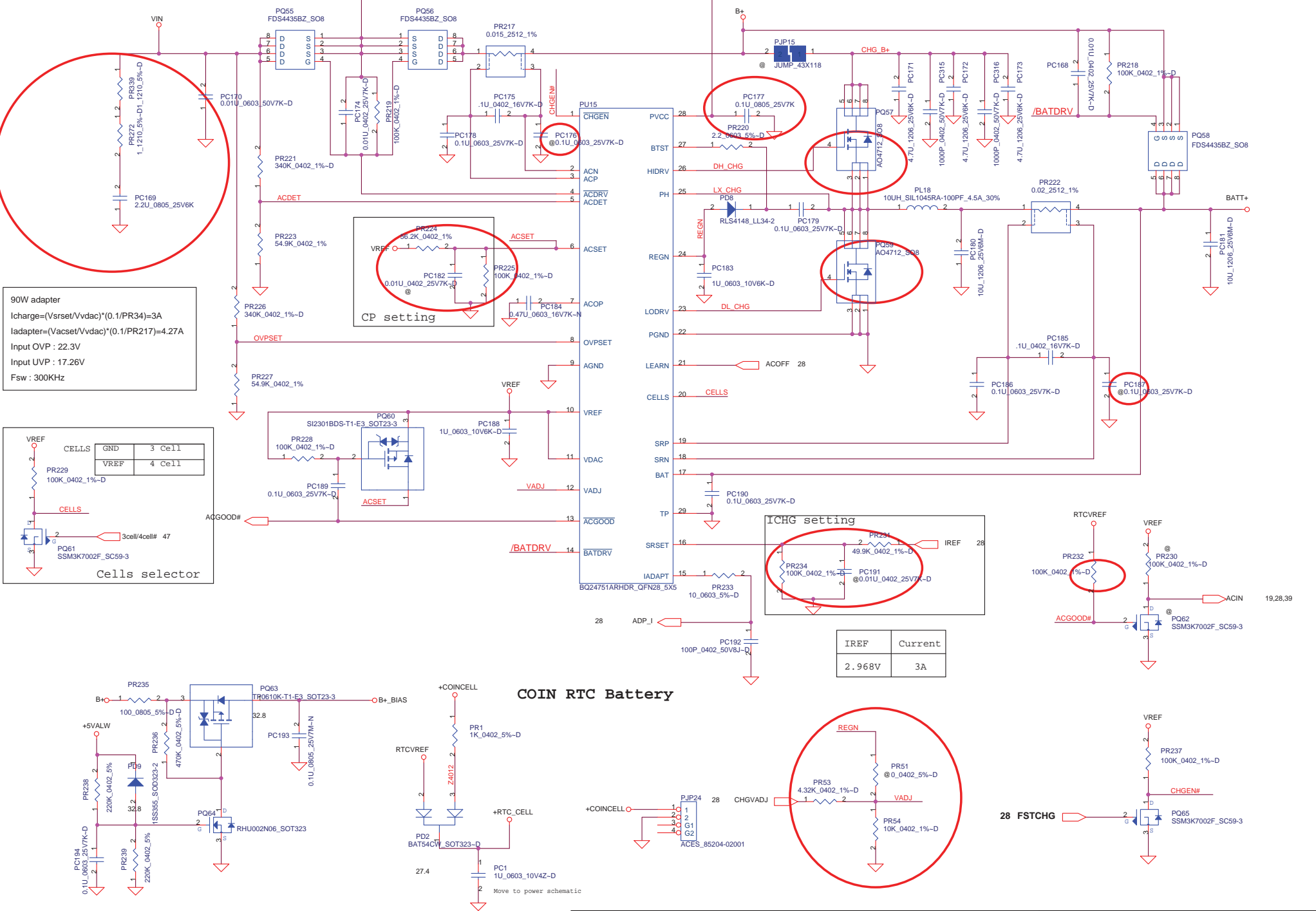
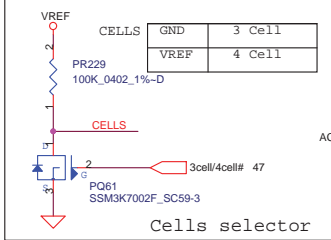
DDR2 BGA MEMORY



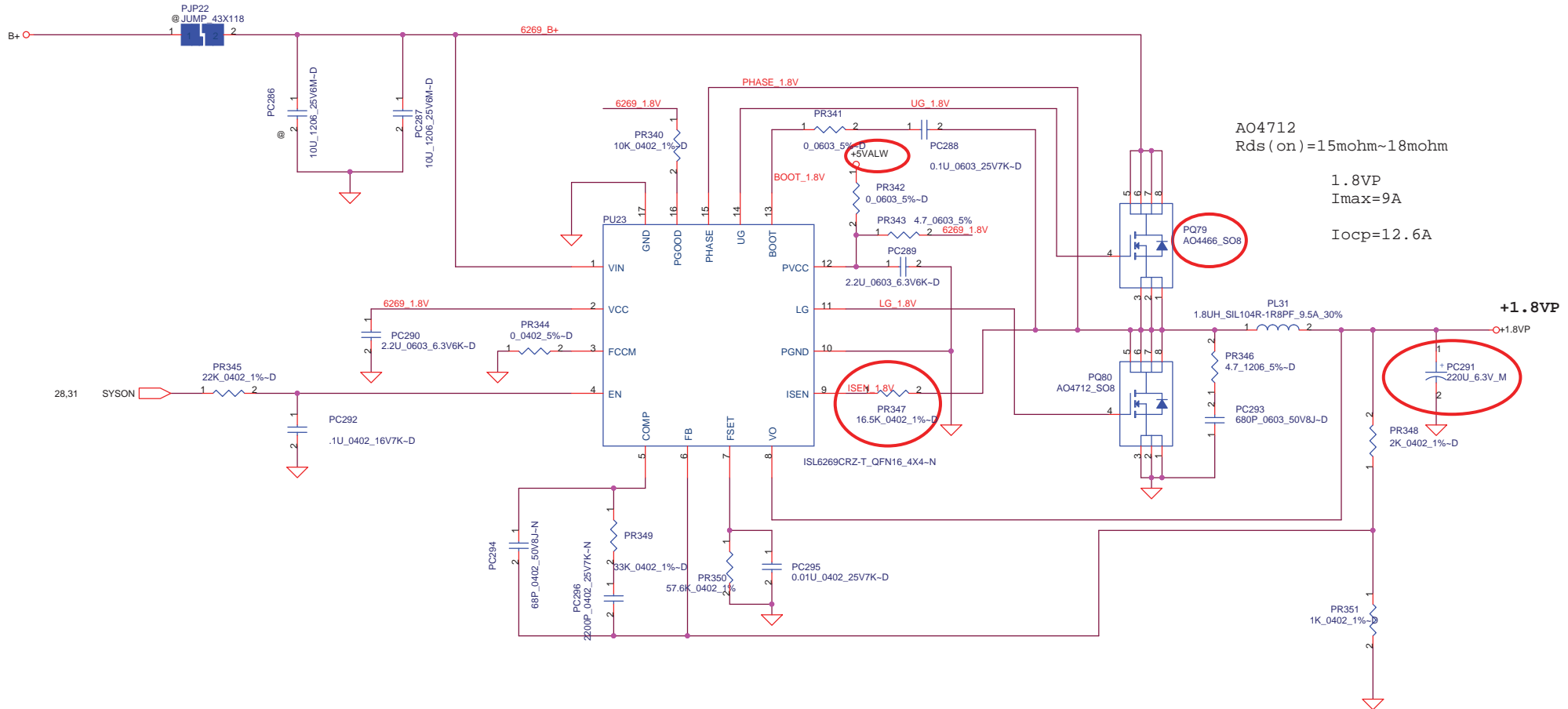
DDR2 BGA MEMORY



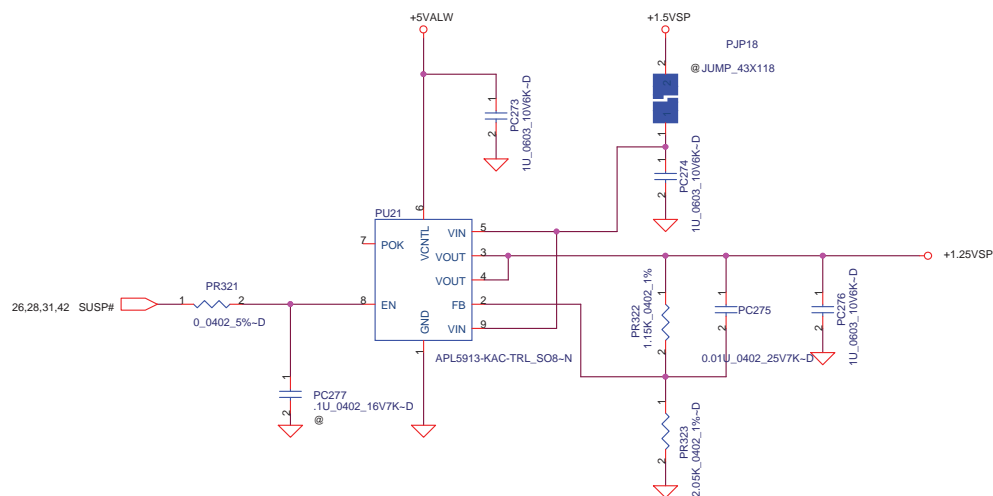
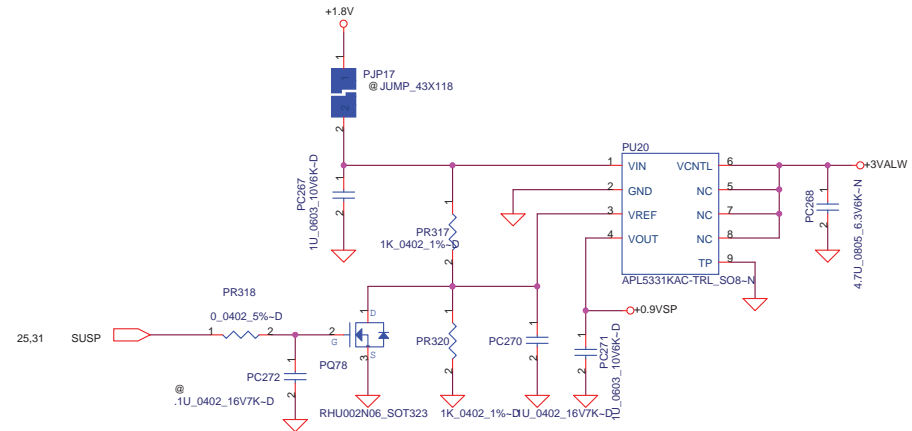
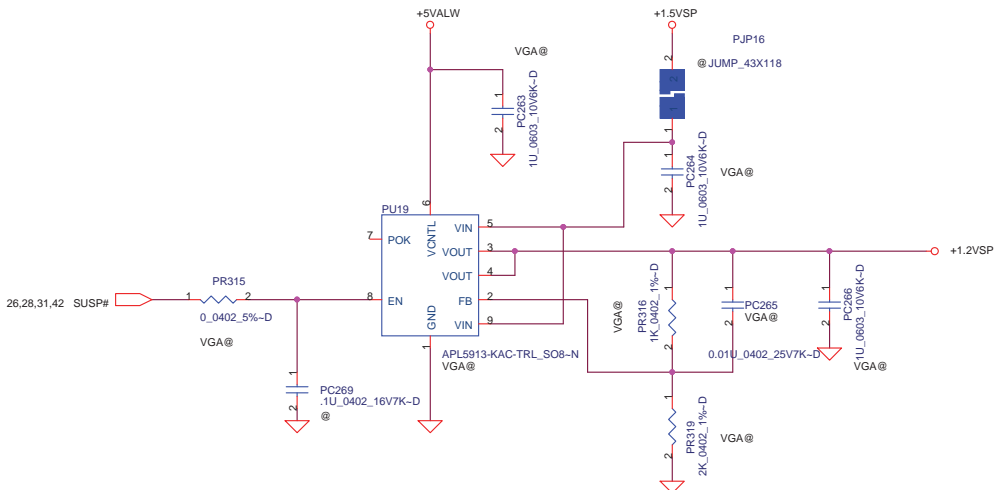
90W adapter
 $I_{charge} = (V_{srset}/V_{vdac}) * (0.1/PR34) = 3A$
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR217) = 4.27A$
 Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz



IREF	Current
2.968V	3A

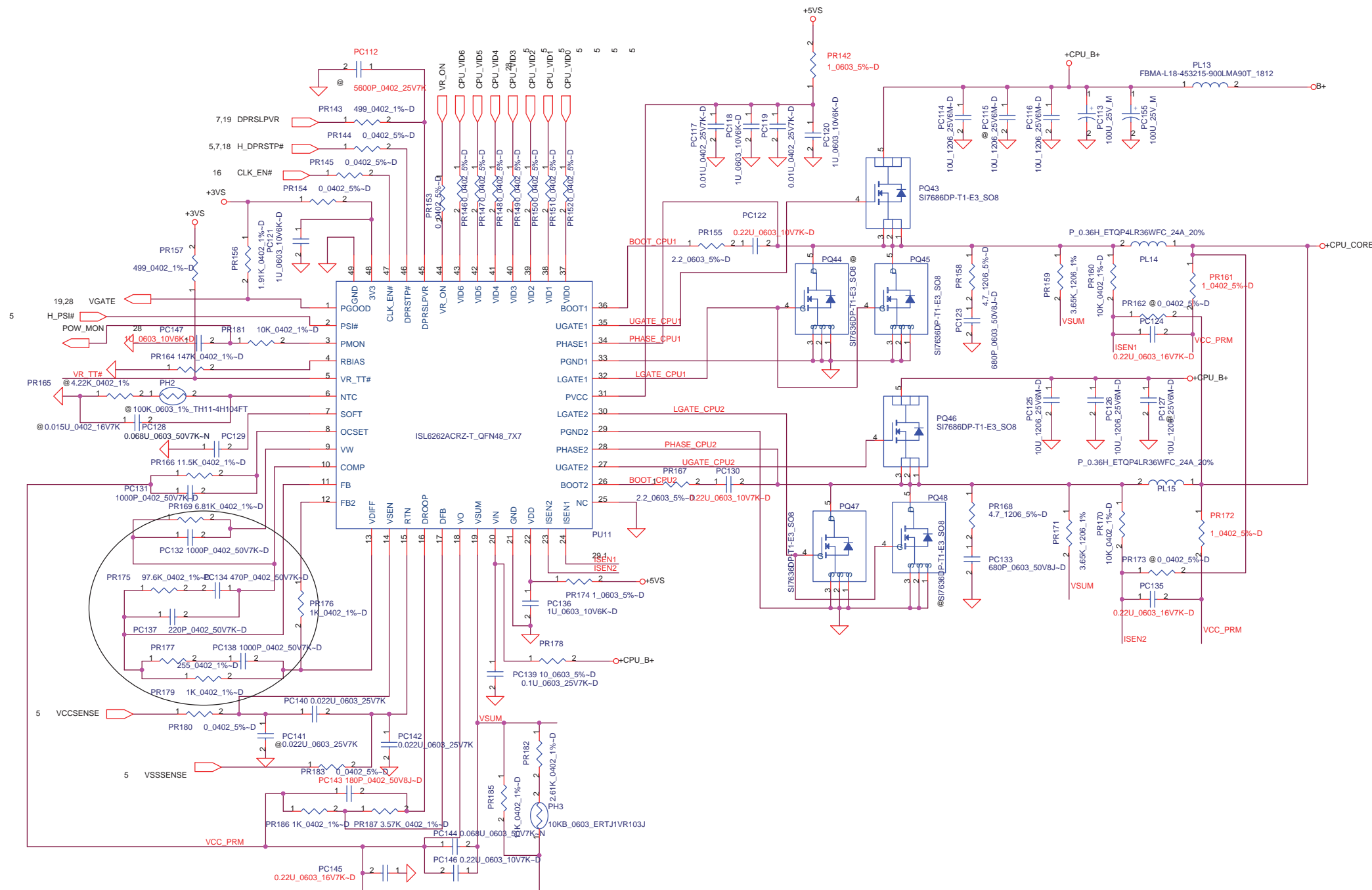


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				NB_CORE			
Size		Document Number		JAL30		Rev 0.11	
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2005/10/1				2007/05/30				+1.25VSP / +0.9VSP / +1.2VSP			
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ONLY BE USED BY COMPANY DESIGNATED WITH WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				JAL30				0.2			
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				Date	Thursday, January 10, 2008
				Sheet	46 of 51
				Rev	0.1

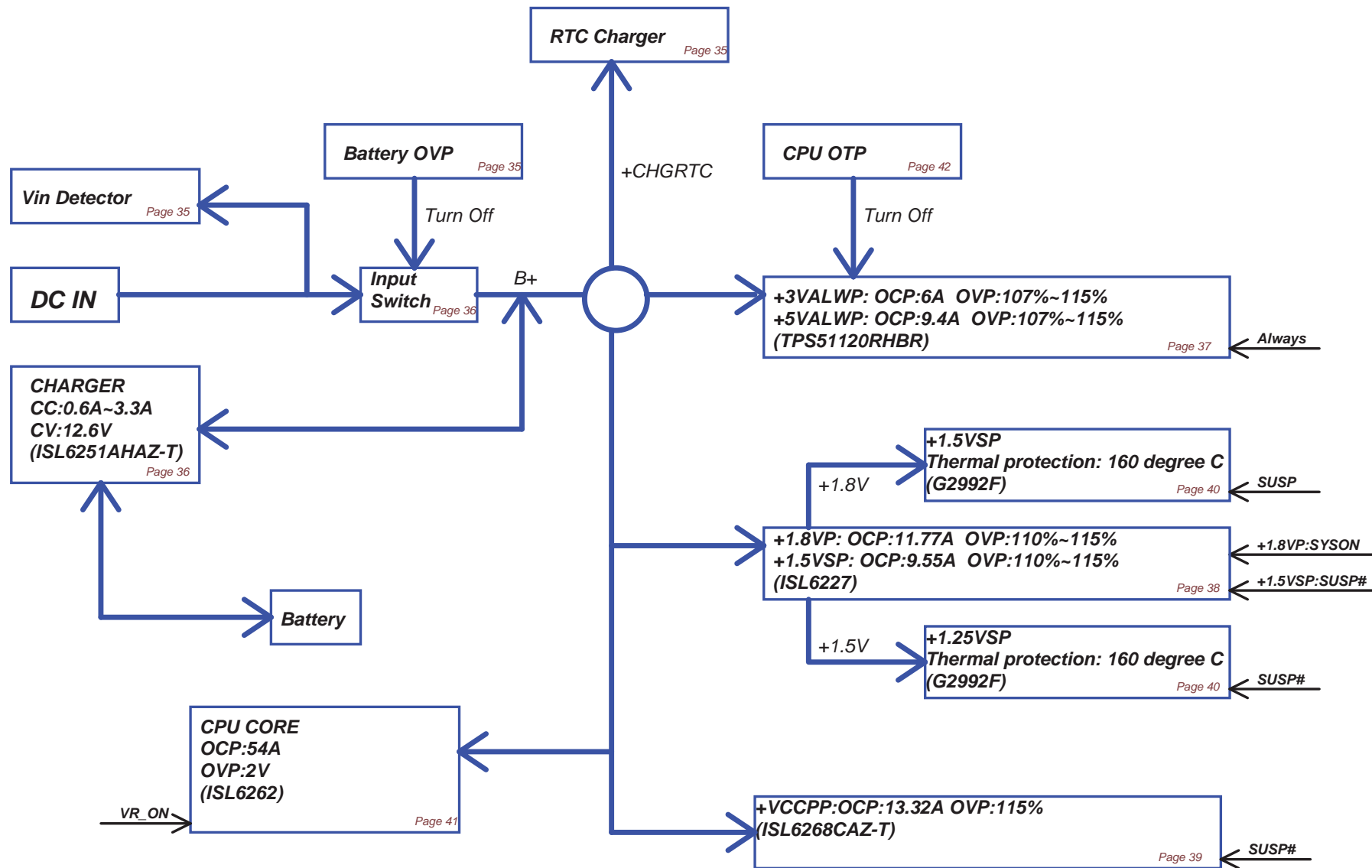
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	+3VALWP/+5VALWP	07/11/19	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD PQ76 to turn off 5VALWP wehn shut down the system in the DC-mode	
2	40	Charge	07/11/25	COMPAL	Change RTC circuitry part	del PD16 PC285 PL29 JRTC1	
3	40	Charge	07/11/25	COMPAL	change charge voltage can to adjust	ADD PR53 PR54	
4	40	Charge	07/11/25	COMPAL	increase Coin RTC battery circuitry	ADD PD2 PR1 PC1	
5	40	Charge	07/11/25	COMPAL	increase BQ24751 Vin Detector function	increase PR232	
6	40	Charge	07/12/26	COMPAL	change charge voltage can to adjust	Change PR53 from 15K to 4.3K	
7	42	1.5VSP/+VCCPP	07/12/26	COMPAL	adjust 1.5VSP/+VCCPP OCP set	Change PR271 PR276 PR278 PR282 from 9.09K to 12.1K	
8	43	1.8VP	07/12/26	COMPAL	adjust 1.8VP OCP set	Change PR347 from 12.1K to 16.5K	
9	44	VGA_CORE	07/12/26	COMPAL	adjust VGA_CORE OCP set	Change PR358 from 12.1K to 16.5K	
10	41	+3VALWP/+5VALWP	07/12/26	COMPAL	The schematic location doesn't correspond to PCBA	Change location from PQ76 to PQ74	
11	43	1.8VP	07/12/26	COMPAL	delete resistor 0ohm for HW request	DEL PR342	
12	44	VGA_CORE	07/12/26	COMPAL	delete resistor 0ohm for HW request	DEL PR354	
13	46	CPU_CORE	07/12/26	COMPAL	modify MOS type S08 to Power Pack for height limit	DEL PQ44 PQ48	
14	43	1.8VP	08/01/04	COMPAL	In order to replace IC for system request	ADD PU23 PR342	
15	44	VGA_CORE	08/01/04	COMPAL	In order to replace IC for system request	ADD PU24 PR354	
16	41	+3VALWP/+5VALWP	08/01/04	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD PD16 to turn off 5VALWP wehn shut down the system in the DC-mode	
17	40	Charge	08/01/04	COMPAL	adjust battery charge voltage set	CHANGE PR53 from 15K to 4.3K	
18	40	Charge	08/01/04	COMPAL	VIN Detector has the same function	DEL PR230 PQ62	
19							
20			08/01/04	COMPAL	Increase Resistor on charge boot for EMI request	CHANGE PR220 PR286from 0 to 2.2 ohm	
21			08/01/04	COMPAL	Increase Capacitor on charge boot for EMI request	ADD PC123 PC133 PC231 PC237 PC309 PC310 PC311 PC313 PC312 PC314 PC293	
22			08/01/04	COMPAL	Increase Resistor on charge boot for EMI request	ADD PR158 PR168 PR285 PR281 PR346	
23			08/01/04	COMPAL	Increase Bead on charge boot for EMI request	ADD PL17 PL28	
24							
25							
26							
27							
28							
29							
30							
31							
32							

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Date: Thursday, January 10, 2008				Sheet	48 of 51

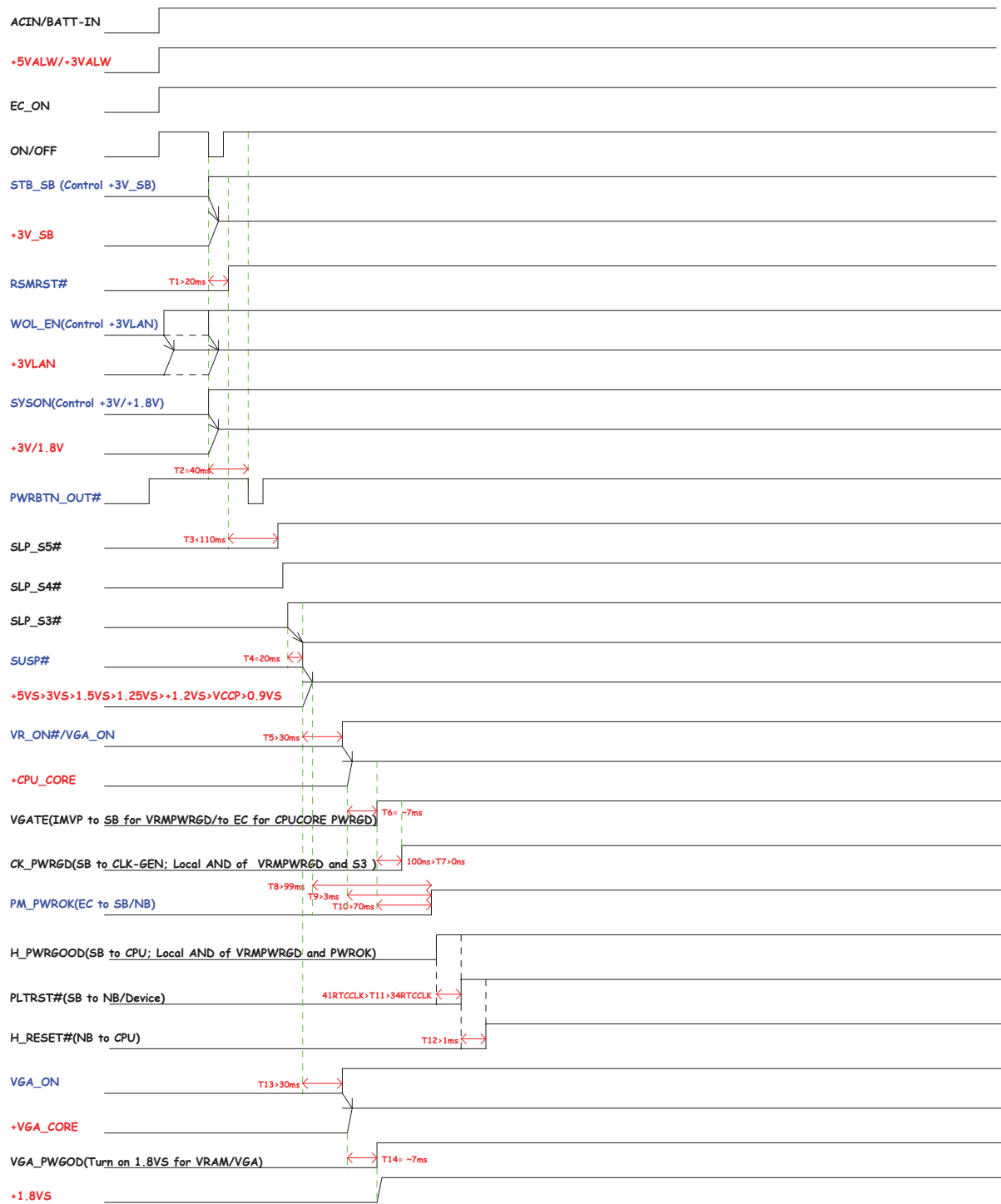
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	24	P24-Mini-Card/WWAN/Roboson	2007/2/3	Compal HW	LED1 Pin3 and Pin4 swap cause BATT_LOW_LED# no function.	Correct LED1 footprint to LED_HT-297UD-CB_4P	0.2 (SW1-13.3*)
2	22	P22-Gigabit LAN(BCM5787M)	2007/2/3	Compal HW	+3VLAN voltage abnormally	Add Q46 for B+_BIAS turn on	0.2 (SW1-13.3*)
3	19	P19-ICH8(3/4)_DMI,USB,GPIO,PCIE	2007/2/3	Compal HW	R121 no need for INTEL no reserve	Un mount R121	0.2 (SW1-13.3*)
4	19	P22-Gigabit LAN(BCM5787M)	2007/2/13	Compal HW	Can't install MAC to EEPROM due to VCC 2.04V only	Change R4 to 0ohm or short R4.	0.2 (SW1-13.3*)
5	29	P29-EC KB926/REED SW/TPM1.2	2007/3/1	Compal HW	KB matrix error by use AK1 KB circuit	Modify to SW1 KB pin define	0.2 (SW1-13.3*)
6	27	P27-CardBus/R5C803	2007/3/1	Compal HW	CB_PME# pull high of two kind power plan (+3V & +3V_SB)	Un-mount R419	0.2 (SW1-13.3*)
7	32	P32-DC/DC Interface	2007/5/11	Compal HW	No VGAPOWERGOOD for turn on +1.8VS	Add pull hish +3VS for VGA_PWGOD	0.2
8	11	P11-CRESTLINE(5/6)-PWR/GND	2007/5/11	Compal HW	VCCP no power	Remove C140(0 ohm in VGA BOM)	0.2
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JAL30 Power Bock



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