

Thurman Discrete VGA nVidia G86 Schematics Document

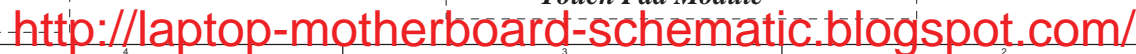
uFCPGA Mobile Merom

Intel Crestline-PM + ICH8M

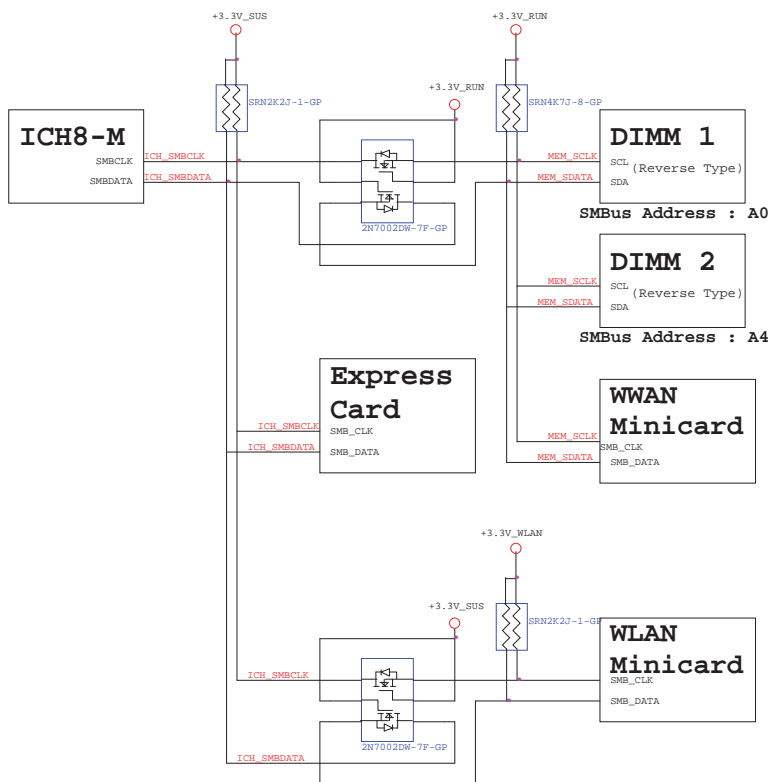
2007-11-06

REV : -1(DELL:A00)

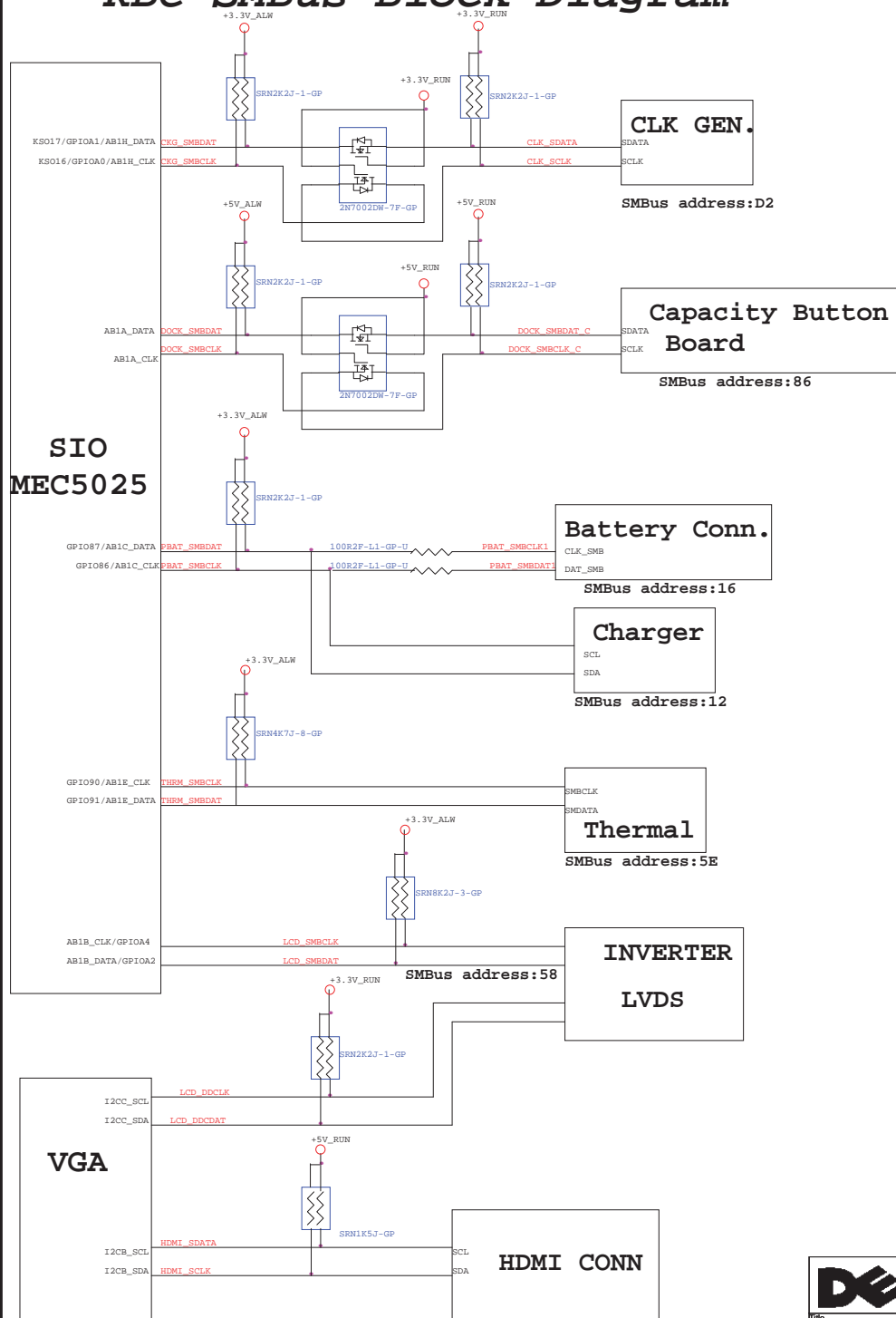
Project code:91.4C301.001
PCB P/N :06247
REVISION :-1



ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 10

Bit5 S1	Bit4 S0	Spread Spectrum S(110)
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

PIN34	0 UMA	1 DISC.
FCTSEL1		
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSusi_05 VccSusi_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSusi_05,VccSusi_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

INTEL CRESTLINE STRAP PIN

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation*	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation*

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	10/100 LOM

ICH USB TABLE

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/MediaCard	AD17	C D	1	1

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

XOR Chain Entrance Strap		
ICH_RSVDtp3	AZ DOUT ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	high = default
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	DCT
1	1	LPC(Default)


Integrated VccSusi_05,VccSusi_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

<http://laptop-motherboard-schematic.blogspot.com/>

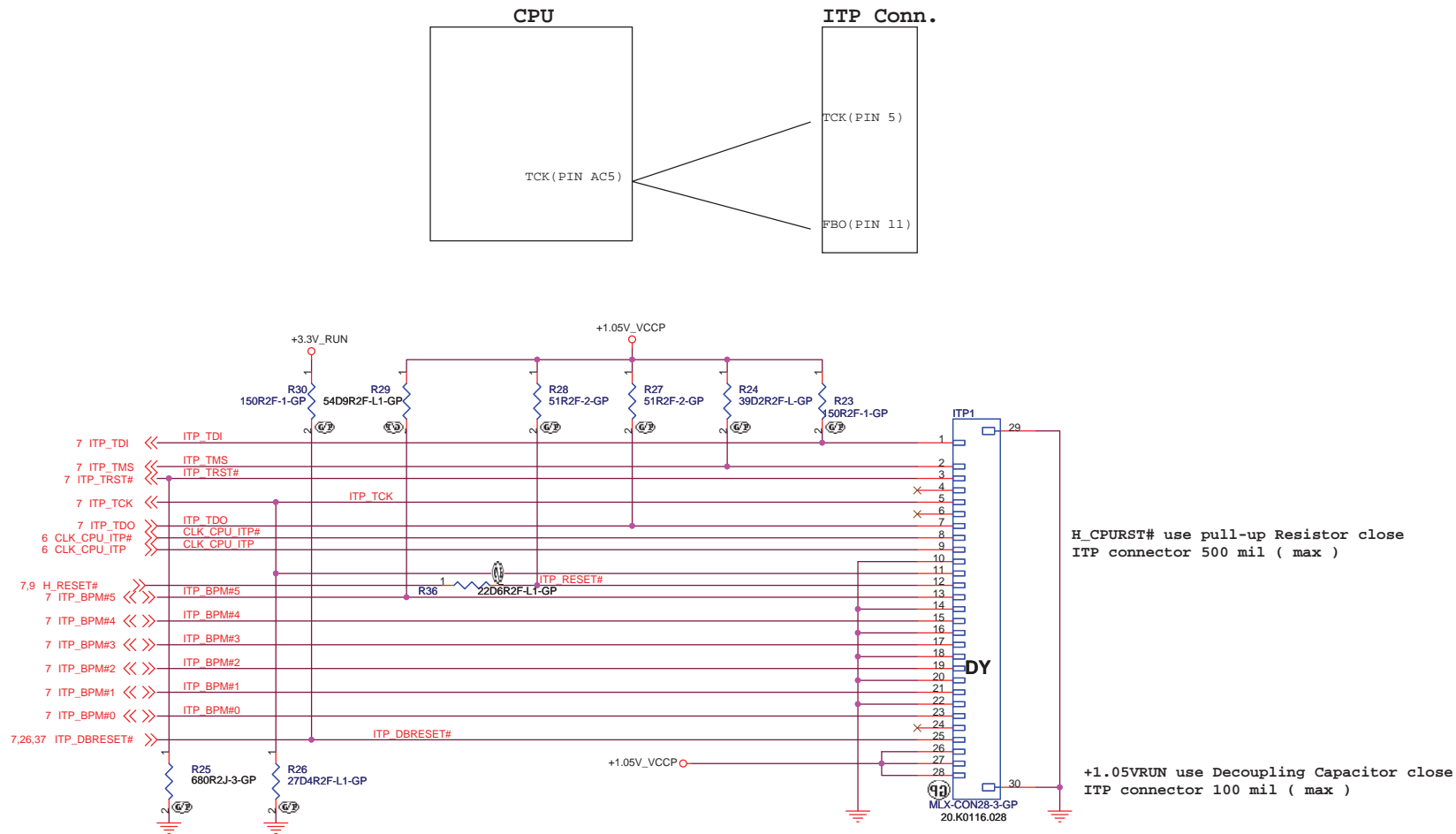


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

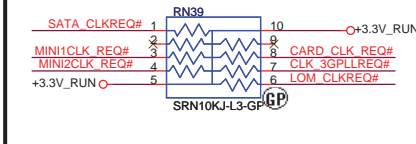
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Size: **A3** Document Number: **Table of Content** Rev: **-1**

Date: Tuesday, November 06, 2007 Sheet 4 of 50



ITP Debug Conn.




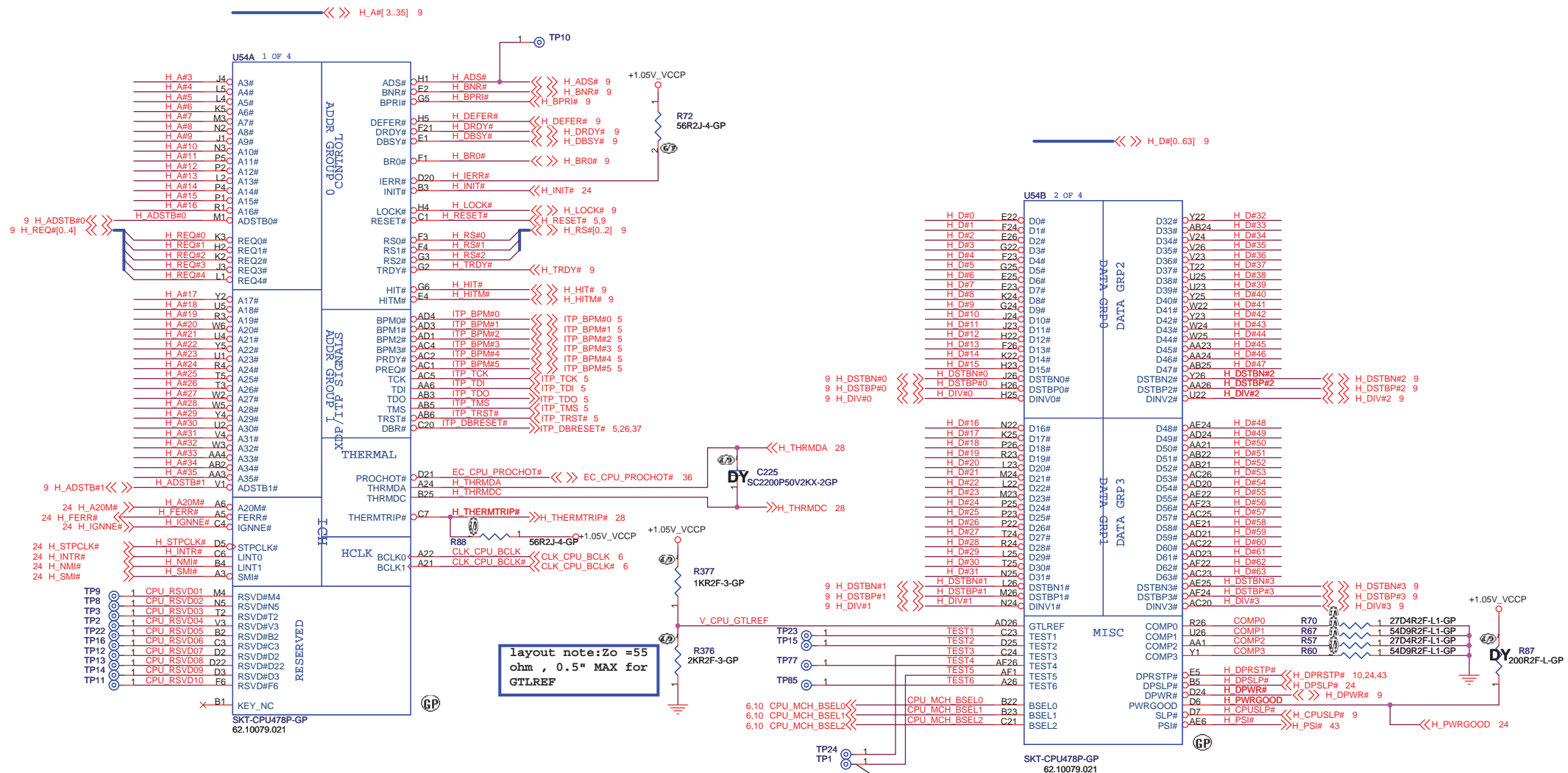
SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

CLK_VGA_27M_NSS_OPTION		
	G72	NB8M
R198	147 ohm 64.14705.6DL	33 ohm
R448	84.5 ohm	no-stuff
clk. Voltage	1.2V	3.3 V

PIN9 PGMODE	PIN39 DISCRIPTION
0	VTT_PWRGD#/PD
1	CKPWRGD/PD#(DEFAULT)

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

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Size	Document Number	Rev	
A3	CLK_GEN CY28547	-1	
Date:	Tuesday, November 06, 2007	Sheet	6 of 50

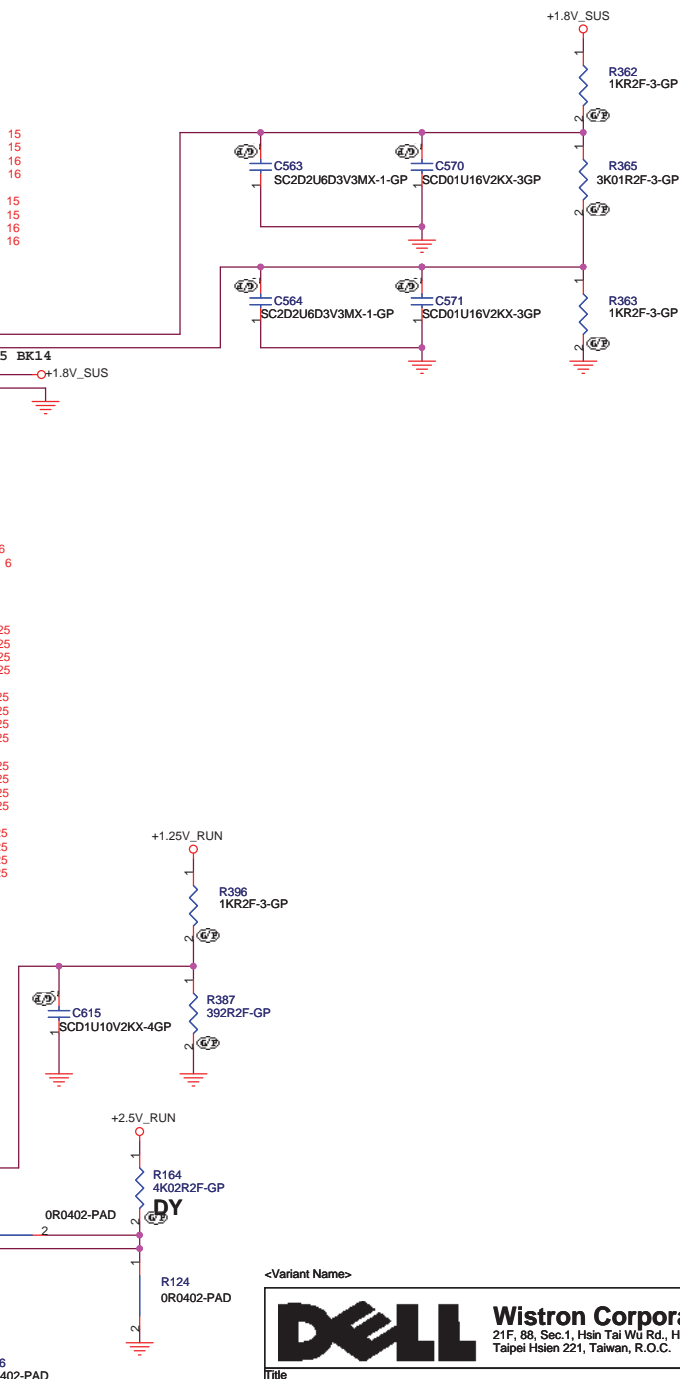
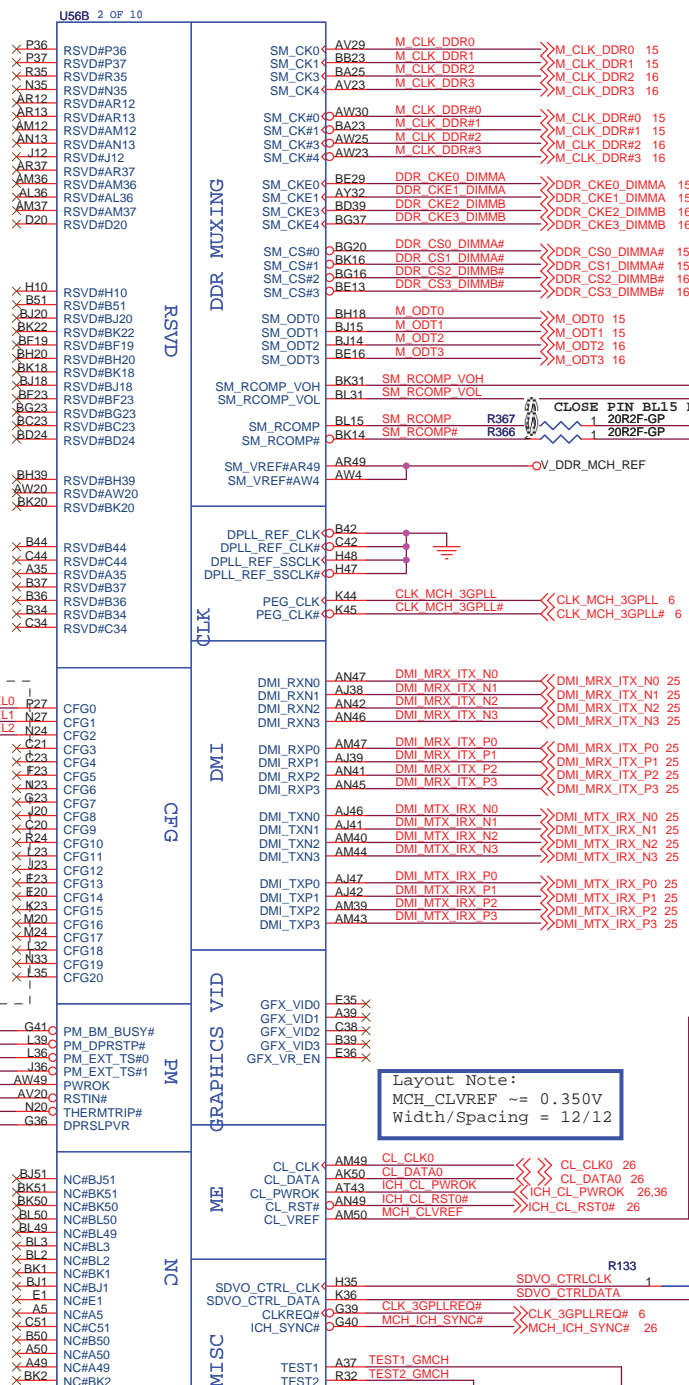
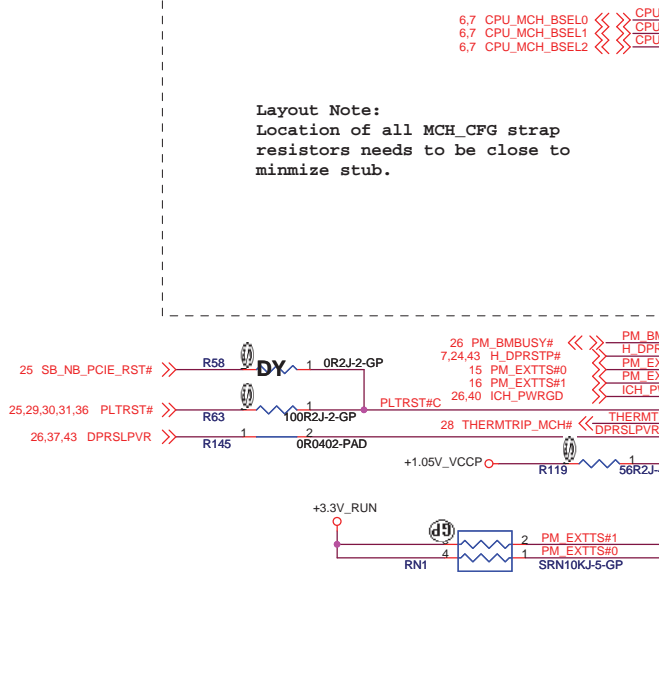


* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation*
	CFG[2..0] FSB Select
LHL	FSB 800
LHH	FSB 667
Other	Reserved

Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minimize stub.

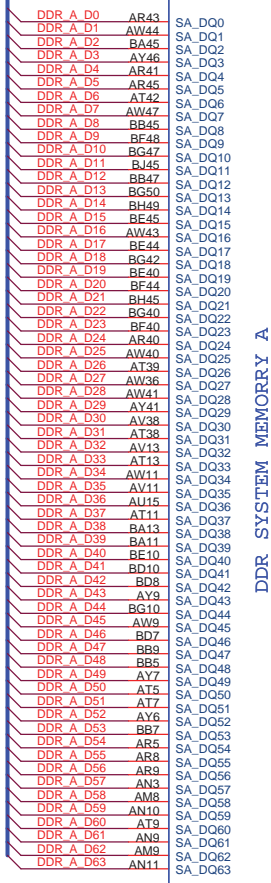


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Size	Document Number		Rev
A3	<i>GMCH-DMI/DDR (2/6)</i>		-1
Date:	Monday, November 12, 2007	Sheet 10 of	50

15 DDR_A_D[0.63] <<>> DDR_A D[0.63]



CRESTLINE-GP-U-NF

DDR_A BS[0.2] <<>> DDR_A_BS[0.2] 15

16 DDR_B_D[0.63] <<>> DDR_B D[0.63]

DDR_A CAS# <<>> DDR_A_CAS# 15

DDR_A DM[0.7] <<>> DDR_A_DM[0.7] 15

DDR_A DQS[0.7] <<>> DDR_A_DQS[0.7] 15

DDR_A DQS#[0.7] <<>> DDR_A_DQS#[0.7] 15

DDR_A MA[0.14] <<>> DDR_A_MA[0.14] 15

DDR_A RAS# <<>> DDR_A_RAS# 15

DDR_A WE# <<>> DDR_A_WE# 15

TP6

TP5

TP4

TP3

TP2

TP1

TP0

TP7

TP8

TP9

TP10

TP11

TP12

TP13

TP14

TP15

TP16

TP17

TP18

TP19

TP20

TP21

TP22

TP23

TP24

TP25

TP26

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TP32

TP33

TP34

TP35

TP36

TP37

TP38

TP39

TP40

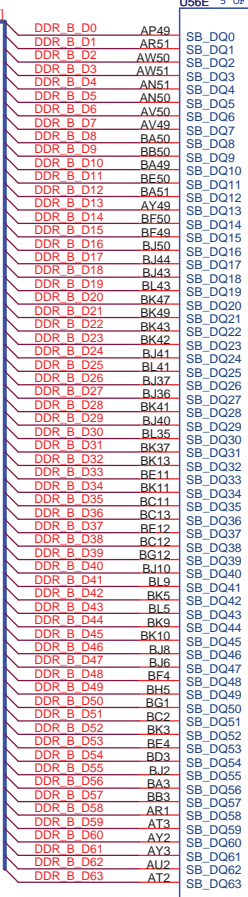
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TP42

TP43

TP44

TP45

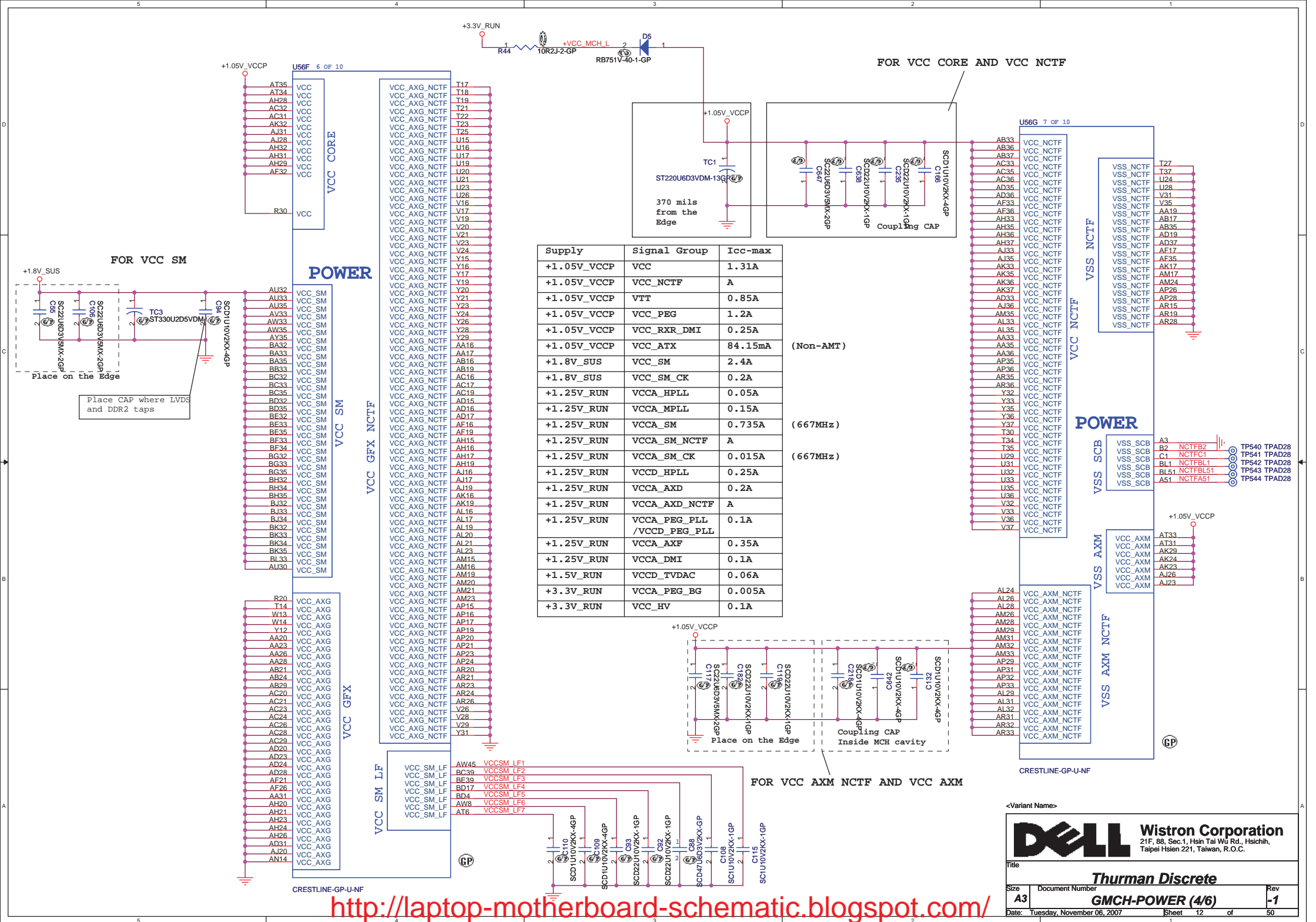


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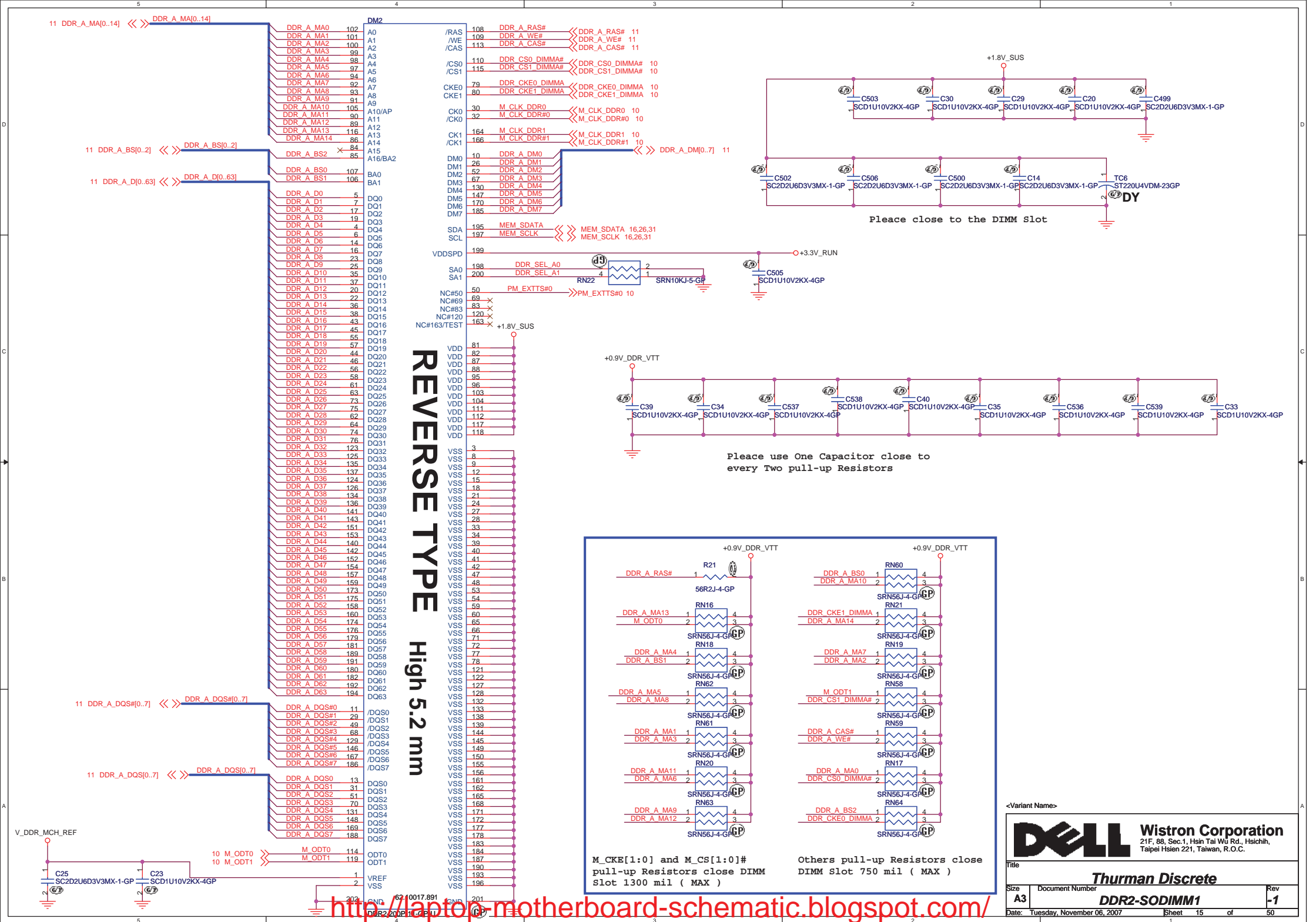
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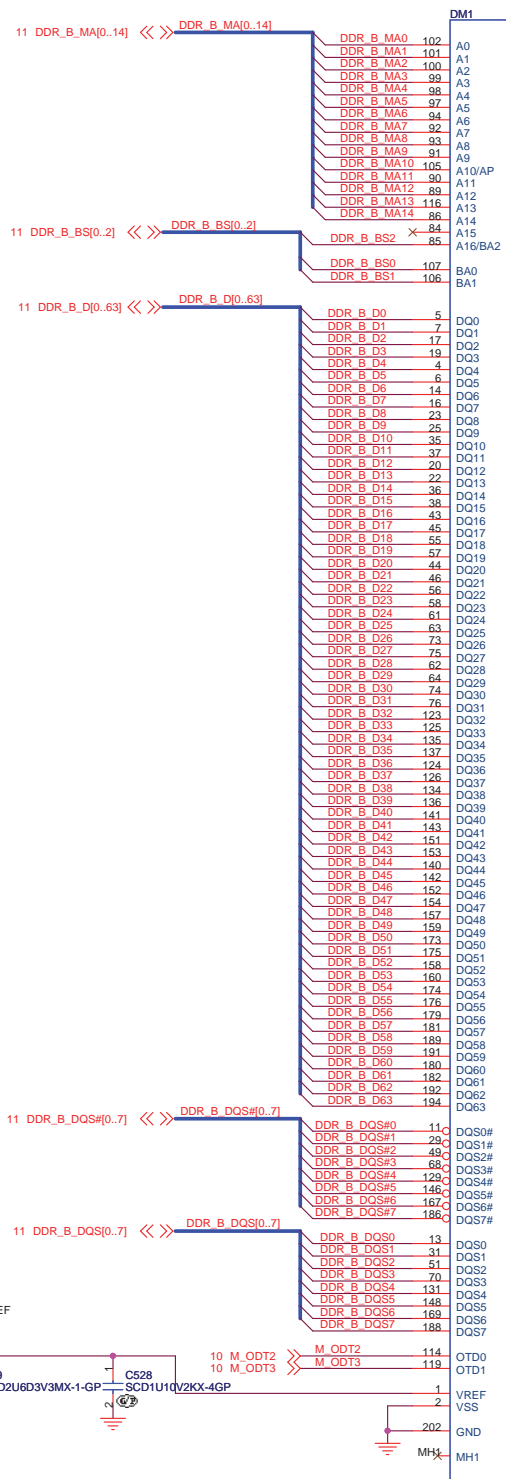


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Date: Tuesday, November 06, 2007			Sheet 11 of 50		
			Rev -1		

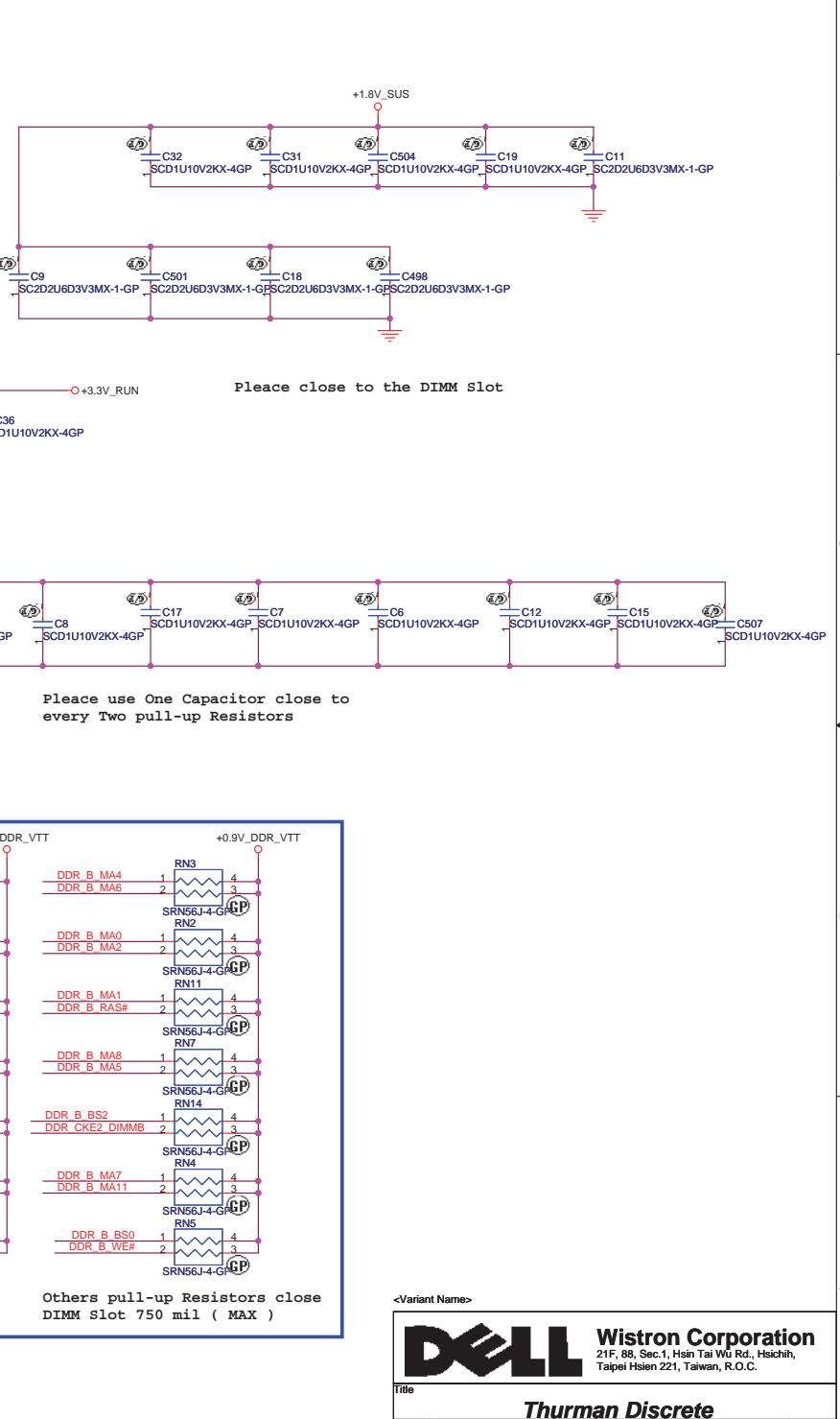
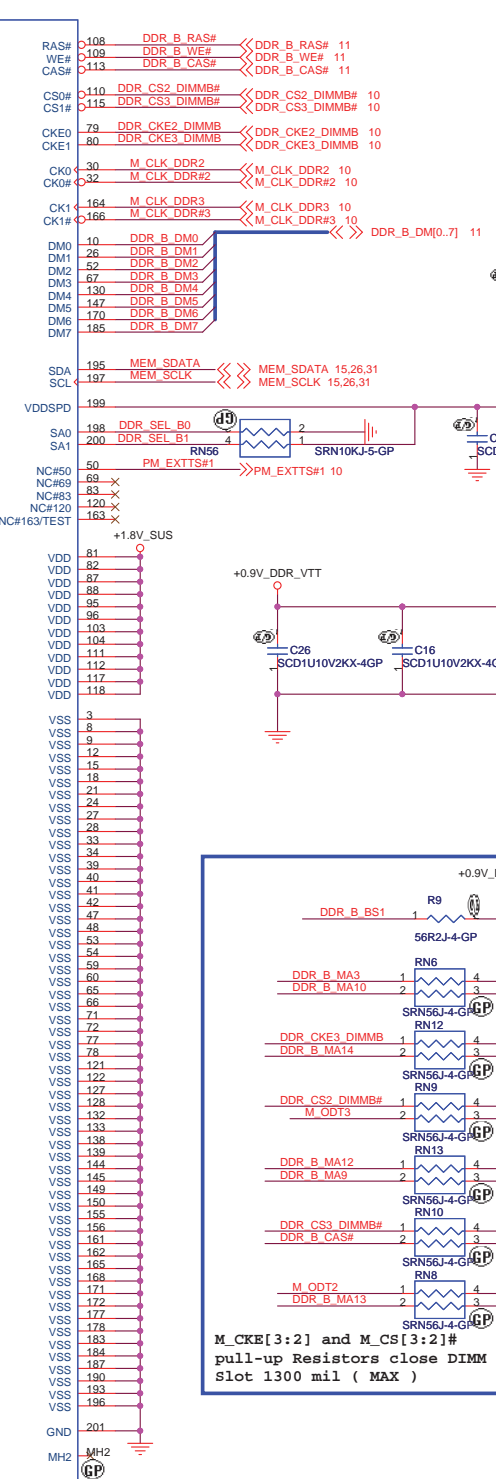








REVERSE TYPE High 9.2 mm



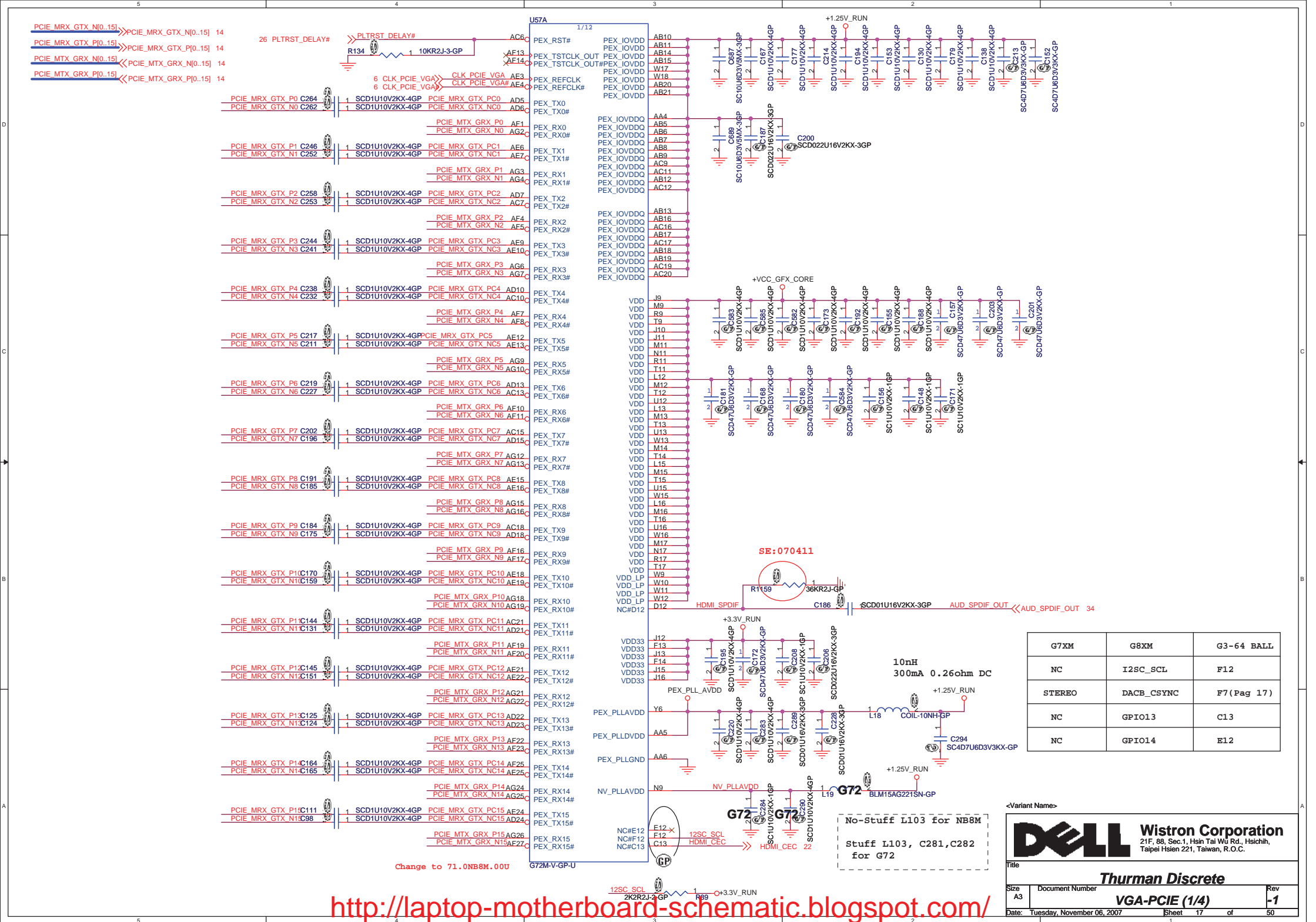
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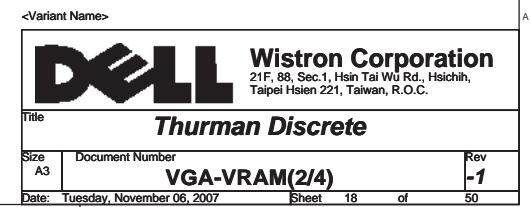
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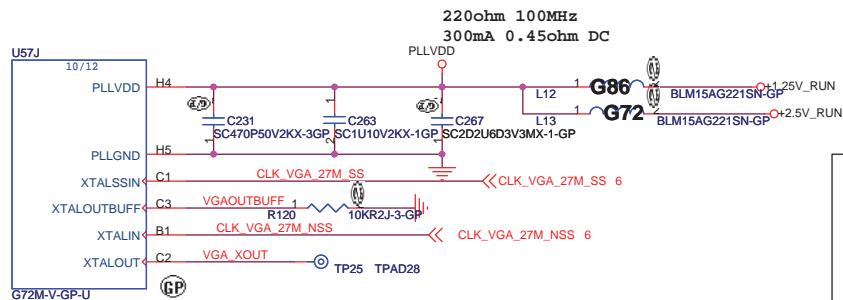
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Date: November 06, 2007 Sheet: 16 of 50



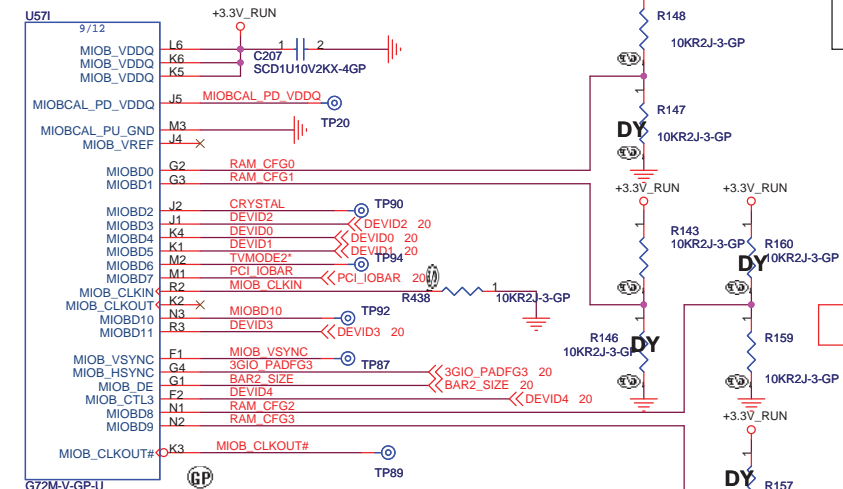
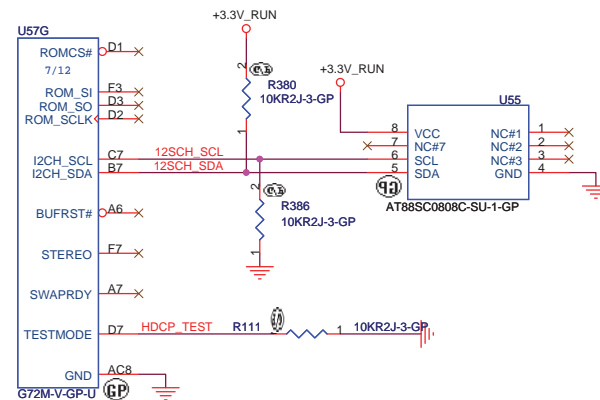




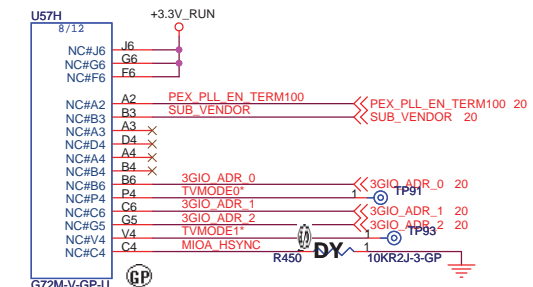
Stuff L100 for G72
Stuff L11 for NB8M

RAM_CFG[3:0]	MIOBD0	Infineon 8MX32 DDR3 1.8V	0101
	MIOBD1	HyNix 8MX32 DDR3 1.8V	0111
	MIOBD8	Samsung 8MX32 DDR3 1.8V	0110
	MIOBD9	Infineon 16MX32 DDR3 1.8V	0001
		HyNix 16MX32 DDR3 1.8V	0010
		Samsung 16MX32 DDR3 1.8V	0011

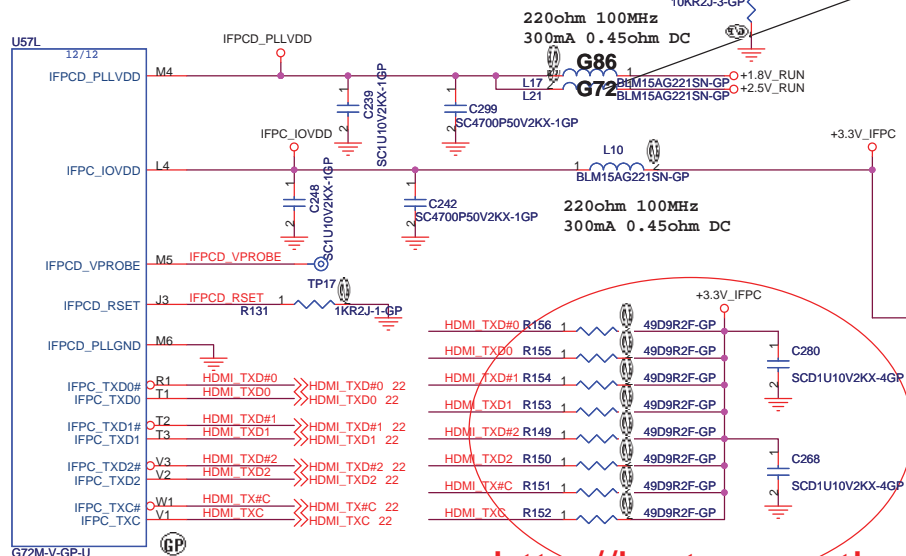
	DEVID3	DEVID2	DEVID1	DEVID0
G72GLM	1	1	0	0
G72M	1	0	0	0
G72MV	0	1	1	1
G86M	0	1	1	1



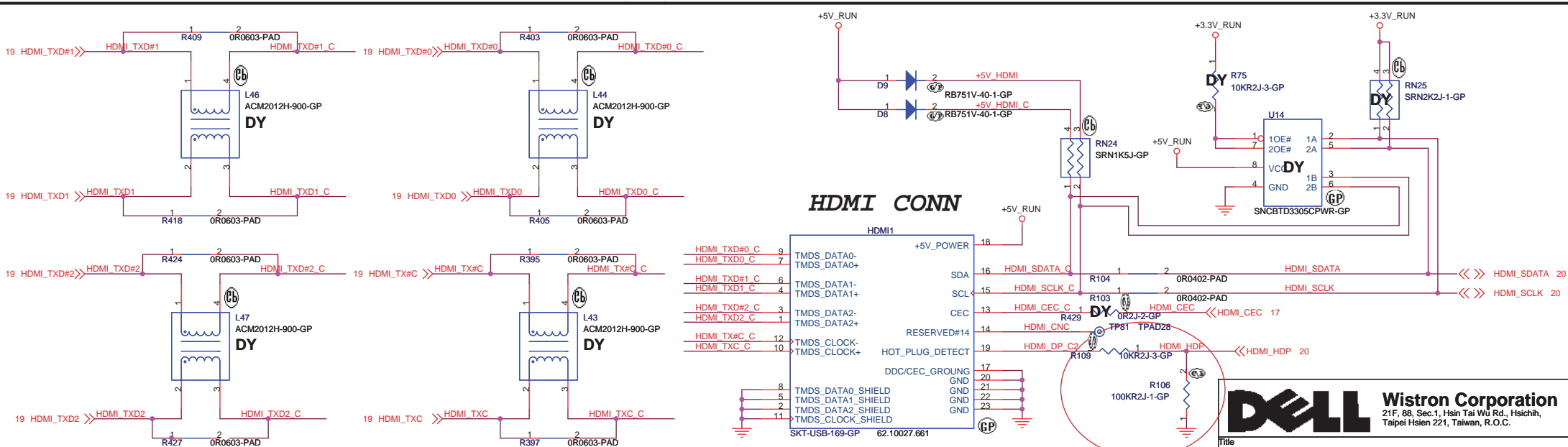
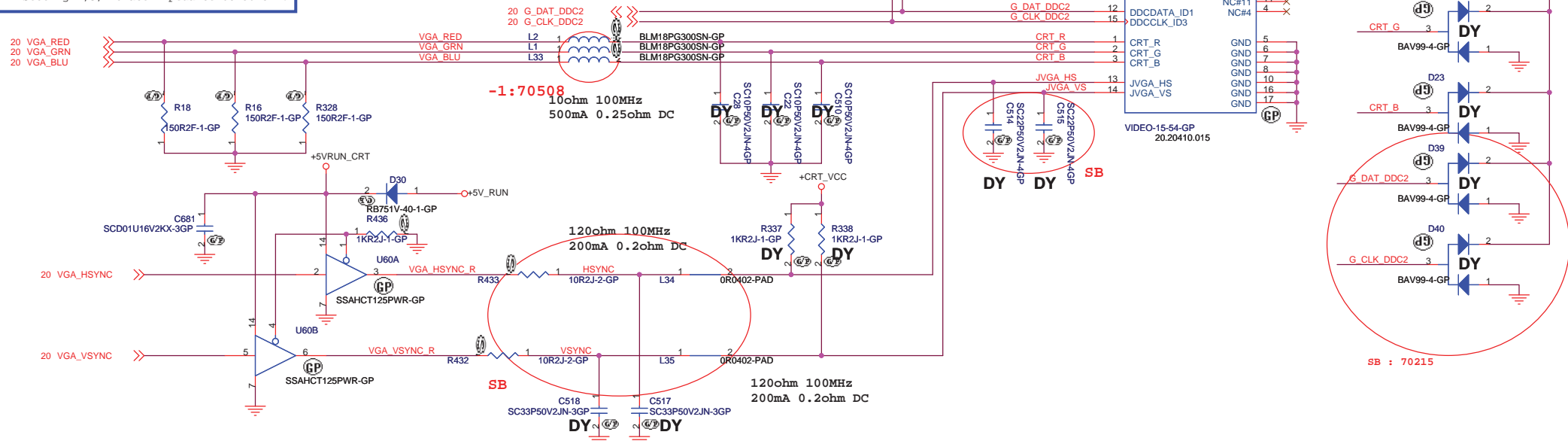
Stuff L101 for G72
Stuff L53 for NB8M

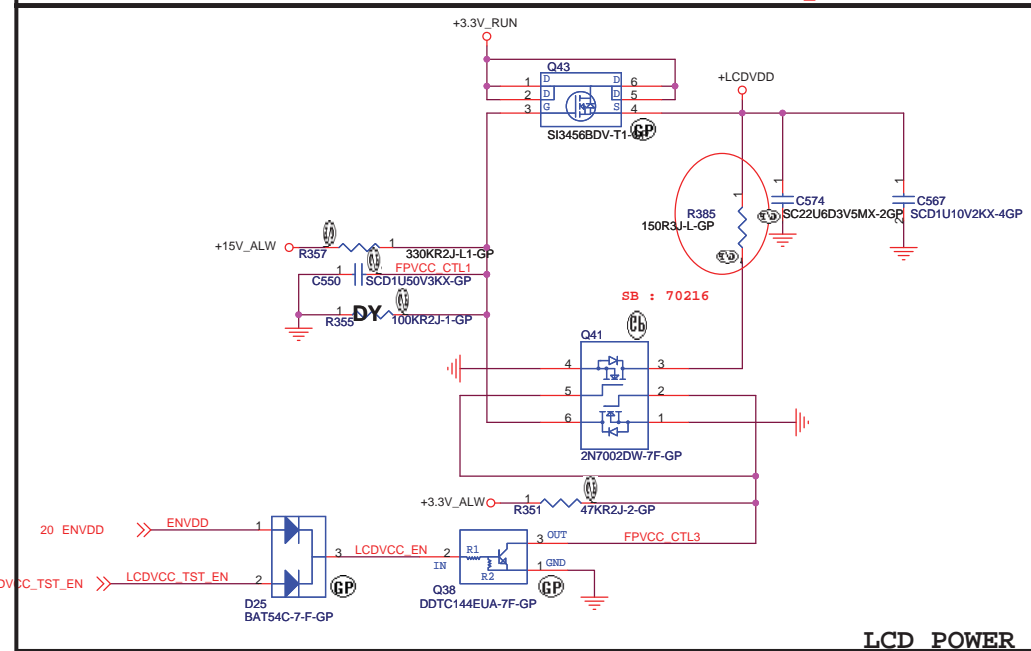
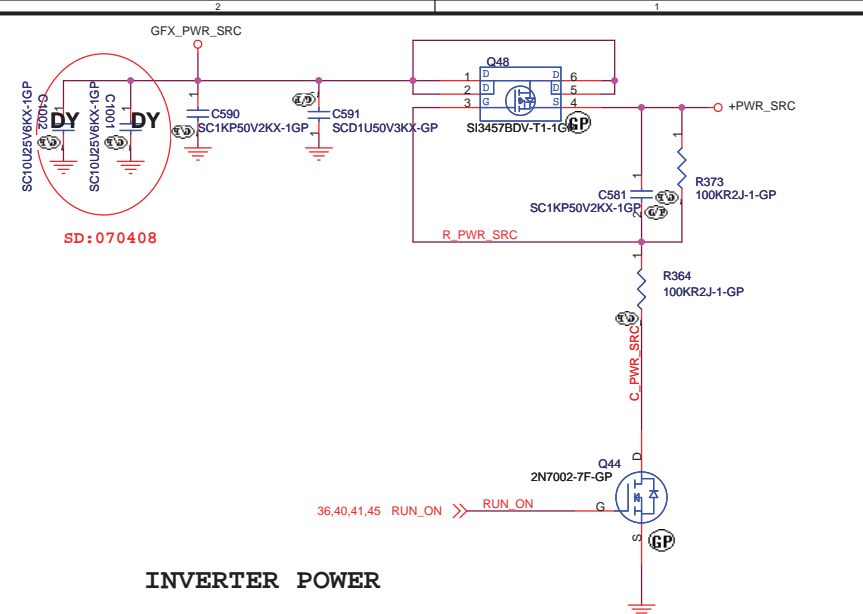
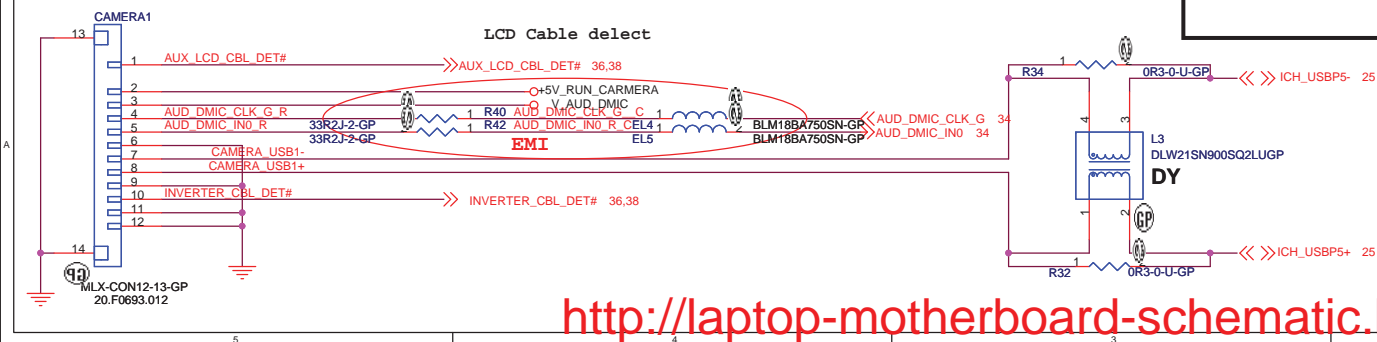
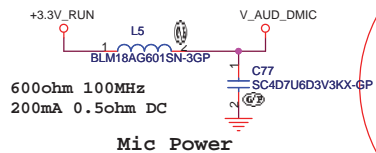
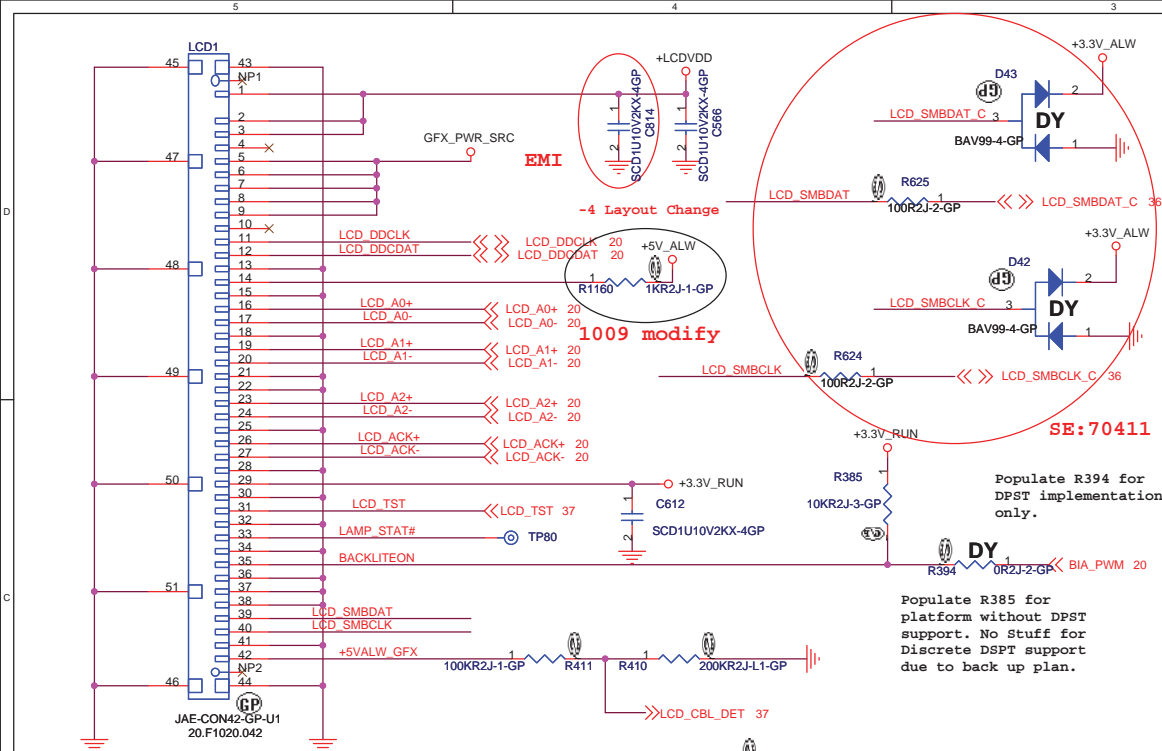


R106:Confirm need to
no stuff not for G72
and G86.

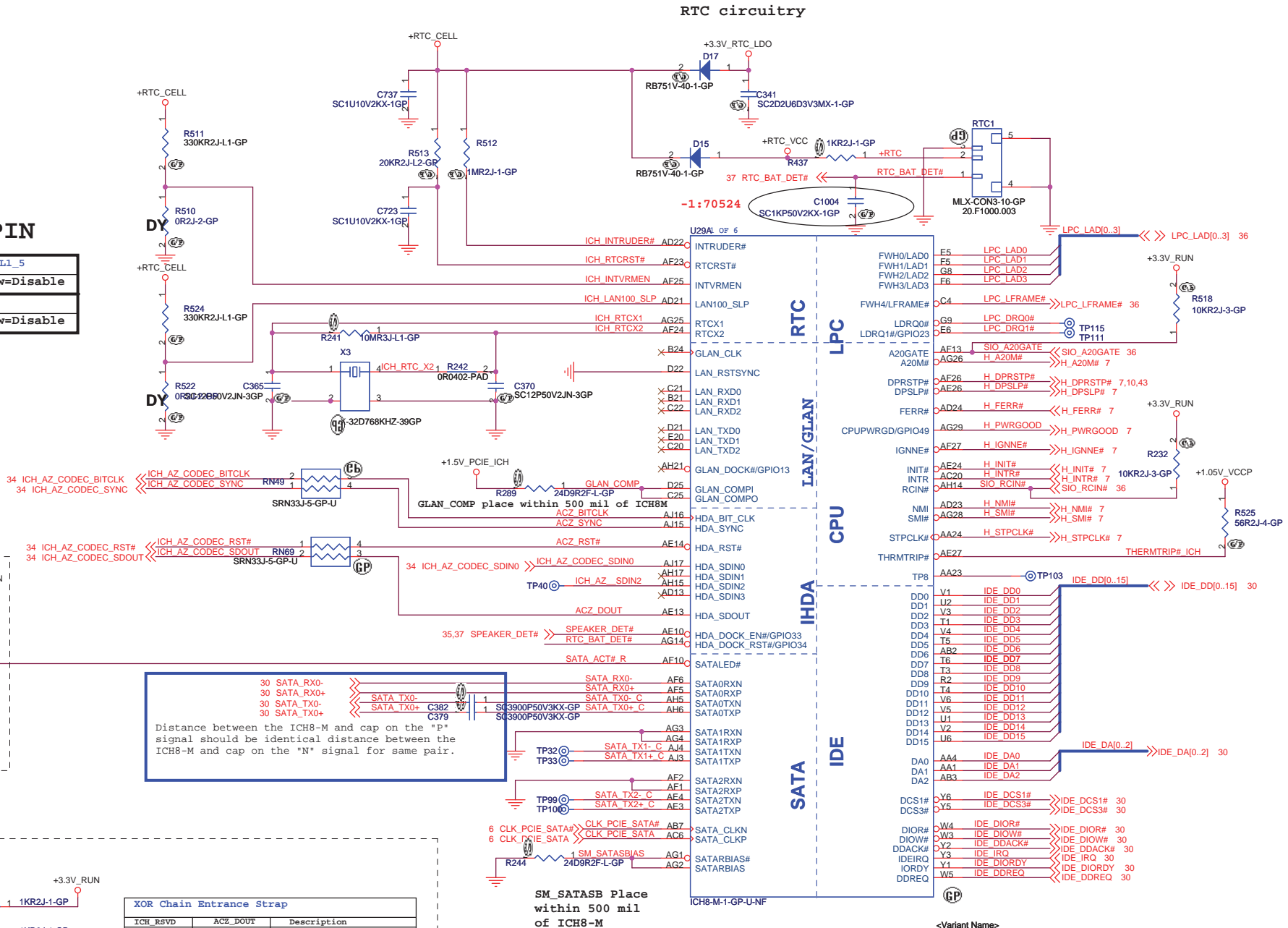








integrated VccSus1_05,VccSus1_5,VccCL1_5		
ICH_INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
ICH_LAN100_SLP	High=Enable	Low=Disable



26 ICH_RSVD <<>> ICH_RSVD

ACZ_DOUT

R517 R230

+3.3V_RUN

1K2J-1-GP

ICH_RSVD	ACZ_DOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIe port cofig bit1

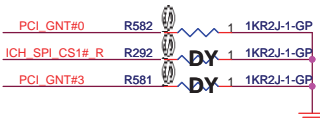
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Title			
Thurman Discrete			
Size	Document Number	Rev	
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Date:	Thursday, November 22, 2007	Sheet	24 of 50

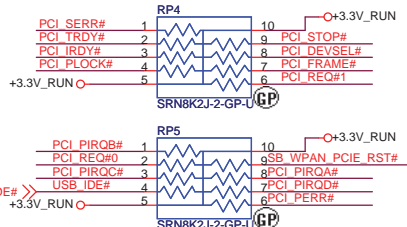
ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

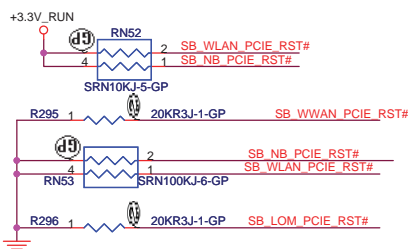
Al6 swap override strap	
PCI_GNT#3 (R168)	
low	= Al6 swap override enable
high	= default



PCI I/F PULL HIGH

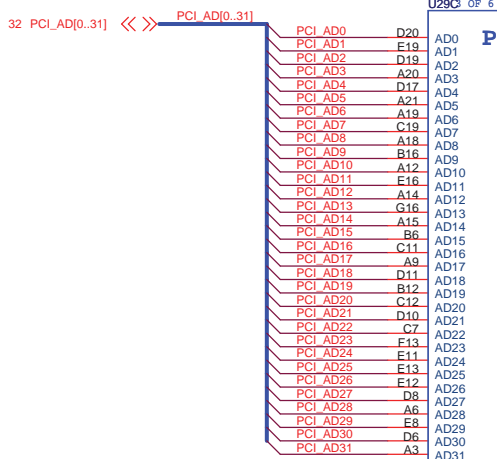
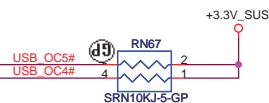


BIOS should not enable the internal GPIO pull up

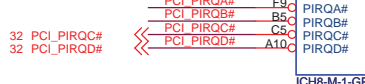


PCIE Interface Routing

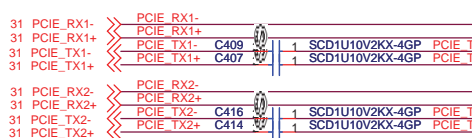
LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	LAN



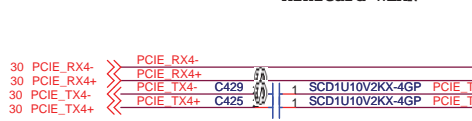
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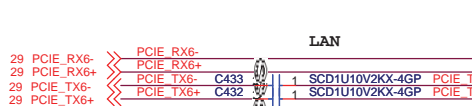
MiniCard WWAN



MiniCard WLAN



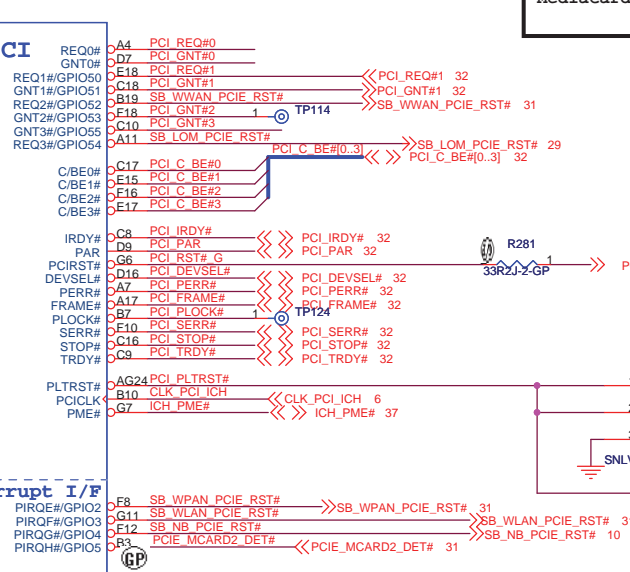
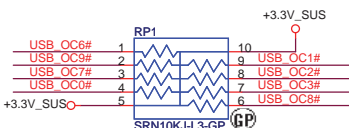
Express Card



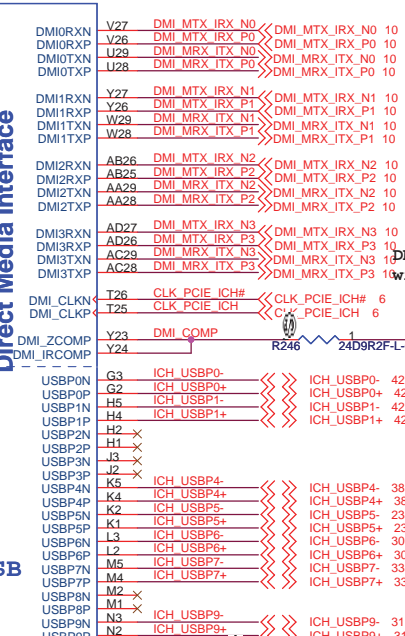
LAN



Layout Note:
Place R235, R237 and R234 within 500 mils from ICH.

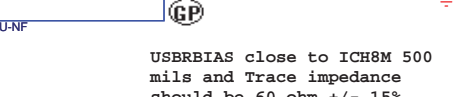


PCI-Express Direct Media Interface



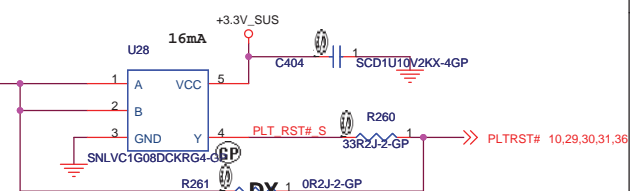
SPI

USB

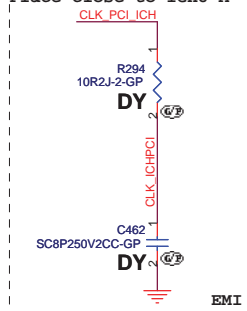


	IDSEL	INT	REQ	GNT	PCI Interface Routing
1394/MediaCard	AD17	C	1	1	

Add Buffers as need for Loading and Fanout concerns



CLK ICH 14M EMI Mode



Place close to ICH8M within 500 mil of ICH8M

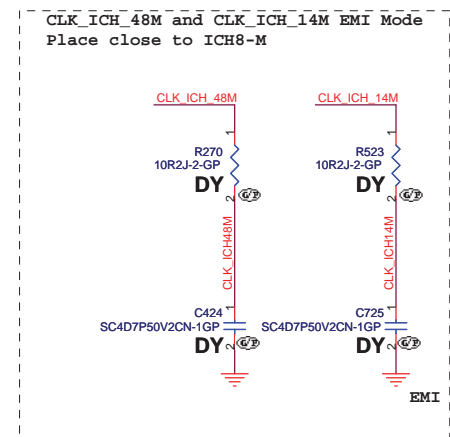
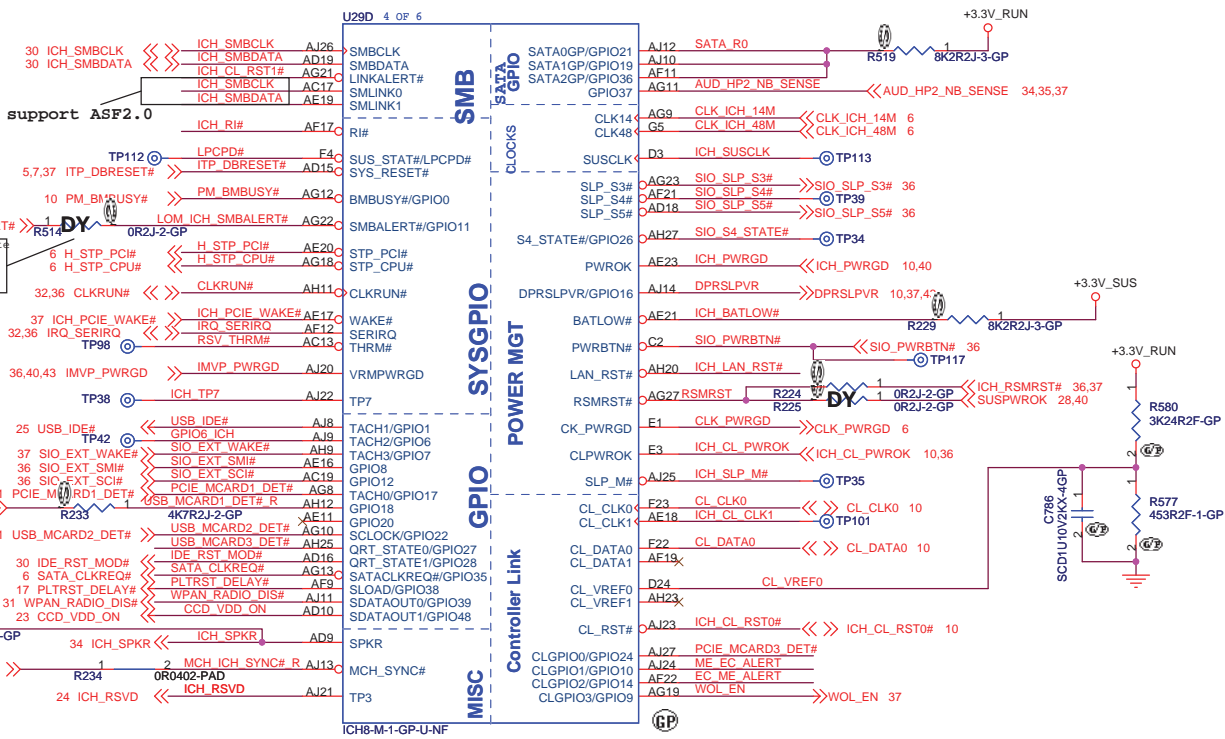
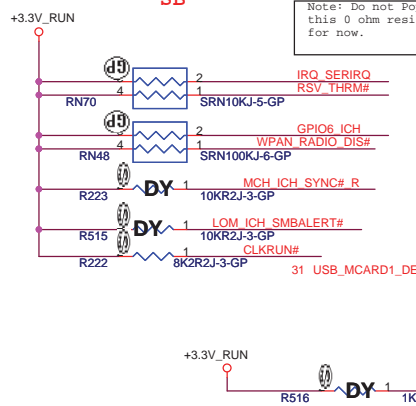
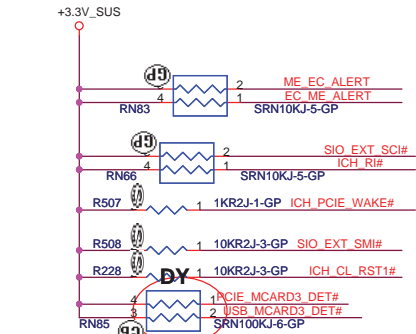
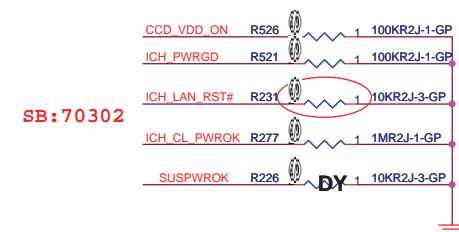
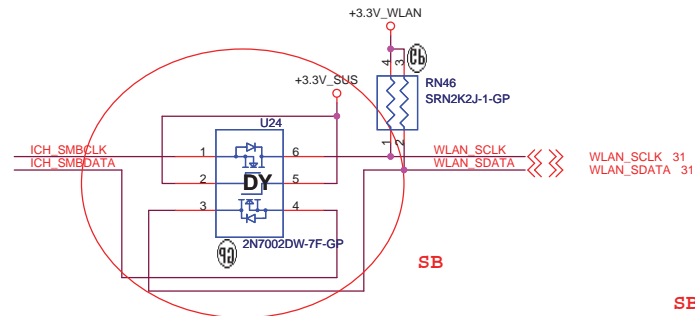
USB0	USB1
USB1	USB2
USB2	USB3
USB3	USB4
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	MINI Card WWAN
USB9	

<Variant Name>

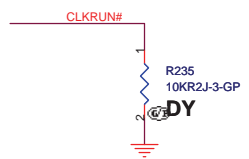


Title		Thurman Discrete	
Size	A3	Document Number	ICH8M-PCIE/USB/SPI/DMI (2/4)
Date	Thursday, November 22, 2007	Sheet	25 of 50

<http://laptop-motherboard-schematic.blogspot.com/>



No Reboot Strap	
ICH_SPKR	LOW = Defaule
	High=No Reboot



SSID = THERMAL

REM_DIODE1_N and REM_DIODE1_P
routing Trace width and Spacing
use 10 / 10 mil

Place inside CPU socket

C455 Please close to Guardian

Close to Pin5, Pin6

Close to Pin9

H_THERMDA and H_THERMDC
routing Trace width and
Spacing use 10 / 10 mil

C456 Please close to Guardian

Note :

$VSET = (T_p - 70) / 21$
 $3.3 * (R411 / R406 + R411) = (T_p - 70) / 21$
 Where $T_p = 70$ to 101 degrees C
 T_p set at 88 degrees C
 Guardian temp tolerance = ± 3 degrees C

Version B: 74.04001.A73

C451 Please Close to Guardian

Place near the bottom SODIMM CONN

REM_DIODE4_N and REM_DIODE4_P
routing Trace width and Spacing
use 10 / 10 mil

Thermal sensor for Mini Card
should be placed TOP Side under WWAN CARD

C459 Please Close to Guardian

Thermal sensor for VGA

C453 Please Close to Guardian

VGA THERMALTRIP

CPU THERMALTRIP

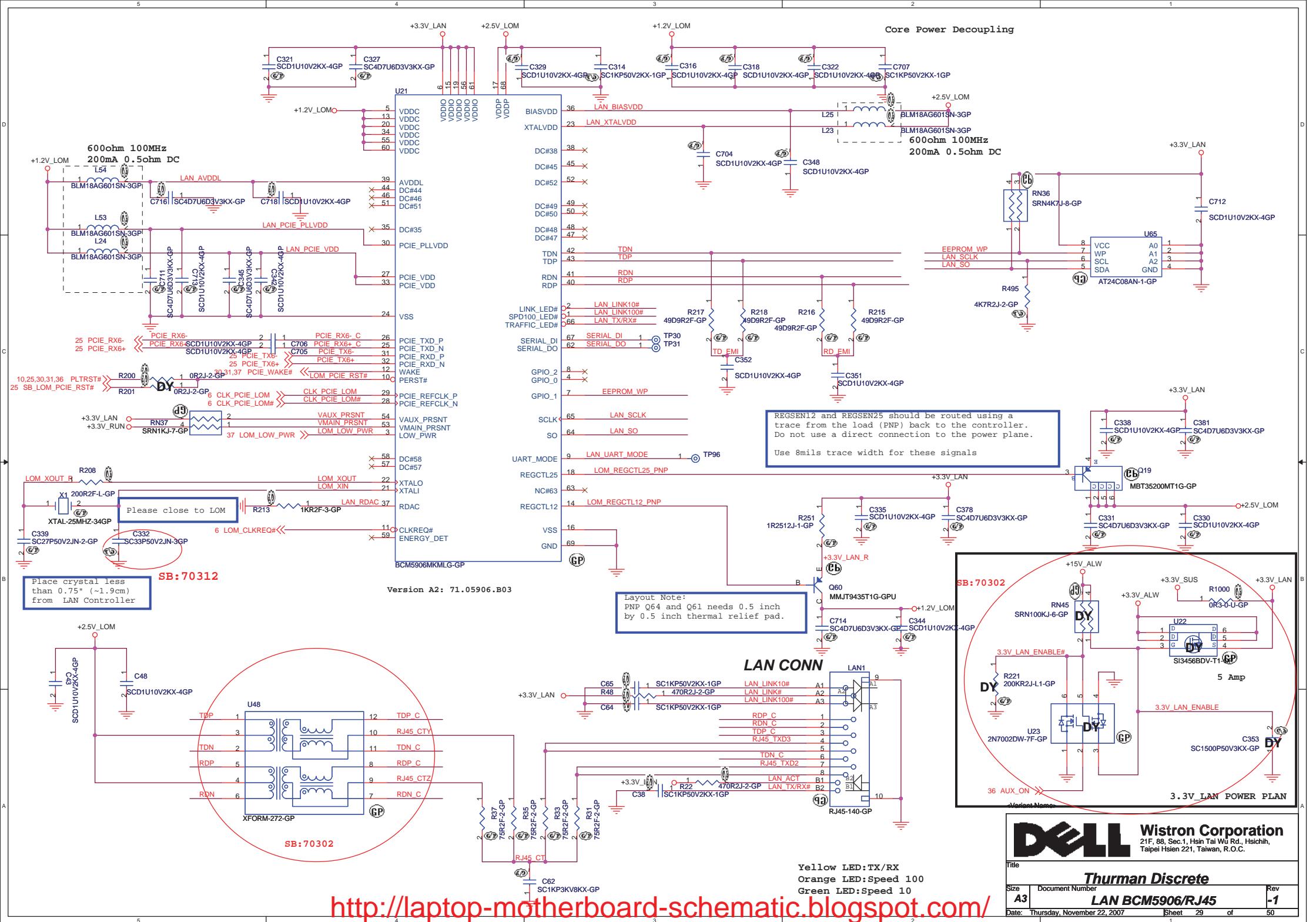
MCH THERMALTRIP

C916, C459, C472 Please Close to Guardian

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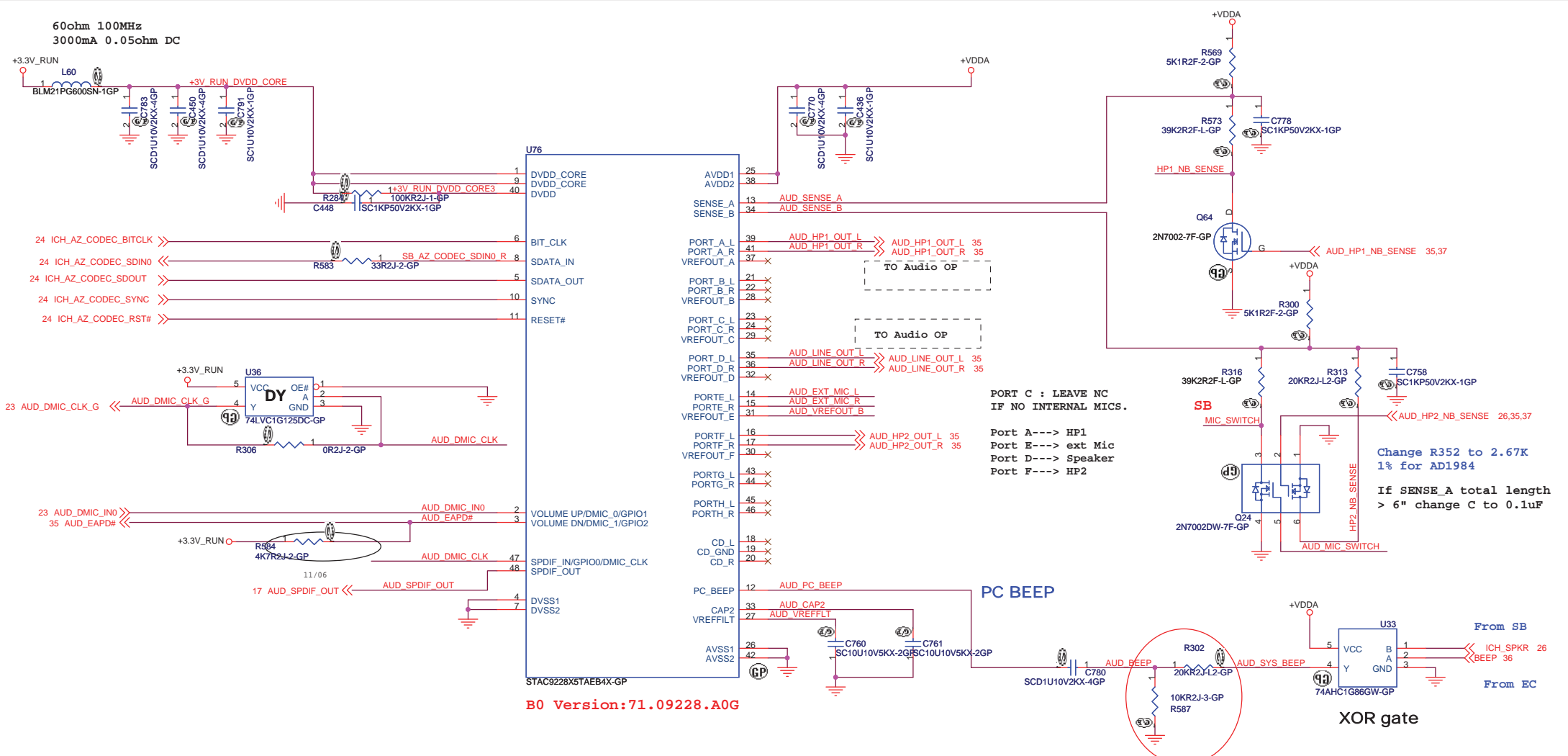
Title			Thurman Discrete	
Size	Document Number	FAN/EMC4001		Rev
A3				-1
Date:	Tuesday, November 06, 2007	Sheet	28	of 50

<http://laptop-motherboard-schematic.blogspot.com/>

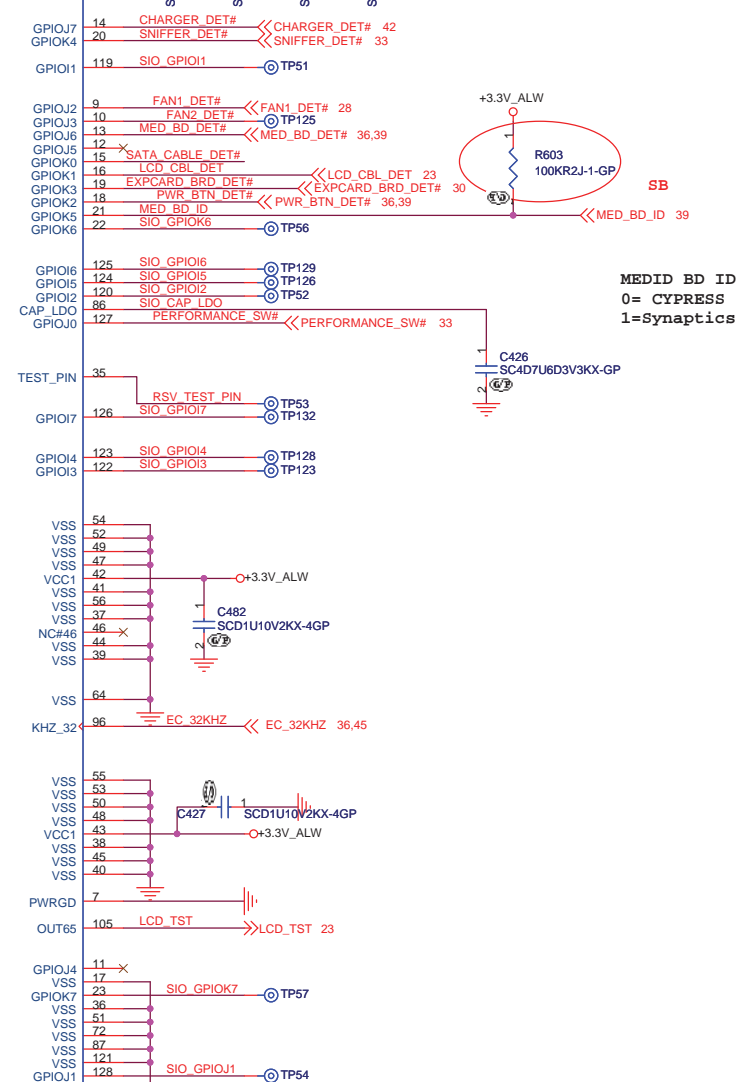
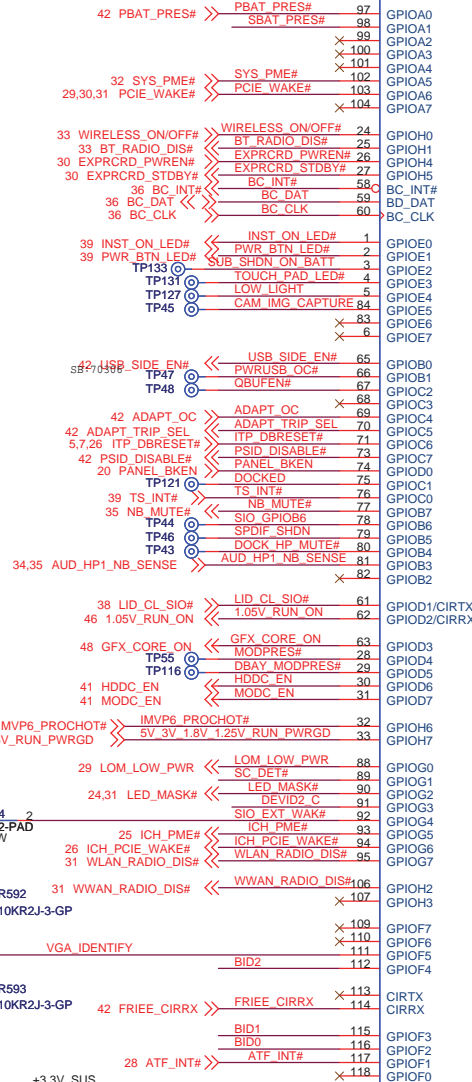
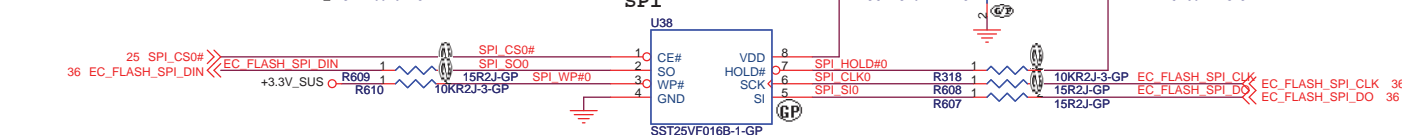
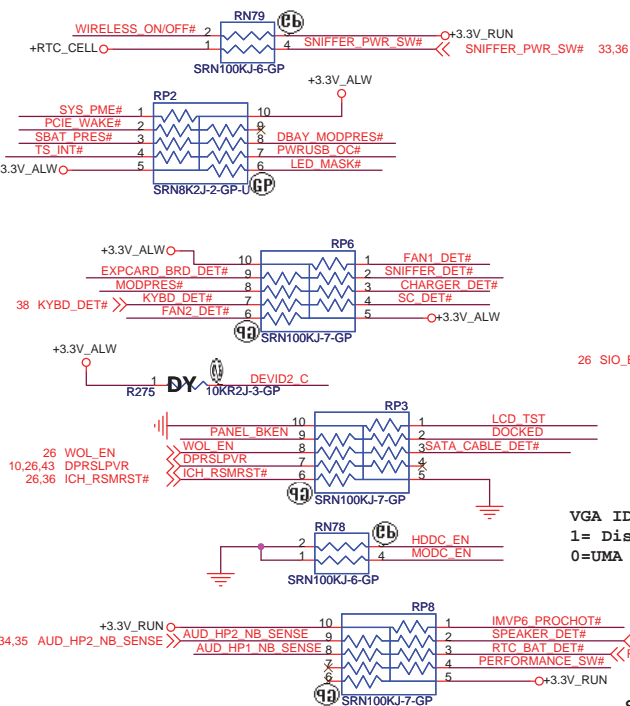
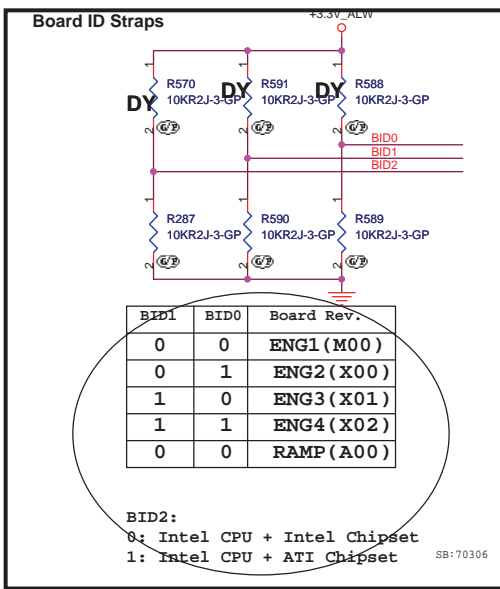


DEBUG PINS









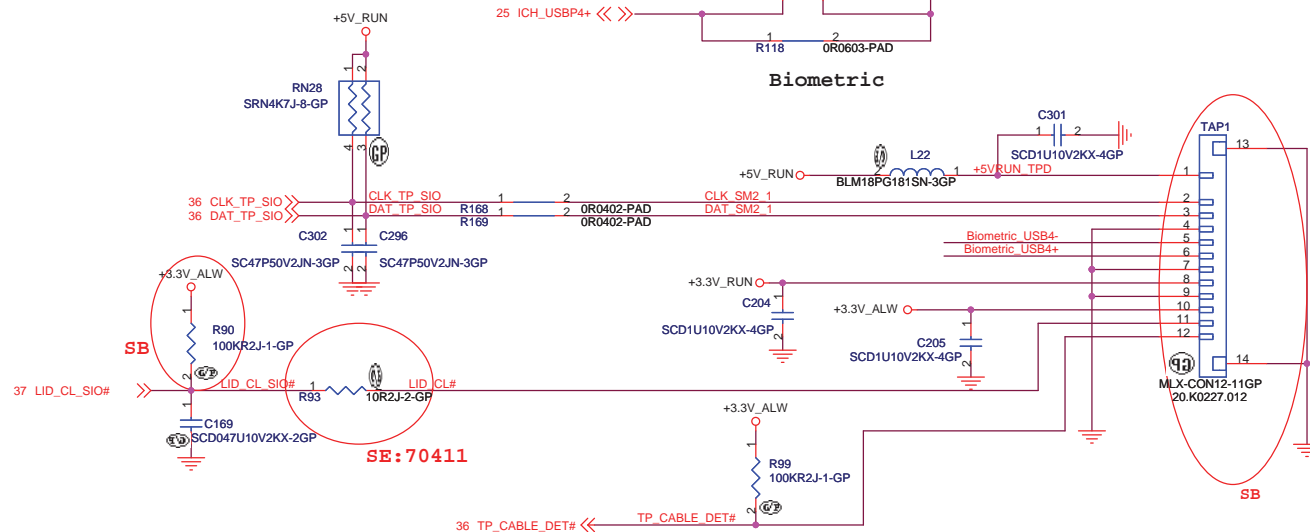
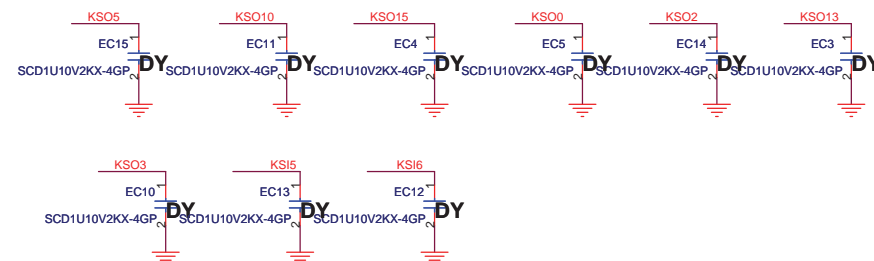
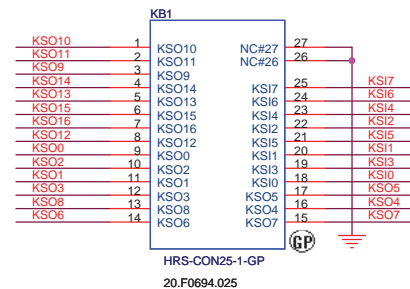
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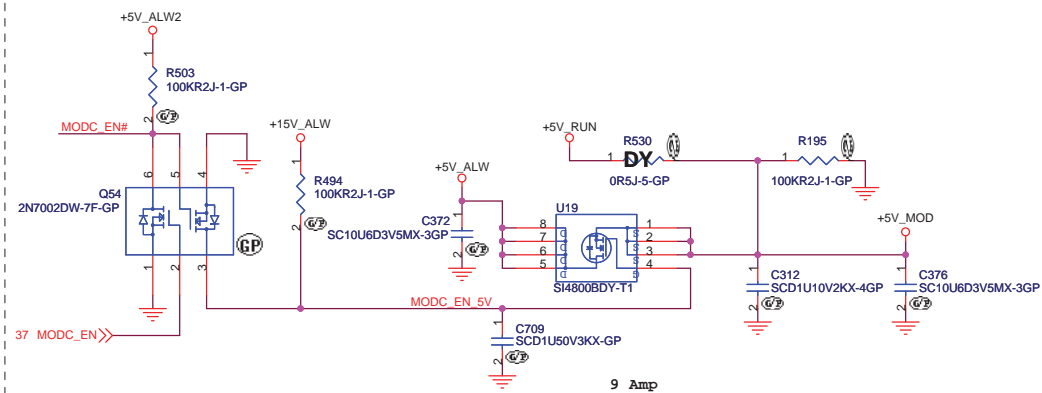
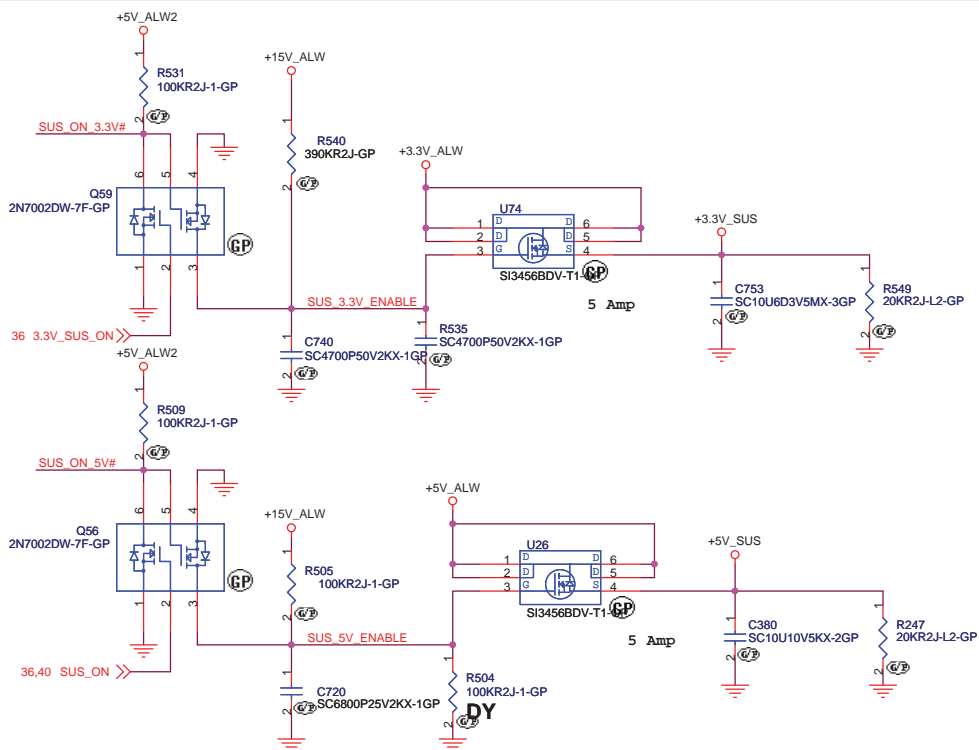
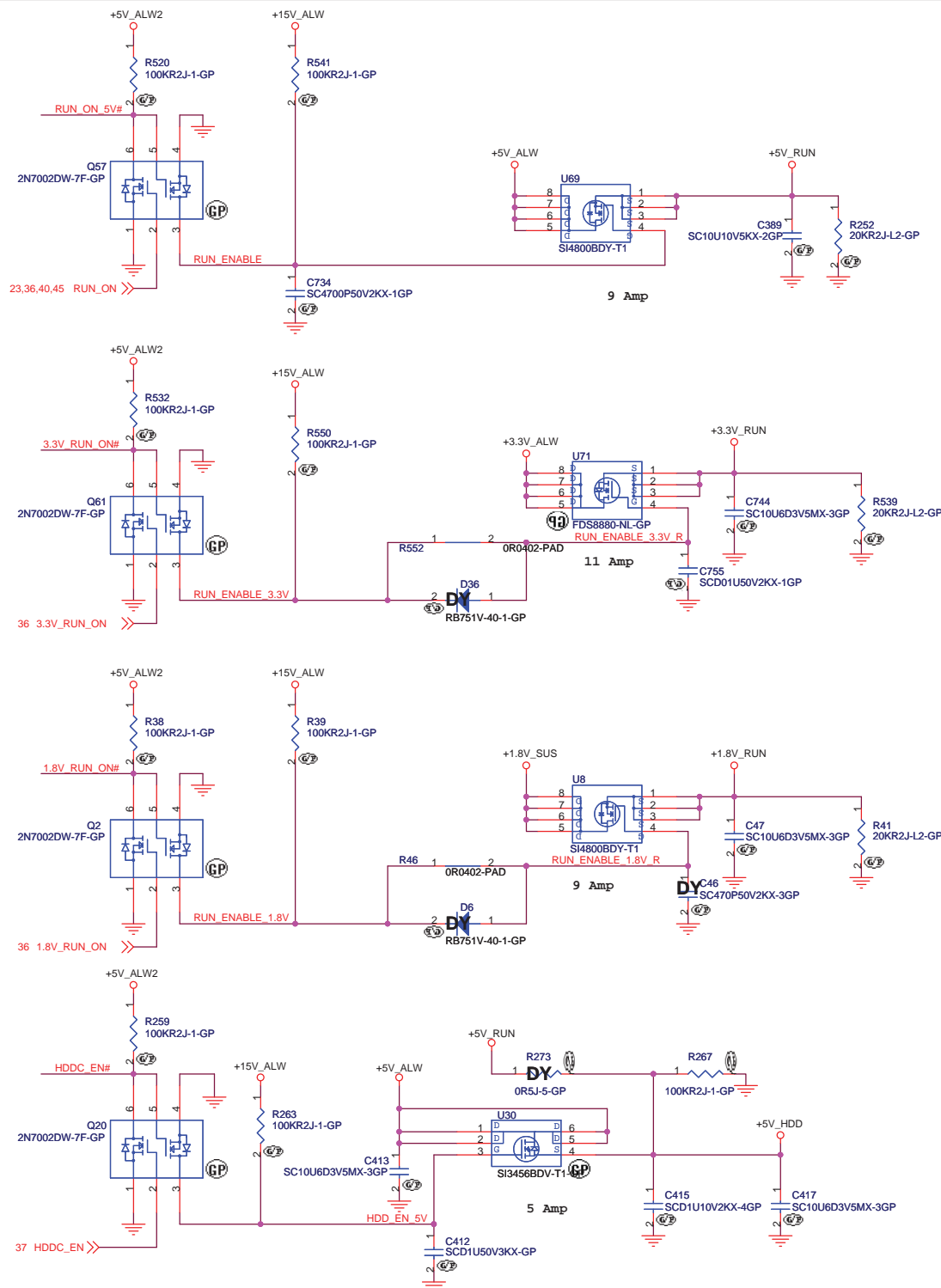
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 Taipei Hsien 221, Taiwan, R.O.C.

File: **Thurman Discrete**

Size: **A3** Document Number: **SIO ECE5011/SPI ROM** Rev: **-1**

Date: Tuesday, November 06, 2007 Sheet 37 of 50





<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

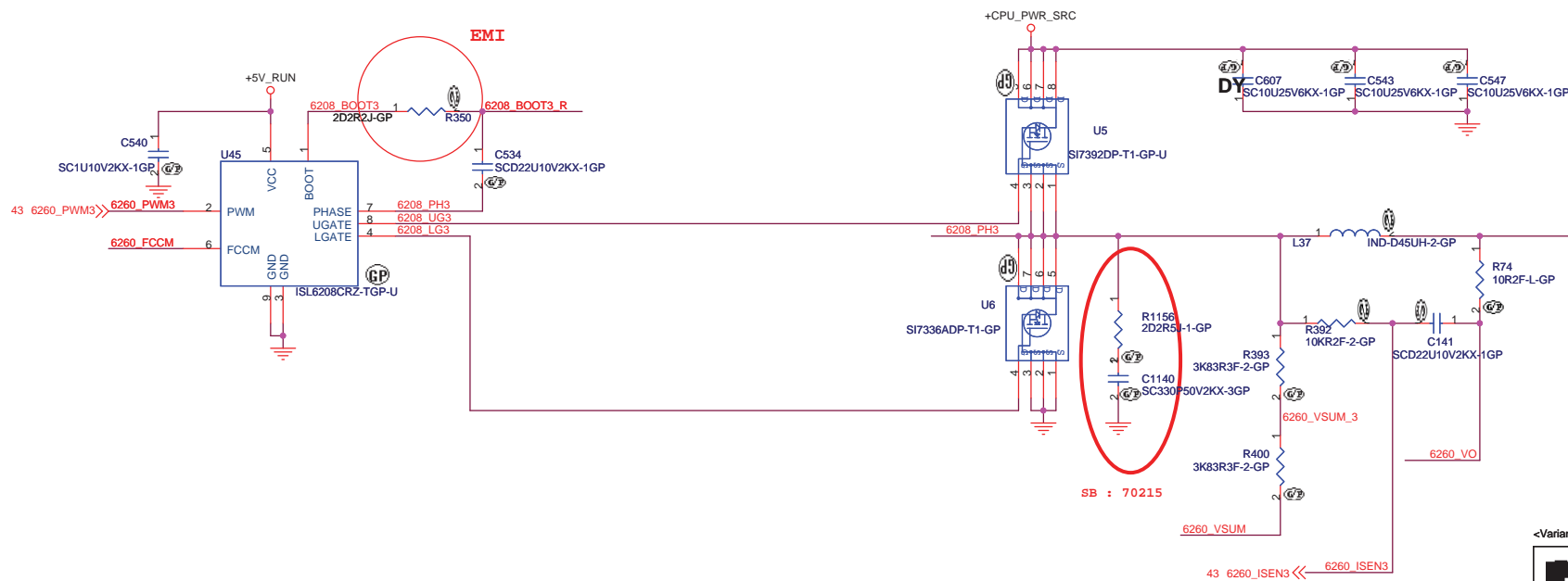
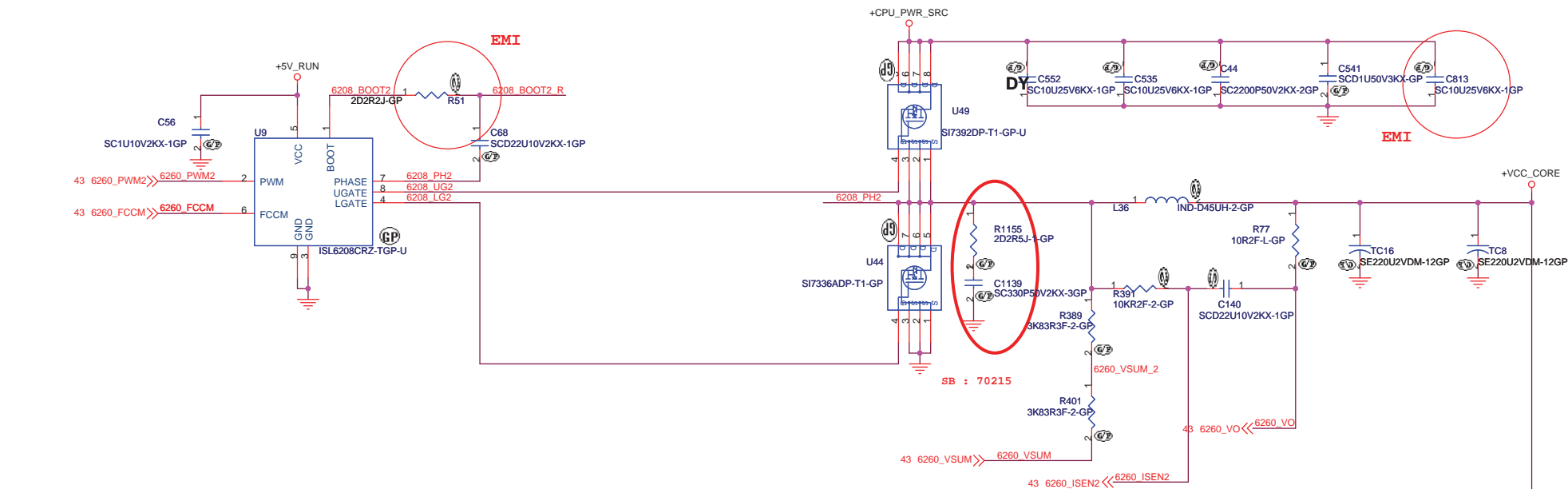
Title

Size A3 Document Number

Rev -1

Date: Thursday, November 22, 2007 Sheet 41 of 50

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<Variant Name>



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Title

Thurman Discrete

Size

Document Number

A3

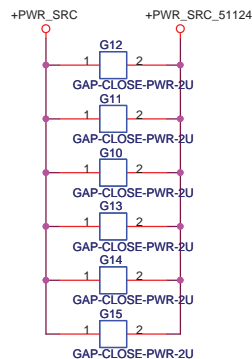
CPU Core-02

Rev

-1

Date: Tuesday, November 06, 2007

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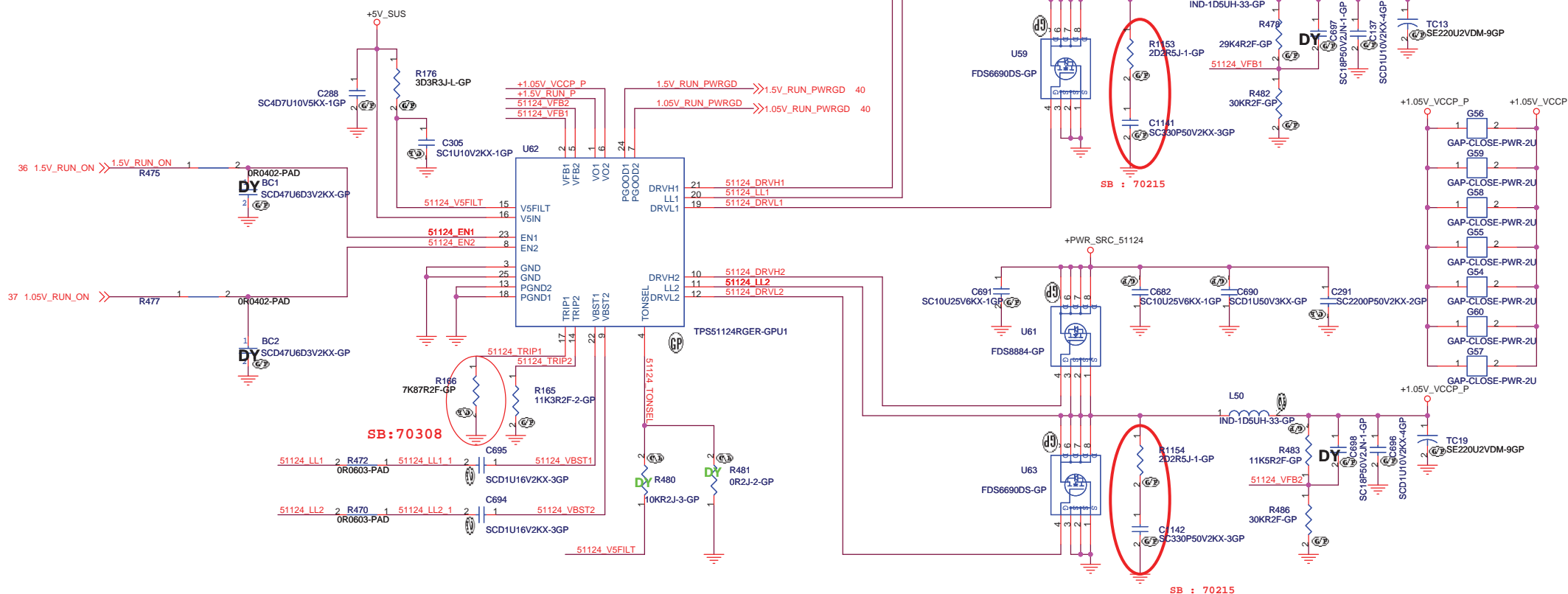


$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
 O/P cap: 220U 2V EEFSX0D221ER 9mOhm 3Arms Panasonic/ 79.22719.2PL
 H/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
 L/S: FDS6690AS SO-8/ 15mOhm/ 4.5Vgs/ 84.06690.E37

Design Current = 6.0A
 OCP design > 6.8A
 Included 1.25V LDO(3.02A)



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode

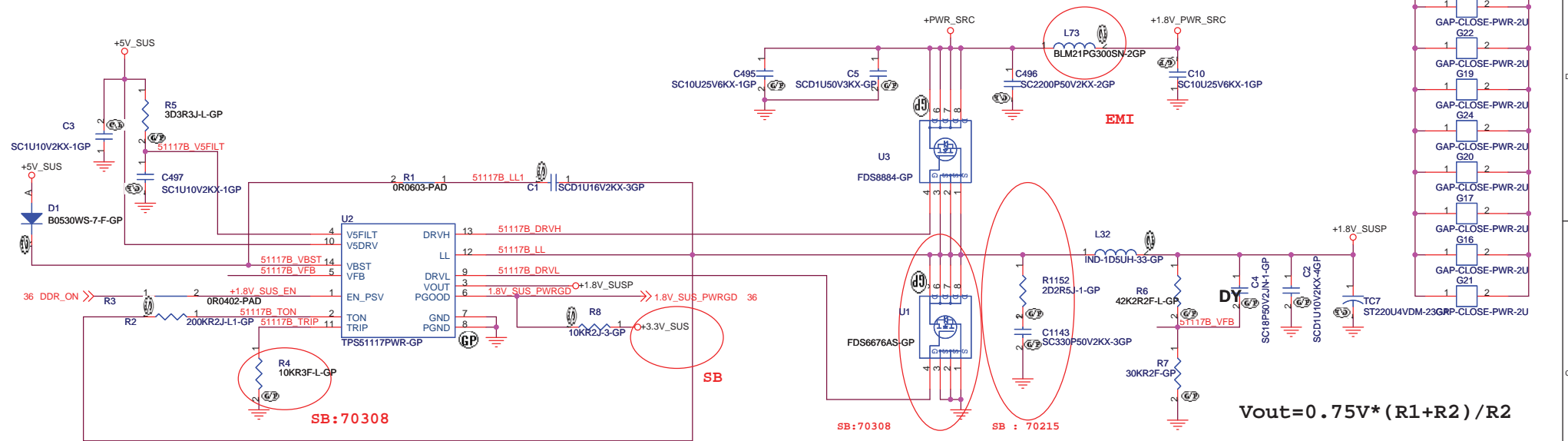
Design Current= 5.9A
 OCP design > 7.3A

<Variant Name>

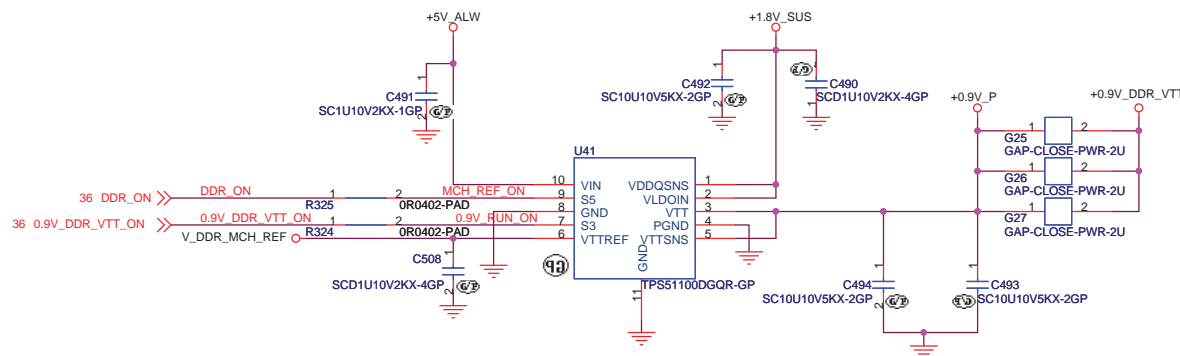


Title		
Thurman Discrete		
Size	Document Number	Rev
A3	DCDC 1.5V/1.05V	-1
Date: Thursday, November 22, 2007	Sheet 46	of 50

Design Current = 8.64A
 OCP design = 12.34A



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
 O/P cap: 220U 4V 4TPE220MF 15mOhm 3.1Arms/ 77.22271.161
 H/S & L/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
 L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037
 Ton = 200KOhm --> 330KHz

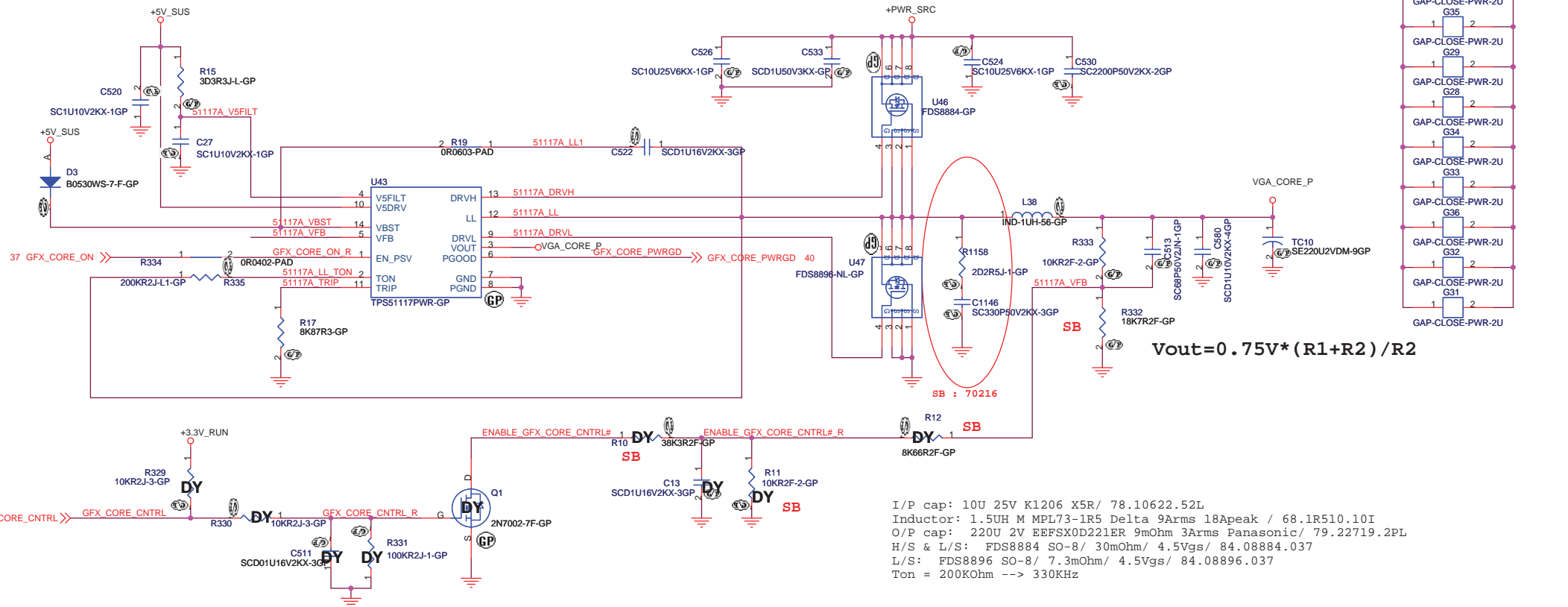


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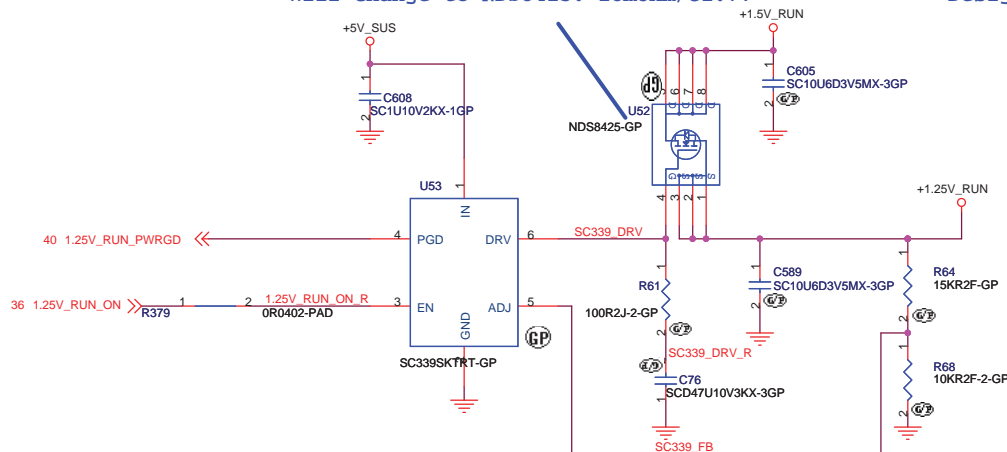
Title		
Thurman Discrete		
Size	Document Number	Rev
A3	DCDC 1.8V/0.9V	-1
Date:	Thursday, November 22, 2007	Sheet 47 of 50

Design Current = 11A
 OCP design = 15A
 VGA_CORE = 1.0V



Will Change to NDS8425. 28mOhm/@2.7V

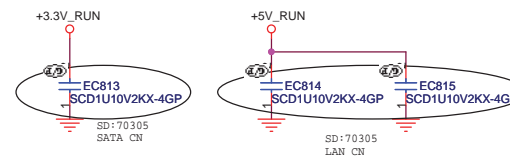
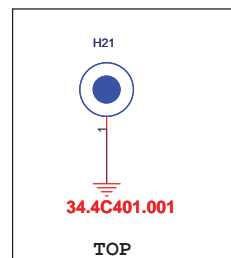
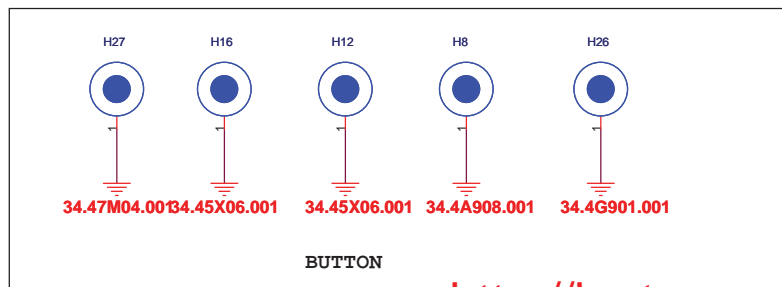
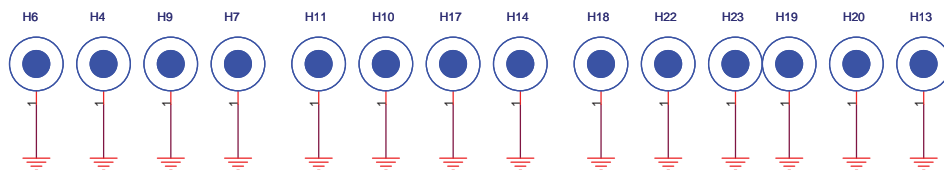
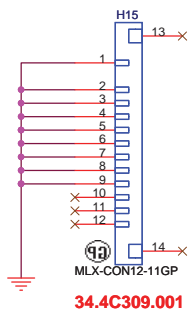
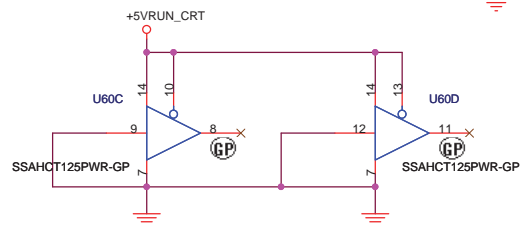
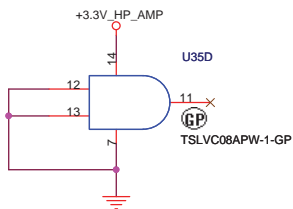
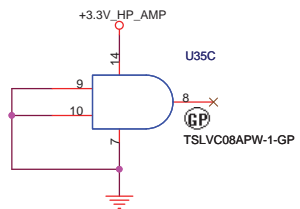
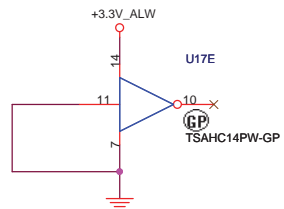
Design Current = 3.0A



<Variant Name>

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Title
Thurman Discrete
 Size A3 Document Number
DCDC VGA_Core/1.25V
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SW3 - 34.43E25.001
SW9 - 34.49Q02.001
SW5 - 34.34T31.001 (Only for UMA)
others-34.45T31.001

