

DJ1 Montevina UMA Schematics Document

uFCPGA Mobile Penryn

Intel GM45+ICH9M

2010-02-10

REV : A00

DY : Nopop Component

DJ1



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
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Title

Cover Page

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Document Number

DJ1 Montevina UMA

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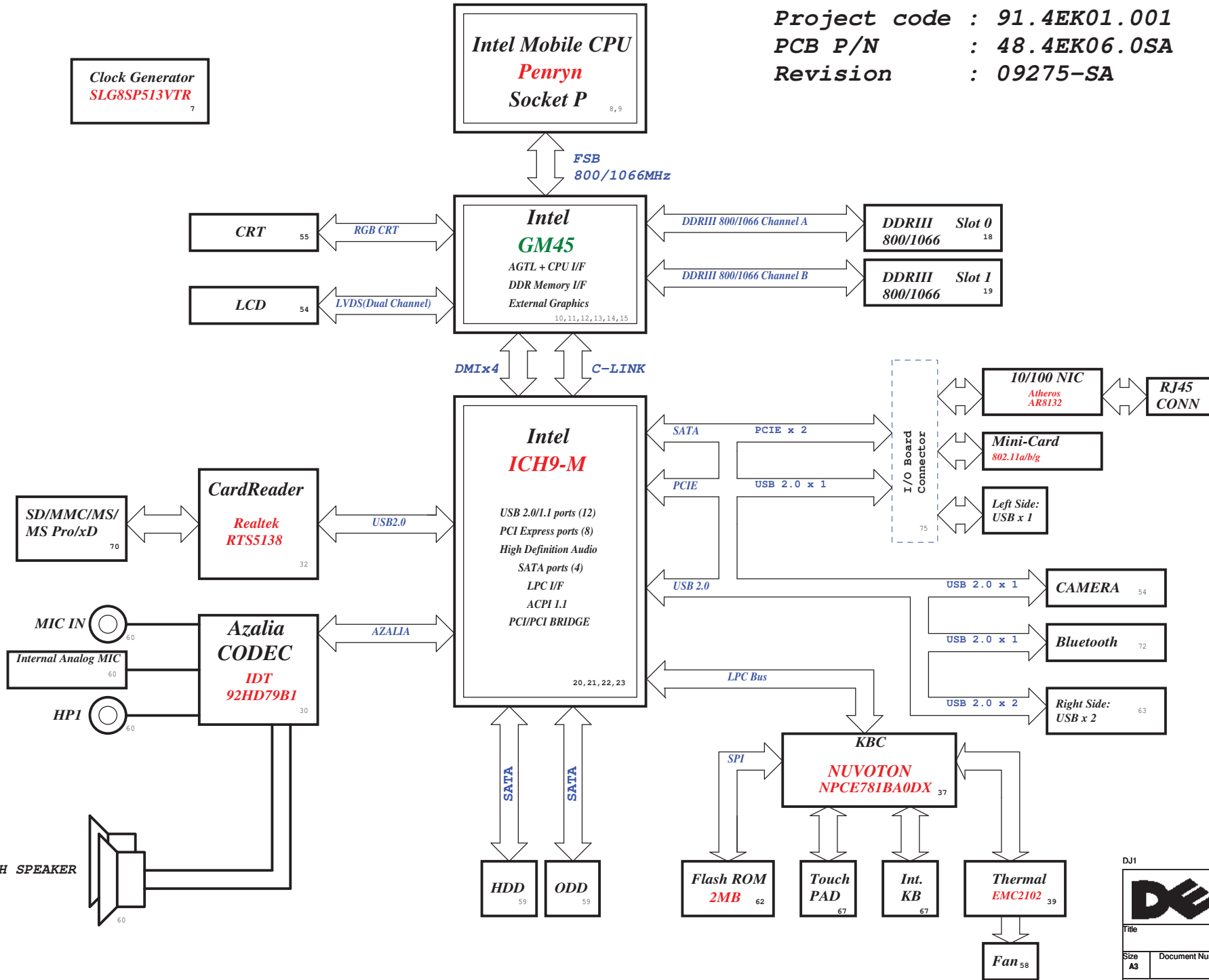
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Date: Wednesday, February 24, 2010

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DJ1 Montevina UMA Block Diagram

Project code : 91.4EK01.001
PCB P/N : 48.4EK06.0SA
Revision : 09275-SA



CPU DC/DC TPS51620 ₄₇	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC TPS51218 ₄₉	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP
SYSTEM DC/DC TPS51125 ₄₆	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW
SYSTEM DC/DC TPS51116 ₅₀	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF
MAXIM CHARGER BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC Switches ₄₂	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN
PCB LAYER	
L1: Top	
L2: VCC	
L3: Signal	
L4: Signal	
L5: GND	
L6: Bottom	

DJ1

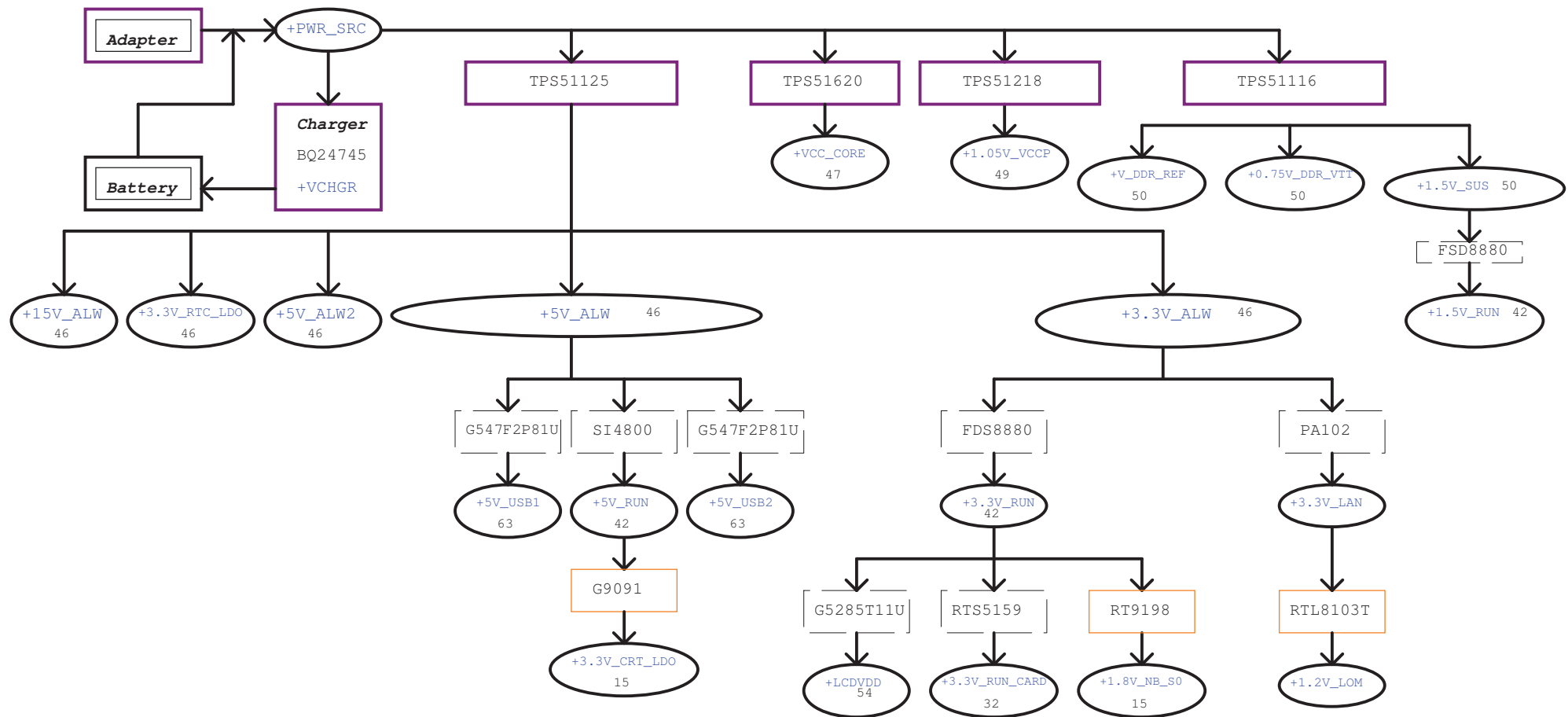
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Title **Block Diagram**

Size A3 Document Number **DJ1 Montevina UMA** Rev **A00**

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DJ1 Montevina UMA Power Block Diagram



Power Shape

Regulator LDO Switch

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Title

Power Block Diagram

Size
A3

Document Number

DJ1 Montevina UMA

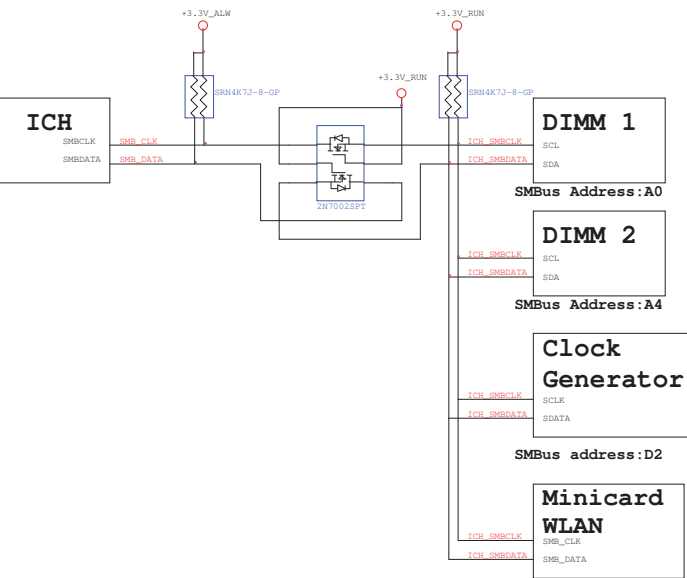
Rev

A00

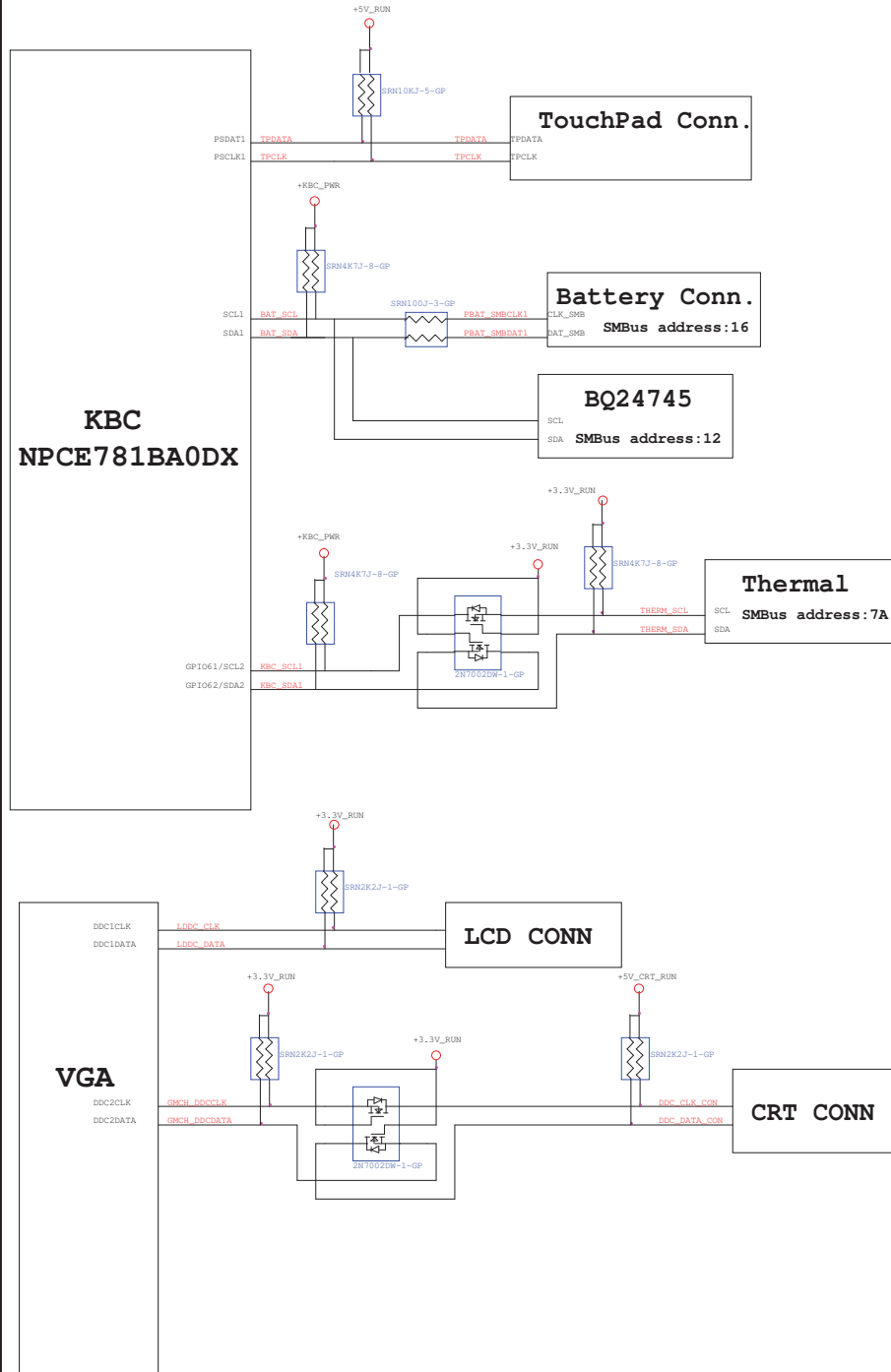
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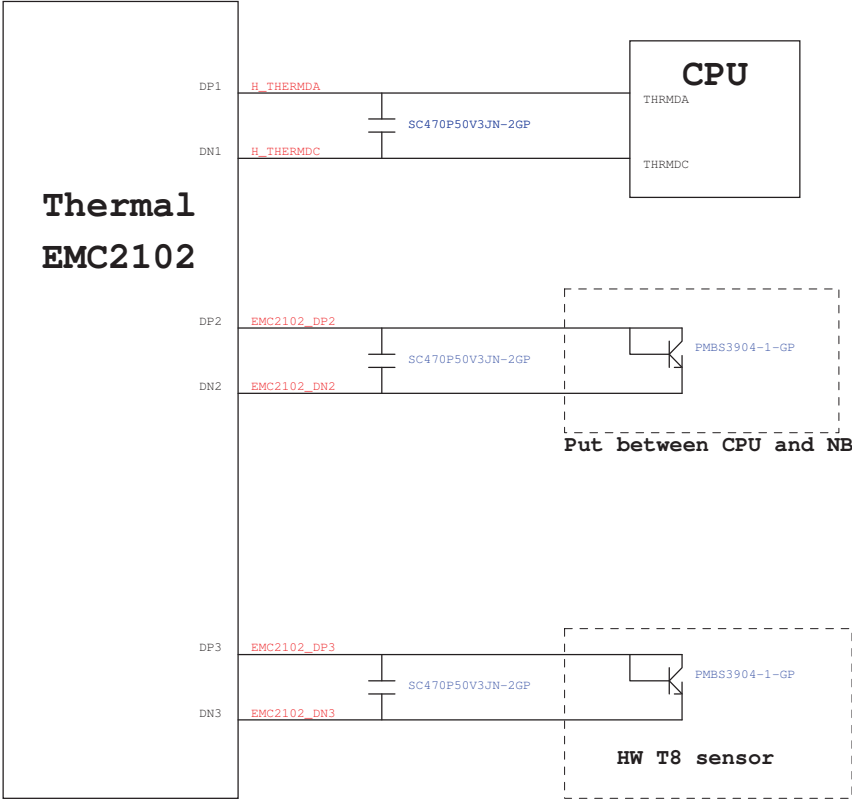
ICH SMBus Block Diagram



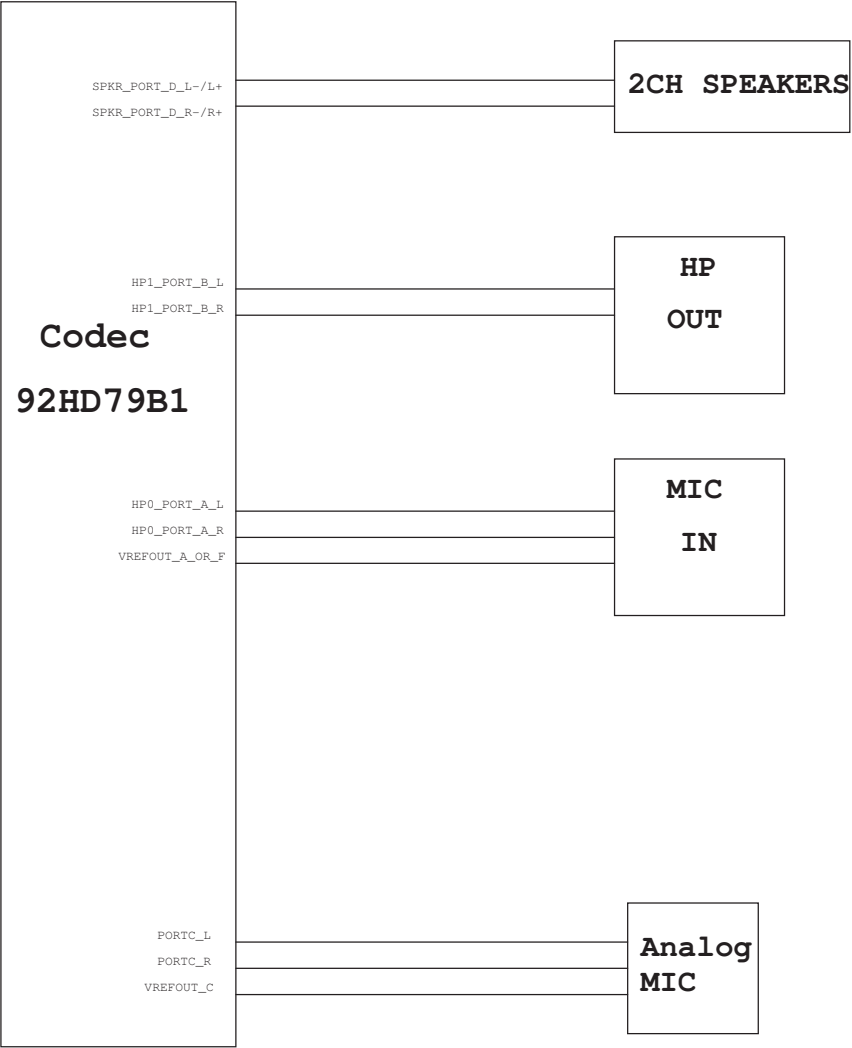
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.2.3

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance / PCI Express* Port Config 1 bit 1 (Port 1-4), Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers: Offset 224h). This signal has a weak internal pull-down.
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4), Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Config Registers: Offset 224h).
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6), Rising Edge of PWROK	This signal has a weak internal pull-up. Sets bit 2 of RPC.PC2 (Chipset Config Registers: Offset 0224h) when sampled low.
GPIO20	Reserved, Rising Edge of PWROK	This signal has a weak internal pull-down. NOTE: This signal should not be pulled high
GNT1# / GPIO51	ESI Strap (Server Only), Rising Edge of PWROK.	Tying this strap low configures DMI for ESIncompatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3# / GPIO55	Top-Block Swap override, Rising Edge of PWROK.	Sampled low: this indicates that the system is strapped to the "top-block swap" mode (IntelR ICH9 inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers: Offset 3414h: bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#	Boot BIOS Destination Selection 1, Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h: bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. <div> <div>Bit11 (GNT0#)</div> <div>Bit 10 (SPI_CS1#)</div> <div>Boot BIOS Destination</div> <div> <div>0</div> <div>1</div> <div>1</div> <div>0</div> </div> <div> <div>SPI</div> <div>PCI</div> <div>LPC</div> <div>Reserved</div> </div> </div>
SPI_CS1# / GPIO58	Boot BIOS Destination Selection 0, Rising Edge of CLPWROK	Controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h: bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. <div> <div>Bit11 (GNT0#)</div> <div>Bit 10 (SPI_CS1#)</div> <div>Boot BIOS Destination</div> <div> <div>0</div> <div>1</div> <div>1</div> <div>0</div> </div> <div> <div>SPI</div> <div>PCI</div> <div>LPC</div> <div>Reserved</div> </div> </div>
SATALED#	PCI Express Lane Reversal (Lanes 1-4). Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0: Offset D8)
SPKR	No Reboot, Rising Edge of PWROK.	Sampled high: this indicates that the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h: bit 5).
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33 / HDA_DOCK_EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK. (Mobile Only)	Sampled low: the Flash Descriptor Security will be overridden. Sampled high: the security measures will be in effect. This strap should only be enabled in manufacturing environments.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be high for mobile applications.
SPI_MOSI (Mobile Only)	Integrated TPM Enable. Rising Edge of CLPWROK.	Sampled low: the Integrated TPM will be disabled. Sampled high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enabled. NOTE: This signal is required to be floating or pulled low for desktop applications.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.2.3

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRS1PVR/GPIO16	PULL-DOWN 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT0#, GNT[3:1]# / GPIO[55, 53, 51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LAD[3:0]# / FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ0	PULL-UP 20K
LDRQ1 / GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1# / GPIO58 (Desktop Only) / CLGPIO6 (Digital Office Only)	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP3	PULL-UP 20K
USB[11:0] [P,N]	PULL-DOWN 15K

PCIE Routing

LANE1	
LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB Pair	Device
0	USB0 (I/O Board)
1	USB1 (I/O Board 17")
2	USB2
3	USB3
4	BLUETOOTH
5	RESERVED
6	WLAN
7	RESERVED
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 355648 Rev.2.3

Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Others = Reserved
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	ITPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2). 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes, 15->0, 14->1 etc. 1 = Normal operation (default): Lane Numbered in Order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG12	ALLZ	0 =ALLZ mode enabled (Note 3) 1 = Disable (Default)
CFG13	XOR	0 = XOR mode enabled (Note 3) 1 = Disable (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIE	0 = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default) 1 = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA (Note4)	SDVO Present	0 = No SDVO/HDMI/DP interface disabled (default) 1 = SDVO/HDMI/DP interface enabled
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled
DDPC_CTRLDATA (Note4)	Digital Display Present	0 = Digital display (HDMI/DP) device absent (default) 1 = Digital display (HDMI/DP) Device Present
CFG4:3 CFG8 CFG11 CFG14 CFG15 CFG17 CFG18	Reserved	

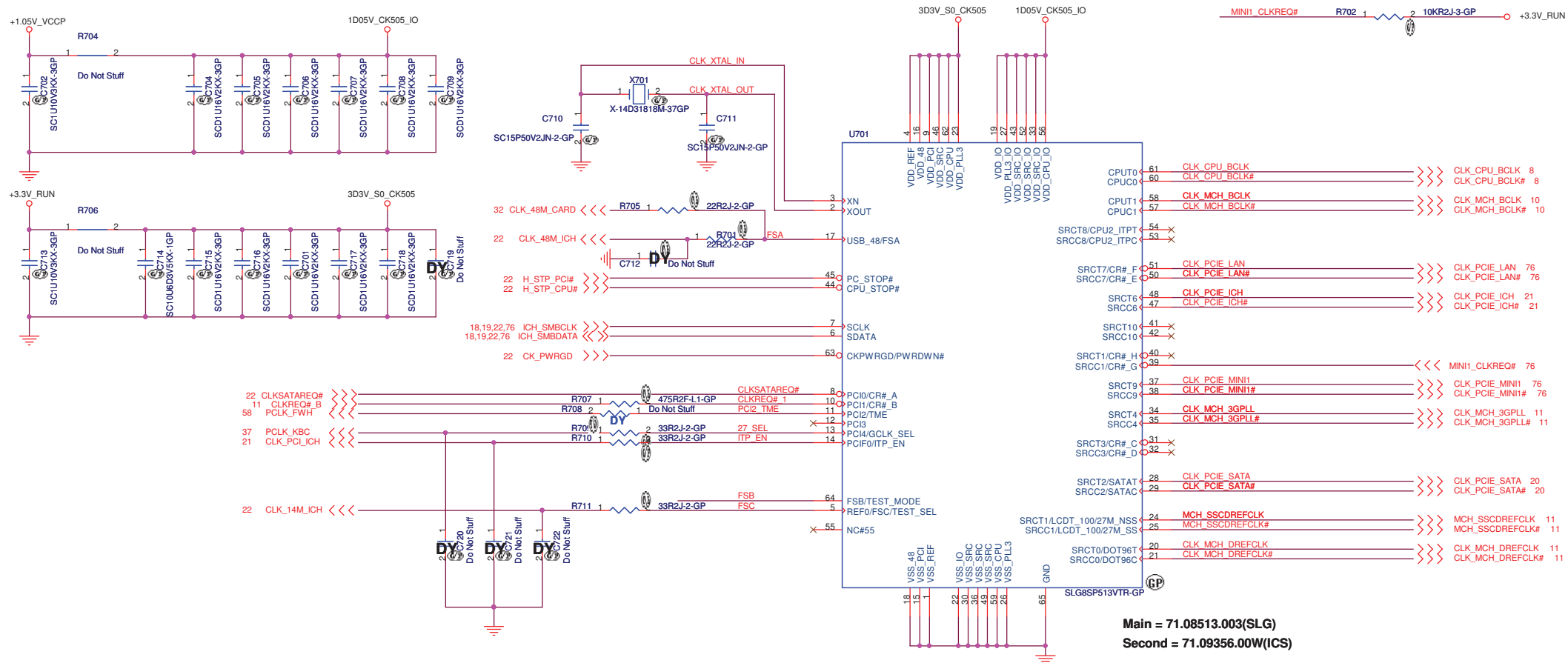
NOTE:

- All strap signals are sampled with respect to the leading edge of the GMCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
- Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.
- DDPC_CTRL_DATA & SDVO_CTRL_DATA straps should both be high to enable Display Port.

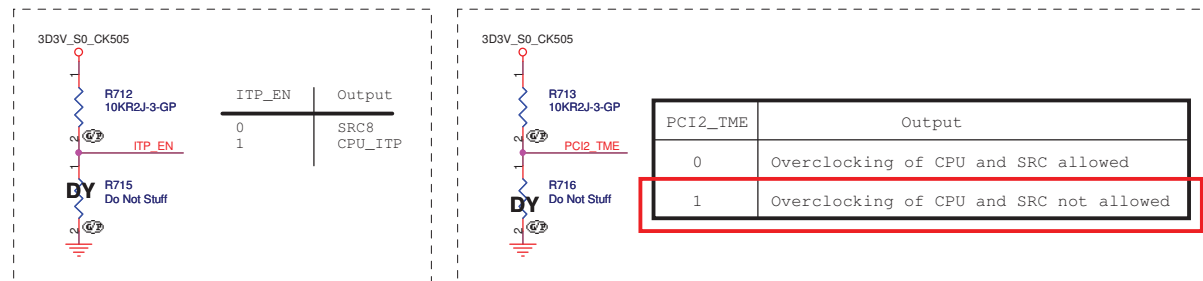
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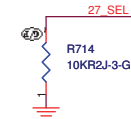
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Second = 71.09356.00W(ICS)

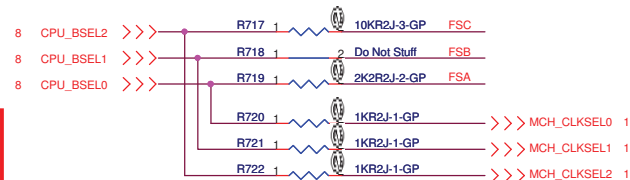


PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed



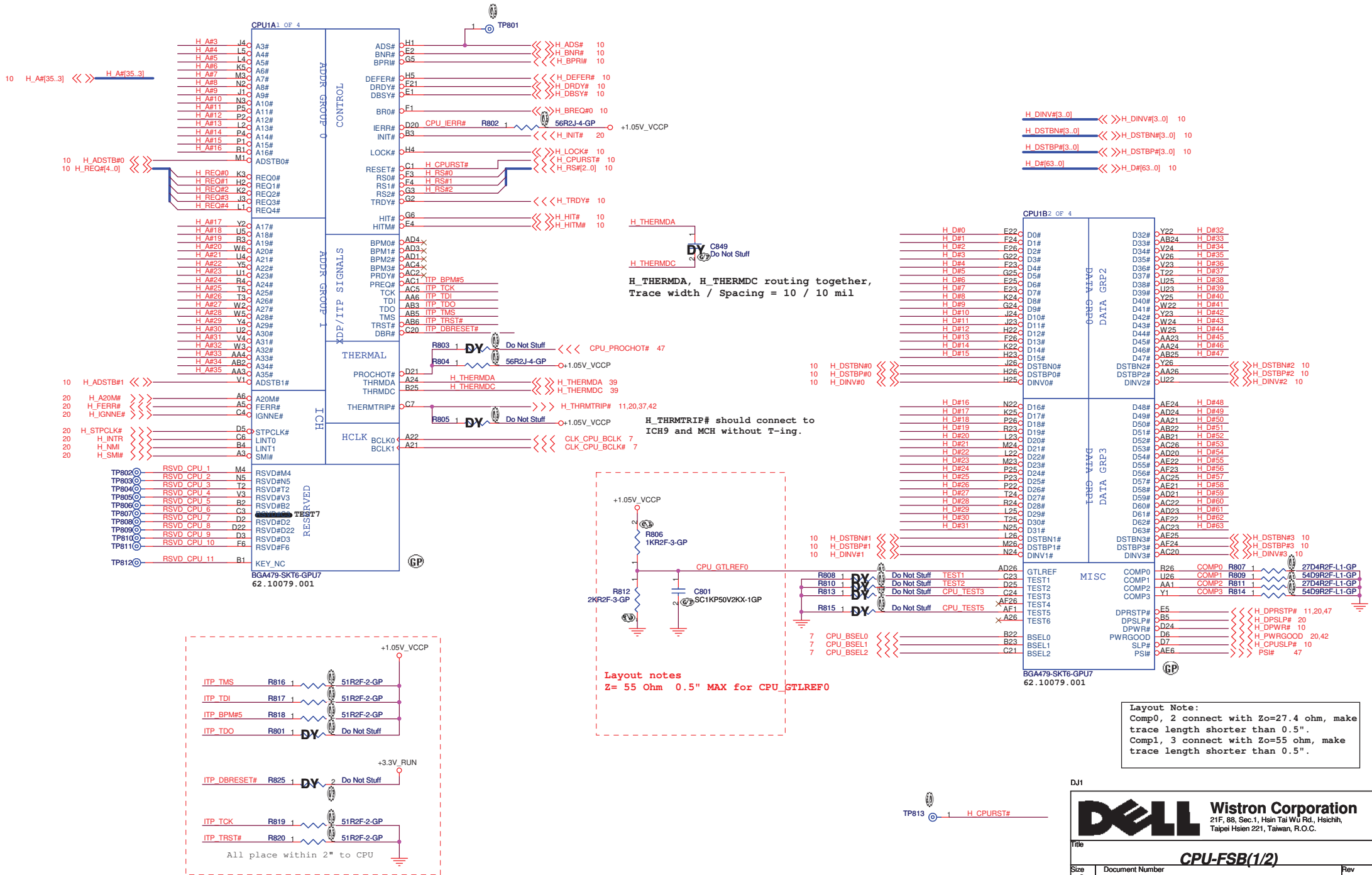
27_SEL	PIN20/21	PIN24/25
0	96M	100M
1	100M	27M

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M



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SSID = CPU



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Rev

CPU-FSB(1/2)

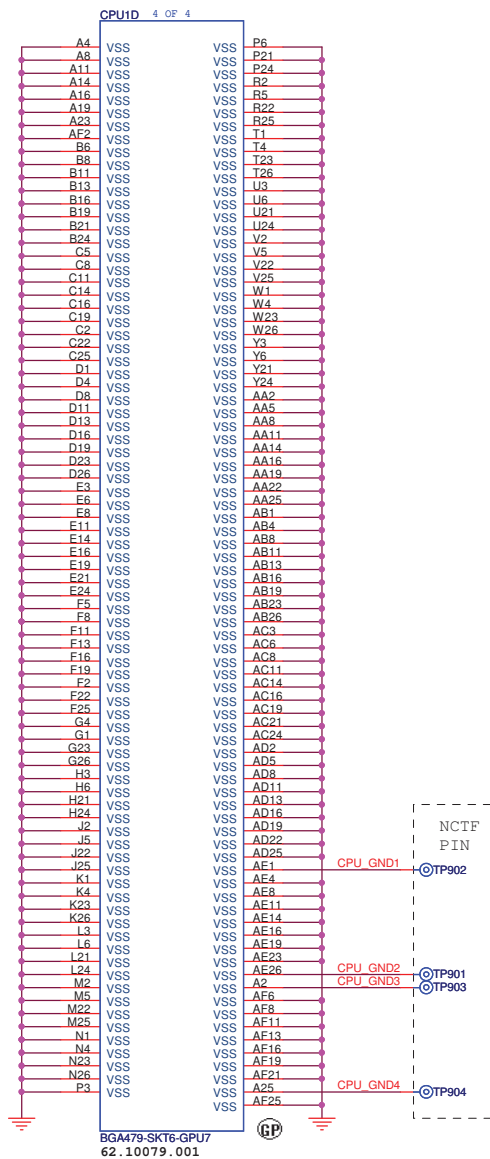
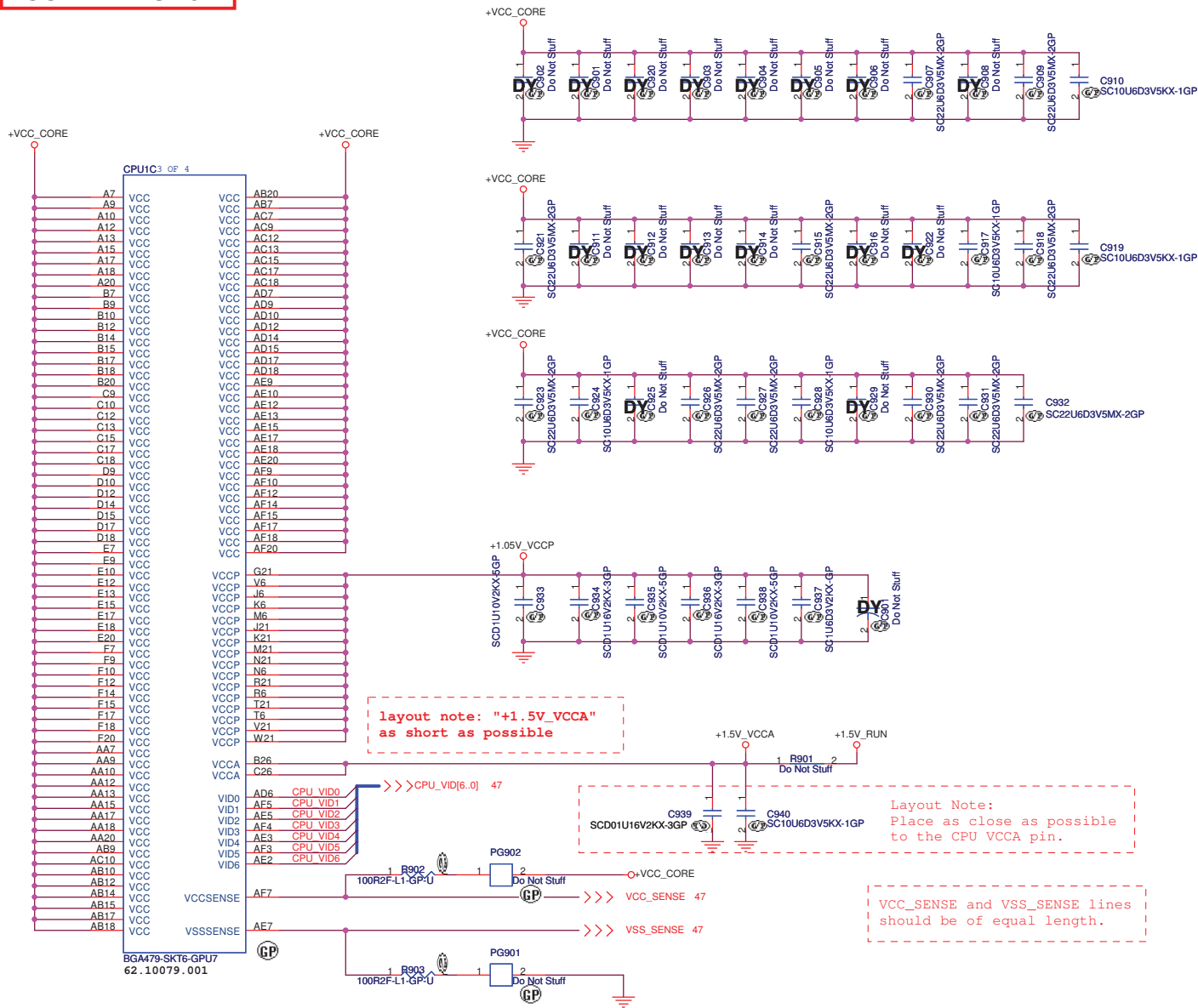
DJ1 Montevina UMA

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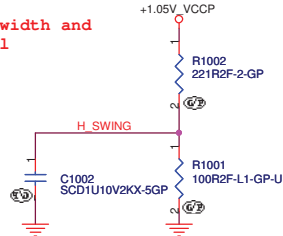
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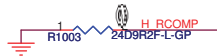
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H_SWING routing Trace width and
Spacing use 10 / 20 mil

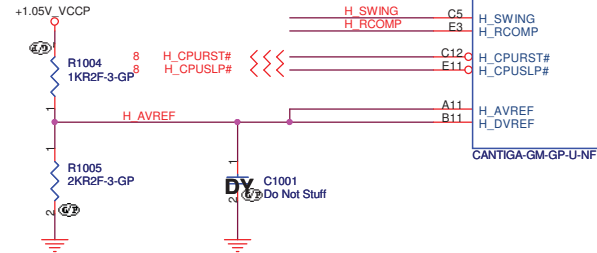
H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)



H_RCOMP routing Trace width and
Spacing use 10 / 20 mil



Place R1001 near to the chip (< 0.5")



NB1A

1 OF 10

H_A#(35..3)

H_A#(35..3) 8

ISOT

H_ADS# 8
H_ADSTB# 0 8
H_ADSTB# 1 8
H_BNR# 8
H_BPRI# 8
H_BREQ# 8
H_DEFER# 8
H_DBSY# 8
HPLL_CLK 7
HPLL_CLK# 7
H_DPWR# 8
H_DRDY# 8
H_HIT# 8
H_HITM# 8
H_LOCK# 8
H_TRDY# 8

H_DINV# 0 8
H_DINV# 1 8
H_DINV# 2 8
H_DINV# 3 8

H_DSTBN# 0 8
H_DSTBN# 1 8
H_DSTBN# 2 8
H_DSTBN# 3 8

H_DSTBP# 0 8
H_DSTBP# 1 8
H_DSTBP# 2 8
H_DSTBP# 3 8

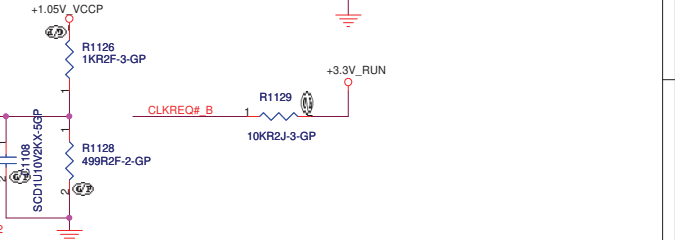
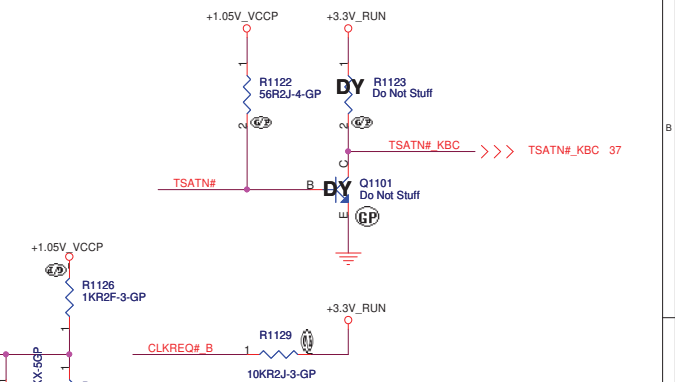
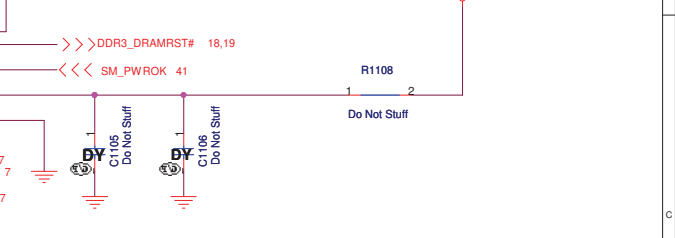
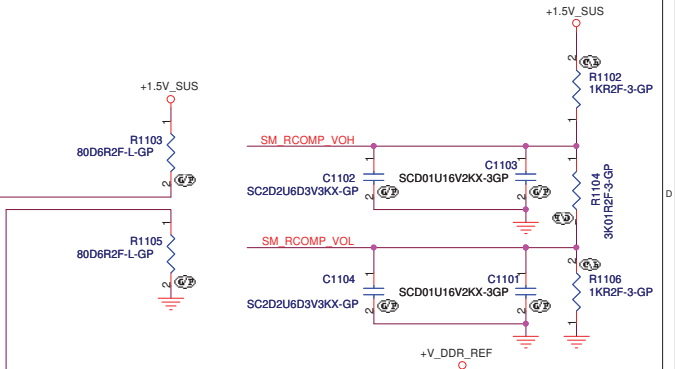
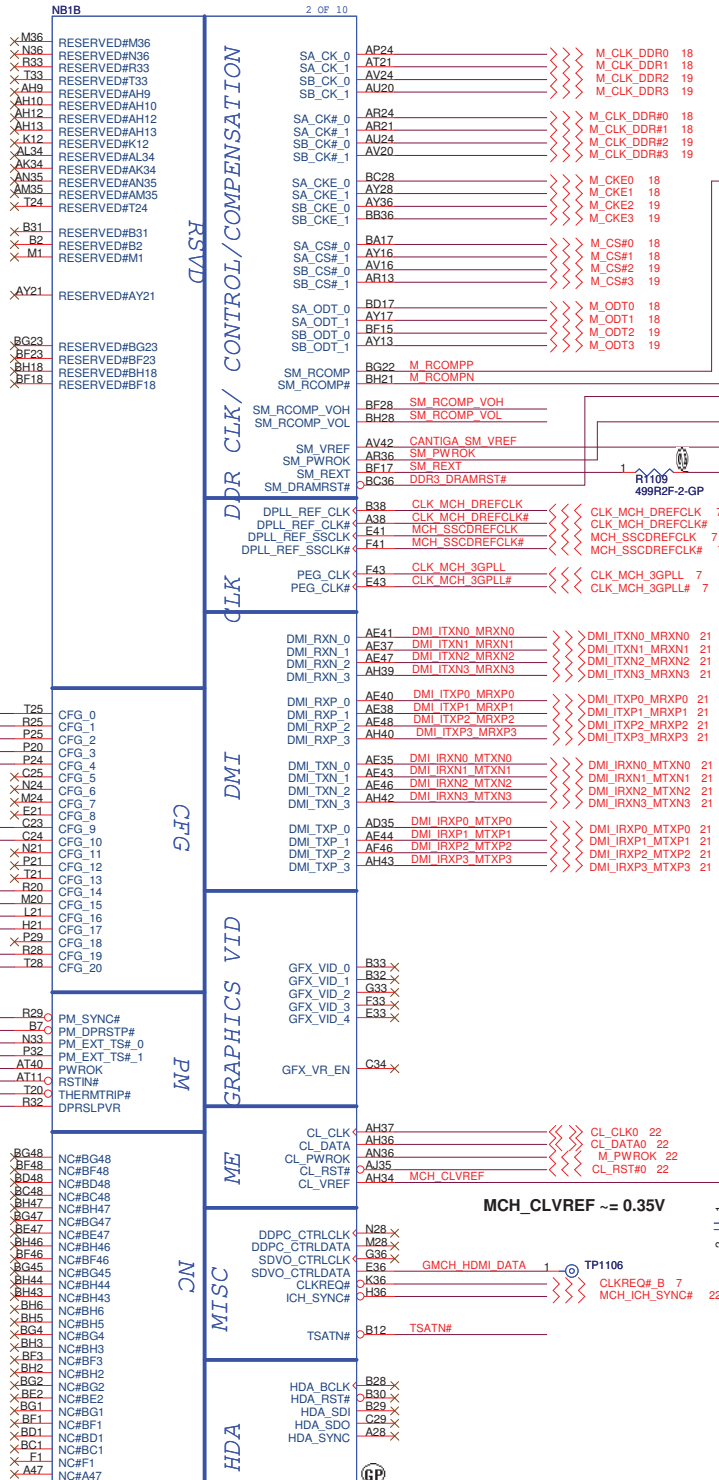
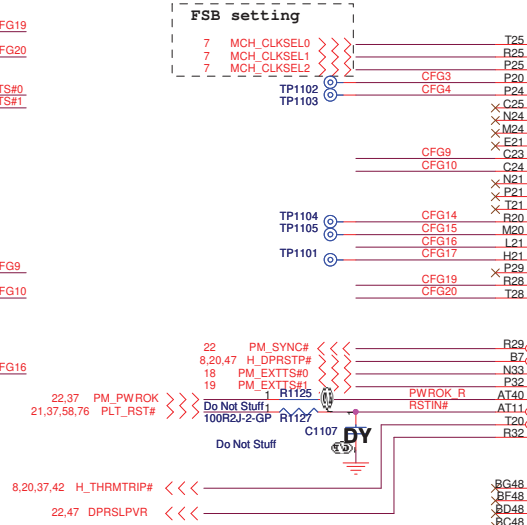
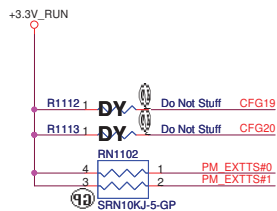
H_REQ# 0 8
H_REQ# 1 8
H_REQ# 2 8
H_REQ# 3 8
H_REQ# 4 8

H_RS# 0 8
H_RS# 1 8
H_RS# 2 8

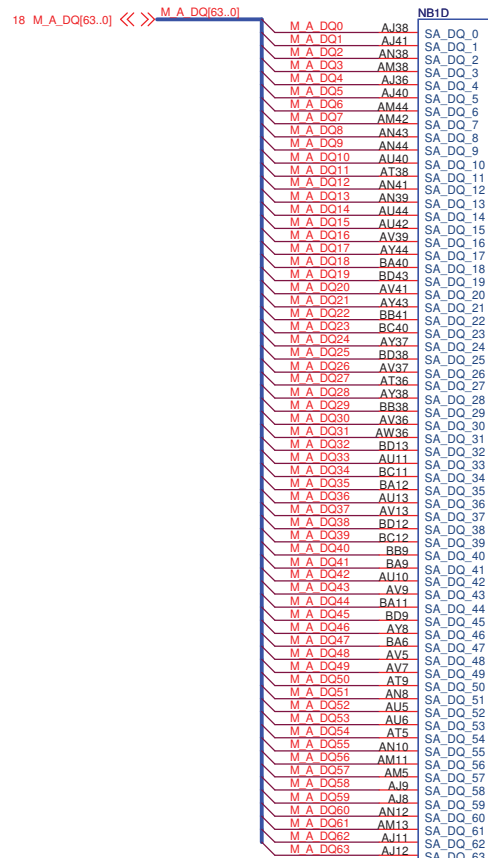
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* is current setting

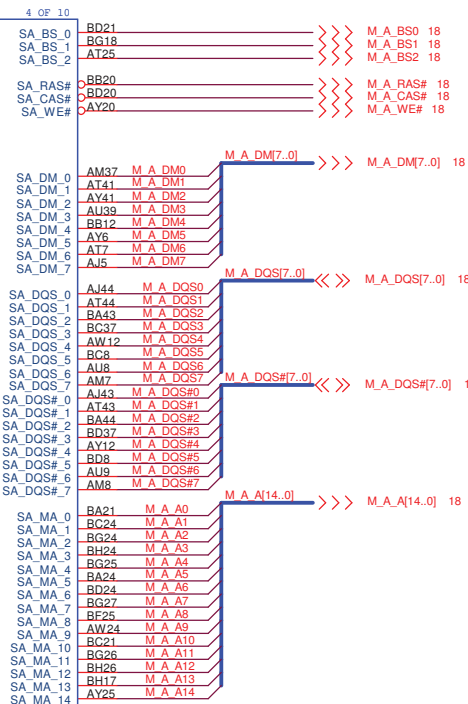
CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 ★
CFG 6	ITPM enable	ITPM disable ★
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality ★
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in order ★
CFG 10	PCIE loopback enable	PCIE loopback disable ★
CFG 12	ALLZ mode enable	ALLZ mode disable ★
CFG 13	XOR mode enable	XOR mode disable ★
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable ★
CFG 19	Normal operation ★	Reverse DMI lanes
DMI Lane Reserved		PCIE and SDVO are operating simultaneously via the PEG port
CFG 20		
SDVO concurrent with PCIE	Only PCIE or SDVO is operational ★	
SDVO_CTRLDATA	SDVO interface disable ★	SDVO interface enable
L_DDC_DATA	LFP disable ★	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled ★	SDVO/iHDMI/DP interface enabled



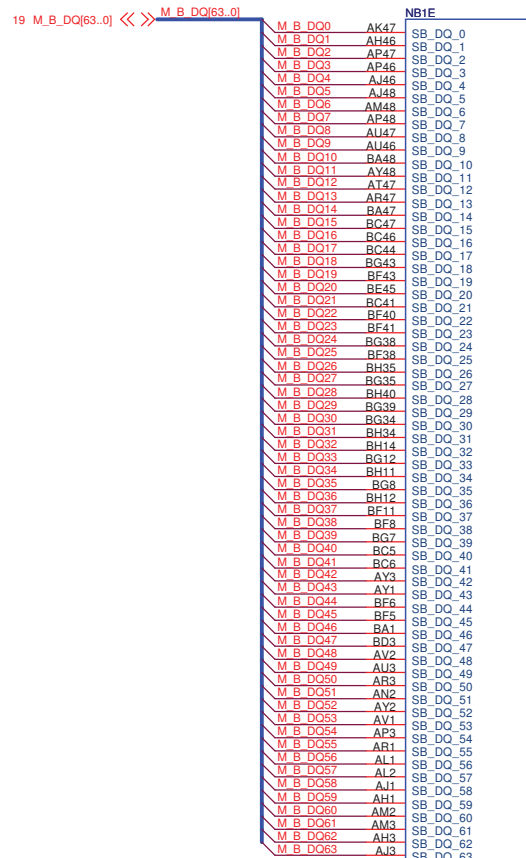
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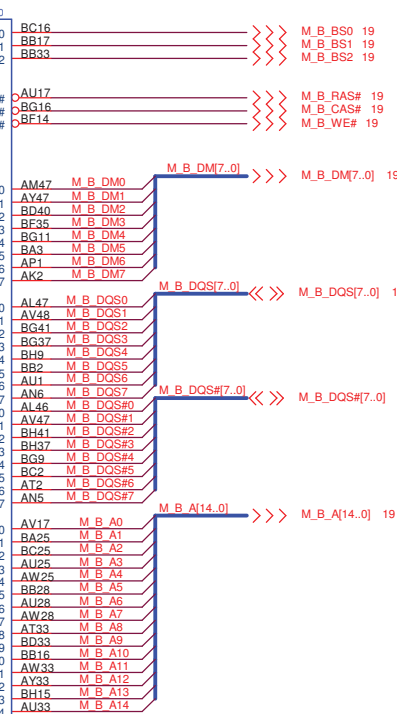
DDR SYSTEM MEMORY A



CANTIGA-GM-GP-U-NF



DDR SYSTEM MEMORY B

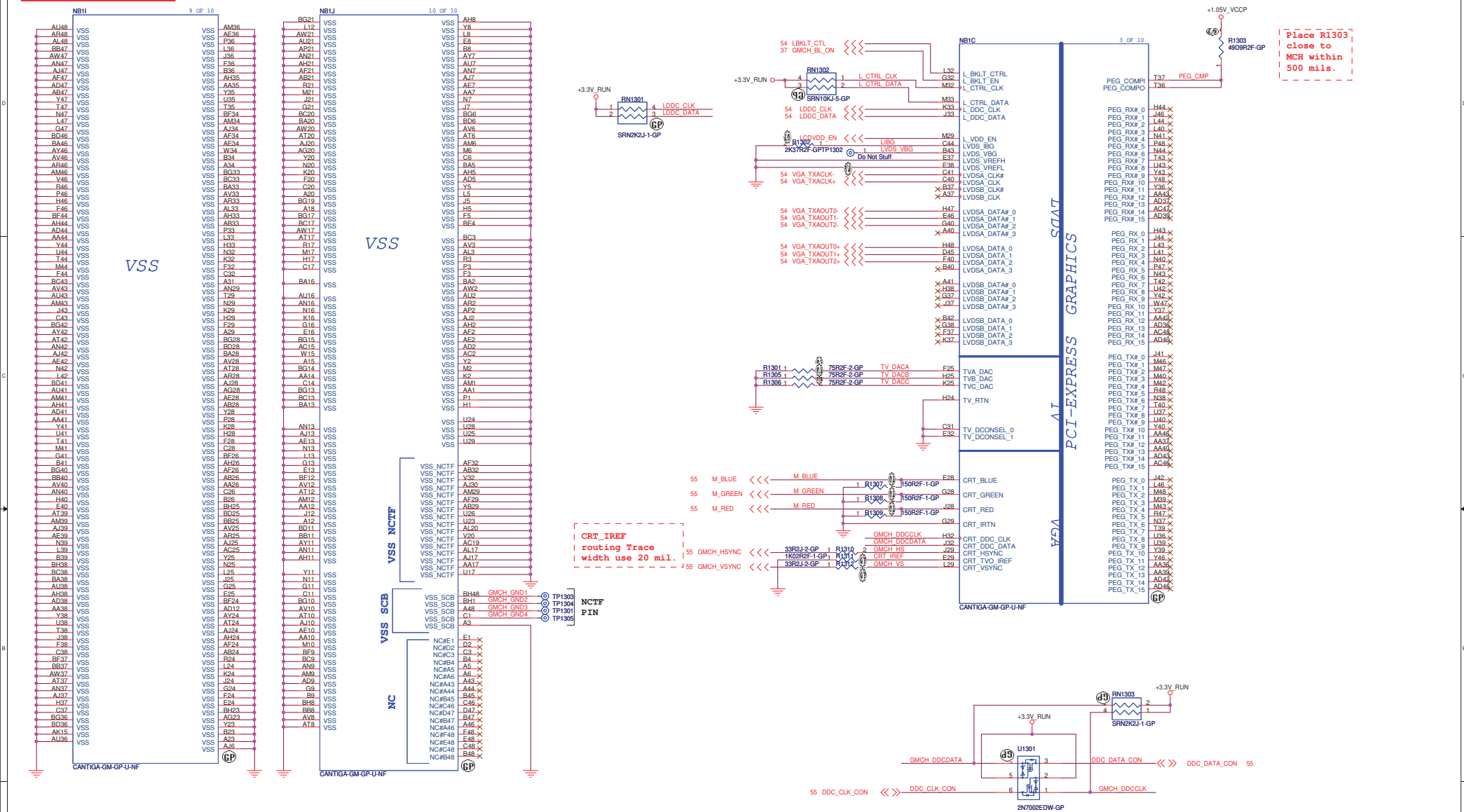


CANTIGA-GM-GP-U-NF

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Cantiga-DDR(3/6)					
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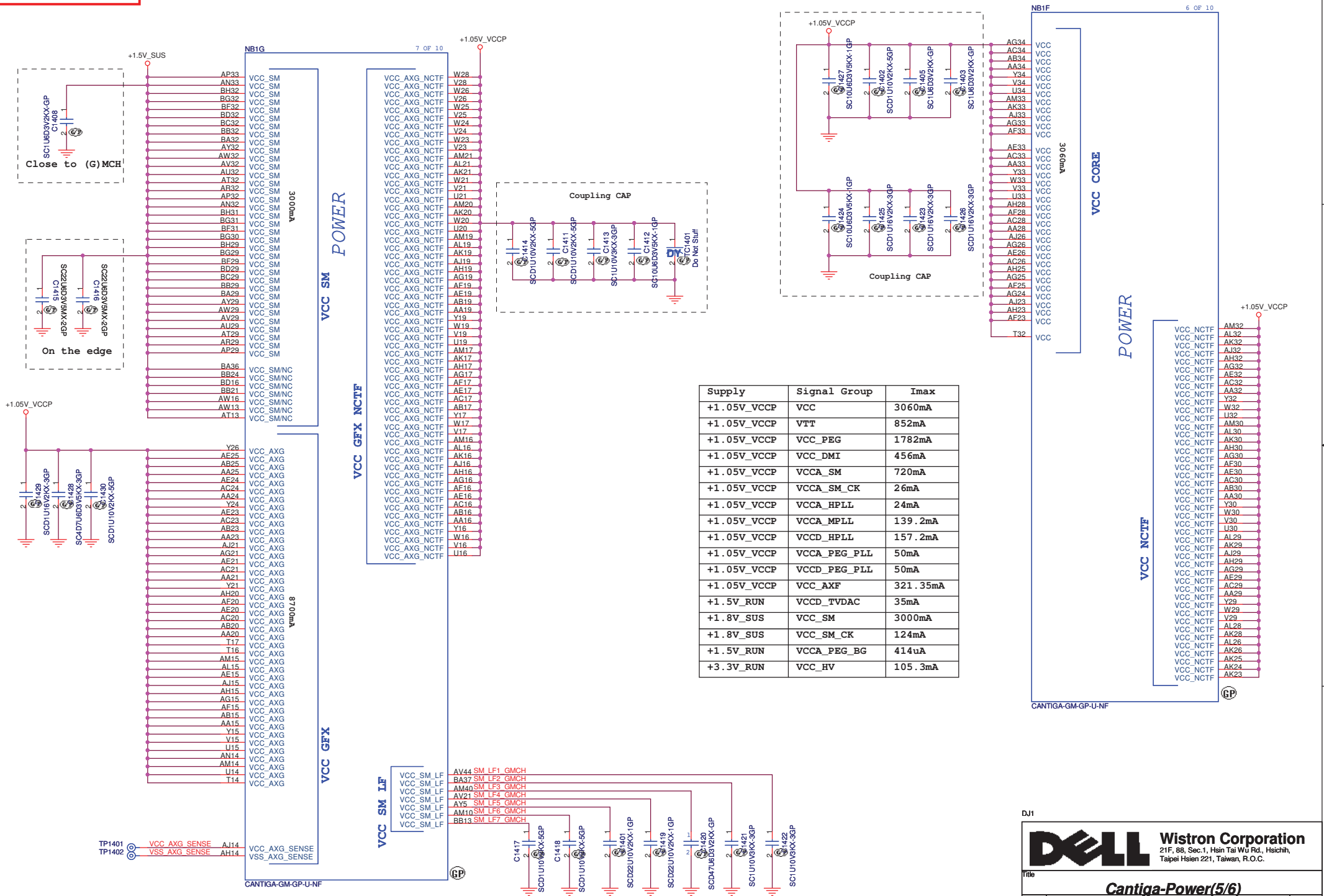
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File **Cantiga-GND/LVDS/VGA(4/6)**
Size Document Number
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SSID = MCH



Supply	Signal Group	Imax
+1.05V_VCCP	VCC	3060mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCCD_TVDC	35mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+1.5V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

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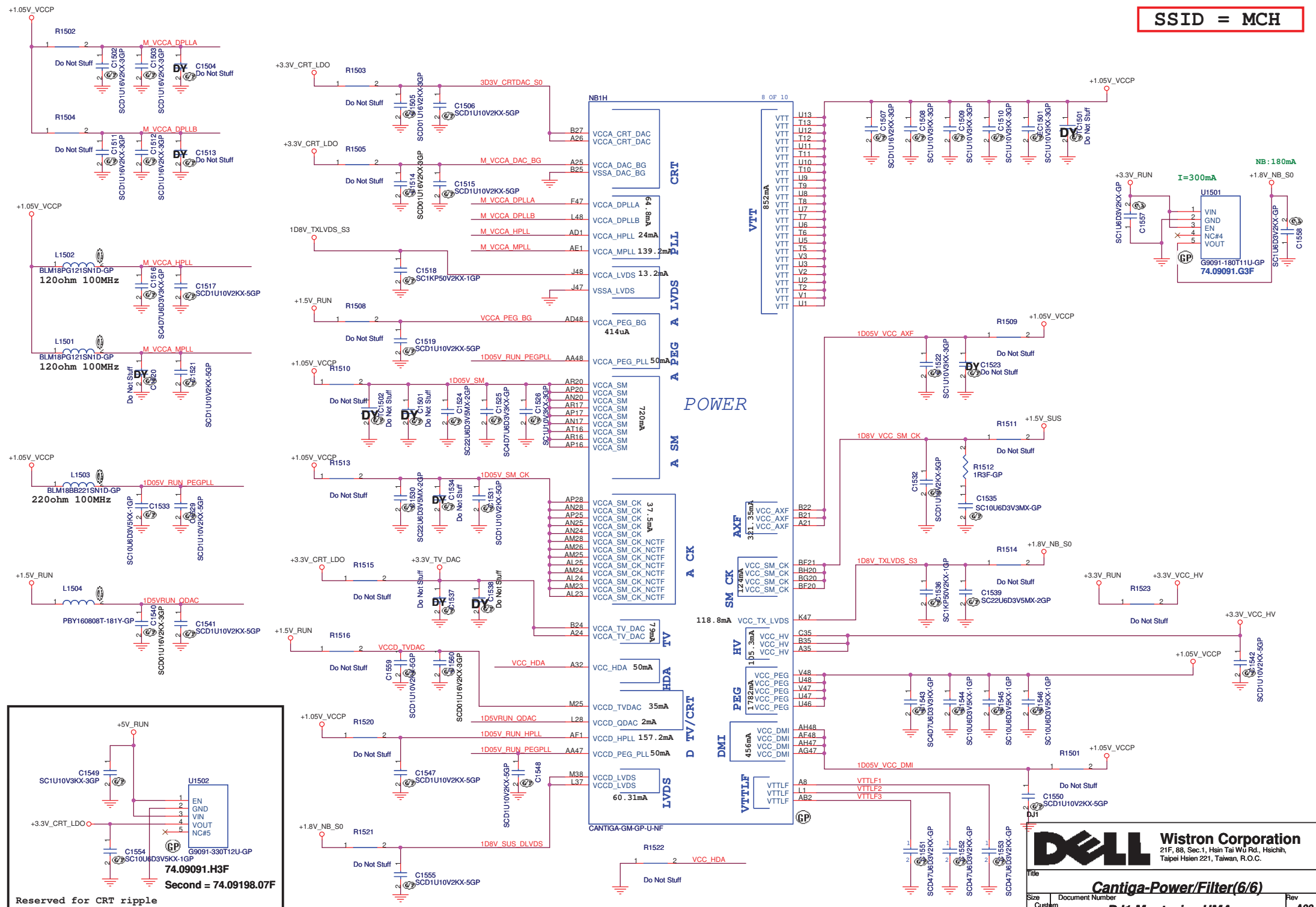
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Title: **Cantiga-Power(5/6)**

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SSID = MCH



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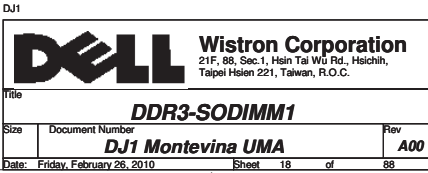
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DJ1 Montevina UMA

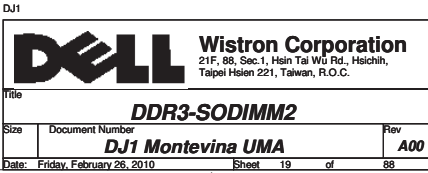
Date: Wednesday, February 24, 2010

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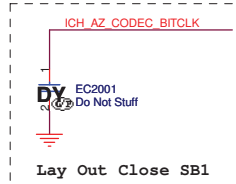
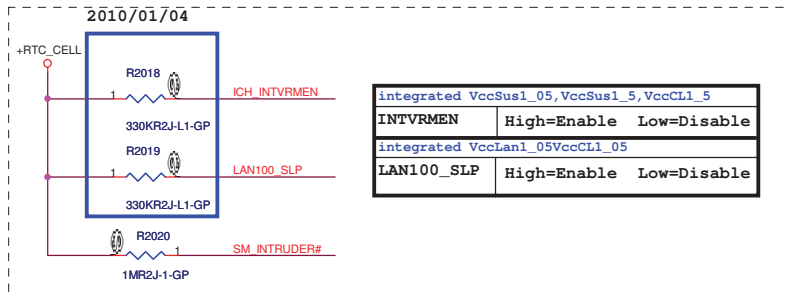
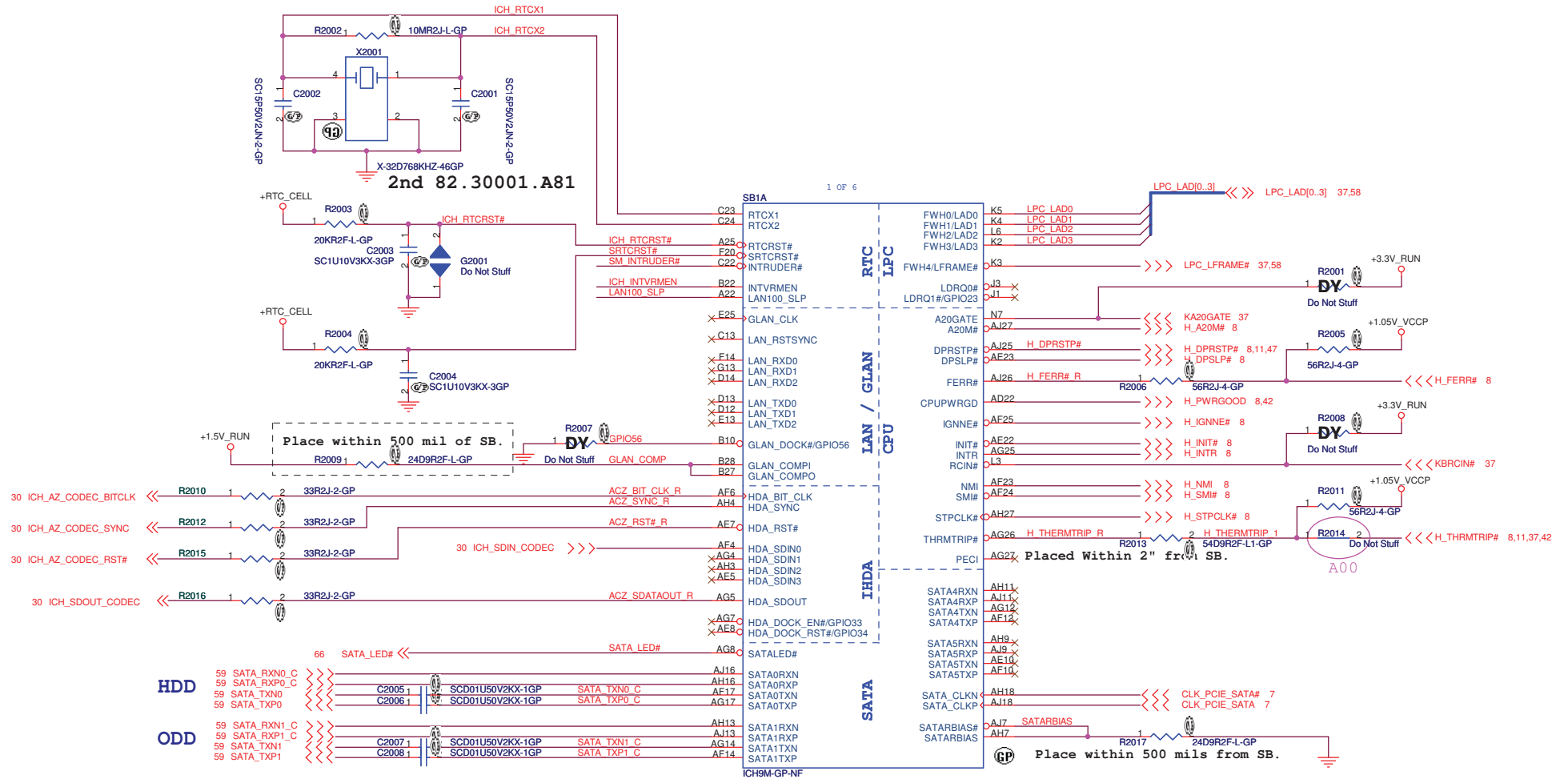
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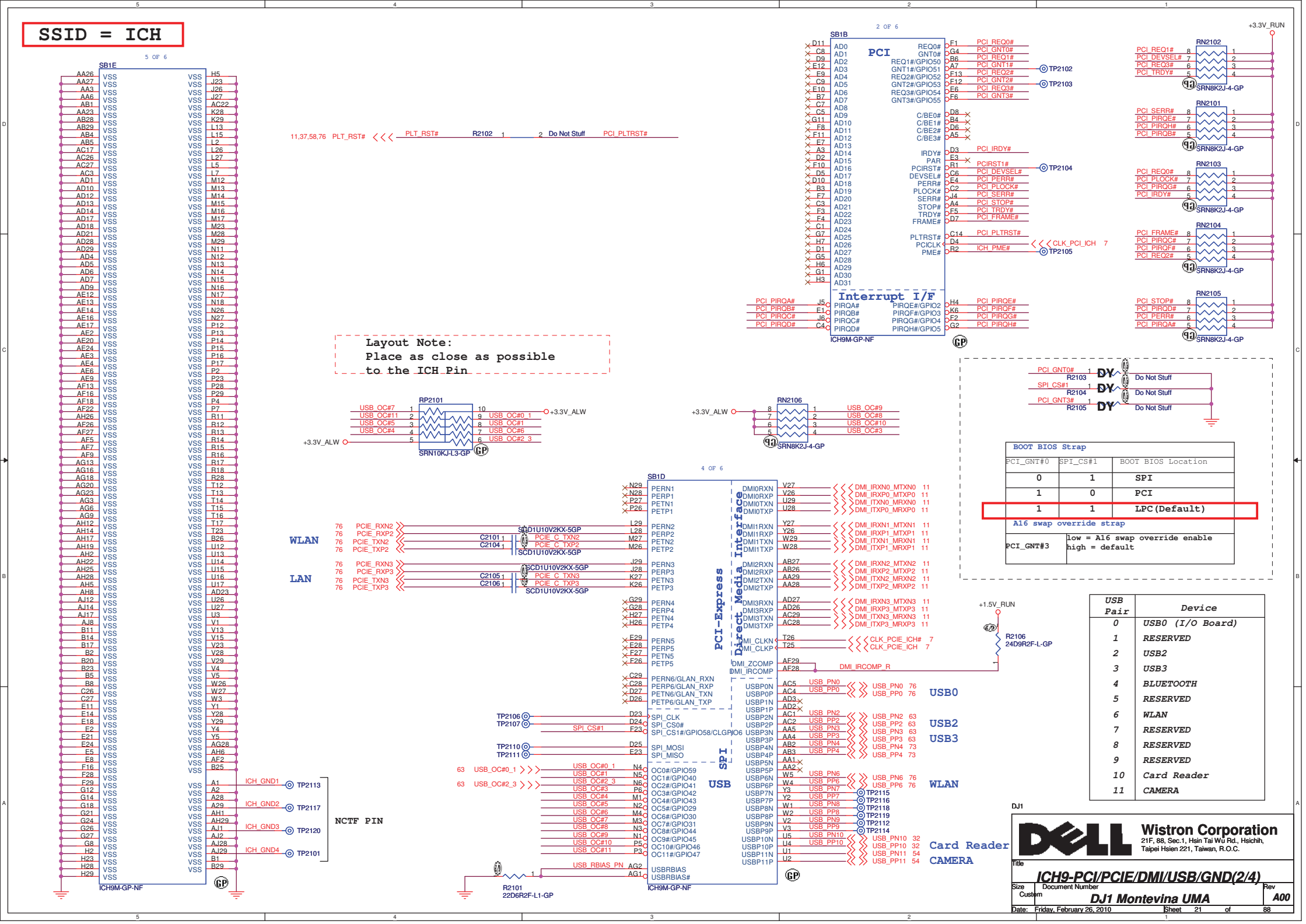




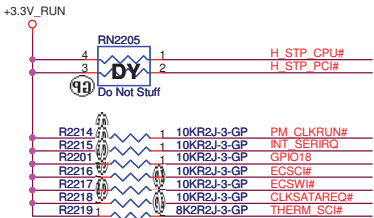
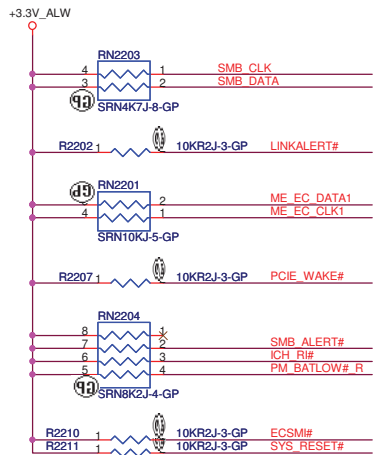
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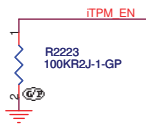
SSID = ICH



SSID = ICH



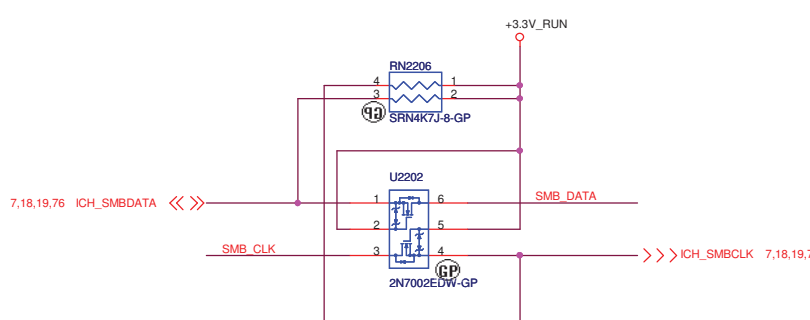
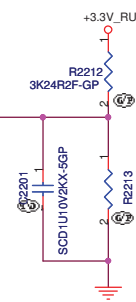
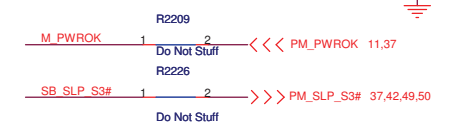
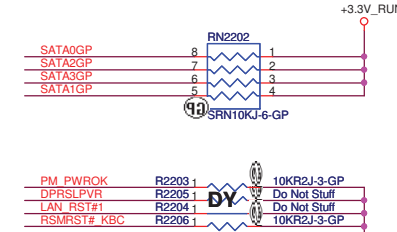
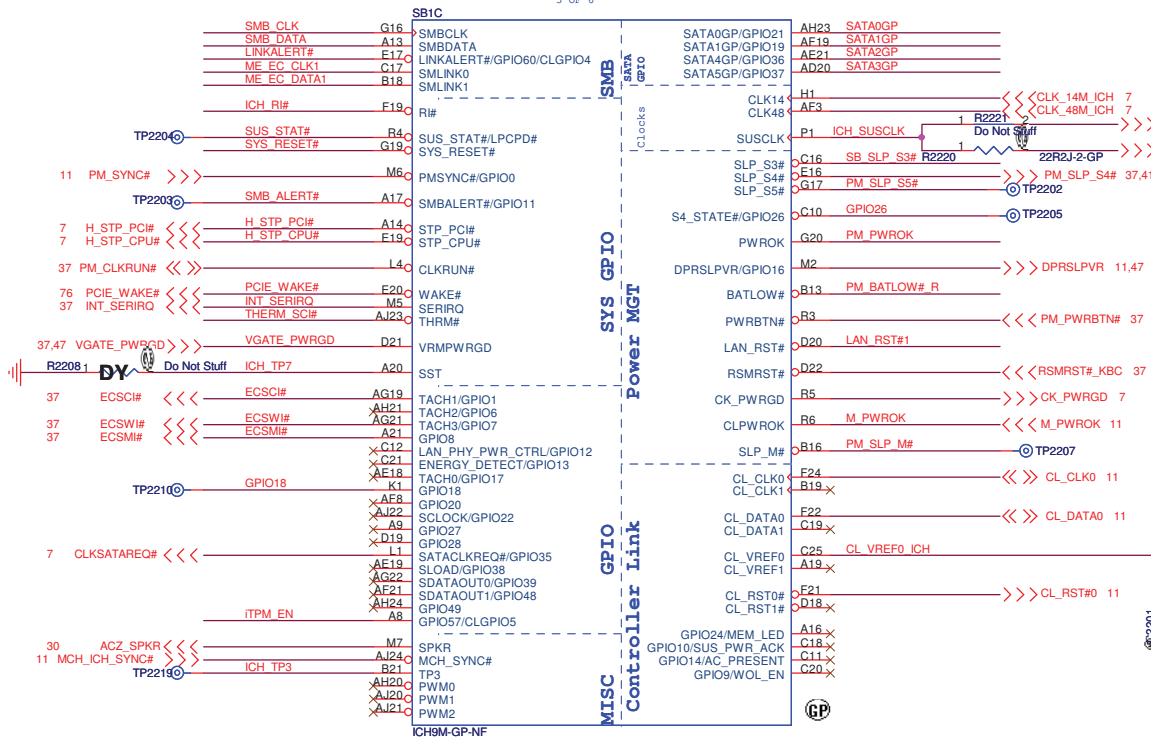
iTPM Select(Not Strap Pin)



iTPM_EN


0 = Disable

1 = Enable



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DJ1



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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Title

Size
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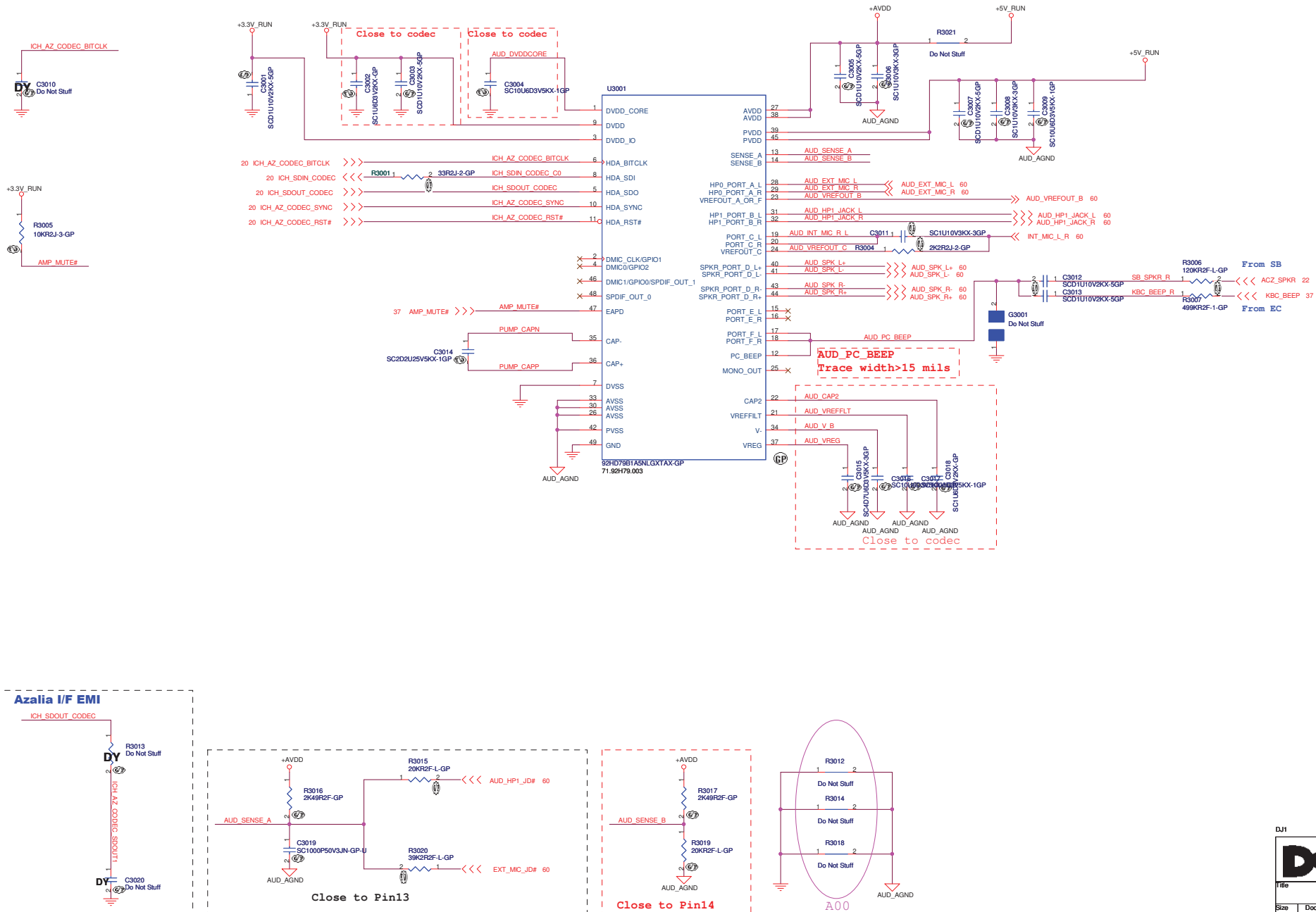
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SSID = AUDIO



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DJ1



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Document Number
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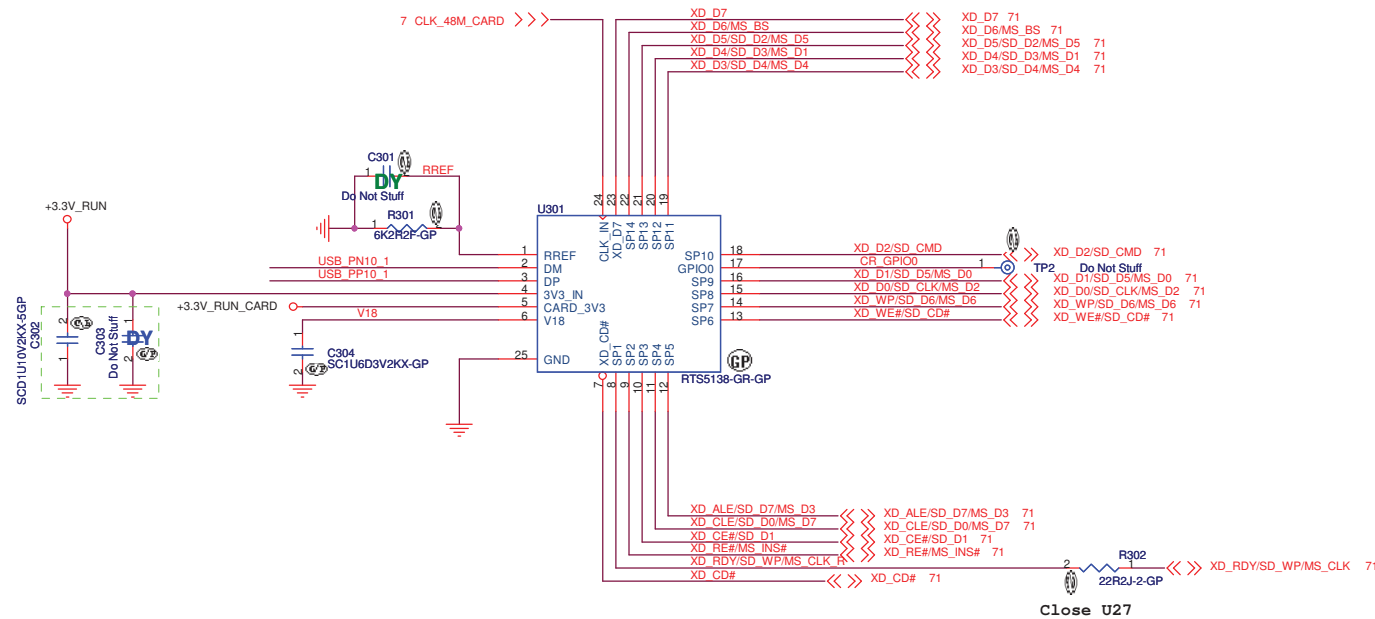
Date: Wednesday, February 24, 2010

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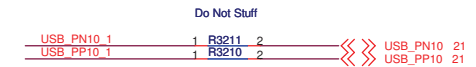
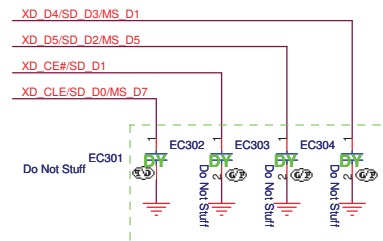
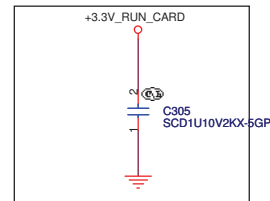
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Reserved

SSID = SDIO



Close to U301




Do Not Stuff

Do Not Stuff
2010/01/05

DJ1

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DJ1



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Title

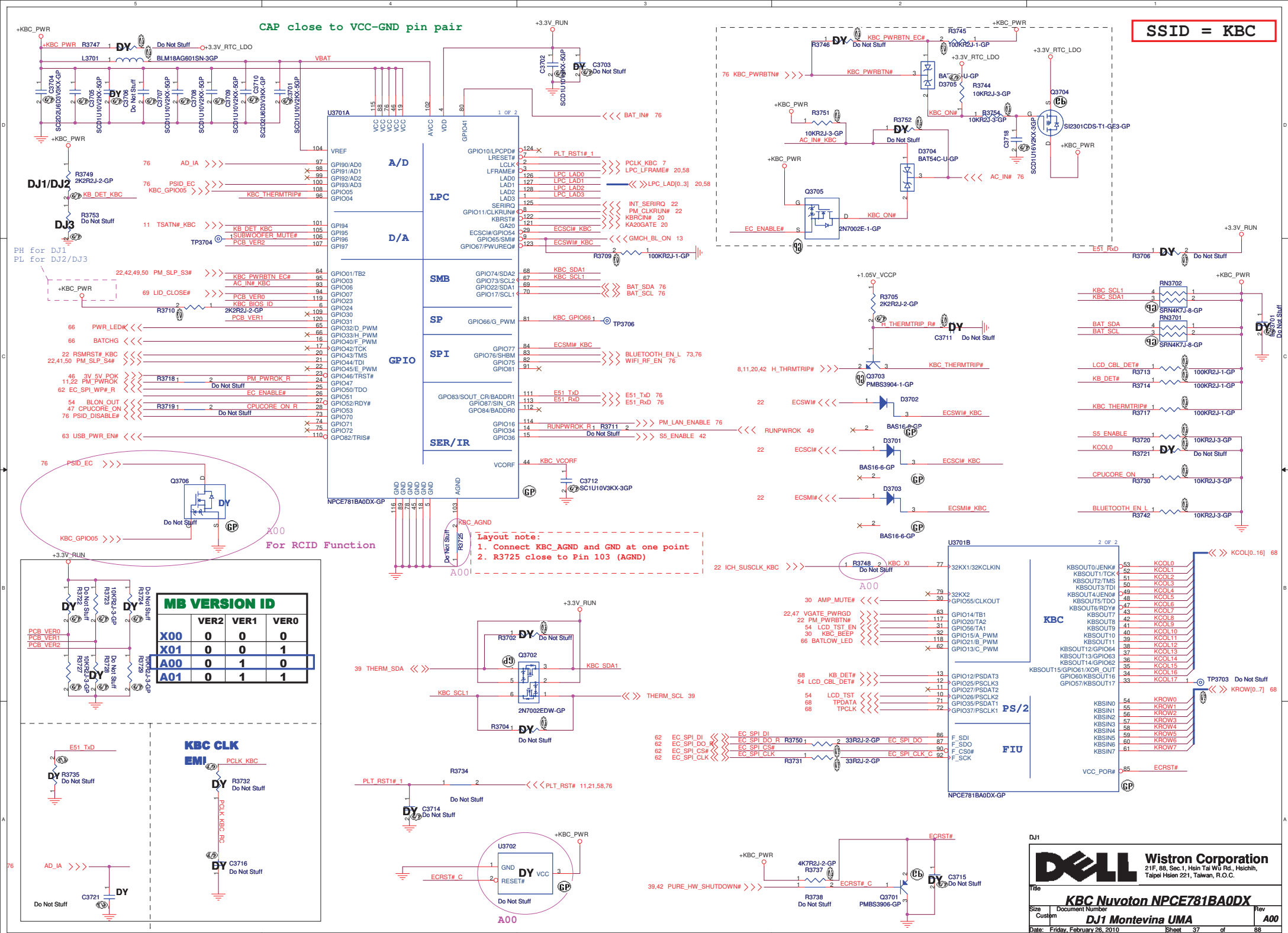
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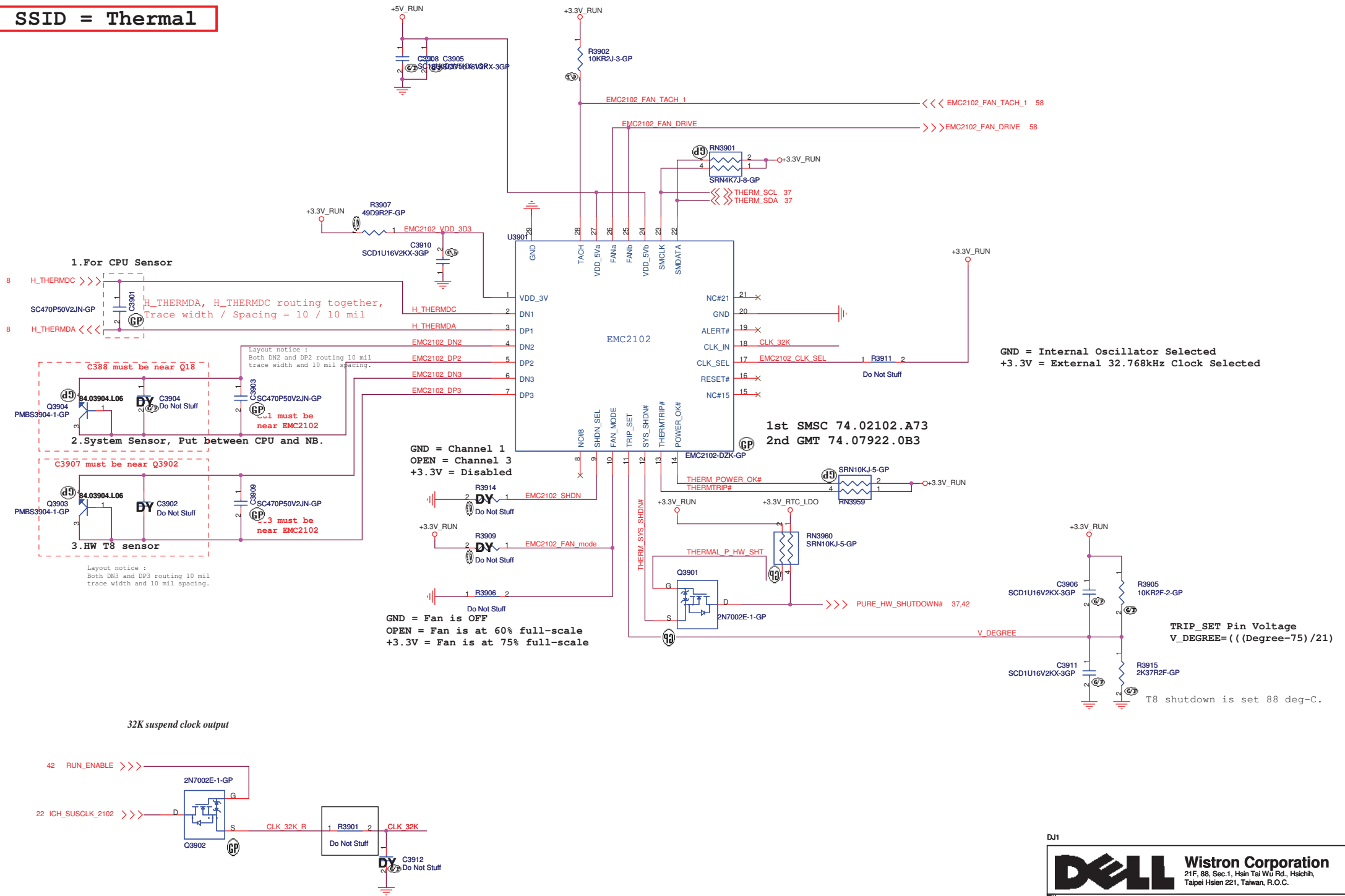
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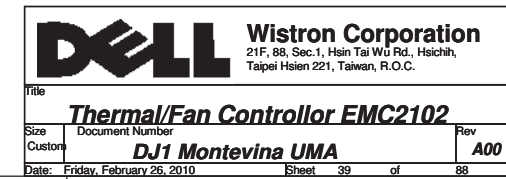
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SSID = Thermal




DJ1



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Title

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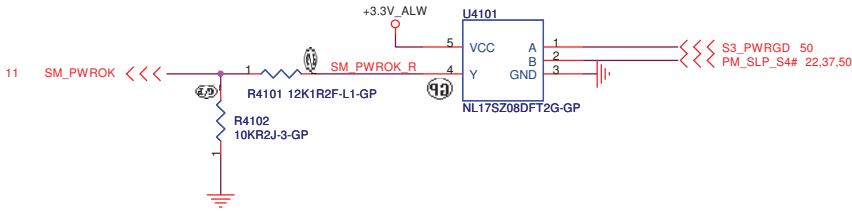
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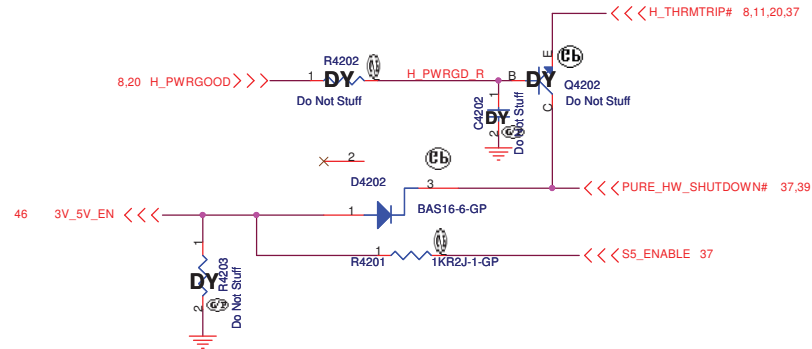
SSID = Reset.Suspend



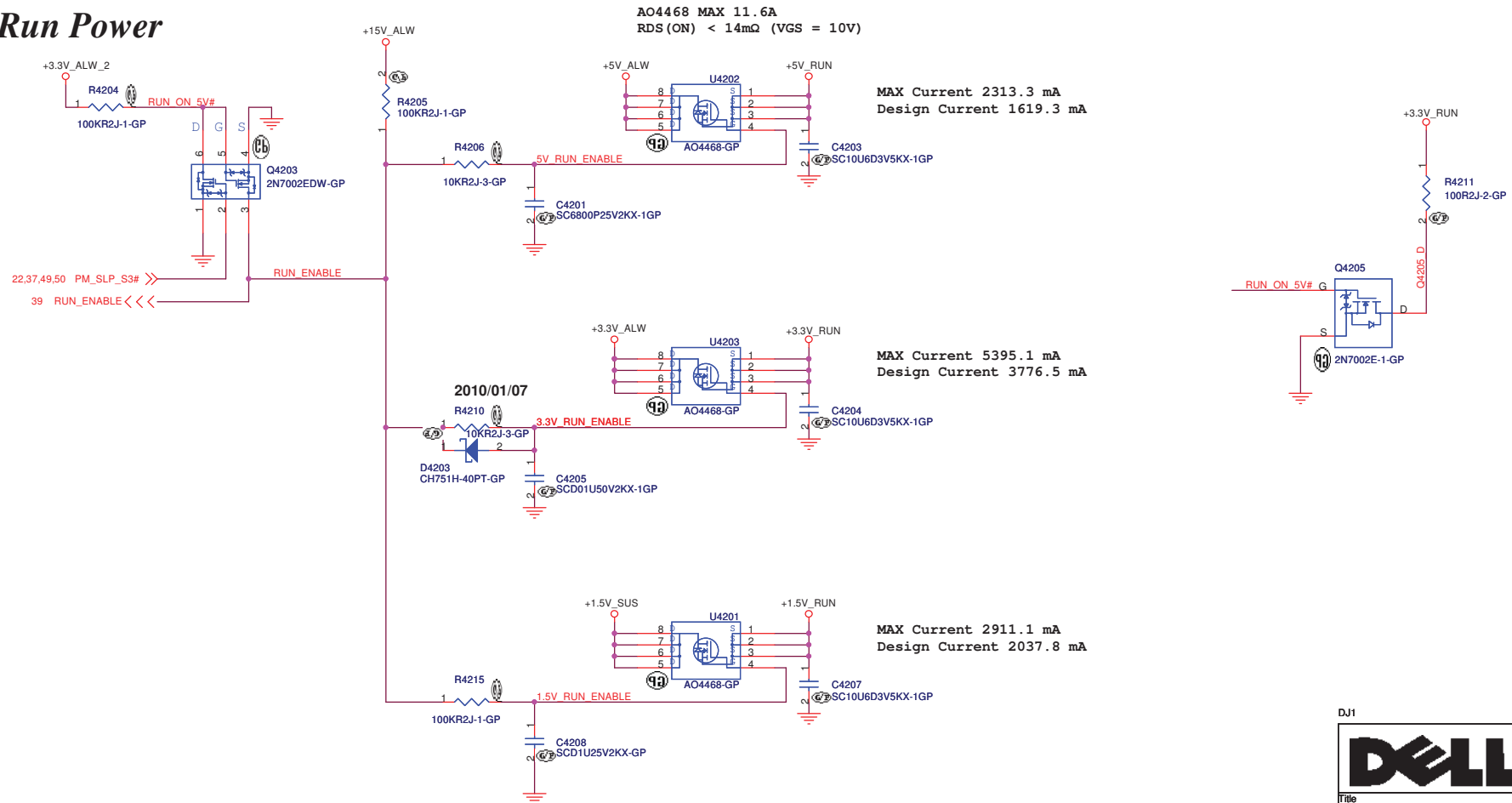
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DELL		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Power On Logic			
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SSID = Reset.Suspend




Run Power



DJ1

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Title

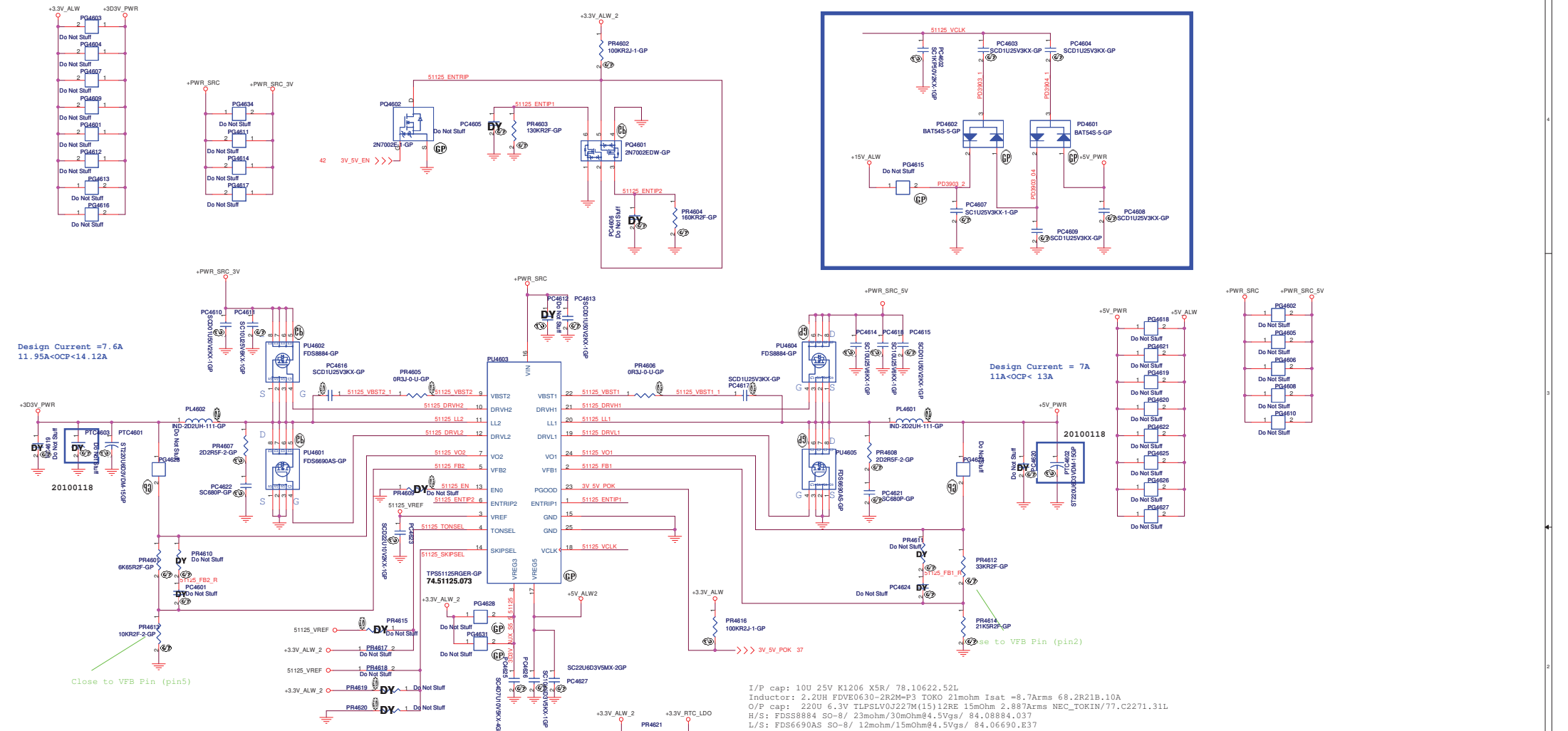
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DJ1 Montevina UMA

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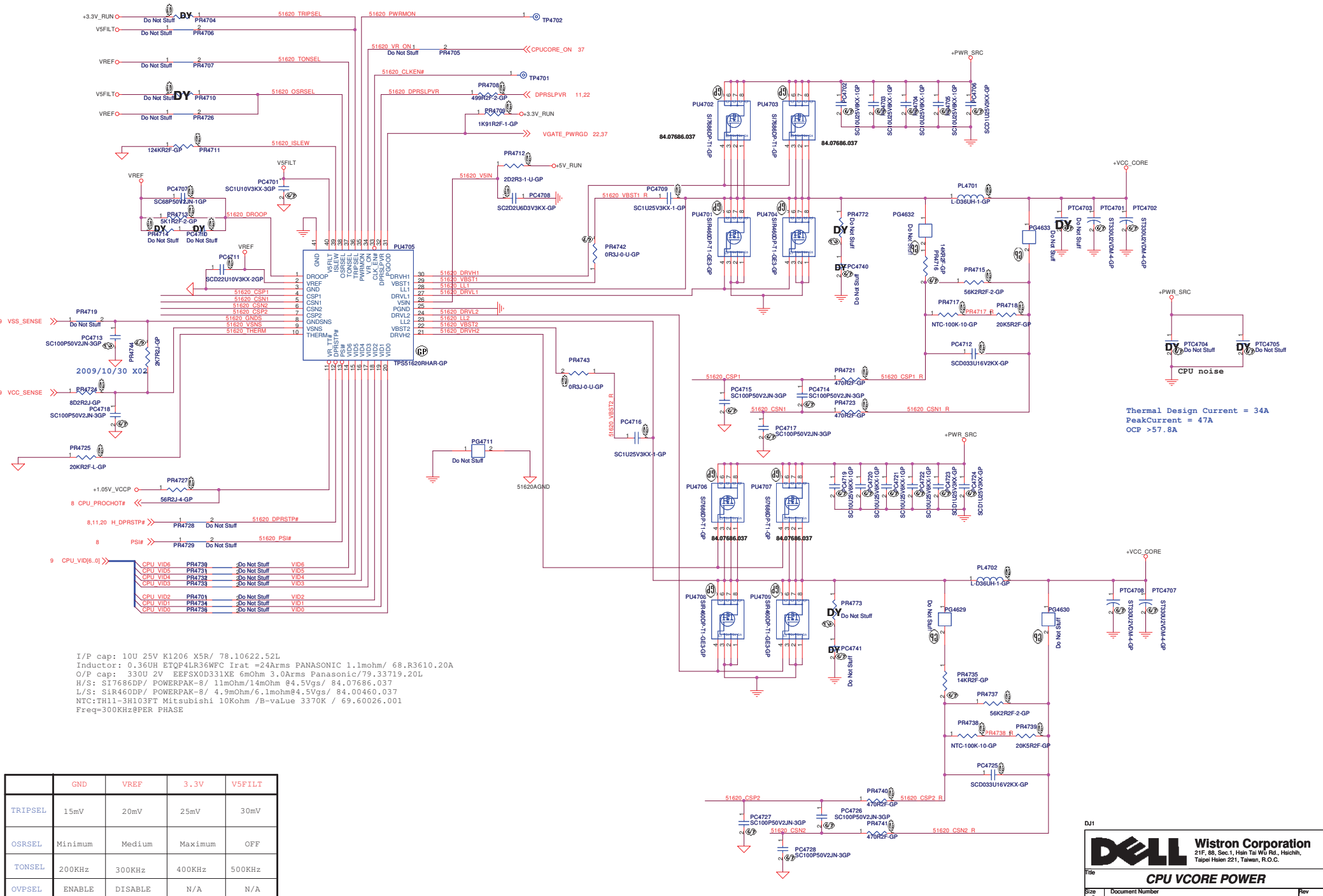
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I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVE0630-2R2M-P3 TOKO 21mohm Isat =8.7Arms 68.2R21B.10A
O/P cap: 220U 6.3V TLP5L0J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37


TONSEL	CH1	CH2	SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
GND	200kHz	265kHz	Operating Mode	ORA Auto Skip	Auto Skip	PWM only
VREF	245kHz	305kHz				
VREG3	300kHz	375kHz	EN0	Open	820kΩ to GND	GND
VREG5	365kHz	460kHz	Operating Mode	enable both LDos, VCLK on and ready to turn on switcher channels	enable both LDos, VCLK off and ready to turn on switcher channels	disable all circuit

SSID = CPU.Regulator



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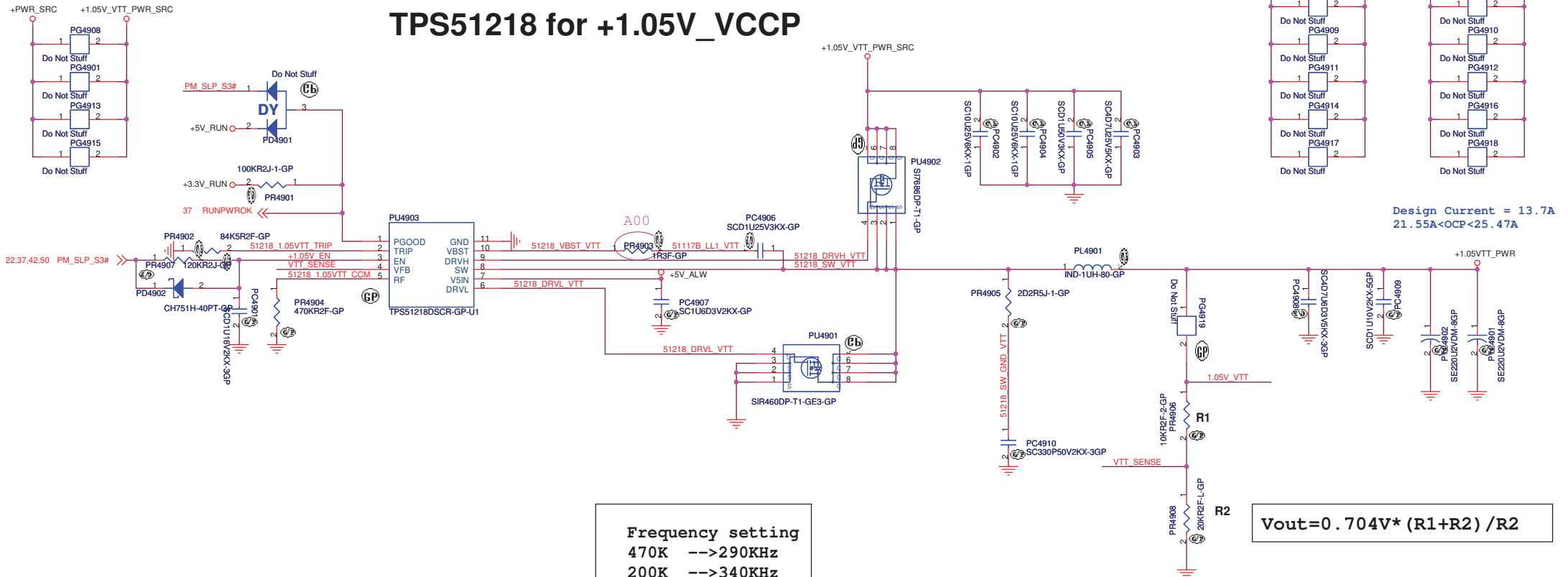
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SSID = PWR.Plane.Regulator_1p05v

TPS51218 for +1.05V_VCCP

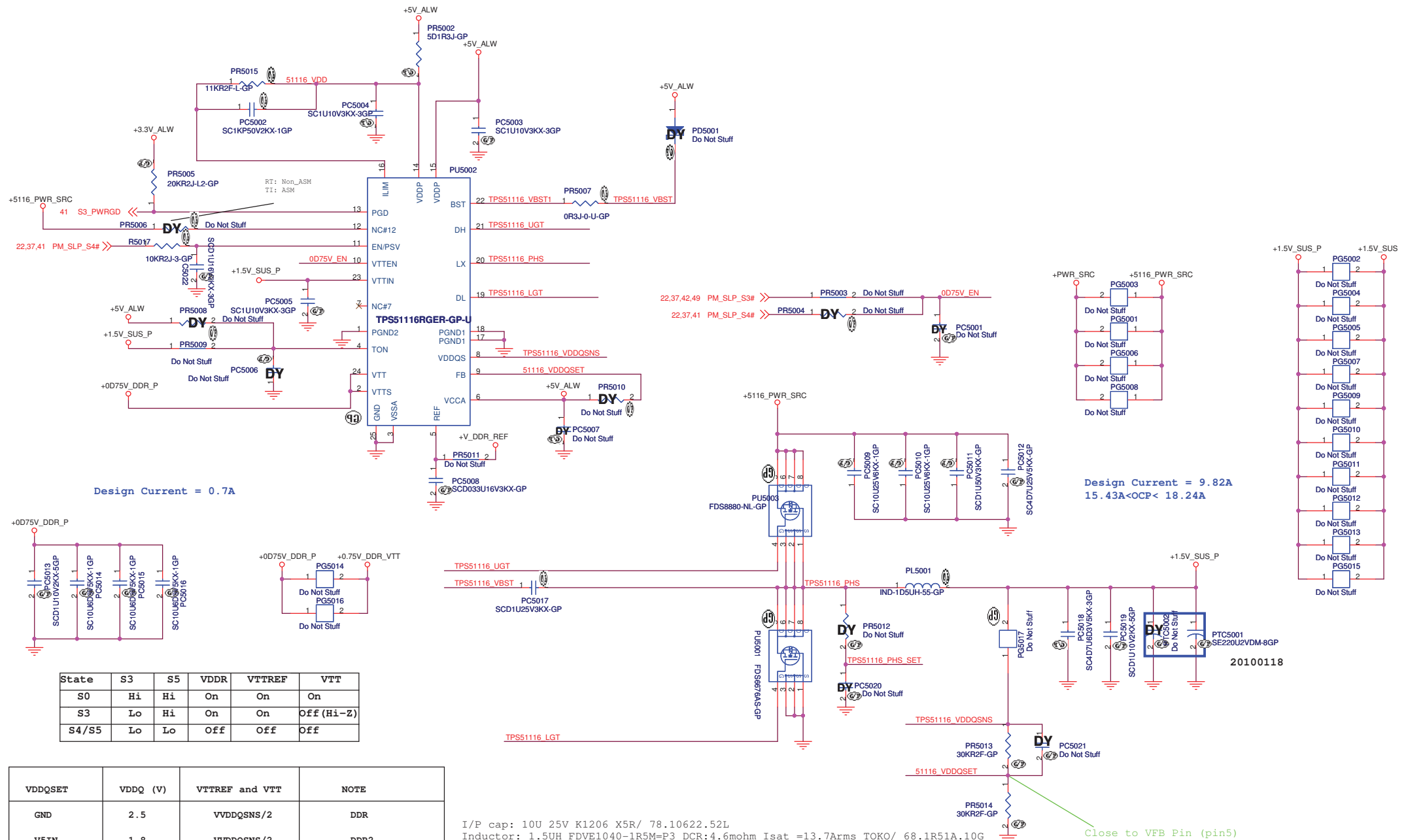


I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1uH FDUE1040D-1R0M=P3 TOKO DCR:2.35mohm Isat =17.9Arms 68.1R01B.10A
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP-T1-E3/11mohm/ 14mOhm@4.5Vgs/ 84.07686.037
L/S: SIR460DP-T1-GE3-GP/4.5mOhm/6.1mohm@4.5Vgs/ 84.00460.037

DJ1

DELL		Wistron Corporation	
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Title TPS51218 +1.05V_VCCP			
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```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



 <div style="margin-left: 20px;"> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C. </div>			
Title			
TPS51116 +1.5V SUS			
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Reserved

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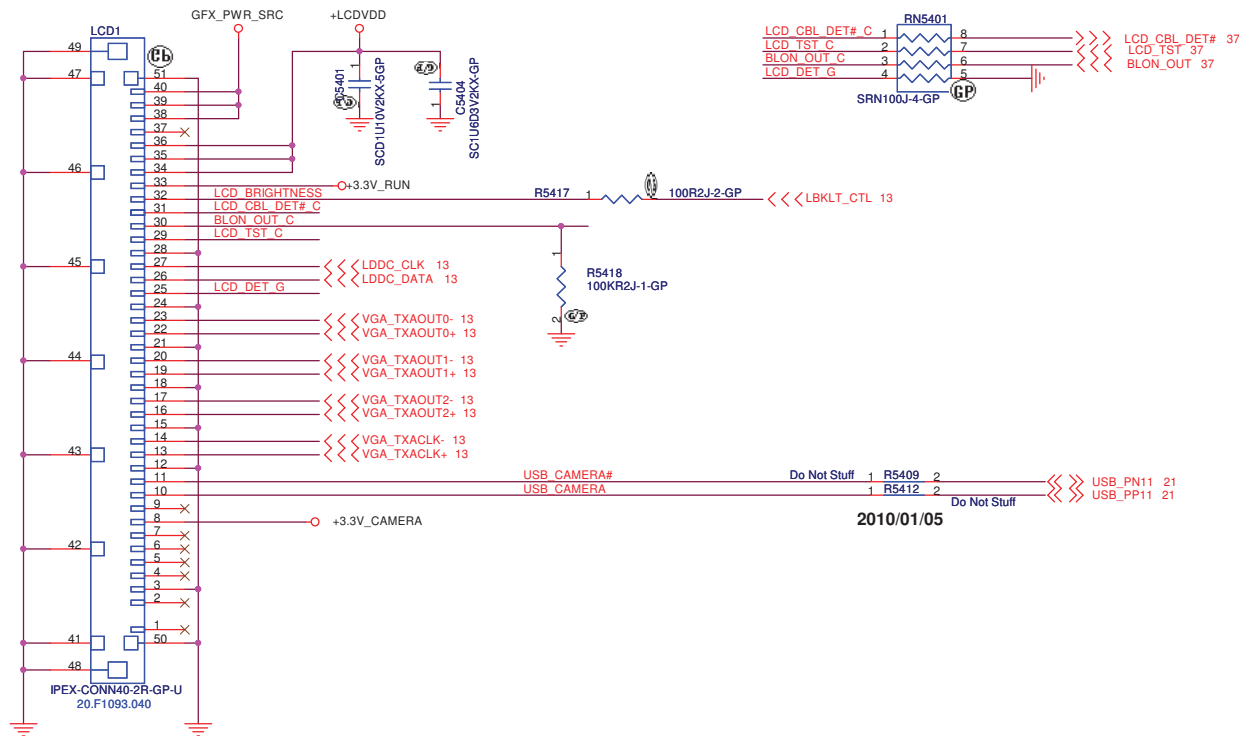
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DJ1 Montevina UMA

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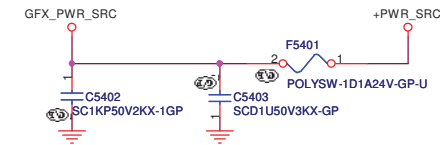
SSID = VIDEO

LVDS CONNECTOR



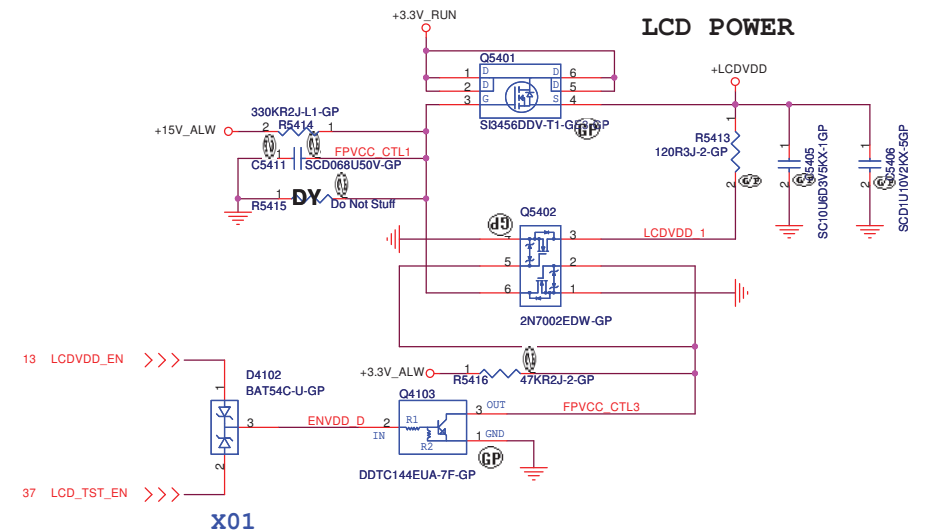
SSID = Inverter

INVERTER POWER

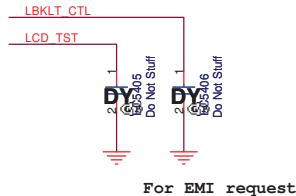
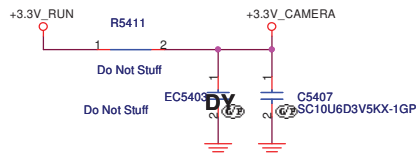


SSID = VIDEO

LCD POWER



Camera Power

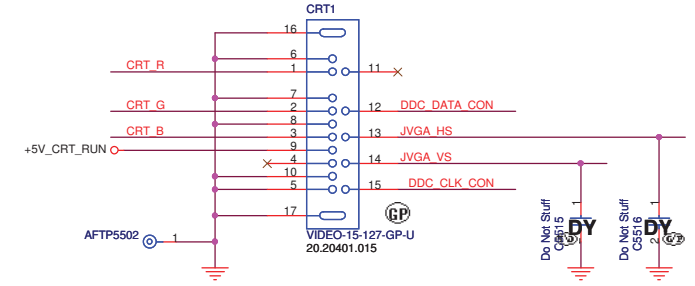
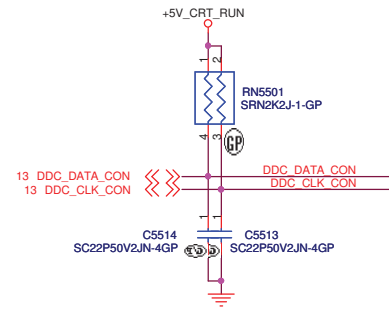
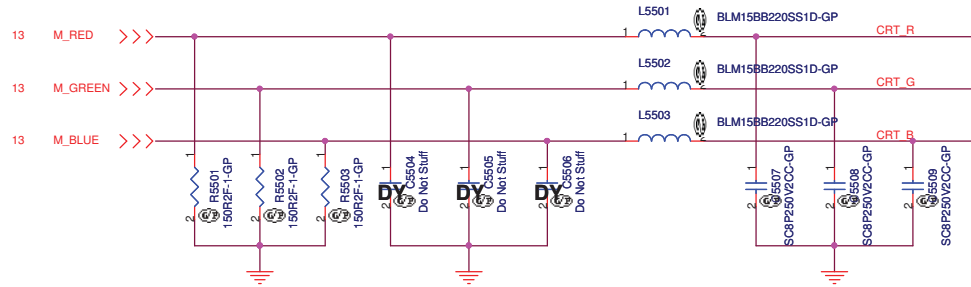


DJ1

SSID = VIDEO

Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

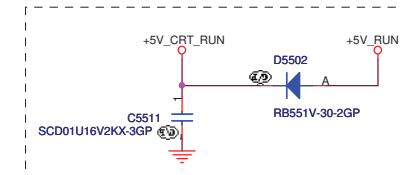
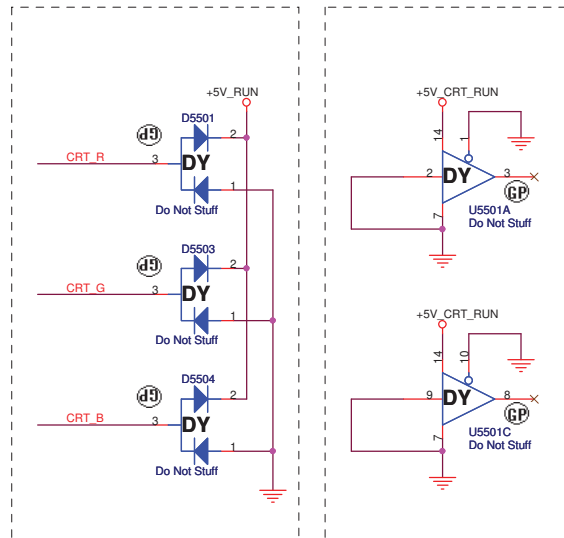
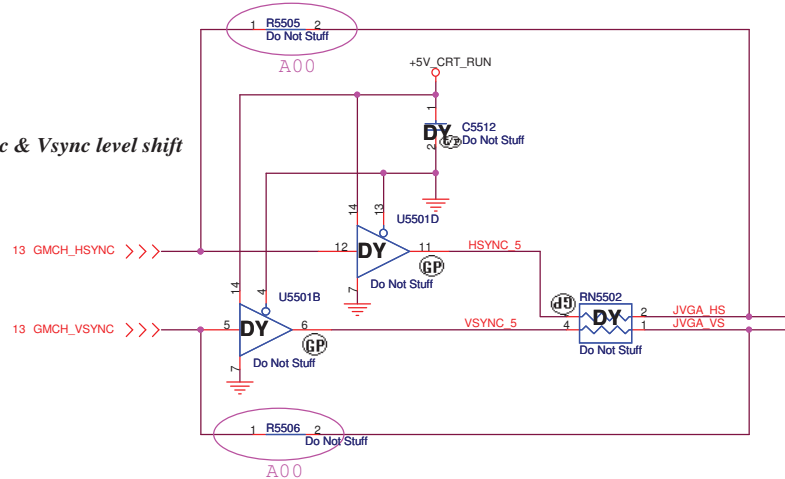


AFTP5501	1	+5V_CRT_RUN
AFTP5508	1	DDC_DATA_CON
AFTP5503	1	DDC_CLK_CON
AFTP5506	1	CRT_R
AFTP5507	1	CRT_G
AFTP5504	1	CRT_B

TP5505	1	JVGA_HS
TP5509	1	JVGA_VS

2010/01/15

Hsync & Vsync level shift




DJ1

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CRT Connector					
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Title

HDMI

Size
A3

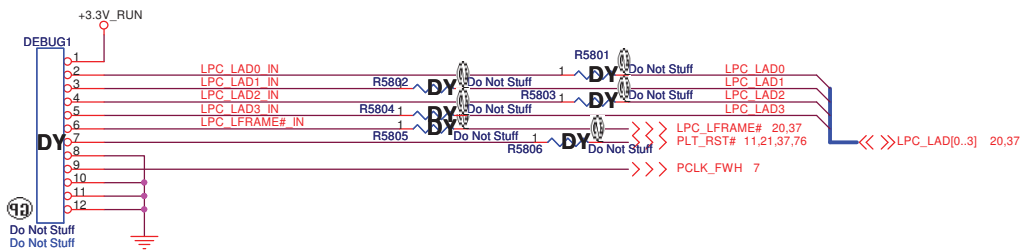
Document Number
DJ1 Montevina UMA

Rev
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Date: Wednesday, February 24, 2010

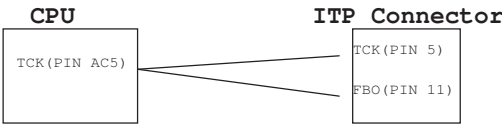
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SSID = User.Interface



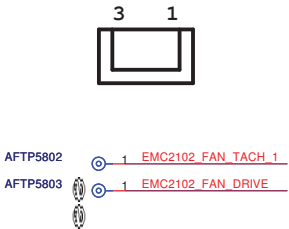
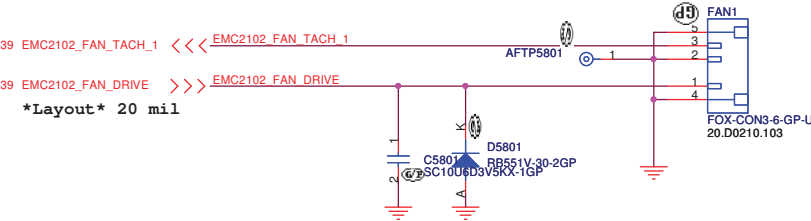
ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



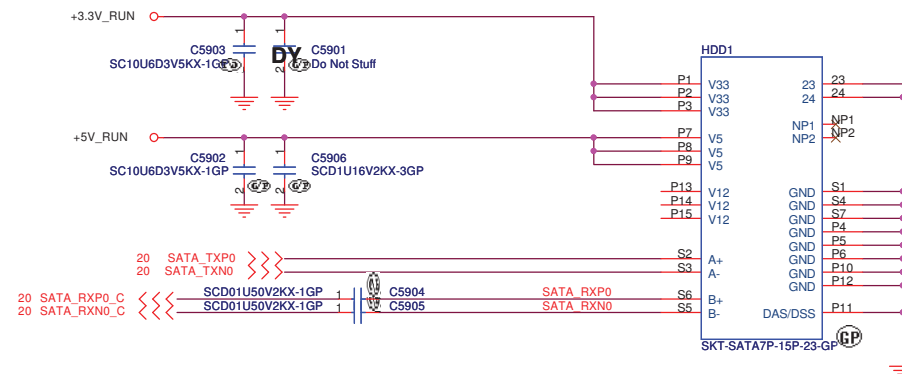
SSID = Thermal

Fan Connector

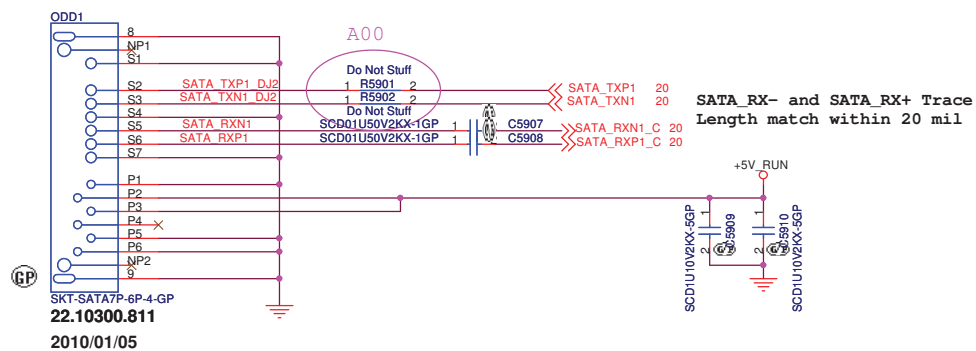


SSID = SATA

SATA HDD Connector



ODD Connector



DJ1

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Title

HDD/ODD

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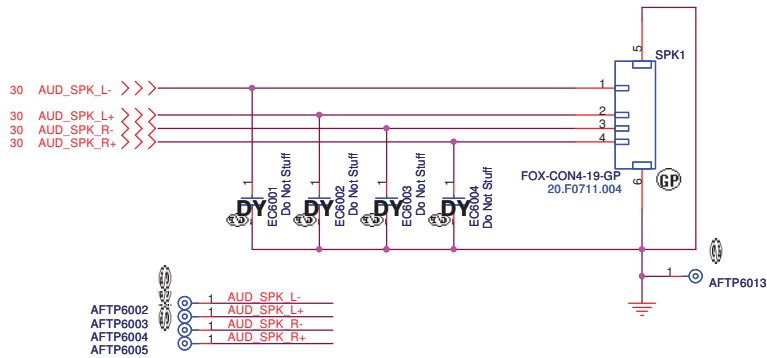
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Date: Friday, February 26, 2010

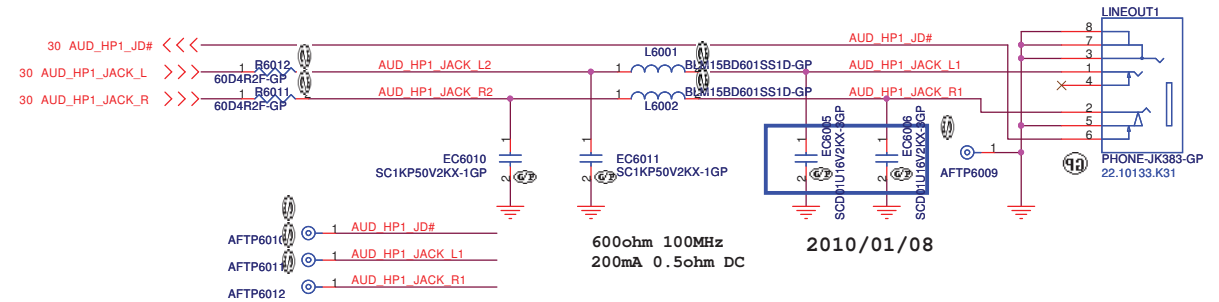
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SSID = AUDIO

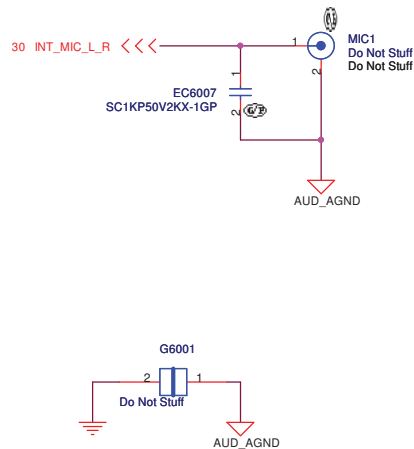
Speaker Connector



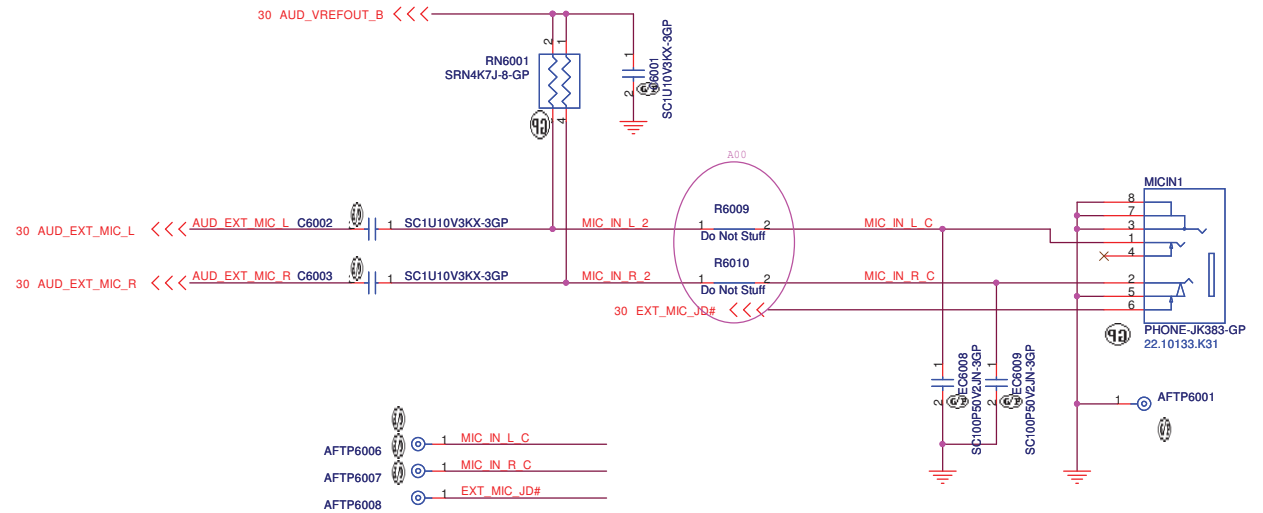
LINE OUT



Internal Microphone




MIC IN



DJ1

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DJ1



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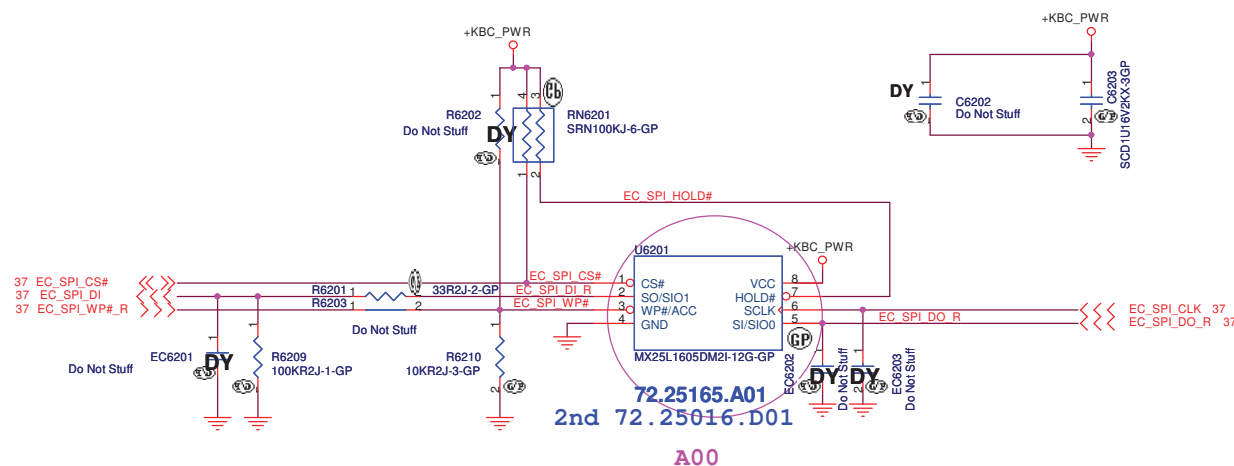
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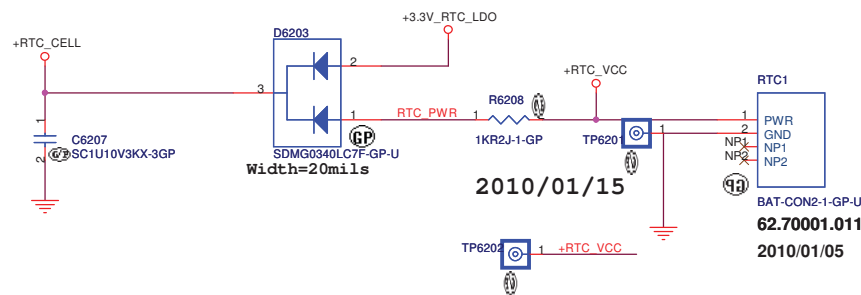
SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



SSID = RBATT

RTC Connector



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Title

Flash/RTC

Size
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Document Number

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Rev

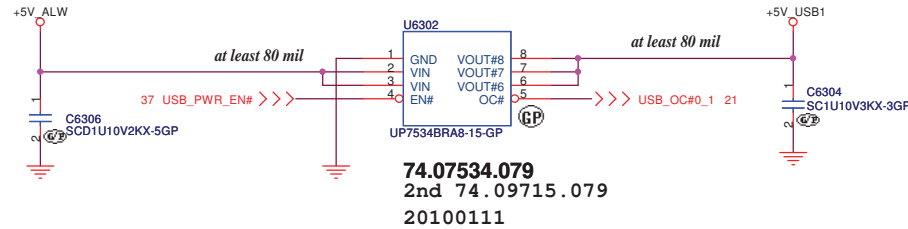
A00

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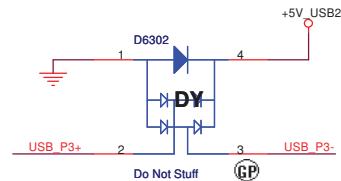
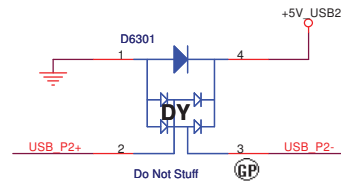
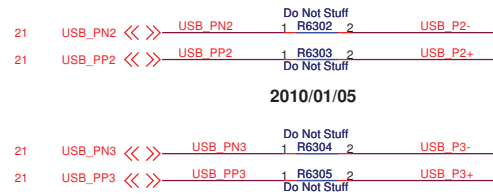
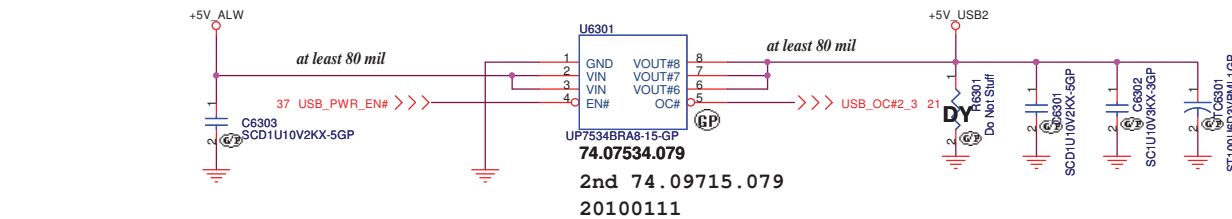
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SSID = USB

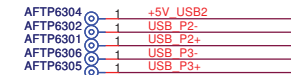
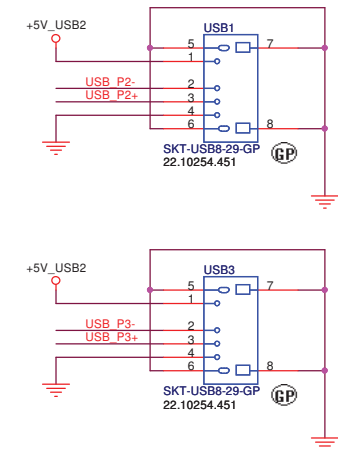
IO Board USB Power



Right USB Power




USB Socket



DJ1

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DJ1



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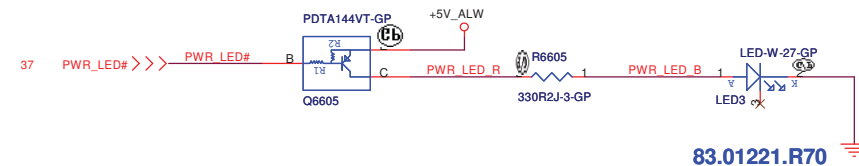
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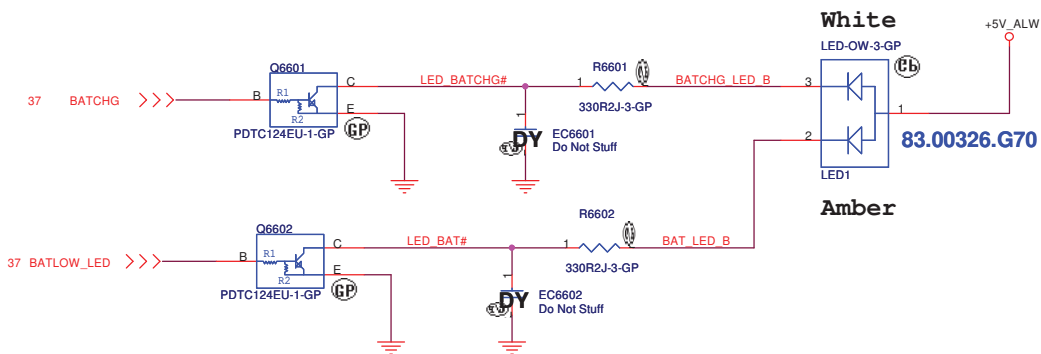
SSID = LED

Power button LED

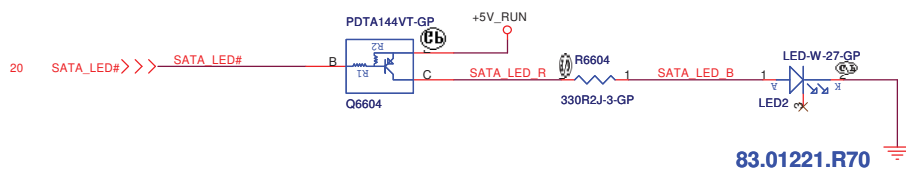
Power LED



Battery LED



HDD LED



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DELL Wistron Corporation
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Title

LED

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DJ1 Montevina UMA

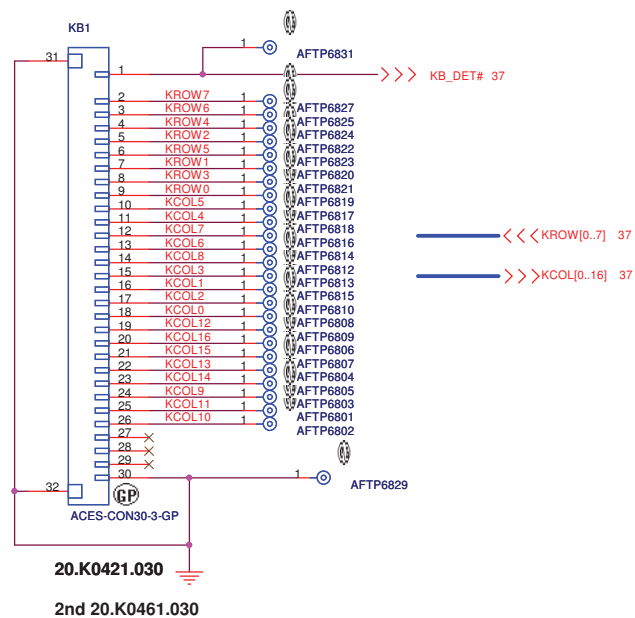
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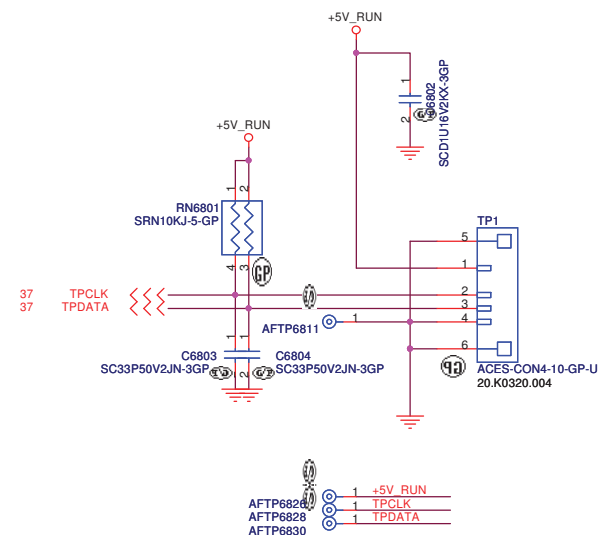
SSID = KBC

Internal KeyBoard Connector



SSID = Touch.Pad

TouchPad Connector



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Title

Key Board/Touch Pad

Size

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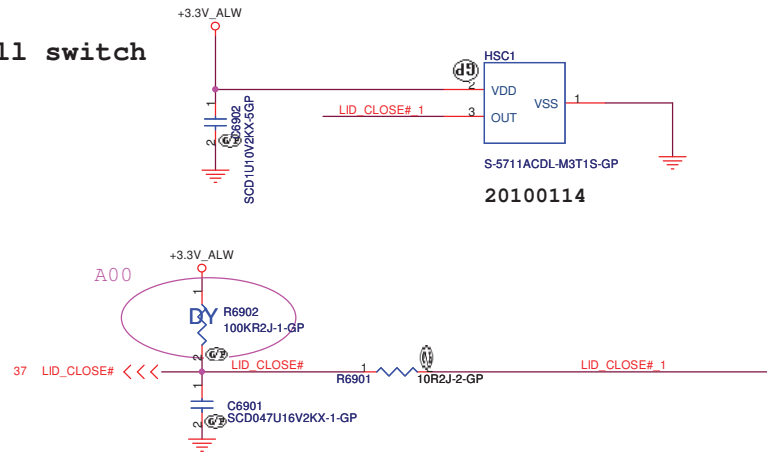
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Hall switch



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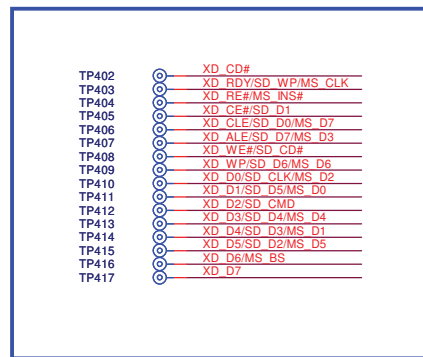
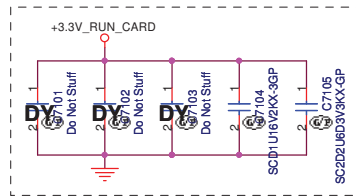
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SSID = SDIO

SD/XD/MS Card Reader



2010/01/15

2010/01/15



32 XD_D0/SD_CLK/MS_D2
32 XD_D1/SD_D5/MS_D0
32 XD_D2/SD_CMD
32 XD_D3/SD_D4/MS_D4
32 XD_D4/SD_D3/MS_D1
32 XD_D5/SD_D2/MS_D5
32 XD_D6/MS_BS
32 XD_D7
32 XD_RDY#/SD_WP/MS_CLK
32 XD_RE#/MS_INS#
32 XD_CE#/SD_D1
32 XD_CLE#/SD_D0/MS_D7
32 XD_ALE#/SD_D7/MS_D3
32 XD_WE#/SD_CD#
32 XD_WP/SD_D6/MS_D6
32 XD_CD#

+3.3V_RUN_CARD

CARD1

SD_VCC
MS_VCC
XD_VCC

8 XD_D0
9 XD_D1
26 XD_D2
27 XD_D3
28 XD_D4
30 XD_D5
31 XD_D6
32 XD_D7
1 XD_R/B
2 XD_RE
3 XD_CE
4 XD_CLE
5 XD_ALE
6 XD_WE
7 XD_WP
34 XD_CD_SW

NP1
NP2

CARDBUS36P-1-GP

20.I0109.001

SD_DAT0
SD_DAT1
SD_DAT2
SD_DAT3

SD_CMD
SD_CLK
SD_CD_SW
SD_WP_SW

MS_DATA0
MS_DATA1
MS_DATA2
MS_DATA3

MS_BS
MS_INS
MS_SCLK

4IN1_GND
4IN1_GND
4IN1_GND
4IN1_GND

>>> XD_CLE/SD_D0/MS_D7 32
>>> XD_CE#/SD_D1 32
>>> XD_D5/SD_D2/MS_D5 32
>>> XD_D4/SD_D3/MS_D1 32
>>> XD_D2/SD_CMD 32
>>> XD_D0/SD_CLK/MS_D2 32
>>> XD_WE#/SD_CD# 32
>>> XD_RDY#/SD_WP/MS_CLK 32
>>> XD_D1/SD_D5/MS_D0 32
>>> XD_D4/SD_D3/MS_D1 32
>>> XD_D0/SD_CLK/MS_D2 32
>>> XD_ALE/SD_D7/MS_D3 32
>>> XD_D6/MS_BS 32
>>> XD_RE#/MS_INS# 32
>>> XD_RDY#/SD_WP/MS_CLK 32




2010/01/15

DJ1

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Title

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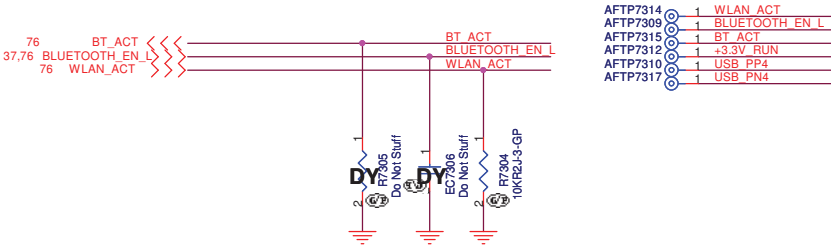
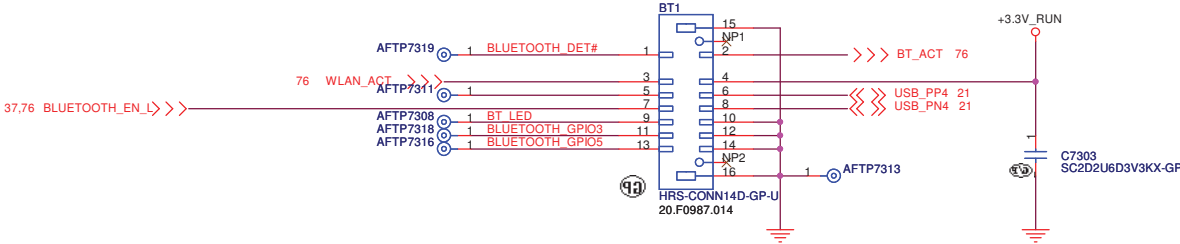
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SSID = User.Interface



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Title

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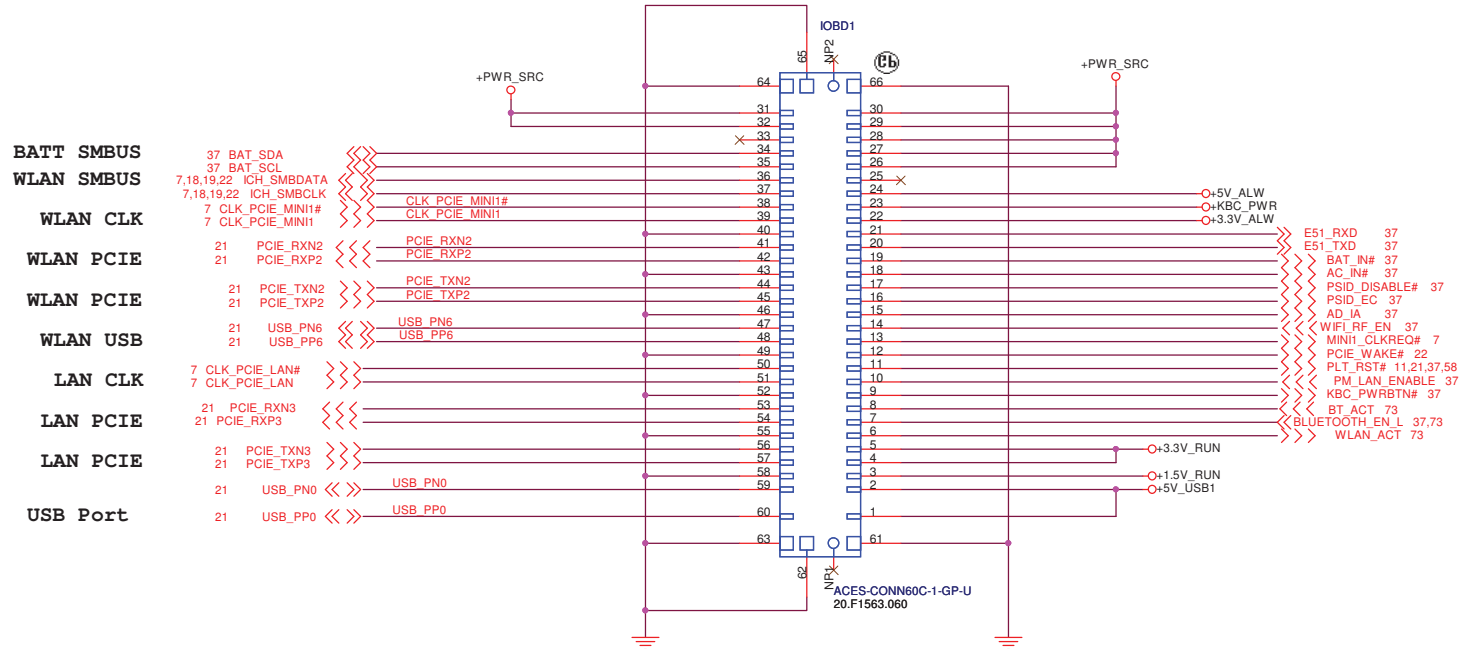
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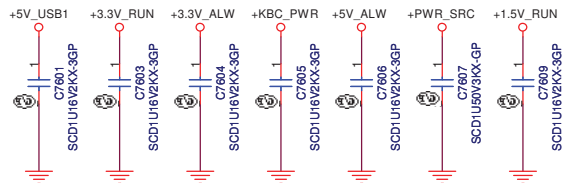
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SSID = PWR.Support



Close to IOBD Conn




DJ1

DELL		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: IO Board Connector			
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Title

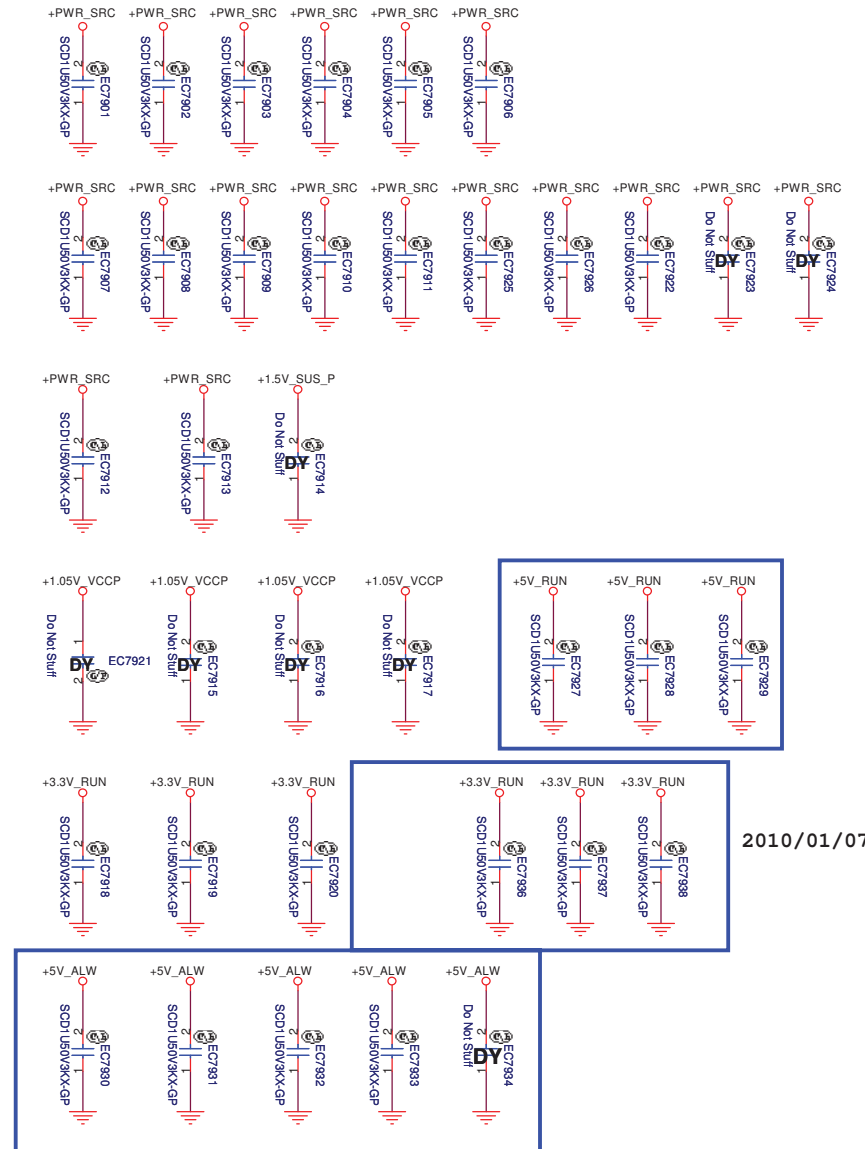
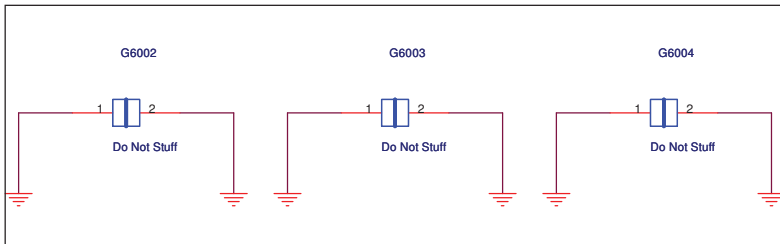
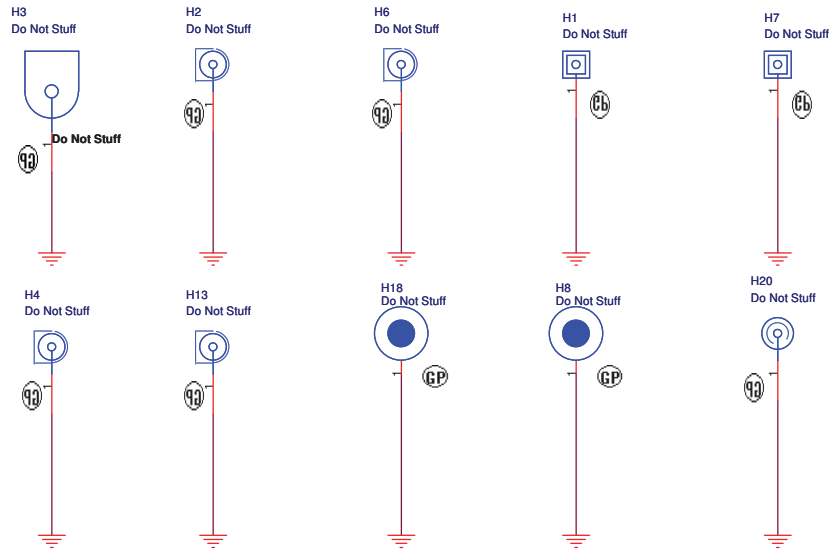
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EMI Request

2010/01/07

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Custom

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	20	2010/01/04	Wistron	R2018.R2019 to J accuracy	Change R2018 R2019 to 63.33434.1DL	X01
2	54	2010/01/04	Wistron	D4102 Change	D4102 change to 83.00054.Q81	X01
3	37	2010/01/04	Wistron	MB version chang to X01	Change R3722 pop,R3727 dummy.	X01
4	59	2009/01/06	Wistron	ME change ODD&RTC Conn	Change ODD Conn to 22.10300.811 Change RTC Conn to 62.70001.011	X01
5	79	2009/01/07	Wistron	EMI Request	Add EC7927 EC7928 EC7929 EC7936 EC7937 EC7938 EC7930 EC7931 EC7932 EC7933 EC7934 POP EC7913 EC7912 EC7925 EC7922 EC7926 PC4610 PC4615	X01
6	54 32 63	2010/01/07	Wistron	USB layout change	Del TR5401 TR3201 TR6301 TR6302 Change R5409 R5412 R3211 R3210 R6302 R6303 R6304 R6305 to 0ohm	X01
7	42	2010/01/07	Wistron	Change R4210 for POP noise	Change R4210 to 10K 63.10334.1DL	X01
8	60	2010/01/08	IDT	IDT Request change EMI CAP to 0.01u	EC6005 EC6006 change to 0.01u 78.10321.2FL	X01
9	63	2010/01/11	Wistron	USB power switch change	Change U6301 U6302 to 74.07534.079	X01
10	37	2010/01/12	Wistron	Prevent BIOS damage	POP U3702 74.00690.I7B	X01
11	37	2010/01/12	DELL	Add one capacitor for IPCC function	Add C3721 close KBC Pin AD_IA	X01
12	69	2010/01/14	Wistron	SMT issue	Change HSC1 layout symbol to Seiko 74.05711.07B	X01
13	47 49 50	2010/01/16	Wistron	Power team request	change PC4740 PC4741 PC4910 PC5020to 78.33124.2FL	X01
14	46	2010/01/18	Wistron	Power team request	DY PTC4603.change PTC5001 PTC4602	X01
15	37	2010/02/10	Wistron	U3702 reset timing is too long	DY U3702	A00
16	37	2010/02/10	Wistron	Change PCB version from X01 to A00	DY R3722 and R3728, stuff R3727 and R3723	A00
17	20 37 55	2010/02/24	Wistron	Change 0ohm to short pad.	Change R2014 R3725 R3748 R5505 R5506 R3012 R3014 R3018 RN5901 R6009 R6010	A00
18	37	2010/02/24	DELL	Add one FET for RCID function	Reserve Q3706	A00
19	69	2010/02/25	Wistron	Do not stuff R6902	Reserve R6902	A00



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Title

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