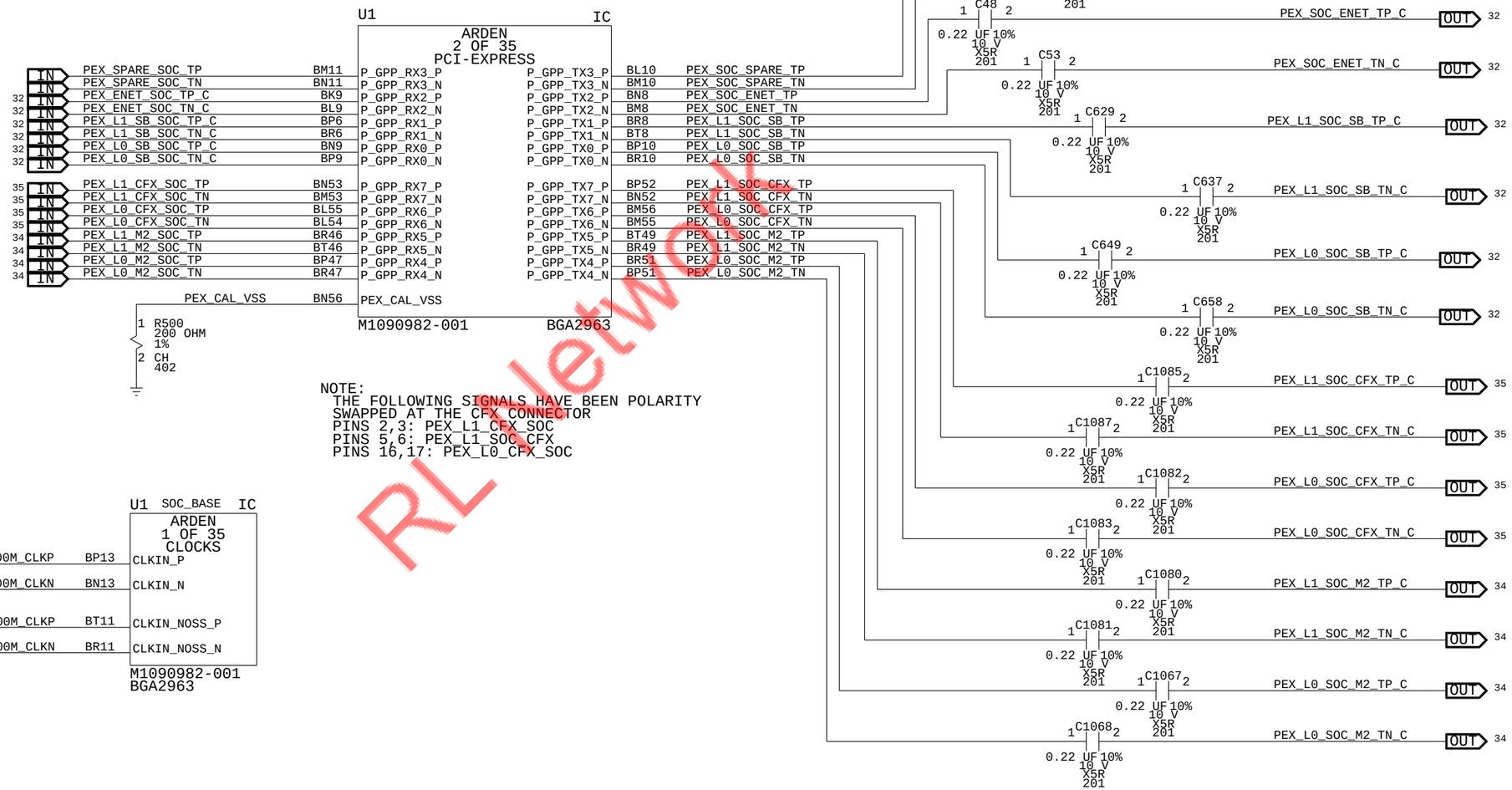
Toledo SoC
FAB E Retail
REV 1.03

RULES: (APPLIED WHEN POSSIBLE)
1. MSB TO LSB IS TOP TO BOTTOM
2. WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT
3. ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING
4. AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS
5. LANED SIGNALS ARE GROUPED ON SYMBOLS
6. TRANSMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS
7. SUFFIX _V IS USED FOR VOLTAGE RAIL SIGNAL NAMES
8. SUFFIX _DP AND _DN ARE USED FOR DIFFERIENTAL PAIRS
9. UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE
10. SUFFIX _N FOR ACTIVE LOW OR N JUNCTION
12. SUFFIX _P FOR P JUNCTION
13. SUFFIX _EN FOR ENABLE
14. 'CLK' FOR CLOCKS, 'RST' FOR RESETS
15. PWRGD FOR POWER GOOD
16. REV AND FAB ARE SET USING CUSTOM VARIABLES
    TOOLS>OPTIONS>VARIABLES

DRAWING
Mon Nov 05 16:42:32 2018

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	1/59	1/59	E Retail	1.03

SOC: PCIEX, CLOCKS

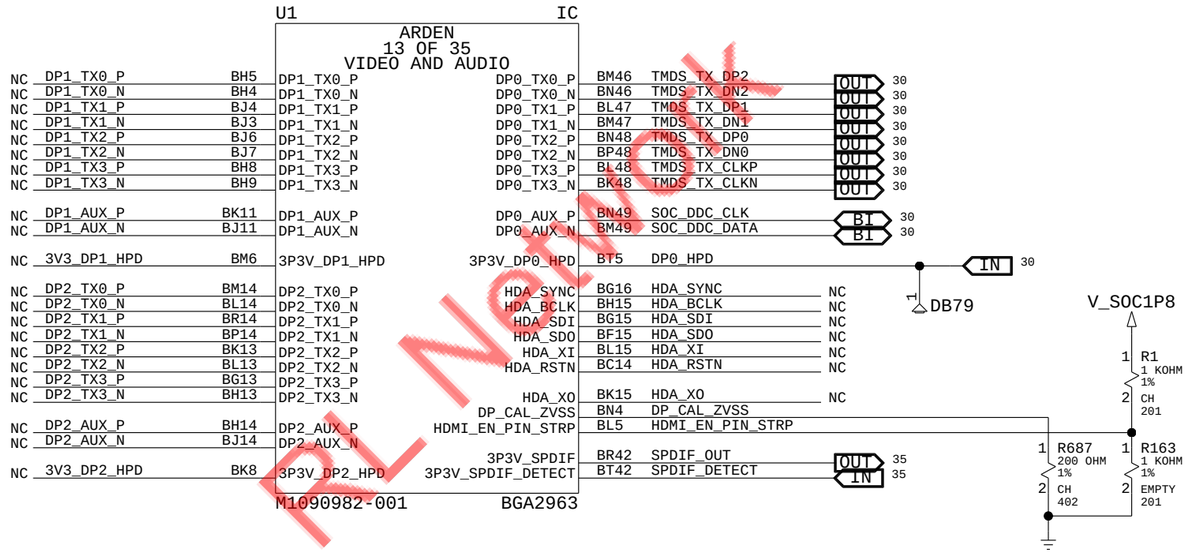


NOTE:
THE FOLLOWING SIGNALS HAVE BEEN POLARITY SWAPPED AT THE CFX CONNECTOR
PINS 2,3: PEX_L1_CFX_SOC
PINS 5,6: PEX_L1_SOC_CFX
PINS 16,17: PEX_L0_CFX_SOC

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1090982-001	IC	U1	PROCSR, SOC, SM, 1100 BGA, ARDEN A0	SOC_INCLUDE
M1090982-001	EMPTY	U1	PROCSR, SOC, SM, 1100 BGA, ARDEN A0	SOC_EMPTY

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	2/59	2/59	E Retail	1.03

SOC: AUDIO, VIDEO



HDMI TO DP SIGNAL MAPPING

DVI PCB ROUTING ORDERING	DP PCB ROUTING ORDERING	PIN NAME
TMDS CLOCK -	DP LANE 3 -	DP0_TX3_N
TMDS CLOCK +	DP LANE 3 +	DP0_TX3_P
TMDS DATA0 -	DP LANE 2 -	DP0_TX2_N
TMDS DATA0 +	DP LANE 2 +	DP0_TX2_P
TMDS DATA1 -	DP LANE 1 -	DP0_TX1_N
TMDS DATA1 +	DP LANE 1 +	DP0_TX1_P
TMDS DATA2 -	DP LANE 0 -	DP0_TX0_N
TMDS DATA2 +	DP LANE 0 +	DP0_TX0_P

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	3/59	3/59	E Retail	1.03

SOC: POWER: MEMIO,MEMPHY,SOC,MISC

POPULATE R268 IF FILTER IS USED

VR SENSE NET

R268 0 OHM 5% 201 EMPTY

VREG_SOC1P8_SNS → OUT 50

R272 0 OHM 5% CH 201

V_3P3_GATED

C972, C980, C977: 1 UF 20% 6.3 V X5R 201

V_SOCPHY

C107, C108, C111, C112, C113, C114: 1 UF 20% 6.3 V X5R 201

V_SOC1P8

C712: 22 UF 20% 6.3 V EMPTY 603

ST11 SHORT

FB714: 8.5 OHM 8 A EMPTY 603 0.004 MOHM

FB713: 80 OHM 5 A EMPTY 805 0.01 OHM

V_SOC1P8_VDD

C715, C717: 22 UF 20% 6.3 V EMPTY 603

C987: 22 UF 20% 6.3 V X5R 603

C101, C990, C983, C32: 1 UF 20% 6.3 V X5R 201

FB714, FB713 ARE FILTER STUFFING OPTIONS
IN CASE VDD18/SOC1P8 IS SENSITIVE TO RIPPLE VOLTAGE
THIS IS NOT EXPECTED TO BE NEEDED AS AMD HAS SINCE
PROVIDED A RIPPLE VOLTAGE REQUIREMENT OF <30MV PK-PK

U1 IC — ARDEN 24 OF 35 VDD_MISC — M1090982-001 BGA2963

BN2	VDD_33_BN2
BM1	VDD_33_BM1
BT4	VDD_18_BT4
BT2	VDD_18_BT2
BR1	VDD_18_BR1
BR2	VDD_18_BR2
BT53	VDD_C_EFUSE
VDD_C_BT55	BT55
VDD_C_BR55	BR55
VDD_C_BR56	BR56
VDD_RTC	BR4

V_BAT

C645: 1 UF 20% 6.3 V X5R 201

V_FUSE

C604: 1 UF 20% 6.3 V X5R 201

U1 IC — ARDEN 23 OF 35 VDD_MEMP — M1090982-001 BGA2963

V_MEMPHY

AA13	VDD_MEMP_AA13		
AA43	VDD_MEMP_AA43	VDD_MEMP_N15	N15
AB14	VDD_MEMP_AB14	VDD_MEMP_N16	N16
AB44	VDD_MEMP_AB44	VDD_MEMP_N18	N18
AC13	VDD_MEMP_AC13	VDD_MEMP_N20	N20
AC43	VDD_MEMP_AC43	VDD_MEMP_N22	N22
AD14	VDD_MEMP_AD14	VDD_MEMP_N24	N24
AD44	VDD_MEMP_AD44	VDD_MEMP_N26	N26
AE13	VDD_MEMP_AE13	VDD_MEMP_N28	N28
AE43	VDD_MEMP_AE43	VDD_MEMP_N30	N30
AF14	VDD_MEMP_AF14	VDD_MEMP_N32	N32
AF44	VDD_MEMP_AF44	VDD_MEMP_N34	N34
AG13	VDD_MEMP_AG13	VDD_MEMP_N36	N36
AG43	VDD_MEMP_AG43	VDD_MEMP_N38	N38
AH14	VDD_MEMP_AH14	VDD_MEMP_N40	N40
AH44	VDD_MEMP_AH44	VDD_MEMP_N41	N41
AJ13	VDD_MEMP_AJ13	VDD_MEMP_P14	P14
AJ43	VDD_MEMP_AJ43	VDD_MEMP_P15	P15
AK14	VDD_MEMP_AK14	VDD_MEMP_P17	P17
AK44	VDD_MEMP_AK44	VDD_MEMP_P19	P19
AL13	VDD_MEMP_AL13	VDD_MEMP_P21	P21
AL43	VDD_MEMP_AL43	VDD_MEMP_P23	P23
AM14	VDD_MEMP_AM14	VDD_MEMP_P25	P25
AM44	VDD_MEMP_AM44	VDD_MEMP_P27	P27
AN13	VDD_MEMP_AN13	VDD_MEMP_P29	P29
AN43	VDD_MEMP_AN43	VDD_MEMP_P31	P31
AP14	VDD_MEMP_AP14	VDD_MEMP_P33	P33
AP44	VDD_MEMP_AP44	VDD_MEMP_P35	P35
AR13	VDD_MEMP_AR13	VDD_MEMP_P37	P37
AR43	VDD_MEMP_AR43	VDD_MEMP_P39	P39
AT14	VDD_MEMP_AT14	VDD_MEMP_P42	P42
AT44	VDD_MEMP_AT44	VDD_MEMP_R13	R13
AU13	VDD_MEMP_AU13	VDD_MEMP_R42	R42
AU43	VDD_MEMP_AU43	VDD_MEMP_R43	R43
AV14	VDD_MEMP_AV14	VDD_MEMP_T14	T14
AV44	VDD_MEMP_AV44	VDD_MEMP_T44	T44
AW13	VDD_MEMP_AW13	VDD_MEMP_U13	U13
AW43	VDD_MEMP_AW43	VDD_MEMP_U43	U43
AY14	VDD_MEMP_AY14	VDD_MEMP_V14	V14
AY44	VDD_MEMP_AY44	VDD_MEMP_V44	V44
BA13	VDD_MEMP_BA13	VDD_MEMP_W13	W13
BA43	VDD_MEMP_BA43	VDD_MEMP_W43	W43
BB14	VDD_MEMP_BB14	VDD_MEMP_Y14	Y14
BB44	VDD_MEMP_BB44	VDD_MEMP_Y44	Y44

V_MEMPHY

U1 IC — ARDEN 16 OF 35 VDD_SOC — M1090982-001 BGA2963

V_SOC

W15	VDD_SOC_W15	VDD_SOC_U28	U28
W16	VDD_SOC_W16	VDD_SOC_U31	U31
W19	VDD_SOC_W19	VDD_SOC_U32	U32
W20	VDD_SOC_W20	VDD_SOC_U35	U35
W23	VDD_SOC_W23	VDD_SOC_U36	U36
W24	VDD_SOC_W24	VDD_SOC_U39	U39
W27	VDD_SOC_W27	VDD_SOC_U40	U40
W28	VDD_SOC_W28	VDD_SOC_T15	T15
W31	VDD_SOC_W31	VDD_SOC_T17	T17
W32	VDD_SOC_W32	VDD_SOC_T18	T18
W35	VDD_SOC_W35	VDD_SOC_T21	T21
W36	VDD_SOC_W36	VDD_SOC_T22	T22
W39	VDD_SOC_W39	VDD_SOC_T25	T25
W40	VDD_SOC_W40	VDD_SOC_T26	T26
V17	VDD_SOC_V17	VDD_SOC_T29	T29
V18	VDD_SOC_V18	VDD_SOC_T30	T30
V21	VDD_SOC_V21	VDD_SOC_T33	T33
V22	VDD_SOC_V22	VDD_SOC_T34	T34
V25	VDD_SOC_V25	VDD_SOC_T37	T37
V26	VDD_SOC_V26	VDD_SOC_T38	T38
V29	VDD_SOC_V29	VDD_SOC_T41	T41
V30	VDD_SOC_V30	VDD_SOC_T42	T42
V33	VDD_SOC_V33	VDD_SOC_R15	R15
V34	VDD_SOC_V34	VDD_SOC_R19	R19
V37	VDD_SOC_V37	VDD_SOC_R20	R20
V38	VDD_SOC_V38	VDD_SOC_R23	R23
V41	VDD_SOC_V41	VDD_SOC_R24	R24
V42	VDD_SOC_V42	VDD_SOC_R27	R27
U15	VDD_SOC_U15	VDD_SOC_R28	R28
U16	VDD_SOC_U16	VDD_SOC_R31	R31
U19	VDD_SOC_U19	VDD_SOC_R32	R32
U20	VDD_SOC_U20	VDD_SOC_R35	R35
U23	VDD_SOC_U23	VDD_SOC_R36	R36
U24	VDD_SOC_U24	VDD_SOC_R39	R39
U27	VDD_SOC_U27	VDD_SOC_R40	R40

V_SOC

U1 IC — ARDEN 22 OF 35 VDD_MEM — M1090982-001 BGA2963

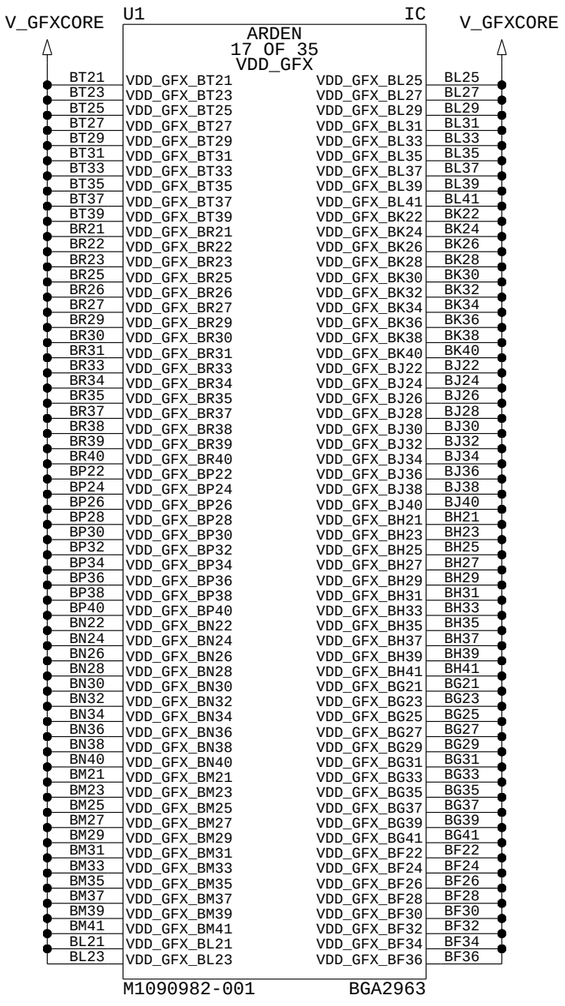
V_MEMIO

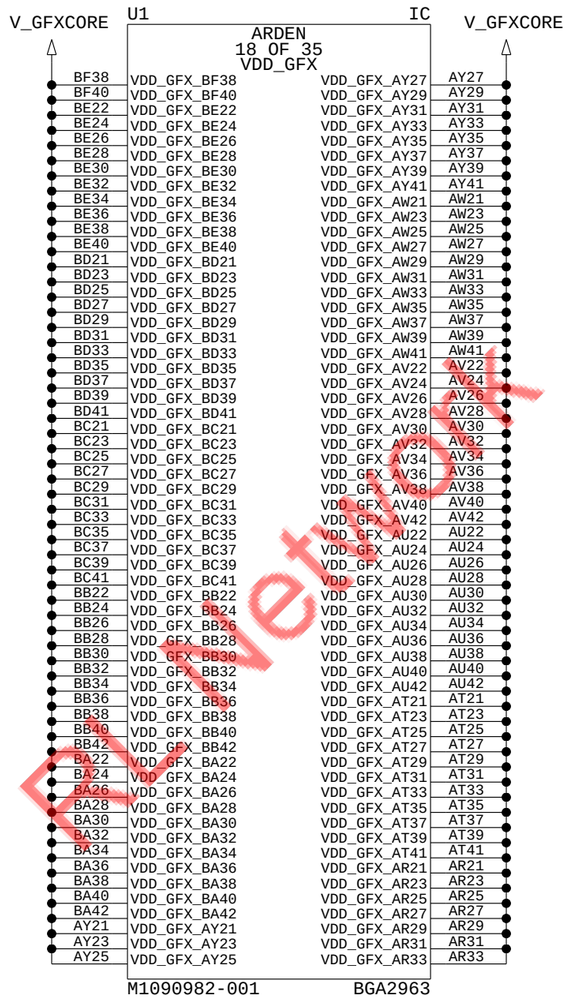
BF9	VDD_MEM_BF9	VDD_MEM_K9	K9
BF47	VDD_MEM_BF47	VDD_MEM_T10	T10
BD45	VDD_MEM_BD45	VDD_MEM_K41	K41
AY10	VDD_MEM_AY10	VDD_MEM_R47	R47
AV47	VDD_MEM_AV47	VDD_MEM_L10	L10
AW47	VDD_MEM_AW47	VDD_MEM_K16	K16
AA11	VDD_MEM_AA11	VDD_MEM_K22	K22
AP10	VDD_MEM_AP10	VDD_MEM_K28	K28
AG11	VDD_MEM_AG11	VDD_MEM_K34	K34
AN47	VDD_MEM_AN47	VDD_MEM_R11	R11
AH46	VDD_MEM_AH46	VDD_MEM_K47	K47
AH10	VDD_MEM_AH10	VDD_MEM_Y45	Y45
AM45	VDD_MEM_AM45	VDD_MEM_L15	L15
AG47	VDD_MEM_AG47	VDD_MEM_L21	L21
AB10	VDD_MEM_AB10	VDD_MEM_L27	L27
AN11	VDD_MEM_AN11	VDD_MEM_L33	L33
AW11	VDD_MEM_AW11	VDD_MEM_J39	J39
AA47	VDD_MEM_AA47	VDD_MEM_J46	J46
		VDD_MEM_P45	P45

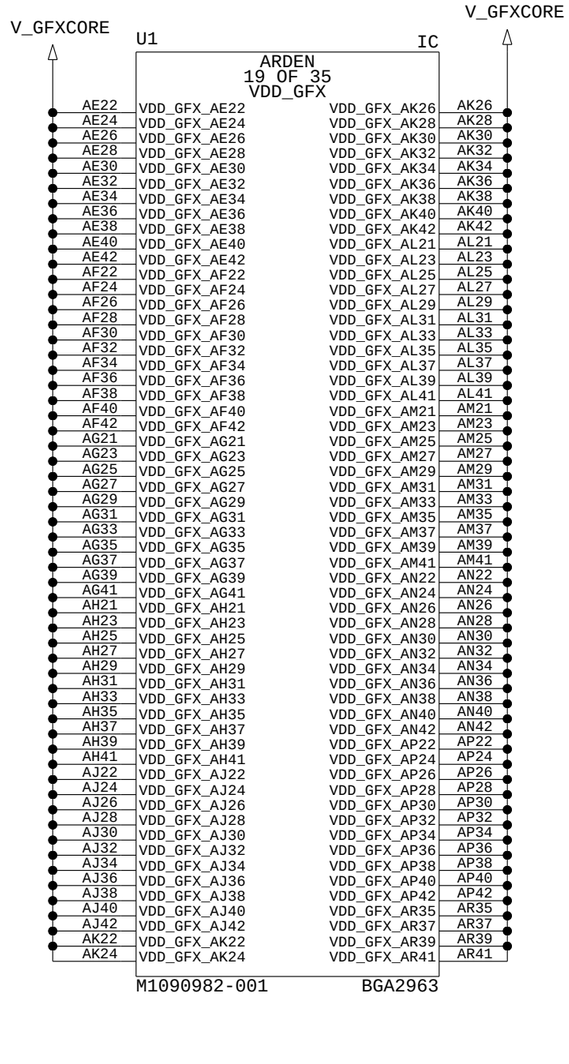
V_MEMIO

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	4/59	4/59	E Retail	1.03

SOC: POWER: GFXCORE

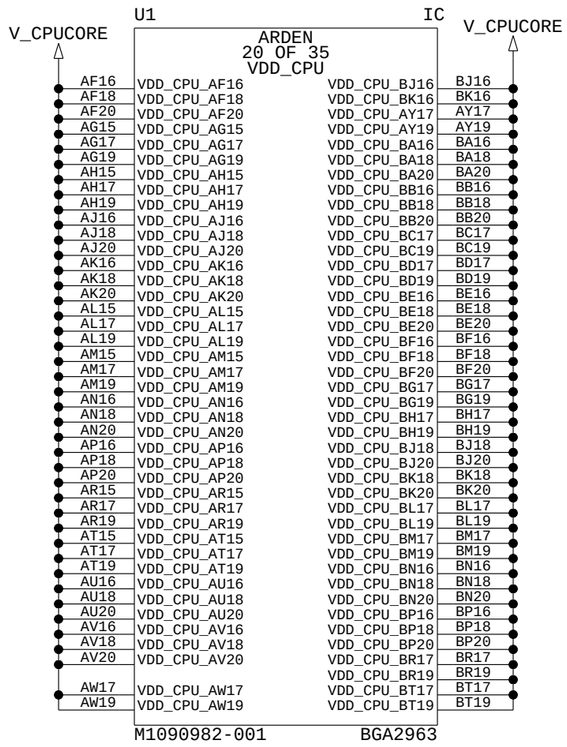


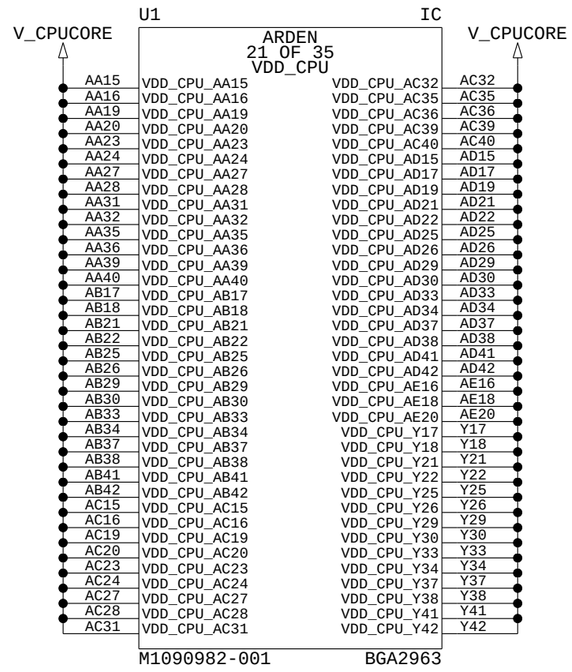




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	5/59	5/59	E Retail	1.03

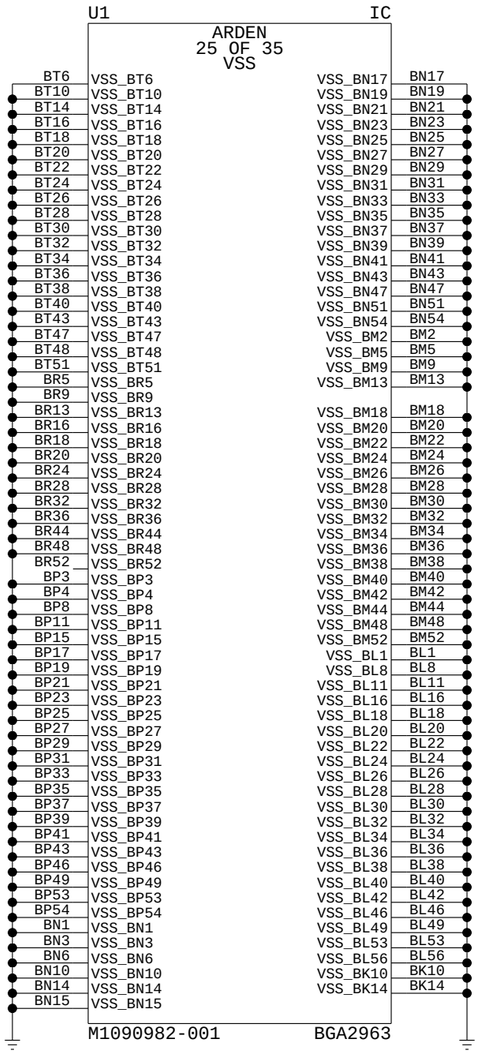
SOC: POWER: CPUCORE

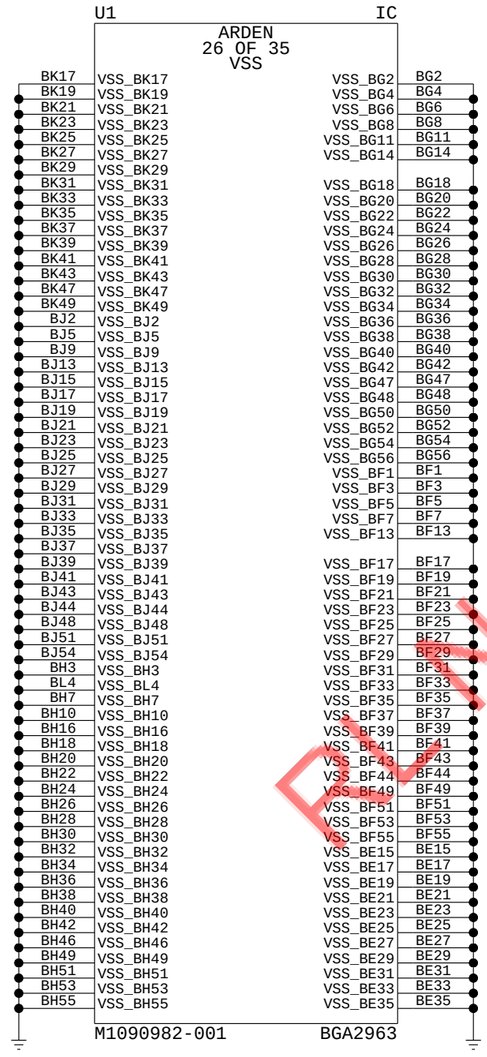


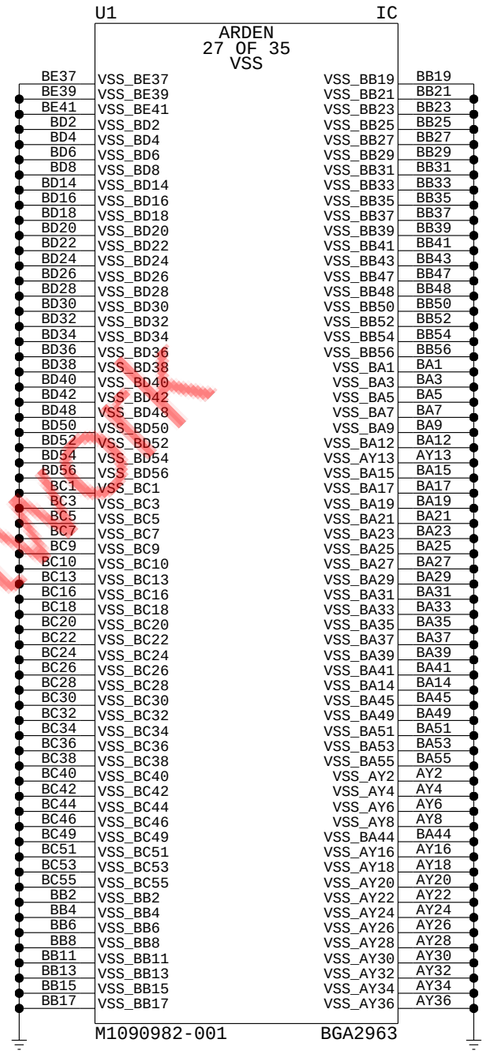


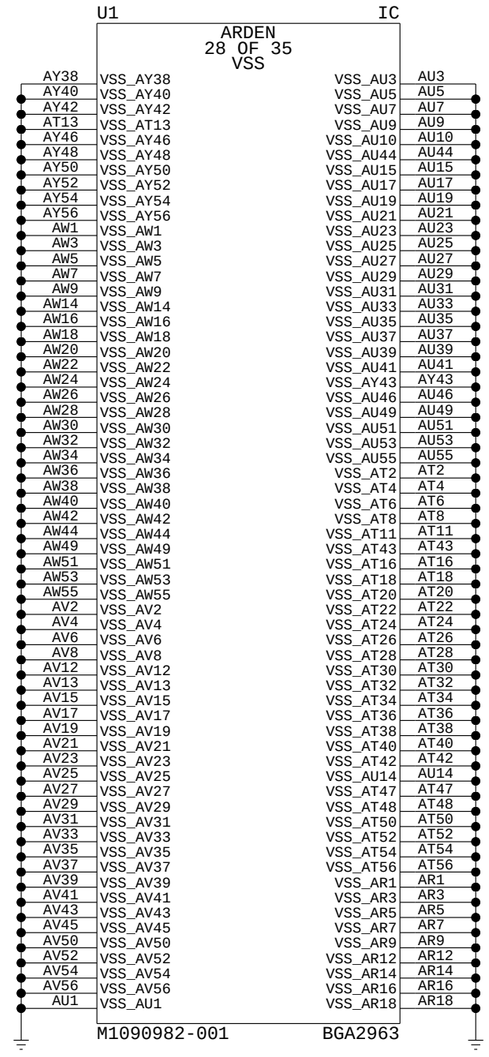
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	6/59	6/59	E Retail	1.03

SOC: POWER: VSS



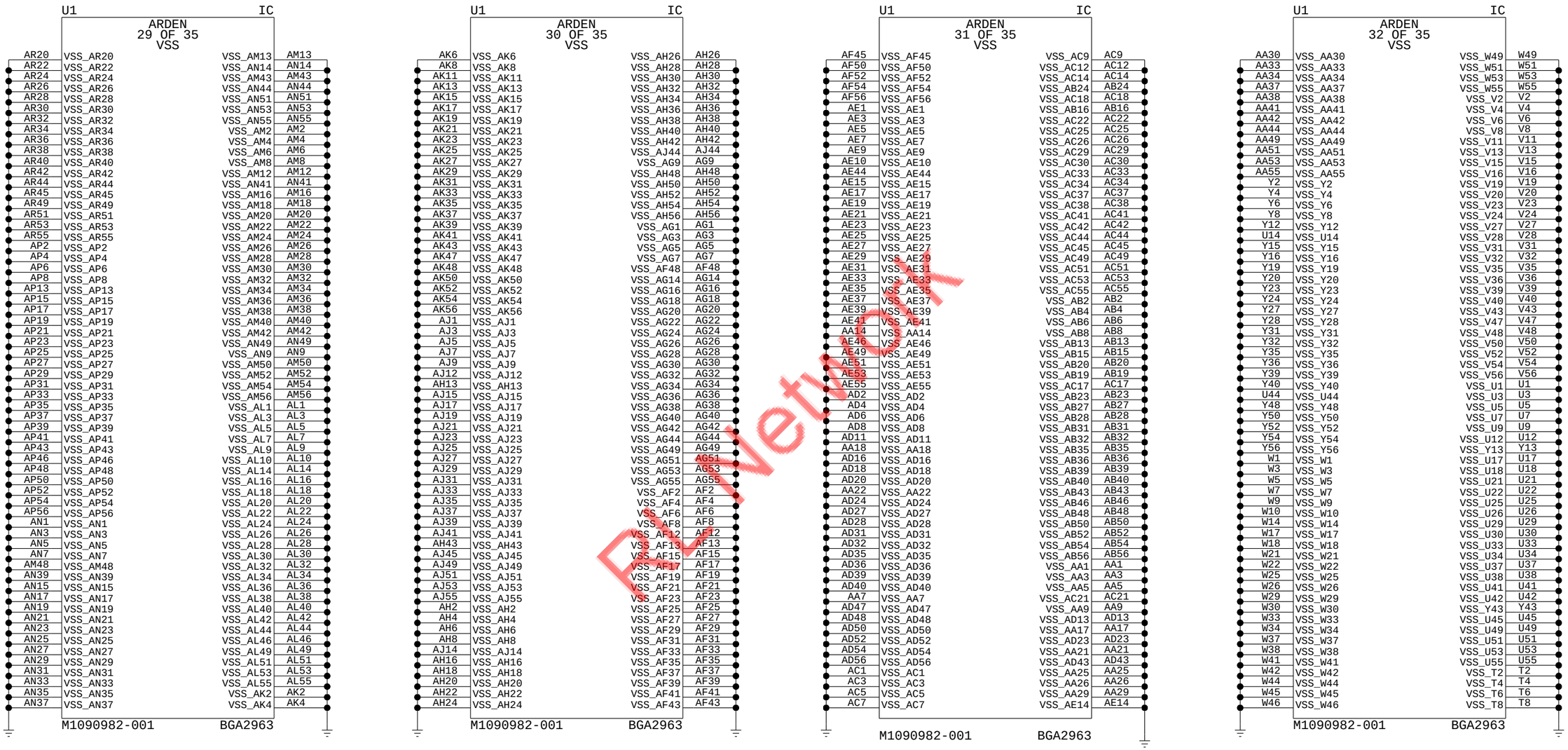






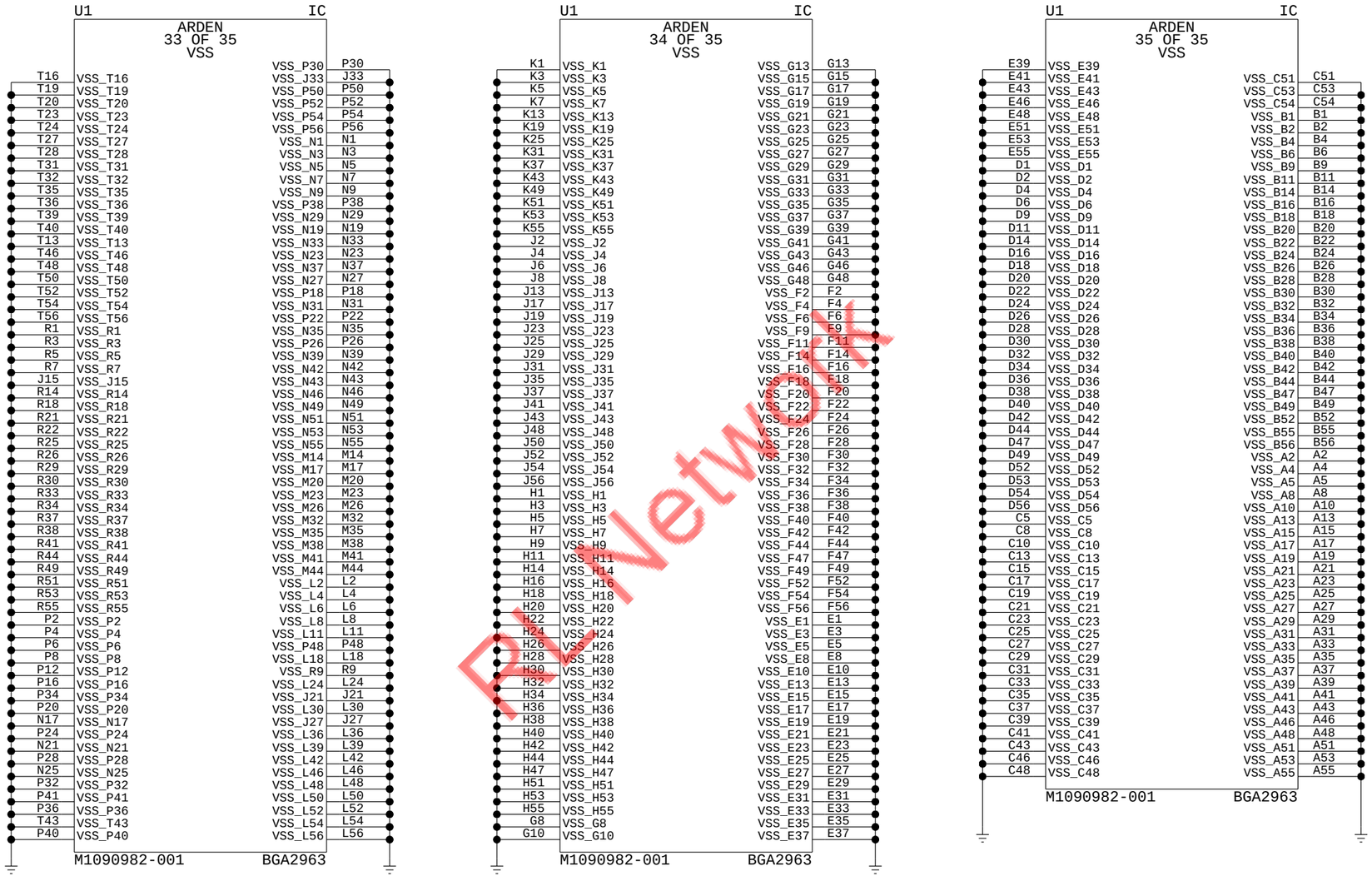
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	7/59	7/59	E Retail	1.03

SOC: POWER: VSS



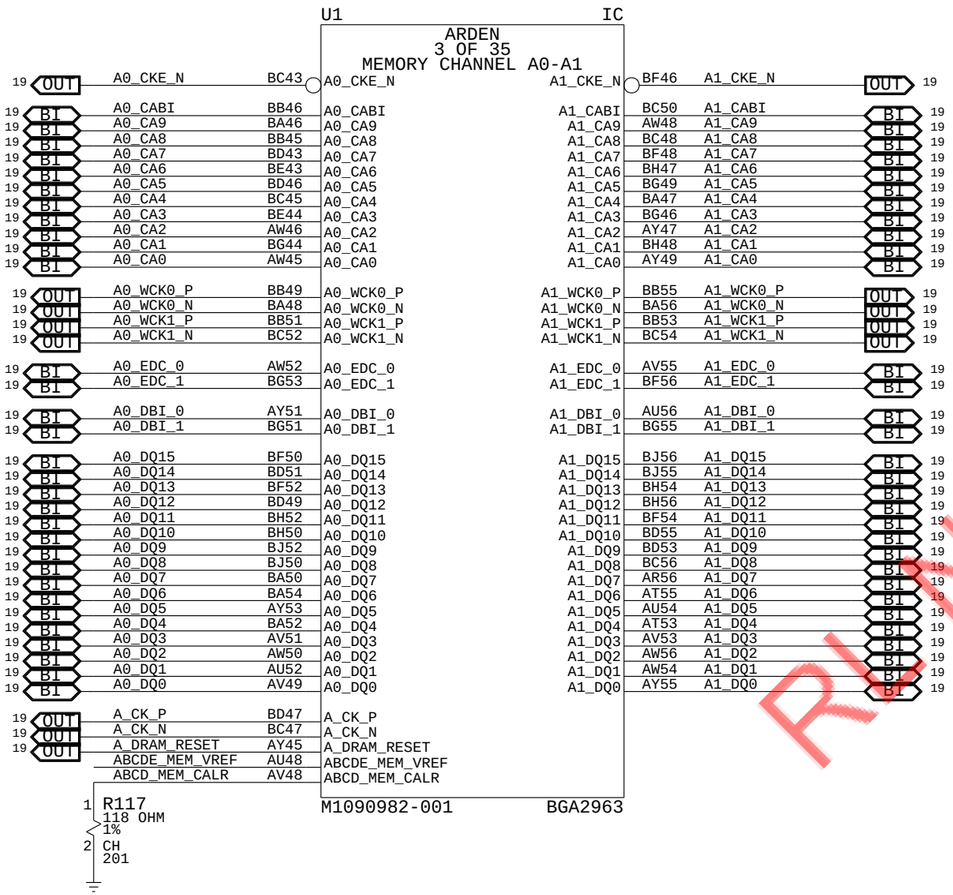
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	8/59	8/59	E Retail	1.03

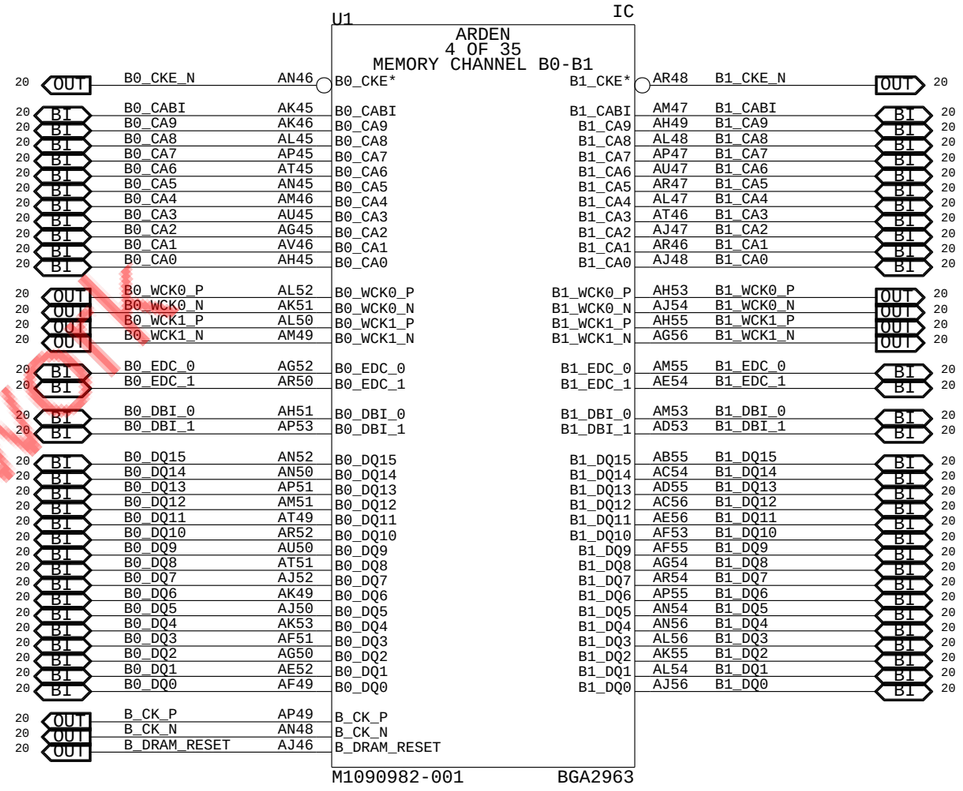
SOC: POWER: VSS



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	9/59	9/59	E Retail	1.03

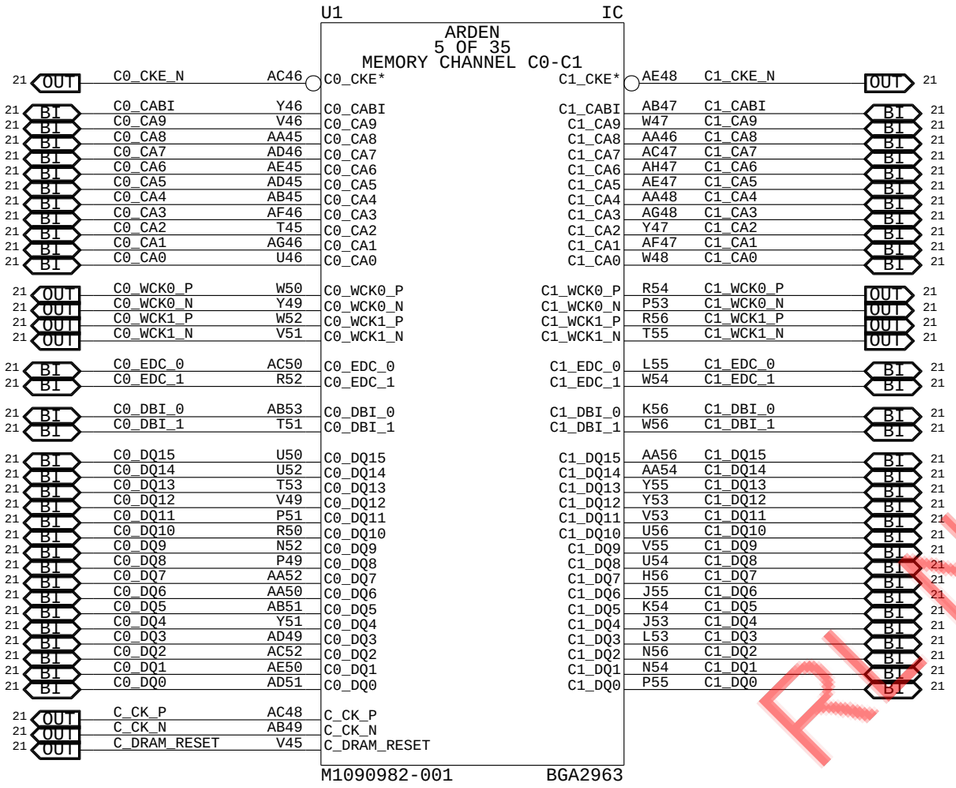
SOC: MEMORY: PARTITION A & B

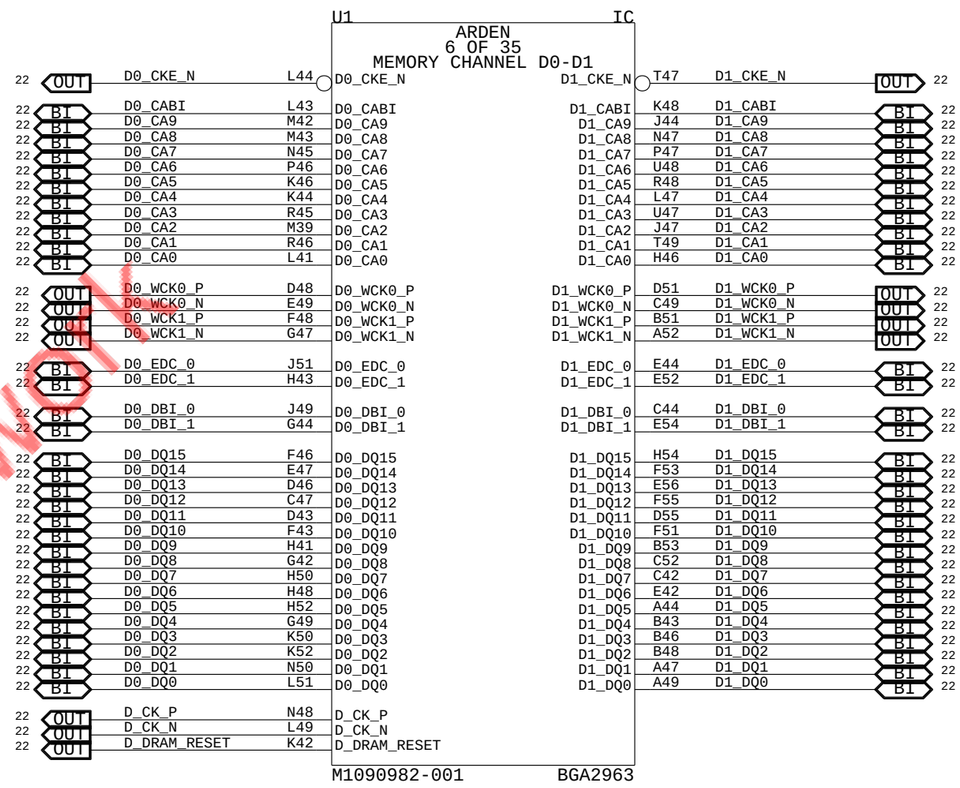




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	10/59	10/59	E Retail	1.03

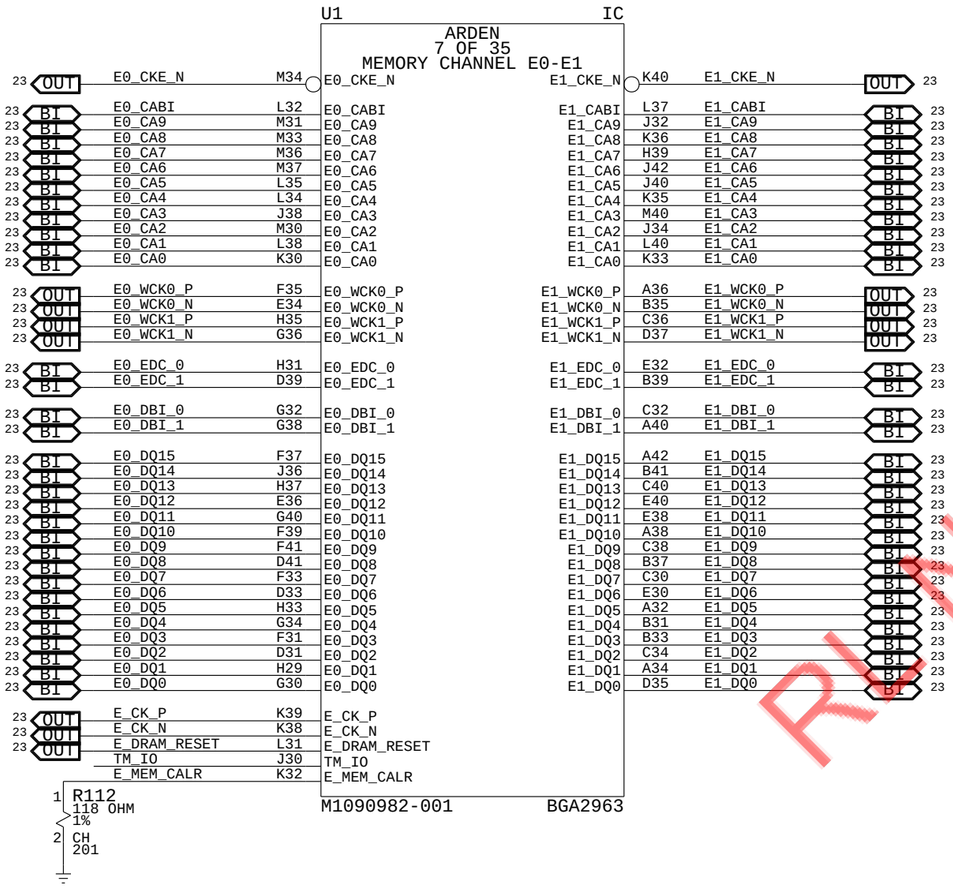
SOC: MEMORY: PARTITION C & D

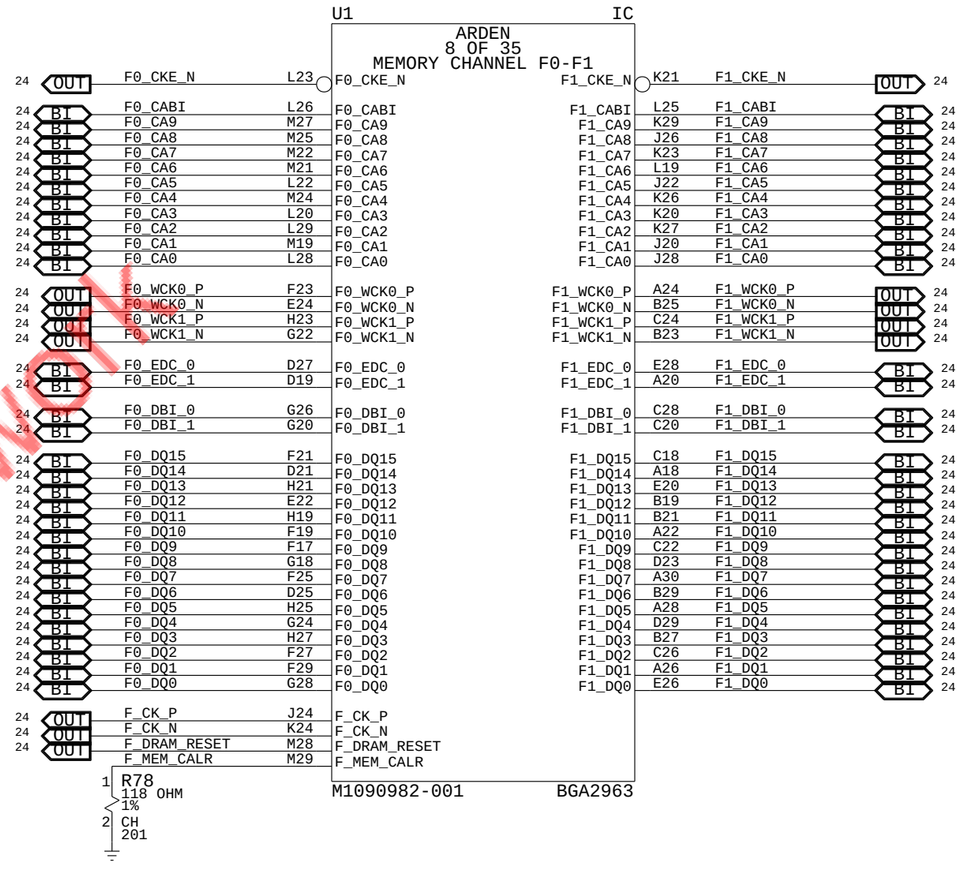




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	11/59	11/59	E Retail	1.03

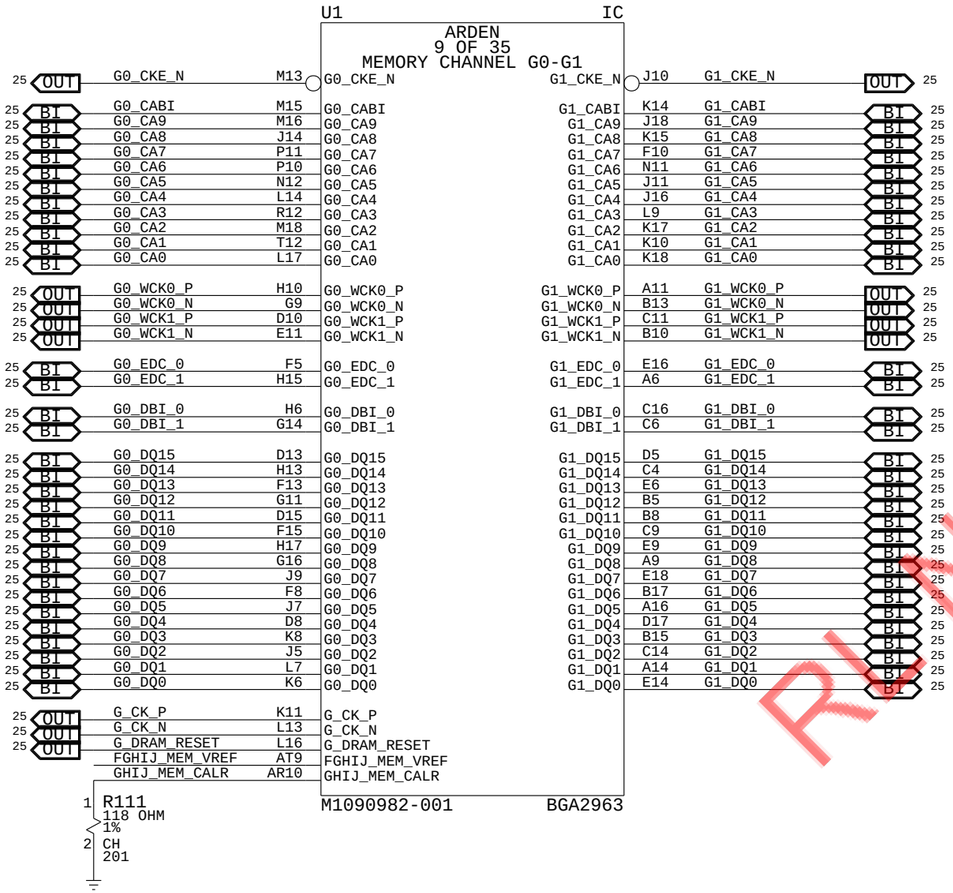
SOC: MEMORY: PARTITION E & F

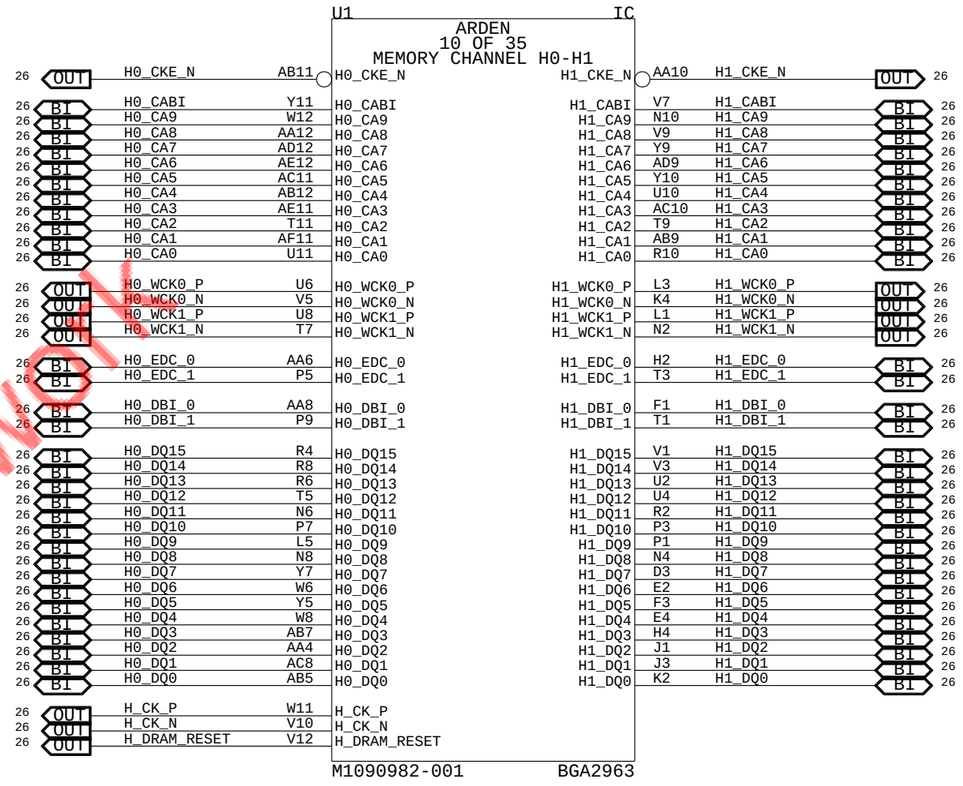




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	12/59	12/59	E Retail	1.03

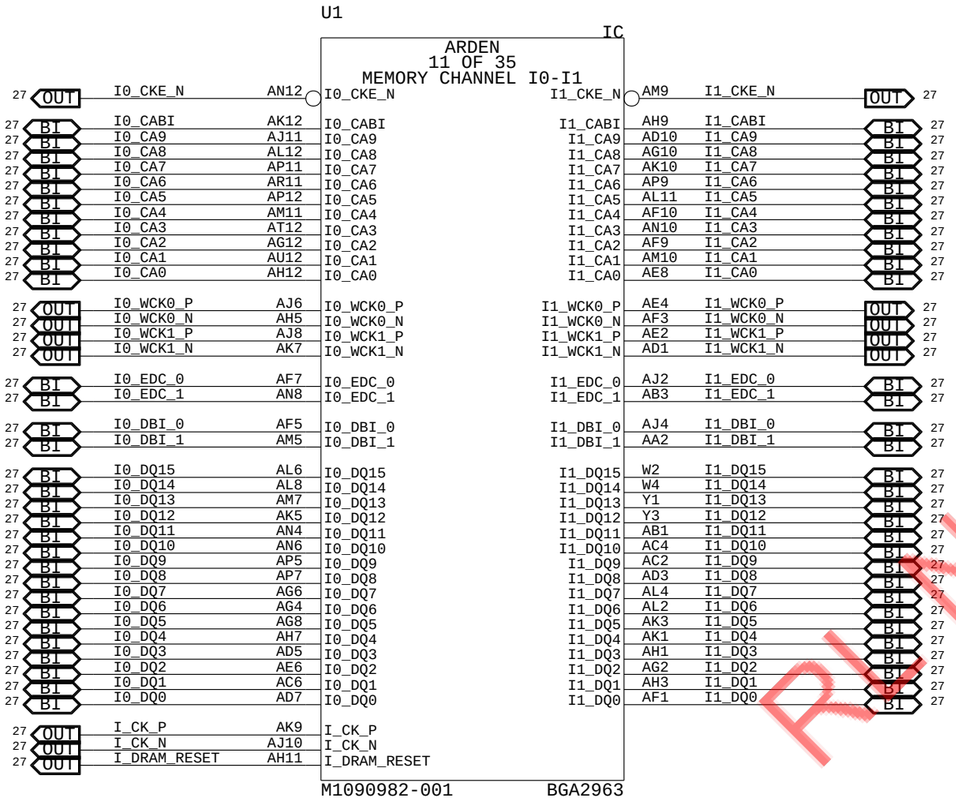
SOC: MEMORY: PARTITION G & H

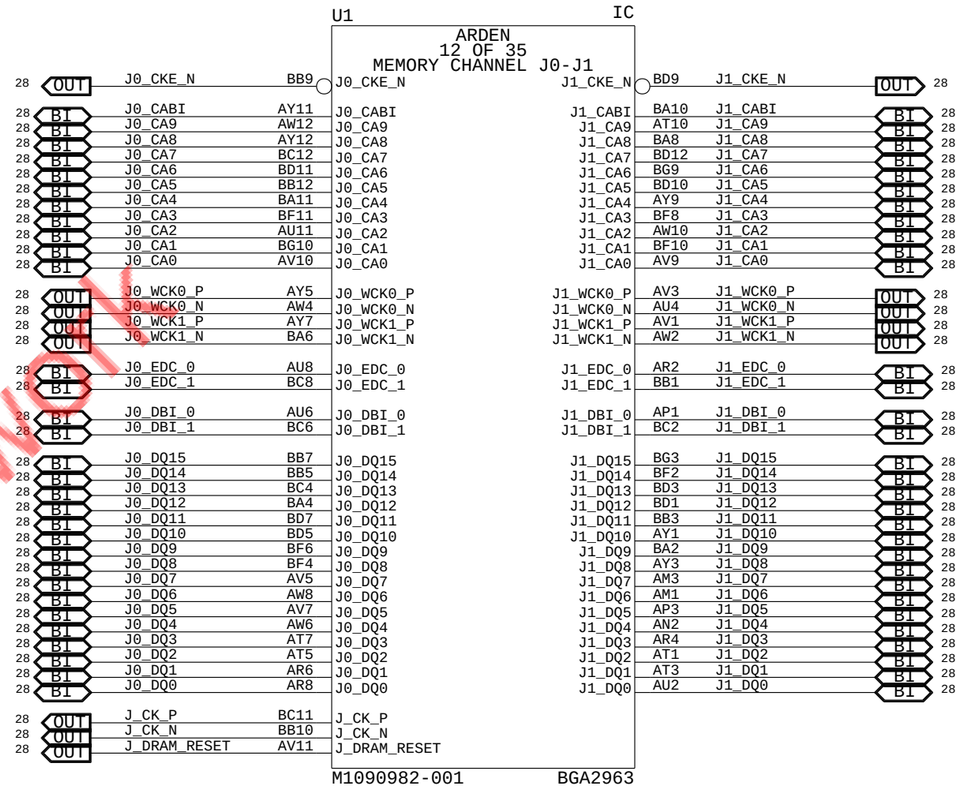




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	13/59	13/59	E Retail	1.03

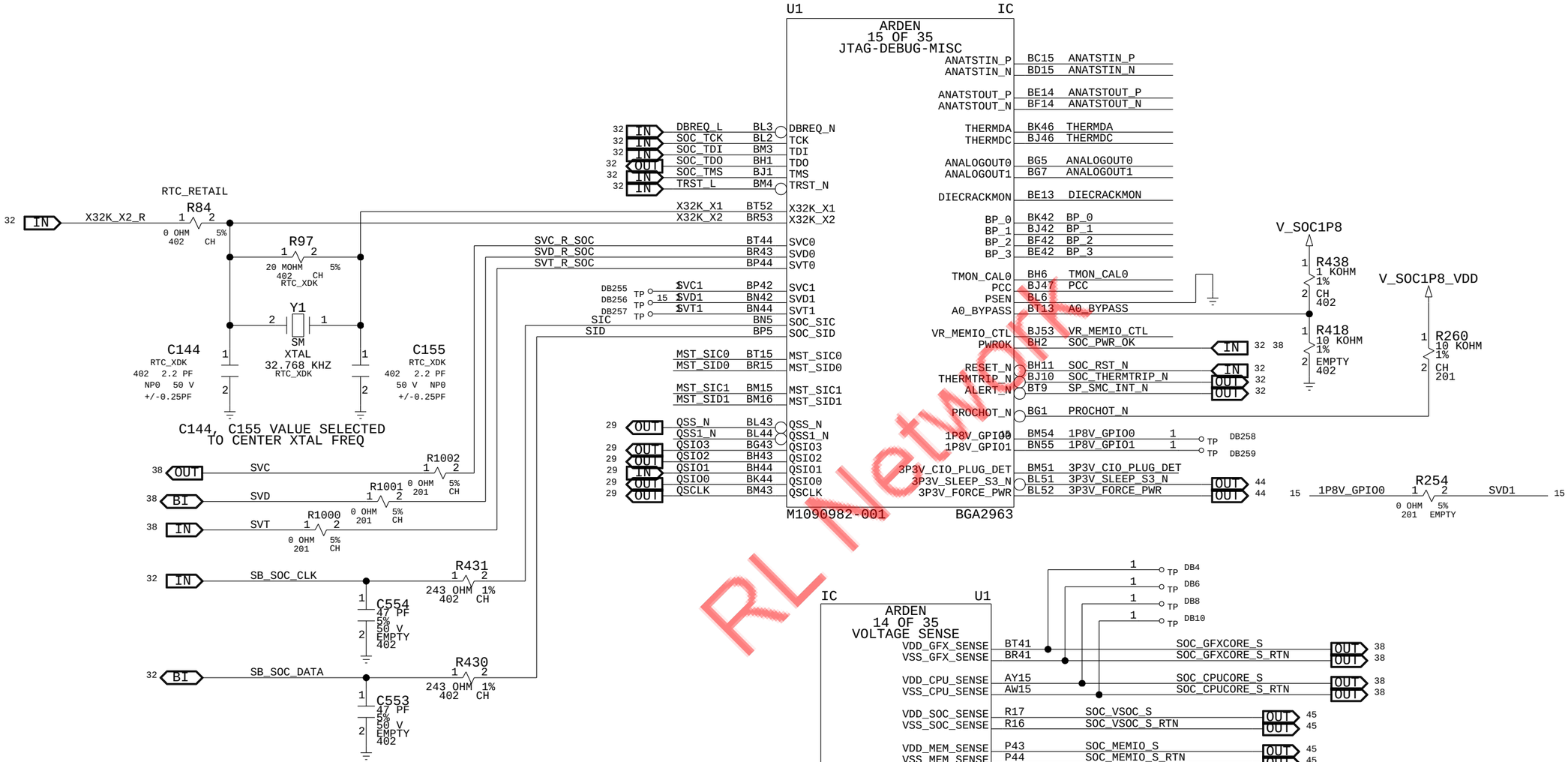
SOC: MEMORY: PARTITION I & J





MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	14/59	14/59	E Retail	1.03

SOC: DEBUG, SB SIGNALS, VOLTAGE SENSE



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	15/59	15/59	E Retail	1.03

SOC: DECOUPLING

V_GFXCORE 22UF 0603 DECOUPLING (116)

V_GFXCORE

C1514 C462 C912 C969 C1011 C1266 C1273 C1283 C1324 C1335
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C1451 C1569 C1475 C1554 C1574 C1465 C1452 C1489 C1580 C1510
22 UF 20% 6.3 V X5R 603

V_GFXCORE 10UF 0603 DECOUPLING (53)

V_GFXCORE

C1573 C1532 C1502 C1562 C1483 C1461 C1472 C1476 C1572 C1575
10 UF 20% 6.3 V X5R 603

V_GFXCORE

C1560 C1457 C1555 C1505 C1445 C1456 C1495 C1564 C1494 C1565
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C1582 C255 C1581 C261 C263 C274 C278 C280 C293 C295
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C1544 C1556 C1541 C1520 C1533 C1543 C1517 C1516 C1524 C1576
10 UF 20% 6.3 V X5R 603

V_GFXCORE

C1531 C1559 C1540 C1549 C1447 C1458 C1449 C1497 C1496 C1506
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C254 C256 C260 C262 C264 C277 C279 C281 C294 C296
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C1521 C1534 C1490 C1477 C1446 C1463 C1469 C1487 C1501 C1529
10 UF 20% 6.3 V X5R 603

V_GFXCORE

C1561 C1530 C1507 C1550 C1448 C1459 C1563 C1474 C1485 C1508
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C1594 C1598 C1602 C1606 C1610 C1614 C1618 C1622 C1626 C1630
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C1518 C328 C1542 C1567 C1523 C1460 C1473 C1484 C1498 C1481
10 UF 20% 6.3 V X5R 603

V_GFXCORE

C1591 C1595 C1599 C1603 C1607 C1611 C1615 C1619 C1623 C1627
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C1552 C1608 C1486 C1500 C1509 C253
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C1522 C1566 C1571 C1482 C1471 C1464 C1578 C1488 C1579 C1470
10 UF 20% 6.3 V X5R 603

V_GFXCORE

C1592 C1596 C1450 C1604 C1631 C1612 C1616 C1620 C1624 C1628
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C1515 C1528 C1539
10 UF 20% 6.3 V X5R 603

V_GFXCORE

C1593 C1597 C1601 C1605 C1609 C1613 C1617 C1621 C1625 C1629
22 UF 20% 6.3 V X5R 603

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	16/59	16/59	E Retail	1.03

SOC: DECOUPLING

V_GFXCORE 22UF 0603 DECOUPLING (53)

V_GFXCORE

C1694 C1700 C1706 C1712 C1718 C1724 C1748 C670 C672 C678
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C309 C333 C352 C443 C671 C673 C684 C685 C686 C687
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C1693 C1699 C1705 C1711 C1717 C1723 C1729 C1735 C1741 C1747
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C1673 C1675 C1677 C1679 C1681 C1683 C1685 C1687 C1689 C1691
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C1674 C1676 C1678 C1680 C1682 C1684 C1686 C1688 C1690 C1692
22 UF 20% 6.3 V X5R 603

V_GFXCORE

C330 C351 C389
22 UF 20% 6.3 V X5R 603

V_CPUCORE 22UF 0603 DECOUPLING (61)

V_CPUCORE

C1525 C1468 C1672 C1480 C1671 C1538 C1454 C1467 C1667 C1590
22 UF 20% 6.3 V X5R 603

V_CPUCORE

C1722 C1703 C1716 C308 C1721 C307 C1733 C1740 C1728 C1734
22 UF 20% 6.3 V X5R 603

V_CPUCORE

C1634 C1638 C1642 C1646 C1650 C1654 C1658 C1662 C1666 C1670
22 UF 20% 6.3 V X5R 603

V_CPUCORE

C1633 C1637 C1641 C1645 C1649 C1653 C1455 C1661 C1665 C1669
22 UF 20% 6.3 V X5R 603

V_CPUCORE

C1632 C1636 C1640 C1644 C1648 C1652 C1656 C1660 C1664 C1504
22 UF 20% 6.3 V X5R 603

V_CPUCORE

C1512 C1635 C1639 C1643 C1647 C1651 C1655 C1659 C1663 C1526 C1479
22 UF 20% 6.3 V X5R 603

V_CPUCORE 1UF 0201 DECOUPLING (4)

V_CPUCORE

C151 C166 C167 C168
1 UF 20% 6.3 V X5R 201

V_CPUCORE 10UF 0603 DECOUPLING (8)

V_CPUCORE

C1513 C1492 C1546 C1586 C1466 C1478 C1585 C1493
10 UF 20% 6.3 V X5R 603

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	17/59	17/59	E Retail	1.03

SOC: DECOUPLING

V_MEMPHY 1UF 201 DECOUPLING (87)

V_MEMPHY

C763 C769 C781 C785 C792 C801 C805 C811 C815 C826
C764 C770 C782 C789 C796 C802 C806 C812 C816 C827
C766 C771 C783 C790 C798 C803 C807 C813 C817 C828
C767 C772 C784 C791 C800 C804 C808 C814 C818 C829
C228 C229 C272 C273 C276 C286 C287 C288 C291 C292
C418 C419 C437 C484 C510 C512 C513 C514 C515 C516
C531 C537 C544 C547 C555 C558 C560 C562 C565 C567
C533 C538 C545 C548 C556 C559 C561 C563 C566 C569
C535 C541 C546 C551 C557 C768 C780

1 UF 20% 6.3 V X5R 201

V_SOC 22UF 0603 DECOUPLING (13)

V_SOC

C688 C690 C691 C692 C693 C694 C702 C696 C697 C698
C699 C700 C701

22 UF 20% 6.3 V X5R 603

V_SOC 1UF 0201 DECOUPLING (4)

V_SOC

C570 C854 C576 C578

1 UF 20% 6.3 V X5R 201

V_MEMIO 1UF 201 DECOUPLING (54)

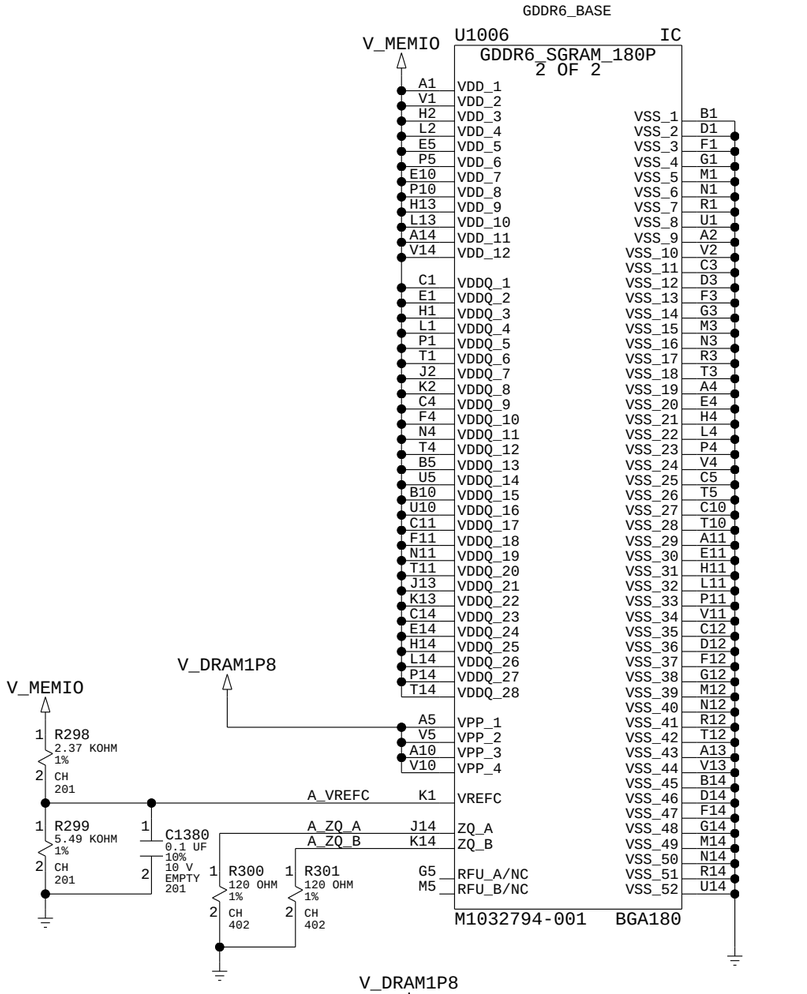
V_MEMIO

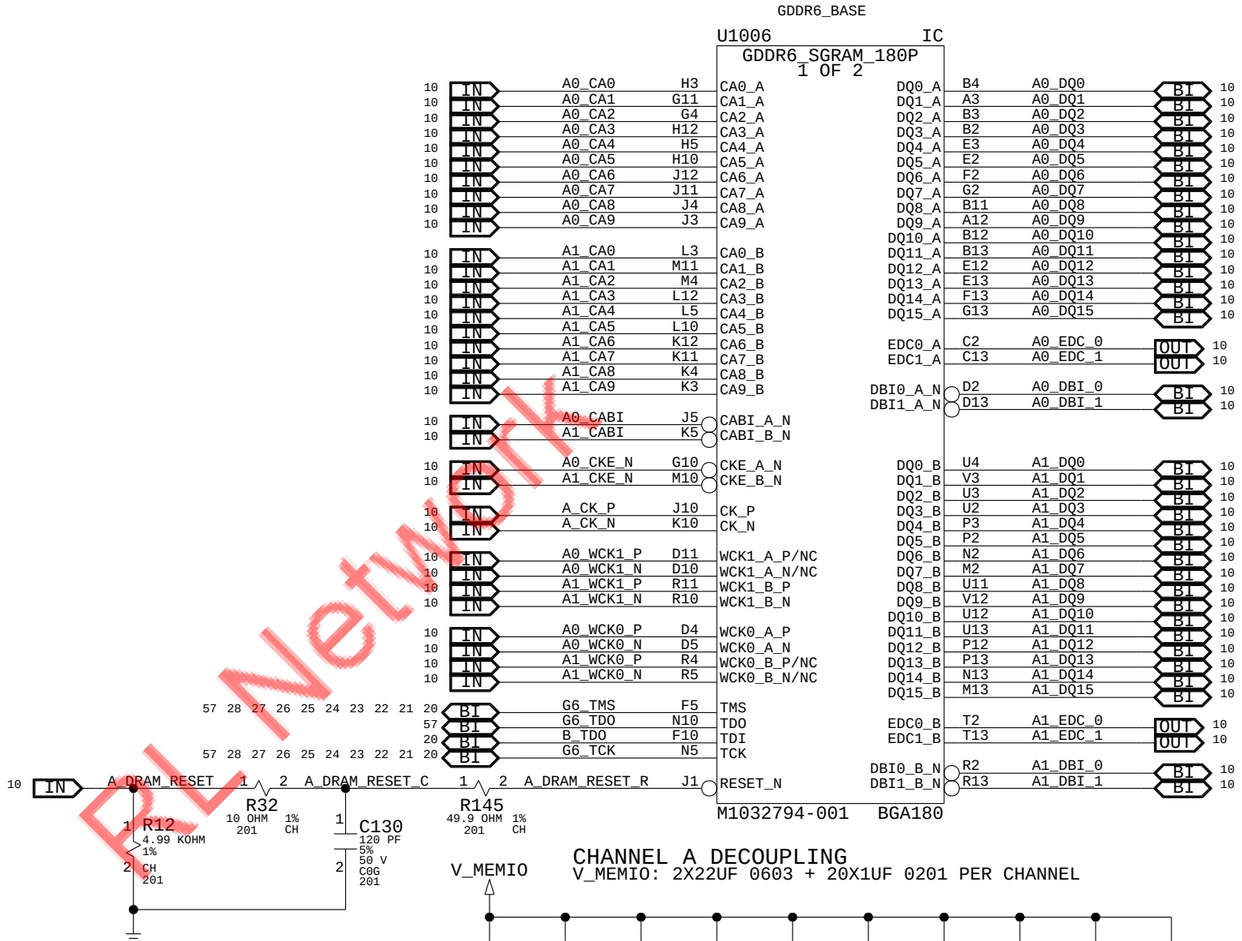
C336 C625 C354 C360 C375 C388 C609 C403 C408 C413
C337 C624 C620 C361 C384 C392 C398 C404 C409 C612
C338 C628 C356 C362 C385 C394 C399 C406 C632 C415
C339 C617 C359 C374 C387 C396 C400 C622 C412 C417
C518 C630 C522 C614 C524 C525 C526 C611 C529 C608
C605 C610 C613 C616

1 UF 20% 6.3 V X5R 201

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	18/59	18/59	E Retail	1.03

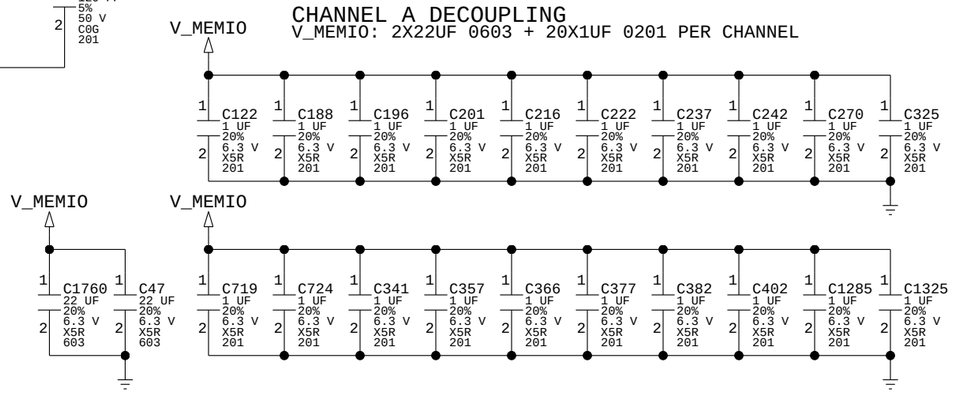
MEMORY: GDDR6 CHANNEL A: 8GB





CHANNEL A DECOUPLING

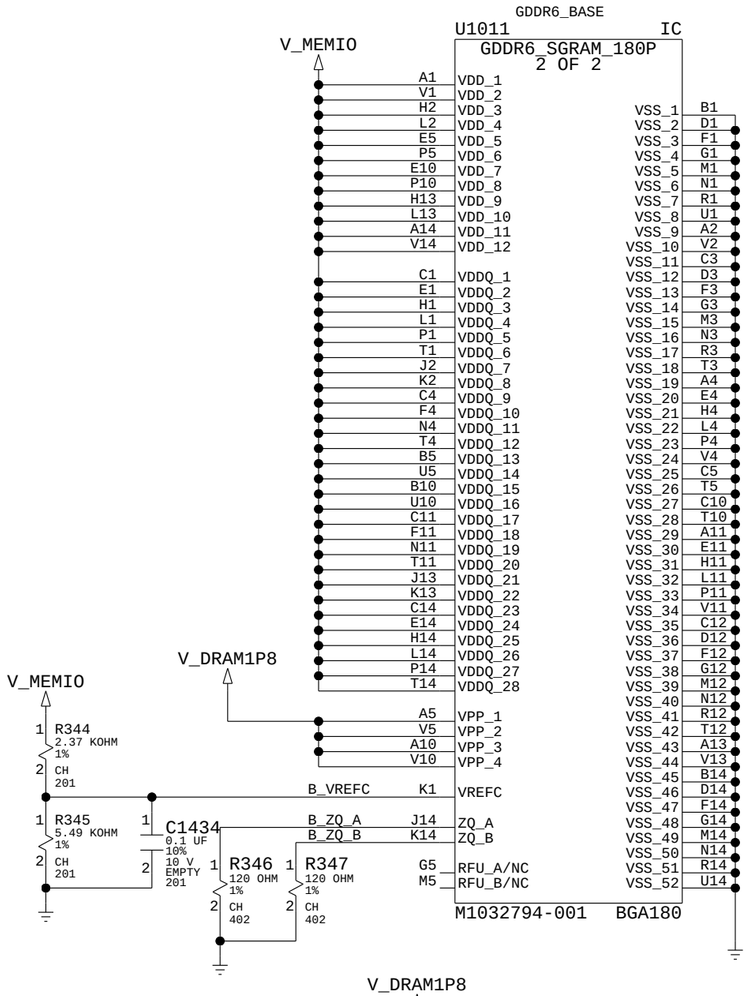
V_MEMIO: 2X22UF 0603 + 20X1UF 0201 PER CHANNEL

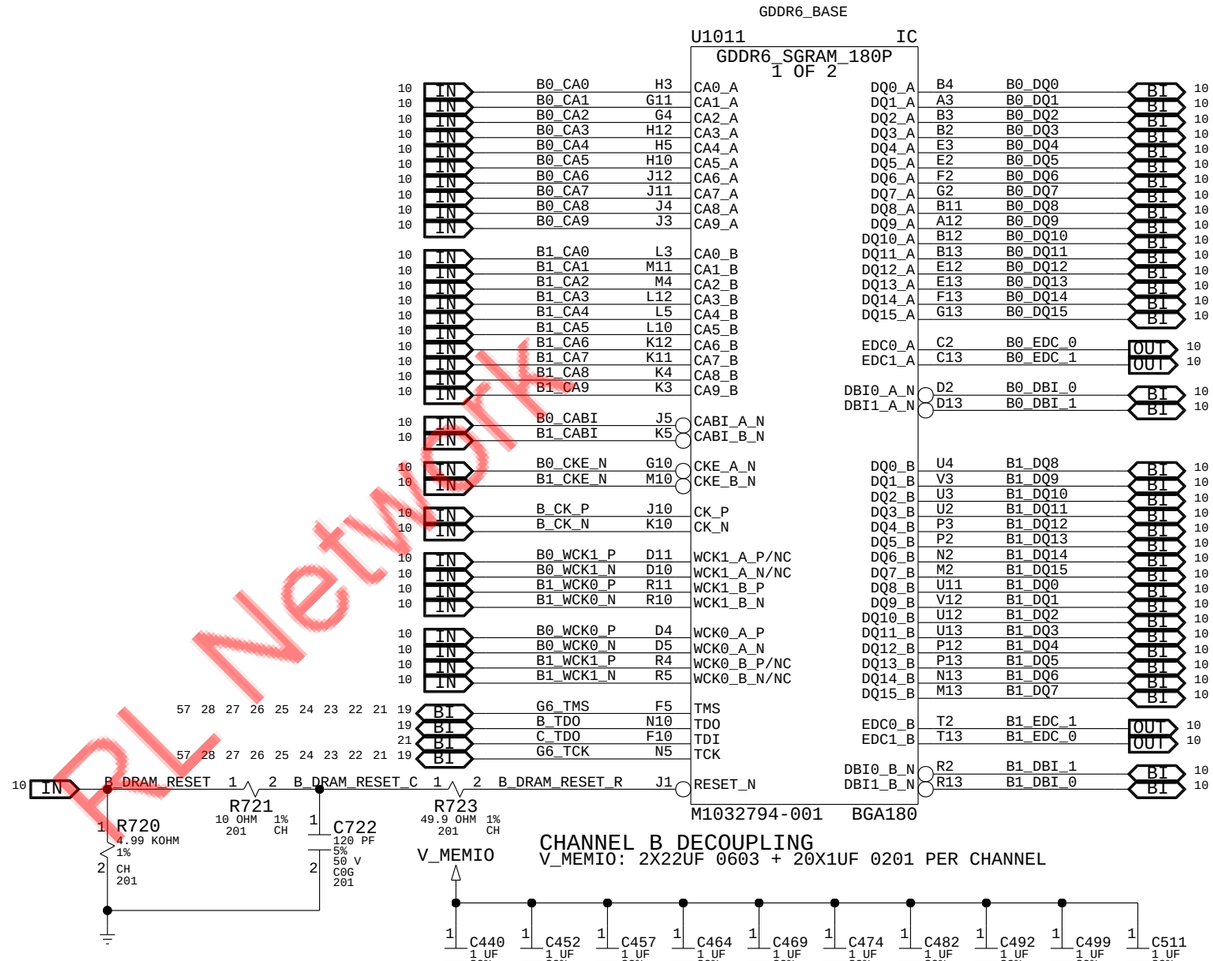


MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1098563-001	IC	U1009,U1003,U1008,U1007,U1002,U1011	GDDR6, SAMSUNG, 16GB	GDDR6_SAMSUNG
M1108660-001	IC	U1004,U1012,U1005,U1006	GDDR6, SAMSUNG, 8GB	GDDR6_SAMSUNG
M1107532-001	IC	U1009,U1003,U1008,U1007,U1002,U1011	GDDR6, HYNIX, 16GB	GDDR6_HYNIX
M1108913-001	IC	U1004,U1012,U1005,U1006	GDDR6, HYNIX, 8GB	GDDR6_HYNIX
M1107537-001	IC	U1009,U1003,U1008,U1007,U1002,U1011	GDDR6, MICRON, 16GB	GDDR6_MICRON
M1107533-001	IC	U1004,U1012,U1005,U1006	GDDR6, MICRON, 8GB	GDDR6_MICRON

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	19/59	19/59	E Retail	1.03

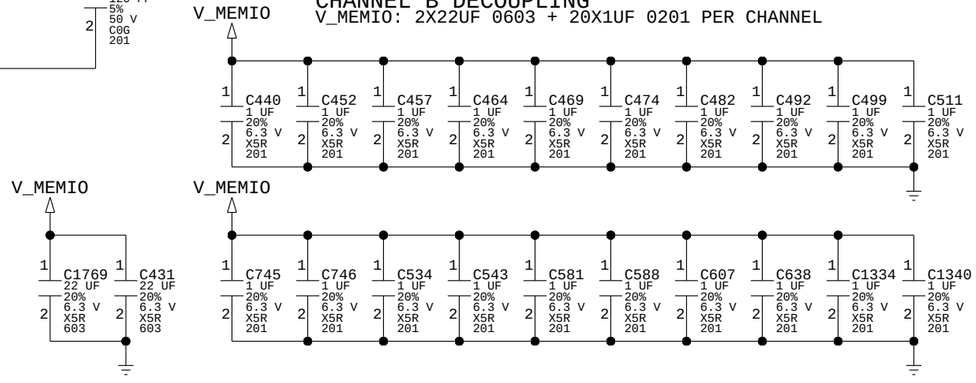
MEMORY: GDDR6 CHANNEL B: 16GB





CHANNEL B DECOUPLING

V_MEMIO: 2X22UF 0603 + 20X1UF 0201 PER CHANNEL



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	20/59	20/59	E Retail	1.03

MEMORY: GDDR6 CHANNEL C: 8GB

GDDR6_BASE

U1005 IC
GDDR6_SGRAM_180P
2 OF 2

V_MEMIO

A1	VDD_1		VSS_1	B1	
V1	VDD_2		VSS_2	D1	
H2	VDD_3		VSS_3	F1	
L2	VDD_4		VSS_4	G1	
E5	VDD_5		VSS_5	M1	
P5	VDD_6		VSS_6	N1	
E10	VDD_7		VSS_7	R1	
P10	VDD_8		VSS_8	U1	
H13	VDD_9		VSS_9	A2	
L13	VDD_10		VSS_10	V2	
A14	VDD_11		VSS_11	C3	
V14	VDD_12		VSS_12	D3	
C1	VDDQ_1		VSS_13	F3	
E1	VDDQ_2		VSS_14	G3	
H1	VDDQ_3		VSS_15	M3	
L1	VDDQ_4		VSS_16	N3	
P1	VDDQ_5		VSS_17	R3	
T1	VDDQ_6		VSS_18	T3	
J2	VDDQ_7		VSS_19	A4	
K2	VDDQ_8		VSS_20	E4	
C4	VDDQ_9		VSS_21	H4	
F4	VDDQ_10		VSS_22	L4	
N4	VDDQ_11		VSS_23	P4	
T4	VDDQ_12		VSS_24	V4	
B5	VDDQ_13		VSS_25	C5	
U5	VDDQ_14		VSS_26	T5	
B10	VDDQ_15		VSS_27	C10	
U10	VDDQ_16		VSS_28	T10	
C11	VDDQ_17		VSS_29	A11	
F11	VDDQ_18		VSS_30	E11	
N11	VDDQ_19		VSS_31	H11	
T11	VDDQ_20		VSS_32	L11	
J13	VDDQ_21		VSS_33	P11	
K13	VDDQ_22		VSS_34	V11	
C14	VDDQ_23		VSS_35	C12	
E14	VDDQ_24		VSS_36	D12	
H14	VDDQ_25		VSS_37	F12	
L14	VDDQ_26		VSS_38	G12	
P14	VDDQ_27		VSS_39	M12	
T14	VDDQ_28		VSS_40	N12	
A5	VPP_1		VSS_41	R12	
V5	VPP_2		VSS_42	T12	
A10	VPP_3		VSS_43	A13	
V10	VPP_4		VSS_44	V13	
			VSS_45	B14	
			VSS_46	D14	
			VSS_47	F14	
			VSS_48	G14	
			VSS_49	M14	
			VSS_50	N14	
			VSS_51	R14	
			VSS_52	U14	
C_VREFC	K1	VREFC			
C_ZQ_A	J14	ZQ_A			
C_ZQ_B	K14	ZQ_B			
G5		RFU_A/NC			
M5		RFU_B/NC			

M1032794-001 BGA180

V_DRAM1P8

V_MEMIO

R308 2.37 KOHM 1% CH 201

R309 5.49 KOHM 1% CH 201

C1392 0.1 UF 10% 10 V EMPTY 201

R310 120 OHM 1% CH 402

R311 120 OHM 1% CH 402

V_DRAM1P8

C1393 10 UF 20% 6.3 V X5R 402

C1394 1 UF 20% 6.3 V X5R 201

C1395 1 UF 20% 6.3 V X5R 201

C1396 1 UF 20% 6.3 V X5R 201

C1397 1 UF 20% 6.3 V X5R 201

GDDR6_BASE

U1005 IC
GDDR6_SGRAM_180P
1 OF 2

IN	C0_CA0	H3	CA0_A		
IN	C0_CA1	G11	CA1_A		
IN	C0_CA2	G4	CA2_A		
IN	C0_CA3	H12	CA3_A		
IN	C0_CA4	H5	CA4_A		
IN	C0_CA5	H10	CA5_A		
IN	C0_CA6	J12	CA6_A		
IN	C0_CA7	J11	CA7_A		
IN	C0_CA8	J4	CA8_A		
IN	C0_CA9	J3	CA9_A		
IN	C1_CA0	L3	CA0_B		
IN	C1_CA1	M11	CA1_B		
IN	C1_CA2	M4	CA2_B		
IN	C1_CA3	L12	CA3_B		
IN	C1_CA4	L5	CA4_B		
IN	C1_CA5	L10	CA5_B		
IN	C1_CA6	K12	CA6_B		
IN	C1_CA7	K11	CA7_B		
IN	C1_CA8	K4	CA8_B		
IN	C1_CA9	K3	CA9_B		
IN	C0_CABI	J5	CABI_A_N		
IN	C1_CABI	K5	CABI_B_N		
IN	C0_CKE_N	G10	CKE_A_N		
IN	C1_CKE_N	M10	CKE_B_N		
IN	C_CK_P	J10	CK_P		
IN	C_CK_N	K10	CK_N		
IN	C0_WCK0_P	D11	WCK1_A_P/NC		
IN	C0_WCK0_N	D10	WCK1_A_N/NC		
IN	C1_WCK1_P	R11	WCK1_B_P		
IN	C1_WCK1_N	R10	WCK1_B_N		
IN	C0_WCK1_P	D4	WCK0_A_P		
IN	C0_WCK1_N	D5	WCK0_A_N		
IN	C1_WCK0_P	R4	WCK0_B_P/NC		
IN	C1_WCK0_N	R5	WCK0_B_N/NC		
BI	G6_TMS	F5	TMS		
BI	C_TDO	N10	TDO		
BI	D_TDO	F10	TDI		
BI	G6_TCK	N5	TCK		
IN	C_DRAM_RESET	J1	RESET_N		
BI	DQ0_A	B4	C0_DQ8	BI	
BI	DQ1_A	A3	C0_DQ9	BI	
BI	DQ2_A	B3	C0_DQ10	BI	
BI	DQ3_A	B2	C0_DQ11	BI	
BI	DQ4_A	E3	C0_DQ12	BI	
BI	DQ5_A	E2	C0_DQ13	BI	
BI	DQ6_A	F2	C0_DQ14	BI	
BI	DQ7_A	G2	C0_DQ15	BI	
BI	DQ8_A	B11	C0_DQ0	BI	
BI	DQ9_A	A12	C0_DQ1	BI	
BI	DQ10_A	B12	C0_DQ2	BI	
BI	DQ11_A	B13	C0_DQ3	BI	
BI	DQ12_A	E12	C0_DQ4	BI	
BI	DQ13_A	E13	C0_DQ5	BI	
BI	DQ14_A	F13	C0_DQ6	BI	
BI	DQ15_A	G13	C0_DQ7	BI	
OUT	EDC0_A	C2	C0_EDC_1	OUT	
OUT	EDC1_A	C13	C0_EDC_0	OUT	
BI	DBI0_A_N	D2	C0_DBI_1	BI	
BI	DBI1_A_N	D13	C0_DBI_0	BI	
BI	DQ0_B	U4	C1_DQ0	BI	
BI	DQ1_B	V3	C1_DQ1	BI	
BI	DQ2_B	U3	C1_DQ2	BI	
BI	DQ3_B	U2	C1_DQ3	BI	
BI	DQ4_B	P3	C1_DQ4	BI	
BI	DQ5_B	P2	C1_DQ5	BI	
BI	DQ6_B	N2	C1_DQ6	BI	
BI	DQ7_B	M2	C1_DQ7	BI	
BI	DQ8_B	U11	C1_DQ8	BI	
BI	DQ9_B	V12	C1_DQ9	BI	
BI	DQ10_B	U12	C1_DQ10	BI	
BI	DQ11_B	U13	C1_DQ11	BI	
BI	DQ12_B	P12	C1_DQ12	BI	
BI	DQ13_B	P13	C1_DQ13	BI	
BI	DQ14_B	N13	C1_DQ14	BI	
BI	DQ15_B	M13	C1_DQ15	BI	
OUT	EDC0_B	T2	C1_EDC_0	OUT	
OUT	EDC1_B	T13	C1_EDC_1	OUT	
BI	DBI0_B_N	R2	C1_DBI_0	BI	
BI	DBI1_B_N	R13	C1_DBI_1	BI	

M1032794-001 BGA180

C_DRAM_RESET R662 4.99 KOHM 1% CH 201

R663 10 OHM 1% CH 201

C667 120 PF 5% 50 V C0G 201

R674 49.9 OHM 1% CH 201

V_MEMIO

C1762 22 UF 20% 6.3 V X5R 603

C62 22 UF 20% 6.3 V X5R 603

CHANNEL C DECOUPLING

V_MEMIO: 2X22UF 0603 + 20X1UF 0201 PER CHANNEL

V_MEMIO

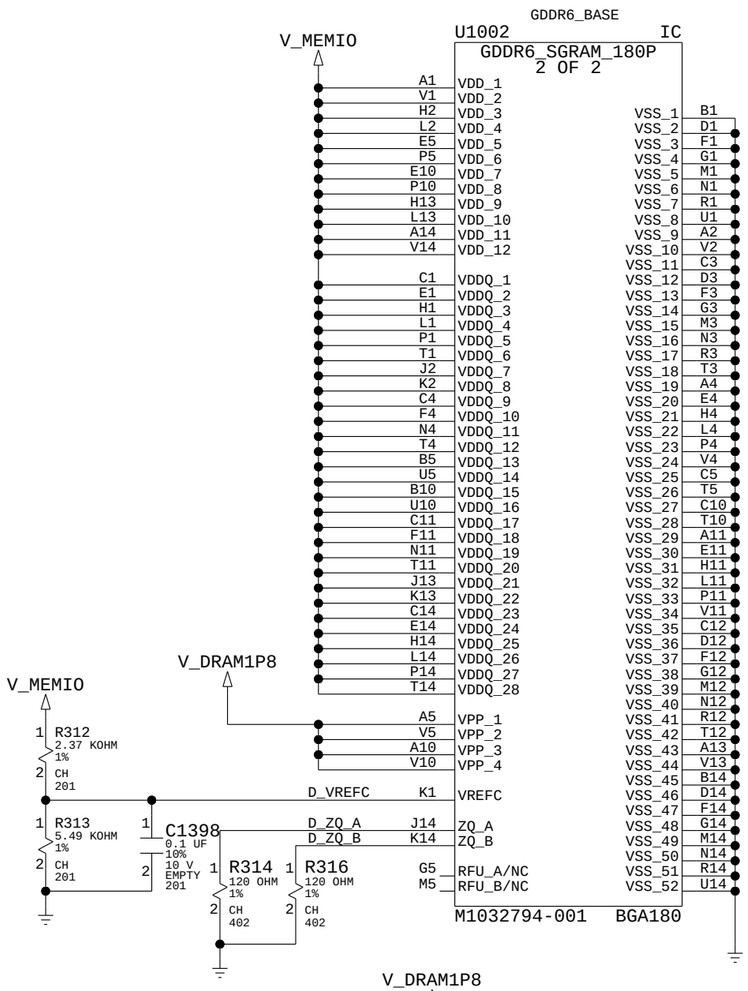
C125 C189 C197 C204 C218 C232 C238 C243 C301 C326
1 UF 20% 6.3 V X5R 201

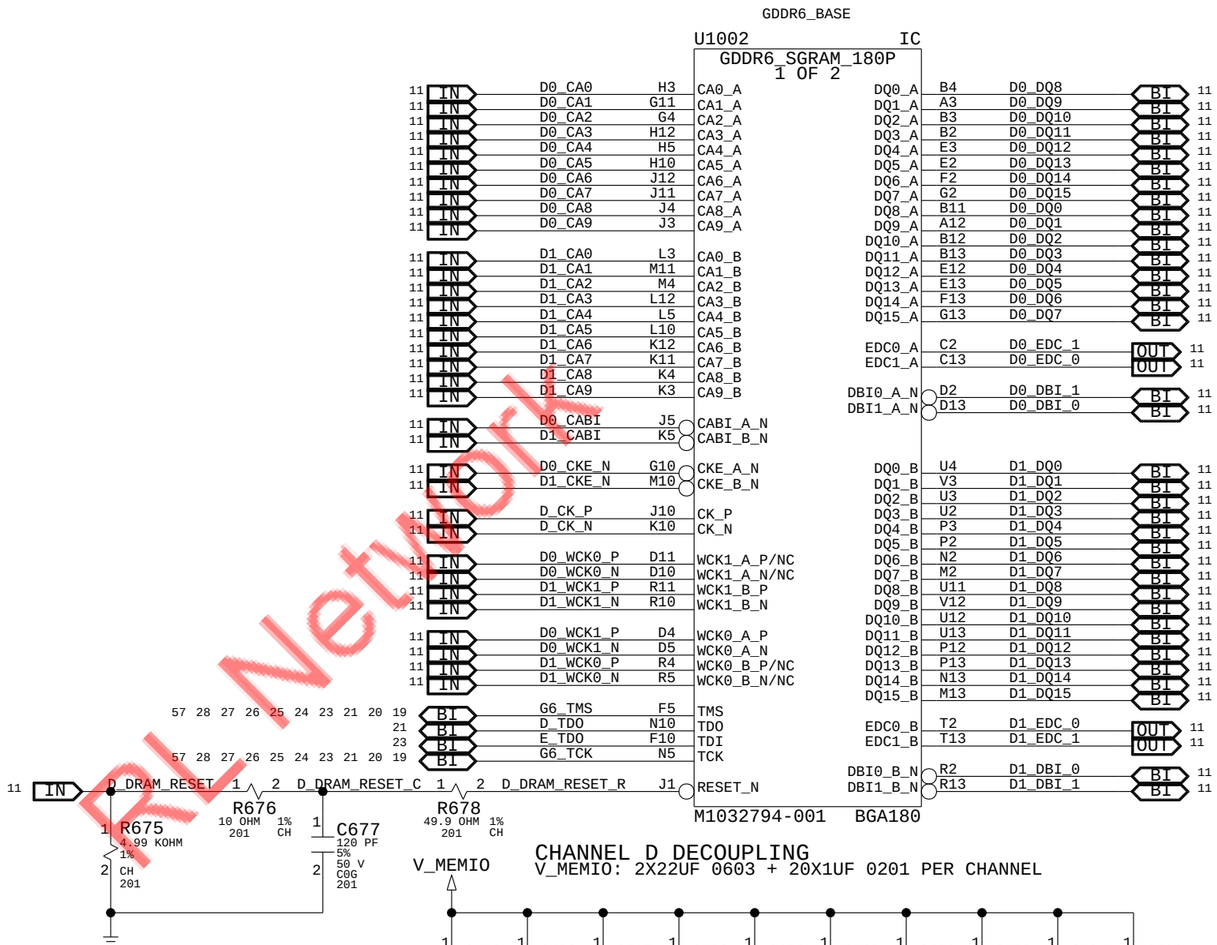
V_MEMIO

C727 C732 C342 C358 C368 C378 C383 C405 C1294 C1326
1 UF 20% 6.3 V X5R 201

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	21/59	21/59	E Retail	1.03

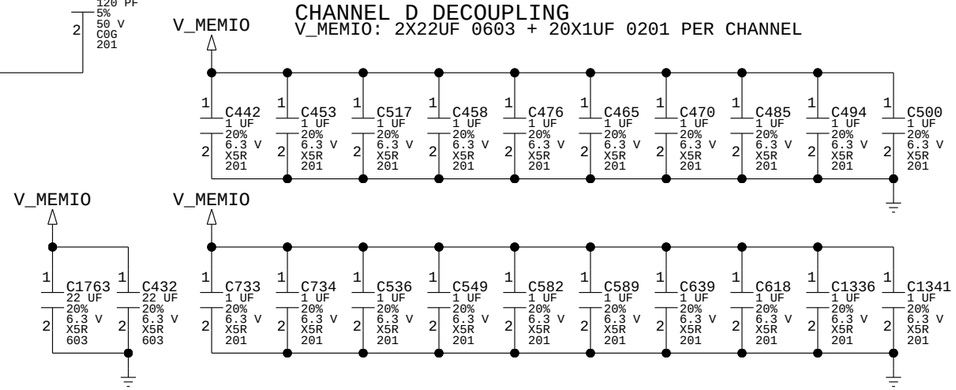
MEMORY: GDDR6 CHANNEL D: 16GB





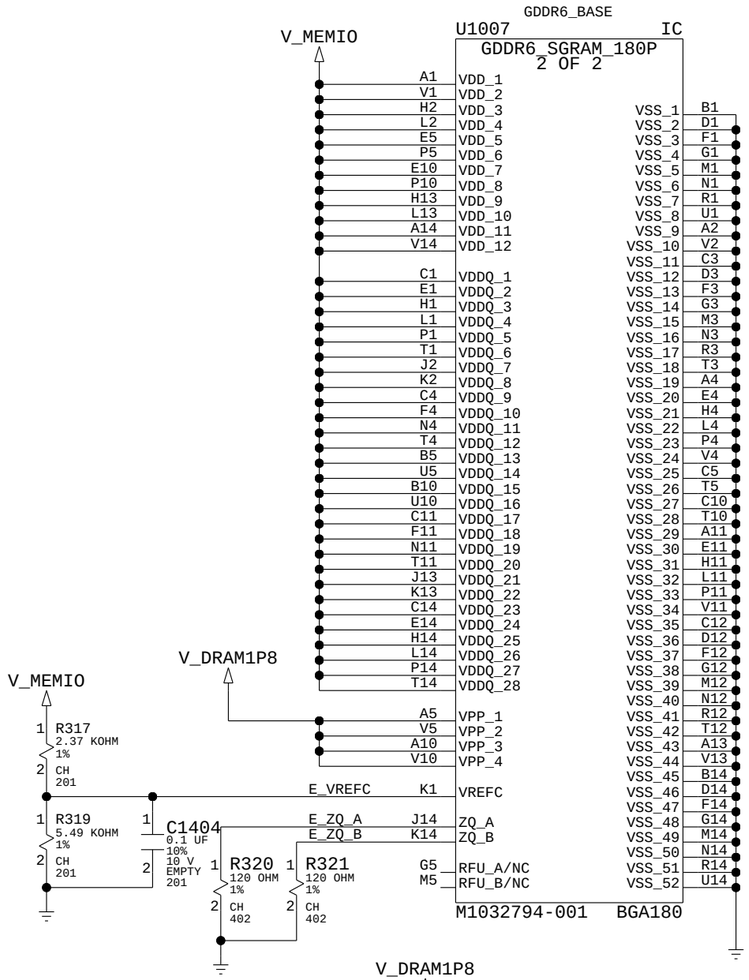
CHANNEL D DECOUPLING

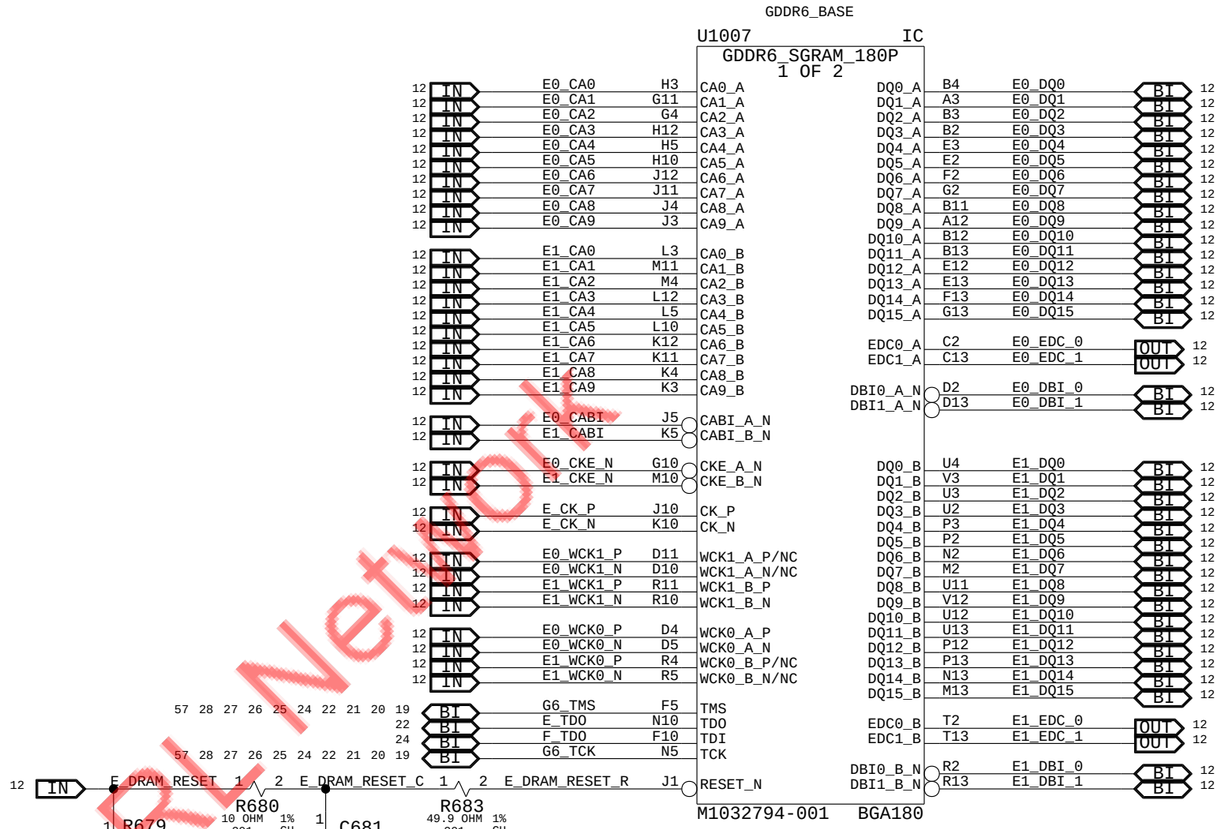
V_MEMIO: 2X22UF 0603 + 20X1UF 0201 PER CHANNEL

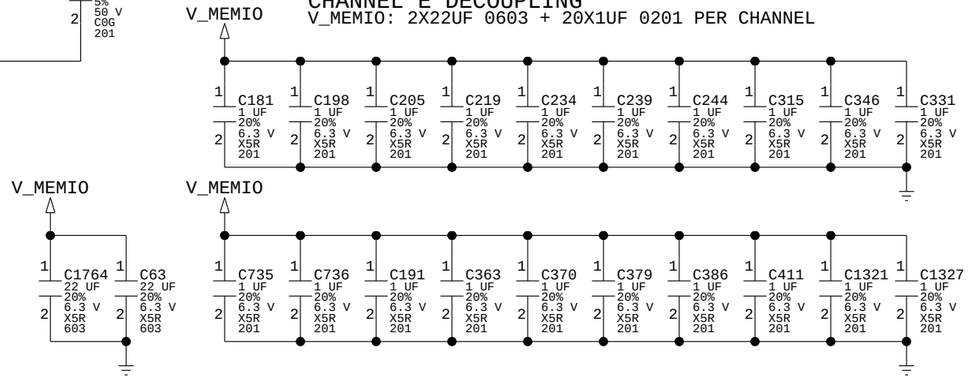


MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	22/59	22/59	E Retail	1.03

MEMORY: GDDR6 CHANNEL E: 16GB







MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	23/59	23/59	E Retail	1.03

MEMORY: GDDR6 CHANNEL F: 16GB

GDDR6_BASE

U1008 IC
GDDR6_SGRAM_180P
2 OF 2

A1	VDD_1		VSS_1	B1	
V1	VDD_2		VSS_2	D1	
H2	VDD_3		VSS_3	F1	
L2	VDD_4		VSS_4	G1	
E5	VDD_5		VSS_5	M1	
P5	VDD_6		VSS_6	N1	
E10	VDD_7		VSS_7	R1	
P10	VDD_8		VSS_8	U1	
H13	VDD_9		VSS_9	A2	
L13	VDD_10		VSS_10	V2	
A14	VDD_11		VSS_11	C3	
V14	VDD_12		VSS_12	D3	
C1	VDDQ_1		VSS_13	F3	
E1	VDDQ_2		VSS_14	G3	
H1	VDDQ_3		VSS_15	M3	
L1	VDDQ_4		VSS_16	N3	
P1	VDDQ_5		VSS_17	R3	
T1	VDDQ_6		VSS_18	T3	
J2	VDDQ_7		VSS_19	A4	
K2	VDDQ_8		VSS_20	E4	
C4	VDDQ_9		VSS_21	H4	
F4	VDDQ_10		VSS_22	L4	
N4	VDDQ_11		VSS_23	P4	
T4	VDDQ_12		VSS_24	V4	
B5	VDDQ_13		VSS_25	C5	
U5	VDDQ_14		VSS_26	T5	
B10	VDDQ_15		VSS_27	C10	
U10	VDDQ_16		VSS_28	T10	
C11	VDDQ_17		VSS_29	A11	
F11	VDDQ_18		VSS_30	E11	
N11	VDDQ_19		VSS_31	H11	
T11	VDDQ_20		VSS_32	L11	
J13	VDDQ_21		VSS_33	P11	
K13	VDDQ_22		VSS_34	V11	
C14	VDDQ_23		VSS_35	C12	
E14	VDDQ_24		VSS_36	D12	
H14	VDDQ_25		VSS_37	F12	
L14	VDDQ_26		VSS_38	G12	
P14	VDDQ_27		VSS_39	M12	
T14	VDDQ_28		VSS_40	N12	
A5	VPP_1		VSS_41	R12	
V5	VPP_2		VSS_42	T12	
A10	VPP_3		VSS_43	A13	
V10	VPP_4		VSS_44	V13	
			VSS_45	B14	
			VSS_46	D14	
			VSS_47	F14	
			VSS_48	G14	
			VSS_49	M14	
			VSS_50	N14	
			VSS_51	R14	
			VSS_52	U14	
F_VREFC	K1	VREFC			
F_ZQ_A	J14	ZQ_A			
F_ZQ_B	K14	ZQ_B			
	G5	RFU_A/NC			
	M5	RFU_B/NC			

M1032794-001 BGA180

V_MEMIO

R322 2.37 KOHM 1% CH 201

R323 5.49 KOHM 1% CH 201

C1410 0.1 UF 10% 10 V EMPTY 201

V_DRAM1P8

R326 120 OHM 1% CH 402

R327 120 OHM 1% CH 402

V_DRAM1P8

C1411 10 UF 20% 6.3 V X5R 402

C1412 1 UF 20% 6.3 V X5R 201

C1413 1 UF 20% 6.3 V X5R 201

C1414 1 UF 20% 6.3 V X5R 201

C1415 1 UF 20% 6.3 V X5R 201

GDDR6_BASE

U1008 IC
GDDR6_SGRAM_180P
1 OF 2

12 IN	F1_CA0	H3	CA0_A		
12 IN	F1_CA1	G11	CA1_A		
12 IN	F1_CA2	G4	CA2_A		
12 IN	F1_CA3	H12	CA3_A		
12 IN	F1_CA4	H5	CA4_A		
12 IN	F1_CA5	H10	CA5_A		
12 IN	F1_CA6	J12	CA6_A		
12 IN	F1_CA7	J11	CA7_A		
12 IN	F1_CA8	J4	CA8_A		
12 IN	F1_CA9	J3	CA9_A		
12 IN	F0_CA0	L3	CA0_B		
12 IN	F0_CA1	M11	CA1_B		
12 IN	F0_CA2	M4	CA2_B		
12 IN	F0_CA3	L12	CA3_B		
12 IN	F0_CA4	L5	CA4_B		
12 IN	F0_CA5	L10	CA5_B		
12 IN	F0_CA6	K12	CA6_B		
12 IN	F0_CA7	K11	CA7_B		
12 IN	F0_CA8	K4	CA8_B		
12 IN	F0_CA9	K3	CA9_B		
12 IN	F1_CABI	J5	CABI_A_N		
12 IN	F0_CABI	K5	CABI_B_N		
12 IN	F1_CKE_N	G10	CKE_A_N		
12 IN	F0_CKE_N	M10	CKE_B_N		
12 IN	F_CK_P	J10	CK_P		
12 IN	F_CK_N	K10	CK_N		
12 IN	F1_WCK1_P	D11	WCK1_A_P/NC		
12 IN	F1_WCK1_N	D10	WCK1_A_N/NC		
12 IN	F0_WCK1_P	R11	WCK1_B_P		
12 IN	F0_WCK1_N	R10	WCK1_B_N		
12 IN	F1_WCK0_P	D4	WCK0_A_P		
12 IN	F1_WCK0_N	D5	WCK0_A_N		
12 IN	F0_WCK0_P	R4	WCK0_B_P/NC		
12 IN	F0_WCK0_N	R5	WCK0_B_N/NC		
57 28 27 26 25 23 22 21 20 19 BI	G6_TMS	F5	TMS		
23 BI	F_TDO	N10	TDO		
25 BI	G_TDO	F10	TDI		
57 28 27 26 25 23 22 21 20 19 BI	G6_TCK	N5	TCK		
12 IN F_DRAM_RESET		J1	RESET_N		
DQ0_A	B4	F1_DQ0		BI	12
DQ1_A	A3	F1_DQ1		BI	12
DQ2_A	B3	F1_DQ2		BI	12
DQ3_A	B2	F1_DQ3		BI	12
DQ4_A	E3	F1_DQ4		BI	12
DQ5_A	E2	F1_DQ5		BI	12
DQ6_A	F2	F1_DQ6		BI	12
DQ7_A	G2	F1_DQ7		BI	12
DQ8_A	B11	F1_DQ8		BI	12
DQ9_A	A12	F1_DQ9		BI	12
DQ10_A	B12	F1_DQ10		BI	12
DQ11_A	B13	F1_DQ11		BI	12
DQ12_A	E12	F1_DQ12		BI	12
DQ13_A	E13	F1_DQ13		BI	12
DQ14_A	F13	F1_DQ14		BI	12
DQ15_A	G13	F1_DQ15		BI	12
EDC0_A	C2	F1_EDC_0		OUT	12
EDC1_A	C13	F1_EDC_1		OUT	12
DBI0_A_N	D2	F1_DBI_0		BI	12
DBI1_A_N	D13	F1_DBI_1		BI	12
DQ0_B	U4	F0_DQ0		BI	12
DQ1_B	V3	F0_DQ1		BI	12
DQ2_B	U3	F0_DQ2		BI	12
DQ3_B	U2	F0_DQ3		BI	12
DQ4_B	P3	F0_DQ4		BI	12
DQ5_B	P2	F0_DQ5		BI	12
DQ6_B	N2	F0_DQ6		BI	12
DQ7_B	M2	F0_DQ7		BI	12
DQ8_B	U11	F0_DQ8		BI	12
DQ9_B	V12	F0_DQ9		BI	12
DQ10_B	U12	F0_DQ10		BI	12
DQ11_B	U13	F0_DQ11		BI	12
DQ12_B	P12	F0_DQ12		BI	12
DQ13_B	P13	F0_DQ13		BI	12
DQ14_B	N13	F0_DQ14		BI	12
DQ15_B	M13	F0_DQ15		BI	12
EDC0_B	T2	F0_EDC_0		OUT	12
EDC1_B	T13	F0_EDC_1		OUT	12
DBI0_B_N	R2	F0_DBI_0		BI	12
DBI1_B_N	R13	F0_DBI_1		BI	12

M1032794-001 BGA180

R685 4.99 KOHM 1% CH 201

R686 10 OHM 1% CH 201

C689 120 PF 5% 50 V C0G 201

R690 49.9 OHM 1% CH 201

CHANNEL F DECOUPLING

V_MEMIO: 2X22UF 0603 + 20X1UF 0201 PER CHANNEL

V_MEMIO

C444 C454 C459 C466 C477 C488 C495 C501 C539 C521
1 UF 20% 6.3 V X5R 201

V_MEMIO

C1765 22 UF 20% 6.3 V X5R 603

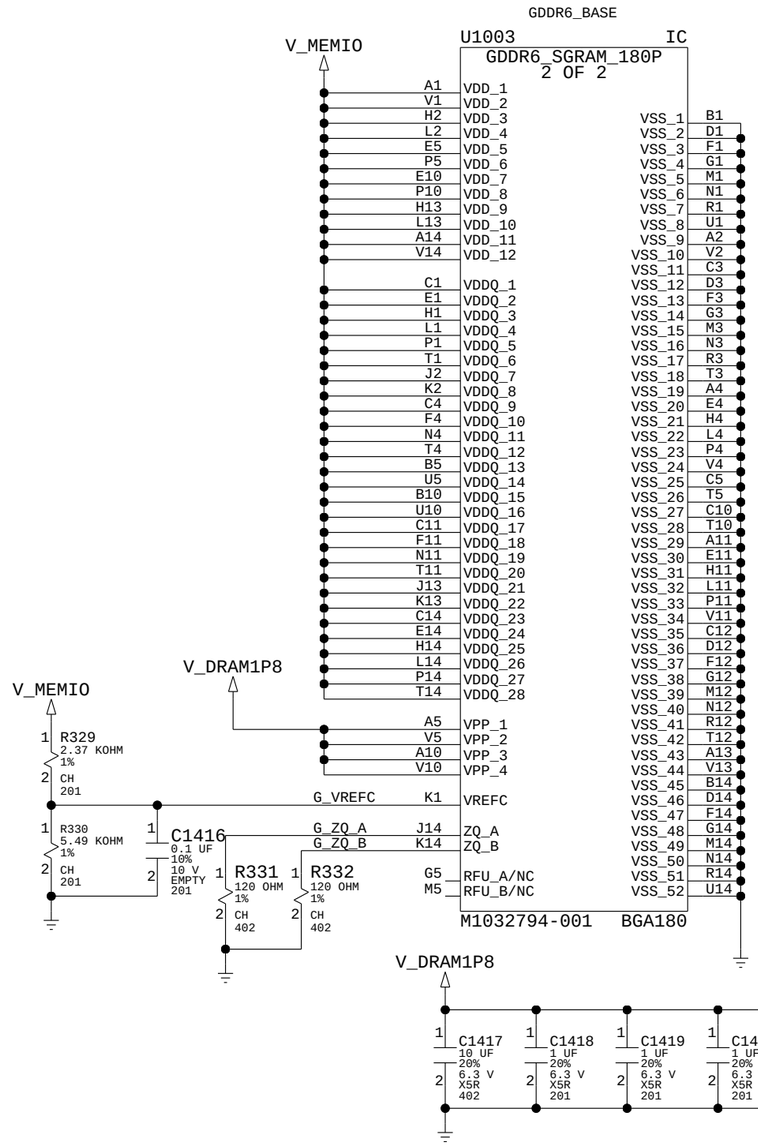
C435 22 UF 20% 6.3 V X5R 603

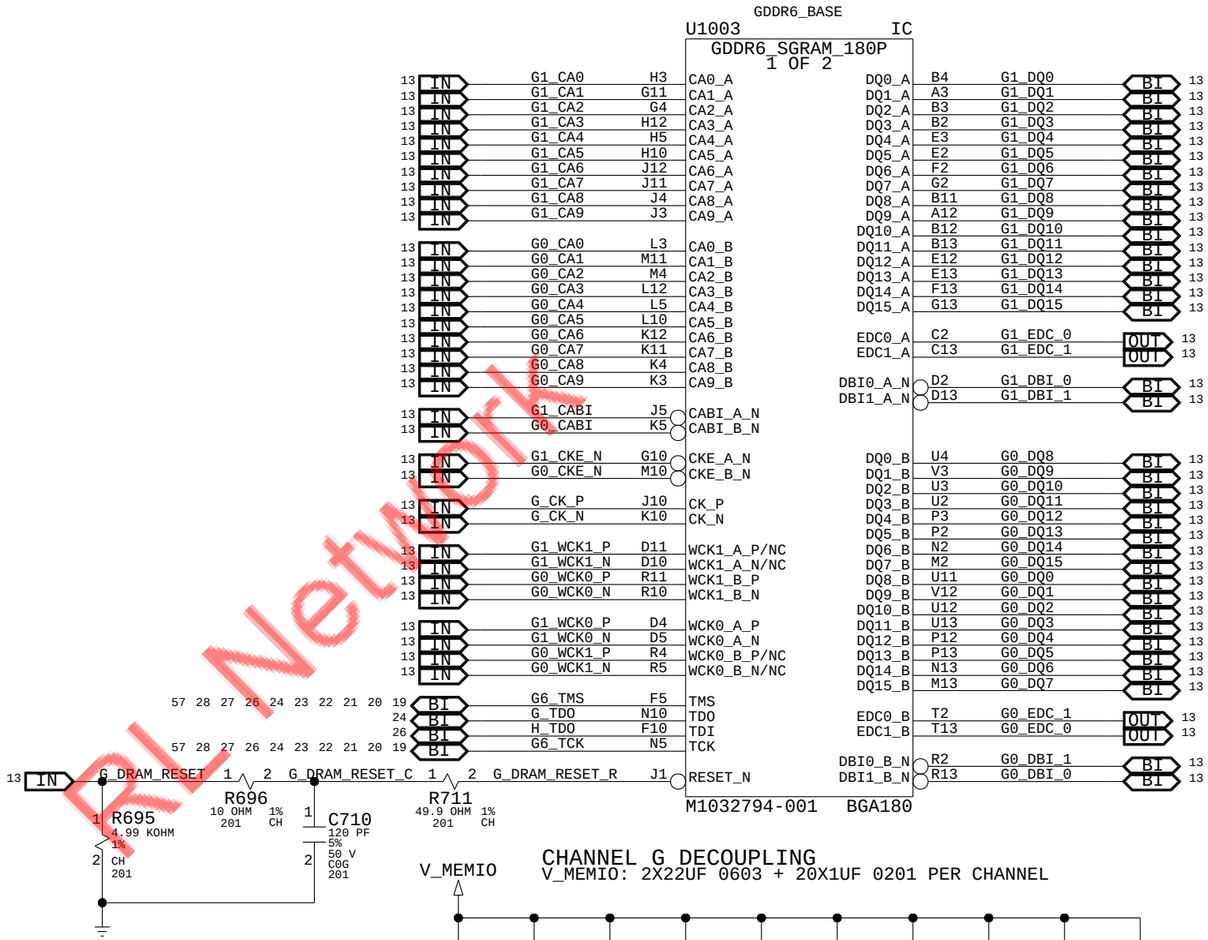
V_MEMIO

C737 C738 C471 C552 C585 C593 C619 C640 C1337 C1342
1 UF 20% 6.3 V X5R 201

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	24/59	24/59	E Retail	1.03

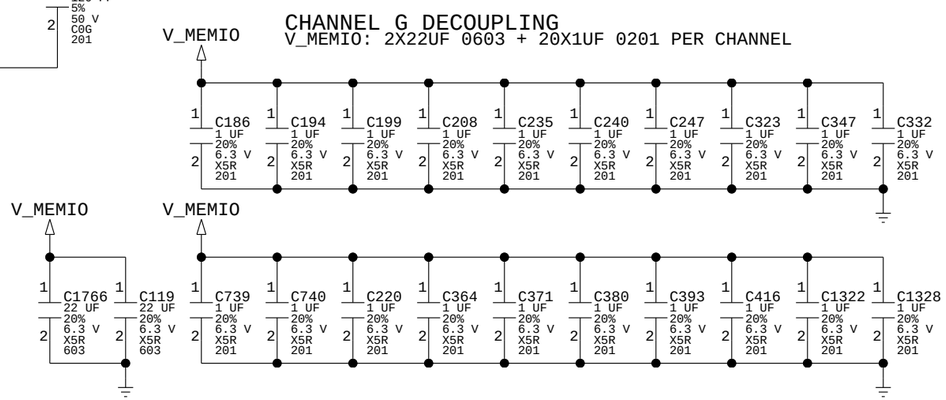
MEMORY: GDDR6 CHANNEL G: 16GB





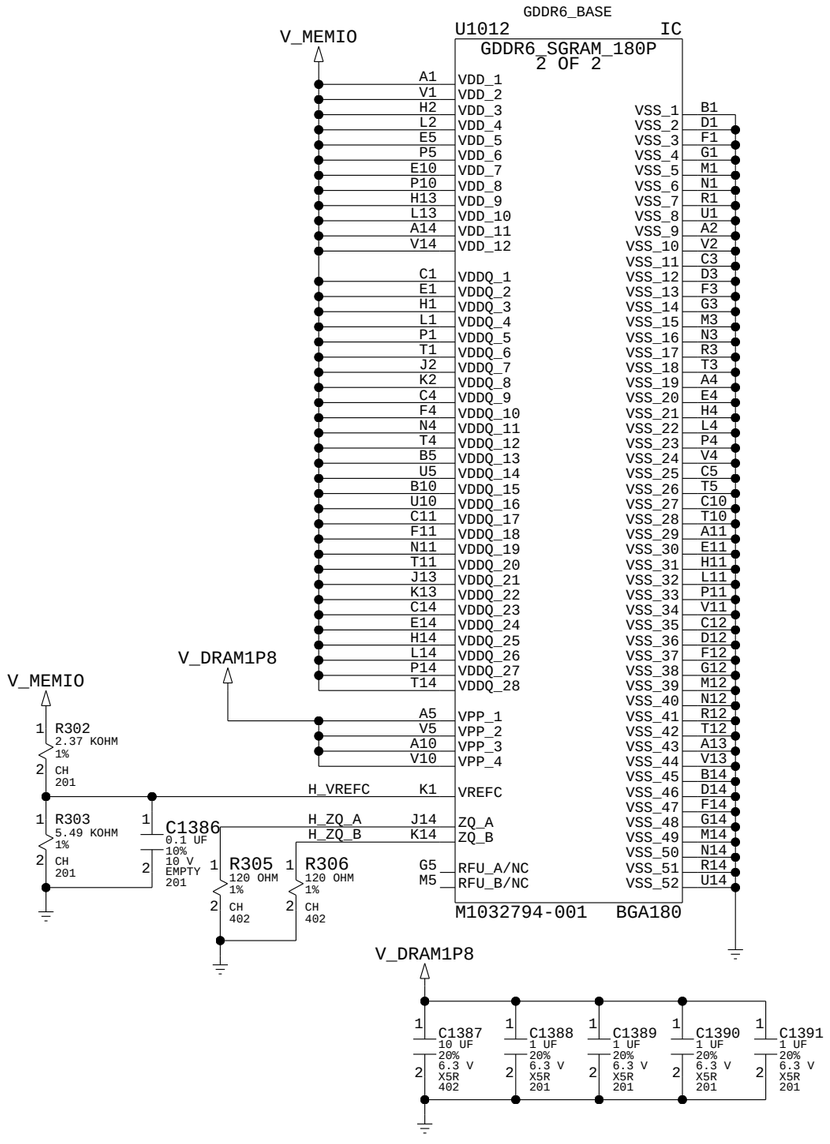
CHANNEL G DECOUPLING

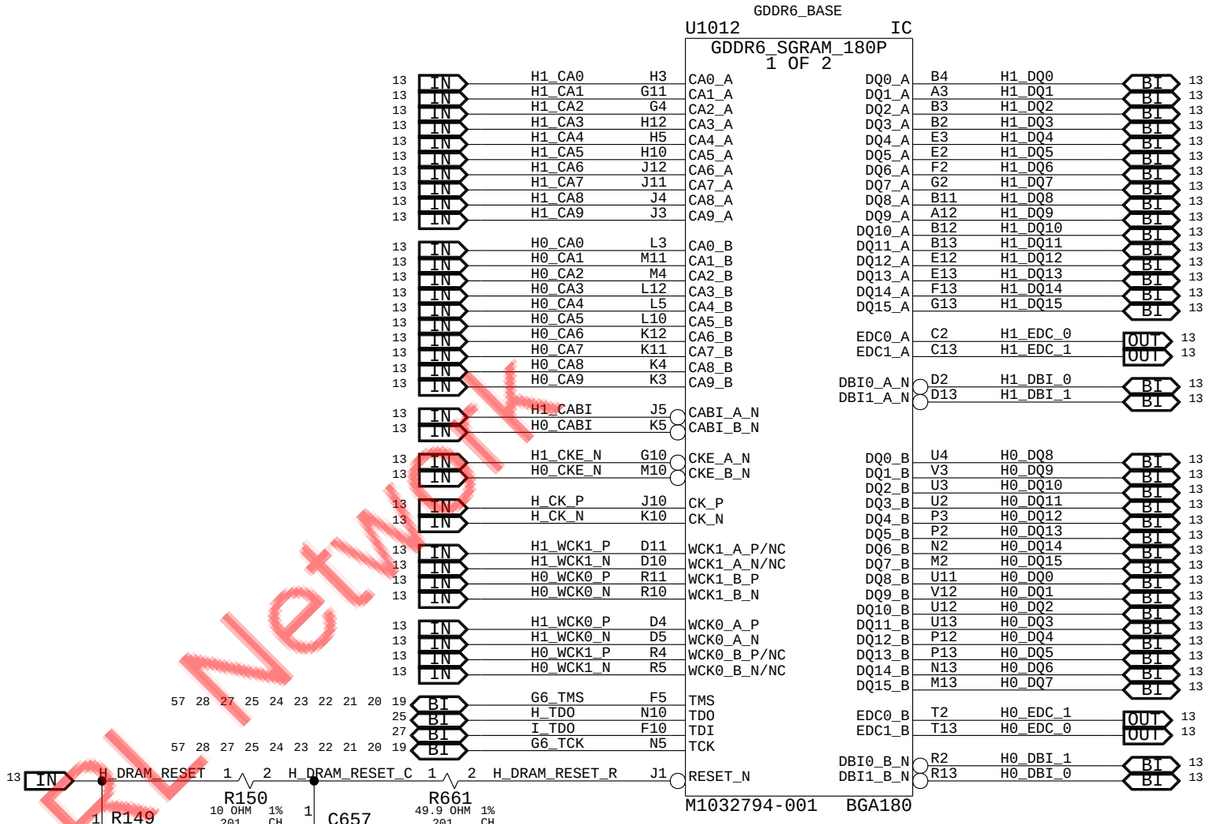
V_MEMIO: 2X22UF 0603 + 20X1UF 0201 PER CHANNEL



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	25/59	25/59	E Retail	1.03

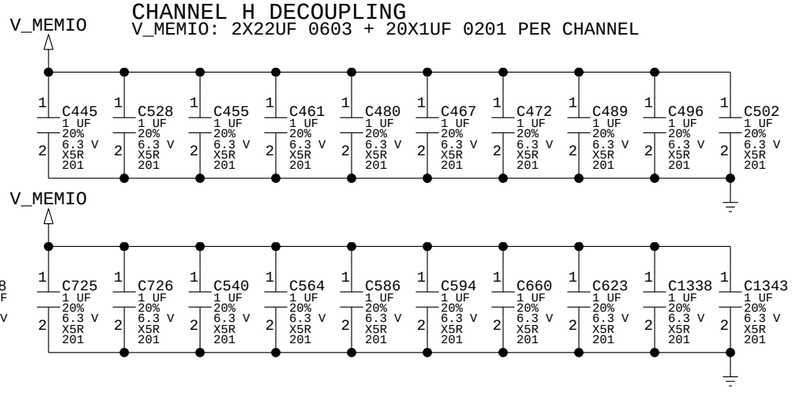
MEMORY: GDDR6 CHANNEL H: 8GB





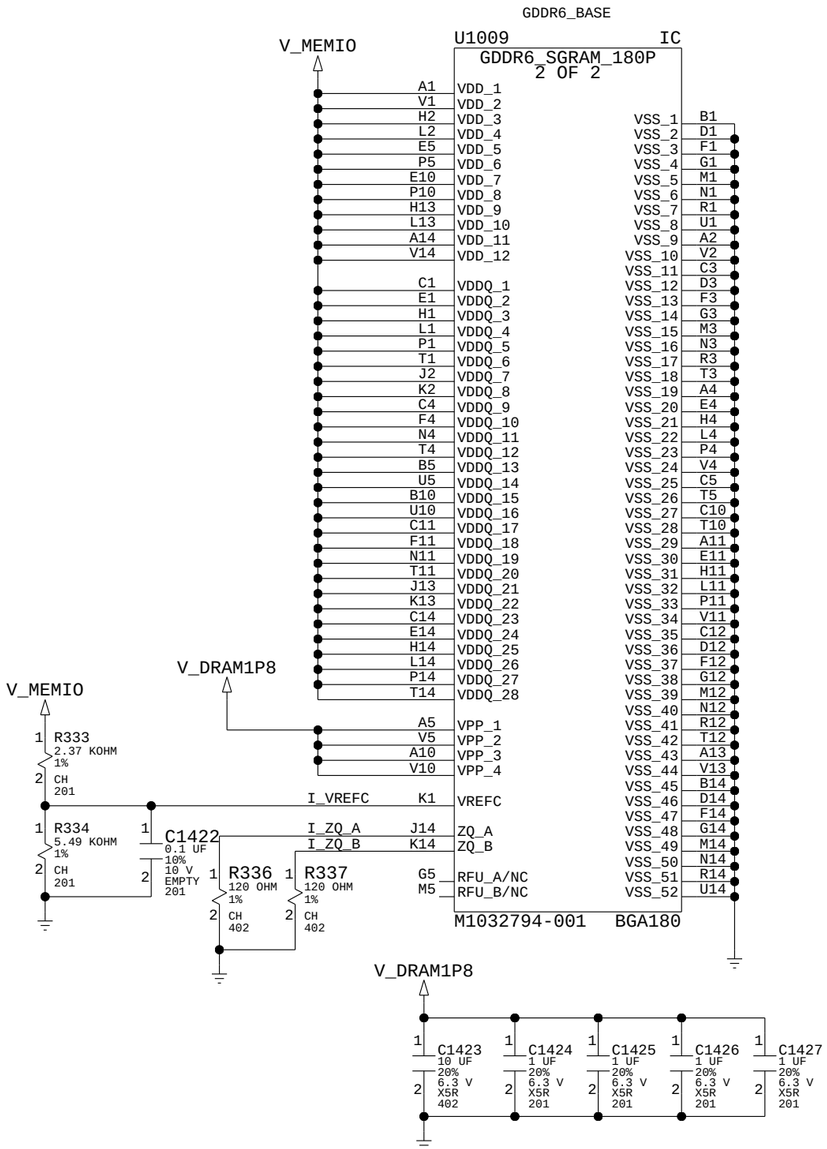
CHANNEL H DECOUPLING

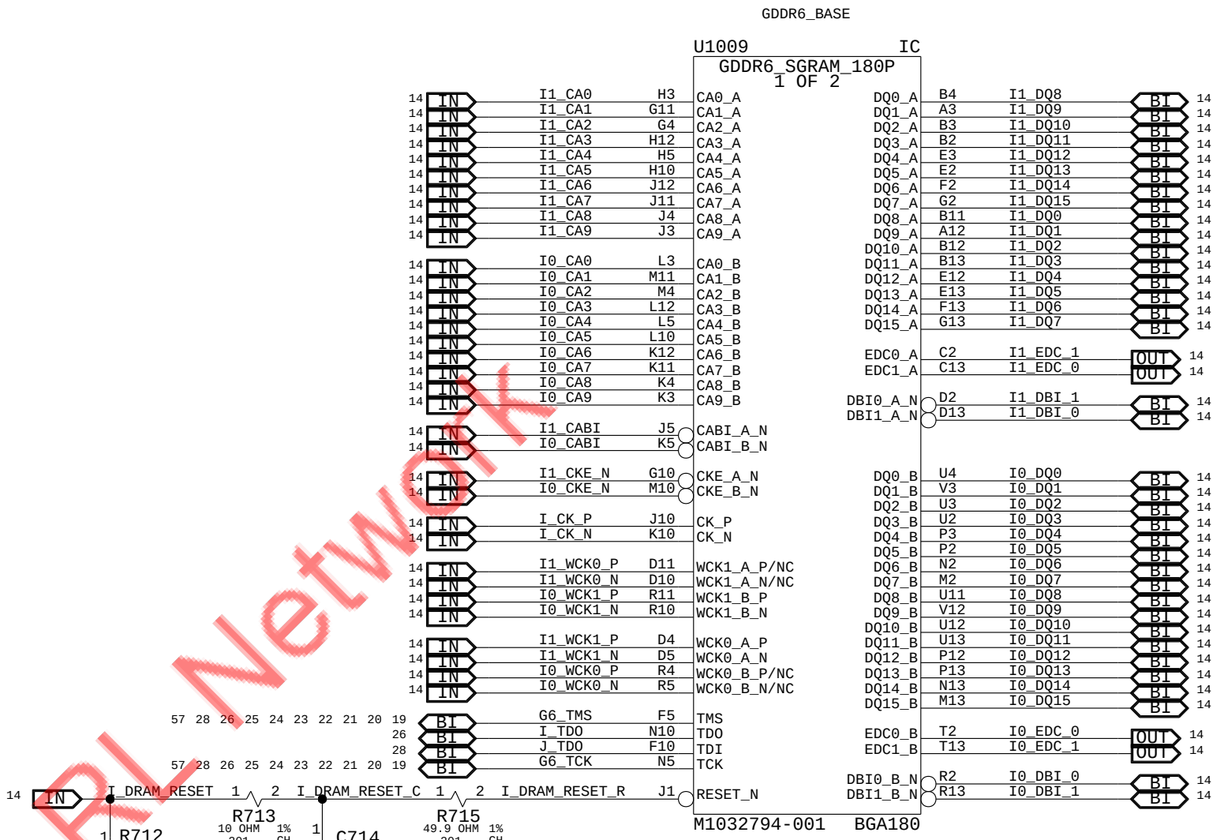
V_MEMIO: 2X22UF 0603 + 20X1UF 0201 PER CHANNEL

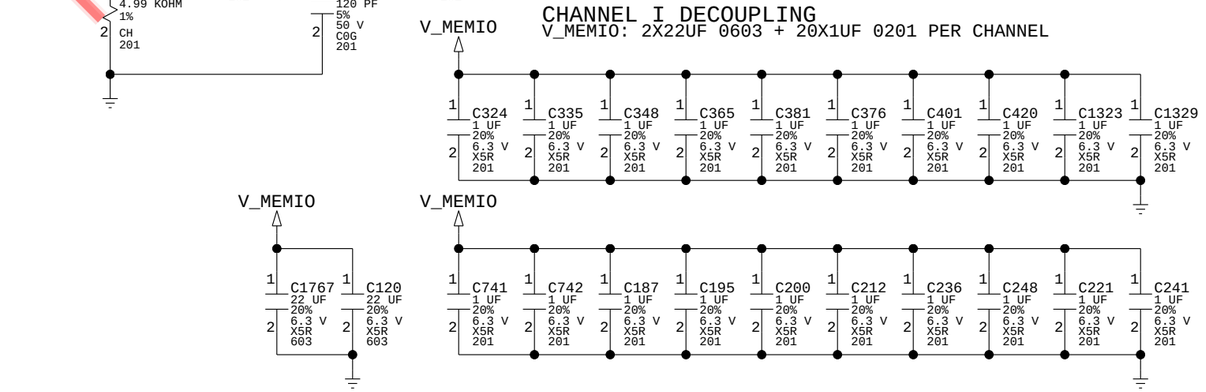


MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	26/59	26/59	E Retail	1.03

MEMORY: GDDR6 CHANNEL I: 16GB

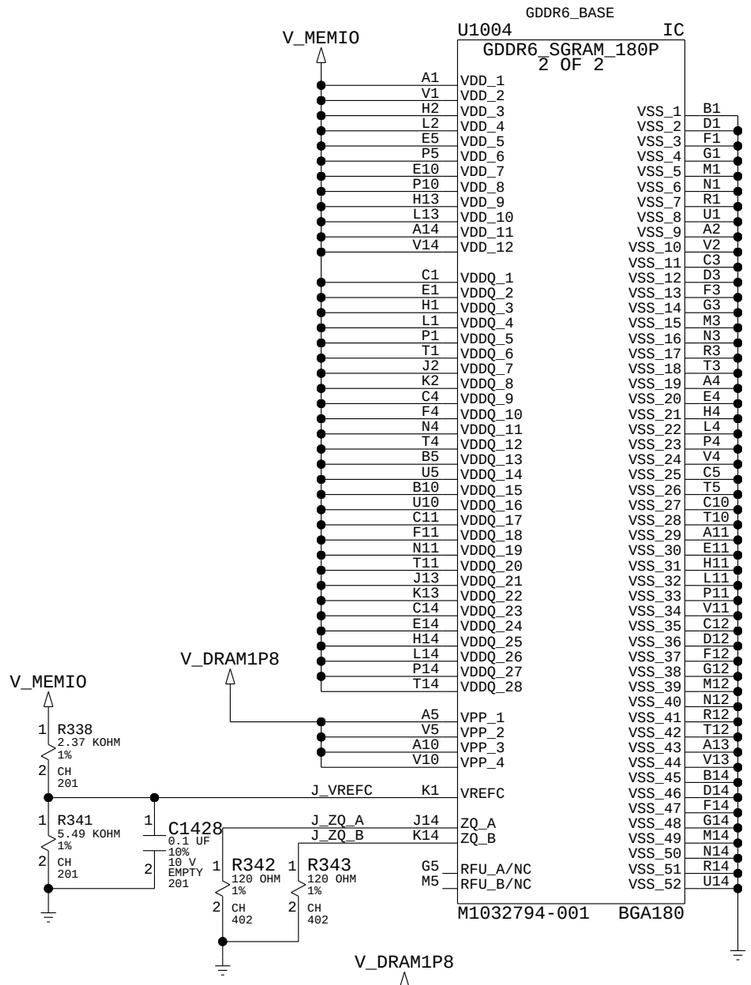


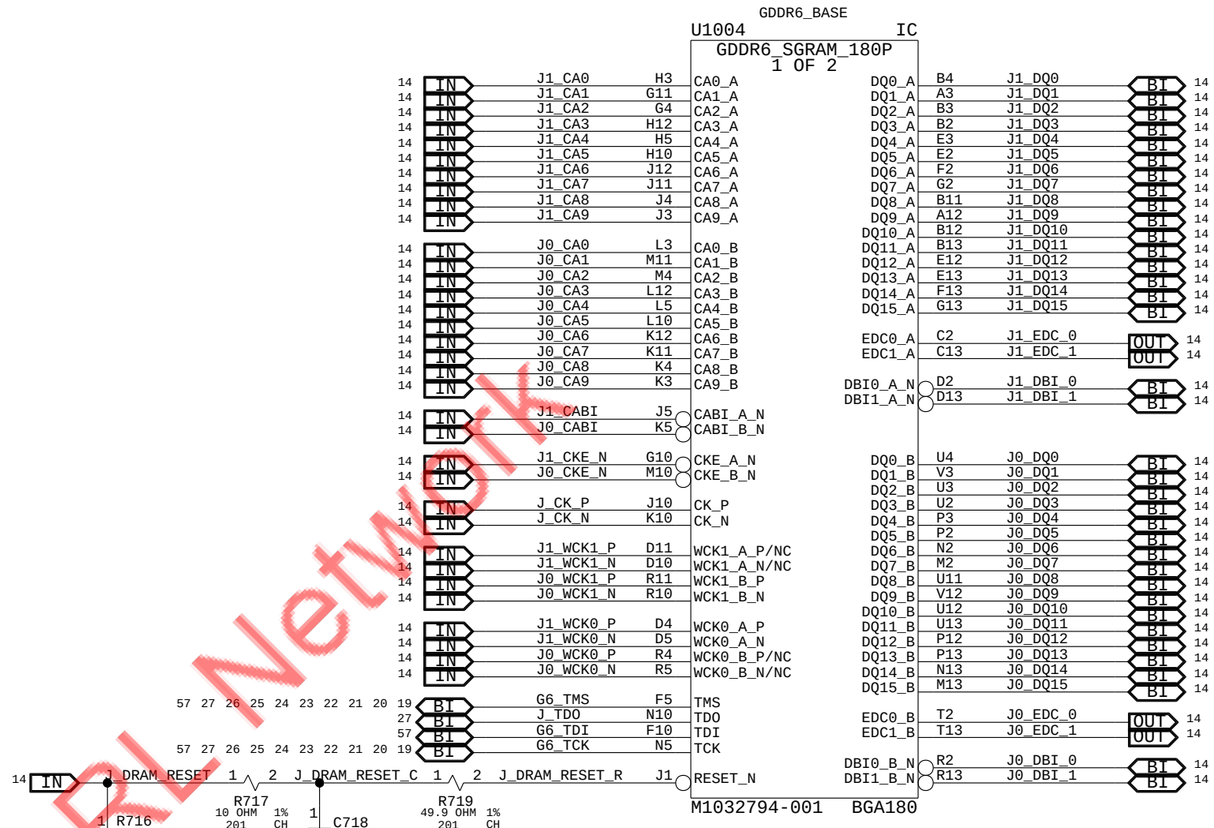


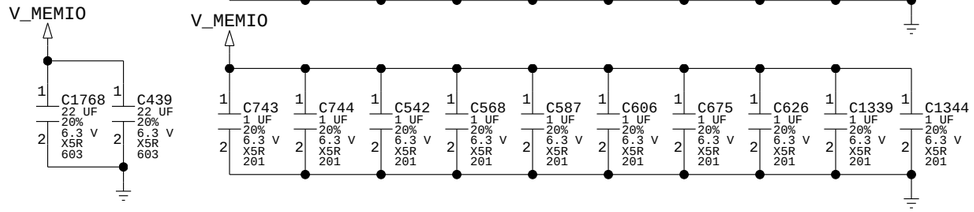


MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	27/59	27/59	E Retail	1.03

MEMORY: GDDR6 CHANNEL J: 8GB



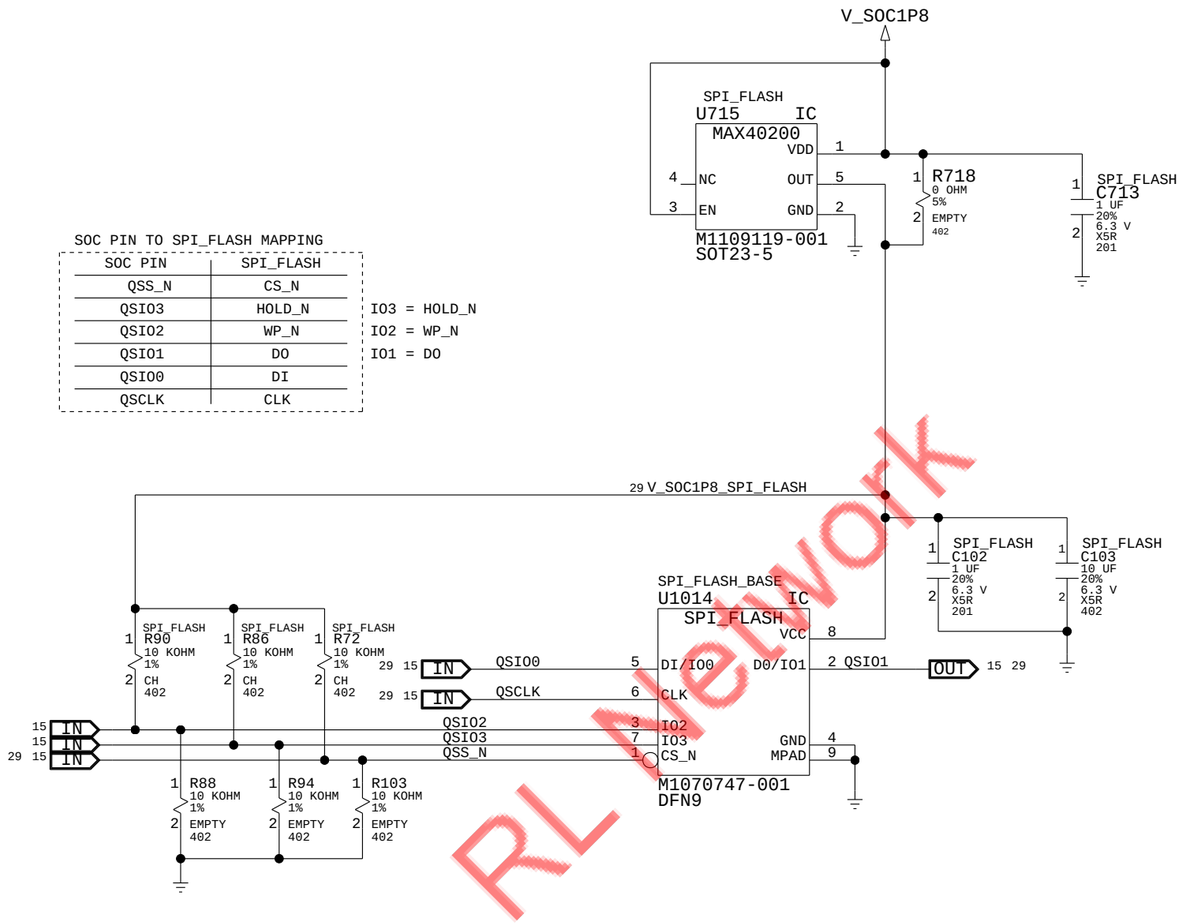




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	28/59	28/59	E Retail	1.03

MEMORY: SPI FLASH

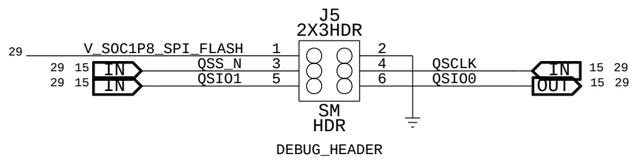
MAX40200 IDEAL DIODE PROVIDES BACKDRIVE PROTECTION FROM DEDIPROG



SOC PIN TO SPI_FLASH MAPPING

SOC PIN	SPI_FLASH
QSS_N	CS_N
QSIO3	HOLD_N
QSIO2	WP_N
QSIO1	DO
QSIO0	DI
QSCLK	CLK

IO3 = HOLD_N
IO2 = WP_N
IO1 = DO



DEBUG_HEADER

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1070747-001	IC	U1014	FLASH MEMORY,FLASH,256MBIT,SM,WSON8,SERIAL,W/DUAL/QUAD SPI	SPI_FLASH_WINBOND
M1104466-001	IC	U1014	FLASH MEMORY,FLASH,256MBIT,SM,8-WSON,SERIAL,MULTI I/O,DTR,1.8V	SPI_FLASH_MACRONIX

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	29/59	29/59	E Retail	1.03

HDMI: VIDEO OUT

Q621M CONTROL SLAVE ADDRESS		
ADDR0/ADDR1	7-BIT ADDRESS	8-BIT ADDRESS
FLOAT/FLOAT	0X5E	BC/BD

16 AVAILABLE OPTIONS (7-BIT): 0X50 - 0X5E
SEE DATASHEET FOR MORE DETAILS

V_3P3STBY_HDMI

C192 0.1 UF 20% 10% 16 V X5R 201
C703 0.1 UF 20% 10% 16 V X5R 201
C705 0.1 UF 20% 10% 16 V X5R 201
C707 0.1 UF 20% 10% 16 V X5R 201
C708 0.1 UF 20% 10% 16 V X5R 201
C709 0.1 UF 20% 10% 16 V X5R 201

C704 22 PF 2% 50 V NP0 201
C706 1000 PF 10% 50 V EMPTY 201
C267 0.01 UF 10% 16 V EMPTY 201
C475 10 UF 20% 6.3 V X5R 402
C479 22 UF 20% 6.3 V EMPTY 402

U40 IC
NB7NQ621M
3 OF 3
POWER
M1093444-002
QFN39

3	VCC	GND	6
9	VCC	GND	15
16	VCC	GND	25
22	VCC	GND	35
28	VCC	MPAD	39
34	VCC		

STRAP CONFIG: HIGH FLOAT FLOAT FLOAT LOW

V_3P3STBY_HDMI

R183 0 OHM 5% CH 402
R691 0 OHM 5% EMPTY 402
R693 0 OHM 5% EMPTY 402
R697 0 OHM 5% EMPTY 402
R699 0 OHM 5% EMPTY 402

R184 0 OHM 5% EMPTY 402
R692 0 OHM 5% EMPTY 402
R694 0 OHM 5% EMPTY 402
R698 0 OHM 5% EMPTY 402
R700 0 OHM 5% CH 402

U40 IC
NB7NQ621M
1 OF 3
CONTROL
M1093444-002
QFN39

OS/SCL	13	I2C_EN	18 HDMI_TX_RDRVR_I2C_EN
FG/SDA	12	EQ0/ADDR0	31 HDMI_TX_RDRVR_ADDR0
		EQ1/ADDR1	17 HDMI_TX_RDRVR_ADDR1
EN	36	MODE	37 HDMI_TX_RDRVR_MODE
		LANE_SWAP	14 HDMI_TX_RDRVR_LANE_SWAP

57 52 44 38 32 IN SMBUS_CLK — R28 0 OHM 5% CH 402 — HDMI_TX_RDRVR_SCL_CTL
57 52 44 38 32 BI SMBUS_DATA — R29 0 OHM 5% CH 402 — HDMI_TX_RDRVR_SDA_CTL
32 IN HDMI_TX_RDRVR_EN_R — R30 0 OHM 5% CH 402 — HDMI_TX_RDRVR_EN
FT15 FTP

HDMI_TX_RDRVR_EN — R31 10 KOHM 1% CH 402 — C39 0.1 UF 10% 16 V EMPTY 201

U40 IC
NB7NQ621M
2 OF 3
HDMI

A_RXP	1	A_TXP	30
A_RXN	2	A_TXN	29
B_RXP	4	B_TXP	27
B_RXN	5	B_TXN	26
C_RXP	7	C_TXP	24
C_RXN	8	C_TXN	23
D_RXP	10	D_TXP	21
D_RXN	11	D_TXN	20
AUXP		AUXP	33 NC
AUXN		AUXN	32 NC
NC 38 HPD_SRC		HPD_SNK	19

M1093444-002
QFN39

3 IN TMDS_TX_DP2 — C52 0.1 UF 10% 16 V X5R 201 — TMDS_TX_DP2_C
3 IN TMDS_TX_DN2 — C49 0.1 UF 10% 16 V X5R 201 — TMDS_TX_DN2_C
3 IN TMDS_TX_DP1 — C57 0.1 UF 10% 16 V X5R 201 — TMDS_TX_DP1_C
3 IN TMDS_TX_DN1 — C55 0.1 UF 10% 16 V X5R 201 — TMDS_TX_DN1_C
3 IN TMDS_TX_DP0 — C38 0.1 UF 10% 16 V X5R 201 — TMDS_TX_DP0_C
3 IN TMDS_TX_DN0 — C36 0.1 UF 10% 16 V X5R 201 — TMDS_TX_DN0_C
3 IN TMDS_TX_CLKP — C45 0.1 UF 10% 16 V X5R 201 — TMDS_TX_CLKP_C
3 IN TMDS_TX_CLKN — C42 0.1 UF 10% 16 V X5R 201 — TMDS_TX_CLKN_C

EG688 DIO SM M1015860-001
EG690 DIO SM M1015860-001
EG696 DIO SM M1015860-001
EG702 DIO SM M1015860-001
EG41 DIO SM M1015860-001
EG689 DIO SM M1015860-001
EG695 DIO SM M1015860-001
EG701 DIO SM M1015860-001

HDMI_TX_RDRVR_HPD

R178 0 OHM 5% CH 402

V_3P3STBY_SOC V_5P0

C25 4.7 UF 20% 10 V X5R 402
C478 0.1 UF 10% 16 V X5R 201

V_3P3STBY_SOC

R50 2 KOHM 1% CH 402
R54 2 KOHM 1% CH 402

3 OUT DP0_HPD

32 IN SB_DDC_CLK — R52 0 OHM 5% CH 402
32 BI SB_DDC_DATA — R51 0 OHM 5% CH 402
3 BI SOC_DDC_CLK — C24 0.1 UF 10% 16 V X5R 201 — SOC_AUXP
3 BI SOC_DDC_DATA — C15 0.1 UF 10% 16 V X5R 201 — SOC_AUXN

32 OUT DP0_HPD_SB — R382 0 OHM 5% CH 402
32 IN HDMIDPOUT_MODE_SEL
32 IN HDMI_V_5P0_EN
FT6 FTP
R48 10 KOHM 1% CH 402
R148 10 KOHM 1% CH 402

U21 IC
HDMIDP1_5F6
M1004155-003
WLCSP18

C4	VDD_5V	CEC	E1
C3	VDD_IC		
HDMI_TX_SCL_R E5	R_SCL_IC	SCL	D2
HDMI_TX_SDA_R D5	R_SDA_IC	SDA	C1
D4	AUX_P	5V_OUT	A3
E4	SCL_IC		
D3	AUX_N		
E2	SDA_IC		
	HPD_IC	HPD	A1
B5			
A2	SELECT_IC	GND	B1
A5	ENABLE_IC	GND	C2

HDMI 5V LOAD SWITCH: 5V, 250MA MAX TDC
DP PWR LOAD SWITCH: 3.3V, 500MA MAX TDC

C14 2.2 UF 20% 6.3 V X5R 201

32 BI
32 OUT
EG24 X882235-001 DIO 402

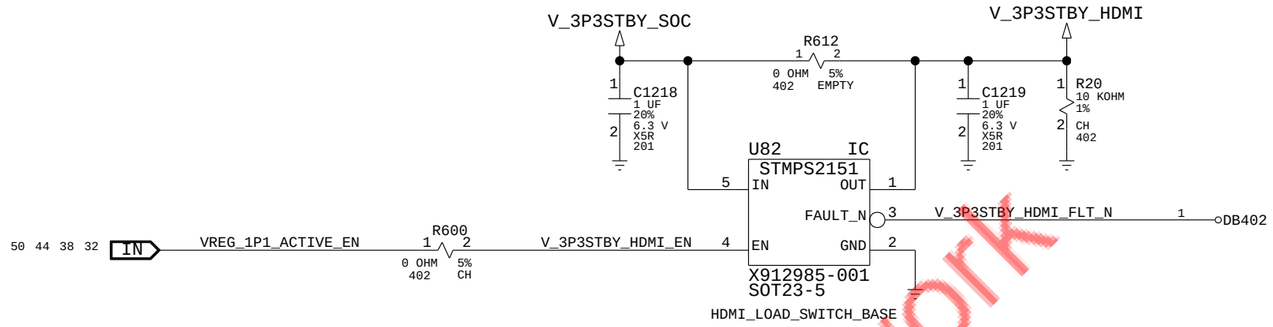
HDMI_TX_SCL_BUF — R19 0 OHM 5% CH 402
HDMI_TX_SDA_BUF — R18 0 OHM 5% CH 402

J2 CONN
HDMI_19P_10MH
M1087810-001 SM

TMDS_TX_DP2_CONN	1	TMDS_DATA2_DP	
	2	TMDS_DATA2_SHD	
TMDS_TX_DN2_CONN	3	TMDS_DATA2_DN	
TMDS_TX_DP1_CONN	4	TMDS_DATA1_DP	
	5	TMDS_DATA1_SHD	
TMDS_TX_DN1_CONN	6	TMDS_DATA1_DN	
TMDS_TX_DP0_CONN	7	TMDS_DATA0_DP	
	8	TMDS_DATA0_SHD	
TMDS_TX_DN0_CONN	9	TMDS_DATA0_DN	
TMDS_TX_CLKP_CONN	10	TMDS_CLK_DP	MT1 20
	11	TMDS_CLK_SHD	MT2 21
TMDS_TX_CLKN_CONN	12	TMDS_CLK_DN	MT3 22
HDMI_CEC	13	CEC	MT4 23
HDMIDPOUT_MODE_DET	14	UTILITY	MT5 24
HDMI_TX_SCL_CONN	15	SCL	MT6 25
HDMI_TX_SDA_CONN	16	SDA	MT7 26
	17	DDC/CEC_GND	MT8 27
V_5P0_HDMI_OUT	18	+5V_POWER	MT9 28
HDMI_TX_HPD_CONN	19	HOT_PLUG_DET	MT10 29

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	30/59	30/59	E Retail	1.03

HDMI: LOAD SWITCHES

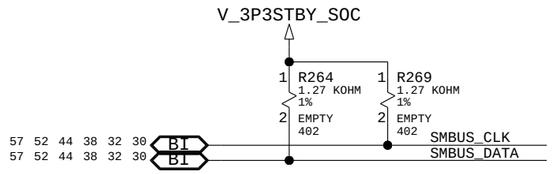


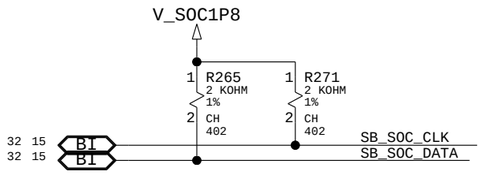
U82 IS MITIGATION FOR HDMI TMDS BACK-DRIVE CURRENT THROUGH Q621M RE-DRIVER

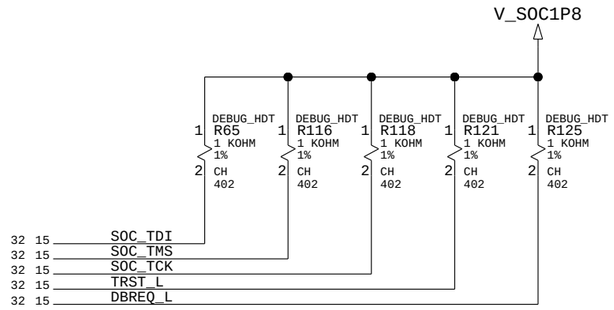
MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
X912985-001	IC	U82	IC,SM,SOT23-5,STMPS2151STR,PWR SW,1CH,0.5A	HDMI_LOAD_SWITCH_ST
X862402-001	IC	U82	IC,SM,SOT23-5,TPS2065DBVR,HI SIDE SW,1.5A	HDMI_LOAD_SWITCH_TI
X934019-001	IC	U82	IC,SM,SOT23-5,AP2151D,PWR SW,1CH,0.5A,DIODES QUAL	HDMI_LOAD_SWITCH_DIODES

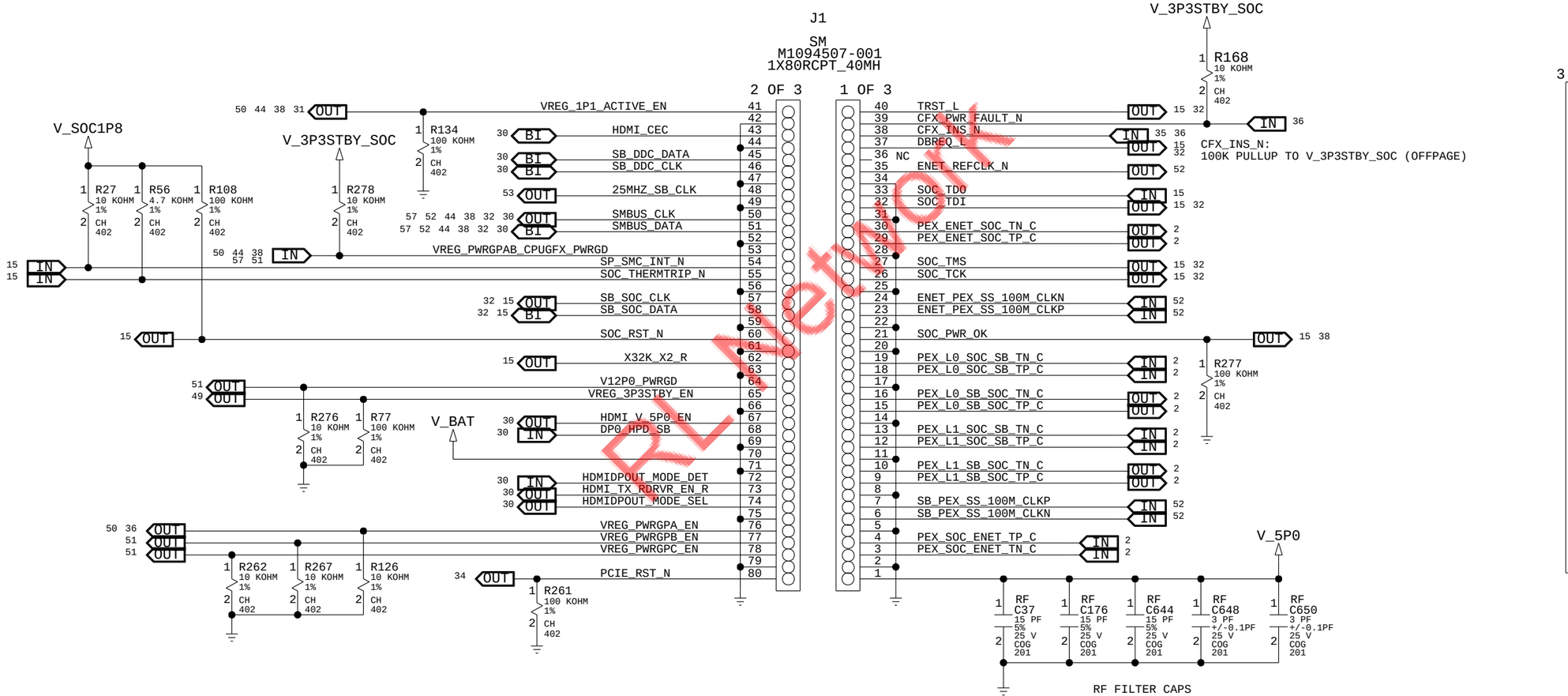
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	31/59	31/59	E Retail	1.03

CONN: BOARD TO BOARD





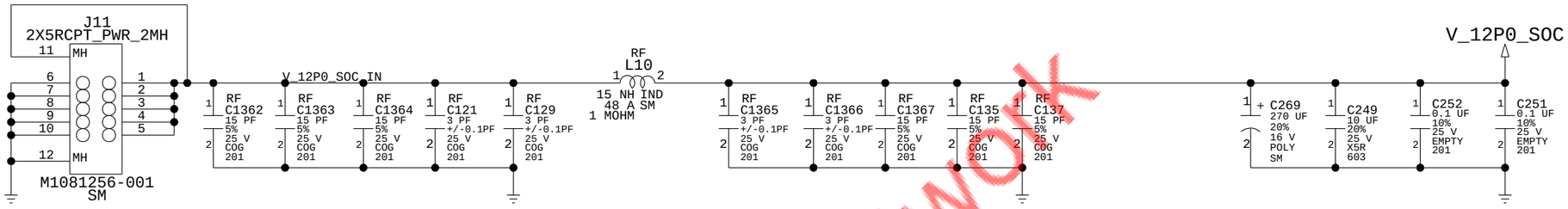




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	32/59	32/59	E Retail	1.03

CONN: POWER

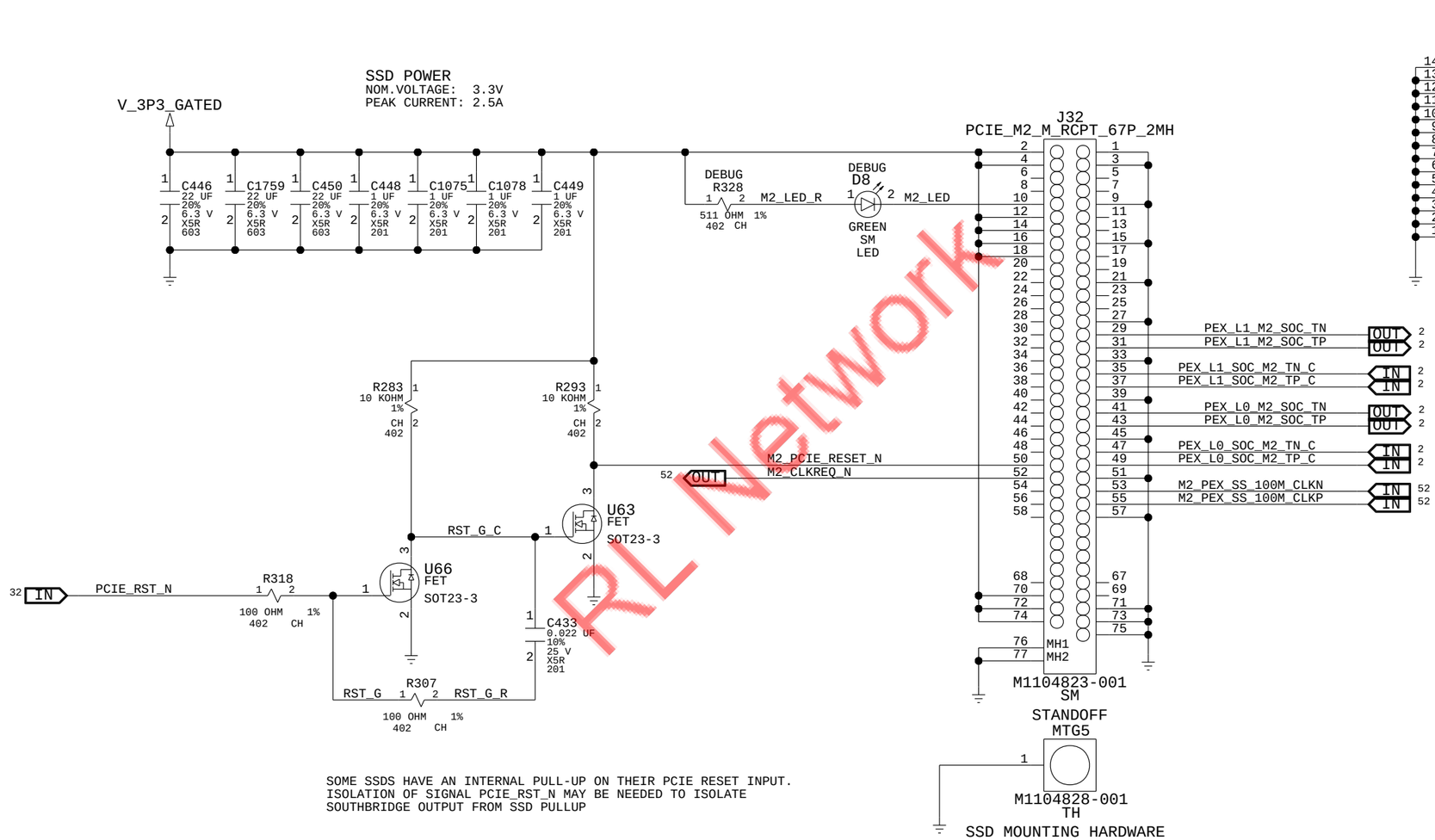
CRITICAL NOTE:
THE RF BOM STUFFING OPTION
SHOULD BE USED BY DEFAULT
NON-RF BOM CONFIGURATIONS WILL REQUIRE
INDUCTOR L10 TO BE PHYSICALLY SHORTED



J11.11 CONNECTED TO V_12P0_IN TO AVOID CUTTING 12V PLANE

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	33/59	33/59	E Retail	1.03

CONN: M.2



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	34/59	34/59	E Retail	1.03

CONN: SPDIF, CFEXPRESS

CFX_PERST_N DRIVEN BY GPIO FROM MP2926
NCP803 RESET SUPERVISOR FOOTPRINT LEFT IN DESIGN AS BACKUP

V_3P3_CFX
EMPTY
U132
NCP803
VCC
RESET_N
GND
M1095945-001
SOT23-3
C131
0.1 UF
10%
10 V
EMPTY
201
CFX_PERST_MONITOR_N
R154
0 OHM 5%
402 EMPTY
R104
10 KOHM
1%
CH
402
R209
100 KOHM 1%
402 EMPTY
44 IN CFX_PERST_GPIO_N
R175
0 OHM 5%
402 CH

35 OUT PEX_L1_CFX_SOC_TP
35 OUT PEX_L1_CFX_SOC_TN
35 IN PEX_L1_SOC_CFX_TP_C
35 IN PEX_L1_SOC_CFX_TN_C

CFEXPRESS
2.5A EDC
1.55A TDC

J3 CONN
CF_EXPRESS
1 GND
2 PER1_N
3 PER1_P
4 GND
5 PET1_N
6 PET1_P
7 RESERVED
8 RESERVED
9 PERST_N
10 +3.3V
11 CLKREQ_N
12 INS_N
13 REFCLK-
14 REFCLK+
15 GND
16 PER0_N
17 PER0_P
18 GND
19 PET0_N
20 PET0_P
21 GND
22 MH1
23 MH2
24 MH3
25 MH4
26 MH5
27 MH6
28 MH7
29 MH8
30 MH9
31 MH10
32 MH11
MH12 33
MH13 34
MH14 35
MH15 36
MH16 37
MH17 38
MH18 39
MH19 40
MH20 41
MH21 42
MH22 43
MH23 44
MH24 45
MH25 46
MH26 47
MH27 48
MH28 49
MH29 50
MH30 51
MH31 52
MH32 53
MH33 54
MH34 55
MH35 56
MH36 57
MH37 58
MH38 59
MH39 60
MH40 61
MH41 62
MH42 63
MH43 64
M1097401-003
SM

R106
0 OHM 5%
402 CH
CFX_RSV1
35 CFX_PERST_N
52 35 OUT CFX_CLKREQ_N
OUT CFX_INS_N
52 35 IN CFX_PEX_SS_100M_CLKN
52 35 IN CFX_PEX_SS_100M_CLKP
35 2 OUT PEX_L0_CFX_SOC_TN
35 2 OUT PEX_L0_CFX_SOC_TP
35 2 IN PEX_L0_SOC_CFX_TN_C
35 2 IN PEX_L0_SOC_CFX_TP_C

V_3P3_CFX
C1444 22 UF 20% 6.3 V X5R 603
C1758 22 UF 20% 6.3 V X5R 603
C752 10 UF 20% 6.3 V X5R 402
C750 1 UF 20% 6.3 V X5R 201

32 36 OUT
DB18
EG86
EMPTY
SM
M1015860-001

NOTE:
THE FOLLOWING SIGNALS HAVE BEEN POLARITY
SWAPPED AT THE CFX CONNECTOR
PINS 2,3: PEX_L1_CFX_SOC
PINS 5,6: PEX_L1_SOC_CFX

35 CFX_PERST_N
52 35 CFX_CLKREQ_N
EG2
EG6
EMPTY SM M1015860-001
EMPTY SM M1015860-001

35 2 PEX_L1_SOC_CFX_TN_C
35 2 PEX_L1_SOC_CFX_TP_C
EG7
EG12
EMPTY SM M1015860-001
EMPTY SM M1015860-001

35 2 PEX_L1_CFX_SOC_TN
35 2 PEX_L1_CFX_SOC_TP
EG8
EG13
EMPTY SM M1015860-001
EMPTY SM M1015860-001

52 35 CFX_PEX_SS_100M_CLKN
52 35 CFX_PEX_SS_100M_CLKP
EG9
EG14
EMPTY SM M1015860-001
EMPTY SM M1015860-001

35 2 PEX_L0_SOC_CFX_TN_C
35 2 PEX_L0_SOC_CFX_TP_C
EG10
EG15
EMPTY SM M1015860-001
EMPTY SM M1015860-001

35 2 PEX_L0_CFX_SOC_TN
35 2 PEX_L0_CFX_SOC_TP
EG11
EG16
EMPTY SM M1015860-001
EMPTY SM M1015860-001

V_3P3_CFX
RF FILTER CAPS
RF C651 15 PF 5% 25 V COG 201
RF C652 15 PF 5% 25 V COG 201
RF C653 15 PF 5% 25 V COG 201
RF C654 3 PF +/-0.1PF 25 V COG 201
RF C655 3 PF +/-0.1PF 25 V COG 201

V_3P3_GATED
R164
1 KOHM
1%
CH
402
3 OUT SPDIF_DETECT
Q166
FET
SOT23-3
1 SPDIF_DETECT_N_R
R165
0 OHM 5%
402 EMPTY

V_3P3_GATED
R644
100 KOHM
1%
CH
402
R643
1 KOHM 1% CH
402
SPDIF_DETECT_N
C646
0.1 UF
10%
10 V
X5R
201
EG1
X882235-001
DIO
402
C647
22 PF
2%
50 V
NP0
201
3 IN SPDIF_OUT
EG5
X882235-001
EMPTY
402
C8
22 PF
2%
50 V
NP0
201

V_3P3_GATED
C1268 1 UF 20% 6.3 V X5R 201
C1269 10 UF 20% 6.3 V X5R 402

J7 CONN
SPDIF_4P_10MH
VCC
DETECT
VIN
GND
MH 5
MH 6
MH 7
MH 8
MH 9
MH 10
MH 11
MH 12
MH 13
MH 14
M1087812-001
TH

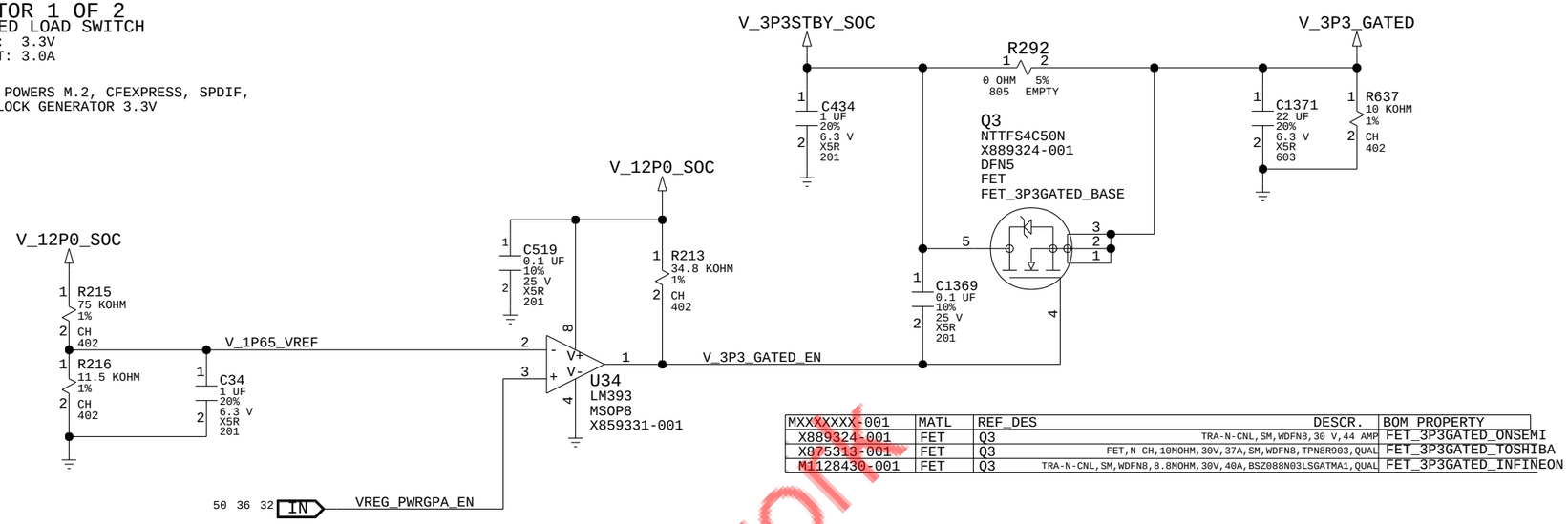
Q166 PROVIDES LOGIC INVERSION
SPDIF DETECT IS ACTIVE LOW
SOC REQUIRES ACTIVE HIGH

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	35/59	35/59	E Retail	1.03

VREGS: V_3P3_GATED, V_3P3_CFX

COMPARATOR 1 OF 2
V_3P3_GATED LOAD SWITCH
NOM.VOLTAGE: 3.3V
PEAK CURRENT: 3.0A

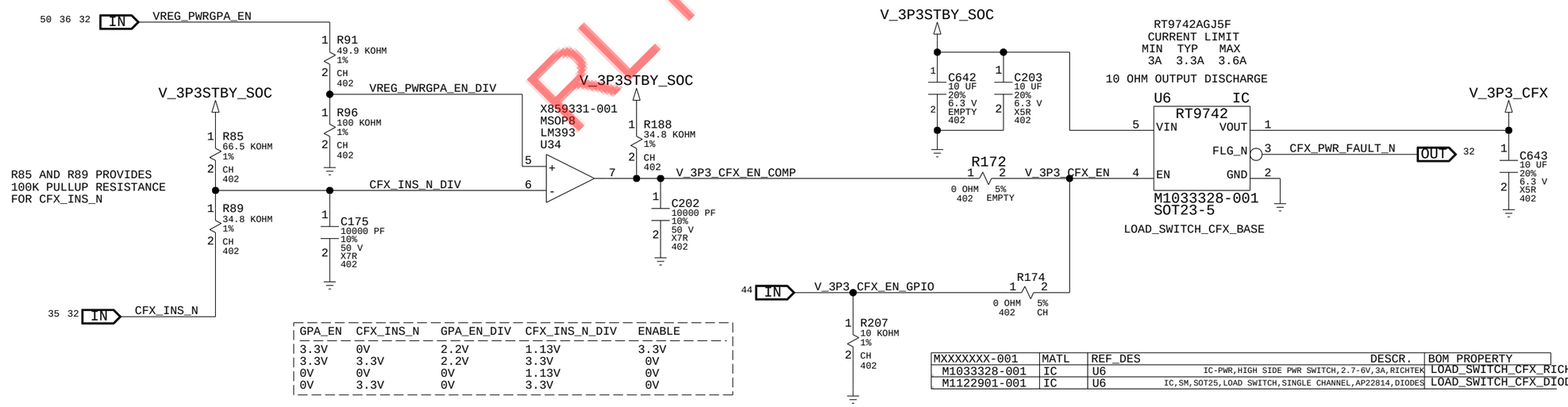
V_3P3_GATED POWERS M.2, CFEXPRESS, SPDIF,
SOC VDD3, CLOCK GENERATOR 3.3V



MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
X889324-001	FET	Q3	TRA-N-CNL,SM,WDFN8,30 V,44 AMP	FET_3P3GATED_ONSEMI
X875313-001	FET	Q3	FET,N-CH,10MOHM,30V,37A,SM,WDFN8,TPN8R903,QUAL	FET_3P3GATED_TOSHIBA
M1128430-001	FET	Q3	TRA-N-CNL,SM,WDFN8,8.8MOHM,30V,40A,BSZ088N03LSGATMA1,QUAL	FET_3P3GATED_INFINEON

COMPARATOR 2 OF 2
V_3P3_CFX LOAD SWITCH
NOM.VOLTAGE: 3.3V
EDC: 2.5A
TDC: 1.5A

V_3P3_CFX_EN DRIVEN VIA GPIO FROM MP2926
COMPARATOR CIRCUIT LEFT IN AS BACKUP



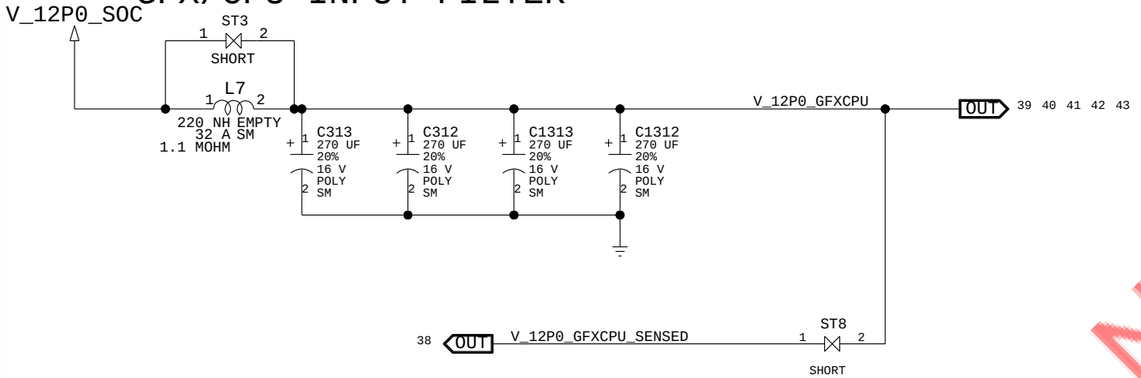
GPA_EN	CFX_INS_N	GPA_EN_DIV	CFX_INS_N_DIV	ENABLE
3.3V	0V	2.2V	1.13V	3.3V
3.3V	3.3V	2.2V	3.3V	0V
0V	0V	0V	1.13V	0V
0V	3.3V	0V	3.3V	0V

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1033328-001	IC	U6	IC-PWR,HIGH SIDE PWR SWITCH,2.7-6V,3A,RICHTEK	LOAD_SWITCH_CFX_RICHTEK
M1122901-001	IC	U6	IC,SM,SOT25,LOAD SWITCH,SINGLE CHANNEL,AP22814,DIODES	LOAD_SWITCH_CFX_DIODES

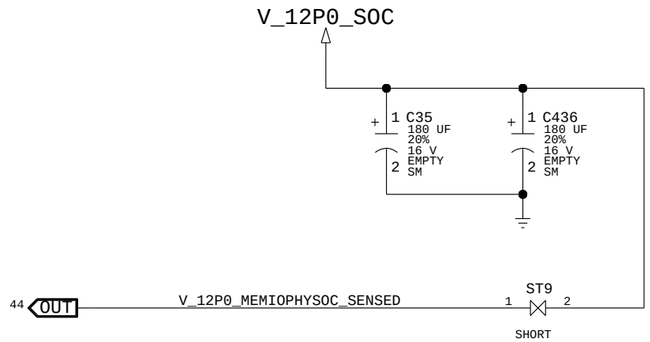
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	36/59	36/59	E Retail	1.03

VREGS: INPUT FILTERS

GFX/CPU INPUT FILTER

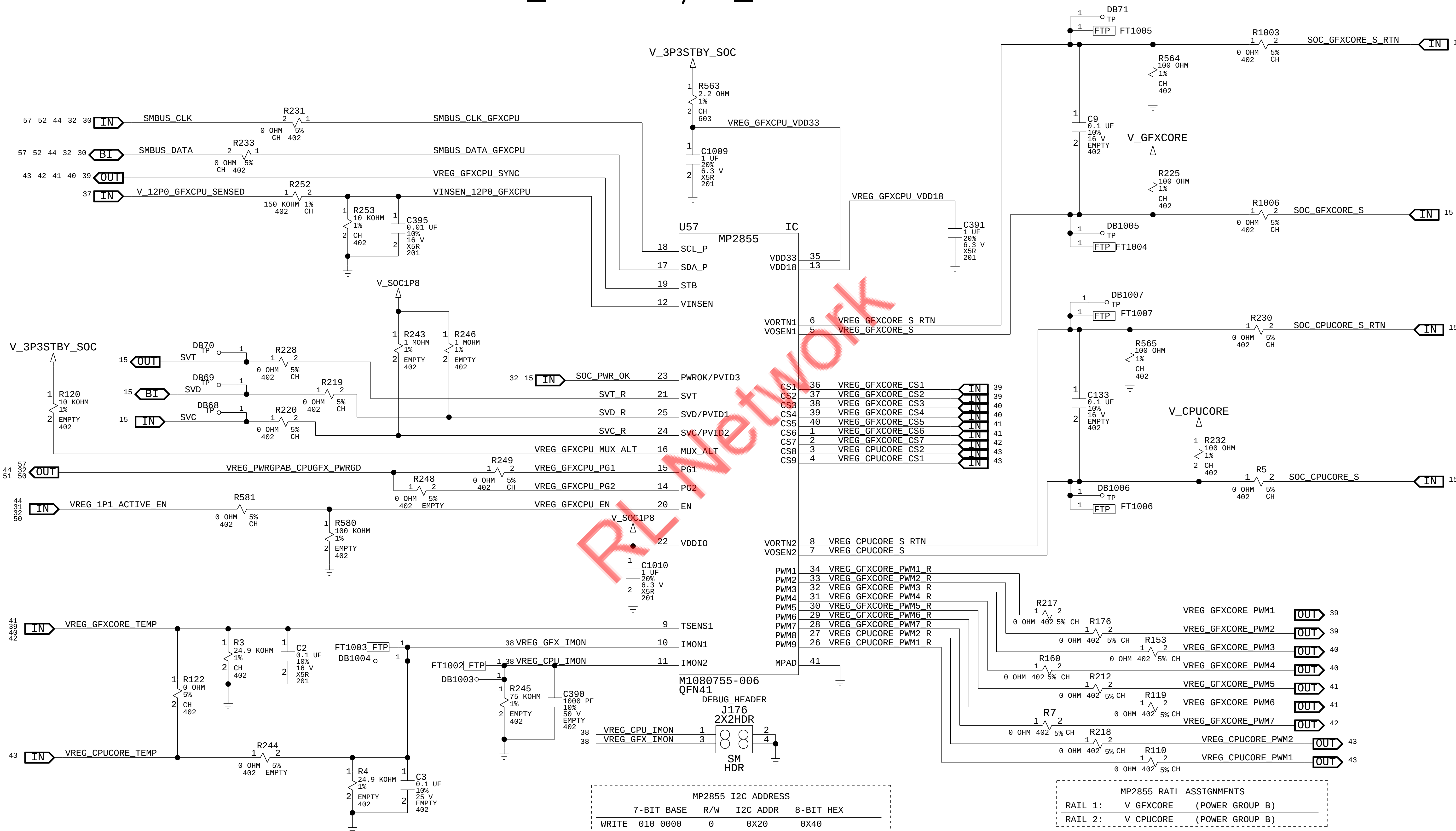


MEMIO/MEMPHY/SOC INPUT CAPS



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	37/59	37/59	E Retail	1.03

VREGS: V_CPUCORE, V_GFXCORE CONTROLLER



MP2855 I2C ADDRESS

	7-BIT BASE	R/W	I2C ADDR	8-BIT HEX
WRITE	010 0000	0	0X20	0X40
READ	010 0000	1	0X20	0X41

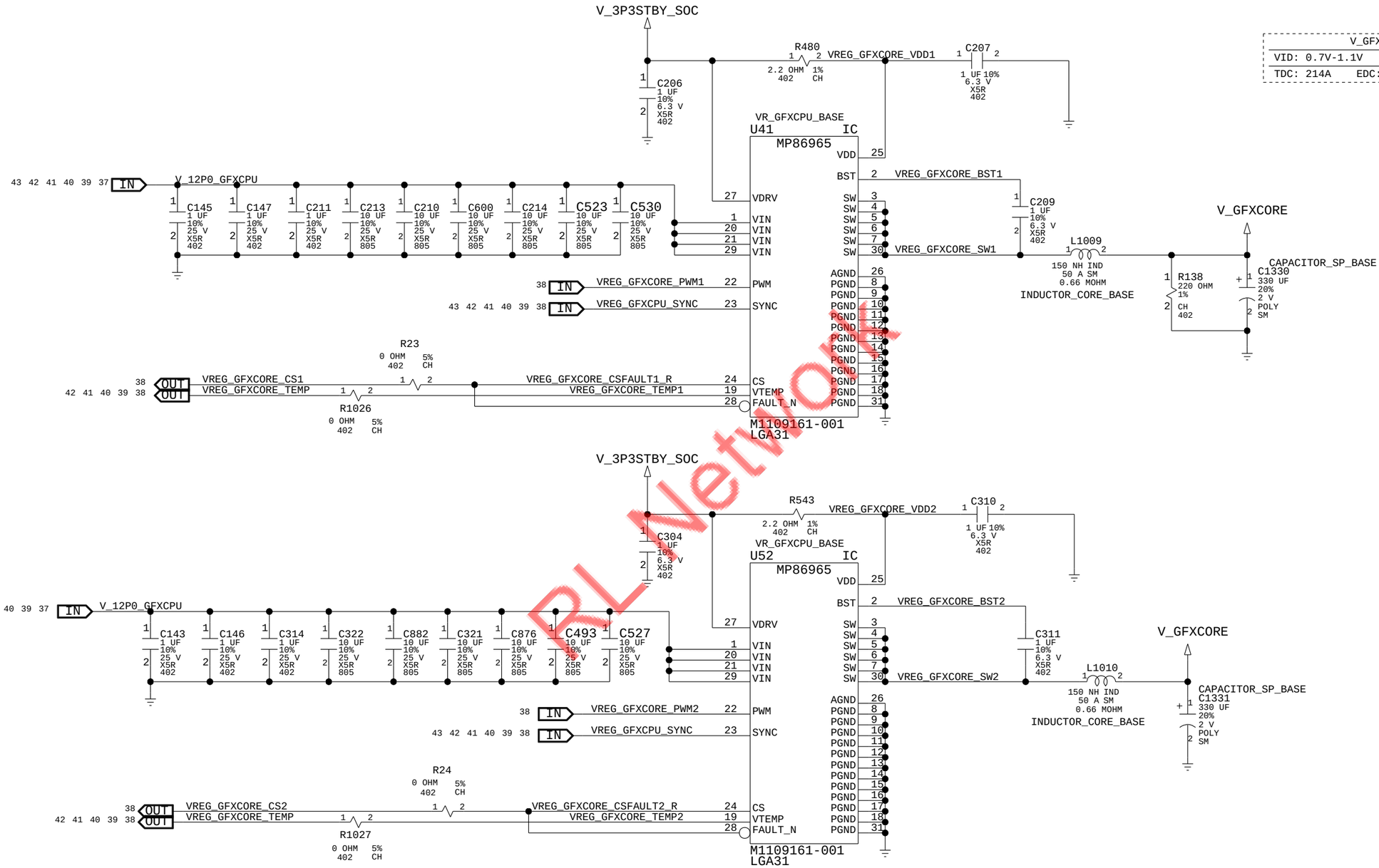
MP2855 RAIL ASSIGNMENTS

RAIL 1:	V_GFXCORE	(POWER GROUP B)
RAIL 2:	V_CPUCORE	(POWER GROUP B)

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	38/59	38/59	E	Retail.03

VREGS: V_GFXCORE OUTPUT PHASE 1 & 2

V_GFXCORE	
VID: 0.7V-1.1V	BOOT: .8V
TDC: 214A	EDC: 288A FSW: 500KHZ



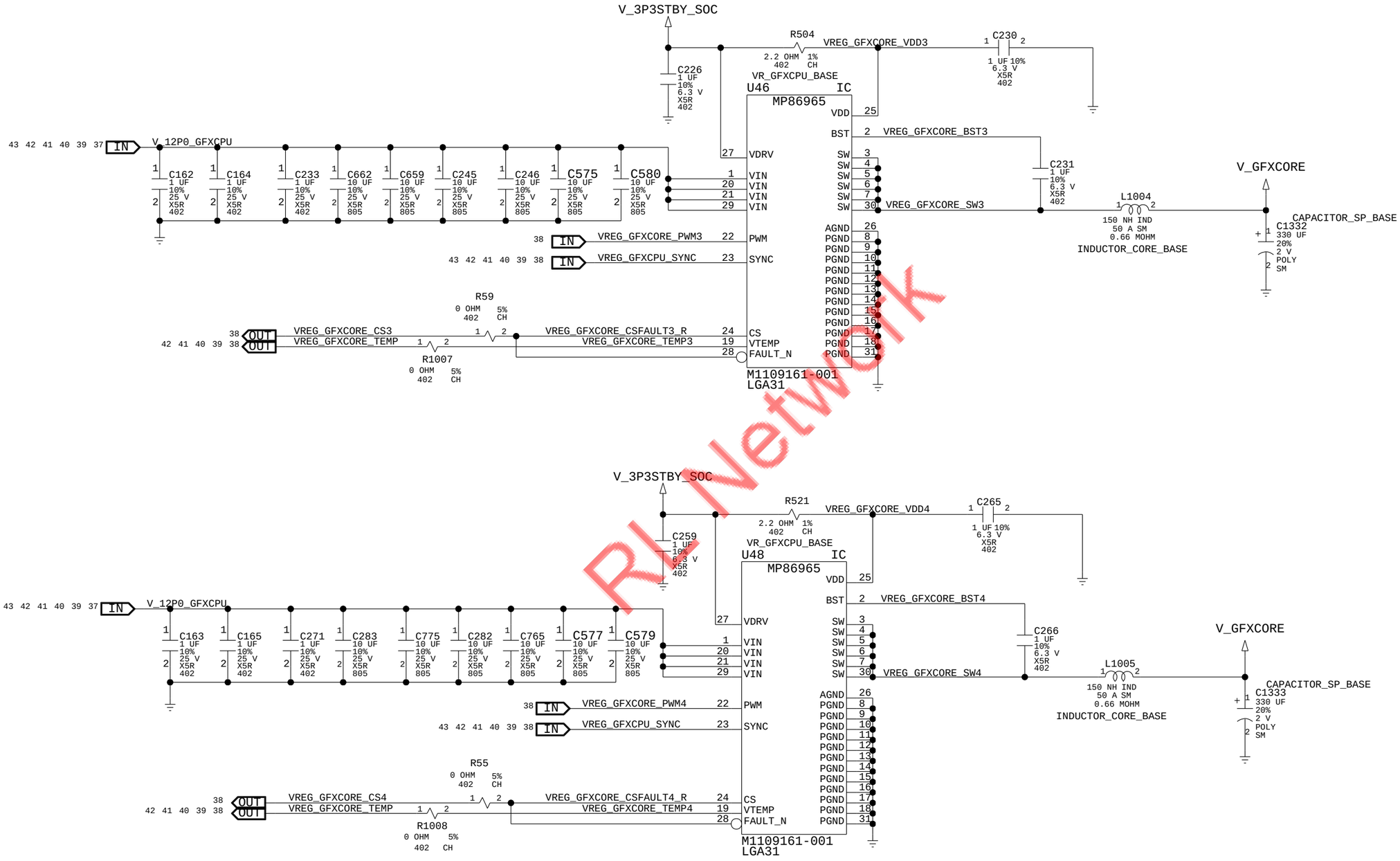
MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1067777-001	IC	U41,U52,U46,U48,U1000,U1001,U4,U55,U1013	IC-PWR, DC/DC CONV, MP86955	VR_GFXCPU_MP86955
M1109161-001	IC	U41,U52,U46,U48,U1000,U1001,U4,U55,U1013	IC-PWR, DC/DC CONV, MP86965	VR_GFXCPU_MP86965

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1116117-001	IC	L1009,L1010,L1004,L1005,L1007,L1008,L6,L1006,L1011		INDUCTOR_CORE_EATON
M1117589-001	IC	L1009,L1010,L1004,L1005,L1007,L1008,L6,L1006,L1011		INDUCTOR_CORE_SUNLORD
M1126117-001	IC	L1009,L1010,L1004,L1005,L1007,L1008,L6,L1006,L1011		INDUCTOR_CORE_ITG

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
X913175-001	IC	C1330,C1331,C1332,C1333,C1257,C1256	PANASONIC 330UF SP QUAL	CAPACITOR_SP_PANASONIC
X913175-001	IC	C1263,C1260	PANASONIC 330UF SP QUAL	CAPACITOR_SP_PANASONIC
M1070340-001	IC	C1330,C1331,C1332,C1333,C1257,C1256	MURATA 330UF SP QUAL	CAPACITOR_SP_MURATA
M1070340-001	IC	C1263,C1260	MURATA 330UF SP QUAL	CAPACITOR_SP_MURATA

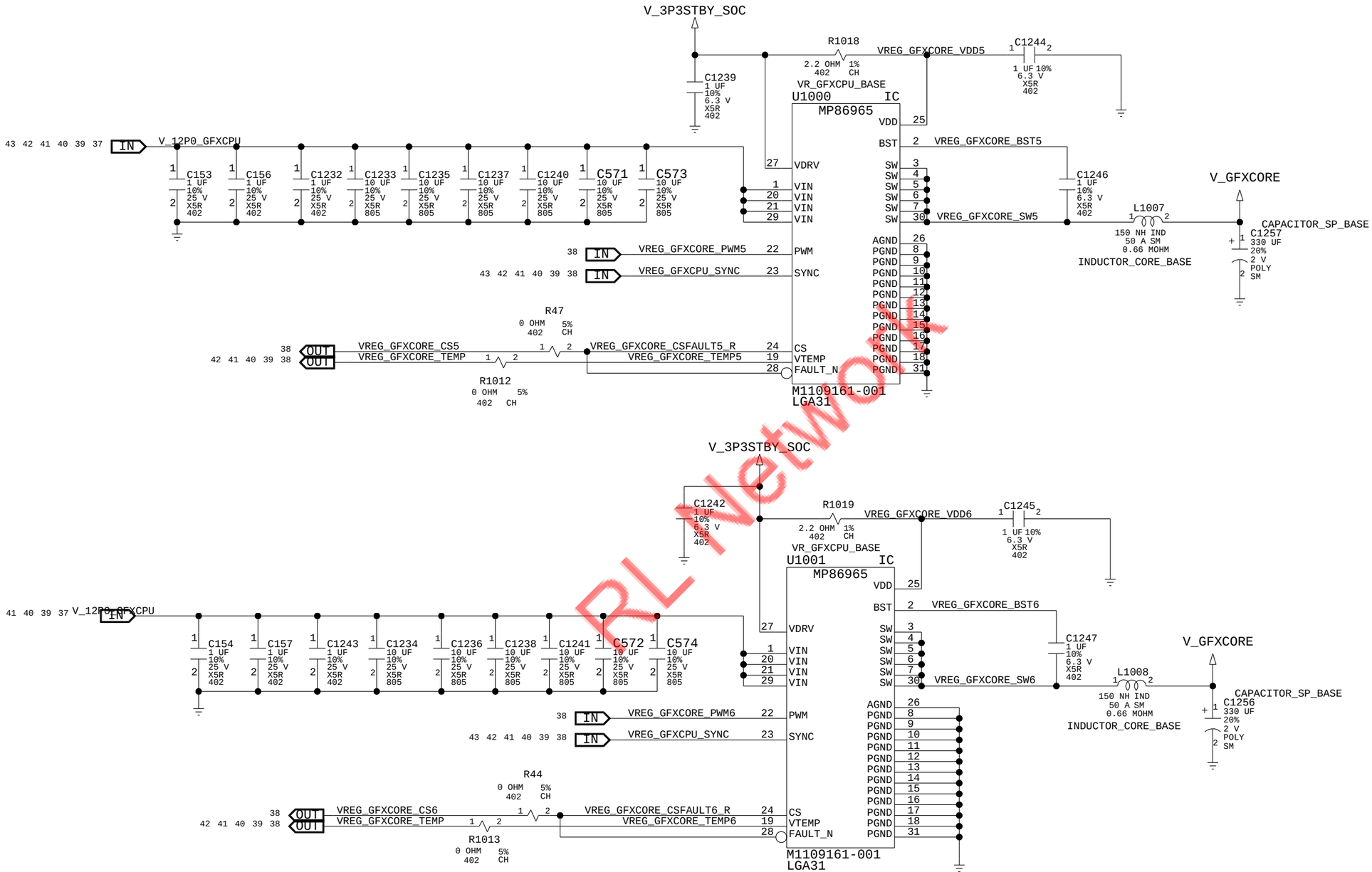
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	39/59	39/59	E Retail	1.03

VREGS: V_GFXCORE OUTPUT PHASE 3 & 4



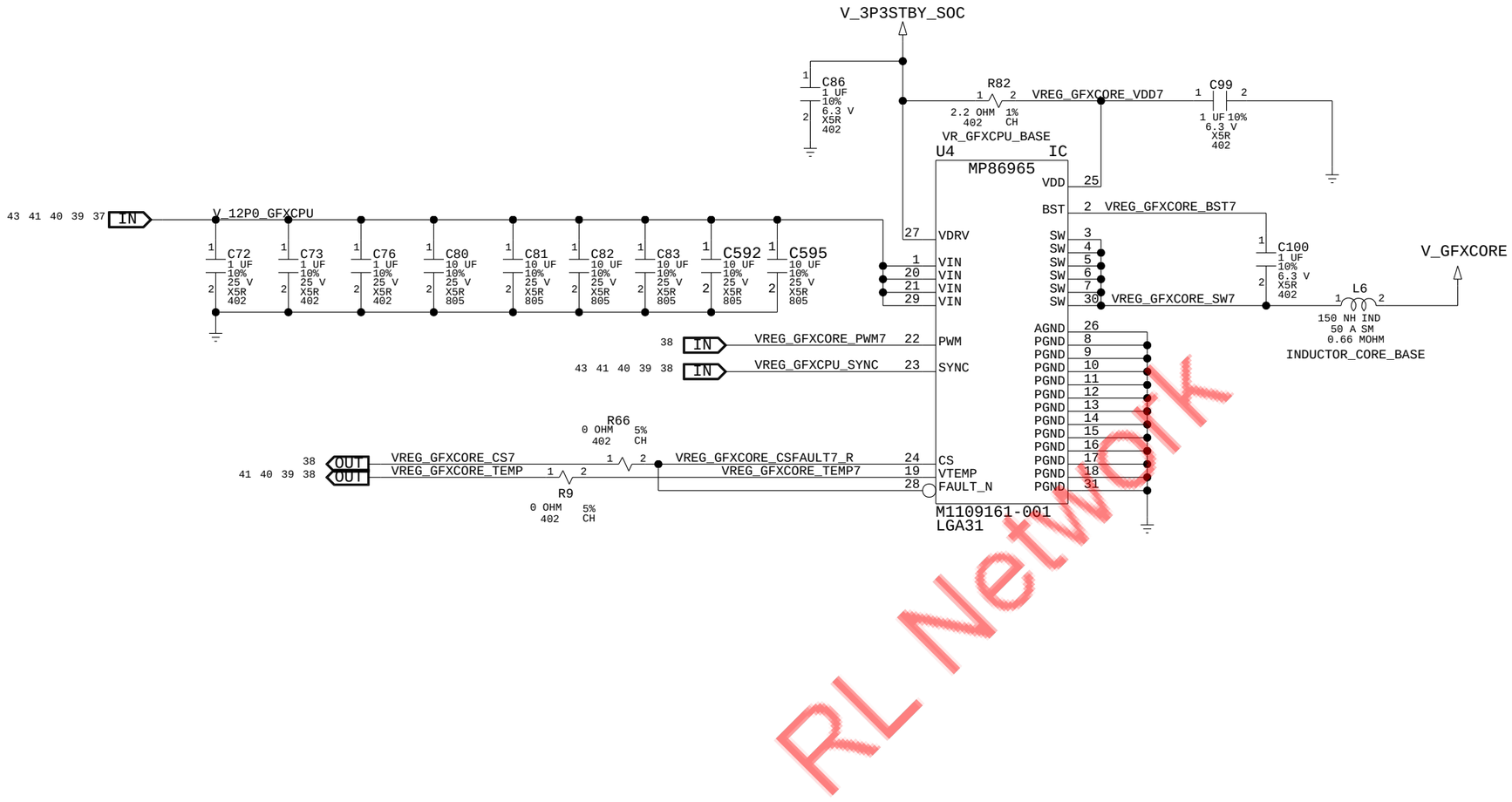
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	40/59	40/59	E Retail	1.03

VREGS: V_GFXCORE OUTPUT PHASE 5 & 6



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	41/59	41/59	E Retail	1.03

VREGS: V_GFXCORE OUTPUT PHASE 7



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	42/59	42/59	E Retail	1.03

VREGS: V_CPUCORE OUTPUT

V_CPUCORE		
VID: 0.7V-1.23V	BOOT: .8V	
TDC: 36A	EDC: 97A	FSW: 700KHZ

V_3P3STBY_SOC

R556 2.2 OHM 1% 402 CH

VREG_CPUCORE_VDD1

C349 1 UF 10% 6.3 V X5R 402

C353 1 UF 10% 6.3 V X5R 402

VR_GFXCPU_BASE

U55 IC MP86965

M1109161-001 LGA31

43 42 41 40 39 37 IN V_12P0_GFXCPU

C183 1 UF 10% 25 V X5R 402

C185 1 UF 10% 25 V X5R 402

C369 1 UF 10% 25 V X5R 402

C373 10 UF 10% 25 V X5R 805

C992 10 UF 10% 25 V X5R 805

C989 10 UF 10% 25 V X5R 805

C372 10 UF 10% 25 V X5R 805

C583 10 UF 10% 25 V X5R 805

C590 10 UF 10% 25 V X5R 805

Pin	Name
25	VDD
2	BST
27	VDRV
1	VIN
20	VIN
21	VIN
29	VIN
3	SW
4	SW
5	SW
6	SW
7	SW
30	SW
26	AGND
8	PGND
9	PGND
10	PGND
11	PGND
12	PGND
13	PGND
14	PGND
15	PGND
16	PGND
17	PGND
18	PGND
31	PGND
22	PWM
23	SYNC
24	CS
19	VTEMP
28	FAULT_N

VREG_CPUCORE_BST1

C367 1 UF 10% 6.3 V X5R 402

VREG_CPUCORE_SW1

L1006 150 NH IND 50 A SM 0.66 MOHM INDUCTOR_CORE_BASE

V_CPUCORE

R186 1 KOHM 1% CH 402

C1263 330 UF 20% 2 V POLY SM

CAPACITOR_SP_BASE

38 IN VREG_CPUCORE_PWM1

43 42 41 40 39 38 IN VREG_GFXCPU_SYNC

R255 0 OHM 5% 402 CH

38 OUT VREG_CPUCORE_CS1

43 38 OUT VREG_CPUCORE_TEMP

VREG_CPUCORE_CSFAULT1_R

VREG_CPUCORE_TEMP1

R1009 0 OHM 5% 402 CH

V_3P3STBY_SOC

R1087 2.2 OHM 1% 402 CH

VREG_CPUCORE_VDD2

C1350 1 UF 10% 6.3 V X5R 402

C1353 1 UF 10% 6.3 V X5R 402

VR_GFXCPU_BASE

U1013 IC MP86965

M1109161-001 LGA31

43 42 41 40 39 37 IN V_12P0_GFXCPU

C182 1 UF 10% 25 V X5R 402

C184 1 UF 10% 25 V X5R 402

C1352 1 UF 10% 25 V X5R 402

C1347 10 UF 10% 25 V X5R 805

C1348 10 UF 10% 25 V X5R 805

C1349 10 UF 10% 25 V X5R 805

C1351 10 UF 10% 25 V X5R 805

C584 10 UF 10% 25 V X5R 805

C591 10 UF 10% 25 V X5R 805

Pin	Name
25	VDD
2	BST
27	VDRV
1	VIN
20	VIN
21	VIN
29	VIN
3	SW
4	SW
5	SW
6	SW
7	SW
30	SW
26	AGND
8	PGND
9	PGND
10	PGND
11	PGND
12	PGND
13	PGND
14	PGND
15	PGND
16	PGND
17	PGND
18	PGND
31	PGND
22	PWM
23	SYNC
24	CS
19	VTEMP
28	FAULT_N

VREG_CPUCORE_BST2

C1354 1 UF 10% 6.3 V X5R 402

VREG_CPUCORE_SW2

L1011 150 NH IND 50 A SM 0.66 MOHM INDUCTOR_CORE_BASE

V_CPUCORE

C1260 330 UF 20% 2 V POLY SM

CAPACITOR_SP_BASE

38 IN VREG_CPUCORE_PWM2

43 42 41 40 39 38 IN VREG_GFXCPU_SYNC

R247 0 OHM 5% 402 CH

38 OUT VREG_CPUCORE_CS2

43 38 OUT VREG_CPUCORE_TEMP

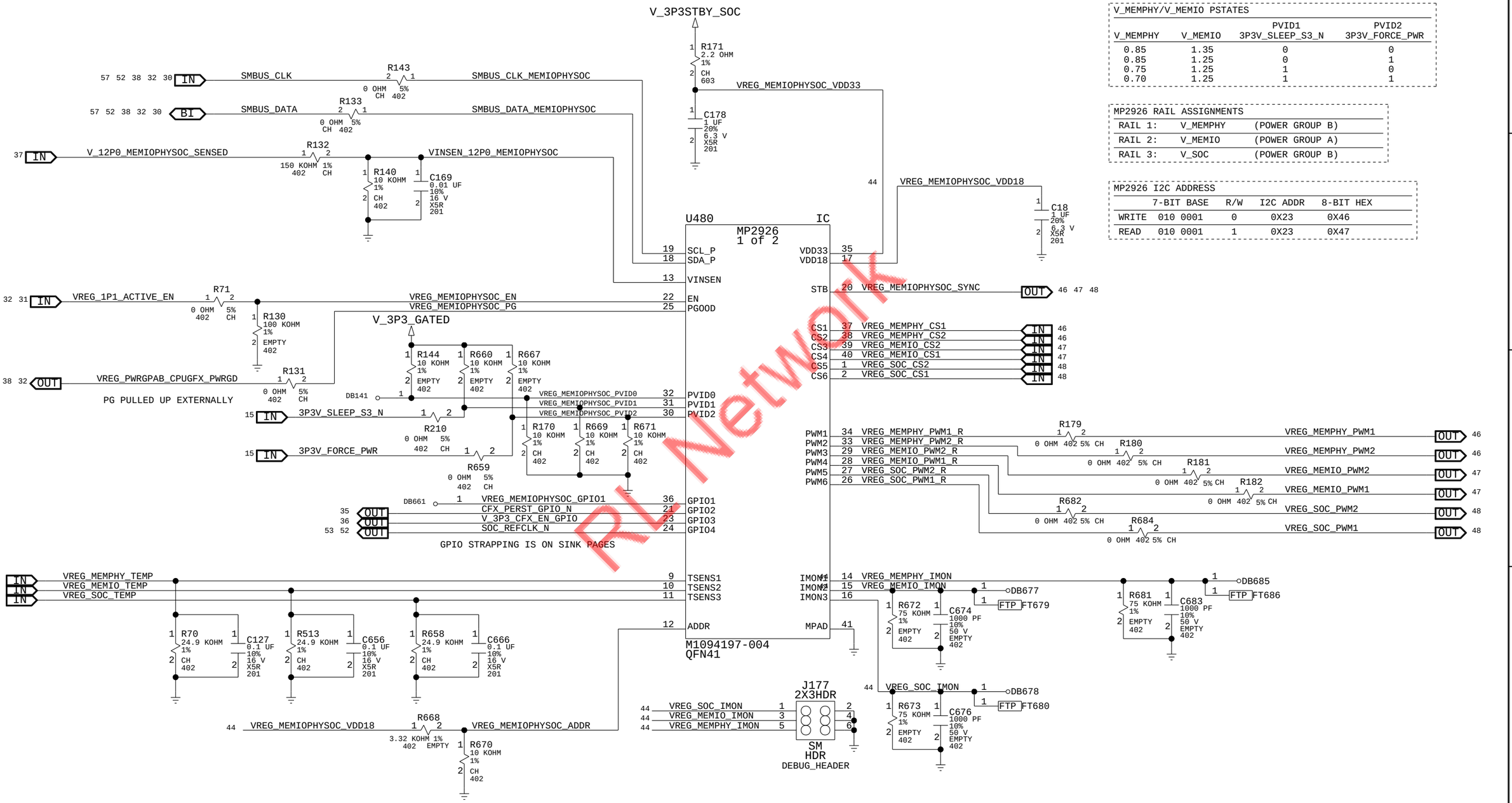
VREG_CPUCORE_CSFAULT2_R

VREG_CPUCORE_TEMP2

R1083 0 OHM 5% 402 CH

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	43/59	43/59	E Retail	1.03

VREGS: V_MEMIO, V_MEMPHY, V_SOC CONTROLLER



V_MEMPHY/V_MEMIO PSTATES			
		PVID1	PVID2
V_MEMPHY	V_MEMIO	3P3V_SLEEP_S3_N	3P3V_FORCE_PWR
0.85	1.35	0	0
0.85	1.25	0	1
0.75	1.25	1	0
0.70	1.25	1	1

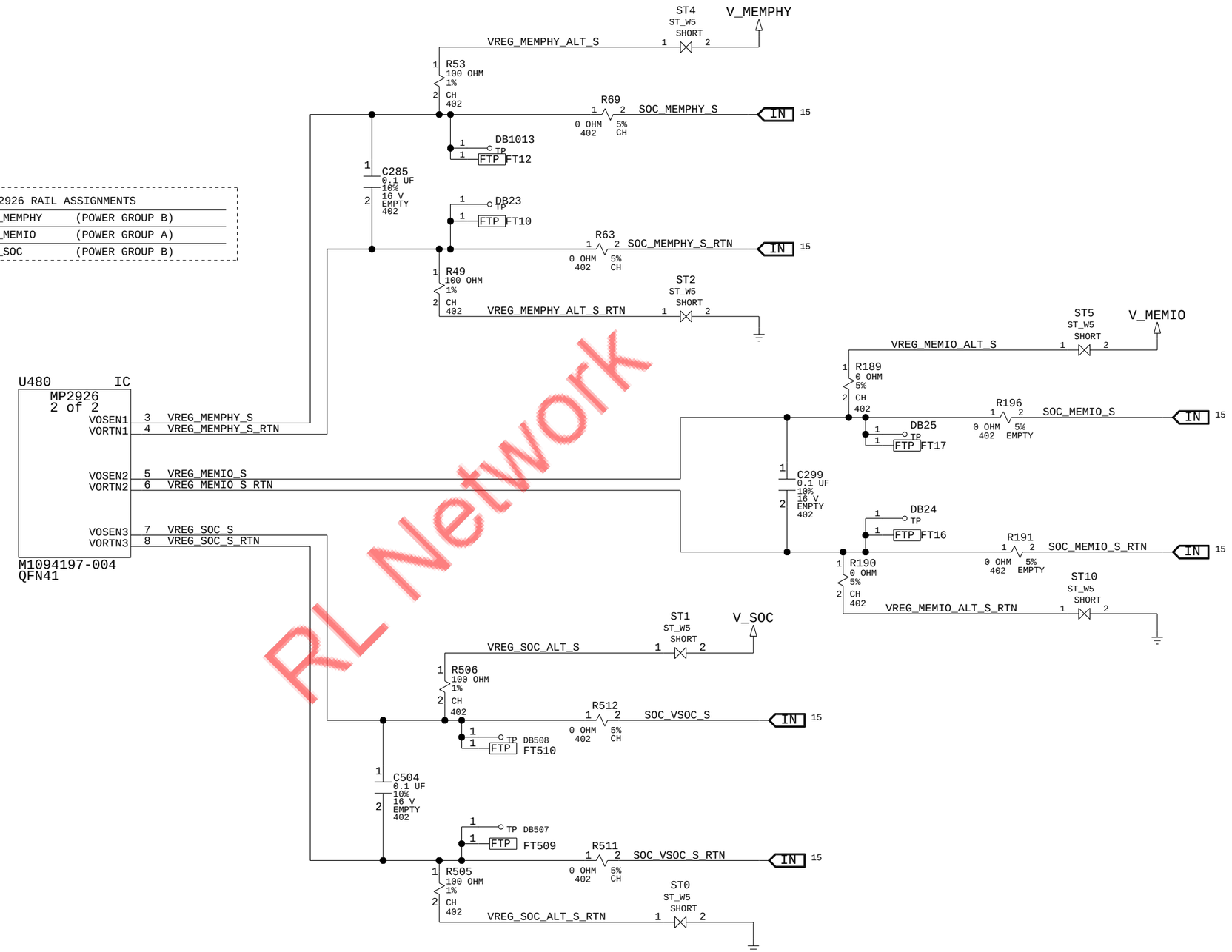
MP2926 RAIL ASSIGNMENTS		
RAIL 1:	V_MEMPHY	(POWER GROUP B)
RAIL 2:	V_MEMIO	(POWER GROUP A)
RAIL 3:	V_SOC	(POWER GROUP B)

MP2926 I2C ADDRESS				
	7-BIT BASE	R/W	I2C ADDR	8-BIT HEX
WRITE	010 0001	0	0X23	0X46
READ	010 0001	1	0X23	0X47

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	44/59	44/59	E Retail	1.03

VREGS: V_MEMIO, V_MEMPHY, V_SOC SENSE

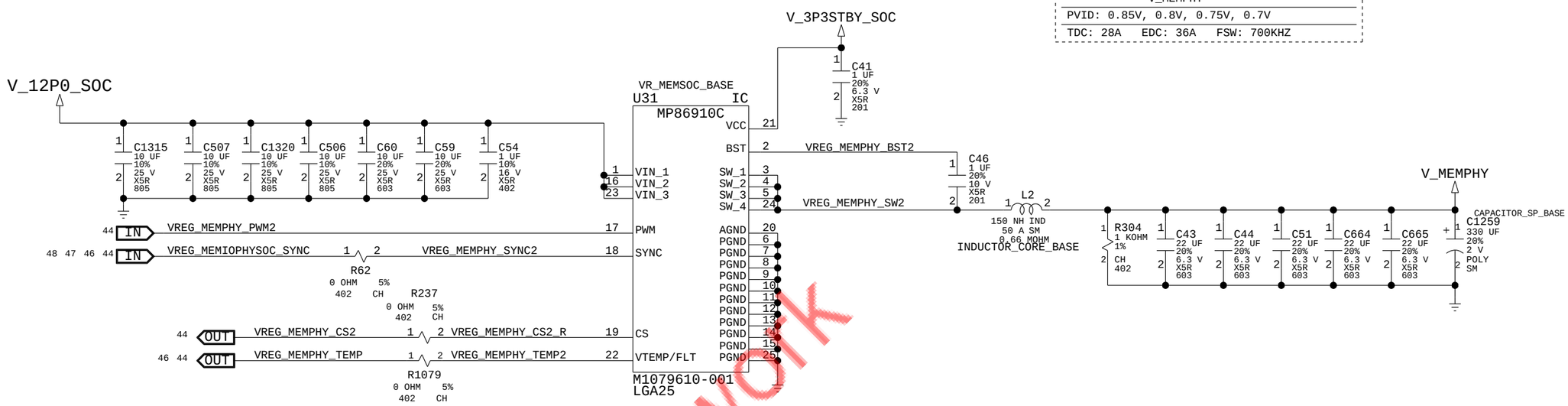
MP2926 RAIL ASSIGNMENTS		
RAIL 1:	V_MEMPHY	(POWER GROUP B)
RAIL 2:	V_MEMIO	(POWER GROUP A)
RAIL 3:	V_SOC	(POWER GROUP B)



MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	45/59	45/59	E Retail	1.03

VREGS: V_MEMPHY OUTPUT

V_MEMPHY
PVID: 0.85V, 0.8V, 0.75V, 0.7V
TDC: 28A EDC: 36A FSW: 700KHZ



MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
X913175-001	IC	C1259,C1258,C1261,C1262,C110,C109	PANASONIC 330UF SP QUAL	CAPACITOR_SP_PANASONIC
M1070340-001	IC	C1259,C1258,C1261,C1262,C110,C109	MURATA 330UF SP QUAL	CAPACITOR_SP_MURATA

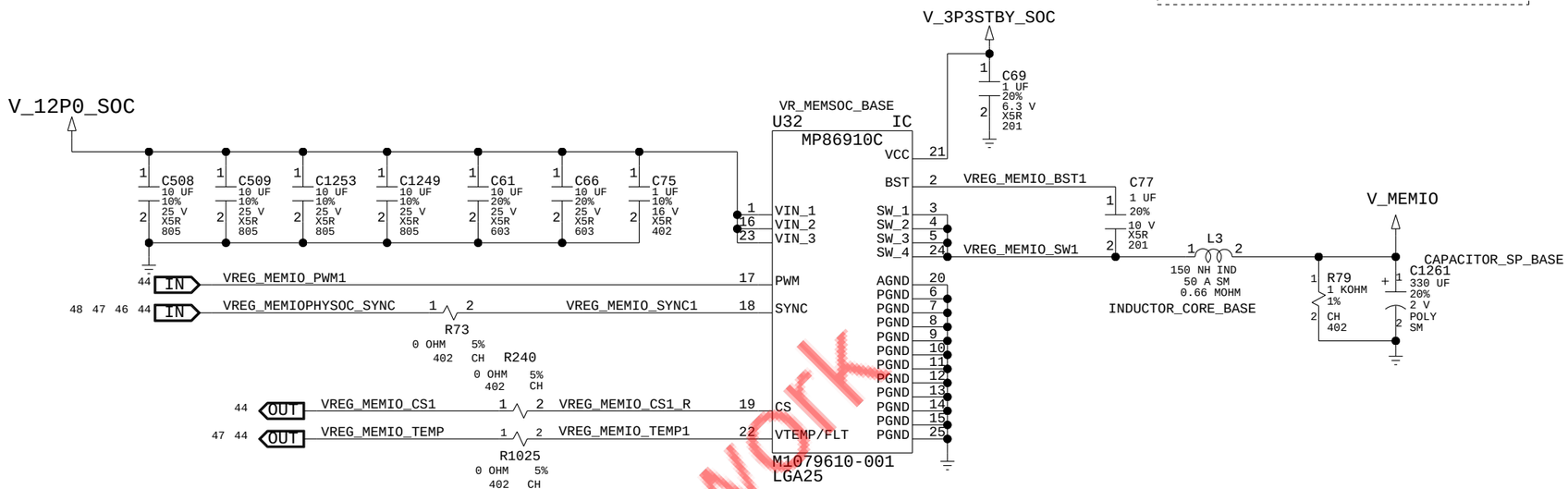
MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1116117-001	IC	L2,L16,L3,L15,L0,L1002		INDUCTOR_CORE_EATON
M1117589-001	IC	L2,L16,L3,L15,L0,L1002		INDUCTOR_CORE_SUNLORD
M1126117-001	IC	L2,L16,L3,L15,L0,L1002		INDUCTOR_CORE_ITG

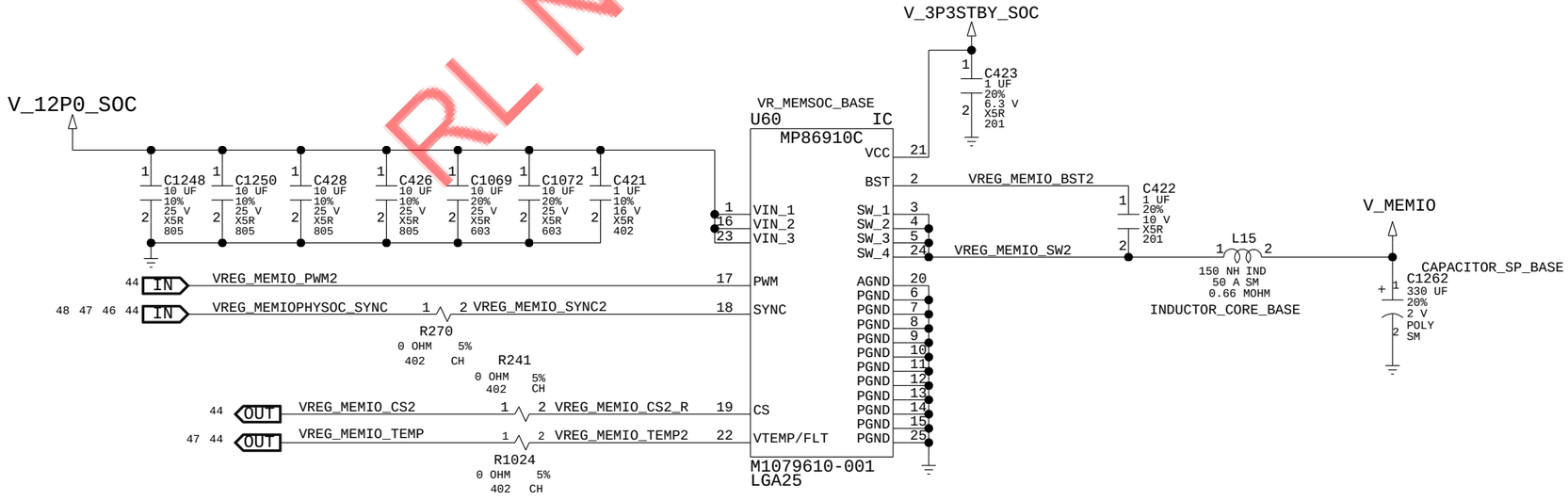
MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1079610-001	IC	U31,U62,U32,U60,U0,U59	IC-PWR, DC/DC CONV, MP86910C	VR_MEMSOC_MP86910C
M1126229-001	IC	U31,U62,U32,U60,U0,U59	IC-PWR, DC/DC CONV, MP86912C	VR_MEMSOC_MP86912C

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	46/59	46/59	E Retail	1.03

VREGS: V_MEMIO OUTPUT

V_MEMIO
PVID: 1.35V, 1.25V
TDC: --A EDC: --A FSW: 700KHZ

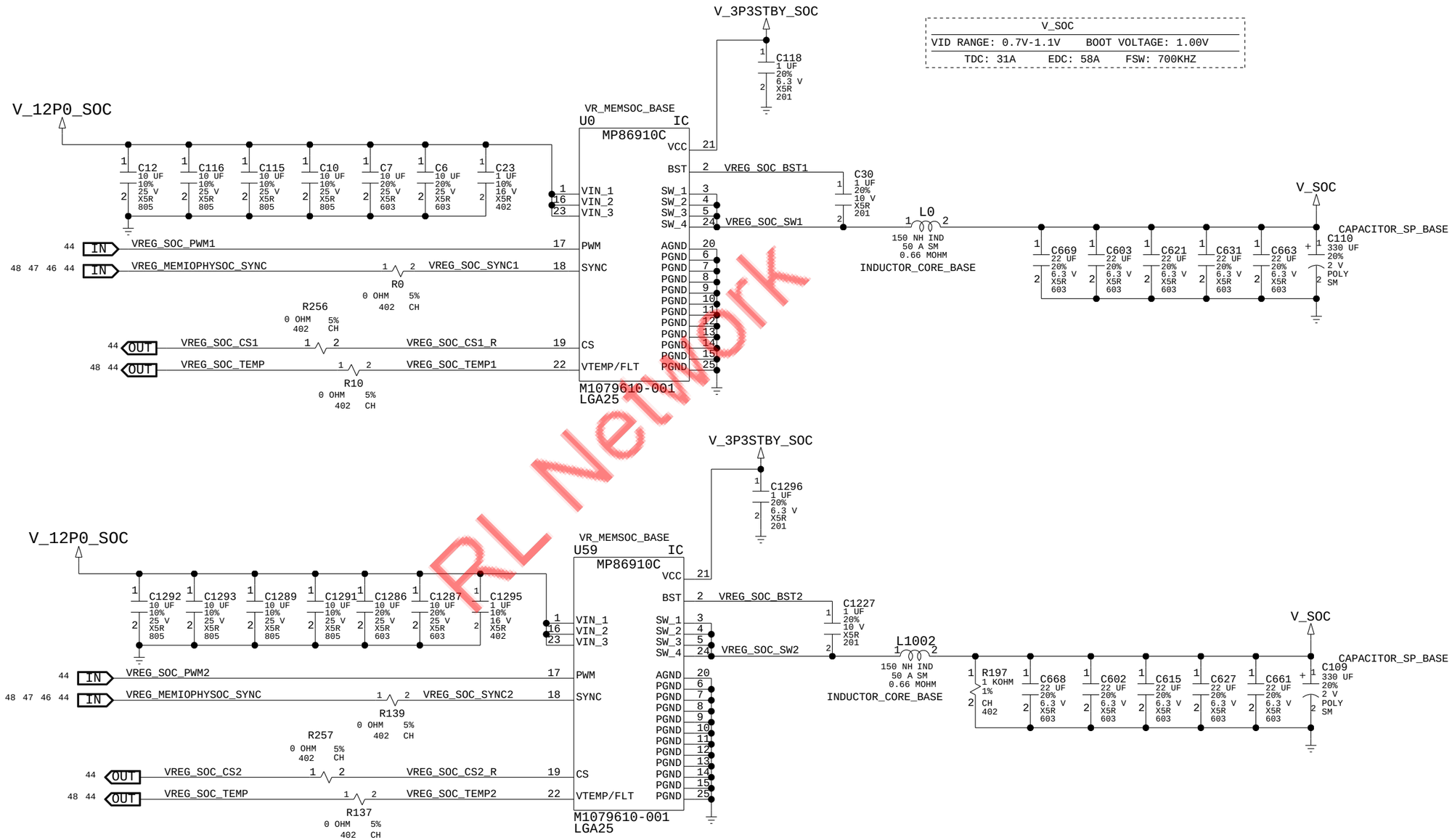




MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	47/59	47/59	E Retail	1.03

VREGS: V_SOC OUTPUT

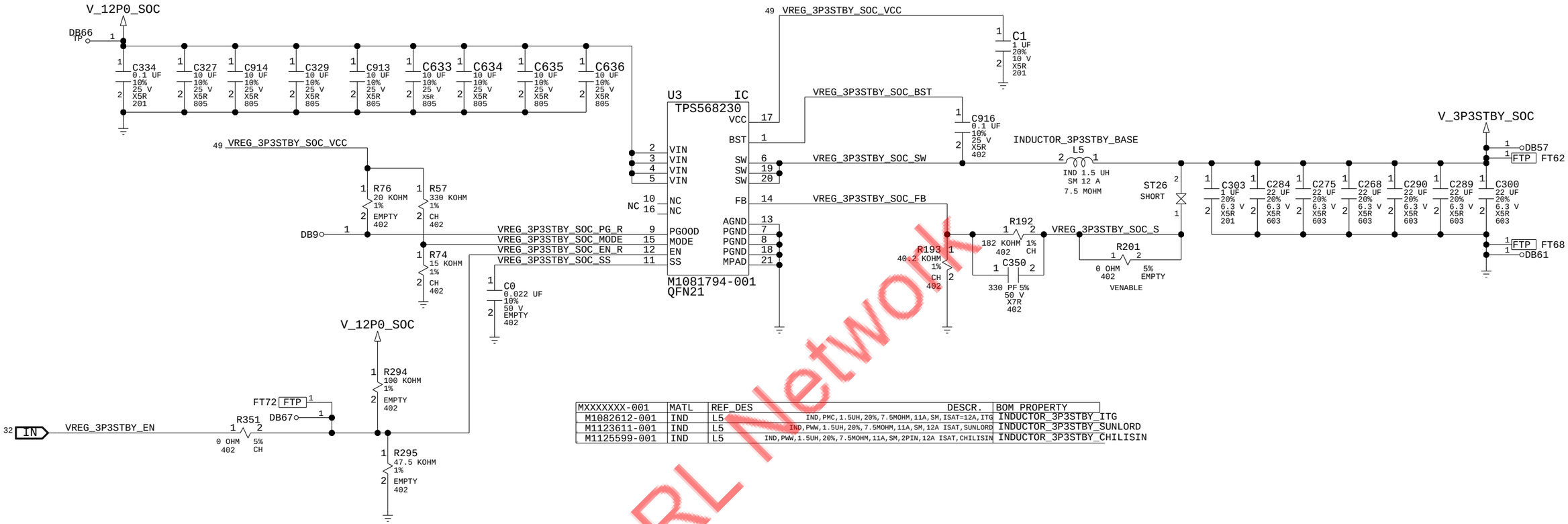
V_SOC		
VID RANGE: 0.7V-1.1V	BOOT VOLTAGE: 1.00V	
TDC: 31A	EDC: 58A	FSW: 700KHZ



PROJECT NAME	PAGE	CSA PAGE	FAB	VER
Toledo SoC	48/59	48/59	E Retail	1.03

VREGS: V_3P3STBY_SOC

V_3P3STBY_SOC
NOM. VOLTAGE: 3.32



MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1082612-001	IND	L5	IND,PMC,1.5UH,20%,7.5MOHM,11A,SM,ISAT=12A,ITG	INDUCTOR_3P3STBY_ITG
M1123611-001	IND	L5	IND,PWW,1.5UH,20%,7.5MOHM,11A,SM,12A ISAT,SUNLORD	INDUCTOR_3P3STBY_SUNLORD
M1125599-001	IND	L5	IND,PWW,1.5UH,20%,7.5MOHM,11A,SM,2PIN,12A ISAT,CHILISIN	INDUCTOR_3P3STBY_CHILISIN

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	49/59	49/59	E Retail	1.03

VREGS: V_SOC1P8, V_DRAM1P8

U914 IS A LINEAR REGULATOR STUFFING OPTION
IN CASE VDD18/SOC1P8 IS SENSITIVE TO RIPPLE VOLTAGE
THIS IS NOT EXPECTED TO BE NEEDED AS AMD HAS SINCE
PROVIDED A RIPPLE VOLTAGE REQUIREMENT OF <30MV PK-PK

V_SOC1P8: 1.80V
TDC: 1.8 EDC: 2.8 FSW: 1.5MHZ

V_3P3STBY_SOC

U681 IC
RT5788B
M1111231-001
SOT23-8

C679 22 UF 20% 6.3 V X5R 603
C680 22 UF 20% 6.3 V X5R 603
L682 1 UH IND 8.7 A SM 26 MOHM
C720 10000 PF 10% 50 V EMPTY 402
R259 69.8 KOHM 1% EMPTY 402
C695 22 UF 20% 6.3 V X5R 603
C711 22 UF 20% 6.3 V X5R 603
C730 22 UF 20% 6.3 V X5R 603
C723 22 UF 20% 6.3 V X5R 603
C682 22 UF 20% 6.3 V X5R 603

VREG_SOC1P8_PG
VREG_SOC1P8_SW
VREG_SOC1P8_OUT
VREG_SOC1P8_FB
VREG_SOC1P8_EN

R725 0 OHM 5% 402 CH
R722 0 OHM 5% 402 CH
R724 0 OHM 5% 402 EMPTY
R726 34.8 KOHM 1% CH 402
R258 0 OHM 5% 402 CH VR_FIXED
R728 69.8 KOHM 1% 402 CH VR_FIXED

VREG_PWRGPAB_CPUGFX_PWRGD
VREG_PWRGPA_EN
VREG_1P1_ACTIVE_EN
VREG_SOC1P8_SNS
VREG_SOC1P8_FB_MID

R688 0 OHM 5% 402 EMPTY
R263 0 OHM 5% 402 EMPTY
ST12 SHORT

U714 EMPTY
TPS7A84A
M1110730-001
QFN21

14 EN
15 16 17 IN
13 NR/SS
12 BIAS
NC 5 6 7 9 10 11 50mV 100mV 200mV 400mV 800mV 1P6V
PG 4
OUT 1 19 20
SNS 2 NC
FB 3
GND 8 18 21 MPAD

V_3P3STBY_SOC
C731 10 UF 20% 6.3 V EMPTY 402
C729 10000 PF 10% 50 V EMPTY 402
VREG_1P8LDO_NR
10NF NR/SS SETS RISE ~1MS

C728 10000 PF 10% 50 V EMPTY 402
R729 31.6 KOHM 1% EMPTY 402
R732 31.6 KOHM 1% 402 EMPTY
R730 0 OHM 5% EMPTY 402
R731 24.9 KOHM 1% EMPTY 402
C721 22 UF 20% 6.3 V EMPTY 603
C716 22 UF 20% 6.3 V EMPTY 603

V_SOC1P8
VREG_SOC1P8_SNS
VREG_1P8LDO_FB_MID
VREG_1P8LDO_FB

FOR FIXED OPERATION @1.8V STUFF R732, R730 AS SHOWN
FOR M&M STUFF R732= 6.65KOHM, EMPTY R730
SNS CONNECTS AN INTERNAL DIVIDER FOR USE WITH ANYOUT VOLTAGE SETTING
FOR EXTERNAL DIVIDER, SNS IS LEFT DISCONNECTED

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
X850496-001	CH	R728	(RES-FXD,SM,45.3 KOHM,1%,1/16W,0402, PREFERRED)	VR_MM
X800967-001	EMPTY	R258	(RES_FXD,SM,0 OHM,5%,1/16W,0402,JUMPER,PREFERRED)	VR_MM

V_DRAM1P8: 1.80V
TDC: ??A EDC 3A FSW 1 5MHZ

L1661: MWSA0518 USED FOR LOWER HEIGHT

V_3P3STBY_SOC

U7 IC
RT5788B
M1111231-001
SOT23-8

C13 22 UF 20% 6.3 V X5R 603
C19 22 UF 20% 6.3 V X5R 603
C21 1 UF 20% 6.3 V X5R 201

VREG_DRAM1P8_PG
VREG_DRAM1P8_SW
VREG_DRAM1P8_EN
VREG_DRAM1P8_FB

INDUCTOR_DRAM1P8_BASE
L1661 0.47 UH IND 12 A SM 9 MOHM

R1659 0 OHM 5% 402 CH
R811 0 OHM 5% 402 CH

VREG_PWRGPAB_CPUGFX_PWRGD
VREG_PWRGPA_EN

R823 69.8 KOHM 1% EMPTY 402
C22 22 UF 20% 6.3 V X5R 603
C26 22 UF 20% 6.3 V X5R 603
C27 22 UF 20% 6.3 V X5R 603
C29 22 UF 20% 6.3 V X5R 603
C31 100 PF 5% 25 V EMPTY 201
VR_FIXED R481 69.8 KOHM 1% 402 CH
ST482 SHORT
VREG_DRAM1P8_SNS
VR_FIXED R586 0 OHM 5% CH 402
VREG_DRAM1P8_FB_MID
R825 34.8 KOHM 1% CH 402

V_DRAM1P8
DB137
FTP FT138

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1120971-001	IND	L1661	IND,PMC,0.47UH,9MOHM,10.5A,SM,SUNLORD	INDUCTOR_DRAM1P8_SUNLORD
M1126490-001	IND	L1661	IND,PMC,0.47UH,8.57MOHM,10.5A,SM,CHILISIN	INDUCTOR_DRAM1P8_CHILISIN

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
X850496-001	CH	R481	(RES-FXD,SM,45.3 KOHM,1%,1/16W,0402, PREFERRED)	VR_MM
X800967-001	EMPTY	R586	(RES_FXD,SM,0 OHM,5%,1/16W,0402,JUMPER,PREFERRED)	VR_MM

VREGS: V_SOCPHY, V_FUSE

V_SOCPHY: 0.75V
TDC: 1.4A EDC: 3.7A FSW: 2.2MHZ

V_3P3STBY_SOC

C483 1 UF 20% 6.3 V X5R 201
C497 10 UF 20% 6.3 V X5R 402
C490 10 UF 20% 6.3 V X5R 402

U129 IC TPS62826
M1087390-001 DFN6
VIN SW FB PG EN GND

OUT VREG_PWRGPAB_CPUGFX_PWRGD
IN VREG_PWRGPB_EN
R136 0 OHM 5% 402 CH
R135 0 OHM 5% 402 CH
VREG_SOCPHY_PG
VREG_SOCPHY_EN

INDUCTOR_SOCPHY_BASE
L1 0.47 UH IND 7.8 A SM 0.01 OHM
VREG_SOCPHY_SW

V_SOCPHY
FTP FT14 DB7
C503 22 UF 20% 6.3 V X5R 603
C123 22 UF 20% 6.3 V X5R 603
C124 22 UF 20% 6.3 V EMPTY 603
C126 22 UF 20% 6.3 V EMPTY 603
FTP FT13 DB5
SHORT ST13

PWRGPAB_CPUGFX_PWRGD TIED TO 3P3_MAIN WITH 10K
VREG_PWRGPB_EN PULLED DOWN TO GND WITH 10K

C40 120 PF 5% 50 V NPO 402

MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1102580-001	IND	L1	IND,0.47UH,30%,0.010OHM,5.2A,SM,SUNLORD QUAL	INDUCTOR_SOCPHY_SUNLORD
M1125677-001	IND	L1	IND,0.47UH,20%,.0095OHM,6.5A,SM,CYNTEC QUAL	INDUCTOR_SOCPHY_CYNTEC

VREG_SOCPHY_FB
VR_FIXED R68 24.9 KOHM 1% 402 CH
VREG_SOCPHY_S
R64 100 KOHM 1% CH 402
IN
OUT

V_FUSE: 0.83V
TDC: 100MA

V_3P3_GATED
V_3P3STBY_SOC
R324 100 KOHM 1% CH 402
C447 1 UF 20% 10 V X5R 201
VREG_PWRGPC_EN_R
D9 SOD123 MBR130L
D7 SOD123 MBR130L
R599 20 KOHM 1% EMPTY 402
VREG_PWRGPC_EN
V12P0_PWRGD

U68 IC AP7331_ADJ
M1012324-001 SOT23-5
IN OUT ADJ GND EN

V_FUSE OUTPUT ADJUSTED TO .72V FOR A0
REVERT R596 TO 45.3KOHM FOR B0

VREG_VFUSE_ADJ
R596 34 KOHM 1% CH 402
R595 42.2 KOHM 1% CH 402
C1084 0.022 UF 10% 25 V EMPTY 402
C441 4.7 UF 20% 10 V X5R 402
R597 49.9 OHM 1% CH 402
V_FUSE
DB74

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	51/59	51/59	E Retail	1.03

CLOCK: PCIE 100MHZ SS

9FGL0651 SMBUS ADDRESS
1101 010 R/W HEX
WRITE 1101 010 0 0XD4
READ 1101 010 1 0XD5

V_SOC1P8
V_1P8_SS_CLK_SEL
R33 0 OHM 5% 402 EMPTY
V_3P3_GATED
V_3P3_SS_CLK
FB0 1000 OHM 200 MA 1 OHM BEAD 402
R87 0 OHM 5% 402 CH
FB3 1000 OHM 200 MA 1 OHM BEAD 402
V_3P3_GATED
C105 1 UF 20% 6.3 V X5R 201
C95 0.1 UF 10% 16 V X5R 201

POWER SUBJECT TO REVIEW

52 V_3P3_SS_CLK
R624 10 KOHM 1% CH 402
R15 10 KOHM 1% CH 402
SPREAD SPECTRUM TURNED ON
R14 10 KOHM 1% EMPTY 402
R16 10 KOHM 1% EMPTY 402

V_1P8_SS_CLK
C64 10 UF 20% 6.3 V X5R 402
C65 0.1 UF 10% 16 V X5R 201
C67 0.1 UF 10% 16 V X5R 201
C70 0.1 UF 10% 16 V X5R 201
C74 0.1 UF 10% 16 V X5R 201
C79 0.1 UF 10% 16 V X5R 201
PLACE 0.1UF CAPS CLOSE TO EACH POWER PINS

U17 IC
6V41466

VDDIO	12		
VDDIO	17		
VDDIO	27		
VDDIO	32		
VDDIO	39		
VSS_EN_TRI	1	SS_LEVEL_SS_CLK	
VSADR/REF3.3	6	ADR_SEL_SS_CLK	
VOE0_N	13	52 34 IN M2_CLKREQ_N	
VOE1_N	21	52 35 IN CFX_CLKREQ_N	
VOE2_N	24	53 52 44 IN SOC_REFCLK_N	R21 0 OHM 402 EMPTY 52 SPARE_CLKREQ_N
VOE3_N	30	52 32 IN ENET_REFCLK_N	R22 0 OHM 402 EMPTY 52 SB_CLKREQ_N
VOE4_N	35		R25 0 OHM 402 52 ENET_CLKREQ_N
VOE5_N	38		R83 0 OHM 402 52 SOC_CLKREQ_N
CKPWRGD_PD_N	40		52 SS_CKPWRGD_PD_N
SCLK_3.3	9		52 SS_SCLK
SDATA_3.3	10		52 SS_SDATA
X1_25	2	53 IN 25MHZ_REF	
X2	3	1 SS_XTAL_X2	
VDD3.3	16		
VDD3.3	31		
VDDA3.3	26		
VDDDIG3.3	11		
VDDREF3.3	5		
VDDXTAL3.3	4		
DIF0	14	M2_PEX_SS_100M_CLKP	OUT 34
DIF0_N	15	M2_PEX_SS_100M_CLKN	OUT 34
DIF1	18	CFX_PEX_SS_100M_CLKP	OUT 35
DIF1_N	19	CFX_PEX_SS_100M_CLKN	OUT 35
DIF2	22	SPARE_PEX_SS_100M_CLKP	1 DB1
DIF2_N	23	SPARE_PEX_SS_100M_CLKN	1 DB2
DIF3	28	SB_PEX_SS_100M_CLKP	OUT 32
DIF3_N	29	SB_PEX_SS_100M_CLKN	OUT 32
DIF4	33	ENET_PEX_SS_100M_CLKP	OUT 32
DIF4_N	34	ENET_PEX_SS_100M_CLKN	OUT 32
DIF5	36	SOC_PEX_SS_100M_CLKP	OUT 2
DIF5_N	37	SOC_PEX_SS_100M_CLKN	OUT 2
NC	7		
NC	20		
NC	25		
GNDDIG	8		
EPAD	41		

M1092049-001
QFN41

C84 C85 C87 C550 C88 C89 0.1 UF 10% 16 V X5R 201
C90 10 UF 20% 6.3 V X5R 402
PLACE 0.1UF CAPS CLOSE TO EACH POWER PIN

85 OHM DIFF OUTPUTS

DEFAULT CONFIG DOES NOT REQ SMBUS
DEBUG
53 52 SMBUS_CLK_BUFFERED R152 0 OHM 402 CH
53 52 SMBUS_DATA_BUFFERED R155 0 OHM 402 CH DEBUG

V_3P3STBY_SOC
V_3P3_SS_CLK
C58 1 UF 20% 10 V X5R 201 DEBUG
C128 1 UF 20% 10 V X5R 201 DEBUG

U12 IC
TCA9803
M1090212-001
VSSOP
DEBUG

57 44 38 32 30	BI IN	SMBUS_DATA	3	SDAA	SDAB	6 SMBUS_DATA_BUFFERED	BI 52 53
57 44 38 32 30		SMBUS_CLK	2	SCLA	SCLB	7 SMBUS_CLK_BUFFERED	OUT 52 53
52 V_3P3_SS_CLK	R2 0 OHM 5% 402 CH DEBUG	SS_SMBUS_EN	5	EN	GND	4	

R11 10 KOHM 1% EMPTY 402

EN: 450K INTERNAL PU TO VCCA
V_3P3_SS_CLK HAS 10K PD TO GND

I2C BUFFER PREVENTS LEAKAGE PATH FROM SMBUS PULLUPS TO V_3P3_GATED THROUGH CLOCK GENERATORS

STUFF R109 AND R113 TO PREVENT SCLK/SDATA FROM FLOATING

V_3P3_SS_CLK
RETAIL R109 10 KOHM 1% CH 402
RETAIL R113 10 KOHM 1% CH 402
R35 10 KOHM 1% CH 402
R36 10 KOHM 1% CH 402
R37 10 KOHM 1% CH 402
R38 10 KOHM 1% EMPTY 402
R13 10 KOHM 1% CH 402
R39 10 KOHM 1% EMPTY 402
R41 10 KOHM 1% EMPTY 402
R42 10 KOHM 1% CH 402
R43 10 KOHM 1% CH 402
R166 1 KOHM 1% CH 402

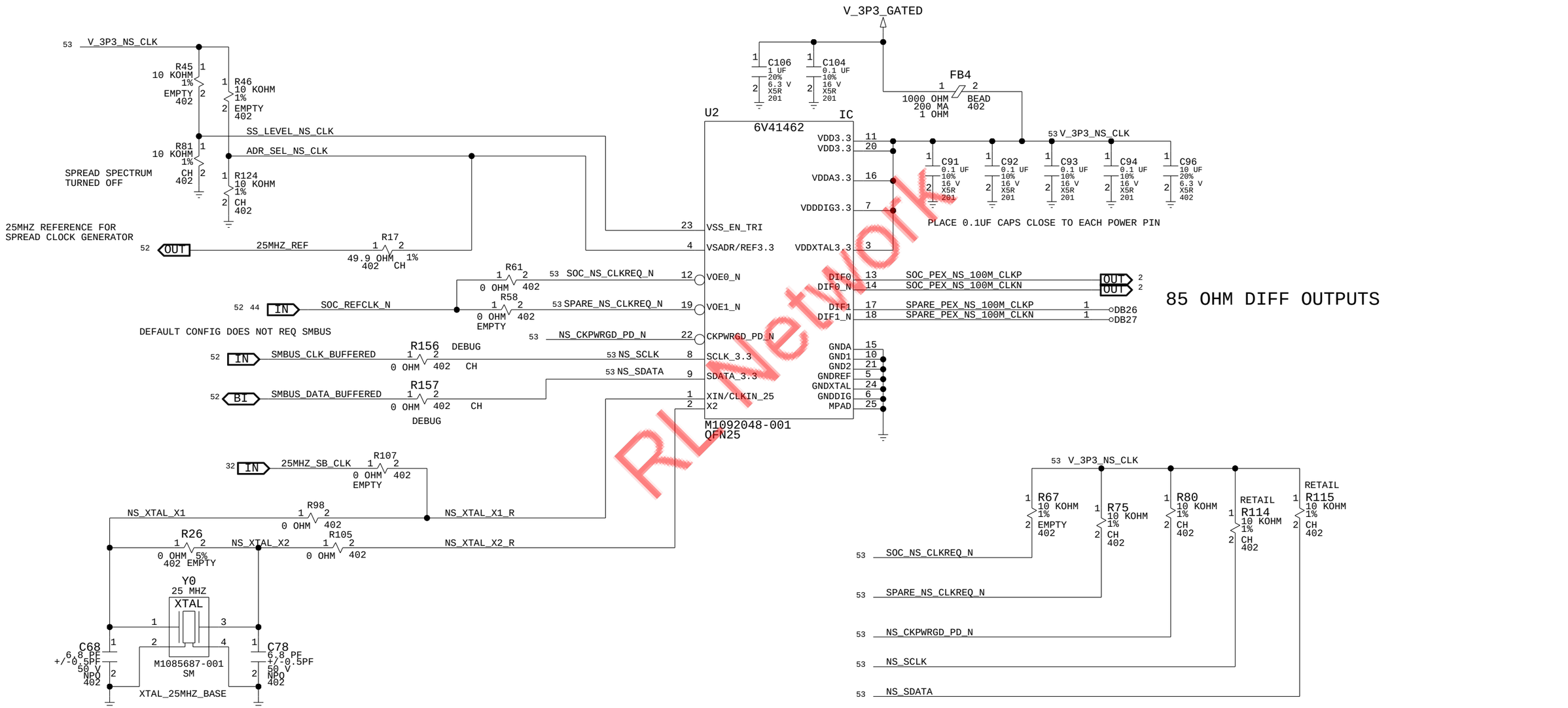
52	SS_SCLK
52	SS_SDATA
52 34	M2_CLKREQ_N
52 35	CFX_CLKREQ_N
52	SPARE_CLKREQ_N
52	SB_CLKREQ_N
52	ENET_CLKREQ_N
52	SOC_CLKREQ_N
52 32	ENET_REFCLK_N
52	SS_CKPWRGD_PD_N
53 52 44	SOC_REFCLK_N

R166 = 1K TO ACCOUNT FOR ~60KOHM COMBINED INPUT IMPEDANCE OF CLOCK GENS

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	52/59	52/59	E Retail	1.03

CLOCK: PCIE 100MHZ NS

9FGL04 SMBUS ADDRESS
1101 000 R/W HEX
WRITE 1101 000 0 0XD0
READ 1101 000 1 0XD1



MXXXXXXX-001	MATL	REF_DES	DESCR.	BOM PROPERTY
M1115898-001	IC	Y0	XTAL,25MHZ,15PPM,8PF,3.2X2.5MM	XTAL_25MHZ_KDS
M1085687-001	IC	Y0	XTAL,25MHZ,15PPM,8PF,3.2X2.5MM	XTAL_25MHZ_TXC
M1115904-001	IC	Y0	XTAL,25MHZ,15PPM,8PF,3.2X2.5MM	XTAL_25MHZ_NDK

MARGIN: V_SOCPHY,V_SOC1P8, V_DRAM1P8

REMOVED FOR RETAIL FAB

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	54/59	54/59	E Retail	1.03

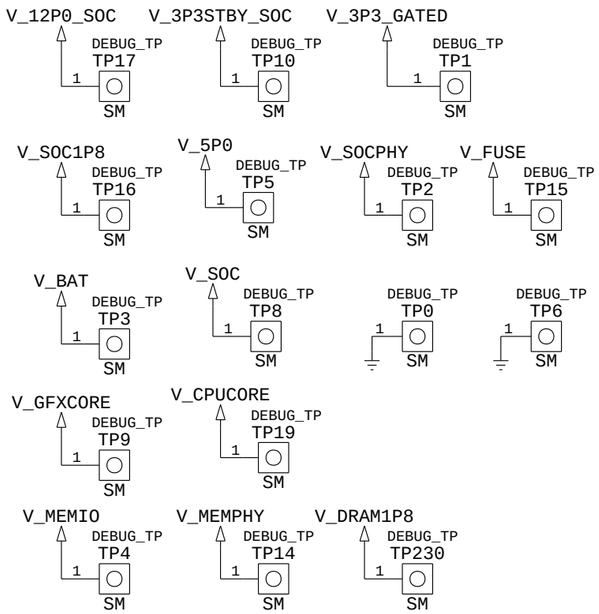
MONITOR: V_SOC1P8, V_SOCPHY, V_12P0_SOC, V_DRAM1P8

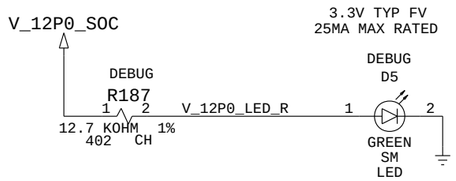
REMOVED FOR RETAIL FAB

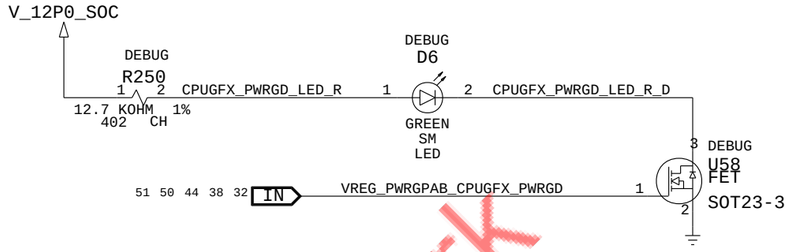
MONITOR: M.2, CFEXPRESS

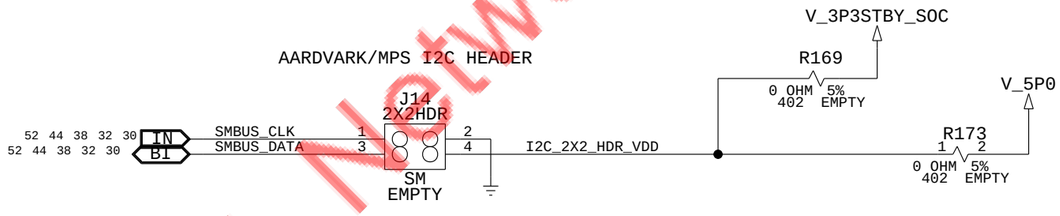
REMOVED FOR RETAIL FAB

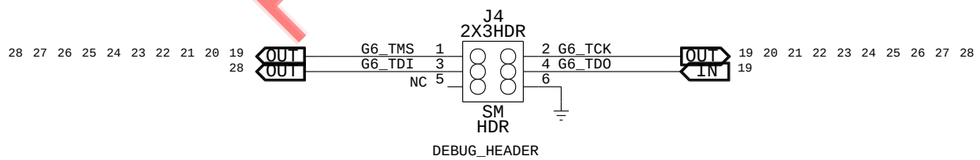
DEBUG: VR HEADERS, TEST POINTS, CONNECTORS







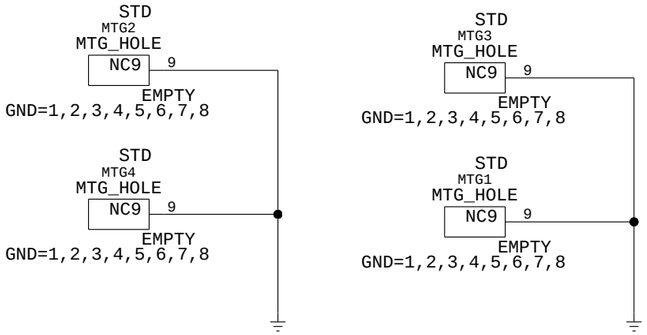




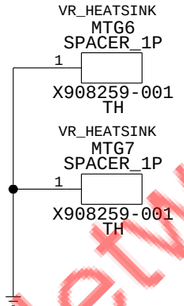
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	VER
	Toledo SoC	57/59	57/59	E Retail	1.03

LABELS AND MOUNTING

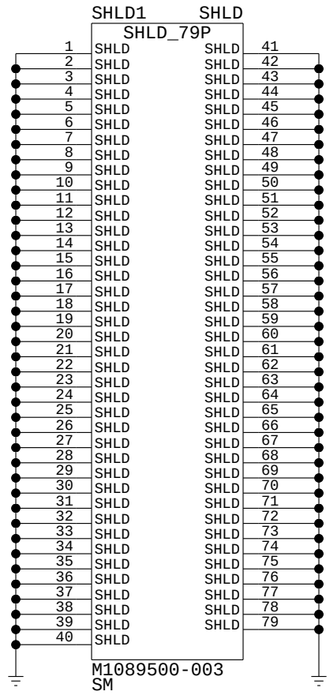
HEAT SINK MOUNTING HOLES



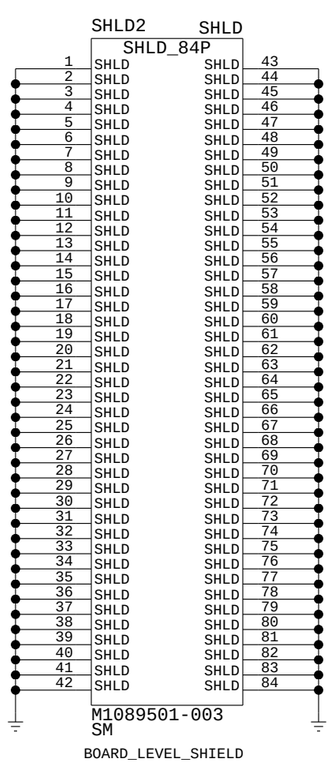
MEMIO/PHY/SOC HEATSINK MOUNTING PEMNUTS



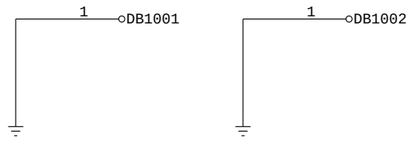
TOPSIDE BOARD LEVEL SHIELD



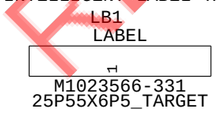
BOTTOMSIDE BOARD LEVEL SHIELD



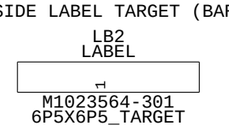
GND PADS FOR HEATSINK ALIGNMENT PINS



TOPSIDE INTELLIGENT LABEL TARGET



BOTTOMSIDE LABEL TARGET (BARCODE ONLY)



MXXXXXXX-001	MATL	REF DES	DESCR.	BOM PROPERTY
M1090324-006	FR4	PCB1	PCB,TOLEDO SOC,10LAYERS,GI,FR4,FAB E	PCB_GI
M1125041-002	FR4	PCB1	PCB,TOLEDO SOC,10LAYERS,OSP,FR4,DEBUG RF, FAB E	PCB_OSP_DEBUG_RF
M1128163-001	FR4	PCB1	PCB,TOLEDO SOC,10LAYERS,OSP,FR4,RETAIL RF,FAB E	PCB_OSP_RETAIL_RF
M1128164-001	FR4	PCB1	PCB,TOLEDO SOC,10LAYERS,OSP,FR4,RETAIL NON-RF,FAB E	PCB_OSP_RETAIL_NO_RF

USES DEBUG NETLIST
USES DEBUG NETLIST
USES RETAIL NETLIST
USES RETAIL NETLIST. INDUCTOR REMOVED BY LAYOUT

BOM DEFINITIONS

BOM	DEFINITION
BOARD_LEVEL_SHIELD	POPULATES TOP AND BOTTOM BOARD LEVEL SHIELDS. POPULATES M.2 BOARD LEVEL SHIELD
COMMON	ALL COMPONENTS WITH NO BOM PROPERTY
DEBUG	COMPONENTS REQUIRED FOR BRING UP & DEBUG
DEBUG_HDT	HDT-RELATED DEBUG COMPONENTS
DEBUG_TP	DEBUG TEST HOOKS. POPULATE IF BUILDING BARE PCBAS
DEBUG_HEADER	DEBUG HEADERS WITH HEIGHT CLEARANCE ISSUES WITH CHASSIS. POPULATE ONLY ON PCBAS NOT INTENEDED FOR USE IN A CONSOLE ASSEMBLY
DEBUG_SHUNT	COMPONENTS WHICH ARE ON DEBUG BOARDS, BUT ARE REMOVED/SHORTED ON RETAIL
GDDR6_BASE	DUMMY PLACE HOLDER FOR GDDR6/DRAM. NEVER USE THIS IN THE RECIPE FILE.
GDDR6_HYNIX	STUFFS HYNIX GDDR6
GDDR6_SAMSUNG	STUFFS SAMSUNG GDDR6
PCB_GI	FAB TYPE: GOLD
PCB_HG	FAB TYPE: HARD GOLD, RAISED PADS. FOR SOCKETED BOARDS
PCB_OSP	FAB TYPE: ORGANIC SOLDERABILITY PRESERVATIVE GREEN SOLDERMASK
RETAIL	COMPONENTS STUFFED FOR A RETAIL CONSOLE. DO NOT USE WITH DEBUG
RF	STUFFS 2.4/5GHZ FILTERS FOR DESENSE MITIGATION
RTC_RETAIL	RTC CIRCUIT IMPLEMENTATION FOR RETAIL BOARDS
RTC_XDK	RTC CIRCUIT IMPLEMENTATION FOR XDK BOARDS
SOC_BASE	DUMMY PLACE HOLDER FOR SOC. NEVER USE THIS IN THE RECIPE FILE.
SOC_EMPTY	DOES NOT STUFF ARDEN
SOC_INCLUDE	STUFFS ARDEN
SPI_FLASH_BASE	DUMMY PLACE HOLDER FOR SPI FLASH. NEVER USE THIS IN THE RECIPE FILE.
SPI_FLASH_MACRONIX	STUFFS MACRONIX SPI FLASH
SPI_FLASH_WINBOND	STUFFS WINBOND SPI FLASH
VR_FIXED	SET ALL VRS TO FIXED VOLTAGES (NON-MARGINED). EXCLUDES V_MEMIO
VR_HEATSINK	STUFFS PEMNUTS FOR MOUNTING VRM HEATSINK (BARE PCBAS ONLY)
INDUCTOR_CORE_BASE	DUMMY PLACE HOLDER FOR HIGH POWER SOC INDUCTORS. NEVER USE THIS IN THE RECIPE FILE
INDUCTOR_CORE_CHILISIN	STUFFS CHILISIN INDUCTORS FOR HIGH POWER SOC DOMAINS
INDUCTOR_CORE_EATON	STUFFS EATON INUDCTORS FOR HIGH POWER SOC DOMAINS
INDUCTOR_CORE_SUNLORD	STUFFS SUNLORD INUDCTORS FOR HIGH POWER SOC DOMAINS
VR_GFXCPU_BASE	DUMMY PLACE HOLDER FOR GFX/CPU POWER STAGES. NEVER USE THIS IN THE RECIPE FILE
VR_GFXCPU_MP86955	STUFFS GFX/CPU POWER STAGES WITH THE MP86955 (8" WAFER QUAL)
VR_GFXCPU_MP86965	STUFFS GFX/CPU POWER STAGES WITH THE MP86955 (12" WAFER QUAL)
XTAL_25MHZ_BASE	DUMMY PLACE HOLDER FOR 25MHZ XTAL. NEVER USE THIS IN THE RECIPE FILE
XTAL_25MHZ_KDS	STUFFS 25MHZ XTAL WITH THE KDS PART
XTAL_25MHZ_NDK	STUFFS 25MHZ XTAL WITH THE NDK PART
XTAL_25MHZ_TXC	STUFFS 25MHZ XTAL WITH THE TXC PART
HDMI_LOAD_SWITCH_BASE	DUMMY PLACE HOLDER FOR HDMI LOAD SWITCH. NEVER USE THIS IN THE RECIPE FILE
HDMI_LOAD_SWITCH_DIODES	STUFFS HDMI LOAD SWITCH WITH DIODES INC QUAL PART
HDMI_LOAD_SWITCH_ST	STUFFS HDMI LOAD SWITCH WITH STMICRO QUAL PART
HDMI_LOAD_SWITCH_TI	STUFFS HDMI LOAD SWITCH WITH TEXAS INSTRUMENTS QUAL PART
VR_MEMSOC_BASE	DUMMY PLACE HOLDER FOR MEMIO/MEMPHY/SOC POWER STAGES. NEVER USE THIS IN THE RECIPE FILE
VR_MEMSOC_MP86910C	STUFFS MEMIO/MEMPHY/SOC POWER STAGES WITH THE MP86910C (8" WAFER QUAL)
VR_MEMSOC_MP86912C	STUFFS MEMIO/MEMPHY/SOC POWER STAGES WITH THE MP86912C (12" WAFER QUAL)