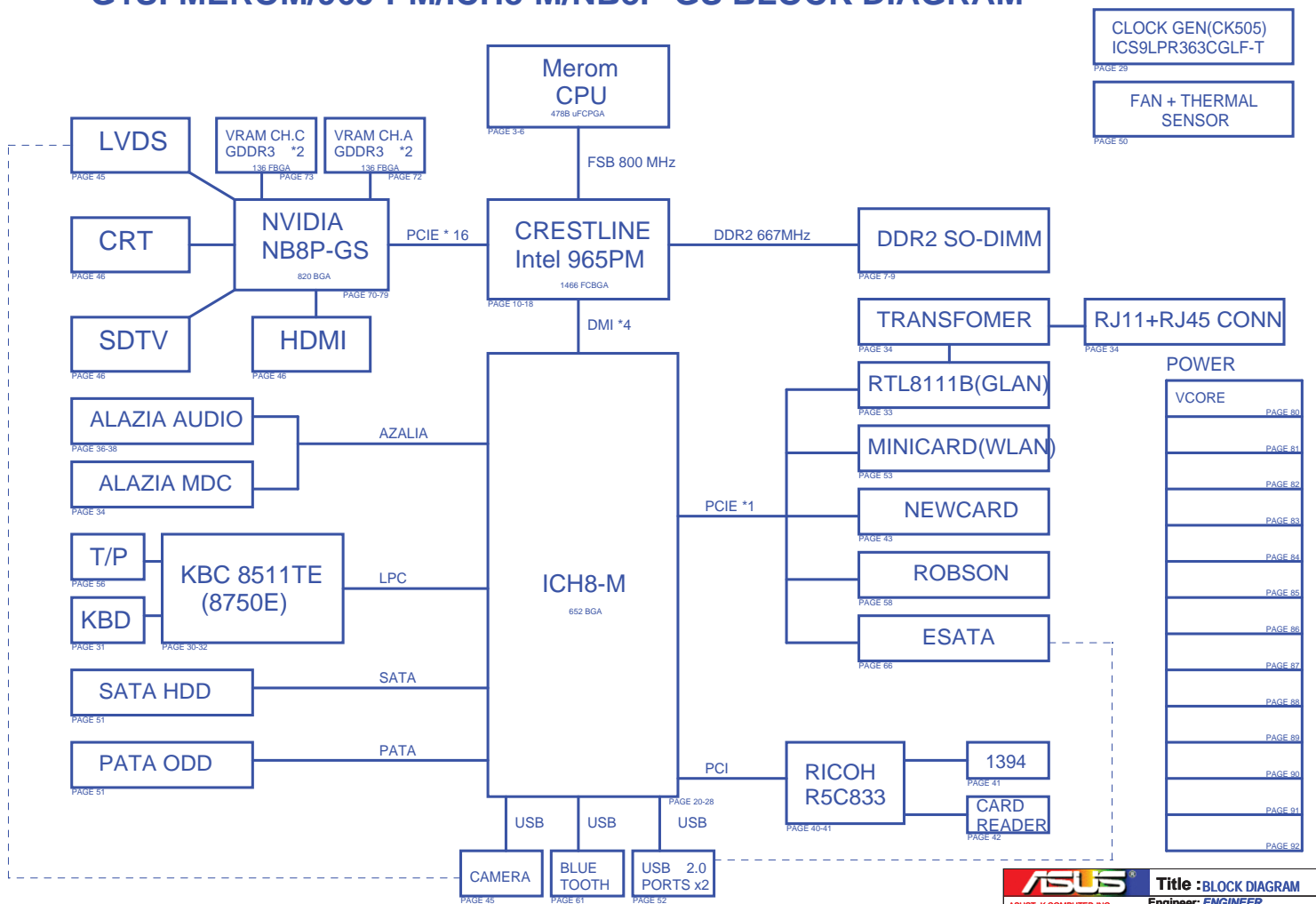
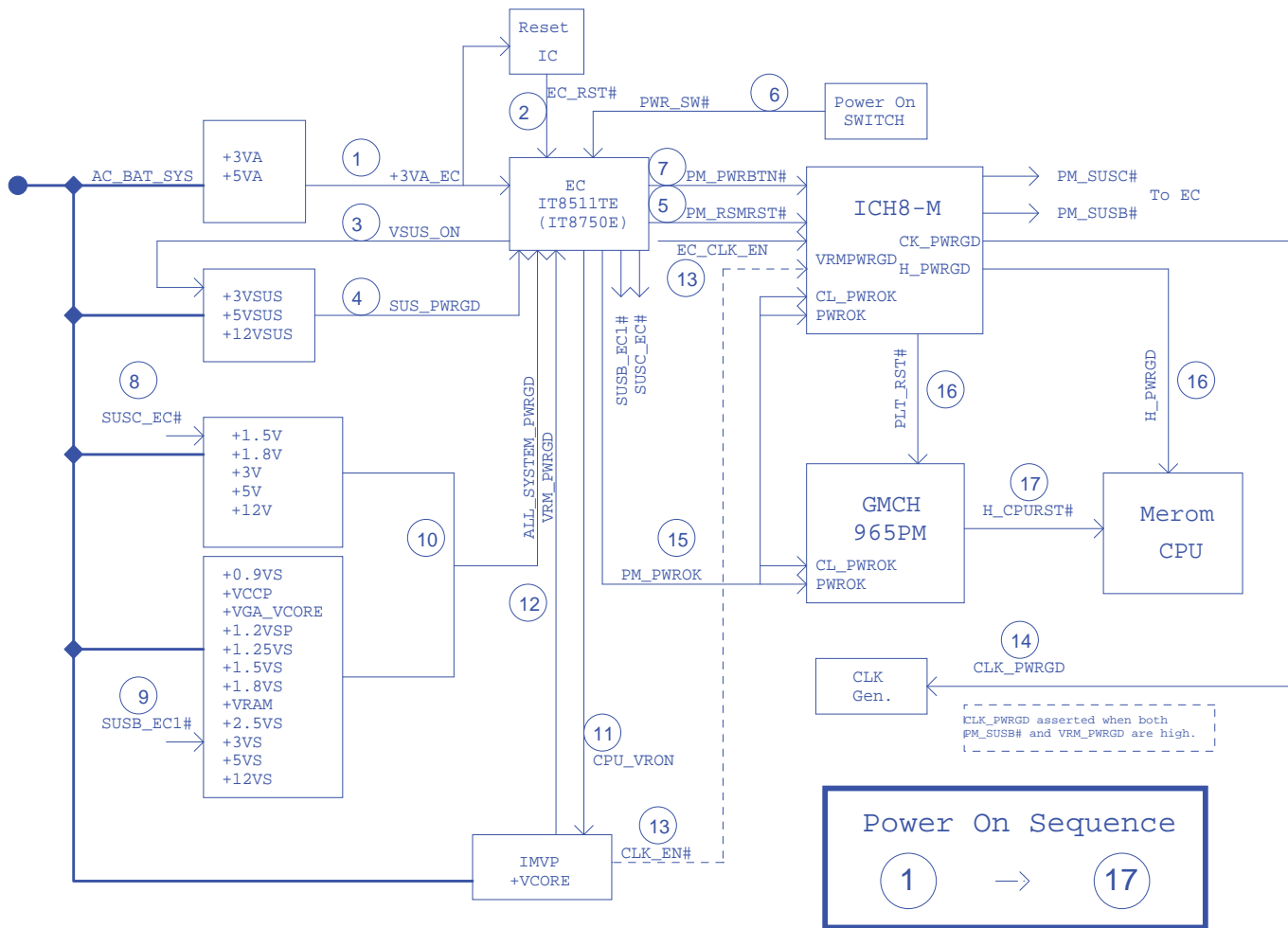
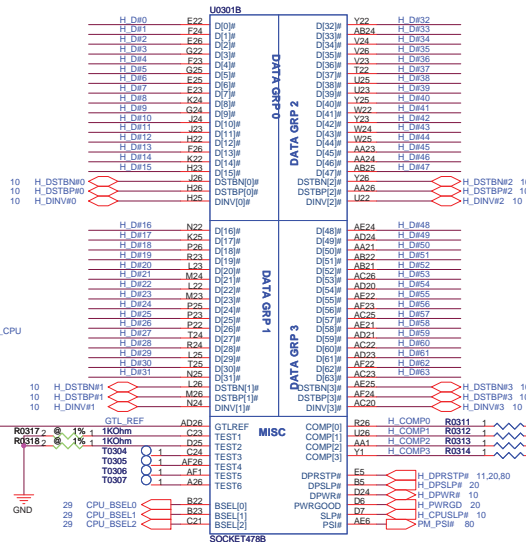


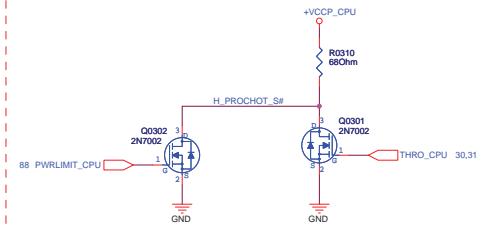
G1S: MEROM/965-PM/ICH8-M/NB8P-GS BLOCK DIAGRAM

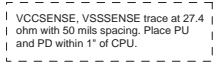


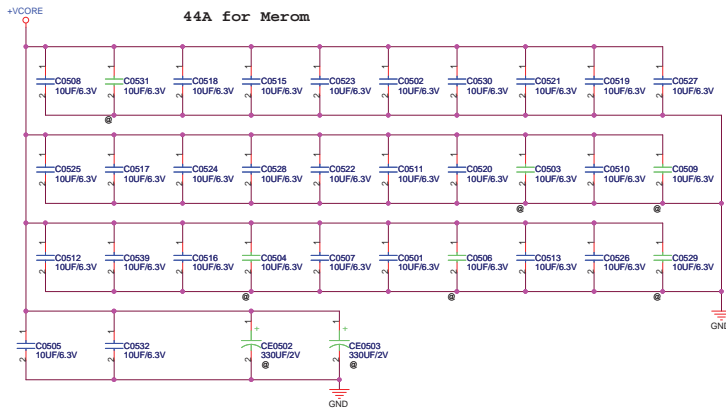




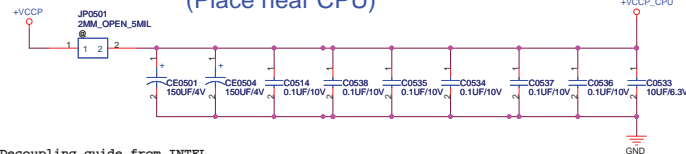
A circuit diagram showing four resistors connected in parallel to a common ground. Each resistor is labeled with a value of 1%. The ground is represented by a standard ground symbol and the label 'GND'.





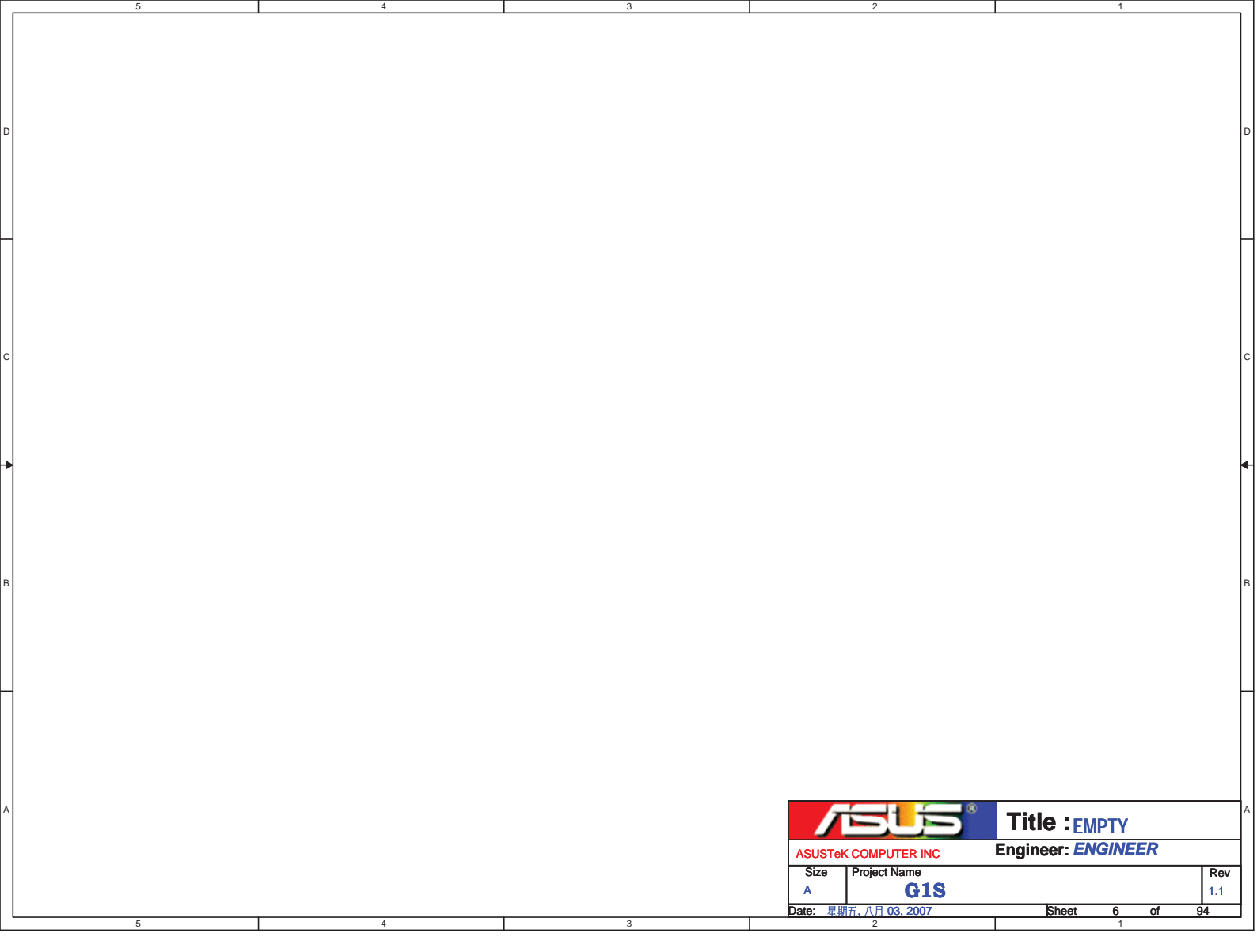



+VCCP Decoupling Capacitor (Place near CPU)



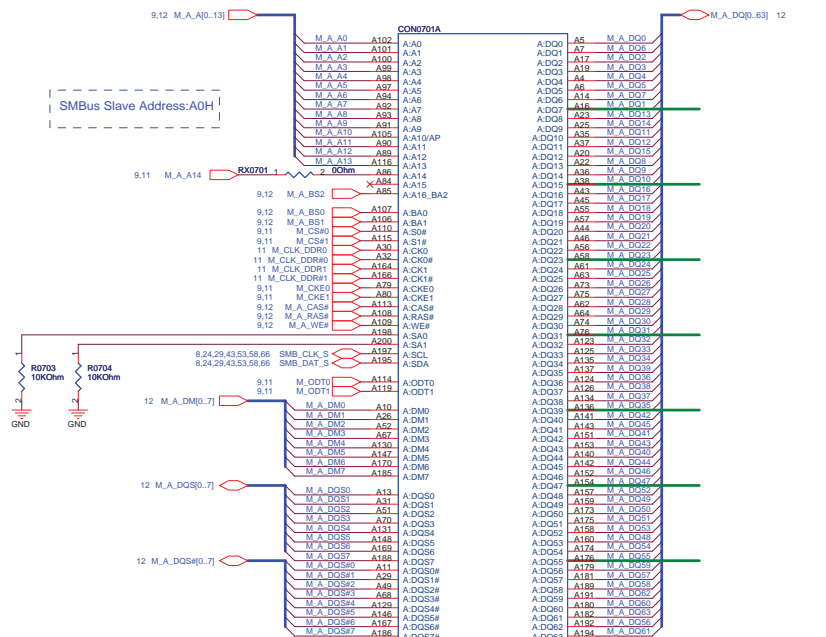
Decoupling guide from INTEL

VCORE 22uF/10V	* 32pcs
330uF/2V	* 6pcs
VCCP 0.1uF	* 6pcs for CPU
150uF	* 1pcs for CPU

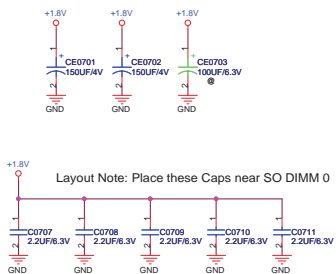


		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: <i>ENGINEER</i>	
Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet 6 of 94	

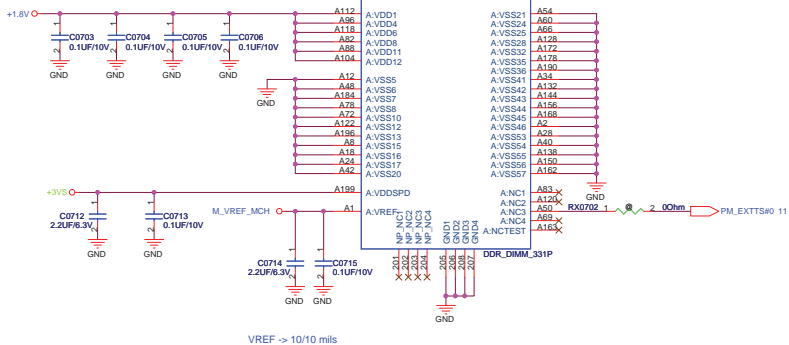
Address reference +1.8V, add four 0.1uF decoupling CAP.



Layout Note: Place these Caps near SO DIMM 0

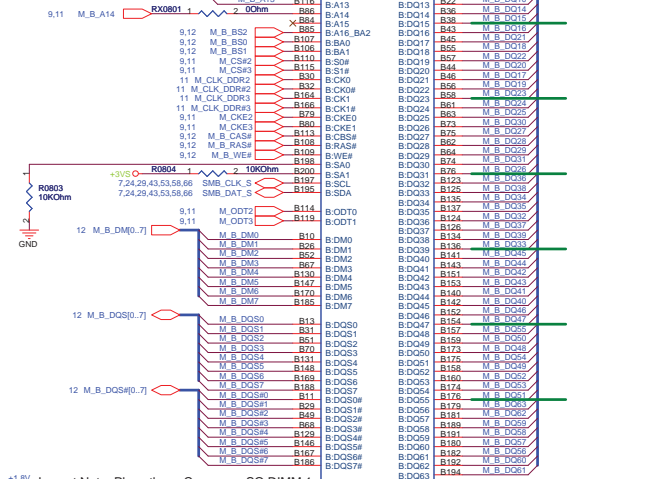


SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1

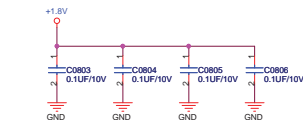


Address reference +1.8V, add four
0.1uF decoupling CAP.

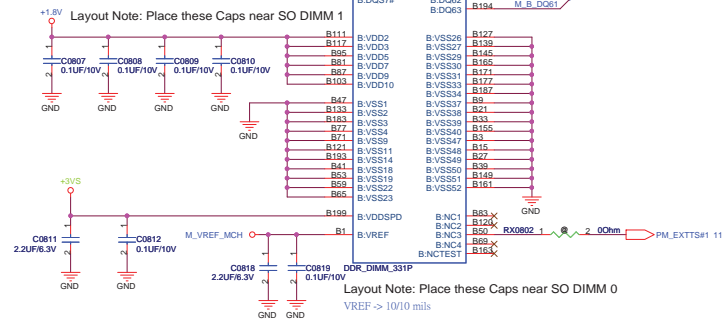
SMBus Slave Address:A4H



Layout Note: Place these High-Freq decoupling Caps near the GMCH

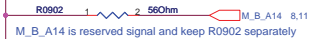
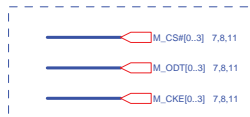


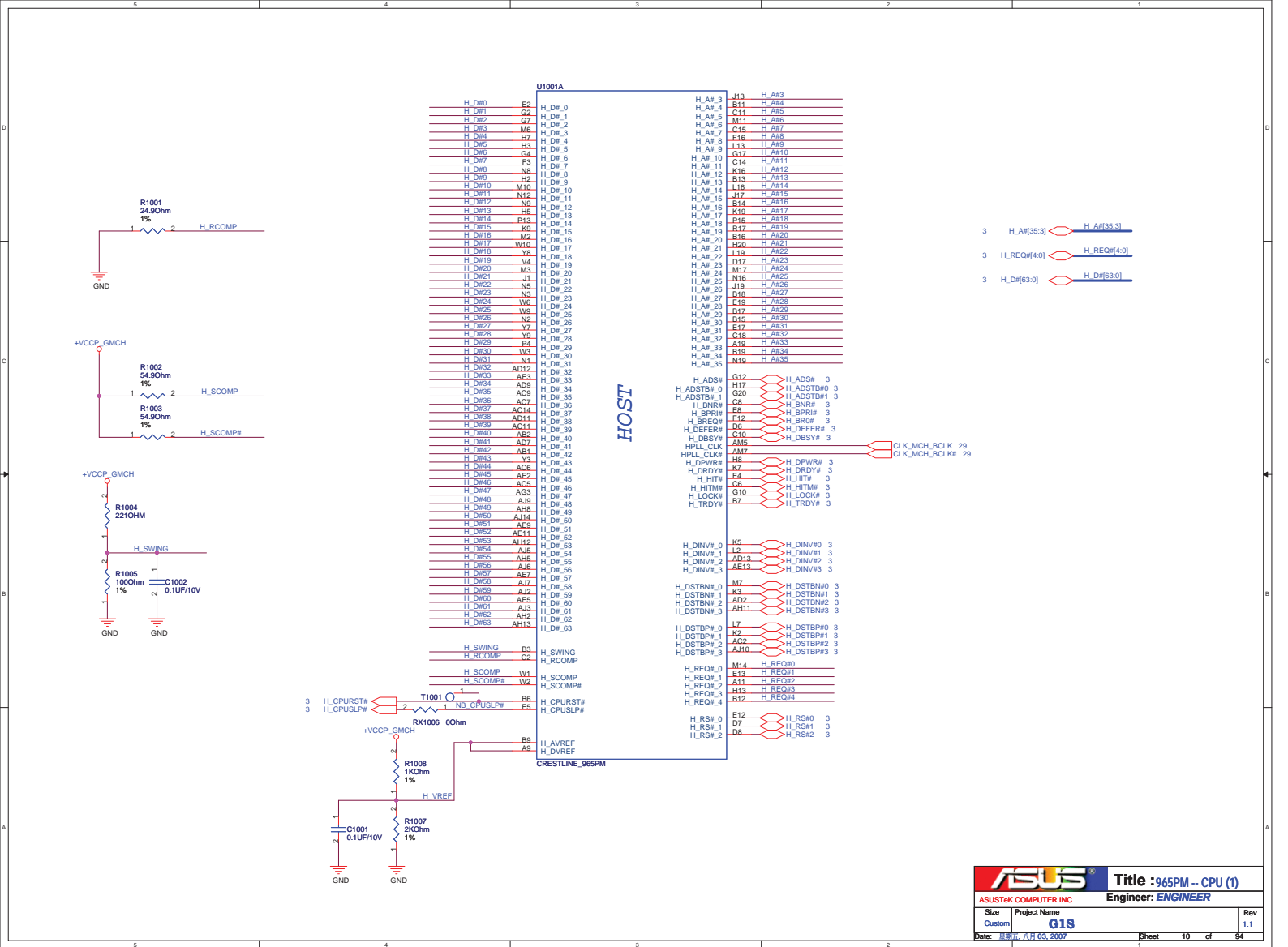
Layout Note: Place these CAPs near the GMCH

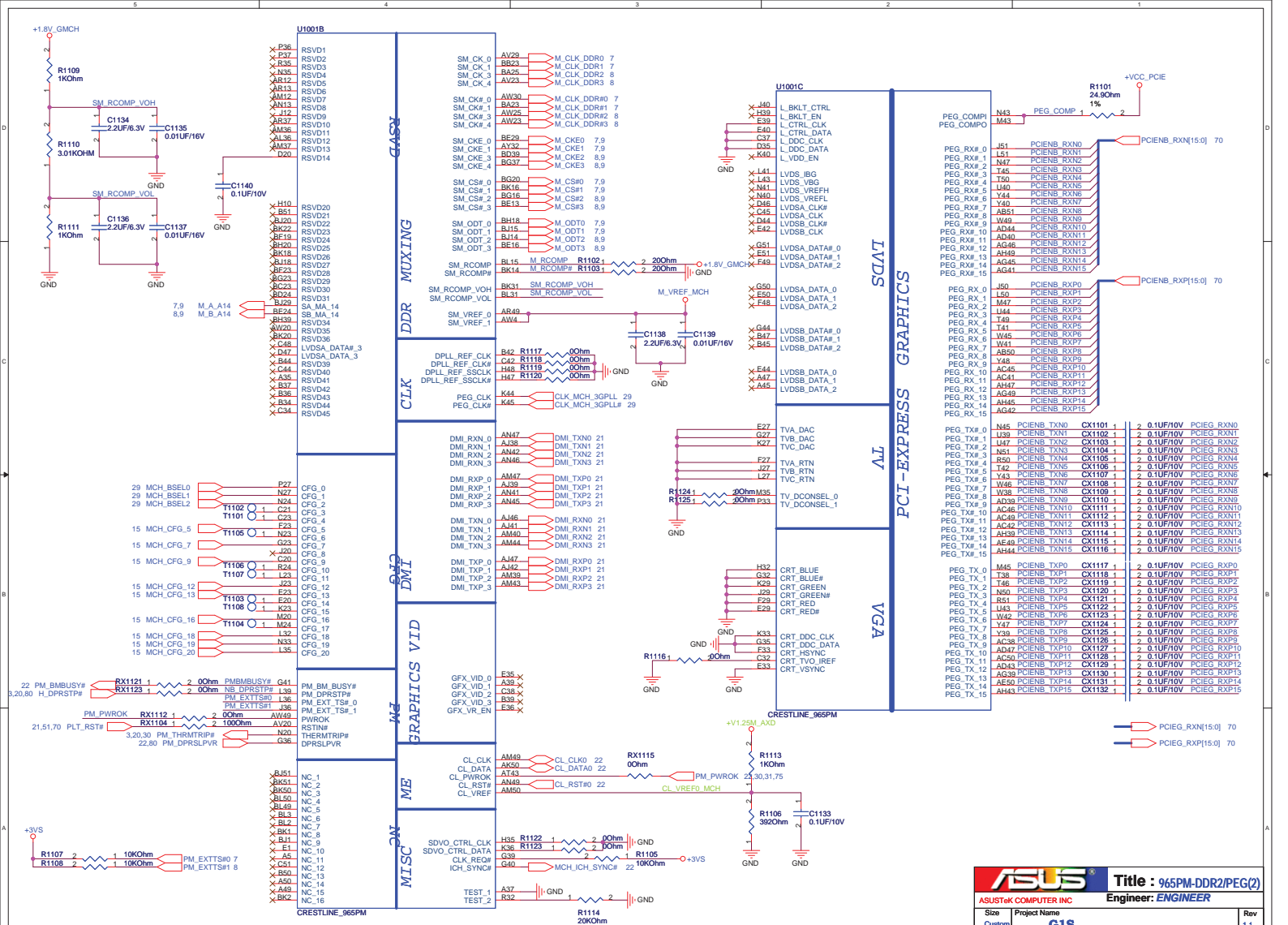


VREF -> 10/10 mils

HAD SWAPED







7 M_A_DQ[0:63]

U1001D
M_A_DQ0 AR43 SA, DO_0
M_A_DQ1 AR44 SA, DO_1
M_A_DQ2 AR45 SA, DO_2
M_A_DQ3 AV46 SA, DO_3
M_A_DQ4 AR41 SA, DO_4
M_A_DQ5 AR45 SA, DO_5
M_A_DQ6 AT42 SA, DO_6
M_A_DQ7 AW47 SA, DO_7
M_A_DQ8 BR45 SA, DO_8
M_A_DQ9 BF48 SA, DO_9
M_A_DQ10 BC47 SA, DO_10
M_A_DQ11 BJ45 SA, DO_11
M_A_DQ12 BR47 SA, DO_12
M_A_DQ13 BG40 SA, DO_13
M_A_DQ14 BR49 SA, DO_14
M_A_DQ15 BE45 SA, DO_15
M_A_DQ16 AW43 SA, DO_16
M_A_DQ17 BE44 SA, DO_17
M_A_DQ18 BG42 SA, DO_18
M_A_DQ19 BE40 SA, DO_19
M_A_DQ20 BF44 SA, DO_20
M_A_DQ21 BR45 SA, DO_21
M_A_DQ22 BG40 SA, DO_22
M_A_DQ23 BF40 SA, DO_23
M_A_DQ24 AR40 SA, DO_24
M_A_DQ25 AW40 SA, DO_25
M_A_DQ26 AT39 SA, DO_26
M_A_DQ27 AW36 SA, DO_27
M_A_DQ28 AW41 SA, DO_28
M_A_DQ29 AV41 SA, DO_29
M_A_DQ30 AV38 SA, DO_30
M_A_DQ31 AT38 SA, DO_31
M_A_DQ32 AV13 SA, DO_32
M_A_DQ33 AT13 SA, DO_33
M_A_DQ34 AW11 SA, DO_34
M_A_DQ35 AV11 SA, DO_35
M_A_DQ36 AV15 SA, DO_36
M_A_DQ37 AT14 SA, DO_37
M_A_DQ38 BA13 SA, DO_38
M_A_DQ39 BA11 SA, DO_39
M_A_DQ40 BE10 SA, DO_40
M_A_DQ41 BD10 SA, DO_41
M_A_DQ42 BD8 SA, DO_42
M_A_DQ43 A19 SA, DO_43
M_A_DQ44 BG10 SA, DO_44
M_A_DQ45 AW9 SA, DO_45
M_A_DQ46 BD7 SA, DO_46
M_A_DQ47 BR9 SA, DO_47
M_A_DQ48 BR5 SA, DO_48
M_A_DQ49 AV7 SA, DO_49
M_A_DQ50 AT5 SA, DO_50
M_A_DQ51 AT7 SA, DO_51
M_A_DQ52 AV6 SA, DO_52
M_A_DQ53 BR7 SA, DO_53
M_A_DQ54 AR5 SA, DO_54
M_A_DQ55 AR8 SA, DO_55
M_A_DQ56 AR9 SA, DO_56
M_A_DQ57 AN3 SA, DO_57
M_A_DQ58 AM5 SA, DO_58
M_A_DQ59 AN10 SA, DO_59
M_A_DQ60 AT9 SA, DO_60
M_A_DQ61 AN2 SA, DO_61
M_A_DQ62 AM9 SA, DO_62
M_A_DQ63 AN11 SA, DO_63

CRESTLINE_965PM

DDR SYSTEM MEMORY A

SA_BS_0 BB19 M_A_BS0 7.9
SA_BS_1 BA15 M_A_BS1 7.9
SA_BS_2 BF22 M_A_BS2 7.9
SA_CAS# BL17 M_A_CAS# 7.9
SA_DM_0 AT45 M_A_DM0
SA_DM_1 BD44 M_A_DM1
SA_DM_2 BD42 M_A_DM2
SA_DM_3 AW38 M_A_DM3
SA_DM_4 AW13 M_A_DM4
SA_DM_5 BG38 M_A_DM5
SA_DM_6 A15 M_A_DM6
SA_DM_7 AN6 M_A_DM7
SA_DQS_0 AT46 M_A_DQS0
SA_DQS_1 BE48 M_A_DQS1
SA_DQS_2 BR43 M_A_DQS2
SA_DQS_3 BC37 M_A_DQS3
SA_DQS_4 BR16 M_A_DQS4
SA_DQS_5 BR46 M_A_DQS5
SA_DQS_6 BR2 M_A_DQS6
SA_DQS_7 AP3 M_A_DQS7
SA_DQS8_0 AT47 M_A_DQS8_0
SA_DQS8_1 BD47 M_A_DQS8_1
SA_DQS8_2 BC41 M_A_DQS8_2
SA_DQS8_3 BA37 M_A_DQS8_3
SA_DQS8_4 BA16 M_A_DQS8_4
SA_DQS8_5 BH7 M_A_DQS8_5
SA_DQS8_6 BC1 M_A_DQS8_6
SA_DQS8_7 AF2 M_A_DQS8_7
SA_MA_0 BJ19 M_A_A0
SA_MA_1 BD20 M_A_A1
SA_MA_2 BK27 M_A_A2
SA_MA_3 BK28 M_A_A3
SA_MA_4 BL24 M_A_A4
SA_MA_5 BK28 M_A_A5
SA_MA_6 BJ27 M_A_A6
SA_MA_7 BJ25 M_A_A7
SA_MA_8 BL28 M_A_A8
SA_MA_9 BA28 M_A_A9
SA_MA_10 BC19 M_A_A10
SA_MA_11 BE28 M_A_A11
SA_MA_12 BC30 M_A_A12
SA_MA_13 BJ16 M_A_A13
SA_RAS# BE18 M_A_RAS# 7.9
SA_RCVEN# AY23 M_A_RCVEN# 7.9
SA_WE# BA19 M_A_WE# 7.9

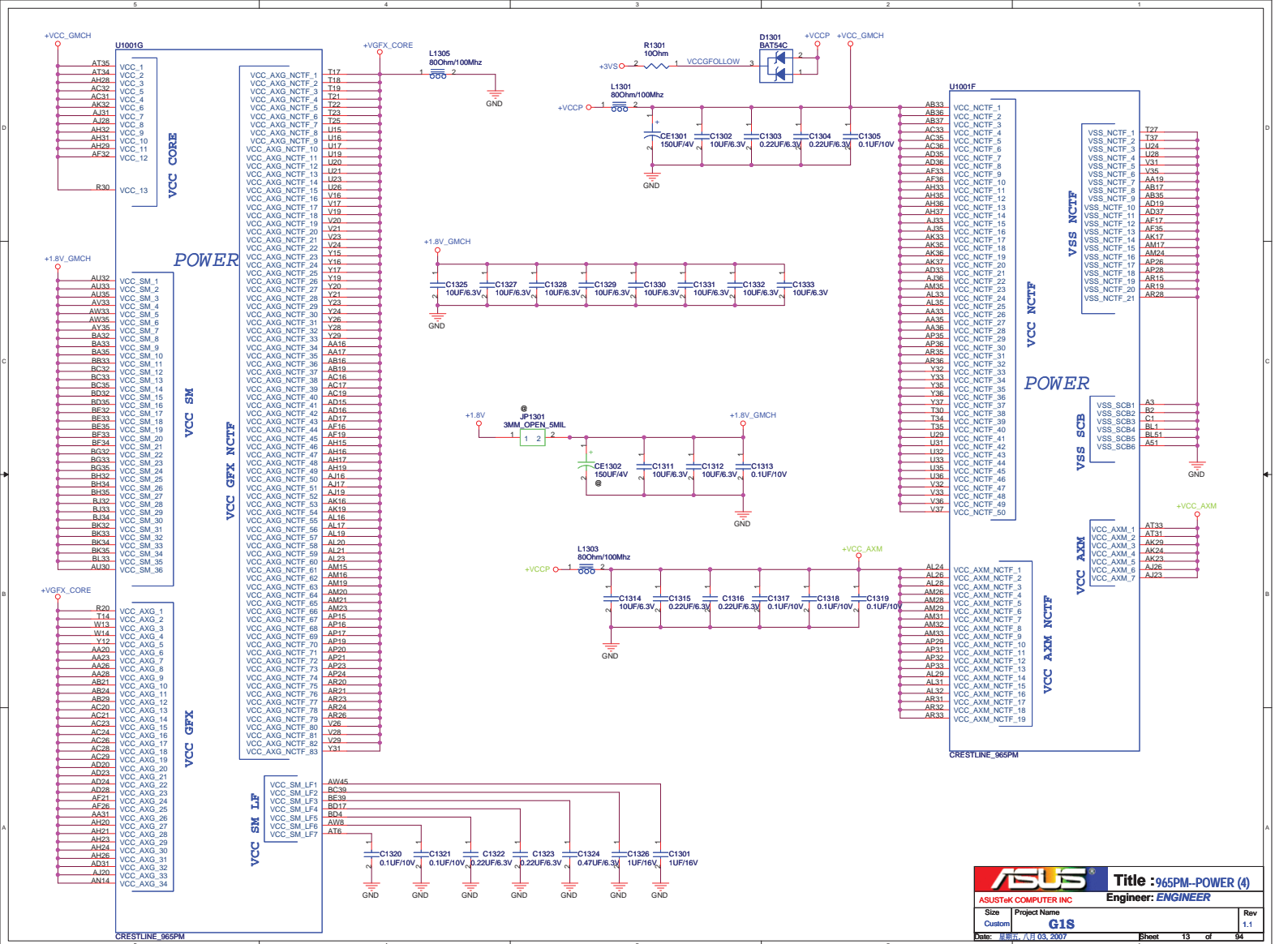
8 M_B_DQ[0:63]


U1001E
M_B_DQ0 AP49 SB, DO_0
M_B_DQ1 AW50 SB, DO_1
M_B_DQ2 AW50 SB, DO_2
M_B_DQ3 AW51 SB, DO_3
M_B_DQ4 AN51 SB, DO_4
M_B_DQ5 AN50 SB, DO_5
M_B_DQ6 AV50 SB, DO_6
M_B_DQ7 AV49 SB, DO_7
M_B_DQ8 BA50 SB, DO_8
M_B_DQ9 BR50 SB, DO_9
M_B_DQ10 BA49 SB, DO_10
M_B_DQ11 BE50 SB, DO_11
M_B_DQ12 BA51 SB, DO_12
M_B_DQ13 AV49 SB, DO_13
M_B_DQ14 BE50 SB, DO_14
M_B_DQ15 BE49 SB, DO_15
M_B_DQ16 BJ50 SB, DO_16
M_B_DQ17 BJ44 SB, DO_17
M_B_DQ18 BJ43 SB, DO_18
M_B_DQ19 BR43 SB, DO_19
M_B_DQ20 BK47 SB, DO_20
M_B_DQ21 BK49 SB, DO_21
M_B_DQ22 BK43 SB, DO_22
M_B_DQ23 BK42 SB, DO_23
M_B_DQ24 BJ41 SB, DO_24
M_B_DQ25 BL41 SB, DO_25
M_B_DQ26 BJ37 SB, DO_26
M_B_DQ27 BJ36 SB, DO_27
M_B_DQ28 BK41 SB, DO_28
M_B_DQ29 BJ40 SB, DO_29
M_B_DQ30 BL35 SB, DO_30
M_B_DQ31 BK37 SB, DO_31
M_B_DQ32 BK13 SB, DO_32
M_B_DQ33 BE11 SB, DO_33
M_B_DQ34 BK11 SB, DO_34
M_B_DQ35 BC11 SB, DO_35
M_B_DQ36 BK12 SB, DO_36
M_B_DQ37 BE12 SB, DO_37
M_B_DQ38 BC12 SB, DO_38
M_B_DQ39 BG12 SB, DO_39
M_B_DQ40 BJ10 SB, DO_40
M_B_DQ41 BL9 SB, DO_41
M_B_DQ42 BK5 SB, DO_42
M_B_DQ43 BL5 SB, DO_43
M_B_DQ44 BK9 SB, DO_44
M_B_DQ45 BK10 SB, DO_45
M_B_DQ46 BL8 SB, DO_46
M_B_DQ47 BL6 SB, DO_47
M_B_DQ48 BR4 SB, DO_48
M_B_DQ49 BH5 SB, DO_49
M_B_DQ50 BG1 SB, DO_50
M_B_DQ51 BC2 SB, DO_51
M_B_DQ52 BK3 SB, DO_52
M_B_DQ53 BE4 SB, DO_53
M_B_DQ54 BD3 SB, DO_54
M_B_DQ55 BL2 SB, DO_55
M_B_DQ56 BA3 SB, DO_56
M_B_DQ57 BL3 SB, DO_57
M_B_DQ58 AR1 SB, DO_58
M_B_DQ59 AT3 SB, DO_59
M_B_DQ60 AV2 SB, DO_60
M_B_DQ61 AY3 SB, DO_61
M_B_DQ62 AU2 SB, DO_62
M_B_DQ63 AT2 SB, DO_63

DDR SYSTEM MEMORY B

SB_BS_0 AY17 M_B_BS0 8.9
SB_BS_1 BG18 M_B_BS1 8.9
SB_BS_2 BG36 M_B_BS2 8.9
SB_CAS# BE17 M_B_CAS# 8.9
SB_DM_0 AR50 M_B_DM0
SB_DM_1 BD49 M_B_DM1
SB_DM_2 BK45 M_B_DM2
SB_DM_3 BL39 M_B_DM3
SB_DM_4 BH12 M_B_DM4
SB_DM_5 BJ7 M_B_DM5
SB_DM_6 BF3 M_B_DM6
SB_DM_7 AW2 M_B_DM7
SB_DQS_0 AT50 M_B_DQS0
SB_DQS_1 BD50 M_B_DQS1
SB_DQS_2 BK46 M_B_DQS2
SB_DQS_3 BK39 M_B_DQS3
SB_DQS_4 BL12 M_B_DQS4
SB_DQS_5 BL7 M_B_DQS5
SB_DQS_6 BE2 M_B_DQS6
SB_DQS_7 AV2 M_B_DQS7
SB_DQS8_0 AU50 M_B_DQS8_0
SB_DQS8_1 BC50 M_B_DQS8_1
SB_DQS8_2 BL45 M_B_DQS8_2
SB_DQS8_3 BK38 M_B_DQS8_3
SB_DQS8_4 BK12 M_B_DQS8_4
SB_DQS8_5 BK1 M_B_DQS8_5
SB_DQS8_6 BF2 M_B_DQS8_6
SB_DQS8_7 AV3 M_B_DQS8_7
SB_MA_0 BC18 M_B_A0
SB_MA_1 BG28 M_B_A1
SB_MA_2 BG25 M_B_A2
SB_MA_3 AW17 M_B_A3
SB_MA_4 BE25 M_B_A4
SB_MA_5 BA29 M_B_A5
SB_MA_6 BC28 M_B_A6
SB_MA_7 AY28 M_B_A7
SB_MA_8 BD37 M_B_A8
SB_MA_9 BG17 M_B_A9
SB_MA_10 BE37 M_B_A10
SB_MA_11 BA39 M_B_A11
SB_MA_12 BG13 M_B_A12
SB_MA_13
SB_RAS# AV16 M_B_RAS# 8.9
SB_RCVEN# AY15 M_B_RCVEN# 8.9
SB_WE# BC17 M_B_WE# 8.9

CRESTLINE_965PM



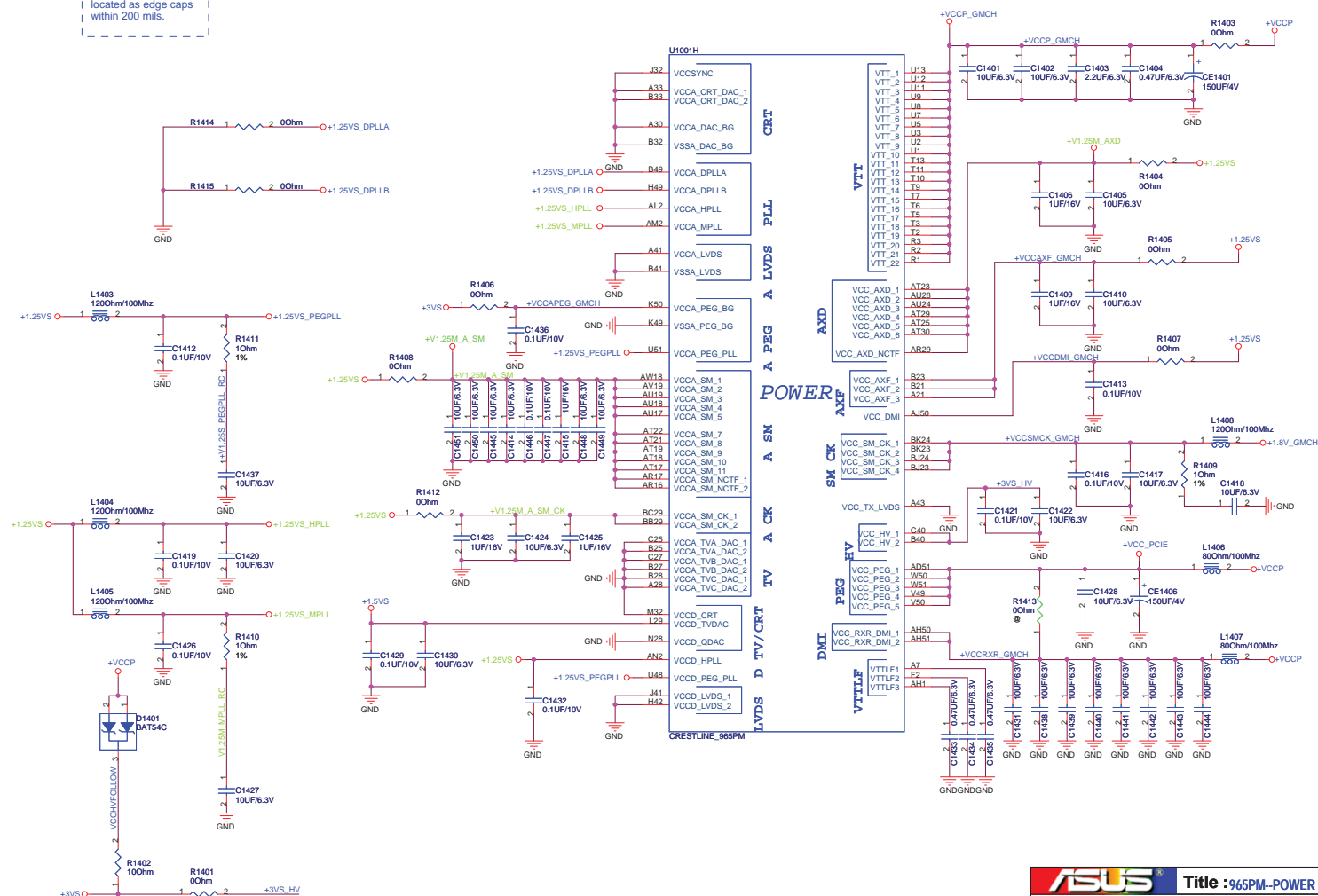


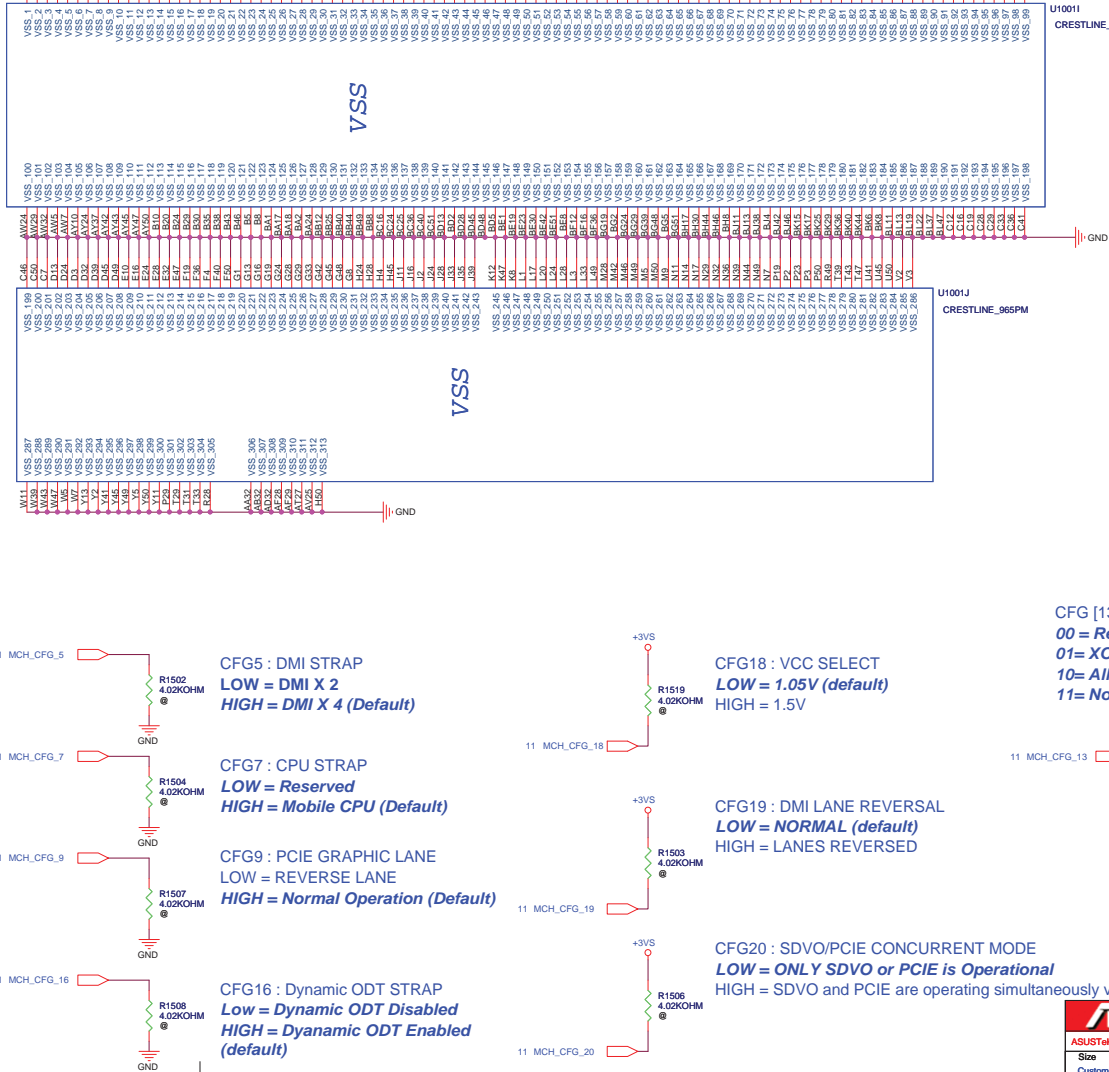
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Engineer: ENGINEER

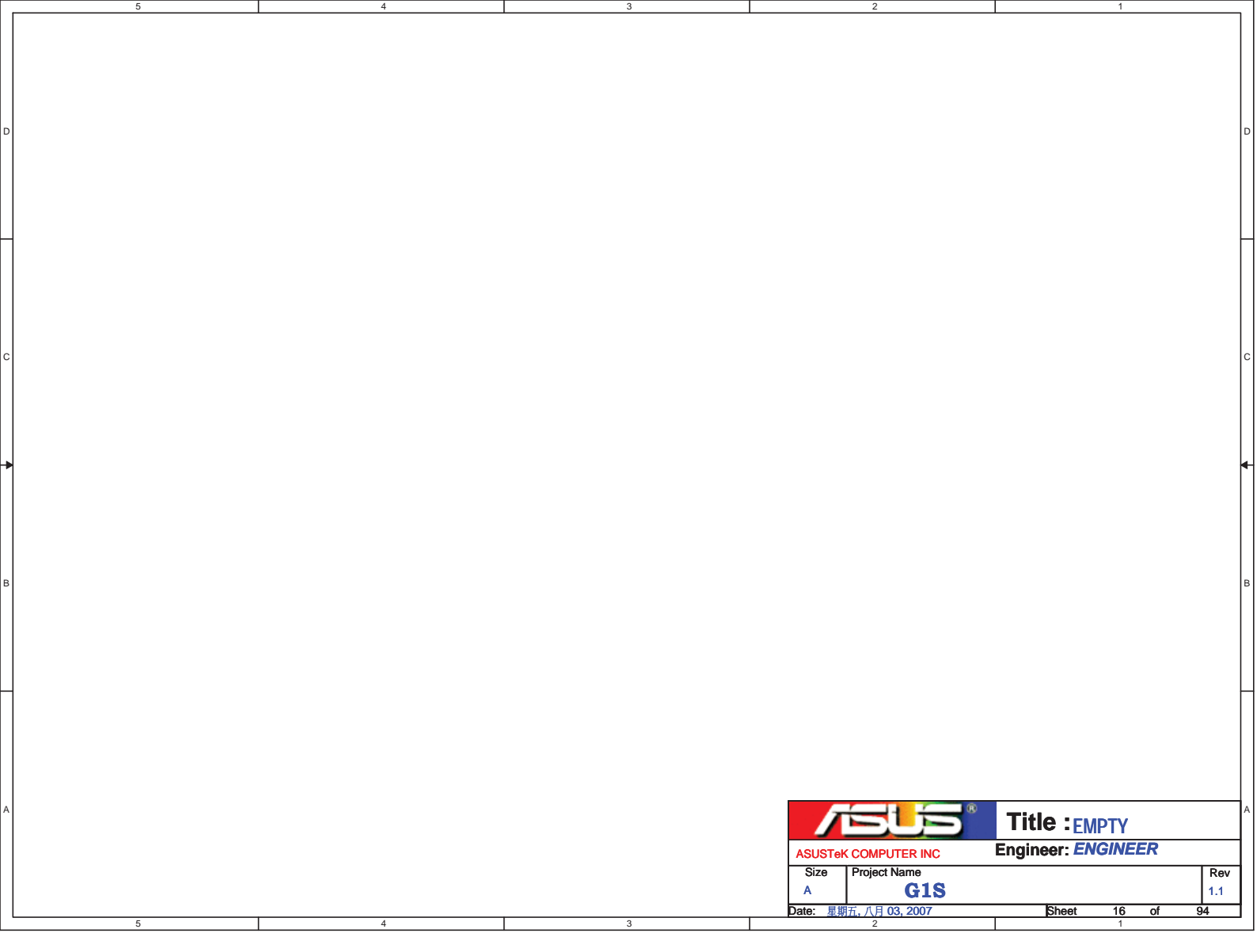
Size	Project Name	Rev
Custom	G1S	1.1


Date: 2007/03/03 13:00 Sheet 13 of 94

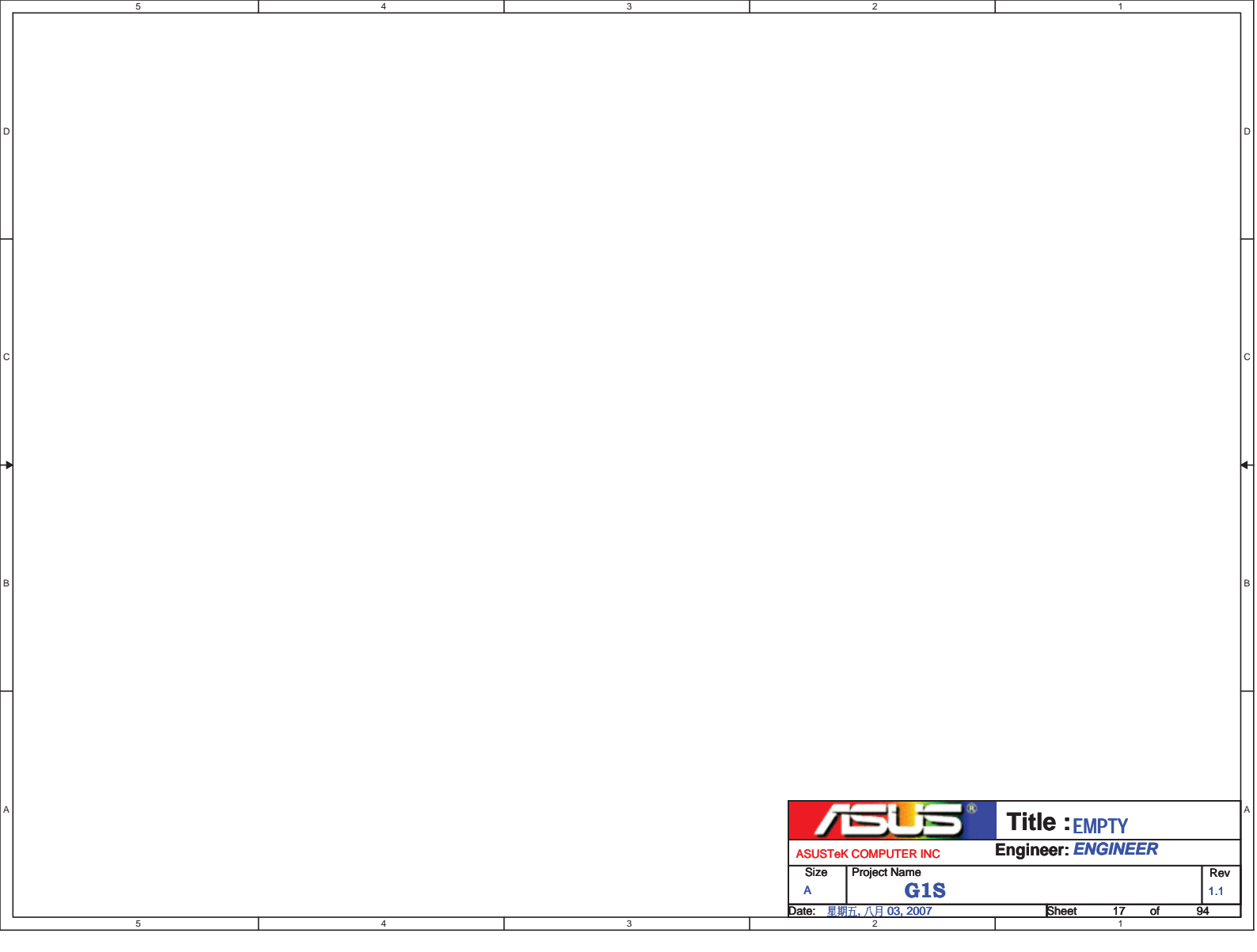
NOTE: 0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.




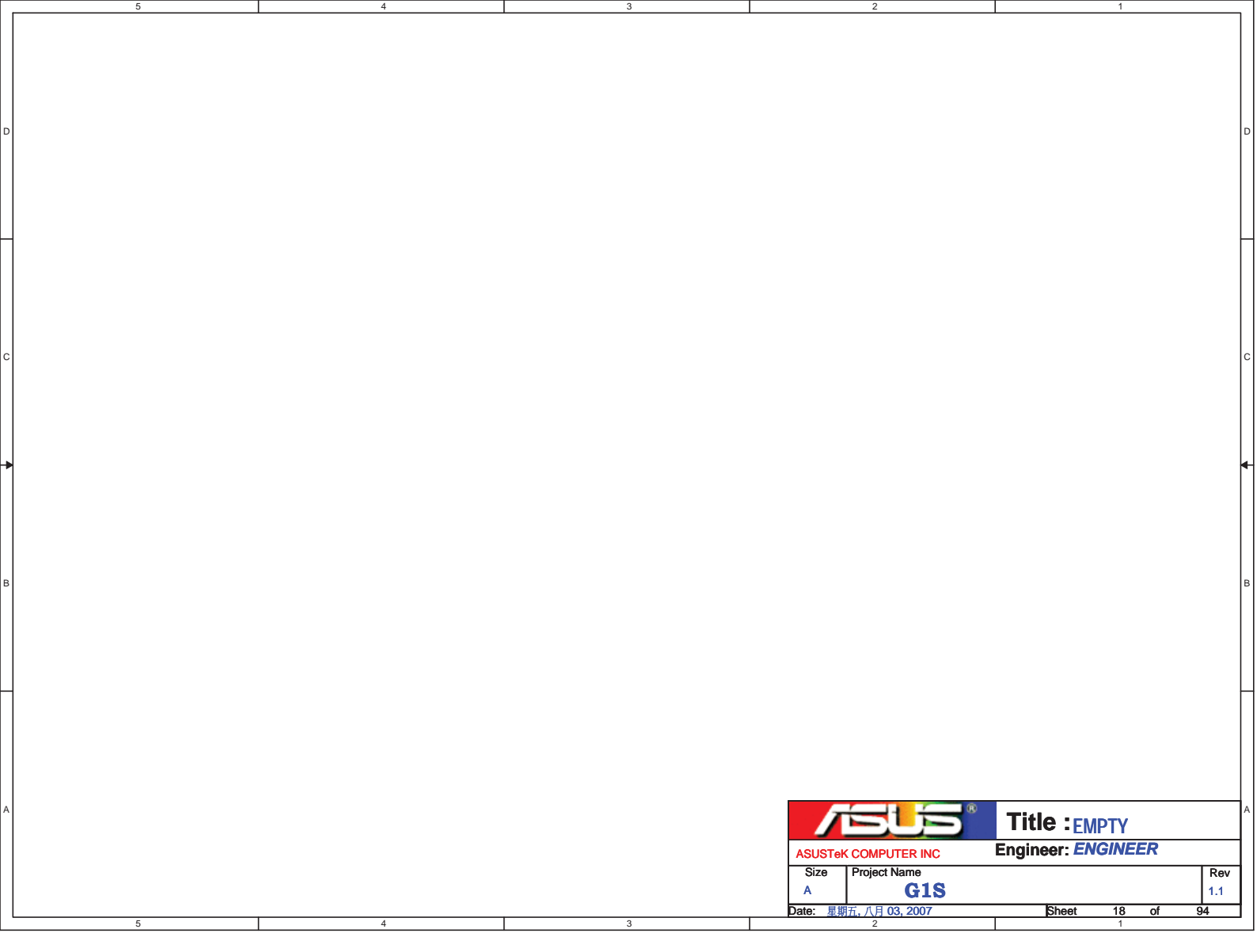





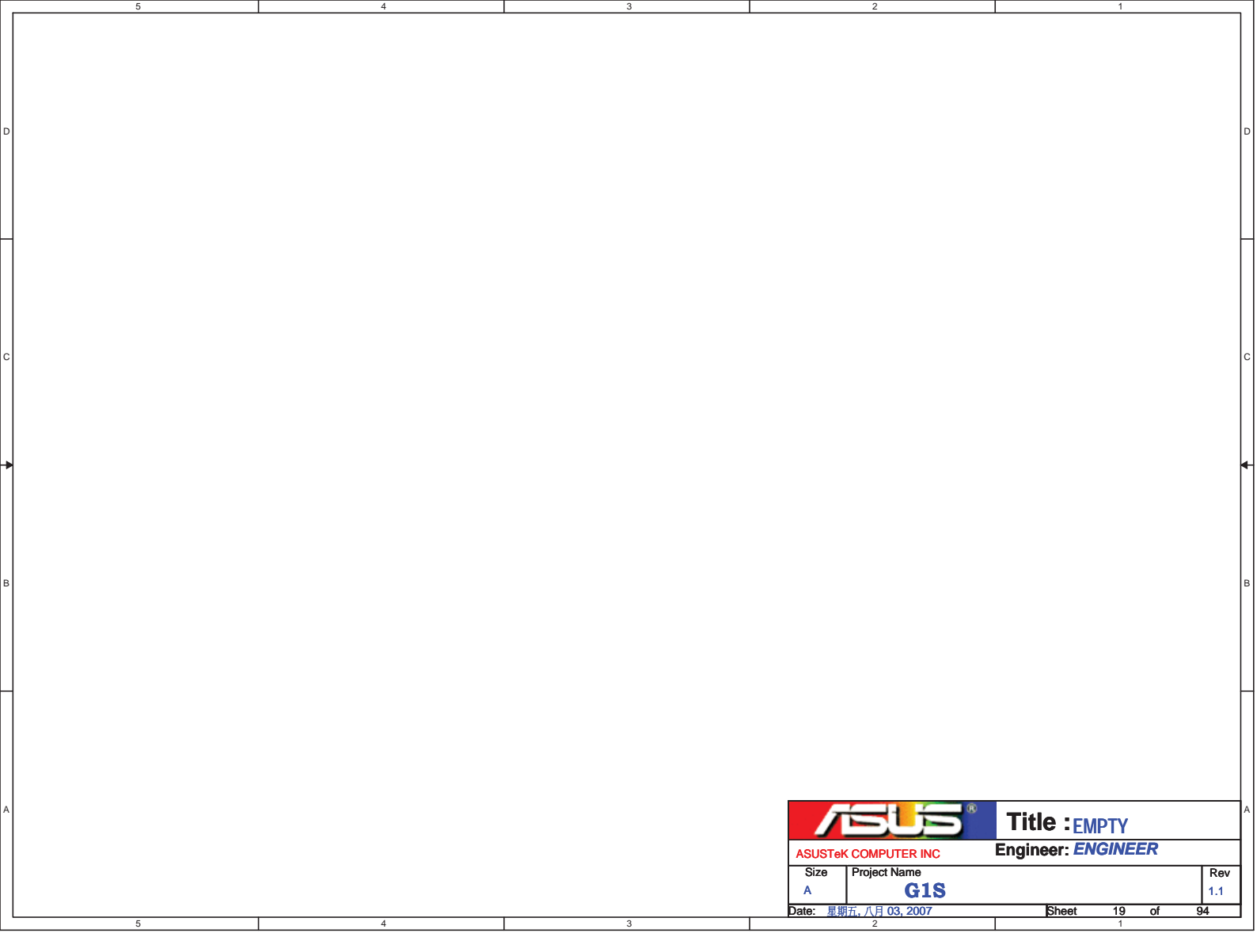
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ASUSTeK COMPUTER INC		Engineer: <i>ENGINEER</i>	
Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	16 of 94




		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: <i>ENGINEER</i>	
Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	17 of 94

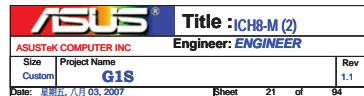


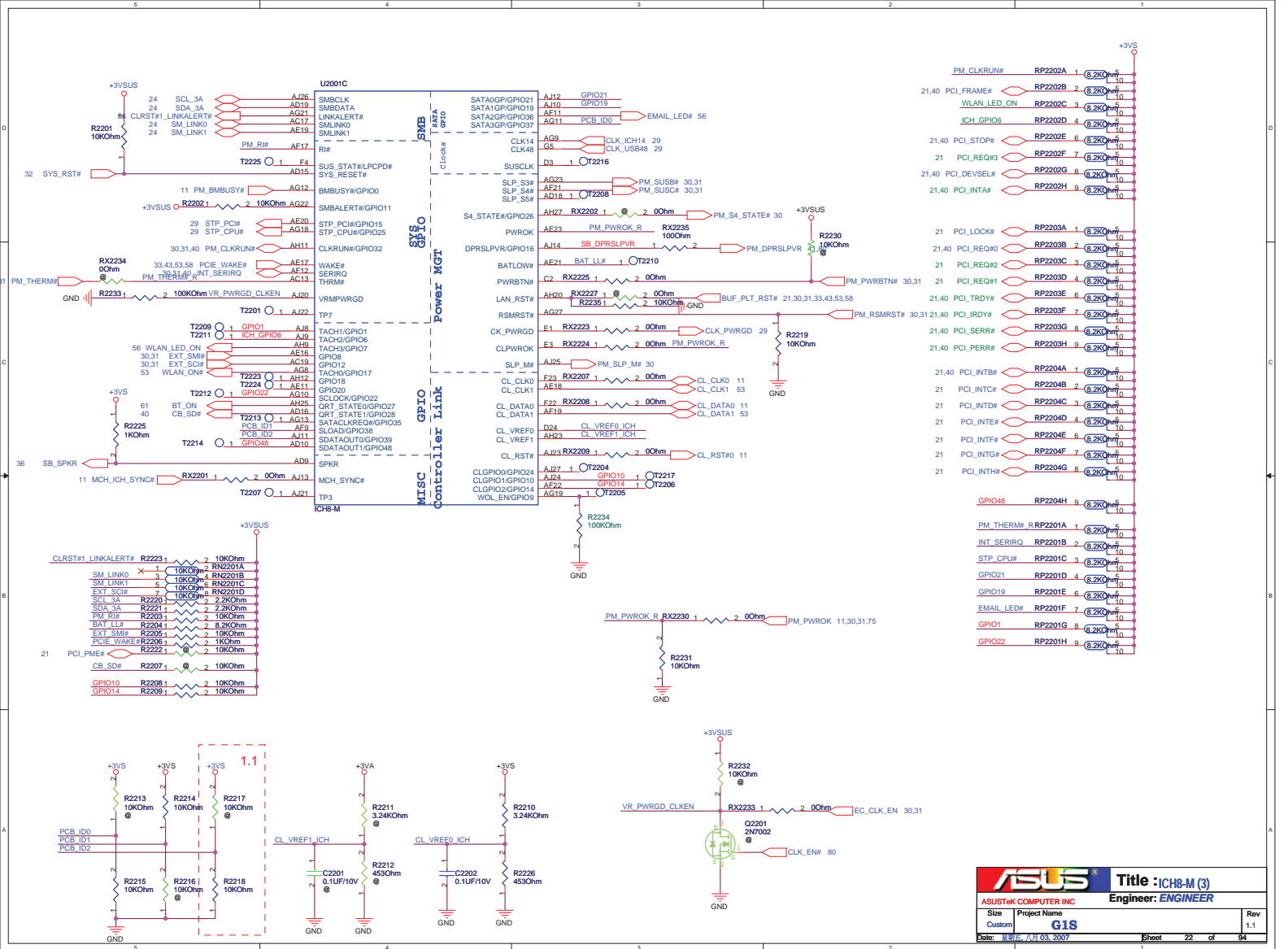
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Date: 星期五, 八月 03, 2007		Sheet	18 of 94

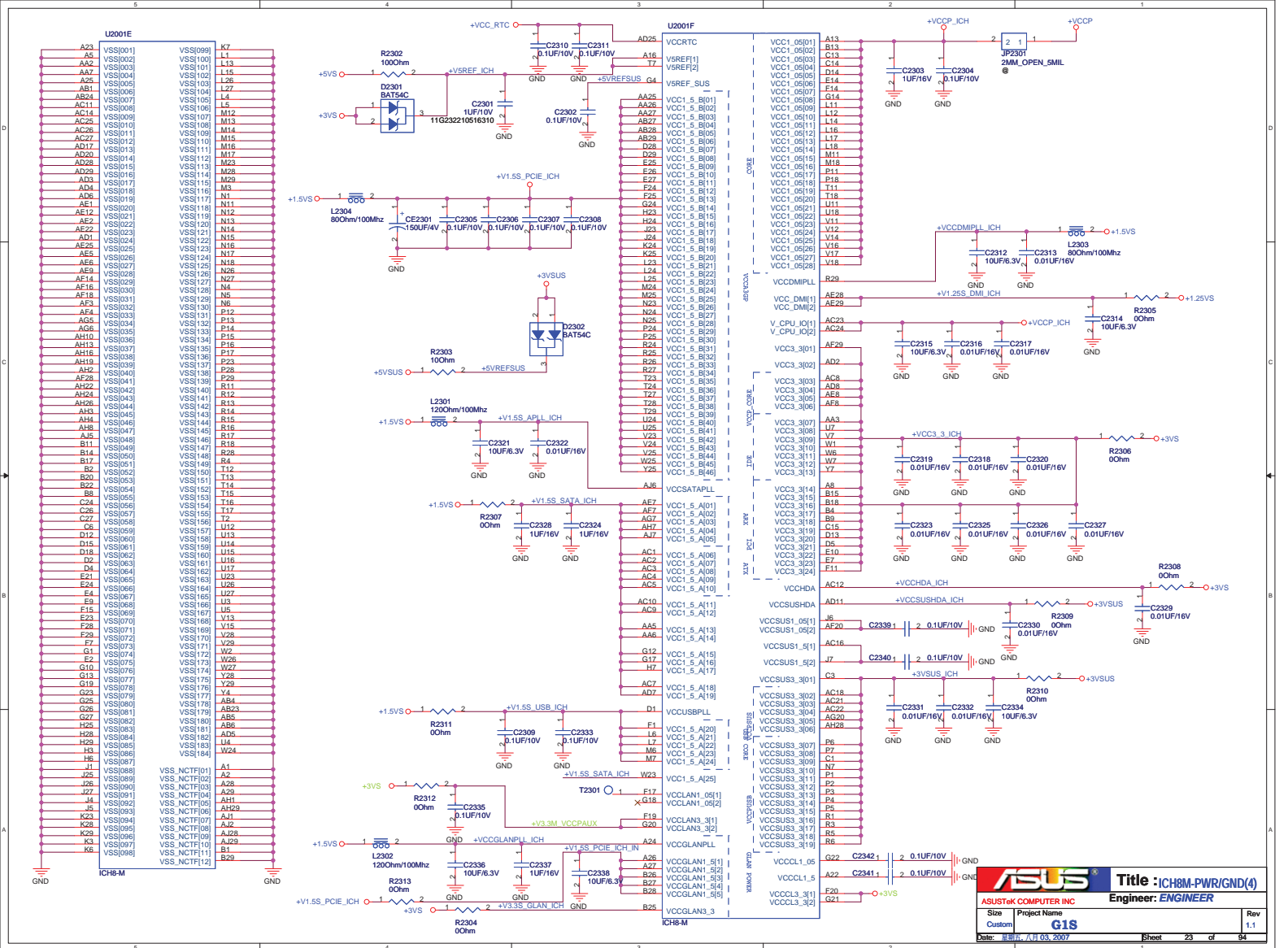


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ASUSTeK COMPUTER INC		Engineer: <i>ENGINEER</i>	
Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	19 of 94





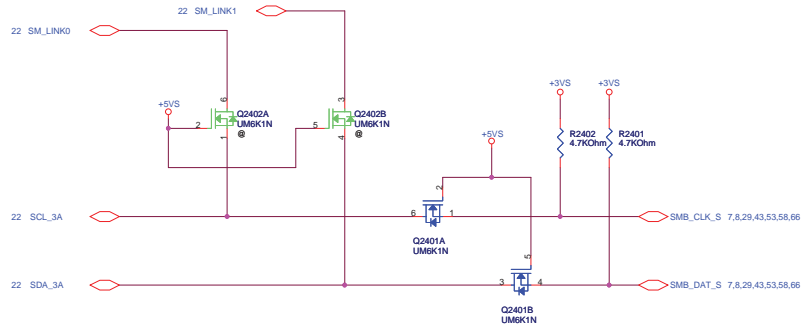


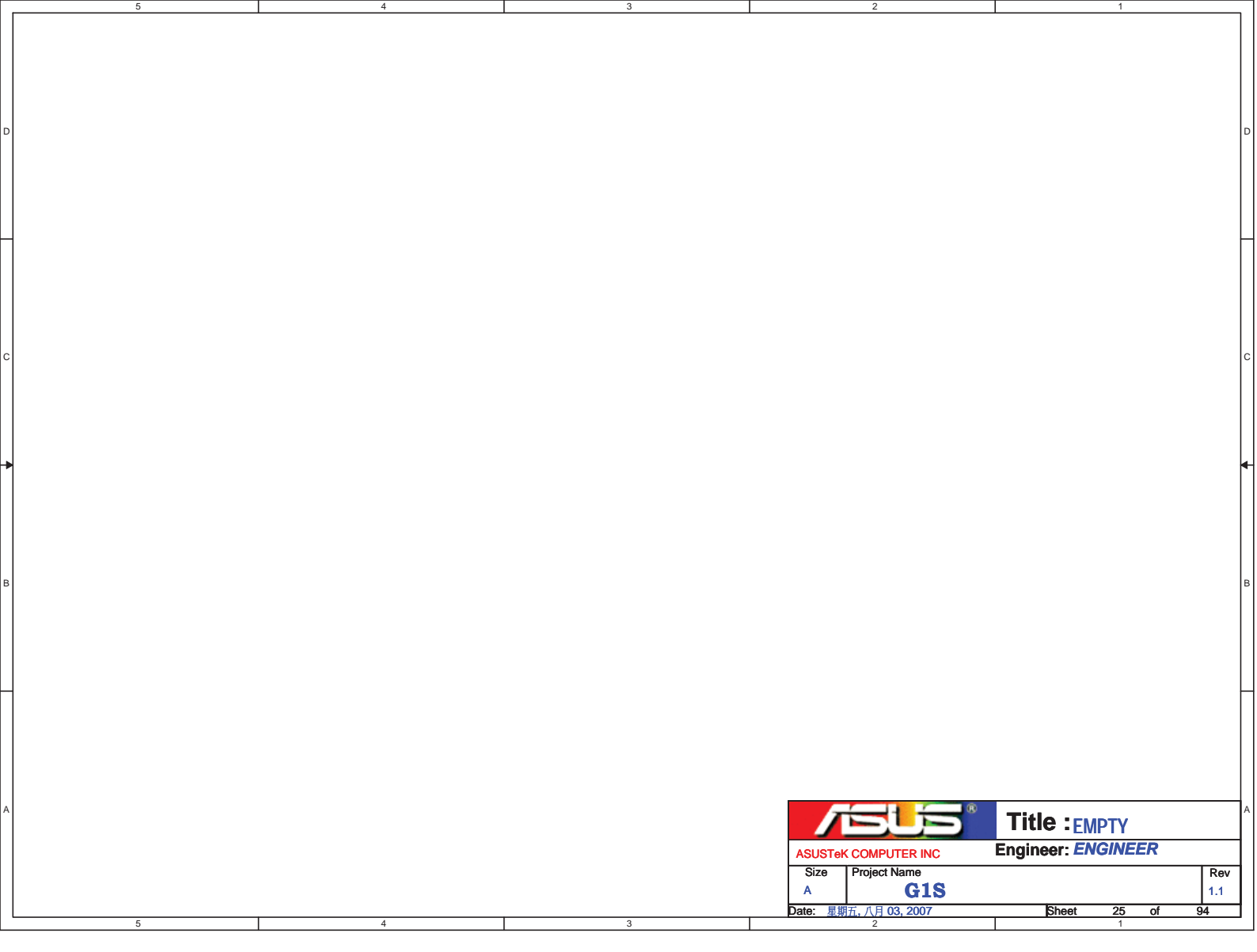



ICH8-M

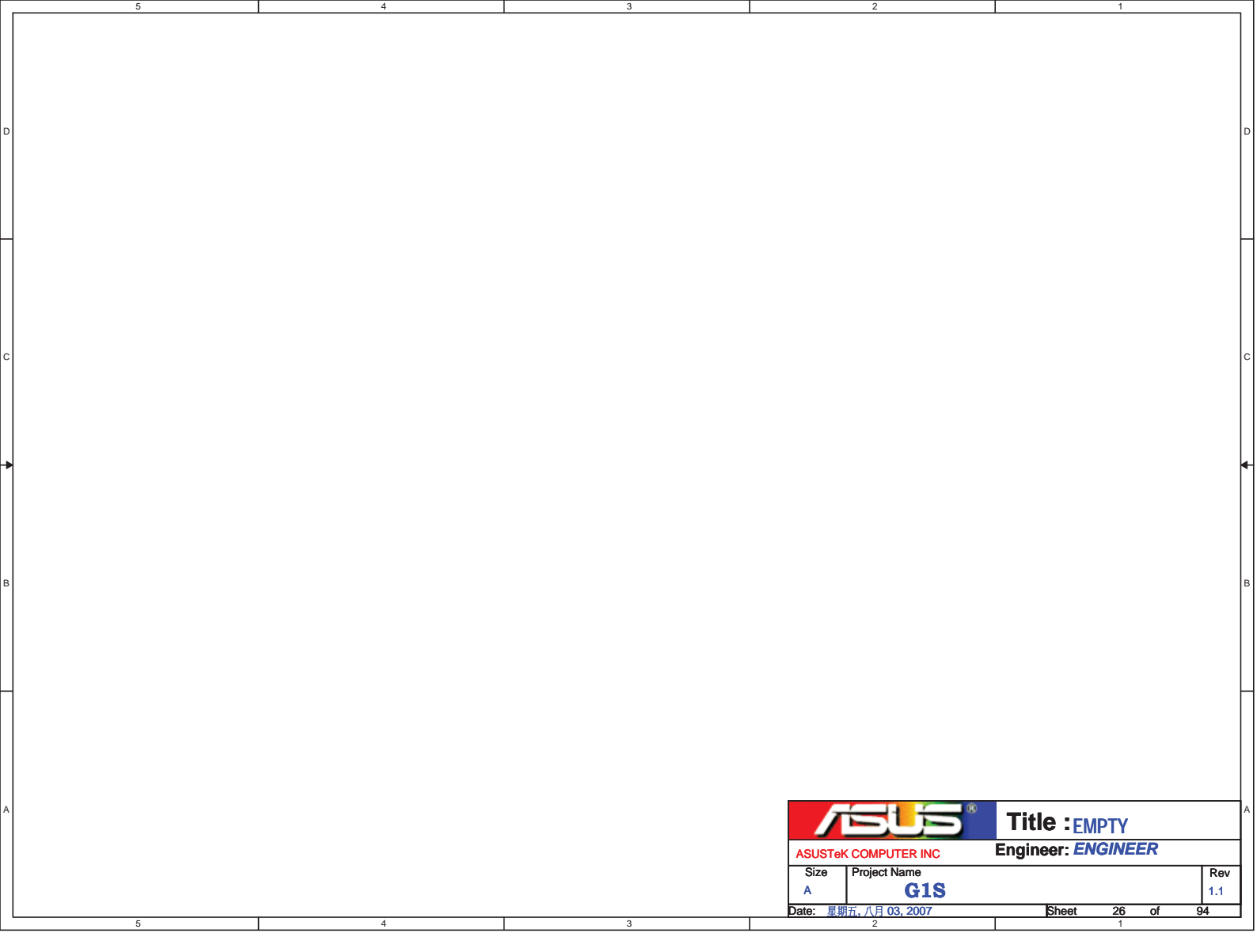
ICH8-M


Connect SMLINK and SMBUS
for SMBus 2.0 compliance.

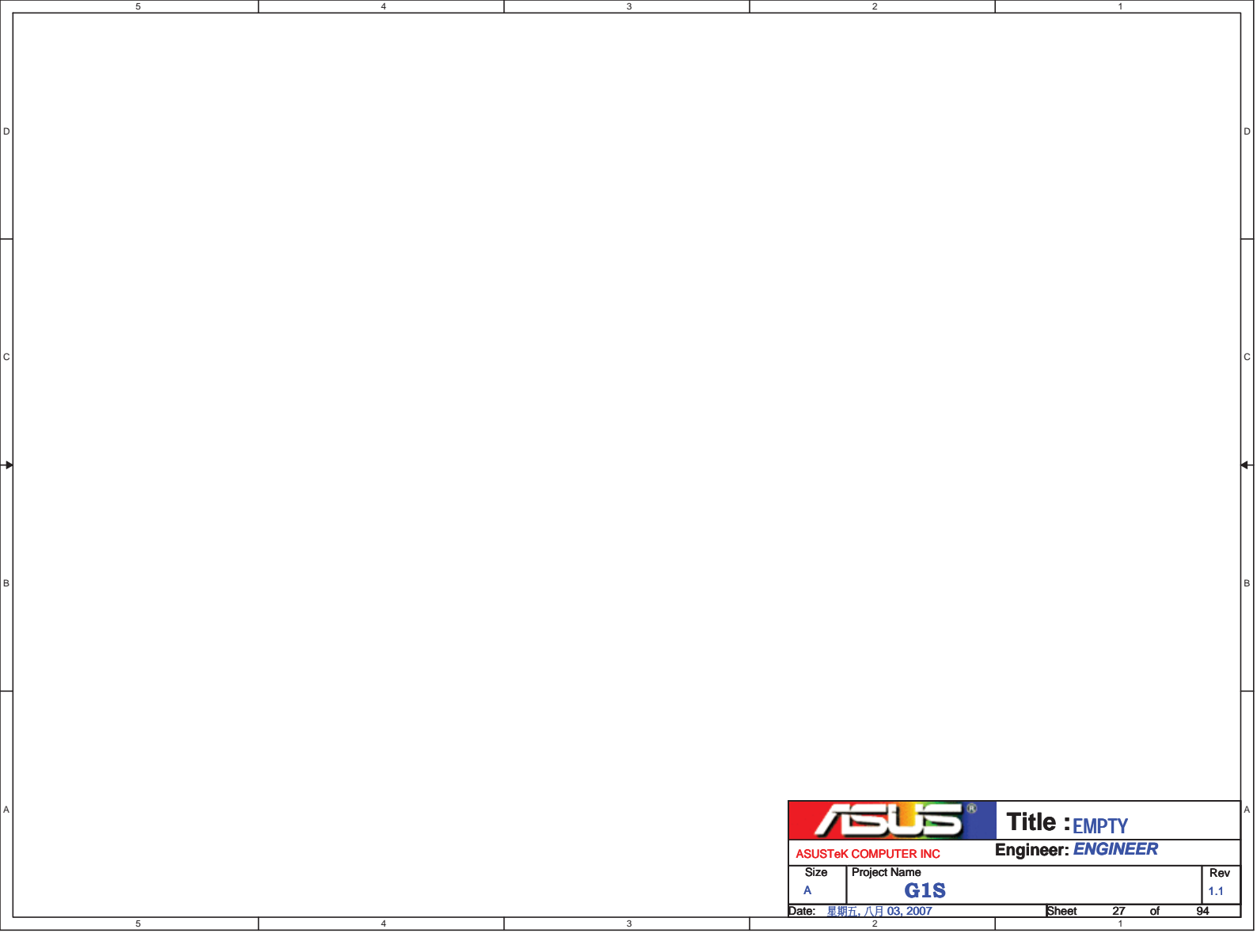





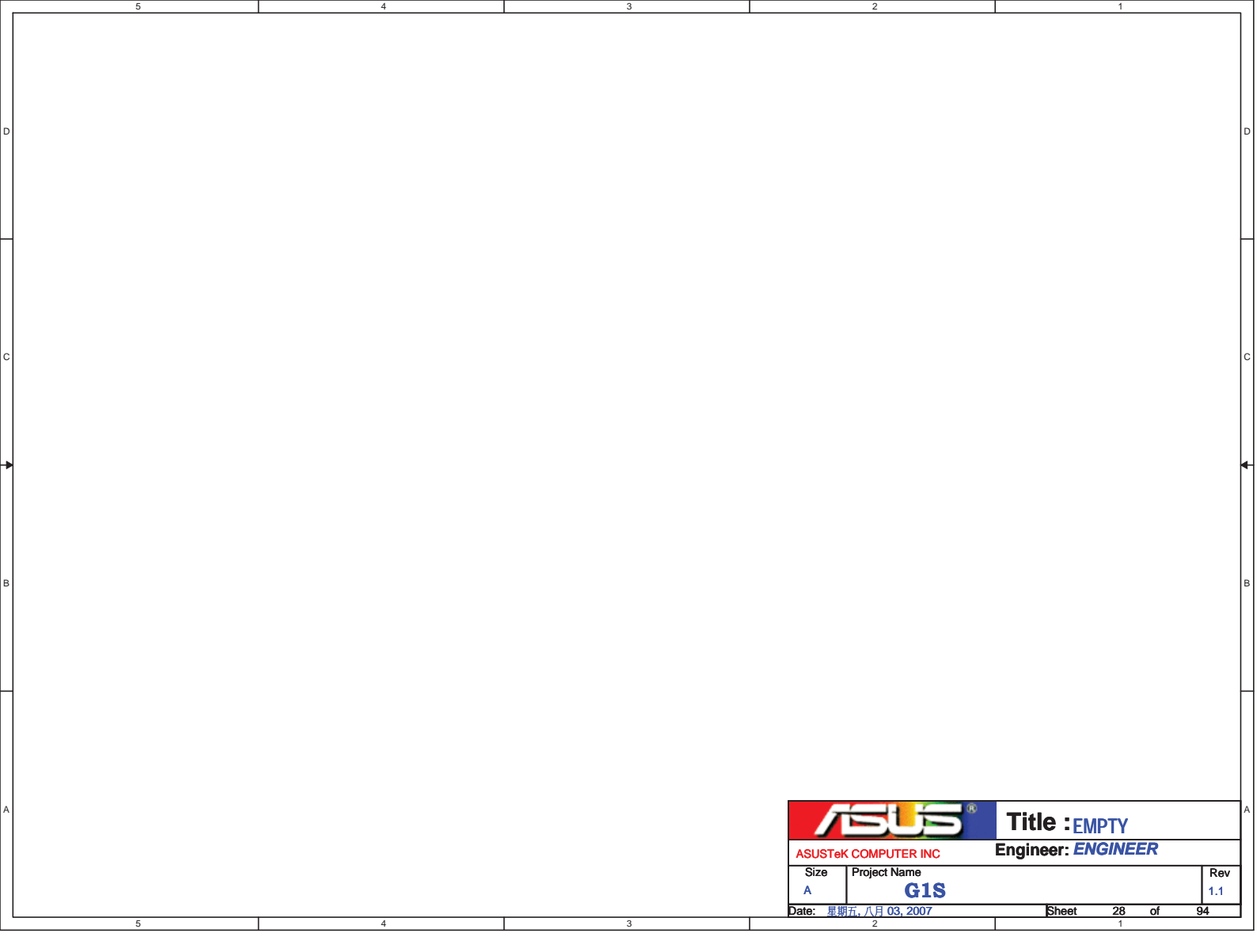
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ASUSTeK COMPUTER INC		Engineer: <i>ENGINEER</i>	
Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	25 of 94




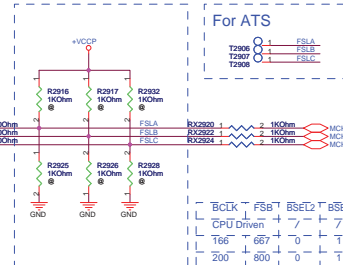
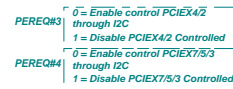
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Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	26 of 94



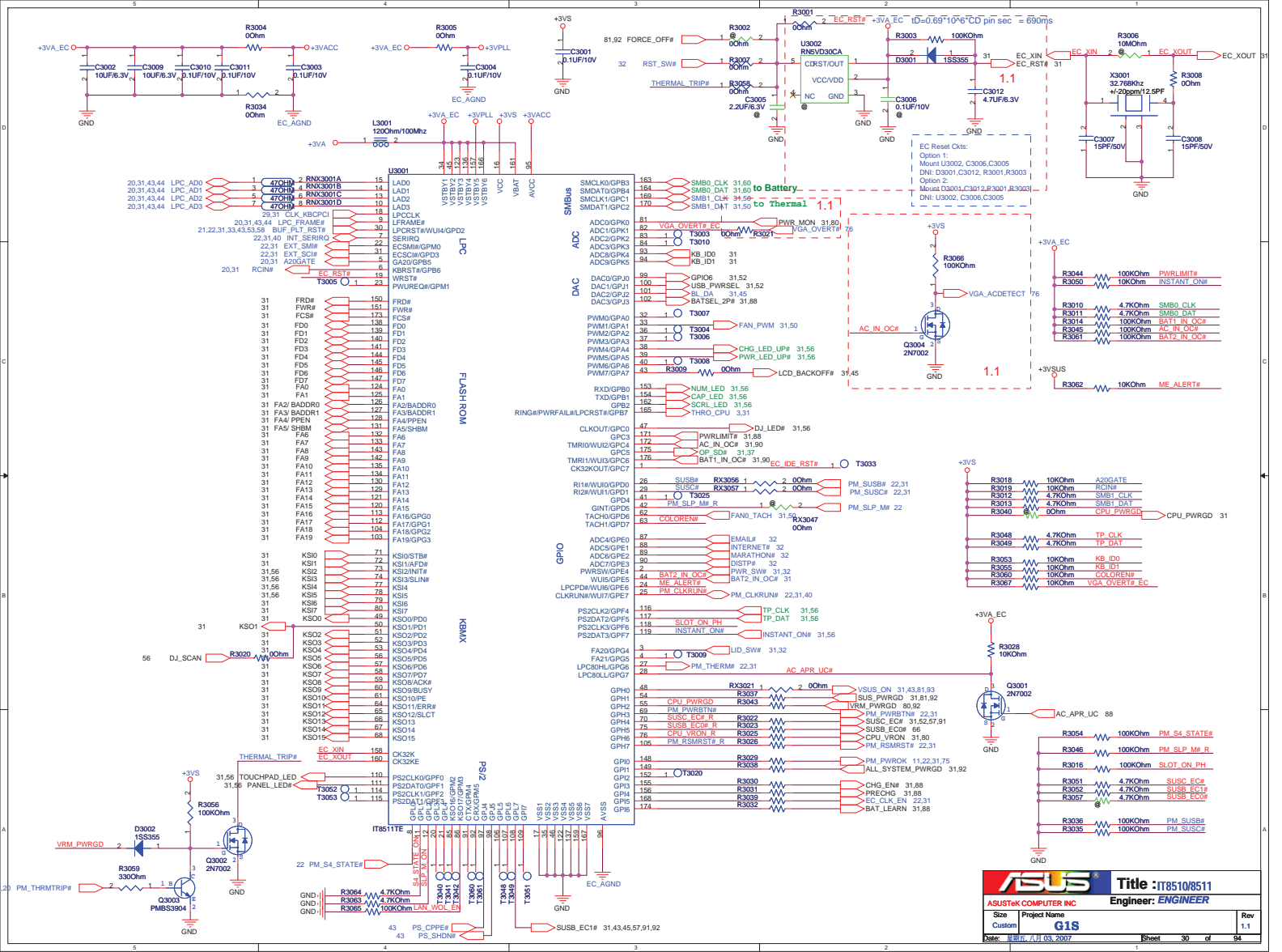
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ASUSTeK COMPUTER INC		Engineer: <i>ENGINEER</i>	
Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	27 of 94



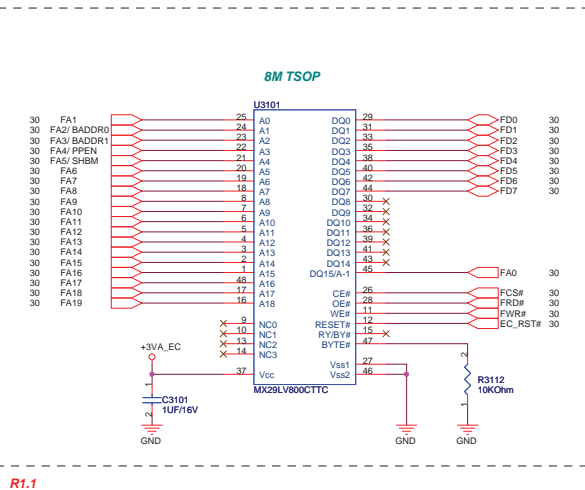
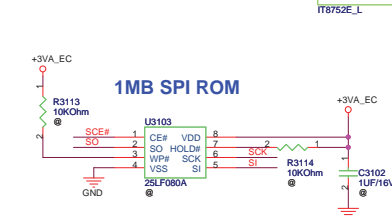
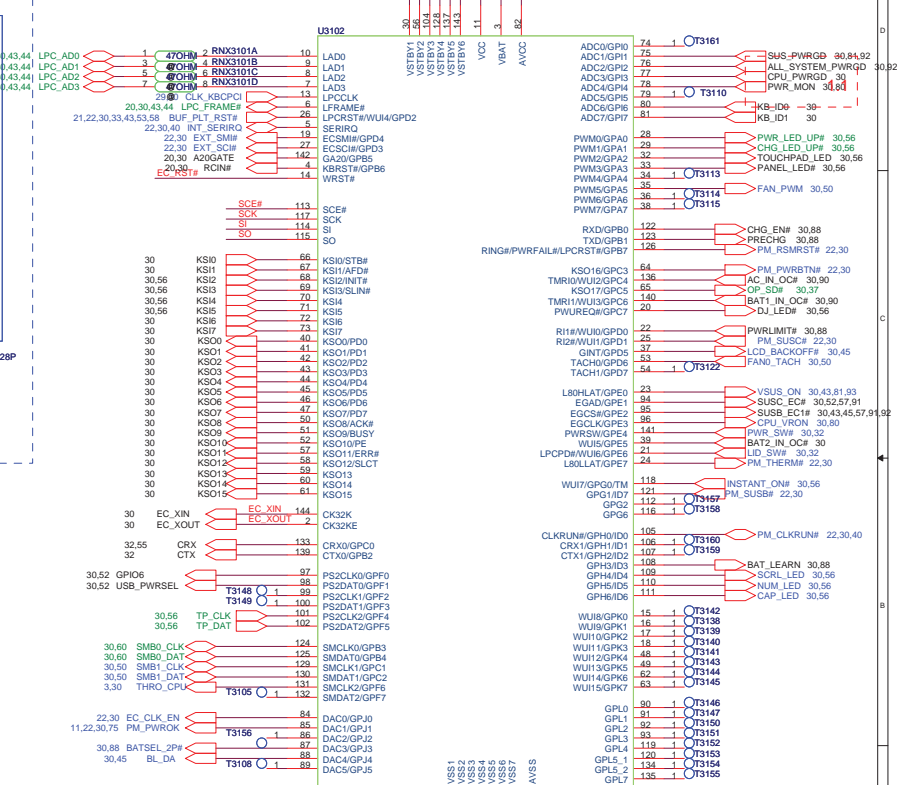
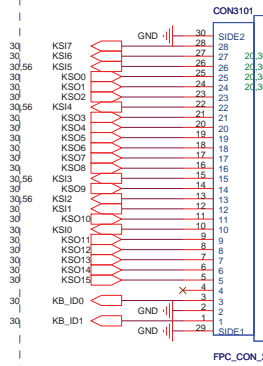
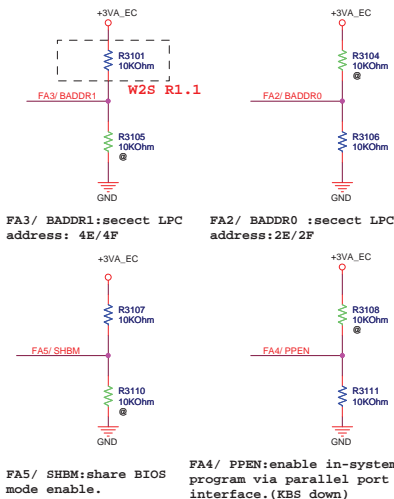
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Size A	Project Name G1S		Rev 1.1
Date: 星期五, 八月 03, 2007		Sheet	28 of 94

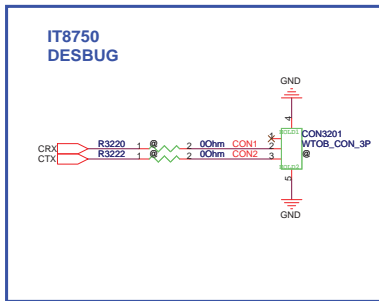
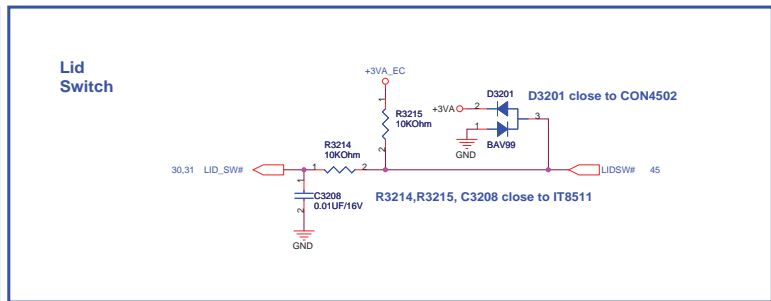
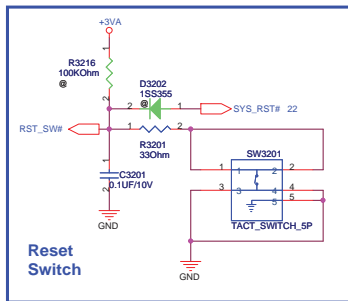
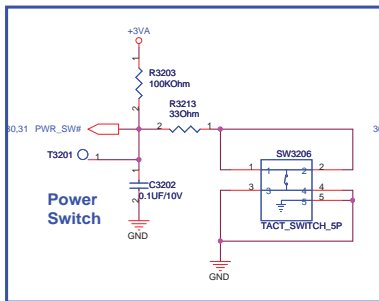
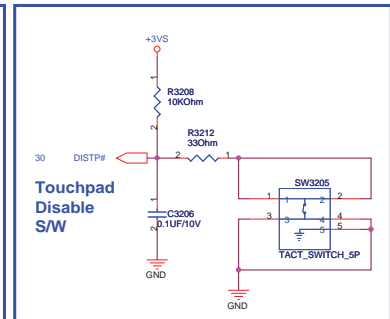
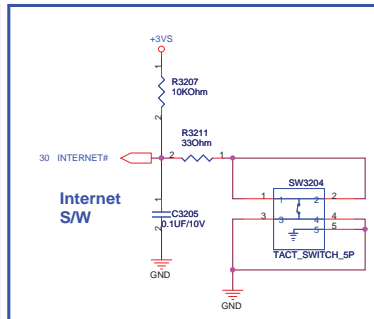
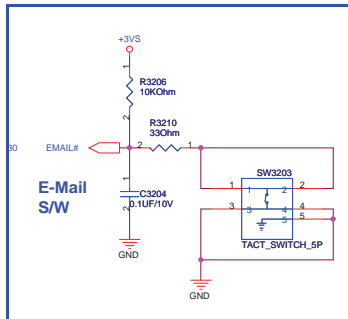
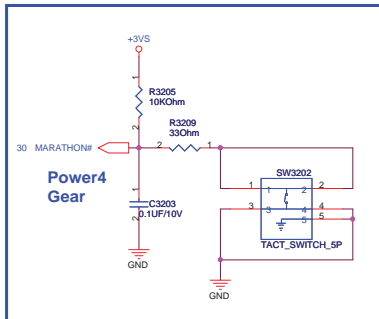


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ASUSTeK COMPUTER INC	Engineer: ENGINEER

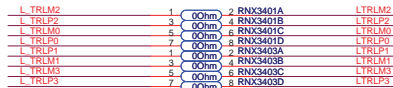
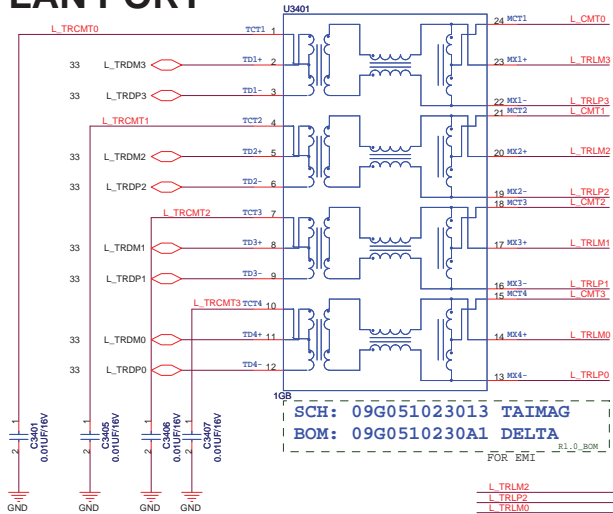


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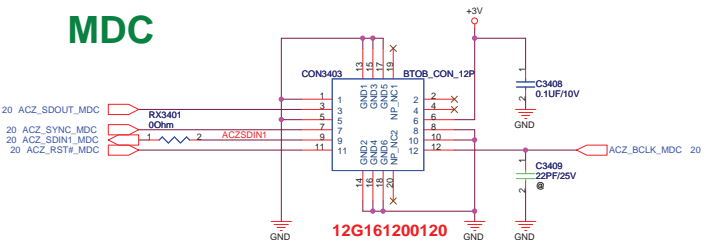




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