1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2010-07-22

SCHEM,MLB DVT,K99

07/22/10

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38	SMC	K16_MLB 07/07/2010
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8379	1	SCHEM,MLB,K99	SCH	CRITICAL	
820-2796	1	PCBF,MLB,K99	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,K99

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

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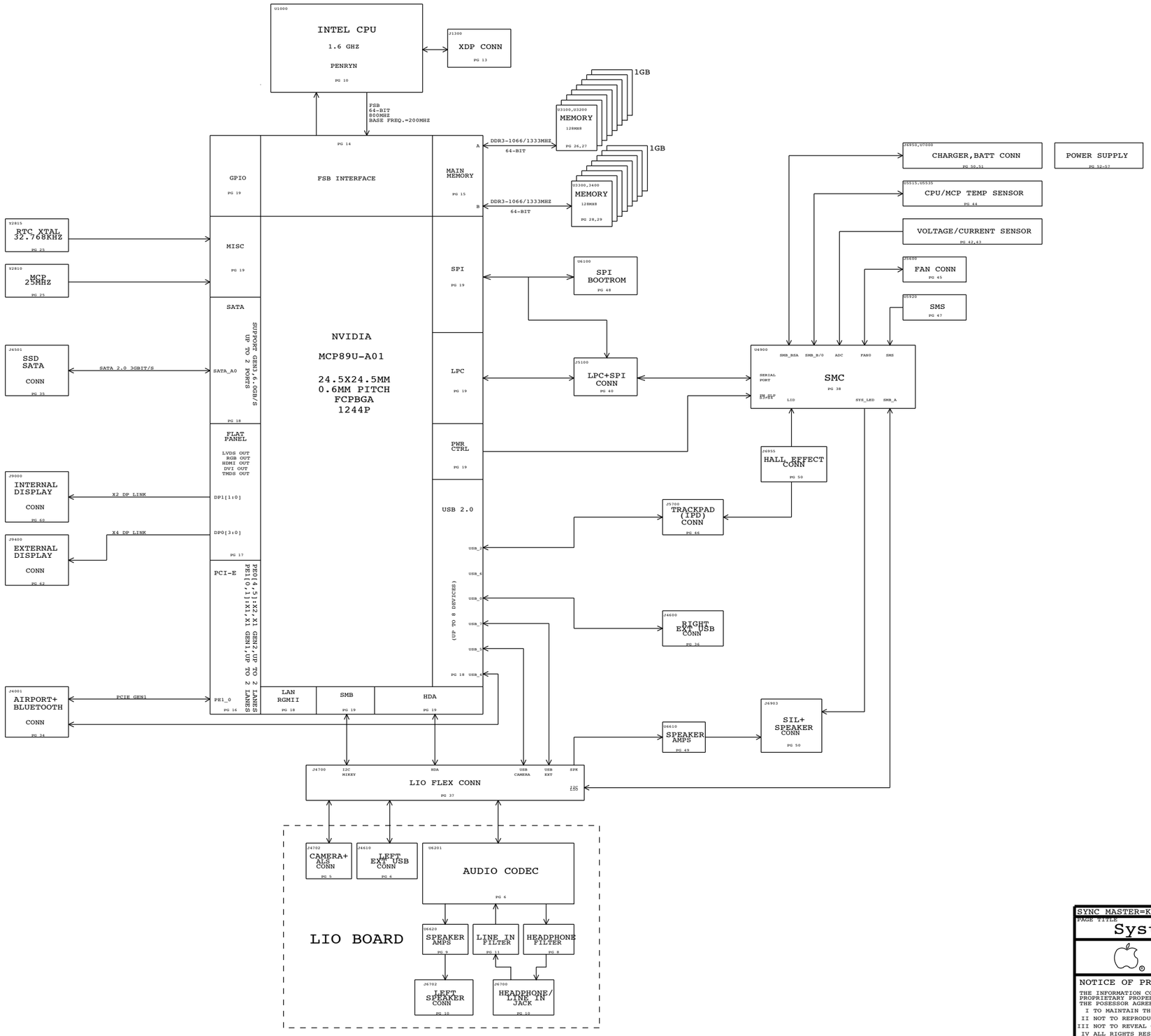

SYNC MASTER=K6 MLB SYNC DATE=12/11/2009

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System Block Diagram

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K99 POWER SYSTEM ARCHITECTURE

Need to update!!!

PP18V5_DCIN_CONN
Q7080
Q7085
PPDCIN_G3H_OR_PBUS
PBUS_VSENSE
ENABLE
3.425V G3HOT
LT3470
U6990
VOUT
PP3V42_G3H_REG
SMC PWRGD
RN5VD30A-F
U5010
V
Q5315
8A FUSE
F7040
PPVBAT_G3H_CHGR_REG
PPBUS_G3H
PBUS_G3H_VSENSE
AC
ADAPTER
IN
DCIN(16.5V)
F6905
6A FUSE
A
R7020
SMC_DCIN_ISENSE
CHGR_EN
(S5)
ENABLES
VIN
VOUT
PBUS SUPPLY/
BATTERY CHARGER
ISL6259
U7000
R7050
SMC_BATT_ISENSE
CPUVTTS0_EN
(S0)
EN_PSV
CPUVTT
(1.05V)
ISL95870
U7600
PGOOD
PP1V05_S0
(8A MAX CURRENT)
CPUVTTS0_PGOOD
J6950
3S2P
(9 TO 12.6V)
PPVBAT_G3H_CONN
Q7055
PPVBAT_G3H_CHGR_R
CHGR_BGATE
CPU VCORE
ISL6261A
IMVP_VR_ON_R
VR_ON
PGOOD
VR_PWRGOOD_DELAY
SMC_CPU_VSENSE
SMC_CPU_ISENSE
PPVCORE_S0_CPU
(44A MAX CURRENT)
MCP89
PM_SLP_S4_L
PM_SLP_S3_L
U1400
P3V3S3_EN
DDRREG_EN
P5VS3_EN_L
RC DELAY
SMC
U4900
SMC_PM_G2_EN
(S5)
P5VS3_EN_L
P3V3S5_EN_L
U7840
5V
(RT)
3.3V
TPS51980
U7201
PP5V_S3_REG
(13A MAX CURRENT)
PP3V3_S5_REG
(5.5A MAX CURRENT)
PGOOD1,2
VREG3
P5V3V3_PGOOD
MC34845
U9700
BKLT_EN
ENA
PPVOUT_SW_LCDBKLT
Q7910
P3V3S3_EN
PP3V3_S3_FET
Q4050
PP3V3_S3_WLAN
PM_WLAN_EN_L
Q7940
PP5V_S0_FET
P5VS0_EN
4.5V AUDIO
MAX8840
U6200
PP4V5_AUDIO_ANALOG
CPU
PWRGOOD
RESET*
U1000
MCP89
PWRBTN*
PLTRST*
RSMRST*
CPUPWRGD(GPIO49)
U1400
LPC_RESET_L
CPU_PWRGD
MCP_PS_PWRGD
U2850
PM_DPRSLPVR
Q7890
AP_PWR_EN
PM_WLAN_EN_L
Q7890,Q7891
PM_SLP_S3_L
SMC_ADAPTER_EN
Q2300
PP1V5R1V35_SW_MCP
MCPMEM_GATE
=DDRREG_EN
=DDTVTT_EN
1.5V
0.75V
TPS51116
U7300
PP1V5_S3_REG
(12A MAX CURRENT)
PP0V75_S0_REG
(1A MAX CURRENT)
MCP_CORE
ISL9563B
U7500
PPMCPCORE_S0_R
R7525
PPMCPCORE_S0_REG
(25A MAX CURRENT)
MCPCORES0_EN
ISL8009B
U7750
PP0V9_S5_REG
P3V3S0_EN
1.8V
TPS62202
U7760
PP1V8_S0_REG
1.5V
ISL8009B
U7710
PP1V5_S0_REG
1.05V
TPS74701
U7740
PP1V05_S0_MCP_PLL_REG
1.2V
ST1S12G12R
U7720
PP1V2_ENET_REG
ISL88042
U7870
PP3V3_S0
PP1V5_S0
PP1V05_S0
RST*
SMC
RSMRST_OUT(P15)
PWRGD(P12)
9ms DLY
IMVP_VR_ON(P16)
RSMRST_IN(P13)
PLT_RST*
PWR_BUTTON(P90)
P17(BTN_OUT)
U4900
PM_RSMRST_L
PM_PWRBTN_L
SMC_RESET_L
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
P1V5S0_PGOOD
P5V3V3_PGOOD
MCPCORES0_PGOOD
CPUVTTS0_PGOOD
MCPPLLDO_PGOOD
S0PGOOD_RST_L
SLP_S5_L
SLP_S4_L
SLP_S3_L
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
P1V8S0_EN
P1V5S0_EN
CPUVTTS0_EN
DDRVTT_EN
MCPCORES0_EN
P3V3S0_EN
PBUSVSENSE_EN
(S0)
P5VS0_EN
(S0)

SYNC_MASTER=K6_MLB	SYNC_DATE=12/11/2009
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0651	PCBA,MLB,HY 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DX7,DDR3:HYNIX_2GB,CAPS:SS
639-1055	PCBA,MLB,HY 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD15,DDR3:HYNIX_2GB,CAPS:MU
639-1048	PCBA,MLB,HY 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0X,DDR3:HYNIX_2GB,CAPS:TY
639-1043	PCBA,MLB,HY 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0Q,DDR3:HYNIX_4GB,CAPS:SS
639-1044	PCBA,MLB,HY 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0R,DDR3:HYNIX_4GB,CAPS:MU
639-1039	PCBA,MLB,HY 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0L,DDR3:HYNIX_4GB,CAPS:TY
639-1045	PCBA,MLB,SA 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0T,DDR3:SAMSUNG_2GB,CAPS:SS
639-1054	PCBA,MLB,SA 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD14,DDR3:SAMSUNG_2GB,CAPS:MU
639-1049	PCBA,MLB,SA 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0Y,DDR3:SAMSUNG_2GB,CAPS:TY
639-1052	PCBA,MLB,SA 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD12,DDR3:SAMSUNG_4GB,CAPS:SS
639-1046	PCBA,MLB,SA 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0V,DDR3:SAMSUNG_4GB,CAPS:MU
639-1040	PCBA,MLB,SA 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0M,DDR3:SAMSUNG_4GB,CAPS:TY
639-1042	PCBA,MLB,MI 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0P,DDR3:MICRON_2GB,CAPS:SS
639-1053	PCBA,MLB,MI 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD13,DDR3:MICRON_2GB,CAPS:MU
639-1047	PCBA,MLB,MI 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0W,DDR3:MICRON_2GB,CAPS:TY
639-1051	PCBA,MLB,MI 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD11,DDR3:MICRON_4GB,CAPS:SS
639-1041	PCBA,MLB,MI 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0N,DDR3:MICRON_4GB,CAPS:MU
639-1050	PCBA,MLB,MI 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD10,DDR3:MICRON_4GB,CAPS:TY
639-1446	PCBA,MLB,1.6GHZ,EL 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4Q,DDR3:ELPIDA_2GB,CAPS:SS
639-1438	PCBA,MLB,1.6GHZ,EL 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4G,DDR3:ELPIDA_2GB,CAPS:MU
639-1444	PCBA,MLB,1.6GHZ,EL 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4N,DDR3:ELPIDA_2GB,CAPS:TY
639-1449	PCBA,MLB,1.6GHZ,EL 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4V,DDR3:ELPIDA_4GB,CAPS:SS
639-1448	PCBA,MLB,1.6GHZ,EL 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4T,DDR3:ELPIDA_4GB,CAPS:MU
639-1445	PCBA,MLB,1.6GHZ,EL 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4P,DDR3:ELPIDA_4GB,CAPS:TY
607-6999	CMN PTS,PCBA,MLB,K99	K99_COMMON
085-1121	K99 MLB DEVELOPMENT BOM	K99_DEVEL:ENG
639-1355	PCBA,MLB,1.4GHZ,HY 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8L,DDR3:HYNIX_2GB,CAPS:SS
639-1341	PCBA,MLB,1.4GHZ,HY 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF83,DDR3:HYNIX_2GB,CAPS:MU
639-1353	PCBA,MLB,1.4GHZ,HY 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8J,DDR3:HYNIX_2GB,CAPS:TY
639-1350	PCBA,MLB,1.4GHZ,HY 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8F,DDR3:HYNIX_4GB,CAPS:SS
639-1356	PCBA,MLB,1.4GHZ,HY 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8M,DDR3:HYNIX_4GB,CAPS:MU
639-1348	PCBA,MLB,1.4GHZ,HY 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8C,DDR3:HYNIX_4GB,CAPS:TY
639-1349	PCBA,MLB,1.4GHZ,SA 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8D,DDR3:SAMSUNG_2GB,CAPS:SS
639-1351	PCBA,MLB,1.4GHZ,SA 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8G,DDR3:SAMSUNG_2GB,CAPS:MU
639-1357	PCBA,MLB,1.4GHZ,SA 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8N,DDR3:SAMSUNG_2GB,CAPS:TY
639-1344	PCBA,MLB,1.4GHZ,SA 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF86,DDR3:SAMSUNG_4GB,CAPS:SS
639-1352	PCBA,MLB,1.4GHZ,SA 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8H,DDR3:SAMSUNG_4GB,CAPS:MU
639-1354	PCBA,MLB,1.4GHZ,SA 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8K,DDR3:SAMSUNG_4GB,CAPS:TY
639-1342	PCBA,MLB,1.4GHZ,MI 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF84,DDR3:MICRON_2GB,CAPS:SS
639-1346	PCBA,MLB,1.4GHZ,MI 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF88,DDR3:MICRON_2GB,CAPS:MU
639-1343	PCBA,MLB,1.4GHZ,MI 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF85,DDR3:MICRON_2GB,CAPS:TY
639-1347	PCBA,MLB,1.4GHZ,MI 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF89,DDR3:MICRON_4GB,CAPS:SS
639-1345	PCBA,MLB,1.4GHZ,MI 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF87,DDR3:MICRON_4GB,CAPS:MU
639-1340	PCBA,MLB,1.4GHZ,MI 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF82,DDR3:MICRON_4GB,CAPS:TY
639-1442	PCBA,MLB,1.4GHZ,EL 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4L,DDR3:ELPIDA_2GB,CAPS:SS
639-1443	PCBA,MLB,1.4GHZ,EL 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4M,DDR3:ELPIDA_2GB,CAPS:MU
639-1447	PCBA,MLB,1.4GHZ,EL 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4R,DDR3:ELPIDA_2GB,CAPS:TY
639-1441	PCBA,MLB,1.4GHZ,EL 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4K,DDR3:ELPIDA_4GB,CAPS:SS
639-1439	PCBA,MLB,1.4GHZ,EL 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4H,DDR3:ELPIDA_4GB,CAPS:MU
639-1440	PCBA,MLB,1.4GHZ,EL 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4J,DDR3:ELPIDA_4GB,CAPS:TY

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7557	1	LABEL,MLB,K16/K99	[EEE_DX7]	CRITICAL	EEE:DX7
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0L]	CRITICAL	EEE:DD0L
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0M]	CRITICAL	EEE:DD0M
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0N]	CRITICAL	EEE:DD0N
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0P]	CRITICAL	EEE:DD0P
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0Q]	CRITICAL	EEE:DD0Q
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0R]	CRITICAL	EEE:DD0R
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0T]	CRITICAL	EEE:DD0T
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0V]	CRITICAL	EEE:DD0V
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0W]	CRITICAL	EEE:DD0W
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0X]	CRITICAL	EEE:DD0X
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0Y]	CRITICAL	EEE:DD0Y
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD10]	CRITICAL	EEE:DD10
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD11]	CRITICAL	EEE:DD11
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD12]	CRITICAL	EEE:DD12
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD13]	CRITICAL	EEE:DD13
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD14]	CRITICAL	EEE:DD14
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD15]	CRITICAL	EEE:DD15
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF82]	CRITICAL	EEE:DF82
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF83]	CRITICAL	EEE:DF83
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF84]	CRITICAL	EEE:DF84
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF85]	CRITICAL	EEE:DF85
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF86]	CRITICAL	EEE:DF86
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF87]	CRITICAL	EEE:DF87
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF88]	CRITICAL	EEE:DF88
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF89]	CRITICAL	EEE:DF89
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8C]	CRITICAL	EEE:DF8C
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8D]	CRITICAL	EEE:DF8D
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8F]	CRITICAL	EEE:DF8F
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8G]	CRITICAL	EEE:DF8G
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8H]	CRITICAL	EEE:DF8H
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8J]	CRITICAL	EEE:DF8J
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8K]	CRITICAL	EEE:DF8K
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8L]	CRITICAL	EEE:DF8L
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8M]	CRITICAL	EEE:DF8M
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8N]	CRITICAL	EEE:DF8N
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4G]	CRITICAL	EEE:DG4G
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4H]	CRITICAL	EEE:DG4H
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4J]	CRITICAL	EEE:DG4J
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4K]	CRITICAL	EEE:DG4K
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4M]	CRITICAL	EEE:DG4M
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4N]	CRITICAL	EEE:DG4N
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4P]	CRITICAL	EEE:DG4P
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4Q]	CRITICAL	EEE:DG4Q
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4R]	CRITICAL	EEE:DG4R
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4L]	CRITICAL	EEE:DG4L
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4T]	CRITICAL	EEE:DG4T
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4V]	CRITICAL	EEE:DG4V

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
2GB	0
4GB	1

DIE REV	CFG 3
A	0
B	1

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1121	1	K99 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-6999	1	CMN PTS,PCBA,MLB,K99	CMNPTS	CRITICAL	K99_CMNPTS

SYNC_MASTER=K6 MLB SYNC_DATE=12/11/2009

PAGE TITLE

K99 BOM Variants

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

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Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC:BLANK
341T0261	1	IC ASSY,SMC EXTERNAL,K99	U4900	CRITICAL	SMC:PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM:BLANK
341T0262	1	IC ASSY,EFI UNLOCKED,K99	U6100	CRITICAL	BOOTROM:UNLOCKED
341T0263	1	IC ASSY,EFI,LOCKED,K99	U6100	CRITICAL	BOOTROM:LOCKED

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0681	138S0638		ALL	TAIYO YUDEN AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
353S2987	353S2988	HVDDLDO:FIXED	ALL	TPS71725DCK AS ALTERNATE FOR U2590
104S0023	104S0018		ALL	CYNTEC/DALE AS ALTERNATES
107S0139	107S0075		ALL	CYNCYNC AS ALTERNATE
138S0671	138S0673		ALL	TAIYO AS ALTERNATE
155S0578	155S0367		ALL	TAIYO AS ALTERNATE
376S0926	376S0610		ALL	FAIRCHILD AS ALTERNATE
155S0457	155S0329		ALL	MAGLAYERS AS ALTERNATE
377S0107	377S0066		ALL	OHSEMI AS ALTERNATE

BOM Groups

BOM GROUP	BOM OPTIONS
K99_COMMON	COMMON,ALTERNATE,PROJ:K99,K99_MISC,MCP89U:A03,K99_DEBUG:ENG,K99_PROGPARTS,SPI:41MHZ,LVDDR3:YES,WLAN_PCTL:HW,IPD_5V:S5_INT,IPD_3V3:S5
K99_MISC	DP_ESD,DP_PWR:SMC,VFRQ:ELPS3,HVDDLDO:FIXED,MCPHVDD:P2V5,MCPPLL_R:REG,S0PGOOD_BJT,ISL6259_SCREENED:YES,DPI2C:SMC
K99_PROGPARTS	BOOTROM:UNLOCKED,SMC:PROG
K99_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,LPCPLUS,VREFMRGN:YES,EFI_DEBUG,S0PGOOD_ISL,MCPPLL_LDO,S3_S0_LED
K99_DEVEL:PVT	LPCPLUS
K99_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG:YES,XDP
K99_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
K99_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_2GB	DRAM_CFG0:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_2GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_4GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:MICRON_4GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB
CAPS:SS	SS_CAP_2_2UF,SS_CAP_10UF,SS_CAP_1UF,SS_CAP_22UF
CAPS:MU	MU_CAP_2_2UF,MU_CAP_10UF,MU_CAP_1UF,MU_CAP_22UF
CAPS:TY	TY_CAP_2_2UF,TY_CAP_10UF,TY_CAP_1UF,TY_CAP_22UF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3792	1	CDC,QWNN,QS,1,2,19W,890,80,1M,BGA	U1000	CRITICAL	CPU:1.2GHZ
337S3947	1	PDC,ELGFN,PBQ,1,4,10W,80,3M,BGA	U1000	CRITICAL	CPU:1.6GHZ
337S3954	1	PDC,ELGAK,PBQ,1,4,10W,80,3M,BGA	U1000	CRITICAL	CPU:1.4GHZ
337S3820	1	IC,MCP89U-A01,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A01
337S3868	1	IC,MCP89U-A02,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A02
337S3939	1	IC,MCP89U-A03,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A03
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,9X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,9X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,9X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,9X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_4GB
353S2392	1	IC,ISL6259,BATCHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6259_SCREENED:NO
353S2929	1	IC,ISL6259,BATCHARGER,39,4C4MM,QFN28	U7000	CRITICAL	ISL6259_SCREENED:YES
607-6811	1	ASSEMBLY,SUBASSY,PCBA HALL EFFECT, K99	J6955	CRITICAL	

SYNC MASTER=K24 MLB SYNC DATE=07/20/2009

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BOM Configuration

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

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Revision History NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

03/05/2010: RELEASE 0.41.0 (MAJOR)-
- PAGE 9: ADDED 20920 (OMIT) APN 998-3068 METAL TAB SYMBOL FOR MDP CONNECTOR
- PAGE 19: ADDED 10K R1954 APN 117S0007 PD ON MLB_RAM_CFG0 AS THERE IS NO INTERNAL PD ON GPIO_48
- PAGE 72: RENAMED NET P3V3_EN_L TO =P5VS3_EN AND =P3V3S5_EN_L TO =P3V3S5_EN
- PAGE 78: MOVED P3V3S5_EN NET FROM PIN 7 TO PIN 1 (NON-INVERTING) AND RENAMED IT TO P3V3S5_EN AS IT IS ACTIVE HIGH SIGNAL. LEFT PIN 4 NC
- PAGE 78: NO STUFF C7801
- PAGE 78: ALIASED =PDV9S5_EN TO CONNECT TO =PP3V3_S5_P0V0S5
- PAGE 78: ADDED 0402 C7801 AS 47PF NPO (NON-INVERTING) AND RENAMED IT TO P3V3S5_EN AS IT IS ACTIVE HIGH SIGNAL. LEFT PIN 4 NC
- PAGE 78: NO STUFF C7801
- PAGE 78: ALIASED =PDV9S5_EN TO CONNECT TO =PP3V3_S5_P0V0S5
- PAGE 78: ADDED 0402 C7801 AS 47PF NPO (NON-INVERTING) AND RENAMED IT TO P3V3S5_EN AS IT IS ACTIVE HIGH SIGNAL. LEFT PIN 4 NC
- PAGE 78: REPLACED R7813 WITH 0 OHMS APN 117S0002 FOR NOW

03/05/2010: RELEASE 0.42.0 (MAJOR)-
- PAGE 11: ADDED DRAM_CFG0:L TO RAM TABLES NOT CALLING OUT DRAM_CFG0:H, AND REMOVED DRAM_CFG1:H AS IT IS NO LONGER NEEDED
- PAGE 4: DELETED MODULE TABLE ENTRY FOR Z59007 AS POR SYMBOL IS READY
- PAGE 4: ADDED MODULE-1176 ENTRY FOR BOM OPTION MLB_SPITFIRE:1266-1176
- PAGE 9: REPLACED Z59007 WITH POR APN 870-1938 AND DELETED OMIT ATTRIBUTE
- PAGE 9: REPLACED P0603 P1E Z80906 WITH APN 870-1938 PER PD
- PAGE 19: REMOVED R1955 PULL-UP ON MLB_RAM_CFG1 (INTERNAL PULL-UP)
- PAGE 19: CHANGED R1958 PULL-DOWN TO 470 OHMS (STRONGER PD VS 8.5K PU) APN 117S0102
- PAGE 19: REPLACED R1957 WITH 10K APN 117S0007 TO BE CONSISTENT
- PAGE 78: ADDED BYPASS PROPERTIES TO C7895 AND C7896
- PAGE 78: CHANGED BASE NET FOR PM_SLP_S4_DLY_L PER WILL

03/05/2010: RELEASE 0.43.0 (MAJOR)-
- PAGE 2: REPLACED THIS PAGE WITH QUANTA'S UPDATED ONE
- PAGE 4: ALL SWITCHED_NOM TABLE USE SCREENED ISL6259 PART
- PAGE 4: ADDED APN 376S0895 UNDER MODULE PART TABLE FOR Q7220 & Q7225 PER DAYU FOR PART SUPPLY ISSUE
- PAGE 4: MOVED SMS_YES BOM OPTION FROM K99 MISC TO DEVEL_BOM
- PAGE 4: UPDATED MICRON 2GB APN 353S0712 IN THE BOM TABLE
- PAGE 9: FIXED MCPCORE1SNS SIGNALS ALIASES PER WILL'S CHANGES ON K16
- PAGE 19: REMOVED R1957 CRITICAL ATTRIBUTE FROM THE BOM TABLE AS IT IS NOT NEEDED
- PAGE 70: NO STUFF Q7080, D7005,Q7055 AND F7040 FOR NON-FUNCTIONAL BOARD
- PAGE 72: ADDED OMIT_BOM OPTION TO Q7220 & Q7225 AS SYMBOL IS NOT READY
- PAGE 72: CHANGED R7215 AND R7216 TO 4.02K 1% APN 115S0134 PER VENDOR
- PAGE 73: CHANGED R7216 AND R7256 TO 4.02K 1% APN 115S0354 PER VENDOR
- PAGE 73: CHANGED C7239 TO 47PF 5% 50V NPO APN 132S0122 PER VENDOR
- PAGE 76: CHANGED OCP TEXT NOTE PAR VENDOR
- PAGE 78: CHANGED R7641 AND R7642 TO 100K 1% APN 115S0144 PER VENDOR
- PAGE 78: ADDED NC SYMBOL TO PIN 5 OF U7896

03/07/2010: PROTO1 NON-FUNCTIONAL AGILE RELEASE 1.0.0 (FAB)-
- NON-FUNCTIONAL PROTO 1 OK2FAB RELEASE!!!

3/19/2010: RELEASE 1.1.0 (MAJOR)-

- PAGE 4: REMOVED SMS_YES BOM OPTION FROM K99_DEVEL:ENG_BOM GROUP, INSTEAD, ADDED SMS:NO TO K99-MISC TABLE (ALSO SEE BELOW CHANGES FOR P0S 50,51)
- PAGE 50: ADDED BOM OPTION ATTRIBUTE SMS:NO TO R5093 PU ON SMS_INT_L. IDEA IS TO PULL THIS NET TO 5V ONLY WHEN SMS IS NOT STUFFED, ELSE FLOAT TO SAVE LARGE 2.4K PU PER RADAR 7654926
- PAGE 71: CONNECTED SMC 0 SMBUS INTERFACE TO THE TCON-A CHIP IN THE INTERNAL DISPLAY. PROVIDED A CLUMSY SYNTAX FOR SMBUS NETS TO BE DRIVEN FROM MCP89 0 SMBUS [R5240-R5243 APN 117S0002] PER RADAR 7749046
- PAGE 59: REPLACED BOM OPTION SMS_YES WITH SMS:YES
- PAGE 78: ADDED SMS:NO R5934 PU ON SMS_INT_L TO PP3V3_S3_SMS WITH BOM OPTION ATTRIBUTE SMS:YES PER RADAR 7765442
- PAGE 70: NO STUFF Q7080, D7005,Q7055 AND F7040
- PAGE 75: REPLACED L7560 WITH 10X10X3MM APN 152S1236 PER RADAR 7769386
- PAGE 12: RENAMED NEWLY ADDED TCON_SDA/SCL TO PINS 1 AND 2 OF J9000 RESPECTIVELY PER RADAR 7749046
- PAGE 93: ADDED 3300PF APN 132S0241 C9302 CAP ON DP_CA_DET TO GND PER RADAR 7742010
- PAGE 108: ADDED SMBUS_SMC_0_S0_SCL/SDA_R CONSTRAINTS SET

03/24/2010: Release 1.2.0 (MAJOR)-
- Text size has been fixed - safe to sync
- Page 8: Renamed PP3V3_S5_LCD to PP3V3_S0_LCD
- Page 8: Moved PP3V3_S0_LCD / PP3V3_S5_DP_POST_PWR to S5 rail
- Page 71: Added =I2 TCON_SCL/SDA FETs under INT_DP_FUNC_TEST group
- Page 12: After syncing from K16, delete C1273 as it MA to K99
- Page 90: After syncing, renamed PP3V3_S5_LCD to PP3V3_S0_LCD

Sync'ed ALL but pages 1-9,28,47,69,70,74,75 and 97 from K16
Please NOTE that some of the below changes were already part of 1.1 release. Below list depicts all the changes since 3/1 K16 release.

- Page 12: Fixed invisible pins on CPU bypass caps. Also changed all OMITs to OMIT_TABLES and performed other cleanup
- Page 13: Swapped BCLK_IN N/P after library symbol refresh
- Page 17: Added CKPLUS_WATVE properties to VDD_IFPx pins that are legally grounded on K16
- Page 19: Removed PM_SLP_S5_L alias. Other cleanup to make all CRefs V1S1b1e
- Page 19: Removed pull-up on MLB_RAM_CFG1 (internal pull-up), changed pull-down to 470 ohms. Added pull-down of MLB_RAM_CFG0. Made both pull-up and pull-down 10K
- Page 25: Added voltage divider for HVDD_LDO. OMIT_TABLE'd U2590, added tables to fixed 2.5V (and adjustable) LDO regulators
- Page 39: Removed CRITICAL flag from 0-ohm resistor table
- Page 43: PB 3 changed from SMC_PARK to SMC_PME_L. P74 changed from PM_SLP_S4_L to SMC_DP_HPD_L. P75 changed from PM_SLP_S5_L to PM_SLP_S4_L
- Page 49: C4902 changed from 0805 to 0603 to free up some layout space for MCP power resources
- Page 50: Added SMS:NO BOMOPTION to SMS_INT_L pull-up. Other cleanup including adding unused alias to SMC_PB3
- Page 70: Added P3V3_S5 registers to control DP_PWR and gnd to connect DP_EXT_HPD to SMC. Updated netname on R5090 and added BOMOPTION of DP_PWR:so
- Page 53: Added TCON_I2C block and R's to connect to SMC_0 and MCP 0
- Page 53: Removed PP prefix from non-power nets. Added OMIT_TABLE to buses. Other cosmetic cleanup including grid compliance
- Page 59: Synced with K99 (adds R5924, S3 pull-up on SMS_INT_L), plus lots of cleanup including removing PP prefix from signal nets, correcting BYPASS & PLACE_NEAR properties, correcting offpages, etc
- Page 72: Changed Q7220 & Q7221 to 376S0895 as alternate part. Fixed netnames on switcher enables, removing _L suffixes since they are active-high
- Page 72: Value changes to C7237/C7239/R7216/R7246/R7247/R7256 per Dayu.
- Changed C7288 to marking 0 C7218. Removed alias to marking 0 as purpose and was incorrect since it lacked a MAKE_BASE anyhow
- Page 74: Value changes to R7417/R7642 and OCP resistors per Dayu
- Page 78: Removed RAM power-down circuit, reconnecting =DDRREG_EN to original net
- Page 78: Disconnected half of Q7891 from 5V S3 power sequencing, gate left floating. Removed inverter U7895 and renamed P5VS3_EN net reconnected P3V3S5_EN to be non-inverted. R7813 changed from pull-up to series R (0-ohms) to PDV9S5_EN changed to alias to 3.4V S5 rail. Cleaned up page including fixing grid issues. Added PPVBAT_G3H properties to C7895 and C7896. Changed netnames for PM_SLP_S4_DLY
- Page 93: Added RC between DP_CA_DET and DDC bypass FETs. Also cleaned up page, adding offpages, fixed grid issues, made power nets convention-compliant and added note about DP_CA_DET pull-up / FET Vgs requirements
- Page 93: Added RC between DP_CA_DET and DDC bypass FETs. Also cleaned up page, adding offpages, fixed grid issues, made power nets convention-compliant and added note about DP_CA_DET pull-up / FET Vgs requirements
- Page 93: Added CKPLUS_WAIVE properties to _P nets connecting to FET DRAIN pins
- Page 94: Renamed DP_PWR nets to indicate 'SW' state instead of 'SO'. Switch input changed from PM_SLP_S3_L to =DP_PWR_EN. HPD_L netname changed, offpage added and pull-up changed to DP_PWR. Other cleanup including removing PLACE_NEARs that should be handled via Constraints, OMIT_TABLES for caps, CRITICAL flags on common-mode chokes and cosmetic changes
- Page 108: Added net constraints for diffpairs reported by diffpNoPhysNet report (except 4 false errors). Other cleanup including removing some unnecessary net properties

03/25/2010: Release 1.3.0 (MAJOR)-
- Page 4: Fixed DRAM_CFG table - swapped CFG 1 and 0 columns
- Page 4: Updated EEE numbers
- Page 4: Pulled new 607-XXXX APN and added K99_CMNPTS BOM option corresponding to this new sub-BOM consisting of common parts between 18 BOMs
- Page 41: Replaced K99 COMMON with K99_CMNPTS in the BOM variant table
- Page 44: Replaced K99-SS/MU/TY_CAP BOM option with better nomenclature - CAPs:SS/MU/TY
- Page 4: Removed K99_ prefix from K99_DDR3_ BOM Group
- Page 4: Deleted 376S0895 APN module parts table entry as it is already duplicated on page 72
- Page 4: Deleted module table entry for 806-1176 as actual symbol has been added
- Page 9: Replaced Z0920 with POR stiffener symbol for APN 806-1176 and deleted OMIT
- Page 46: Replaced Q4690 with single port switch APN 353S1930 (Higher DCR) to fix USB current limit
- Page 46: Changed BOM attribute OMIT to OMIT_TABLE for C4690 & C4695
- Page 53: Changed R2411 to 2.43K 1% APN 115S0287
- Page 54: Changed R5471 to 4.53K 0402 APN 115S0287
- Page 72: Changed R7249, R7247 to 1.87K 1% APN 115S0159 per Dayu
- Page 72: Changed R7216, R7256 to 3.16K 1% APN 115S0161 per Dayu
- Page 72: Changed C7237, C7239 to 4.7UF 10% APN 132S0087 per Dayu
- Page 72: Changed C7257, C7259 to 100PF 10% APN 131S0287 per Dayu
- Page 97: Replaced V9701 with new improved 600 version APN 353S2967
- Page 97: Changed R9704 to 33 ohms APN 117S0080 per Kiran
- Page 97: Stuffed C9704 per Kiran

3/26/2010: Release 1.4.0 (MAJOR)-
- Page 4: Added 376S0895 as an alternate for 376S0749 per Dayu
- Page 4: Added 138S0681 as an alternate for 138S0638 per GSM
- Page 4: Added 138S0676 as an alternate for 138S0635 per GSM
- Page 4: Removed alternates that were NA to K99
- Page 72: Deleted OMIT_TABLE attribute from Q7220 & Q7225. Also deleted the BOM table. Plan is to use 376S0895 as alternate instead

03/30/2010: Release 1.5.0 (MAJOR)-

- Page 4: Deleted 376S0895 alternate part entry to avoid mixing of vendors between high & low side FETs per Dayu
- Page 4: Deleted DPI2C:SMC BOM OPTION as eDP I2C Bus won't be routed on =I2C_TCON
- Page 4: Changed BOM OPTION SPI:25MHz to 62MHz
- Page 9: Changed BOM OPTION attribute of Z59904 to OMIT_TABLE
- Page 10-11: Changed BOM OPTION attribute of U1000 to OMIT_TABLE
- Page 19, 20: Changed BOM OPTION attribute of U1400 to OMIT_TABLE
- Page 23: Changed BOM OPTION attribute of C2600 to OMIT_TABLE
- Page 31-34: Changed BOM OPTION attribute of U3400-U3430 to OMIT_TABLE
- Page 35-36: Changed BOM OPTION attribute of all caps to OMIT_TABLE
- Page 51: Changed name of BOM OPTION from SMS_YES to SMS
- Page 52: Changed R5290 & R5291 to 2K APN 1188S0174 per RADAR# 7810865
- Page 53: Changed BOM OPTION attribute of U6100 to OMIT_TABLE
- Page 69: Changed R6905 to 10 Ohms APN 101S0089 & C6990 to 2.2uF APN 138S0672 to improve noise immunity & reduce inrush stress, per Dayu
- Page 69: Changed BOM OPTION attribute of U6955 to OMIT_TABLE
- Page 69: Changed BOM OPTION attribute of C6999 to OMIT_TABLE
- Page 69: Changed BOM OPTION attribute of Q7000 to OMIT_TABLE
- Page 72: Replaced Q7220 & Q7225 with APN 376S0895 (RJK03E0) per Dayu
- Page 72: Changed R7220 to 41.2K APN 1188S0360 to boost 5V, per Dayu
- Page 73: Replaced Q7330 with APN 376S0749 (SiSS26) per Dayu
- Page 73: Changed Q7335 to APN 376S0895 (RJK03E0) OMIT_TABLE per Dayu
- Page 77: Changed R7751 to 2.55K APN 1188S0234 & R7752 to 20K APN 1188S0175 to improve noise immunity & reduce inrush stress, per Dayu

03/31/2010 - Proto 1 Agile Release 2.0.0 (FAB)
- Proto 1 ok2FAB Agile Release!!!

3/31/2010: Proto 1+ Release 2.1.0 (MAJOR)

- Page 4: Activated PROJ:K99_BOMOPTION to select proper APN for U9701
- Page 97: Changed BOM OPTION attribute of C9797 to OMIT_TABLE after syncing with K16

Sync'ed from K16

-Page 90: Added Q9090 isolation FET to support LCD panel power-down per radar 7761747
-Page 97: Removed previous change, U9701 back to 353S2896, handled via a table now to support/clarify different values for K16/K99
-Page 108: Added constraints for new nets on page90, I2C_TCON_SCL/SDA_CONN per radar 7761747

3/31/2010: Proto 1+ Release 2.2.0 (MAJOR)
- Page 97: Swapped U9701 back to 0mm 353S2896 original orientation before syncing with K16
- Page 97: Deleted OMIT_TABLE BOM option attribute from C9797 and replaced it with actual POR APN 138S0673 symbol. Also, deleted it from BOM table as it is no longer required

5/12/2010: Proto 1+ Agile Release 3.0.0 (FAB)
- Proto 1+ ok2FAB Agile Release!!!

5/17/2010: Release 3.1.0 (Major)-

<rdar://problem/7992365> K99 MLB: Change MCP HVDD_PLL rail to 2.85V
- Page 4: Added APNs 353S2987 & 353S2988 as alternates for 353S2986

<rdar://problem/7964678> K99 MLB BOM: Change MCP APN to A03 version
- Page 4: Added MCP07A03 table. Changed K99_Common to call out A03

<rdar://problem/7861271> K99 MLB: Set SPI operating frequency to 42MHz
<rdar://problem/7851795> K16/K99: Set SPI operating frequency to 42MHz
- Page 4: SPI1 62MHz for PP3V3_S2 WLAN BOM option

<rdar://problem/7838450> K99 MLB: WoW / WoL power control architecture change
- Page 4: Added WLAN_PCTL:HW to K99_Common

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
<rdar://problem/7953783> K99 IPD power regulator new design
- Page 4: Added IPD_PWR:S5 to K99_Common
- Page 41: Aliased =PPBUS_G3H to =PP5V_S5 to =PPBUS_G3H signal

<rdar://problem/7825507> K99 MLB BOM: Change label P/N
- Page 4: Replaced label APN 826-4393 with 825-7557

<rdar://problem/7749046> K99 MLB: Connect SMBUS to internal display connector
- Page 7: Renamed PP3V3_S0_LCDVDD_SW_F to PP3V3_SW_LCD to match page 90 changes, making it convention compliant power net

<rdar://problem/7779132> K99 MLB: Implement deeper sleep S4 state
- Page 7: Renamed PP3V3_S0_LCDVDD_SW_F to PP3V3_SW_LCD to match page 94 changes, making it convention compliant power net

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 8: Removed SYS_LED_ANODE_R
- Page 8: Removed =PP5V_S5 alias

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 8: Added =PP3V3_S5_TPAD to PP3V3_S5 net

<rdar://problem/7963570> K99 MLB: Remove SMS circuit from layout
- Page 59: Deleted cap pads as SMS_INT_L is no longer used

<rdar://problem/7795028> K99 MLB: 5V/3V3 power supply BOM changes per characterization
- Page 74: Changed C7451/C7452 to same APN 131S0287 as C7237/C7239 for BOM consolidation

<rdar://problem/7993241> K99 MLB: Cleanup of CheckPlus warnings/errors
- Page 4: Deleted Z58104 entry (Z58104 is the multi-caps table as symbol is ready
- Page 9: Renamed stiffener Z0920 to MT0900 (Z0920 similar to K16
- Page 9: Tagged POGOS with MT0900 and deleted Z0920
- Page 9: Replaced Z59904 with actual symbol for APN 870-1940 and deleted OMIT_TABLE
- Page 9: Cleaned-up P7/8c 8317/3 SS_WLAN**
- Page 74: Renamed VSNS net$ to VSEN to match page 100 constraints and deleted these nets from constraints table on the same page

- Page 79: Changed OMIT associated with C7980 to OMIT_TABLE
- Page 99: Changed OMIT associated with all caps to OMIT_TABLE

<rdar://problem/7935301> K99 MLB BOM: Change CPU BOM per CE request
- Page 79: Added Critical attribute to R7960
- Page 97: Added Critical attribute to R9700

Synced ALL but pages 1-9,12,28,47,69,70,74,75 and 97 from K16
** Didn't sync page 40 as K16 need to sync it first from K99 to fix OMIT_TABLE attribute as mentioned above**

<rdar://problem/7749046> K99 MLB: Connect SMBUS to internal display connector
- Page 7: Added netclass name to bus, may not be 100% accurate yet

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 53: Changed eDP SMBus nets to "I2C_XDP_" for new aliases on page52
- Page 53: Added XDP to SMBUS_SMC_0_S0 alignment
- Page 76: Cleaned-up page, including correcting application of two PLACE_NEAR grouping and adding an OMIT_TABLE

<rdar://problem/7779132> K99 MLB: Implement deeper sleep S4 state
- Page 50: Added PLACE_NEAR property on R5022 to ensure no stub in fallback case.

<rdar://problem/7794868> K99 MLB: Change to single USB port power switch
- Page 46: Changed U4690 APN to 353S2298

<rdar://problem/7993278> K99 MLB: Schematic sync with K16 MLB
- Page 26: Synced with K16, OMIT changed to OMIT_TABLE
- Page 94: Synced with K16, OMIT changed to OMIT_TABLE and cosmetic clean-up

<rdar://problem/7994057> K99 MLB: Need to add Need_TP=true property to CPU
- Page 10: Added Need_TP=true attribute to pin E37 & D40

<rdar://problem/7871167> K99 MLB: Change RC on CPUVCORE PMON output
- Page 54: Changed C5470 from 0.22UF to 68nF 10% only one in the library

<rdar://problem/7934374> K99 MLB BOM: Replace 376S0868 with 376S0912
- Page 23: Changed Q2300 from 376S0868 to 376S0912

<rdar://problem/7838450> K99 MLB: WoW / WoL power control architecture change
- Page 78: Swapped unused PM_SLP_S3_L to PM_SLP_SUS_L and SMC_ADAPTER_EN_ET to 0.1mm
- Page 78: Added BOM options WLAN_PCTL:HW to Q7891 both halves
- Page 78: Added R7891 0 ohm 1% 0603
- Page 78: Added Bom option WLAN_PCTL:SW to R7891

<rdar://problem/7871918> K99 MLB: Investigate larger replacement for LCD backlight fuse
- Page 90: Changed F9800 to 0603 package APN 740S0115

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
<rdar://problem/7953783> K99 IPD power regulator new design
- Page 77: LP320.2 now connects to PP5V_S5 now
- Page 77: Added U7760 and surrounding circuits. BOM table need to replace later
- Page 77: Added R7760 and R7761 to provide stability
- Page 77: Added min_line_and_neck_width properties to PP5V_S5_LDO
- Page 78: Added R7846 and C7846 0ohm 0.47F (NO STUFF) stuffing options

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 46: Changed R5740 & R5741 for power switch on PP3V3_S2TPAD
- Page 57: Added U5750 USB Mux
- Page 57: Added R5751 (NO STUFF) to bypass U5750 MUX
- Page 78: Added =USB_TPAD_MUX_EN aliased to DDREG_EN

<rdar://problem/7935301> K99 MLB BOM: Change CPU BOM per CE request
- Page 53: Added Critical attribute to Q5400,Q5410
- Page 54: Added Critical attribute to Q5430,Q5413
- Page 97: Removed Critical from C7715

5/19/2010: Release 3.2.0 (Major)-

<rdar://problem/80060377> K99 MLB: Change RC Filter Values on AMON, and BMON
- Page 54: Changed R5481 to 100K APN 115S0196 and C5480 to 0.0033uF APN 132S0009
- Page 54: Changed R5490 to 100K APN 115S0196 and C5490 to 0.0033uF APN 132S0049

<rdar://problem/7986457> K99 MLB: Change LIO Flex connector J4700 to accommodate new LIO Flex
- Page 47: Replaced J4700 with new POR connector APN 516S0862

<rdar://problem/7992365> K99 MLB: Change MCP HVDD_PLL rail to 2.85V
- Page 4: Deleted APN 353S2988 entry from the alternate table
- Page 4: Replaced APN 353S2987 entry with APN 353S3047 (TI) as an alternate
- Page 25: Replaced U2590 with 2.85V LDO APN 353S3048 (MICREL)
- Page 25: Replaced APN 353S2986 with 353S3048 in the BOM table too for HVDDLDO:FIXED

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 57: Connected a new PME signal SMC_PME_S4_L to pin 2

<rdar://problem/8004981> K99 MLB: Connect eDP SMBUS interface to SMC SMBUS 0
- Page 41: Added BOM option for PP3V3_SMC to stuff R5747 & R5743

<rdar://problem/7963570> K99 MLB: Remove SMS circuit from layout
- Page 41: Deleted SMS:NO BOM option as SMS has been removed
- Page 59: Deleted BOM option SMS:YES from R5093
- Page 59: Deleted accelerometer block from the SMBUS page

<rdar://problem/8007333> K99 MLB: Stuff R7872 to enable output connection of ISL power monitor to ADC SYS_PWRGD
- Page 78: Added BOM option S0PGOOD_ISL to R7872

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 81 Added =PP3V3_S3_DBGLEDS alias to =PP3V3_S3_FET for debug LEDS (like K16)
- Page 69: Changed =PP3V3_S3_TPAD to =PP3V3_S3_TPAD_CONN
- Page 69: Renamed PP3V3_S3 going to debug LEDs to =PP3V3_S3_DBGLEDS

<rdar://problem/8007524> K99 MLB: Stuff C9799 to provide better phase margin
- Page 97: Changed C9799 to 22pF

<rdar://problem/8007560> K99 MLB: Change min_neck_width to meet layout requirements
- Page 81: Changed min_neck_width of PP3V3_S3 to 0.1mm
- Page 78: Changed min_neck_width of PP5V_S5 to 0.2mm
- Page 74: Deleted IMVP6_CS_P/N & IMVP6_CS_R_P/N nets from the constraints set as the IMVP6 portion of the page

- Page 97: Changed min_neck_width of PPBUS_SW_BKL to 0.25mm

05/19/2010: Release 3.3.0 (Major)-
<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 69: Fixed netname =PP3V3_S3_DBGLEDS (= sign was missing)

05/21/2010: Release 3.4.0 (Major)-
<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 2: Updated CP0 block to reflect 1.6GHz

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
- Page 41: Changed IPD_PWR:S5 to IPD_5V:S5_EN BOM option to use internal LDO of 5V/3.3V switcher for IPD 5V supply

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 46: Changed R5740 & R5741 for power switch on PP3V3_S2TPAD to PP5V_S5
- Page 57: Changed U5750 USB Mux to PP5V_S5 power supply
- Page 57: Renamed pins 5 & 6 of U5750 USB_IPD CONN_P/N as before
- Page 78: Removed =USB_TPAD_MUX_EN alias to DDREG_EN as MUX has been removed

<rdar://problem/7779132> K99 MLB: Implement deeper sleep S4 state
- Page 41: Added alias for PM_SLP_S4_L to SMC_PME_S4_L
- Page 49: Changed port P34 from SMC_DP_HPD_L to PM_SLP_S4_L
- Page 49: Changed port P35 from PM_SLP_S4_L to PM_SLP_S5_L
- Page 49: Changed ports PB6 from SMC_PB6 to SMC_DP_HPD_L
- Page 50: Removed R5095 PU resistor on SMC_PB6

07/07/2010: Release 4.2.0 (MAJOR)-

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Moved BOM group table on page 4 to page 5 for space limitations

<rdar://problem/8065425> K99 MLB: Add new CPU APN for U1000 - SU9400
- Page 4: Updated SU9400 BOMs with correct EEEEs (Elpida's still pending)
- Page 4: Updated Label table with correct EEEEs for SU9400 configs

<rdar://problem/8151087> K99 MLB BOM: Add new Elpida 2Gb memory
- Page 4: Added 2Gb BOM configuration to Elpida 2GB and 4GB configs
- Page 5: Added DDR3:ELPIDA 4GB BOM group
- Page 5: Added ELPIDA_4GB_BOM option to the Module Parts table (2GB APN is not ready yet- using 2Gb Micron APN as a placeholder)

<rdar://problem/8168390> K99 MLB BOM: Swap 155S0556-> 155S0578, fix 0402 padstack
- Page 51: Changed 155S0556 to 155S0578 to address the 0603 0402 mismatch alternate

<rdar://problem/8151651> K99 MLB BOM: Reduce CPU VCORE 0603 bypass caps
- Page 12: Changed BOM option attribute of C1200,C1201,C1202,C1203,C1204, C1210,C1220,C1221,C1222,C1224,C1225,C1226,C1228,C1229,C1231 from OMIT_TABLE to BOMOPTION=1.6GHZ_ONLY to gate tied to P3V3S5_EN_L, 978914
- Page 110: Removed caps listed above on page 12 from the BOM table as these would get NOSTUFF'ed

7/12/2010: Release 4.3.0 (MAJOR)-

<rdar://problem/8151087> K99 MLB BOM: Add new Elpida 2Gb memory
- Page 4: Updated BOM options table with correct EEEEs for Elpida configs
- Page 4: Added label table with correct EEEEs for Elpida configs
- Page 5: Added 2GB_ELPIDA_BOM option to the Module Parts table
- Page 5: Updated schematic note too for address

<rdar://problem/8141673> K99 MLB: Change eDP connector J9000 pinout
- Page 90: Changed pins 2 to NC and connected pin 4 to PPVOUT_SW_LCDBKLT

<rdar://problem/8224515> K99 MLB: Remove O9090 isolation FET
- Page 90: Removed Q9090 FET and directly connected TCON_I2C bus J9000
- Page 12: Renamed =I2C_TCON_SCL/SDA_CONN net names and kept =I2C_TCON_SCL/SDA

<rdar://problem/8224857> K99 MLB: Replace APN 155S0559 with 155S0423
- (incompatible pad stack)
- Page 4: Changed FL9400-FL9403 and FL9001 back to the original APN 155S0423
- Page 94: Changed FL9400-FL9403back to the original APN 155S0423

<rdar://problem/8224921> K99 MLB: Change R9714 (BKLT_ISET) resistor to 18.2K 1% APN 115S0155
- Page 97: Fixed schematic note - I_LED=369/Riset

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 97: Fixed schematic note - I_LED=369/Riset

7/26/2010: Release 4.4.0 (MAJOR)-

<rdar://problem/8175202> K99 MLB: Move MCP Temp Sensor to SMC B SMBUS
- Page 52: Move MCP TEMP I2C connections to SMC B Bus
- Page 52: Changed R5232 & R5233 to 10K
- Page 52: Changed MCP TEMP I2C address note to reflect 0XD8/0XD9
- Page 53: Added 1.5K APN 115S0105 to set ADDR = 0XD8/0XD9. Updated schematic note too for address

<rdar://problem/8141673> K99 MLB: Change eDP connector J9000 pinout
- Page 90: Changed pine 2 to NC and connected pin 4 to PPVOUT_SW_LCDBKLT

<rdar://problem/8224515> K99 MLB: Remove O9090 isolation FET
- Page 90: Removed Q9090 FET and directly connected TCON_I2C bus J9000
- Page 12: Renamed =I2C_TCON_SCL/SDA_CONN net names and kept =I2C_TCON_SCL/SDA

<rdar://problem/8224857> K99 MLB: Replace APN 155S0559 with 155S0423
- (incompatible pad stack)
- Page 4: Changed FL9400-FL9403 and FL9001 back to the original APN 155S0423
- Page 94: Changed FL9400-FL9403back to the original APN 155S0423

<rdar://problem/8224921> K99 MLB: Change R9714 (BKLT_ISET) resistor to 18.2K 1% APN 115S0155
- Page 97: Fixed schematic note - I_LED=369/Riset

7/27/2010: Release 4.4.1 (MAJOR)-

<rdar://problem/8233353> K99_MLB: Change to dual USB port power switch
- Page 46: Changed USB port power switch U4690 back to dual port TPS2052B APN 353S2298

<rdar://problem/7744955> K99 Proto0 Task: Characterize Voltage/Current/Temperature Sensor
- Page 53: For I2DM, change U5360 to INA210 (APN : 353S2073)
- Page 54: For INIC, change R5412 to 118 Ohms, APN : 115S0127

<rdar://problem/8033256> K99 MLB: Implement 3V3 S5 bleed resistor to satisfy IPD Cumulus Power sequencing shutdown
- Page 78: Added R7894 10Ohm 0603 (will change later) pull-up to =EN_3V3_S5_REG and connected R7894 to pin 1 of U7840 NAND gate tied to P3V3S5_EN_L, 978914 to GND and, U7840.4 output to P3V3S5_EN_L

<rdar://problem/8007560> K99 MLB: Change min_neck width to meet layout requirements
- Page 108: Changed Therm, Sense, Audio line-to-line spacing to 1:1 instead of 2:1

05/28/2010: Release 3.6.0 (Major)-

<rdar://problem/7992365> K99 MLB: Change MCP HVDD_PLL rail to 2.85V (not POR)
- Page 4: Removed APN 353S2986 from the alternate table as it is primary now and replaced 353S2946 with 353S2988 making it its alternate
- Page 4: Changed APN 138S0676 to first alternate (as it's been replaced per GSM(see below)
<rdar://problem/8036605> K99 MLB BOM: Implement MCP_VCORE characterization changes
- Page 4: Added APN 376S0749 as alternate for APN 376S0801 per Intersil FAE

Synced ALL but pages 1-9,12,28,47,69,70,74,75 and 97 from K16 - changes below

<rdar://problem/7992365> K99 MLB: Change MCP HVDD_PLL rail to 2.85V (not POR)
- Page 25: Changed BOM table from 1SU 353S2986 to MIC5366 353s2988, as Intersil is NOT POR

<rdar://problem/8027047> K99 MLB BOM: Swap 132s0247 w/132s0257, 138s0621 w/138s0653, 138s0635 w/138s0654
- Page 25,26: Swapped 138s0621 w/138s0653 as per GSM
- Page 41,73,74: Swapped 138s0635 w/138s0654 as per GSM
- Page 49,73: Swapped 138s0633 w/138s0652 as per GSM

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
- Page 77: Fixed BOM table attribute to attach BOM option value to TBL_BOMOPTION

6/4/2010: EVT Agile Release 4.0.0 (FAB)-

*** EVT OK2FAB Agile Release ***
- No changes since last release 3.6.0
- This release matches Quanta's official BOM for EVT build
- Upcoming changes (Acoustic, Alternates) will be reflected in 4.1 major release, which will match Quanta's deviations for EVT

06/06/2010: Release 4.1.0 (MAJOR)-

<rdar://problem/8065425> K99 MLB: Add new CPU APN for U1000 - SU9400
- Page 4: Added 18 BOMs corresponding to new BOMs
- Page 4: Added 18 new EEEs corresponding to new BOMs
- Page 41: Replaced APN 337S3954 to the BOM module parts table

<rdar://problem/8065431> K99 MLB: Add new Elpida 1Gb memory APN - 333S0565
- Page 4: Added DDR3:ELPIDA_2GB_BOM group and set appropriate CFG bits
- Page 4: Added ELPIDA_4GB_BOM group and CFG bits
- Page 5: Added Elpida 1Gb APN 333S0565 to the BOM module parts table with DRAM_TYPE: ELPIDA_2GB_BOM option

<rdar://problem/8066033> K99 MLB BOM: Change CPU VCORE 0603 bypass caps for acoustics
- Page 4: Added SS_CAP_22uF, MU_CAP_22uF and TY_CAP_22uF BOM options for corresponding vendor BOM group
- Page 4: Added OMIT_TABLE BOM option to C4902
- Page 4: Added OMIT_TABLE BOM option to C4900 & C7361
- Page 41: Added OMIT_TABLE BOM option to C9480
- Page 110: Added BOM config table for 22uF caps for three vendors - Samsung (138S0635), Murata (138S0688). Also assigned C1200-C1231, C4902, C7360, C7361 and C9480 to these groups
- Page 110: Removed C1200-C1231 from 10uF caps BOM config table

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 5: Deleted revision history and replaced it with BOM module parts, Programmable parts and Alternate parts tables as space was limited

<rdar://problem/8065428> K99 MLB: Add alternates per GSM
- Page 5: Added APN 1G4S0029 as an alternate for APN 1G4S0018 per GSM/CE
- Page 5: Added APN 1G7S0139 as an alternate for APN 1G4S0075 per GSM/CE
- Page 5: Added APN 138S0671 as an alternate for APN 138S0673 per GSM/CE
- Page 5: Added APN 138S0672 as an alternate for APN 138S0367 per GSM/CE
- Page 5: Added APN 376S0926 as an alternate for APN 376S0610 per GSM/CE
- Page 5: Added APN 376S0927 as an alternate for APN 376S0329 per GSM/CE
- Page 5: Added APN 377S0107 as an alternate for APN 377S0066 per GSM/CE

<rdar://problem/8064296> K99 MLB: Change pull-up values for SMC 0 SMBus for TCON I2C
- Page 52: Changed R5

Functional Test Points

Fan Connectors

J9700	TRUE	PP5V_S0	7 8 57
J9700	TRUE	FAN_RT_PWM	45
J9700	TRUE	FAN_RT_TACH	45

(NEED TO ADD 1 GND TP)

SPEAKER FUNC_TEST

J9705	TRUE	SPKRAMP_R_N_OUT	48 49
J9705	TRUE	SPKRAMP_R_P_OUT	48 49

INT DP FUNC_TEST

J9800	TRUE	PP3V3_SW_LCD	7 59 (NEED 2 TP)
J9800	TRUE	PPVOUT_SW_LCDBKLT	7 42 59 62 (NEED 2 TP)
J9800	TRUE	DP_INT_ML_F_N<0>	59 71
J9800	TRUE	DP_INT_ML_F_P<0>	59 71
J9800	TRUE	DP_INT_ML_F_N<1>	59 71
J9800	TRUE	DP_INT_ML_F_P<1>	59 71
J9800	TRUE	DP_INT_AUX_CH_C_N	59 71
J9800	TRUE	DP_INT_AUX_CH_C_P	59 71
J9800	TRUE	DP_INT_HPD_CONN	59
J9800	TRUE	LED_RETURN_1	59 62
J9800	TRUE	LED_RETURN_2	59 62
J9800	TRUE	LED_RETURN_3	59 62
J9800	TRUE	LED_RETURN_4	59 62
J9800	TRUE	LED_RETURN_5	59 62
J9800	TRUE	LED_RETURN_6	59 62
J9800	TRUE	=I2C_TCON_SCL	41 59
J9800	TRUE	=I2C_TCON_SDA	41 59

(NEED TO ADD 5 GND TP)

HALL EFFECT CONN (PLACEHOLDER)

J9700	TRUE	SMC_LID_R	49
J9400	TRUE	=PP3V42_G3H_HALL	8 49

SATA HDD

J9300	TRUE	PP3V3_S0_HDD_R	7 35 (NEED 5 TP)
J9300	TRUE	SATA_HDD_R2D_P	35 67
J9300	TRUE	SATA_HDD_R2D_N	35 67
J9300	TRUE	SATA_HDD_D2R_C_P	35 67
J9300	TRUE	SATA_HDD_D2R_C_N	35 67
J9300	TRUE	SMC_HDD_OOB_TEMP	35 38
J9300	TRUE	SMC_HDD_TEMP_CTL	35 38

(NEED TO ADD 6 GND TP)

BATT POWER CONN

J9600	TRUE	SMBUS_SMC_BSA_SCL	41 70
J9600	TRUE	SMBUS_SMC_BSA_SDA	41 70
J9600	TRUE	SYS_DETECT_L	49
J9600	TRUE	PPVBAT_G3H_CONN	49 50 (NEED 4 TP)

(NEED TO ADD 4 GND TP NEAR J6950 AND 1 FOR SHIELD)

LIO CONNECTOR

J9900	TRUE	=PP3V3_S0_AUDIO	37 (NEED 2 TP)
J9900	TRUE	=PP3V42_G3H_ONEWIRE	8 37
J9900	TRUE	SMC_BC_ACOK	9 37 38 39
J9900	TRUE	SYS_ONEWIRE	37 38
J9900	TRUE	=USB_PWR_EN	36 37 57
J9900	TRUE	USB_EXTD_OC_L	18 37
J9900	TRUE	USB_CAMERA_P	18 37 68
J9900	TRUE	USB_CAMERA_N	18 37 68
J9900	TRUE	USB_EXTD_P	18 37 68
J9900	TRUE	USB_EXTD_N	18 37 68
J9900	TRUE	=PP1V8R1V5_S0_AUDIO	8 37
J9900	TRUE	=I2C_LIO_SDA	37 41
J9900	TRUE	=I2C_LIO_SCL	37 41
J9900	TRUE	AUD_GPIO_3	37 48
J9900	TRUE	AUD_I2C_INT_L	19 37
J9900	TRUE	=I2C_MIKEY_SDA	37 41
J9900	TRUE	=I2C_MIKEY_SCL	37 41
J9900	TRUE	AUD_IP_PERIPHERAL_DET	17 37
J9900	TRUE	SPKRAMP_INR_P	37 48 71
J9900	TRUE	SPKRAMP_INR_N	37 48 71
J9900	TRUE	HDA_SDIN0	19 37 68
J9900	TRUE	HDA_SDOUT	19 37 68
J9900	TRUE	HDA_BIT_CLK	19 37 68
J9900	TRUE	HDA_SYNC	19 37 68
J9900	TRUE	HDA_RST_L	19 37 68
J9900	TRUE	AUD_IPHS_SWITCH_EN	19 37

(NEED TO ADD 5 GND TP)

AIRPORT / BT

J9400	TRUE	PCIE_AP_R2D_P	34 67
J9400	TRUE	PCIE_AP_R2D_N	34 67
J9400	TRUE	PCIE_AP_D2R_P	16 34 67
J9400	TRUE	PCIE_AP_D2R_N	16 34 67
J9400	TRUE	PCIE_CLK100M_AP_P	16 34 67
J9400	TRUE	PCIE_CLK100M_AP_N	16 34 67
J9400	TRUE	USB_BT_P	18 34 68
J9400	TRUE	USB_BT_N	18 34 68
J9400	TRUE	WIFI_EVENT_L	34 38 39
J9400	TRUE	=PP3V3_S3_BT	8 34
J9400	TRUE	PP3V3_WLAN_F	7 34 39 (NEED 6 TP)
J9400	TRUE	PCIE_WAKE_L	16 34
J9400	TRUE	AP_RESET_CONN_L	34
J9400	TRUE	AP_CLKREQ_O_L	34

(NEED TO ADD 8 GND TP)

IPD_FLEX_CONN

J9500	TRUE	SMC_TPAD_RST_L	39 46
J9500	TRUE	SMC_LID	38 39 46 49
J9500	TRUE	SMC_ONOFF_L	38 39 46
J9500	TRUE	=I2C_TPAD_SCL	41 46
J9500	TRUE	=I2C_TPAD_SDA	41 46
J9500	TRUE	=PP3V42_G3H_TPAD	8 46
J9500	TRUE	PP3V3_TPAD_CONN	46
J9500	TRUE	PP5V_TPAD_FILT	46
J9500	TRUE	USB_TPAD_CONN_N	46 71
J9500	TRUE	USB_TPAD_CONN_P	46 71

(NEED TO ADD 5 GND TP)

LCP + SPI CONN

J9700	TRUE	=PP3V3_S5_LPCPLUS	8 40
J9700	TRUE	=PP5V_S0_LPCPLUS	8 40
J9700	TRUE	LPC_AD<3..0>	19 38 40 68
J9700	TRUE	SPI_ALT_MOSI	40 68
J9700	TRUE	SPI_ALT_MISO	40 68
J9700	TRUE	LPC_FRAME_L	19 38 40 68
J9700	TRUE	PM_CLKRUN_L	19 38 40
J9700	TRUE	SMC_TMS	38 39 40
J9700	TRUE	LPCPLUS_RESET_L	25 40
J9700	TRUE	SMC_TDO	38 39 40
J9700	TRUE	SMC_TRST_L	38 40
J9700	TRUE	SMC_MD1	38 40
J9700	TRUE	SMC_TX_L	36 38 39 40
J9700	TRUE	LPC_CLK33M_LPCPLUS	25 40 68
J9700	TRUE	SPIROM_USE_MLB	19 40 47
J9700	TRUE	SPI_ALT_CLK	40 68
J9700	TRUE	SPI_ALT_CS_L	40 68
J9700	TRUE	LPC_SERIRQ	19 38 40
J9700	TRUE	LPC_PWRDWN_L	19 38 40
J9700	TRUE	SMC_TDI	38 39 40
J9700	TRUE	SMC_TCK	38 39 40
J9700	TRUE	SMC_RESET_L	38 39 40 50
J9700	TRUE	SMC_NMI	38 40
J9700	TRUE	SMC_RX_L	36 38 39 40
J9700	TRUE	LPCPLUS_GPIO	19 40

(NEED TO ADD 6 GND TP)

DC POWER CONN

J9700	TRUE	=PP18V5_DCIN_CONN	8 49 (NEED 6 TP)
J9700	TRUE	=PP5V_S3_LIO_CONN	8 49

(NEED TO ADD 6 GND TP)

DEBUG VOLTAGE

J9700	TRUE	PPVCORE_S0_CPU	8 42
J9700	TRUE	PPVCORE_S0_MCP	8 42
J9700	TRUE	PP1V05_S0	8 57
J9700	TRUE	PP1V5_S0	8 57 71
J9700	TRUE	PP3V3_S0	8 57 71
J9700	TRUE	PP5V_S0	7 8 57
J9700	TRUE	PP3V3_S3	8
J9700	TRUE	PP5V_S3	8
J9700	TRUE	PP0V9_S5	8
J9700	TRUE	PP3V3_S5	8 57 71
J9700	TRUE	PP3V42_G3H	8
J9700	TRUE	PPBUS_G3H	8 42 49
J9700	TRUE	PP3V3_WLAN_F	7 34 39
J9700	TRUE	PP3V3_S0_HDD_R	7 35
J9700	TRUE	PPDCIN_S5_S5	8
J9700	TRUE	PPVOUT_SW_LCDBKLT	7 42 59 62
J9700	TRUE	PP3V3_SW_LCD	7 59
J9700	TRUE	PP1V5R1V35_S3	8 71
J9700	TRUE	SMC_PM_G2_EN	38 57
J9700	TRUE	PM_SLP_S4_L	19 38 57
J9700	TRUE	PM_SLP_S3_L	19 38 39 57
J9700	TRUE	PP0V9_ENET	8
J9700	TRUE	PP1V05_S0_MCP_PLL_UF	8
J9700	TRUE	PP3V3_ENET	8
J9700	TRUE	PP3V3_SW_DPPWR	41
J9700	TRUE	PP5V_S3_RTUSB_A_F	36
J9700	TRUE	PPBUS_G3H_ISNS	8

(NEED TO ADD 27 GND TP)

FSB SIGNALS WITH NOTEST

J9700	NO_TEST=TRUE	FSB_A_L<35..3>	10 14 65
J9700	NO_TEST=TRUE	FSB_ADS_L	10 14 65
J9700	NO_TEST=TRUE	FSB_ADSTB_L<1..0>	10 14 65
J9700	NO_TEST=TRUE	FSB_D_L<63..0>	10 14 65
J9700	NO_TEST=TRUE	FSB_DINV_L<3..0>	10 14 65
J9700	NO_TEST=TRUE	FSB_DSTB_L_N<3..0>	10 14 65
J9700	NO_TEST=TRUE	FSB_DSTB_L_P<3..0>	10 14 65
J9700	NO_TEST=TRUE	FSB_HIT_L	10 14 65
J9700	NO_TEST=TRUE	FSB_HITM_L	10 14 65
J9700	NO_TEST=TRUE	FSB_LOCK_L	10 14 65
J9700	NO_TEST=TRUE	FSB_REQ_L<4..0>	10 14 65

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE

FUNCTIONAL TEST

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

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"S0,S0M" RAILS

53 =PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU — 7 42
18 A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU — 11 12 64

55 =PPCPUVTT_S0_REG — PP1V05_S0 — 7 57
9.40 A
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU — 10 11 12
=PP1V05_S0_MCP_FSB — 14 20 23
=PP1V05_S0_MCP_AVDD_UF — 23
=PP1V05_S0_MCP_SATA_DVDD — 20 23
=PP1V05_S0_MCP_PLL_UF_R — 56
=PP1V05_SW_MCP_FSB — 20 23
=PP1V05_S0_MCP_PE_DVDD — 20 23
=PP1V05_S0_MCP_M2CLK_DLL — 15 23
=PP1V05_S0_MCP_DP0_VDD — 17 24
=PP1V05_S0_XDP — 13

54 =PPMCPCORE_S0_REG — PPVCORE_S0_MCP — 7 42
(MCP VCORE AFTER SENSE RES)
23.8 A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP — 20 23
=PPVCORE_S0_MCPGFXFET — 22

LVDDR VRef/VTT (0.75V/0.675V) Rails

52 =PPVTT_S0_DDR_LDO — PPDDRVTT_S0
1.20 A
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PPDDRVTT_S0_MEM_A — 32
=PPDDRVTT_S0_MEM_B — 32

52 33 =PPVTT_S3_DDR_BUF — PPDDRVREF_S3
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

56 =PP1V5_S0_REG — PP1V5_S0 — 7 57 71
.210 A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU — 11 12
=PP1V5_S0_MCP_PLL_VLDO — 56
=PP1V8R1V5_S0_AUDIO — 7 37
=PP3V3R1V5_S0_MCP_HDA — 19 23

56 =PP1V05_S0_MCP_PLL_OR — PP1V05_S0_MCP_PLL_UF — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_MCP_PLL_UF — 23

58 =PP5V_S0_FET — PP5V_S0 — 7 57
0.100 A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_LPCPLUS — 7 40
=PP5V_S0_FAN — 45
=PP5V_S0_CPU_IMVP — 53
=PP5VR3V3_S0_DPCADET — 61
=PP5V_S0_CPUVTTS0 — 55
=PP5V_S0_BKL — 62
=PP5V_S0_MCPREG — 54
=PP5V_S0_MCPFSBFET — 22

59 =PP3V3_S0_FET — PP3V3_S0 — 7 57 71
3.30 A
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_XDP — 13
=PP3V3_S0_MCP — 20 23
=PP3V3_S0_P1V5S0 — 56
=PP3V3_S0_DEBUGROM — 40
=PP3V3_S0_SMBUS_SMC_0_S0 — 41
=PP3V3_S0_SMBUS_SMC_B_S0 — 41
=PP3V3_S0_SMBUS_MCP_0 — 41
=PP3V3_S0_FAN — 45
=PP3V3_S0_AUDIO — 7 37
=PP3V3_S0_IMVP — 53
=PP3V3_S0_MCP_GPIO — 17 18 19
=PP3V3_S0_MCP_PLL_UF — 23
=PP3V3_S0_MCP_HVDD — 20 23
=PP3V3_S0_SMC — 39
=PP3V3_S0_MCPTHMSNS — 44
=PP3V3_S0_CPUTHMSNS — 44
=PP3V3_S0_PWRCTL — 57
=PP3V3_S0_SMBUS_MCP_1 — 41
=PP3V3_S0_HDD — 35
=PP3V3_S0_MCP_PLL_VLDO — 56
=PP3V3_S0_MCPCOREISNS — 43
=PP3V3_S0_MCPDDRISNS — 43
=PP3V3_S0_BKLTISNS — 42
=PP3V3_S0_CSREGISNS — 43
=PP3V3_S0_BKL_VDDIO — 62
=PP3V3_S0_DPCONN — 61
=PP3V3_S0_HDDISNS — 42

"ENET" RAILS

9 =PP3V3_ENET_FET_R — PP3V3_ENET — 7
400mA
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
300mA =PP3V3_ENET_MCP_RMGT — 18 20 23
~100mA =PP3V3_ENET_MCP_PLL_MAC — 23

58 =PP0V9_ENET_FET — PP0V9_ENET — 7
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V9_ENET_MCP_RMGT — 20 23

"S3" RAILS

LVDDR (1.5V/1.35V) Rails

52 =PPDDR_S3_REG — PP1V5R1V35_S3 — 7 71
11.30 A
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE (OR 1.35V)
=PPLVDDR_S3_MEM_A — 26 27 30
=PPLVDDR_S3_MEM_B — 28 29 31
0 mA =PP1V5R1V35_S3_MCP_MEM — 15
4250 mA =PP1V5R1V35_S0_MCPDDRFET — 21
=PPVIN_S0_DDRREG_LDO — 52

58 =PP3V3_S3_FET — PP3V3_S3 — 7
1.274 A
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_SMBUS_SMC_A_S3 — 41
=PP3V3_S3_PDCISENS — 52
=PP3V3_S3_VREFMRGN — 33
=PP3V3_S3_MCP_GPIO — 19
=PP3V3_S3_SMS — 39
=PP3V3_S3_1V5S3ISNS — 42
=PP3V3_S3_WLANISNS — 42
=PP3V3_S3_DBGLEDS — 49
=PP3V3_S3_BT — 7 34
=PP3V3_S3_WLAN — 34
=PP3V3_S3_TPAD — 46

51 =PP5V_S3_REG — PP5V_S3 — 7
5.40 A
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_MCPDDRFET — 21
=PP5V_S3_SYSLED — 39
=PP5V_S3_TPAD — 56
=PP5V_S3_DDRREG — 52
=PP5V_S3_AUDIO_AMP — 48
=PP5V_S3_P5VS0FET — 58
=PP5V_S3_RTUSB — 36
=PP5V_S3_LIO_CONN — 7 49

"S5" RAILS

57 51 =PP3V3_S5_REG — PP3V3_S5 — 7 57 71
1.07 A + S3 + S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_MCP_GPIO — 18 19
=PP3V3_S5_ROM — 47
=PP3V3_S5_MCP — 20 23
=PP3V3_S5_MCPPWRGD — 25
=PP3V3_S5_P3V3S3FET — 58
=PP3V3_S5_P3V3S0FET — 58
=PP3V3_S5_P3V3ENETFET — 58
=PP3V3_S5_P0V9S5 — 56 57
=PP3V3_S5_VMON — 57
=PP3V3_S5_SMBUS_SMC_MGMT — 41
=PP3V3_S5_P0V9ENETFET — 58
=PP3V3_S5_TPAD — 46
=PP3V3_S5_DP_PORT_PWR — 61
=PP3V3_S0_LCD — 59
=PP3V3_SMC_PME — 39

56 =PP0V9_S5_REG — PP0V9_S5 — 7
0.290 A
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
105 mA/241 mA =PP0V9_S5_MCP_VDD_AUXC — 20 23
=PP0V9_ENET_P0V9ENETFET — 58

"G3H" RAILS

49 =PP3V42_G3H_REG — PP3V42_G3H — 7
0.064
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PPVIN_S5_SMCVREF — 39
=PP3V42_G3H_SMBUS_SMC_BSA — 41
=PP3V42_G3H_PWRCTL — 57
=PP3V42_G3H_CHGR — 50 57
=PP3V42_G3H_SMCUSBMUX — 36
=PP3V42_G3H_TPAD — 7 46
=PP3V42_G3H_HALL — 7 49
=PP3V3_S5_SMC — 38 39
=PP3V3_S5_LPCPLUS — 7 40
=PP3V42_G3H_BMON_ISNS — 43
=PP3V42_G3H_ONEWIRE — 7 37
PP3V3_G3_RTC — 19 20 23

49 7 =PP18V5_DCIN_CONN — PPDCIN_S5_S5 — 7
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PPDCIN_S5_CHGR — 50

50 =PPBUS_G3H — PPBUS_G3H — 7 42 49
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPBUS_S0_LCDBKLT — 63
=PPVIN_S5_P5VP3V3 — 51
=PPBUS_G3H_R_IN — 43
=PPBUS_5V_S5 — 56

43 =PPBUS_G3H_R_OUT — PPBUS_G3H_ISNS — 7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=8.4V
MAKE_BASE=TRUE
=PPVIN_S0_CPUVTTS0 — 55
=PPVIN_S5_CPU_IMVP — 53
=PPVIN_S0_MCPCORE — 54
=PPVIN_S3_DDRREG — 52

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009
PAGE TITLE: Power Aliases
Apple Inc.
DRAWING NUMBER 051-8379 SIZE D
REVISION 4.4.0
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HEAT SINK MOUNTING BOSSES

Z0906 STDOFF-4.5OD1.8H-SM
Z0907 STDOFF-4.5OD1.8H-SM
Z0908 STDOFF-4.5OD1.8H-SM
Z0909 STDOFF-4.5OD1.8H-SM
Z0910 STDOFF-4.5OD1.8H-SM
Z0911 STDOFF-4.5OD1.8H-SM
Z0912 STDOFF-4.5OD1.8H-SM
Z0913 STDOFF-4.5OD1.8H-SM

FAN BOSS

Z0905 STDOFF-4.5OD1.8H-SM

SSD BOSS

Z0915 STDOFF-4.5OD1.9H-SM

X16 BOSS

Z0914 STDOFF-4.5OD1.9H-SM

MDP CONN METAL TAB

NOSTUFF
MT0900
STIFFENER-K16-K99
SM-SP

EMI IO POGO PINS

CRITICAL
ZS0904
POGO-2.0OD-2.95H-K86-K87
SM

CRITICAL
ZS0905
1.4DIA-SHORT-SILVER-K99
SM

CRITICAL
ZS0906
POGO-2.0OD-3.6H-K86-K87
SM

CRITICAL
ZS0907
POGO-2.0OD-3.6H-K86-K87
SM

PCI-E ALIASES

UNUSED GPU LANES

16	=PEG_D2R_N<5:4>	NC_PEG_D2RN<5:4>	NO_TEST=TRUE, MAKE_BASE=TRUE
16	=PEG_D2R_P<5:4>	NC_PEG_D2RP<5:4>	NO_TEST=TRUE, MAKE_BASE=TRUE
16	=PEG_R2D_C_N<5:4>	NC_PEG_R2DCN<5:4>	NO_TEST=TRUE, MAKE_BASE=TRUE
16	=PEG_R2D_C_P<5:4>	NC_PEG_R2DCP<5:4>	NO_TEST=TRUE, MAKE_BASE=TRUE
67 16	PEG_CLK100M_P	NC_PEG_CLK100MP	NO_TEST=TRUE, MAKE_BASE=TRUE
67 16	PEG_CLK100M_N	NC_PEG_CLK100MN	NO_TEST=TRUE, MAKE_BASE=TRUE
16	PEG_CLKREQ_L	NC_PEG_CLKREQ_L	NO_TEST=TRUE, MAKE_BASE=TRUE
16	ENET_CLKREQ_L	NC_ENET_CLKREQ_L	NO_TEST=TRUE, MAKE_BASE=TRUE

USB ALIASES

UNUSED USB PORTS

68 18	USB_SDCARD_P	NC_USB_SDCARDP	NO_TEST=TRUE, MAKE_BASE=TRUE
68 18	USB_SDCARD_N	NC_USB_SDCARDN	NO_TEST=TRUE, MAKE_BASE=TRUE
68 19	USB_MINI_P	NC_USB_MINIP	NO_TEST=TRUE, MAKE_BASE=TRUE
68 19	USB_MINI_N	NC_USB_MININ	NO_TEST=TRUE, MAKE_BASE=TRUE
68 19	USB_EXTC_P	NC_USB_EXTCP	NO_TEST=TRUE, MAKE_BASE=TRUE
68 19	USB_EXTC_N	NC_USB_EXTCN	NO_TEST=TRUE, MAKE_BASE=TRUE

ETHERNET ALIASES

PLACE_NEAR=U7980.A1:5MM
R0911 0 5% 1/16W MF-LF 402
PP3V3_ENET_FET — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
=PP3V3_ENET_FET 58
=PP3V3_ENET_FET_R OUTPUT 8

ENET_RXD_PD MAKE_BASE=TRUE
ENET_RXD<0> OUTPUT 18 69
ENET_RXD<1> OUTPUT 18 69
ENET_RXD<2> OUTPUT 18 69
ENET_RXD<3> OUTPUT 18 69
ENET_RXCLK_PD MAKE_BASE=TRUE
ENET_CLK125M_RXCLK OUTPUT 18 69
ENET_RX_CTRL OUTPUT 18 69
ENET_MDIO BI 18 69
MCP_RGMII_VREF OUTPUT 18
ENET_ENERGY_DET OUTPUT 18

R0980 10K 5% 1/20W MF 201
R0981 10K 5% 1/20W MF 201
R0982 10K 5% 1/20W MF 201
R0983 10K 5% 1/20W MF 201
R0984 10K 5% 1/20W MF 201
R0985 10K 5% 1/20W MF 201

GND — VOLTAGE=0V, MIN_LINE_WIDTH=0.50MM, MIN_NECK_WIDTH=0.20MM

LVDS ALIASES

17	=MCP_IFPA_TXC_P	NC_LVDS_IG_A_CLKP	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPA_TXC_N	NC_LVDS_IG_A_CLKN	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPA_TXD_P<0..3>	NC_LVDS_IG_A_DATAP<0..3>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPA_TXD_N<0..3>	NC_LVDS_IG_A_DATAN<0..3>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPB_TXC_P	NC_LVDS_IG_B_CLKP	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPB_TXC_N	NC_LVDS_IG_B_CLKN	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPB_TXD_P<0..3>	NC_LVDS_IG_B_DATAP<0..3>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPB_TXD_N<0..3>	NC_LVDS_IG_B_DATAN<0..3>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	LCD_IG_BKLT_PWM	LCD_BKLT_PWM 62	MAKE_BASE=TRUE
59 17 9	LCD_IG_PWR_EN	LCD_IG_PWR_EN 9 17 59	MAKE_BASE=TRUE
17	LCD_IG_BKLT_EN	LCD_BKLT_EN 63	MAKE_BASE=TRUE
17	=MCP_IFPAB_DDC_CLK	TP_LVDS_DDC_CLK	MAKE_BASE=TRUE
17	=MCP_IFPAB_DDC_DATA	TP_LVDS_DDC_DATA	MAKE_BASE=TRUE

DISPLAY PORT ALIASES

67 17	DP_IG_ML0_P<0..3>	DP_EXT_ML_P<0..3> 61 71	MAKE_BASE=TRUE
67 17	DP_IG_ML0_N<0..3>	DP_EXT_ML_N<0..3> 61 71	MAKE_BASE=TRUE
17	DP_IG_HPD0	DP_EXT_HPD 61	MAKE_BASE=TRUE
67 17	DP_IG_AUX_CH0_P	DP_EXT_AUX_CH_P 61	MAKE_BASE=TRUE
67 17	DP_IG_AUX_CH0_N	DP_EXT_AUX_CH_N 61	MAKE_BASE=TRUE
60	DP_AUX_CH_C_N	DP_EXT_AUX_CH_C_N 61 71	MAKE_BASE=TRUE
60	DP_AUX_CH_C_P	DP_EXT_AUX_CH_C_P 61 71	MAKE_BASE=TRUE
60	DP_CA_DET	DP_EXT_CA_DET 61	MAKE_BASE=TRUE
67 17	DP_IG_ML1_P<1:0>	DP_INT_ML_P<1:0> 59 71	MAKE_BASE=TRUE
67 17	DP_IG_ML1_N<1:0>	DP_INT_ML_N<1:0> 59 71	MAKE_BASE=TRUE
67 17	DP_IG_AUX_CH1_P	DP_INT_AUX_CH_P 59 71	MAKE_BASE=TRUE
67 17	DP_IG_AUX_CH1_N	DP_INT_AUX_CH_N 59 71	MAKE_BASE=TRUE
17	DP_IG_HPD1	DP_INT_HPD 59	MAKE_BASE=TRUE
17	DP_IG_ML1_P<3:2>	TP_DP_INT_MLP<3:2>	MAKE_BASE=TRUE
17	DP_IG_ML1_N<3:2>	TP_DP_INT_MLN<3:2>	MAKE_BASE=TRUE

SATA ALIASES

UNUSED SATA ODD SIGNALS

67 18	SATA_ODD_R2D_C_P	NC_SATA_ODD_R2DCP	NO_TEST=TRUE, MAKE_BASE=TRUE
67 18	SATA_ODD_R2D_C_N	NC_SATA_ODD_R2DCN	NO_TEST=TRUE, MAKE_BASE=TRUE
67	SATA_ODD_R2D_P	NC_SATA_ODD_R2DP	NO_TEST=TRUE, MAKE_BASE=TRUE
67	SATA_ODD_R2D_N	NC_SATA_ODD_R2DN	NO_TEST=TRUE, MAKE_BASE=TRUE
67 18	SATA_ODD_D2R_P	NC_SATA_ODD_D2RP	NO_TEST=TRUE, MAKE_BASE=TRUE
67 18	SATA_ODD_D2R_N	NC_SATA_ODD_D2RN	NO_TEST=TRUE, MAKE_BASE=TRUE

CPU ALIASES

65 10	CPU_BSEL<0:2>	=MCP_BSEL<0:2>	MAKE_BASE=TRUE
14	CPU_PECI_MCP	TP_CPU_PECI_MCP	MAKE_BASE=TRUE

BSEL<2..0> 14	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

MCP89 ALIASES

17	TP_MCP_RGB_DAC_VREF	NC_MCP_RGB_DAC_VREF	NO_TEST=TRUE, MAKE_BASE=TRUE
66 15	MEM_A_CLK_P<1>	TP_MEM_A_CLKP<1>	MAKE_BASE=TRUE
66 15	MEM_A_CLK_N<1>	TP_MEM_A_CLKN<1>	MAKE_BASE=TRUE
66 15	MEM_B_CLK_P<1>	TP_MEM_B_CLKP<1>	MAKE_BASE=TRUE
66 15	MEM_B_CLK_N<1>	TP_MEM_B_CLKN<1>	MAKE_BASE=TRUE
66 15	MEM_A_A<15>	TP_MEM_A_A<15>	MAKE_BASE=TRUE
66 15	MEM_B_A<15>	TP_MEM_B_A<15>	MAKE_BASE=TRUE
19	MCP_MEM_VDD_SEL_1V5	TP_MEM_VDD_SEL_1V5	MAKE_BASE=TRUE

CHARGER SIGNAL

50 =CHGR_ACOK IN — SMC_BC_ACOK MAKE_BASE=TRUE OUTPUT 7 37 38 39

MCPCOREISNS SIGNAL

54 MCPCORES0_VO — MAKE_BASE=TRUE — =MCPCOREISNS_N 43
54 MCPCORES0_ISP_R — MAKE_BASE=TRUE — =MCPCOREISNS_P 43

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE
SIGNAL ALIAS

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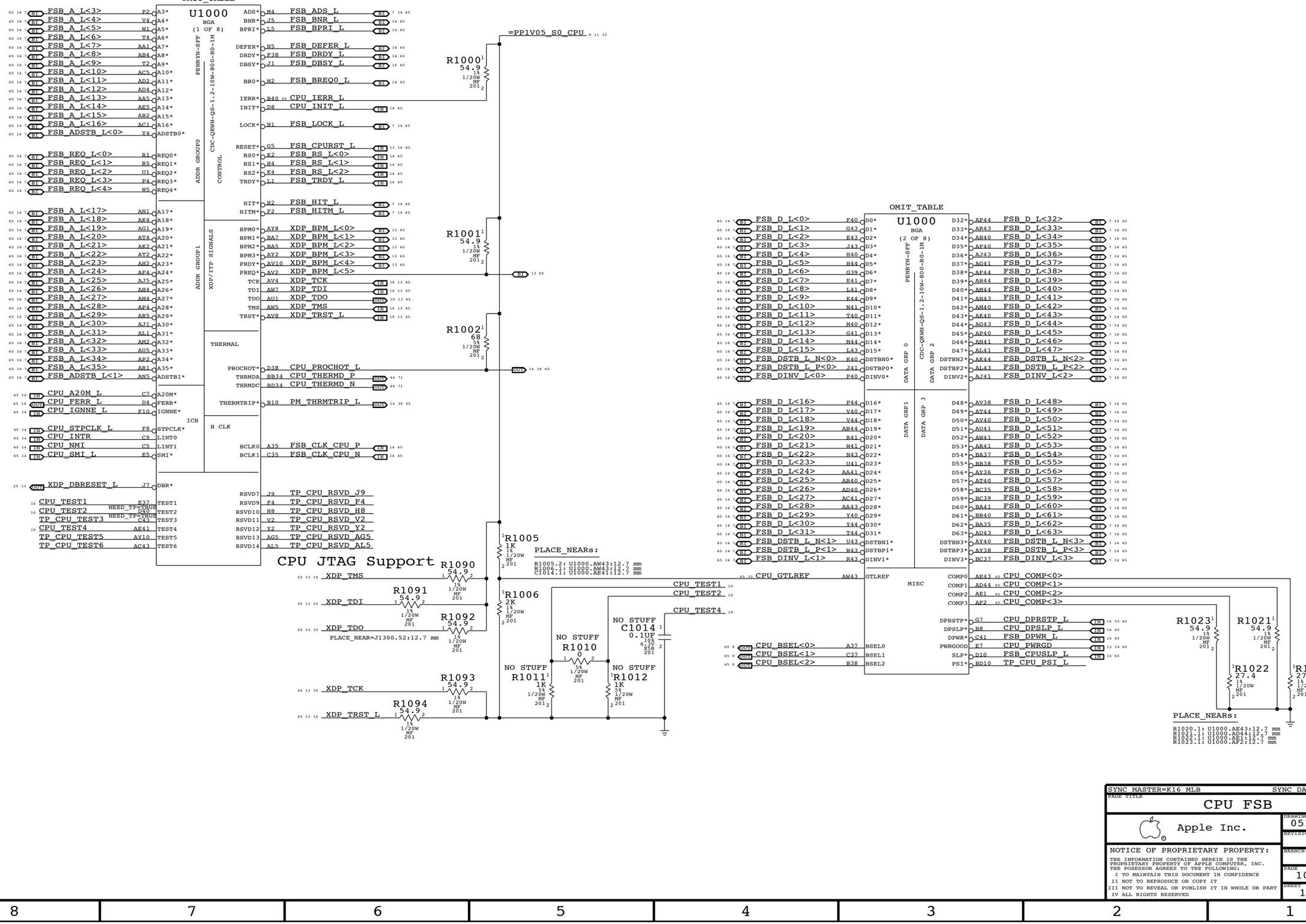

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

CPU FSB

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(CPU CORE POWER)
=PPVCORE_S0_CPU 8 11 12 64

18 A (CULV Design Target)
17.6 A (CULV ICC_Max)

OMIT_TABLE

U1000
BGA
(7 OF 8)
PENRYN-SFF
CDC-QKWH-QS-1.2-10W-800-R0-1M

BD30	K20		
BB28	M16		
BB30	M18		
B24	K16		
B22	K18		
H22	V20		
H24	T20		
F22	P20		
F24	V16		
D24	V18		
D22	T16		
M22	T18		
M24	P16		
K22	P18		
K24	AD20		
V22	AB20		
V24	Y20		
T22	AD16		
T24	AD18		
P22	AB16		
P24	AB18		
AD22	Y16		
AD24	Y18		
AB22	AK20		
AB24	AK16		
Y22	AK18		
Y24	AH20		
AK22	AP20		
AK24	AH16		
AH22	AH18		
AH24	AF16		
AF22	AF18		
AF24	AP20		
AP22	AM20		
AP24	AP16		
AM22	AP18		
AM24	AM16		
AY22	AM18		
AY24	AY20		
AV22	AV20		
AV24	AT20		
AT22	AY16		
AT24	AY18		
BD22	AV16		
BD24	AV18		
BB22	AT16		
BB24	AT18		
B20	BD20		
B18	BB20		
B16	BD16		
H20	BD18		
F20	BB16		
D20	BB18		
H16	AP14		
H18	AM14		
F16	AY14		
F18	AV14		
D18	AT14		
D16	BD14		
M20	BB14		

VCC

OMIT_TABLE

U1000
BGA
(3 OF 8)
PENRYN-SFF
CDC-QKWH-QS-1.2-10W-800-R0-1M

H32	AD28		
G33	AD30		
F32	AB28		
N33	AB30		
M32	Y28		
L33	Y30		
K32	AK26		
J33	AH26		
W33	AF26		
V32	AK28		
U33	AK30		
T32	AH28		
R33	AH30		
P32	AF28		
AD32	AF30		
AC33	AP26		
AB32	AM26	VCC	
AA33	AP28		
Y32	AP30		
AK32	AM28		
AJ33	AM30		
AH32	AY26		
AG33	AV26		
AF32	AT26		
AE33	AY28		
AR33	AY30		
AP32	AV28		
AN33	AV30		
AM32	AT28		
AL33	AT30		
AY32	BD26		
AV32	BB26		
AU33	BD28		
AT32			
AT34			
BD32			
BB32			
B26			
B30			
B28			
H26			
F26			
D26			
H28			
H30			
F28			
F30			
D30			
D28			
M26			
K26			
M28			
M30			
K28			
K30			
V26			
T26			
P26			
V28			
V30			
T28			
T30			
P28			
P30			
AD26			
AB26			
Y26			

VCC

(CPU IO POWER 1.05V)
=PP1V05_S0_CPU 8 10 11 12

4500 mA (before VCC stable)
2500 mA (after VCC stable)

N37			
L37			
K38			
J37			
W37			
V38			
U37			
R37		VCCP	
P38			
AC37			
AB38			
AA37			
AK38			
AJ37			
AG37			
AF38			

(CPU INTERNAL PLL POWER 1.5V)
=PP1V5_S0_CPU 8 12

B34		
D34		VCCA

130 mA

BD8	CPU_VID<0>	OUT	12 53 65
BC7	CPU_VID<1>	OUT	12 53 65
BB10	CPU_VID<2>	OUT	12 53 65
BB8	CPU_VID<3>	OUT	12 53 65
BC5	CPU_VID<4>	OUT	12 53 65
BB4	CPU_VID<5>	OUT	12 53 65
AY4	CPU_VID<6>	OUT	12 53 65

VID

=PPVCORE_S0_CPU 8 11 12 64

R1100
100
1%
1/20W
MF
201
PLACE_NEAR=U1000.BD12:25.4 mm

VCCSENSE	BD12	CPU_VCCSENSE_P	OUT 53 65
VSSSENSE	BC13	CPU_VCCSENSE_N	OUT 53 65

PLACE_NEAR=U1000.BC13:25.4 mm
R1101
100
1%
1/20W
MF
201

=PP1V05_S0_CPU 8 10 11 12

OMIT_TABLE

U1000
BGA
(8 OF 8)
PENRYN-SFF
CDC-QKWH-QS-1.2-10W-800-R0-1M

AE37	R13		
AP38	P12		
AN37	P14		
AL37	AB10		
C33	AD14		
B32	AC11		
H36	AC13		
F36	AB12		
G35	AB14		
F34	AA11		
E33	AA13		
E35	Y14		
D32	AK10		
K36	AP10		
N35	AK12		
L35	AK14		
J35	AJ11		
W35	AJ13		
V36	AH14		
P36	AG11		
U35	AG13		
R35	AF12		
AB36	AF14		
AC35	AE11		
AA35	AE13		
AK36	AP10		
AF36	AR11		
AJ35	AR13		
AG35	AP12		
AE35	AN11		
AP36	AN13	VCCP	
AN35	AL11		
AL35	AL13		
C13	AU11		
B14	AU13		
B12	N7		
H12	N9		
H14	L7		
G11	L9		
G13	W7		
F12	W9		
F14	U7		
E11	U9		
E13	R7		
D14	R9		
D12	AC7		
K10	AC9		
N11	AA7		
N13	AA9		
M14	AJ7		
L11	AJ9		
L13	AG7		
K12	AG9		
K14	AE7		
J11	AE9		
J13	AR7		
V10	AR9		
P10	AN7		
W11	AN9		
W13	AL7		
V12	AL9		
V14	A33		
U11	A13		
U13			
T14			
R11			

VCCP

OMIT_TABLE

U1000
BGA
(4 OF 8)
PENRYN-SFF
CDC-QKWH-QS-1.2-10W-800-R0-1M

B42	AP34		
H42	AM34		
F42	AV36		
D42	AT36		
D44	AY34		
F44	AW33		
M42	AW35		
K42	AV34		
V42	AU35		
T42	BD36		
P42	BB36		
AD42	BC33		
AB42	BA33		
Y42	C31		
AK42	C29		
AH42	C27		
AF42	G31		
AP42	E31		
AM42	G27		
AY42	G29		
AV42	E27		
AT42	E29		
AV44	N31		
AY44	L31		
BB42	J31		
BA43	N27		
C39	N29		
H38	L27		
G37	L29		
E39	J27		
N39	J29		
M38	W31		
L39	W27		
J39	W29		
W39	U31		
U39	R31		
T38	U27		
R39	U29		
AD38	R27		
AC39	R29		
AA39	AC31	VSS	
Y38	AA31		
AJ39	AC27		
AH38	AC29		
AG39	AA27		
AE39	AA29		
AR37	AJ31		
AR39	AG31		
AN39	AE31		
AM38	AJ27		
AL39	AJ29		
AW37	AG27		
AW39	AG29		
AU37	AE27		
AU39	AE29		
AT38	AR31		
BD38	AR27		
BD40	AR29		
BC41	AN31		
BA39	AL31		
B36	AN27		
D36	AN29		
H34	AL27		
M36	AL29		
M34	AW31		
K34	AU31		
T36	AW27		
V34	AW29		
T34	AU27		
P34	AU29		
AD36	BC31		
Y36	BA31		
AD34	BC27		
AB34	BC29		
Y34	BA27		
AK34	BA29		
AH36	C25		
AH34	C23		
AF34	C21		
AR35	G21		
AM36	G23		
	G25		

VSS

OMIT_TABLE

U1000
BGA
(5 OF 8)
PENRYN-SFF
CDC-QKWH-QS-1.2-10W-800-R0-1M

E21	AE17		
E23	AE19		
E25	AR17		
N21	AR19		
N23	AN17		
N25	AN19		
L21	AL17		
L23	AL19		
L25	AW17		
J21	AW19		
J23	AU17		
J25	AU19		
W21	BC17		
W23	BC19		
W25	BA17		
U21	BA19		
U23	C15		
U25	C11		
R21	H10		
R23	G15		
R25	E15		
AC21	M10		
AC23	N15		
AC25	L15		
AA21	J15		
AA23	M12		
AA25	T10		
AJ21	W15		
AJ23	U15		
AJ25	R15		
AG21	T12		
AG23	AD10		
AG25	Y10		
AE21	AC15		
AE23	AA15		
AE25	AD12		
AR21	Y12		
AR23	AH10		
AR25	AJ15		
AN21	AG15		
AN23	AE15	VSS	
AN25	AH12		
AL21	AM10		
AL23	AR15		
AL25	AN15		
AW21	AL15		
AW23	AM12		
AW25	AT10		
AU21	AW15		
AU23	AU15		
AU25	AY12		
BC21	AW11		
BC23	AW13		
BC25	AV12		
BA21	AT12		
BA23	BC15		
BA25	BA15		
C19	BC11		
C17			
G17	BB12		
G19	BA11		
E17	BA13		
E19	B6		
N17	H6		
N19	G9		
L17	F6		
L19	E9		
J17	D6		
J19	M6		
W17	M8		
W19	K6		
U17	K8		
U19	U5		
R17	V6		
R19	V8		
AC17	T6		
AC19	T8		
AA17	P6		
AA19	P8		
AJ17	AD6		
AJ19	AD8		
AG17	AB6		
AG19	AB8		

VSS

OMIT_TABLE

U1000
BGA
(6 OF 8)
PENRYN-SFF
CDC-QKWH-QS-1.2-10W-800-R0-1M

Y6	AJ3		
Y8	AG3		
AK6	AE3		
AK8	AR3		
AH6	AN3		
AH8	AL3		
AF6	AW3		
AF8	AU3		
AP6	BD4		
AP8	BC3		
AM6	BB2		
AM8	BA3		
AY6	G1		
AW9	E1		
AU7	AW1		
AV6	BA1		
AU9	A39		
AT6	A41	VSS	
AT8	A31		
BD6	A27		
BC9	A29		
BB6	A21		
BA9	A23		
C3	A25		
B4	A17		
G3	A19		
E3	A15		
D2	A11		
N3	A9		
L3	A5		
J3	A7		
W3			
U3			
R3			
AC3			
AA3			

VSS

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE
CPU Power & Ground

Apple Inc.

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CPU VCORE HF AND BULK DECOUPLING

4x 270uF. 32x 10uF 0603, 28x 2.2uF 0402 + 40x 2.2uF 0402

64 11 8 =PPVCORE_S0_CPU

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL NOSTUFF C1200 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1201 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1202 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1203 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1204 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1205 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1206 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1207 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1208 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1209 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1210 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1211 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1212 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1213 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1214 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1215 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1216 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1217 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1218 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1219 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL NOSTUFF C1220 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1221 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1222 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1223 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1224 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1225 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1226 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1227 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1228 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1229 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1230 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1231 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1240 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1241 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1242 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1243 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1244 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1245 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1246 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1247 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1248 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1249 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1250 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1251 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1252 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1253 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1254 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1255 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1256 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1257 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1258 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1259 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1260 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1261 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1262 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1263 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1264 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1265 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1266 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1267 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

CRITICAL C1270 270UF 20% 2V TANT CASE-B4-SM
CRITICAL C1271 270UF 20% 2V TANT CASE-B4-SM
CRITICAL C1272 270UF 20% 2V TANT CASE-B4-SM

CPU VCORE VID CONNECTIONS

65 53 11 CPU_VID<0..6> — IMVP6_VID<0..6> 65
MAKE_BASE=TRUE

VCCA (CPU AVdd) DECOUPLING

11 8 =PP1V5_S0_CPU 1x 10uF, 1x 0.01uF

OMIT_TABLE C1280 10uF 20% 6.3V X5R 603
C1281 0.01UF 10% 16V X5R 201

LAYOUT NOTE:
PLACE C1281 NEAR PIN B34 OF U1000

VCCP (CPU I/O) DECOUPLING

11 10 8 =PP1V05_S0_CPU 1x 270uF, 12x 2.2uF

OMIT_TABLE C1283 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1284 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1285 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1286 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1287 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1288 2.2UF 20% 6.3V CERM 402-LF

CRITICAL C1290 270UF 20% 2V TANT CASE-B4-SM
OMIT_TABLE C1291 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1292 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1293 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1294 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1295 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1296 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE C1290 CLOSE TO CPU
PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
PLACE C1291-C1296 CLOSE TO FSB DATA PINS

SYNC_MASTER=K16_MLB SYNC_DATE=03/24/2010

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CPU Decoupling & VID

Apple Inc.

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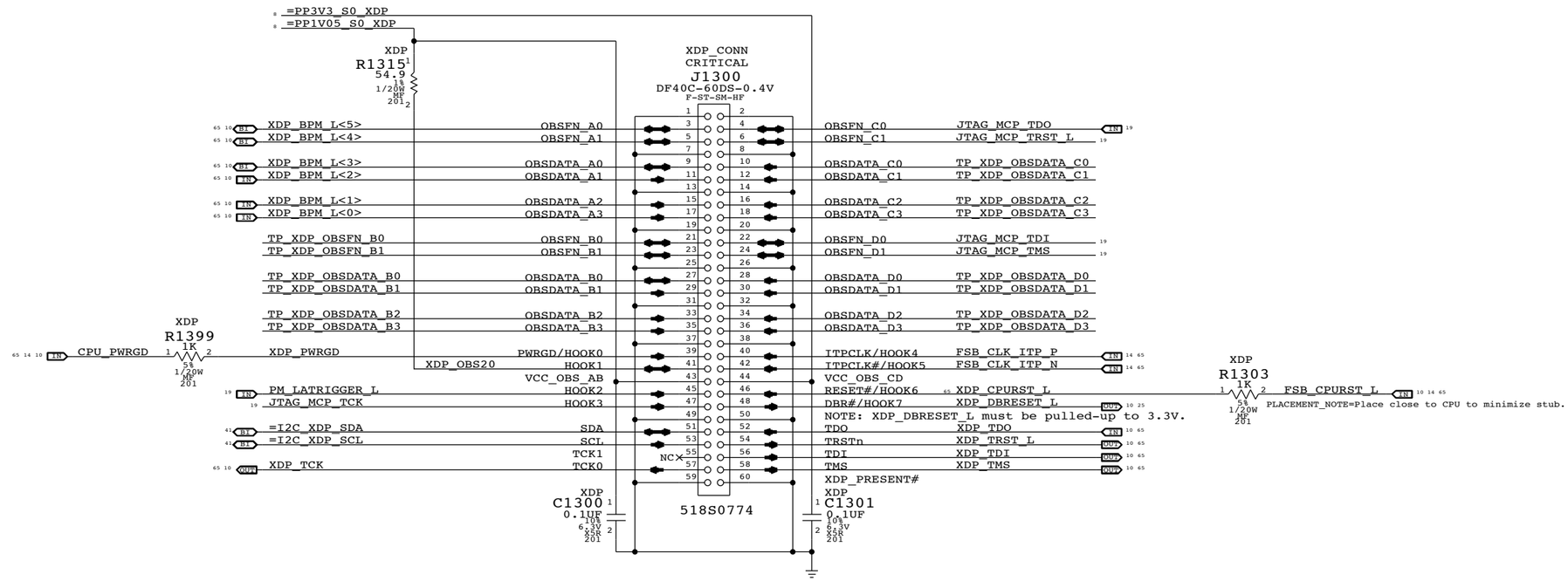
Micro2-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0782 Adapter Flex to support chipset debug.



Direction of XDP adapter flex

Please place J1300 within 1" of
board edge with odd-numbered pins
facing edge. Avoid any tall
components between J1300 and edge.

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE

eXtended Debug Port (Micro-XDP)

Apple Inc.

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OMIT_TABLE

U1400
MCP89U-A01
BGA
SYMBOL 1 OF 11

FSB

FSB_DSTB_L_P<0>	J38	CPU_DSTBP0*	CPU_D0*	M37	FSB_D_L<0>	
FSB_DSTB_L_N<0>	J39	CPU_DSTBN0*	CPU_D1*	M39	FSB_D_L<1>	
FSB_DINV_L<0>	F39	CPU_DBI0*	CPU_D2*	P39	FSB_D_L<2>	
			CPU_D3*	L38	FSB_D_L<3>	
FSB_DSTB_L_P<1>	R34	CPU_DSTBP1*	CPU_D4*	L39	FSB_D_L<4>	
FSB_DSTB_L_N<1>	R35	CPU_DSTBN1*	CPU_D5*	L40	FSB_D_L<5>	
FSB_DINV_L<1>	U36	CPU_DBI1*	CPU_D6*	M40	FSB_D_L<6>	
			CPU_D7*	P40	FSB_D_L<7>	
FSB_DSTB_L_P<2>	J37	CPU_DSTBP2*	CPU_D8*	H40	FSB_D_L<8>	
FSB_DSTB_L_N<2>	J36	CPU_DSTBN2*	CPU_D9*	L37	FSB_D_L<9>	
FSB_DINV_L<2>	L35	CPU_DBI2*	CPU_D10*	F38	FSB_D_L<10>	
			CPU_D11*	F40	FSB_D_L<11>	
FSB_DSTB_L_P<3>	C37	CPU_DSTBP3*	CPU_D12*	H38	FSB_D_L<12>	
FSB_DSTB_L_N<3>	C38	CPU_DSTBN3*	CPU_D13*	M38	FSB_D_L<13>	
FSB_DINV_L<3>	B35	CPU_DBI3*	CPU_D14*	H39	FSB_D_L<14>	
			CPU_D15*	J40	FSB_D_L<15>	
FSB_A_L<3>	U38	CPU_A3*	CPU_D16*	U35	FSB_D_L<16>	
FSB_A_L<4>	V37	CPU_A4*	CPU_D17*	R36	FSB_D_L<17>	
FSB_A_L<5>	Y36	CPU_A5*	CPU_D18*	R37	FSB_D_L<18>	
FSB_A_L<6>	V40	CPU_A6*	CPU_D19*	P35	FSB_D_L<19>	
FSB_A_L<7>	Y39	CPU_A7*	CPU_D20*	R38	FSB_D_L<20>	
FSB_A_L<8>	Y40	CPU_A8*	CPU_D21*	R33	FSB_D_L<21>	
FSB_A_L<9>	V39	CPU_A9*	CPU_D22*	U34	FSB_D_L<22>	
FSB_A_L<10>	AA39	CPU_A10*	CPU_D23*	R40	FSB_D_L<23>	
FSB_A_L<11>	AA36	CPU_A11*	CPU_D24*	P34	FSB_D_L<24>	
FSB_A_L<12>	AA37	CPU_A12*	CPU_D25*	P37	FSB_D_L<25>	
FSB_A_L<13>	Y38	CPU_A13*	CPU_D26*	P38	FSB_D_L<26>	
FSB_A_L<14>	AC36	CPU_A14*	CPU_D27*	P36	FSB_D_L<27>	
FSB_A_L<15>	AA40	CPU_A15*	CPU_D28*	P33	FSB_D_L<28>	
FSB_A_L<16>	AA38	CPU_A16*	CPU_D29*	P32	FSB_D_L<29>	
FSB_A_L<17>	AF39	CPU_A17*	CPU_D30*	R32	FSB_D_L<30>	
FSB_A_L<18>	AD38	CPU_A18*	CPU_D31*	R39	FSB_D_L<31>	
FSB_A_L<19>	AC38	CPU_A19*	CPU_D32*	H36	FSB_D_L<32>	
FSB_A_L<20>	AJ38	CPU_A20*	CPU_D33*	F36	FSB_D_L<33>	
FSB_A_L<21>	AD37	CPU_A21*	CPU_D34*	L33	FSB_D_L<34>	
FSB_A_L<22>	AJ39	CPU_A22*	CPU_D35*	M35	FSB_D_L<35>	
FSB_A_L<23>	AC40	CPU_A23*	CPU_D36*	L34	FSB_D_L<36>	
FSB_A_L<24>	AC37	CPU_A24*	CPU_D37*	M33	FSB_D_L<37>	
FSB_A_L<25>	AD40	CPU_A25*	CPU_D38*	M36	FSB_D_L<38>	
FSB_A_L<26>	AC39	CPU_A26*	CPU_D39*	M32	FSB_D_L<39>	
FSB_A_L<27>	AF36	CPU_A27*	CPU_D40*	J34	FSB_D_L<40>	
FSB_A_L<28>	AF40	CPU_A28*	CPU_D41*	H35	FSB_D_L<41>	
FSB_A_L<29>	AG39	CPU_A29*	CPU_D42*	H34	FSB_D_L<42>	
FSB_A_L<30>	AD39	CPU_A30*	CPU_D43*	L36	FSB_D_L<43>	
FSB_A_L<31>	AD36	CPU_A31*	CPU_D44*	M34	FSB_D_L<44>	
FSB_A_L<32>	AF37	CPU_A32*	CPU_D45*	F37	FSB_D_L<45>	
FSB_A_L<33>	AJ40	CPU_A33*	CPU_D46*	H37	FSB_D_L<46>	
FSB_A_L<34>	AG40	CPU_A34*	CPU_D47*	J35	FSB_D_L<47>	
FSB_A_L<35>	AG38	CPU_A35*	CPU_D48*	D39	FSB_D_L<48>	
			CPU_D49*	E36	FSB_D_L<49>	
FSB_ADSTB_L<0>	Y37	CPU_ADSTB0*	CPU_D50*	D40	FSB_D_L<50>	
FSB_ADSTB_L<1>	AF38	CPU_ADSTB1*	CPU_D51*	E40	FSB_D_L<51>	
			CPU_D52*	C39	FSB_D_L<52>	
FSB_REQ_L<0>	U40	CPU_REQ0*	CPU_D53*	E38	FSB_D_L<53>	
FSB_REQ_L<1>	U39	CPU_REQ1*	CPU_D54*	A37	FSB_D_L<54>	
FSB_REQ_L<2>	V38	CPU_REQ2*	CPU_D55*	C36	FSB_D_L<55>	
FSB_REQ_L<3>	U37	CPU_REQ3*	CPU_D56*	B38	FSB_D_L<56>	
FSB_REQ_L<4>	V36	CPU_REQ4*	CPU_D57*	E37	FSB_D_L<57>	
			CPU_D58*	C35	FSB_D_L<58>	
FSB_ADS_L	AG33	CPU_ADS*	CPU_D59*	A35	FSB_D_L<59>	
FSB_BNR_L	AD35	CPU_BNR*	CPU_D60*	B37	FSB_D_L<60>	
FSB_BREQ0_L	AG34	CPU_BR0*	CPU_D61*	D36	FSB_D_L<61>	
FSB_DBSY_L	AF35	CPU_DBSY*	CPU_D62*	A36	FSB_D_L<62>	
FSB_DRDY_L	U32	CPU_DRDY*	CPU_D63*	D38	FSB_D_L<63>	
FSB_HIT_L	AD34	CPU_HIT*				
FSB_HITM_L	AD32	CPU_HITM*				
FSB_LOCK_L	AG37	CPU_LOCK*				
FSB_TRDY_L	AG32	CPU_TRDY*				
CPU_PECI_MCP	AG36	CPU_PECI				
CPU_PROCHOT_L	V32	CPU_PROCHOT*				
	V35	CPU_THERMTRIP*				
	AC33	CPU_FERR*				
	D35	CPU_BSEL2				
	E35	CPU_BSEL1				
	F35	CPU_BSEL0				
FSB_RS_L<0>	AF33	CPU_RS0*				
FSB_RS_L<1>	AD33	CPU_RS1*				
FSB_RS_L<2>	AF34	CPU_RS2*				
MCP_BCLK_VML_COMP_VDD	AK39	BCLK_VML_COMP_VDD				
MCP_BCLK_VML_COMP_GND	AK40	BCLK_VML_COMP_GND				
MCP_CPU_COMP_VCC	AK38	CPU_COMP_VCC				
MCP_CPU_COMP_GND	AK37	CPU_COMP_GND				

		CPU_BPRI*	AF32	FSB_BPRI_L	
		CPU_DEFER*	AG35	FSB_DEFER_L	
		BCLK_OUT_CPU_P	AJ37	FSB_CLK_CPU_P	
		BCLK_OUT_CPU_N	AJ36	FSB_CLK_CPU_N	
		BCLK_OUT_ITP_P	AK32	FSB_CLK_ITP_P	
		BCLK_OUT_ITP_N	AK33	FSB_CLK_ITP_N	
		BCLK_OUT_NB_P	AJ35	FSB_CLK_MCP_P	
		BCLK_OUT_NB_N	AJ34	FSB_CLK_MCP_N	
		BCLK_IN_N	AJ32		
		BCLK_IN_P	AJ33		
		CPU_A20M*	AA33	CPU_A20M_L	
		CPU_IGNNE*	V33	CPU_IGNNE_L	
		CPU_INIT*	Y33	CPU_INIT_L	
		CPU_INTR	Y35	CPU_INTR	
		CPU_NMI	AA35	CPU_NMI	
		CPU_SMI*	AC35	CPU_SMI_L	
		CPU_PWRGD	AA32	CPU_PWRGD	
		CPU_RESET*	AC34	FSB_CPURST_L	
		CPU_DPRSLPVR	D2	PM_DPRSLPVR	
		CPU_SLP*	V34	FSB_CPUSLP_L	
		CPU_DPSLP*	Y32	CPU_DPSLP_L	
		CPU_DPWR*	U33	FSB_DPWR_L	
		CPU_STPCLK*	Y34	CPU_STPCLK_L	
		CPU_DPRSTP*	AA34	CPU_DPRSTP_L	

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB

R1410 1 54.9 1% 1/20W MF 201 2
R1415 1 62 5% 1/20W MF 201 2
R1430 1 49.9 1% 1/20W MF 201 2
R1435 1 49.9 1% 1/20W MF 201 2
R1431 1 49.9 1% 1/20W MF 201 2
R1436 1 49.9 1% 1/20W MF 201 2

PM_THRMTRIP_L
CPU_FERR_L
=MCP_BSEL<2>
=MCP_BSEL<1>
=MCP_BSEL<0>

=PP1V05_S0_MCP_FSB
NO STUFF
R1440 1 150 5% 1/20W MF 201 2

SYNC_MASTER=K16_MLB	SYNC_DATE=07/07/2010
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OMIT_TABLE

U1400
MCP89U-A01
BGA
SYMBOL 2 OF 11

MEMORY PARTITION 0

MEM_A_DQ<63>	AN6	MDQ0_63	MDQS0_7_P	AR4	MEM_A_DQS_P<7>
MEM_A_DQ<62>	AN4	MDQ0_62	MDQS0_7_N	AR5	MEM_A_DQS_N<7>
MEM_A_DQ<61>	AT4	MDQ0_61	MDQS0_6_P	AT6	MEM_A_DQS_P<6>
MEM_A_DQ<60>	AU3	MDQ0_60	MDQS0_6_N	AU6	MEM_A_DQS_N<6>
MEM_A_DQ<59>	AM7	MDQ0_59	MDQS0_5_P	AN11	MEM_A_DQS_P<5>
MEM_A_DQ<58>	AN7	MDQ0_58	MDQS0_5_N	AM11	MEM_A_DQS_N<5>
MEM_A_DQ<57>	AT5	MDQ0_57	MDQS0_4_P	AT12	MEM_A_DQS_P<4>
MEM_A_DQ<56>	AT3	MDQ0_56	MDQS0_4_N	AR12	MEM_A_DQS_N<4>
MEM_A_DQ<55>	AU5	MDQ0_55	MDQS0_3_P	AR29	MEM_A_DQS_P<3>
MEM_A_DQ<54>	AV5	MDQ0_54	MDQS0_3_N	AP29	MEM_A_DQS_N<3>
MEM_A_DQ<53>	AR6	MDQ0_53	MDQS0_2_P	AR32	MEM_A_DQS_P<2>
MEM_A_DQ<52>	AN9	MDQ0_52	MDQS0_2_N	AP32	MEM_A_DQS_N<2>
MEM_A_DQ<51>	AV3	MDQ0_51	MDQS0_1_P	AV36	MEM_A_DQS_P<1>
MEM_A_DQ<50>	AV4	MDQ0_50	MDQS0_1_N	AU36	MEM_A_DQS_N<1>
MEM_A_DQ<49>	AM8	MDQ0_49	MDQS0_0_P	AN35	MEM_A_DQS_P<0>
MEM_A_DQ<48>	AN8	MDQ0_48	MDQS0_0_N	AN34	MEM_A_DQS_N<0>
MEM_A_DQ<47>	AP8	MDQ0_47			
MEM_A_DQ<46>	AP9	MDQ0_46			
MEM_A_DQ<45>	AN12	MDQ0_45			
MEM_A_DQ<44>	AT11	MDQ0_44	MRAS0*	AR17	MEM_A_RAS_L
MEM_A_DQ<43>	AT8	MDQ0_43	MCAS0*	AM17	MEM_A_CAS_L
MEM_A_DQ<42>	AR8	MDQ0_42	MWE0*	AM18	MEM_A_WE_L
MEM_A_DQ<41>	AT9	MDQ0_41			
MEM_A_DQ<40>	AM12	MDQ0_40	MBA0_2	AR26	MEM_A_BA<2>
MEM_A_DQ<39>	AP12	MDQ0_39	MBA0_1	AR18	MEM_A_BA<1>
MEM_A_DQ<38>	AN14	MDQ0_38	MBA0_0	AP17	MEM_A_BA<0>
MEM_A_DQ<37>	AT14	MDQ0_37			
MEM_A_DQ<36>	AR14	MDQ0_36	MA0_15	AN26	MEM_A_A<15>
MEM_A_DQ<35>	AR11	MDQ0_35	MA0_14	AP26	MEM_A_A<14>
MEM_A_DQ<34>	AP11	MDQ0_34	MA0_13	AR15	MEM_A_A<13>
MEM_A_DQ<33>	AM15	MDQ0_33	MA0_12	AR24	MEM_A_A<12>
MEM_A_DQ<32>	AN15	MDQ0_32	MA0_11	AP23	MEM_A_A<11>
MEM_A_DQ<31>	AR27	MDQ0_31	MA0_10	AP18	MEM_A_A<10>
MEM_A_DQ<30>	AT27	MDQ0_30	MA0_9	AP24	MEM_A_A<9>
MEM_A_DQ<29>	AM30	MDQ0_29	MA0_8	AN24	MEM_A_A<8>
MEM_A_DQ<28>	AN30	MDQ0_28	MA0_7	AR23	MEM_A_A<7>
MEM_A_DQ<27>	AN27	MDQ0_27	MA0_6	AM23	MEM_A_A<6>
MEM_A_DQ<26>	AP27	MDQ0_26	MA0_5	AM24	MEM_A_A<5>
MEM_A_DQ<25>	AN29	MDQ0_25	MA0_4	AN23	MEM_A_A<4>
MEM_A_DQ<24>	AM29	MDQ0_24	MA0_3	AR21	MEM_A_A<3>
MEM_A_DQ<23>	AT30	MDQ0_23	MA0_2	AP20	MEM_A_A<2>
MEM_A_DQ<22>	AT32	MDQ0_22	MA0_1	AP21	MEM_A_A<1>
MEM_A_DQ<21>	AP33	MDQ0_21	MA0_0	AR20	MEM_A_A<0>
MEM_A_DQ<20>	AR33	MDQ0_20		=PP1V05_S0_MCP_M2CLK_DLL	
MEM_A_DQ<19>	AP30	MDQ0_19	+VIO_M2CLK_DLL	AJ30	550 mA
MEM_A_DQ<18>	AR30	MDQ0_18	+VIO_M2CLK_DLL	AK30	
MEM_A_DQ<17>	AM33	MDQ0_17	+VIO_M2CLK_DLL	AK31	
MEM_A_DQ<16>	AN33	MDQ0_16		PP1V05_S0_MCP_PLL_FSBMEM	
MEM_A_DQ<15>	AU35	MDQ0_15	+VIO_PLL_MEM	AH29	20 mA 70 mA
MEM_A_DQ<14>	AV35	MDQ0_14	+VIO_PLL_MEM	AH30	
MEM_A_DQ<13>	AT37	MDQ0_13	+VIO_PLL_MEM	AJ31	25 mA
MEM_A_DQ<12>	AT38	MDQ0_12	+VIO_PLL_FSB	AF29	
MEM_A_DQ<11>	AT33	MDQ0_11	+VIO_PLL_FSB	AF30	
MEM_A_DQ<10>	AT35	MDQ0_10	+VIO_PLL_FSB	AF31	25 mA
MEM_A_DQ<9>	AV37	MDQ0_9			
MEM_A_DQ<8>	AU38	MDQ0_8	+VIO_PLL_CPU	AG29	
MEM_A_DQ<7>	AR35	MDQ0_7	+VIO_PLL_CPU	AG30	
MEM_A_DQ<6>	AN36	MDQ0_6	+VIO_PLL_CPU	AG31	
MEM_A_DQ<5>	AM35	MDQ0_5			
MEM_A_DQ<4>	AM34	MDQ0_4	MCLK0A_1_P	AM21	MEM_A_CLK_P<1>
MEM_A_DQ<3>	AR36	MDQ0_3	MCLK0A_1_N	AN21	MEM_A_CLK_N<1>
MEM_A_DQ<2>	AR37	MDQ0_2			
MEM_A_DQ<1>	AM36	MDQ0_1	MCLK0A_0_P	AM20	MEM_A_CLK_P<0>
MEM_A_DQ<0>	AM37	MDQ0_0	MCLK0A_0_N	AN20	MEM_A_CLK_N<0>
MEM_A_DM<7>	AN5	MDQM0_7	MCS0A_1*	AP15	MEM_A_CS_L<1>
MEM_A_DM<6>	AM9	MDQM0_6	MCS0A_0*	AN18	MEM_A_CS_L<0>
MEM_A_DM<5>	AR9	MDQM0_5			
MEM_A_DM<4>	AM14	MDQM0_4	MODT0A_1	AP14	MEM_A_ODT<1>
MEM_A_DM<3>	AT29	MDQM0_3	MODT0A_0	AN17	MEM_A_ODT<0>
MEM_A_DM<2>	AN32	MDQM0_2			
MEM_A_DM<1>	AT36	MDQM0_1	MCKE0A_1	AM27	MEM_A_CKE<1>
MEM_A_DM<0>	AN37	MDQM0_0	MCKE0A_0	AM26	MEM_A_CKE<0>

OMIT_TABLE

U1400
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MEMORY PARTITION 1

MEM_B_DQ<63>	AM1	MDQ1_63	MDQS1_7_P	AN2	MEM_B_DQS_P<7>
MEM_B_DQ<62>	AN1	MDQ1_62	MDQS1_7_N	AN3	MEM_B_DQS_N<7>
MEM_B_DQ<61>	AT1	MDQ1_61	MDQS1_6_P	AY5	MEM_B_DQS_P<6>
MEM_B_DQ<60>	AU1	MDQ1_60	MDQS1_6_N	AY4	MEM_B_DQS_N<6>
MEM_B_DQ<59>	AM3	MDQ1_59	MDQS1_5_P	AV11	MEM_B_DQS_P<5>
MEM_B_DQ<58>	AM2	MDQ1_58	MDQS1_5_N	AW11	MEM_B_DQS_N<5>
MEM_B_DQ<57>	AR2	MDQ1_57	MDQS1_4_P	AV14	MEM_B_DQS_P<4>
MEM_B_DQ<56>	AR1	MDQ1_56	MDQS1_4_N	AW14	MEM_B_DQS_N<4>
MEM_B_DQ<55>	AW3	MDQ1_55	MDQS1_3_P	AW27	MEM_B_DQS_P<3>
MEM_B_DQ<54>	AW4	MDQ1_54	MDQS1_3_N	AY27	MEM_B_DQS_N<3>
MEM_B_DQ<53>	AU8	MDQ1_53	MDQS1_2_P	AV32	MEM_B_DQS_P<2>
MEM_B_DQ<52>	AV8	MDQ1_52	MDQS1_2_N	AW32	MEM_B_DQS_N<2>
MEM_B_DQ<51>	AU2	MDQ1_51	MDQS1_1_P	AY37	MEM_B_DQS_P<1>
MEM_B_DQ<50>	AV2	MDQ1_50	MDQS1_1_N	AY36	MEM_B_DQS_N<1>
MEM_B_DQ<49>	AW6	MDQ1_49	MDQS1_0_P	AN38	MEM_B_DQS_P<0>
MEM_B_DQ<48>	AV6	MDQ1_48	MDQS1_0_N	AN39	MEM_B_DQS_N<0>
MEM_B_DQ<47>	AY9	MDQ1_47			
MEM_B_DQ<46>	AW9	MDQ1_46			
MEM_B_DQ<45>	AY11	MDQ1_45	MRAS1*	AW18	MEM_B_RAS_L
MEM_B_DQ<44>	AY12	MDQ1_44	MCAS1*	AV17	MEM_B_CAS_L
MEM_B_DQ<43>	AW8	MDQ1_43	MWE1*	AY18	MEM_B_WE_L
MEM_B_DQ<42>	AY8	MDQ1_42			
MEM_B_DQ<41>	AU9	MDQ1_41	MBA1_2	AW24	MEM_B_BA<2>
MEM_B_DQ<40>	AU11	MDQ1_40	MBA1_1	AT18	MEM_B_BA<1>
MEM_B_DQ<39>	AU12	MDQ1_39	MBA1_0	AV18	MEM_B_BA<0>
MEM_B_DQ<38>	AU14	MDQ1_38			
MEM_B_DQ<37>	AV15	MDQ1_37	MA1_15	AU24	MEM_B_A<15>
MEM_B_DQ<36>	AU15	MDQ1_36	MA1_14	AV24	MEM_B_A<14>
MEM_B_DQ<35>	AW12	MDQ1_35	MA1_13	AU17	MEM_B_A<13>
MEM_B_DQ<34>	AV12	MDQ1_34	MA1_12	AY24	MEM_B_A<12>
MEM_B_DQ<33>	AY15	MDQ1_33	MA1_11	AW23	MEM_B_A<11>
MEM_B_DQ<32>	AW15	MDQ1_32	MA1_10	AU18	MEM_B_A<10>
MEM_B_DQ<31>	AW26	MDQ1_31	MA1_9	AY23	MEM_B_A<9>
MEM_B_DQ<30>	AY26	MDQ1_30	MA1_8	AU23	MEM_B_A<8>
MEM_B_DQ<29>	AV29	MDQ1_29	MA1_7	AV23	MEM_B_A<7>
MEM_B_DQ<28>	AW29	MDQ1_28	MA1_6	AT21	MEM_B_A<6>
MEM_B_DQ<27>	AU26	MDQ1_27	MA1_5	AT23	MEM_B_A<5>
MEM_B_DQ<26>	AV26	MDQ1_26	MA1_4	AU21	MEM_B_A<4>
MEM_B_DQ<25>	AU27	MDQ1_25	MA1_3	AV21	MEM_B_A<3>
MEM_B_DQ<24>	AU29	MDQ1_24	MA1_2	AY21	MEM_B_A<2>
MEM_B_DQ<23>	AW30	MDQ1_23	MA1_1	AW21	MEM_B_A<1>
MEM_B_DQ<22>	AV30	MDQ1_22	MA1_0	AY20	MEM_B_A<0>
MEM_B_DQ<21>	AY33	MDQ1_21			
MEM_B_DQ<20>	AW33	MDQ1_20			
MEM_B_DQ<19>	AY29	MDQ1_19			
MEM_B_DQ<18>	AY30	MDQ1_18			
MEM_B_DQ<17>	AU32	MDQ1_17			
MEM_B_DQ<16>	AY32	MDQ1_16			
MEM_B_DQ<15>	AW35	MDQ1_15			
MEM_B_DQ<14>	AY35	MDQ1_14			
MEM_B_DQ<13>	AV39	MDQ1_13			
MEM_B_DQ<12>	AU39	MDQ1_12			
MEM_B_DQ<11>	AV33	MDQ1_11			
MEM_B_DQ<10>	AU33	MDQ1_10			
MEM_B_DQ<9>	AW38	MDQ1_9			
MEM_B_DQ<8>	AV38	MDQ1_8			
MEM_B_DQ<7>	AR40	MDQ1_7			
MEM_B_DQ<6>	AR39	MDQ1_6			
MEM_B_DQ<5>	AM39	MDQ1_5			
MEM_B_DQ<4>	AM38	MDQ1_4			
MEM_B_DQ<3>	AT40	MDQ1_3			
MEM_B_DQ<2>	AU40	MDQ1_2			
MEM_B_DQ<1>	AN40	MDQ1_1			
MEM_B_DQ<0>	AM40	MDQ1_0			
MEM_B_DM<7>	AR3	MDQM1_7			
MEM_B_DM<6>	AY6	MDQM1_6			
MEM_B_DM<5>	AV9	MDQM1_5			
MEM_B_DM<4>	AY14	MDQM1_4			
MEM_B_DM<3>	AV27	MDQM1_3			
MEM_B_DM<2>	AU30	MDQM1_2			
MEM_B_DM<1>	AW37	MDQM1_1			
MEM_B_DM<0>	AR38	MDQM1_0			
MEM_COMP_GND	AL23				
MEM_COMP_VDD	AL24				

=PP1V5R1V35_SW_MCP_MEM

R1510 1
40.2
1%
1/20W
MF
201 2

R1511 1
40.2
1%
1/20W
MF
201 2

MCP_MEM_COMP_GND
MCP_MEM_COMP_VDD

=PP1V5R1V35_S3_MCP_MEM

R1520 1
1K
5%
1/20W
MF
201 2

MRESET0*	AM6	MEM_RESET_L
MCLK1A_1_P	AV20	MEM_B_CLK_P<1>
MCLK1A_1_N	AW20	MEM_B_CLK_N<1>
MCLK1A_0_P	AT20	MEM_B_CLK_P<0>
MCLK1A_0_N	AU20	MEM_B_CLK_N<0>
MCS1A_1*	AT15	MEM_B_CS_L<1>
MCS1A_0*	AY17	MEM_B_CS_L<0>
MODT1A_1	AT17	MEM_B_ODT<1>
MODT1A_0	AW17	MEM_B_ODT<0>
MCKE1A_1	AT24	MEM_B_CKE<1>
MCKE1A_0	AT26	MEM_B_CKE<0>

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
MCP Memory Interface

Apple Inc.

DRAWING NUMBER 051-8379
SIZE D
REVISION 4.4.0
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MCP89U-A01
BGA
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PCI EXPRESS

9	IN	PEG_CLKREQ_L	V1	PEA_CLKREQ*/GIO_49	PE0_REFCLK_P	V5	PEG_CLK100M_P
					PE0_REFCLK_N	V4	PEG_CLK100M_N
34	IN	AP_CLKREQ_L	U1	PEB_CLKREQ*/GIO_50	PE1_REFCLK_P	V2	PCIE_CLK100M_AP_P
					PE1_REFCLK_N	V3	PCIE_CLK100M_AP_N
9	IN	ENET_CLKREQ_L	U4	PEC_CLKREQ*/GIO_51	PE2_REFCLK_P	U3	TP_PCIE_CLK100M_PE2P
					PE2_REFCLK_N	U2	TP_PCIE_CLK100M_PE2N
34 7	IN	PCIE_WAKE_L	U7	PE_WAKE*			
9	IN	=PEG_D2R_P<4>	Y4	PE0_RX4_P	PE0_TX4_P	Y3	=PEG_R2D_C_P<4>
9	IN	=PEG_D2R_N<4>	Y5	PE0_RX4_N	PE0_TX4_N	Y2	=PEG_R2D_C_N<4>
9	IN	=PEG_D2R_P<5>	AA9	PE0_RX5_P	PE0_TX5_P	AA7	=PEG_R2D_C_P<5>
9	IN	=PEG_D2R_N<5>	AA8	PE0_RX5_N	PE0_TX5_N	AA6	=PEG_R2D_C_N<5>
67 34 7	IN	PCIE_AP_D2R_P	AA4	PE1_RX0_P	PE1_TX0_P	AA2	PCIE_AP_R2D_C_P
67 34 7	IN	PCIE_AP_D2R_N	AA5	PE1_RX0_N	PE1_TX0_N	AA3	PCIE_AP_R2D_C_N
		TP_PCIE_PE1_D2RP	Y7	PE1_RX1_P	PE1_TX1_P	Y8	TP_PCIE_PE4_R2D_CP
		TP_PCIE_PE1_D2RN	Y6	PE1_RX1_N	PE1_TX1_N	Y9	TP_PCIE_PE4_R2D_CN
23		PP3V3_S0_MCP_PLL_HVDD	W10	+3.3V_PLL_HVDD			
23		PP1V05_S0_MCP_PLL_PEXSATA	AG10	+VIO_PLL_PE	PEX_RST*	U6	PCIE_RESET_L
			AG11	+VIO_PLL_PE			
			AG12	+VIO_PLL_PE			
			AH10	+VIO_PLL_XREF_XS			
			AH11	+VIO_PLL_XREF_XS			
			AH12	+VIO_PLL_XREF_XS			
			AE10	+VIO_PLL_SATA			
			AE11	+VIO_PLL_SATA			
			AF12	+VIO_PLL_SATA			
			AF10	+VIO_PLL_H			
			AF11	+VIO_PLL_H	PEX0_TERM_P	U5	MCP_PEX0_TERMP

PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1
PE1 ports are Gen1-only. 2 RCs: x1, x1

If PE0[3:0] are not used,
+VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

If PE0[4:5] and PE1[0:1] are not used,
+VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND

R1600
22K
5%
1/20W
MF
201

R1610
2.49K
1%
1/20W
MF
201

PLACE_NEAR=U1400.U5:12.7 mm

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE
MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D
REVISION 4.4.0
BRANCH
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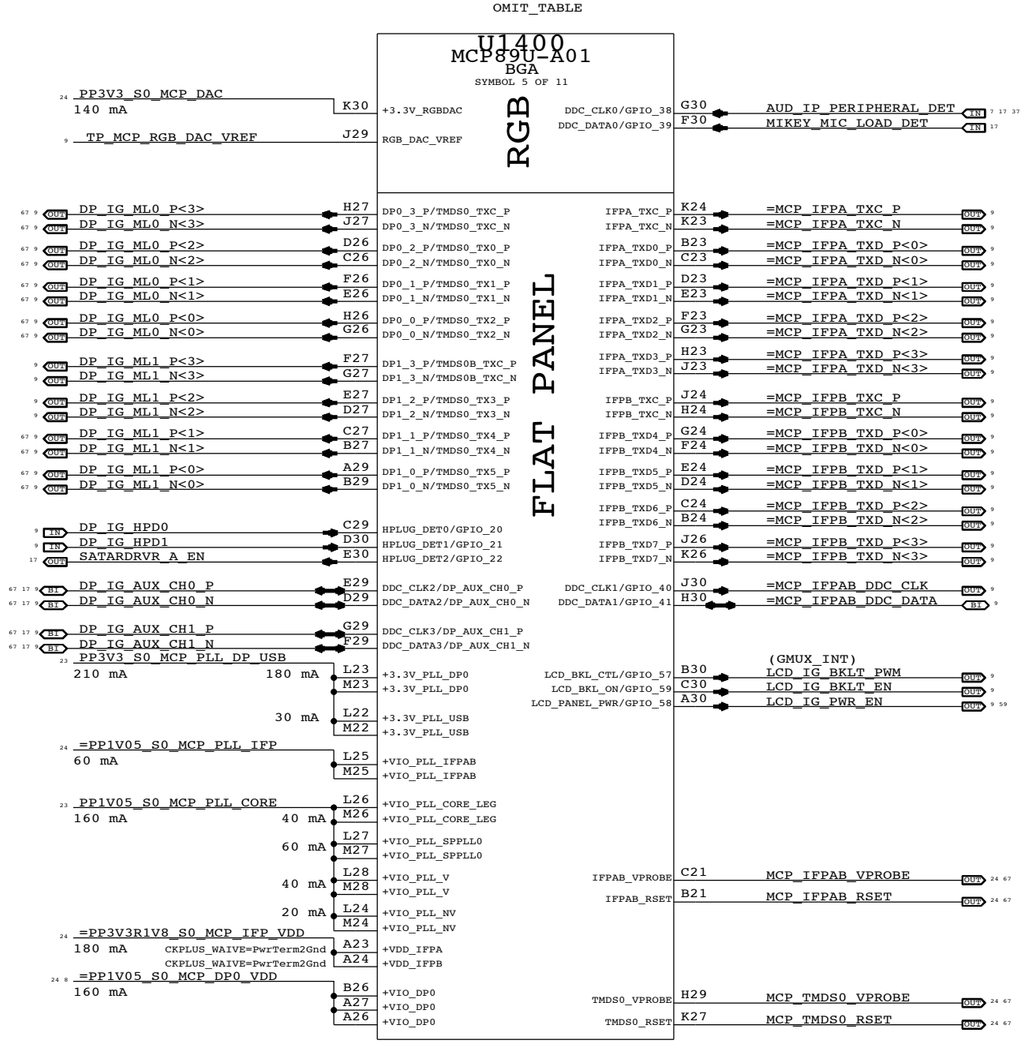


NOTE: 100K pull-downs required if HPLUG_DET0/HPLUG_DET1 are not used.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
Connect +3.3V_RGBDAC pin to GND.

NOTE: No Composite/S-Video/Component Video support on MCP89

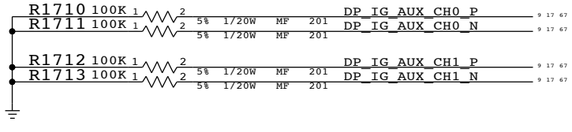
Interface Mode

MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPAB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPAB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

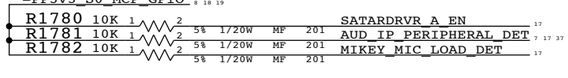
LVDS: Power +VDD_IFPx at 1.8V
TMDS: Power +VDD_IFPx at 3.3V

DDC Mode Pull-downs

NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.



GPIO Pull-Ups



Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: MCP Graphics

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D
REVISION: 4.4.0
BRANCH:
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SATA

USB

LAN

Only USB811 support nV USB JTAG in S3/S4/S5.

Internal 19.5K Pull-Downs on all USB pairs

OHCI0/EHCI0

OHCI1/EHCI1

67 35 OUT SATA_HDD_R2D_C_P	AF1	SATA_A0_TX_P	
67 35 OUT SATA_HDD_R2D_C_N	AG1	SATA_A0_TX_N	
67 35 IN SATA_HDD_D2R_N	AG3	SATA_A0_RX_N	
67 35 IN SATA_HDD_D2R_P	AG2	SATA_A0_RX_P	
67 9 OUT SATA_ODD_R2D_C_P	AF2	SATA_A1_TX_P	
67 9 OUT SATA_ODD_R2D_C_N	AF3	SATA_A1_TX_N	
67 9 IN SATA_ODD_D2R_N	AF5	SATA_A1_RX_N	
67 9 IN SATA_ODD_D2R_P	AF4	SATA_A1_RX_P	
MXM_GOOD_L	AG5	SATA_LED*/GPIO_30	
67 MCP_SATA_TERMP	AG4	SATA_TERMP	
	G5, V6, AM4, H15, AK36	NC	
69 9 IN ENET_RXD<0>	C15	RGMII_RXD0	
69 9 IN ENET_RXD<1>	H17	RGMII_RXD1	
69 9 IN ENET_RXD<2>	C17	RGMII_RXD2	
69 9 IN ENET_RXD<3>	G15	RGMII_RXD3	
69 9 IN ENET_CLK125M_RXCLK	D17	RGMII_RXCLK	
69 9 IN ENET_RX_CTRL	A15	RGMII_RXCTL	
9 IN ENET_ENERGY_DET	E17	RGMII_INTR/GPIO_35	
23 PP3V3_ENET_MCP_PLL_MAC 20 mA	J18	+3.3V_PLL_MAC_DUAL	
69 MCP_MII_COMP_VDD	K15	RGMII_COMP_VDD	
69 MCP_MII_COMP_GND	K14	RGMII_COMP_GND	
USB0_P	E21	USB_EXTA_P	External A
USB0_N	D21	USB_EXTA_N	
USB1_P	F21	USB_MINI_P	AirPort (PCIe Mini-Card)
USB1_N	G21	USB_MINI_N	
USB2_P	E20	USB_TPAD_P	Geyser Trackpad/Keyboard
USB2_N	D20	USB_TPAD_N	
USB3_P	L21	USB_EXTC_P	External C
USB3_N	K21	USB_EXTC_N	
USB4_P	A20	USB_BT_P	Bluetooth
USB4_N	A21	USB_BT_N	
USB5_P	H21	USB_CAMERA_P	Camera/External E
USB5_N	J21	USB_CAMERA_N	
USB6_P	G20	USB_SDCARD_P	SD Card/ExpressCard
USB6_N	F20	USB_SDCARD_N	
USB7_P	H20	USB_EXTD_P	EXTERNAL D
USB7_N	J20	USB_EXTD_N	
USB_OC0*/GPIO_25	H14	USB_EXTA_OC_L	
USB_OC1*/GPIO_26	G12	USB_EXTD_OC_L	
USB_RBIAS_GND	L19	68 MCP_USB_RBIAS_GND	
RGMII_VREF	B15	MCP_RGMII_VREF	IN 9
RGMII_TXD0	F15	TP_ENET_TXD<0>	
RGMII_TXD1	F17	TP_ENET_TXD<1>	
RGMII_TXD2	J17	TP_ENET_TXD<2>	
RGMII_TXD3	D15	TP_ENET_TXD<3>	
RGMII_TXCLK	G14	TP_ENET_CLK125M_TXCLK	
RGMII_TXCTL	C14	TP_ENET_TX_CTRL	
RGMII_MDC	E15	TP_ENET_MDC	
RGMII_MDIO	H18	ENET_MDIO	BI 9 69
BUF_25MHZ	J14	TP_MCP_CLK25M_BUF0_R	
RGMII_RESET*	G17	TP_ENET_RESET_L	

23 20 8 =PP3V3_ENET_MCP_RMGT

19 17 8 =PP3V3_S0_MCP_GPIO

R1800[1] 100K 5% 1/20W MF 201 [2]

R1805[1] 2.49K 1% 1/20W MF 201 [2]

R1810[1] 49.9 1% 1/20W MF 201 [2]

R1811[1] 49.9 1% 1/20W MF 201 [2]

=PP3V3_S5_MCP_GPIO 8 19

R1851[1] 8.2K 5% 1/20W MF 201 [2]

R1850[1] 8.2K 5% 1/20W MF 201 [2]

R1860[1] 887 1% 1/20W MF 201 [2]

USB_EXTA_OC_L 36

USB_EXTD_OC_L 7 37

Internal MAC Disable:

Connect RGMII_RXD<0:3> together to 10K pull-down.
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXCTL to 10K pull-down.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
RGMII_COMP_VDD/_GND must remain connected as shown.
Connect RGMII_VREF to 10K pull-down.
Connect RGMII_MDIO to 10K pull-down.
All other pins can be left TP or NC.

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE: MCP SATA, USB & Ethernet

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

BRANCH:

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OMIT_TABLE

U1400
MCP89U-A01
BGA
SYMBOL 7 OF 11

=PP3V3R1V5_S0_MCP_HDA
70 mA

R1900 49.9 1% 1/20W MF 201

J12 +VDD_HDA
70 mA

HDA

HDA_SDIN0	C3	HDA_SDATA_IN0 (IPD)	HDA_SDATA_OUT B3
MCP_HDA_PULLDN_COMP	A5	HDA_PULLDN_COMP (IPD)	HDA_BITCLK B4
			HDA_RESET* C4
			HDA_SYNC A4

=PP3V3_S0_MCP_GPIO

R1961 10K 5% 1/20W MF 201

HDA_SDOUT_R	R1950 22 5% 1/20W MF 201	HDA_SDOUT
HDA_BIT_CLK_R	R1951 22 5% 1/20W MF 201	HDA_BIT_CLK
HDA_RST_R_L	R1952 22 5% 1/20W MF 201	HDA_RST_L
HDA_SYNC_R	R1953 22 5% 1/20W MF 201	HDA_SYNC

LPC

LPC_AD<0>	R1910 22 5% 1/20W MF 201	LPC_AD_R<0>	H1 LPC_AD0 (IPU)
LPC_AD<1>	R1911 22 5% 1/20W MF 201	LPC_AD_R<1>	H2 LPC_AD1 (IPU)
LPC_AD<2>	R1912 22 5% 1/20W MF 201	LPC_AD_R<2>	H3 LPC_AD2 (IPU)
LPC_AD<3>	R1913 22 5% 1/20W MF 201	LPC_AD_R<3>	H4 LPC_AD3 (IPU)
MLB_RAM_CFG1			F2 LPC_DRQ0*/GPIO_43 (IPU)
PM_CLKRUN_L			F1 LPC_CLKRUN*/GPIO_42 (IPU)
			LPC_SERIRQ (IPU) H5
			LPC_FRAME* F3
			(IPD) LPC_RESET* F5
			LPC_CLK0 F4

LPC_SERIRQ		LPC_SERIRQ
LPC_FRAME_R_L	R1960 22 5% 1/20W MF 201	LPC_FRAME_L
		LPC_RESET_L
		LPC_CLK33M_SMC_R

PP3V3_G3_RTC

R1920 49.9K 1% 1/20W MF 201
R1921 49.9K 1% 1/20W MF 201

RTC_RST_L → D18 RTC_RST*

MISC

SMC_WAKE_SCI_L	D14	SIO_PME*/GPIO_31	MISC_VDDEN0/GPIO_47 A11
PM_LATRIGGER_L	J11	EXT_SMI*/GPIO_32	MISC_VDDEN1/GPIO_48 F14
AUD_I2C_INT_L	F6	A20GATE/GPIO_55	MISC_VDDEN2/GPIO_17 E11
SMC_RUNTIME_SCI_L	D3	KBRDRSTIN*/GPIO_56 (IPU-S5)	MISC_VDDEN3/GPIO_18 F11
			MISC_VDDEN4/GPIO_19 G11
			MEM_VDD_SEL/GPIO_46 D11
PM_PWRBTN_L	H12	PWRBTN* (IPU-S5)	FANCTL0/GPIO_61 D8
PM_SYSRST_DEBOUNCE_L	F12	RSTBTN* (IPU-S5)	FANRPM0/GPIO_60/MGPIO_2 E8
			FANCTL1/GPIO_62 F8
			FANRPM1/GPIO_63/MGPIO_3 G7
PM_RSMRST_L	F18	PWRGD_SB	(IPD) SLP_S3* A8
MCP_PS_PWRGD	E9	PWRGD	(IPD) SLP_RMGT* C9
			(IPD) SLP_S5* B8
MCP_WAKE_REQ_L	E18	MCP_WAKE_REQ*	MCP_VID0/GPIO_13 E3
PM_BATLOW_L	A9	MCP_WAKE_DIS* (IPU-S5)	MCP_VID1/GPIO_14 E4
MCP_MEM_VDD_EN	B11	MCP_MEMVDD_EN/GPIO_44	MCP_VID2/GPIO_15 E5
MCP_MEM_VTT_EN	C11	MEMVTT_EN/GPIO_45	MCP_VID3/GPIO_16 D6
SM_INTRUDER_L	G18	INTRUDER*	SPI_CS0*/GPIO_10 H10
			SPI_CLK/GPIO_11 G8
			SPI_DI/GPIO_08 B9
			SPI_DO/GPIO_09 E14
SMC_IG_THROTTLE_L	D5	MGPU_PIO0/GPIO_6	SPKR/GPIO_1 E1
AUD_IPHS_SWITCH_EN	E6	MGPU_PIO1/GPIO_7	THERM_DIODE_P C2
GFXVCORE_PWR_EN	F9	MGPU_PIO2/GPIO_23	THERM_DIODE_N D1
SPIROM_USE_MLB	G9	MGPU_PIO3/GPIO_24	SMB_CLK0 C5
			SMB_DATA0 C8
JTAG_MCP_TDI	D12	JTAG_TDI (IPU)	SMB_CLK1/MSMB_CLK B6
JTAG_MCP_TDO	C12	JTAG_TDO	SMB_DATA1/MSMB_DATA C6
JTAG_MCP_TMS	B12	JTAG_TMS (IPU)	SMB_ALERT*/GPIO_64 D9
JTAG_MCP_TRST_L	E12	JTAG_TRST* (IPD)	SUS_CLK/GPIO_34 H9
JTAG_MCP_TCK	A12	JTAG_TCK	TEST_MODE_EN A6
			PKG_TEST B20
MCP_CLK25M_XTALIN	A14	XTALIN	PKG_TEST2 C20
MCP_CLK25M_XTALOUT	B14	XTALOUT	
RTC_CLK32K_XTALIN	B18	XTALIN_RTC	
RTC_CLK32K_XTALOUT	C18	XTALOUT_RTC	

MCP_CPU_VTT_EN_L		
MLB_RAM_CFG0		
MLB_RAM_CFG2		
SMC_ADAPTER_EN		
LPCPLUS_GPIO		
MCP_MEM_VDD_SEL_1V5		
MLB_RAM_CFG3		
MEM_EVENT_L		
ENET_LOW_PWR		
SDCARD_RESET		
PM_SLP_S3_L		
PM_SLP_RMGT_L		
PM_SLP_S4_L		
MCP_VID<0>		
MCP_VID<1>		
MCP_VID<2>		
MCP_VID<3>		
SPI_CS0_R_L		
SPI_CLK_R		
SPI_MISO		
SPI_MOSI_R		
MCP_SPKR		
MCP_THMDIODE_P		
MCP_THMDIODE_N		
SMBUS_MCP_0_CLK		
SMBUS_MCP_0_DATA		
SMBUS_MCP_1_CLK		
SMBUS_MCP_1_DATA		
AP_PWR_EN		
PM_CLK32K_SUSCLK_R		
MCP_TEST_MODE_EN		

NOTE: MCP SLP_S5# pin has the behavior of Intel's SLP_S4# signal.

R1970 10K 1% 1/20W MF 201 — MCP_SPKR:
0 = USER mode (Normal boot mode)
1 = SAFE mode (For ROMSIP recovery)
Connects to SMC for automatic recovery.

R1959 10K 5% 1/20W MF 201
R1966 10K 5% 1/20W MF 201 — NO STUFF
R1975 1K 1% 1/20W MF 201

R1930 10K 5% 1/20W MF 201
R1931 100K 5% 1/20W MF 201

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select

I/F	LPC_FRAME#
LPC	0
SPI	1

NOTE: MCP89 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command. Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface

HDA_SDOUT_R
HDA_BIT_CLK_R
HDA_RST_R_L
HDA_SYNC_R

C1950 10PF 5% 25V NPO 201
C1952 10PF 5% 25V NPO 201
C1951 10PF 5% 25V NPO 201
C1953 10PF 5% 25V NPO 201

GPIO Pull-Ups/Downs

=PP3V3_S5_MCP_GPIO
=PP3V3_S3_MCP_GPIO
=PP3V3_S0_MCP_GPIO

R1991 10K	SMC_IG_THROTTLE_L	
R1981 10K	AUD_IPHS_SWITCH_EN	
R1999 100K	GFXVCORE_PWR_EN	
R1986 100K	SPIROM_USE_MLB	
R1983 10K	MCP_CPU_VTT_EN_L	
R1987 100K	LPCPLUS_GPIO	
R1989 10K	MEM_EVENT_L	
R1990 10K	ENET_LOW_PWR	
R1980 10K	SDCARD_RESET	
R1992 100K	MCP_VID<0>	
R1993 100K	MCP_VID<1>	
R1994 100K	MCP_VID<2>	
R1995 100K	MCP_VID<3>	
R1998 20K	SPI_MISO	
R1996 10K	AP_PWR_EN	

All: 5% 1/20W MF 201

Platform-Specific Connections

R1965 33 5% 1/20W MF 201

LPC_RESET_L → LPC_PWRDWN_L
PM_SLP_S4_L → PM_SLP_S5_L (MAKE_BASE=TRUE)

NOTE: MCP SLP_S5# signal has the behavior of Intel's SLP_S4# signal

=PP3V3_S3_MCP_GPIO

DRAM_CFG3:H	R1976 10K	MLB_RAM_CFG3
DRAM_CFG2:H	R1978 10K	MLB_RAM_CFG2
		MLB_RAM_CFG1
DRAM_CFG0:H	R1957 10K	MLB_RAM_CFG0
DRAM_CFG3:L	R1977 10K	
DRAM_CFG2:L	R1979 10K	
DRAM_CFG1:L	R1956 470	
DRAM_CFG0:L	R1958 10K	

GPIO43 has internal ~9K pull-up.

All: 5% 1/20W MF 201

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: MCP HDA, LPC & MISC

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D
REVISION 4.4.0
BRANCH
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NOTE: "SW" rails are dynamically switched in the S0 state as needed, controlled by MCP89 GPIOs.

OMIT_TABLE

U1400
MCP89U-A01
BGA
SYMBOL 8 OF 11
POWER I

=PP1V05_SW_MCP_FSB (2000 mA)	C32	+VTT_CPU	
	E33	+VTT_CPU	
	L29	+VTT_CPU	
	AA29	+VTT_CPU	
	E32	+VTT_CPU	
	AA30	+VTT_CPU	
	L31	+VTT_CPU	
	T30	+VTT_CPU	
	N30	+VTT_CPU	
	M31	+VTT_CPU	
	F33	+VTT_CPU	
	H33	+VTT_CPU	
	J32	+VTT_CPU	
	B33	+VTT_CPU	
	G33	+VTT_CPU	
	B32	+VTT_CPU	
	J33	+VTT_CPU	
	F32	+VTT_CPU	
	H32	+VTT_CPU	
	G32	+VTT_CPU	
	A33	+VTT_CPU	
	D32	+VTT_CPU	
	AB30	+VTT_CPU	
	AB29	+VTT_CPU	
	C33	+VTT_CPU	
	D33	+VTT_CPU	
	A32	+VTT_CPU	
	M29	+VTT_CPU	
	M30	+VTT_CPU	
	R30	+VTT_CPU	
	P30	+VTT_CPU	
	L32	+VTT_CPU	
	T29	+VTT_CPU	
	L30	+VTT_CPU	
	U30	+VTT_CPU	
	P29	+VTT_CPU	
	R29	+VTT_CPU	
	V30	+VTT_CPU	
	U29	+VTT_CPU	
	V29	+VTT_CPU	
	Y30	+VTT_CPU	
	Y29	+VTT_CPU	
	W29	+VTT_CPU	
	W30	+VTT_CPU	
	N29	+VTT_CPU	
	K31	+VTT_CPU	
=PP1V05_S0_MCP_FSB (200 mA)	AC29	+VTT_CPU2	
	AD29	+VTT_CPU2	
	AC30	+VTT_CPU2	
	AD30	+VTT_CPU2	
	AB31	+VTT_CPU2	
	AC31	+VTT_CPU2	
	AD31	+VTT_CPU2	
	AC32	+VTT_CPU2	
=PP3V3_S0_MCP_HVDD (30 mA)	V9	+3.3V_HVDD	
	V10	+3.3V	
=PP3V3_S0_MCP (250 mA)	H11	+3.3V	
	K29	+3.3V	
=PP0V9_S5_MCP_VDD_AUXC (150 mA)	L18	+VDD_DUAL_AUXC	
	K18	+VDD_DUAL_AUXC	
PP3V3_G3_RTC (22 uA (G3), 5 mA (S0))	A18	+3.3V_VBAT	
	L20	+3.3V_DUAL_USB	
(200 mA)	K20	+3.3V_DUAL_USB	
	J15	+3.3V_DUAL	
=PP3V3_S5_MCP (240 mA, 40 mA)			

	AK19	+VDD_MEM	
	AJ23	+VDD_MEM	
	AJ24	+VDD_MEM	
	AK21	+VDD_MEM	
	AJ17	+VDD_MEM	
	AK15	+VDD_MEM	
	AK5	+VDD_MEM	
	AJ26	+VDD_MEM	
	AK13	+VDD_MEM	
	AK16	+VDD_MEM	
	AJ19	+VDD_MEM	
	AK12	+VDD_MEM	
	AK4	+VDD_MEM	
	AK26	+VDD_MEM	
	AK20	+VDD_MEM	
	AJ27	+VDD_MEM	
	AJ10	+VDD_MEM	
	AJ12	+VDD_MEM	
	AK17	+VDD_MEM	
	AK23	+VDD_MEM	
	AJ2	+VDD_MEM	
	AK3	+VDD_MEM	
	AJ22	+VDD_MEM	
	AJ21	+VDD_MEM	
	AK14	+VDD_MEM	
	AK22	+VDD_MEM	
	AK8	+VDD_MEM	
	AK27	+VDD_MEM	
	AJ4	+VDD_MEM	
	AK29	+VDD_MEM	
	AK18	+VDD_MEM	
	AK24	+VDD_MEM	
	AJ9	+VDD_MEM	
	AK11	+VDD_MEM	
	AK6	+VDD_MEM	
	AK2	+VDD_MEM	
	AK25	+VDD_MEM	
	AJ28	+VDD_MEM	
	AK9	+VDD_MEM	
	AK28	+VDD_MEM	
	AJ11	+VDD_MEM	
	AJ5	+VDD_MEM	
	AJ29	+VDD_MEM	
	AJ3	+VDD_MEM	
	AJ20	+VDD_MEM	
	AK10	+VDD_MEM	
	AJ18	+VDD_MEM	
	AK1	+VDD_MEM	
	AJ1	+VDD_MEM	
	AJ7	+VDD_MEM	
	AJ8	+VDD_MEM	
	AJ25	+VDD_MEM	
	AJ16	+VDD_MEM	
	AJ15	+VDD_MEM	
	AK7	+VDD_MEM	
	AJ6	+VDD_MEM	
	AJ13	+VDD_MEM	
	AJ14	+VDD_MEM	
	AL11	+VDD_MEM	
	AL12	+VDD_MEM	
	AL14	+VDD_MEM	
	AL15	+VDD_MEM	
	AL17	+VDD_MEM	
	AL18	+VDD_MEM	
	AL20	+VDD_MEM	
	AL21	+VDD_MEM	
	AL26	+VDD_MEM	
	AL27	+VDD_MEM	
	AL29	+VDD_MEM	
	AL30	+VDD_MEM	
	K17	+VDD_DUAL_RMGT	=PP0V9_ENET_MCP_RMGT (140 mA)
	L17	+VDD_DUAL_RMGT	
	A17	+3.3V_DUAL_RMGT	=PP3V3_ENET_MCP_RMGT (300 mA)
	B17	+3.3V_DUAL_RMGT	

=PP1V5R1V35_SW_MCP_MEM (4300 mA)

NOTE: VDD_COREx_SENSE signals should NOT be used for remote sensing unless COREA/COREB are powered by separate regulators.
Instead connect regulator sense point as close to COREB FET as possible.

OMIT_TABLE

U1400
MCP89U-A01
BGA
SYMBOL 9 OF 11
POWER II

=PPVCORE_S0_MCP (8450 mA (0.85V))

	N7	+VDD_COREA	
	N2	+VDD_COREA	
	N11	+VDD_COREA	
	R12	+VDD_COREA	
	P9	+VDD_COREA	
	R8	+VDD_COREA	
	N4	+VDD_COREA	
	R5	+VDD_COREA	
	R3	+VDD_COREA	
	P3	+VDD_COREA	
	P4	+VDD_COREA	
	P8	+VDD_COREA	
	R2	+VDD_COREA	
	P1	+VDD_COREA	
	R9	+VDD_COREA	
	N5	+VDD_COREA	
	N10	+VDD_COREA	
	P10	+VDD_COREA	
	R1	+VDD_COREA	
	P2	+VDD_COREA	
	R4	+VDD_COREA	
	N8	+VDD_COREA	
	R10	+VDD_COREA	
	P5	+VDD_COREA	
	AD24	+VDD_COREA	
	R7	+VDD_COREA	
	P6	+VDD_COREA	
	R6	+VDD_COREA	
	AB24	+VDD_COREA	
	AC24	+VDD_COREA	
	P11	+VDD_COREA	
	P12	+VDD_COREA	
	P7	+VDD_COREA	
	R11	+VDD_COREA	
	AD23	+VDD_COREA	
	Y24	+VDD_COREA	
	AA24	+VDD_COREA	
	N12	+VDD_COREA	
	AD17	+VDD_COREA	
	AD18	+VDD_COREA	
	AD19	+VDD_COREA	
	AD20	+VDD_COREA	
	AD21	+VDD_COREA	
	AD22	+VDD_COREA	
	U24	+VDD_COREA	
	V24	+VDD_COREA	
	W24	+VDD_COREA	
	T11	+VDD_COREA	
	T12	+VDD_COREA	
	U11	+VDD_COREA	
	V11	+VDD_COREA	
TP_MCP_VDDCOREA_SENSEP	U9	+VDD_COREA_SENSE	
TP_MCP_VDDCOREA_SENSEN	U8	GND_COREA_SENSE	
=PP1V05_S0_MCP_PE_DVDD (400 mA (PE0[5:0], PE1[1:0]))	AD8	+VIO_PE_DVDD	
	AD6	+VIO_PE_DVDD	
	AC8	+VIO_PE_DVDD	
	AC9	+VIO_PE_DVDD	
	AD9	+VIO_PE_DVDD	
	AC7	+VIO_PE_DVDD	
	AC10	+VIO_PE_DVDD	
	AD7	+VIO_PE_DVDD	
	AD11	+VIO_PE_DVDD	
	AD10	+VIO_PE_DVDD	
	AC11	+VIO_PE_DVDD	
	AC12	+VIO_PE_DVDD	
	AD12	+VIO_PE_DVDD	
	AE12	+VIO_PE_DVDD	
PP1V05_S0_MCP_PE_AVDD (1000 MA (PE0[5:0], PE1[1:0]))	AA10	+VIO_PE_AVDD	
	U12	+VIO_PE_AVDD	
	AB10	+VIO_PE_AVDD	
	V12	+VIO_PE_AVDD	
	W11	+VIO_PE_AVDD	
	W12	+VIO_PE_AVDD	
	Y11	+VIO_PE_AVDD	
	Y12	+VIO_PE_AVDD	
	AA11	+VIO_PE_AVDD	
	AA12	+VIO_PE_AVDD	
	AB11	+VIO_PE_AVDD	
	AB12	+VIO_PE_AVDD	

=PPVCORE_SW_MCP_GFX (15350 mA (0.85V))

	M9	+VDD_COREB	
	K2	+VDD_COREB	
	L7	+VDD_COREB	
	M7	+VDD_COREB	
	Y23	+VDD_COREB	
	M2	+VDD_COREB	
	AB23	+VDD_COREB	
	M11	+VDD_COREB	
	M12	+VDD_COREB	
	L8	+VDD_COREB	
	M8	+VDD_COREB	
	M10	+VDD_COREB	
	L10	+VDD_COREB	
	M6	+VDD_COREB	
	L12	+VDD_COREB	
	K10	+VDD_COREB	
	K7	+VDD_COREB	
	M1	+VDD_COREB	
	K8	+VDD_COREB	
	K5	+VDD_COREB	
	L9	+VDD_COREB	
	M3	+VDD_COREB	
	J4	+VDD_COREB	
	M4	+VDD_COREB	
	L11	+VDD_COREB	
	L5	+VDD_COREB	
	J2	+VDD_COREB	
	J1	+VDD_COREB	
	J7	+VDD_COREB	
	M5	+VDD_COREB	
	L4	+VDD_COREB	
	L3	+VDD_COREB	
	J3	+VDD_COREB	
	K11	+VDD_COREB	
	J6	+VDD_COREB	
	L2	+VDD_COREB	
	L1	+VDD_COREB	
	J5	+VDD_COREB	
	L6	+VDD_COREB	
	K4	+VDD_COREB	
	V23	+VDD_COREB	
	V17	+VDD_COREB	
	V19	+VDD_COREB	
	V18	+VDD_COREB	
	V20	+VDD_COREB	
	V21	+VDD_COREB	
	V22	+VDD_COREB	
	AB21	+VDD_COREB	
	Y17	+VDD_COREB	
	Y18	+VDD_COREB	
	Y19	+VDD_COREB	
	Y20	+VDD_COREB	
	Y21	+VDD_COREB	
	Y22	+VDD_COREB	
	AB22	+VDD_COREB	
	AB17	+VDD_COREB	
	AB18	+VDD_COREB	
	AB19	+VDD_COREB	
	AB20	+VDD_COREB	
	L13	+VDD_COREB	
	L14	+VDD_COREB	
	M13	+VDD_COREB	
	M14	+VDD_COREB	
	J9	+VDD_COREB_SENSE	TP_MCP_VDDCOREB_SENSEP
	J8	GND_COREB_SENSE	TP_MCP_VDDCOREB_SENSEN
PP1V05_S0_MCP_SATA_AVDD (300 mA)	AF6	+VIO_SATA_AVDD	
	AG8	+VIO_SATA_AVDD	
	AF7	+VIO_SATA_AVDD	
	AF8	+VIO_SATA_AVDD	
	AG9	+VIO_SATA_AVDD	
	AG6	+VIO_SATA_AVDD	
	AF9	+VIO_SATA_AVDD	
	AG7	+VIO_SATA_AVDD	
=PP1V05_S0_MCP_SATA_DVDD (100 mA)	AD1	+VIO_SATA_DVDD	
	AD2	+VIO_SATA_DVDD	
	AD3	+VIO_SATA_DVDD	
	AD4	+VIO_SATA_DVDD	
	AC3	+VIO_SATA_DVDD	
	AC4	+VIO_SATA_DVDD	
	AC5	+VIO_SATA_DVDD	
	AD5	+VIO_SATA_DVDD	
	AC6	+VIO_SATA_DVDD	
	AC1	+VIO_SATA_DVDD	
	AC2	+VIO_SATA_DVDD	

OMIT_TABLE

U1400
MCP89U-A01
BGA
SYMBOL 10 OF 11
GND

AL34	G13	
AT10	E10	
AE4	B10	
K37	AM32	
AL25	AU25	
T36	AY38	
T37	W4	
AB2	AU10	
AB4	D10	
C40	H31	
B5	AL31	
G4	U31	
AE8	AT31	
AW34	AH31	
AC20	AN25	
AE5	AC21	
W18	AA22	
AT16	AN16	
AB5	AE31	
N34	AU34	
AT2	AW19	
W20	G10	
AW16	B22	
D7	B19	
B2	B34	
G37	E22	
D16	AC18	
K39	K34	
G31	AL22	
B7	AP36	
L15	G34	
W19	P31	
Y10	U21	
AW2	H25	
AH7	B31	
B13	AU4	
AE37	AA19	
AV1	W8	
AN19	AT19	
AP10	AT13	
W33	AH2	
AB36	AP19	
K13	A38	
AU13	AT34	
AA23	AE39	
AA31	AA18	
Y31	AT25	
AE33	AW31	
AY3	U23	
N33	D22	
T2	W36	
B39	W39	
T4	W37	
AH37	AC23	
V31	AP22	
AU37	AN13	
AW5	AP31	
AU7	AU31	
AT7	AL19	
AN28	AL2	
D4	AA20	
AU19	E28	
AP25	AH34	
AU22	B28	
AW13	AV40	
T33	D28	
E7	H28	
AW7	G36	
H13	AE36	

OMIT_TABLE

U1400
MCP89U-A01
BGA
SYMBOL 11 OF 11
GND

B16	B36	
E16	AB37	
AP16	AE2	
AL36	AL7	
G19	D13	
AA21	T39	
K16	AH4	
K28	AB7	
D25	AH36	
AL16	AC17	
AP4	AH5	
G25	AL33	
K25	AW10	
E31	W17	
G16	G39	
AP13	AB39	
U22	AH39	
AP28	AL5	
AT28	AW39	
H16	AN10	
AH33	AB8	
AT22	N39	
AL8	N36	
AA1	N37	
AP37	AE29	
W22	AW28	
H19	AU28	
A3	E19	
AH8	L16	
G28	K22	
R31	AW22	
AW25	T34	
AP39	AN22	
AB33	D31	
B25	AE30	
U10	T8	
W34	M16	
U19	M15	
K12	M17	
E34	M18	
AL28	M19	
AE34	M20	
AT39	M21	
AP5	AE7	
W21	W5	
D34	W7	
E25	AP2	
K36	AL10	
D19	AP34	
Y1	U18	
W23	T7	
AC22	W31	
H22	AL39	
H8	T31	
K19	N31	
G2	AA17	
E2	T10	
T5	K33	
AC19	E13	
AN31	AL13	
AL37	AP7	
AU16	U17	
AB34	W2	
U20	AK34	
G22	AK35	
AW36	H6	
AL4	H7	
C1	V7	
E39	V8	
D37	AM5	

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE: MCP Power & Ground

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

BRANCH:

PAGE: 20 OF 110

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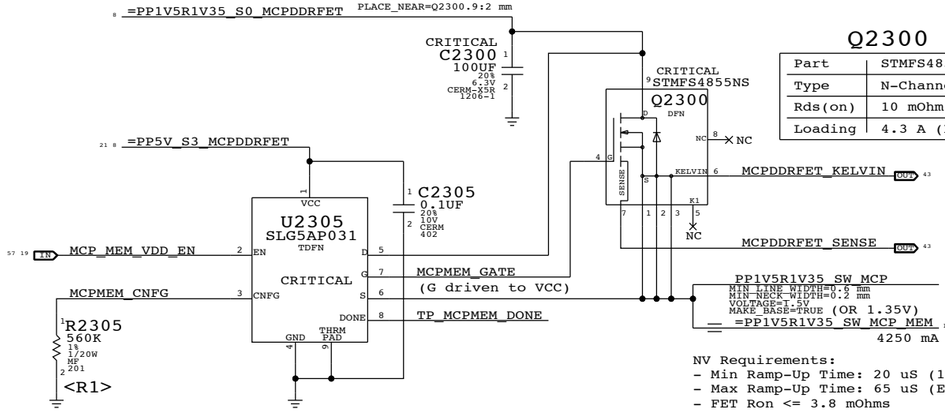
C2300 helps reduce input rail
droop during Q2300 turn-on.



Q2300	
Part	STMFS4854N
Type	N-Channel
Rds(on)	10 mOhm @3.2V
Loading	4.3 A (EDP)

Approx. Ramp Time (EN to 1.35V, uS): 7.91 + 0.0678 * R1(Kohms)

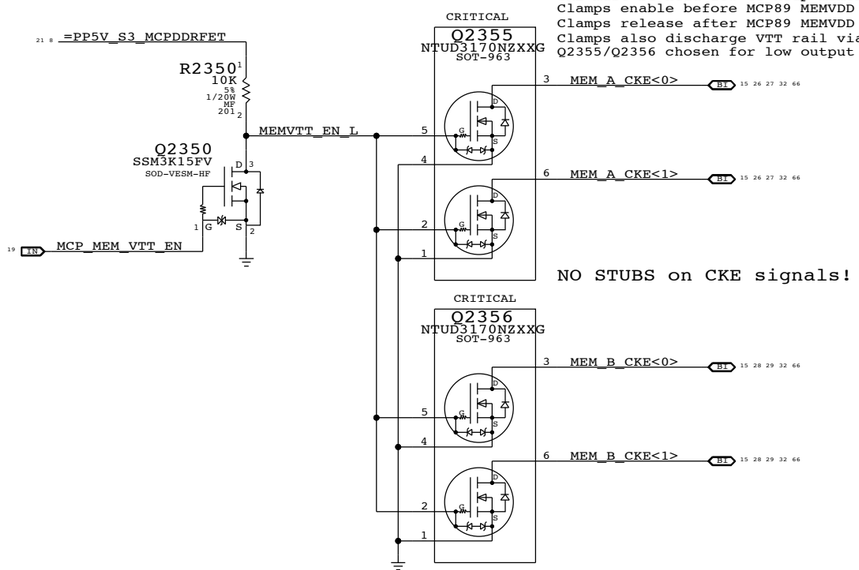
NV Requirements:
- Min Ramp-Up Time: 20 uS (10% to 90%)
- Max Ramp-Up Time: 65 uS (ENABLE to 90%)
- FET Ron <= 3.8 mOhms

NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.

Gated Rail Savings: 120mW

DIMM CKE Clamps

CKE must be held low to keep memory in self-refresh.
Clamps enable before MCP89 MEMVDD rail switched off.
Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.
Clamps also discharge VTT rail via termination resistor on each CKE signal on DIMM.
Q2355/Q2356 chosen for low output capacitance.



SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE
MCP89 Memory Rail Gating

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DRAWING NUMBER 051-8379 SIZE D
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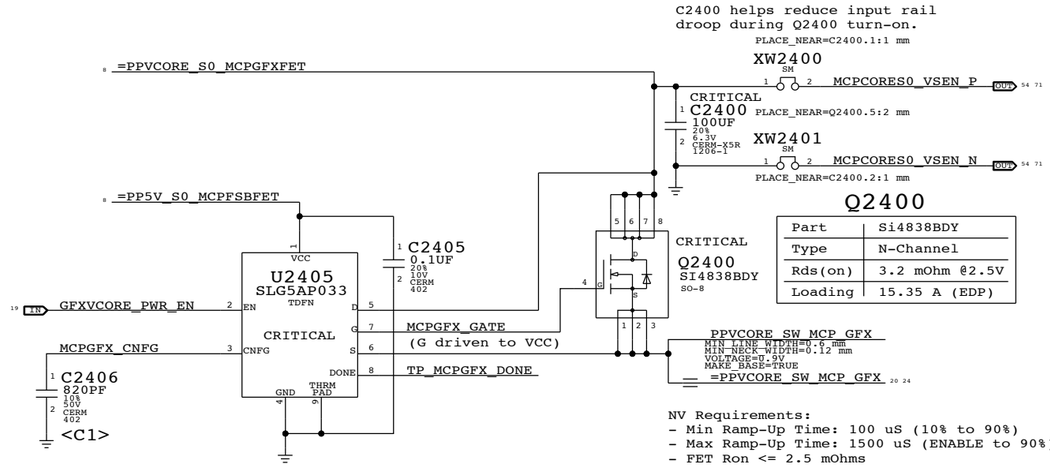

C2400 helps reduce input rail droop during Q2400 turn-on.

Q2400

Part	Si4838BDY
Type	N-Channel
Rds(on)	3.2 mOhm @2.5V
Loading	15.35 A (EDP)

Approx. Ramp Time (EN to 1V, uS): 43.9 + 0.6943 * C1(pF)

NV Requirements:
- Min Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- FET Ron <= 2.5 mOhms

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

Gated Rail Savings: 860mW

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE
MCP89 GFX Core Rail Gating

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DRAWING NUMBER 051-8379 SIZE D
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MCP Non-GFX Core Power

=PPVCORE_S0_MCP
8450 mA (0.85V)

OMIT_TABLE
C2500 10UF 20% 6.3V X5R 603-1
C2501 4.7UF 20% 4V X5R-1 402
C2502 1.0UF 20% 6.3V X5R 0201
C2503 0.22UF 20% 6.3V X5R 201
C2504 0.1UF 10% 6.3V X5R 201
C2505 0.1UF 10% 6.3V X5R 201
C2506 0.1UF 10% 6.3V X5R 201
C2507 0.1UF 10% 6.3V X5R 201
C2508 0.1UF 10% 6.3V X5R 201

MCP Memory Power

=PP1V5R1V35_SW_MCP_MEM
4300 mA (1.5V)

C2510 4.7UF 20% 4V X5R-1 402
C2511 0.1UF 10% 6.3V X5R 201
C2512 0.1UF 10% 6.3V X5R 201
C2513 0.1UF 10% 6.3V X5R 201
C2514 0.1UF 10% 6.3V X5R 201
C2515 0.1UF 10% 6.3V X5R 201
C2516 0.1UF 10% 6.3V X5R 201
C2517 0.1UF 10% 6.3V X5R 201
C2518 0.1UF 10% 6.3V X5R 201
C2519 0.1UF 10% 6.3V X5R 201

MCP CPU FSB (VTT) Power

=PP1V05_SW_MCP_FSB
2000 mA

OMIT_TABLE
C2520 10UF 20% 6.3V X5R 603-1
C2521 4.7UF 20% 4V X5R-1 402
C2522 1.0UF 20% 6.3V X5R 0201
C2523 1.0UF 20% 6.3V X5R 0201

MCP S0 FSB (VTT) Power

=PP1V05_S0_MCP_FSB
200 mA

C2524 4.7UF 20% 4V X5R-1 402
C2525 1.0UF 20% 6.3V X5R 0201

MCP 0.9V AUX Core Power

=PP0V9_S5_MCP_VDD_AUXC
150 mA

C2526 0.1UF 10% 6.3V X5R 201
C2527 0.1UF 10% 6.3V X5R 201

MCP 0.9V MAC/SMU Power

=PP0V9_ENET_MCP_RMGT
140 mA

C2528 4.7UF 20% 4V X5R-1 402
C2529 0.1UF 10% 6.3V X5R 201

MCP 1.05V PCIE Digital Power

=PP1V05_S0_MCP_PE_DVDD
200 mA

C2530 4.7UF 20% 4V X5R-1 402
C2538 4.7UF 20% 4V X5R-1 402
C2531 1.0UF 20% 6.3V X5R 0201
C2532 1.0UF 20% 6.3V X5R 0201
C2533 0.1UF 10% 6.3V X5R 201
C2534 0.1UF 10% 6.3V X5R 201
C2535 0.1UF 10% 6.3V X5R 201

MCP 1.05V SATA Digital Power

=PP1V05_S0_MCP_SATA_DVDD
100 mA

C2536 4.7UF 20% 4V X5R-1 402
C2537 0.1UF 10% 6.3V X5R 201

MCP 1.05V Memory DLL Power

=PP1V05_S0_MCP_M2CLK_DLL
550 mA

C2540 4.7UF 20% 4V X5R-1 402

MCP 3.3V PCIe/SATA I/O PLL Power

=PP3V3_S0_MCP_HVDD
30 mA

C2541 4.7UF 20% 6.3V CERM 603
C2542 0.1UF 20% 10V CERM 402

MCP 3.3V I/O Power

=PP3V3_S0_MCP
250 mA

C2543 4.7UF 20% 6.3V CERM 603
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402

MCP 3.3V/1.5V HDA Power

=PP3V3R1V5_S0_MCP_HDA
70 mA

C2548 4.7UF 20% 6.3V CERM 603
C2549 0.1UF 10% 6.3V X5R 201

MCP 3.3V AUX/USB Power

=PP3V3_S5_MCP
240 mA

C2550 4.7UF 20% 6.3V CERM 603
C2551 0.1uF 20% 10V CERM 402

MCP 2.0V-3.3V RTC Power

PP3V3_G3_RTC
? uA (G3)
5 mA (S0)

C2552 4.7UF 20% 6.3V CERM 603

MCP 3.3V MAC/SMU Power

=PP3V3_ENET_MCP_RMGT
300 mA

C2553 4.7UF 20% 6.3V CERM 603
C2554 0.1uF 20% 10V CERM 402

MCP 1.05V PCIe Analog Power

=PP1V05_S0_MCP_AVDD_UF
800 mA

L2560 30-OHM-5A 0603
OMIT_TABLE
C2560 10UF 20% 6.3V X5R 603-1
C2561 4.7UF 20% 4V X5R-1 402
C2559 4.7UF 20% 4V X5R-1 402
C2562 1.0UF 20% 6.3V X5R 0201
C2563 1.0UF 20% 6.3V X5R 0201
C2564 0.1UF 10% 6.3V X5R 201
C2565 0.1UF 10% 6.3V X5R 201
C2566 0.1UF 10% 6.3V X5R 201

PP1V05_S0_MCP_PE_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=T.05V
500 mA

MCP 1.05V SATA Analog Power

L2567 30-OHM-5A 0603
OMIT_TABLE
C2567 10UF 20% 6.3V X5R 603-1
C2568 4.7UF 20% 4V X5R-1 402
C2569 0.1UF 10% 6.3V X5R 201

PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=T.05V
300 mA

MCP 1.05V CPU/FSB/MEM PLL Power

=PP1V05_S0_MCP_PLL_UF
555 mA

CRITICAL
L2570 220-OHM-2.2A 0603
C2570 4.7UF 20% 4V X5R-1 402
PLACE_NEAR=R2570.1:50 mil
R2570 0.33 5% 1/16W MF 0402
GND_MCP_PLL_FSB
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=0V
C2571 0.1UF 10% 6.3V X5R 201
C2572 0.1UF 10% 6.3V X5R 201
C2573 0.1UF 10% 6.3V X5R 201

PP1V05_S0_MCP_PLL_FSBMEM
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=T.05V
70 mA

MCP 1.05V PCIe/SATA PLL Power

CRITICAL
L2575 220-OHM-2.2A 0603
C2575 4.7UF 20% 4V X5R-1 402
C2576 0.1UF 10% 6.3V X5R 201
C2577 0.1UF 10% 6.3V X5R 201
C2578 0.1UF 10% 6.3V X5R 201
C2579 0.1UF 10% 6.3V X5R 201

PP1V05_S0_MCP_PLL_PEXSATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=T.05V
325 mA

MCP 1.05V Core/Misc PLL Power

CRITICAL
L2580 220-OHM-2.2A 0603
C2580 4.7UF 20% 4V X5R-1 402
C2581 0.1UF 10% 6.3V X5R 201
C2582 0.1UF 10% 6.3V X5R 201
C2583 0.1UF 10% 6.3V X5R 201
C2584 0.1UF 10% 6.3V X5R 201

PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=T.05V
160 mA

MCP 3.3V PLL Power

=PP3V3_S0_MCP_PLL_UF
260 mA

MCPHVDD:P3V3
CRITICAL
L2590 FERR-240-OHM-200MA 0402
MCPHVDD:P2V5
R2590 10K 5% 1/20W MF 201
MCPHVDD:P2V5
C2592 1.0UF 20% 6.3V X5R 0201
CRITICAL
OMIT_TABLE
U2590 MIC5365-2.5V SC70
VIN VOUT EN NC GND
P2V8HVDD_EN
P2V8HVDD_FB
HVDDLDO:ADJ
R2591 665K 1% 1/20W MF 201
<Ra>
HVDDLDO:ADJ
R2592 316K 1% 1/20W MF 201
<Rb>
C2590 4.7UF 20% 6.3V CERM 603
C2591 0.1UF 20% 10V CERM 402

PP3V3_S0_MCP_PLL_HVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
50 mA

Vout = 0.8V * (Ra + Rb) / Rb, Rb ~ 320kOhms

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2988	1	IC,MIC5366,LDO RBG,2.5V,150MA,SC70	U2590	CRITICAL	HVDDLDO:FIXED
353S2979	1	IC,LDO,TPS717,ADJ,150MA,3%,SC70,HF	U2590	CRITICAL	HVDDLDO:ADJ

MCP 3.3V DP & USB PLL Power

CRITICAL
L2595 220-OHM-2.2A 0603
C2595 4.7UF 20% 6.3V CERM 603
PLACE_NEAR=R2595.1:50 mil
R2595 0.33 5% 1/16W MF 0402
GND_MCP_PLL_DP_USB
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=0V
C2596 0.1UF 20% 10V CERM 402
C2597 0.1uF 20% 10V CERM 402

PP3V3_S0_MCP_PLL_DP_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
210 mA

MCP 3.3V MAC PLL POWER

=PP3V3_ENET_MCP_PLL_MAC
20 mA

CRITICAL
L2555 FERR-240-OHM-200MA 0402
C2555 4.7UF 20% 6.3V CERM 603
C2556 0.1UF 20% 10V CERM 402

PP3V3_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
20 mA

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB
SYNC_DATE=07/07/2010

PAGE TITLE
MCP Standard Decoupling

Apple Inc.

DRAWING NUMBER 051-8379
SIZE D
REVISION 4.4.0
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PAGE 25 OF 110
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MCP GFX Core Power

22 20 =PPVCORE_SW_MCP_GFX

15350 mA (0.85V)

OMIT_TABLE

C2600 10UF 20% 6.3V X5R 603-1

C2601 4.7UF 20% 4V X5R-1 402

C2602 1.0UF 20% 6.3V X5R 0201

C2603 1.0UF 20% 6.3V X5R 0201

C2604 0.22UF 20% 6.3V X5R 201

C2605 0.22UF 20% 6.3V X5R 201

C2606 0.1UF 10% 6.3V X5R 201

C2607 0.1UF 10% 6.3V X5R 201

C2608 0.1UF 10% 6.3V X5R 201

C2609 0.1UF 10% 6.3V X5R 201

C2610 0.1UF 10% 6.3V X5R 201

C2611 0.1UF 10% 6.3V X5R 201

C2612 0.1UF 10% 6.3V X5R 201

MCP 3.3V RGBDAC Power

GND_MCP_DAC_P3V3 — PP3V3_S0_MCP_DAC 17

MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
MAKE_BASE=TRUE

140 mA

R2670 0 5% 1/20W MF 201

If RGBDAC is used, requires ferrite (155S0382) plus 1x 4.7uF 0603 & 1x 0.1uF 0402 cap.

If RGBDAC is not used, tie to GND.

— =PP3V3R1V8_S0_MCP_IFP_VDD 17

— =PP1V05_S0_MCP_PLL_IFP 17

MCP 1.05V DisplayPort Power

17 8 =PP1V05_S0_MCP_DP0_VDD

160 mA

C2640 4.7UF 20% 4V X5R-1 402

C2641 0.1UF 10% 6.3V X5R 201

67 17 MCP_TMDS0_RSET

67 17 MCP_TMDS0_VPROBE

NO STUFF C2650 0.1UF 10% 6.3V X5R 201

R2650 1K 1% 1/20W MF 201

67 17 MCP_IFPAB_RSET

67 17 MCP_IFPAB_VPROBE

NO STUFF C2655 0.1UF 10% 6.3V X5R 201

NO STUFF R2655 1K 1% 1/20W MF 201

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE

MCP Graphics Support

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

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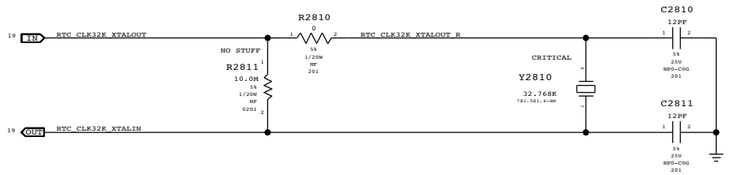
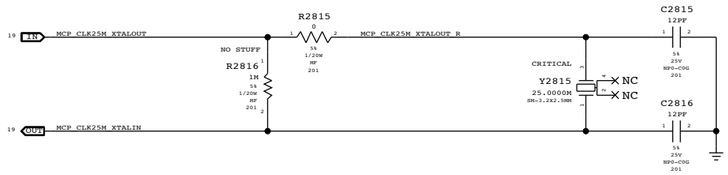
RTC Crystal



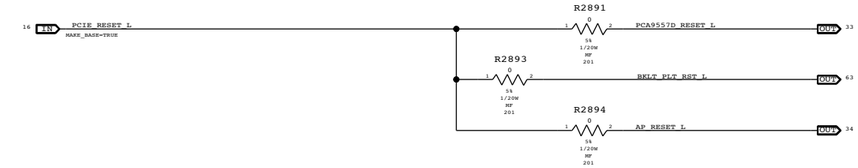
MCP 25MHz Crystal

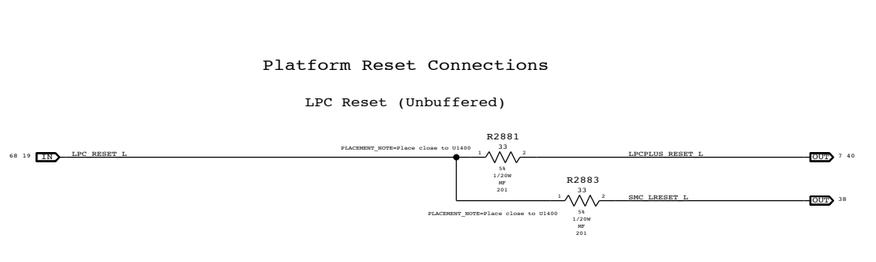


Platform Reset Connections

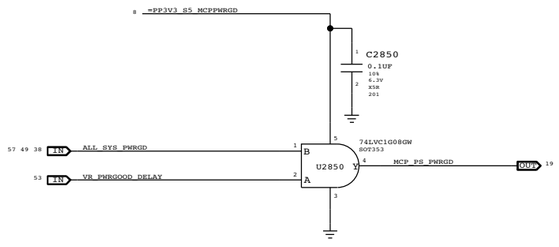
LPC Reset (Unbuffered)

PCIE Reset (Unbuffered)

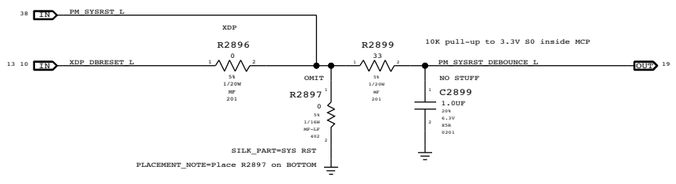




MCP S0 PWRGD & CPU_VLD



System Reset Circuit



SYNC MASTER=K6_MLB	SYNC DATE=12/11/2009
PAGE TITLE: SB Misc	
Apple Inc.	DRAWING NUMBER: 051-8379 SIZE: D
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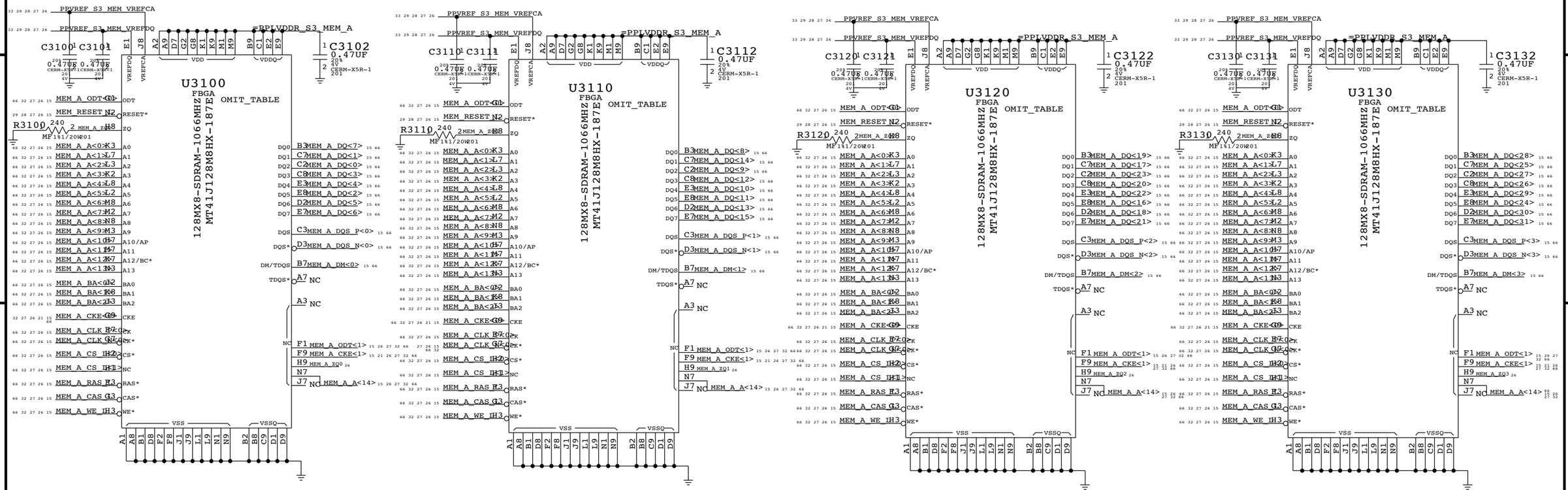

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
DDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D
REVISION 4.4.0
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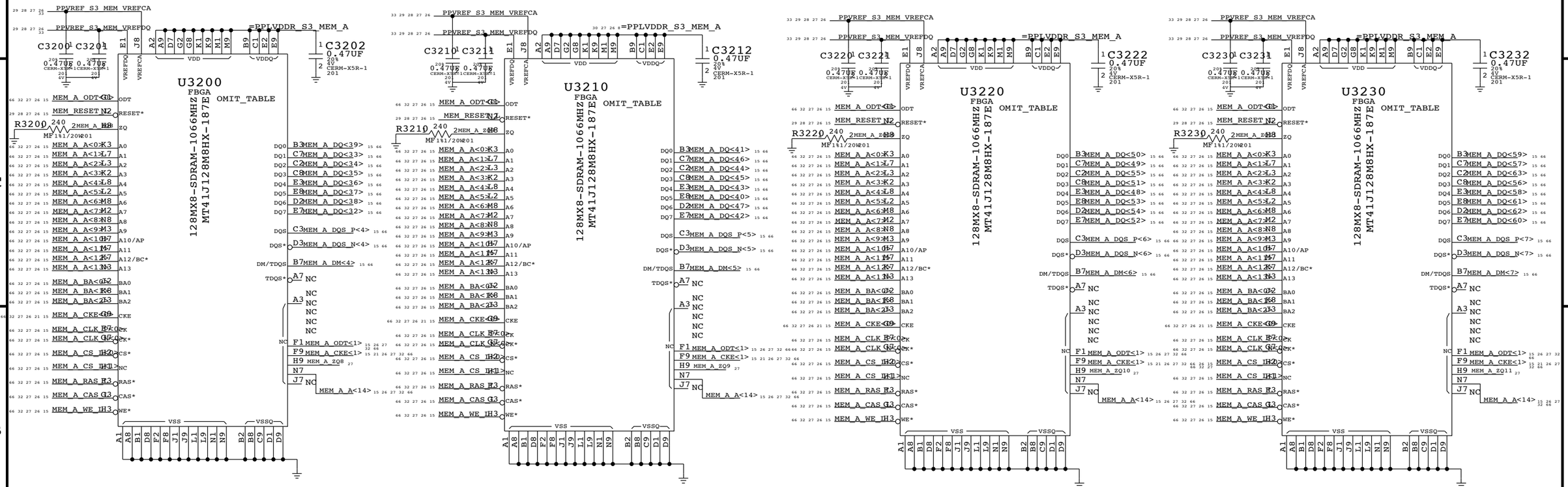

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE

DDR3 DRAM Channel A (32-63)

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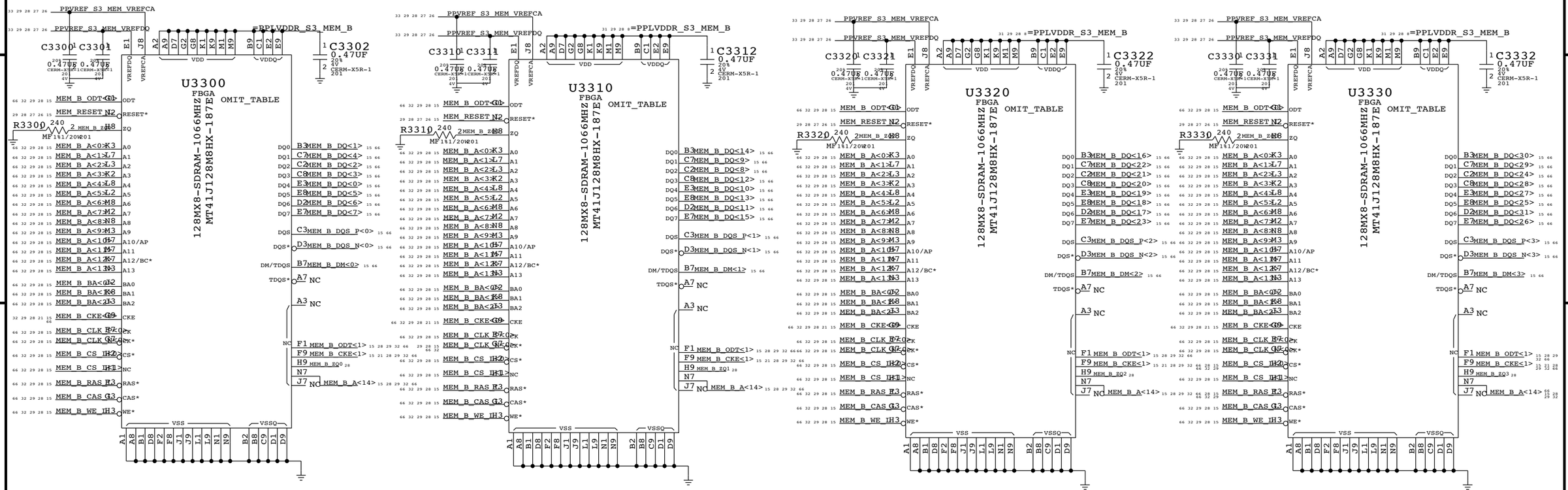

A14/A15 FOR 2G/4G MONO ONLY
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PAGE TITLE
DDR3 DRAM Channel B (0-31)

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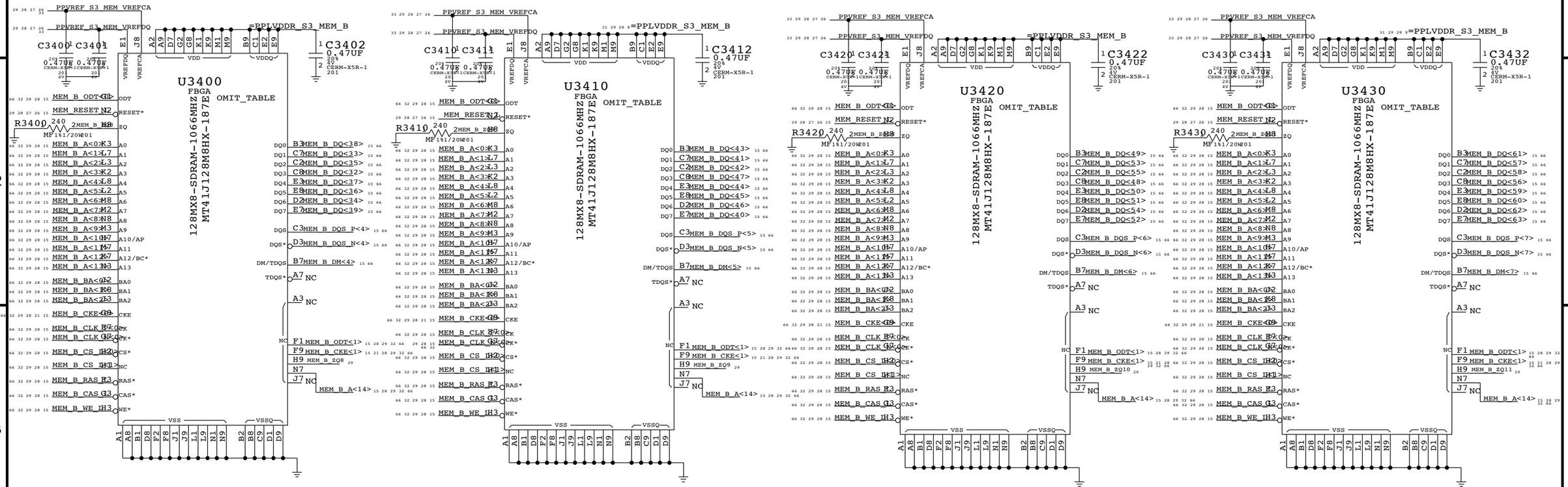

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
DDR3 DRAM Channel B (32-63)

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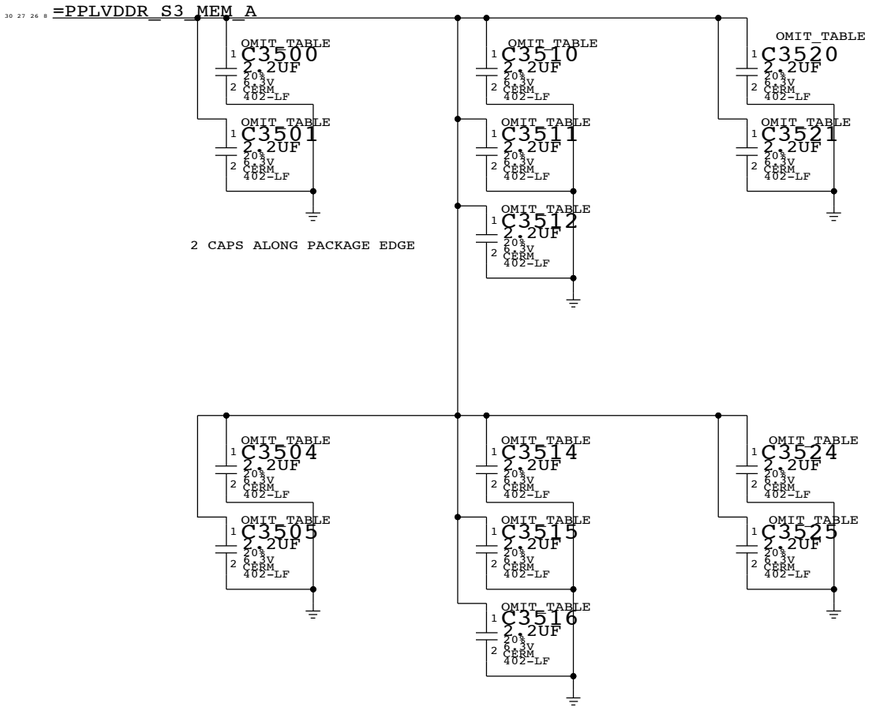

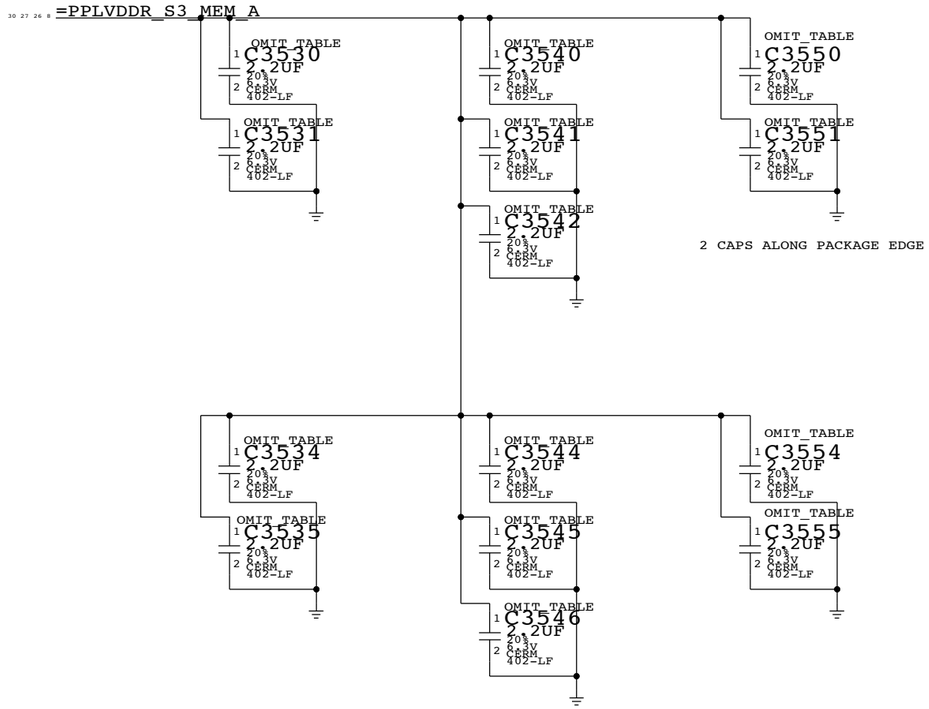

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PAGE TITLE

DDR BYPASSING 1

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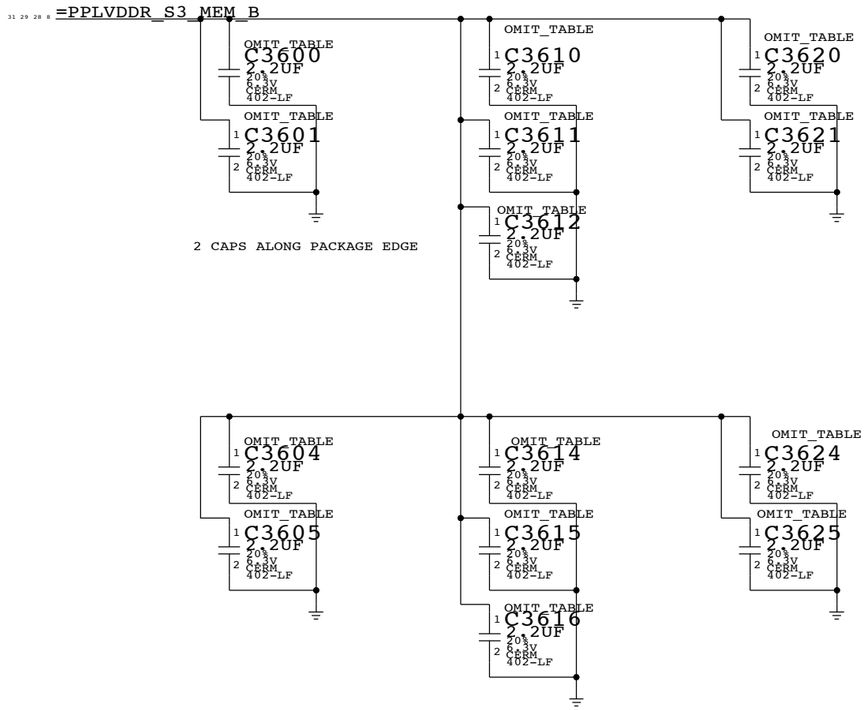

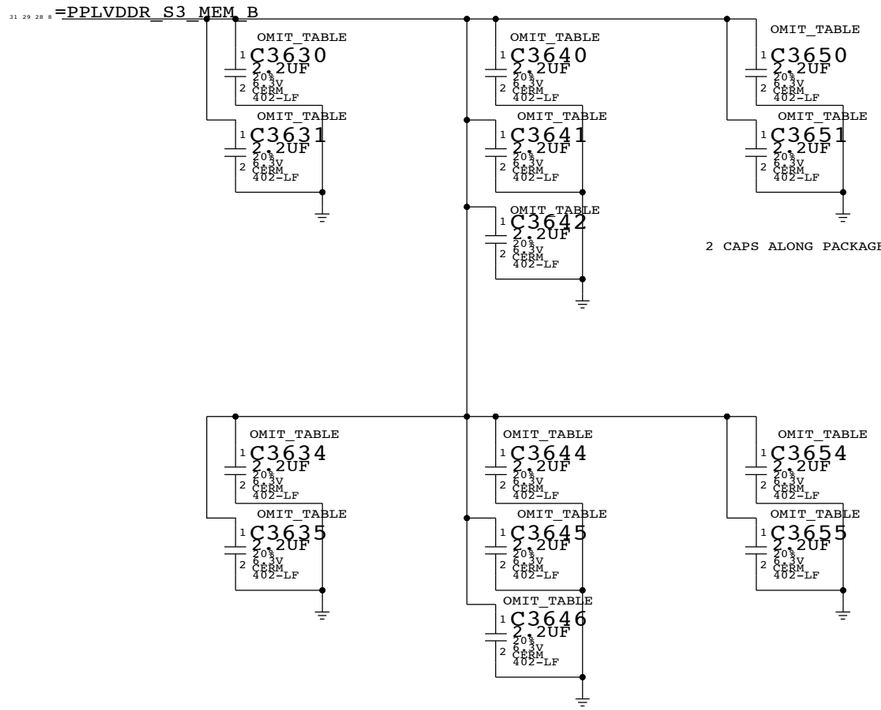

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PAGE TITLE

DDR BYPASSING 2

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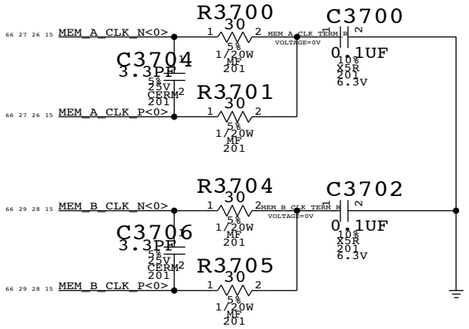
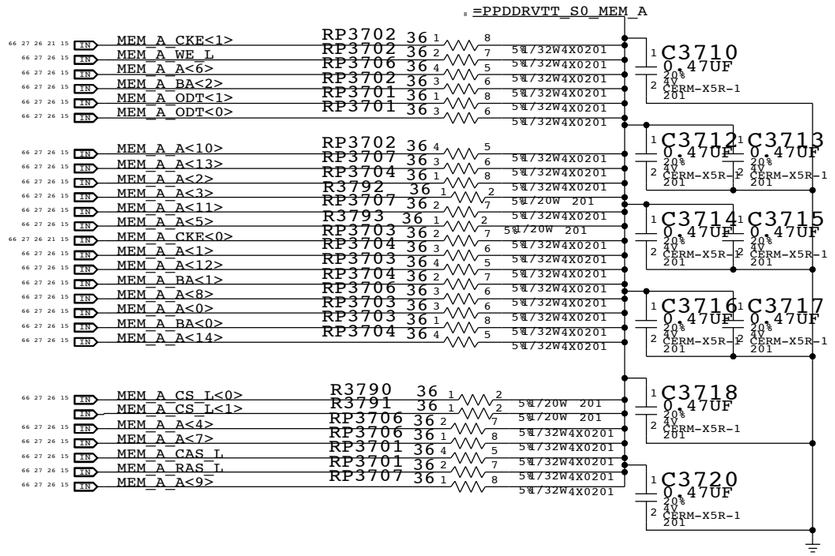
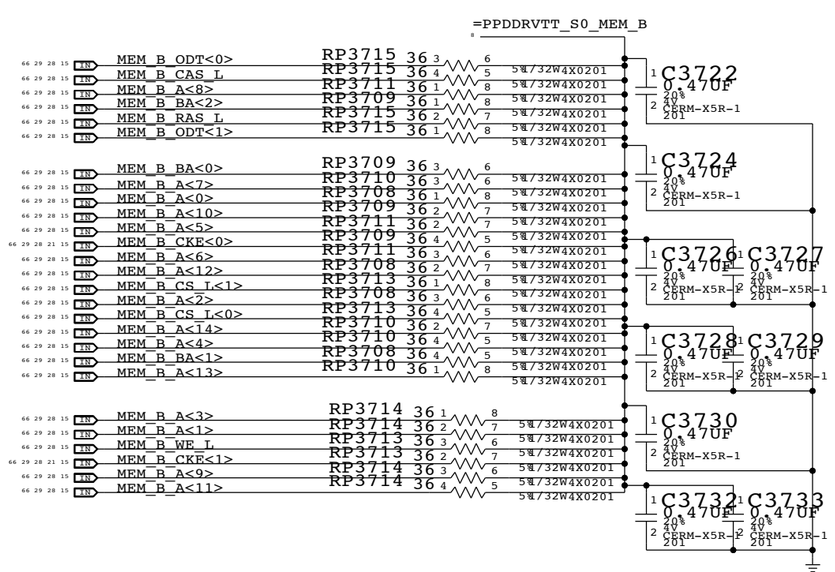
MEM CLOCK TERMINATION

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE
Memory Active Termination

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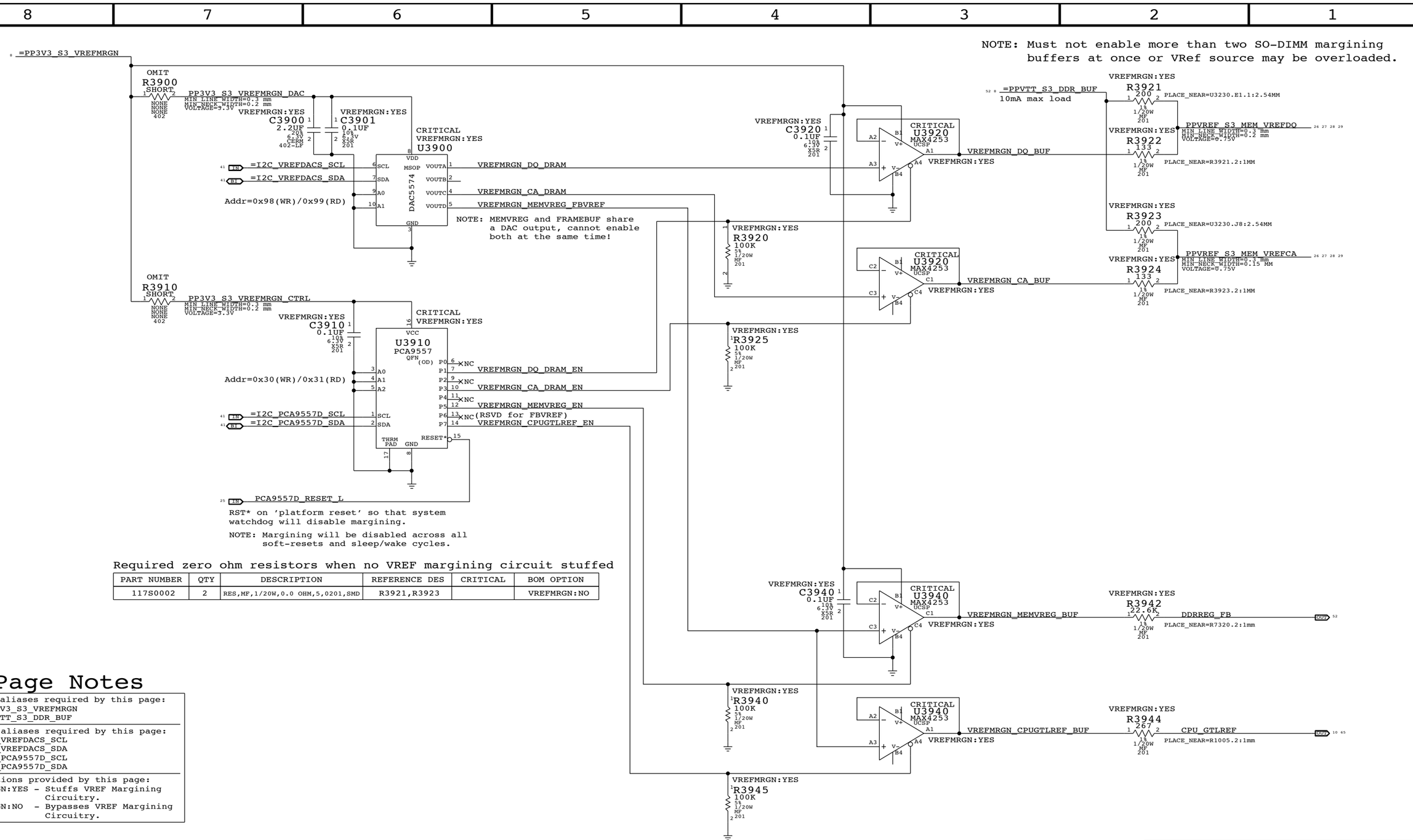

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3921,R3923		VREFMRGN:NO

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN:YES - Stuffs VREF Margining Circuitry.
VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM VREF DQ	MEM VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	C	D	D
PCA9557D Pin:	1	3	5	7
Nominal value		0.75V (DAC: 0x3A)	1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)	1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
VRef current:		+3.4mA - -3.4mA (- = sourced)	+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:		7.69mV / step @ output	8.59mV / step @ output	9.24mV / step @ output

SYNC MASTER=K16 MLB
SYNC DATE=07/07/2010
PAGE TITLE: FSB/DDR3 Vref Margining
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AIRPORT

CRITICAL
J4001
SSD-K99
F-RT-SM1

514S0335

WIFI_EVENT_L
PCIE_AP_R2D_N
PCIE_AP_R2D_C_N
PCIE_AP_R2D_P
PCIE_AP_R2D_C_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_P
PCIE_AP_D2R_N
PCIE_WAKE_L

C4030 0.1UF 10% 6.3V 201 X5R
PLACEMENT_NOTE=Place close to J4001.

C4031 0.1UF 10% 6.3V X5R 201
PLACEMENT_NOTE=Place close to J4001.

BLUETOOTH

USB_BT_N
USB_BT_P

=PP3V3_S3_BT

C4032 0.1UF 10% 6.3V X5R 201
PLACE_NEAR=J4001.27:1.5mm

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.750 A (EDP)

CRITICAL
R4052 0.020 1% 0.25W ME-LR 805
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

CRITICAL
Q4050 TPCP8102 23VIK-SM

PP3V3_WLAN_F
PP3V3_WLAN_R
=PP3V3_S3_WLAN

C4021 0.1UF 10% 6.3V X5R 201
C4020 10UF 20% 10V X5R 805
PLACEMENT_NOTE=Place close to Q4050.

C4050 0.1UF 10% 16V X5R 402
PLACEMENT_NOTE=Place close to Q4050.

C4051 0.033UF 10% 16V X5R 402

R4050 100K 5% 1/20W MF 201

R4051 10K 5% 1/20W MF 201

P3V3WLAN_SS
PM_WLAN_EN_L

ISNS_AIRPORT_P
ISNS_AIRPORT_N

DLY = 60 MS +/- 20%

=PP3V3_S3_WLAN

C4053 0.1UF 10% 6.3V X5R 201

CRITICAL
U4002
SLG4AP016V
TDFN
VDD
SENSE 0.7V
DLY
RESET*
MR*
EN
IN
OUT (OD)
THRM PAD
GND

R4053 100K 5% 1/20W MF 201
R4054 232K 1% 1/20W MF 201
R4055 100K 5% 1/20W MF 201

P3V3WLAN_VMON
AP_RESET_CONN_L
AP_CLKREQ_O_L

AP_RESET_L
AP_PWR_EN
AP_CLKREQ_L

SYNC MASTER=K16 MLB
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PAGE TITLE
X21 WIRELESS CONNECTOR

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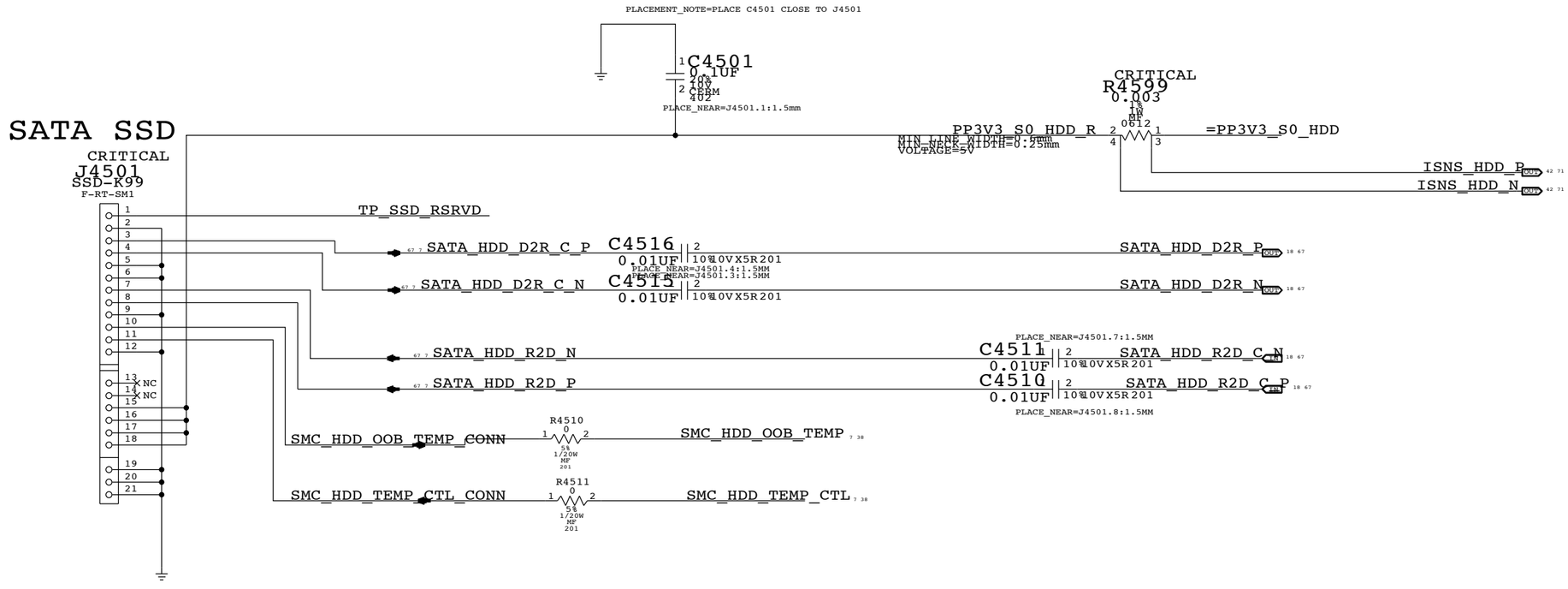

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PAGE TITLE

SATA CONNECTOR

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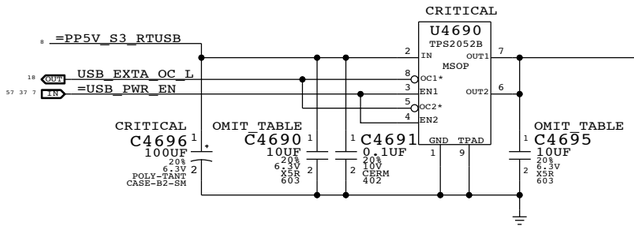
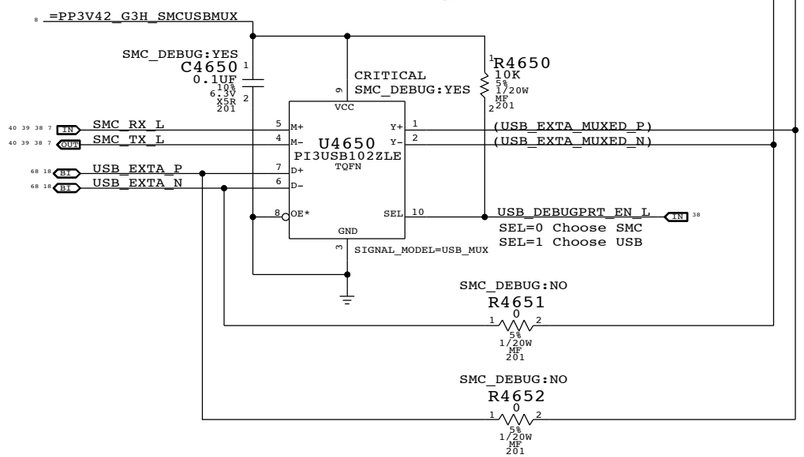
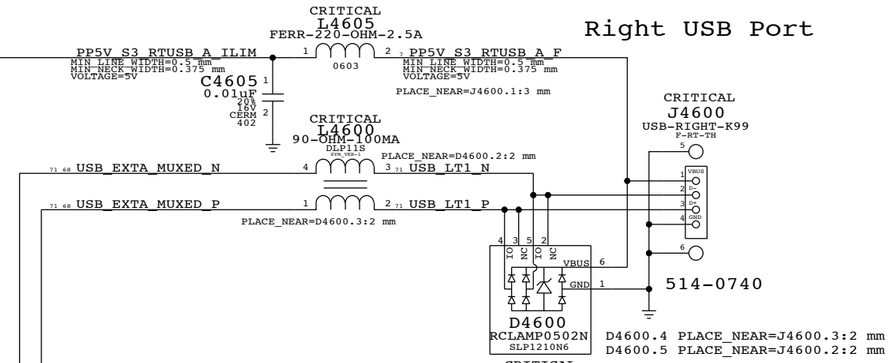
Port Power Switch



USB/SMC Debug Mux



Right USB Port



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
External USB Connectors

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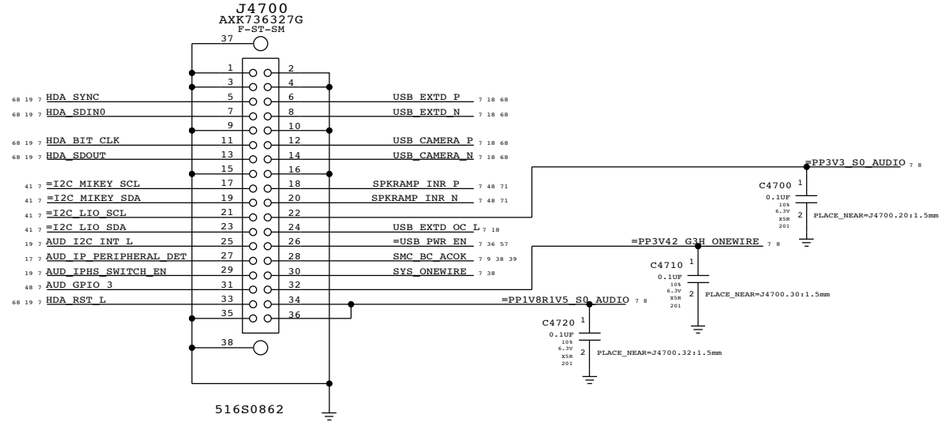
LIO CONNECTOR



SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE

LIO CONNECTORS

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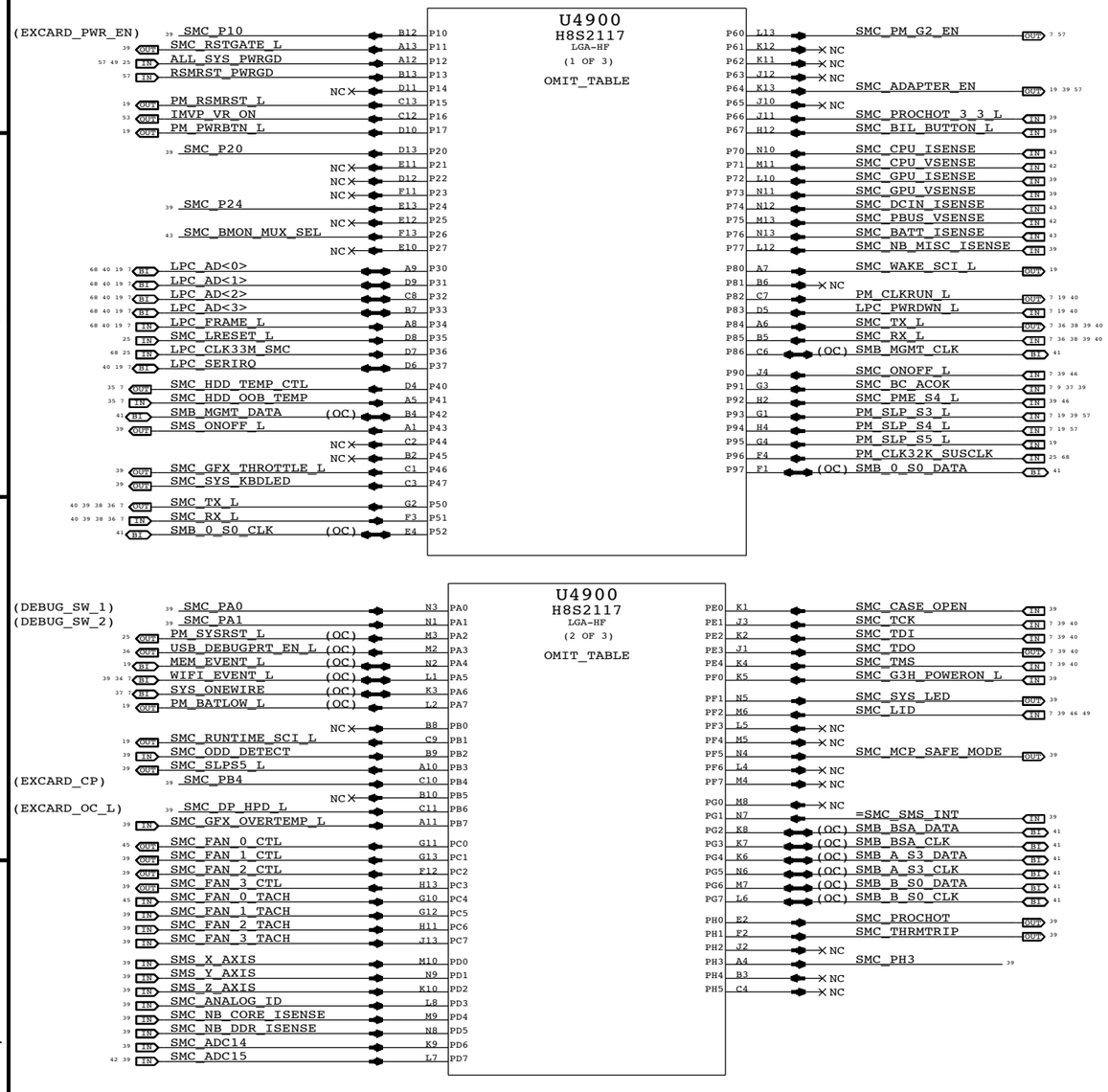
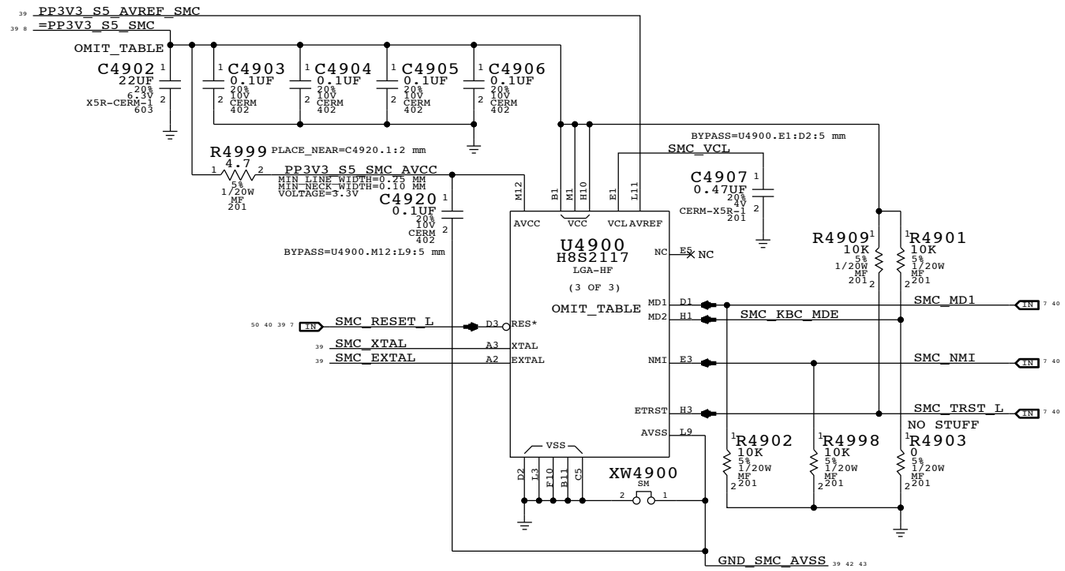
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

H8S2117-R:
(SMC_PECI)
(SMC_PECI_VREF)
(SMC_PECI_VSTP)

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
SMC

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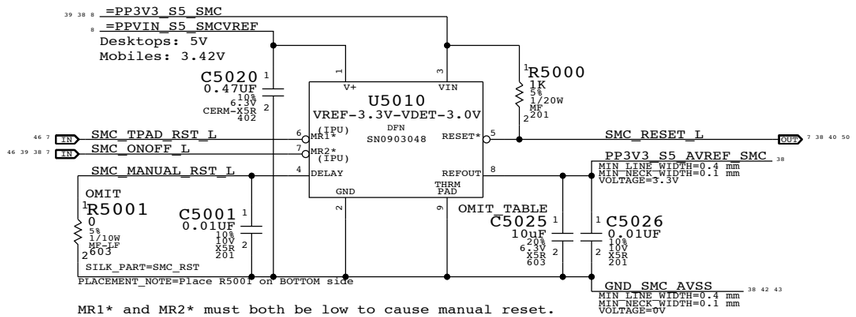
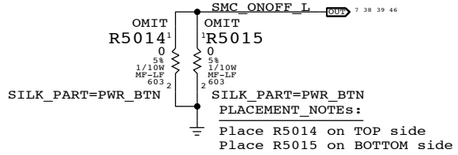
SMC Reset "Button", Supervisor & AVREF Supply



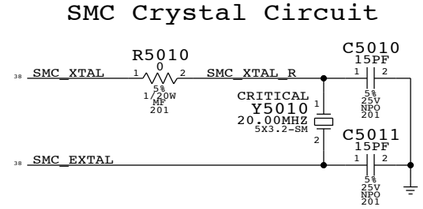
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

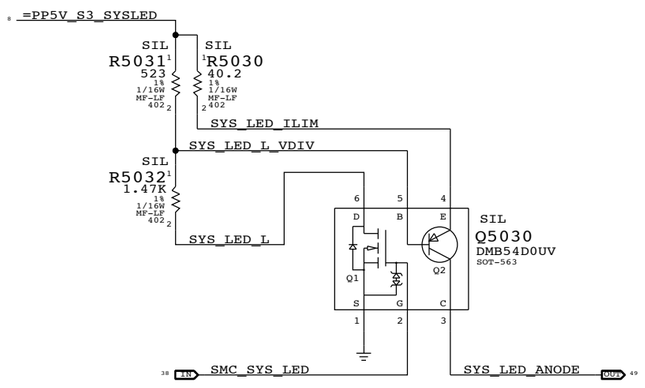
Debug Power "Buttons"



SMC Crystal Circuit



System (Sleep) LED Circuit



SMC Aliases

SMC_LCDBKLT_ISENSE	SMS_X_AXIS	
SMC_WLAN_ISENSE	SMS_Y_AXIS	
SMC_HDD_ISENSE	SMS_Z_AXIS	
SMC_CSREG_ISENSE	SMC_ADC14	
SMC_LCDBKLT_VSENSE	SMC_ADC15	
SMC_MCP_CORE_ISENSE	SMC_NB_CORE_ISENSE	
SMC_MCP_DDR_ISENSE	SMC_NB_DDR_ISENSE	
SMC_1V5S3_ISENSE	SMC_NB_MISC_ISENSE	
TP_SMC_ANALOG_ID	SMC_ANALOG_ID	
TP_SMC_GPU_ISENSE	SMC_GPU_ISENSE	
SMC_MCP_VSENSE	SMC_GPU_VSENSE	
SMC_GFX_THROTTLE_L	SMC_IG_THROTTLE_L	
SMS_INT_L	=SMC_SMS_INT	
MCP_WAKE_REQ_L	SMC_G3H_POWERON_L	

MAKE_BASE=TRUE; NO_TEST=TRUE

R5096 0 5% 1/20W MF 201: SMC_MCP_SAFE_MODE — MCP_SPKR

DP_PWR:S0 R5020 0 5% 1/20W MF 201: PM_SLP_S3_L — DP_PWR_EN =DP_PWR_EN

DP_PWR:SMC R5021 0 5% 1/20W MF 201: SMC_SLPS5_L

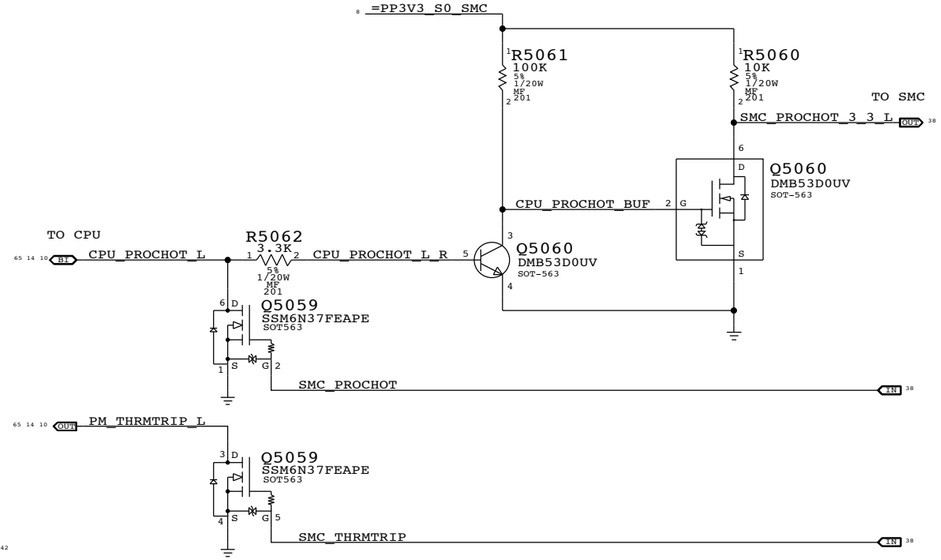
DP_PWR:SMC R5022 0 5% 1/20W MF 201: SMC_DP_HPD_L — DP_EXT_HPD_L, PLACE_NEAR=Q9441.2:5 mm

Unused Pins

SMS_ONOFF_L	TP_SMS_ONOFF_L
SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED
SMC_FAN_1_CTL	TP_SMC_FAN_1_CTL
TP_SMC_FAN_1_TACH	SMC_FAN_1_TACH
SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL
NC_SMC_FAN_2_TACH	SMC_FAN_2_TACH
SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL
NC_SMC_FAN_3_TACH	SMC_FAN_3_TACH
SMC_RSTGATE_L	TP_SMC_RSTGATE_L
SMC_P10	TP_SMC_P10
SMC_P20	TP_SMC_P20
SMC_P24	TP_SMC_P24
SMC_PH3	TP_SMC_PH3

MAKE_BASE=TRUE; NO_TEST=TRUE

SMC FSB to 3.3V Level Shifting



SMC Pull-ups

SMC_PA0	R5091	100K	5% 1/20W MF 201
SMC_PA1	R5092	100K	5% 1/20W MF 201
SMC_PB4	R5088	10K	5% 1/20W MF 201
SMC_ONOFF_L	R5070	10K	5% 1/20W MF 201
SMC_LID	R5071	100K	5% 1/20W MF 201
SMC_TX_L	R5073	10K	5% 1/20W MF 201
SMC_RX_L	R5074	100K	5% 1/20W MF 201
SMC_TMS	R5077	10K	5% 1/20W MF 201
SMC_TDO	R5078	10K	5% 1/20W MF 201
SMC_TDI	R5079	10K	5% 1/20W MF 201
SMC_TCK	R5080	10K	5% 1/20W MF 201
SMC_ODD_DETECT	R5040	10K	5% 1/20W MF 201
SMC_BIL_BUTTON_L	R5081	10K	5% 1/20W MF 201
SMC_BC_ACOK	R5087	470K	5% 1/20W MF 201
SMC_GFX_OVERTEMP_L	R5094	10K	5% 1/20W MF 201
SMC_G3H_POWERON_L	R5098	100K	5% 1/20W MF 201
SMS_INT_L	R5093	10K	5% 1/20W MF 201

=PP3V3_S5_SMC

PP3V3_WLAN_F

WIFI_EVENT_L — R5089 10K, NO STUFF, 5% 1/20W MF 201

=PP3V3_SMC_PME

SMC_PME_S4_L — R5076 100K 5% 1/20W MF 201

SMC Pull-downs

SMC_ADAPTER_EN	R5085	10K	5% 1/20W MF 201
SMC_CASE_OPEN	R5086	10K	5% 1/20W MF 201
SMC_DP_HPD_L	R5090	100K	DP_PWR:S0, 5% 1/20W MF 201

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: SMC Support

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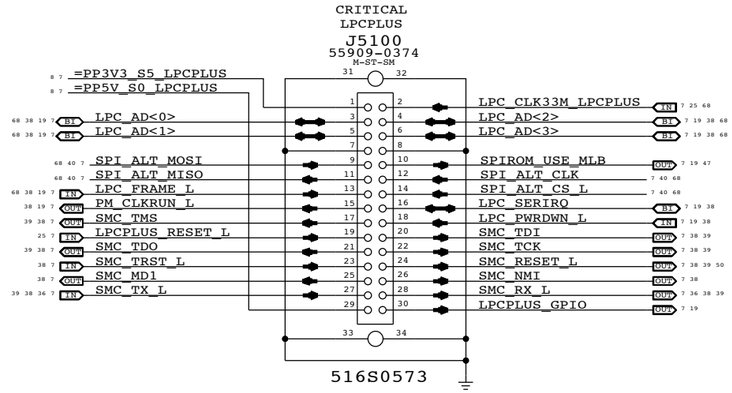
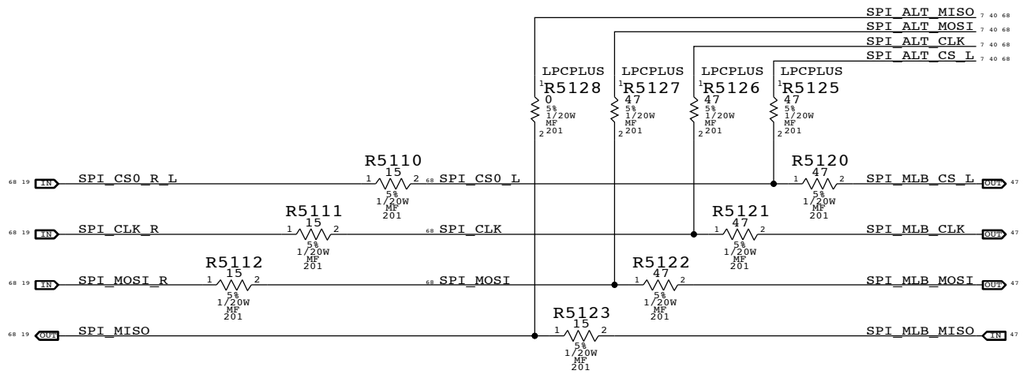
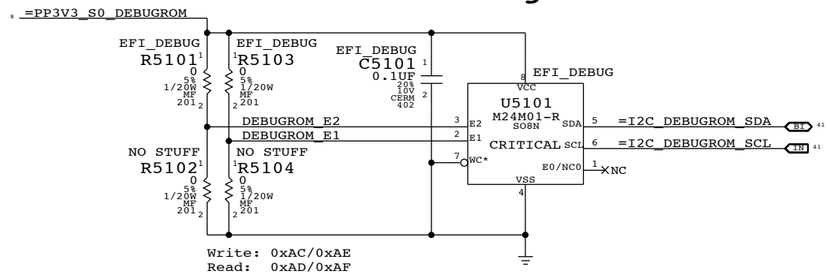
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE
LPC+SPI Debug Connector

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MCP89 SMBus "0" Connections

=PP3V3_S0_SMBUS_MCP_0

MCP89
U1400
(MASTER)

SMBUS_MCP_0_CLK (MAKE_BASE=TRUE)
SMBUS_MCP_0_DATA (MAKE_BASE=TRUE)

R5200 1K 5% 1/20W MF 201
R5201 1K 5% 1/20W MF 201

LP8545 (Bklt)
U9701
(Write: 0x58 Read: 0x59)

=I2C_BKL_1_SCL
=I2C_BKL_1_SDA

DPI2C:MCP
R5241 0 5% 1/20W MF 201

XDP Connector
J1300
(MASTER)

=I2C_XDP_SCL
=I2C_XDP_SDA

DPI2C:MCP
R5240 0 5% 1/20W MF 201

Vref DACs
U3900
(Write: 0x98 Read: 0x99)

=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA

Margin Control
U3910
(Write: 0x30 Read: 0x31)

=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA

EFI Debug Serial
U5101
(Write: 0xAC/0xAE
Read: 0xAD/0xAF)

=I2C_DEBUGROM_SCL
=I2C_DEBUGROM_SDA

Mikey
J4700 (LIO Connector)
(Write: 0x72 Read: 0x73)

=I2C_MIKEY_SCL
=I2C_MIKEY_SDA

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

SMC
U4900
(MASTER)

SMB_0_S0_CLK
SMB_0_S0_DATA

NO STUFF R5250 2.0K 5% 1/20W MF 201
NO STUFF R5251 2.0K 5% 1/20W MF 201

SMBUS_SMC_0_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_0_S0_SDA (MAKE_BASE=TRUE)

DPI2C:SMC
R5242 0 5% 1/20W MF 201

DPI2C:SMC
R5243 0 5% 1/20W MF 201

Internal DP
J9000
(See Table)

I2C_TCON_SCL (MAKE_BASE=TRUE)
I2C_TCON_SDA (MAKE_BASE=TRUE)

=I2C_TCON_SCL
=I2C_TCON_SDA

Internal DP

Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)
Parade T-con - (0x10-0x1F or 0x30-0x3F)
DVR - (Write: 0x4E Read: 0x4F)

(* = Multiple options)

K16		K99		
Samsung	LGD	Samsung	LGD	AUO
N	Y	*	Y	*
Y	N	*	N	*
Y	Y	Y	Y	N

SMC "Battery A" SMBus Connections

=PP3V42_G3H_SMBUS_SMC_BSA

SMC
U4900
(MASTER)

SMB_BSA_CLK
SMB_BSA_DATA

R5280 2.61K 1% 1/20W MF 201
R5281 2.61K 1% 1/20W MF 201

SMBUS_SMC_BSA_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_BSA_SDA (MAKE_BASE=TRUE)

Battery Charger
ISL6259 - U7000
(Write: 0x12 Read: 0x13)

=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA

Battery
J6950
(See Table)

=SMBUS_BATT_SCL
=SMBUS_BATT_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

=PP3V3_S5_SMBUS_SMC_MGMT

SMC
U4900
(MASTER)

SMB_MGMT_CLK
SMB_MGMT_DATA

R5290 2.0K 5% 1/20W MF 201
R5291 2.0K 5% 1/20W MF 201

SMBUS_SMC_MGMT_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_MGMT_SDA (MAKE_BASE=TRUE)

Trackpad
J5700
(Write: 0x90 Read: 0x91)

=I2C_TPAD_SCL
=I2C_TPAD_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_A_S3

SMC
U4900
(MASTER)

SMB_A_S3_CLK
SMB_A_S3_DATA

R5270 1K 5% 1/20W MF 201
R5271 1K 5% 1/20W MF 201

SMBUS_SMC_A_S3_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_A_S3_SDA (MAKE_BASE=TRUE)

Left I/O Board
J4700
(See Table)

=I2C_LIO_SCL
=I2C_LIO_SDA

Left I/O Board

ALS - N/A (Feature Removed)
Finstack Temp - (Write: 0x98 Read: 0x99)

MCP89 SMBus "1" Connections

=PP3V3_S0_SMBUS_MCP_1

MCP89
U1400
(Write: 0xE0 Read: 0xE1)

SMBUS_MCP_1_CLK (MAKE_BASE=TRUE)
SMBUS_MCP_1_DATA (MAKE_BASE=TRUE)

NO STUFF R5230 2.0K 5% 1/20W MF 201
NO STUFF R5231 2.0K 5% 1/20W MF 201

R5235 0 5% 1/20W MF 201
R5236 0 5% 1/20W MF 201

MCP89 SMBus 1 is slave port to access internal thermal diodes.

Another slave port is available at 0x10/0x11, probably not used.

SMC "B" SMBus Connections

=PP3V3_S0_SMBUS_SMC_B_S0

SMC
U4900
(MASTER)

SMB_B_S0_CLK
SMB_B_S0_DATA

R5260 4.7K 5% 1/20W MF 201
R5261 4.7K 5% 1/20W MF 201

SMBUS_SMC_B_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_B_S0_SDA (MAKE_BASE=TRUE)

CPU Temp
EMC1413: U5515
(Write: 0x98 Read: 0x99)

=I2C_CPUTHMSNS_SCL
=I2C_CPUTHMSNS_SDA

MCP Temp
EMC1413: U5535
(Write: 0xD8 Read: 0xD9)

=I2C_MCPTHMSNS_SCL
=I2C_MCPTHMSNS_SDA

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
K16/K99 SMus Connections

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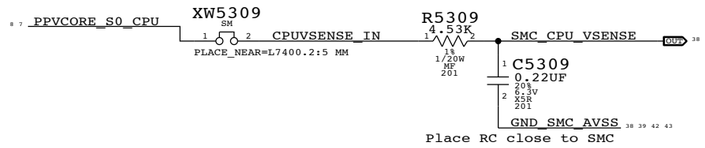
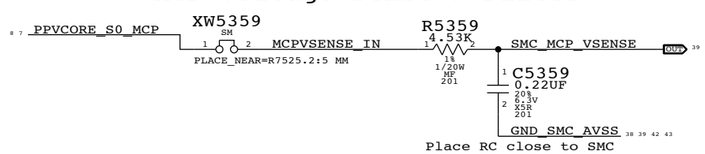
CPU Voltage Sense / Filter



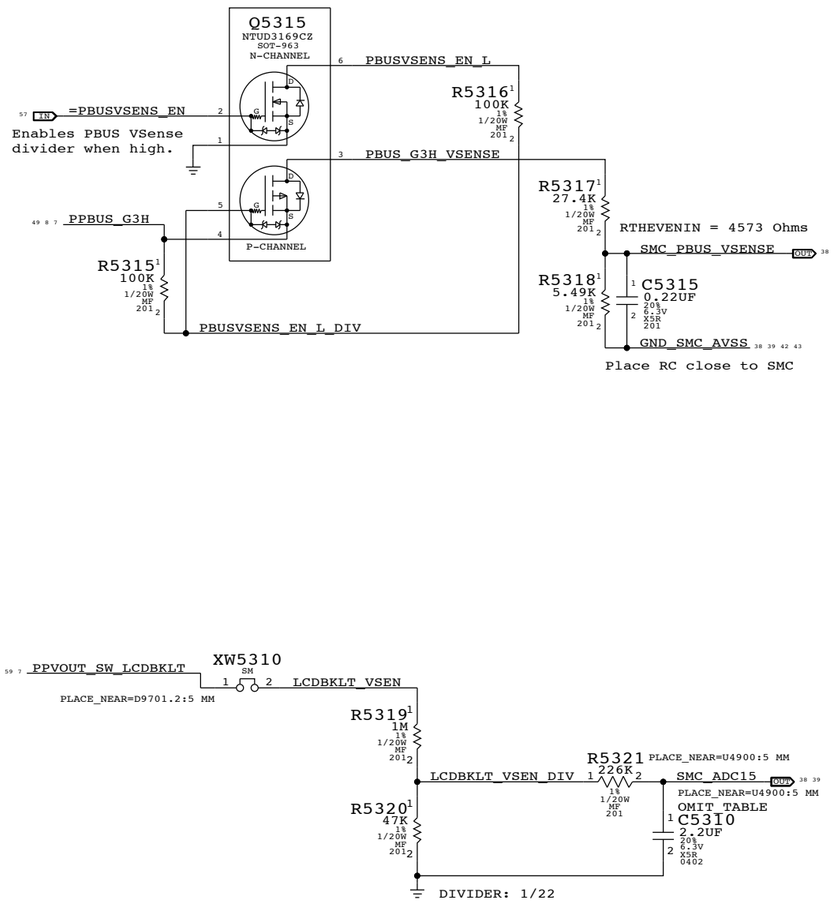
Place RC close to SMC

MCP Voltage Sense / Filter



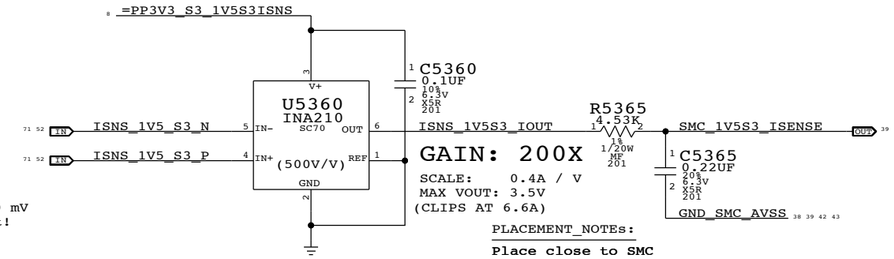
Place RC close to SMC

PBUS Voltage Sense Enable & Filter



Place RC close to SMC

DDR3 1V5R1V35 Current Sense / Filter



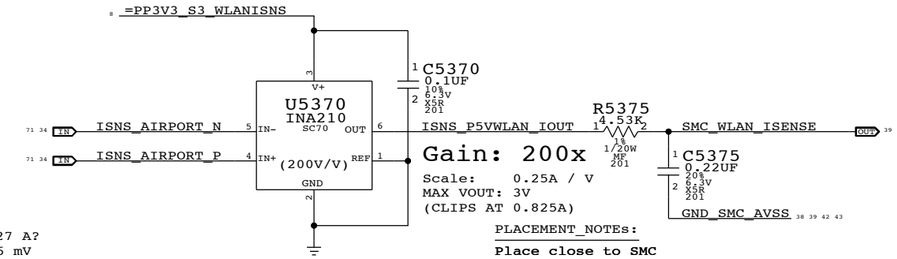
GAIN: 200X

SCALE: 0.4A / V
MAX VOUT: 3.5V
(CLIPS AT 6.6A)

EDP Current: 7 A
Max Vdiff: 13.0 mV
WF: Verify SO-DIMM current!

PLACEMENT_NOTES:
Place close to SMC
(For R and C)

AirPort Current Sense / Filter



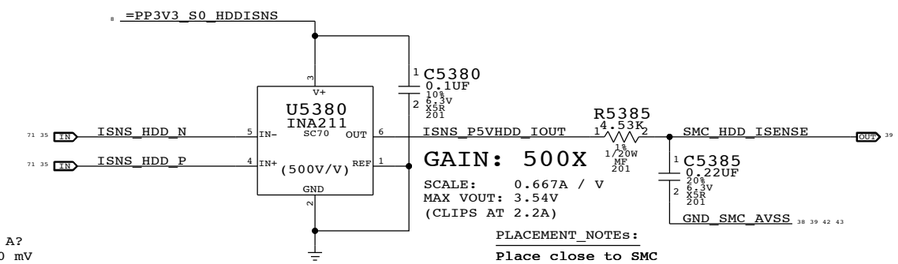
Gain: 200x

Scale: 0.25A / V
MAX VOUT: 3V
(CLIPS AT 0.825A)

EDP Current: 0.727 A?
Max Vdiff: 14.6 mV
WF: Verify Airport current!

PLACEMENT_NOTES:
Place close to SMC
(For R and C)

HDD Current Sense / Filter



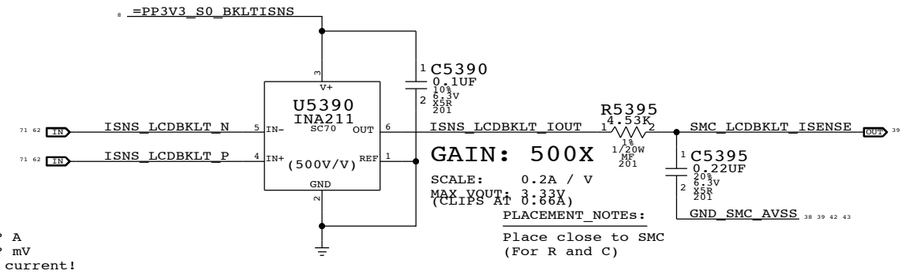
GAIN: 500X

SCALE: 0.667A / V
MAX VOUT: 3.54V
(CLIPS AT 2.2A)

EDP Current: 1.2 A?
Max Vdiff: 24.0 mV
WF: Verify SSD current!

PLACEMENT_NOTES:
Place close to SMC
(For R and C)

LCD Backlight Driver Input Current Sense / Filter



GAIN: 500X

SCALE: 0.2A / V
MAX VOUT: 3.33V
(CLIPS AT 0.66A)

EDP Current: ??? A
Max Vdiff: ??? mV
WF: Verify LCD backlight current!

PLACEMENT_NOTES:
Place close to SMC
(For R and C)

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
Voltage & Current Sensing

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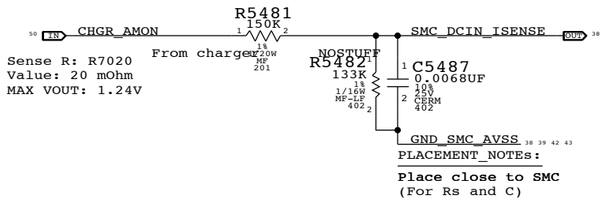
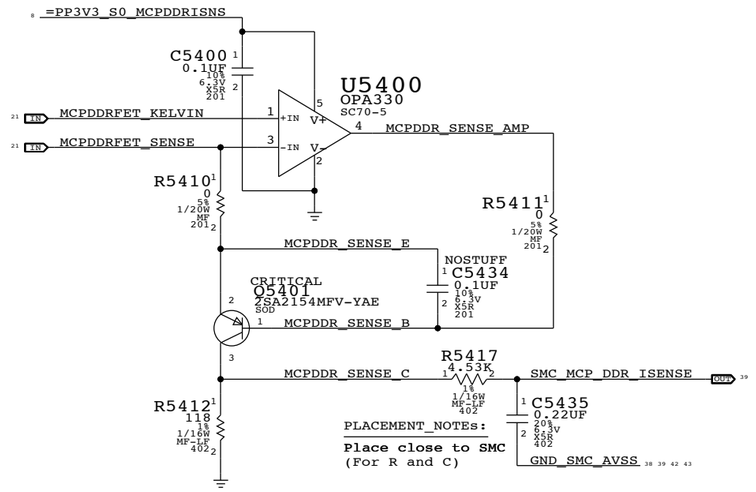
DCIN (AMON) Current Sense, RMUX & Filter

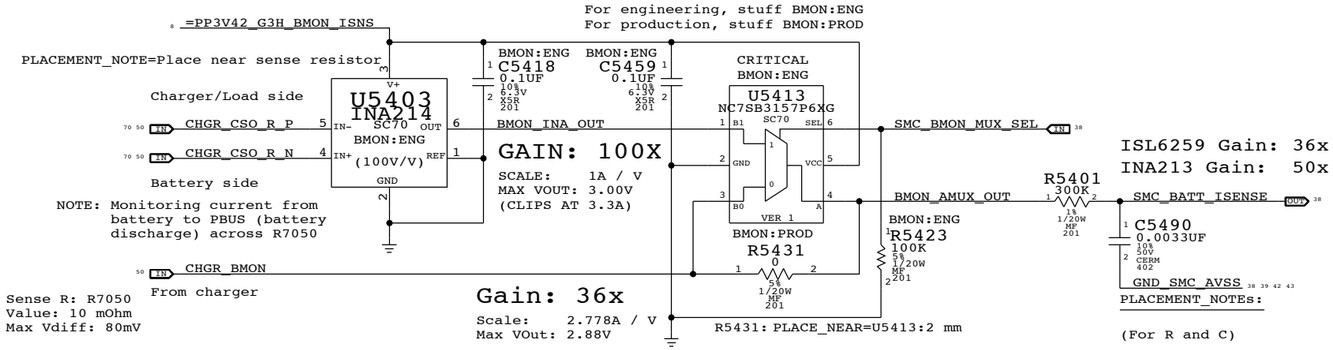
ISL6259 Gain: 20x



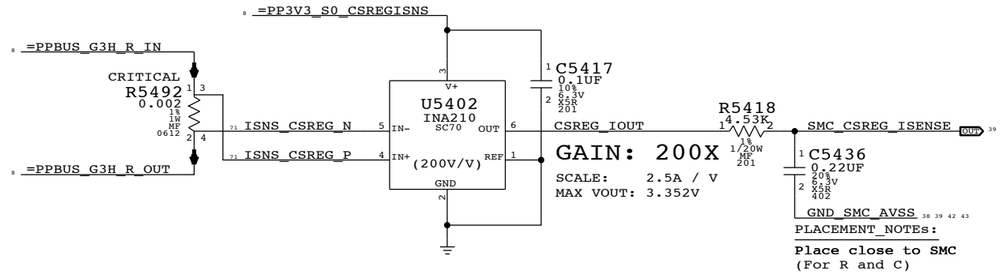
MCP MEM VDD Current Sense / Filter



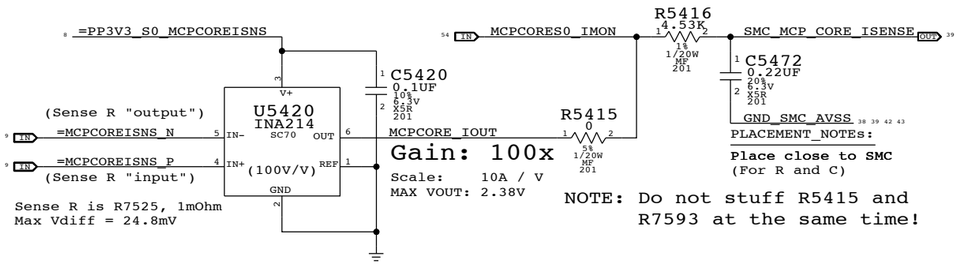
Battery (BMON) Current Sense, MUX & Filter



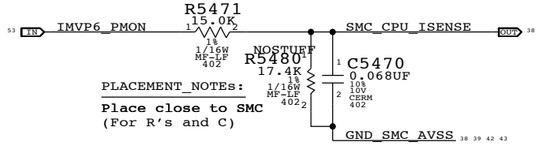
Chipset Regulators High-Side Current Sense / Filter



MCP VCore Current Sense Filter



CPU VCore Load Side Current Sense / Filter



VERIFY ALL RESISTOR AND GAINS

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: Current Sensing

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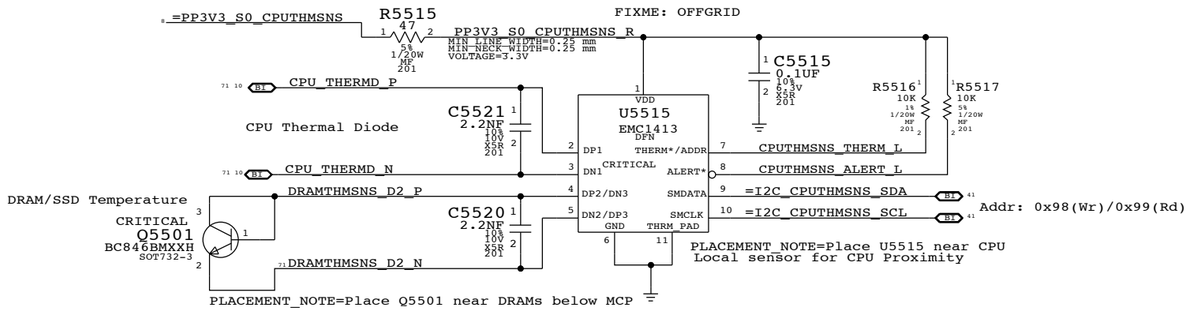
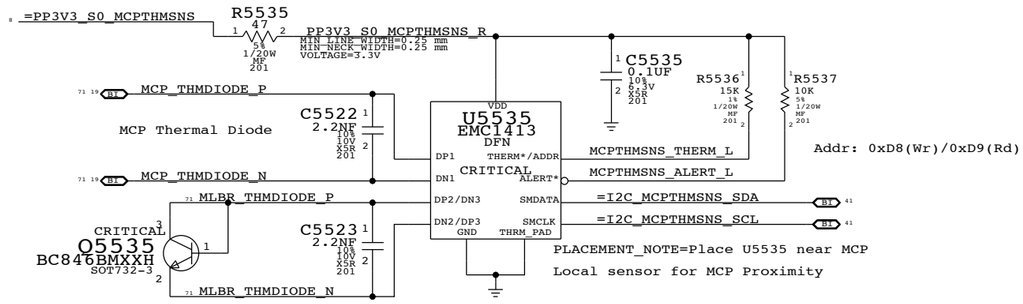
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

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Thermal Sensors

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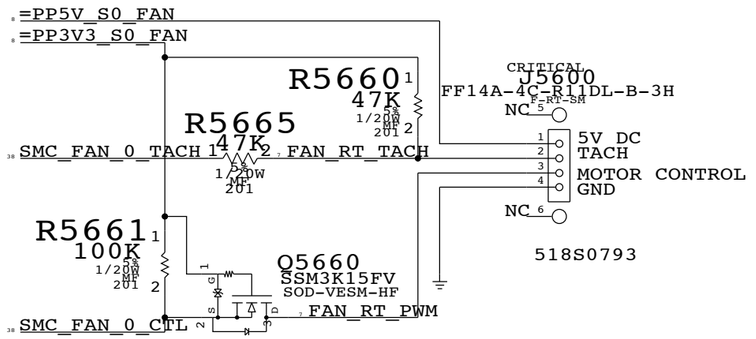
FAN CONNECTOR



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: Fan

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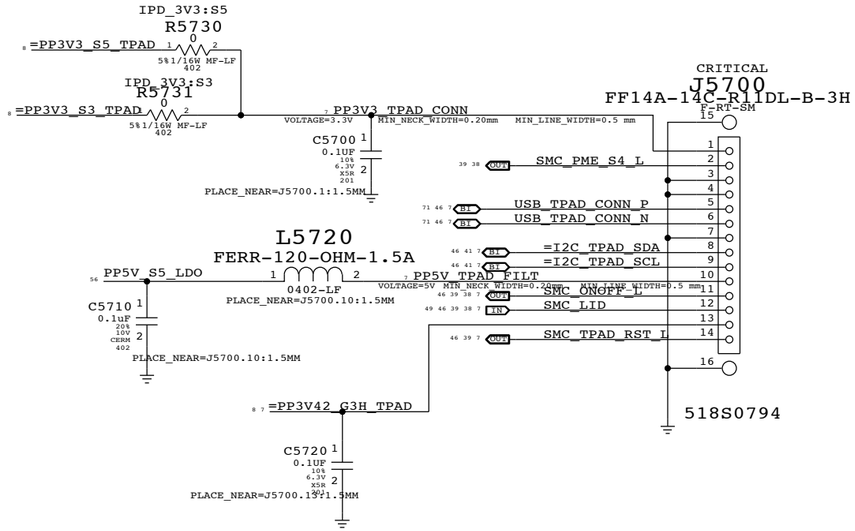
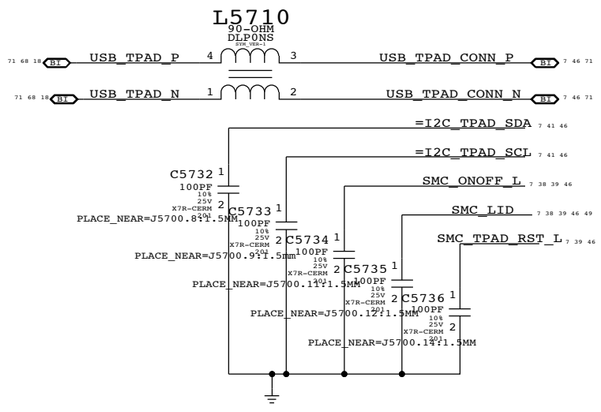
IPD Flex Connector





SYNC MASTER=K16 MLB	SYNC DATE=07/07/2010
PAGE TITLE: WELLSPRING 1	
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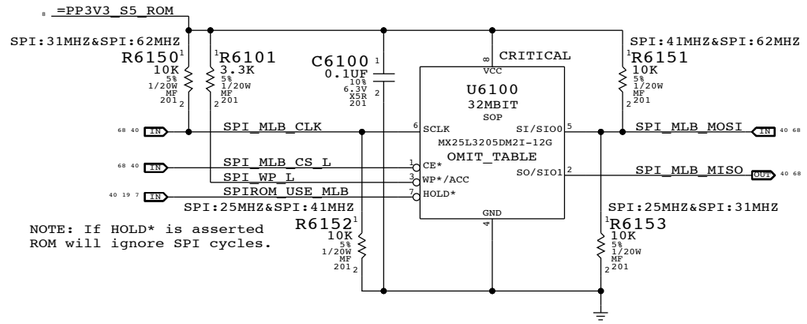

MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command.

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

BRANCH

PAGE 61 OF 110

SHEET 47 OF 73

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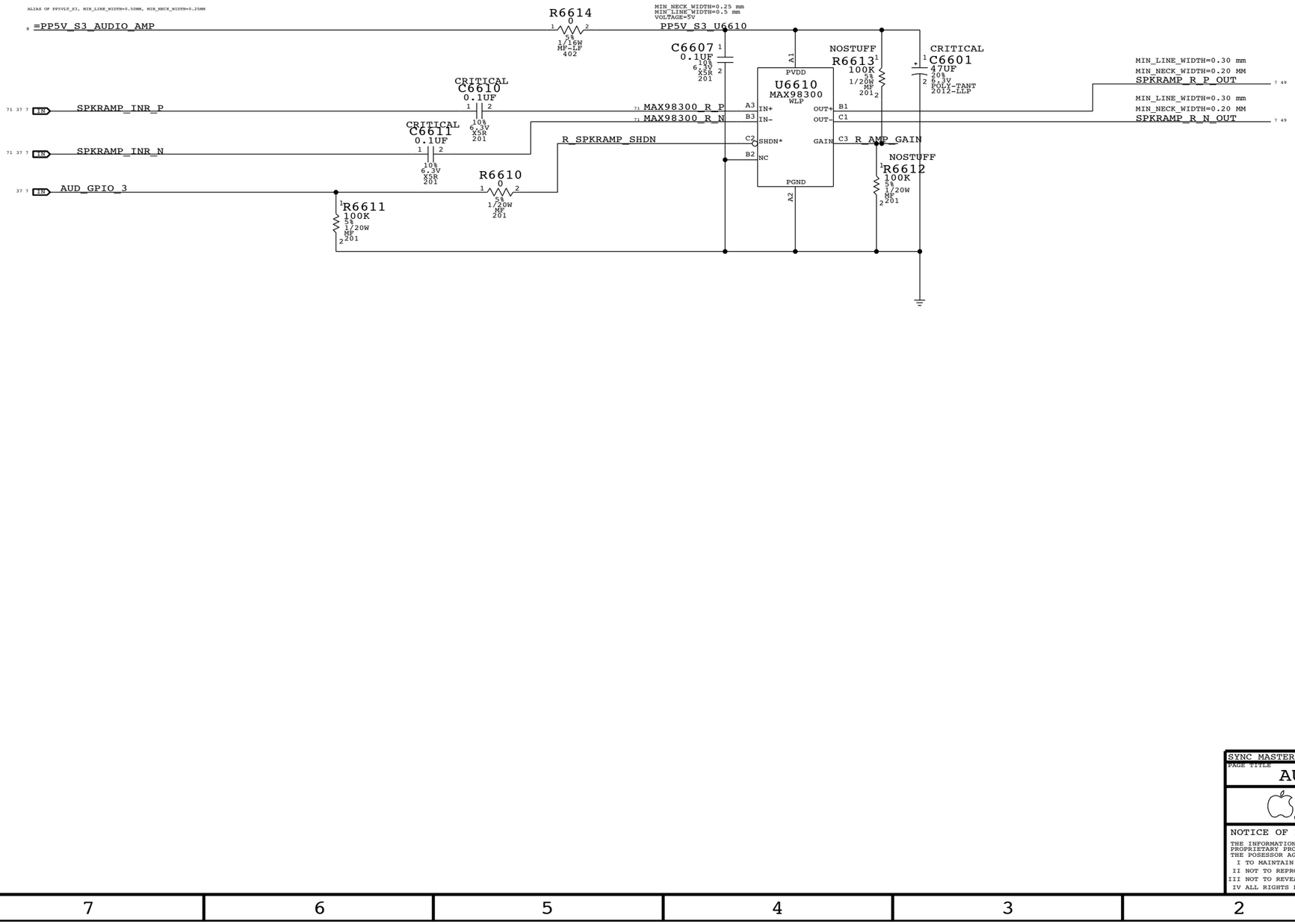
SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB



SYNC MASTER=AUDIO SYNC DATE=02/09/2010

PAGE TITLE

AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

BRANCH

PAGE 66 OF 110

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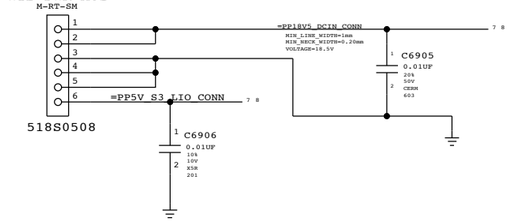
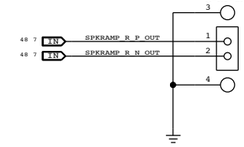
MLB TO LIO POWER CABLE CONNECTOR

J6900
WTB-PWR-M82
M-RT-SM

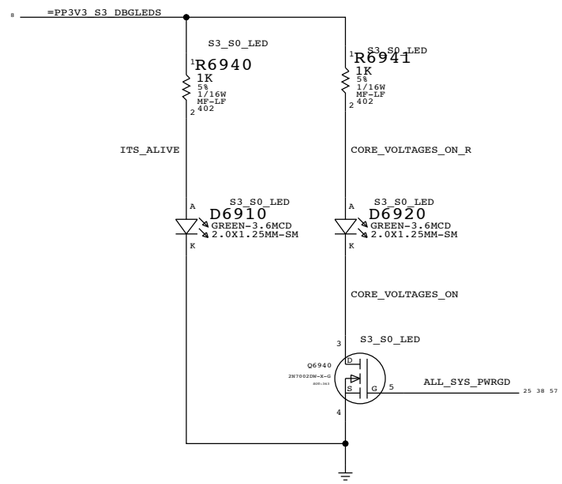


518S0508

APN:518S0519
CRITICAL
J6903
78171-0002
M-RT-SM



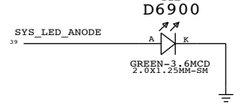
SPKR



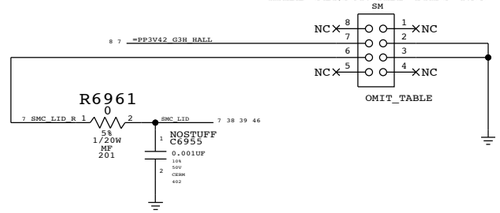
S3 AND S0 INDICATOR LEDS FOR DEVELOPMENT ONLY

SIL ON MLB FOR DEVELOPMENT ONLY

SIL
D6900



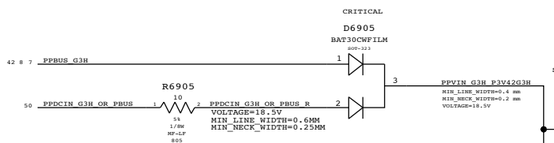
998-3029
J6955
HALL-SENSOR-MLB-PADS-K99
SM



OMIT_TABLE

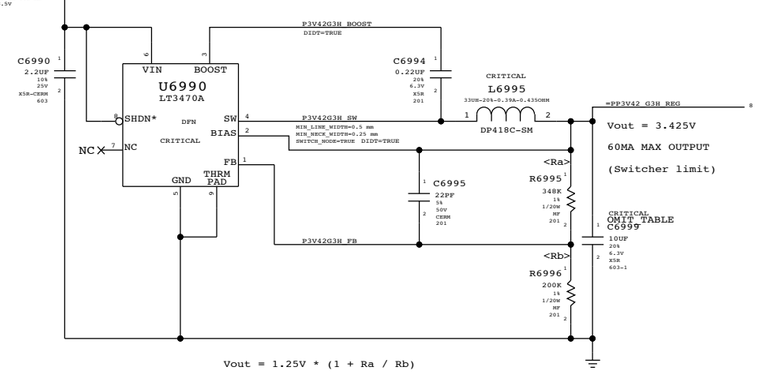
HALL EFFECT PADS

CRITICAL
D6905
BAT30CWFILM



3.425V "G3Hot" Supply

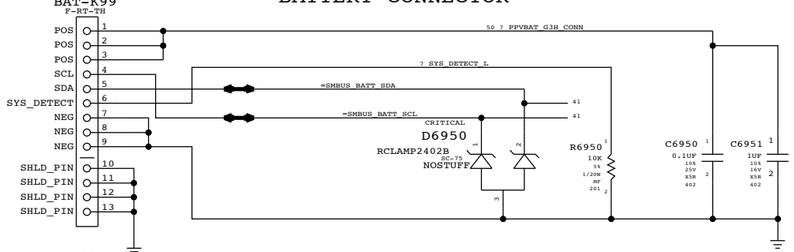
Supply needs to guarantee 3.31V delivered to SMC VRef generator



Vout = 1.25V * (1 + Ra / Rb)

BATTERY CONNECTOR

CRITICAL
J6950
BAT-K99
F-RT-TH



518-0369

SYNC_MASTER=K84_MLB	SYNC_DATE=11/09/2009
PAGE TITLE	DC-In & Battery Connectors
Apple Inc.	DRAWING NUMBER 051-8379 SIZE D
	REVISION 4.4.0
	BRANCH
	PAGE 69 OF 110
	SHEET 49 OF 73

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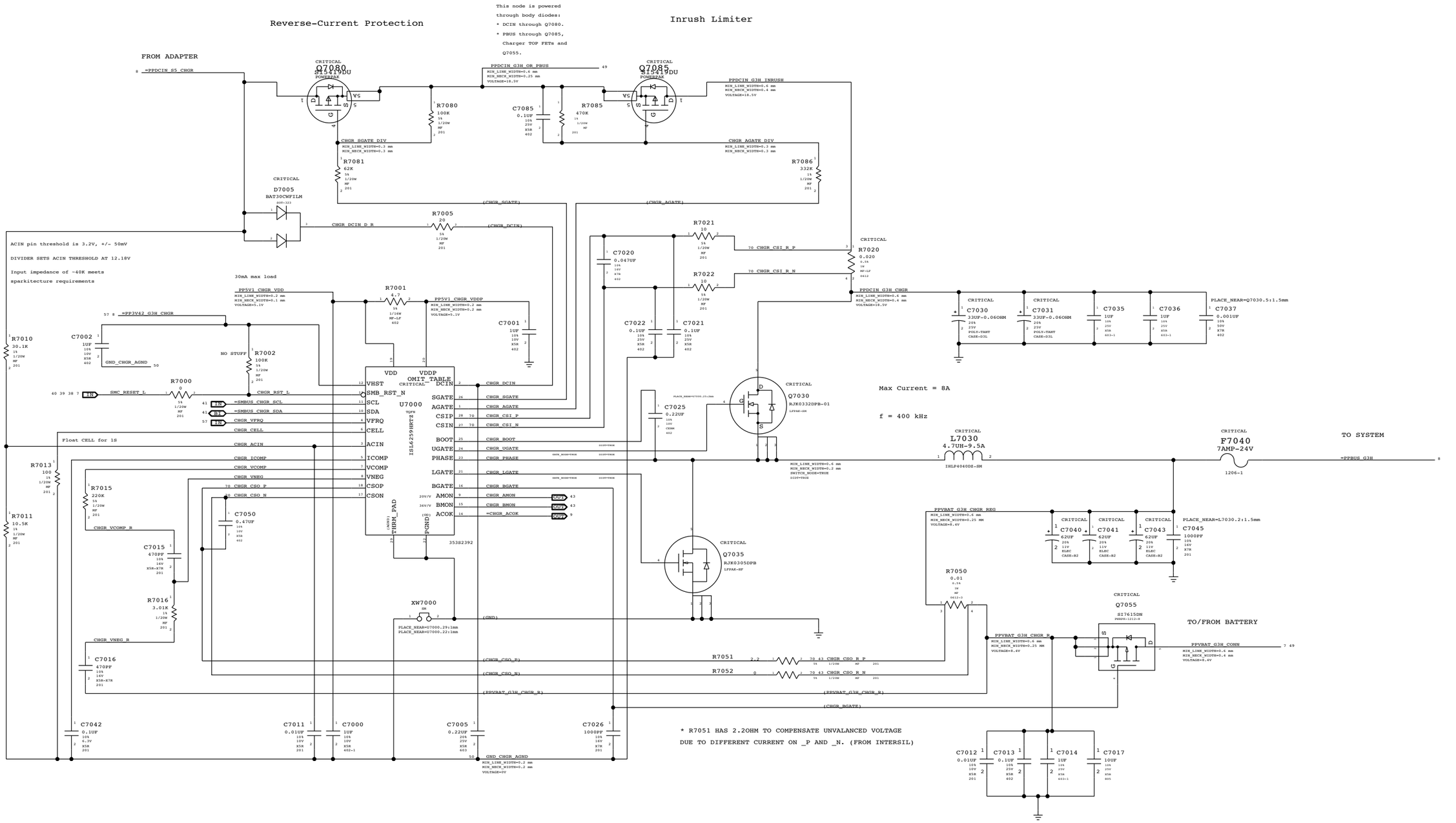

SYNC MASTER=K6 MLB
SYNC DATE=11/09/2009

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-8379
SIZE D
REVISION 4.4.0
BRANCH
PAGE 70 OF 110
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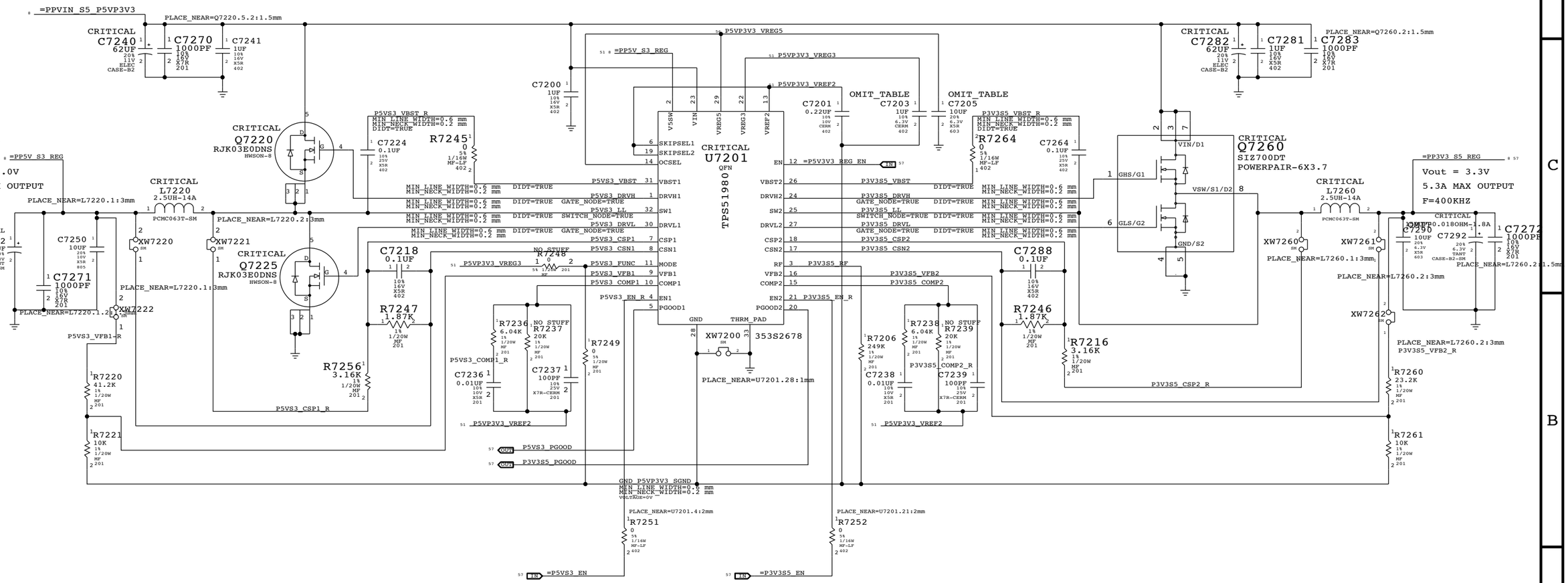

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE
5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D
REVISION 4.4.0
BRANCH
PAGE 72 OF 110
SHEET 51 OF 73

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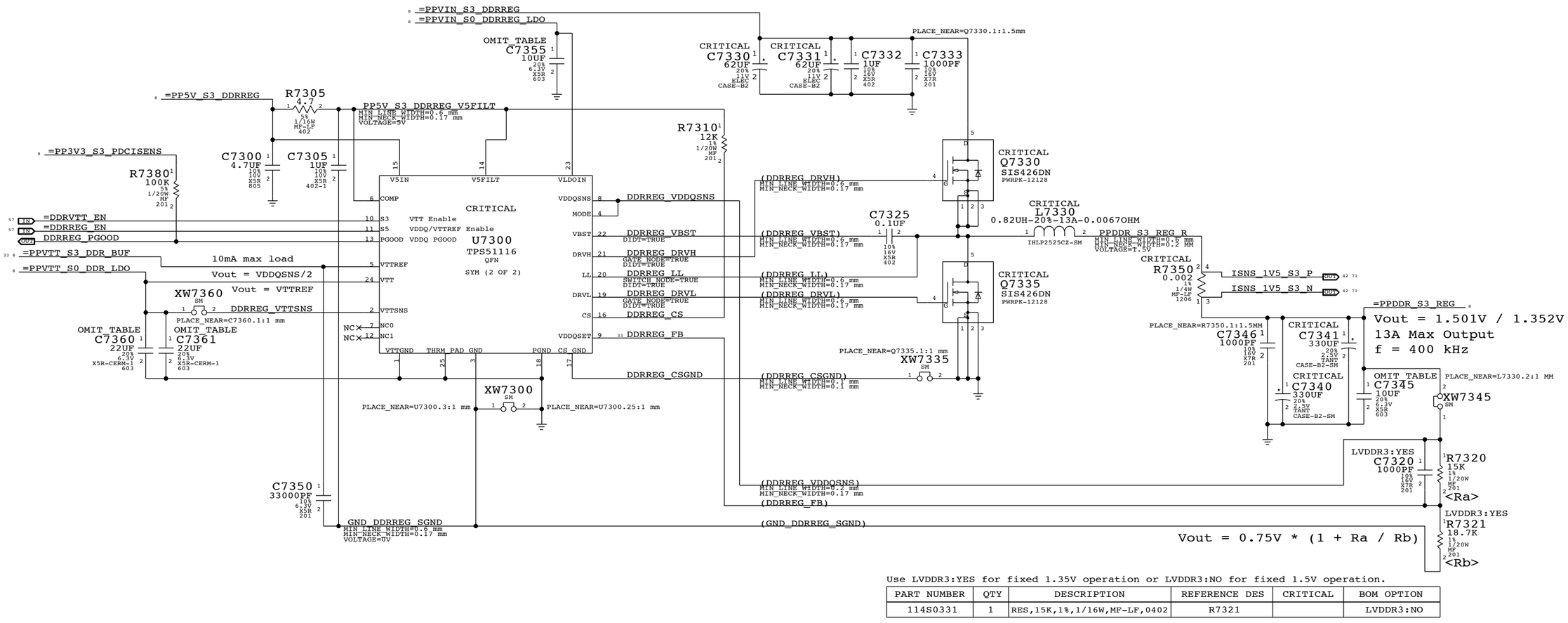

Use LVDDR3:YES for fixed 1.35V operation or LVDDR3:NO for fixed 1.5V operation.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0331	1	RES,15K,1%,1/16W,MF-LF,0402	R7321		LVDDR3:NO

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE
1.5V/1.35V LVDDR3 Supply

Apple Inc.

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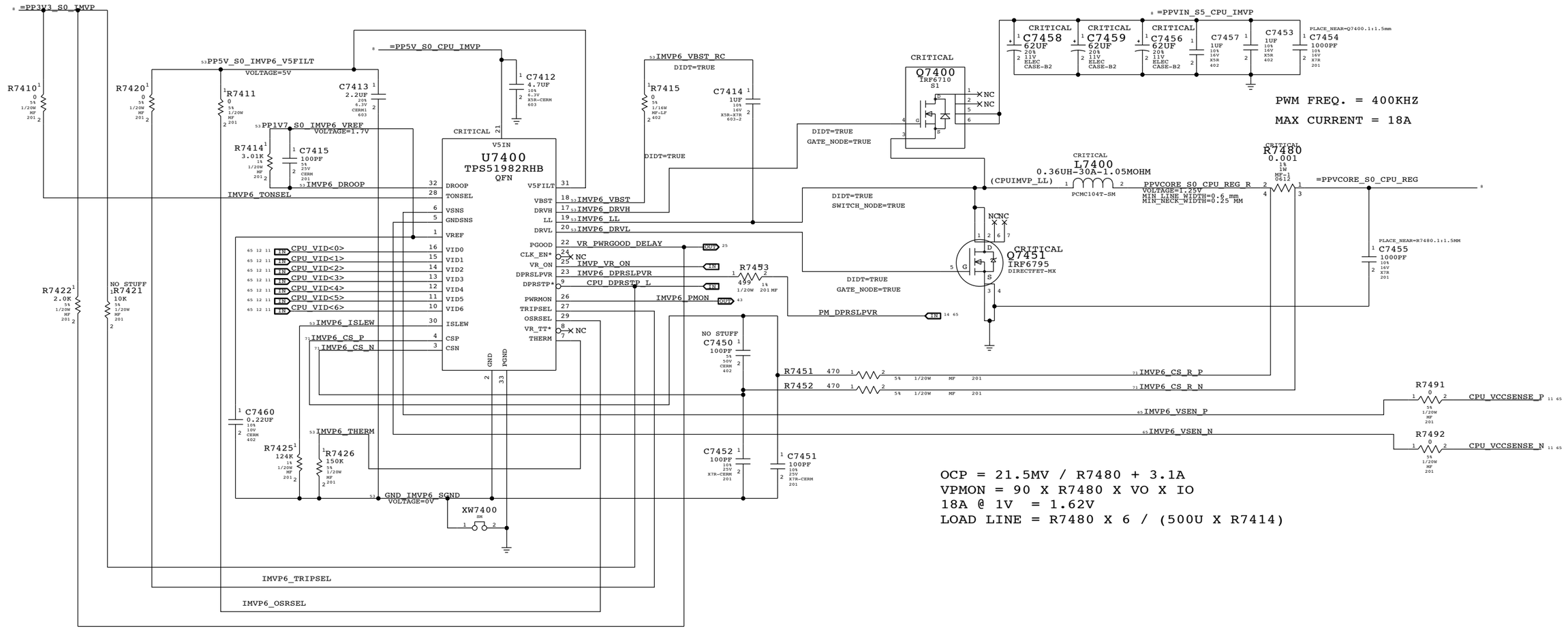
IMVP6 CPU VCORE REGULATOR



	MIN_LINE_WIDTH	MIN_NECK_WIDTH
53 IMVP6_LL	1.5 MM	0.20 MM
53 IMVP6_VBST	0.25 MM	0.20 MM
53 IMVP6_DRVH	1.5 MM	0.20 MM
53 IMVP6_DRVL	1.5 MM	0.20 MM
53 IMVP6_VBST_RC	1.5 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
53 GND_IMVP6_SGND	0.50 MM	0.20 MM
53 IMVP6_DROOP	0.25 MM	0.20 MM
53 IMVP6_THERM	0.25 MM	0.20 MM
53 IMVP6_ISLEW	0.25 MM	0.20 MM
53 PP1V7_S0_IMVP6_VREF	0.25 MM	0.20 MM
53 PP5V_S0_IMVP6_V5FILT	0.25 MM	0.20 MM

SYNC MASTER=POWER SYNC DATE=07/13/2005

PAGE TITLE: IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

BRANCH:

PAGE: 74 OF 110

SHEET: 53 OF 73

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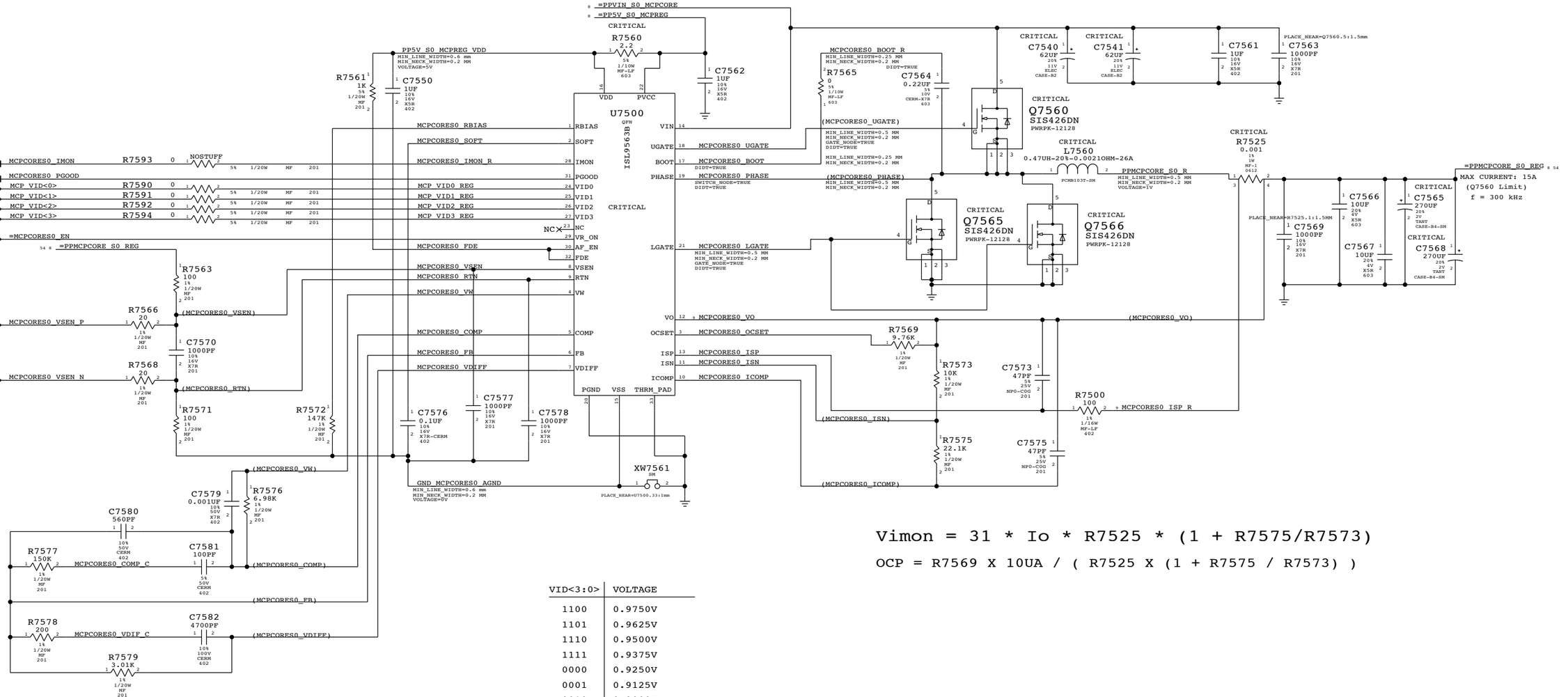

VID<3:0>	VOLTAGE
1100	0.9750V
1101	0.9625V
1110	0.9500V
1111	0.9375V
0000	0.9250V
0001	0.9125V
0010	0.9000V
0011	0.8875V
0100	0.8750V
0101	0.8625V
0110	0.8500V
0111	0.8375V
1000	0.8250V
1001	0.8125V
1010	0.8000V
1011	0.7875V

Vimon = 31 * Io * R7525 * (1 + R7575/R7573)

OCP = R7569 X 10UA / (R7525 X (1 + R7575 / R7573))

K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE: MCP VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

BRANCH:

PAGE: 75 OF 110

SHEET: 54 OF 73

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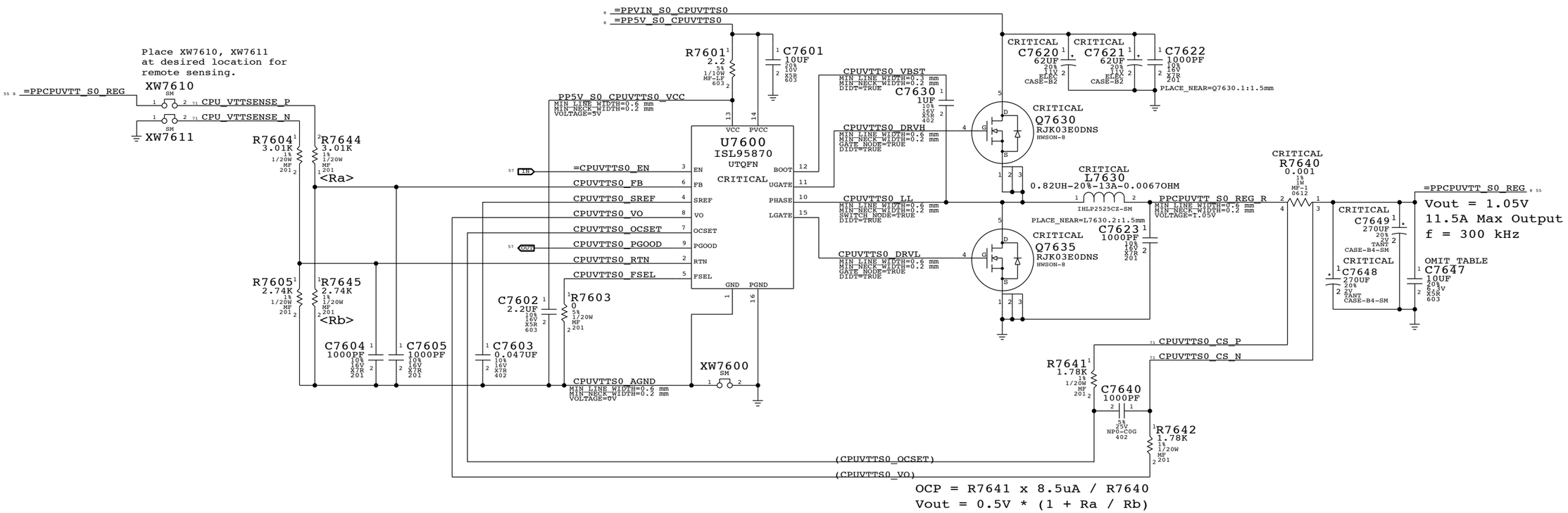

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE
CPUVTT (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D
REVISION 4.4.0
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SHEET 55 OF 73

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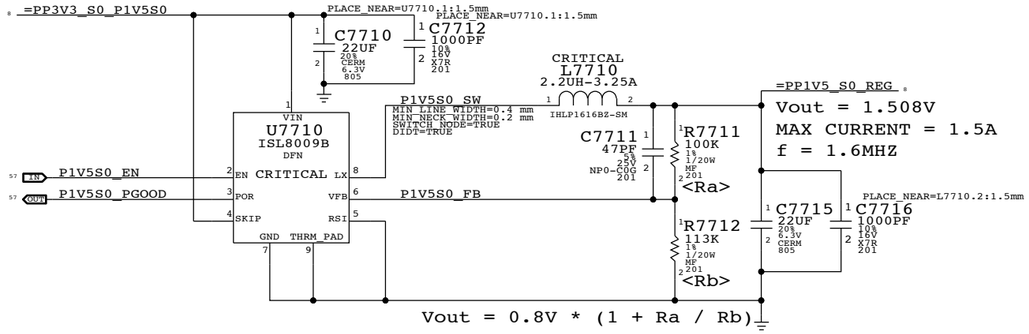
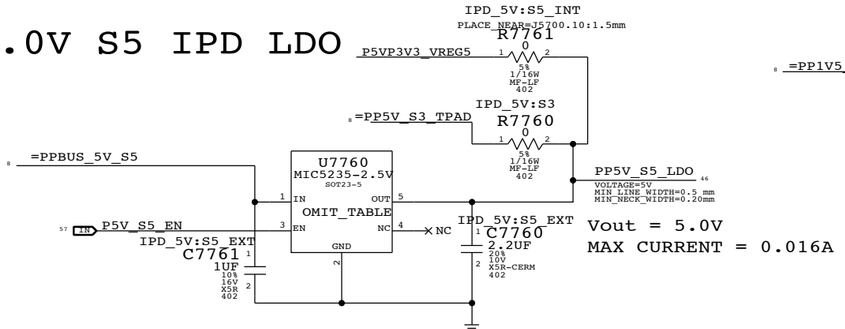
1.5V S0 Regulator

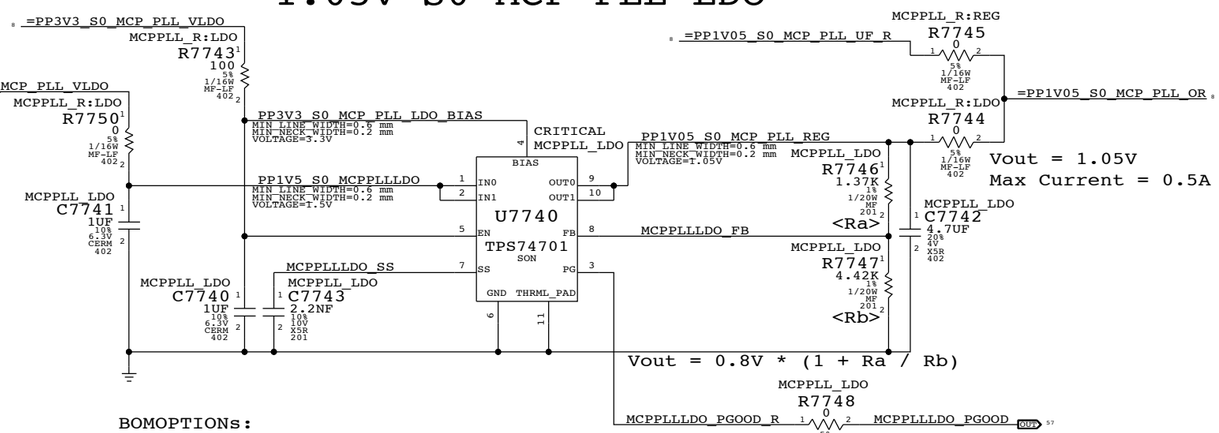


5.0V S5 IPD LDO



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3034	1	IC,LDO,MIC5235,5V,1%,150MA,SOT23-5	U7760		IPD_5V:S5_EXT

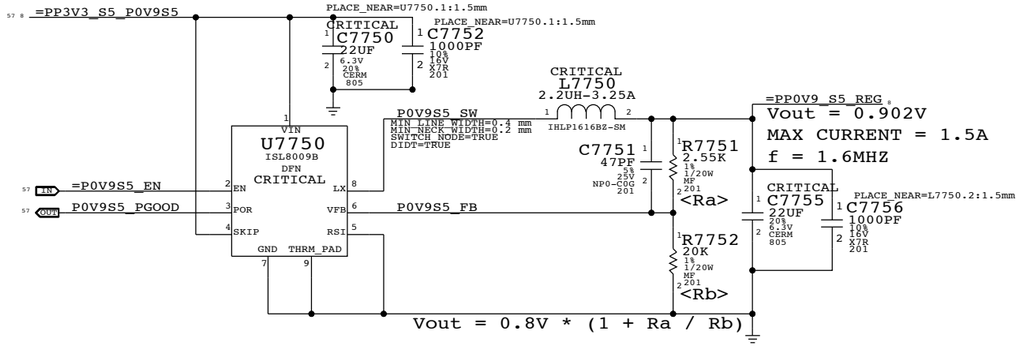
1.05V S0 MCP PLL LDO



BOMOPTIONs:

MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.

MCP 0.9V S5 (AUXC) Switcher



SYNC MASTER=K16 MLB	SYNC DATE=07/07/2010
PAGE TITLE: Misc Power Supplies	
Apple Inc.	DRAWING NUMBER 051-8379 SIZE D
	REVISION 4.4.0
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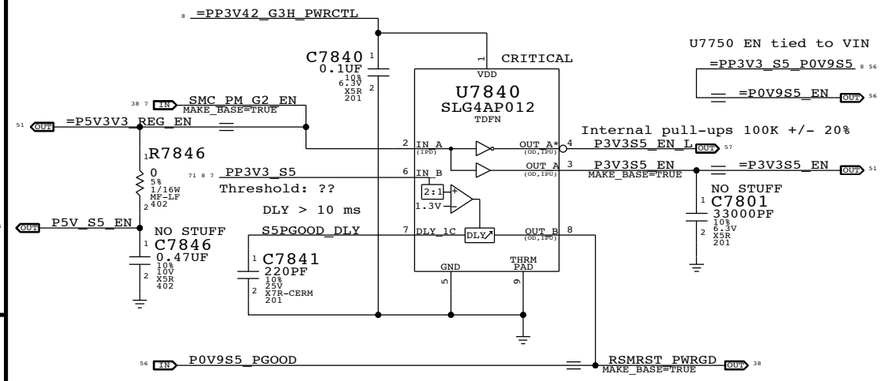
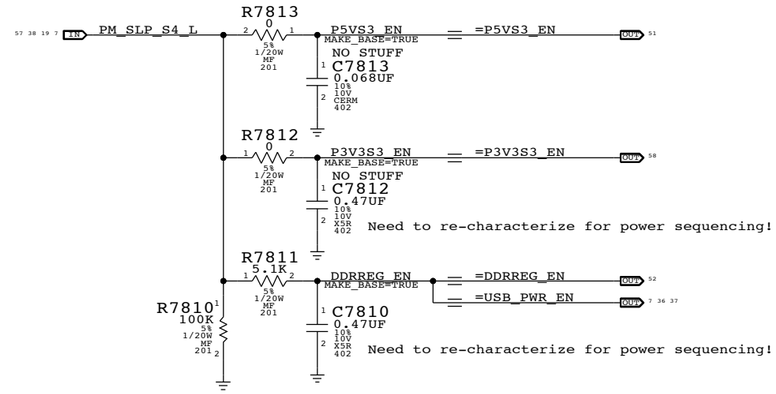
S5 Rail Enables & PGOOD

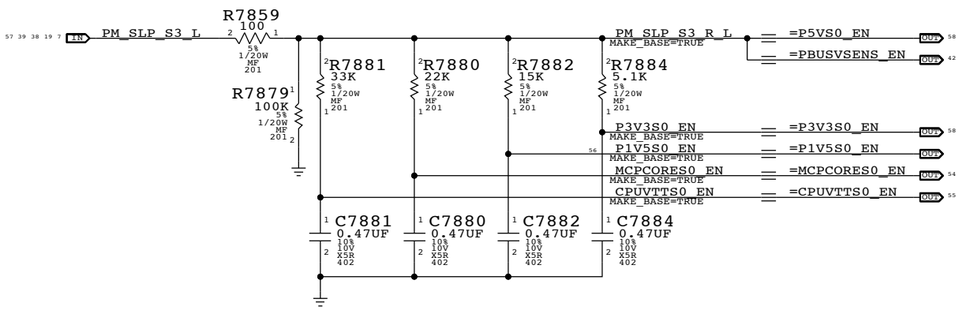


S3 Rail Enables



ENET Rail Enables

S0 Rail Enables

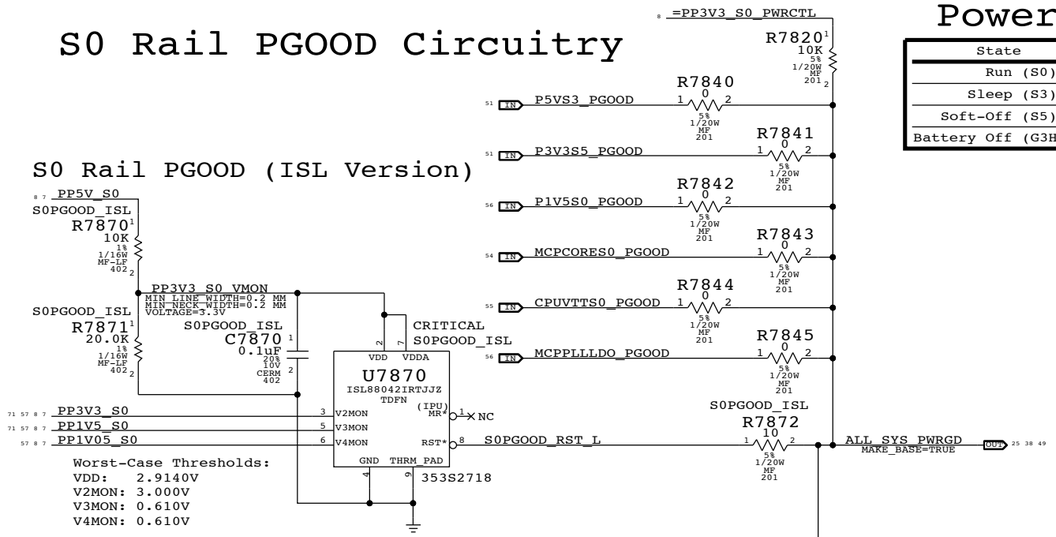


VTT Rail Enable

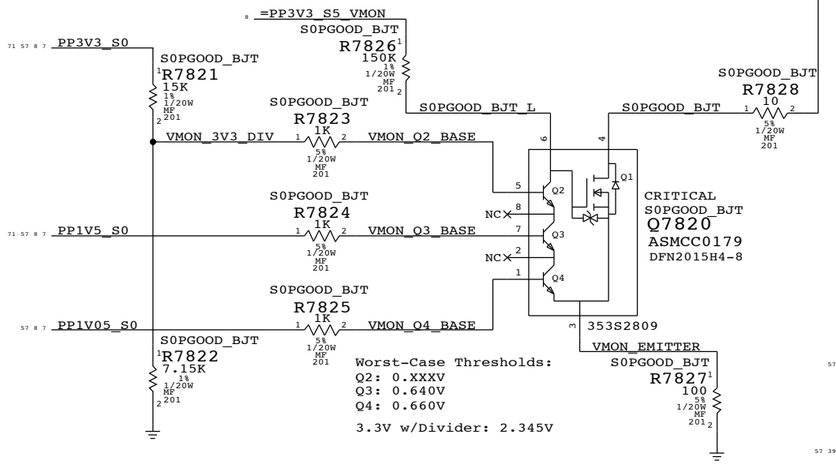
VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).

S0 Rail PGOOD Circuitry

S0 Rail PGOOD (ISL Version)



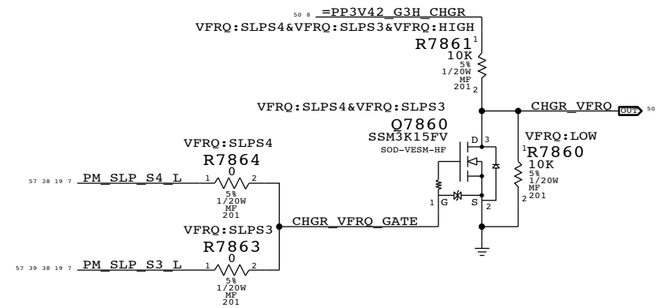
S0 Rail PGOOD (BJT Version)



Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

ISL6259 Frequency Select

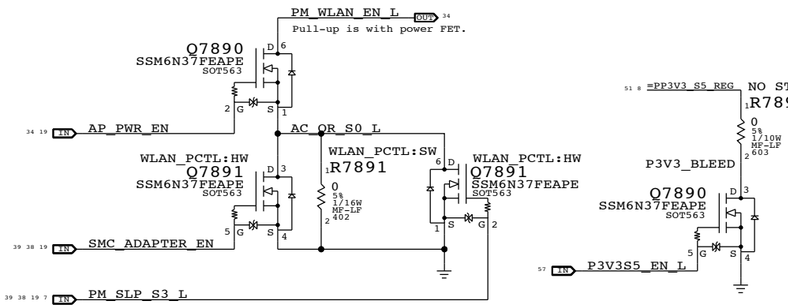


WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

NOTE: "AC" term valid only when Q7891 is stuffed



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: Power Sequencing

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

BRANCH:

PAGE: 78 OF 110

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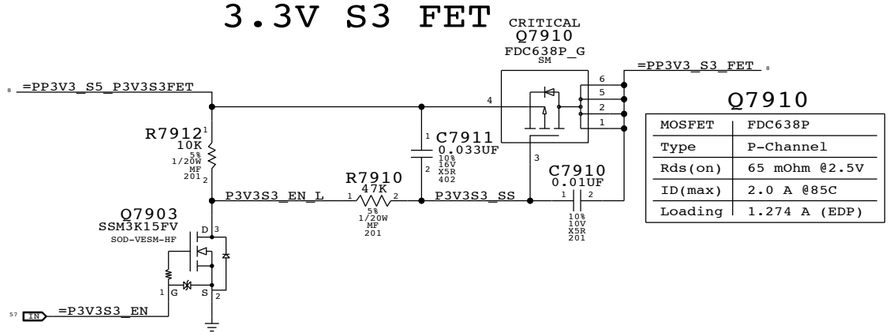
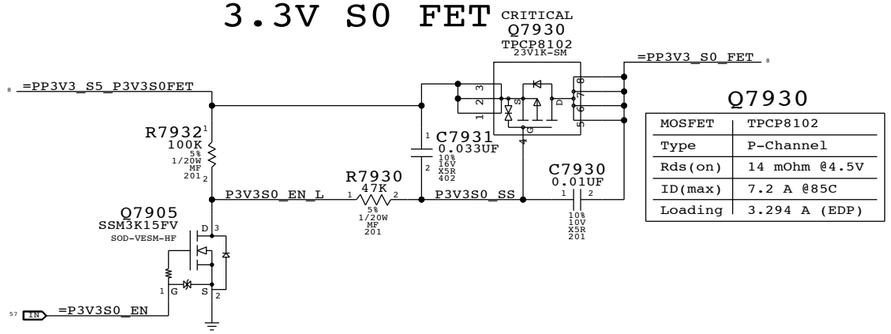
3.3V S3 FET



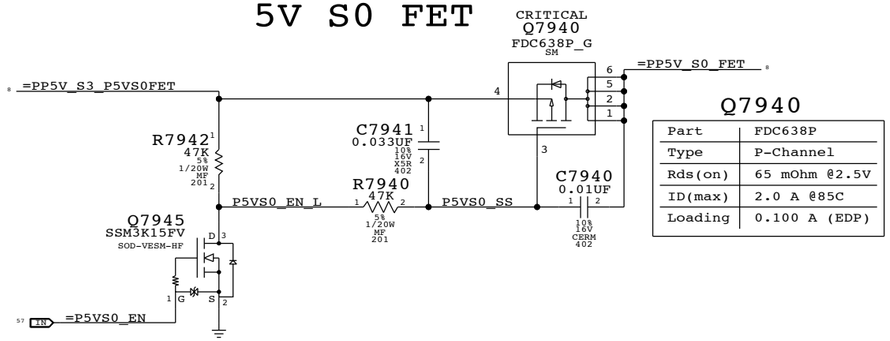
Q7910	
MOSFET	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	1.274 A (EDP)

3.3V S0 FET



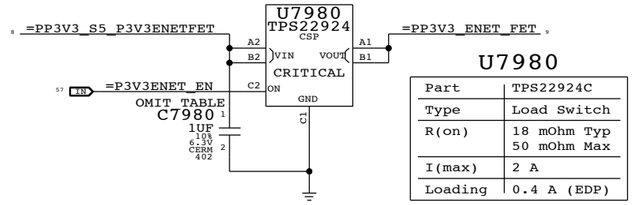
Q7930	
MOSFET	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
ID(max)	7.2 A @85C
Loading	3.294 A (EDP)

5V S0 FET



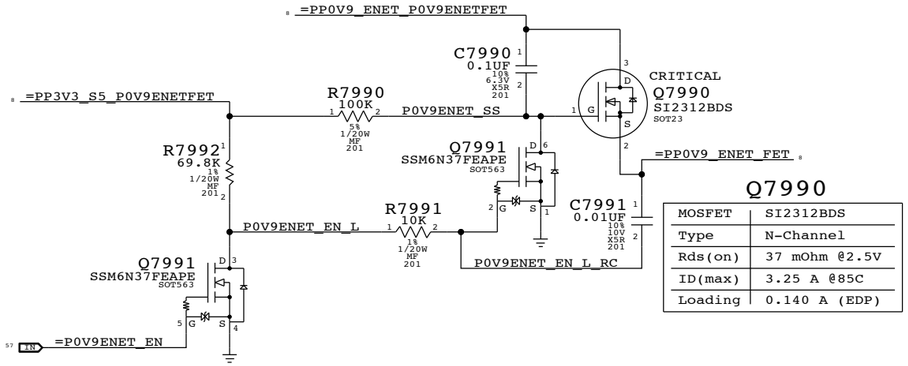
Q7940	
Part	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	0.100 A (EDP)

3.3V ENET Switch



U7980	
Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max
I(max)	2 A
Loading	0.4 A (EDP)

0.9V ENET FET



Q7990	
MOSFET	SI2312BDS
Type	N-Channel
Rds(on)	37 mOhm @2.5V
ID(max)	3.25 A @85C
Loading	0.140 A (EDP)

SYNC MASTER=K16_MLB SYNC DATE=07/07/2010

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

BRANCH:

PAGE: 79 OF 110

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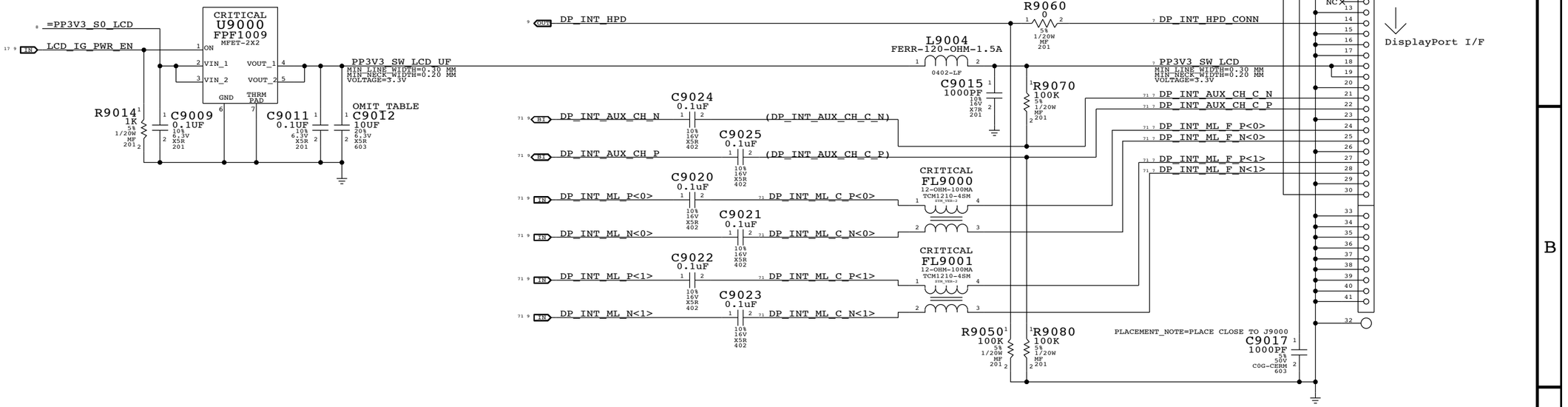
LCD Connector

Internal DP Connector: 518S0787

CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

Pull-ups on panel side, 4.7 kOhm to 3.3V



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

Internal DisplayPort Connector

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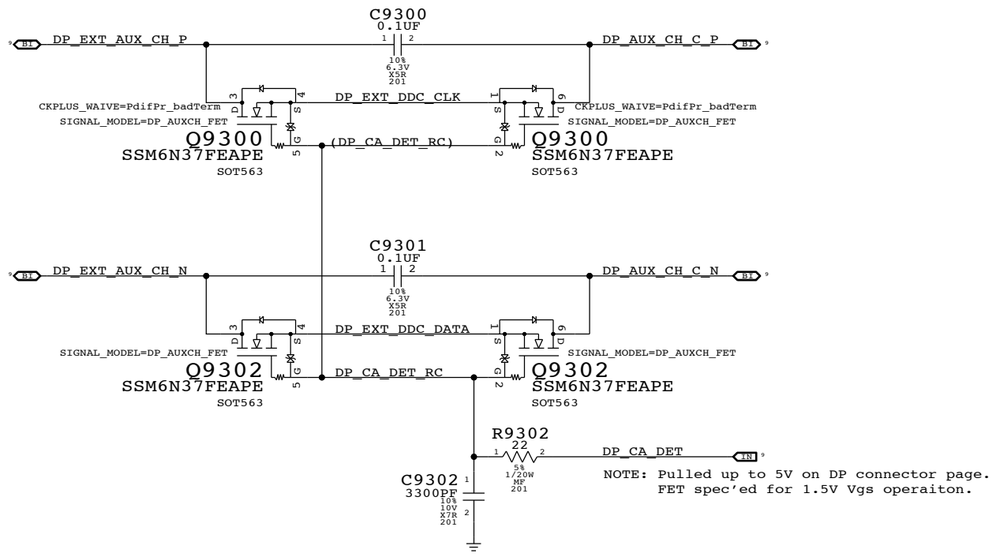

NOTE: Pulled up to 5V on DP connector page.
FET spec'ed for 1.5V Vgs operaiton.

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE
External DisplayPort Support

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Port Power Switch

=PP3V3_S5_DP_PORT_PWR
=DP_PWR_EN
U9480 TPS2051B SOT23
PP3V3_SW_DPILIM
MIN_LINE_WIDTH=0.50 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V
TP_DPPWR_OC_L
L9400 FERR-120-OHM-3A 0603
PP3V3_SW_DPPWR
MIN_LINE_WIDTH=0.50 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V
C9400 0.01UF 10% 10V X5R 201
CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM
OMIT_TABLE C9480 22UF 20% 6.3V X5R-CERM-1 603
C9481 0.1UF 10% 6.3V X5R 201
C9485 0.1UF 10% 6.3V X5R 201
OMIT_TABLE C9486 10UF 20% 6.3V X5R 603

HDMI_CEC
R9425 1M 5% 1/20W MF 201

CRITICAL J9400 MINIDSPLYPRT-K99 F-RT-TH
HOT_PLUG_DETECT, CONFIG1, CONFIG2, GND, ML_LANE3P, ML_LANE3N, GND, AUX_CHP, AUX_CHN, DP_PWR
GND, ML_LANE0P, ML_LANE0N, GND, ML_LANE1P, ML_LANE1N, GND, ML_LANE2P, ML_LANE2N, RETURN
SHIELD PINS

CRITICAL DP_ESD D9410 RCLAMP0524P SLP2510P8

CRITICAL FL9403 12-OHM-100MA TCM1210-48M
R9420 100K 5% 1/20W MF 201
DP_EXT_ML_P<3> C9414 0.1UF 10% 6.3V X5R 201 DP_EXT_ML_C_P<3>
DP_EXT_ML_N<3> C9415 0.1UF 10% 6.3V X5R 201 DP_EXT_ML_C_N<3>
DP_EXT_ML_F_P<3>
DP_EXT_ML_F_N<3>
DP_EXT_AUX_CH_C_P
DP_EXT_AUX_CH_C_N

CRITICAL FL9400 12-OHM-100MA TCM1210-48M
DP_EXT_ML_C_P<0> C9410 0.1UF DP_EXT_ML_P<0>
DP_EXT_ML_C_N<0> C9411 0.1UF DP_EXT_ML_N<0>
DP_EXT_ML_F_P<0>
DP_EXT_ML_F_N<0>

CRITICAL FL9401 12-OHM-100MA TCM1210-48M
DP_EXT_ML_C_P<1> C9412 0.1UF DP_EXT_ML_P<1>
DP_EXT_ML_C_N<1> C9413 0.1UF DP_EXT_ML_N<1>
DP_EXT_ML_F_P<1>
DP_EXT_ML_F_N<1>

CRITICAL FL9402 12-OHM-100MA TCM1210-48M
DP_EXT_ML_C_P<2> C9416 0.1UF DP_EXT_ML_P<2>
DP_EXT_ML_C_N<2> C9417 0.1UF DP_EXT_ML_N<2>
DP_EXT_ML_F_P<2>
DP_EXT_ML_F_N<2>

CRITICAL DP_ESD D9411 RCLAMP0524P SLP2510P8

=PP3V3_S0_DPCONN
=PP5VR3V3_S0_DPCADET
R9443 100K 5% 1/20W MF 201
R9442 100K 5% 1/20W MF 201
R9421 100K 5% 1/20W MF 201
DP_EXT_CA_DET
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q_L
NOTE: Q9440 must have Drain to Gate leakage of < 500 nA and gate to Source resistance of > 5 MOhm.
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q
R9422 1M 5% 1/20W MF 201
DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

CRITICAL DP_ESD D9400 RCLAMP0504F SC70-6-1

=PP3V3_S0_DPCONN
R9445 10K 5% 1/20W MF 201
DP_EXT_HPD
PP3V3_SW_DPILIM
R9444 10K 5% 1/20W MF 201
Q9441 2N7002DW-X-G SOT-363
DP_EXT_HPD_L
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q
R9423 100K 5% 1/20W MF 201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: DisplayPort Connector

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D
REVISION: 4.4.0
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*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

CRITICAL
R9700 0.01 0.5% 1W MF 0612
63 62 PPBUS_SW_LCDBKLT_PWR
PPBUS_SW_BKL
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=12.6V
71 42 OUT ISNS_LCDBKLT_P
71 42 OUT ISNS_LCDBKLT_N

8 =PP5V_S0_BKL
R9701 0 5% 1/20W MF 201

CRITICAL
L9701 22UH-2.5A IHLP2525CZ-SM
PPBUS_SW_LCDBKLT_PWR_SW
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=24V
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
D9701 SOD-123 RB160M-60G

PLACE_NEAR=U9701.21:3mm
C9796 220PF 10% 50V X7R-CERM 402
C9797 10UF 10% 50V X5R 1210-1
C9799 10UF 10% 50V X5R 1210-1
PPVOUT_SW_LCDBKLT 7 42 59
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=24V

CRITICAL
C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
PLACE_NEAR=L9701.1:3mm
PLACE_NEAR=L9701.1:3mm

NO STUFF
R9703 0 5% 1/20W MF 201
R9702 0 5% 1/20W MF 201
PPVIN_SW_BKL_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V

PLACE_NEAR=U9701.22:5mm
PLACE_NEAR=U9701.8:4mm
8 =PP3V3_S0_BKL_VDDIO
PP5V_S0_BKL_VLDO
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V

C9711 0.1UF 10% 6.3V X5R 201
C9710 1UF 10% 25V X5R 603-1
PLACE_NEAR=U9701.22:3mm
C9714 0.01UF 10% 10V X7R 0201

CRITICAL
OMIT_TABLE
U9701 LLP LP8545SQX

VDDIO	8		
VLDO	22		
VIN	23		
NC	6	GD	
BKL_FSET	5	FSET	
BKL_FLTR	20	FILTER	
BKL_ISET	3	ISET	
BKL_SCL	10	SCLK	
BKL_SDA	11	SDA	
BKL_PWM	2	PWM	
	7	FAULT	TP_BKL_FAULT
BKL_EN	4	EN	
		SW	24
		FB	21
BKL_ISEN1		OUT1	12
BKL_ISEN2		OUT2	13
BKL_ISEN3		OUT3	14
BKL_ISEN4		OUT4	16
BKL_ISEN5		OUT5	17
BKL_ISEN6		OUT6	18
BKL_VSYNC_R		VSYNC	19
GND_SW	1		
GND_S	9		
GND_L	15		
THRM PAD	25		

R9741 10K 5% 1/20W MF 201
41 I2C =I2C_BKL_1_SCL
R9753 0 5% 1/20W MF 201
41 I2C =I2C_BKL_1_SDA
R9757 0 5% 1/20W MF 201
Addr: 0x58(Wr)/0x59(Rd)

63 62 PPBUS_SW_LCDBKLT_PWR
R9731 200K 1% 1/20W MF 201
R9715 100K 1% 1/20W MF 201
NO STUFF
C9723 0.1UF 10% 25V X5R 402

9 LCD_BKLT_PWM
R9704 33 5% 1/20W MF 201
C9704 33PF 5% 25V NP0-C0G 201

R9716 90.9K 1% 1/20W MF 201
R9714 18.2K 1% 1/20W MF 201 I_LED=23.2mA
Fpwm=9.62kHz
see spec for others
GND_BKL_SGND
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
XW9710 SM
R9755 10K 1% 1/20W MF 201

I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

BKLT:PROD
R9717 0 5% 1/16W MF-LF 402
LED_RETURN_1 7 59 OUT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm
BKLT:PROD
R9718 0 5% 1/16W MF-LF 402
LED_RETURN_2 7 59 OUT
BKLT:PROD
R9719 0 5% 1/16W MF-LF 402
LED_RETURN_3 7 59 OUT
BKLT:PROD
R9720 0 5% 1/16W MF-LF 402
LED_RETURN_4 7 59 OUT
BKLT:PROD
R9721 0 5% 1/16W MF-LF 402
LED_RETURN_5 7 59 OUT
BKLT:PROD
R9722 0 5% 1/16W MF-LF 402
LED_RETURN_6 7 59 OUT

FOR LP8543:
STUFF R9741
NO STUFF R9740, C9740, C9741, R9754

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
353S2896	1	IC,LP8545,LED BKLT CTRLR,PRODUCTIO,LLP24	U9701	CRITICAL	PROJ:K16
353S2967	1	IC,LP8545,LED BKLT CTRLR,LLP24,K99 VER	U9701	CRITICAL	PROJ:K99

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K16 MLB SYNC DATE=03/31/2010
PAGE TITLE
LCD Backlight Driver
Apple Inc.
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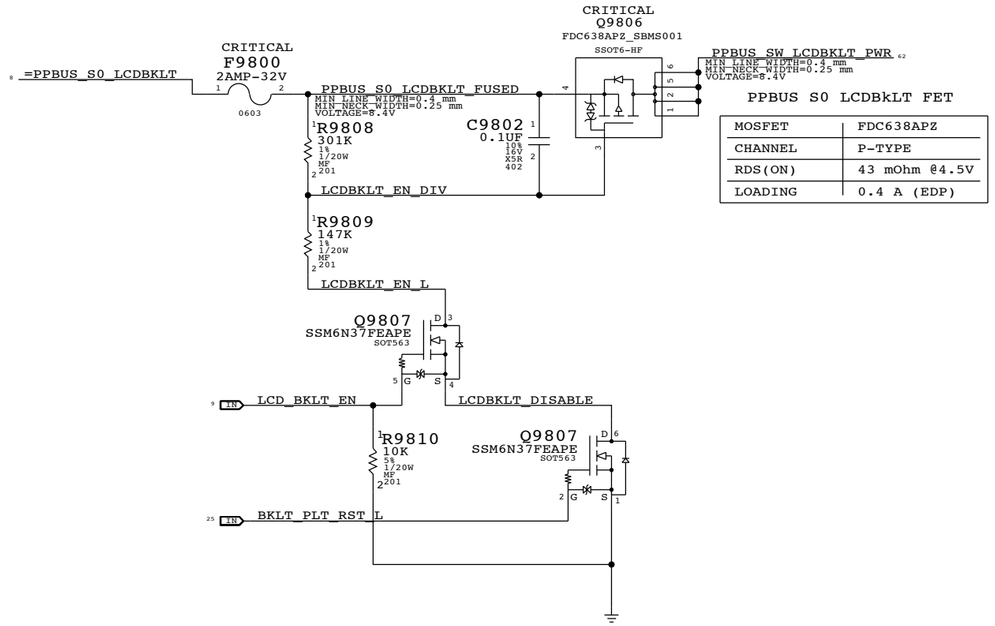

PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE
LCD Backlight Support

Apple Inc.

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ADDITIONAL CPU VCORE HF DECOUPLING

40x 1uF 0402

12 11 8 =PPVCORE_S0_CPU

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT TABLE
CRITICAL
C9900 C9901 C9902 C9903 C9904 C9905 C9906 C9907 C9908 C9909
2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT TABLE
CRITICAL
C9910 C9911 C9912 C9913 C9914 C9915 C9916 C9917 C9918 C9919
2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT TABLE
CRITICAL
C9920 C9921 C9922 C9923 C9924 C9925 C9926 C9927 C9928 C9929
2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT TABLE
CRITICAL
C9930 C9931 C9932 C9933 C9934 C9935 C9936 C9937 C9938 C9939
2.2UF 20% 6.3V CERM 402-LF

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

PAGE TITLE
Additional CPU/GPU Decoupling

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0> 7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0> 7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0> 7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0> 7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16> 7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1> 7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1> 7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1> 7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32> 7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2> 7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2> 7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2> 7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48> 7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3> 7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3> 7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3> 7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3> 7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0> 7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0> 7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17> 7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1> 7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_ADS_L 7 10 14
FSB_BREQ0_L	FSB_55S	FSB_1X	FSB_BREQ0_L 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_BNR_L 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_BPRI_L 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_DBSY_L 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_DEFER_L 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_DRDY_L 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_HIT_L 7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_HITM_L 7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_LOCK_L 7 10 14
FSB_CPURST_L	FSB_55S	FSB_1X	FSB_CPURST_L 10 13 14
FSB_1X	FSB_55S	FSB_1X	FSB_RS_L<2..0> 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_TRDY_L 10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_A20M_L 10 14
CPU_BSEL	CPU_55S	CPU_AGTL	CPU_BSEL<2..0> 9 10
CPU_FERR_L	CPU_55S	CPU_8MIL	CPU_FERR_L 10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_IGNNE_L 10 14
CPU_INIT_L	CPU_55S	CPU_AGTL	CPU_INIT_L 10 14
CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU_INTR 10 14
CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU_NMI 10 14
CPU_PROCHOT_L	CPU_55S	CPU_AGTL	CPU_PROCHOT_L 10 14 39
CPU_PWRGD	CPU_55S	CPU_AGTL	CPU_PWRGD 10 13 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_SMI_L 10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_STPCLK_L 10 14
PM_THRMTRIP_L	CPU_55S	CPU_8MIL	PM_THRMTRIP_L 10 14 39
FSB_CPUSLP_L	CPU_55S	CPU_AGTL	FSB_CPUSLP_L 10 14
CPU_FROM_SB	CPU_55S	CPU_AGTL	CPU_DPSLP_L 10 14
CPU_DPRSTP_L	CPU_55S	CPU_AGTL	CPU_DPRSTP_L 10 14 53
CPU_ASYNC	CPU_55S	CPU_AGTL	FSB_DPWR_L 10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P 10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N 10 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P 13 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N 13 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N 14
CPU_IERR_L	CPU_55S		CPU_IERR_L 10
PM_DPRSLPVR	CPU_55S	CPU_AGTL	PM_DPRSLPVR 14 53
(See above)	CPU_55S	CPU_AGTL	IMVP_DPRSLPVR
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND 14
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF 10 33
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3> 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2> 10
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1> 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0> 10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI 10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO 10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS 10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK 10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L 10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0> 10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5> 10 13
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L 13
	CPU_55S	CPU_8MIL	CPU_VID<6..0> 11 12 53
	CPU_55S	CPU_8MIL	IMVP6_VID<6..0> 12
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P 11 53
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N 11 53
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P 53
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N 53

FSB 4X Signal Groups

FSB 2X Signals

FSB 1X Signals

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PAGE TITLE: CPU/FSB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
MEM_CLK2MEM	*	=4:1_SPACING	?	NV DG says 3x inner, 4x outer
MEM_CTRL2CTRL	*	=2:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CTRL2MEM	*	=2.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2CMD	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2DATA	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DQS2MEM	*	=3:1_SPACING	?	NV DG says 4x inner, 5x outer
MEM_2OTHER	*	25 MIL	?	

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 360 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
CMD/CTRL signals should be matched within 150 ps.
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

MEM_A/B_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_P<5..0>	9 15 26 27 32
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_N<5..0>	9 15 26 27 32
MEM_A_CKE	MEM_50S	MEM_CTRL	MEM_A_CKE<3..0>	15 21 26 27 32
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_CS_L<3..0>	15 26 27 32
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_ODT<3..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_A<15..0>	9 15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_BA<2..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_RAS_L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_CAS_L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_WE_L	15 26 27 32
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DM<0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DM<1>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DM<2>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DM<3>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 26
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 26
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_P<5..0>	9 15 28 29 32
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_N<5..0>	9 15 28 29 32
MEM_B_CKE	MEM_50S	MEM_CTRL	MEM_B_CKE<3..0>	15 21 28 29 32
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_CS_L<3..0>	15 28 29 32
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_ODT<3..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_A<15..0>	9 15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_BA<2..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_RAS_L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_CAS_L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_WE_L	15 28 29 32
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15

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Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

	NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	PCIE_90D	PCIE	PEG_R2D_P<15..0>
	PCIE_90D	PCIE	PEG_R2D_N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>
	PCIE_90D	PCIE	PEG_D2R_N<15..0>
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>
	PCIE_90D	PCIE	PCIE_AP_R2D_P 7 34
	PCIE_90D	PCIE	PCIE_AP_R2D_N 7 34
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE_AP_R2D_C_P 16 34
	PCIE_90D	PCIE	PCIE_AP_R2D_C_N 16 34
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE_AP_D2R_P 7 16 34
	PCIE_90D	PCIE	PCIE_AP_D2R_N 7 16 34
	PCIE_90D	PCIE	PCIE_ENET_R2D_P
	PCIE_90D	PCIE	PCIE_ENET_R2D_N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE_ENET_R2D_C_P
	PCIE_90D	PCIE	PCIE_ENET_R2D_C_N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE_ENET_D2R_P
	PCIE_90D	PCIE	PCIE_ENET_D2R_N
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_P
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_N
	PCIE_90D	PCIE	PCIE_FW_R2D_P
	PCIE_90D	PCIE	PCIE_FW_R2D_N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P
	PCIE_90D	PCIE	PCIE_FW_D2R_N
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P 9 16
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N 9 16
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_P 7 16 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_N 7 16 34
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX0_TERMP 16
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF
DP_INT_ML	DP_90D	DISPLAYPORT	DP_IG_ML1_P<1..0> 9 17
DP_INT_ML	DP_90D	DISPLAYPORT	DP_IG_ML1_N<1..0> 9 17
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH1_P 9 17
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH1_N 9 17
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML0_P<3..0> 9 17
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML0_N<3..0> 9 17
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH0_P 9 17
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH0_N 9 17
MCP_TMDS0_RSET	MCP_DV_COMP		MCP_TMDS0_RSET 17 24
MCP_TMDS0_VPROBE			MCP_TMDS0_VPROBE 17 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET 17 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE 17 24
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P 18 35
	SATA_90D	SATA	SATA_HDD_R2D_C_N 18 35
	SATA_90D	SATA	SATA_HDD_R2D_P 7 35
	SATA_90D	SATA	SATA_HDD_R2D_N 7 35
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P 18 35
	SATA_90D	SATA	SATA_HDD_D2R_N 18 35
	SATA_90D	SATA	SATA_HDD_D2R_C_P 7 35
	SATA_90D	SATA	SATA_HDD_D2R_C_N 7 35
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P 9 18
	SATA_90D	SATA	SATA_ODD_R2D_C_N 9 18
	SATA_90D	SATA	SATA_ODD_R2D_P 9
	SATA_90D	SATA	SATA_ODD_R2D_N 9
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P 9 18
	SATA_90D	SATA	SATA_ODD_D2R_N 9 18
	SATA_90D	SATA	SATA_ODD_D2R_C_P
	SATA_90D	SATA	SATA_ODD_D2R_C_N
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP 18

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	7 19 38 40
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	7 19 38 40
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	25 38
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	7 25 40
USB_EXTA	USB_90D	USB	USB_EXTA_P	18 36
	USB_90D	USB	USB_EXTA_N	18 36
	USB_90D	USB	USB_EXTA_MUXED_P	36 71
	USB_90D	USB	USB_EXTA_MUXED_N	36 71
USB_MINI	USB_90D	USB	USB_MINI_P	9 18
	USB_90D	USB	USB_MINI_N	9 18
USB_EXTD	USB_90D	USB	USB_EXTD_P	7 18 37
	USB_90D	USB	USB_EXTD_N	7 18 37
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7 18 37
	USB_90D	USB	USB_CAMERA_N	7 18 37
USB_BT	USB_90D	USB	USB_BT_P	7 18 34
	USB_90D	USB	USB_BT_N	7 18 34
USB_TPAD	USB_90D	USB	USB_TPAD_P	18 46 71
	USB_90D	USB	USB_TPAD_N	18 46 71
USB_IR	USB_90D	USB	USB_IR_P	
	USB_90D	USB	USB_IR_N	
USB_EXTB	USB_90D	USB	USB_EXTB_P	
	USB_90D	USB	USB_EXTB_N	
USB_T57	USB_90D	USB	USB_T57_P	
	USB_90D	USB	USB_T57_N	
USB_EXTC	USB_90D	USB	USB_EXTC_P	9 18
	USB_90D	USB	USB_EXTC_N	9 18
USB_SDCARD	USB_90D	USB	USB_SDCARD_P	9 18
	USB_90D	USB	USB_SDCARD_N	9 18
USB_WM	USB_90D	USB	USB_WM_P	
	USB_90D	USB	USB_WM_N	
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	18
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	19 41
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	19 41
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS_MCP_1_CLK	19 41
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS_MCP_1_DATA	19 41
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	7 19 37
	HDA_55S	HDA	HDA_BIT_CLK_R	19
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	7 19 37
	HDA_55S	HDA	HDA_SYNC_R	19
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	19
	HDA_55S	HDA	HDA_RST_L	7 19 37
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	7 19 37
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	7 19 37
	HDA_55S	HDA	HDA_SDOUT_R	19
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	19
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	19 25
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	25 38
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	19 40
	SPI_55S	SPI	SPI_CLK	40
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	19 40
	SPI_55S	SPI	SPI_MOSI	40
SPI_MISO	SPI_55S	SPI	SPI_MISO	19 40
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	19 40
	SPI_55S	SPI	SPI_CS0_L	40
	SPI_55S	SPI	SPI_MLB_CLK	40 47
	SPI_55S	SPI	SPI_MLB_MOSI	40 47
	SPI_55S	SPI	SPI_MLB_MISO	40 47
	SPI_55S	SPI	SPI_MLB_CS_L	40 47
	SPI_55S	SPI	SPI_ALT_CLK	7 40
	SPI_55S	SPI	SPI_ALT_MOSI	7 40
	SPI_55S	SPI	SPI_ALT_MISO	7 40
	SPI_55S	SPI	SPI_ALT_CS_L	7 40

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

SD Card Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

RGMII Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	9 18
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	9 18
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<0>	9 18
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	9 18
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	9 18
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	
	ENET_MII_55S	ENET_MII	ENET_RESET_L	

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>

SD Card Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SD_DATA	SD_55S	SD_INTERFACE	SD_D<4..0>
	SD_55S	SD_INTERFACE	SDCONN_DATA<4..0>
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<4>
SD_DATA_R	SD_55S	SD_INTERFACE	SD_D<7..5>
	SD_55S	SD_INTERFACE	SDCONN_DATA<7..5>
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<7..5>
SD_CLK	SD_55S	SD_INTERFACE	SD_CLK
	SD_55S	SD_INTERFACE	SD_CLK_R
	SD_55S	SD_INTERFACE	SDCONN_CLK
SD_CMD	SD_55S	SD_INTERFACE	SD_CMD
	SD_55S	SD_INTERFACE	SDCONN_CMD
	SD_55S	SD_INTERFACE	BCM57765_CR_CMD

NOTE: SD_D<7..5> are different to support BCM5764M/BCM57765 co-layout.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5S	SMB	SMBUS_SMC_A_S3_SCL	41
SMBUS_SMC_A_S3_SDA	SMB_5S	SMB	SMBUS_SMC_A_S3_SDA	41
SMBUS_SMC_B_S0_SCL	SMB_5S	SMB	SMBUS_SMC_B_S0_SCL	41
SMBUS_SMC_B_S0_SDA	SMB_5S	SMB	SMBUS_SMC_B_S0_SDA	41
SMBUS_SMC_0_S0_SCL	SMB_5S	SMB	SMBUS_SMC_0_S0_SCL	41
SMBUS_SMC_0_S0_SDA	SMB_5S	SMB	SMBUS_SMC_0_S0_SDA	41
SMBUS_SMC_BSA_SCL	SMB_5S	SMB	SMBUS_SMC_BSA_SCL	7 41
SMBUS_SMC_BSA_SDA	SMB_5S	SMB	SMBUS_SMC_BSA_SDA	7 41
SMBUS_SMC_MGMT_SCL	SMB_5S	SMB	SMBUS_SMC_MGMT_SCL	41
SMBUS_SMC_MGMT_SDA	SMB_5S	SMB	SMBUS_SMC_MGMT_SDA	41

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	50
	1TO1_DIFFPAIR		CHGR_CSI_N	50
	1TO1_DIFFPAIR		CHGR_CSI_R_P	50
	1TO1_DIFFPAIR		CHGR_CSI_R_N	50
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	50
	1TO1_DIFFPAIR		CHGR_CSO_N	50
	1TO1_DIFFPAIR		CHGR_CSO_R_P	43 50
	1TO1_DIFFPAIR		CHGR_CSO_R_N	43 50

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=1:1_SPACING	?
AUDIO	*	=1:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SD CARD READER LAYOUT RELAXATIONS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*		=STANDARD				
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	5.8 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	*			0.25 MM	250 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_P	36 68
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_N	36 68
(USB_EXTA)	USB_90D	USB	USB_LT1_P	36
(USB_EXTA)	USB_90D	USB	USB_LT1_N	36
(USB_TPAD)	USB_90D	USB	USB_TPAD_P	18 46 68
(USB_TPAD)	USB_90D	USB	USB_TPAD_N	18 46 68
(USB_TPAD)	USB_90D	USB	USB_TPAD_CONN_P	7 46
(USB_TPAD)	USB_90D	USB	USB_TPAD_CONN_N	7 46
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	I2C_SMC_SMS_SDA_R	
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	I2C_SMC_SMS_SCL_R	
	SMB_55S	SMB	I2C_TCON_SCL	41
	SMB_55S	SMB	I2C_TCON_SDA	41
	SMB_55S	SMB	I2C_TCON_SCL_CONN	
	SMB_55S	SMB	I2C_TCON_SDA_CONN	

Graphics Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_90D	DISPLAYPORT	DP_INT_ML_P<1..0>	9 59
	DP_90D	DISPLAYPORT	DP_INT_ML_N<1..0>	9 59
	DP_90D	DISPLAYPORT	DP_INT_ML_C_P<1..0>	59
	DP_90D	DISPLAYPORT	DP_INT_ML_C_N<1..0>	59
	DP_90D	DISPLAYPORT	DP_INT_ML_F_P<1..0>	7 59
	DP_90D	DISPLAYPORT	DP_INT_ML_F_N<1..0>	7 59
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_C_P	7 59
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_C_N	7 59
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_P	9 59
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_N	9 59
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP_EXT_ML_P<3..0>	9 61
	DP_90D	DISPLAYPORT	DP_EXT_ML_N<3..0>	9 61
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_P<3..0>	61
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_N<3..0>	61
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_P<3..0>	61
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_N<3..0>	61
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_P	9 61
	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_N	9 61

Power Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPUTHMSNS_D2	THERM_1TO1_55S	THERM	DRAMTHMSNS_D2_P	44
	THERM_1TO1_55S	THERM	DRAMTHMSNS_D2_N	44
CPU_THERMD	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 44
	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 44
MCPTHMSNS_D2	THERM_1TO1_55S	THERM	MLBR_THMDIODE_P	44
	THERM_1TO1_55S	THERM	MLBR_THMDIODE_N	44
MCP_THMDIODE	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	19 44
	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	19 44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	42 52
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	42 52
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	34 42
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	34 42
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CSREG_P	43
	SENSE_1TO1_55S	SENSE	ISNS_CSREG_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	35 42
	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	35 42
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	42 62
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	42 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_P	55
	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_N	55
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	IMVP6_CS_P	53
	SENSE_1TO1_55S	SENSE	IMVP6_CS_N	53
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	IMVP6_CS_R_P	53
	SENSE_1TO1_55S	SENSE	IMVP6_CS_R_N	53
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VTTSENSE_P	55
	SENSE_1TO1_55S	SENSE	CPU_VTTSENSE_N	55
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_P	22 54
	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_N	22 54
		MEM_POWER	PP1V5R1V35_S3	7 8
		SB_POWER	PP3V3_S5	7 8 57
		SB_POWER	PP3V3_S0	7 8 57
		SB_POWER	PP1V5_S0	7 8 57
		GND	GND	

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P	7 37 48
	DIFFPAIR	AUDIO	SPKRAMP_INR_N	7 37 48
MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R_P	48
	DIFFPAIR	AUDIO	MAX98300_R_N	48

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K99 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL3,ISL10	Y	0.250 MM	0.250 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.250 MM	0.250 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.140 MM	0.140 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.090 MM	0.090 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.076 MM	0.076 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.155 MM	0.155 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.125 MM	0.125 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
75_OHM_DIFF	TOP,BOTTOM	Y	0.160 MM	0.160 MM		0.160 MM	0.160 MM
75_OHM_DIFF	ISL3,ISL10	Y	0.120 MM	0.120 MM		0.140 MM	0.140 MM
75_OHM_DIFF	ISL4,ISL9	Y	0.140 MM	0.140 MM		0.140 MM	0.140 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
95_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
95_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL3,ISL10	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM
100_OHM_DIFF	ISL4,ISL9	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V5_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
1.5X_DIELECTRIC	*	0.105 MM	?
5X_DIELECTRIC	*	0.350 MM	?

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1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	SS_CAP_1UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0628	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	MU_CAP_1UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0630	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909,C9910	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919,C9920	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929,C9930	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939,C9940	CRITICAL	SS_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1285,C1286,C1287,C1289,C1291,C1292,C1293,C1294,C1295,C1296,C1297,C1298	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516,C3517	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3536,C3537,C3538	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616,C3617	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3636,C3637,C3638	CRITICAL	SS_CAP_2_2UF
138S0632	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655,C3656	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909,C9910	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919,C9920	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929,C9930	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939,C9940	CRITICAL	MU_CAP_2_2UF
138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296,C1297,C1298	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516,C3517	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3536,C3537,C3538	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616,C3617	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3636,C3637,C3638	CRITICAL	MU_CAP_2_2UF
138S0633	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655,C3656	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909,C9910	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919,C9920	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929,C9930	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939,C9940	CRITICAL	TY_CAP_2_2UF
138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296,C1297,C1298	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516,C3517	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3536,C3537,C3538	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616,C3617	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3636,C3637,C3638	CRITICAL	TY_CAP_2_2UF
138S0634	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655,C3656	CRITICAL	TY_CAP_2_2UF

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SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C7360,C7370,C7380	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C4912,C9486,C2500,C2520,C2560,C2567,C2600,C2610,C2620,C2630	CRITICAL	SS_CAP_10UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0625	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C7360,C7370,C7380	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C4912,C9486,C2500,C2520,C2560,C2567,C2600,C2610,C2620,C2630	CRITICAL	MU_CAP_10UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0627	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C7360,C7370,C7380	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C4912,C9486,C2500,C2520,C2560,C2567,C2600,C2610,C2620,C2630	CRITICAL	TY_CAP_10UF

22UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0635	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	SS_CAP_22UF
138S0635	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	SS_CAP_22UF
138S0635	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	SS_CAP_22UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0676	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	MU_CAP_22UF
138S0676	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	MU_CAP_22UF
138S0676	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	MU_CAP_22UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0688	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	TY_CAP_22UF
138S0688	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	TY_CAP_22UF
138S0688	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	TY_CAP_22UF

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