

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X200 | MLB-C1

LAST_MODIFIED= Tue Oct 29 15:52:27 2013

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
A	0002535199	PRODUCTION RELEASED		2014-01-13

SCH AND BOARD PART NUMBERS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-0886	1	SCH_MLB-C1_X200	SCH1	
820-4124	1	PCBF_MLB-C1_X200	PCB1	

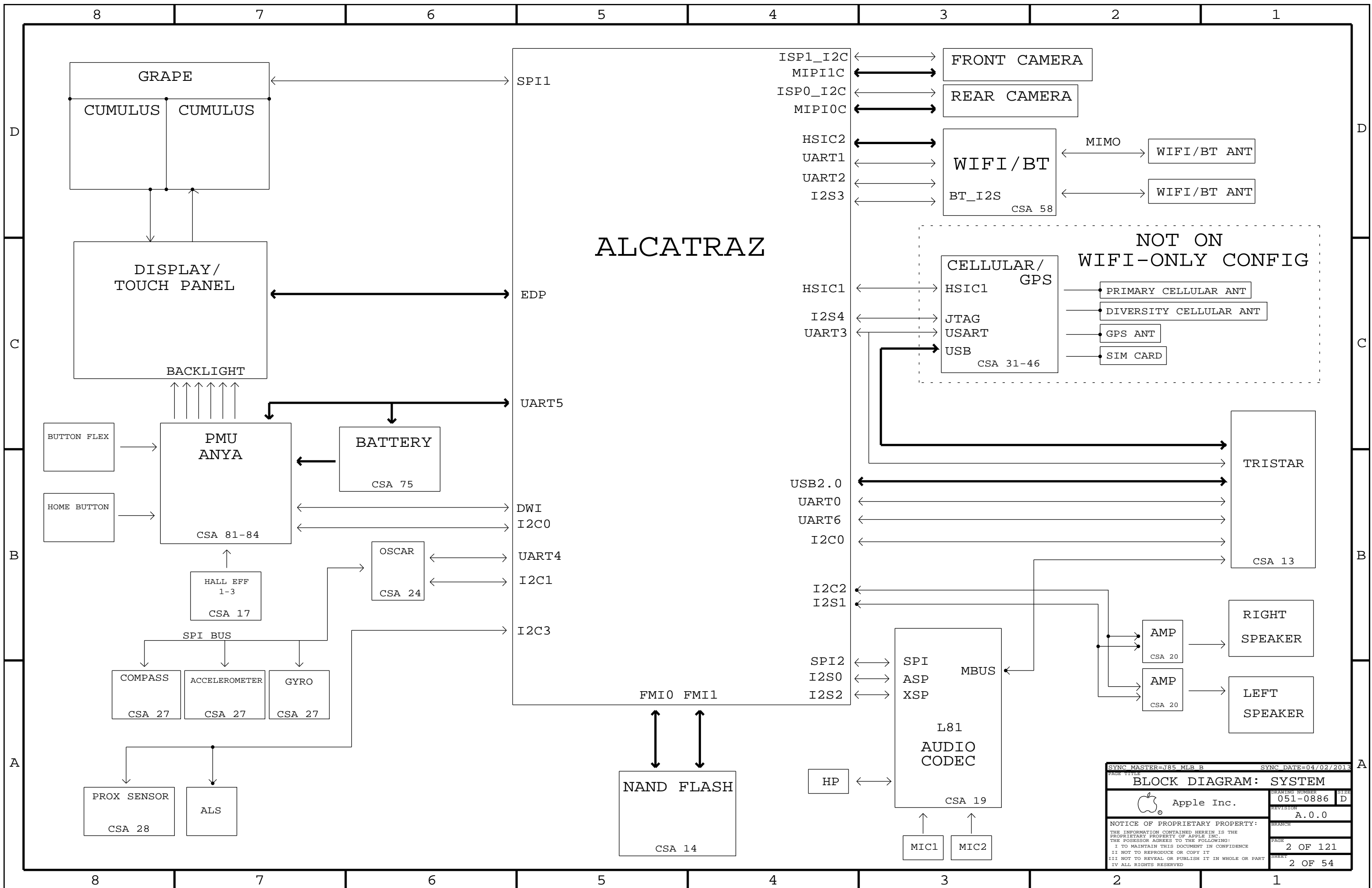
PDF CSA CONTENTS

PDF	CSA	CONTENTS	SYNC MASTER	DATE
21	27	SENSOR: ACCEL, COMPASS, GYRO	N/A	N/A
22	28	SENSOR: PROX	J85_MLB_I2	05/12
23	29	CAMERA: REAR CONN & FILTERS	N/A	N/A
24	30	CELL:AP INTERFACE & DEBUG CONNECTORS	RADIO_MLB_I2	08/29/2013
25	32	CELL: BASEBAND PMU (1 OF 2)	RADIO_MLB_I2	08/29/2013
26	33	CELL: BASEBAND PMU (2 OF 2)	RADIO_MLB_I2	08/29/2013
27	34	CELL: BASEBAND (1 OF 2)	RADIO_MLB_I2	08/29/2013
28	35	CELL: BASEBAND (2 OF 2)	RADIO_MLB_I2	08/29/2013
29	36	CELL: RF TRANSCEIVER (1 OF 2)	RADIO_MLB_I2	08/29/2013
30	37	CELL: RF TRANSCEIVER (2 OF 2)	RADIO_MLB_I2	08/29/2013
31	38	CELL: RX MATCHING	RADIO_MLB_I2	08/29/2013
32	39	CELL: RF TRANSCEIVER (3 OF 4)	RADIO_MLB_I2	08/29/2013
33	40	CELL: PENTABAND PA	RADIO_MLB_I2	08/29/2013
34	41	CELL: BAND 2/3 PAD	RADIO_MLB_I2	08/29/2013
35	42	CELL: BAND 7/20 PAD	RADIO_MLB_I2	08/29/2013
36	43	CELL: BAND 5/8 PAD	RADIO_MLB_I2	08/29/2013
37	44	CELL: 2G PA	RADIO_MLB_I2	08/29/2013
38	45	CELL: PA DCDC CONVERTER	RADIO_MLB_I2	08/29/2013
39	46	CELL: ASM AND HB LTE FRONT-END	RADIO_MLB_I2	08/29/2013
40	47	CELL: RX DIVERSITY	RADIO_MLB_I2	08/29/2013
41	48	CELL: GPS	RADIO_MLB_I2	08/29/2013
42	49	CELL: ANTENNA FEEDS	RADIO_MLB_I2	08/29/2013
43	57	IO: FILTERS & HOTBAR CONN	N/A	04/18/2011
44	58	WIFI/BT: MODULE	WIFI_DEV05	20/2013
45	75	POWER: BATTERY CONNECTOR	N/A	N/A
46	81	PMU: ANYA PAGE 1	J72_MLB_I1	26/2012
47	82	PMU: ANYA PAGE 2	J85_MLB_I2	03/2012
48	83	PMU: ANYA PAGE 3	J72_MLB_I1	26/2012
49	84	PMU: ANYA PAGE 4	J72_MLB_I1	26/2012
50	85	POWER: PPIV8_SW	J85_MLB_I2	05/2012
51	90	SEP: EEPROM & SOC DEBUG	J72_MLB_I1	26/2012
52	93	TEST: TP/HOLES/FIDUCIALS	J85_MLB_I2	03/12
53	94	TEST: EE TP/PP	J72_MLB_I1	26/2012
54	121	POWER: ALIASES	J72_MLB_I1	26/2012

PDF CSA CONTENTS

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	TABLE OF CONTENTS	N/A	N/A
2	2	BLOCK DIAGRAM: SYSTEM	J85_MLB_I2	04/02/2013
3	4	BOM TABLES	J72_MLB_I1	26/2012
4	6	SOC: MAIN	N/A	04/18/2011
5	7	SOC: I/OS	N/A	05/05/2011
6	8	SOC: NAND	N/A	04/18/2011
7	9	SOC: DP,MIPI	MLB	05/04/2012
8	10	SOC: SRAM, IO PWRS	N/A	04/18/2011
9	11	SOC: VDD, SRAM, CPU, GPU PWRS	N/A	04/18/2011
10	12	SOC: MISC & ALIASES	N/A	04/11/2011
11	13	IO: TRISTAR	N/A	N/A
12	14	NAND STORAGE	MLB	05/04/2012
13	17	TOUCH: SUPPORT CKT & CONN	N/A	06/21/2010
14	18	AUDIO: HP FLEX CONN	N/A	03/31/2011
15	19	AUDIO: L81 CODEC	KAVITHA	01/18/2012
16	20	AUDIO: CS35L19A AMPS	KAVITHA	01/18/2012
17	21	BUTTON: CONN	N/A	N/A
18	22	VIDEO: EDP SUPPORT & CONN	J85_MLB_I2	05/2012
19	24	SENSOR: OSCAR	J72_MLB_I1	26/2012
20	26	CAMERA: FF-ALS CONN & FILTERS	J85_MLB_I2	03/2012

DRAWING TITLE		SCH,MLB-C1,X200	
DRAWING NUMBER	051-0886	SIZE	D
	REVISION		A.0.0
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SYNC MASTER=J85 MLB B		SYNC DATE=04/02/2013	
BLOCK DIAGRAM: SYSTEM			
Apple Inc.		DRAWING NUMBER	SIZE
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

BOM OPTIONS

COMMON
ALTERNATE
16GB_PROD
32GB_PROD
64GB_PROD
128GB_PROD
DEVELOPMENT_JTAG_TAP
JTAG_DAP
MLB (WDOG TO PMU)

WIFI BOM OPTIONS

ANDGATE_TI
FERRITE_TY
FERRITE_IDK

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0207	1	H6P + 1GB ELPIDA	U0652	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0208	339S0207		U0652	HYNIX DDR

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0656	1	IC,PMU,ANYA,D2089A1,OTFXX,FCCSP342	U8100	CRITICAL	

FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0921	1	TOS,19NM,PPN1.5,C,DDP,16GB	U1400	16GB
335S0922	1	TOS,19NM,PPN1.5,C,QDP,32GB	U1400	32GB
335S0923	1	TOS,19NM,PPN1.5,C,ODP,64GB	U1400	64GB
335S0929	1	TOS,19NM,PPN1.5,C,12DP,64GB	U1400	96GB
335S0924	1	TOS,19NM,PPN1.5,C,16DP,128GB	U1400	128GB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0930	335S0921	16GB	U1400	HYNIX 20NM PPN1.5 16GB
335S0931	335S0922	32GB	U1400	HYNIX 20NM PPN1.5 32GB
335S0932	335S0923	64GB	U1400	HYNIX 20NM PPN1.5 64GB

U2200

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S4272	1	IC,SIGMA1423V,PMU SW,SEESFF3,4A,TDFH	U2200	

NOTE: FOLLOWING J72, U2200 USES 353S3672 FOOTPRINT (353S4272 HAS SMALLER PADS DUE TO NEW DFM RULES)

4.3UF CAP

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657		C1009,C1015...	RDAR #13988471

WIFI

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0223	339S0213		U5800	

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-6207	1	FENCE,TALL,MLB,X221	FD_FENCE_MLB	CRITICAL	
806-7613	1	FENCE,RADIO,MLB,C BRD,X221	FD_CAN_RADIO	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	EEEE FOR 639-5393 (X200C1 GOOD)	FNJD	CRITICAL	EEEE_X200C_GOOD
825-7639	1	EEEE FOR 639-5394 (X200C1 BETTER)	FNJ5	CRITICAL	EEEE_X200C_BETTER
825-7639	1	EEEE FOR 639-5385 (X200C1 BEST)	FNJ9	CRITICAL	EEEE_X200C_BEST
825-7639	1	EEEE FOR 639-5386 (X200C1 BEST+)	FNJH	CRITICAL	EEEE_X200C_BEST+
825-7639	1	EEEE FOR 639-5387 (X200C1 ULTIMATE)	FNJ6	CRITICAL	EEEE_X200C_ULTIMATE
825-7639	1	EEEE FOR 639-5388 (X200C1 GOOD IVS)	FNJ8	CRITICAL	EEEE_X200C_GOOD_IVS
825-7639	1	EEEE FOR 639-5389 (X200C1 BETTER IVS)	FNJF	CRITICAL	EEEE_X200C_BETTER_IVS
825-7639	1	EEEE FOR 639-5390 (X200C1 BEST IVS)	FNJC	CRITICAL	EEEE_X200C_BEST_IVS
825-7639	1	EEEE FOR 639-5391 (X200C1 BEST+ IVS)	FNJ7	CRITICAL	EEEE_X200C_BEST+_IVS
825-7639	1	EEEE FOR 639-5392 (X200C1 ULTIMATE IVS)	FNJG	CRITICAL	EEEE_X200C_ULTIMATE_IVS

GYRO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1192	1	GYRO, ST MICRO	U2720	CRITICAL	GYRO_STMICRO
338S1218	1	GYRO, INVENSENSE	U2720	CRITICAL	GYRO_INVENSENSE
132S0391	1	CAP 0.01UF 25V 0201	C2726	CRITICAL	GYRO_STMICRO
132S0288	1	CAP 0.1UF 16V 0201	C2726	CRITICAL	GYRO_INVENSENSE

338S1158 OLD GYRO - ST MICRO
OLDER INVENSENSE P/N 338S1135
OLD INVENSENSE P/N 338S1200 (3/22/13)

ACCEL

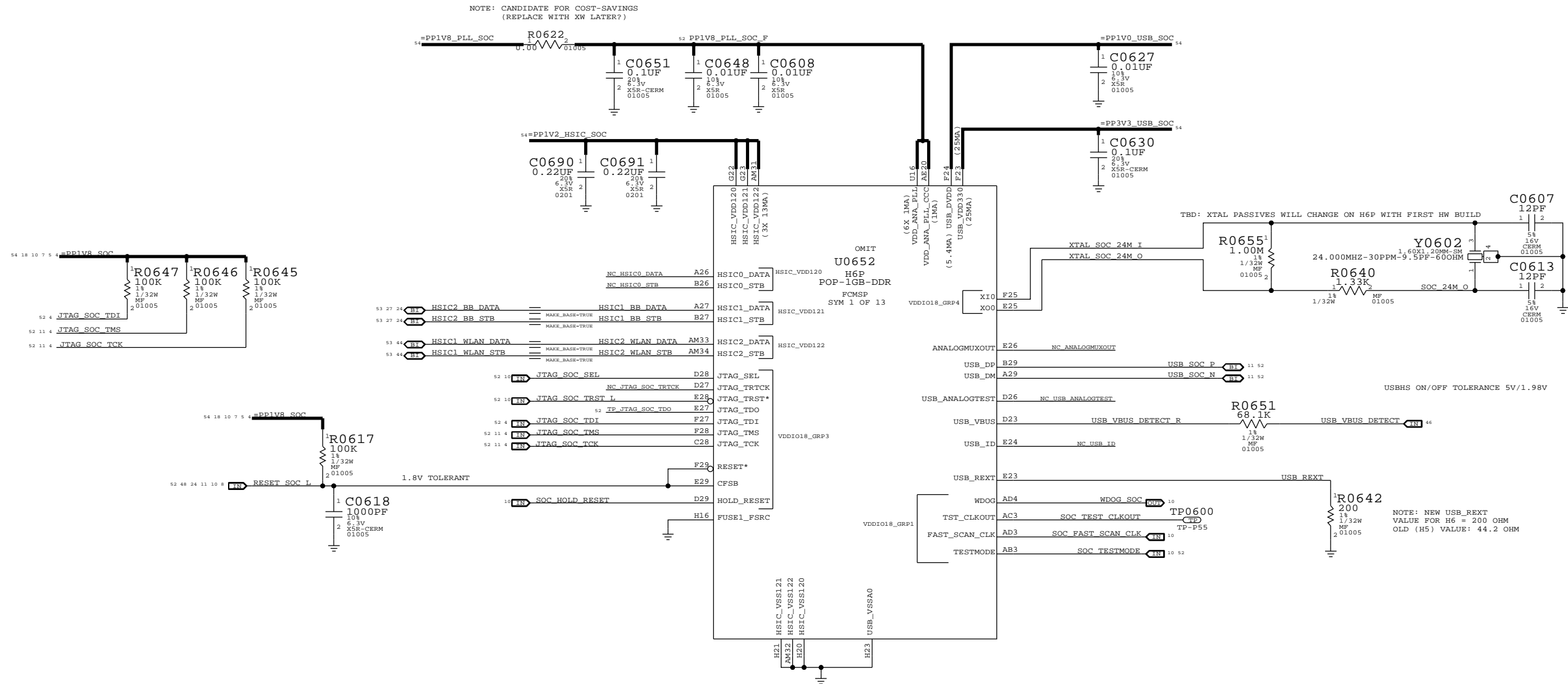
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1163	1	IC,ACCEL,3-AXIS,DIG,BMA282,LGA14	U2700	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

338S1233 ST MICRO - DISQUAL'ED
338S1114 OLD ACCEL - ST MICRO
338S1191 OLD ACCEL - ST MICRO

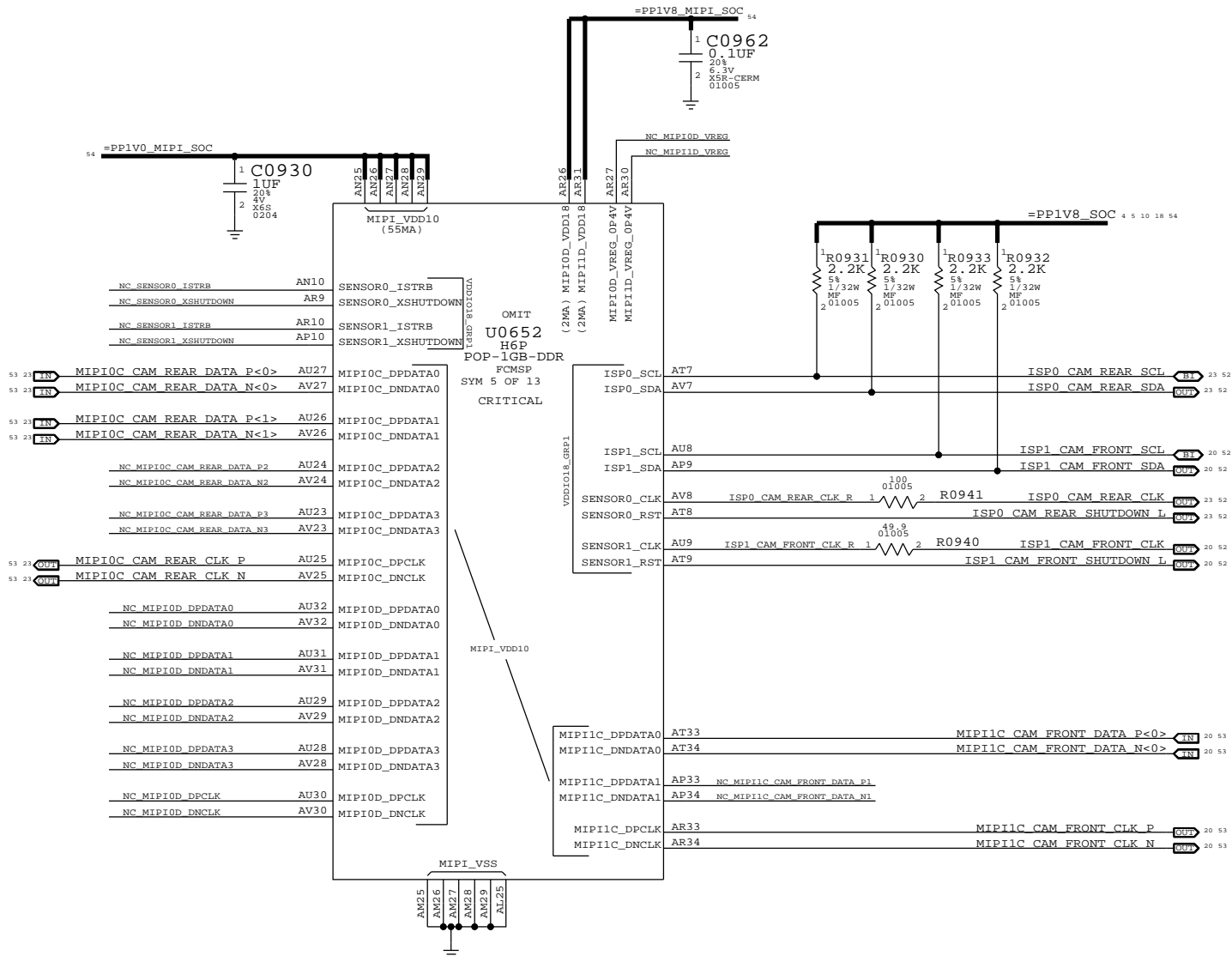
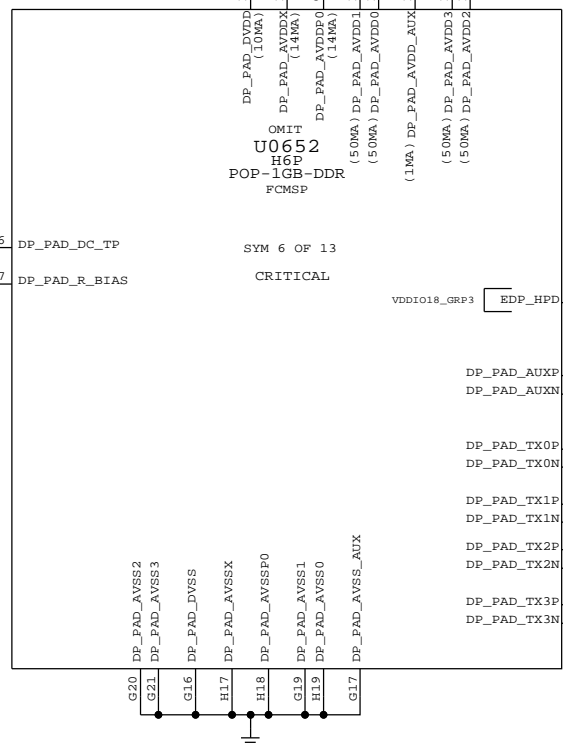
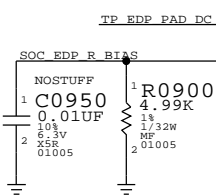
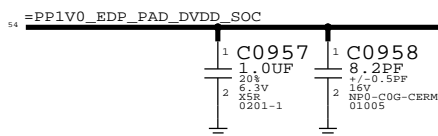
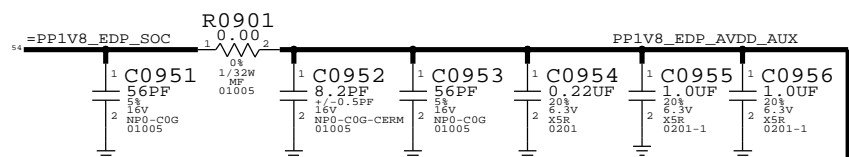
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BOM TABLES			
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		SHEET	3 OF 54

H6P: JTAG, USB, PLL, HSIC, XTAL

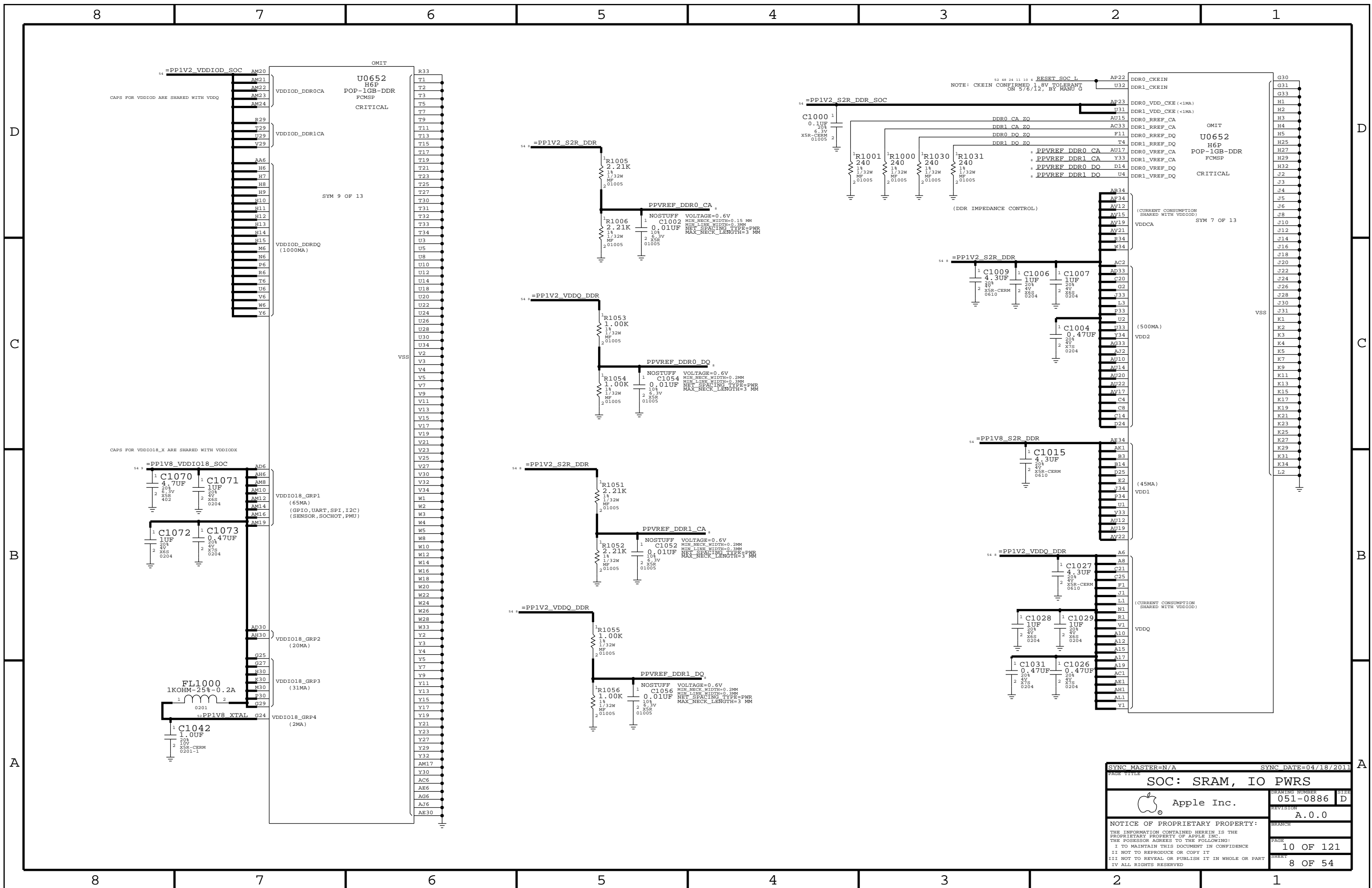


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SOC: MAIN			
Apple Inc.		DRAWING NUMBER	SIZE
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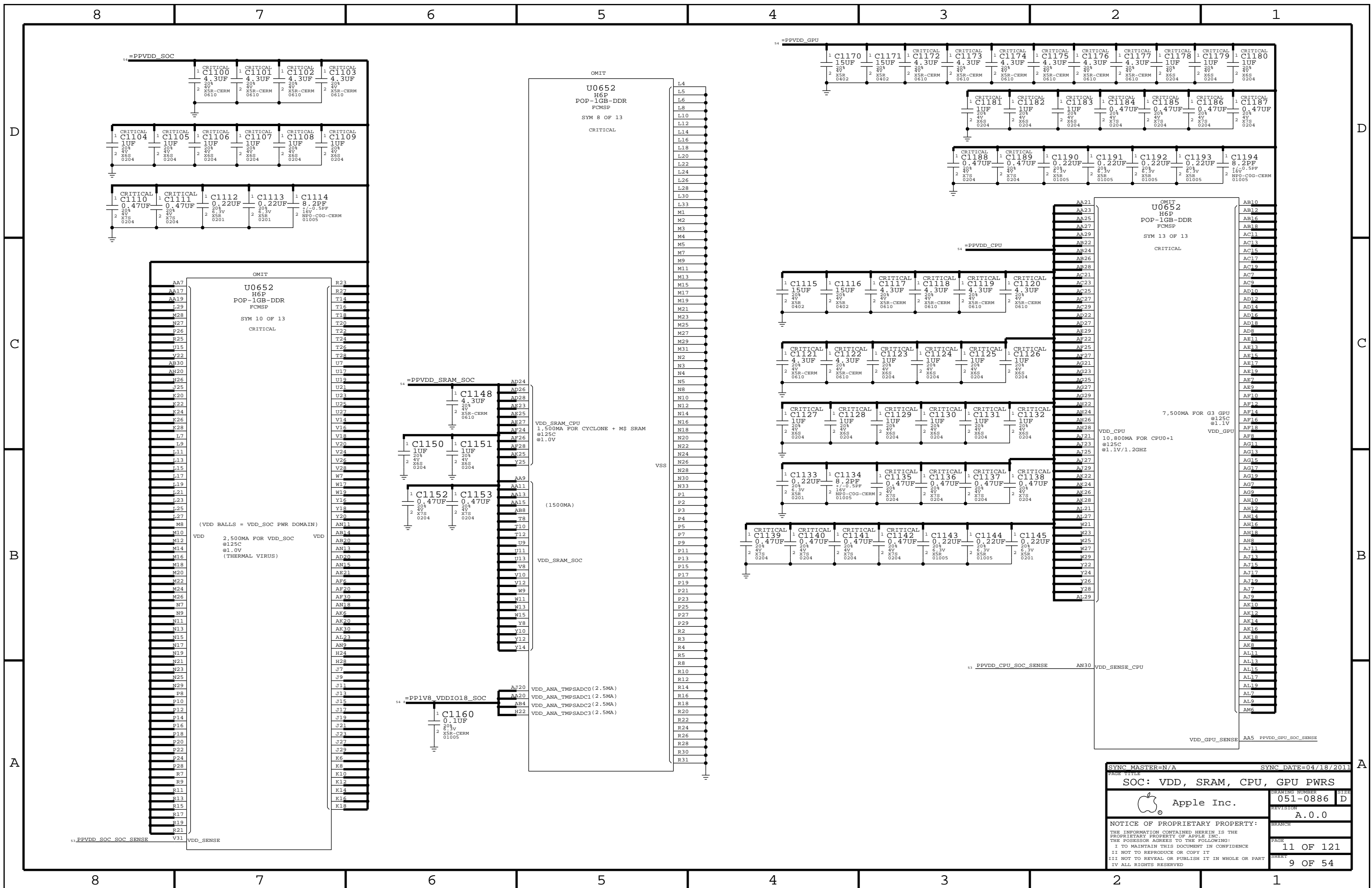
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PAGE TITLE			
SOC: DP, MIPI		DRAWING NUMBER	SIZE
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PAGE TITLE			
SOC: SRAM, IO PWRS			
Apple Inc.		DRAWING NUMBER	051-0886
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SYNC MASTER=N/A		SYNC DATE=04/18/2011	
PAGE TITLE			
SOC: VDD, SRAM, CPU, GPU PWRS			
DRAWING NUMBER		SIZE	
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REVISION		BRANCH	
A.0.0		PAGE	
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		9 OF 54	



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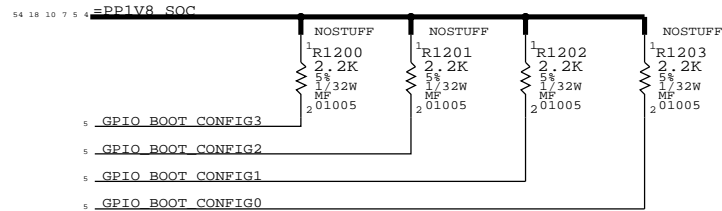
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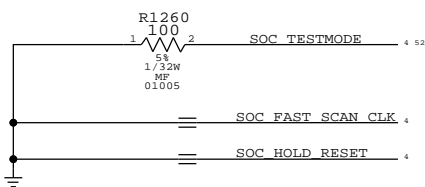
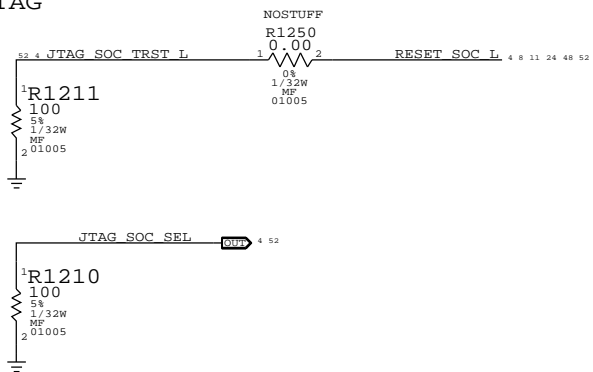
BOOT CONFIG ID

BOOT_CONFIG[3] (GPIO29)
 BOOT_CONFIG[2] (GPIO28)
 BOOT_CONFIG[1] (GPIO25)
 BOOT_CONFIG[0] (GPIO18)



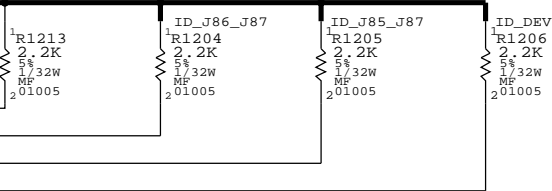
BOOT_CONFIG[3-0]	S/W READ FLOW
0000 SPI0	1. SET GPIO AS INPUT
0001 SPI0 TEST MODE	2. DISABLE PU AND ENABLE PD
0010 NAND <-- SELECTED	3. READ
0011 NAND TEST MODE	

JTAG



BOARD ID

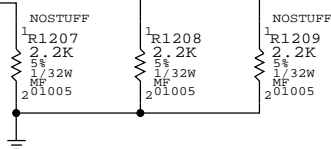
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 BOARD_ID[2] GPIO_BOARD_ID2
 BOARD_ID[1] GPIO_BOARD_ID1
 BOARD_ID[0] GPIO_BOARD_ID0



ID[3-0]	SYSTEM	S/W READ FLOW
1010 J85 AP	SYSTEM	1. SET GPIO AS INPUT 2. DISABLE PU AND ENABLE PD 3. READ
1011 J85 DEV		
1100 J86 AP	MLB	
1101 J86 DEV		
1110 J87 AP	MLB_B	
1111 J87 DEV		

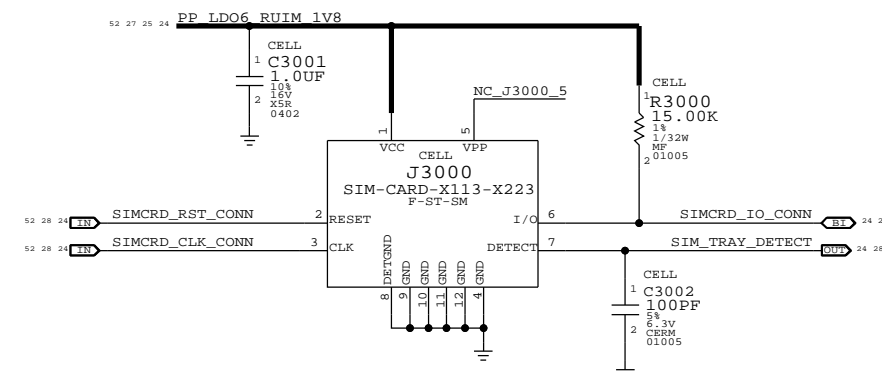
BOARD REVISION

GPIO_BOARD_REV2
 GPIO_BOARD_REV1
 GPIO_BOARD_REV0



BRD_REV[2-0]	S/W READ FLOW
101 EVT	1. SET GPIO AS INPUT
	2. ENABLE PU AND DISABLE PD
	3. READ

SIM CARD

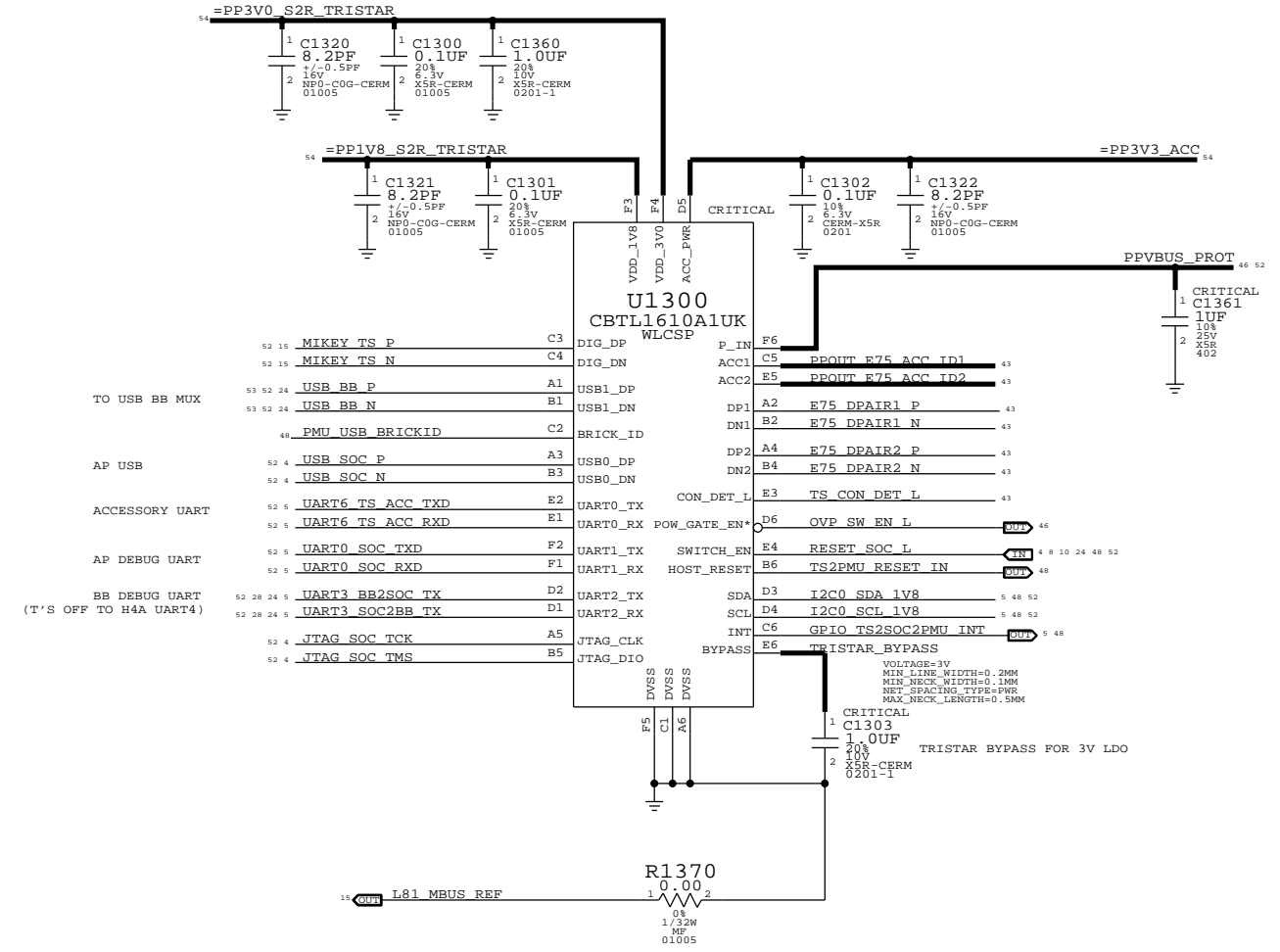


CKPLUS RULE EXCEPTIONS	REQUIRED
SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

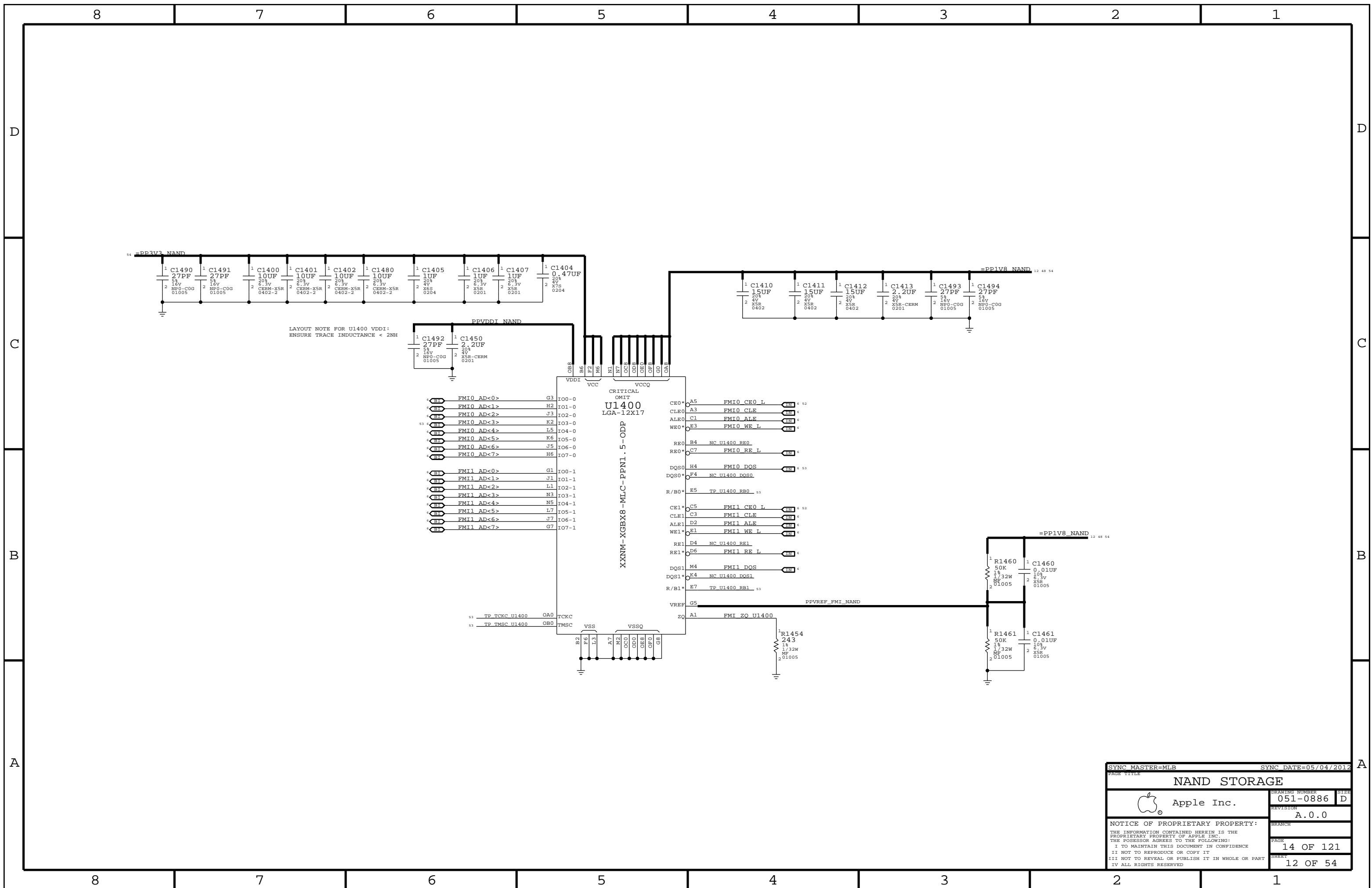
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SOC: MISC & ALIASES			
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343S0658 = TRISTAR 2, A1
 998-5855 = TRISTAR 2, TC
 343S0639 = TRISTAR 2, A0
 343S0614 = TRISTAR 1

TRISTAR



SYNC MASTER=N/A		SYNC DATE=N/A	
IO: TRISTAR			
Apple Inc.		DRAWING NUMBER	SIZE
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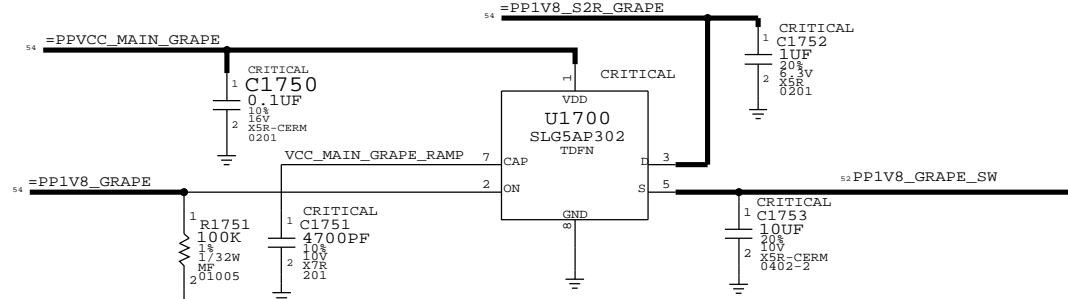
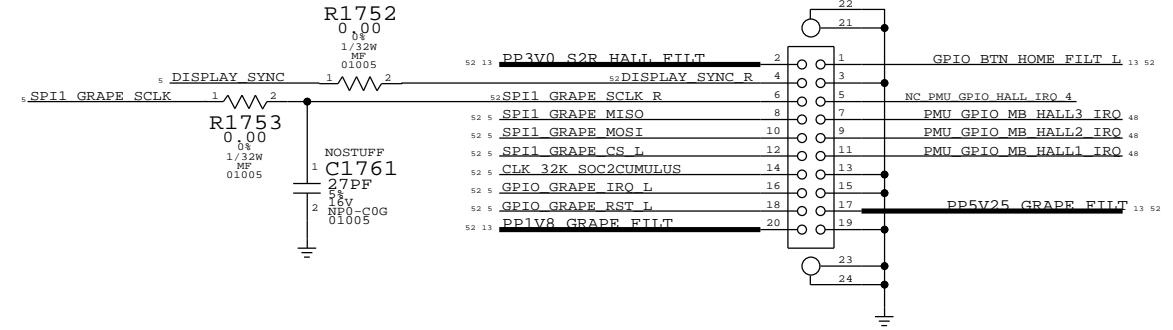
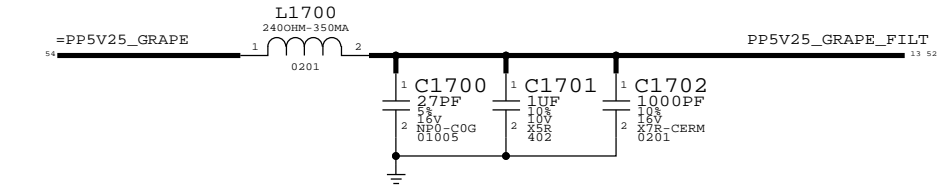
LAYOUT NOTE FOR U1400 VDDI:
ENSURE TRACE INDUCTANCE < 2NH

SYNC MASTER=MLB		SYNC DATE=05/04/2012	
NAND STORAGE			
Apple Inc.		DRAWING NUMBER	051-0886
		REVISION	A.0.0
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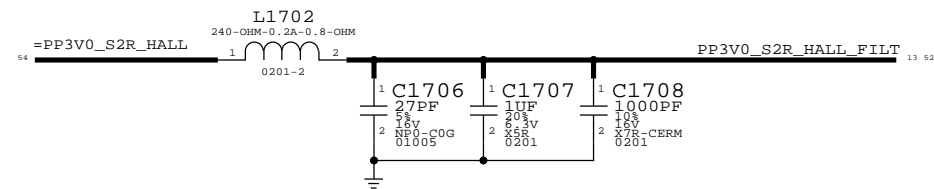
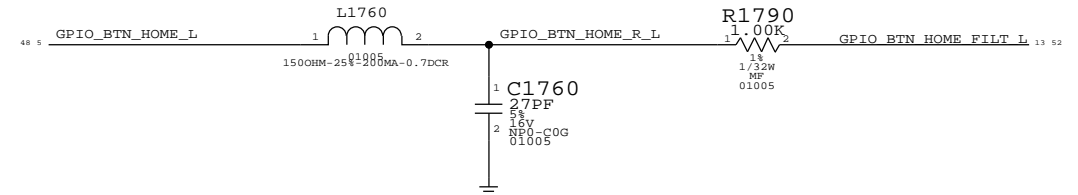
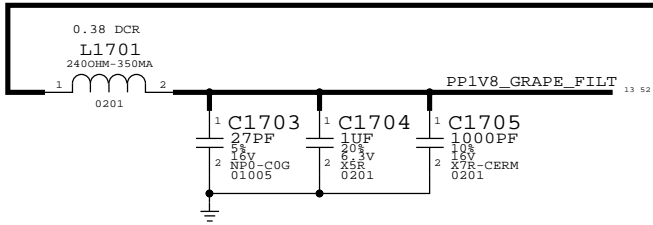
TOUCH SUBSYSTEM

RCPT - MLB 998-4526 -> 516S1054
(PLUG - FLEX 998-4527)

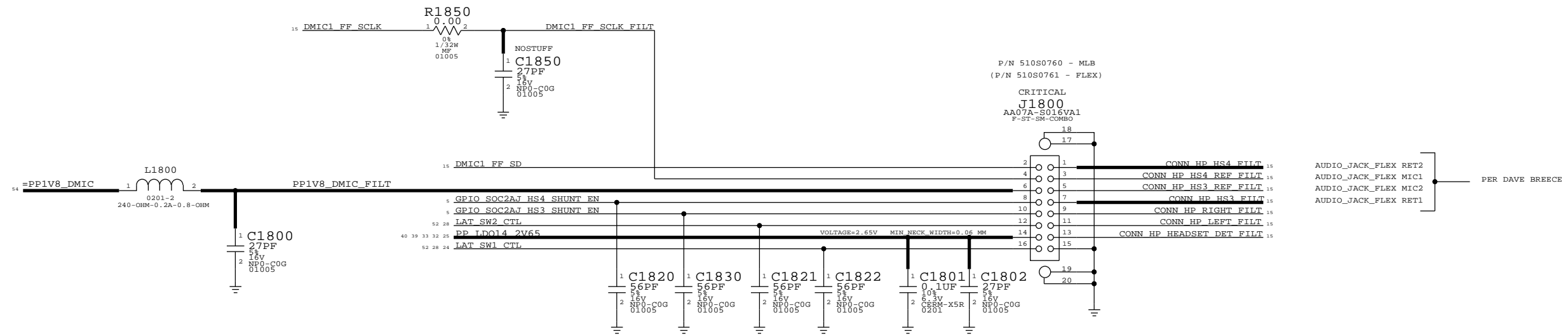
CRITICAL
J1700
503304-2010
F-ST-SM-1



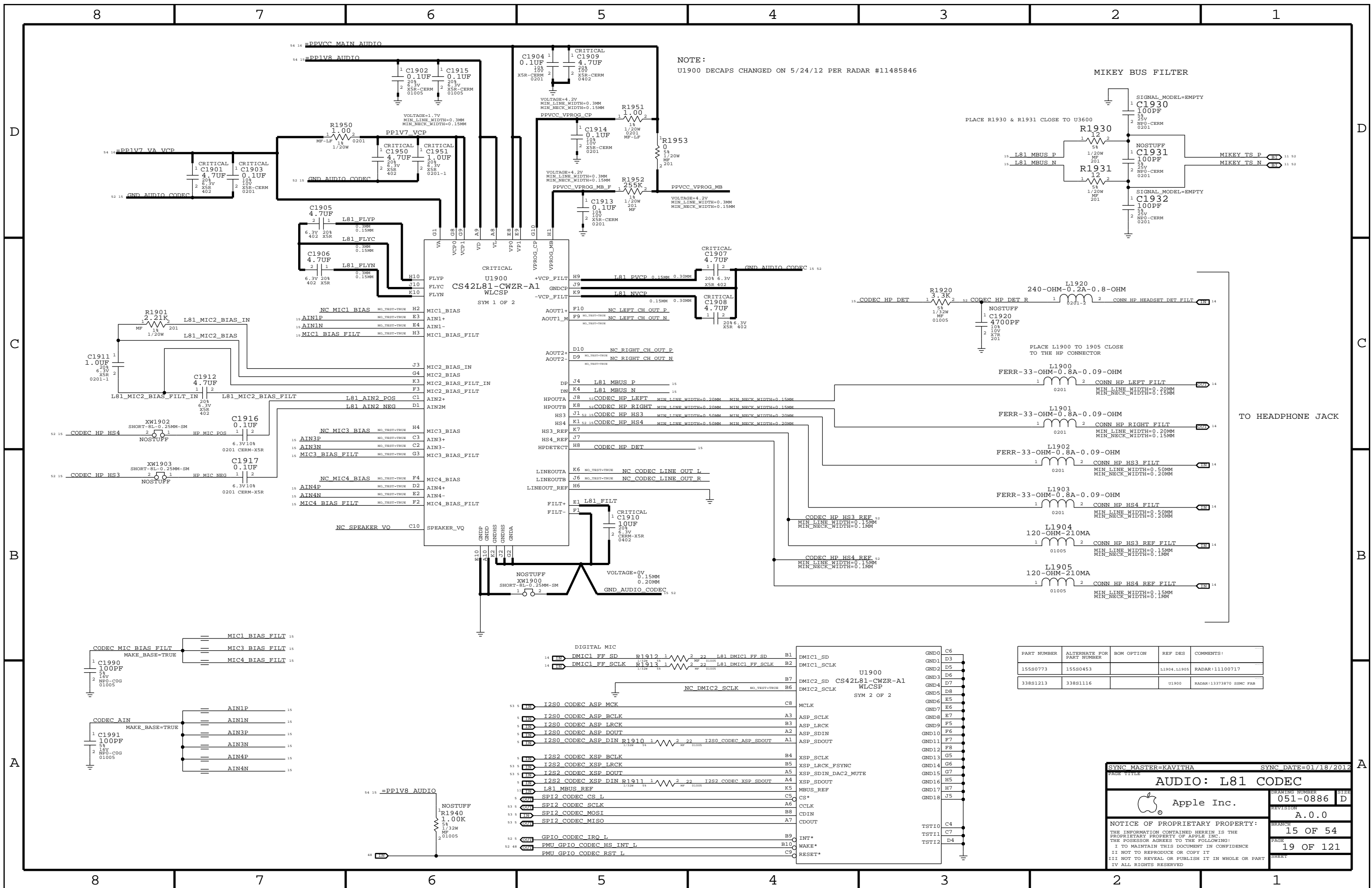
LAYOUT NOTE:
PUT THERMAL VIAS AROUND U2200 IN CASE OF SHORTED CONDITION



SYNC MASTER=N/A		SYNC DATE=06/21/2010	
PAGE TITLE TOUCH: SUPPORT CKT & CONN			
DRAWING NUMBER 051-0886		SIZE D	
REVISION A.0.0		BRANCH	
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PAGE 17 OF 121		SHEET 13 OF 54	

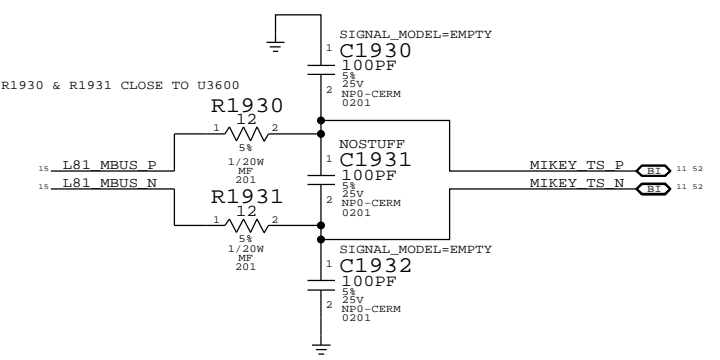


SYNC MASTER=N/A		SYNC DATE=03/31/2011	
AUDIO: HP FLEX CONN			
Apple Inc.		DRAWING NUMBER	SIZE
		051-0886	D
		REVISION	
		A.0.0	
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			14 OF 54
		PAGE	18 OF 121
		SHEET	



NOTE:
U1900 DECAPS CHANGED ON 5/24/12 PER RADAR #11485846

MIKEY BUS FILTER



PLACE R1930 & R1931 CLOSE TO U3600

PLACE L1900 TO L1905 CLOSE TO THE HP CONNECTOR

TO HEADPHONE JACK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15580773	15580453		L1904, L1905	RADAR:11100717
33881213	33881116		U1900	RADAR:13373870 SEMC FAB

SYNC MASTER=KAVITHA SYNC DATE=01/18/2012

AUDIO: L81 CODEC

Apple Inc.

DRAWING NUMBER: 051-0886 SIZE: D

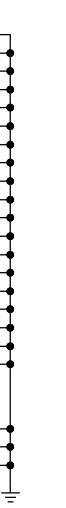
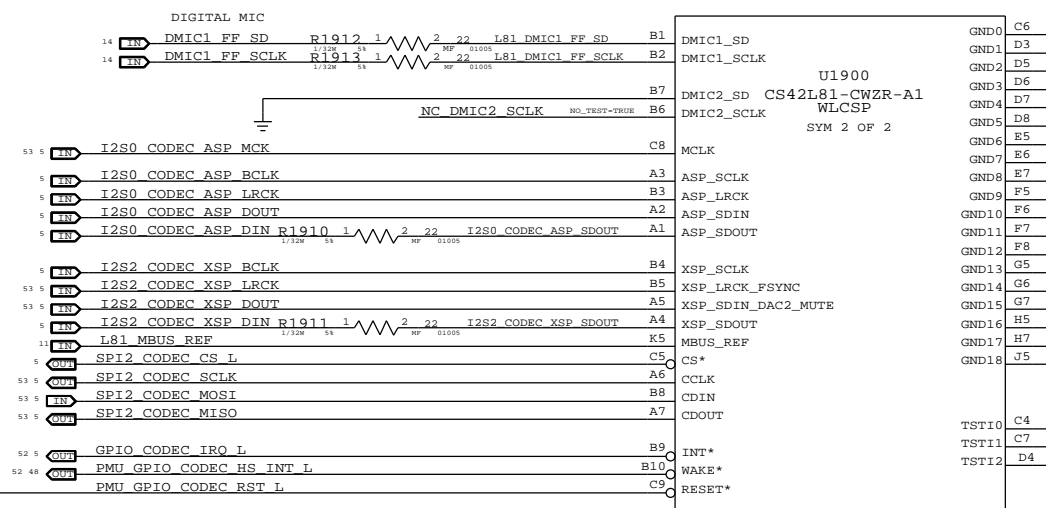
REVISION: A.0.0

BRANCH: 15 OF 54

PAGE: 19 OF 121

SHEET

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D

C

B

A

D

C

B

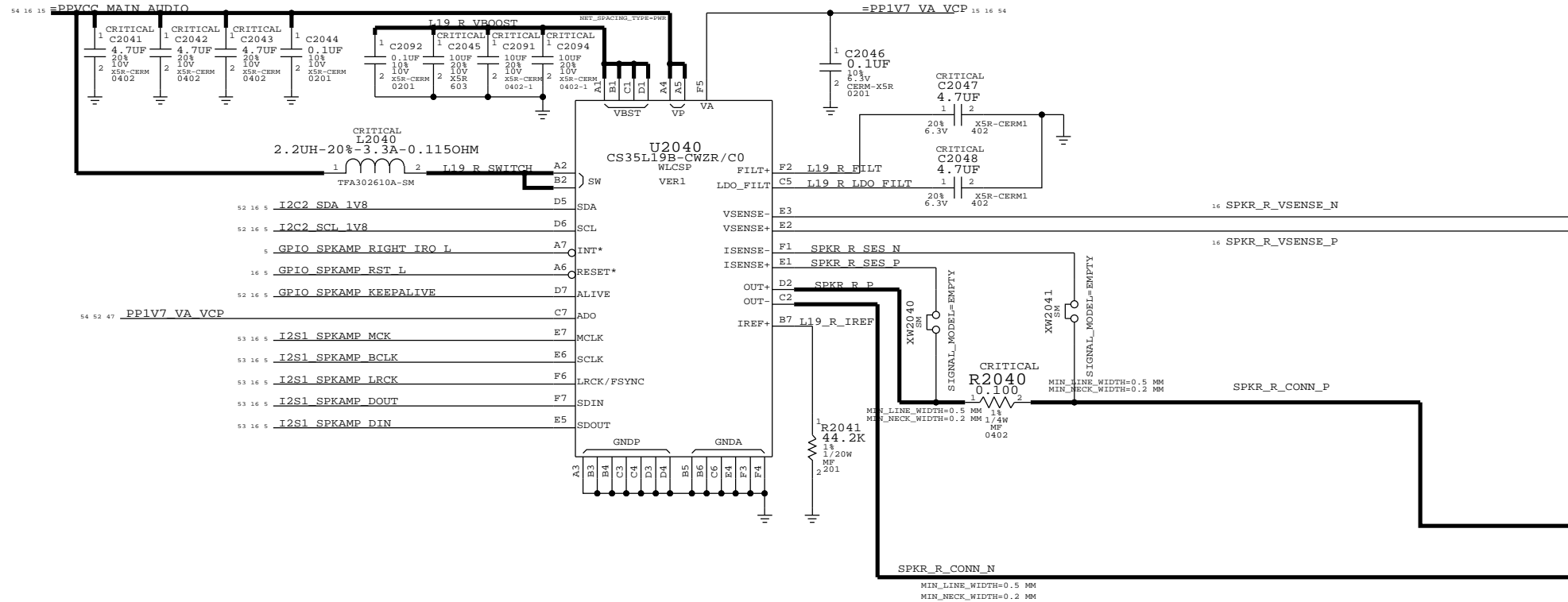
A

8 7 6 5 4 3 2 1

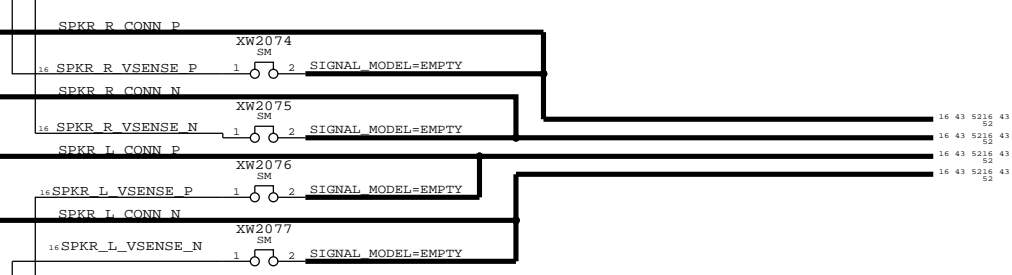
8 7 6 5 4 3 2 1

RIGHT SPEAKER AMP

I2C ADDRESS: 100001X

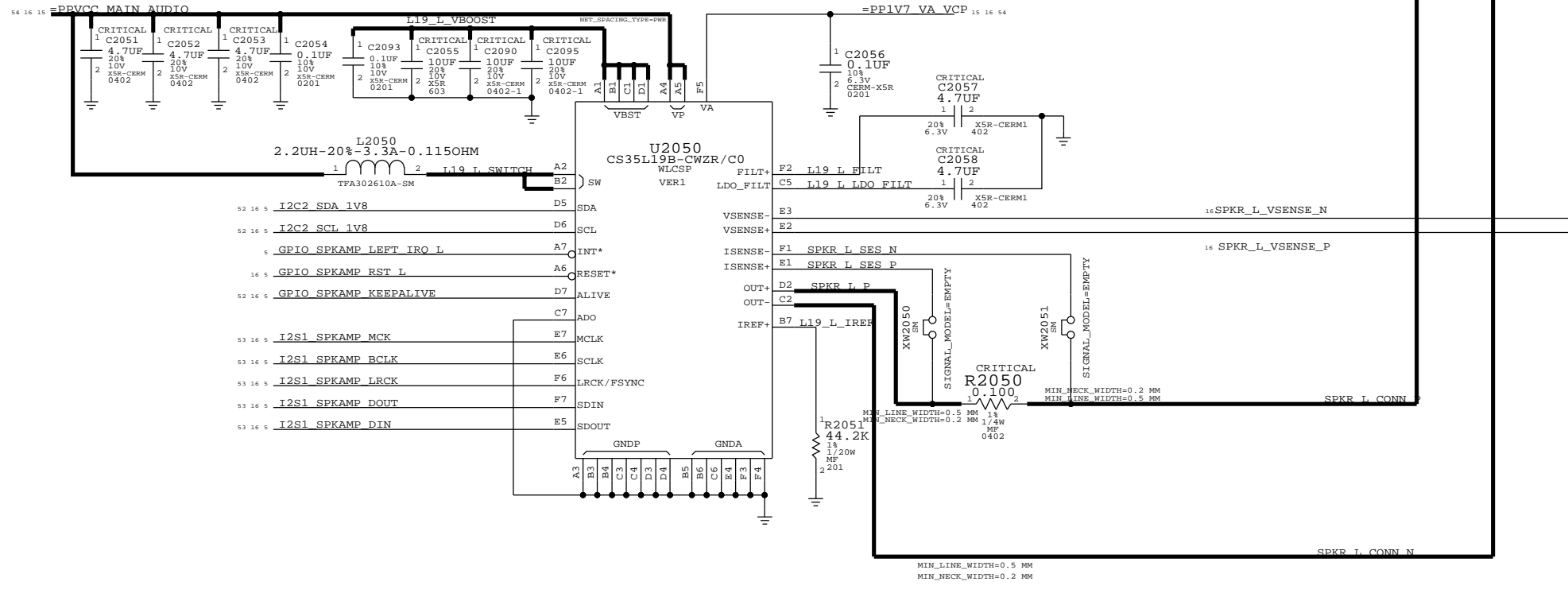


SPEAKER CONNECTOR



LEFT SPEAKER AMP

I2C ADDRESS: 100000X



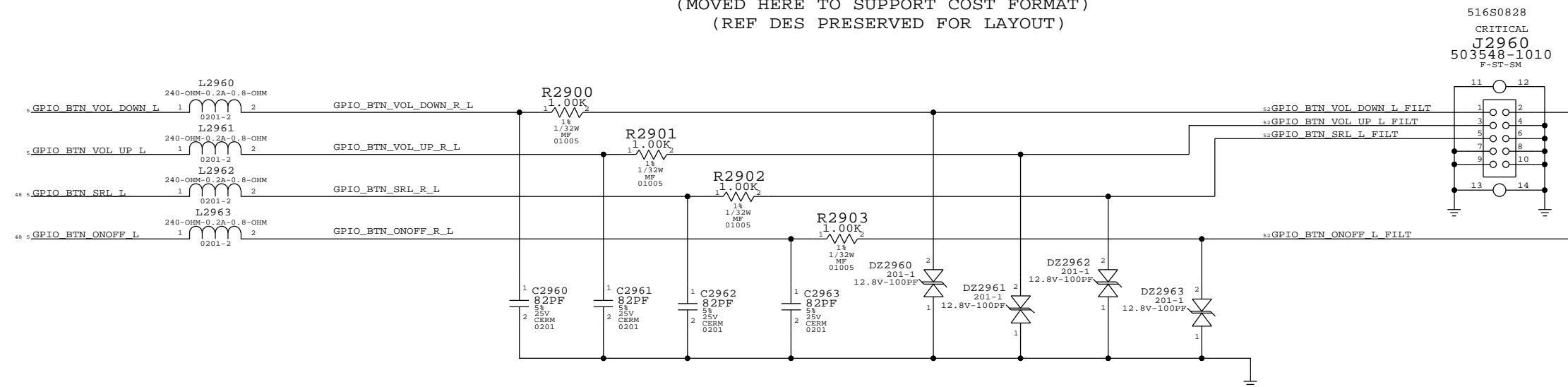
UPDATED: DEC 13

1. ALL THE EMI/DESENSE FILTER COMPONENTS HAVE BEEN REMOVED BASED ON PERFORMANCE ON J65
2. THE CURRENT VERSION OF L19 IS B0 AND WILL CHANGE TO C0 BY MARCH 2013. C0 FIXES PROCESS ISSUES.

SYNC MASTER=KAVITHA		SYNC DATE=01/18/2012	
PAGE TITLE AUDIO: CS35L19A AMPS			
DRAWING NUMBER 051-0886		SIZE D	
REVISION A.0.0		BRANCH	
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PAGE 20 OF 121		SHEET 16 OF 54	

BUTTON CONNECTOR

(MOVED HERE TO SUPPORT COST FORMAT)
(REF DES PRESERVED FOR LAYOUT)



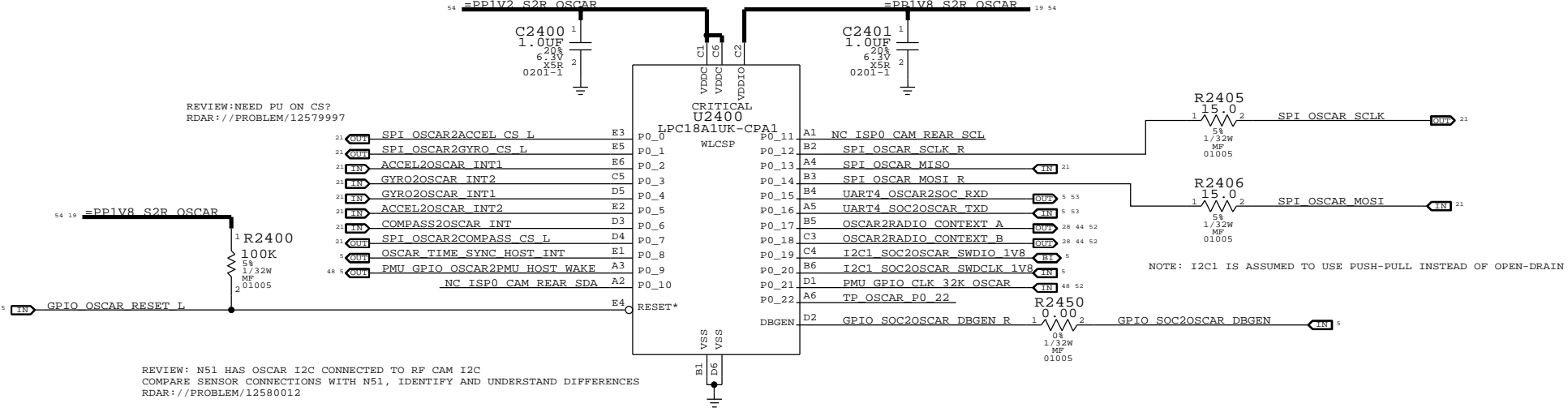
516S0828
CRITICAL
J2960
503548-1010
P-ST-SM

SYNC MASTER=N/A		SYNC DATE=N/A	
BUTTON: CONN			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
		A.0.0	
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		PAGE	21 OF 121
		SHEET	17 OF 54

OSCAR

APN 337S4416

OSCAR VDDIO = 1.8V HIBERNATE (NEED TO WAKE HOST)
OSCAR CORE = 1.2V HIBERNATE (NEED TO RUN IN S2R)

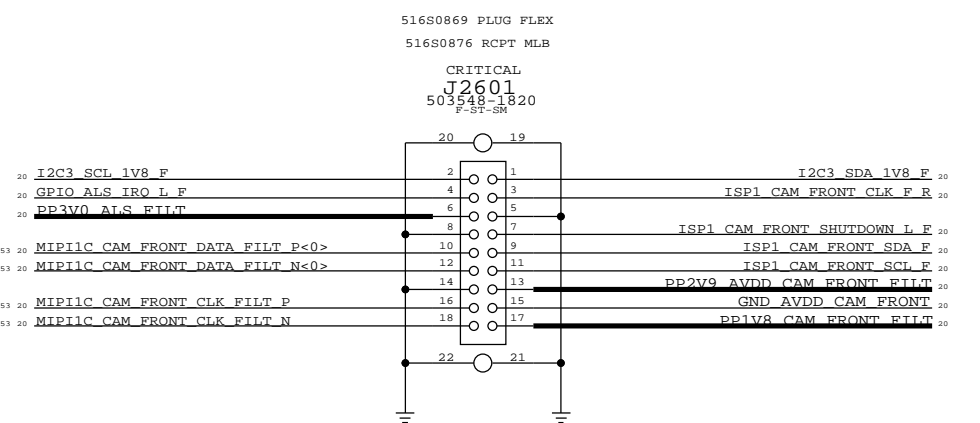
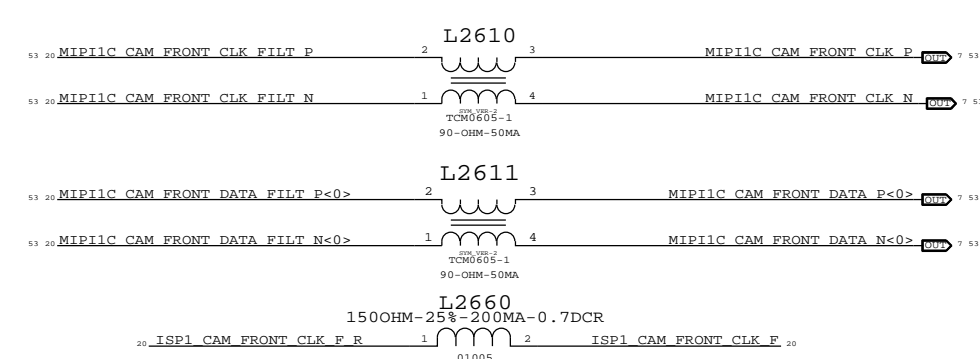
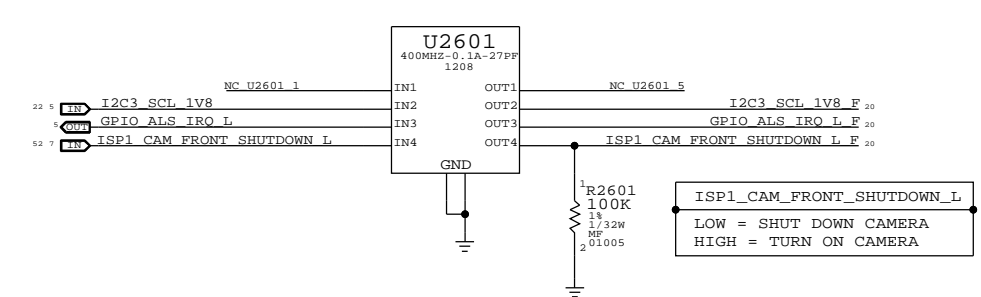
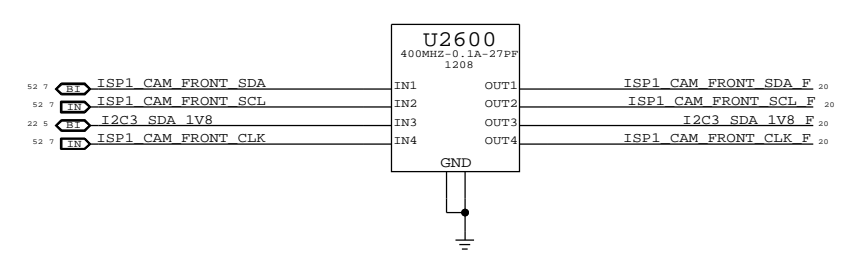
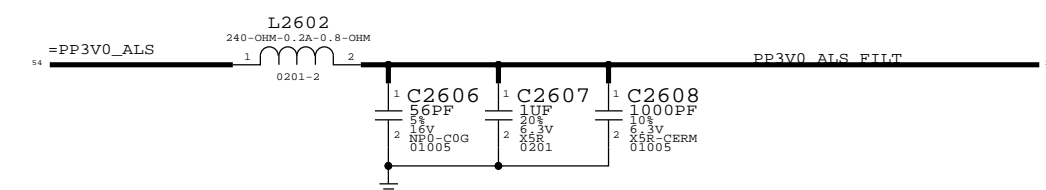
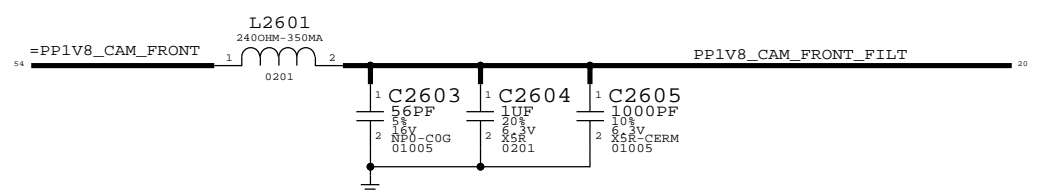
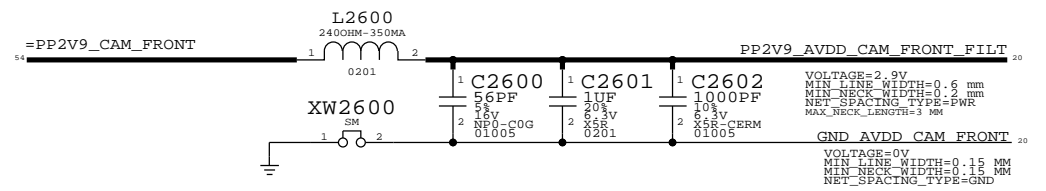


REVIEW: NEED PU ON CS?
RDAR://PROBLEM/12579997

REVIEW: N51 HAS OSCAR I2C CONNECTED TO RF CAM I2C
COMPARE SENSOR CONNECTIONS WITH N51, IDENTIFY AND UNDERSTAND DIFFERENCES
RDAR://PROBLEM/12580012

SYNC MASTER=j72.MLB.C		SYNC DATE=11/26/2012	
SENSOR: OSCAR			
		DRAWING NUMBER	051-0886
		REVISION	A.0.0
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		PAGE	24 OF 121
		SHEET	19 OF 54
		SIZE	D

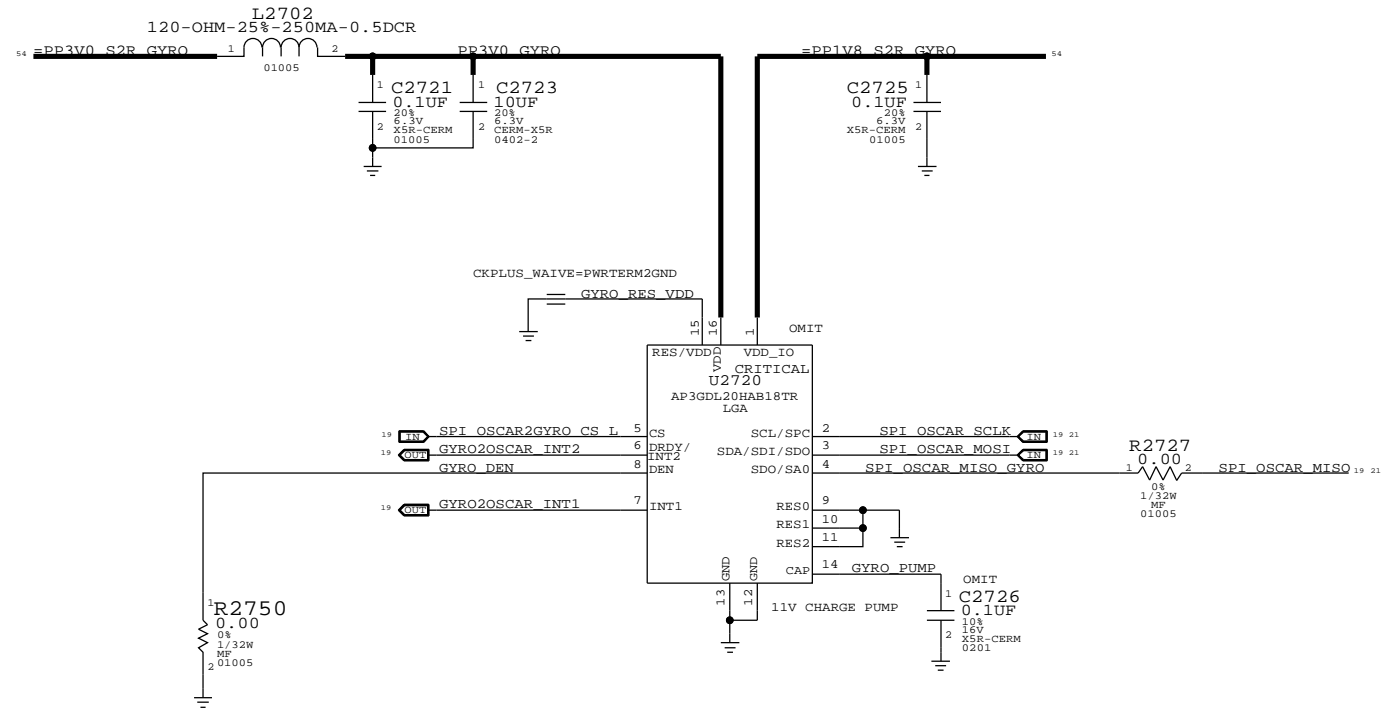
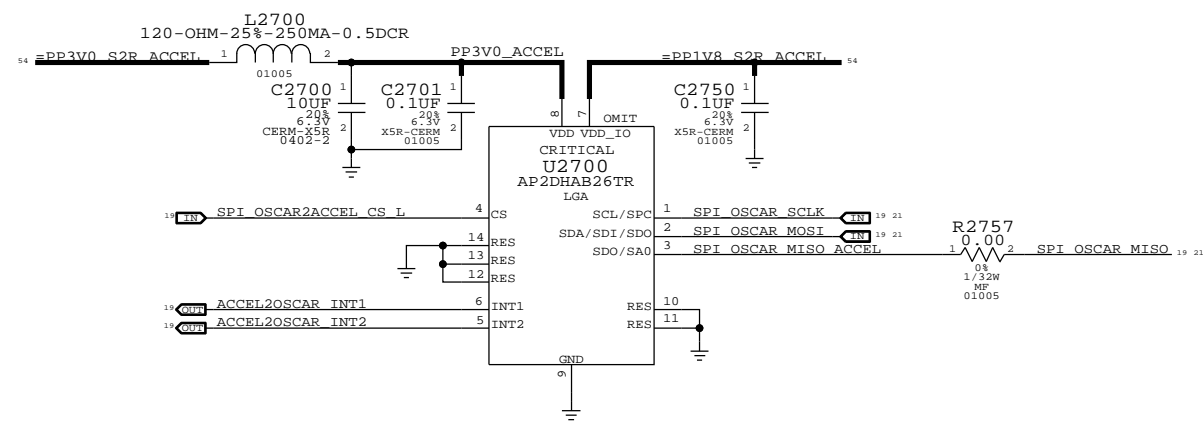
VGA FRONT CAMERA CONNECTOR



PAGE TITLE		SYNC MASTER=J85 MLB C		SYNC DATE=12/03/2012	
CAMERA: FF-ALS CONN & FILTERS					
Apple Inc.		DRAWING NUMBER	051-0886	SIZE	D
		REVISION	A.0.0		
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		PAGE	26 OF 121		
		SHEET	20 OF 54		

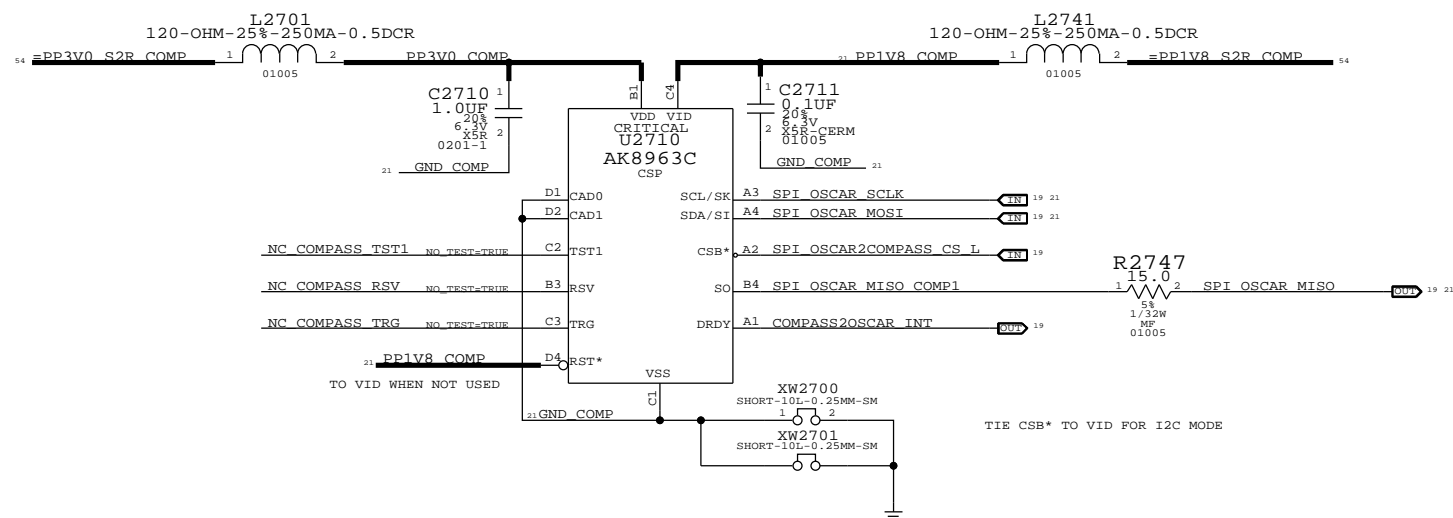
GYRO

ACCELEROMETER



COMPASS

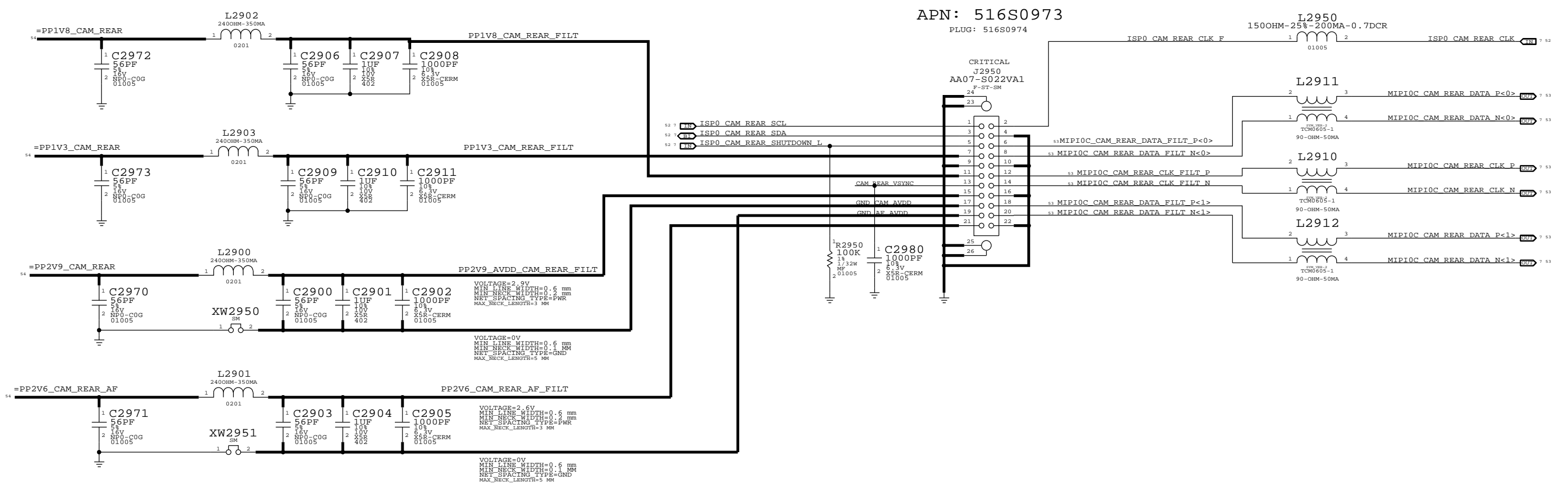
APN 338S1014



SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE: SENSOR: ACCEL, COMPASS, GYRO			
DRAWING NUMBER: 051-0886		SIZE: D	
REVISION: A.0.0		BRANCH:	
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REAR CAMERA CONNECTOR

APN: 516S0973
PLUG: 516S0974

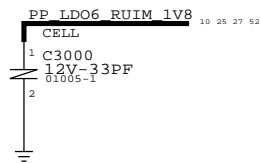


SYNC MASTER=N/A		SYNC DATE=N/A	
CAMERA: REAR CONN & FILTERS			
Apple Inc.		DRAWING NUMBER	SIZE
		051-0886	D
		REVISION	
		A.0.0	
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		PAGE	
		29 OF 121	
		SHEET	
		23 OF 54	

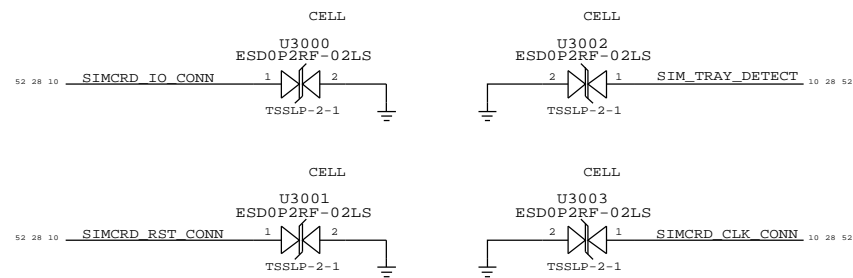
AP INTERFACE & DEBUG CONNECTORS

PROBE POINTS

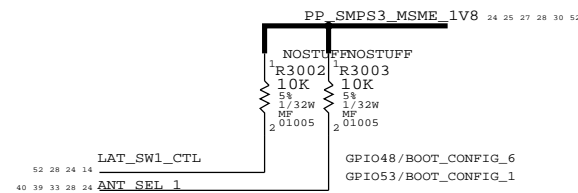
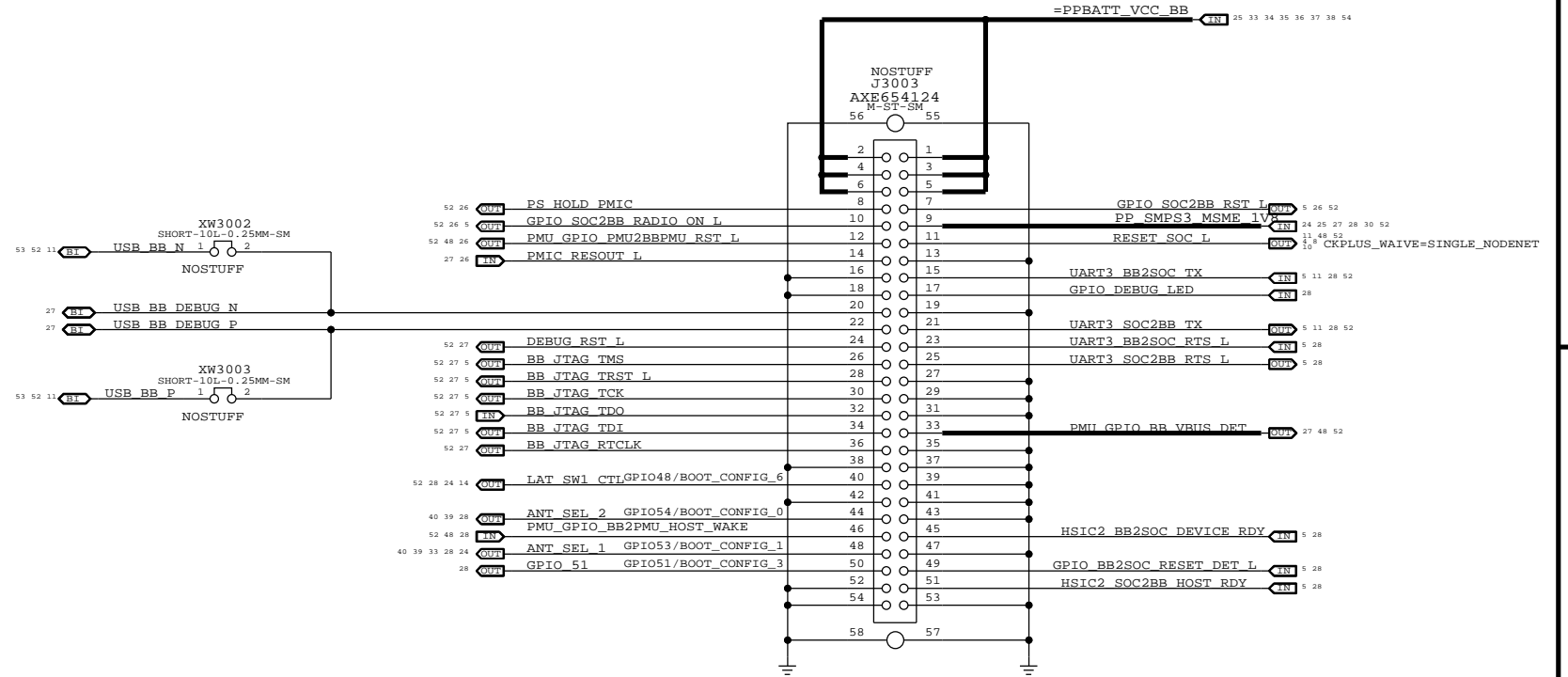
- PP3000
P4MM
1 BB_ERROR_FLAG 28
- PP3001
P4MM
1 SLEEP_CLK_32K 26 27
- PP3002
P4MM
1 PMIC_SSBI 26 27
- PP3003
P4MM
1 19P2M_MDM 26 27
- PP3008
P4MM
1 WTR_SSBI_TX_GPS 28 29
- PP3009
P4MM
1 WTR_SSBI_PRX_DRX 28 29
- PP3010
P4MM
1 WTR_RX_ON 28 29
- PP3011
P4MM
1 WTR_RF_ON 28 29
- PP3012
P4MM
1 UART_WLAN2BB_LTE_COEX 28 44
- PP3013
P4MM
1 UART_BB2WLAN_LTE_COEX 28 44



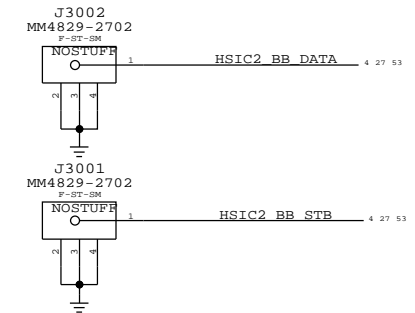
SIM CARD ESD PROTECTION



DEBUG CONNECTOR

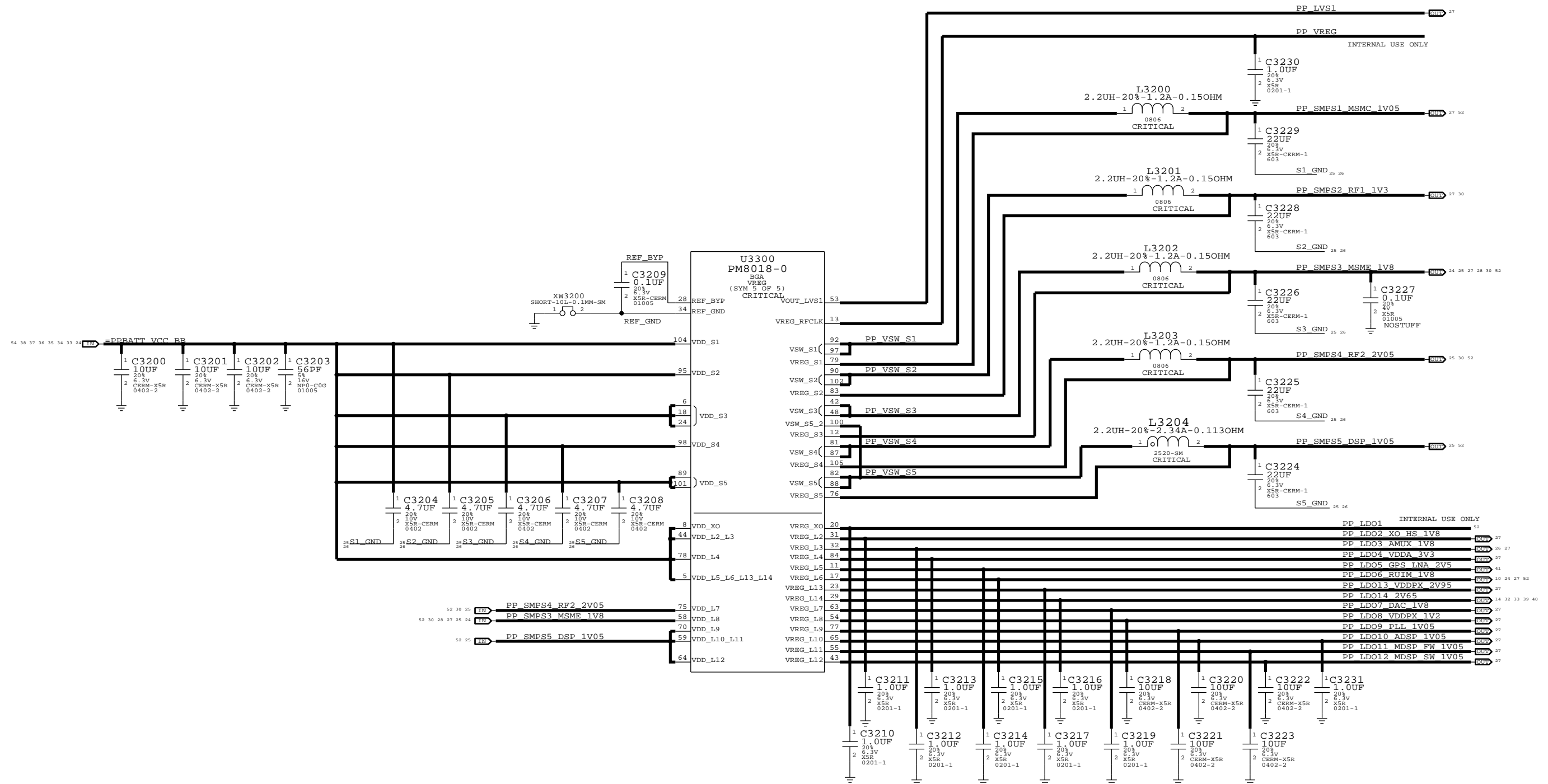


BOOT OPTIONS	BOOT_CONFIG SW REGISTER VALUE	GPIO/BOOT_CONFIG CONFIGURATION								
		6	5	4	3	2	1	0		
BOOT_DEFAULT_OPTION	0x00	X	0	0	0	0	0	0	0	X
BOOT_NAND_OPTION	0x01	X	1	0	0	0	0	0	0	1
BOOT_HSIC_OPTION	0x02	X	1	0	0	0	0	0	1	0
BOOT_USB_OPTION	0x03	X	1	0	0	0	0	0	1	1
ENABLE SAHARA PROTOCOL	0x08	X	1	0	0	1	0	X	X	X



PAGE TITLE CELL:AP INTERFACE & DEBUG CONNECTORS		
Apple Inc.	DRAWING NUMBER 051-0886	SIZE D
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PAGE 30 OF 121		SHEET 24 OF 54

PMU (1 OF 2)



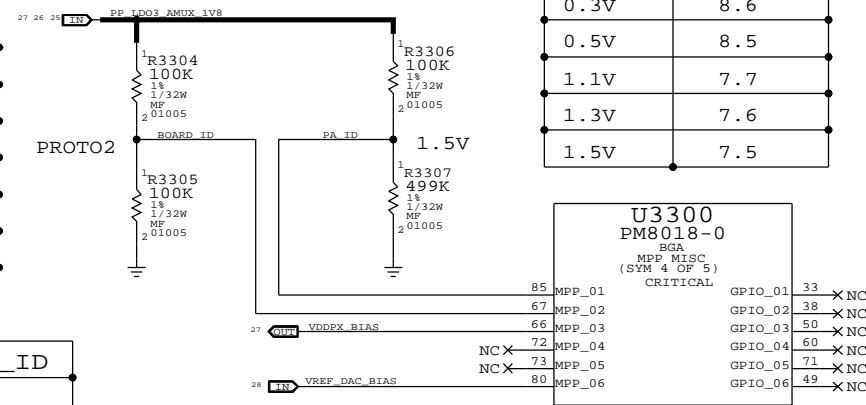
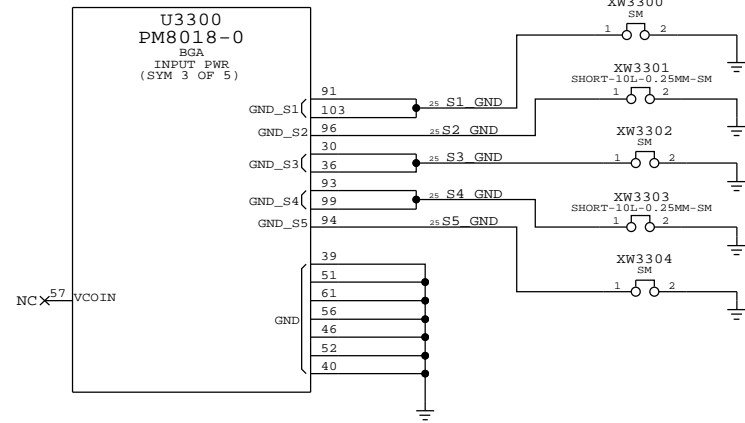
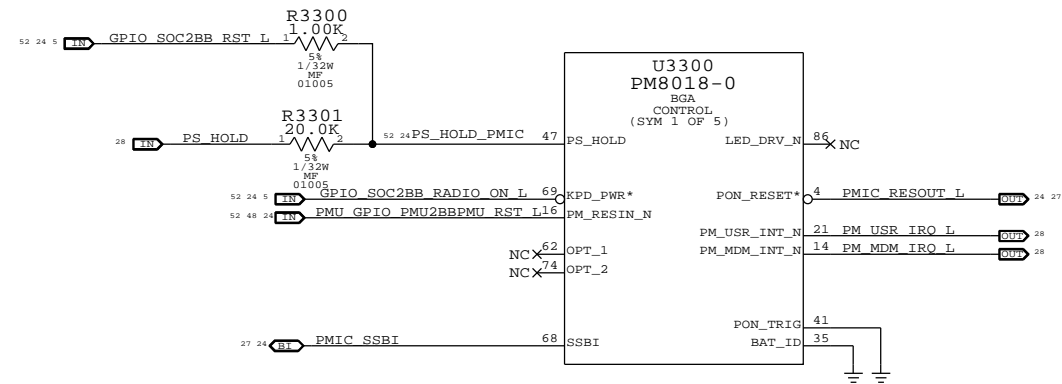
PAGE TITLE CELL: BASEBAND PMU (1 OF 2)		
Apple Inc.	DRAWING NUMBER	051-0886
	REVISION	A.0.0
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PMU (2 OF 2)

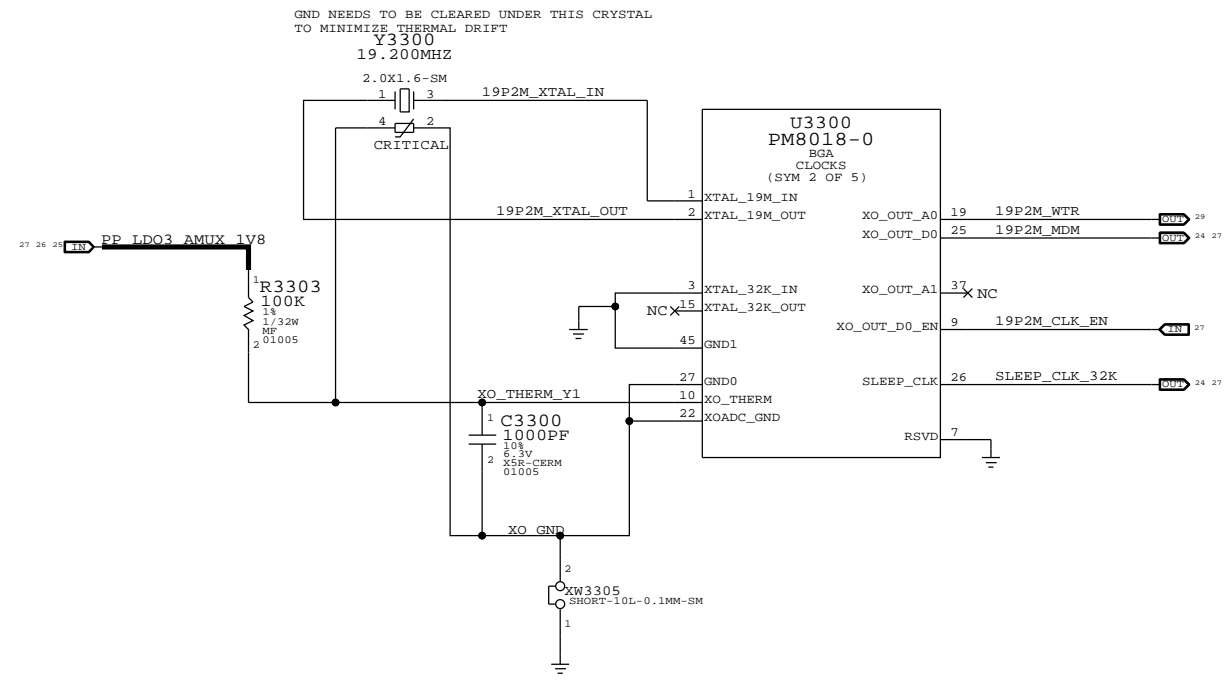
BOARD_ID	REVISION
0.7V	PROTO1
0.9V	PROTO2
1.1V	EVT1
1.3V	EVT2
1.5V	DVT
1.7V	PVT

BB GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX

PA_ID	MAV VER
0.1V	8.7
0.3V	8.6
0.5V	8.5
1.1V	7.7
1.3V	7.6
1.5V	7.5



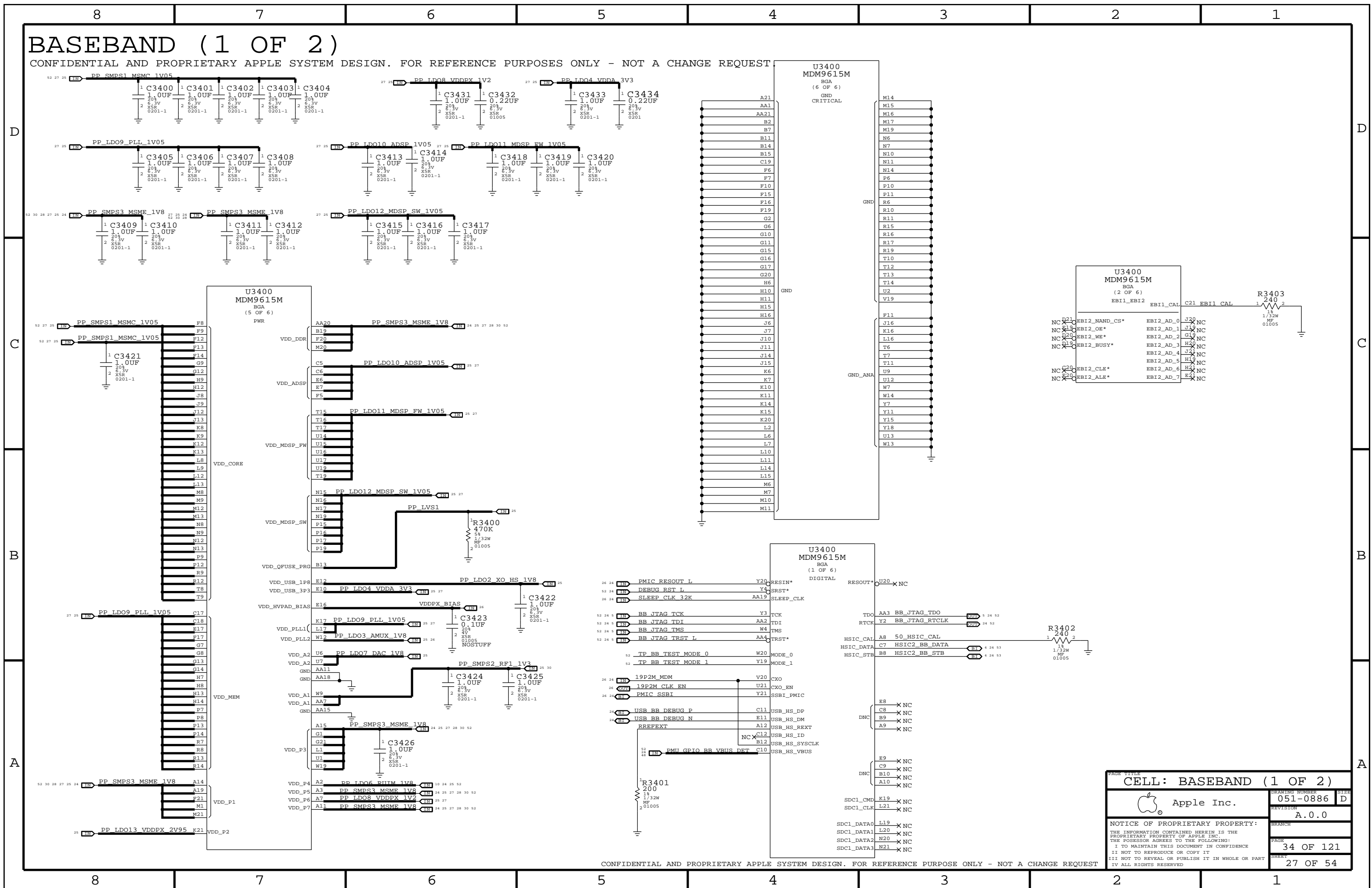
AP SECTION NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.



CELL: BASEBAND PMU (2 OF 2)		
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	REVISION	A.0.0
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BASEBAND (1 OF 2)

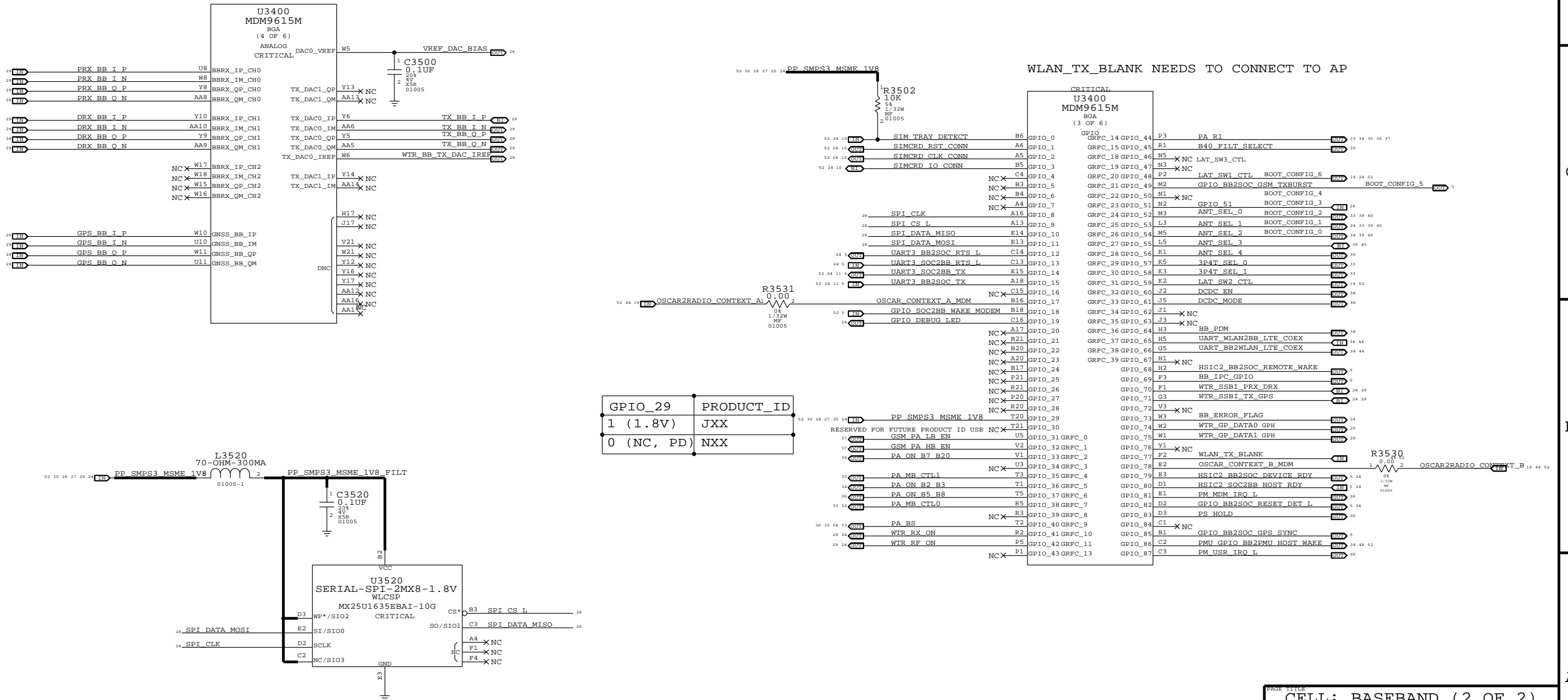
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST



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BASEBAND (2 OF 2)



CELL: BASEBAND (2 OF 2)

Apple Inc.

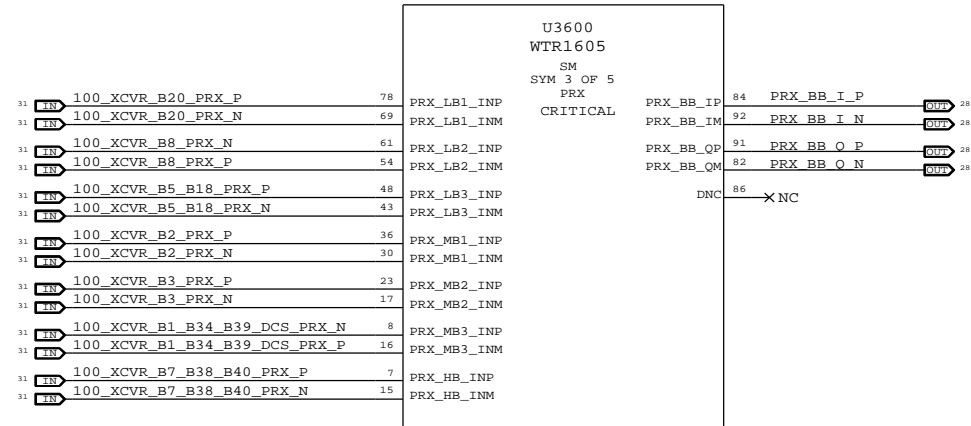
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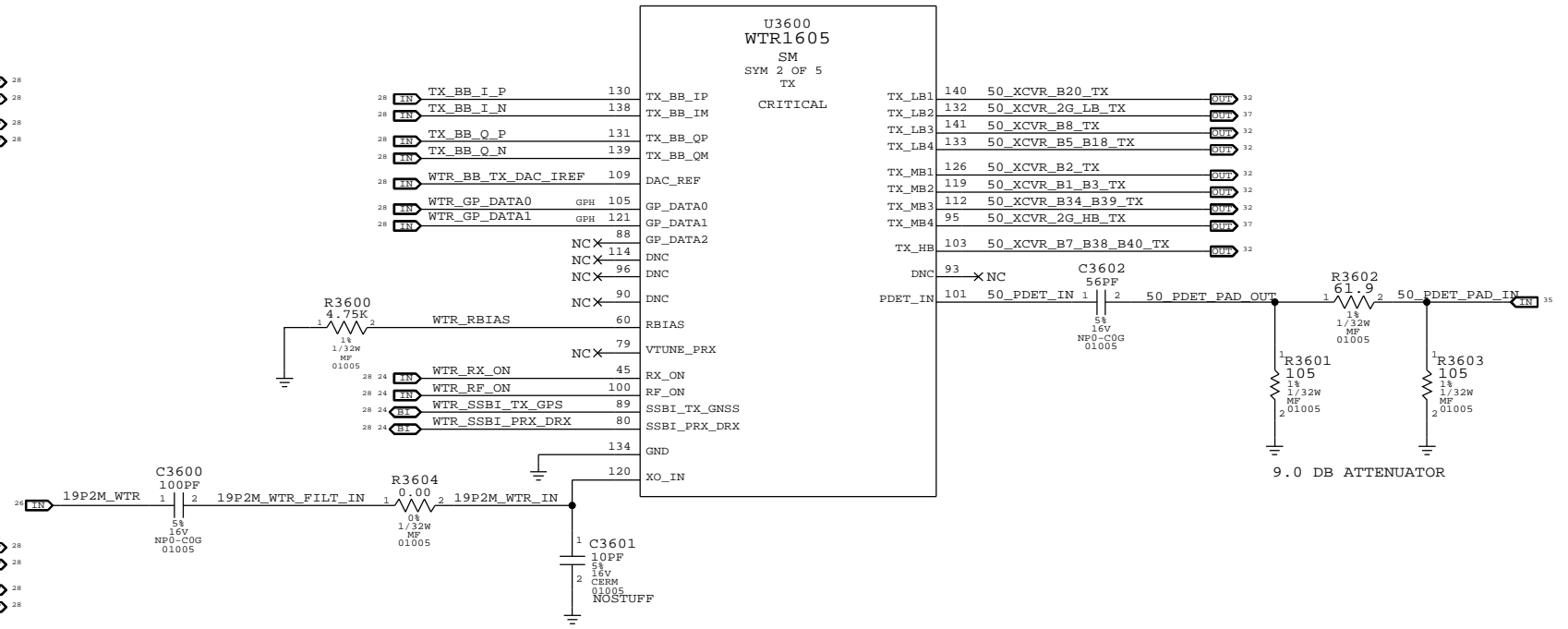
PAGE: 35 OF 121
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RF TRANSCEIVER (1 OF 2)

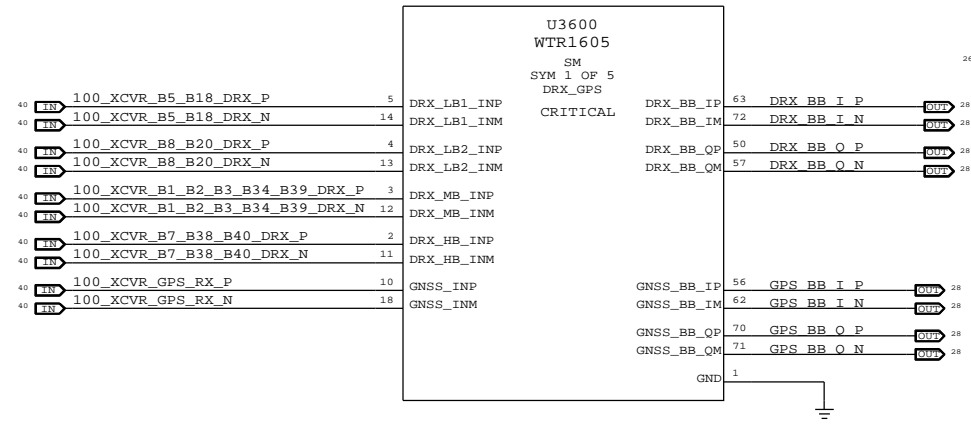
PRX TRANSCEIVER RF AND IQ PORTS



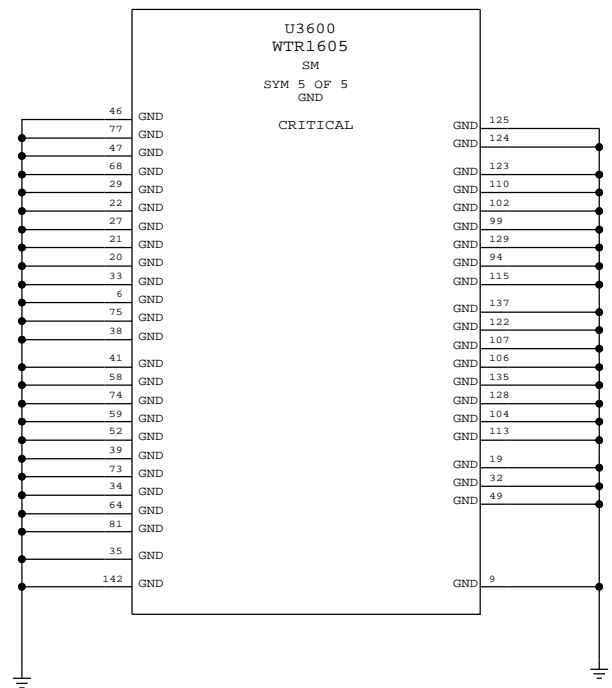
TRANSCEIVER PHASE CONTROL, TX RF & IQ PORTS



DRX TRANSCEIVER RF AND IQ PORTS

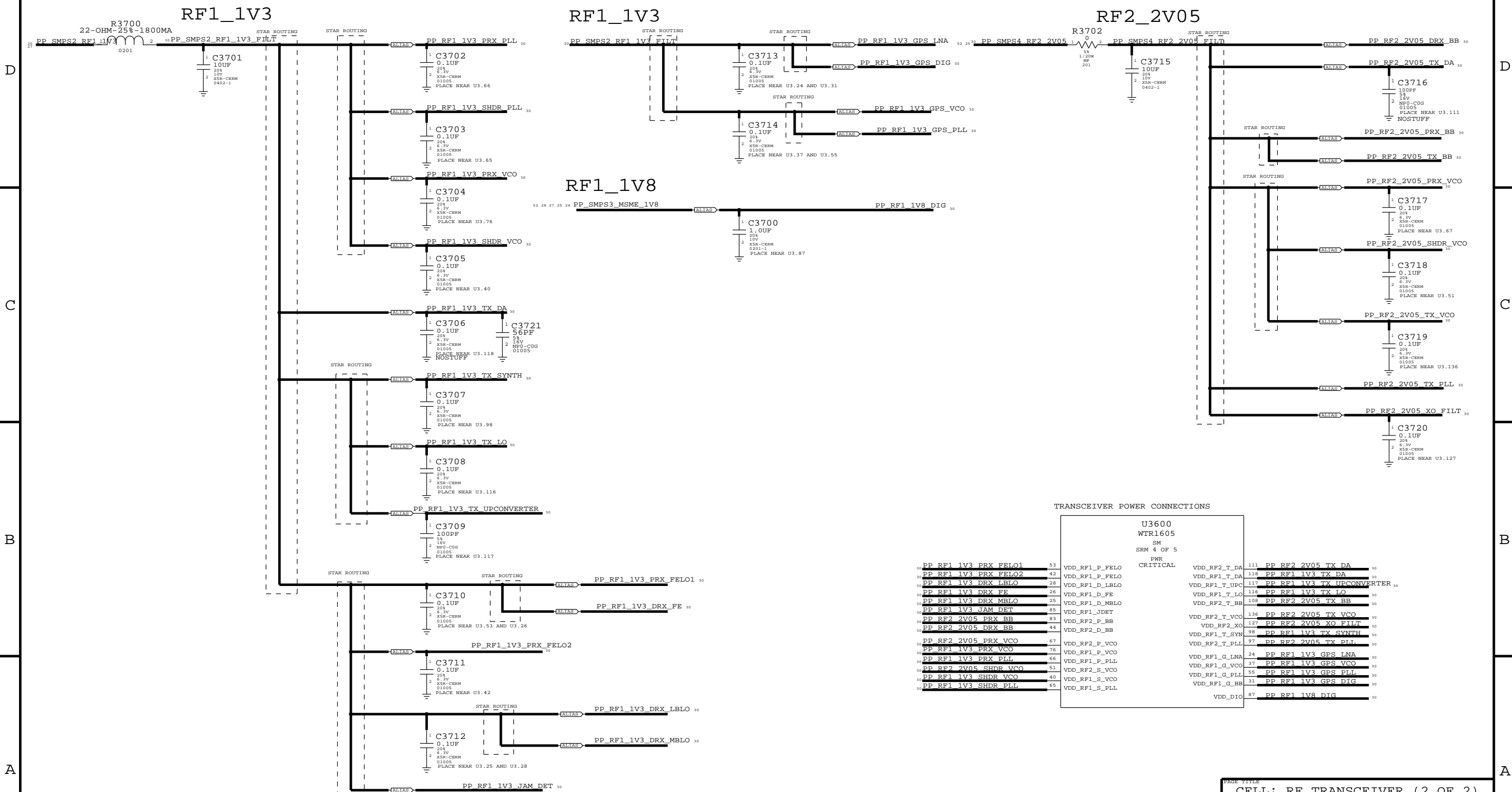


TRANSCEIVER GROUND CONNECTIONS



PAGE TITLE		CELL: RF TRANSCEIVER (1 OF 2)	
DRAWING NUMBER		051-0886	SIZE D
REVISION		A.0.0	
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RF TRANSCEIVER (2 OF 2)



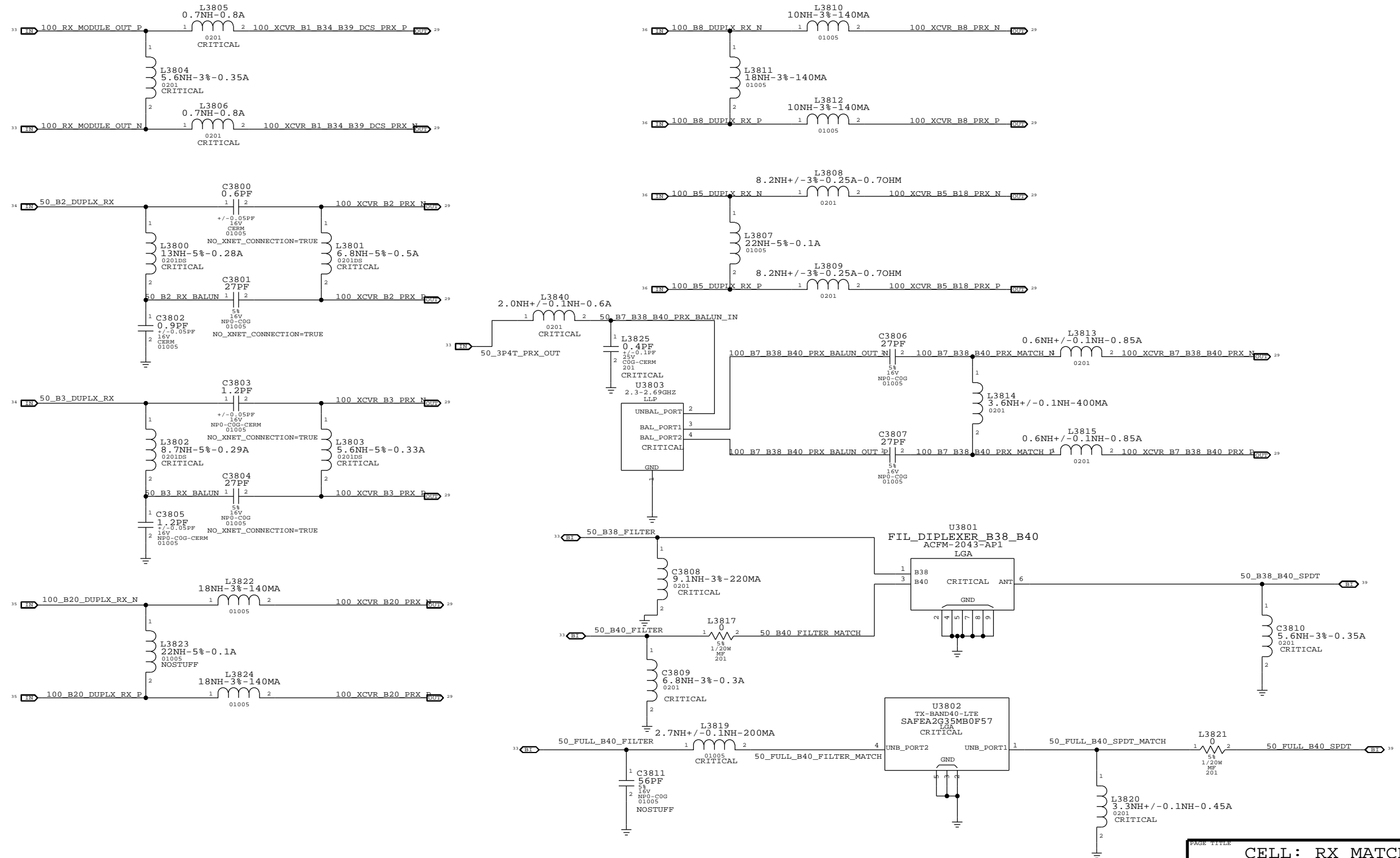
TRANSCEIVER POWER CONNECTIONS

U3600		U3600	
WTR1605		WTR1605	
SM		SM	
SRM 4 OF 5		SRM 4 OF 5	
PWR		PWR	
CRITICAL		CRITICAL	
30 PP RF1 1V3 PRX FELO1	53 VDD_RF1_P_FELO	VDD_RF2_T_DA	111 PP RF2 2V05 TX DA
30 PP RF1 1V3 PRX FELO2	42 VDD_RF1_P_FELO	VDD_RF1_T_DA	118 PP RF1 1V3 TX DA
30 PP RF1 1V3 DRX LBLO	28 VDD_RF1_D_LBLO	VDD_RF1_T_UPC	117 PP RF1 1V3 TX UPCONVERTER
30 PP RF1 1V3 DRX FE	26 VDD_RF1_D_FE	VDD_RF1_T_LO	116 PP RF1 1V3 TX LO
30 PP RF1 1V3 DRX MBLO	25 VDD_RF1_D_MBLO	VDD_RF2_T_BB	108 PP RF2 2V05 TX BB
30 PP RF1 1V3 JAM DET	85 VDD_RF1_JDET	VDD_RF2_T_VCO	136 PP RF2 2V05 TX VCO
30 PP RF2 2V05 PRX BB	83 VDD_RF2_P_BB	VDD_RF2_XO	127 PP RF2 2V05 XO FILT
30 PP RF2 2V05 DRX BB	44 VDD_RF2_D_BB	VDD_RF1_T_SYN	98 PP RF1 1V3 TX SYNTH
30 PP RF2 2V05 PRX VCO	67 VDD_RF2_P_VCO	VDD_RF2_T_PLL	97 PP RF2 2V05 TX PLL
30 PP RF1 1V3 PRX VCO	76 VDD_RF1_P_VCO	VDD_RF1_G_LNA	24 PP RF1 1V3 GPS LNA
30 PP RF1 1V3 PRX PLL	66 VDD_RF1_P_PLL	VDD_RF1_G_VCO	37 PP RF1 1V3 GPS VCO
30 PP RF2 2V05 SHDR VCO	51 VDD_RF2_S_VCO	VDD_RF1_G_PLL	55 PP RF1 1V3 GPS PLL
30 PP RF1 1V3 SHDR VCO	40 VDD_RF1_S_VCO	VDD_RF1_G_BB	31 PP RF1 1V3 GPS DIG
30 PP RF1 1V3 SHDR PLL	65 VDD_RF1_S_PLL	VDD_DIO	87 PP RF1 1V8 DIG

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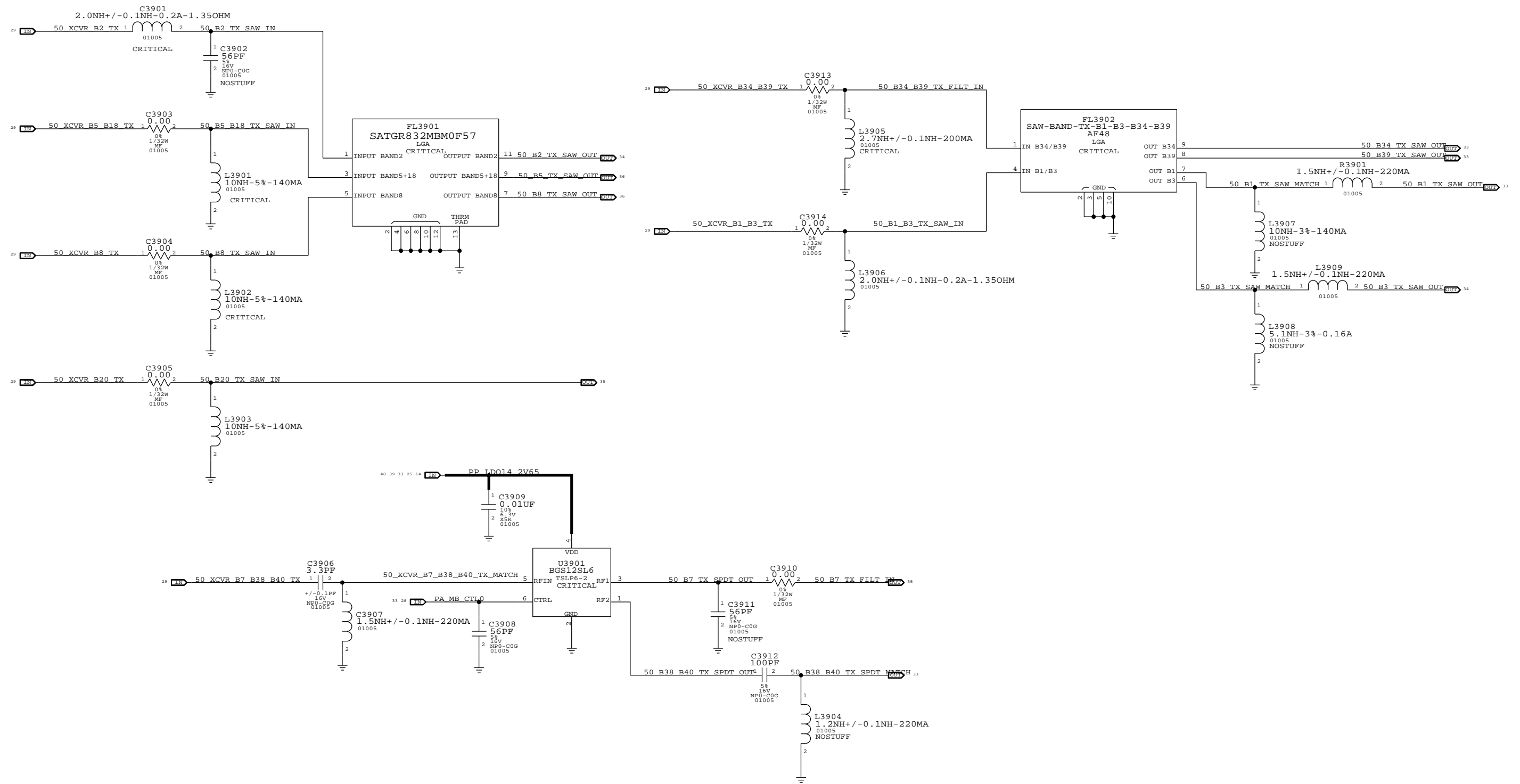
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	PAGE	37 OF 121
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	SIZE	D

RX MATCHING



PAGE TITLE		
CELL: RX MATCHING		
Apple Inc.	DRAWING NUMBER	SIZE
	051-0886	D
REVISION		
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BRANCH		
PAGE		
38 OF 121		
SHEET		
31 OF 54		

TX INTERSTAGE FILTERS

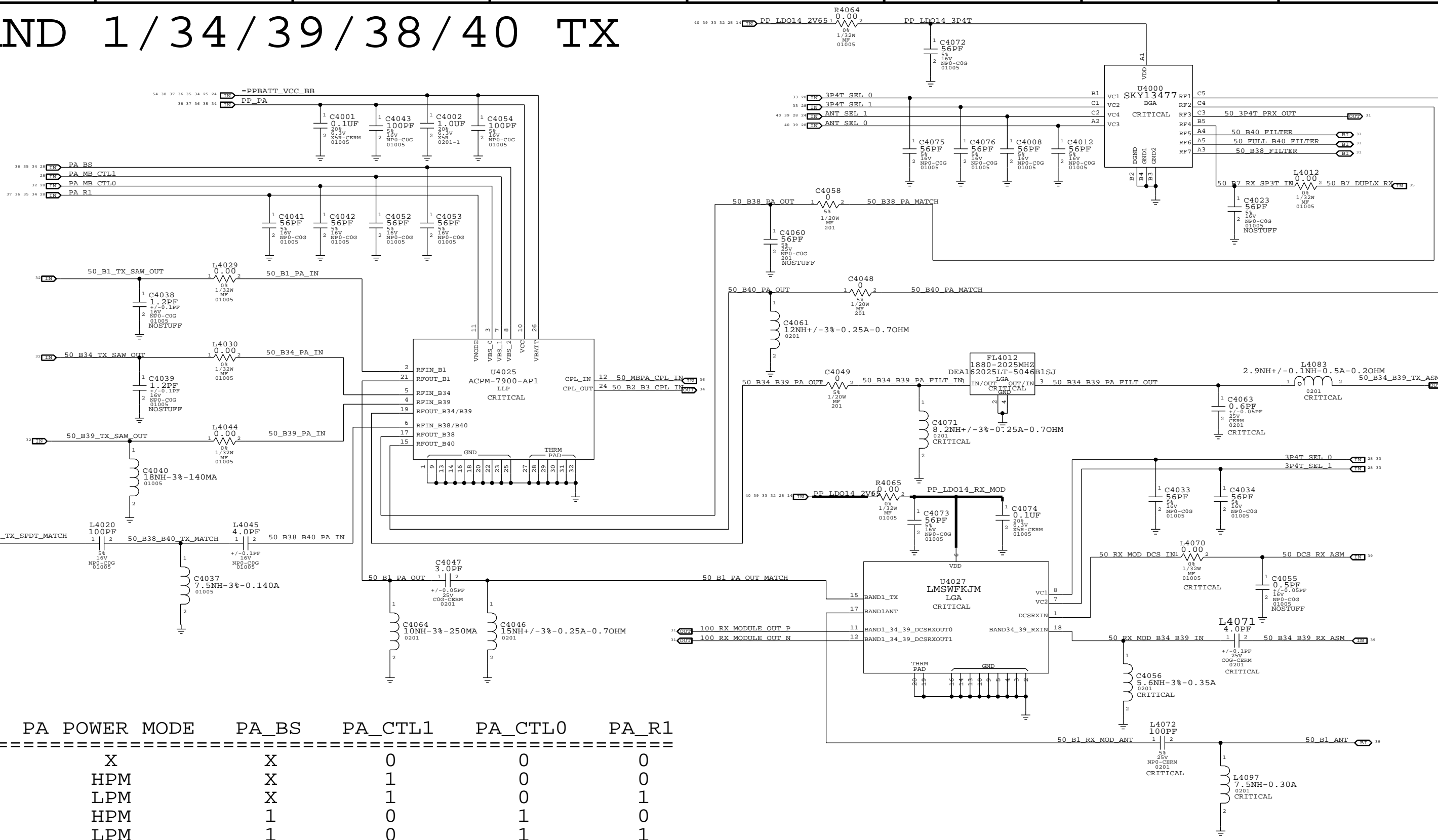


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BAND 1 / 34 / 39 / 38 / 40 TX

D
C
B
A

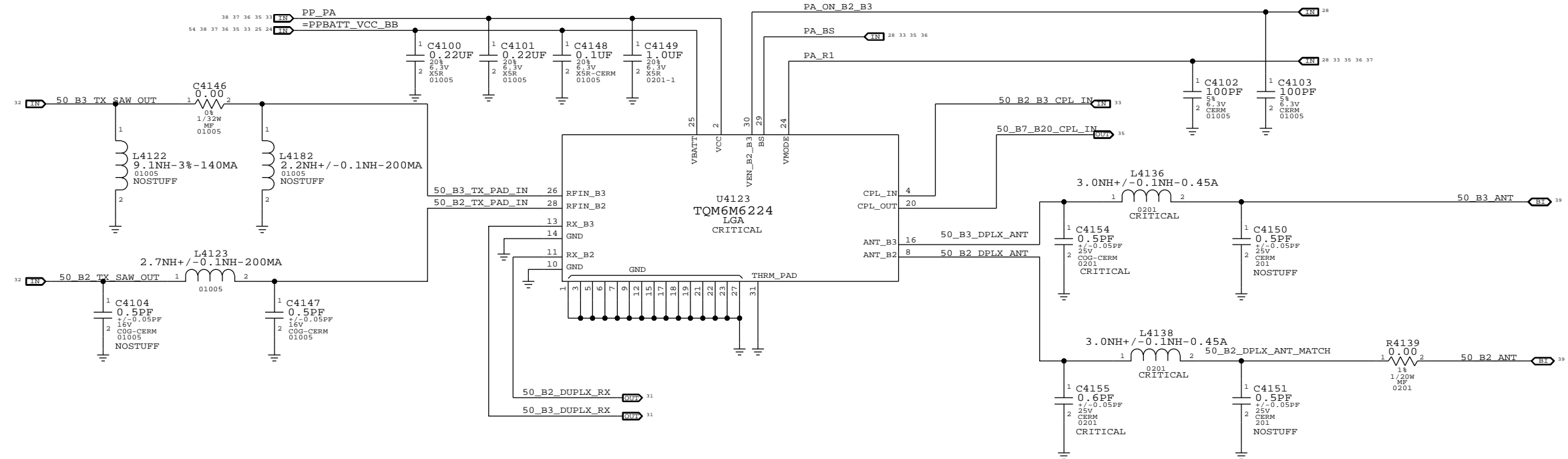


BAND	PA POWER MODE	PA_BS	PA_CTL1	PA_CTL0	PA_R1
OFF	X	X	0	0	0
B1	HPM	X	1	0	0
B1	LPM	X	1	0	1
B34	HPM	1	0	1	0
B34	LPM	1	0	1	1
B39	HPM	0	0	1	0
B39	LPM	0	0	1	1
B38	HPM	1	1	1	0
B38	LPM	1	1	1	1
B40	HPM	0	1	1	0
B40	LPM	0	1	1	1

PAGE TITLE		CELL: PENTABAND PA	
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8 7 6 5 4 3 2 1

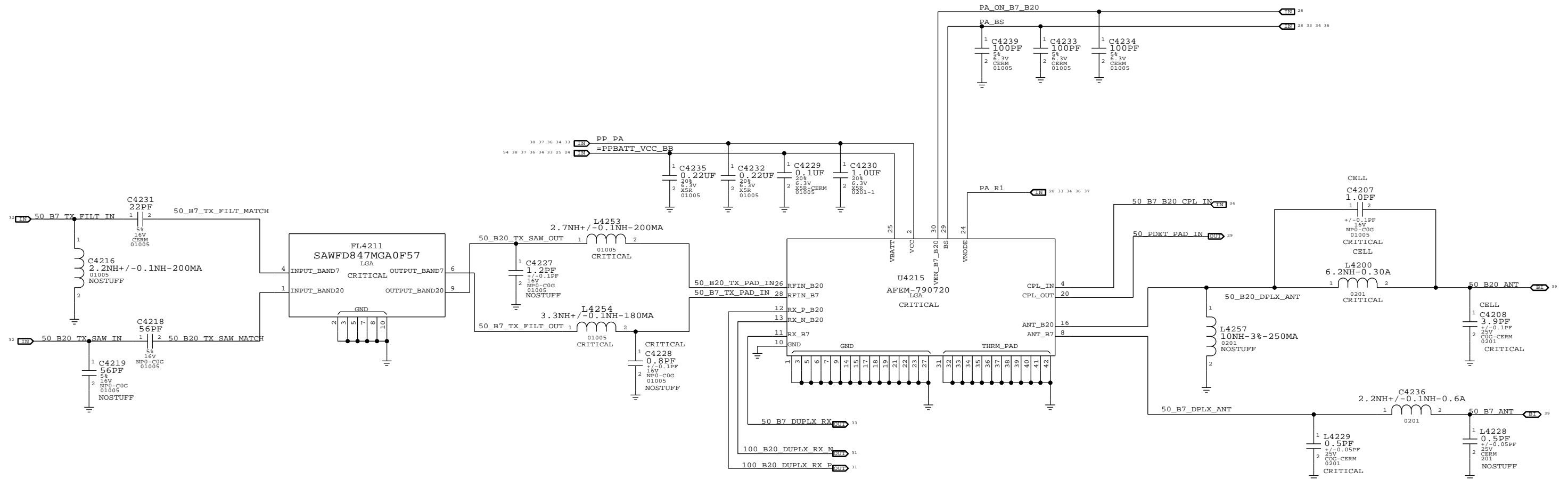
BAND 2/3 PAD



BAND	PA POWER MODE	PA_BS	PA_ON_B2_B3	PA_R1
OFF	X	X	0	X
B3	HPM	0	1	0
B3	LPM	0	1	1
B2	HPM	1	1	0
B2	LPM	1	1	1

PAGE TITLE CELL: BAND 2/3 PAD		
Apple Inc.	DRAWING NUMBER	051-0886
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		PAGE 41 OF 121
		SHEET 34 OF 54

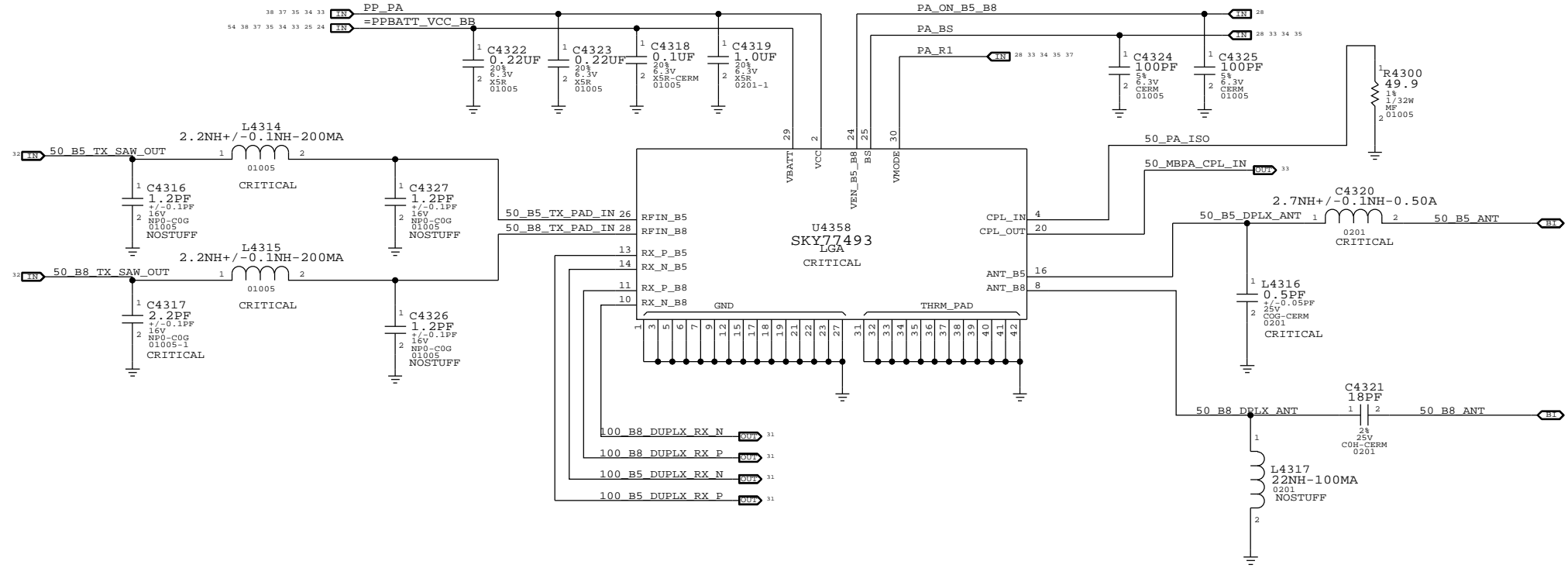
BAND 20/7 PAD



BAND	PA POWER MODE	PA_BS	PA_ON_B20_B7	PA_R1
OFF	X	X	0	X
B20	HPM	0	1	0
B20	LPM	0	1	1
B7	HPM	1	1	0
B7	LPM	1	1	1

PAGE TITLE CELL: BAND 7/20 PAD		
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BAND 5/8 PAD



BAND	PA POWER MODE	PA_BS	PA_ON_B5_B8	PA_R1
OFF	X	X	0	X
B5	HPM	0	1	0
B5	LPM	0	1	1
B8	HPM	1	1	0
B8	LPM	1	1	1

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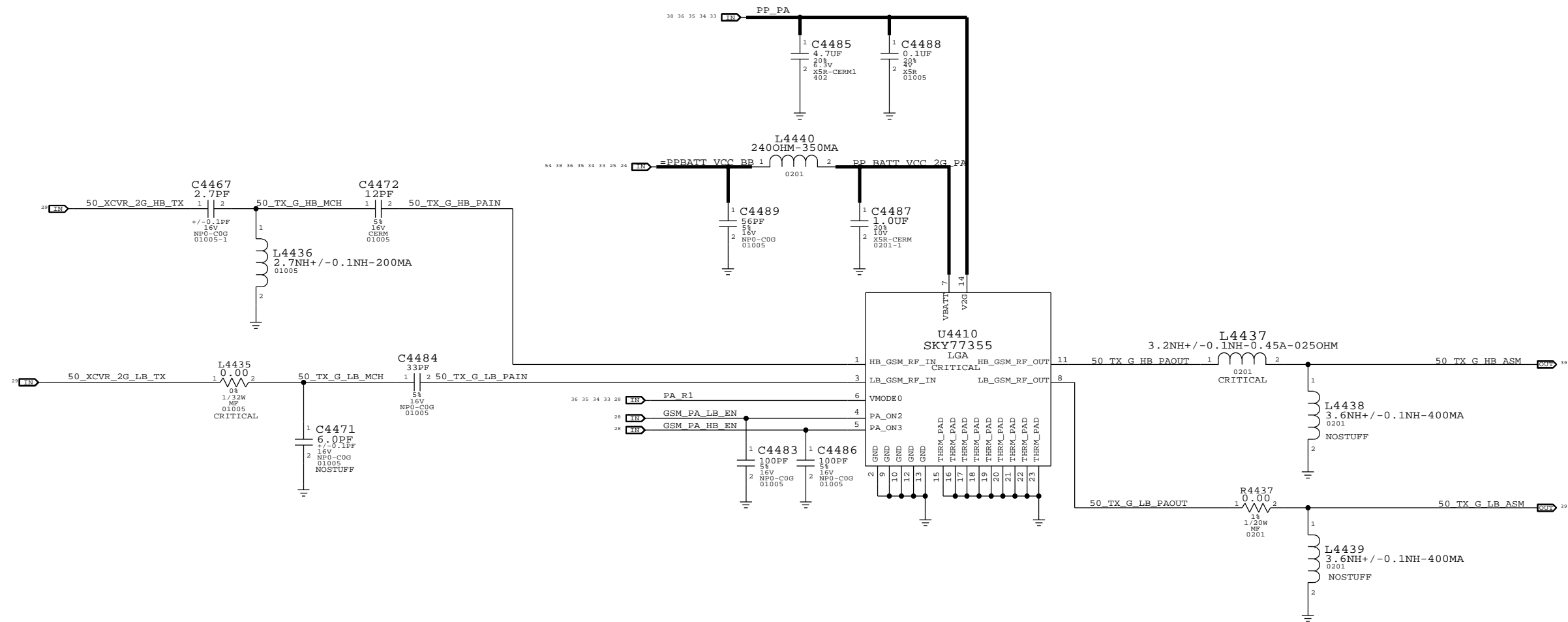
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PAGE 43 OF 121		SHEET 36 OF 54

2G PA

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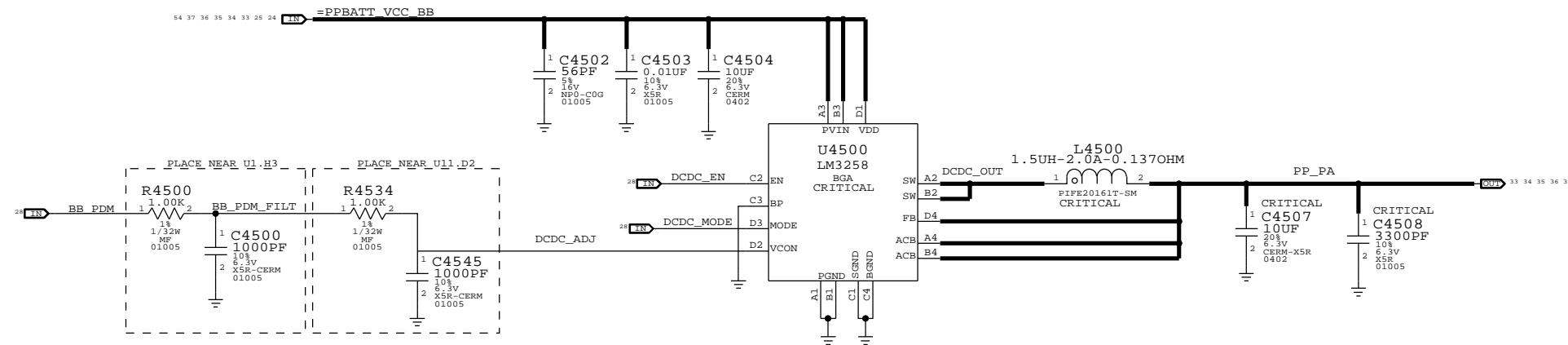
2G PA GAIN MODES

BAND	MODE	GAIN MODE	PA_R1	PCL RANGE
LOW BAND	GSM	ULTRA LOW	HIGH	16 TO 19
LOW BAND	GSM	LOW	HIGH	14 TO 15
LOW BAND	GSM	MEDIUM	LOW	7 TO 13
LOW BAND	GSM	HIGH	LOW	5 TO 6
HIGH BAND	GSM	ULTRA LOW	HIGH	10 TO 15
HIGH BAND	GSM	LOW	HIGH	7 TO 9
HIGH BAND	GSM	HIGH	LOW	0 TO 6
LOW BAND	EDGE	LOW	HIGH	15 TO 19
LOW BAND	EDGE	MEDIUM	LOW	10 TO 14
LOW BAND	EDGE	HIGH	LOW	8 TO 9
HIGH BAND	EDGE	LOW	HIGH	9 TO 15
HIGH BAND	EDGE	HIGH	LOW	2 TO 8



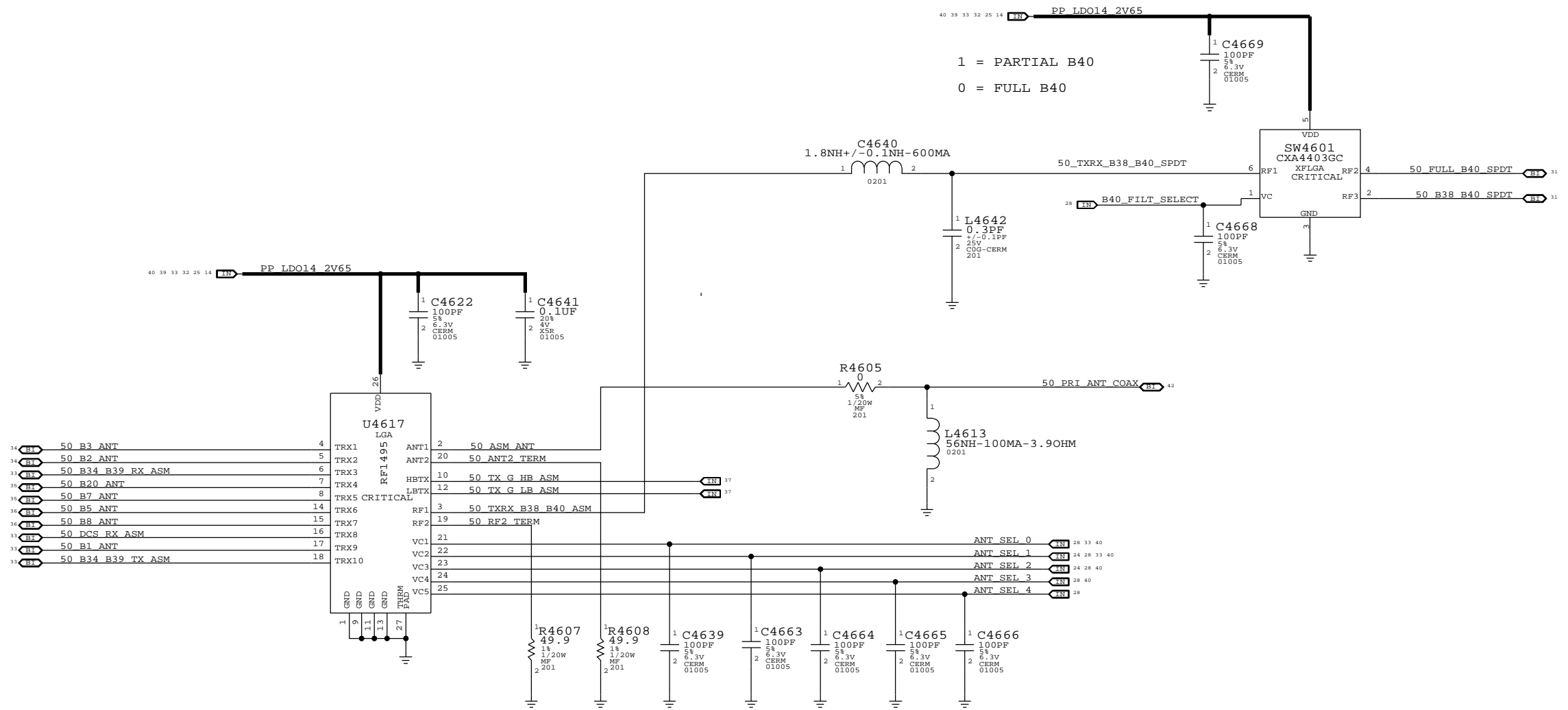
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PA DC/DC CONVERTER



PAGE TITLE CELL: PA DCDC CONVERTER		
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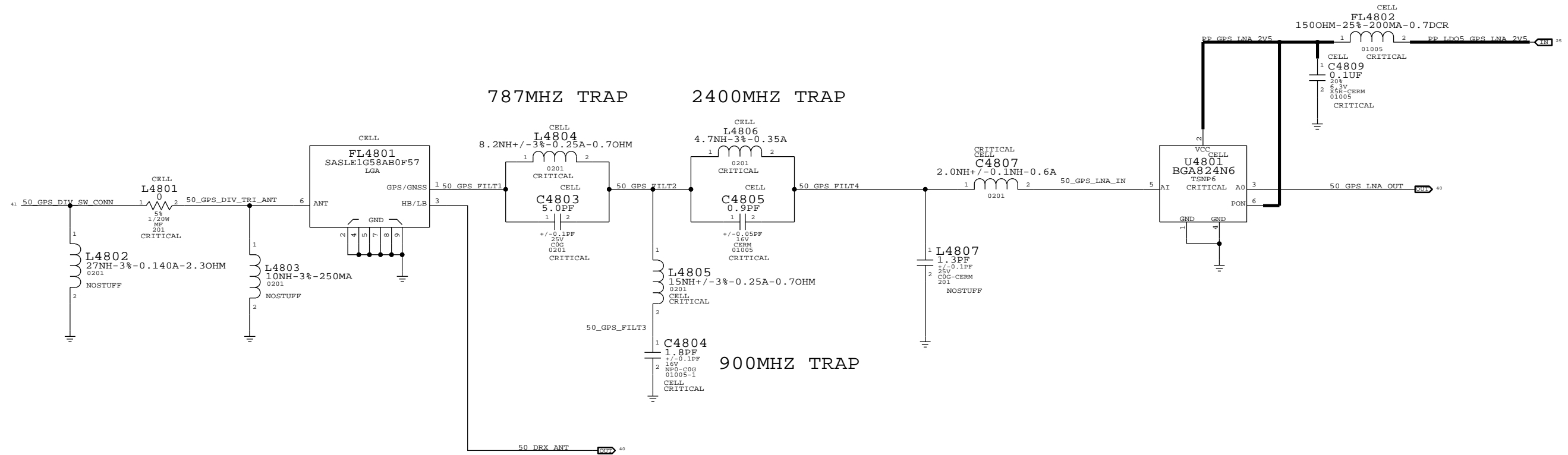
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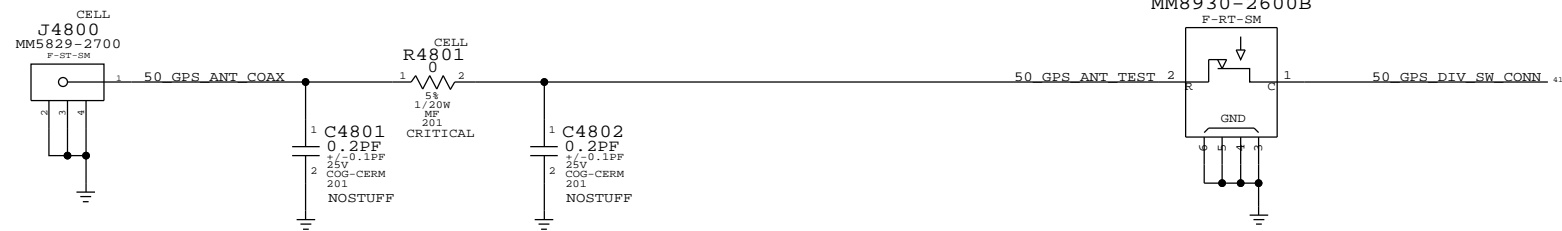
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GPS

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GPS_DRX_ANT



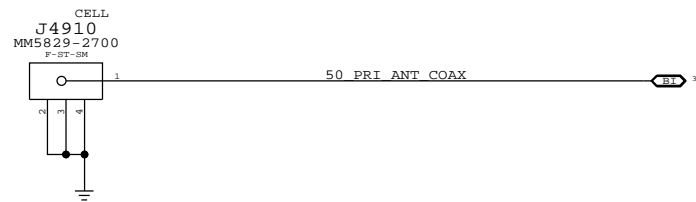
TOP MOUNT

TOP MOUNT

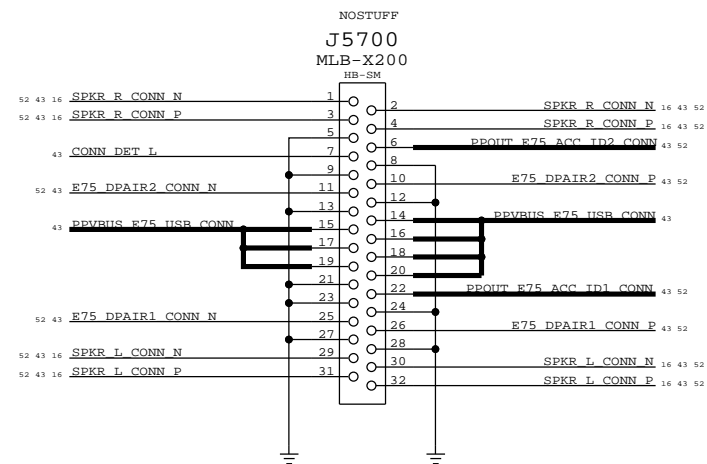
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CELL: GPS			
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ANTENNA FEEDS

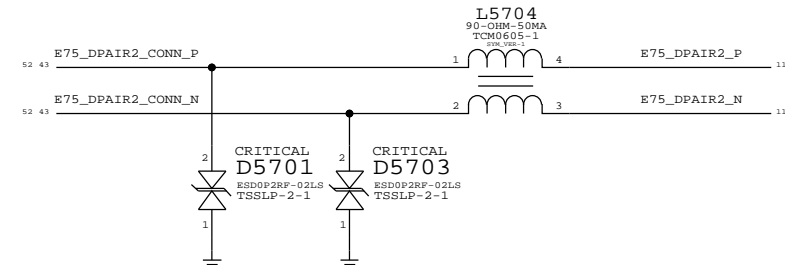
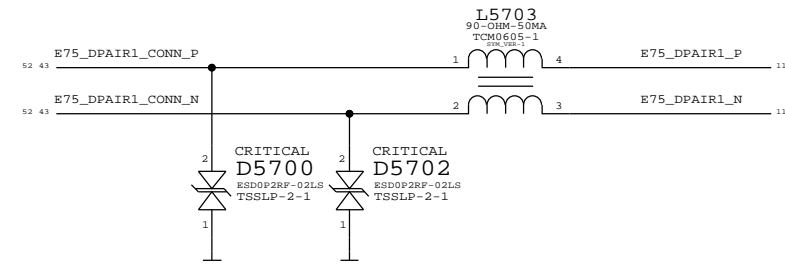
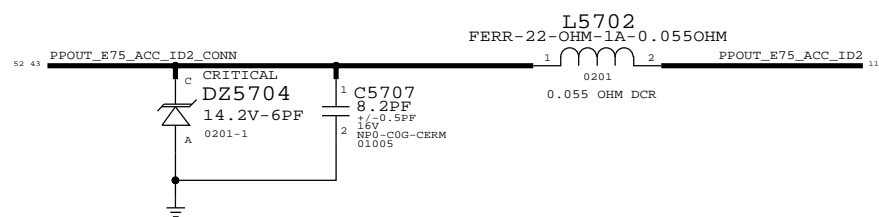
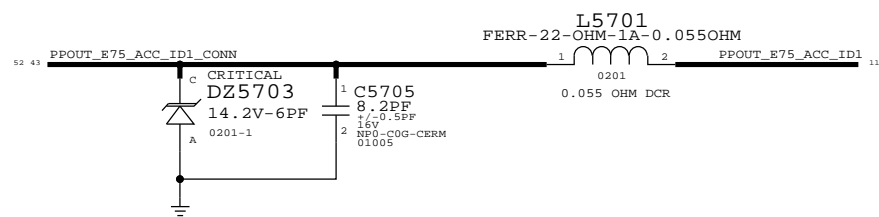
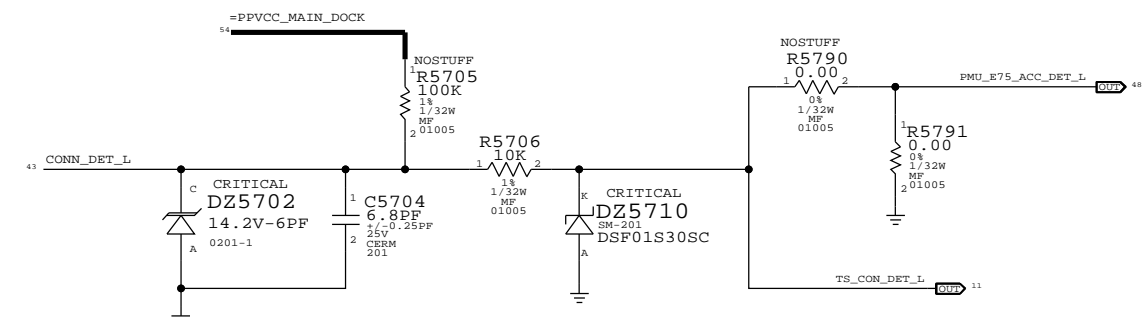
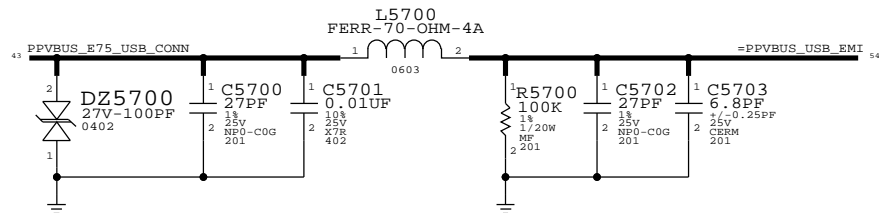
PRI_ANT COAX



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CELL: ANTENNA FEEDS			
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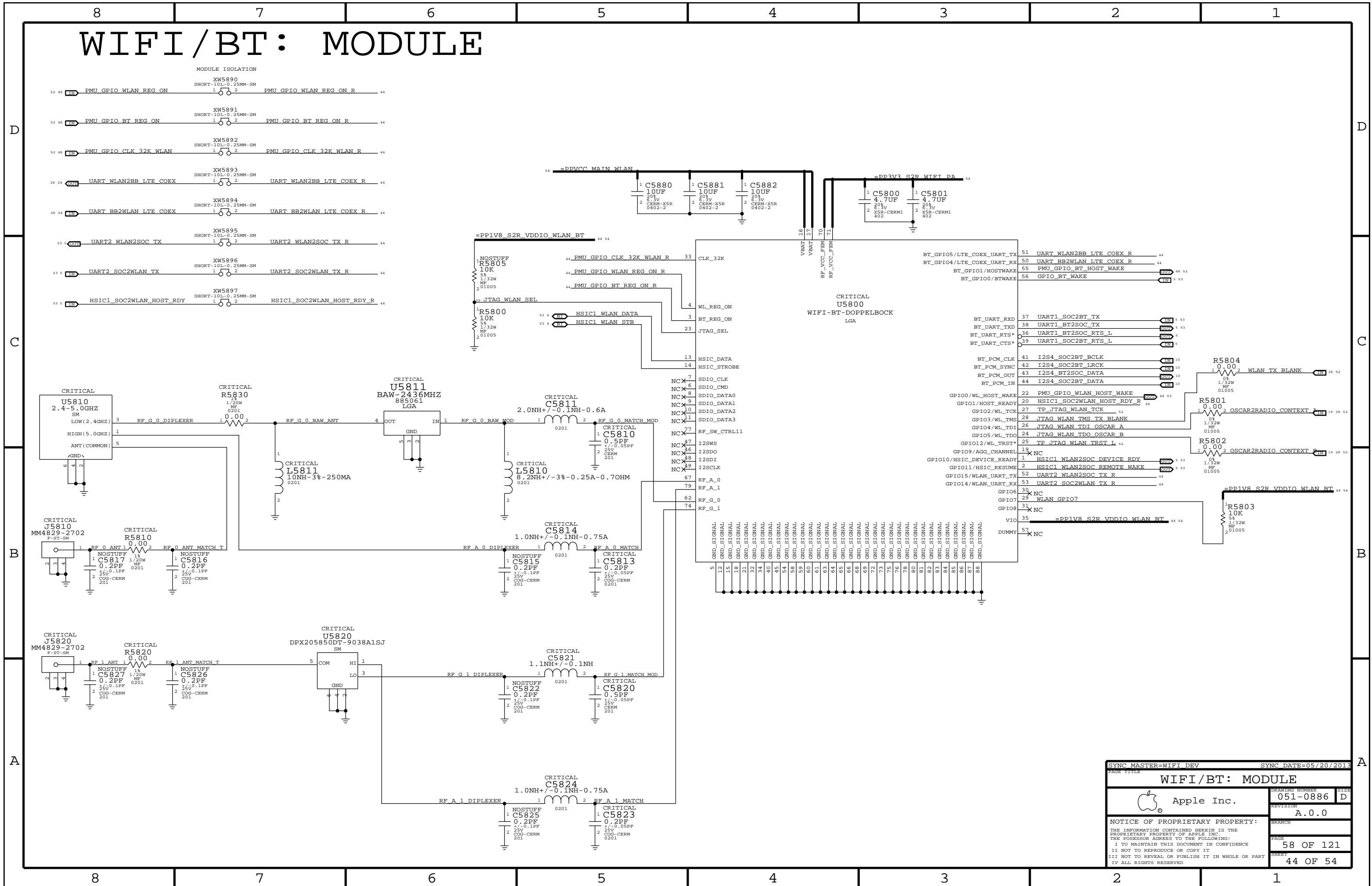


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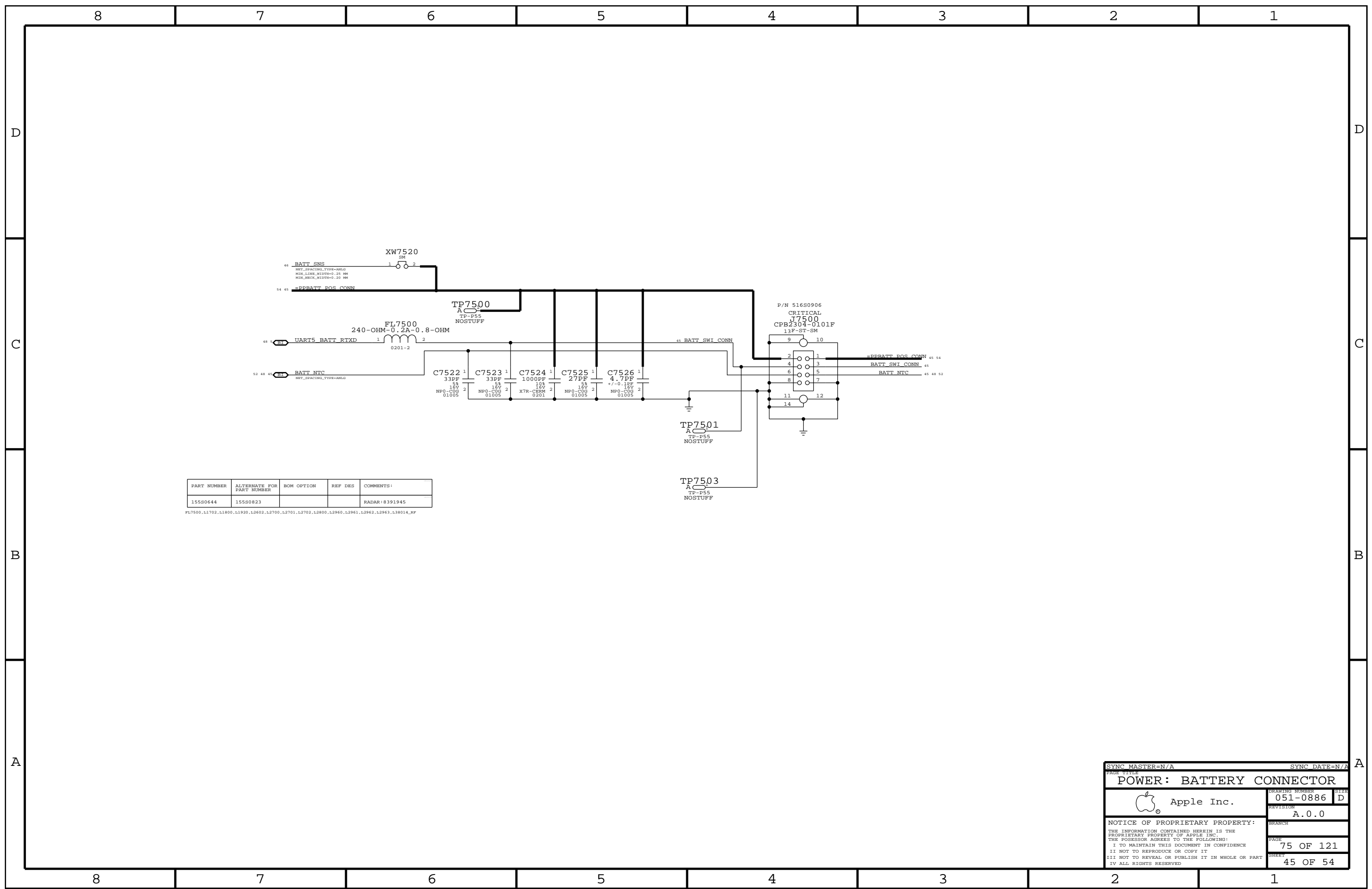


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WIFI/BT: MODULE



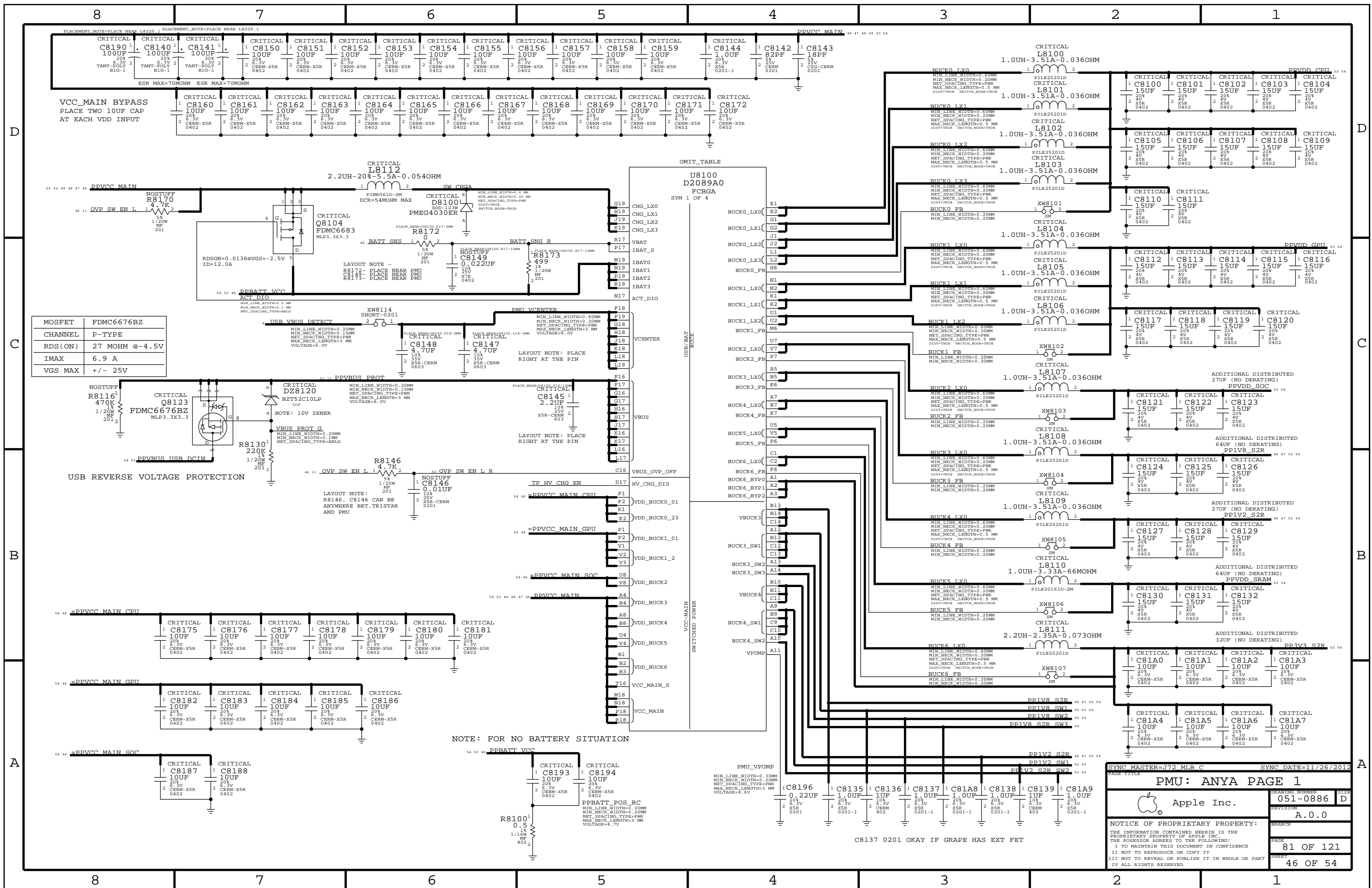
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0823			RADAR:8391945

FL7500, L1702, L1800, L1920, L2602, L2700, L2701, L2702, L2800, L2960, L2961, L2962, L2963, L38014_RF

SYNC MASTER=N/A		SYNC DATE=N/A	
POWER: BATTERY CONNECTOR			
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MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

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PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PMU: ANYA PAGE 1

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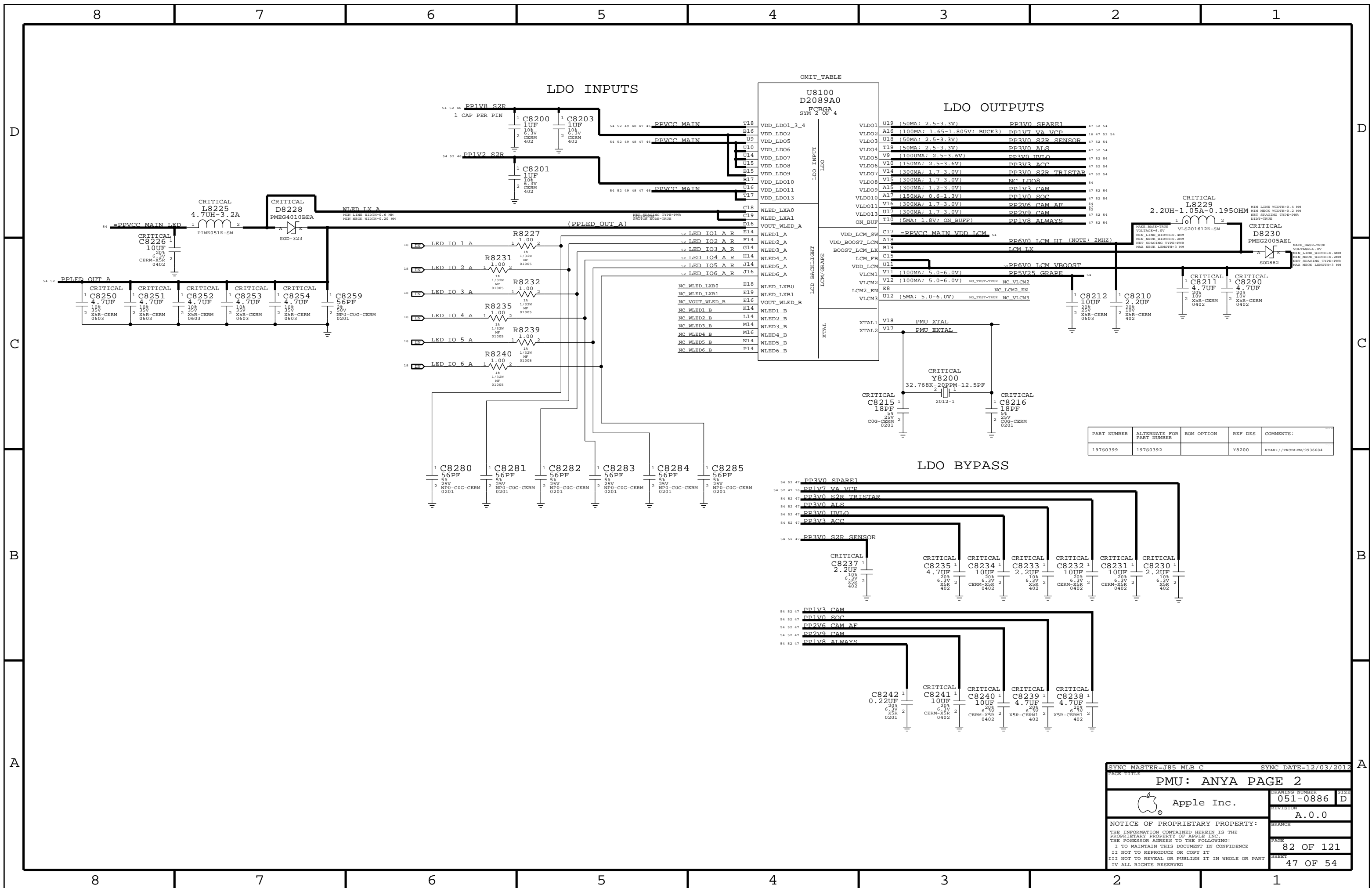
DRAWING NUMBER: 051-0886

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C8137 0201 OKAY IF GRAPE HAS EXT FET



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392		Y8200	RDAR://PROBLEM/9936684

SYNC MASTER=J85 MLB C		SYNC DATE=12/03/2012	
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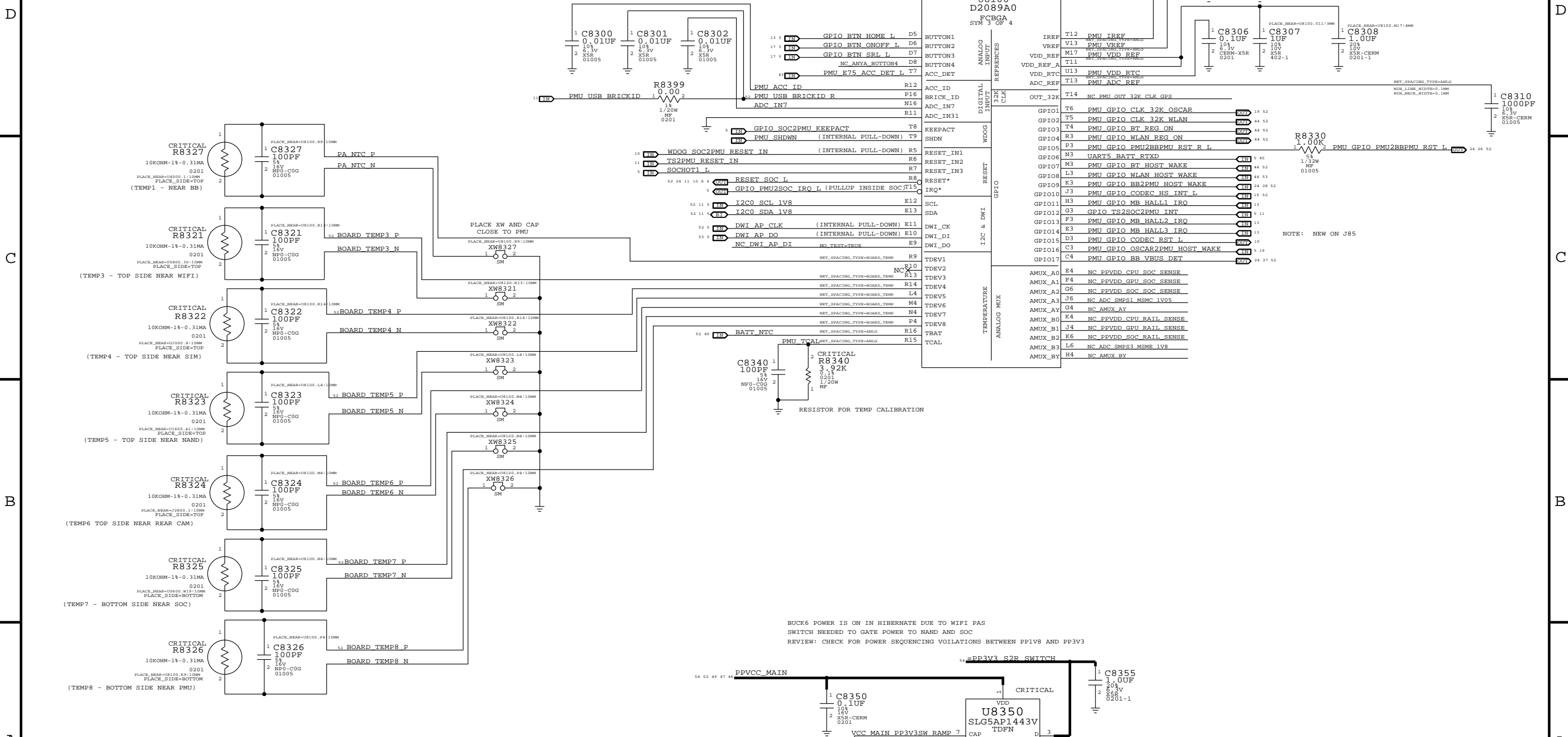
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REVIEW: VERIFY NC ON TDEV2 IS OK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0739	138S0706		C8308	

I2C ADDRESS: 0111100X (0X78)



BUCK6 POWER IS ON IN HIBERNATE DUE TO WIFI PAS
 SWITCH NEEDED TO GATE POWER TO NAND AND SOC
 REVIEW: CHECK FOR POWER SEQUENCING VIOLATIONS BETWEEN PP1V8 AND PP3V3

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0150	107S0208	R8321, R8322	R8323, R8324	RDAR: // PROBLEM/8380367
118S0764	118S0717		R8340	RDAR: // PROBLEM/8380367

SYNC MASTER=J72 MLB C SYNC DATE=11/26/2012

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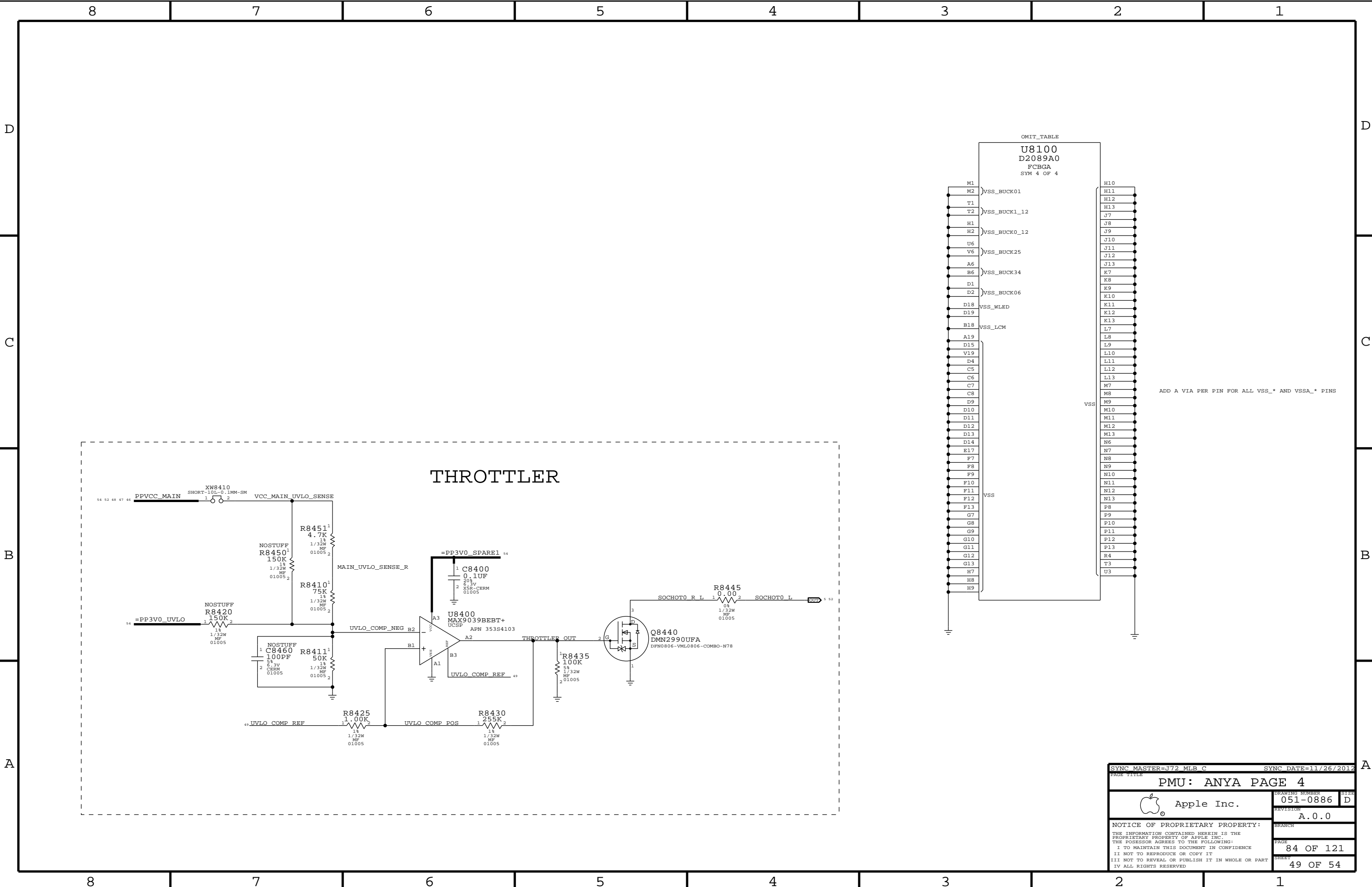
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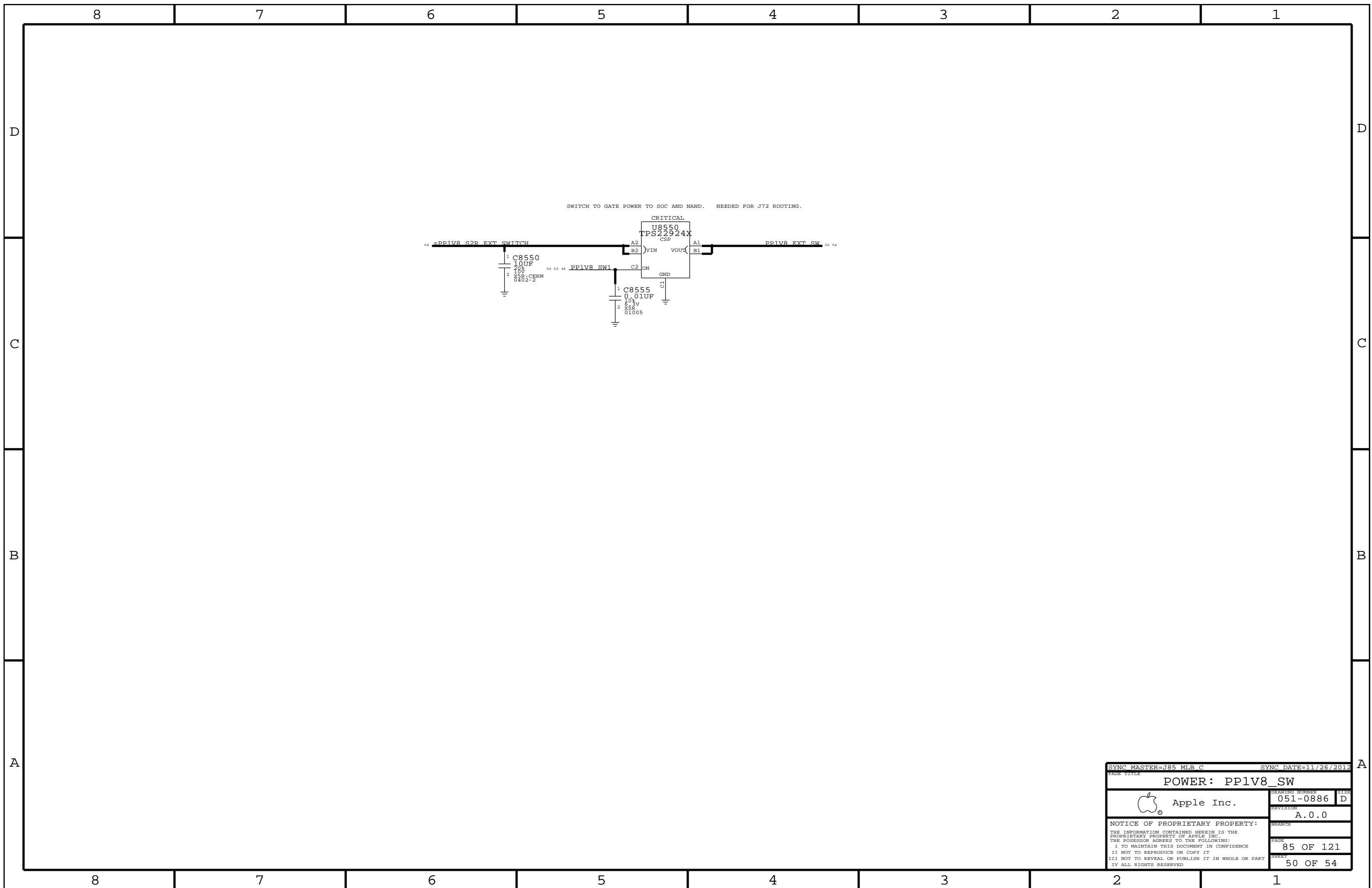
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POWER: PP1V8_SW		051-0886		D
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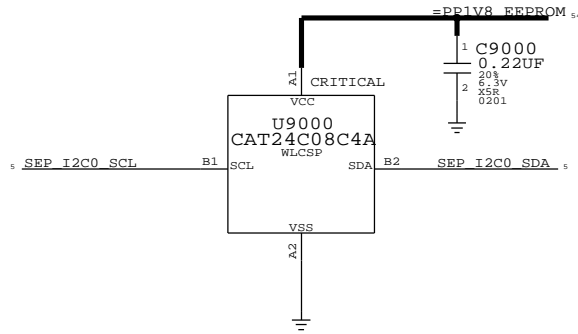
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DEBUG

TP9002
TP-P55

SEP EEPROM

UNPROGRAMMED P/N: 335S0894



SYNC MASTER=J72 MLB C		SYNC DATE=11/26/2012	
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EE CHARACTERIZATION TP

FOR FRANK (SEG)

NAND

PP9401	1	FMI0_DQS	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652.D34:2MM	4 12 53
PP9402	1	FMI0_AD<3>	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652.C34:2MM	6 12
PP9403	1	FMI0_DQS	PLACE_NEAR=U0652.D34:2MM	4 12 53
PP9410	1	TP_TCKC_U1400		12
PP9411	1	TP_TMSC_U1400		12
PP9412	1	TP_U1400_RB0		12
PP9413	1	TP_U1400_RB1		12

DWI

PP9405	1	DWI_AP_DO	PLACE_SIDE=BOTTOM PLACE_NEAR=U8100:2MM	6 48
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AUDIO

PP9406	1	I2S0_CODEC_ASP_MCK	PLACE_NEAR=U1900:2MM	6 15
--------	---	--------------------	----------------------	------

PP9416	1	I2S2_CODEC_XSP_LRCK	PLACE_NEAR=U1900:2MM	6 15
PP9417	1	I2S2_CODEC_XSP_DOUT	PLACE_NEAR=U1900:2MM	6 15

PP9419	1	I2S1_SPKAMP_MCK	PLACE_NEAR=U2040:2MM	6 16
PP9420	1	I2S1_SPKAMP_BCLK	PLACE_NEAR=U2040:2MM	6 16
PP9421	1	I2S1_SPKAMP_LRCK	PLACE_NEAR=U2040:2MM	6 16
PP9422	1	I2S1_SPKAMP_DOUT	PLACE_NEAR=U2040:2MM	6 16
PP9423	1	I2S1_SPKAMP_DIN	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM	6 16

PP9424	1	SPI2_CODEC_SCLK	PLACE_NEAR=U1900:2MM	6 15
PP9425	1	SPI2_CODEC_MOSI	PLACE_NEAR=U1900:2MM	6 15
PP9426	1	SPI2_CODEC_MISO	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM	6 15

GRAPE

OSCAR

PP9428	1	UART4_SOC2OSCAR_TXD	PLACE_SIDE=BOTTOM PLACE_NEAR=U2400:2MM	6 19
PP9429	1	UART4_OSCAR2SOC_RXD	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM	6 19

UART5

PP9450	1	PPVDD_SOC_SOC_SENSE	PLACE_NEAR=U0652.V31:1MM	
PP9451	1	PPVDD_CPU_SOC_SENSE	PLACE_NEAR=U0652.AN30:1MM	

WIFI

PP9480	1	HSIC1_WLAN2SOC_DEVICE_RDY		5 44
PP9481	1	HSIC1_WLAN2SOC_REMOTE_WAKE		5 44
PP9482	1	PMU_GPIO_WLAN_HOST_WAKE		44 48
PP9483	1	HSIC1_SOC2WLAN_HOST_RDY		5 44

GPIO_BT_WAKE	FUNC_TEST=TRUE	5 44
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FOR HSIC CHARACTERIZATION

PP9460	1	HSIC1_WLAN_DATA	PLACE_NEAR=U0652.AM33:3MM	4 44 53
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PP9462	1	HSIC1_WLAN_DATA	PLACE_NEAR=U5800.13:3MM	4 44 53
PP9463	1	HSIC1_WLAN_STB	PLACE_NEAR=U5800.14:3MM	4 44

PP9468	1	UART1_BT2SOC_TX	PLACE_NEAR=U0652:3MM	5 44
PP9469	1	UART1_SOC2BT_TX	PLACE_NEAR=U5800:3MM	5 44

PP9471	1	UART2_WLAN2SOC_TX	PLACE_NEAR=U0652:3MM	5 44
PP9472	1	UART2_SOC2WLAN_TX	PLACE_NEAR=U5800:3MM	5 44

BASEBAND

USB_BB_P	FUNC_TEST=TRUE	11 24 52
USB_BB_N	FUNC_TEST=TRUE	11 24 52

FOR HSIC CHARACTERIZATION

PP9465	1	HSIC2_BB_STB	PLACE_NEAR=U0652.B27:3MM	4 24 27
PP9466	1	HSIC2_BB_DATA	PLACE_NEAR=U3400.C7:3MM	4 24 27

PROX

HIGH SPEED, NO TEST

MIPI0C_CAM_REAR_CLK_P	NO_TEST=TRUE	7 23 53
MIPI0C_CAM_REAR_CLK_N	NO_TEST=TRUE	7 23 53
MIPI0C_CAM_REAR_DATA_P<0..3>	NO_TEST=TRUE	7 23 53
MIPI0C_CAM_REAR_DATA_N<0..3>	NO_TEST=TRUE	7 23 53
MIPI0C_CAM_REAR_CLK_FILT_P	NO_TEST=TRUE	23
MIPI0C_CAM_REAR_CLK_FILT_N	NO_TEST=TRUE	23
MIPI0C_CAM_REAR_DATA_FILT_P<0..3>	NO_TEST=TRUE	23
MIPI0C_CAM_REAR_DATA_FILT_N<0..3>	NO_TEST=TRUE	23
MIPI1C_CAM_FRONT_CLK_P	NO_TEST=TRUE	7 20 53
MIPI1C_CAM_FRONT_CLK_N	NO_TEST=TRUE	7 20 53
MIPI1C_CAM_FRONT_DATA_P<0>	NO_TEST=TRUE	7 20 53
MIPI1C_CAM_FRONT_DATA_N<0>	NO_TEST=TRUE	7 20 53
MIPI1C_CAM_FRONT_CLK_FILT_P	NO_TEST=TRUE	20
MIPI1C_CAM_FRONT_CLK_FILT_N	NO_TEST=TRUE	20
MIPI1C_CAM_FRONT_DATA_FILT_P<0>	NO_TEST=TRUE	20
MIPI1C_CAM_FRONT_DATA_FILT_N<0>	NO_TEST=TRUE	20
EDP_DATA_P<0..3>	NO_TEST=TRUE	7 18
EDP_DATA_N<0..3>	NO_TEST=TRUE	7 18
EDP_DATA_EMI_P<0..3>	NO_TEST=TRUE	18
EDP_DATA_EMI_N<0..3>	NO_TEST=TRUE	18
EDP_DATA_EMI_CONN_P<0..3>	NO_TEST=TRUE	18
EDP_DATA_EMI_CONN_N<0..3>	NO_TEST=TRUE	18

CAMERA

PP9440	1	MIPI1C_CAM_FRONT_CLK_P	PLACE_NEAR=U0652.AR33:3MM	7 20 53
PP9441	1	MIPI1C_CAM_FRONT_CLK_N	PLACE_NEAR=U0652.AR34:3MM	7 20 53
PP9442	1	MIPI1C_CAM_FRONT_DATA_P<0>	PLACE_NEAR=U0652.AT33:3MM	7 20 53
PP9443	1	MIPI1C_CAM_FRONT_DATA_N<0>	PLACE_NEAR=U0652.AT34:3MM	7 20 53
PP9444	1	MIPI0C_CAM_REAR_CLK_P	PLACE_NEAR=U0652.AU25:3MM	7 23 53
PP9445	1	MIPI0C_CAM_REAR_CLK_N	PLACE_NEAR=U0652.AV25:3MM	7 23 53
PP9446	1	MIPI0C_CAM_REAR_DATA_P<0>	PLACE_NEAR=U0652.AU27:3MM	7 23 53
PP9447	1	MIPI0C_CAM_REAR_DATA_N<0>	PLACE_NEAR=U0652.AV27:3MM	7 23 53

SYNC MASTER=J72_MLB_C		SYNC DATE=11/26/2012	
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POWER CONNECTIONS

BUCK0

52 46 PPVDD_CPU == =PPVDD_CPU 9

BUCK1

52 46 PPVDD_GPU == =PPVDD_GPU 9

BUCK2

52 46 PPVDD_SOC == =PPVDD_SOC 9

BUCK3

52 47 44 PP1V8_S2R == =PP1V8_S2R_MISC 5 51
 == =PP1V8_S2R_VDDIO_WLAN_BT 44
 == =PP1V8_S2R_TRISTAR 11
 == =PP1V8_S2R_DDR 8
 == =PP1V8_S2R_GRAPE 13
 == =PP1V8_S2R_EXT_SWITCH 50
 == =PP1V8_S2R_REAR_CAMERA 13
 == =PP1V8_S2R_MESA 13
 == =PP1V8_S2R_VDD_CORE_GPS 13
 == =PP1V8_S2R_VDD_IO_GPS 13

BUCK3_SW

52 50 46 PP1V8_SW1 == =PP1V8_AUDIO 15
 == =PP1V8_DMIC 14
 == =PP1V8_CAM_FRONT 20
 == =PP1V8_CAM_REAR 23
 == =PP1V8_PROX 22

PP1V8_EXT SW

52 50 50 PP1V8_EXT SW == =PP1V8_VDDIO18_SOC 8 9
 == =PP1V8_SOC 4 5 7 10 18
 == =PP1V8_MIPI_SOC 7
 == =PP1V8_EDP_SOC 7
 == =PP1V8_NAND_SOC 6
 == =PP1V8_NAND 12 48
 == =PP1V8_PLL_SOC 4
 == =PP1V8_SPKRAMP 13
 == =PP1V8_EEPROM 51
 == =PP1V8_BEACON 13

PP1V8_SW2

52 46 PP1V8_SW2 == =PP1V8_GRAPE 13

PP1V8_S2R_SW3

46 PP1V8_S2R_SW3 == =PP1V8_S2R_GYRO 21
 == =PP1V8_S2R_ACCEL 21
 == =PP1V8_S2R_OSCAR 19
 == =PP1V8_S2R_SW3_COMP 52 54

PP1V8_S2R_SW3 COMP

54 52 PP1V8_S2R_SW3 COMP == =PP1V8_S2R_COMP 21

PP1V8_S2R_SW3 SHOULD BE ON IN HIBERNATE CURRENTLY POWERS OSCAR AND 1.8V RAIL ON SENSOR

BUCK4

52 47 46 PP1V2_S2R == =PP1V2_S2R_DDR 8
 == =PP1V2_S2R_DDR_SOC 8
 == =PP1V2_S2R_CAM_REAR 8

BUCK4_SW

52 46 PP1V2_SW1 == =PP1V2_VDDO_DDR 8
 == =PP1V2_VDDIOD_SOC 8
 == =PP1V2_HSIC_SOC 4

PP1V2_S2R_SW2

52 46 PP1V2_S2R_SW2 == =PP1V2_S2R_OSCAR 19

PP1V2_S2R_SW2 SHOULD BE ON IN HIBERNATE PROVIDE 1.2V TO OSCAR

BUCK5

52 46 PPVDD_SRAM == =PPVDD_SRAM_CPU 9
 == =PPVDD_SRAM_SOC 9

BUCK6

52 46 PP3V3_S2R == =PP3V3_S2R_SWITCH 48
 == =PP3V3_S2R_WIFI_PA 44

PP3V3_SW

52 48 PP3V3_SW == =PP3V3_EDP_PU 13
 == =PP3V3_NAND 13
 == =PP3V3_USB_SOC 4

LDO1

52 47 PP3V0_SPARE1 == =PP3V0_SPARE1 49

LDO2

52 47 16 PP1V7_VA_VCP == =PP1V7_VA_VCP 15 16

LDO3

52 47 PP3V0_S2R_SENSOR == =PP3V0_S2R_HALL 13
 == =PP3V0_S2R_GYRO 21
 == =PP3V0_S2R_ACCEL 21
 == =PP3V0_S2R_COMP 21

LDO3 SHOULD BE ON IN HIBERNATE COMPASS, ACCEL, GYRO, PROX ARE ON OSCAR HALL EFFECT NEEDS TO BE ON IN HIBERNATE

LDO4

52 47 PP3V0_ALS == =PP3V0_ALS 20
 == =PP3V0_PROX 22
 == =PP3V0_HP_ALS 22
 == =PP3V0_IO_ALS 22

SHOULD IO ALS POWER HERE?

LDO5

52 47 PP3V0_UVLO == =PP3V0_UVLO 49

LDO6

52 47 PP3V3_ACC == =PP3V3_ACC 11

LDO7

52 47 PP3V0_S2R_TRISTAR == =PP3V0_S2R_TRISTAR 11

LDO7 SHOULD BE ON IN HIBERNATE

LDO8

47 NC_LDO8 NO_TEST=TRUE == =NC_LDO8

LDO9

52 47 PP1V3_CAM == =PP1V3_CAM_FRONT 23
 == =PP1V3_CAM_REAR 23

BACKUP RAIL. CAN BE BOOSTED TO MEET 1.1V MIN ON CAMERA IF NEEDED.

LDO10

52 47 PP1V0_SOC == =PP1V0_USB_SOC 4
 == =PP1V0_MIPI_SOC 7
 == =PP1V0_EDP_PAD_DVDD_SOC 7

LDO11

52 47 PP2V6_CAM_AF == =PP2V6_CAM_REAR_AF 23

LDO13

52 47 PP2V9_CAM == =PP2V9_CAM_FRONT 20
 == =PP2V9_CAM_REAR 23

VLCM1

47 PP5V25_GRAPE == =PP5V25_GRAPE 13

CHARGER MAIN

52 49 48 47 46 PPVCC_MAIN == =PPVCC_MAIN_AUDIO 15 16
 == =PPVCC_MAIN_LED 47
 == =PPVCC_MAIN_DOCK 43
 == =PPVCC_MAIN_DEV 46
 == =PPVCC_MAIN_CPU 46
 == =PPVCC_MAIN_GPU 46
 == =PPVCC_MAIN_SOC 46
 == =PPVCC_MAIN_GRAPE 13
 == =PPVCC_MAIN_LCD 18
 == =PPVCC_MAIN_NAVAJA 47
 == =PPVCC_MAIN_VDD_LCM 44
 == =PPVCC_MAIN_WLAN 44
 == =PPVCC_MAIN_GPS 44

BATTERY

52 46 PPBATT_VCC == =PPBATT_POS_CONN 45
 == =PPBATT_VCC_BB 24 25 33 34 35 36 37 38
 == =PPBATT_AUDIO 45

USB POWER INPUT

52 46 PPVBUS_USB_DCIN == =PPVBUS_USB_EMI 43

ON_BUF

52 47 PP1V8_ALWAYS == =PP1V8_ALWAYS 5

BACKLIGHT BOOST

52 47 PPLED_OUT_A == =PPLED_REG_A 18

SYNC_MASTER=J72_MLB_C SYNC_DATE=11/26/2012

POWER: ALIASES



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