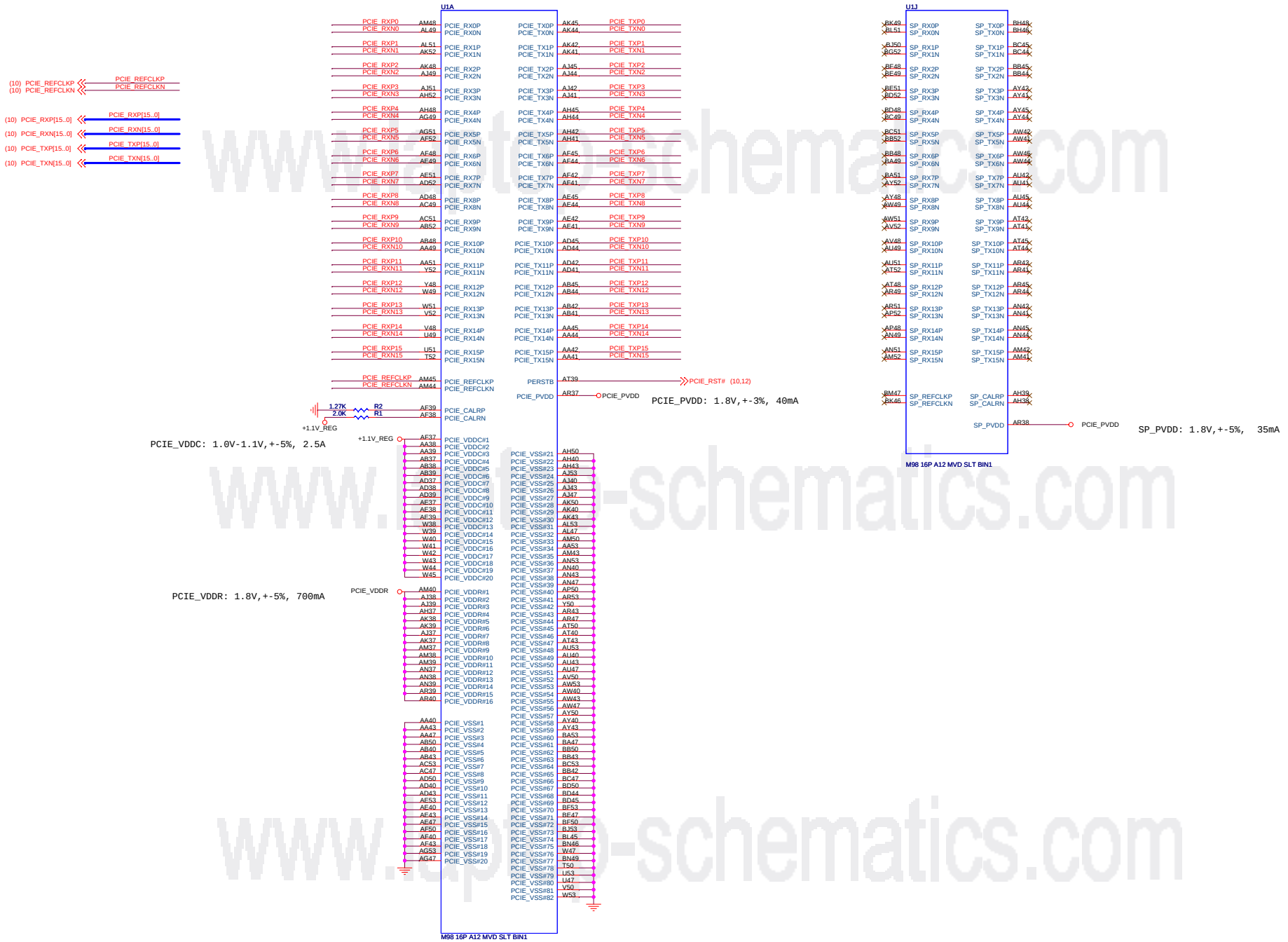

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Doc No. 105-B911xx-0A

DPAVDDR: 1.1V,+-3%, 200mA

DPBVDDR: 1.1V,+-3%, 200mA

LVDDC: 1.8V,+-3%, 400mA

DPA_PVDD: 1.8V,+-3%, 20mA

DPB_PVDD: 1.8V,+-3%, 20mA

LPVDD: 1.8V,+-3%, 40mA

AVDD: 1.8V,+-5%, 70mA

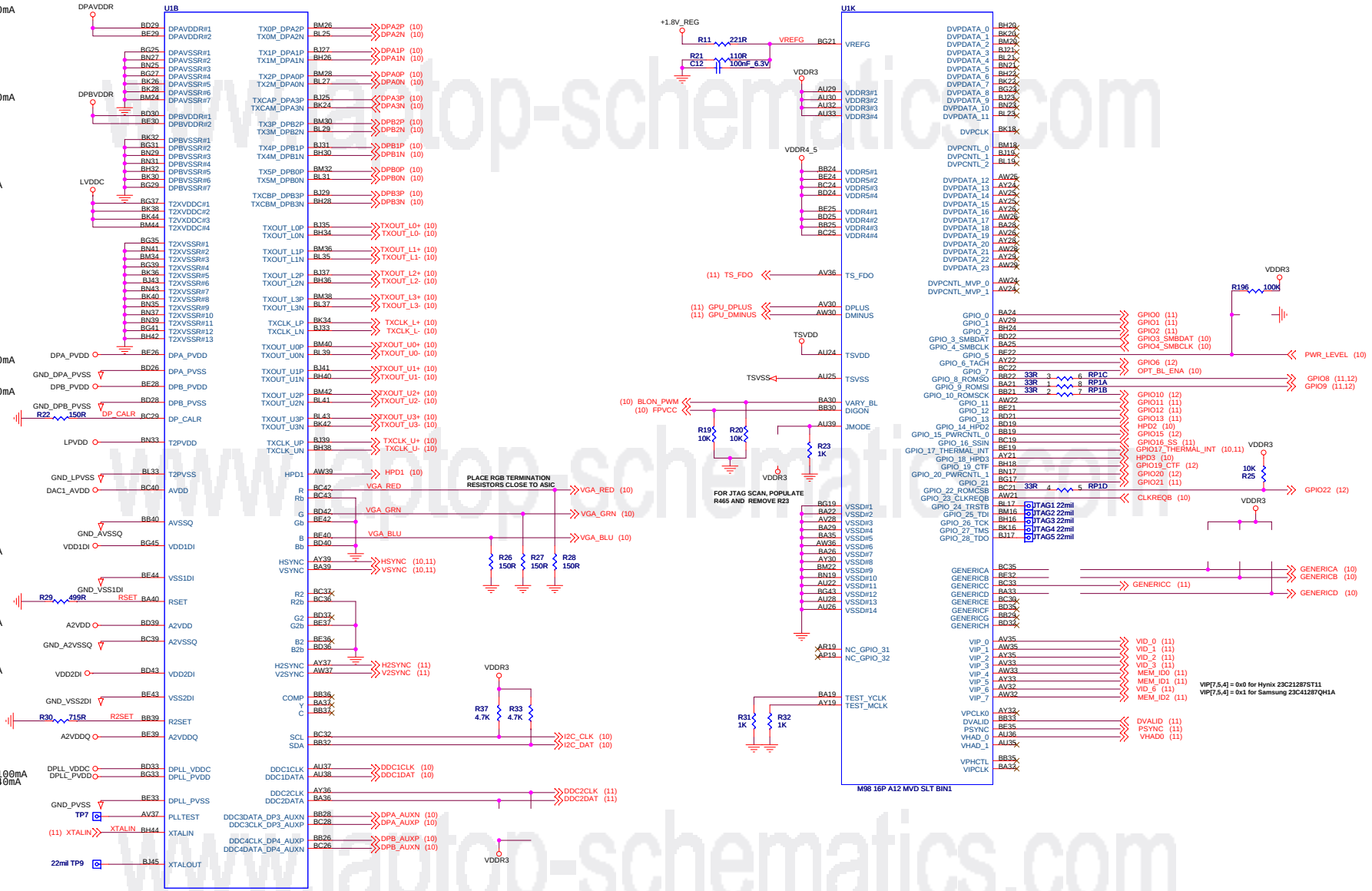
VDD1DI: 1.8V,+-5%, 50mA

A2VDD: 3.3V,+-5%, 135mA

VDD2DI: 1.8V,+-5%, 40mA

A2VDDQ: 1.8V,+-5%, 1mA

DPLL_VDDC: 1.1V,+-5%, 100mA
DPLL_PVDD: 1.8V,+-3%, 40mA



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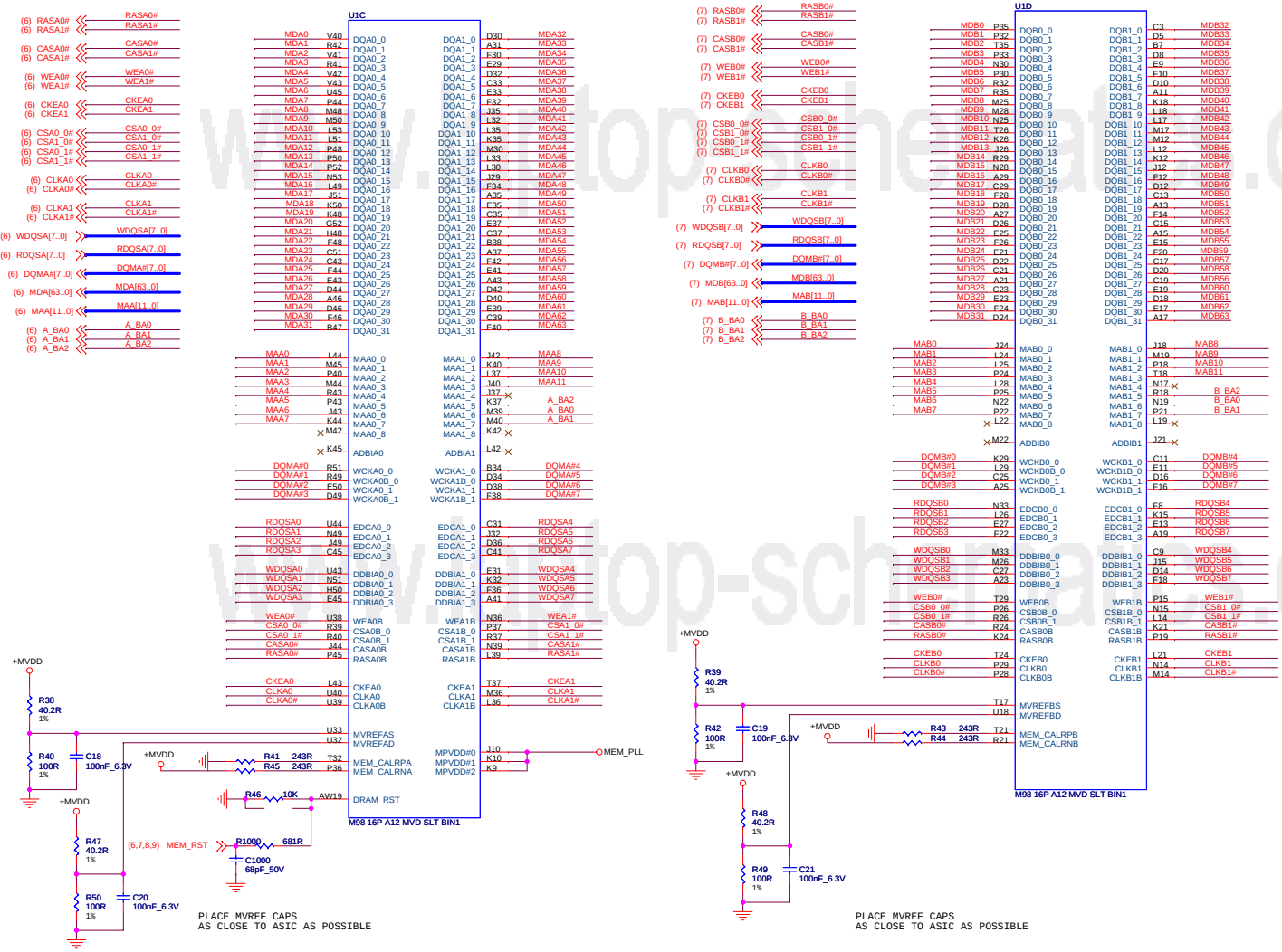

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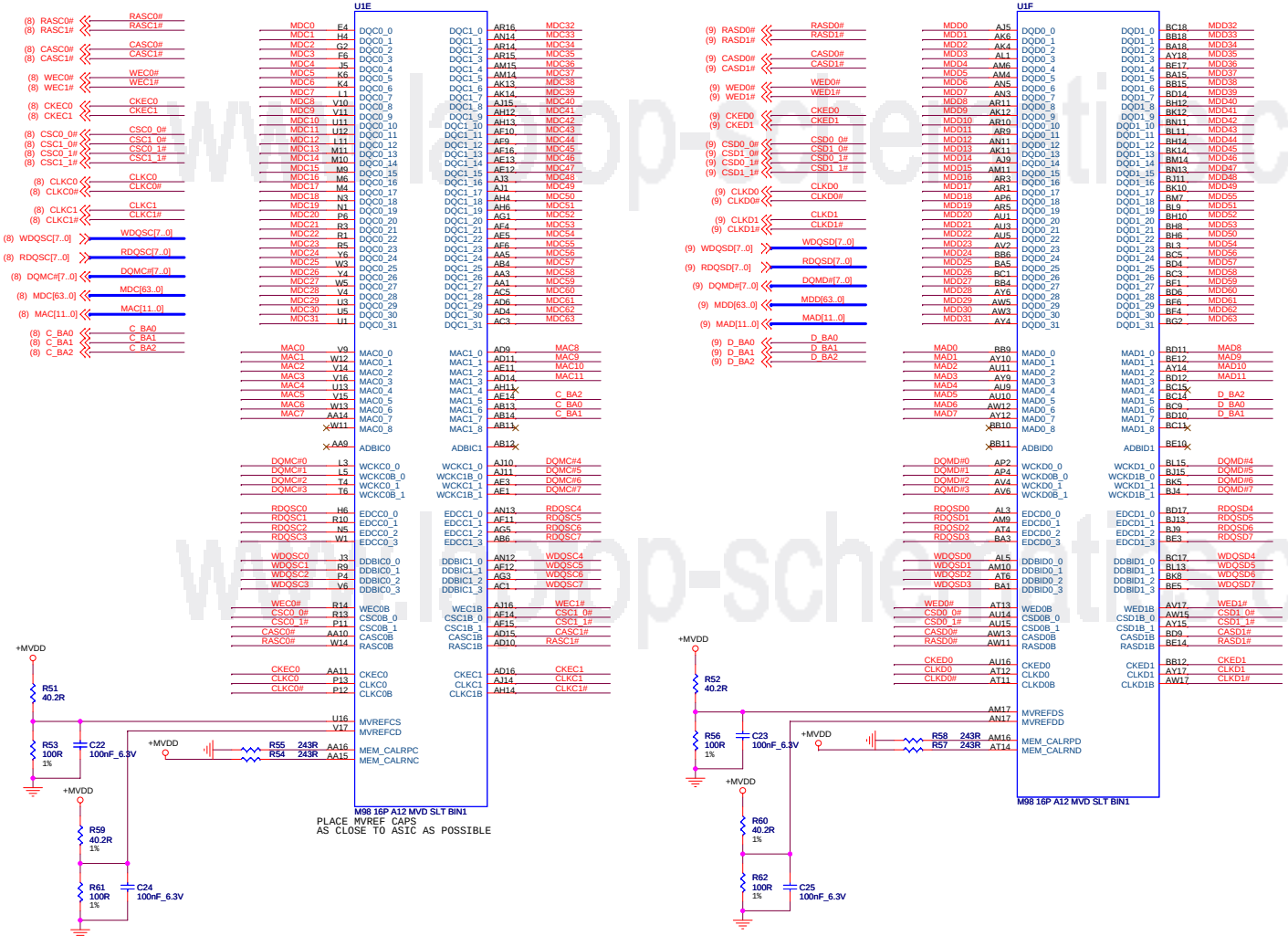

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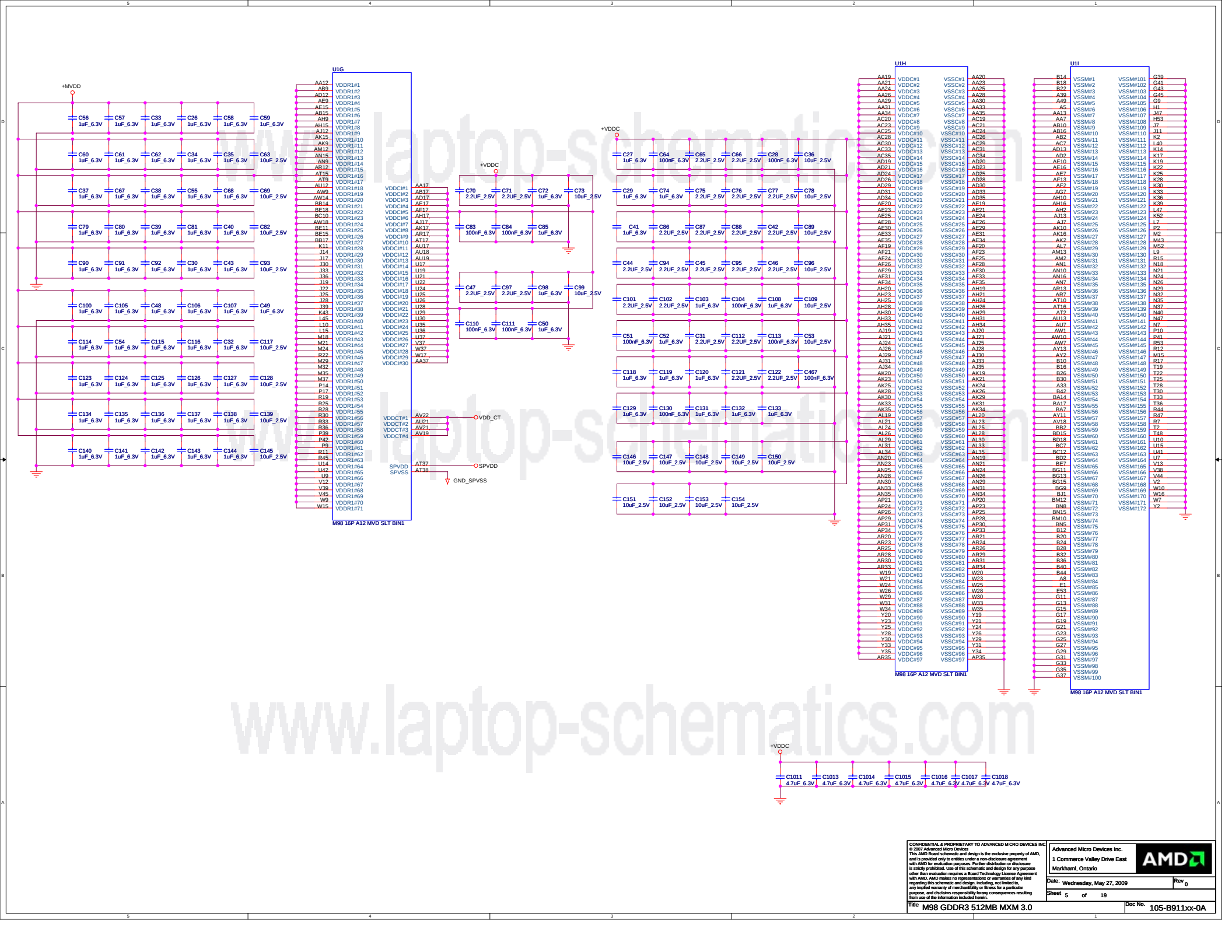

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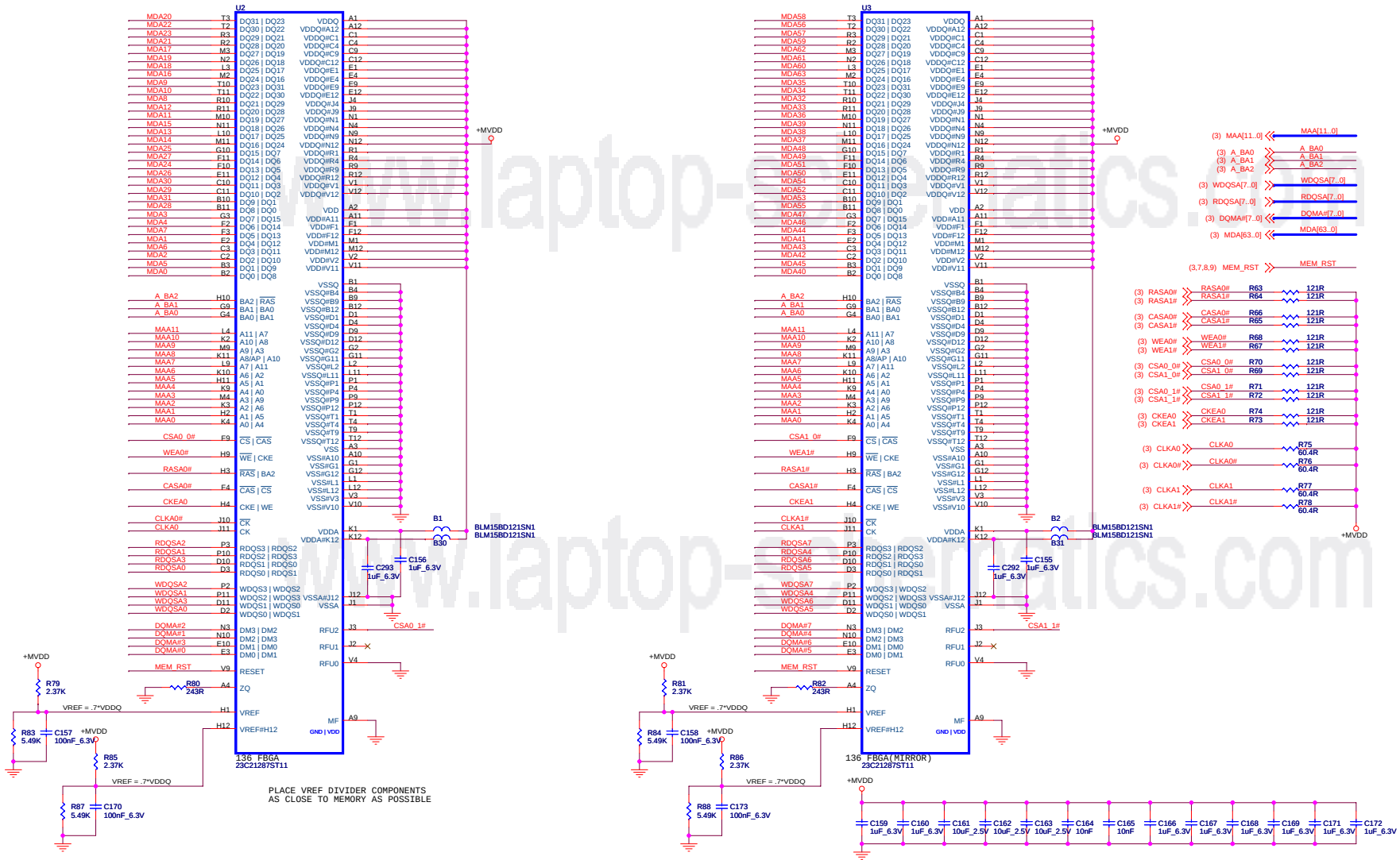

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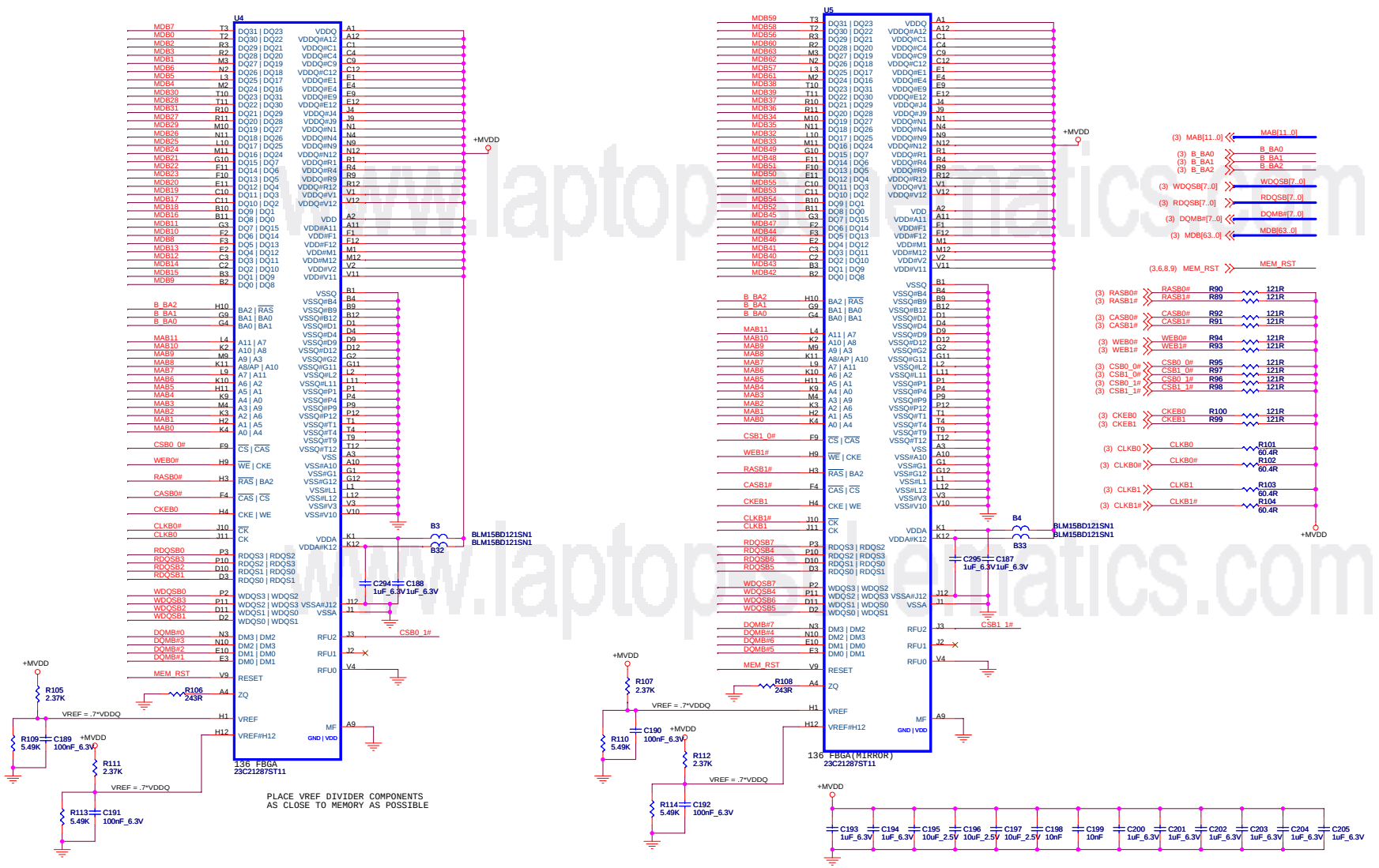

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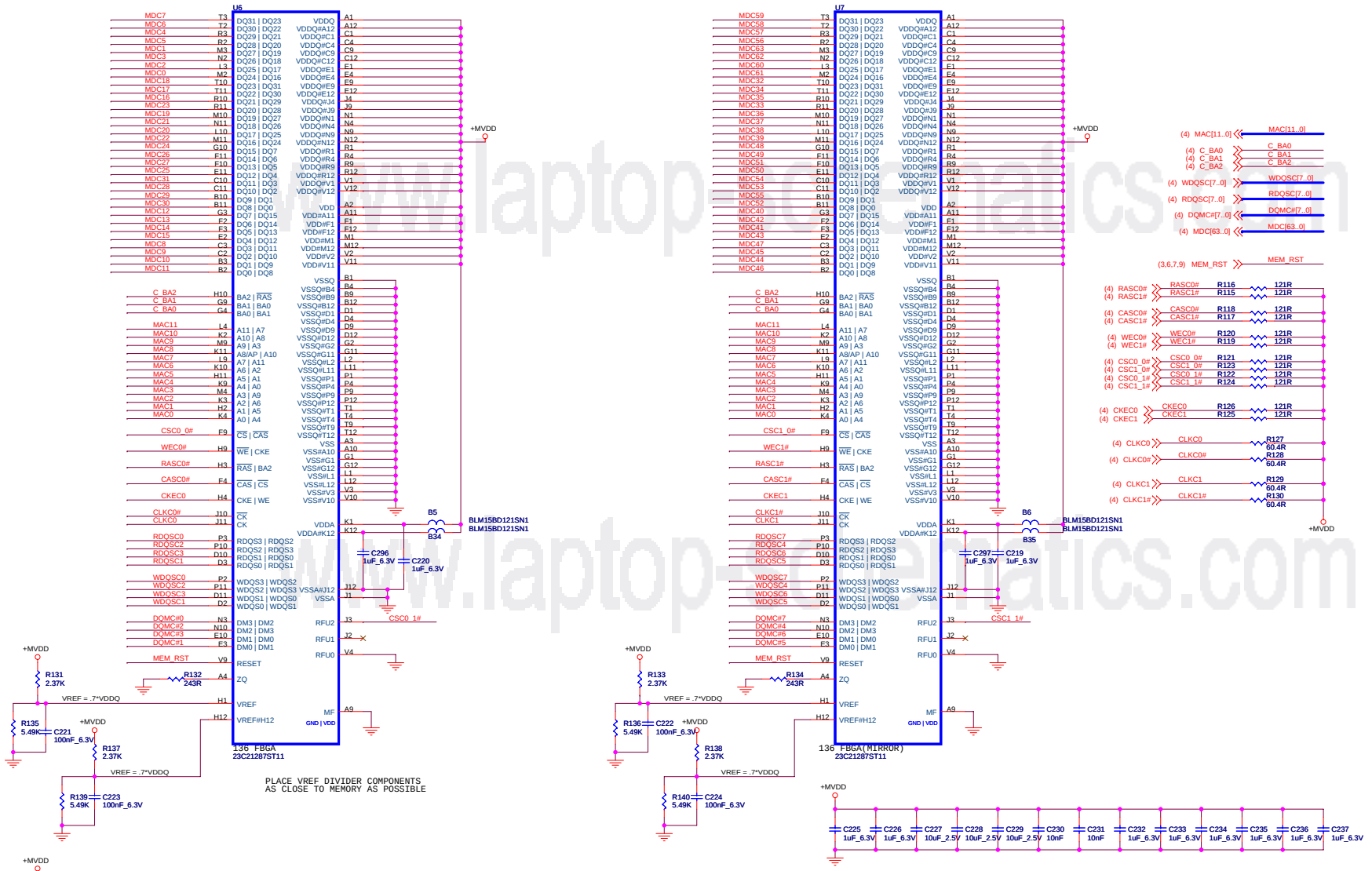

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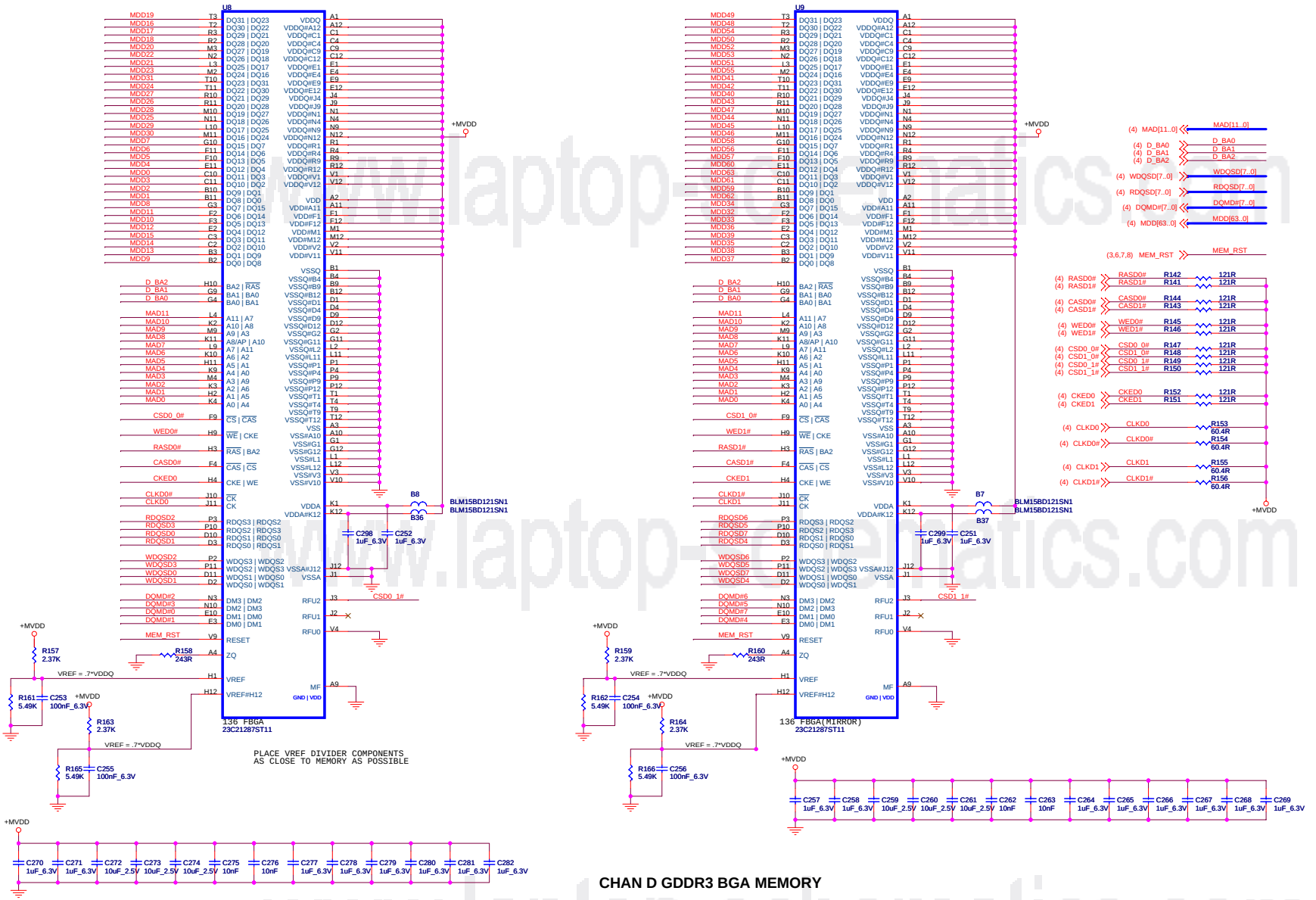

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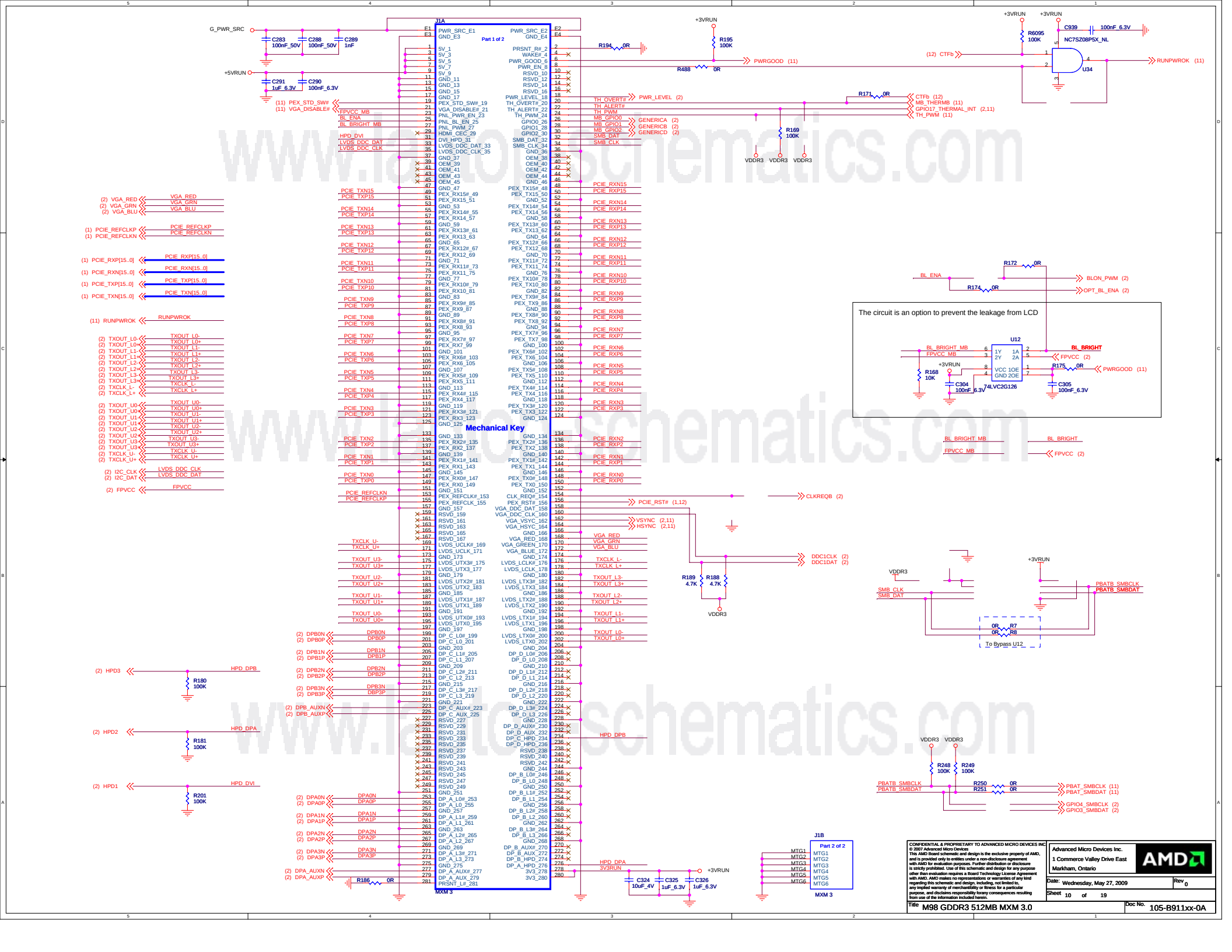
J1A
Part 1 of 2
Mechanical Key
MXM 3
J1B
Part 2 of 2
MXM 3
The circuit is an option to prevent the leakage from LCD
U12
74LVC2G126
U34
NC7SZ08P5X_NL
R180 100K
R181 100K
R201 100K
R186 0R
R194 0R
R195 100K
R488 0R
R171 0R
R169 100K
R172 0R
R174 0R
R168 10K
R175 0R
R6095 100K
R189 4.7K
R188 4.7K
R7 0R
R8 0R
R248 100K
R249 100K
R250 0R
R251 0R
C283 100nF_50V
C288 100nF_50V
C289 1nF
C291 1uF_6.3V
C290 100nF_6.3V
C324 10uF_4V
C325 1uF_6.3V
C326 1uF_6.3V
C939 100nF_6.3V
C304 100nF_6.3V
C305 100nF_6.3V
G_PWR_SRC
+5VRUN
+3VRUN
VDDR3
PWRGOOD (11)
RUNPWROK (11)
CTFb (12)
PWM_LEVEL (2)
CLKREQB (2)
PCIE_RST# (1,12)
VSYNC (2,11)
HSYNC (2,11)
DDC1CLK (2)
DDC1DAT (2)
BLON_PWM (2)
OPT_BL_ENA (2)
BL_ENA
BL_BRIGHT
FPVCC (2)
PBAT_SMBCLK
PBAT_SMBDAT
To Bypass U12
HPD_DPB
HPD_DPA
HPD_DVI
HPD_LEVEL (2)
GENERICA (2)
GENERICB (2)
GENERICD (2)
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_RXP[15..0]
PCIE_RXN[15..0]
PCIE_TXP[15..0]
PCIE_TXN[15..0]
VGA_RED
VGA_GRN
VGA_BLU
TXOUT_L0-
TXOUT_L0+
TXOUT_L1-
TXOUT_L1+
TXOUT_L2-
TXOUT_L2+
TXOUT_L3-
TXOUT_L3+
TXCLK_L-
TXCLK_L+
TXOUT_U0-
TXOUT_U0+
TXOUT_U1-
TXOUT_U1+
TXOUT_U2-
TXOUT_U2+
TXOUT_U3-
TXOUT_U3+
TXCLK_U-
TXCLK_U+
I2C_CLK
I2C_DAT
LVDS_DDC_CLK
LVDS_DDC_DAT
FPVCC
DPB0N
DPB0P
DPB1N
DPB1P
DPB2N
DPB2P
DPB3N
DPB3P
DPB_AUXN
DPB_AUXP
DPA0N
DPA0P
DPA1N
DPA1P
DPA2N
DPA2P
DPA3N
DPA3P
DPA_AUXN
DPA_AUXP
PEX_STD_SW#
VGA_DISABLE#
FPVCC_MB
BL_ENA
BL_BRIGHT_MB
HPD_DVI
LVDS_DDC_DAT
LVDS_DDC_CLK
SMB_CLK
SMB_DAT
TH_OVERT#
TH_ALERT#
TH_PWM
MB_GPIO0
MB_GPIO1
MB_GPIO2
SMB_DAT
SMB_CLK
MB_THERMB (11)
GPIO17_THERMAL_INT (2,11)
TH_PWM (11)
GPIO4_SMBCLK (2)
GPIO3_SMBDAT (2)
3V3RUN
PCIE_RXN15
PCIE_RXP15
PCIE_RXN14
PCIE_RXP14
PCIE_RXN13
PCIE_RXP13
PCIE_RXN12
PCIE_RXP12
PCIE_RXN11
PCIE_RXP11
PCIE_RXN10
PCIE_RXP10
PCIE_RXN9
PCIE_RXP9
PCIE_RXN8
PCIE_RXP8
PCIE_RXN7
PCIE_RXP7
PCIE_RXN6
PCIE_RXP6
PCIE_RXN5
PCIE_RXP5
PCIE_RXN4
PCIE_RXP4
PCIE_RXN3
PCIE_RXP3
PCIE_RXN2
PCIE_RXP2
PCIE_RXN1
PCIE_RXP1
PCIE_RXN0
PCIE_RXP0
TXCLK_U-
TXCLK_U+
TXOUT_U3-
TXOUT_U3+
TXOUT_U2-
TXOUT_U2+
TXOUT_U1-
TXOUT_U1+
TXOUT_U0-
TXOUT_U0+
TXCLK_L-
TXCLK_L+
TXOUT_L3-
TXOUT_L3+
TXOUT_L2-
TXOUT_L2+
TXOUT_L1-
TXOUT_L1+
TXOUT_L0-
TXOUT_L0+
HPD_DPB
HPD_DPA
3V3RUN
MTG1
MTG2
MTG3
MTG4
MTG5
MTG6
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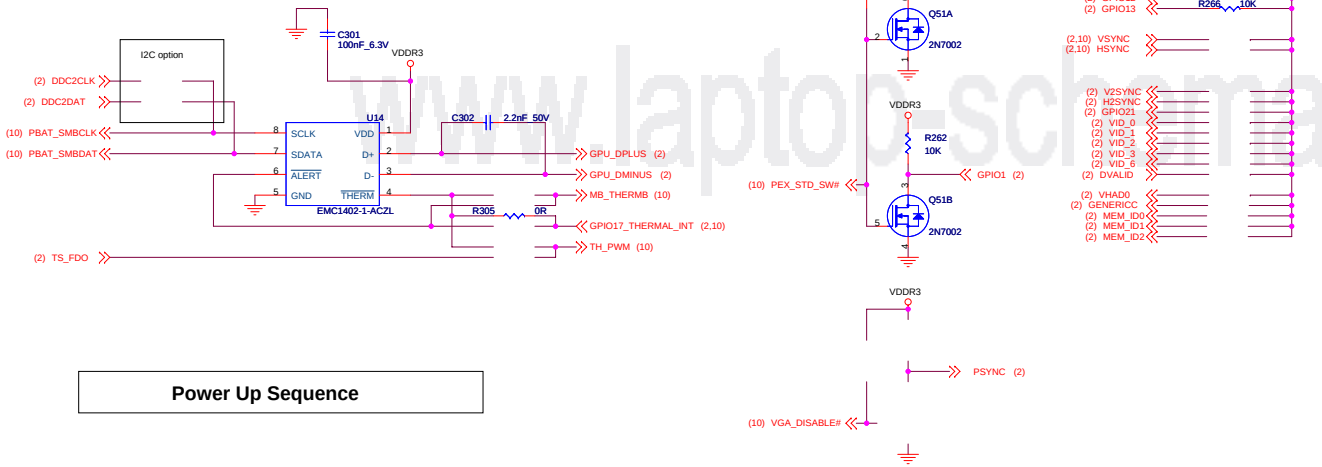
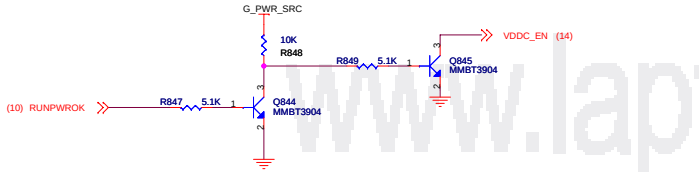
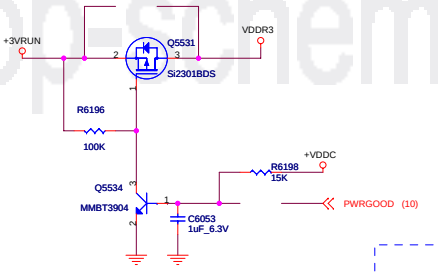
External Thermal Sensor



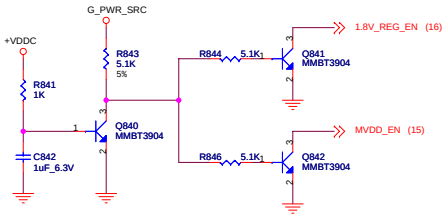
Strap Name	Pin Straps description		Default Value
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop) GPIO0 and GPIO1 pulls ups need to be stuffed with Q51 if system board is controlling the PCIE swing.	0
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
BIF_GEN2_EN	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
DEBUG_I2C_ENABLE	GPIO6	Internal use only, THIS PAD HAS AN INTERNALPULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected, however, if it is connected to additional logic on the board, the logic must not allow this signal to be driven or pulled to any value except GND at reset.	0
MSI_DIS	VID_1	Disable Message Signaled Interrupt is both a ROM strap and a pin strap. The pin strap is only applicable if a BIOS ROM is not present.	0
AUDIO_EN	GPIO8	Enable HD Audio function in the PCI configuration space. 0 - Disable HD Audio 1 - Enable HD Audio	1
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11	GPIO9,13,12,11 (config 3,2,1,0): a> If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM Type: b> If BIOS_ROM_EN = 0, then Config[3:0] defines the Aperture size:Size of the primary memory apertures claimed in PCI configuration space 000 = 128MB 001 = 256MB 010 = 64MB 011 = 32MB 100 = 512MB 101 = 1GB 110 = 2GB 111 = 4GB	0101
BIF_CLK_PM_EN	DVALID	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
VIP_DEVICE_STRAP_EN	VSYNC	VSYNC - VIP_DEVICE_STRAP_EN 0: Driver would ignore the value sampled on VHAD_0 during reset. 1: Driver would use the sampled value sampled at reset from VHAD_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (0 indicates yes, 1 indicates no)	0
VIP_DEVICE	VHAD_0	If VIP_DEVICE_STRAP_EN is set to '1', then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to '0', then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
VGA_DIS	PSYNC	PSYNC - VGA DISABLE : 0 – VGA Controller capacity enabled 1 – The device will not be recognized as the system's VGA ontroller PSYNC pull up needs to be stuffed with Q5537 if system board is controlling the VGA capacity	0
HDMI_EN	HSYNC	HSYNC - HDMI_EN HDMI connector presence. 0 – No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
RX_PLL_CALIB_BYPASS	GPIO21	Internal use only.	0
FORCE_COMPLIANCE_A	VID_3	Internal use only.	0

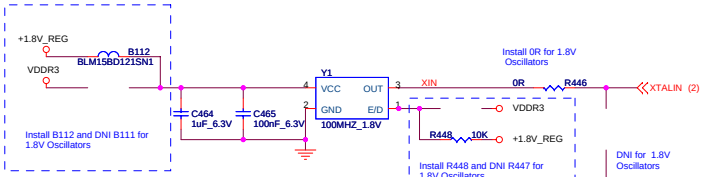
Power Up Sequence





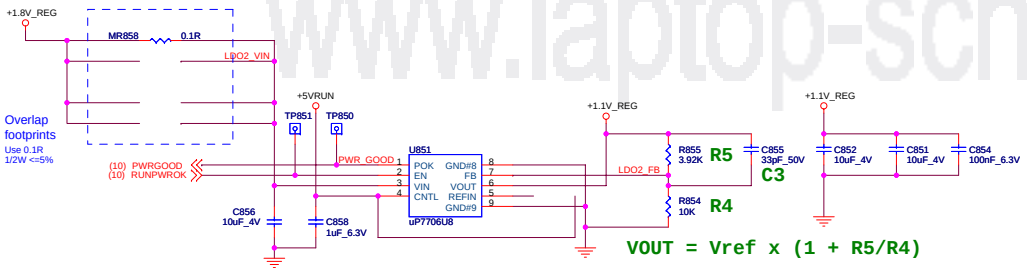
VDDR3 Enable Circuit

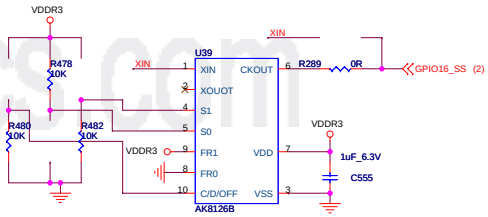




LDO #2: Vin = +1.8V +/-5% Vout = +1.1V +/- 2% Iout = 1.7A (TBV) RMS MAX

PCB: 50 to 70mm sq. copper area for cooling





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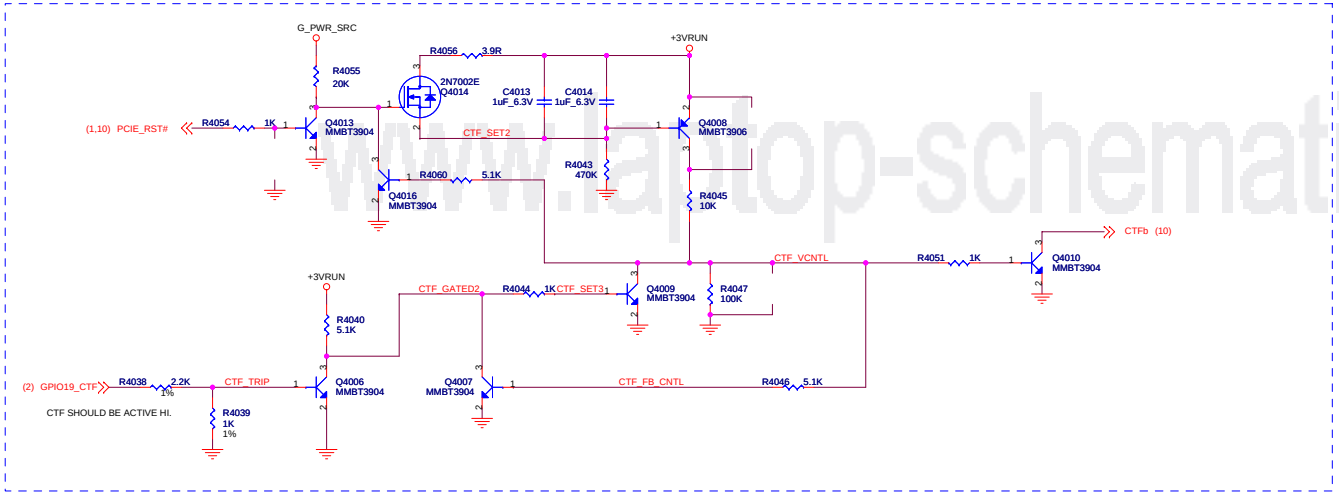
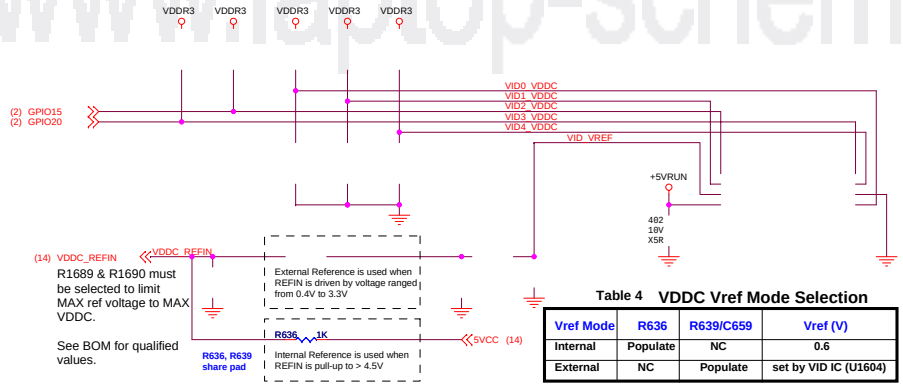
Optional Critial Temperature Fault



Power Play

Optional VID for VDDC Setting



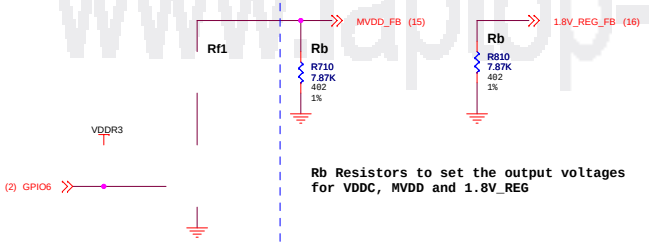
GPIO20	GPIO15	VDDC
0	0	TBD
0	1	TBD
1	0	TBD
1	1	TBD

Table 4 VDDC Vref Mode Selection

Vref Mode	R636	R639/C659	Vref (V)
Internal	Populate	NC	0.6
External	NC	Populate	set by VID IC (U1604)

Optional MVDD Voltage Control

	GPIO6	MVDD
	0	TBD
	1	TBD

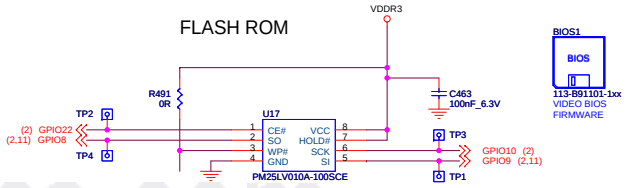


Rb VDDC Lower Resistor

R650 must be populated only if VID is not used. This will set VDDC to a fixed value

Rb Resistors to set the output voltages for VDDC, MVDD and 1.8V_REG

Vout = Vref * (1+Rt/Rb)
Dual: Vref = 0.6V, Rt = 10k
Single: Vref = 0.8V, Rt = 10k



SERIAL EEPROM 512K/1M
PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

DESIGN MUST KEEP TEST POINTS AND TRACES OUT OF ASIC BALLS FOR DEBUG.

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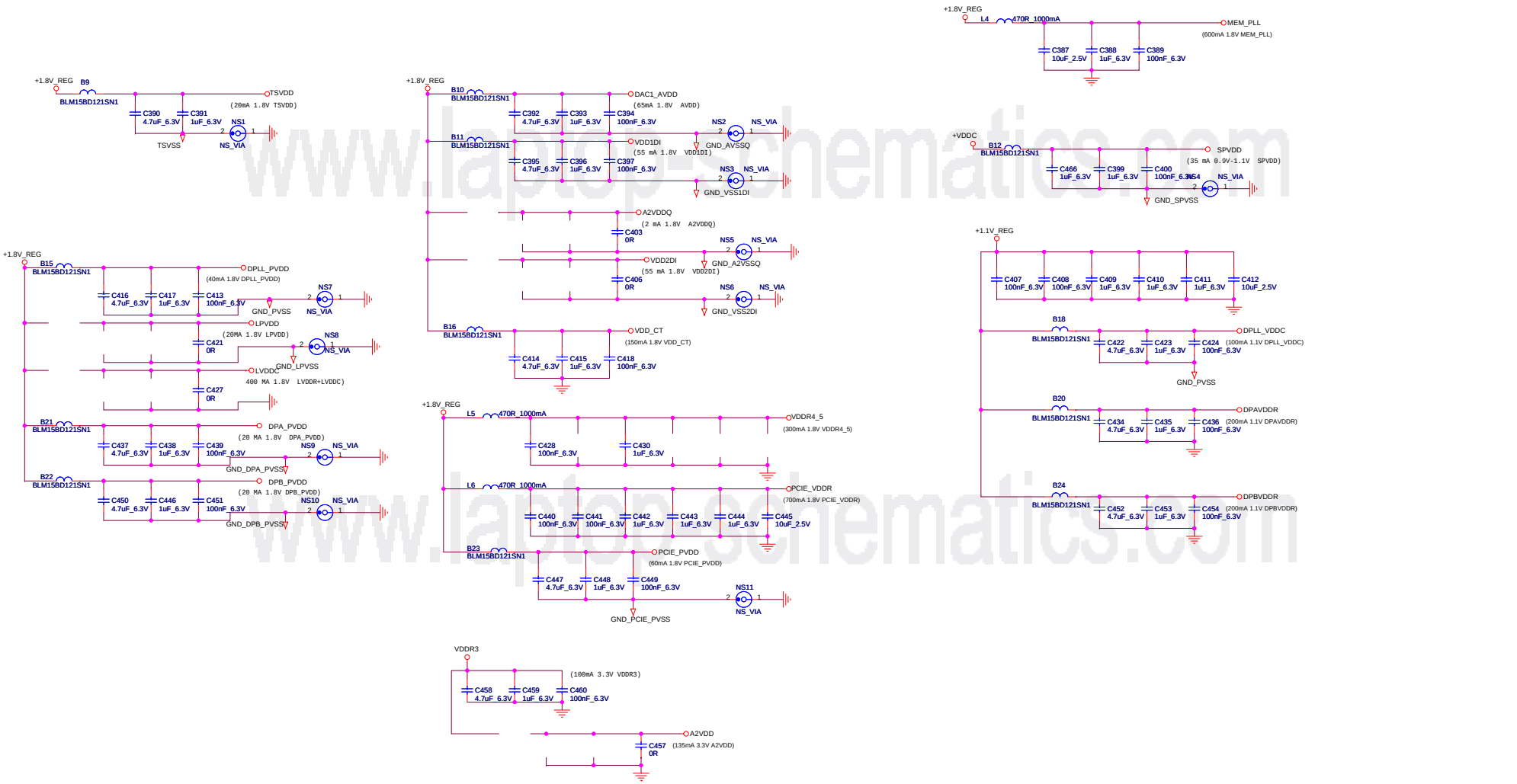

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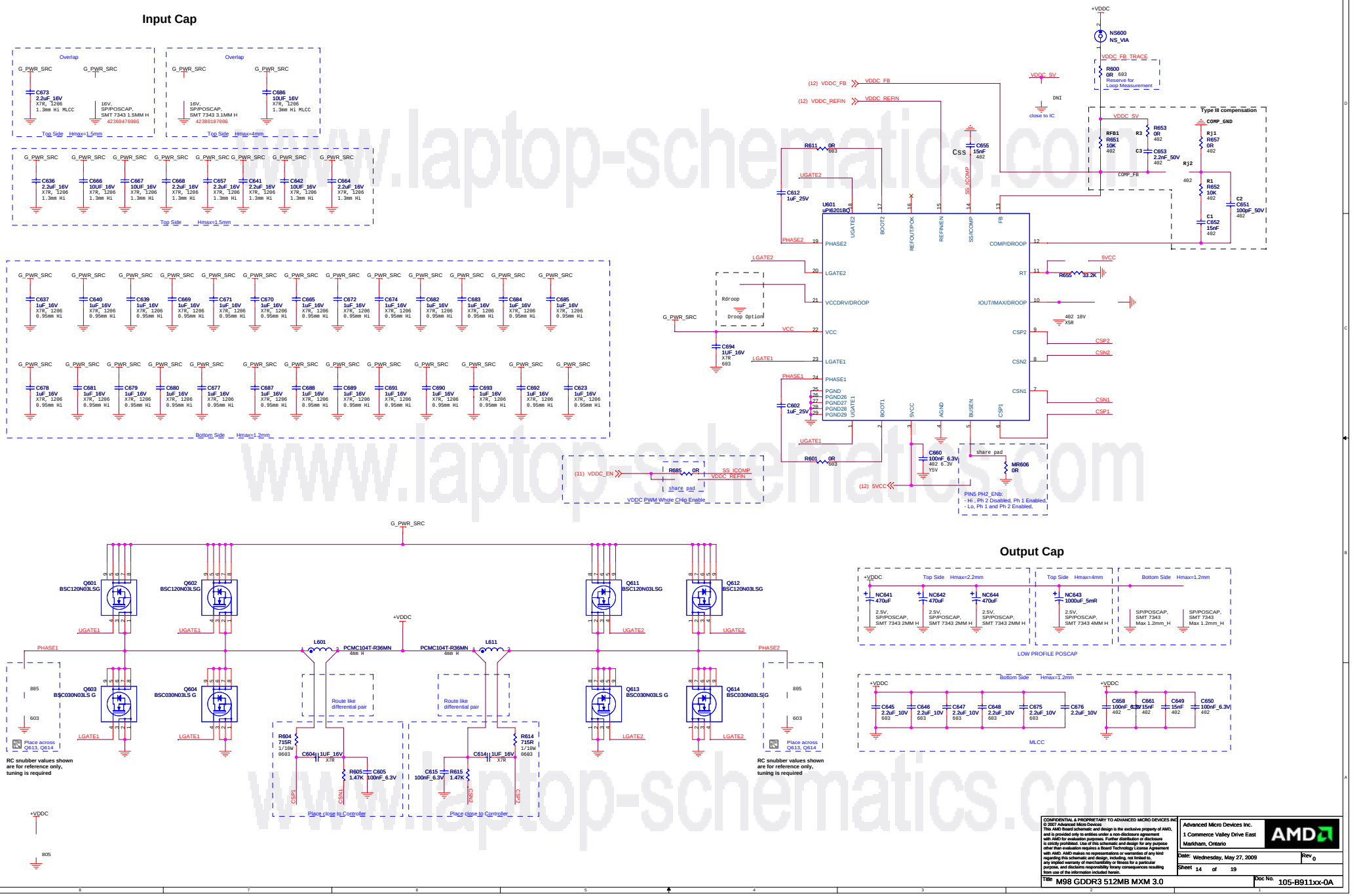

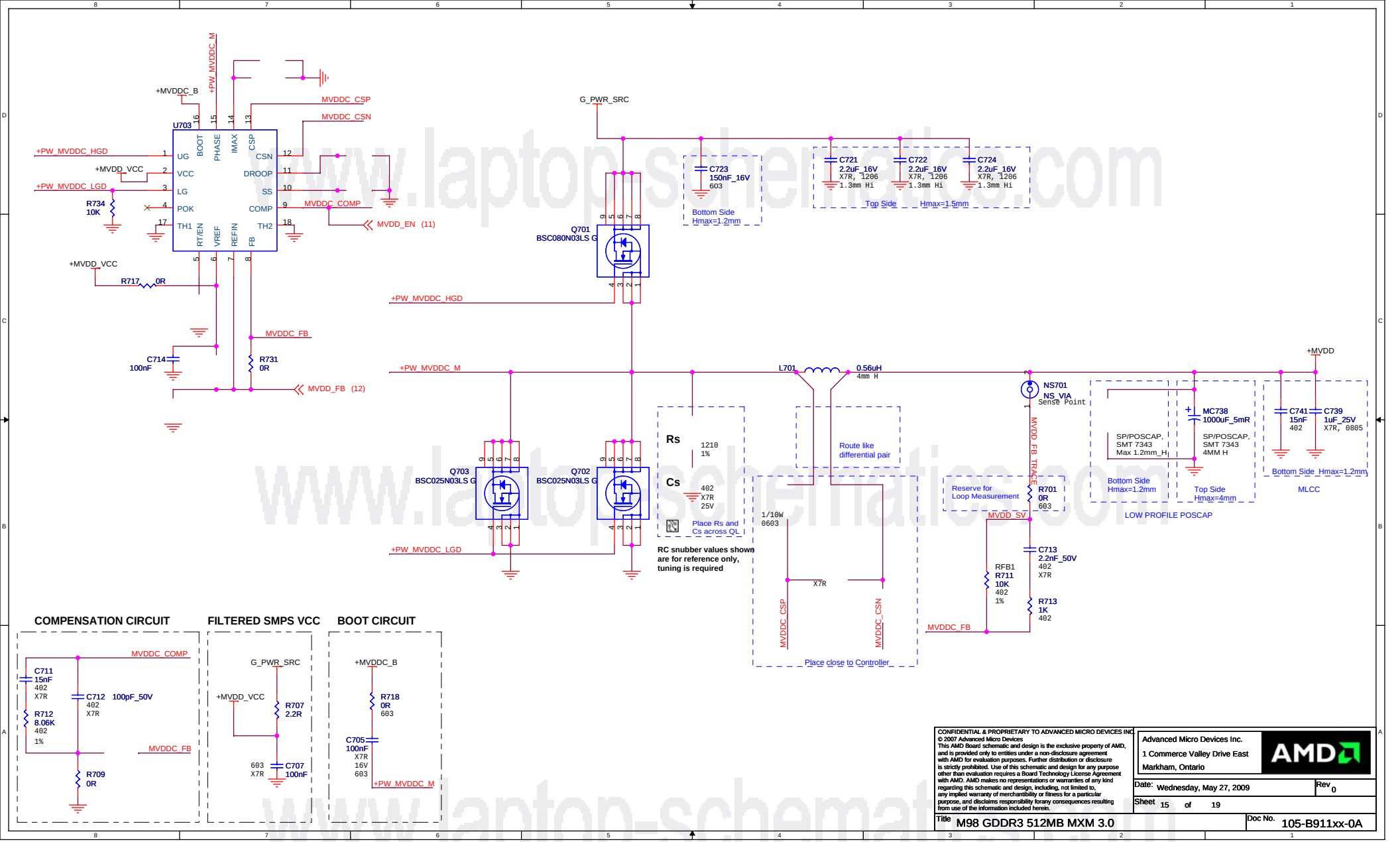

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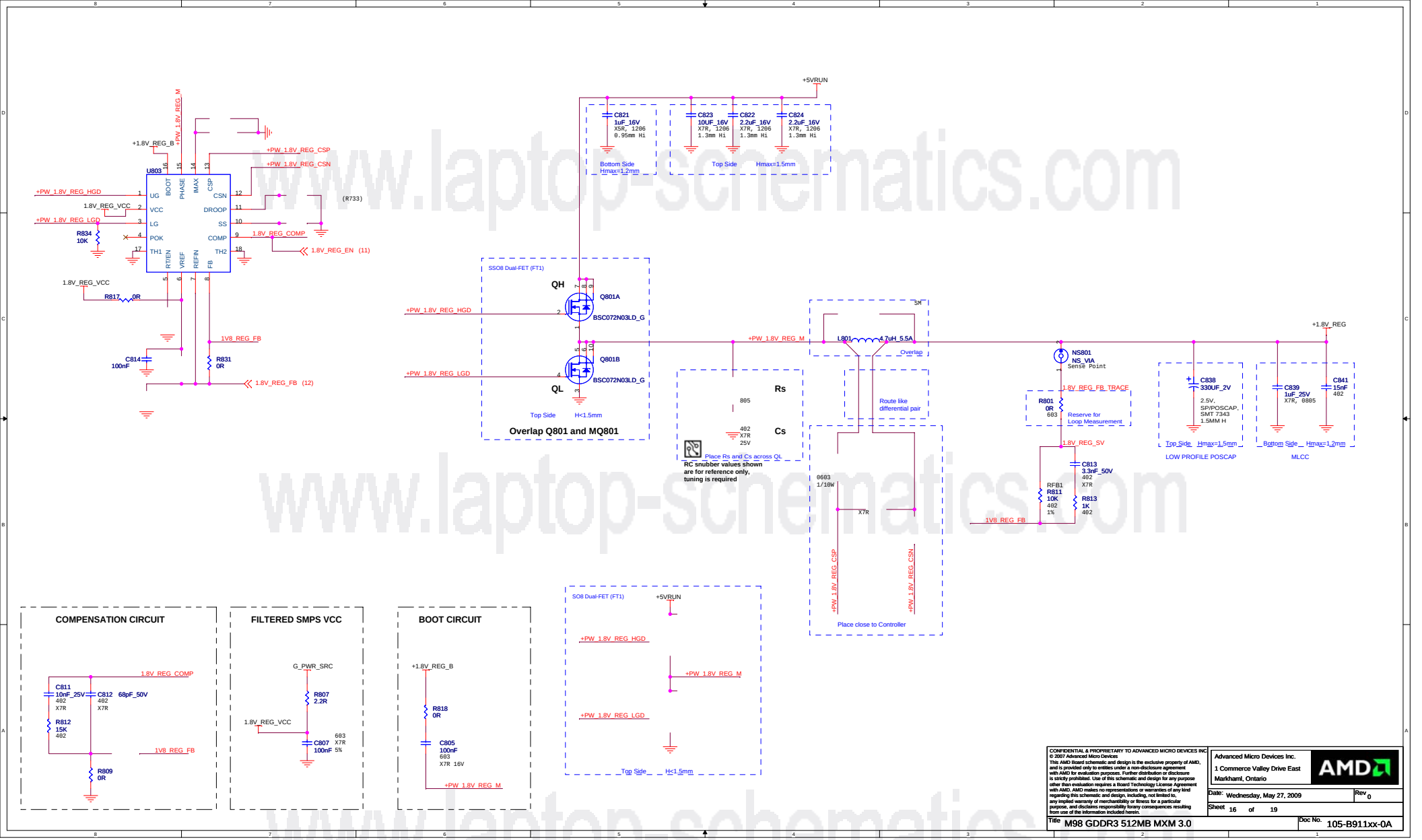

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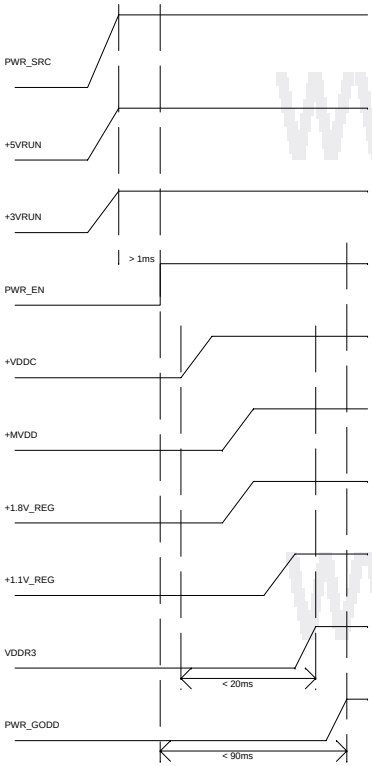
POWER UP SEQUENCE (not to scale)



VDDC, VDDCI, SPVDD

VDDR1, MVDDQ/C

VDDR4/5, VDD_CT, TSVDD, PCIE_VDDR, PCIE_PVDD, DPLL_PVDD, DPx_PVDD, LPVDD, LVDDC, MPVDD, AVDD, VDD1DI

PCIE_VDDC, DPLL_VDDC, DPxVDDR

+1.1V_REG AND VDDR3 RAMP UP SEQUENCE CAN BE INTERCHANGED.

VDDR3

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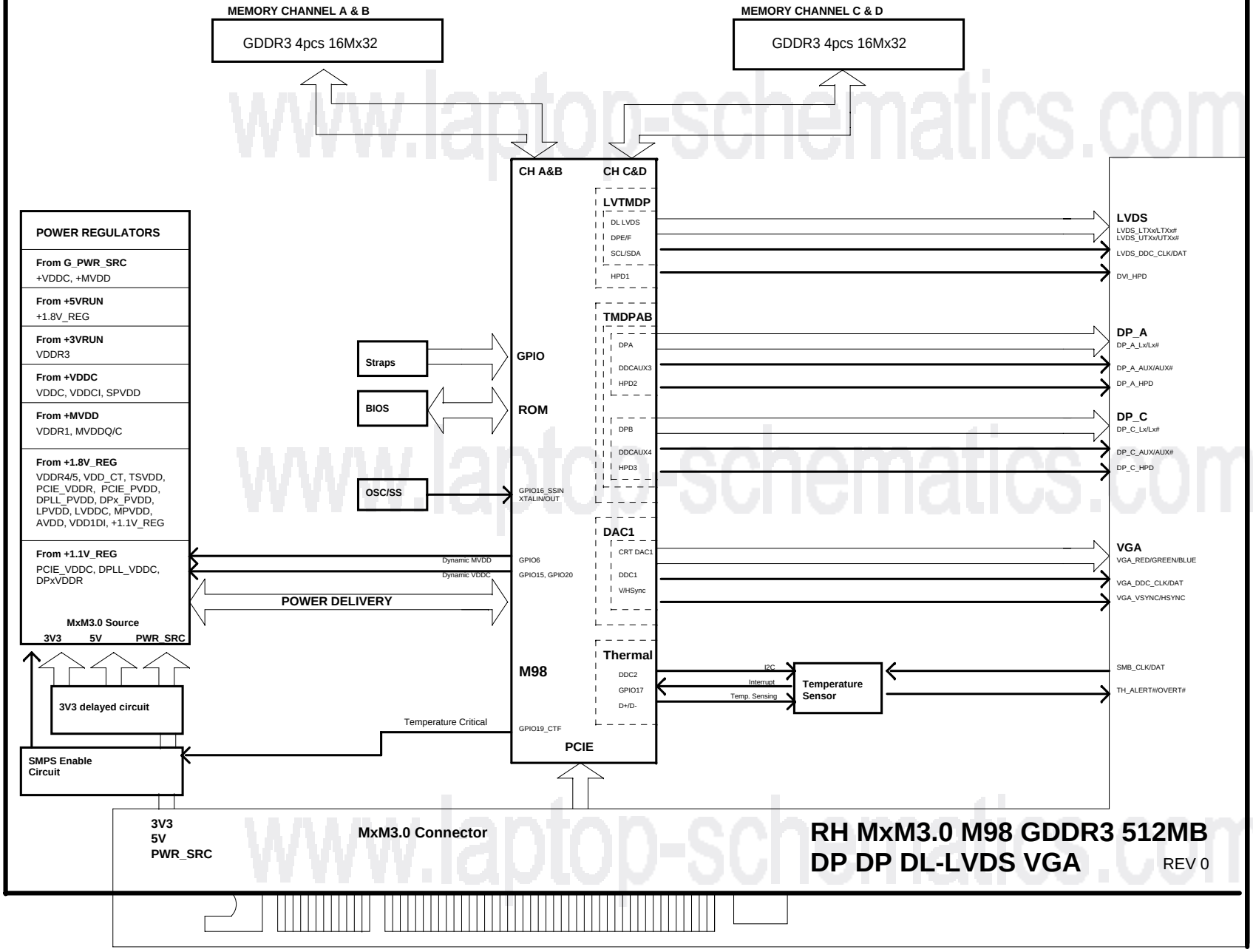

RH MxM3.0 M98 GDDR3 512MB
DP DP DL-LVDS VGA REV 0

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Title	M98 GDDR3 512MB MXM 3.0
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Title	Schematic No.	Date:
M98 GDDR3 512MB MXM 3.0	105-B911xx-0A	Wednesday, May 27, 2009

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 0

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	09/04/15	Initial design based on B909-00; A series resistor (R1000) and a shunt cap (C1000) are added to mem_rst signal