P815-D00: G96 MXM V3.0
128/256MB 128-BIT GDDR3
LVDS, QUAD DP

Table of Contents

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10815-base-300	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL.
1	SKU0000	600-10815-0000-300	G96M 128bit GDDR3 MXM V3.0
2	SKU0001	600-10815-0001-300	P815-C00 SKU1 G96-600 MXM3.0 TYPE-B 512MB 4pcs 32Mx32
3	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	Cover Page

NVIDIA CORPORATION
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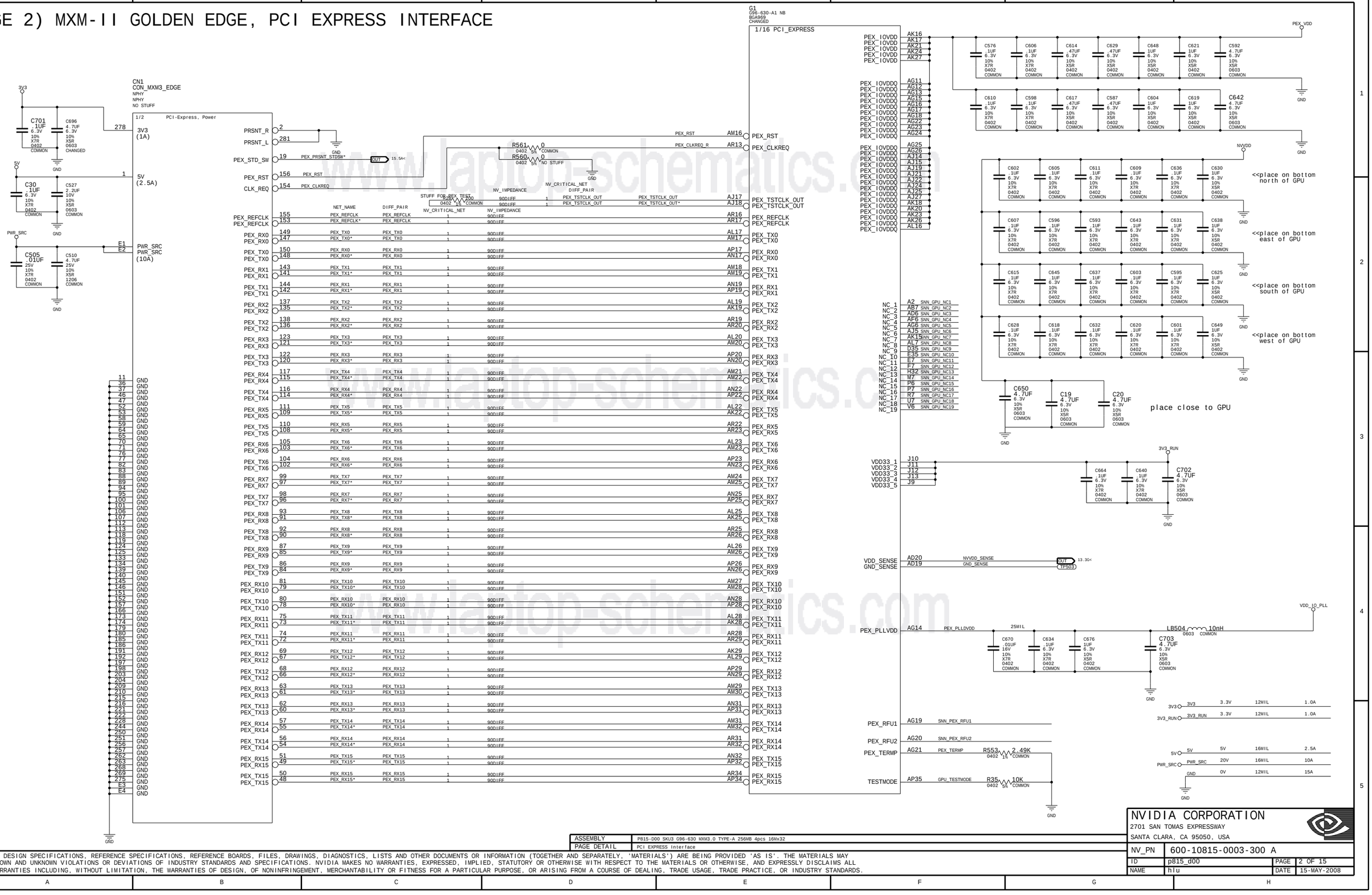
NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	1 OF 15
NAME	hlu	DATE	15-MAY-2008

PAGE 2) MXM-II GOLDEN EDGE, PCI EXPRESS INTERFACE



ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	PCI EXPRESS Interface

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2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	2 OF 15
NAME	hlu	DATE	15-MAY-2008

PAGE 3) GPU MEMORY INTERFACE

ASSEMBLY	P815-D00 SKU3 G96-630 WXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	Frame Buffer GPU Interface

NVIDIA CORPORATION
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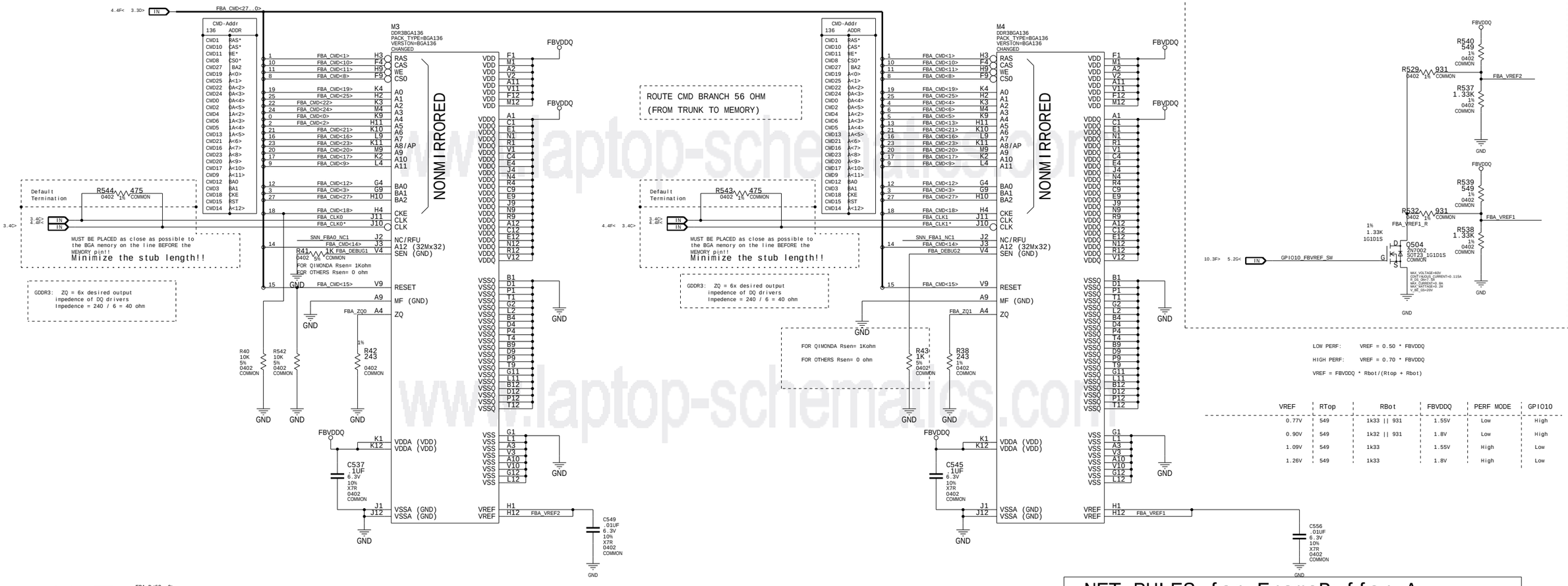
NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	3 OF 15
NAME	hlu	DATE	15-MAY-2008

FRAME BUFFER PARTITION A



NET RULES for FrameBuffer A

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBA_CLK0	1	80DIFF	FBA_CLK0
FBA_CLK0*	1	80DIFF	FBA_CLK0
FBA_CLK1	1	80DIFF	FBA_CLK1
FBA_CLK1*	1	80DIFF	FBA_CLK1

NET	NV_CRITICAL	NV_IMPEDANCE
FBA_DQS_WP<7..0>	1	40OHM
FBA_DQS_RN<7..0>	1	40OHM
FBA_DQM<7..0>	1	40OHM
FBA_D<63..0>	1	40OHM
FBA_CMD<27..0>	1	60OHM

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBA_VREF0	1.26V	0.02A	12MIL
FBA_VREF1	1.26V	0.02A	12MIL
FBA_VREF2	1.26V	0.02A	12MIL
FBA_VREF3	1.26V	0.02A	12MIL
FBA_ZQ0	1.26V	0.02A	12MIL
FBA_ZQ1	1.26V	0.02A	12MIL

ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	Frame Buffer Partition A Memories

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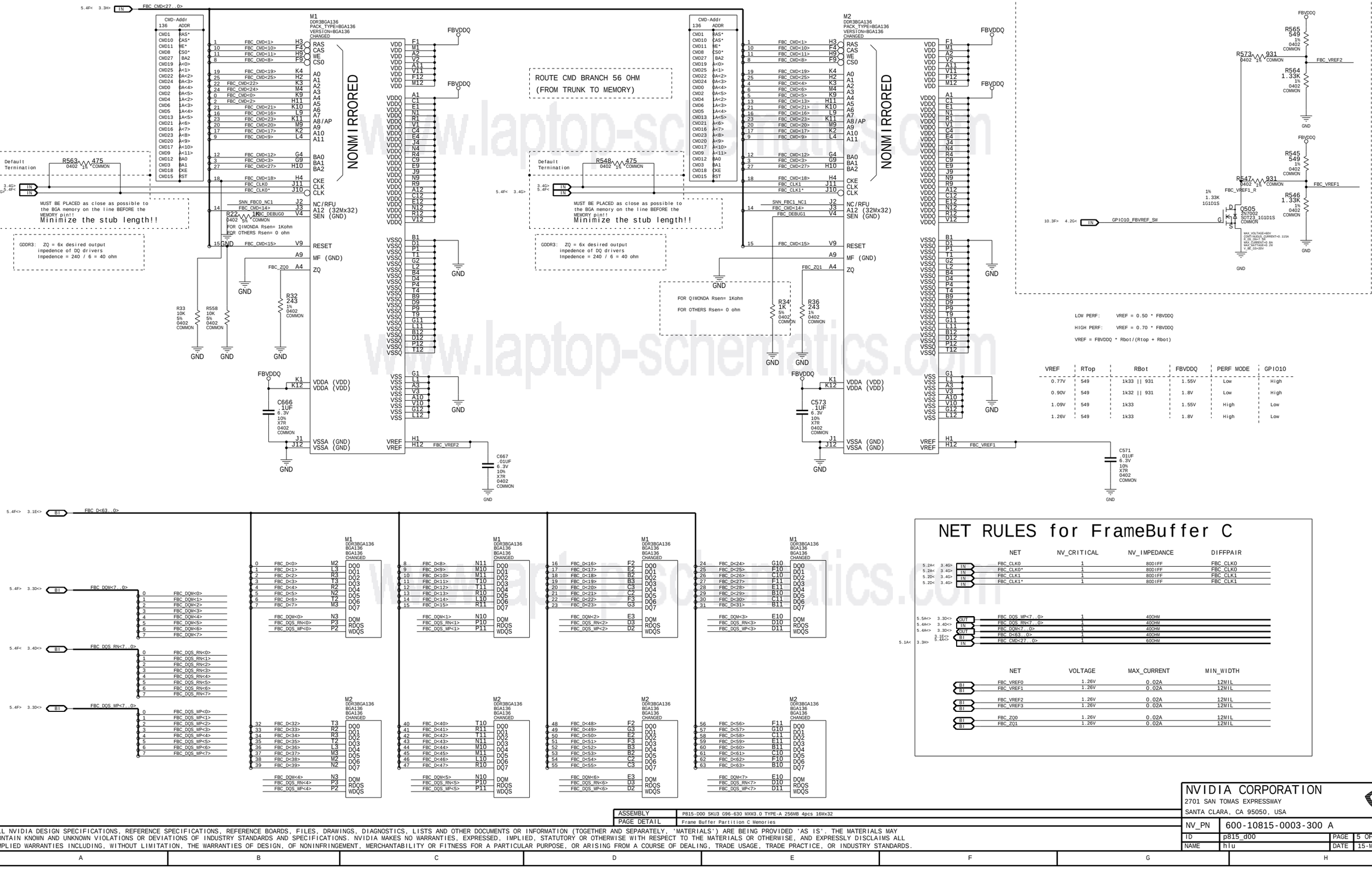
SANTA CLARA, CA 95050, USA

NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	4 OF 15
NAME	hlu	DATE	15-MAY-2008

PAGE 5) MEMORY PARTITION C



VREF	RTop	RBot	FBVDDQ	PERF MODE	GPIO10
0.77V	549	1k33 || 931	1.55V	Low	High
0.90V	549	1k32 || 931	1.8V	Low	High
1.09V	549	1k33	1.55V	High	Low
1.26V	549	1k33	1.8V	High	Low

NET RULES for FrameBuffer C

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FBC_CLK0	1	80DIFF	FBC_CLK0
FBC_CLK0*	1	80DIFF	FBC_CLK0
FBC_CLK1	1	80DIFF	FBC_CLK1
FBC_CLK1*	1	80DIFF	FBC_CLK1

NET	NV_CRITICAL	NV_IMPEDANCE
FBC_DQS_WP<7..0>	1	40OHM
FBC_DQS_RN<7..0>	1	40OHM
FBC_DQM<7..0>	1	40OHM
FBC_D<63..0>	1	40OHM
FBC_CMD<27..0>	1	60OHM

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
FBC_VREF0	1.26V	0.02A	12MIL
FBC_VREF1	1.26V	0.02A	12MIL
FBC_VREF2	1.26V	0.02A	12MIL
FBC_VREF3	1.26V	0.02A	12MIL
FBC_ZQ0	1.26V	0.02A	12MIL
FBC_ZQ1	1.26V	0.02A	12MIL

ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	Frame Buffer Partition C Memories

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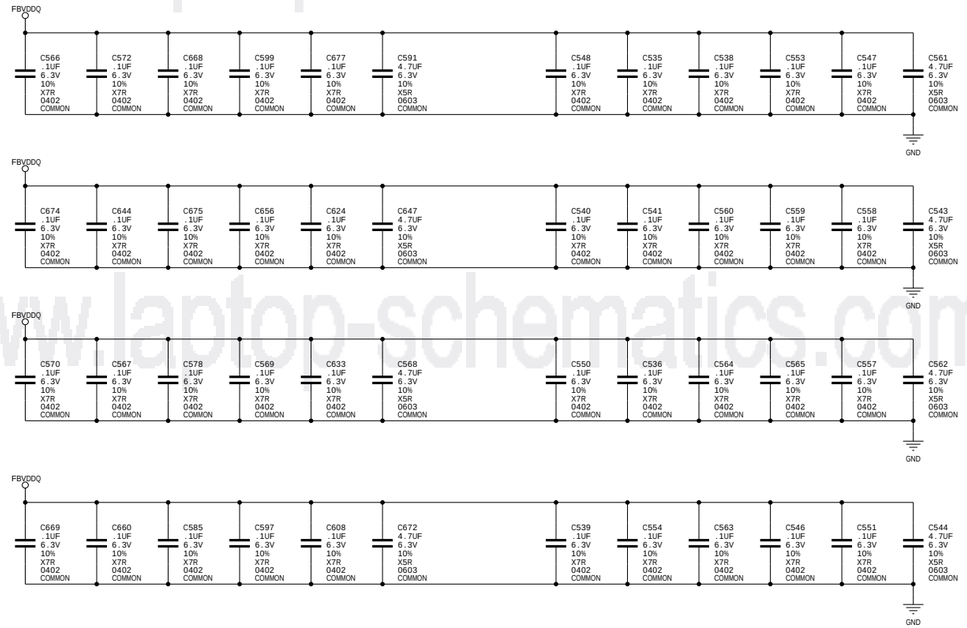
NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	5 OF 15
NAME	hlu	DATE	15-MAY-2008

PAGE 6) MEMORY DECOUPLING CAPS

DECOUPLING CAPS FOR MEMORYS (PARTION A AND PARTION C)



ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	Memory Decoupling Caps

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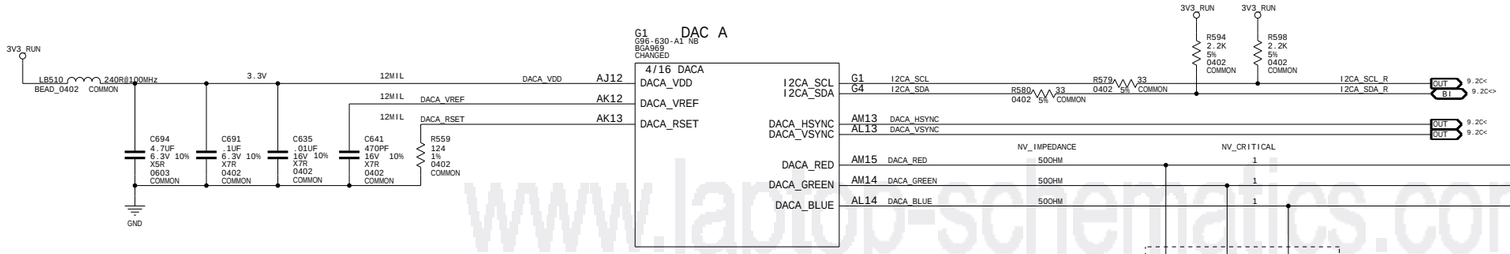
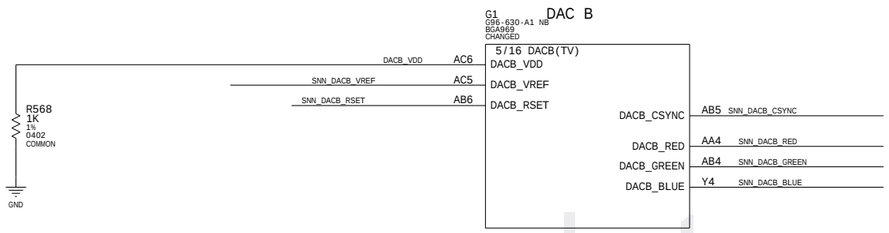
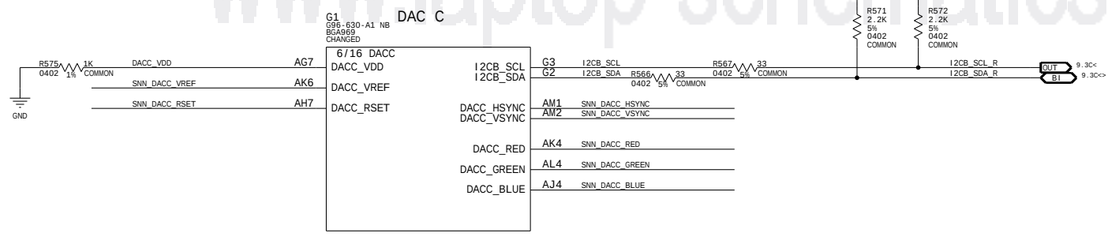
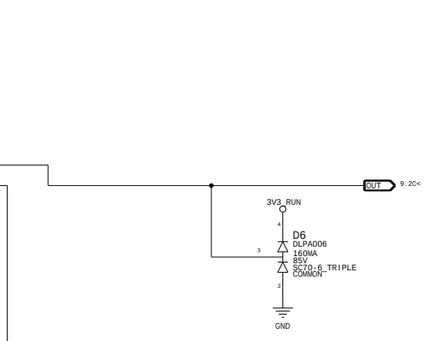
NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	6 OF 15
NAME	hlu	DATE	15-MAY-2008

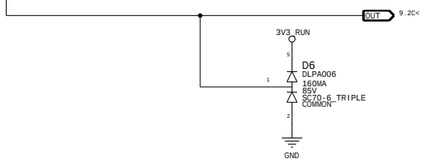
PAGE 7) DAC_A, DAC_B, DAC_C, PLL, CRYSTAL

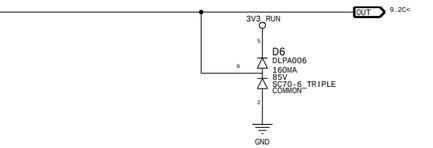








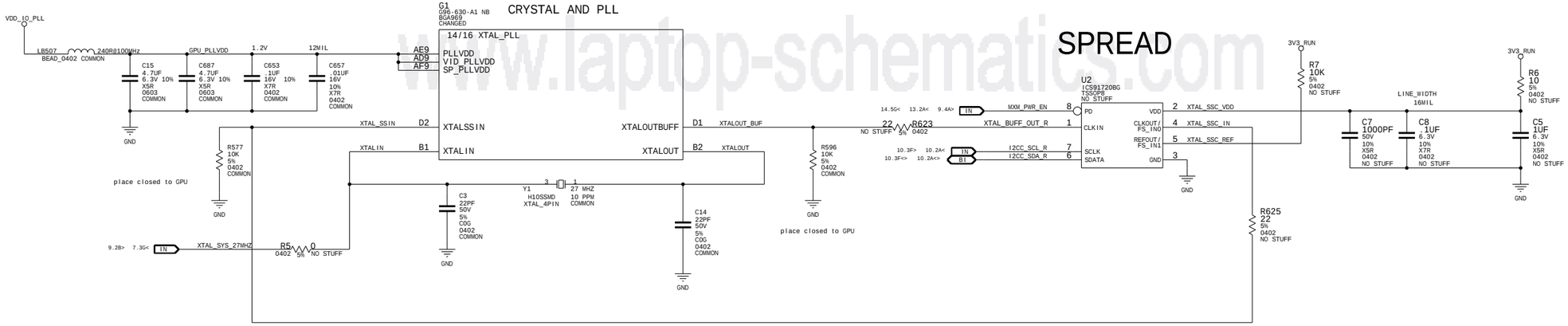




NV_NET_NAME	NV_IMPEDANCE	NV_CRITICAL_NET
XTALOUT	50OHM	1
XTALIN	50OHM	1
XTAL_SYS_27MHZ	50OHM	1

CRYSTAL AND PLL

SPREAD



ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	DACs, Clock-Generation

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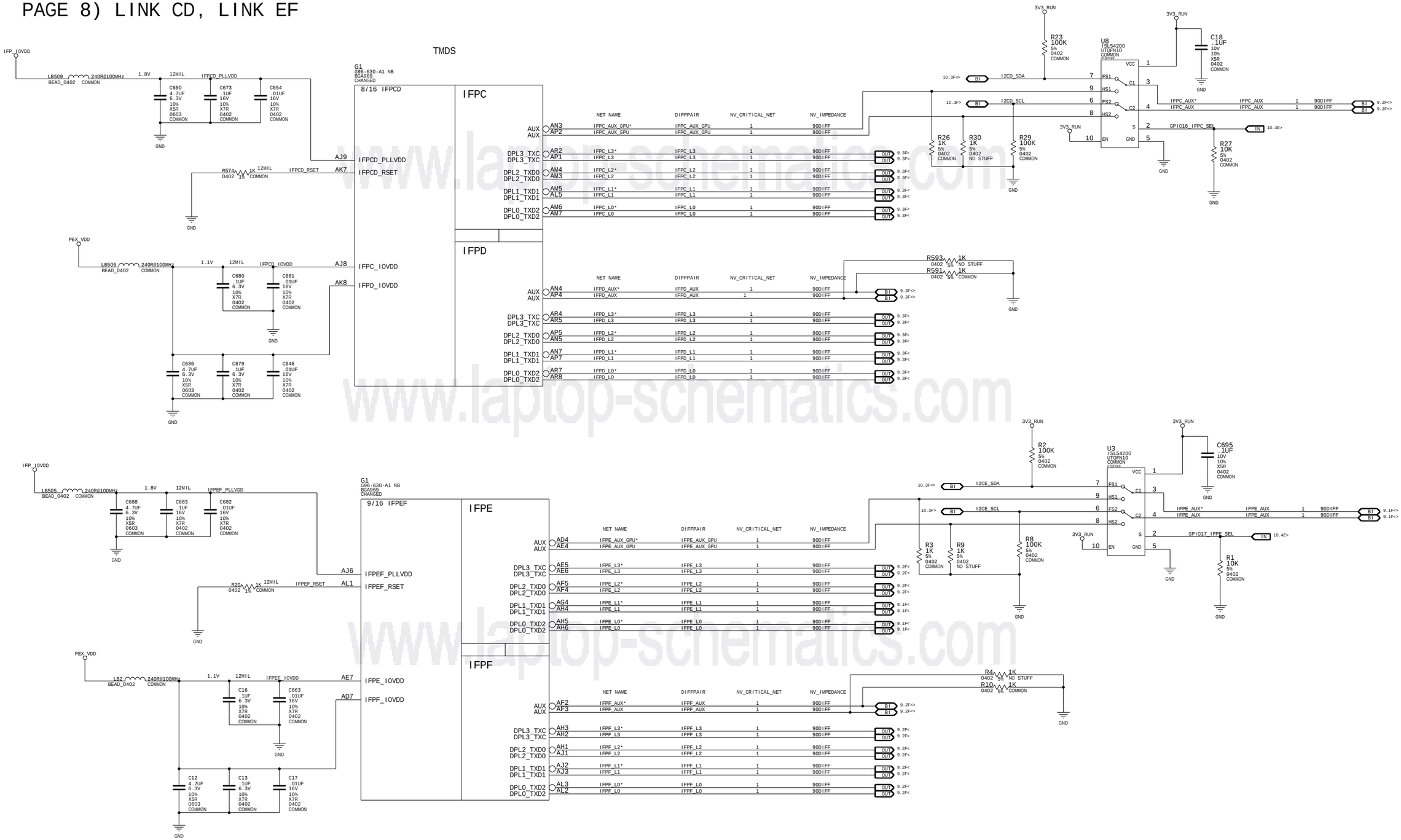
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	7 OF 15
NAME	hlu	DATE	15-MAY-2008

PAGE 8) LINK CD, LINK EF



ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	DP LINK C,D,E,F

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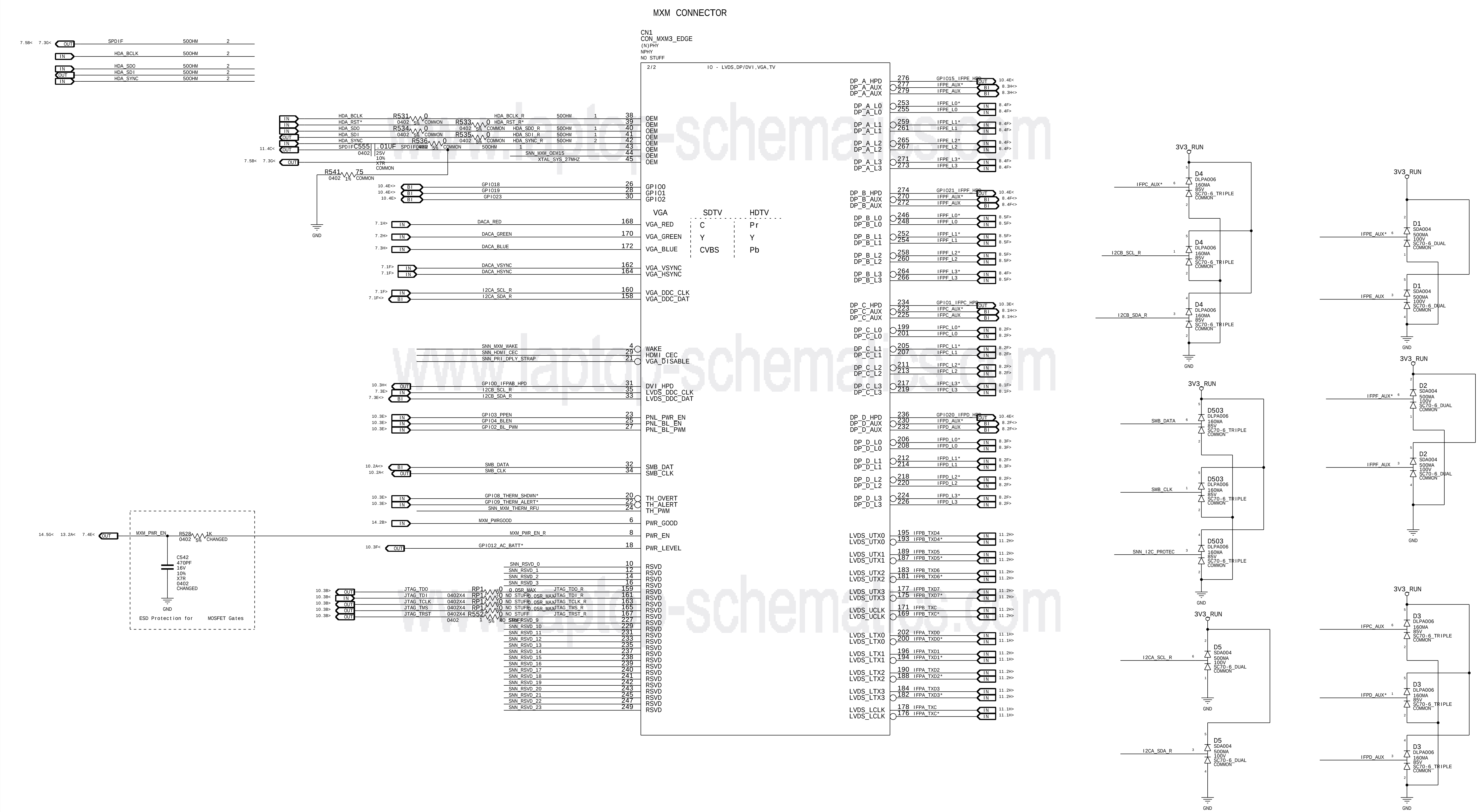
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	8 OF 15
NAME	hlu	DATE	15-MAY-2008

PAGE 9) MXM CONNECTOR

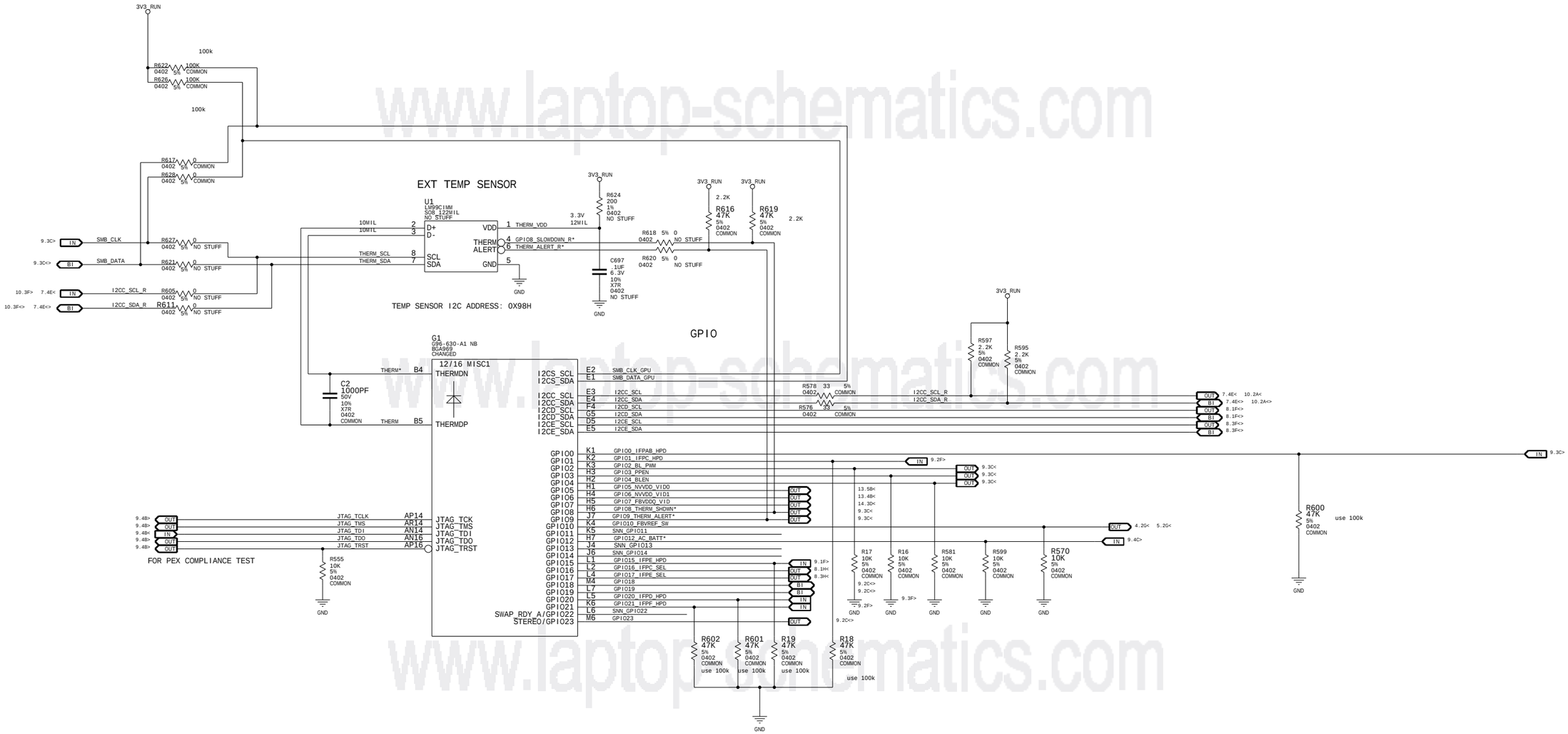


ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	MXM Connector, IO-Section

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	9 OF 15
NAME	hlu	DATE	15-MAY-2008

PAGE 10) GPIO, JTAG, TEMP SENSOR



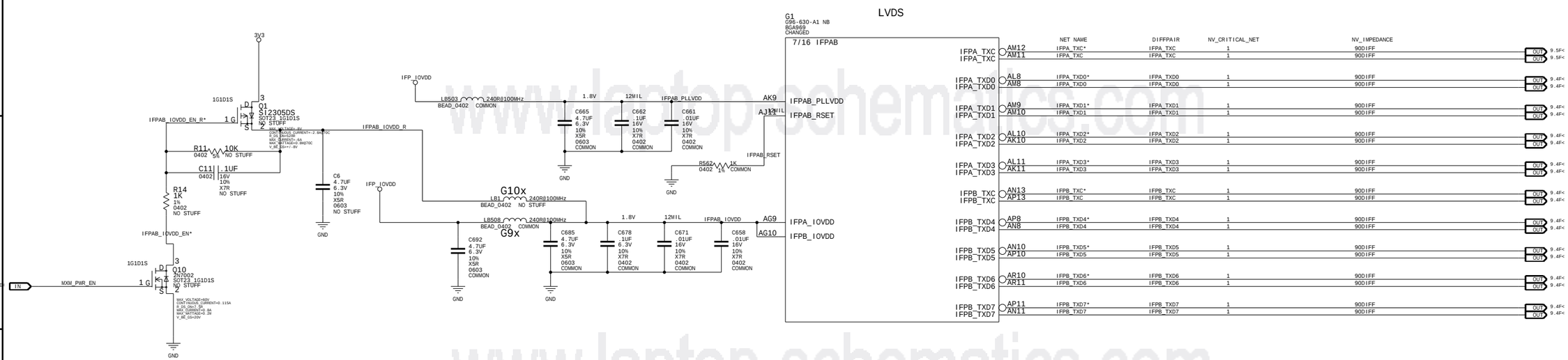
ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	GPIOs. JTAG, Thermal Senser

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

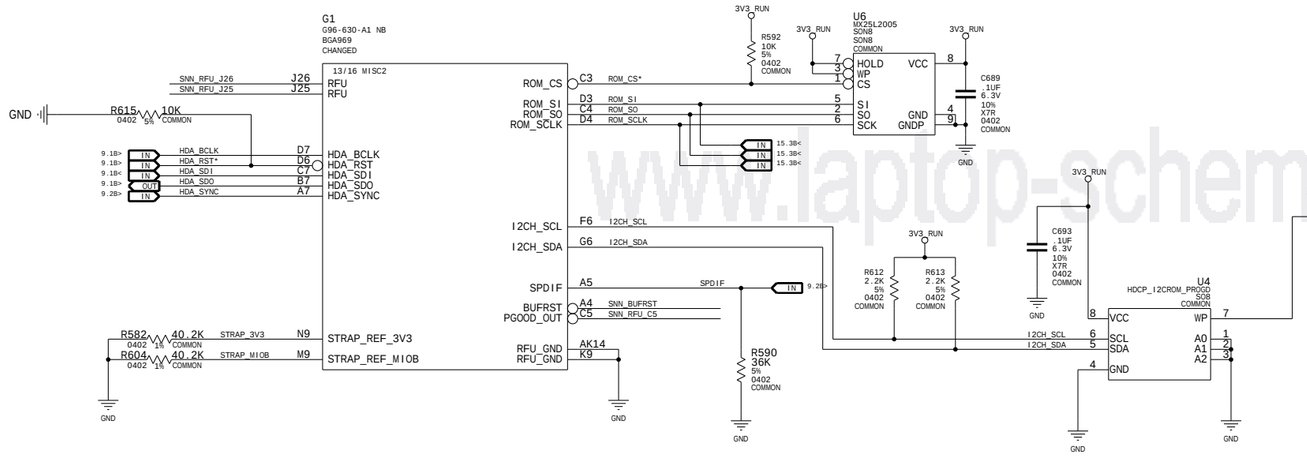
NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	10 OF 15
NAME	hlu	DATE	15-MAY-2008

PAGE 11) LVDS, VBIOS, HDCP ROM

LVDS



VBIOS AND HDCP ROM



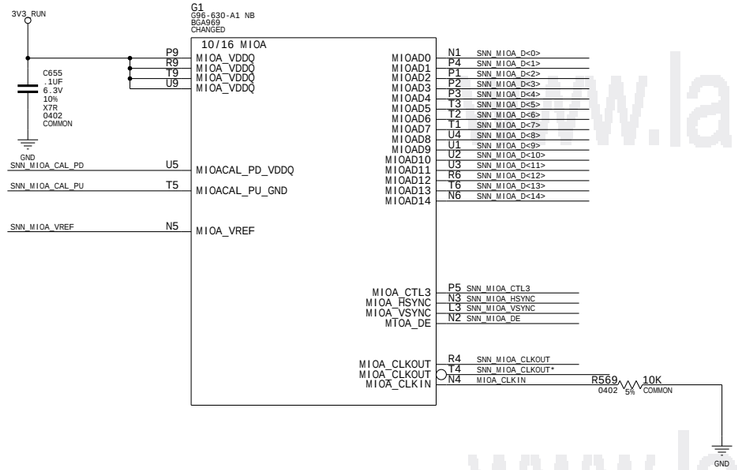
ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	LVDS, VBIOS and HDCP ROM

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

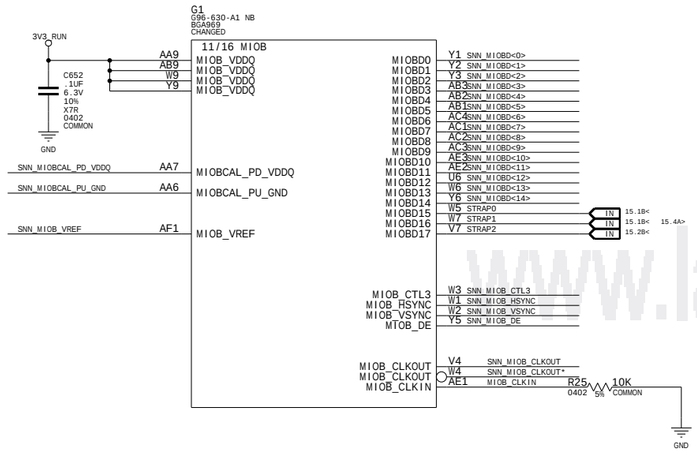
NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	11 OF 15
NAME	hlu	DATE	15-MAY-2008

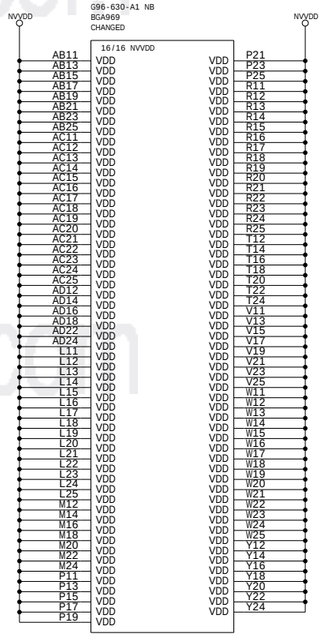
PAGE 12) MIOA(SLI), MIOB, GPU GND,

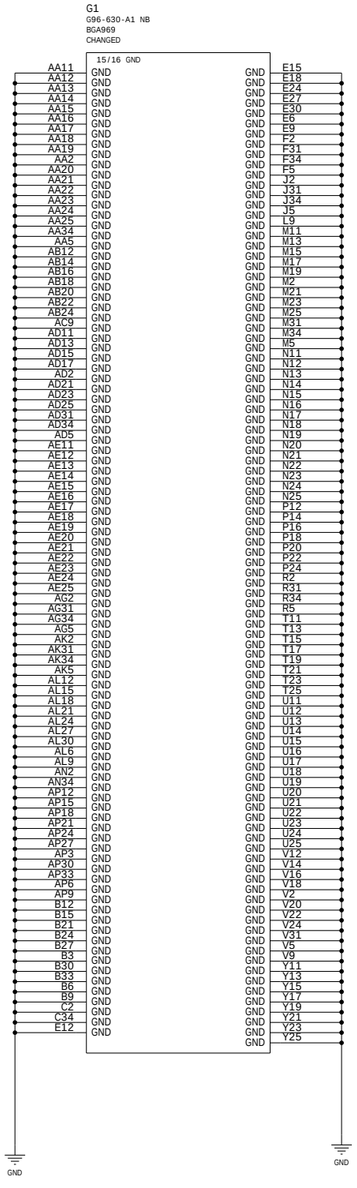
MIOA



MIOB







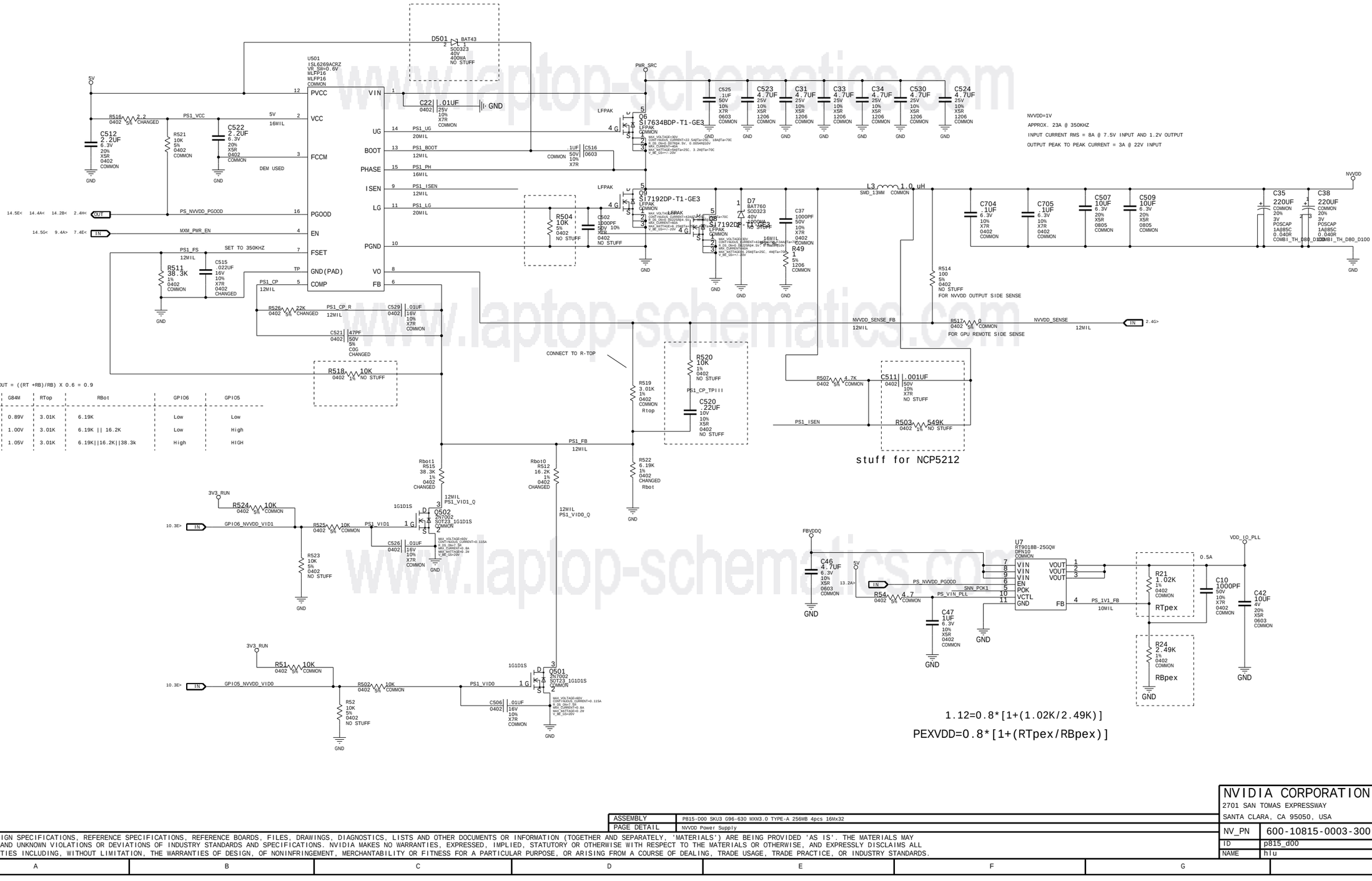
ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	MIOA, MIOB, GPU GND

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	12 OF 15
NAME	hlu	DATE	15-MAY-2008

PAGE 13) NVVDD POWER SUPPLY

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
NVVDD	1V	12MIL	30A



ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	NVVDD Power Supply

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	13 OF 15
NAME	hlu	DATE	15-MAY-2008

PAGE 14) FBVDDQ AND PEX1V2 POWER SUPPLY

NET	VOLTAGE	MIN_WIDTH_LINE	NV_NET_MAX_CURRENT
PEX_VDD	1.2V	12MIL	3.48A
FBVDDQ	1.8V	12MIL	10A
PS_VIN_PEX		12MIL	

FBVDDQ=1.8V
APPROX. 5A @ 400KHZ
INPUT CURRENT RMS = 2.15A @ 7.5V INPUT
OUTPUT PEAK TO PEAK CURRENT = 1.51A @ 22V INPUT
SWITCHING FREQ = 500KHZ

300-0309-000 can be the alternative

CONNECT TO R-TOP

place close to the inductor

Vout = Vref * (1 + Rtop / Rbot)
1.805V = 0.6V * (1 + 3.09K/(1.96K||7.15K))
1.546V = 0.6V * (1 + 3.09K/1.96K)

PEXVDD = 1.1V @ 4A
Vout = Vref * (1+R1/R2)
1.10V = 0.8V * (1+324K/866K)

STUFF FOR G10x

STUFF FOR G9x (NO DYNAMIC FBVDDQ)

STUFF REGULATOR FOR G9x (WITH DYNAMIC FBVDDQ)

stuff for NCP5212

ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	FBVDDQ, PEX1V2 and IPF_VDD Power Supply

NVIDIA CORPORATION
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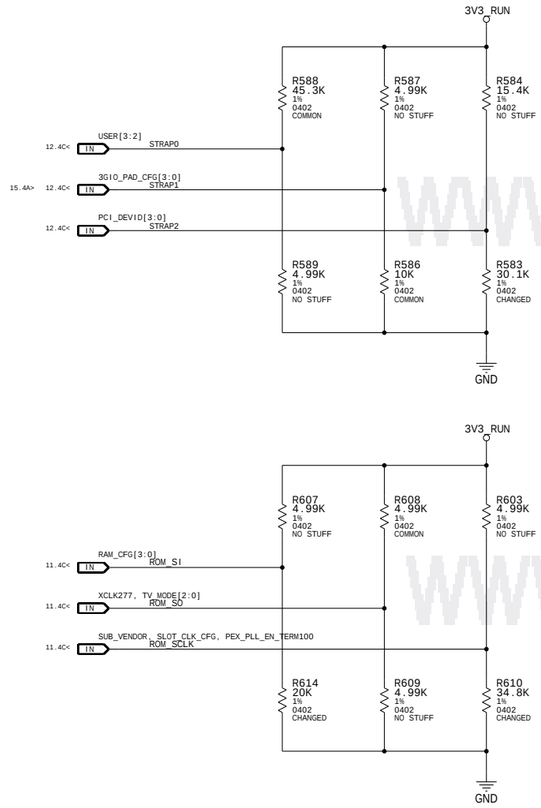
SANTA CLARA, CA 95050, USA

NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	14 OF 15
NAME	hlu	DATE	15-MAY-2008

PAGE 15) STRAPS, MOUNTING HOLES



	3V3	GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

STRAP0

USER_BIT0	0xF: 45K PU (unused)
USER_BIT1	
USER_BIT2	
USER_BIT3	

STRAP1

3GIO_PADCFG_LUT_ADR0	
3GIO_PADCFG_LUT_ADR1	0x0: Desktop default (normal swing) - 5k PD
3GIO_PADCFG_LUT_ADR2	0x1: Mobile default (low swing) - 10k PD
3GIO_PADCFG_LUT_ADR3	acc. to //hw/tesla_g98b/manuals/dev_ext_devices.ref

STRAP2

PCI_DEVID_0	all 4 bits set by HW strapping
PCI_DEVID_1	0x064A: 15K PU (NB9E-GE)
PCI_DEVID_2	
PCI_DEVID_3	

ROM_SO

TV_MODE_BIT0	0x0: NTSC-M
TV_MODE_BIT1	5K PU
TV_MODE_BIT2	
XCLK_277	1: PCI-E GEN2

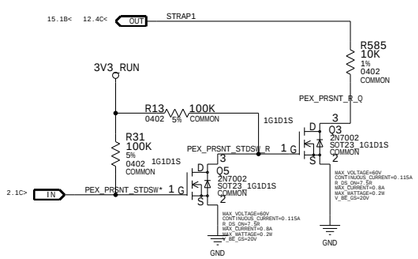
ROM_SI

	256 MB (4pcs. 16Mx32)		512 MB (4pcs. 32Mx32)		
RAM_CFG_0	RAM_CFG[3:0]	Definitions	RAM_CFG[3:0]	Definitions	
RAM_CFG_1	0000	Reserved	0100	25k PD	Reserved
RAM_CFG_2	0001	Qimonda	0101	30k PD	Qimonda
RAM_CFG_3	0010	Hynix	0110	35k PD	Hynix
	0011	Samsung	0111	45k PD	Samsung

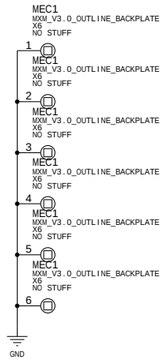
ROM_SCLK (30K PD)

PCI_DEVID_EXT	0:
SUB_VENDOR	1: SUB_VENDOR BIOS
SLOT_CLK_CONFIG	1:
PEX_PLL_EN_TERM100	1: TERM100 ENABLED

PEX_PADCFG



PEX_PRSNT_R*	R_STRAP1	3_GIO_PADCFG_LUT<3..0>
FLOAT	10k	0x1 MOBILE_DEFAULT
GND	5k (10k ll 10k)	0x0 DESKTOP_DEFAULT



ASSEMBLY	P815-D00 SKU3 G96-630 MXM3.0 TYPE-A 256MB 4pcs 16Mx32
PAGE DETAIL	STRAPS, TTP, MOUNTING HOLE

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10815-0003-300 A		
ID	p815_d00	PAGE	15 OF 15
NAME	hlu	DATE	15-MAY-2008