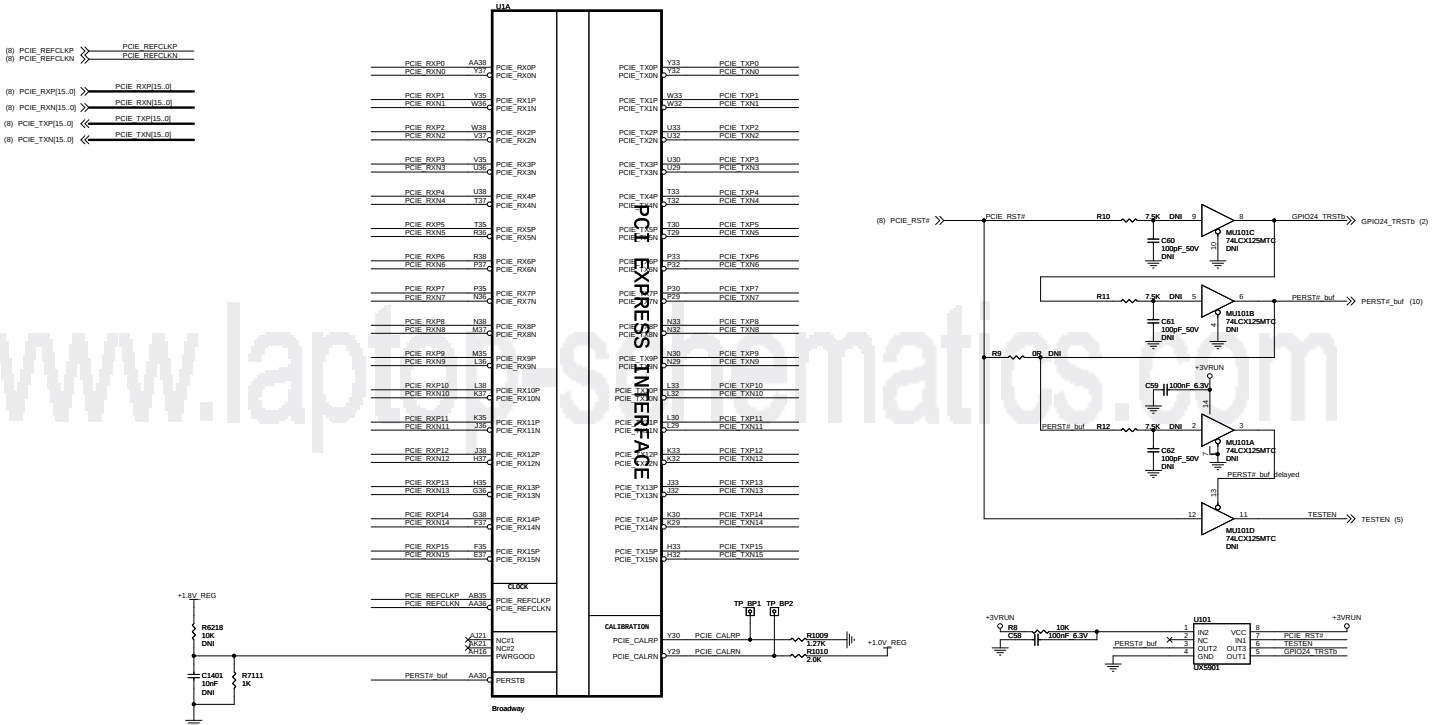

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SERIAL EEPROM 512K/1M

PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

PM25LV010A-100SCE

113-B971XX-XXX VIDEO BIOS FIRMWARE

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

PLACE RGB TERMINATION RESISTORS CLOSE TO ASIC

(DPLL_PVDD: 75mA @ 1.8V)

(DPLL_VDDC: 125mA @ 1.0V)

(TSVDD: 5mA @ 1.8V)

(VDD2DI: 50mA @ 1.8V)

(A2VDD: 130mA @ 3.3V)

(A2VDDQ: 1.5mA @ 1.8V)

DPA

DPB

LVDS

VGA

External thermal sensor

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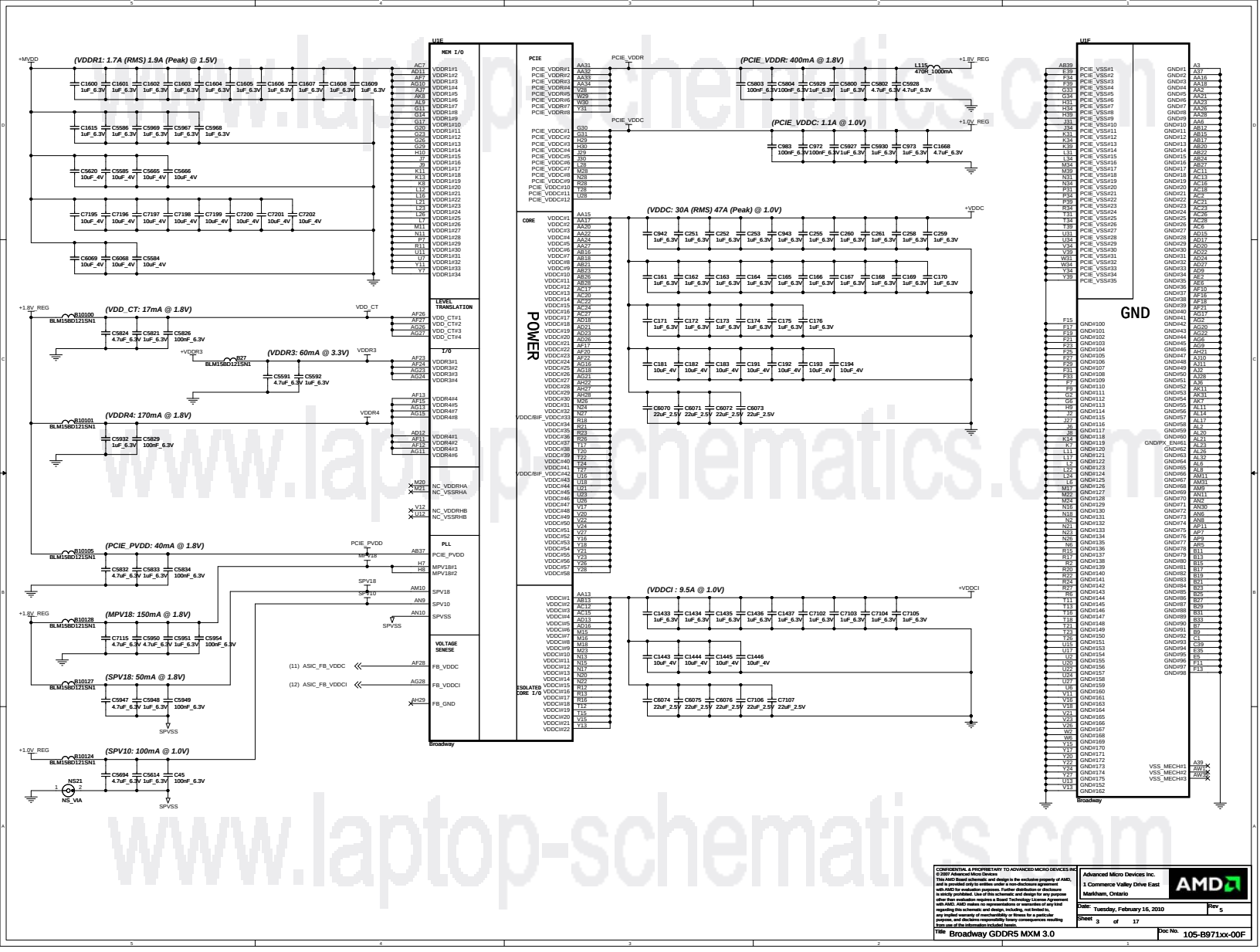
(VDDR1: 1.7A (RMS) 1.9A (Peak) @ 1.5V)
(VDD_CT: 17mA @ 1.8V)
(VDDR3: 60mA @ 3.3V)
(VDDR4: 170mA @ 1.8V)
(PCIE_PVDD: 40mA @ 1.8V)
(MPV18: 150mA @ 1.8V)
(SPV18: 50mA @ 1.8V)
(SPV10: 100mA @ 1.0V)
(PCIE_VDDR: 400mA @ 1.8V)
(PCIE_VDDC: 1.1A @ 1.0V)
(VDDC: 30A (RMS) 47A (Peak) @ 1.0V)
(VDDCI : 9.5A @ 1.0V)
U1E
MEM I/O
PCIE
POWER
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENSE
Broadway
GND
Advanced Micro Devices Inc.
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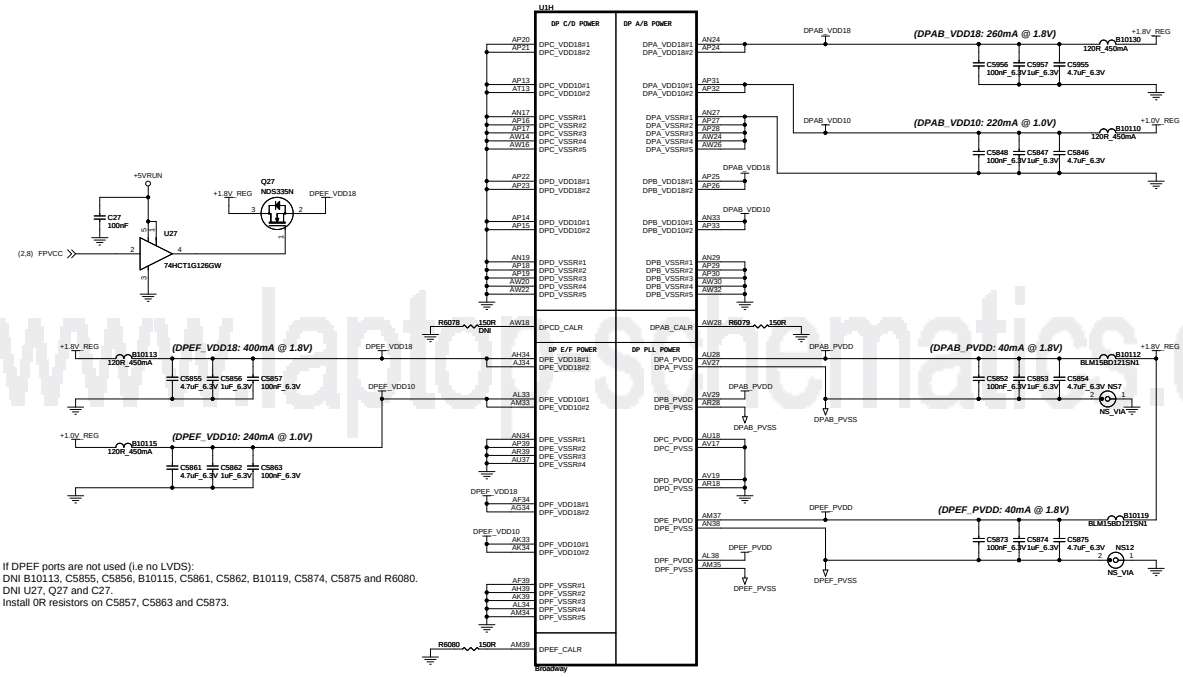
Markham, Ontario
Tuesday, February 16, 2010
Broadway GDDR5 MXM 3.0
105-B971xx-00F



If DPEF ports are not used (i.e no LVDS):
DNI B10113, C5855, C5856, B10115, C5861, C5862, B10119, C5874, C5875 and R6080.
DNI U27, Q27 and C27.
Install 0R resistors on C5857, C5863 and C5873.

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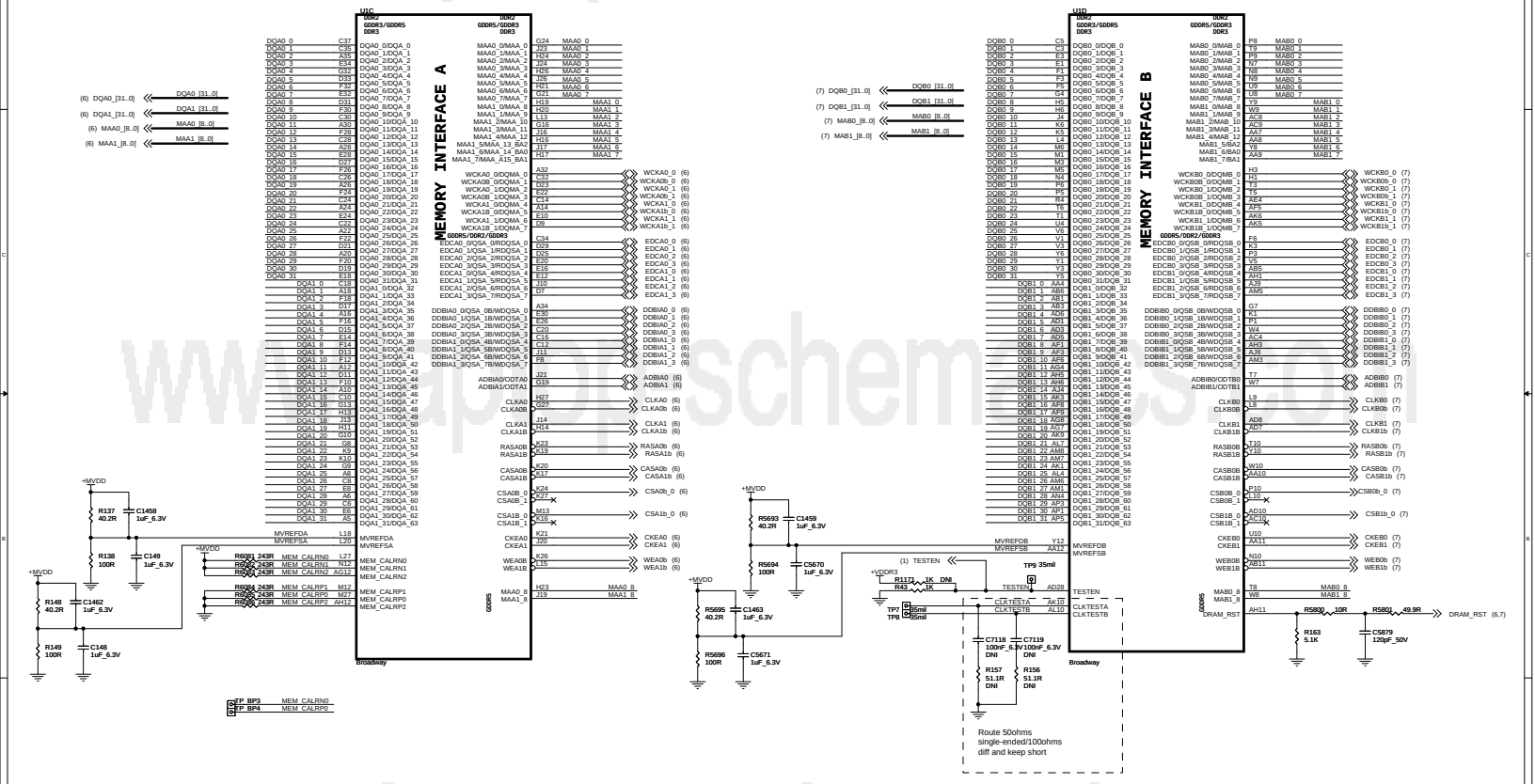

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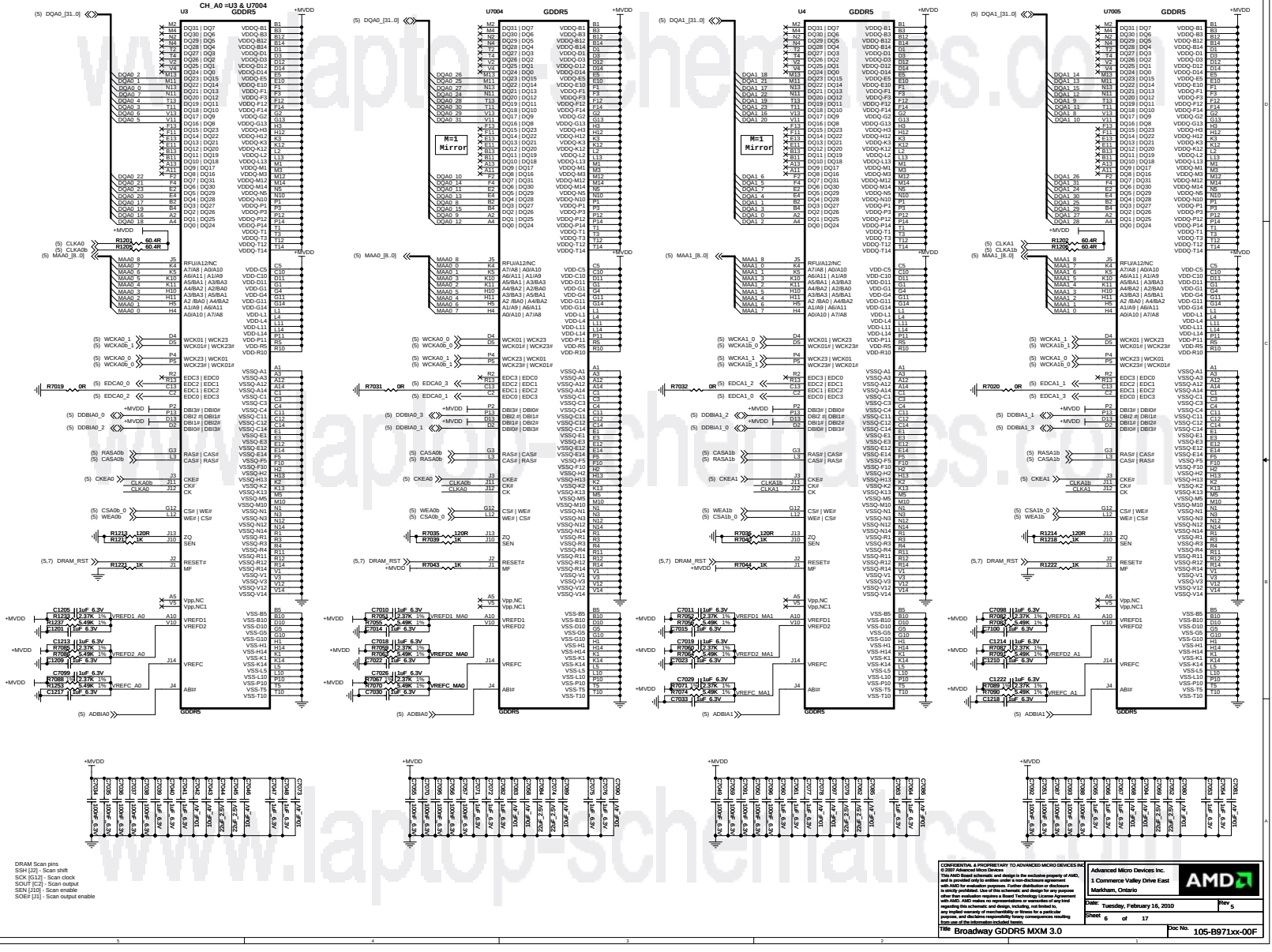
CH_A0 =U3 & U7004
U3
GDDR5
U7004
GDDR5
U4
GDDR5
U7005
GDDR5
M=1 Mirror
M=1 Mirror
+MVDD
(5) DQA0_[31..0]
(5) DQA1_[31..0]
(5) CLKA0
(5) CLKA0b
(5) MAA0_[8..0]
(5) CLKA1
(5) CLKA1b
(5) MAA1_[8..0]
R1201 60.4R
R1202 60.4R
R1205 60.4R
R1206 60.4R
(5) WCKA0_1
(5) WCKA0b_1
(5) WCKA0_0
(5) WCKA0b_0
(5) WCKA1_1
(5) WCKA1b_1
(5) WCKA1_0
(5) WCKA1b_0
WCK01 | WCK23
WCK01# | WCK23#
WCK23 | WCK01
WCK23# | WCK01#
R7019 0R
R7031 0R
R7032 0R
R7020 0R
(5) EDCA0_0
(5) EDCA0_2
(5) EDCA0_3
(5) EDCA0_1
(5) EDCA1_2
(5) EDCA1_0
(5) EDCA1_3
(5) EDCA1_1
EDC3 | EDC0
EDC2 | EDC1
EDC1 | EDC2
EDC0 | EDC3
(5) DDBIA0_0
(5) DDBIA0_2
(5) DDBIA0_3
(5) DDBIA0_1
(5) DDBIA1_2
(5) DDBIA1_0
(5) DDBIA1_1
(5) DDBIA1_3
+MVDD
DBI3# | DBI0#
DBI2 #| DBI1#
DBI1# | DBI2#
DBI0# | DBI3#
(5) RASA0b
(5) CASA0b
(5) CASA0_0
(5) CASA0_1
(5) CASA1_0
(5) CASA1_1
(5) RASA1b
(5) CASA1b
RAS# | CAS#
CAS# | RAS#
(5) CKEA0
(5) CKEA1
CLKA0b
CLKA0
CLKA1b
CLKA1
CKE#
CK#
CK
(5) CSA0b_0
(5) WEA0b
(5) CSA0_0
(5) WEA0_0
(5) WEA1b
(5) CSA1b_0
(5) CSA1_0
(5) WEA1_0
CS# | WE#
WE# | CS#
R1213 120R
R1221 1K
R7035 120R
R7039 1K
R7036 120R
R7040 1K
R1214 120R
R1218 1K
ZQ
SEN
(5,7) DRAM_RST
R1222 1K
R7043 1K
R7044 1K
RESET#
MF
Vpp,NC
Vpp,NC1
C1205 1uF 6.3V
C1201 1uF 6.3V
C7010 1uF 6.3V
C7014 1uF 6.3V
C7011 1uF 6.3V
C7015 1uF 6.3V
C7098 1uF 6.3V
C7100 1uF 6.3V
VREFD1_A0
VREFD1_MA0
VREFD1_MA1
VREFD1_A1
VREFD1
VREFD2
C1213 1uF 6.3V
C1209 1uF 6.3V
C7018 1uF 6.3V
C7022 1uF 6.3V
C7019 1uF 6.3V
C7023 1uF 6.3V
C1214 1uF 6.3V
C1210 1uF 6.3V
R7082 2.37K 1%
R7086 5.49K 1%
R7055 2.37K 1%
R7059 5.49K 1%
R7060 2.37K 1%
R7064 5.49K 1%
R7088 2.37K 1%
R7092 5.49K 1%
VREFD2_A0
VREFD2_MA0
VREFD2_MA1
VREFD2_A1
VREFC
C7099 1uF 6.3V
R7088 2.37K 1%
R1253 5.49K 1%
C1217 1uF 6.3V
C7026 1uF 6.3V
R7067 2.37K 1%
R7070 5.49K 1%
C7030 1uF 6.3V
C7029 1uF 6.3V
R7071 2.37K 1%
R7074 5.49K 1%
C7033 1uF 6.3V
C7090 1uF 6.3V
R7090 2.37K 1%
R7094 5.49K 1%
C1218 1uF 6.3V
VREFC_A0
VREFC_MA0
VREFC_MA1
VREFC_A1
ABI#
(5) ADBIA0
(5) ADBIA1
RFU/A12/NC
A7/A8 | A0/A10
A6/A11 | A1/A9
A5/BA1 | A3/BA3
A4/BA2 | A2/BA0
A3/BA3 | A5/BA1
A2 /BA0 | A4/BA2
A1/A9 | A6/A11
A0/A10 | A7/A8
VDD-C5
VDD-C10
VDD-D11
VDD-G1
VDD-G4
VDD-G11
VDD-G14
VDD-L1
VDD-L4
VDD-L11
VDD-L14
VDD-P11
VDD-R5
VDD-R10
VSSQ-A1
VSSQ-A3
VSSQ-A12
VSSQ-A14
VSSQ-C1
VSSQ-C3
VSSQ-C4
VSSQ-C11
VSSQ-C12
VSSQ-C14
VSSQ-E1
VSSQ-E3
VSSQ-E12
VSSQ-E14
VSSQ-F5
VSSQ-F10
VSSQ-H2
VSSQ-H13
VSSQ-K2
VSSQ-K13
VSSQ-M5
VSSQ-M10
VSSQ-N1
VSSQ-N3
VSSQ-N12
VSSQ-N14
VSSQ-R1
VSSQ-R3
VSSQ-R4
VSSQ-R11
VSSQ-R12
VSSQ-R14
VSSQ-V1
VSSQ-V3
VSSQ-V12
VSSQ-V14
VSS-B5
VSS-B10
VSS-D10
VSS-G5
VSS-G10
VSS-H1
VSS-H14
VSS-K1
VSS-K14
VSS-L5
VSS-L10
VSS-P10
VSS-T5
VSS-T10
C7001 C7002 C7003 C7004 C7005 C7006 C7007 C7008 C7009 C7012 C7013 C7016 C7017 C7020 C7021 C7024 C7025 C7027 C7028 C7031 C7032 C7034 C7035 C7036 C7037 C7038 C7039 C7040 C7041 C7042 C7043 C7044 C7045 C7046 C7047 C7048 C7049 C7050 C7051 C7052 C7053 C7054 C7055 C7056 C7057 C7058 C7059 C7060 C7061 C7062 C7063 C7064 C7065 C7066 C7067 C7068 C7069 C7070 C7071 C7072 C7073 C7074 C7075 C7076 C7077 C7078 C7079 C7080 C7081 C7082 C7083 C7084 C7085 C7086 C7087 C7088 C7089 C7091 C7092 C7093 C7094 C7095 C7096 C7097
0.1uF 16V
1uF 6.3V
22uF 25V
47uF 2V
DRAM Scan pins
SSH [J2] - Scan shift
SCK [G12] - Scan clock
SOUT [C2] - Scan output
SEN [J10] - Scan enable
SOE# [J1] - Scan output enable
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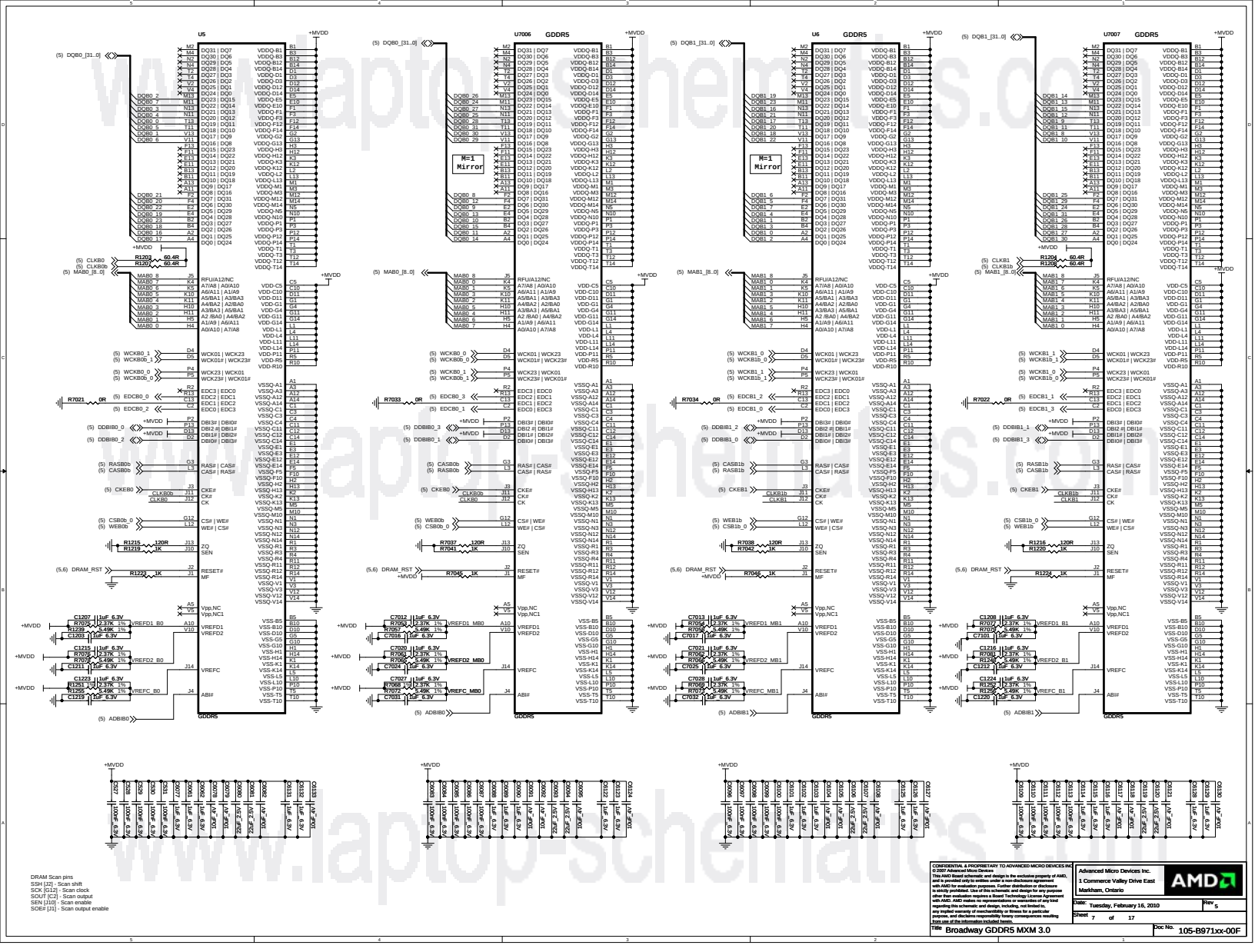

DRAM Scan pins
SSH [J2] - Scan shift
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SEN [J10] - Scan enable
SOE# [J1] - Scan output enable

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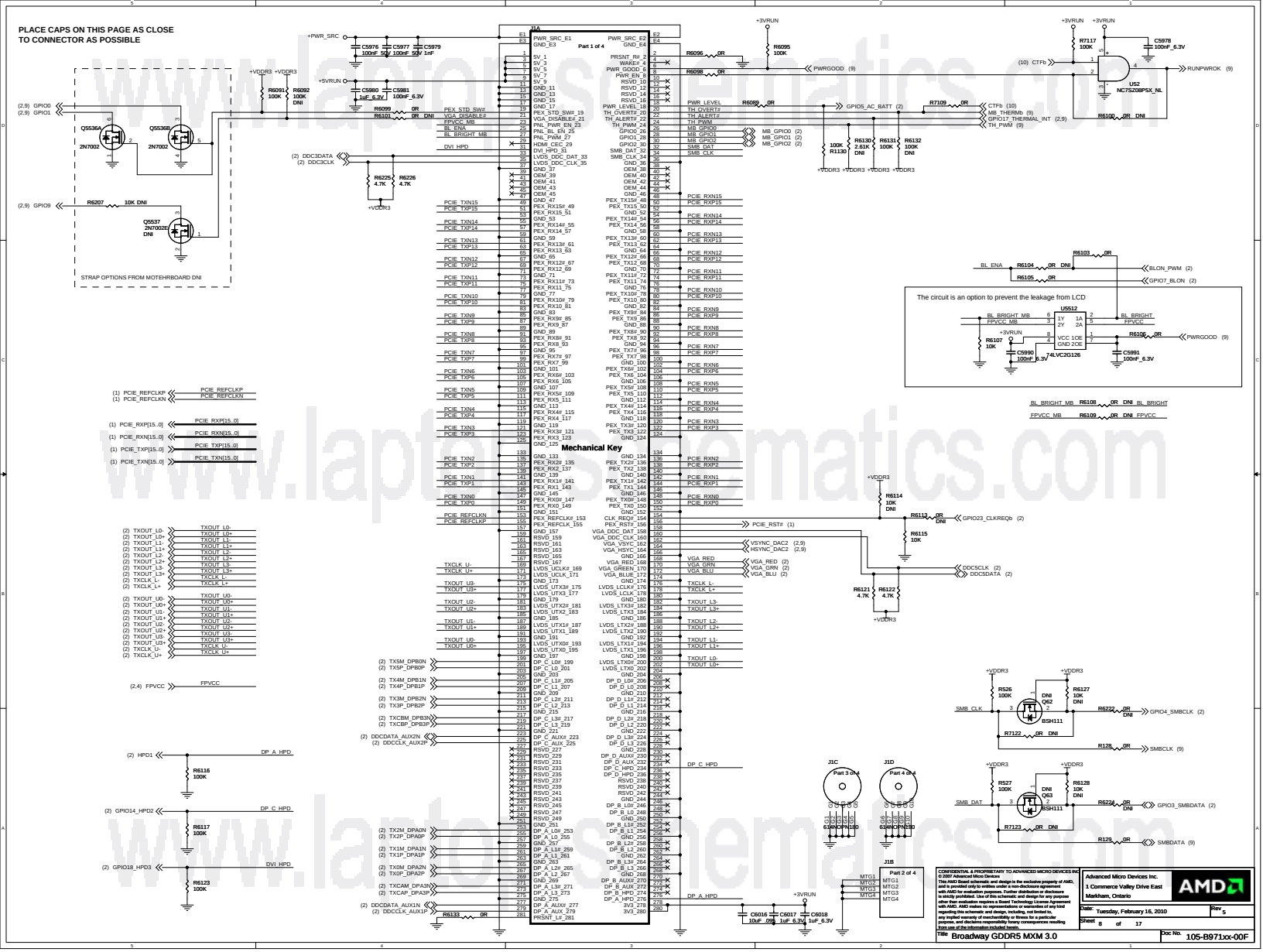
PLACE CAPS ON THIS PAGE AS CLOSE TO CONNECTOR AS POSSIBLE
STRAP OPTIONS FROM MOTHERBOARD DNI
Mechanical Key
The circuit is an option to prevent the leakage from LCD
Part 1 of 4
Part 2 of 4
Part 3 of 4
Part 4 of 4
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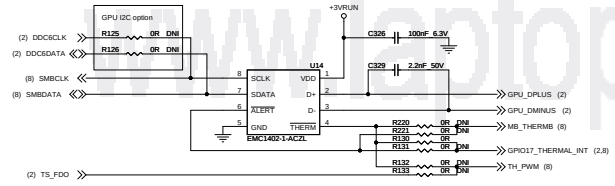
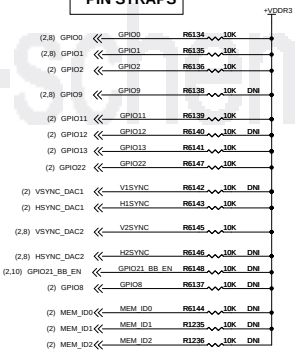
EXTERNAL THERMAL SENSOR



PIN STRAPS



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

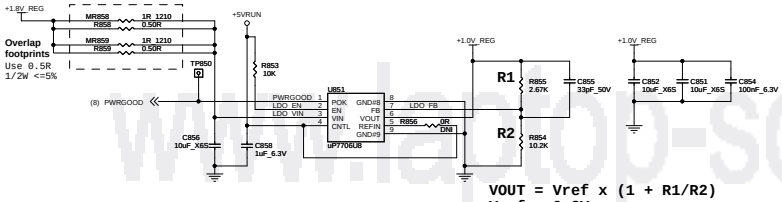
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE Gen2 Enable 0: Advertises the PCIE device as 2.5GT/s capable at power-on 1: Advertises the PCIE device as 5.0GT/s capable at power-on	1
BIF_VGA DIS	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	101
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	1
AUD[1] AUD[0]	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	10
VIP_DEVICE_STRAP_DIS	V2SYNC	VIP Device Strap Enable 0: Slave VIP host port devices present 1: No slave VIP host port devices reporting presence	0
SMS_EN_HARD GPIO21_BB_EN BIF_CLK_PM_EN	H2SYNC GPIO21_BBEN GPIO8	Reserved Reserved Reserved	0
MEM_ID2 MEM_ID1 MEM_ID0	GENERICC GENERICB GENERICA	Optional memory ID straps	XXX

GPIO0 and GPIO1 pulls ups need to be stuffed with Q5536 if system board is to control the PCIE swing

GPIO9 pull up needs to be stuffed with Q5537 if system board is to control the VGA capacity

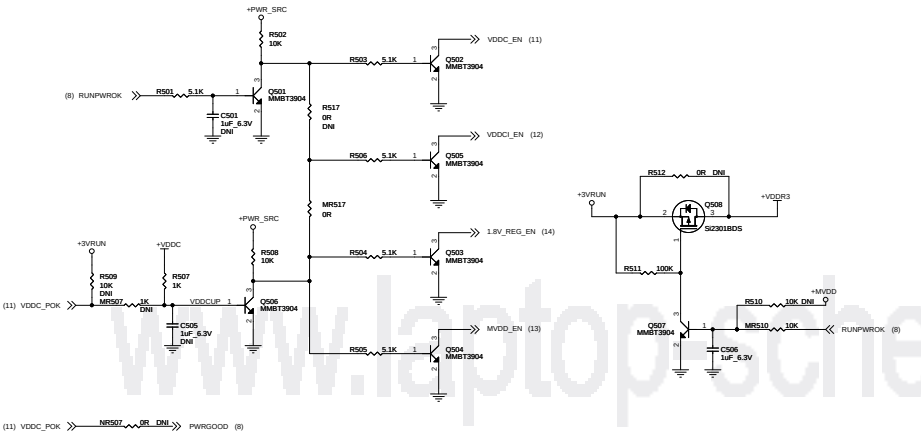
LDO Vin = +1.8V +/-5% Vout = +1.0V +/-2% Iout = 1.7A RMS MAX

PCB: 50 to 70mm sq. copper area for cooling

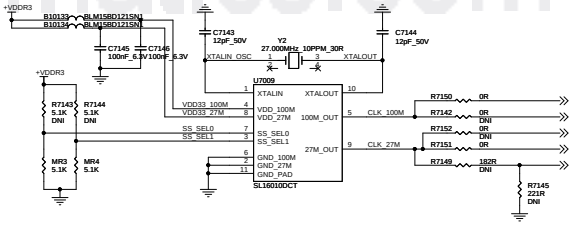


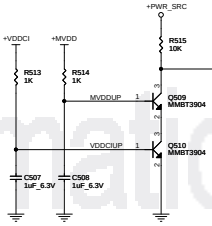
VOUT = Vref x (1 + R1/R2)
Vref = 0.8V

POWER UP SEQUENCE



CLOCK





PCB1
PCB
109-B97157-00

ASSY2
ANTISTATIC BAG
6_X_8

ASSY1
BLANK LABEL
1.50W_X_0.50H

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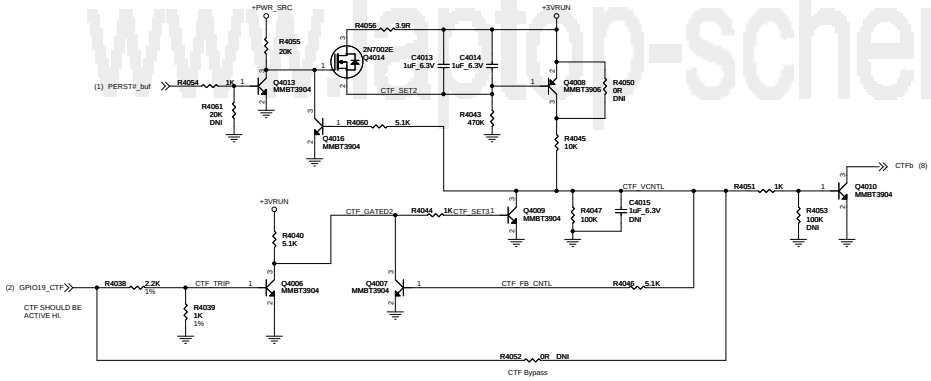
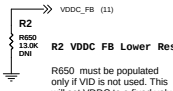
CRITICAL TEMPERATURE FAULT



POWER PLAY

GPIO20	GPIO6	VDDC
0	0	1.05V
0	1	1.00V
1	0	0.90V
1	1	0.85V

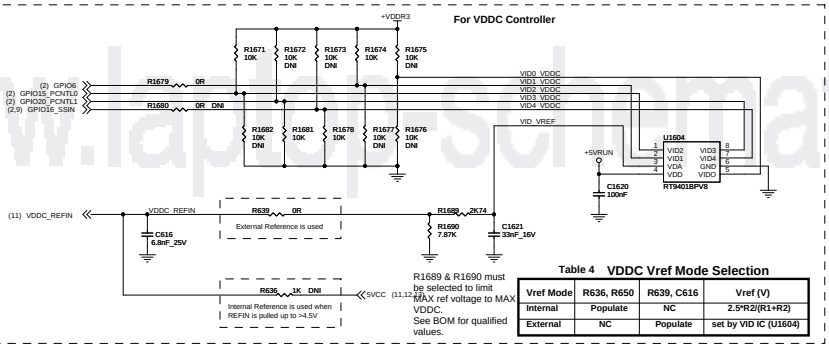


R2 VDDC FB Lower Resistor

R650 must be populated only if VID is not used. This will set VDDC to a fixed value

Vout = Vref * (1+Rt/Rb)
Dual: Vref = 0.6V, Rt = 10k
Single: Vref = 0.8V, Rt = 10k

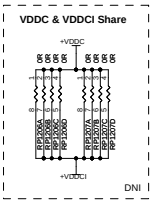
For VDDC Controller



R1689 & R1690 must be selected to limit MAX ref voltage to MAX VDDC.
See BOM for qualified values.

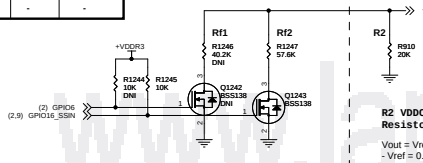
Table 4 VDDC Vref Mode Selection

Vref Mode	R636, R650	R639, C616	Vref (V)
Internal	Populate	NC	2.5*R2/(R1+R2)
External	NC	Populate	set by VID IC (U1604)



GPIO6	GPIO16	VDDCI
-	0	0.90V
-	1	1.00V
-	-	-
-	-	-

For VDDCI Controller



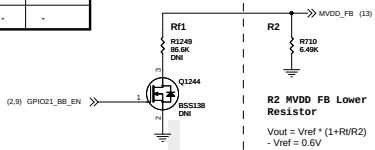
R2 VDDCI FB Lower Resistor

Vout = Vref * (1+Rt/R2)
- Vref = 0.6V
- Rt = 10k

Vout = Vref * (1+Rt/Rb)
- Vref = 0.8V
- Rt = 10k
- Rb = R2 // Rf1// Rf2

GPIO21	MVDD
-	1.5V
-	-

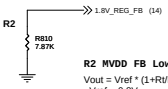
For MVDD Controller



R2 MVDD FB Lower Resistor

Vout = Vref * (1+Rt/R2)
- Vref = 0.6V
- Rt = 10k

Vout = Vref * (1+Rt/Rb)
- Vref = 0.8V
- Rt = 10k
- Rb = R2 // Rf1



R2 MVDD FB Lower Resistor

Vout = Vref * (1+Rt/R2)
- Vref = 0.8V
- Rt = 10k

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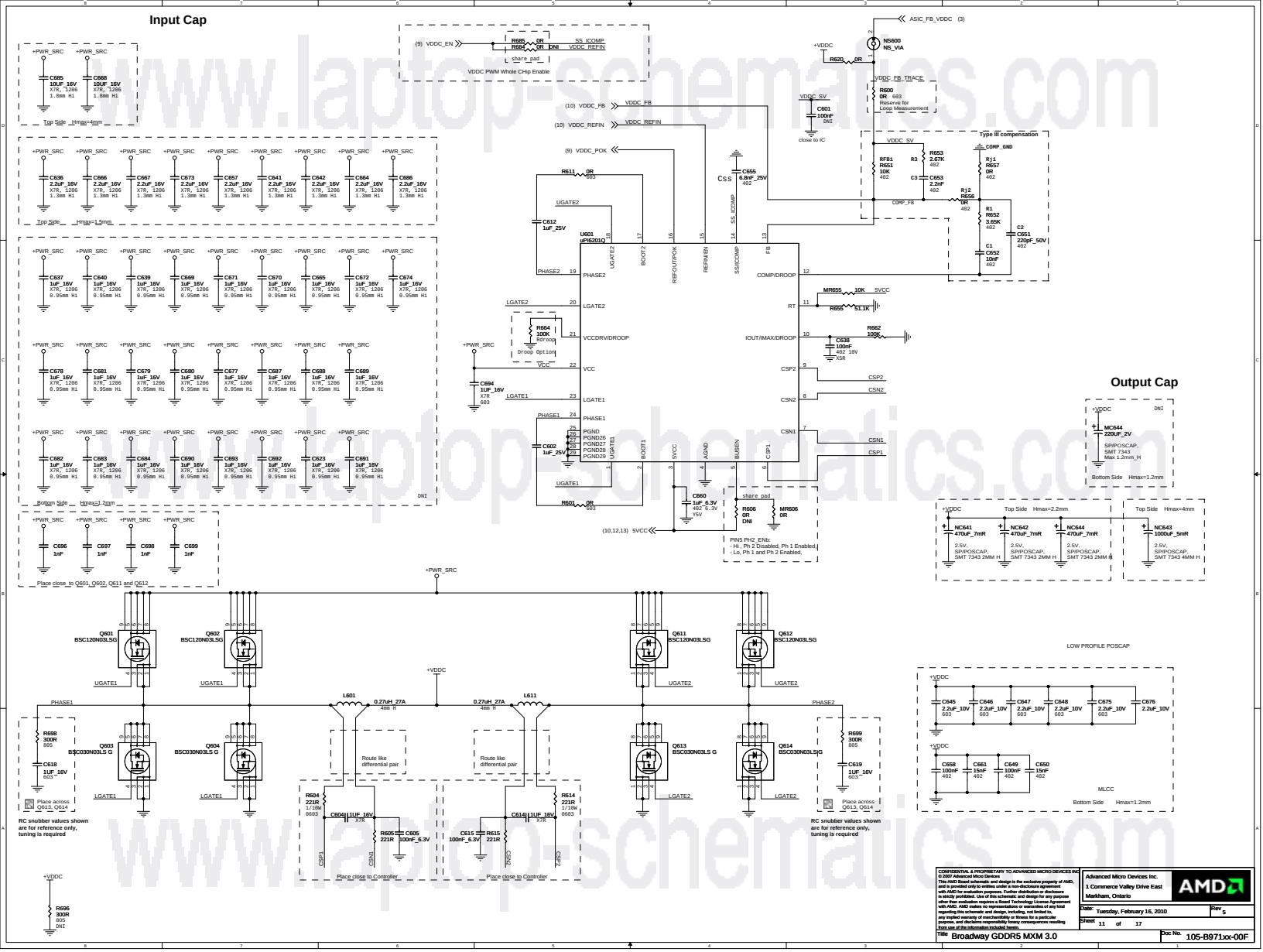
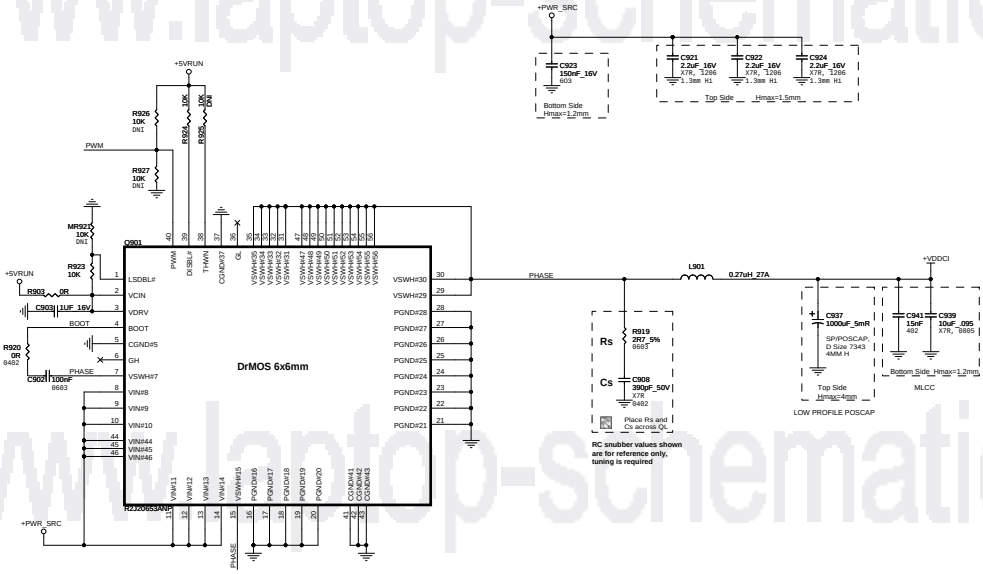
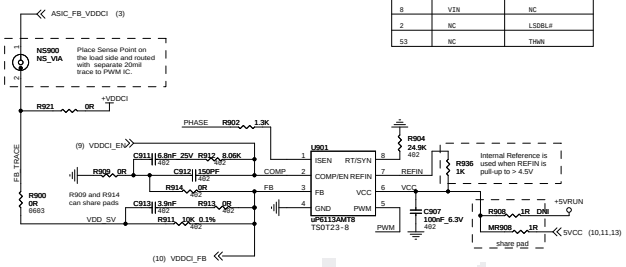




Pin Difference Between R2J2062NP and R2J2065NP		
	R2J2062NP	R2J2065NP
3	VLDRV	NC
8	VIN	NC
2	NC	LSDBL#
53	NC	THWN



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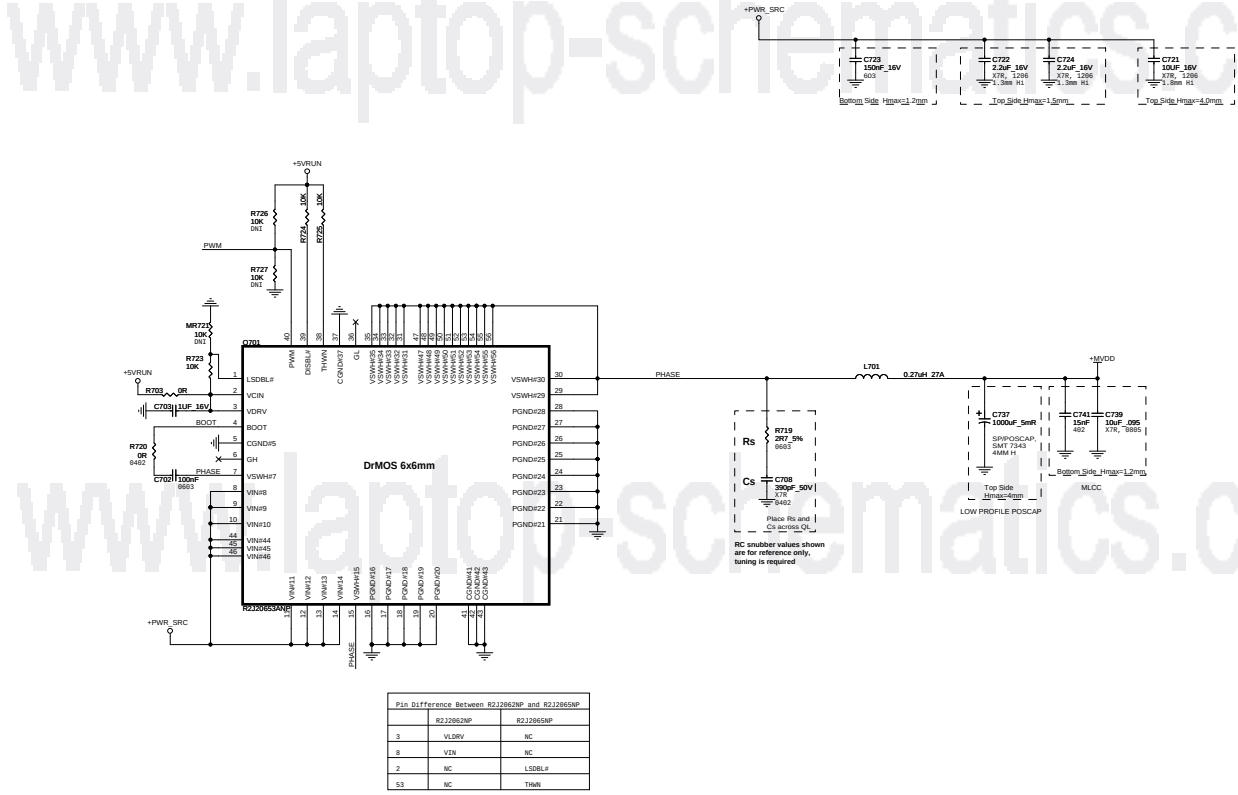
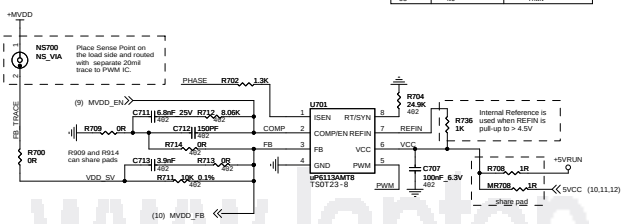


Pin Difference Between R2J2062NP and R2J20865NP

	R2J20662NP	R2J20865NP
3	VLDRV	NC
8	VIN	NC
2	NC	LSDBL#
53	NC	THWN



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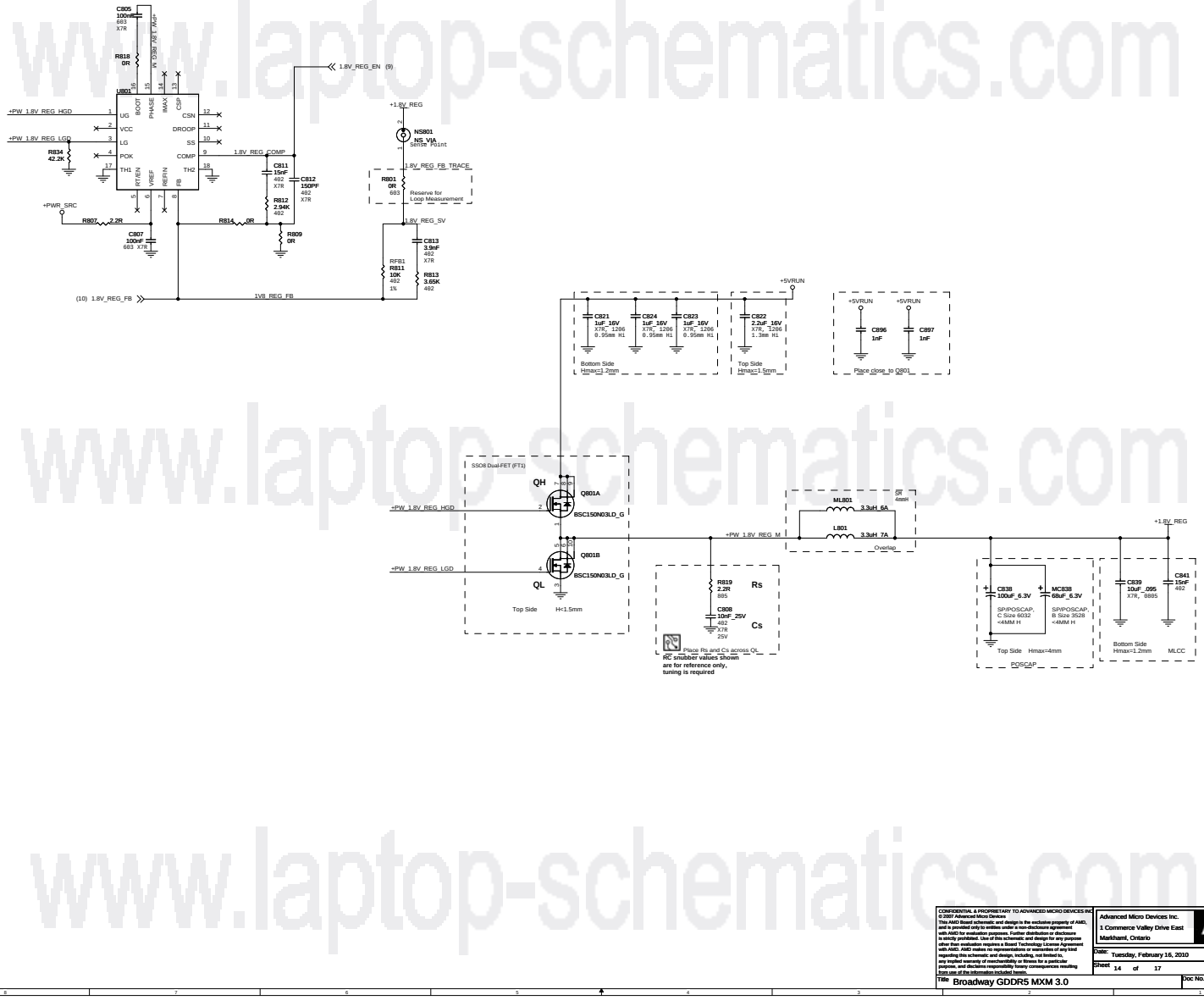

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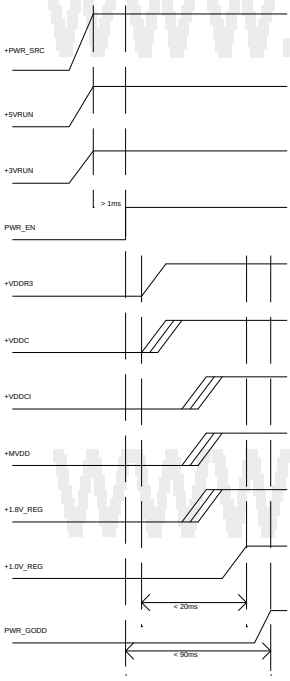
POWER UP SEQUENCE (not to scale)



VDDR3, A2VDD

VDDC

VDDCI

VDDR1, MVDDQ/C

VDDR4, VDD_CT, TSVDD, PCIE_VDDR, PCIE_PVDD, DPLL_PVDD, DPx_PVDD, DPx_VDD18, MPV18, SPV18, AVDD, VDD1DI, A2VDDQ, VDD2DI

PCIE_VDDC, DPLL_VDDC, DPx_VDD10, SPV10

+VDDR3 should ramp before or simultaneously with +VDDC.
+VDDC should ramp before or simultaneously with +VDDCI.
+VDDCI should ramp before or simultaneously with +MVDD.
+VDDC should ramp before +1.8V_REG. +VDDC and +1.8V_REG should not ramp-up simultaneously.
For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18.
The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and +1.8V_REG have ramped up.

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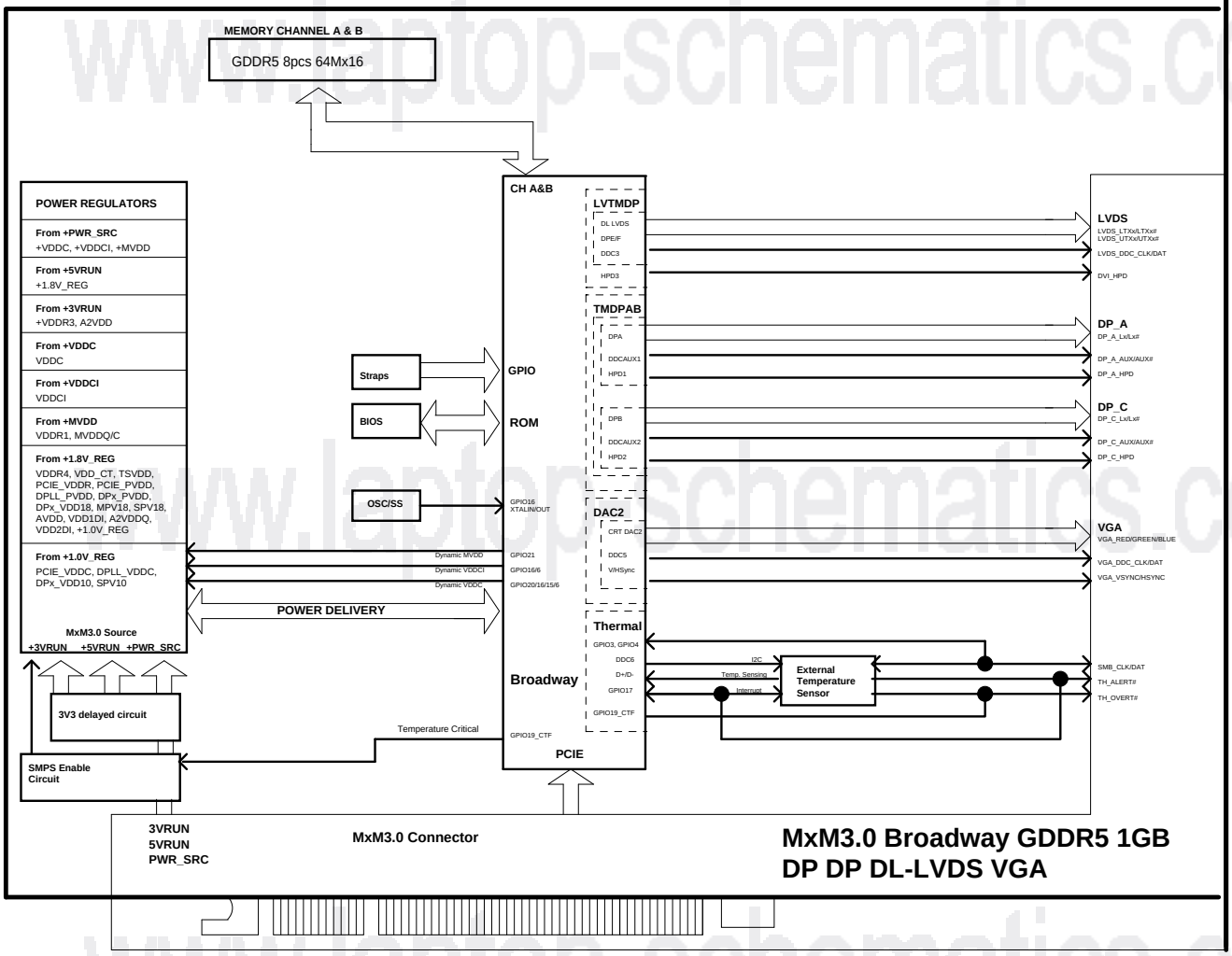

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Title	Schematic No.	Date:
Broadway GDDR5 MXM 3.0	105-B971xx-00F	Monday, February 22, 2010

REVISION HISTORY

NOTE: **This schematic represents the PCB, it does not represent any specific SKU.**
For Stuffing options (component values, DNI's, ...) please consult the product specific BOM.
Please contact AMD representative to obtain latest BOM closest to the application desired.

Rev 5

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	09/05/28	Initial design for Broadway GDDR5 MxM3.0
1	00B	09/05/29	Add U27, Q27, C27 - Gating circuit to delay DPE/F_VDD18; Add RP1206, RP1207 - For VDDC and VDDCI sharing Add R1681, R1682 - Pull downs for VID circuits Add R1, MR1, R2, R7152 Add R5801
2	00C	09/10/30	Add C696, C697, C698, C699, C896, C897 (0402 input caps for power supplies) Change J1 symbol (includes non-plated tooling holes) Add TP_BP1, TP_BP2, TP_BP3, TP_BP4 (Bead test points) Move JTAG TPs out of the back plate area Increase TP coverage
3	00D	09/12/10	Add U101, MU101, R8~R12, C58~C62, R3 (JTAG workaround) Pull back power planes
4	00E	10/01/04	Increase spacing between C7042 & C7043 and C5976 & C5977
5	00F	10/02/16	Increase spacing between C6076&C7106&C6075, R1237&R1233&C1205&C1201 and C5706&Q27. Move C5861&C5784 further away from the heatsink backplate area.