1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2011-02-08

K60 MLB

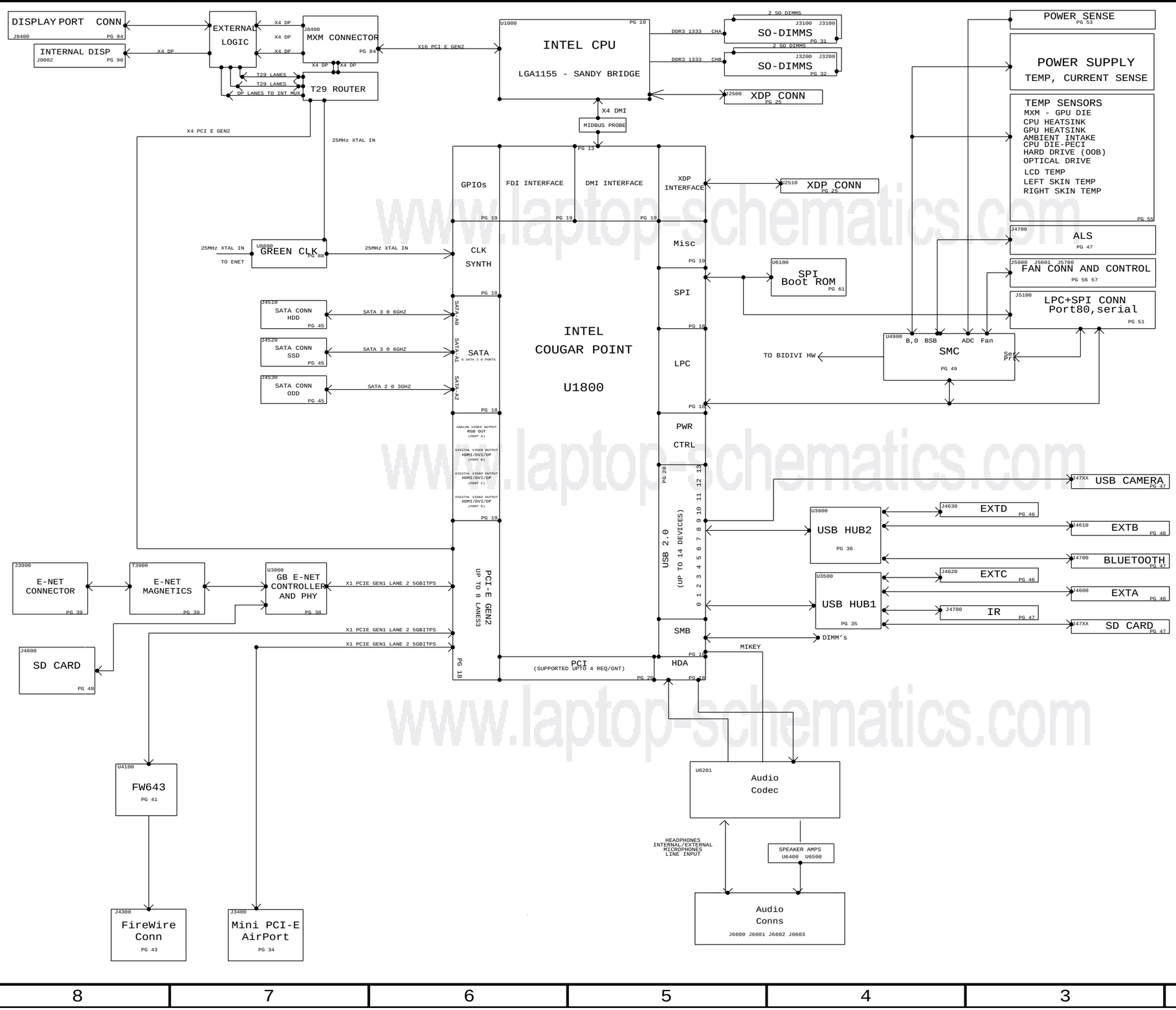
LAST_MODIFIED=Tue Feb 8 14:39:56 2011

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST MODIFIED=Tue Feb 8 14 39 56 2011

DRAWING TITLE: SCH,K60,MLB

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 1 OF 110
SHEET: 1 OF 98



SYNC MASTER=K60 SIJI SYNC DATE=01/06/2011

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

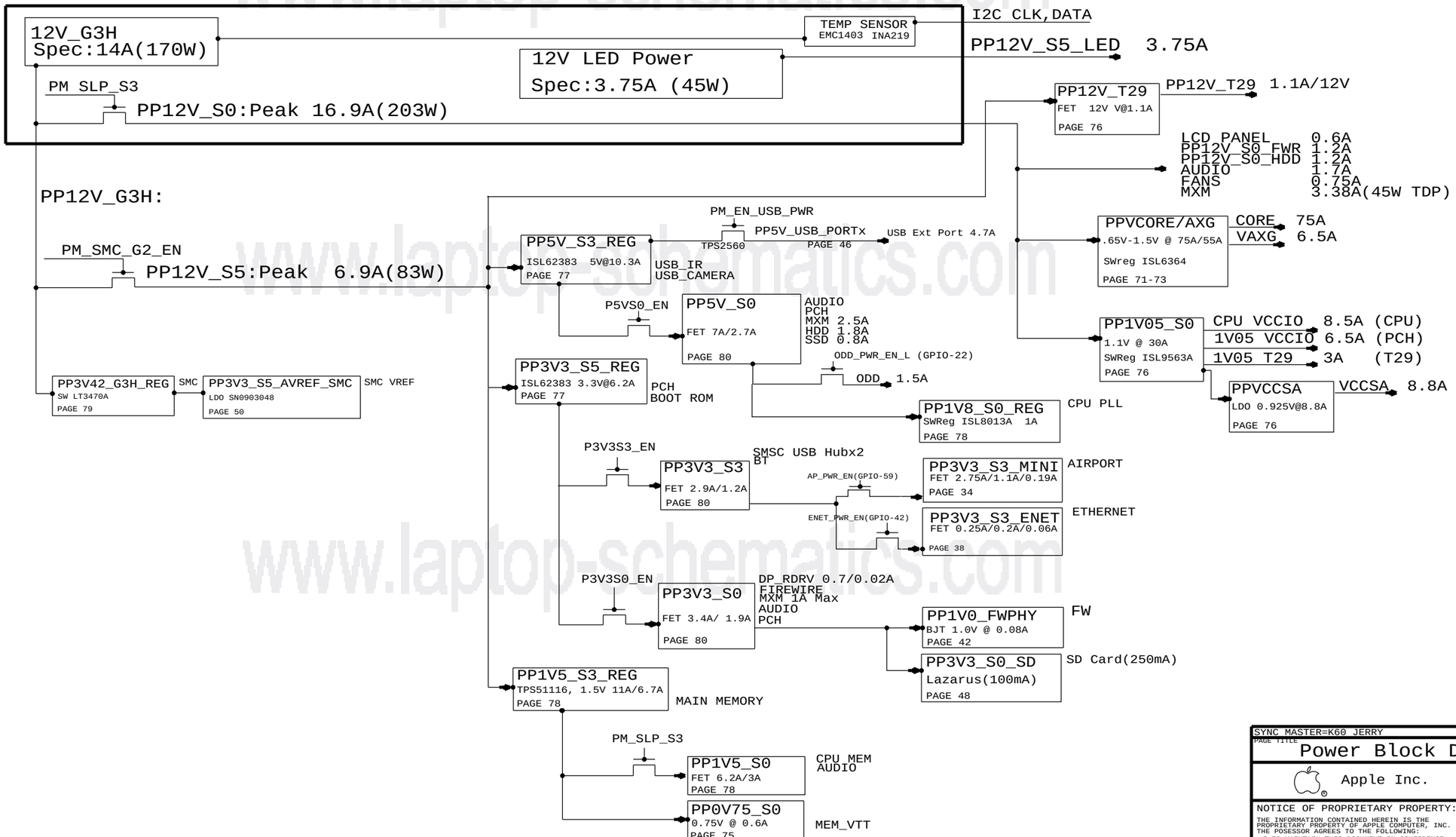
REVISION 11.1.0

BRANCH

PAGE 2 OF 110

SHEET 2 OF 98

AC/DC POWER SUPPLY (Spec:215W)



SYNC_MASTER=K60_JERRY SYNC_DATE=01/06/2011

PAGE TITLE

Power Block Diagram

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

BRANCH

PAGE 3 OF 110

SHEET 3 OF 98

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-0801	PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD	DEVELOPMENT,DEV_GROUP
639-1767	PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-1820	PCBA,MLB,K60,2.7G,4C,PRQ,P2_ODD	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-1821	PCBA,MLB,K60,2.8G,4C,PRQ,P2_ODD	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-2160	PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD,NO_DBG	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2159	PCBA,MLB,K60,2.7G,4C,PRQ,P2_ODD,NO_DBG	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2161	PCBA,MLB,K60,2.8G,4C,PRQ,P2_ODD,NO_DBG	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2118	PCBA,MLB,K60,2.5G,4C,PRQ,P1_ODD	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2122	PCBA,MLB,K60,2.7G,4C,PRQ,P1_ODD	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2119	PCBA,MLB,K60,2.8G,4C,PRQ,P1_ODD	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2132	PCBA,MLB,K60,2.5G,4C,PRQ,P1_ODD,NO_DBG	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG
639-2133	PCBA,MLB,K60,2.7G,4C,PRQ,P1_ODD,NO_DBG	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG
639-2134	PCBA,MLB,K60,2.8G,4C,PRQ,P1_ODD,NO_DBG	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC1	COMMON,ALTERNATE,MXM,FCIM,CPU_1V5_SENSE,CPU_VCCSA_SENSE,1V05_PCH_SENSE,HUB_USX2061,PRODUCTION,VAXG,SSD
BASIC2	AP,BT,IR,T29
DEV_GROUP	VREFMRGN_A,VREFMRGN_B,DIMM_1V5_SENSE
YES_DBG	XDP,XDP_CONN,XDP_CPU_BPM,MOJOMUX:YES,LPCPLUS:YES
NO_DBG	MOJOMUX:NO,LPCPLUS:NO

CPU SOCKET & ILM SUB-BOMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0071	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	TYCO_SOCKET
604-1474	1	ASSY,PURCHASED,ILM,TYCO	ILM	CRITICAL	TYCO_SOCKET
511S0073	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	MOLEX_SOCKET
604-1161	1	ASSY,PURCHASED,ILM,MOLEX	ILM	CRITICAL	MOLEX_SOCKET

BOM NUMBER	BOM NAME	BOM OPTIONS
085-2452	SUB ASSY,CPU SOCKET,K60,TYCO	TYCO_SOCKET
085-2453	SUB ASSY,CPU SOCKET,K60,MOLEX	MOLEX_SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
085-2452	1	TYCO CPU SOCKET AND ILM	SKT_ILM	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
085-2453	085-2452		SKT_ILM	MOLEX ALTERNATE

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	337S4088	1	IC COUGAR POINT SLJ4F BD82Z68 PRQ B3	U1800	CRITICAL	
	353S3055	1	IC PI3VEDP212 X2 DP MUX QFN	U9390	CRITICAL	
	338S0753	1	IC,FW643,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
	825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
	343S0534	1	IC,BCM57765,ENET&SD,8X8	U3900	CRITICAL	
RAW: 335S0807	341T0184	1	FLASH,EFI BOOTROM,K60/K62	U6100	CRITICAL	
RAW: 335S0539	341T0328	1	SFLASH ENET 2MBIT,CIV	U3990	CRITICAL	
	338S0945	1	T29 ROUTER, IC ASSP	U9700	CRITICAL	T29
RAW: 335S0550	341T0257	1	IC,T29,SERIAL EEPROM	U9790	CRITICAL	T29
RAW: 337S3997	341T0326	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29
RAW: 335S0709	341T0330	1	IC,MXM SYS ROM,24C02	U8570	CRITICAL	
RAW: 338S0878	341T0185	1	IC,SMC,K60	U4900	CRITICAL	K60

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4043	1	SNB SR00S PRQ D2 2 5 65W 4+1 6M LGA	CPU	CRITICAL	2P5GHZ_SNB_CPU_PRQ
337S4062	1	SNB SR009 PRQ D2 2 7 65W 4+1 6M LGA	CPU	CRITICAL	2P7GHZ_SNB_CPU_PRQ
337S4061	1	SNB SR00E PRQ D2 2 8 65W 4+1 8M LGA	CPU	CRITICAL	2P8GHZ_SNB_CPU_PRQ

K60 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8115	1	SCH,MLB,K60	SCH1		K60
820-2641	1	PCBF,MLB,K60	MLB1		K60

K60 ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0298	128S0293			330UF
371S0679	371S0652			PIN DIODE
377S0107	377S0066			USB DIODE
376S0972	376S0612			ROHM TRA-BJT

SYNC MASTER=K60 AARON SYNC DATE=N/A

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

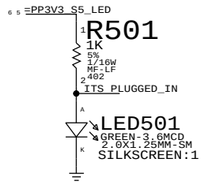
REVISION: 11.1.0

BRANCH:

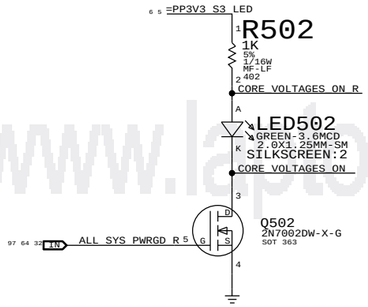
PAGE: 4 OF 110

SHEET: 4 OF 98

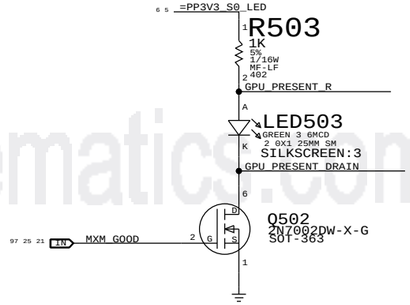
S5 Led



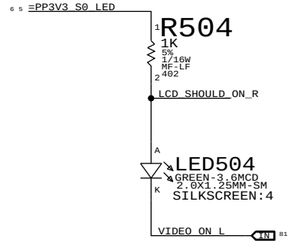
ALL_SYS_PWRGD Led



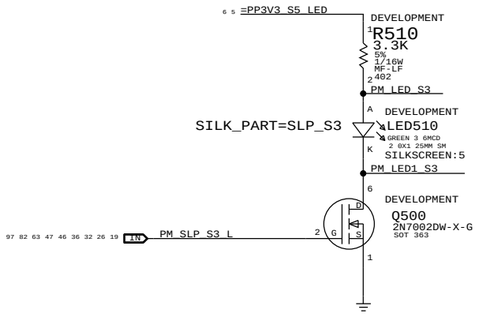
MXM PWR GOOD Led

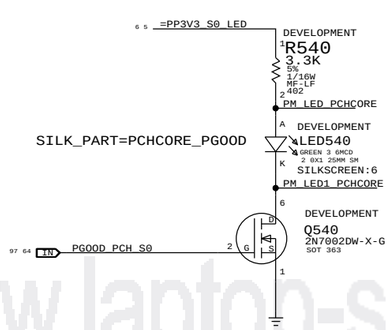


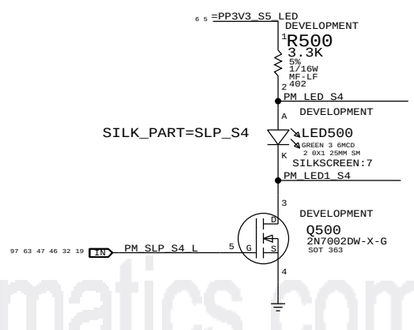
VIDEO ON Led

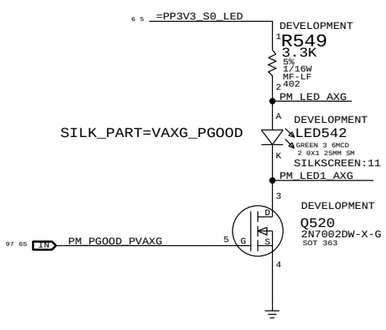


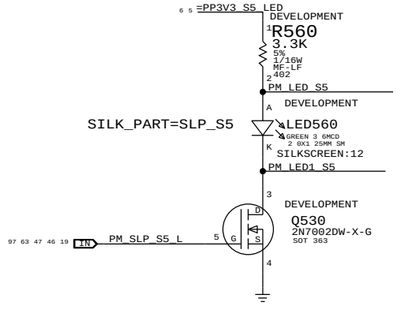
PROTO DEBUG LEDS ARE SHOWN BELOW

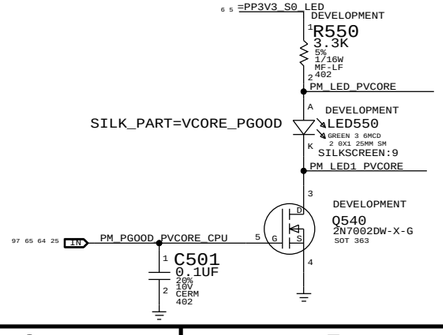


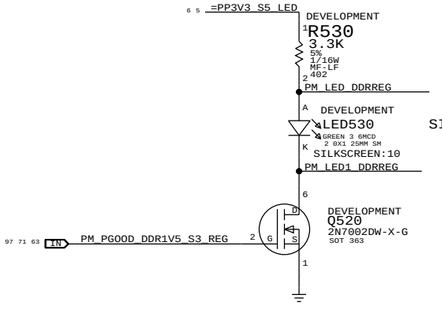


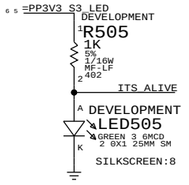












SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: DEBUG LEDS

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 5 OF 110

SHEET: 5 OF 98

POWER SUPPLY TO MLB

J600
76833-0106
M-RT-TH

518-0373

PP12V_G3H_ACDC 6
PP12V_S0_PS 6

C611 1UF 10% 25V X5R 603-1
PLACE C611 CLOSE TO CONNECTOR

C610 1UF 10% 25V X5R 603-1
PLACE C610 CLOSE TO CONNECTOR

MLB TO BLC

94 81 49 BI SMB_BLC_TCON_SDA
94 81 49 IN SMB_BLC_TCON_SCL

R630 0 1/16W 402 5%
R631 0 1/16W 402 5%
SMB_BLC_TCON_SDA_R
SMB_BLC_TCON_SCL_R

NOSTUFF C627 47PF 5% 50V CERM 402
NOSTUFF C628 47PF 5% 50V CERM 402

49 6 =PP3V3_S0_SMBUS

FET DIODE IS S TO D (FACES BLC WHICH 3V3 RISES BEFORE MLB 3V3).

NOSTUFF C621 47PF 5% 50V CERM 402
Q600 2N7002DW-X-G SOT-363

49 BI =SMB_BLC_PCH_SDA
49 IN =SMB_BLC_PCH_SCL

NOSTUFF R618 0 1/16W 402 5%
NOSTUFF R617 0 1/16W 402 5%
SMB_BLC_PCH_SDA_R
SMB_BLC_PCH_SCL_R

BLC SDA/SCL ISOLATION CIRCUIT

NOSTUFF C622 47PF 5% 50V CERM 402
Q600 2N7002DW-X-G SOT-363

R622 0 1/16W 402 5%

91 21 19 IN BLC_GPIO
BLC_GPIO_R

L602
FERR-1000-OHM
0402
97 81 IN VSYNC_DP_CONN
VSYNC_DP_CONN_R

CRITICAL
J602
53780-8608
F-RT-SM

518S0543

ISOLATED_GND
R620 0 5% 1/16W MF-LF 402

MLB TO PS

97 63 IN PM_EN_P12V_S0_FET

Q610 2N7002 SOT23-HF1

PLACE C606 CLOSE TO CONNECTOR
C606 0.001UF 10% 50V X7R 402

49 IN =SMB_ACDC_SCL
49 BI =SMB_ACDC_SDA

R602 0 1/16W 402 5%
R601 0 1/16W 402 5%
SMB_ACDC_SCL_RC
SMB_ACDC_SDA_RC

R605 0 1/16W 402 5%
PS_ON
ISOLATED_GND2

97 81 BL_EN
97 83 BL_PWM

C604 47PF 5% 50V CERM 402
C602 47PF 5% 50V CERM 402
C603 0.001UF 10% 50V X7R 402
PLACE C603 CLOSE TO CONNECTOR

CRITICAL
J601
50293-00771-H01
M-ST-SM

518S0813

95 PP0V75_S0
MAKE BASE=TRUE
VOLTAGE=0.75V
MIN LINE WIDTH=0 4 mm
MIN NECK WIDTH=0 2 mm
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PPVTT_S0_DDR_LDO 71
→ =PP0V75_S0_MEM_VTT_S0FET 32

95 PPVTT_S0_DDR
MAKE BASE=TRUE
VOLTAGE=0.75V
MIN LINE WIDTH=0 4 mm
MIN NECK WIDTH=0 2 mm
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PPVTT_S0_DDR_FET 32
→ =PP0V75_S0_MEM_VTT_B 31
→ =PP0V75_S0_MEM_VTT_A 30

95 PPVCORE_S0_CPU
MAKE BASE=TRUE
VOLTAGE=1.1V
MIN LINE WIDTH=0 6MM
MIN NECK WIDTH=0 3MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PPVCORE_S0_CPU_REG 66
→ =PPVCORE_S0_CPU 13 16 50 65

95 PPVAXG_S0
MAKE BASE=TRUE
VOLTAGE=1.05V
MIN LINE WIDTH=0 6MM
MIN NECK WIDTH=0 3MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PPVAXG_S0_REG 67
→ =PPVAXG_S0_CPU 13 17 50 65

95 PP1V05_S0
MAKE BASE=TRUE
VOLTAGE=1.05V
MIN LINE WIDTH=0 5MM
MIN NECK WIDTH=0 25MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP1V05_S0_REG 68
→ =PP1V05_S0_PWR 50
→ =PPVCCIO_S0_XDP 25
→ =PPVCCIO_S0_CPU 10 11 13 16 65
→ =PPVCCIO_S0_SMC 46 47
→ =PP1V05_S0_PCH_PWR 50
→ =PPVCCSA_S0_INPUT_PWR 50 69
→ =PP1V05_S0_CK505 26

95 PP1V05_S0_PCH
MAKE BASE=TRUE
VOLTAGE=1.05V
MIN LINE WIDTH=0 6 mm
MIN NECK WIDTH=0 2 mm
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP1V05_S0_PCH_SNS 50
→ =PP1V05_S0_PCH_VCC_DMI 22 24
→ =PP1V05_S0_PCH_VCCADPLL 17
→ =PP1V05_S0_PCH_VCCIO_DMI 22 24
→ =PP1V05_S0_PCH_VCCIO_SATA 18 22 24
→ =PP1V05_S0_PCH_VCCIO_PCIE 18 19 22 24
→ =PP1V05_S0_PCH_VCC_CORE 22 24
→ =PP1V05_S0_PCH_VCCIO_USB 22 24
→ =PP1V05_S0_PCH 18 24 79
→ =PP1V05_S0_PCH_VCCDIFFCLK 22 24
→ =PP1V05_S0_PCH_VCCSSC 22 24
→ =PP1V05_S0_PCH_V_PROC_IO 22 24
→ =PP1V05_S0_PCH_VCCASW 22 24
→ =PP1V05_S0_P1V05T29FET 80

95 PP1V05_S0_INPUT_VCCSA
MAKE BASE=TRUE
VOLTAGE=1.05V
MIN LINE WIDTH=0 5MM
MIN NECK WIDTH=0 25MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PPVCCSA_S0_INPUT_SNS 50
→ =PPVCCIO_S0_CPU_VCCSA 69

95 PPVCCSA_S0_CPU
MAKE BASE=TRUE
VOLTAGE=0.925V
MIN LINE WIDTH=0 6MM
MIN NECK WIDTH=0 3MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PPVCCSA_S0_FET 69
→ =PPVCCSA_S0_CPU 13 50
→ =PPVCCSA_S0_PWRCTL 64

95 PP1V5_S0
MAKE BASE=TRUE
VOLTAGE=1.5V
MIN LINE WIDTH=0 4MM
MIN NECK WIDTH=0 2MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP1V5_S0_FET 73
→ =PP1V5_S0_AUD_DIG 56
→ =PP1V5_S0_CK505 26
→ =PP1V5_S0_MINI 33
→ =PP1V5_S0_PWR 50
→ =PP1V5_S0_DP 83

95 PP1V5_S0_CPU_MEM
MAKE BASE=TRUE
VOLTAGE=1.5V
MIN LINE WIDTH=0 4MM
MIN NECK WIDTH=0 2MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP1V5_S0_CPU_MEM_SNS 50
→ =PP1V5_S0_CPU_MEM 11 13 16 28 29

95 PP3V3_S0
MAKE BASE=TRUE
VOLTAGE=3.3V
MIN LINE WIDTH=0 4MM
MIN NECK WIDTH=0 2MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP3V3_S0_FET 73
→ =PP3V3_S0_PCH 18 21 24
→ =PP3V3_S0_FAN 53 54
→ =PP3V3_S0_PCH_VCCADAC 17
→ =PPSPD_S0_MEM_A 30 47
→ =PPSPD_S0_MEM_B 31
→ =PP3V3_S0_AUDIO 56 58 59 60 61 62
→ =PP3V3R1V5_S0_PCH_VCCSUSHDA 24
→ =PP3V3_S0_SMBUS 6 49
→ =PP3V3_S0_SMC_LS 47 51
→ =PP3V3_S0_SMBUS_SMC_0 49
→ =PP3V3_S0_SMBUS_SMC_B 49
→ =PP3V3_S0_SMBUS_SMC_MGMT 49
→ =PP3V3_S0_MXM 21 64 75 76
→ =PP3V3_S0_ODD 42
→ =PP3V3_S0_SATALED 18 42
→ =PP3V3_S0_SENSE 50 52
→ =PP3V3_S0_PWRCTL 63 64 73 80
→ =PP3V3_S0_PCH_VCC3_3_GPIO 22 24
→ =PP3V3_S0_FWPHY 39 40 41
→ =PP3V3_S0_DP 81
→ =PP3V3_S0_PCH_VCC3_3_PCI 22 24
→ =PP3V3_S0_CK505 26
→ =PP3V3_S0_PCH_GPIO 20 45
→ =PP3V3_S0_PCH_STRAPS 15
→ =PP3V3_S0_PCH_VCC3_3_SATA 22 24
→ =PP3V3_S0_RSTBUF 11 27
→ =PP3V3_S0_PCH_PM 27
→ =PP3V3_S0_SMBUS_SMC_BSA 49
→ =PP3V3_S0_SDCARD 45
→ =PP3V3_S0_P1V05_VREG 68
→ =PP3V3_S0_PCH_VCC3V3 22 24
→ =PP3V3_S0_VRD 65 68
→ =PP3V3_S0_LED 5
→ =PP3V3_S0_P3V3T29FET 80
→ =PP3V3_S0_DPSDRVA 84
→ =PP3V3_S0_INTDPMUX 83
→ =PP3V3_S0_T29PWRCTL 80
→ =PP3V3_S0_T29I2C 49
→ =PP3V3_S0_ENET_PHY 36 37

"S0" RAILS

ONLY ON IN RUN

95 PP1V8_S0
MAKE BASE=TRUE
VOLTAGE=1.8V
MIN LINE WIDTH=0 5MM
MIN NECK WIDTH=0 25MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP1V8_S0_REG 71
→ =PP3V3R1V8_S0_PCH_VCCDFTERM 22 24
→ =PP1V8R1V5_S0_PCH_VCCVRM 24 79
→ =PP1V8_S0_CPU_PLL 13 16
→ =PP1V8_S0_PCH 19
→ =PP1V8_S0_PWRCTL 64

98 95 PP5V_S0
MAKE BASE=TRUE
VOLTAGE=5V
MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 2 MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP5V_S0_FET 73
→ =PP5V_S0_AUDIO 56
→ =PP5V_S0_SATA 42
→ =PP5V_S0_MXM 75
→ =PP5V_S0_VRD 65 67
→ =PP5V_S0_ISENSE 50
→ =PP5V_S0_PCH 24
→ =PP5V_S0_P1V05_VREG 68
→ =PP5V_S0_LPCPLUS 48
→ =PP5V_S0_P1V8_REG 71

95 PP12V_S0
MAKE BASE=TRUE
VOLTAGE=12V
MIN LINE WIDTH=1mm
MIN NECK WIDTH=0 5mm
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP12V_S0_PS 6
→ =PP12V_S0_AUDIO_SPKRAMP 58 59
→ =PP12V_S0_VRD 65
→ =PP12V_S0_MXM_PWR 50
→ =PP12V_S0_LCD 81
→ =PP12V_S0_P1V05_VREG 68
→ =PP12V_S0_PWRCTL 63 64 80
→ =PP12V_S0_SENSE 51
→ =PP12V_S0_FW 41
→ =PP12V_S0_CPU_VCCSA 69
→ =PP12V_S0_SATA 42
→ =PP12V_S0_FAN 53 54

95 PP12V_S0_MXM
MAKE BASE=TRUE
VOLTAGE=12V
MIN LINE WIDTH=0 6MM
MIN NECK WIDTH=0 2MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP12V_S0_MXM_SNS 50
→ =PP12V_S0_MXM 75

"S3" RAILS

ON IN RUN AND SLEEP

95 PP1V5_S3
MAKE BASE=TRUE
VOLTAGE=1.5V
MIN LINE WIDTH=0 6 mm
MIN NECK WIDTH=0 2 mm
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP1V5_S3_REG 71
→ =PP1V5_S3_MEM_PWR 50
→ =PP1V5_S3_S0FET 73

95 PP1V5_S3_MEM
MAKE BASE=TRUE
VOLTAGE=1.5V
MIN LINE WIDTH=0 6 mm
MIN NECK WIDTH=0 2 mm
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP1V5_S3_MEM_SNS 50
→ =PP1V5_S3_MEMRESET 32
→ =PP1V5_S3_MEM_A 28 29 30
→ =PP1V5_S3_MEM_B 28 29 31

98 95 PP3V3_S3
MAKE BASE=TRUE
VOLTAGE=3.3V
MIN LINE WIDTH=0 4MM
MIN NECK WIDTH=0 2MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP3V3_S3_FET 73
→ =PP3V3_S3_BT 44
→ =PP3V3_S3_SMBUS_SMC_A 49
→ =PP3V3_S3_MINI 33
→ =PP3V3_S3_PWRCTL 64 73 82
→ =PP3V3_S3_MEMRESET 32
→ =PP3V3_S3_USB_HUB 34 35
→ =PP3V3_S3_ENET_PHY 36
→ =PP3V3_S3_SDCARD 44 45
→ =PP3V3_S3_VREFMRGN 28
→ =PP3V3_S3_VRD 71
→ =PP3V3_S3_LED 5
→ =PP3V3_SW_DPAPWR 78
→ =PP3V3_S3_SYSCLK 79
→ =PP3V3_S3_P3V3R2V9_REG_A 82
→ =PP3V3_S3_PCH 21

98 95 PP5V_S3
MAKE BASE=TRUE
VOLTAGE=5V
MIN LINE WIDTH=0 6MM
MIN NECK WIDTH=0 2MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP5V_S3_REG 70
→ =PP5V_S3_USB 43
→ =PP5V_S3_S0FET 73
→ =PP5V_S3_CAMERA 44
→ =PP5V_S3_IR 44
→ =PP5V_S3_MEMRESET 32
→ =PP5V_S3_DDR_VREG 71
→ =PP5V_S3_VREFMRGN 28
→ =PP5V_S3_P3V3R2V9_REG_A 82

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN S5

95 PP3V3_S5
MAKE BASE=TRUE
VOLTAGE=3.3V
MIN LINE WIDTH=0 4MM
MIN NECK WIDTH=0 2MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP3V3_S5_REG 70
→ =PP3V3_S5_PCH 18 19 21 24
→ =PP3V3_S5_PCH_GPIO 20
→ =PP3V3_S5_ROM 48 55
→ =PP3V3_S5_PCH_VCCSUS3_3_USB 22 24
→ =PP3V3_S5_PWRCTL 11 63 64
→ =PP3V3_S5_S3FET 73
→ =PP3V3_S5_S0FET 73
→ =PP3V3_S5_PCH_STRAPS 15
→ =PP3V3_S5_XDP 25
→ =PP3V3_S5_LPCPLUS 48
→ =PP3V3_S5_PCH_VCCDSW 22 24
→ =PP3V3_S5_USB_HUB 34
→ =PP3V3_S5_CPU_VCCSA 69
→ =PP3V3_S5_PCH_VCCSPI 22 24
→ =PP3V3_S5_VRD 70
→ =PP3V3_S5_LED 5
→ =PP3V3_S5_MEMRESET 32
→ =PP3V3_S5_RSTBUF 27
→ =PP3V3_S5_P3V3R2V9_A 82
→ =PP3V3_S5_SMCUSBMUX 43
→ =PP3V3R1V5_S5_PCH_VCCSUSHDA 24

95 PP5V_S5
MAKE BASE=TRUE
VOLTAGE=5V
MIN LINE WIDTH=0 4 MM
MIN NECK WIDTH=0 2 MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP5V_S5_LDO 70
→ =PP5V_S5_PCH 24

95 PP12V_S5
MAKE BASE=TRUE
VOLTAGE=12V
MIN LINE WIDTH=0 6 mm
MIN NECK WIDTH=0 2 mm
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP12V_S5_FET 74 95
→ =PP12V_S5_DDR_VREG 71
→ =PP12V_S5_P5VS3_VREG 70
→ =PP12V_S5_PWRCTL 33 64 73
→ =PP12V_S5_T29_A 82

"G3H" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN G3HOT PER SMC

G3H: ALIASES

95 PP3V42_G3H
MAKE BASE=TRUE
VOLTAGE=3.42V
MIN LINE WIDTH=0 6MM
MIN NECK WIDTH=0 2MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP3V42_G3H_REG 72
→ =PP3V3_G3H_RTC_D 27
→ =PP3V3_G3H_SMC 46 47
→ =PP3V3_G3H_SMCUSBMUX 43
→ =PP3V3_G3H_LPCPLUS 48

95 PP12V_G3H
MAKE BASE=TRUE
VOLTAGE=12V
MIN LINE WIDTH=0 6 mm
MIN NECK WIDTH=0 2 MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP12V_G3H_ACDC 6
→ =PP12V_G3H_S5_FET 74
→ =PP12V_G3H_3V42 72

T29 RAILS

95 PP3V3_S0_T29
MAKE BASE=TRUE
VOLTAGE=3.3V
MIN LINE WIDTH=0 6MM
MIN NECK WIDTH=0 2MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP3V3_T29_FET 80
→ =PP3V3_T29_RTR 79 80 86 87

95 PP1V05_S0_T29
MAKE BASE=TRUE
VOLTAGE=1.05V
MIN LINE WIDTH=0 6MM
MIN NECK WIDTH=0 2MM
NET SPACING TYPE=POWER
MAX NECK LENGTH=3 MM
→ PP1V05_T29_FET 80
→ =PP1V05_T29_RTR 87
→ =PP1V05_T29 80

GND RAILS

GND
MIN LINE WIDTH=0 6MM
MIN NECK WIDTH=0 2MM
VOLTAGE=0V
NET SPACING TYPE=GND
MAKE BASE=TRUE
MAX NECK LENGTH=4 1 MM

SYNC_MASTER=K60_MARK SYNC_DATE=12/30/2010

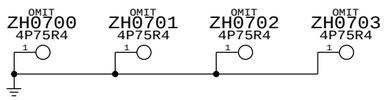
PAGE TITLE
Power Conn / Alias

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 6 OF 110
SHEET 6 OF 98

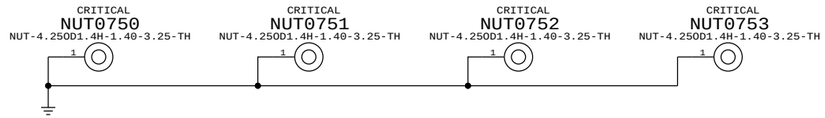
CPU Heatsink

4mm Plated Holes (998-0850)



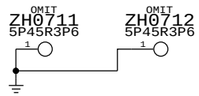
DIMM CONNECTOR NUTS

Nuts (805-9582)



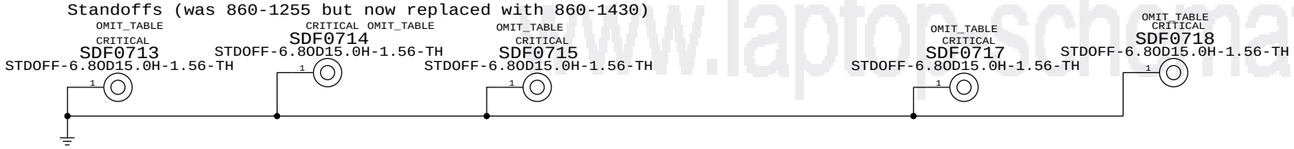
PCH HEATSINK

MOUNTING HOLES (998-0873, 998-0976)



Rear Cover

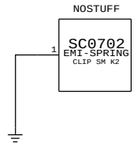
Standoffs (was 860-1255 but now replaced with 860-1430)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-1430	5	STANDOFF,MLB,K60/K62	SDF0713 SDF0714 SDF0715 SDF0717 SDF0718	

For EMC

EMC Spring (870-1577); Near DIMMs



MXM STANDOFFS (835-0272)

SYNC MASTER=K74 MASTER SYNC DATE=N/A

PAGE TITLE: Holes

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 7 OF 110

SHEET: 7 OF 98

UNUSED CPU SIGNALS

10 TP_CPU_RSVD<16..1> = NC_CPU_RSVD<16..1> MAKE_BASE=TRUE NO_TEST=TRUE
10 TP_CPU_RSVD<46..19> = NC_CPU_RSVD<46..19> MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCI ALIASES

20 TP_PCI_AD<31..0> = NC_PCI_AD<31..0> MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_PCI_C_BE_L<3..0> = NC_PCI_C_BE_L<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_PCI_PAR = NC_PCI_PAR MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_PCI_RESET_L = NC_PCI_RESET_L MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_LPC_DREQ0_L = NC_LPC_DREQ0_L MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MEM ALIASES

12 TP_MEM_A_DQ_CB<7..0> = NC_MEM_A_DQ_CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
12 TP_MEM_A_DQS_N<8> = NC_MEM_A_DQSN<8> MAKE_BASE=TRUE NO_TEST=TRUE
12 TP_MEM_A_DQS_P<8> = NC_MEM_A_DQSP<8> MAKE_BASE=TRUE NO_TEST=TRUE
12 TP_MEM_B_DQ_CB<7..0> = NC_MEM_B_DQ_CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
12 TP_MEM_B_DQS_N<8> = NC_MEM_B_DQSN<8> MAKE_BASE=TRUE NO_TEST=TRUE
12 TP_MEM_B_DQS_P<8> = NC_MEM_B_DQSP<8> MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MISC ALIASES

18 TP_HDA_SDIN1 = NC_HDA_SDIN1 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_HDA_SDIN2 = NC_HDA_SDIN2 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_HDA_SDIN3 = NC_HDA_SDIN3 MAKE_BASE=TRUE NO_TEST=TRUE

21 TP_PCH_PWM0 = NC_PCH_PWM0 MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCH_PWM1 = NC_PCH_PWM1 MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCH_PWM2 = NC_PCH_PWM2 MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCH_PWM3 = NC_PCH_PWM3 MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCH_SST = NC_PCH_SST MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCH_CL_CLK1 = NC_PCH_CL_CLK1 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCH_CL_DATA1 = NC_PCH_CL_DATA1 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCH_CL_RST1 = NC_PCH_CL_RST1 MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCIE ALIASES

18 TP_PCIE_CLK100M_PE5P = NC_PCIE_CLK100M_PE5P MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCIE_CLK100M_PE5N = NC_PCIE_CLK100M_PE5N MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCIE_CLK100M_PE6P = NC_PCIE_CLK100M_PE6P MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCIE_CLK100M_PE6N = NC_PCIE_CLK100M_PE6N MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCIE_CLK100M_PE7P = NC_PCIE_CLK100M_PE7P MAKE_BASE=TRUE NO_TEST=TRUE
21 TP_PCIE_CLK100M_PE7N = NC_PCIE_CLK100M_PE7N MAKE_BASE=TRUE NO_TEST=TRUE
10 TP_PE_RX_N<3..0> = NC_PE_RXN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
10 TP_PE_RX_P<3..0> = NC_PE_RXP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
10 TP_PE_TX_N<3..0> = NC_PE_TXN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
10 TP_PE_TX_P<3..0> = NC_PE_TXP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCIE_D2R_PERN4 = NC_PCIE_D2R_PERN4 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCIE_D2R_PERP4 = NC_PCIE_D2R_PERP4 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCIE_R2D_PETN4 = NC_PCIE_R2D_PETN4 MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCIE_R2D_PETP4 = NC_PCIE_R2D_PETP4 MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCIE_CLK100M_PE4P = NC_PCIE_CLK100M_PE4P MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCIE_CLK100M_PE4N = NC_PCIE_CLK100M_PE4N MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED USB ALIASES

20 TP_USB_1N = NC_USB_1N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_1P = NC_USB_1P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_2N = NC_USB_2N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_2P = NC_USB_2P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_3N = NC_USB_3N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_3P = NC_USB_3P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_4N = NC_USB_4N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_4P = NC_USB_4P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_5N = NC_USB_5N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_5P = NC_USB_5P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_6N = NC_USB_6N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_6P = NC_USB_6P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_7N = NC_USB_7N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_7P = NC_USB_7P MAKE_BASE=TRUE NO_TEST=TRUE

20 TP_USB_10N = NC_USB_10N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_10P = NC_USB_10P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_11N = NC_USB_11N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_11P = NC_USB_11P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_12N = NC_USB_12N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_12P = NC_USB_12P MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_13N = NC_USB_13N MAKE_BASE=TRUE NO_TEST=TRUE
20 TP_USB_13P = NC_USB_13P MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED DISPLAY ALIASES

19 TP_CRT_IG_DDC_CLK = NC_CRT_IG_DDC_CLK MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_DDC_DATA = NC_CRT_IG_DDC_DATA MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_RED = NC_CRT_IG_RED MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_GREEN = NC_CRT_IG_GREEN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_BLUE = NC_CRT_IG_BLUE MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_HSYNC = NC_CRT_IG_HSYNC MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_CRT_IG_VSYNC = NC_CRT_IG_VSYNC MAKE_BASE=TRUE NO_TEST=TRUE

19 TP_DP_IG_B_MLN<3..0> = NC_DP_IG_B_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_MLP<3..0> = NC_DP_IG_B_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_AUX_N = NC_DP_IG_B_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_AUX_P = NC_DP_IG_B_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_HPD = NC_DP_IG_B_HPD MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_DDC_CLK = NC_DP_IG_B_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_B_DDC_DATA = NC_DP_IG_B_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE

19 TP_DP_IG_C_MLN<3..0> = NC_DP_IG_C_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_MLP<3..0> = NC_DP_IG_C_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_AUX_N = NC_DP_IG_C_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_AUX_P = NC_DP_IG_C_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_HPD = NC_DP_IG_C_HPD MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_CTRL_CLK = NC_DP_IG_C_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_C_CTRL_DATA = NC_DP_IG_C_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE

19 TP_DP_IG_D_MLN<3..0> = NC_DP_IG_D_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_MLP<3..0> = NC_DP_IG_D_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_AUXN = NC_DP_IG_D_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_AUXP = NC_DP_IG_D_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_HPD = NC_DP_IG_D_HPD MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_CTRL_CLK = NC_DP_IG_D_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_DP_IG_D_CTRL_DATA = NC_DP_IG_D_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE

19 TP_SDVO_TVCLKINN = NC_SDVO_TVCLKINN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_TVCLKINP = NC_SDVO_TVCLKINP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_STALLN = NC_SDVO_STALLN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_STALLP = NC_SDVO_STALLP MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_INTN = NC_SDVO_INTN MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_SDVO_INTP = NC_SDVO_INTP MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCH_L_BKLTCTL = NC_PCH_L_BKLTCTL MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCH_L_BKLTEN = NC_PCH_L_BKLTEN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCH_L_VDD_EN = NC_PCH_L_VDD_EN MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCH_CLKOUT_DPN = NC_PCH_CLKOUT_DPN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_PCH_CLKOUT_DPP = NC_PCH_CLKOUT_DPP MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED FDI ALIASES

10 TP_CPU_FDI_TX_N<7..0> = NC_CPU_FDI_TXN<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
10 TP_CPU_FDI_TX_P<7..0> = NC_CPU_FDI_TXP<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_PCH_FDI_RX_N<7..0> = NC_PCH_FDI_RXN<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
19 TP_PCH_FDI_RX_P<7..0> = NC_PCH_FDI_RXP<7..0> MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED SATA ALIASES

18 TP_SATA_D_D2RN = NC_SATA_D_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_D_D2RP = NC_SATA_D_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_D_R2D_CN = NC_SATA_D_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_D_R2D_CP = NC_SATA_D_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_E_D2RN = NC_SATA_E_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_E_D2RP = NC_SATA_E_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_E_R2D_CN = NC_SATA_E_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_E_R2D_CP = NC_SATA_E_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_F_D2RN = NC_SATA_F_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_F_D2RP = NC_SATA_F_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_F_R2D_CN = NC_SATA_F_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
18 TP_SATA_F_R2D_CP = NC_SATA_F_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE

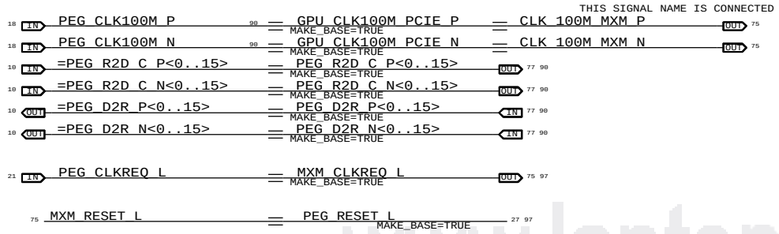
SYNC_MASTER=K62 SYNC_DATE=01/06/2011

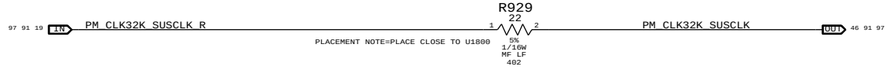
PAGE TITLE: UNUSED SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 8 OF 110
SHEET: 8 OF 98

PEG Slot Support





SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE: Signal Aliases

Apple Inc.

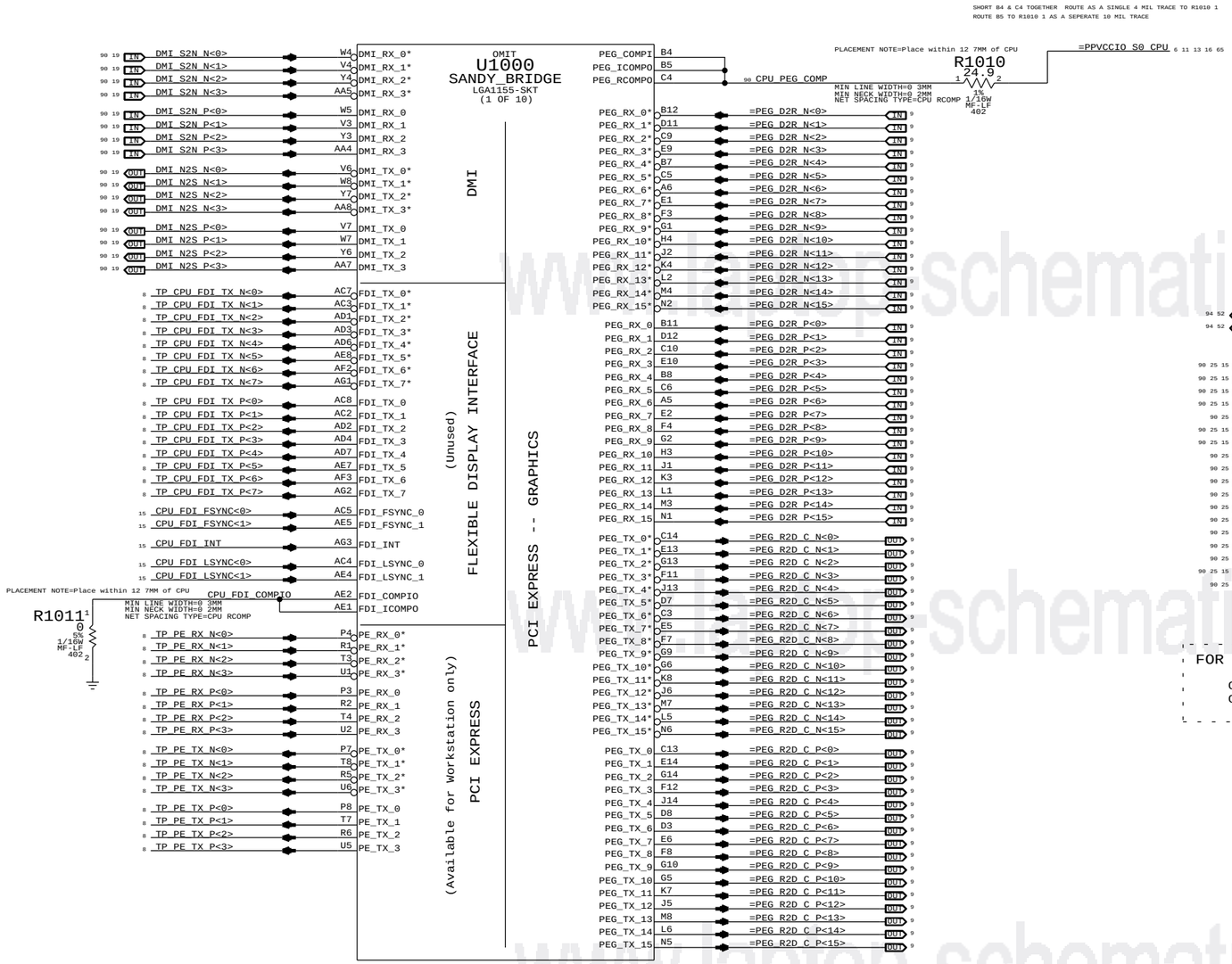
DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

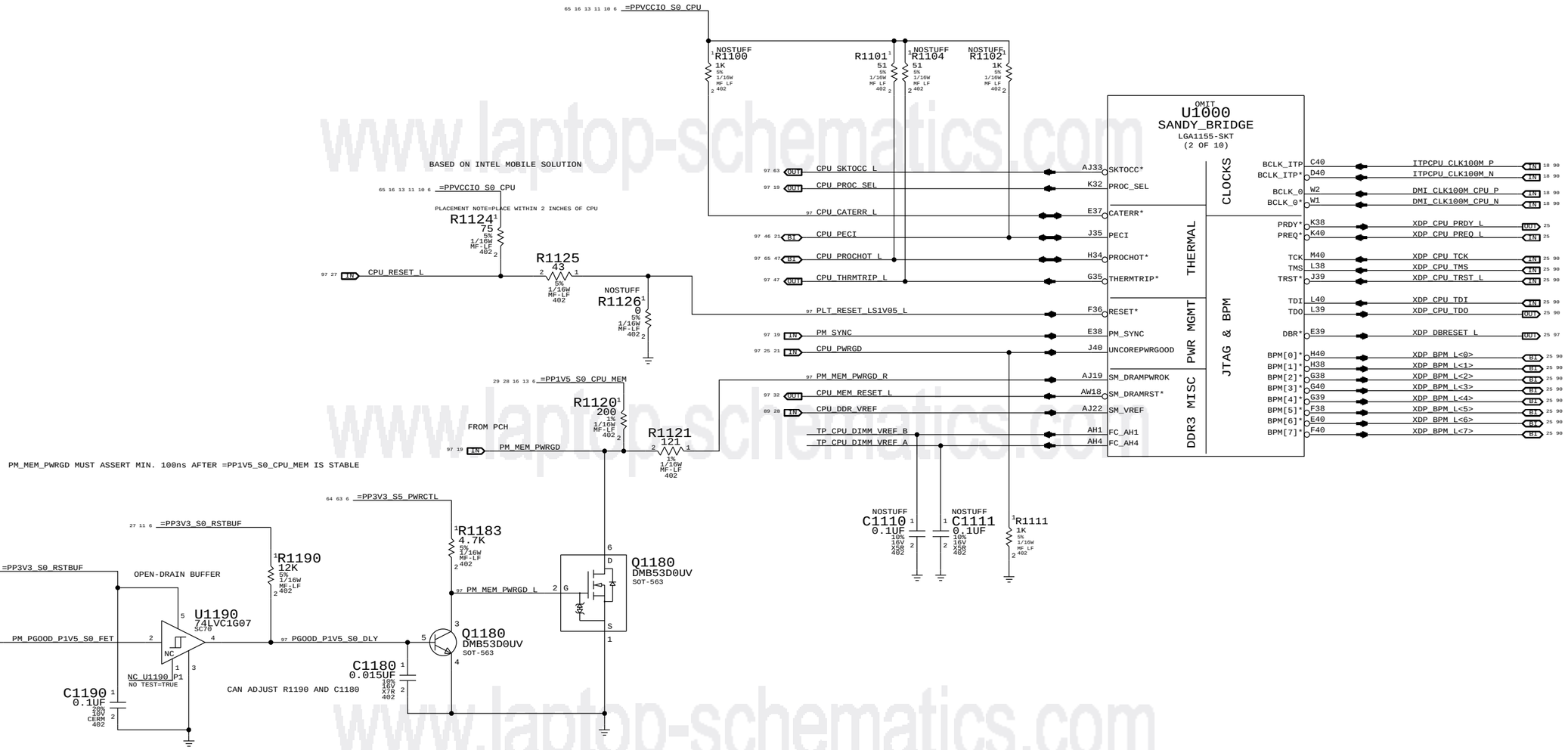
BRANCH:

PAGE: 9 OF 110

SHEET: 9 OF 98



PAGE TITLE	CPU DMI/PEG/FDI/RSVD
	Apple Inc.
DRAWING NUMBER	051-8115
SIZE	D
REVISION	11.1.0
BRANCH	
PAGE	10 OF 110
SHEET	10 OF 98



PAGE TITLE: CPU CLOCK/MISC/JTAG

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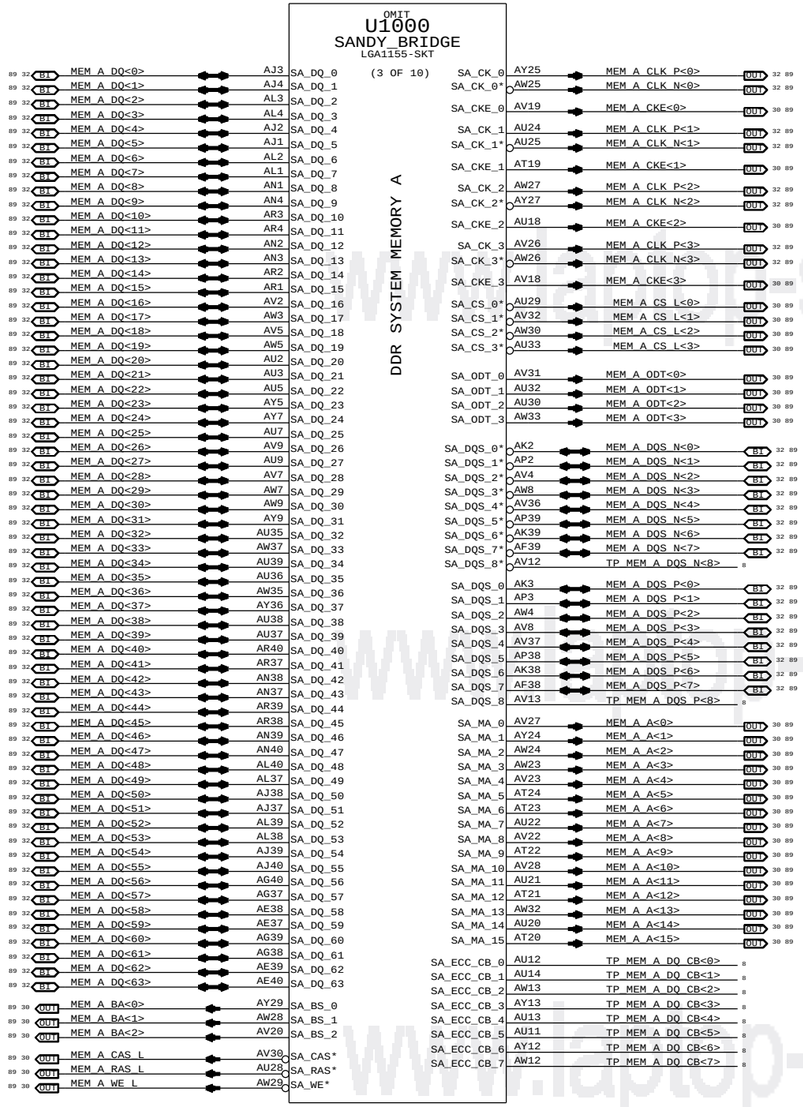
DRAWING NUMBER: 051-8115 | SIZE: D

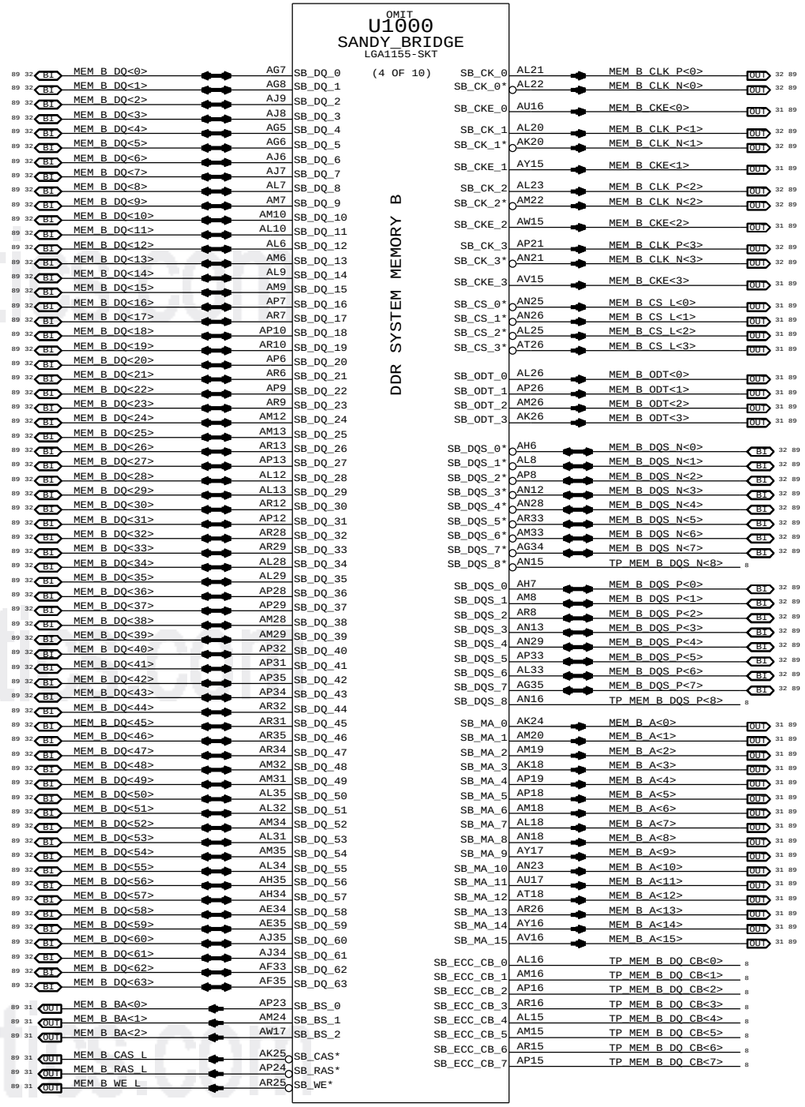
REVISION: 11.1.0

BRANCH:

PAGE: 11 OF 110

SHEET: 11 OF 98



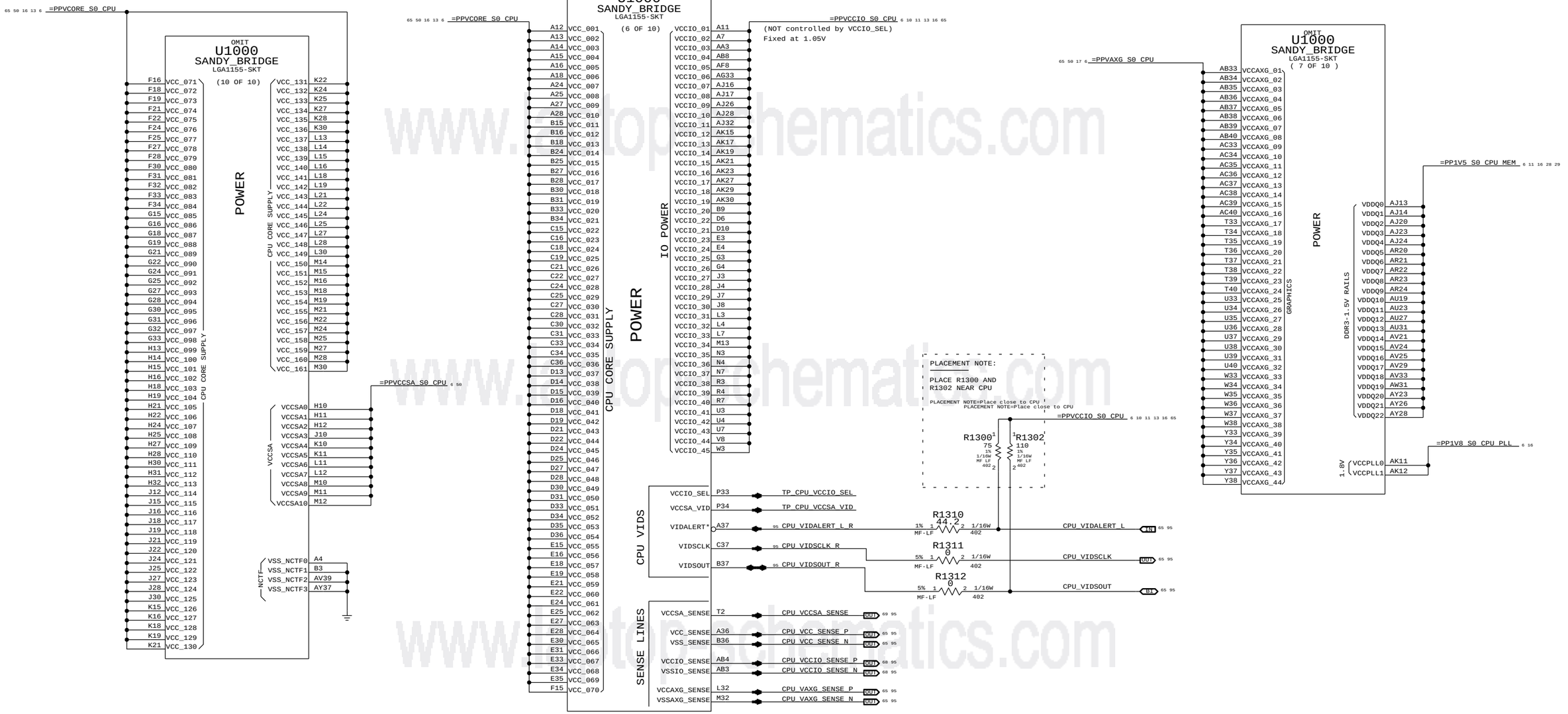


SYNC DATE=01/06/2011

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER 051-8115
SIZE D
REVISION 11.1.0
BRANCH
PAGE 12 OF 110
SHEET 12 OF 98

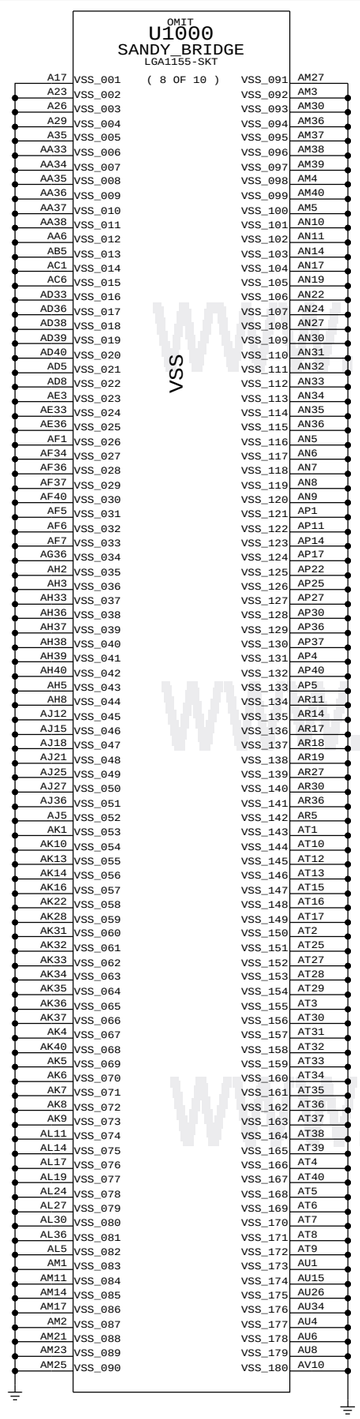


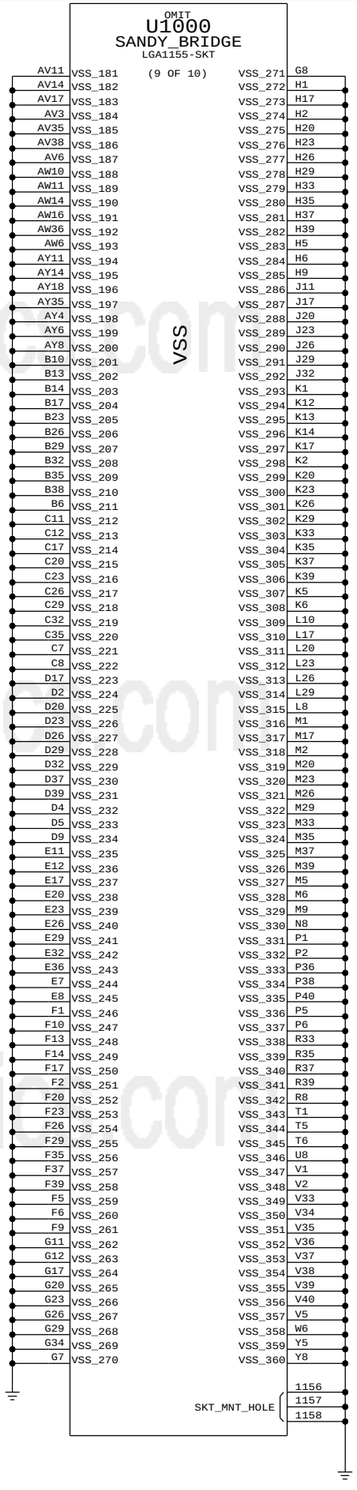
SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
CPU POWER

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 13 OF 110
SHEET 13 OF 98

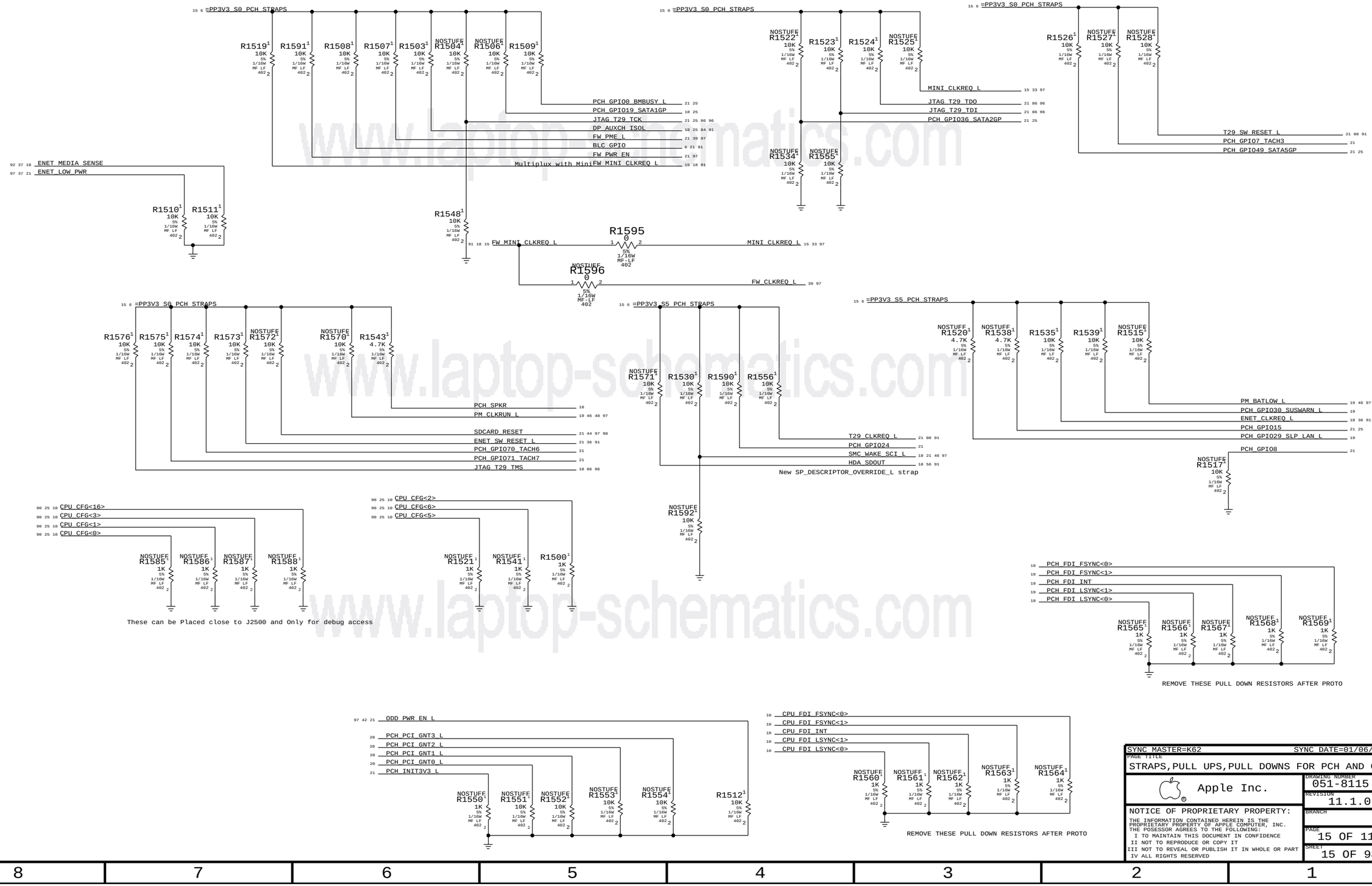




PAGE TITLE
CPU GROUNDS

Apple Inc.

DRAWING NUMBER 051-8115
SIZE D
REVISION 11.1.0
BRANCH
PAGE 14 OF 110
SHEET 14 OF 98



CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

16 13 6 =PPVCORE_S0_CPU
65 50

PLACEMENT_NOTE (C1600-C1613):

Place inside socket cavity

C1600 22UF 20% 6.3V CERM X5R 805 3
C1601 22UF 20% 6.3V CERM X5R 805 3
C1602 22UF 20% 6.3V CERM X5R 805 3
C1603 22UF 20% 6.3V CERM X5R 805 3
C1604 22UF 20% 6.3V CERM X5R 805 3
C1605 22UF 20% 6.3V CERM X5R 805 3
C1606 22UF 20% 6.3V CERM X5R 805 3
C1607 22UF 20% 6.3V CERM X5R 805 3
C1608 22UF 20% 6.3V CERM X5R 805 3
C1609 22UF 20% 6.3V CERM X5R 805 3
C1610 22UF 20% 6.3V CERM X5R 805 3
C1611 22UF 20% 6.3V CERM X5R 805 3
C1612 22UF 20% 6.3V CERM X5R 805 3
C1613 22UF 20% 6.3V CERM X5R 805 3

BULK CAPS ON CPU VREG PAGE 72

10x 10UF and 10x 1UF CAPACITORS

65 50 16 13 6 =PPVCORE_S0_CPU

Place inside socket cavity

C1620 10UF 20% 16V X5R 603
C1621 10UF 20% 16V X5R 603
C1622 10UF 20% 16V X5R 603
C1623 10UF 20% 16V X5R 603
C1624 10UF 20% 16V X5R 603
C1625 10UF 20% 16V X5R 603
C1626 10UF 20% 16V X5R 603
C1627 10UF 20% 16V X5R 603
C1628 10UF 20% 16V X5R 603
C1629 10UF 20% 16V X5R 603
C1630 1UF 10% 16V X5R 402
C1631 1UF 10% 16V X5R 402
C1632 1UF 10% 16V X5R 402
C1633 1UF 10% 16V X5R 402
C1634 1UF 10% 16V X5R 402
C1635 1UF 10% 16V X5R 402
C1636 1UF 10% 16V X5R 402
C1637 1UF 10% 16V X5R 402
C1638 1UF 10% 16V X5R 402
C1639 1UF 10% 16V X5R 402

CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

13 11 10 6 6s =PPVCCIO_S0_CPU

PLACEMENT_NOTE (C1650-C1657):

Place under socket cavity on secondary side.

C1650 22UF 20% 6.3V CERM X5R 805
C1651 22UF 20% 6.3V CERM X5R 805
C1652 22UF 20% 6.3V CERM X5R 805
C1653 22UF 20% 6.3V CERM X5R 805
C1654 22UF 20% 6.3V CERM X5R 805
C1655 22UF 20% 6.3V CERM X5R 805
C1656 22UF 20% 6.3V CERM X5R 805
C1657 22UF 20% 6.3V CERM X5R 805

PLACEMENT_NOTE (C1660-C1665):

Place at edge of socket.

BULK CAPS ON CPU VREG PAGE 72

C1660 10uF 20% 6.3V X5R 603
C1661 10uF 20% 6.3V X5R 603
C1662 10uF 20% 6.3V X5R 603
C1663 10uF 20% 6.3V X5R 603
C1664 10uF 20% 6.3V X5R 603
C1665 10uF 20% 6.3V X5R 603

C1670 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

Memory (CPU VCCDDR) DECOUPLING

6x 22uF 0805, 5x 1uF 0402. INTEL RECOMMENDATION 9X 22uF 0805

28 13 11 6 29 =PP1V5_S0_CPU_MEM

C1676 22uF 20% 6.3V CERM X5R 805
C1677 22uF 20% 6.3V CERM X5R 805
C1678 22uF 20% 6.3V CERM X5R 805
C1679 22uF 20% 6.3V CERM X5R 805
C1680 22uF 20% 6.3V CERM X5R 805
C1681 22uF 20% 6.3V CERM X5R 805
C1682 1UF 10% 10V X5R 402
C1683 1UF 10% 10V X5R 402
C1684 1UF 10% 10V X5R 402
C1685 1UF 10% 10V X5R 402
C1686 1UF 10% 10V X5R 402

Note: VCCSA decoupling is on regulator page

PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 10x 10uF 0805

13 6 =PP1V8_S0_CPU_PLL

C1693 1UF 10% 10V X5R 402
C1694 1UF 10% 10V X5R 402
C1692 2.2UF 10% 6.3V X5R 402
C1691 4.7UF 10% 6.3V X5R CERM 603
C1695 10UF 20% 6.3V X5R 603
C1690 22UF 20% 6.3V CERM X5R 805
C1696 47UF 20% 6.3V X5R 0805
C1697 47UF 20% 6.3V X5R 0805

BULK CAPS ON VTT REG PAGE 78

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
CPU NON-GFX DECOUPLING

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 16 OF 110
SHEET 16 OF 98

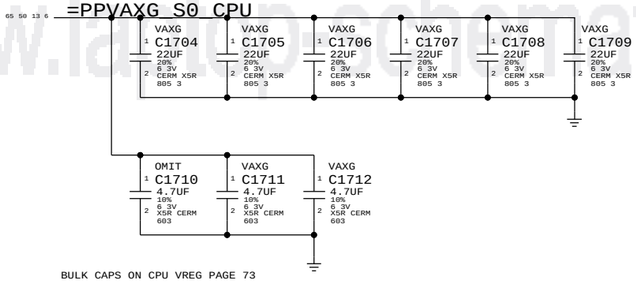
VAXG DECOUPLING

INTEL RECOMMENDATION 6X22UF 0805,3X 4.7UF

PLACEMENT_NOTE (C1704-C1709):

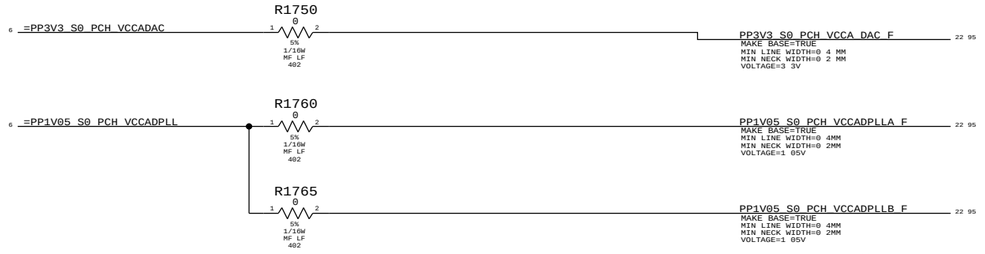
Place inside socket cavity

65 50 13 6 =PPVAXG_S0_CPU



BULK CAPS ON CPU VREG PAGE 73

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
138S0586	1	CAP,4.7UF,10%,6.3V,0603	C1710	VAXG
113S0022	1	RES,0 OHM,5%,0603	C1710	NO_VAXG



SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
GFX DECOUPLING & PCH PWR ALIAS

Apple Inc.

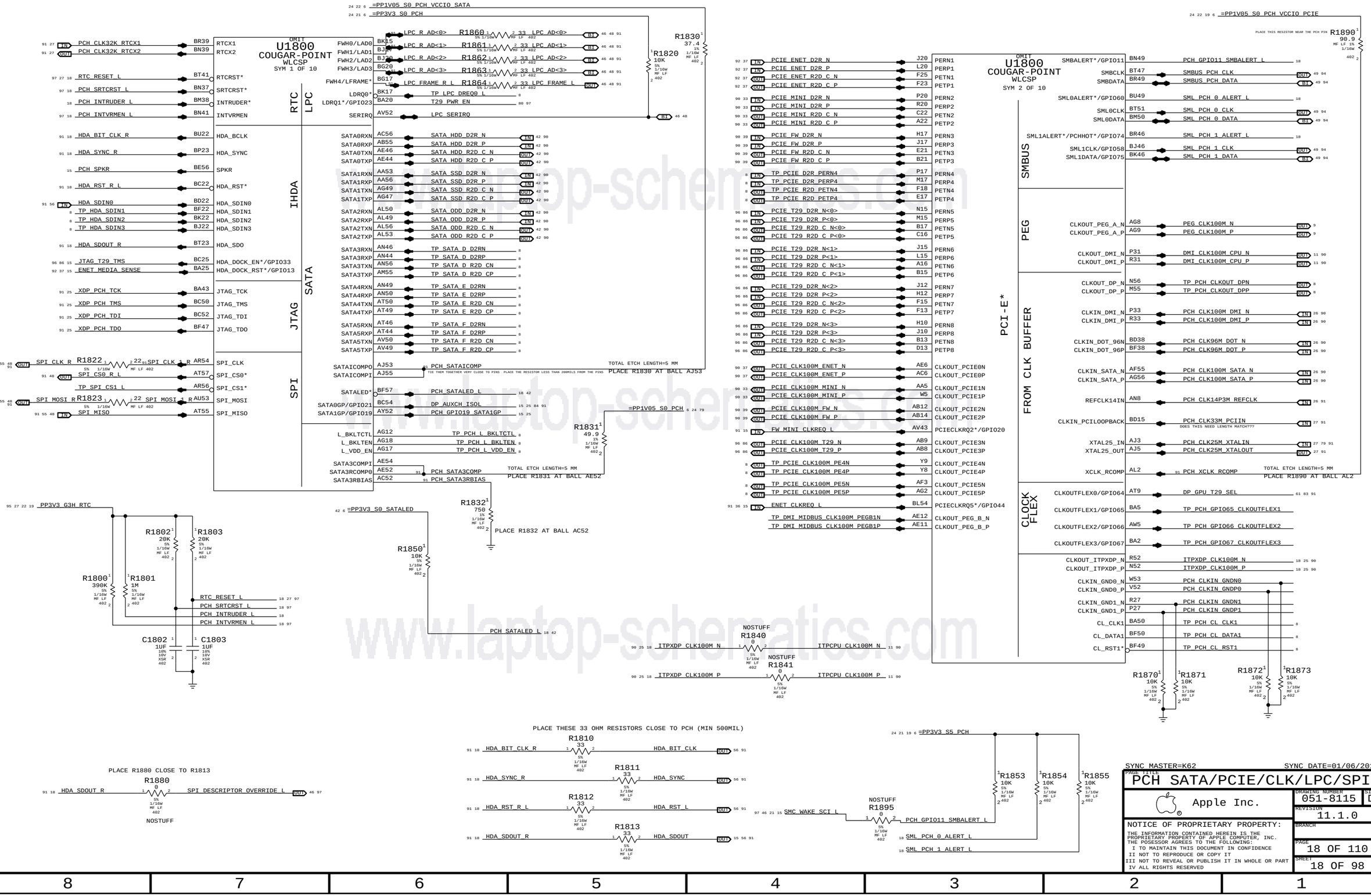
DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

BRANCH

PAGE 17 OF 110

SHEET 17 OF 98



=PP3V3_S5_PCH 6 18 19 21 24
=PP1V05_S0_PCH_VCCIO_PCIE 6 18 22 24

R1905 10K 5% 1/16W MF LF 402
R1900 49.9 1% 1/16W MF LF 402
R1920 750 1% 1/16W MF LF 402
R1909 10K 5% 1/16W MF LF 402

OMIT

U1800 COUGAR-POINT WLCSP SYM 3 OF 10

DMI

DMI_N2S_N<0>	D33	DMI0RXN
DMI_N2S_N<1>	A36	DMI1RXN
DMI_N2S_N<2>	B37	DMI2RXN
DMI_N2S_N<3>	E37	DMI3RXN
DMI_N2S_P<0>	B33	DMI0RXP
DMI_N2S_P<1>	B35	DMI1RXP
DMI_N2S_P<2>	C36	DMI2RXP
DMI_N2S_P<3>	F38	DMI3RXP
DMI_S2N_N<0>	J36	DMI0TXN
DMI_S2N_N<1>	P38	DMI1TXN
DMI_S2N_N<2>	H38	DMI2TXN
DMI_S2N_N<3>	M41	DMI3TXN
DMI_S2N_P<0>	H36	DMI0TXP
DMI_S2N_P<1>	R38	DMI1TXP
DMI_S2N_P<2>	J38	DMI2TXP
DMI_S2N_P<3>	P41	DMI3TXP
PCH_DMI2RBIAS	A32	DMI2RBIAS
PCH_DMI_COMP	E31	DMI_ZCOMP
	B31	DMI_IRCOMP

PLACE R1920 AT BALL A32
SHORT THESE TWO PINS VERY NEAR THE PINS. PLACE THE RESISTOR VERY CLOSE TO COMMON POINT
PLACE R1900 AT BALL E31
TOTAL ETCH LENGTH=5 MM

FDI

FDI_RXN0	C42	TP_PCH_FDI_RX_N<0>
FDI_RXN1	F45	TP_PCH_FDI_RX_N<1>
FDI_RXN2	H41	TP_PCH_FDI_RX_N<2>
FDI_RXN3	C46	TP_PCH_FDI_RX_N<3>
FDI_RXN4	B45	TP_PCH_FDI_RX_N<4>
FDI_RXN5	B47	TP_PCH_FDI_RX_N<5>
FDI_RXN6	J43	TP_PCH_FDI_RX_N<6>
FDI_RXN7	M43	TP_PCH_FDI_RX_N<7>
FDI_RXP0	B43	TP_PCH_FDI_RX_P<0>
FDI_RXP1	F43	TP_PCH_FDI_RX_P<1>
FDI_RXP2	J41	TP_PCH_FDI_RX_P<2>
FDI_RXP3	D47	TP_PCH_FDI_RX_P<3>
FDI_RXP4	A46	TP_PCH_FDI_RX_P<4>
FDI_RXP5	C49	TP_PCH_FDI_RX_P<5>
FDI_RXP6	H43	TP_PCH_FDI_RX_P<6>
FDI_RXP7	P43	TP_PCH_FDI_RX_P<7>
FDI_INT	H46	PCH_FDI_INT
FDI_FSYNC0	B51	PCH_FDI_FSYNC<0>
FDI_FSYNC1	C52	PCH_FDI_FSYNC<1>
FDI_LSYNC0	E49	PCH_FDI_LSYNC<0>
FDI_LSYNC1	D51	PCH_FDI_LSYNC<1>

SYSTEM_POWER MANAGEMENT

PM_SYSRST_L	BE52	SYS_RESET*
PM_SYS_PWRGD	BJ53	SYS_PWROK
PM_PCH_PWRGD	BJ38	PWROK
PM_MEM_PWRGD	BG46	DRAMPWROK
PM_DSW_PWRGD	BT37	DPWROK
PM_ASW_PWRGD	BC46	APWROK
PM_RSMRST_PCH_L	BK38	RSMRST*
PCH_GPIO30_SUSWARN_L	BU46	SUSWARN*/SUSPWRDNACK/GPIO30
PM_PWRBTN_L	BT43	PWRBTN*
PCH_GPIO31_ACPRESENT	BG43	GPIO31
PM_BATLOW_L	AV46	BATLOW*/GPIO72
PCH_RI_L	BJ48	RI*

WAKE*	BC44	PCIE_WAKE_L
CLKRUN*/GPIO32	BC56	PM_CLKRUN_L
SUS_STAT*/GPIO61	BN54	LPC_PWRDWN_L
SUSCLK/GPIO62	BA47	PM_CLK32K_SUSCLK_R
SLP_S5*/GPIO63	BH50	PM_SLP_S5_L
SLP_S4*	BN52	PM_SLP_S4_L
SLP_S3*	BM53	PM_SLP_S3_L
SLP_A*	BC41	TP_PM_SLP_A_L
TP23	J25	TP_PCH_TP23
PMSYNCH	F55	PM_SYNC
SLP_LAN*/GPIO29	BH49	PCH_GPIO29_SLP_LAN_L
DF_TVS	R47	PCH_DF_TVS
DSWVRMEN	BR42	PCH_DSWVRMEN
SLP_SUS*	BD43	TP_PCH_SLP_SUS_L
SUSACK*	BP45	TP_PCH_SUSACK_L

KEEPING TP IF NEED TO USE IT LATER

OMIT

U1800 COUGAR-POINT WLCSP SYM 4 OF 10

TP_PCH_RESERVE_0	J57	RESERVED_0
TP_PCH_RESERVE_1	U43	RESERVED_1
TP_PCH_RESERVE_2	M49	RESERVED_2
TP_PCH_RESERVE_3	M50	RESERVED_3
TP_PCH_RESERVE_4	R50	RESERVED_4
TP_PCH_RESERVE_5	Y41	RESERVED_5
TP_PCH_RESERVE_6	H50	RESERVED_6
TP_PCH_RESERVE_7	U44	RESERVED_7
TP_PCH_RESERVE_8	U46	RESERVED_8
TP_PCH_RESERVE_9	U50	RESERVED_9
TP_PCH_RESERVE_10	R44	RESERVED_10
TP_PCH_RESERVE_11	U49	RESERVED_11
TP_PCH_RESERVE_12	AB44	RESERVED_12
TP_PCH_RESERVE_13	AB49	RESERVED_13
TP_PCH_RESERVE_14	E52	RESERVED_14
TP_PCH_RESERVE_15	H52	RESERVED_15
TP_PCH_RESERVE_16	F53	RESERVED_16
TP_PCH_RESERVE_17	J55	RESERVED_17
TP_PCH_RESERVE_18	L56	RESERVED_18
TP_PCH_RESERVE_19	K46	RESERVED_19
TP_PCH_RESERVE_20	Y50	RESERVED_20
TP_PCH_RESERVE_21	AB50	RESERVED_21
TP_PCH_RESERVE_22	L53	RESERVED_22
TP_PCH_RESERVE_23	Y44	RESERVED_23
TP_PCH_RESERVE_24	G56	RESERVED_24
TP_PCH_RESERVE_25	AB46	RESERVED_25
TP_PCH_RESERVE_26	K49	RESERVED_26
TP_PCH_RESERVE_27	K50	RESERVED_27
TP_PCH_RESERVE_28	M48	RESERVED_28

DIGITAL DISPLAY INTERFACE

CRT

TP_CRT_IG_BLUE	AM1	CRT_BLUE
TP_CRT_IG_GREEN	AN2	CRT_GREEN
TP_CRT_IG_RED	AN6	CRT_RED
TP_CRT_IG_DDC_CLK	AW3	CRT_DDC_CLK
TP_CRT_IG_DDC_DATA	AW1	CRT_DDC_DATA
TP_CRT_IG_HSYNC	AR4	CRT_HSYNC
TP_CRT_IG_VSYNC	AR2	CRT_VSYNC
PCH_DAC_IREF	AT3	DAC_IREF
	AM6	CRT_IRTN

R1951 1K 1% 1/16W MF LF 402
PLACE CLOSE TO U1800 PIN

EXTERNAL DP

SDVO_TVCLKINN	U9	TP_SDVO_TVCLKINN
SDVO_TVCLKINP	U8	TP_SDVO_TVCLKINP
SDVO_STALLN	U5	TP_SDVO_STALLN
SDVO_STALLP	W3	TP_SDVO_STALLP
SDVO_INTN	T3	TP_SDVO_INTN
SDVO_INTP	U2	TP_SDVO_INTP
SDVO_CTRLCLK	AL15	TP_DP_IG_B_DDC_CLK
SDVO_CTRLDATA	AL17	TP_DP_IG_B_DDC_DATA
DDPB_AUXN	R9	TP_DP_IG_B_AUX_N
DDPB_AUXP	R8	TP_DP_IG_B_AUX_P
DDPB_HPD	T1	TP_DP_IG_B_HPD
DDPB_0N	R12	TP_DP_IG_B_MLN<0>
DDPB_0P	R14	TP_DP_IG_B_MLP<0>
DDPB_1N	M12	TP_DP_IG_B_MLN<1>
DDPB_1P	M11	TP_DP_IG_B_MLP<1>
DDPB_2N	K8	TP_DP_IG_B_MLN<2>
DDPB_2P	H8	TP_DP_IG_B_MLP<2>
DDPB_3N	M3	TP_DP_IG_B_MLN<3>
DDPB_3P	L5	TP_DP_IG_B_MLP<3>

INTERNAL DP

DDPC_CTRLCLK	AL12	TP_DP_IG_C_CTRL_CLK
DDPC_CTRLDATA	AL14	TP_DP_IG_C_CTRL_DATA
DDPC_AUXN	U12	TP_DP_IG_C_AUX_N
DDPC_AUXP	U14	TP_DP_IG_C_AUX_P
DDPC_HPD	N2	TP_DP_IG_C_HPD
DDPC_0N	J3	TP_DP_IG_C_MLN<0>
DDPC_0P	L2	TP_DP_IG_C_MLP<0>
DDPC_1N	G4	TP_DP_IG_C_MLN<1>
DDPC_1P	G2	TP_DP_IG_C_MLP<1>
DDPC_2N	F5	TP_DP_IG_C_MLN<2>
DDPC_2P	F3	TP_DP_IG_C_MLP<2>
DDPC_3N	E2	TP_DP_IG_C_MLN<3>
DDPC_3P	E4	TP_DP_IG_C_MLP<3>
DDPD_CTRLCLK	AL9	TP_DP_IG_D_CTRL_CLK
DDPD_CTRLDATA	AL8	TP_DP_IG_D_CTRL_DATA
DDPD_AUXN	R6	TP_DP_IG_D_AUXN
DDPD_AUXP	N6	TP_DP_IG_D_AUXP
DDPD_HPD	M1	TP_DP_IG_D_HPD
DDPD_0N	B5	TP_DP_IG_D_MLN<0>
DDPD_0P	D5	TP_DP_IG_D_MLP<0>
DDPD_1N	D7	TP_DP_IG_D_MLN<1>
DDPD_1P	C6	TP_DP_IG_D_MLP<1>
DDPD_2N	C9	TP_DP_IG_D_MLN<2>
DDPD_2P	B7	TP_DP_IG_D_MLP<2>
DDPD_3N	B11	TP_DP_IG_D_MLN<3>
DDPD_3P	E11	TP_DP_IG_D_MLP<3>

PP3V3_G3H_RTC 18 22 27 95
R1915 390K 5% 1/16W MF LF 402
PCH_DSWVRMEN 19 97

R1990 0 5% 1/16W MF LF 402
PM_RSMRST_PCH_L 97 27 19
PM_DSW_PWRGD 19 97

=PP3V3_S5_PCH 6 18 19 21 24
R1961 10K 5% 1/16W MF LF 402
NOSTUFF
R1960 0 5% 1/16W MF LF 402
SMC_ADAPTER_EN 97 47 46
PCH_GPIO31_ACPRESENT 19

=PP3V3_S5_PCH 6 18 19 21 24
R1925 1K 1% 1/16W MF LF 402
PCIE_WAKE_L 19 33 36 78 97

=PP1V8_S0_PCH 6
R1981 2.2K 5% 1/16W MF LF 402
R1980 4.7K 5% 1/16W MF LF 402
PCH_DF_TVS 97 19
CPU_PROC_SEL 11 97

PAGE TITLE	PCH DMI/FDI/GRAPHICS
Apple Inc.	DRAWING NUMBER 051-8115
	SIZE D
	REVISION 11.1.0
	BRANCH
	PAGE 19 OF 110
	SHEET 19 OF 98

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OMIT

U1800
COUGAR-POINT
WLCSP
SYM 5 OF 10

PCI

TP_PCI_AD<0>	BF15	AD0	
TP_PCI_AD<1>	BF17	AD1	
TP_PCI_AD<2>	BT7	AD2	
TP_PCI_AD<3>	BT13	AD3	
TP_PCI_AD<4>	BG12	AD4	
TP_PCI_AD<5>	BN11	AD5	
TP_PCI_AD<6>	BJ12	AD6	
TP_PCI_AD<7>	BU9	AD7	
TP_PCI_AD<8>	BR12	AD8	
TP_PCI_AD<9>	BJ3	AD9	
TP_PCI_AD<10>	BR9	AD10	
TP_PCI_AD<11>	BJ10	AD11	
TP_PCI_AD<12>	BM8	AD12	
TP_PCI_AD<13>	BF3	AD13	
TP_PCI_AD<14>	BN2	AD14	
TP_PCI_AD<15>	BE4	AD15	
TP_PCI_AD<16>	BE6	AD16	
TP_PCI_AD<17>	BG15	AD17	
TP_PCI_AD<18>	BC6	AD18	
TP_PCI_AD<19>	BT11	AD19	
TP_PCI_AD<20>	BA14	AD20	
TP_PCI_AD<21>	BL2	AD21	
TP_PCI_AD<22>	BC4	AD22	
TP_PCI_AD<23>	BL4	AD23	
TP_PCI_AD<24>	BC2	AD24	
TP_PCI_AD<25>	BM13	AD25	
TP_PCI_AD<26>	BA9	AD26	
TP_PCI_AD<27>	BF9	AD27	
TP_PCI_AD<28>	BA8	AD28	
TP_PCI_AD<29>	BF8	AD29	
TP_PCI_AD<30>	AV17	AD30	
TP_PCI_AD<31>	BK12	AD31	
TP_PCI_C_BE_L<0>	BN4	C/BE0*	
TP_PCI_C_BE_L<1>	BP7	C/BE1*	
TP_PCI_C_BE_L<2>	BG2	C/BE2*	
TP_PCI_C_BE_L<3>	BP13	C/BE3*	
PCI_INTA_L	BK10	PIRQA*	
PCI_INTB_L	BJ5	PIRQB*	
PCI_INTC_L	BM15	PIRQC*	
PCI_INTD_L	BP5	PIRQD*	
PCI_REQ0_L	BG5	REQ0*	
PCI_REQ1_L	BT5	REQ1*/GPIO50	
PCI_REQ2_L	BK8	REQ2*/GPIO52	
PCI_REQ3_L	AV11	REQ3*/GPIO54	
PCH_PCI_GNT0_L	BA15	GNT0*	
PCH_PCI_GNT1_L	AV8	GNT1*/GPIO51	
PCH_PCI_GNT2_L	BU12	GNT2*/GPIO53	
PCH_PCI_GNT3_L	BE2	GNT3*/GPIO55	
USE_HDD_OOB_L	BN9	PIRQE*/GPIO2	
AUD_IP_PERIPHERAL_DET	AV9	PIRQF*/GPIO3	
T29_MCU_INT_L	BT15	PIRQG*/GPIO4	
AUD_I2C_INT_L	BR4	PIRQH*/GPIO5	
TP_PCI_RESET_L	AV14	PCIRST*	
PCI_SERR_L	BR6	SERR*	
PCI_PERR_L	BM3	PERR*	
PCI_IRDY_L	BF11	IRDY*	
TP_PCI_PAR	BH8	PAR	
PCI_DEVSEL_L	BH9	DEVSEL*	
PCI_FRAME_L	BC11	FRAME*	
PCI_PLOCK_L	BA17	PLOCK*	
PCI_STOP_L	BC12	STOP*	
PCI_TRDY_L	BC8	TRDY*	
TP_PCI_PME_L	AV15	PME*	
PLT_RESET_L	BK48	PLTRST*	
LPC_CLK33M_SMC_R	AT11	CLKOUT_PCI0	
LPC_CLK33M_LPCPLUS_R	AN14	CLKOUT_PCI1	
TP_PCI_CLK33M_OUT2	AT12	CLKOUT_PCI2	
TP_PCI_CLK33M_OUT3	AT17	CLKOUT_PCI3	
PCH_CLK33M_PCIOUT	AT14	CLKOUT_PCI4	

USB

USBP0N	BF36	USB_HUB1_UP_N	USB HUB 1
USBP0P	BD36	USB_HUB1_UP_P	
USBP1N	BC33	TP_USB_1N	Unused
USBP1P	BA33	TP_USB_1P	
USBP2N	BM33	TP_USB_2N	Unused
USBP2P	BM35	TP_USB_2P	
USBP3N	BT33	TP_USB_3N	Unused
USBP3P	BU32	TP_USB_3P	
USBP4N	BR32	TP_USB_4N	Unused
USBP4P	BT31	TP_USB_4P	
USBP5N	BN29	TP_USB_5N	Unused
USBP5P	BM30	TP_USB_5P	
USBP6N	BK33	TP_USB_6N	Unused
USBP6P	BJ33	TP_USB_6P	
USBP7N	BF31	TP_USB_7N	Unused
USBP7P	BD31	TP_USB_7P	
USBP8N	BN27	USB_HUB2_UP_N	USB HUB 2
USBP8P	BR29	USB_HUB2_UP_P	
USBP9N	BR26	USB_CAMERA_N	USB CAMERA
USBP9P	BT27	USB_CAMERA_P	
USBP10N	BK25	TP_USB_10N	Unused
USBP10P	BJ25	TP_USB_10P	
USBP11N	BJ31	TP_USB_11N	Unused
USBP11P	BK31	TP_USB_11P	
USBP12N	BF27	TP_USB_12N	Unused
USBP12P	BD27	TP_USB_12P	
USBP13N	BJ27	TP_USB_13N	Unused
USBP13P	BK27	TP_USB_13P	
USBRBIAS*	BP25	PCH_USB_RBIAS	
USBRBIAS	BM25		

PLACE THE RESISTOR CLOSE TO COMMON POINT
TIE TRACES TOGETHER CLOSE TO PIN

OC0*/GPIO59	BM43	
OC1*/GPIO40	BD41	AP_PWR_EN
OC2*/GPIO41	BG41	USB_HUB_SOFT_RESET_L
OC3*/GPIO42	BK43	T29_DP_PORTA_PWR_EN
OC4*/GPIO43	BP43	ENET_PWR_EN
OC5*/GPIO9	BJ41	T29_DP_PORTB_PWR_EN
OC6*/GPIO10	BT45	SDCONN_STATE_CHANGE
OC7*/GPIO14	BM45	PCH_GPIO10_OC6_L
		PCH_GPIO14_OC7_L

=PP3V3_S5_PCH_GPIO

R2060 10K 5% 1/16W MF LF 402
R2061 10K 5% 1/16W MF LF 402
R2062 10K 5% 1/16W MF LF 402
R2063 10K 5% 1/16W MF LF 402
R2064 10K 5% 1/16W MF LF 402
PRODUCTION
R2065 10K 5% 1/16W MF LF 402
R2066 10K 5% 1/16W MF LF 402
R2068 10K 5% 1/16W MF LF 402

R2070 22.6 1% 1/16W MF LF 402

PLACE R2070 AT BALL BM25

=PP3V3_S0_PCH_GPIO

R2010 10K 5% 1/16W MF LF 402 PCI_INTA_L
R2011 10K 5% 1/16W MF LF 402 PCI_INTB_L
R2012 10K 5% 1/16W MF LF 402 PCI_INTC_L
R2013 10K 5% 1/16W MF LF 402 PCI_INTD_L
R2015 10K 5% 1/16W MF LF 402 PCI_REQ0_L
R2016 10K 5% 1/16W MF LF 402 PCI_REQ1_L
R2030 10K 5% 1/16W MF LF 402 USE_HDD_OOB_L
R2031 10K 5% 1/16W MF LF 402 AUD_IP_PERIPHERAL_DET
R2020 10K 5% 1/16W MF LF 402 PCI_SERR_L
R2021 10K 5% 1/16W MF LF 402 PCI_PERR_L
R2022 10K 5% 1/16W MF LF 402 PCI_IRDY_L
R2023 10K 5% 1/16W MF LF 402 TP_PCI_PAR
R2024 10K 5% 1/16W MF LF 402 PCI_DEVSEL_L
R2027 10K 5% 1/16W MF LF 402 PCI_FRAME_L
R2025 10K 5% 1/16W MF LF 402 PCI_PLOCK_L
R2026 10K 5% 1/16W MF LF 402 PCI_STOP_L
PCI_TRDY_L

PCH SATA PORT 1 OPTION SELECT IS ODD OR SSD

PCI_REQ2_L
R2017 10K ODD_SATA:P2 =PP3V3_S0_PCH_GPIO
R2098 10K ODD_SATA:P1
5% 1/16W MF LF 402

K60E MLB CFG SELECT

PCI_REQ3_L
R2018 10K T29 =PP3V3_S0_PCH_GPIO
R2099 10K NO_T29
5% 1/16W MF LF 402

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
PCH PCI/FLASHCACHE/USB

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DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 20 OF 110
SHEET 20 OF 98

=PP3V3_S0_PCH

R2190 47K 5% 1/16W MF LF 402

48 IN

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U1800
COUGAR-POINT
WLCSP
SYM 6 OF 10

PCH_GPIO0_BMBUSY_L	AW55	BMBUSY*/GPIO0	
FW_PME_L	BR19	TACH1/GPIO1	
R2134 0 1/16W 5% 402 MF LF; SMC_RUNTIME_SCI_L → BLC_GPIO	BA22	TACH2/GPIO6	
PCH_GPIO7_TACH3	BR16	TACH3/GPIO7	
PCH_GPIO8	BP51	GPIO8	
ENET_LOW_PWR	BK50	LAN_PHY_PWR_CTRL/GPIO12	
PCH_GPIO15	BM55	GPIO15	
AUD_IPHS_SWITCH_EN_PCH	AU56	SATA4GP/GPIO16	
LPCPLUS_GPIO	BT17	TACH0/GPIO17	
ODD_PWR_EN_L	BA53	SCLOCK/GPIO22	
PCH_GPIO24	BP53	GPIO24/MEM_LED	
SMC_WAKE_SCI_L	BJ43	GPIO27	
ISOLATE_CPU_MEM_L	BJ55	GPIO28	
T29_SW_RESET_L	BL56	STP_PCI*/GPIO34	
MXM_GOOD	BJ57	GPIO35	
PCH_GPIO36_SATA2GP	BB55	SATA2GP/GPIO36	
JTAG_T29_TCK	BG53	SATA3GP/GPIO37	
JTAG_T29_TDO	BE54	SLOAD/GPIO38	
JTAG_T29_TDI	BF55	SDATAOUT0/GPIO39	
PCH_PEG_CLKREQ_L	AV44	PCIECLKRQ6*/GPIO45	
T29_CLKREQ_L	BP55	PCIECLKRQ7*/GPIO46	
FW_PWR_EN	AW53	SDATAOUT1/GPIO48	
PCH_GPIO49_SATA5GP	BA56	SATA5GP/GPIO49	
SPIROM_USE_MLB	BT53	GPIO57	
SDCARD_RESET	BU16	TACH4/GPIO68	
ENET_SW_RESET_L	BM18	TACH5/GPIO69	
PCH_GPIO70_TACH6	BN17	TACH6/GPIO70	
PCH_GPIO71_TACH7	BP15	TACH7/GPIO71	
TP_PCH_PWM0	BN21	PWM0	RSVD
TP_PCH_PWM1	BT21	PWM1	
TP_PCH_PWM2	BM20	PWM2	
TP_PCH_PWM3	BN19	PWM3	
TP_PCH_SST	BC43	SST	
	A4	VSS_NCTF_0	NCTF
	A6	VSS_NCTF_1	
	B2	VSS_NCTF_2	
	BM1	VSS_NCTF_3	
	BM57	VSS_NCTF_4	
	BP1	VSS_NCTF_5	
	BP57	VSS_NCTF_6	
	BT2	VSS_NCTF_7	
	BU4	VSS_NCTF_8	
	BU52	VSS_NCTF_9	
	BU54	VSS_NCTF_10	
	BU6	VSS_NCTF_11	
	D1	VSS_NCTF_12	
	F1	VSS_NCTF_13	
	A54	TS_VSS1	
	A52	TS_VSS2	
	F57	TS_VSS3	
	D57	TS_VSS4	
	AU2	VSSADAC	

MISC
CPU
GPIO

	AB3	CLKOUT_PCIE6N	TP_PCIE_CLK100M_PE6N
	AA2	CLKOUT_PCIE6P	TP_PCIE_CLK100M_PE6P
	AE2	CLKOUT_PCIE7N	TP_PCIE_CLK100M_PE7N
	AF1	CLKOUT_PCIE7P	TP_PCIE_CLK100M_PE7P
	BB57	A20GATE	PCH_A20GATE
PECI	H48	PECI	R2170 0 1/16W 5% MF LF 402 NOSTUFF; PCH_PECI → CPU_PECI
RCIN*	BG56	RCIN*	PCH_RCIN_L
PROCPWRGD	D53	PROCPWRGD	R2140 0 1/16W 5% MF LF 402; PCH_PROCPWRGD → CPU_PWRGD
THRMTRIP*	E56	THRMTRIP*	PM_THRMTRIP_L
TP1	P22		TP_PCH_TP1
TP2	L31		TP_PCH_TP2
TP3	L33		TP_PCH_TP3
TP4	M38		TP_PCH_TP4
TP5	L36		TP_PCH_TP5
TP6	Y18		TP_PCH_TP6
TP7	Y17		TP_PCH_TP7
TP8	AB18		TP_PCH_TP8
TP9	AB17		TP_PCH_TP9
TP10	BM46		TP_PCH_TP10
TP11	BA27		TP_PCH_TP11
TP12	BC49		TP_PCH_TP12
TP13	AE49		TP_PCH_TP13
TP14	AE41		TP_PCH_TP14
TP15	AE43		TP_PCH_TP15
TP16	AE50		TP_PCH_TP16
TP17	BA36		TP_PCH_TP17
TP18	AY36		TP_PCH_TP18
TP19	Y14		TP_PCH_TP19
TP20	Y12		TP_PCH_TP20
TP21	H31		TP_PCH_TP21
TP22	J27		TP_PCH_TP22
TP24	L22		TP_PCH_TP24
TP25	J31		TP_PCH_TP25
TP26	L27		TP_PCH_TP26
TP27	L25		TP_PCH_TP27
TP28	J22		TP_PCH_TP28
TP29	C29		TP_PCH_TP29
TP30	F28		TP_PCH_TP30
TP31	C26		TP_PCH_TP31
TP32	B25		TP_PCH_TP32
TP33	E29		TP_PCH_TP33
TP34	E27		TP_PCH_TP34
TP35	B27		TP_PCH_TP35
TP36	D25		TP_PCH_TP36
NC_1	AY20		TP_PCH_NC
INIT3_3V*	BN56		PCH_INIT3V3_L

THIS SIGNAL IS INTEDED FOR FIRMWARE HUB AND WE ARE NOT USING IT.
This has internal pull up and should not pulled low.

Place this near the T point

R2150 10K 5% 1/16W MF LF 402 2

R2155 10K 5% 1/16W MF LF 402 2

=PP3V3_S0_PCH

=PP3V3_S3_PCH

U2100 MC74VHC1G08 SOT23-5-HF

AUD_IPHS_SWITCH_EN_PCH → AUD_IPHS_SWITCH_EN

PM_PCH_PWRGD

C2110 0.1UF 20% 16V CERM 402

=PP3V3_S5_PCH

R2161 10K 5% 1/16W MF LF 402

Q2100 SSM3K15FV SOD-VESM-HF

=PP3V3_S0_MXM

PCH_PEG_CLKREQ_L → PEG_CLKREQ_L

R2160 0 1/16W 5% 402 MF LF NOSTUFF

MXM CLKREQ ISOLATION

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE: PCH MISC

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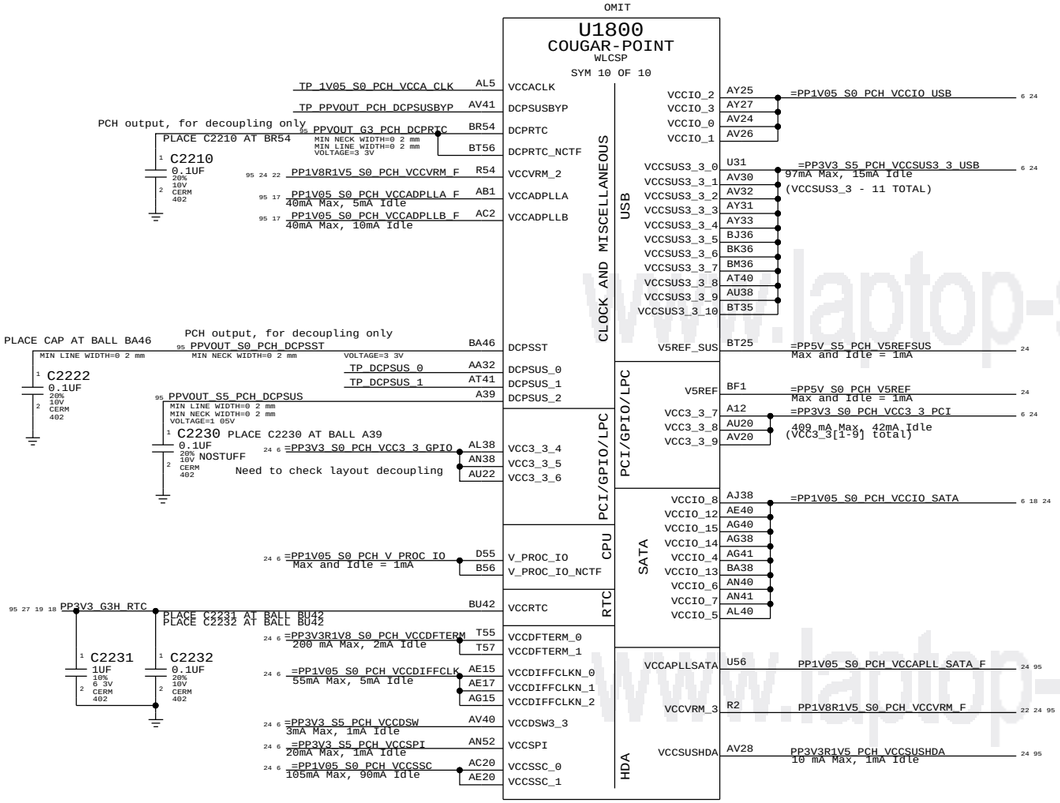
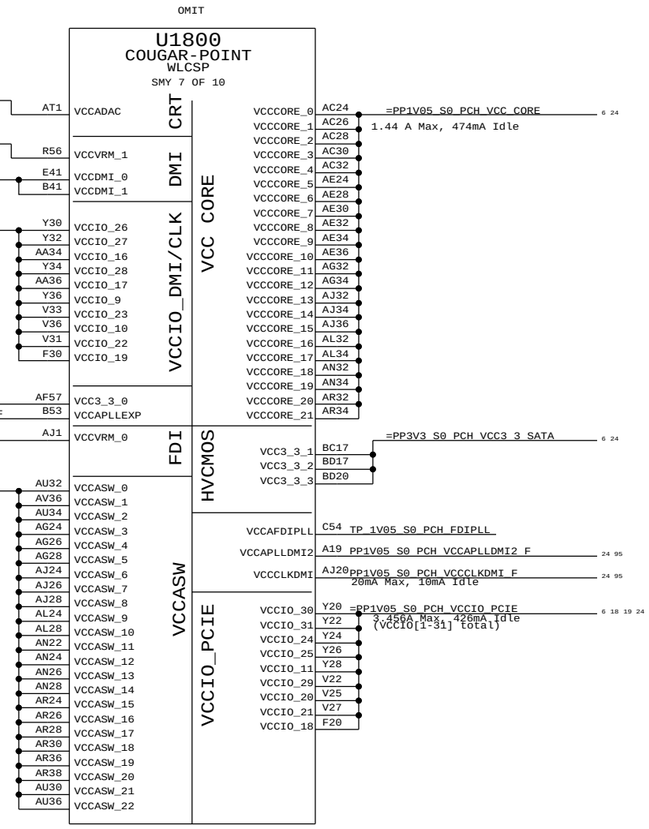
DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 21 OF 110
SHEET 21 OF 98





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PCH POWER

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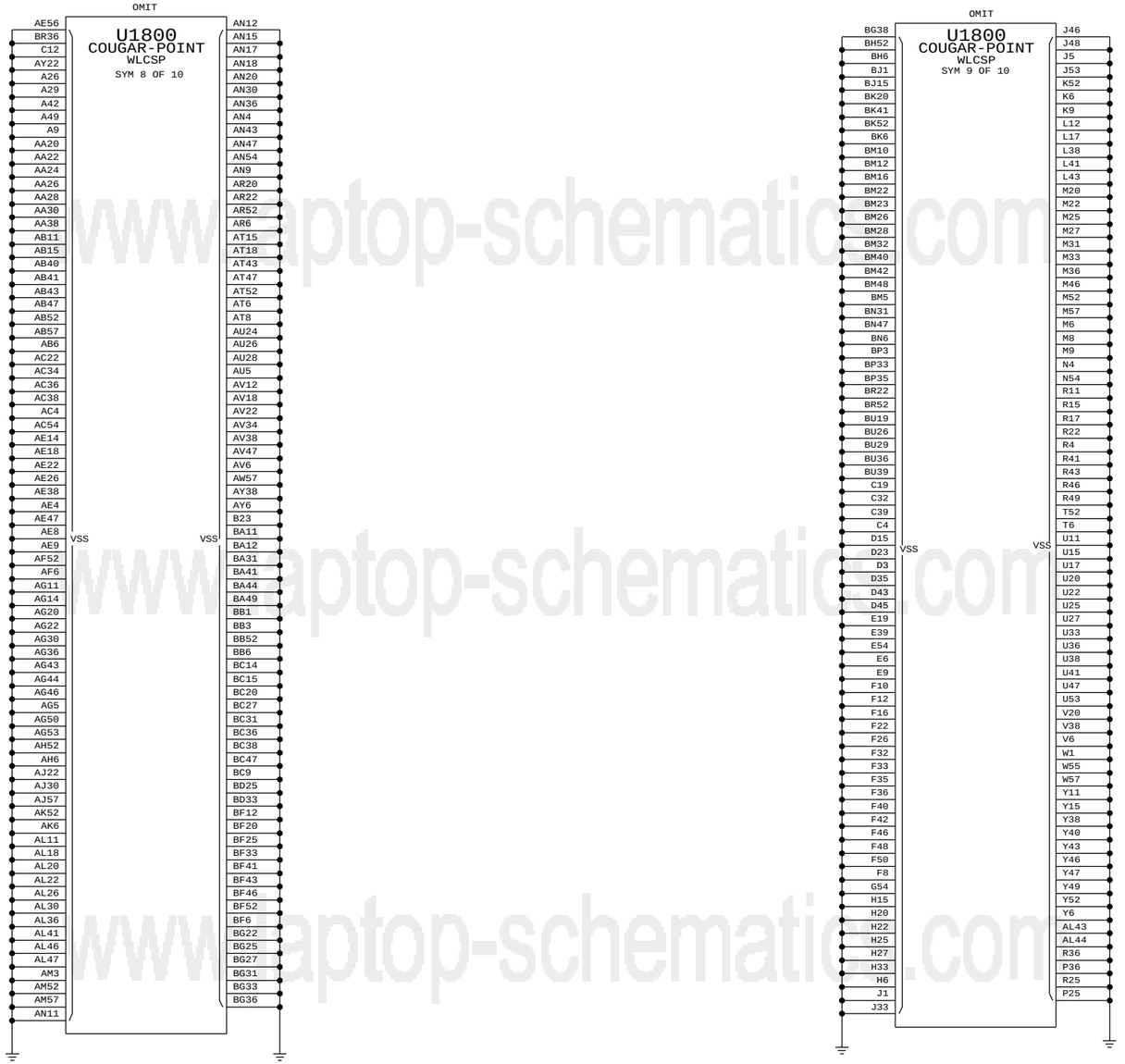
DRAWING NUMBER 051-8115 | SIZE D
REVISION 11.1.0
BRANCH
PAGE 22 OF 110
SHEET 22 OF 98



SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE

PCH GROUNDS

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REVISION 11.1.0

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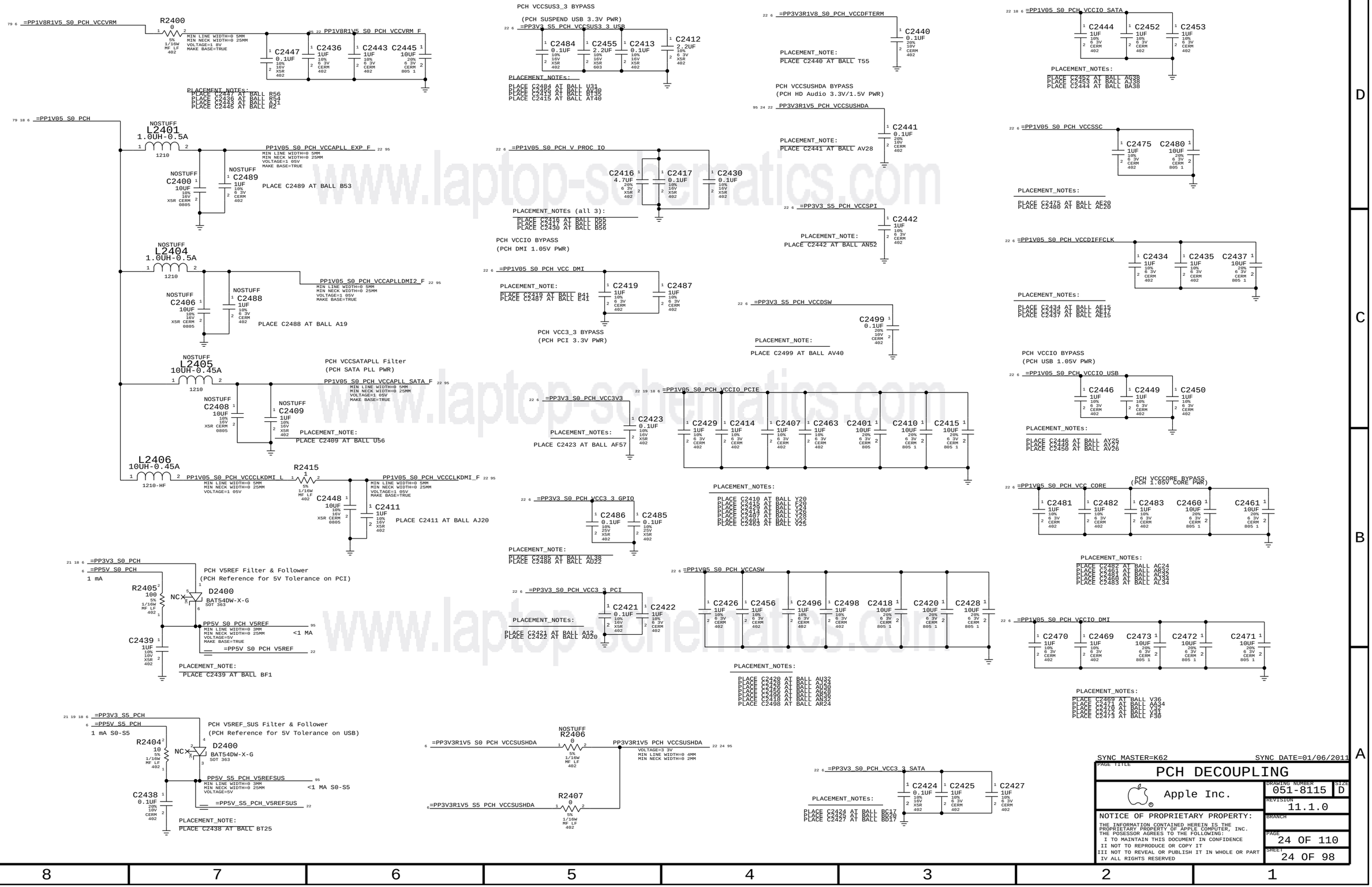
PAGE 23 OF 110

SHEET 23 OF 98



PROCESSOR MINI XDP

PLACEMENT_NOTE=Place R2501 close to R2500 to minimize stubs

XDP_CPU_BPM
RP2500
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_BPM_L<6>
XDP_BPM_L<7>

XDP_CPU_CFG
RP2501
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>

XDP R2500 1K — CPU_PWRGD — PLACEMENT NOTE=Place close to CPU
XDP R2502 0 — PM_PWRBTN_L — PLACEMENT NOTE=Place close to SMC
XDP R2501 1K — CPU_CFG<0> — PLACEMENT NOTE=Place close to CPU
XDP R2504 0 — PM_PGOOD_PVCORE_CPU

=PPVCCIO_S0_XDP

CRITICAL
XDP_CONN
J2500
DF40C-60DS-0.4V
F-ST-SM-HF
518S0774

XDP_CPU_PREQ_L
XDP_CPU_PRDY_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
CPU_CFG<10>
CPU_CFG<11>
XDP_OBSDATA_B<0>
XDP_OBSDATA_B<1>
XDP_OBSDATA_B<2>
XDP_OBSDATA_B<3>
XDP_CPU_PWRGD
XDP_CPU_PWRBTN_L
XDP_CPU_CFG<0>
XDP_VR_READY
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_CPU_TCK

OBSEN_A0 OBSEN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3 OBSEN_B0 OBSEN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3 PWRGD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 SDA SCL TCK1 TCK0

OBSEN_C0 OBSEN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3 OBSEN_D0 OBSEN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 TDO TRSTn TDI TMS XDP_PRESENT#

CPU_CFG<16> CPU_CFG<17> CPU_CFG<0> CPU_CFG<1> CPU_CFG<2> CPU_CFG<3> CPU_CFG<8> CPU_CFG<9> CPU_CFG<4> CPU_CFG<5> CPU_CFG<6> CPU_CFG<7>

XDP_CPU_CLK100M_P
XDP_CPU_CLK100M_N
XDPCPU_PLTRST_L
XDP_DBRESET_L
XDP_CPU_TDO
XDP_CPU_TRST_L
XDP_CPU_TDI
XDP_CPU_TMS

XDP C2500 0.1uF — XDP C2501 0.1uF

XDP R2515 0 — ITPXDP_CLK100M_P — PLACEMENT NOTE=Place close to R1841
XDP R2516 0 — ITPXDP_CLK100M_N — PLACEMENT NOTE=Place close to R1840
<- 1K SERIES R ON PCH SUPPORT P. 28

NOTE: XDP_DBRESET_L pulled-up to 3.3V on P. 28

XDP R2506 0 — XDP_DBRESET_L — PM_SYSRST_L — To Reset Button
PLACEMENT NOTE=Place close to SW2800

DESIGN NOTE:
ODT AVAILABLE ON JTAG

PLACEMENT NOTE:
PLACE TDO TERM NEAR SNB XDP CONN
XDP R2510 51 — PLACEMENT NOTE=Place close to J2500
XDP R2511 51 — PLACEMENT NOTE=Place close to CPU
XDP R2512 51 — PLACEMENT NOTE=Place close to CPU
XDP_CPU_TDO
XDP_CPU_TDI
XDP_CPU_TMS
XDP_CPU_TCK
XDP_CPU_TRST_L
XDP R2513 51 — PLACEMENT NOTE=Place close to CPU
XDP R2514 51 — PLACEMENT NOTE=Place close to CPU
PLACEMENT NOTE:
PLACE TCK/TDI/TMS/TRST* TERM NEAR CPU

PCH MINI XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J2550
DF40C-60DS-0.4V
F-ST-SM-HF
518S0774

TP_XDP_PCH_OBSFN_A<0>
TP_XDP_PCH_OBSFN_A<1>
XDP_PCH_AP_PWR_EN
XDP_PCH_USB_HUB_SOFT_RST_L
XDP_PCH_T29_DP_PORTA_PWR_EN
XDP_PCH_ENET_PWR_EN
TP_XDP_PCH_OBSFN_B<0>
TP_XDP_PCH_OBSFN_B<1>
XDP_PCH_T29_DP_PORTB_PWR_EN
XDP_PCH_SDCONN_CHANGE
PCH_GPIO10_OC6_L
PCH_GPIO14_OC7_L
XDP_PCH_S5_PWRGD
XDP_PCH_PWRBTN_L
TP_XDPPCH_HOOK2
TP_XDPPCH_HOOK3
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_PCH_TCK

OBSEN_A0 OBSEN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3 OBSEN_B0 OBSEN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3 PWRGD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 SDA SCL TCK1 TCK0

OBSEN_C0 OBSEN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3 OBSEN_D0 OBSEN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 TDO TRSTn TDI TMS XDP_PRESENT#

XDP_PCH_GPIO15
PCH_GPIO9_BMBUSY_L
XDP_PCH_ISOLATE_CPU_MEM_L
XDP_PCH_MXM_GOOD
XDP_PCH_DP_AUXCH_ISOL
PCH_GPIO19_SATA1GP
TP_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_D<1>
PCH_GPIO36_SATA2GP
XDP_PCH_JTAG_T29_TCK
XDP_PCH_AUD_IPHS_SWITCH_EN
PCH_GPIO49_SATA5GP
TP_XDP_PCH_HOOK4
TP_XDP_PCH_HOOK5
XDPPCH_PLTRST_L
XDP_DBRESET_L
XDP_PCH_TDO
TP_XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS

XDP C2580 0.1uF — XDP C2581 0.1uF

XDP R2582 0 — AP_PWR_EN — PLACEMENT NOTE=Place close to PCH — OC0#/GPIO59
XDP R2580 0 — USB_HUB_SOFT_RESET_L — PLACEMENT NOTE=Place close to PCH — OC1#/GPIO40
XDP R2583 0 — T29_DP_PORTA_PWR_EN — PLACEMENT NOTE=Place close to PCH — OC2#/GPIO41
XDP R2587 0 — ENET_PWR_EN — PLACEMENT NOTE=Place close to PCH — OC3#/GPIO42
XDP R2586 0 — T29_DP_PORTB_PWR_EN — PLACEMENT NOTE=Place close to PCH — OC4#/GPIO43
XDP R2581 0 — SDCONN_STATE_CHANGE — PLACEMENT NOTE=Place close to PCH — OC5#/GPIO9
XDP R2584 1K — =PP3V3_S5_XDP — PLACEMENT NOTE=Place close to J2550
XDP R2585 0 — PM_PWRBTN_L — PLACEMENT NOTE=Place close to SMC

XDP R2578 0 — PCH_GPIO15 — PLACEMENT NOTE=Place close to PCH — GPIO15
XDP R2576 0 — ISOLATE_CPU_MEM_L — PLACEMENT NOTE=Place close to PCH — MGPIO7/GPIO28
XDP R2577 0 — MXM_GOOD — PLACEMENT NOTE=Place close to PCH — GPIO39
XDP R2575 0 — DP_AUXCH_ISOL — PLACEMENT NOTE=Place close to PCH — SATA0GP/GPIO21
XDP R2573 0 — JTAG_T29_TCK — PLACEMENT NOTE=Place close to PCH — SATA3GP/GPIO37
XDP R2579 0 — AUD_IPHS_SWITCH_EN_PCH — PLACEMENT NOTE=Place close to PCH — SATA4GP/GPIO16
<- 1K SERIES R ON PCH SUPPORT P. 28

=PP3V3_S5_XDP

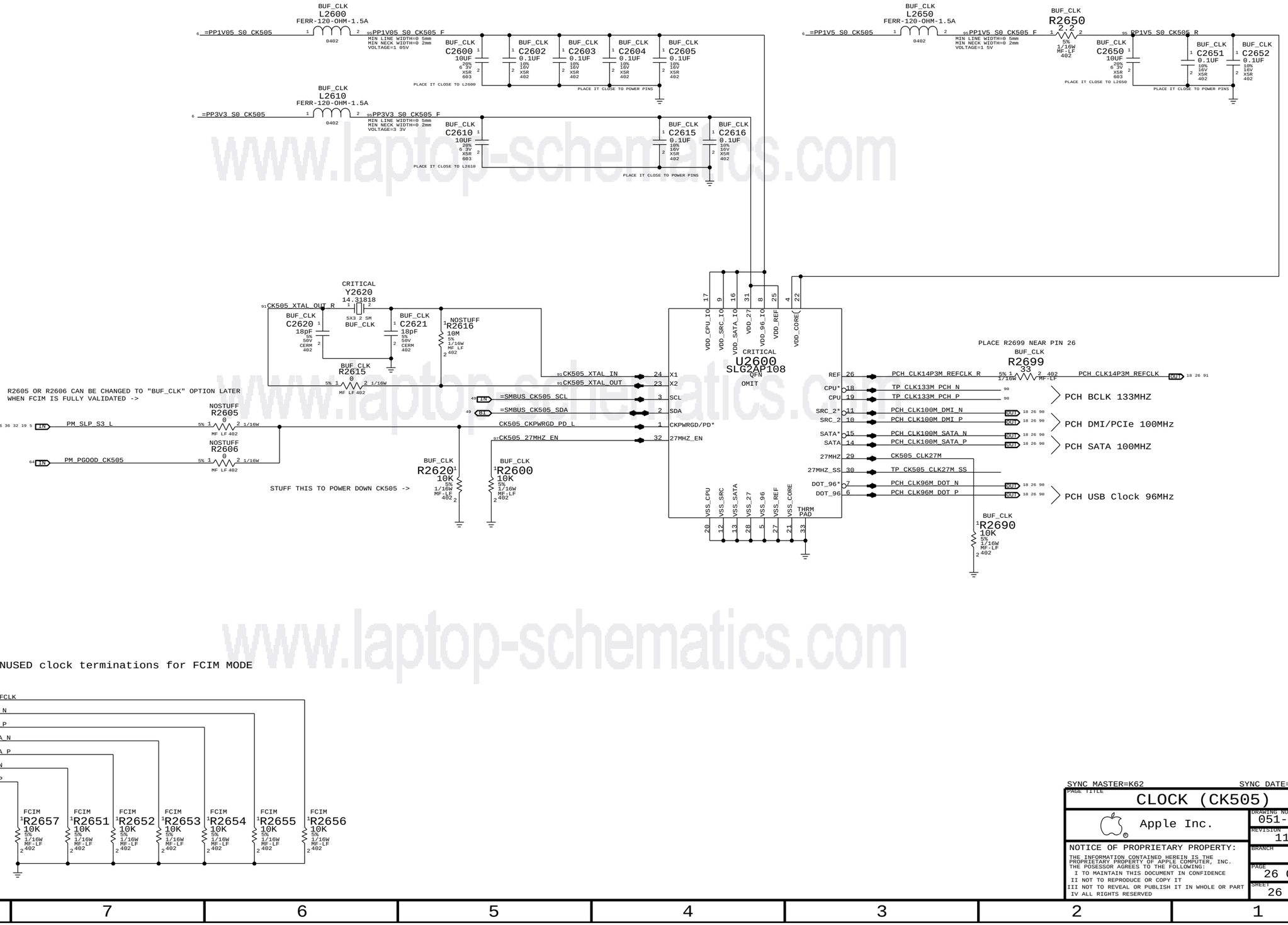
PLACEMENT NOTE:
PLACE TDO TERM NEAR PCH XDP CONN
XDP R2550 200 — PLACEMENT NOTE=Place close to J2550
XDP R2551 200 — PLACEMENT NOTE=Place close to PCH
XDP R2552 200 — PLACEMENT NOTE=Place close to PCH
XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS
XDP_PCH_TCK
XDP R2553 100 — PLACEMENT NOTE=Place close to PCH
XDP R2554 100 — PLACEMENT NOTE=Place close to PCH
XDP R2555 100 — PLACEMENT NOTE=Place close to PCH
XDP R2556 51 — PLACEMENT NOTE=Place close to PCH
This is to derive 1.05V SUS RAIL
PLACEMENT NOTE:
PLACE TCK/TDI/TMS/TRST* TERM NEAR PCH

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: CPU & PCH XDP

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 25 OF 110
SHEET: 25 OF 98



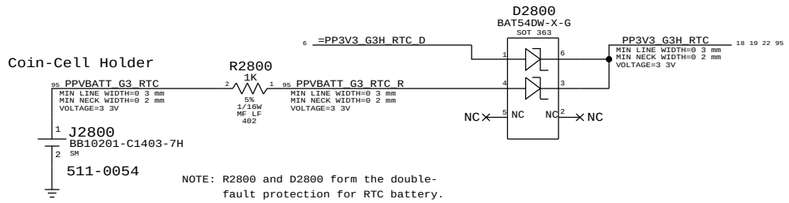
SYNC MASTER=K62 SYNC DATE=01/06/2011

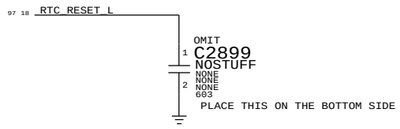
PAGE TITLE
CLOCK (CK505)

Apple Inc.

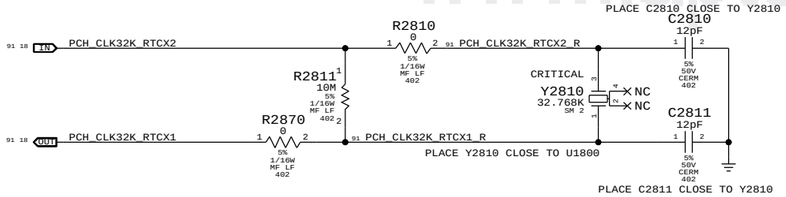
DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 26 OF 110
SHEET 26 OF 98

RTC Power Sources

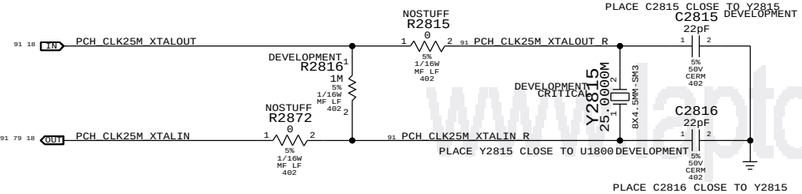




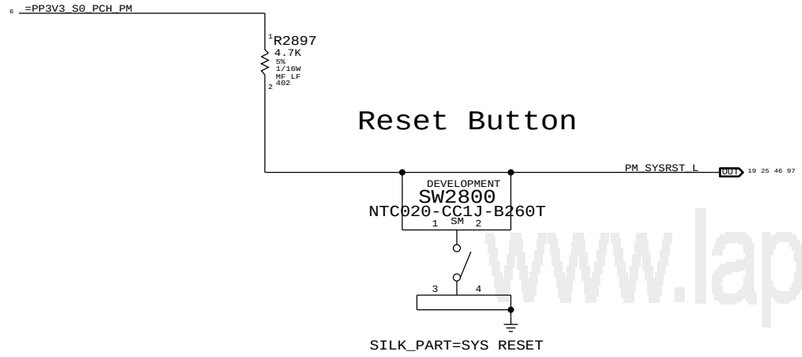
PCH RTC Crystal

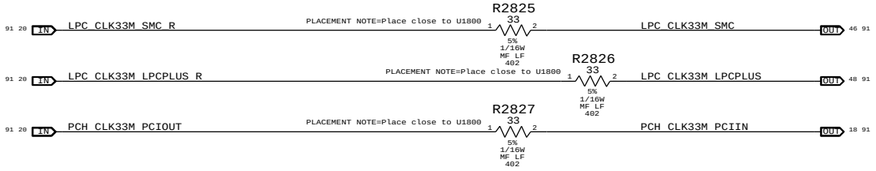


PCH 25MHZ CRYSTAL

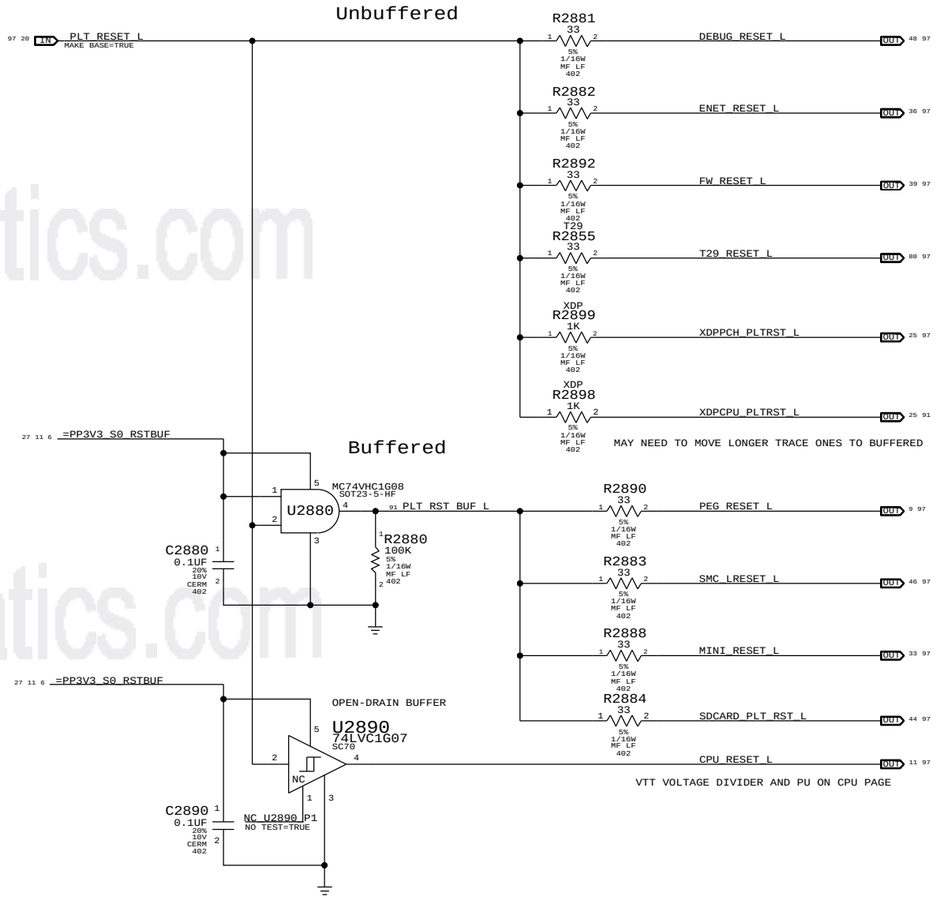


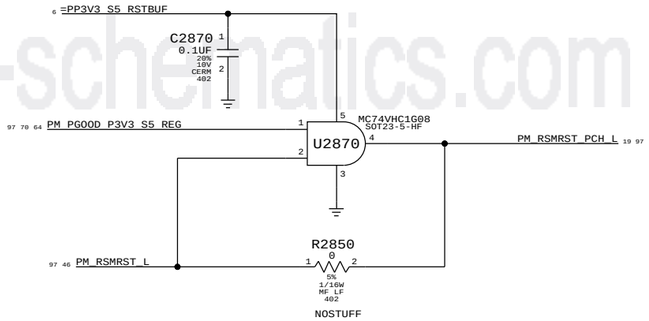
Reset Button





Platform Reset Connections





SMC PROVIDES RSMRST_L DE-ASSERTION DELAY UPON ENTRY TO S5
SMC PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON EXPECTED EXIT FROM S5
SMC MAY FORCE A RSMRST_L ASSERTION WITHOUT AN S5 POWER TRANSITION IN SOME ERROR CASES
PGOOD PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON AN UN-EXPECTED EXIT FROM S5 (POWER LOSS)

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: CHIPSET SUPPORT

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 28 OF 110
SHEET: 27 OF 98

DIMM VREFDQ

=PP1V5_S3_MEM_A
=PP3V3_S3_VREFMRGN
=I2C_VREFMRGN_A_SCL
=I2C_VREFMRGN_A_SDA
I2C_VREFMRGN_DIMMA_SCL
I2C_VREFMRGN_DIMMA_SDA
U2900 ISL90727WIE627ZTK SC-70 (353S2369)
VREFMRGN_A R2900 0 (SCL)
VREFMRGN_A R2901 0 (SDA)
VREFMRGN_A C2900 0.1UF
VREFMRGN_A R2902 12.1K
VREFMRGN_A R2903 12.1K
VREFMARGIN_DIMMA_DACOUT
I2C ADDR = 0X5C (WRITE)
I2C ADDR = 0X5D (READ)
=PP5V_S3_VREFMRGN
VREFMRGN_A R2909 10
PP5V_S3_VREFMRGN_A
VREFMRGN_A C2901 0.1UF
U2901 LM321 SOT23-5 (353S1961)
VREFMRGN_A R2904 2.2
VREFMRGN_A R2905 1K
VREFMRGN_A C2902 1UF
VREFMARGIN_DIMMA_OPFB
VREFMARGIN_DIMMA_DQ

PLACEMENT NOTE:
PLACE R2970, R2971 and C2950 close to DIMM PIN

=PP1V5_S3_MEM_A
R2970 1K
VREFMRGN_A R2958 0
PP0V75_S3_MEM_VREFDQ_A
R2971 1K
NOSTUFF C2950 0.1UF

=PP1V5_S3_MEM_B
=PP3V3_S3_VREFMRGN
=I2C_VREFMRGN_B_SCL
=I2C_VREFMRGN_B_SDA
I2C_VREFMRGN_DIMMB_SCL
I2C_VREFMRGN_DIMMB_SDA
U2910 ISL90728WIE627ZTK SC-70 (353S2370)
VREFMRGN_B R2910 0 (SCL)
VREFMRGN_B R2911 0 (SDA)
VREFMRGN_B C2910 0.1UF
VREFMRGN_B R2912 12.1K
VREFMRGN_B R2913 12.1K
VREFMARGIN_DIMMB_DACOUT
I2C ADDR = 0X7C (WRITE)
I2C ADDR = 0X7D (READ)
=PP5V_S3_VREFMRGN
VREFMRGN_B R2919 10
PP5V_S3_VREFMRGN_B
VREFMRGN_B C2911 0.1UF
U2911 LM321 SOT23-5 (353S1961)
VREFMRGN_B R2914 2.2
VREFMRGN_B R2915 1K
VREFMRGN_B C2912 1UF
VREFMARGIN_DIMMB_OPFB
VREFMARGIN_DIMMB_DQ

PLACEMENT NOTE:
PLACE R2975, R2976 and C2951 close to DIMM PIN

R2956 change to NOSTUFF if use VREFMARGIN_DIMMB_DQ to drive both VREFCA_A and VREFCA_B

=PP1V5_S3_MEM_B
R2975 1K
VREFMRGN_B R2956 0
PP0V75_S3_MEM_VREFDQ_B
R2976 1K
NOSTUFF C2951 0.1UF
PLACE IT CLOSE TO DIMM CONNECTOR PIN

DIMM VREFCA

=PP1V5_S3_MEM_A
R2988 1K
NOSTUFF R2995 0
VREFMARGIN_DIMMB_DQ
PP0V75_S3_MEM_VREFCA_A
R2989 1K
NOSTUFF C2921 0.1UF

PLACEMENT NOTE:
PLACE R2988, R2989 and C2921 close to DIMM PIN

=PP1V5_S3_MEM_B
R2978 1K
NOSTUFF R2996 0
VREFMARGIN_DIMMB_DQ
PP0V75_S3_MEM_VREFCA_B
R2979 1K
NOSTUFF C2991 0.1UF

PLACEMENT NOTE:
PLACE R2978, R2979 and C2991 close to DIMM PIN

CPU VREF

PLACEMENT NOTE:
PLACE R2968, R2969 and C2961 near CPU

=PP1V5_S0_CPU_MEM
R2968 100
R2969 100
C2961 0.1UF
CPU_DDR_VREF

PP0V75_S3_MEM_VREFDQ_A
NOSTUFF R2960 0
PP0V75_S3_MEM_VREFDQ_B

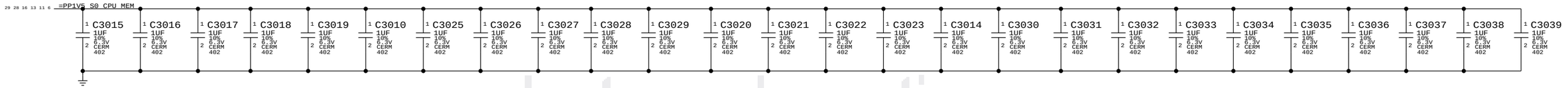
EMPTY ONE SET OF OP-AMP & POT WHEN R2960 IS STUFF

SYNC_MASTER=K62 SYNC_DATE=01/06/2013
PAGE TITLE: DDR3 VREF MARGINING
Apple Inc.
DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 29 OF 110
SHEET: 28 OF 98

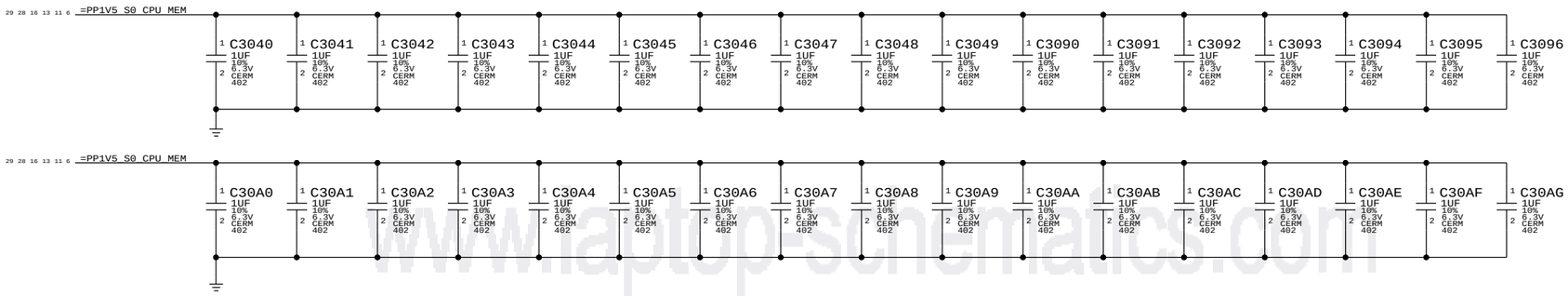
DIMM A (CLOSER TO CPU)

CAPS TO STITCH 1V5_CPU_MEM TO GND NEAR DIMM

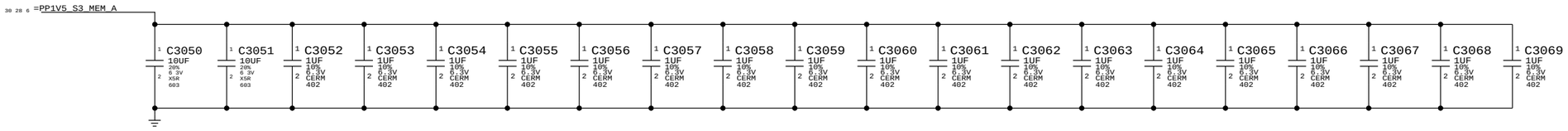
DIMM B (FURTHER FROM CPU)



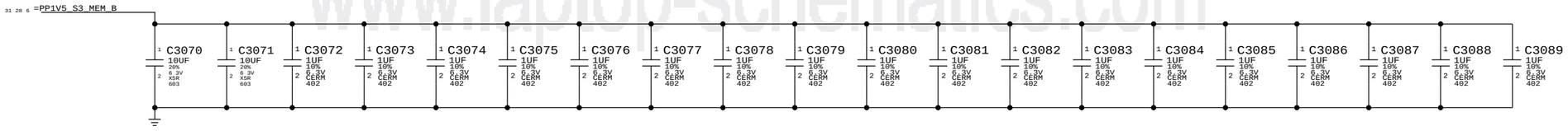
EXTRA DECOUPLING CAPS FOR 1V5_CPU_MEM RAIL



DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL A DIMM CONNECTOR



DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL B DIMM CONNECTOR



SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE: MEMORY CAPS

Apple Inc.

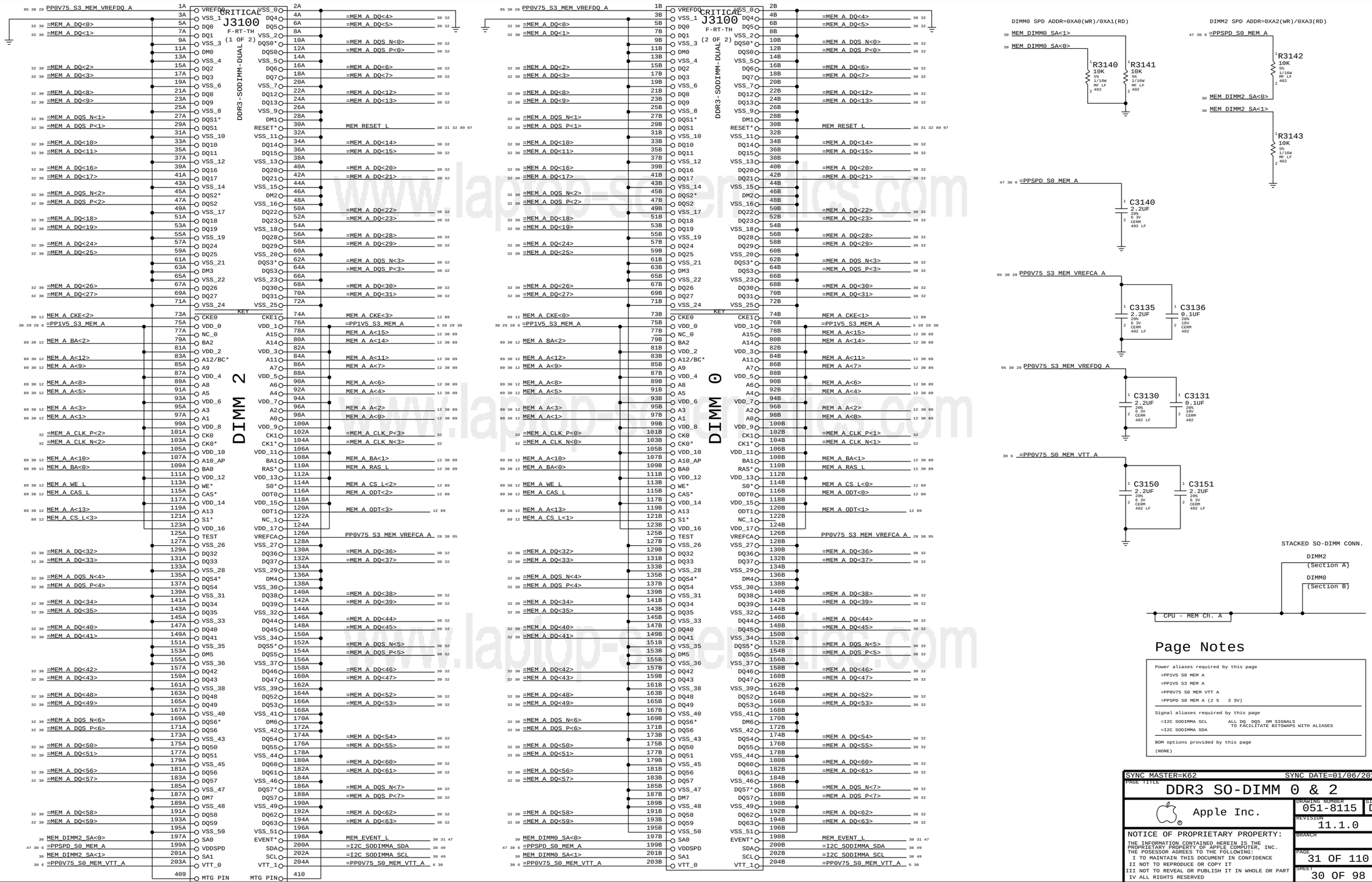
DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 30 OF 110

SHEET: 29 OF 98



Page Notes

Power aliases required by this page
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 3.3V)

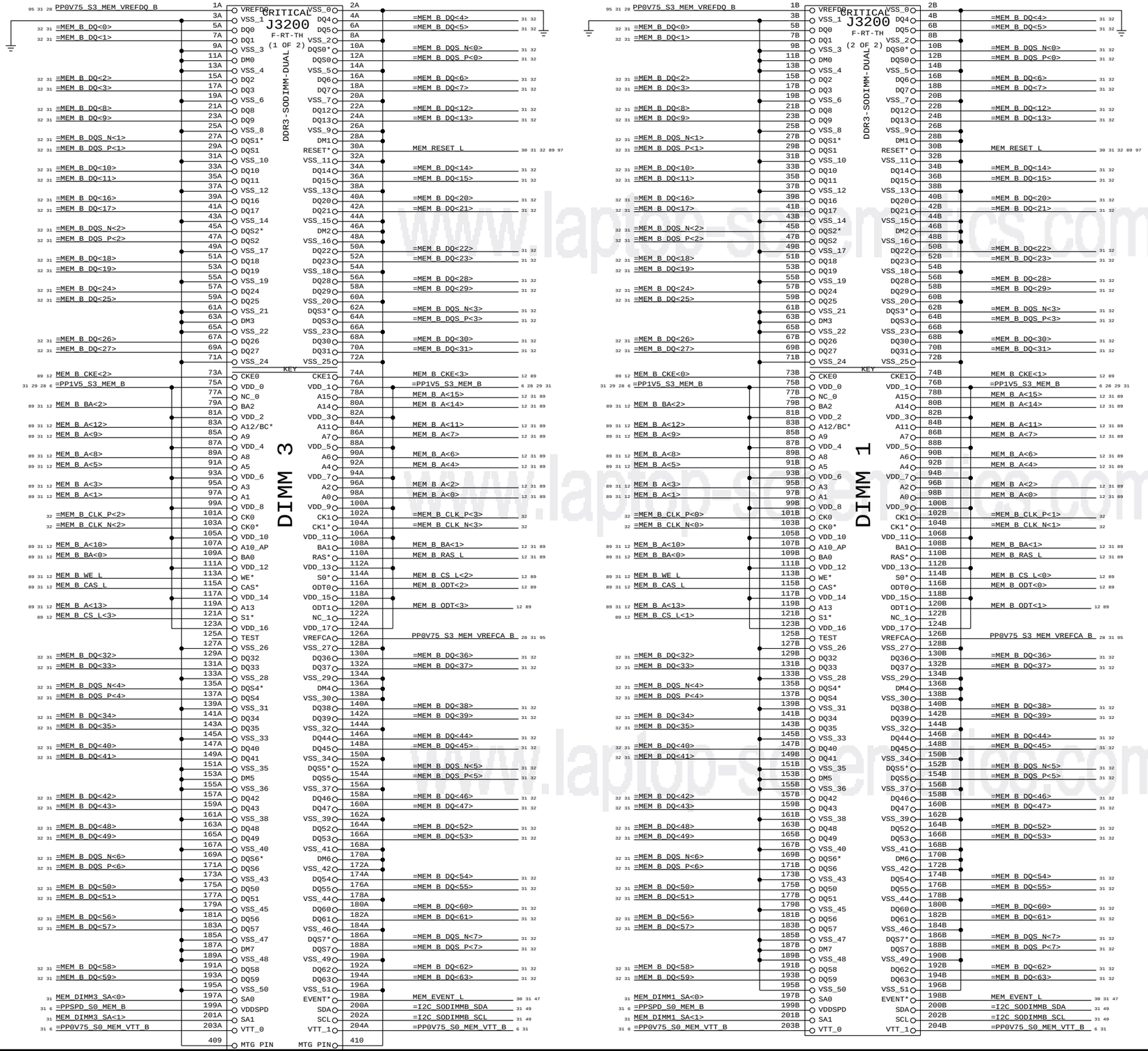
Signal aliases required by this page
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

ALL DQ, DQS, DM SIGNALS TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page

(NONE)

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE	DDR3 SO-DIMM 0 & 2
Apple Inc.	DRAWING NUMBER 051-8115 · SIZE D · REVISION 11.1.0 · BRANCH · PAGE 31 OF 110 · SHEET 30 OF 98



Page Notes

Power aliases required by this page
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2 5 3 3V)

Signal aliases required by this page
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

ALL DQ DQS DM SIGNALS TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page
(NONE)

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: DDR3 SO-DIMM 1 & 3

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 32 OF 110
SHEET: 31 OF 98

CPU CHANNEL A DQS 0 -> DIMM A DQS 7

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<7>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<7>
MEM_A_DQ<7>	MAKE_BASE=TRUE		=MEM_A_DQ<57>
MEM_A_DQ<6>	MAKE_BASE=TRUE		=MEM_A_DQ<56>
MEM_A_DQ<5>	MAKE_BASE=TRUE		=MEM_A_DQ<58>
MEM_A_DQ<4>	MAKE_BASE=TRUE		=MEM_A_DQ<59>
MEM_A_DQ<3>	MAKE_BASE=TRUE		=MEM_A_DQ<60>
MEM_A_DQ<2>	MAKE_BASE=TRUE		=MEM_A_DQ<61>
MEM_A_DQ<1>	MAKE_BASE=TRUE		=MEM_A_DQ<62>
MEM_A_DQ<0>	MAKE_BASE=TRUE		=MEM_A_DQ<63>

CPU CHANNEL A DQS 1 -> DIMM A DQS 6

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<6>
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<6>
MEM_A_DQ<15>	MAKE_BASE=TRUE		=MEM_A_DQ<49>
MEM_A_DQ<14>	MAKE_BASE=TRUE		=MEM_A_DQ<52>
MEM_A_DQ<13>	MAKE_BASE=TRUE		=MEM_A_DQ<51>
MEM_A_DQ<12>	MAKE_BASE=TRUE		=MEM_A_DQ<50>
MEM_A_DQ<11>	MAKE_BASE=TRUE		=MEM_A_DQ<48>
MEM_A_DQ<10>	MAKE_BASE=TRUE		=MEM_A_DQ<53>
MEM_A_DQ<9>	MAKE_BASE=TRUE		=MEM_A_DQ<55>
MEM_A_DQ<8>	MAKE_BASE=TRUE		=MEM_A_DQ<54>

CPU CHANNEL A DQS 2 -> DIMM A DQS 5

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<5>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<5>
MEM_A_DQ<23>	MAKE_BASE=TRUE		=MEM_A_DQ<40>
MEM_A_DQ<22>	MAKE_BASE=TRUE		=MEM_A_DQ<45>
MEM_A_DQ<21>	MAKE_BASE=TRUE		=MEM_A_DQ<46>
MEM_A_DQ<20>	MAKE_BASE=TRUE		=MEM_A_DQ<47>
MEM_A_DQ<19>	MAKE_BASE=TRUE		=MEM_A_DQ<41>
MEM_A_DQ<18>	MAKE_BASE=TRUE		=MEM_A_DQ<44>
MEM_A_DQ<17>	MAKE_BASE=TRUE		=MEM_A_DQ<43>
MEM_A_DQ<16>	MAKE_BASE=TRUE		=MEM_A_DQ<42>

CPU CHANNEL A DQS 3 -> DIMM A DQS 4

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<4>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<4>
MEM_A_DQ<31>	MAKE_BASE=TRUE		=MEM_A_DQ<37>
MEM_A_DQ<30>	MAKE_BASE=TRUE		=MEM_A_DQ<33>
MEM_A_DQ<29>	MAKE_BASE=TRUE		=MEM_A_DQ<35>
MEM_A_DQ<28>	MAKE_BASE=TRUE		=MEM_A_DQ<34>
MEM_A_DQ<27>	MAKE_BASE=TRUE		=MEM_A_DQ<36>
MEM_A_DQ<26>	MAKE_BASE=TRUE		=MEM_A_DQ<32>
MEM_A_DQ<25>	MAKE_BASE=TRUE		=MEM_A_DQ<38>
MEM_A_DQ<24>	MAKE_BASE=TRUE		=MEM_A_DQ<39>

CPU CHANNEL A DQS 4 -> DIMM A DQS 3

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<3>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<3>
MEM_A_DQ<39>	MAKE_BASE=TRUE		=MEM_A_DQ<28>
MEM_A_DQ<38>	MAKE_BASE=TRUE		=MEM_A_DQ<29>
MEM_A_DQ<37>	MAKE_BASE=TRUE		=MEM_A_DQ<27>
MEM_A_DQ<36>	MAKE_BASE=TRUE		=MEM_A_DQ<31>
MEM_A_DQ<35>	MAKE_BASE=TRUE		=MEM_A_DQ<25>
MEM_A_DQ<34>	MAKE_BASE=TRUE		=MEM_A_DQ<24>
MEM_A_DQ<33>	MAKE_BASE=TRUE		=MEM_A_DQ<26>
MEM_A_DQ<32>	MAKE_BASE=TRUE		=MEM_A_DQ<30>

CPU CHANNEL A DQS 5 -> DIMM A DQS 2

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<2>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<2>
MEM_A_DQ<47>	MAKE_BASE=TRUE		=MEM_A_DQ<17>
MEM_A_DQ<46>	MAKE_BASE=TRUE		=MEM_A_DQ<16>
MEM_A_DQ<45>	MAKE_BASE=TRUE		=MEM_A_DQ<22>
MEM_A_DQ<44>	MAKE_BASE=TRUE		=MEM_A_DQ<23>
MEM_A_DQ<43>	MAKE_BASE=TRUE		=MEM_A_DQ<21>
MEM_A_DQ<42>	MAKE_BASE=TRUE		=MEM_A_DQ<20>
MEM_A_DQ<41>	MAKE_BASE=TRUE		=MEM_A_DQ<18>
MEM_A_DQ<40>	MAKE_BASE=TRUE		=MEM_A_DQ<19>

CPU CHANNEL A DQS 6 -> DIMM A DQS 1

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<1>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<1>
MEM_A_DQ<55>	MAKE_BASE=TRUE		=MEM_A_DQ<12>
MEM_A_DQ<54>	MAKE_BASE=TRUE		=MEM_A_DQ<13>
MEM_A_DQ<53>	MAKE_BASE=TRUE		=MEM_A_DQ<10>
MEM_A_DQ<52>	MAKE_BASE=TRUE		=MEM_A_DQ<15>
MEM_A_DQ<51>	MAKE_BASE=TRUE		=MEM_A_DQ<8>
MEM_A_DQ<50>	MAKE_BASE=TRUE		=MEM_A_DQ<9>
MEM_A_DQ<49>	MAKE_BASE=TRUE		=MEM_A_DQ<11>
MEM_A_DQ<48>	MAKE_BASE=TRUE		=MEM_A_DQ<14>

CPU CHANNEL A DQS 7 -> DIMM A DQS 0

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<0>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<0>
MEM_A_DQ<63>	MAKE_BASE=TRUE		=MEM_A_DQ<5>
MEM_A_DQ<62>	MAKE_BASE=TRUE		=MEM_A_DQ<4>
MEM_A_DQ<61>	MAKE_BASE=TRUE		=MEM_A_DQ<3>
MEM_A_DQ<60>	MAKE_BASE=TRUE		=MEM_A_DQ<2>
MEM_A_DQ<59>	MAKE_BASE=TRUE		=MEM_A_DQ<1>
MEM_A_DQ<58>	MAKE_BASE=TRUE		=MEM_A_DQ<0>
MEM_A_DQ<57>	MAKE_BASE=TRUE		=MEM_A_DQ<7>
MEM_A_DQ<56>	MAKE_BASE=TRUE		=MEM_A_DQ<6>

CPU CHANNEL B DQS 0 -> DIMM B DQS 7

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<7>
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<7>
MEM_B_DQ<7>	MAKE_BASE=TRUE		=MEM_B_DQ<61>
MEM_B_DQ<6>	MAKE_BASE=TRUE		=MEM_B_DQ<60>
MEM_B_DQ<5>	MAKE_BASE=TRUE		=MEM_B_DQ<62>
MEM_B_DQ<4>	MAKE_BASE=TRUE		=MEM_B_DQ<63>
MEM_B_DQ<3>	MAKE_BASE=TRUE		=MEM_B_DQ<56>
MEM_B_DQ<2>	MAKE_BASE=TRUE		=MEM_B_DQ<57>
MEM_B_DQ<1>	MAKE_BASE=TRUE		=MEM_B_DQ<58>
MEM_B_DQ<0>	MAKE_BASE=TRUE		=MEM_B_DQ<59>

CPU CHANNEL B DQS 1 -> DIMM B DQS 6

MEM_B_DQS_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<6>
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<6>
MEM_B_DQ<15>	MAKE_BASE=TRUE		=MEM_B_DQ<51>
MEM_B_DQ<14>	MAKE_BASE=TRUE		=MEM_B_DQ<54>
MEM_B_DQ<13>	MAKE_BASE=TRUE		=MEM_B_DQ<53>
MEM_B_DQ<12>	MAKE_BASE=TRUE		=MEM_B_DQ<52>
MEM_B_DQ<11>	MAKE_BASE=TRUE		=MEM_B_DQ<48>
MEM_B_DQ<10>	MAKE_BASE=TRUE		=MEM_B_DQ<49>
MEM_B_DQ<9>	MAKE_BASE=TRUE		=MEM_B_DQ<50>
MEM_B_DQ<8>	MAKE_BASE=TRUE		=MEM_B_DQ<55>

CPU CHANNEL B DQS 2 -> DIMM B DQS 5

MEM_B_DQS_N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<5>
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<5>
MEM_B_DQ<23>	MAKE_BASE=TRUE		=MEM_B_DQ<45>
MEM_B_DQ<22>	MAKE_BASE=TRUE		=MEM_B_DQ<40>
MEM_B_DQ<21>	MAKE_BASE=TRUE		=MEM_B_DQ<42>
MEM_B_DQ<20>	MAKE_BASE=TRUE		=MEM_B_DQ<47>
MEM_B_DQ<19>	MAKE_BASE=TRUE		=MEM_B_DQ<44>
MEM_B_DQ<18>	MAKE_BASE=TRUE		=MEM_B_DQ<41>
MEM_B_DQ<17>	MAKE_BASE=TRUE		=MEM_B_DQ<46>
MEM_B_DQ<16>	MAKE_BASE=TRUE		=MEM_B_DQ<43>

CPU CHANNEL B DQS 3 -> DIMM B DQS 4

MEM_B_DQS_N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<4>
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<4>
MEM_B_DQ<31>	MAKE_BASE=TRUE		=MEM_B_DQ<32>
MEM_B_DQ<30>	MAKE_BASE=TRUE		=MEM_B_DQ<39>
MEM_B_DQ<29>	MAKE_BASE=TRUE		=MEM_B_DQ<37>
MEM_B_DQ<28>	MAKE_BASE=TRUE		=MEM_B_DQ<38>
MEM_B_DQ<27>	MAKE_BASE=TRUE		=MEM_B_DQ<35>
MEM_B_DQ<26>	MAKE_BASE=TRUE		=MEM_B_DQ<34>
MEM_B_DQ<25>	MAKE_BASE=TRUE		=MEM_B_DQ<36>
MEM_B_DQ<24>	MAKE_BASE=TRUE		=MEM_B_DQ<33>

CPU CHANNEL B DQS 4 -> DIMM B DQS 3

MEM_B_DQS_N<4>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<3>
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<3>
MEM_B_DQ<39>	MAKE_BASE=TRUE		=MEM_B_DQ<28>
MEM_B_DQ<38>	MAKE_BASE=TRUE		=MEM_B_DQ<24>
MEM_B_DQ<37>	MAKE_BASE=TRUE		=MEM_B_DQ<31>
MEM_B_DQ<36>	MAKE_BASE=TRUE		=MEM_B_DQ<30>
MEM_B_DQ<35>	MAKE_BASE=TRUE		=MEM_B_DQ<29>
MEM_B_DQ<34>	MAKE_BASE=TRUE		=MEM_B_DQ<25>
MEM_B_DQ<33>	MAKE_BASE=TRUE		=MEM_B_DQ<27>
MEM_B_DQ<32>	MAKE_BASE=TRUE		=MEM_B_DQ<26>

CPU CHANNEL B DQS 5 -> DIMM B DQS 2

MEM_B_DQS_N<5>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<2>
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<2>
MEM_B_DQ<47>	MAKE_BASE=TRUE		=MEM_B_DQ<18>
MEM_B_DQ<46>	MAKE_BASE=TRUE		=MEM_B_DQ<20>
MEM_B_DQ<45>	MAKE_BASE=TRUE		=MEM_B_DQ<23>
MEM_B_DQ<44>	MAKE_BASE=TRUE		=MEM_B_DQ<22>
MEM_B_DQ<43>	MAKE_BASE=TRUE		=MEM_B_DQ<19>
MEM_B_DQ<42>	MAKE_BASE=TRUE		=MEM_B_DQ<21>
MEM_B_DQ<41>	MAKE_BASE=TRUE		=MEM_B_DQ<17>
MEM_B_DQ<40>	MAKE_BASE=TRUE		=MEM_B_DQ<16>

CPU CHANNEL B DQS 6 -> DIMM B DQS 1

MEM_B_DQS_N<6>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<1>
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<1>
MEM_B_DQ<55>	MAKE_BASE=TRUE		=MEM_B_DQ<8>
MEM_B_DQ<54>	MAKE_BASE=TRUE		=MEM_B_DQ<14>
MEM_B_DQ<53>	MAKE_BASE=TRUE		=MEM_B_DQ<10>
MEM_B_DQ<52>	MAKE_BASE=TRUE		=MEM_B_DQ<11>
MEM_B_DQ<51>	MAKE_BASE=TRUE		=MEM_B_DQ<9>
MEM_B_DQ<50>	MAKE_BASE=TRUE		=MEM_B_DQ<15>
MEM_B_DQ<49>	MAKE_BASE=TRUE		=MEM_B_DQ<12>
MEM_B_DQ<48>	MAKE_BASE=TRUE		=MEM_B_DQ<13>

CPU CHANNEL B DQS 7 -> DIMM B DQS 0

MEM_B_DQS_N<7>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<0>
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<0>
MEM_B_DQ<63>	MAKE_BASE=TRUE		=MEM_B_DQ<2>
MEM_B_DQ<62>	MAKE_BASE=TRUE		=MEM_B_DQ<1>
MEM_B_DQ<61>	MAKE_BASE=TRUE		=MEM_B_DQ<3>
MEM_B_DQ<60>	MAKE_BASE=TRUE		=MEM_B_DQ<7>
MEM_B_DQ<59>	MAKE_BASE=TRUE		=MEM_B_DQ<4>
MEM_B_DQ<58>	MAKE_BASE=TRUE		=MEM_B_DQ<5>
MEM_B_DQ<57>	MAKE_BASE=TRUE		=MEM_B_DQ<6>
MEM_B_DQ<56>	MAKE_BASE=TRUE		=MEM_B_DQ<0>

DDR3 RESET SUPPORT

SNB? CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0

S	R	CLK	D	Q	QB
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	POSEDGE	L	L	H
H	H	POSEDGE	H	H	L

=PP3V3_S3_MEMRESET
R3350 20K 5% 1/16W MF-LF 402
=PP5V_S3_MEMRESET
R3351 20K 5% 1/16W MF-LF 402
R3352 20K 5% 1/16W MF-LF 402
ISOLATE_CPU_MEM
Q3306 2N7002DW-X-G SOT 363
ISOLATE_CPU_MEM_L_R1
CPU_MEM_RESET_L
=PP1V5_S3_MEMRESET
NOSTUFF R3355 0 5% 1/16W MF-LF 402
C3353 0.0022UF 20% 16V CERM 402
R3353 20K 5% 1/16W MF-LF 402
Q3304 2N7002 SOT23-HF1
MEM_RESET_L
ISOLATE_CPU_MEM_5V_L

=PP3V3_S5_MEMRESET
MEM_RESET_HW
C3300 0.1UF 20% 16V CERM 402
U3300 74LVC74ABQ DHVQFN
PM_SLP_S4_L
PM_SYS_PWRGD
=PP3V3_S3_MEMRESET
PM_SLP_S4_D_L
=PP3V3_S3_MEMRESET
CPU_MEM_RESET3V3_L
PM_SLP_S3_L
THRM GND_PAD
PM_SLP_S4_D_L
TP_PM_SLP_S4_D
ISOLATE_CPU_MEMHW_L
TP_ISOLATE_CPU
R3385 0 5% 1/16W MF-LF 402
NOSTUFF R3383 0 5% 1/16W MF-LF 402
ISOLATE_CPU_MEM_L_R1
CPU_MEM_RESET_L
NOSTUFF R3380 10K 5% 1/16W MF-LF 402
CPU_MEM_RESET_R_L

=PP3V3_S5_MEMRESET
MEM_RESET_HW R3381 10K 5% 1/16W MF-LF 402
MEM_RESET_HW R3382 10K 5% 1/16W MF-LF 402
CPU_MEM_RESET3V3
CPU_MEM_RESET3V3_L
MEM_RESET_HW
MEM_RESET_HW Q3360 2N3904 SOT23-HF
MEM_RESET_HW Q3350 2N7002 SOT23-HF1

=PP3V3_S5_MEMRESET
NOSTUFF C3390 0.1UF 20% 16V CERM 402
ALL_SYS_PWRGD_R
NOSTUFF R3390 0 5% 1/16W MF-LF 402
NOSTUFF R3391 0 5% 1/16W MF-LF 402
PM_EN_DDRVTT_S0_REG
DDRSYS_EN
U3390 NOSTUFF MC74VHC1G08 SOT23-5-HF
SLP_S3_CTL_L
NOSTUFF R3393 0 5% 1/16W MF-LF 402
R3394 0 5% 1/16W MF-LF 402
PM_SLP_S3_L
PM_SLP_S3_5V_R2

=PP5V_S3_MEMRESET
R3387 20K 5% 1/16W MF-LF 402
R3384 20K 5% 1/16W MF-LF 402
PM_SLP_S3_5V
PM_SLP_S3_5V_L
Q3370 2N7002DW-X-G SOT 363
Q3370 2N7002DW-X-G SOT 363

NOSTUFF R3386 0 5% 1/16W MF-LF 402
Q3375 FDMC8296 POWER33
=PP0V75_S0_MEM_VTT_S0FET
PPVTT_S0_DDR_FET
R3340 100K 5% 1/16W MF-LF 402
PM_SLP_S3_5V_L
R3388 10 5% 1/16W MF-LF 402
VTT_R
Q3380 2N7002 SOT23-HF1
PM_SLP_S3_5V

MEMORY CLOCK ALIASING

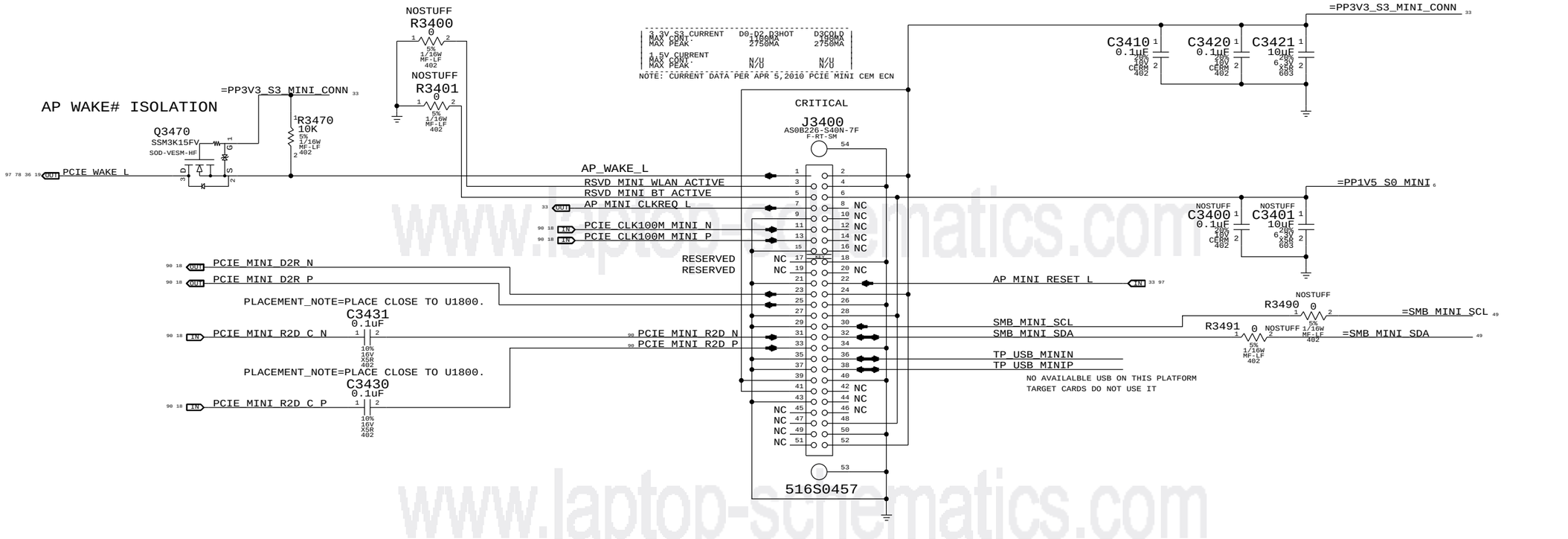
MEM_A_CLK_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_P<0>
MEM_A_CLK_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_N<0>
MEM_A_CLK_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_P<1>
MEM_A_CLK_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_N<1>
MEM_A_CLK_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_P<2>
MEM_A_CLK_N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_N<2>
MEM_A_CLK_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_P<3>
MEM_A_CLK_N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_N<3>
MEM_B_CLK_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_P<0>
MEM_B_CLK_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_N<0>
MEM_B_CLK_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_P<1>
MEM_B_CLK_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_N<1>
MEM_B_CLK_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_P<2>
MEM_B_CLK_N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_N<2>
MEM_B_CLK_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_P<3>
MEM_B_CLK_N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_N<3>

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: DDR3 SUPPORT AND BITSWAPS

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 33 OF 110
SHEET: 32 OF 98



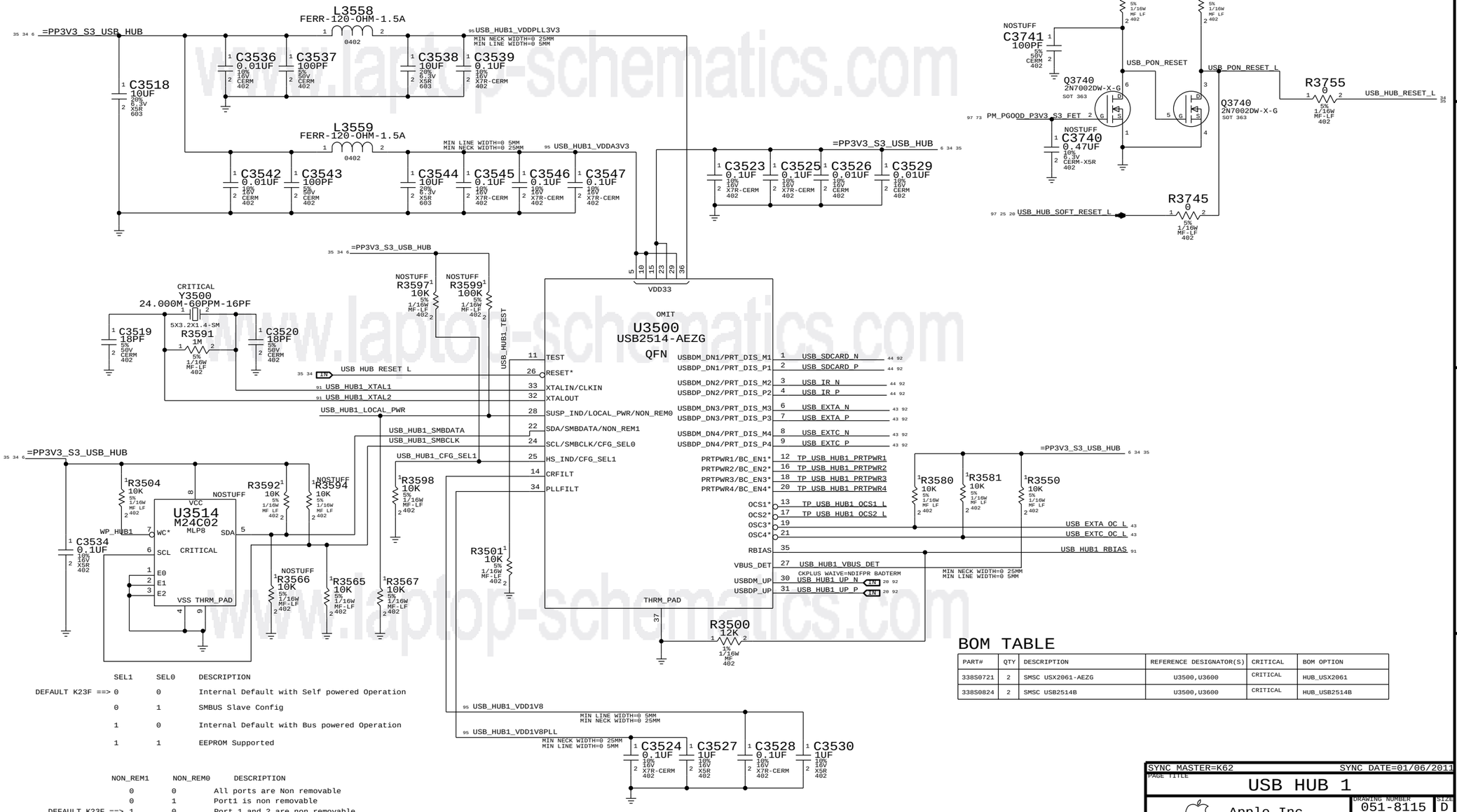
SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
PCI-E Wireless Connector

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 34 OF 110
SHEET 33 OF 98

USB HUB-1



SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==> 0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are Non removable
0	1	Port1 is non removable
DEFAULT K23F ==> 1	0	Port 1 and 2 are non removable
1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0721	2	SMSC USX2061-AEZG	U3500,U3600	CRITICAL	HUB_USX2061
338S0824	2	SMSC USB2514B	U3500,U3600	CRITICAL	HUB_USB2514B

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE

USB HUB 1

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DRAWING NUMBER 051-8115 SIZE D

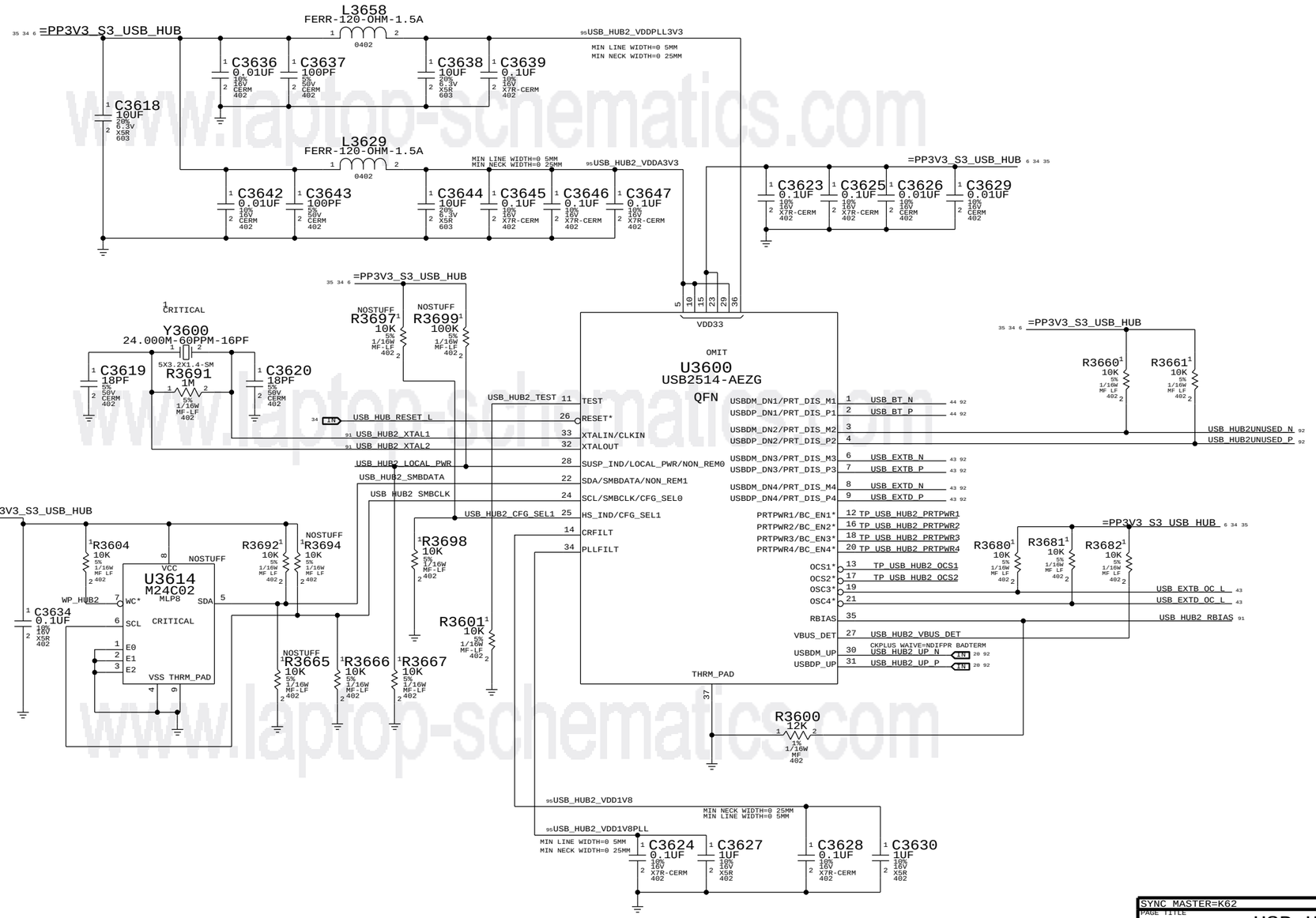
REVISION 11.1.0

BRANCH

PAGE 35 OF 110

SHEET 34 OF 98

USB HUB-2



SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE: USB HUB 2

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DRAWING NUMBER: 051-8115 SIZE: D

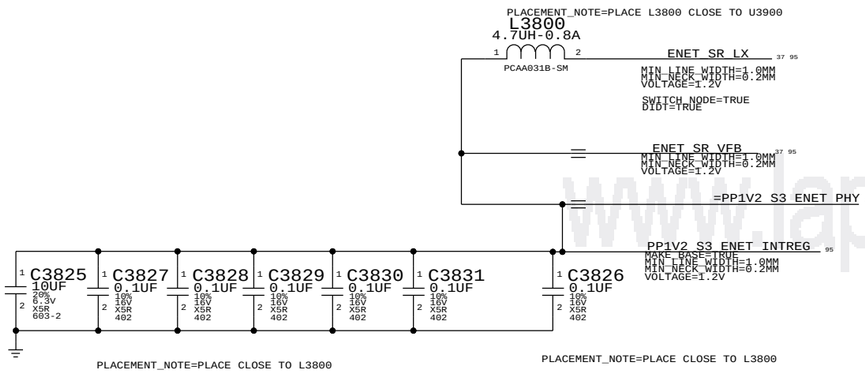
REVISION: 11.1.0

BRANCH:

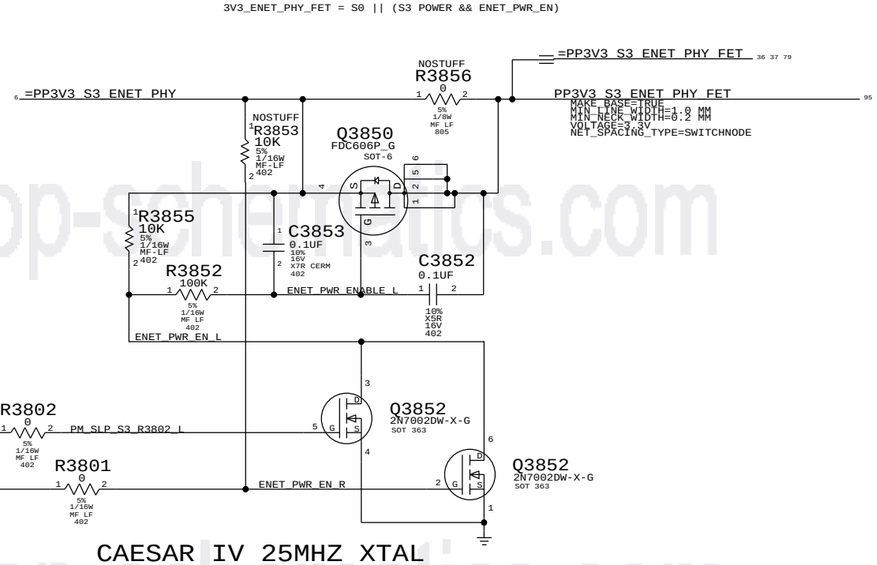
PAGE: 36 OF 110

SHEET: 35 OF 98

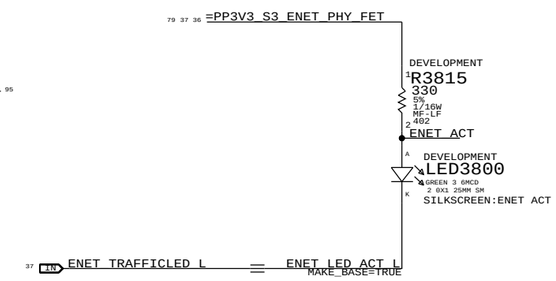
CAESAR IV 1.2V INT.VR CMPTS



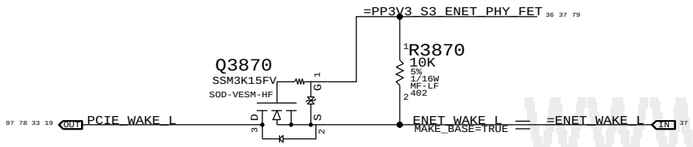
CAESAR IV POWER ENABLE CIRCUIT



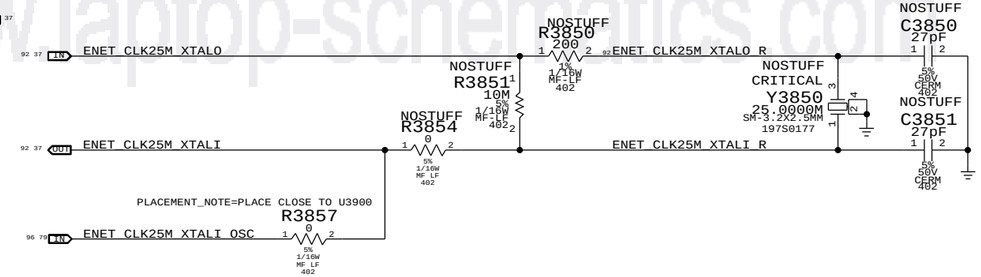
CAESAR IV ACTIVITY LED



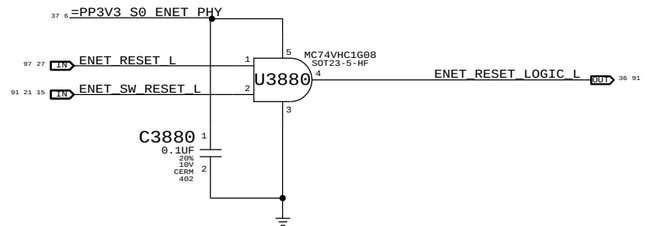
CAESAR IV WAKE# ISOLATION



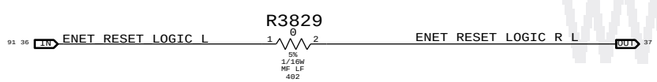
CAESAR IV 25MHZ XTAL



CAESAR IV SW RESET GATING

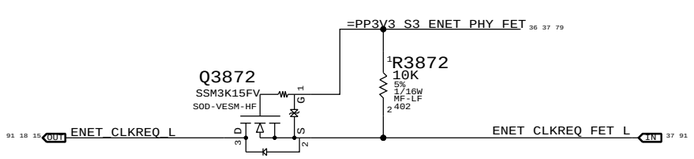


CAESAR IV RESET CONNECTION



CAESAR IV STRAPS (NONE)

CAESAR IV CLKREQ ISOLATION



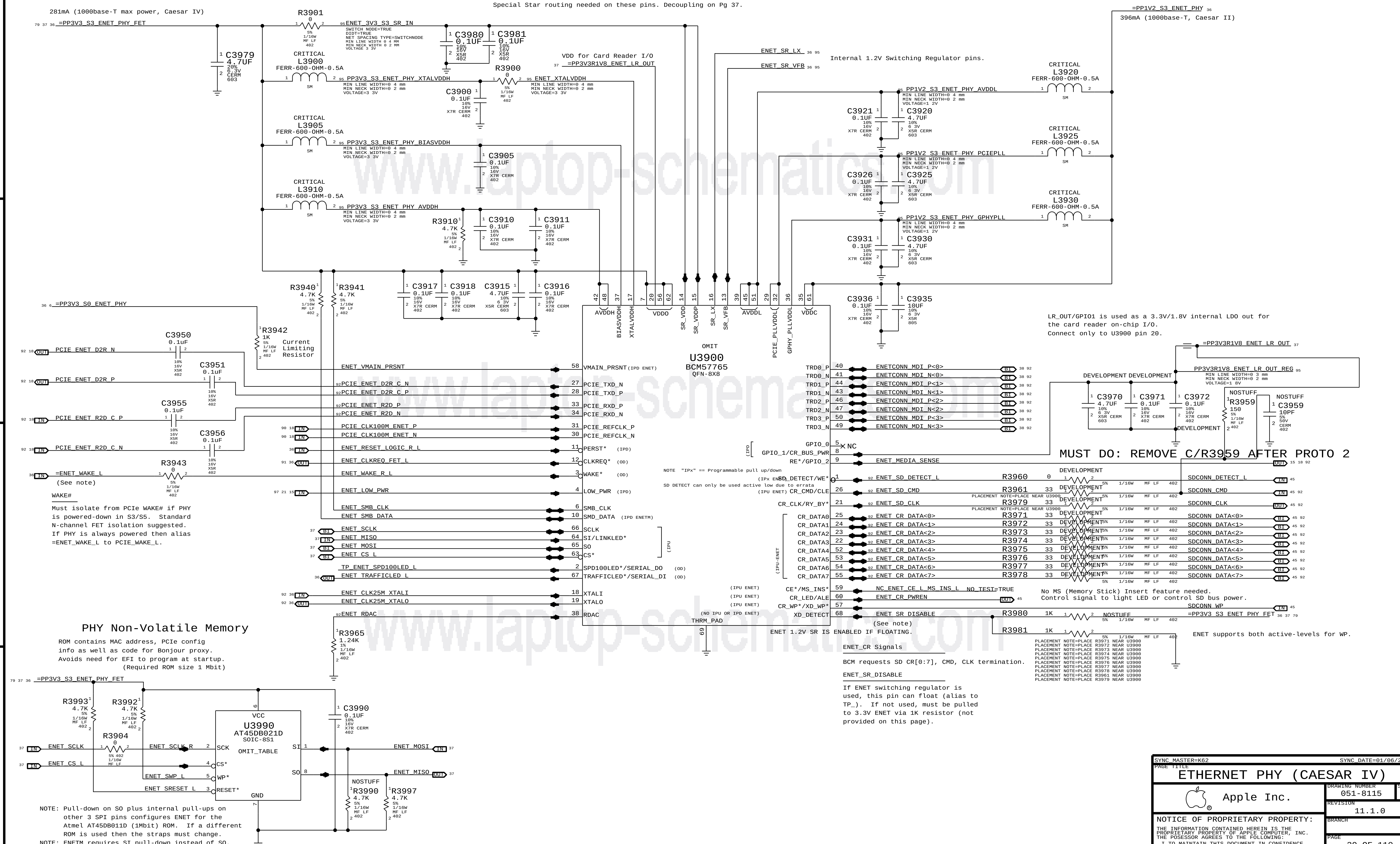
SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
CAESAR IV SUPPORT

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 38 OF 110
SHEET 36 OF 98

BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.



WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup. (Required ROM size 1 Mbit)

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin can float (alias to TP_). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: ETHERNET PHY (CAESAR IV)

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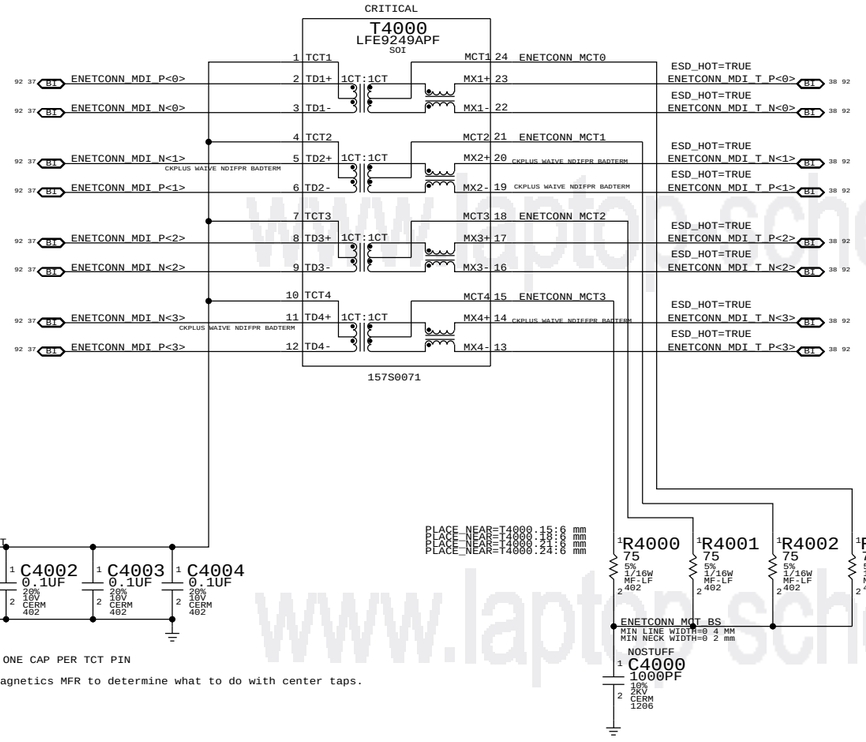
DRAWING NUMBER 051-8115 SIZE D

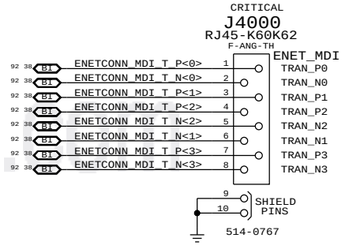
REVISION 11.1.0

NOTICE OF PROPRIETARY PROPERTY:

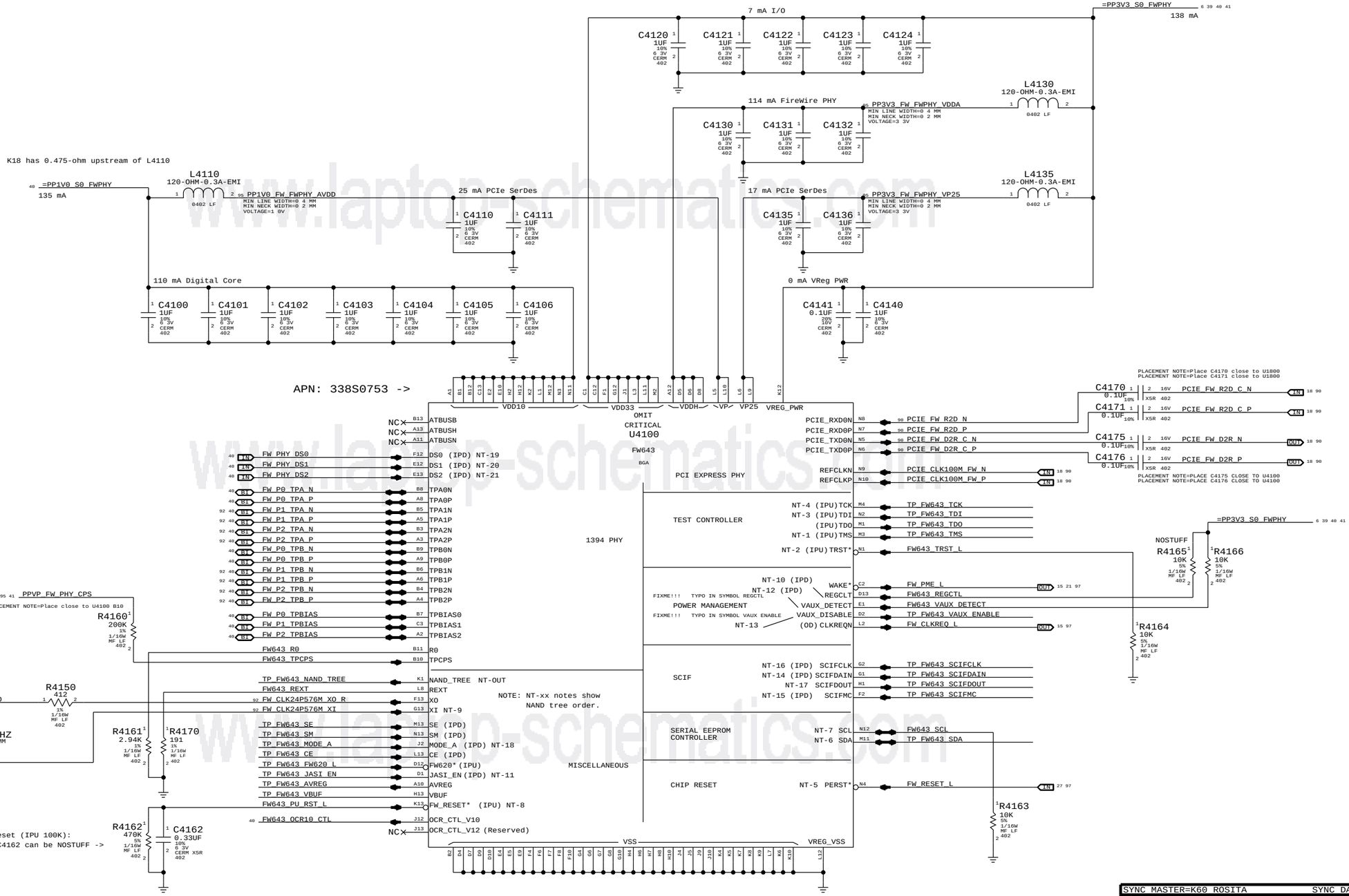
THIS PAGE DIFFERENT BETWEEN K60 and K62.



NO PAIR AND PIN POLARITY SWAPS



SYNC MASTER=K60 MARK	SYNC DATE=01/06/2011
PAGE TITLE: Ethernet Connector	
Apple Inc.	DRAWING NUMBER: 051-8115 SIZE: D
	REVISION: 11.1.0
	BRANCH:
	PAGE: 40 OF 110
	SHEET: 38 OF 98



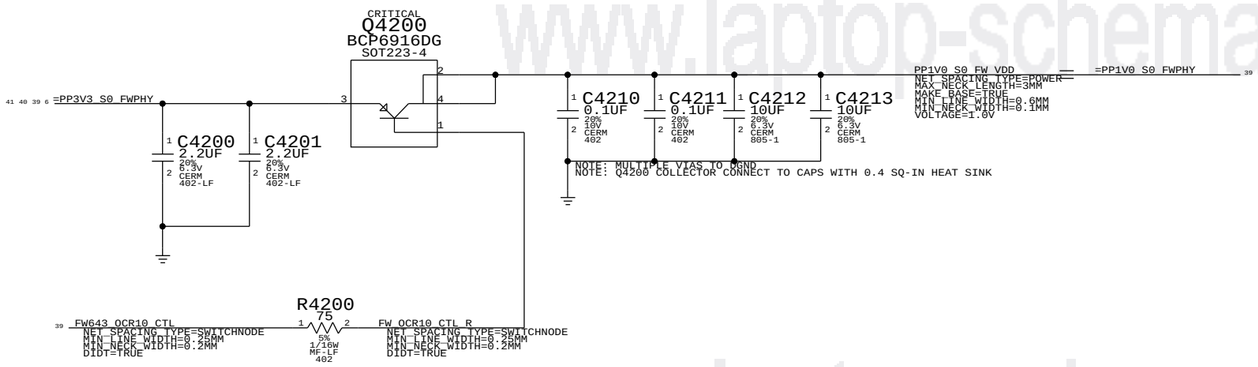
SYNC_MASTER=K60_ROSITA SYNC_DATE=01/06/2011

PAGE TITLE
FireWire LLC/PHY (FW643)

Apple Inc.

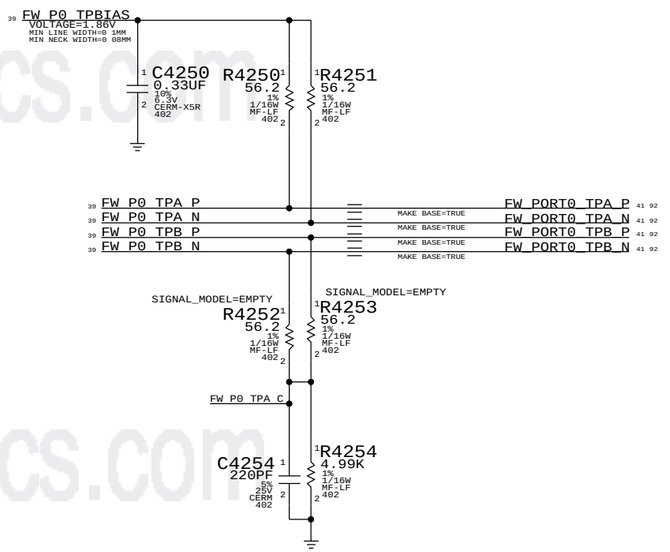
DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 41 OF 110
SHEET 39 OF 98

FW643 1.0V GENERATION

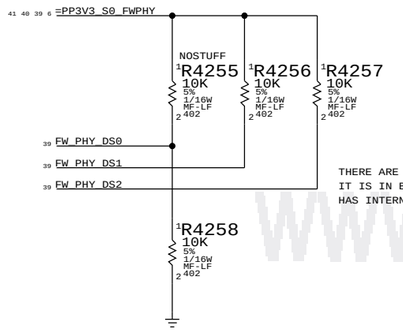


Termination

Place close to FireWire PHY



1394 PHY DATA/STROBE OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

2ND & 3RD TPA/TPB PAIR UNUSED

39	FW_P1_TPBIAS	NC_FW_PORT1_TPBIAS	MAKE_BASE=TRUE, NO TEST=TRUE
92 39	FW_P1_TPA_P	NC_FW_PORT1_TPA_P	MAKE_BASE=TRUE, NO TEST=TRUE
92 39	FW_P1_TPA_N	NC_FW_PORT1_TPA_N	MAKE_BASE=TRUE, NO TEST=TRUE
92 39	FW_P1_TPB_P	NC_FW_PORT1_TPB_P	MAKE_BASE=TRUE, NO TEST=TRUE
92 39	FW_P1_TPB_N	NC_FW_PORT1_TPB_N	MAKE_BASE=TRUE, NO TEST=TRUE
39	FW_P2_TPBIAS	NC_FW_PORT2_TPBIAS	MAKE_BASE=TRUE, NO TEST=TRUE
92 39	FW_P2_TPA_P	NC_FW_PORT2_TPA_P	MAKE_BASE=TRUE, NO TEST=TRUE
92 39	FW_P2_TPA_N	NC_FW_PORT2_TPA_N	MAKE_BASE=TRUE, NO TEST=TRUE
92 39	FW_P2_TPB_P	NC_FW_PORT2_TPB_P	MAKE_BASE=TRUE, NO TEST=TRUE
92 39	FW_P2_TPB_N	NC_FW_PORT2_TPB_N	MAKE_BASE=TRUE, NO TEST=TRUE

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: FireWire: 1394B MISC

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DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 42 OF 110

SHEET: 40 OF 98

12 VOLTS
14 WATTS MAX PER PORT

POUR COPPER TO SINK HEAT
CRITICAL
Q4350
FDC610PZ
SSOT6

41 6 =PP12V_S0_FW
95 P12V_S0_VG_OK
MIN LINE WIDTH=1 7MM
MIN NECK WIDTH=0 5MM
VOLTAGE=12V

R4351 1K 5% 1/16W MF LF 402
NOSTUFF C4351 0.001UF 20% 50V CERM 402
FWPWR_ON_L
R4355 1K 5% 1/16W MF LF 402
FWPWR_EN_L
Q4351 2N7002 SOT23-HF

R4300 0.33 5% 1W MF 2512
95 P12V_FW_R
MIN LINE WIDTH=1 7MM
MIN NECK WIDTH=0 5MM
VOLTAGE=12V

INRUSH RESETABLE PTC
CRITICAL
F4301
0.3AMP-60V
SMD030F-SM

POUR COPPER TO SINK HEAT
CRITICAL
Q4300
FDC610PZ
SSOT6

Q4301
MMBT2907AXG
60V-600MA
SOT23

D4301
5.1V
MMBZ5231BXG
SOT23

R4352 51.1K 1% 1/16W MF-LF 402
41 FW_CURRENT_LIMIT

R4301 10K 5% 1/16W MF-LF 402
FW_TURN_ON_V
R4302 15K 5% 1/16W MF-LF 603
R4303 20K 5% 1/16W MF-LF 402
FW_CURRENT_LIMIT_Q
Q4302 MMBT2222A7F SOT23
FW_FET_LINEAR_LIMIT_OUT
FW_FET_LINEAR_LIMIT_IN
PLACE CLOSE TO COMPARATOR
C4302 0.01UF 20% 16V CERM 402
R4307 20K 5% 1/16W MF-LF 402

PLACEMENT NOTE=PLACE CLOSE TO F4300
XW4300 PPVP_FW_PHY_CPS
MIN LINE WIDTH=0 5MM
MIN NECK WIDTH=0 25MM
VOLTAGE=12V
OUT 39 95

95 P12V_FW_CL
MIN LINE WIDTH=1 7MM
MIN NECK WIDTH=0 5MM
VOLTAGE=12V

CRITICAL
D4300
SM
CRS08-1.5A-30V

95 P12V_FW_D
MIN LINE WIDTH=1 7MM
MIN NECK WIDTH=0 5MM
VOLTAGE=12V

CRITICAL
F4300
3AMP-32V
603

FAST NON-RESETABLE FUSE
THIS FUSE WILL NOT BLOW
IT IS HERE FOR SAFETY ONLY

NOSTUFF
D4305
MMBD914XG
SOT23

95 FW_PORT0_VP_F
MIN LINE WIDTH=1 7MM
MIN NECK WIDTH=0 5MM
VOLTAGE=12V

CRITICAL
L4300
FERR-250-OHM
SM

C4300 0.01UF 10% 50V X7R 603-1

95 FW_PORT0_VP
MIN LINE WIDTH=1 7MM
MIN NECK WIDTH=0 5MM
VOLTAGE=12V

SHOULD BE DONE AS A POWER STRIP(SUBPLANE)

PORT 0
1394B

CRITICAL
J4300
FWB-PL-K62-K62
F-ANG-TH

92 41 40 B1 FW_PORT0_TPB_N
NO_TEST=TRUE
92 41 40 B1 FW_PORT0_TPB_P
NO_TEST=TRUE
92 41 40 B1 FW_PORT0_TPA_N
NO_TEST=TRUE
92 41 40 B1 FW_PORT0_TPA_P
NO_TEST=TRUE

TPB TPB(R)
TPB+ VP
NC SC/NC
TPA VG
TPA+ TPA(R)
SHIELD PINS

FW_PORT0_TPA_R

NOSTUFF C4332 0.001UF 10% 50V CERM 402
514-0769

R4335 1M 1% 1/16W MF-LF 402
C4335 0.1UF 10% 50V X7R 603-1

AREF needs to be isolated from all
local grounds per 1394b spec
When a billingual device is connected to a
beta-only device, there is no DC path
between them (to avoid ground offset issue)

BREF should be hard-connected to logic
ground for speed signaling and connection

R4304 100K 5% 1/16W MF-LF 402
FW_FET_LINEAR_LIMIT_FB
D4302 BAS40XG SOT23
41 6 =PP12V_S0_FW
C4304 0.1UF 10% 16V X7R-CERM 402
V+
U4300
LM393
SOI-HF
NC
GND

5.1V
D4303
SOT23
MMBZ5231BXG
43 IN FW_CURRENT_LIMIT
R4305 100K 5% 1/16W MF-LF 402
FW_CURRENT_LIMIT_R
FW_CURRENT_LIMIT_RD
43 IN FW_FET_LINEAR_LIMIT_IN
FW_FET_LINEAR_LIMIT_OUT OUT 41

PLACE CLOSE TO COMPARATOR
C4305 2.2UF 10% 16V X5R 603
R4306 200K 5% 1/16W MF-LF 402

ACTIVE "LATE VG" + ESD PROTECTION

40 39 6 =PP3V3_S0_FWPHY
C4350 0.1UF 10% 16V X7R-CERM 402
PLACEMENT NOTE=PLACE U4350 CLOSE TO J4300

U4350
TPD4S1394
LLP
CRITICAL
VCC
VCLMP
FWPWR_EN
GND
D1+
D1-
D2+
D2-

TP_FW_LATEVG_VCLMP
FWPWR_EN
NOSTUFF R4350 100K 5% 1/16W MF-LF 402

FW_PORT0_TPB_P
FW_PORT0_TPB_N
FW_PORT0_TPA_P
FW_PORT0_TPA_N
40 41 92 B1

SYNC MASTER=K62 SYNC DATE=01/06/2011
PAGE TITLE
FIREWIRE CONNECTOR
Apple Inc.
DRAWING NUMBER 051-8115
SIZE D
REVISION 11.1.0
BRANCH
PAGE 43 OF 110
SHEET 41 OF 98

BOMOPTION OPTIONS FOR SATA PORT A1 AND A2

A1	A2	ODD_SATA:P1	ODD_SATA:P2
SSD	ODD		X
ODD		X	

USE OF PORT A2 FOR SSD IS NOT INTENDED VIA BOMOPTION THOUGH MLB SUPPORTS IT
K60E should stuff S_P1_ODD:YES because it has no SSD option.

SILKSCREEN:SATA0

SATA PORT A0 FOR HDD

CRITICAL J4510 EP00-081-91 M-ST-SM

518S0251

C4510	0.01UF	SATA_HDD_R2D_C_P	IN
C4511	0.01UF	SATA_HDD_R2D_C_N	IN
C4515	0.01UF	SATA_HDD_D2R_N	OUT
C4516	0.01UF	SATA_HDD_D2R_P	OUT

SILKSCREEN:SATA1

SATA PORT A1 FOR SSD/ODD

SSD CRITICAL J4530 EP00-081-91 M-ST-SM

518S0251

C4530	0.01UF	SATA_SSD_R2D_C_P	IN
C4531	0.01UF	SATA_SSD_R2D_C_N	IN
C4532	0.01UF	SATA_SSD_D2R_N	OUT
C4533	0.01UF	SATA_SSD_D2R_P	OUT

SILKSCREEN:SATA2 ODD_SATA:P2

SATA PORT A2 FOR ODD

CRITICAL J4520 EP00-081-91 M-ST-SM

518S0251

C4520	0.01UF	SATA_ODD_R2D_C_P	IN
C4521	0.01UF	SATA_ODD_R2D_C_N	IN
C4522	0.01UF	SATA_ODD_D2R_N	OUT
C4523	0.01UF	SATA_ODD_D2R_P	OUT

SATA Activity LED

=PP3V3_S0_SATALED

DEVELOPMENT R4599 330 5% 1/10W MF LF 603

SATALED_R_L

DEVELOPMENT DS4599 GREEN-3.6MCD 2 0X1 25MM SM

PCH_SATALED_L — SATALED_L MAKE BASE=TRUE

SILK_PART=SATA ACTIVE

HDD Power

CRITICAL J4511 50293-00771-H01 M-ST-SM

518S0813

=PP12V_S0_SATA 12V 1.2Amp

=PP5V_S0_SATA 5V 1.7Amp

HDD_OOB_TEMP_FB

C4517 10UF 20% 10V X5R 603

C4518 10UF 20% 25V X5R 1206-1

L4511 FERR-220-OHM 0402

HDD_OOB_TEMP_FILT

SSD Power

SSD CRITICAL J4531 50293-00471-H01 M-ST-SM

518S0812

=PP5V_S0_SATA 5V 1.4A/0.8A/ 0.032A

NC

C4537 10UF 20% 10V X5R 603 SSD

ODD PWR CONTROL

CRITICAL J4521 50293-0057N-001 M-ST-SM

518S0792

PP5V_S0_SATA_FET

VOLTAGE=5V NET_PHYSICAL_TYPE=POWER

C4527 10UF 20% 10V X5R 603

C4525 1UF 10% 10V X5R 402

=PP3V3_S0_ODD

R4520 33K 5% 1/16W MF-LF 402

SMC_ODD_DETECT

=PP5V_S0_SATA NET_PHYSICAL_TYPE=POWER

CRITICAL Q4500 FDMC8298 MLP3.3X3.3

NOSTUFF R4550 0 5% 1/8W MF-LF 805

R4503 100K 5% 1/16W MF-LF 402

ODD_PWR_GATE

=PP12V_S0_SATA NET_PHYSICAL_TYPE=POWER

C4500 0.1UF 10% 16V X5R 402

CRITICAL Q4501 SLG5AP001 TDFN

On= 2-5V

R4501 0 5% 1/16W MF-LF 402

ODD_PWR_EN_L

ODD_PWR_EN_L_R

Q4502 2N7002 SOT23-HF1

353S2499 THRM PAD GND

ODD_PWR_EN_LD

SYNC MASTER=K60 JERRY SYNC DATE=01/06/2011

PAGE TITLE: SATA Connectors

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

BRANCH

PAGE 45 OF 110

SHEET 42 OF 98

USB/SMC DEBUG MUX

ADDED AT EVT & SWITCH TO S5 RAIL

Current Limit at 2.1Amp (@ S3 & S0)

=PP5V_S3_USB

PM_EN_USB_PWR

USB_EXTC_OC_L

USB_EXTD_OC_L

USB_EXTA_OC_L

USB_EXTB_OC_L

U4600 TPS2561DR SON — CRITICAL

U4620 TPS2561DR SON — CRITICAL

C4601 0.1UF 20% 10V CERM 402

C4602 330UF 20% 6.3V POLY TANT CASE D3L SM — CRITICAL

C4621 0.1UF 20% 10V CERM 402

C4622 330UF 20% 6.3V POLY-TANT CASE-D3L-SM — CRITICAL

R4600 23.2K 1% 1/16W MF-LF 402

R4620 23.2K 1% 1/16W MF-LF 402

Place R4600 very close to ILIM pin

Place R4620 very close to ILIM pin

PP5V_USB_PORT3

PP5V_USB_PORT2

PP5V_USB_PORT1

PP5V_USB_PORT0

VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

155S0329 L4630 FERR-220-OHM-2.5A 0603 CRITICAL

155S0329 L4660 FERR-220-OHM-2.5A 0603 CRITICAL

155S0329 L4600 FERR-220-OHM-2.5A 0603 CRITICAL

155S0329 L4620 FERR-220-OHM-2.5A 0603 CRITICAL

C4603 0.1UF 20% 10V CERM 402

C4630 0.01UF 20% 16V CERM 402

C4661 0.1UF 20% 10V CERM 402

C4660 0.01UF 20% 16V CERM 402

C4633 0.1UF 20% 10V CERM 402

C4600 0.01UF 20% 16V CERM 402

C4623 0.1UF 20% 10V CERM 402

C4624 0.01UF 20% 16V CERM 402

(PUT CAP ON CONNECTOR SIDE)

PP5V_USB_PORT1_F

PP5V_USB_PORT2_F

PP5V_USB_PORT0_F

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

PP5V_USB_PORT3_F

PP3V3_SMCUSBMUX

=PP3V3_G3H_SMCUSBMUX

=PP3V3_S5_SMCUSBMUX

NOSTUFF R4653 0 5% 1/16W MF-LF 402

R4654 0 5% 1/16W MF-LF 402 MOJOMUX:YES

C4650 0.1UF 20% 10V CERM 402 MOJOMUX:YES

U4650 PI3USB102ZLE TQFN — CRITICAL

SMC_RX_L

SMC_TX_L

USB_EXTD_P

USB_EXTD_N

USB_D_MUXED_P

USB_D_MUXED_N

R4651 0 5% 1/16W MF-LF 402 MOJOMUX:NO

R4652 0 5% 1/16W MF-LF 402 MOJOMUX:NO

USB_DEBUGPRT_EN_L

SEL=1: CHOOSE USB
SEL=0: CHOOSE SMC

L4631 120-OHM-90MA DLP0NS — CRITICAL

USB_PORT3_N

USB_PORT3_P

PORT 3

J4630 USB-K60K62 F-ANG-TH

VBUS
DATA-
DATA+
GND

514-0768

D4630 RCLAMP0502N SLP1210N6 — CRITICAL

PORT 2

L4621 120-OHM-90MA DLP0NS — CRITICAL

USB_EXTC_N

USB_EXTC_P

USB_PORT2_N

USB_PORT2_P

J4620 USB-K60K62 F-ANG-TH

514-0768

D4620 RCLAMP0502N SLP1210N6 — CRITICAL

PORT 1

L4611 120-OHM-90MA DLP0NS — CRITICAL

USB_EXTB_N

USB_EXTB_P

USB_PORT1_N

USB_PORT1_P

J4610 USB-MG6-K60-K62 F-ANG-TH

514-0770

D4610 RCLAMP0502N SLP1210N6 — CRITICAL

PORT 0

L4601 120-OHM-90MA DLP0NS — CRITICAL

USB_EXTA_N

USB_EXTA_P

USB_PORT0_N

USB_PORT0_P

J4600 USB-MG6-K60-K62 F-ANG-TH

514-0770

D4600 RCLAMP0502N SLP1210N6 — CRITICAL

USB PORT POWER:

EACH PORT IS HARDWARE Capable of :

STATE	MAX	MIN (WITHIN THE TOLERANCE)
S0, S3	2.7A	2.1A -- PER PORT

WHEN CURRENT HITS LIMIT, TPS2561 BECOME CONSTANT CURRENT MODE
AND STAY AT THE LIMIT LEVEL UNTIL THERMAL SHUTDOWN WHEN JUNCTION REACH 130C

SOFTWARE WILL ALOW 500MA/PORT, PLUS 2700MA EXTRA POWER TO BE distributed to approved devices on a 1st-come, 1st-served basis.

EXAMPLE: Port 1 - iPad fast charging = 2100mA
Port 2 - Wired Keyboard = 1100mA
Port 3 - iPhone fast charging = 1000mA
PORT 4 - USB 2.0 500MA = 500MA
TOTAL: 4700MA

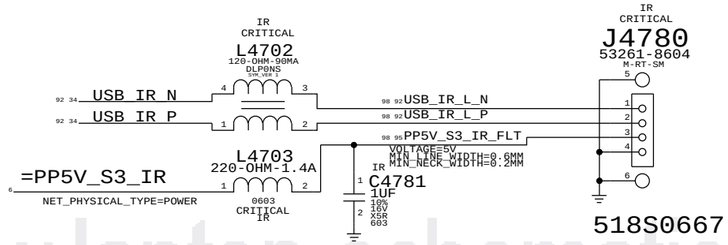
SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: EXTERNAL USB CONNECTORS

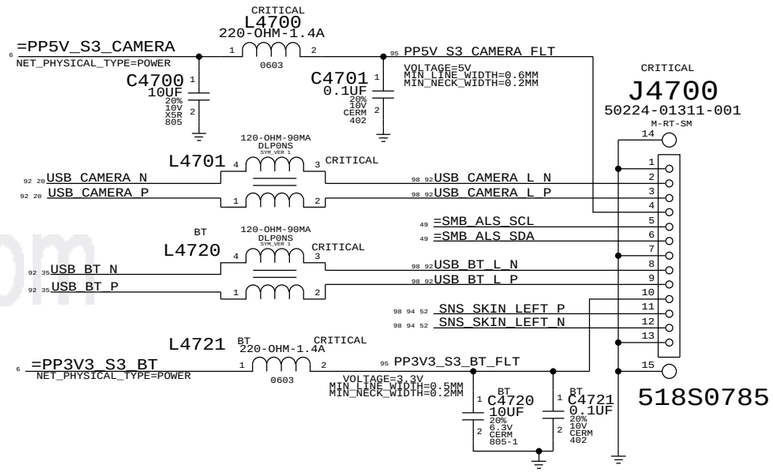
Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 46 OF 110
SHEET 43 OF 98

IR RECEIVER CONNECTOR

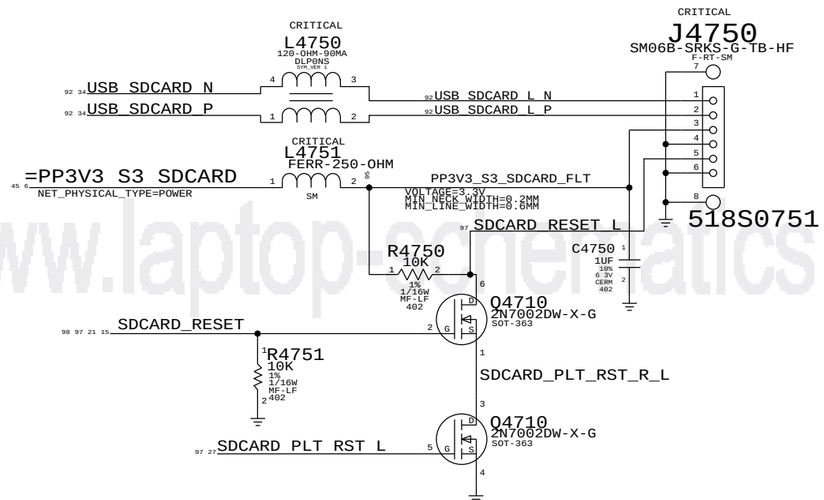


CAMERA/ALS & BLUETOOTH (K37A) CONNECTOR



Skin Temp sense at upper Left Screen corner

SD Card Reader Board (Lazarus)



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

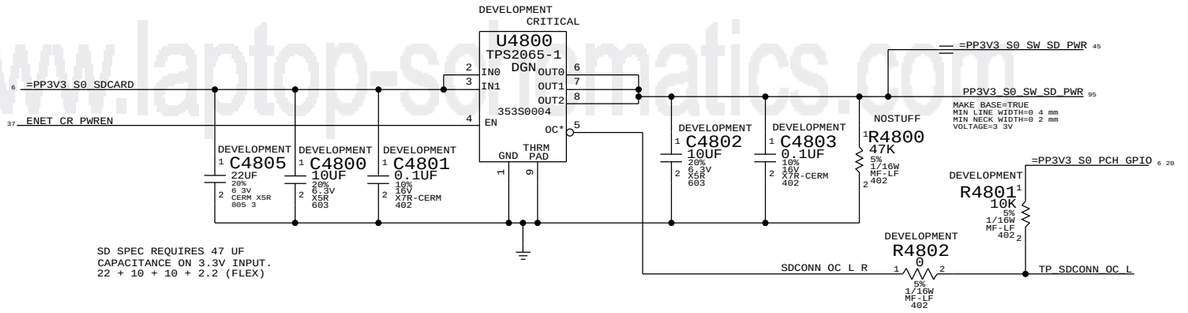
Internal USB Connections

Apple Inc.

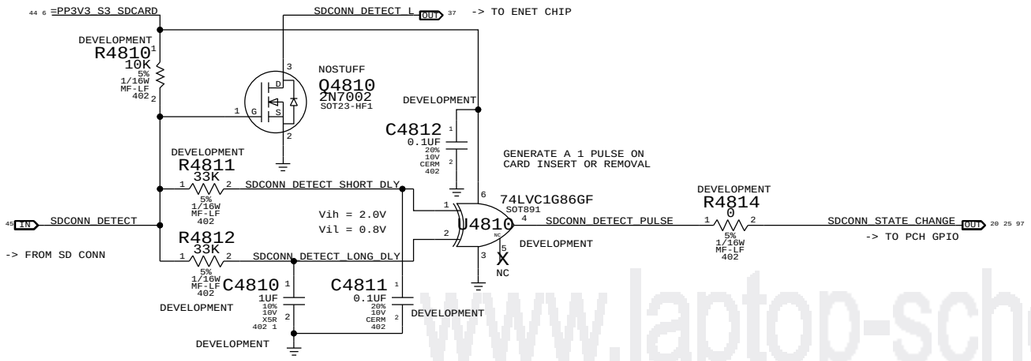
DRAWING NUMBER	051-8115
SIZE	D
REVISION	11.1.0
BRANCH	
PAGE	47 OF 110
SHEET	44 OF 98

SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

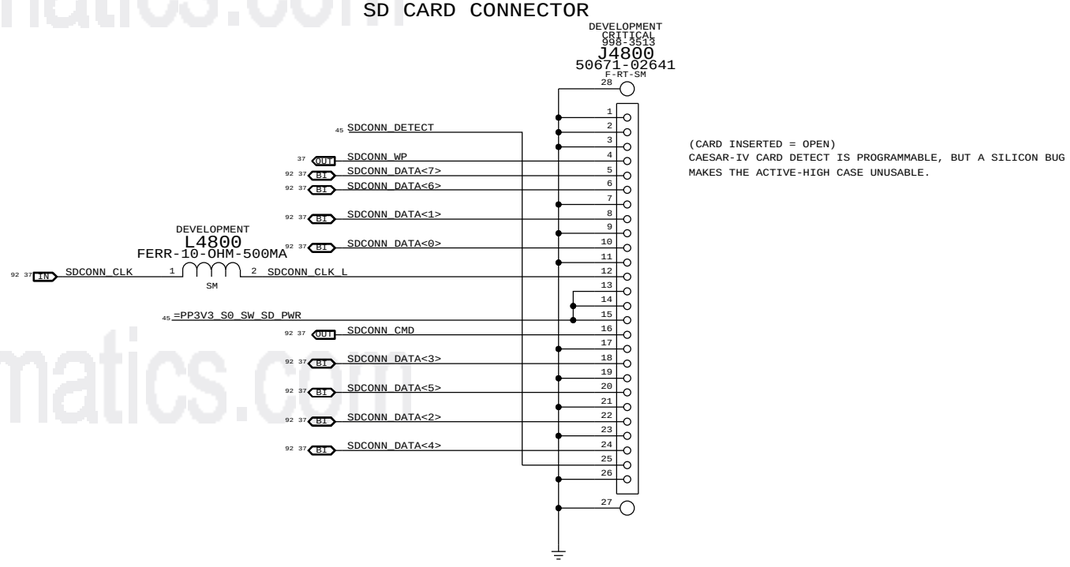
TPS2065-1 (1.0A LIMIT) HAS ACTIVE LOAD DISCHARGE SO R4800 IS NOSTUFF.



SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO CIRCUIT



SD CARD CONNECTOR



SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 48 OF 110
SHEET 45 OF 98

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

338S0878

U4900
H8S2117
LFBGA
(1 OF 4)
OMIT

47	OUT	SMC_EXCARD_PWR_EN	B12	P10	
47	OUT	SMC_RSTGATE_L	C13	P11	
97 64	IN	ALL_SYS_PWRGD_SMC	A15	P12	
97 64	IN	RSMRST_PWRGD	B14	P13	
		NC	B15	P14	
97 27	OUT	PM_RSMRST_L	C14	P15	
47	OUT	CPUIMVP_VR_ON	D12	P16	
97 25 19	OUT	PM_PWRBTN_L	C15	P17	
		K62 NEW:NOT USE NC	D13	P20	
		NC	D14	P21	
		NC	D15	P22	
		NC	E12	P23	
		K62 NEW:NOT USE NC	E14	P24	
		NC	E15	P25	
		K62 NEW:NOT USE NC	E13	P26	
		NC	F14	P27	
91 48 18	BI	LPC_AD<0>	D9	P30	
91 48 18	BI	LPC_AD<1>	C9	P31	
91 48 18	BI	LPC_AD<2>	A9	P32	
91 48 18	BI	LPC_AD<3>	B9	P33	
91 48 18	IN	LPC_FRAME_L	D8	P34	
97 27	IN	SMC_LRESET_L	C8	P35	
91 27	IN	LPC_CLK33M_SMC	A8	P36	
48 18	BI	LPC_SERIRQ	D7	P37	
		NC	A5	P40	
		K62 P1 NOT USED, WAS OOB_TEMP NC	B5	P41	
49	BI	SMB_MGMT_DATA	D5	P42 (OC)	
47	OUT	SMS_ONOFF_L	C3	P43	
		NC	B1	P44	
		NC	C2	P45	
47	OUT	SMC_GFX_THROTTLE_L	D3	P46	
		NC	C1	P47	
48 47 46 43	OUT	SMC_TX_L	G1	P50	
48 47 46 43	IN	SMC_RX_L	G4	P51	
49	BI	SMB_0_S0_CLK	F2	P52 (OC)	

P60	L13	SMC_PM_G2_EN	OUT	74 97	
P61	L14	NC			
P62	L15	NC			
P63	K12	NC			
P64	K13	SMC_ADAPTER_EN	OUT	19 47 97	
P65	K14	NC			
P66	J12	SMC_PROCHOT_3_3_L	IN	47 97	
P67	J13	SMC_BIL_BUTTON_L	IN	47	
P70	N12	SMC_VCORE_ISENSE	IN	50 94 (IMON)	
P71	R13	SMC_VCORE_VSENSE	IN	50 94 (IMON)	
P72	P13	SMC_CPU_1V5_ISENSE	IN	50 94	
P73	R14	SMC_CPU_1V5_VSENSE	IN	50 94	
P74	P14	SMC_VCCSA_ISENSE	IN	50 94	
P75	R15	SMC_VCCSA_VSENSE	IN	50 94	
P76	N13	SMC_VAXG_ISENSE	IN	50 94 (IMON)	
P77	P15	SMC_VAXG_VSENSE	IN	50 94 (IMON)	
P80	C7	SMC_WAKE_SCI_L	OUT	15 18 21 97	PROTO-3, Change back to WAKE_SCI_L
P81	A7	NC			
P82	B7	PM_CLKRUN_L	OUT	15 19 48 97	
P83	D6	LPC_PWRDWN_L	IN	19 48 97	
P84	C6	SMC_TX_L	OUT	43 46 47 48	
P85	A6	SMC_RX_L	IN	43 46 47 48	
P86	B6	(OC) SMB_MGMT_CLK	BI	49	
P90	K4	SMC_ONOFF_L	IN	47 97	
P91	J2	SMC_BC_ACOK	IN	47	
P92	J1	NC			
P93	J3	PM_SLP_S3_L	IN	5 19 26 32 36 47 63 82 97	
P94	J4	PM_SLP_S4_L	IN	5 19 32 47 53 97	K60 New Change
P95	H2	PM_SLP_S5_L	IN	5 19 47 63 97	K60 New Change
P96	H1	PM_CLK32K_SUSCLK	IN	9 91 97	
P97	G2	(OC) SMB_0_S0_DATA	BI	49	

		K62 NEW:NOT USE,PULLED UP SMC_PA0	IN	47	R3 PA0
97 18	OUT	SPI_DESCRIPTOR_OVERRIDE_L (OC)			P3 PA1
97 27 25 19	OUT	PM_SYSRST_L (OC)			R2 PA2
47 43	OUT	USB_DEBUGPRT_EN_L (OC)			N3 PA3
47	IN	MEM_EVENT_A_L (OC)			R1 PA4
47	IN	MEM_EVENT_B_L (OC)			N2 PA5
47	BI	SYS_ONEWIRE (OC)			M4 PA6
97 19 15	OUT	PM_BATLOW_L (OC)			N1 PA7
		NC			B10 PB0
PROTO-3:back to K75F	97 47 23	OUT SMC_RUNTIME_SCI_L			A10 PB1
	98 42	IN SMC_ODD_DETECT			D10 PB2
K62 NEW:NOT USE,PULLED UP	47	IN (See below) SMC_PB3			A11 PB3
	94 51	IN SMC_HDD_OOB_TEMP			B11 PB4
		NC			C11 PB5
K62 NEW:NOT USE,PULLED UP		IN SMC_PB6			A12 PB6
	47	IN SMC_GFX_OVERTEMP_L			D11 PB7
	53	OUT SMC_FAN_0_CTL			G14 PC0
	53	OUT SMC_FAN_1_CTL			G15 PC1
		NC			G13 PC2
	54	OUT SMC_FAN_3_CTL			G12 PC3
	53	IN SMC_FAN_0_TACH			H14 PC4
	53	IN SMC_FAN_1_TACH			H15 PC5
		NC			H13 PC6
	54	IN SMC_FAN_3_TACH			H12 PC7
(IMON)	94 50	IN SMC_1V05_ISENSE			M11 PD0
(IMON)	94 50	IN SMC_1V05_VSENSE			P11 PD1
	94 50	IN SMC_PCH_1V05_ISENSE			R11 PD2
	94 50	IN SMC_PCH_1V05_VSENSE			N11 PD3
	94 50	IN SMC_GPU_ISENSE			P10 PD4
	94 50	IN SMC_GPU_VSENSE			R10 PD5
	94 50	IN SMC_DIMM_ISENSE			N10 PD6
	94 50	IN SMC_DIMM_VSENSE			M10 PD7

U4900
H8S2117
LFBGA
(2 OF 4)
OMIT

PE0	M3	SMC_PE0	IN	47	K62 NEW:NOT USE,PULLED UP
PE1*	M2	SMC_TCK	IN	47 48	
PE2*	M1	SMC_TDI	IN	47 48	
PE3*	L4	SMC_TDO	OUT	47 48	
PE4*	L2	SMC_TMS	IN	47 48	
PF0	M7	G3_POWERON_L	IN	47	
PF1	P6	SMC_SYS_LED	OUT	47	
PF2	R6	SMC_LID		47	
PF3	N6	NC			
PF4	M6	NC			
PF5	R5	BDV_BKL_PWM	OUT	83 97	K62 PROTO-2:NEW
PF6	P5	NC			
PF7	N5	NC			
PG0	P9	NC			
PG1	R9	SMC_SMS_INT	IN	47	
PG2	N9	(OC) SMB_BSA_DATA	BI	49	
PG3	P8	(OC) SMB_BSA_CLK	BI	49	
PG4	R8	(OC) SMB_A_S3_DATA	BI	49	
PG5	M8	(OC) SMB_A_S3_CLK	BI	49	
PG6	P7	(OC) SMB_B_S0_DATA	BI	49	
PG7	R7	(OC) SMB_B_S0_CLK	BI	49	
PH0	E1	SMC_PROCHOT	OUT	47 97	
PH1	F3	SMC_THRMTRIP	OUT		
PH2	K2	NC			
PECI	PH3	C4	97	CPU_PECI_R	
PEVref	PH4	D4		PVCCIO_S0_SMC_R	
PEVSTP	PH5	B3	97	PM_PECI_PWRGD_R	

R4910 0 MF-LF 5% 402 1/16W — CPU_PECI 11 21 97
R4911 0 MF-LF 5% 402 1/16W — =PPVCCIO_S0_SMC 6 47
R4912 0 MF-LF 5% 402 1/16W — PM_PECI_PWRGD 64 97
C4910 0.1UF 20% 10V CERM 402

SMC PB3: SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SMC PG1: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

95 47 46 PP3V3_G3H_AVREF_SMC Peak/Ave/Standby = 2mA/1mA/5uA
47 46 6 =PP3V3_G3H_SMC Peak/Ave/Sleep/Standby = 40mA/25mA/20mA/50uA

C4902 22UF 20% 6.3V CERM 805
C4903 0.1UF 20% 10V CERM 402
C4904 0.1UF 20% 10V CERM 402
C4905 0.1UF 20% 10V CERM 402
C4906 0.1UF 20% 10V CERM 402
PLACEMENT NOTE=Place C4907 close to U4900 pin 13

R4999 4.7 5% 1/16W MF LF 402 — Peak/Ave/Standby= 2mA/1mA/5uA
95 46 PP3V3_G3H_SMC_AVCC
MIN LINE WIDTH=0.25 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=3.4V
SMC_VCL
C4907 0.47UF 10% 6.3V CERM X5R 402
C4920 0.1UF 20% 10V CERM 402
PLACEMENT NOTE=Place R4999 close to U4900 pin 76
PLACEMENT NOTE=Place C4920 close to U4900 pin 76

U4900
H8S2117
LFBGA
(3 OF 4)
OMIT

AVCC N14 — VCC A1 — VCL P1 — AVREF J15 — F1 M14

97 48 47	IN	SMC_RESET_L	E3	RES*
94 47		SMC_XTAL	A2	XTAL
94 47		SMC_EXTAL	B2	EXTAL

R4909 10K 5% 1/16W MF LF 402
R4901 10K 5% 1/16W MF LF 402

MD1	E2	SMC_MD1	IN 48
MD2	K1	SMC_KBC_MDE	
NMI	F4	SMC_NMI	IN 48
ETRST*	L1	SMC_TRST_L	IN 48
AVSS	R12	NOSTUFF	

R4902 10K 5% 1/16W MF LF 402
R4998 10K 5% 1/16W MF LF 402
R4903 0 5% 1/16W MF LF 402

VSS — D2 P4 F12 B13 A4 — XW4900 SM

GND_SMC_AVSS 46 47 50 94

95 47 46 PP3V3_G3H_AVREF_SMC
47 46 6 =PP3V3_G3H_SMC
95 46 PP3V3_G3H_SMC_AVCC

AVCC1 M15 — VCC3 P2 — AVREF1 M15

U4900
H8S2117
LFBGA
(4 OF 4)
OMIT

E4 N4 M9 M12 M13 L12 A3 — NC

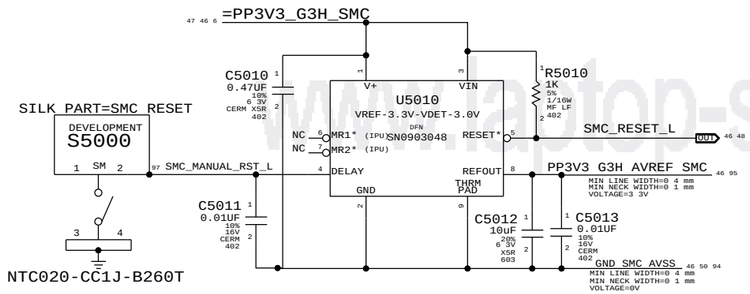
PJ0	C5	NC	
PJ1	B8	NC	
PJ2	C10	NC	
PJ3	C12	NC	
PJ4	A14	NC	
PJ5	F15	NC	
PJ6	J14	NC	
PJ7	K15	NC	
PI0	N8	NC	
PI1	N7	NC	
PI2	M5	NC	
PI3	L3	NC	
PI4	K3	NC	
PI5	H3	NC	
PI6	H4	NC	
PI7	G3	NC	

AVSS1 P12 — R4 — VSS F13 A13 B4 D1

94 50 47 46 GND_SMC_AVSS

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE	SMC
Apple Inc.	DRAWING NUMBER 051-8115 SIZE D
	REVISION 11.1.0
	BRANCH
	PAGE 49 OF 110
	SHEET 46 OF 98

SMC Reset "Button", Supervisor & AVREF Supply



MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

MISC. SIGNAL ALIASES

SMC_GFX_OVERTEMP_L ═ MXM_ALERT_L (MAKE BASE=TRUE)
SMC_GFX_THROTTLE_L ═ MXM_PWR_LEVEL (MAKE BASE=TRUE)
CPUIMVP_VR_ON ═ SMC_DELAYED_PWRGD (MAKE BASE=TRUE)

UNUSED PORT 7 ANALOG SENSORS

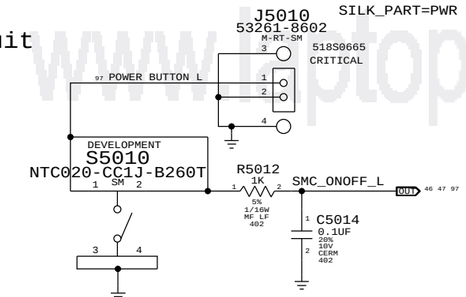
=PP3V3 G3H SMC

SMC_ONOFF_L	R5020	10K	5% 1/16W MF LF 402
SMC_TX_L	R5021	10K	5% 1/16W MF LF 402
SMC_RX_L	R5022	100K	5% 1/16W MF LF 402
SYS_ONEWIRE	R5023	2.0K	5% 1/16W MF LF 402
SMC_TMS	R5024	10K	5% 1/16W MF LF 402
SMC_TDO	R5025	10K	5% 1/16W MF LF 402
SMC_TDI	R5026	10K	5% 1/16W MF LF 402
SMC_TCK	R5027	10K	5% 1/16W MF LF 402
SMC_BI_BUTTON_L	R5028	10K	5% 1/16W MF LF 402
SMC_BC_ACOK	R5029	10K	5% 1/16W MF LF 402
SMC_ADAPTER_EN	R5030	10K	5% 1/16W MF LF 402
USB_DEBUGPRT_EN_L	R5031	10K	5% 1/16W MF LF 402
G3_POWERON_L	R5034	10K	5% 1/16W MF LF 402
SMC_SMS_INT	R5032	10K	5% 1/16W MF LF 402
SMC_LID	R5033	10K	5% 1/16W MF LF 402
SMC_PA0	R5037	100K	5% 1/16W MF LF 402
SMC_PB6	R5038	100K	5% 1/16W MF LF 402
SMC_PE0	R5036	100K	5% 1/16W MF LF 402

=PP3V3_S0_SMC_LS

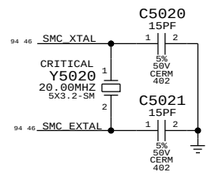
SMC_GFX_OVERTEMP_L	R5035	10K	5% 1/16W MF LF 402
SMC_RUNTIME_SCI_L	R5044	10K	5% 1/16W MF LF 402

POWER BUTTON



SILK_PART=PWR BTN

SMC Crystal Circuit



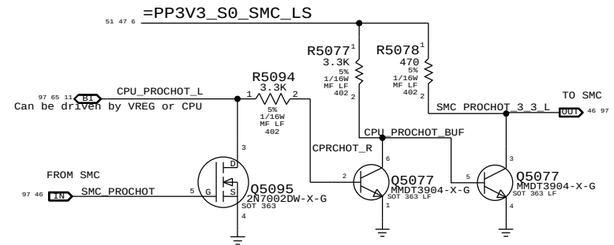
UNUSED TP/NC ALIASES

SMC_EXCARD_PWR_EN ═ TP_SMC_EXCARD_PWR_EN (MAKE BASE=TRUE)
SMS_ONOFF_L ═ TP_SMS_ONOFF_L (MAKE BASE=TRUE)
SMC_RSTGATE_L ═ TP_SMC_RSTGATE_L (MAKE BASE=TRUE)
SMC_SYS_LED ═ TP_SMC_SYS_LED (MAKE BASE=TRUE)
SMC_PB3 ═ TP_SMC_PB3 (MAKE BASE=TRUE)

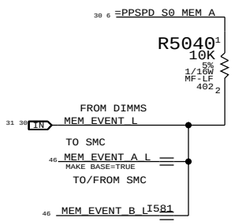
=PP3V3_S0_SMC_LS

PM_SLP_S3_L	R5041	100K	5% 1/16W MF LF 402
PM_SLP_S5_L	R5042	100K	5% 1/16W MF LF 402
PM_SLP_S4_L	R5043	100K	5% 1/16W MF LF 402

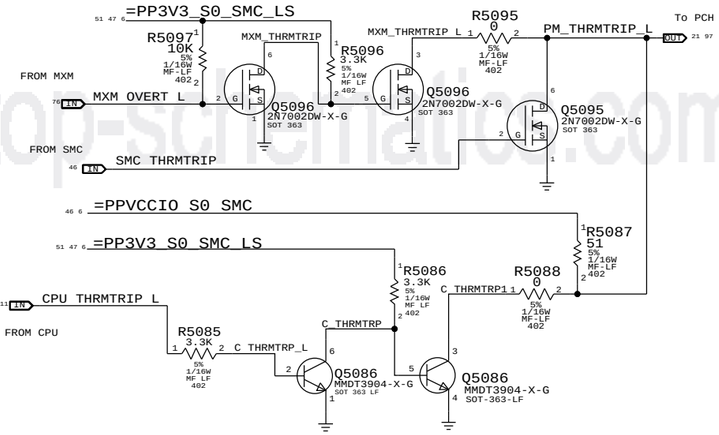
SMC PROCHOT 3.3V LEVEL SHIFTING



MEM_EVENT

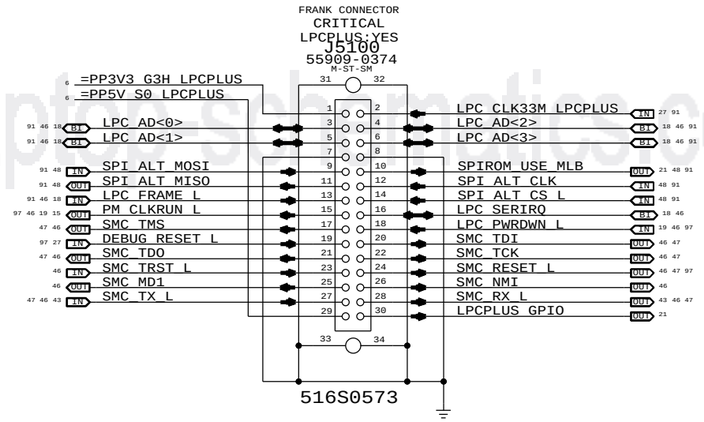


SMC & MXM THERMTRIP LEVEL SHIFTING



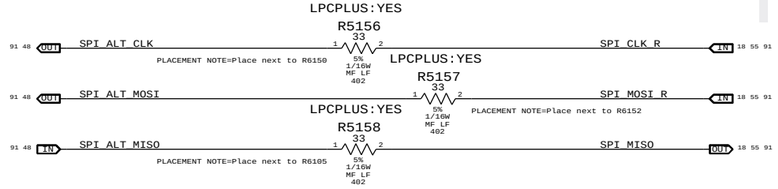
SYNC MASTER=K62	SYNC DATE=01/06/2011
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER 051-8115 · SIZE D
	REVISION 11.1.0
	BRANCH
	PAGE 50 OF 110
	SHEET 47 OF 98

LPC+SPI Connector



Alternate SPI ROM Support

SPI Bus Series Resistance Option



SYNC_MASTER=K62_AARON SYNC_DATE=11/30/2009

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 51 OF 110

SHEET: 48 OF 98

PCH "SMBUS" CONNECTIONS

49 6 =PP3V3_S0_SMBUS

PCH
U1800
(MASTER)

94 18 SMBUS_PCH_CLK
MAKE_BASE=TRUE
94 18 SMBUS_PCH_DATA
MAKE_BASE=TRUE

R5208[1] 2.2K 5% 1/16W MF LF 402 2
[1]R5209 2.2K 5% 1/16W MF LF 2 402

MEMORY A DIMMS
J3100-A/B
(DIMM0: WRITE: 0XA0 READ: 0XA1)
(DIMM2: WRITE: 0XA2 READ: 0XA3)
=I2C_SODIMMA_SCL 30
=I2C_SODIMMA_SDA 30

MEMORY B DIMMS
J3200-A/B
(DIMM1: WRITE: 0XA4 READ: 0XA5)
(DIMM3: WRITE: 0XA6 READ: 0XA7)
=I2C_SODIMMB_SCL 31
=I2C_SODIMMB_SDA 31

XDP (PCH)
J2550
49 25 =SMBUS_XDP_SCL
49 25 =SMBUS_XDP_SDA

MIKEY
U6806
(WRITE: 0X72 READ: 0X73)
=I2C_AUDIO_SCL 62
=I2C_AUDIO_SDA 62

XDP (CPU)
J2500
49 25 =SMBUS_XDP_SCL
49 25 =SMBUS_XDP_SDA

CK505
U2600
(WRITE: 0XD2 READ: 0XD3)
=SMBUS_CK505_SCL 26
=SMBUS_CK505_SDA 26

MEM VREF MARGIN A
U2900
(WRITE: 0X5C READ: 0X5D)
=I2C_VREFMRGN_A_SCL 28
=I2C_VREFMRGN_A_SDA 28

SPTX BLC MICRO
VIA J602
(WRITE: 0X6E READ: 0X6F)
6 =SMB_BLC_PCH_SCL
6 =SMB_BLC_PCH_SDA

MEM VREF MARGIN B
U2910
(WRITE: 0X7C READ: 0X7D)
=I2C_VREFMRGN_B_SCL 28
=I2C_VREFMRGN_B_SDA 28

DP SDRV "A"
U9310, PS8301
(WRITE: 0X94, READ: 0X95)
=I2C_DPSDRVA_SCL 84
=I2C_DPSDRVA_SDA 84

PCH "SML 0" CONNECTIONS

49 6 =PP3V3_S0_SMBUS

PCH
U1800
(MASTER)

94 18 SML_PCH_0_CLK
MAKE_BASE=TRUE
94 18 SML_PCH_0_DATA
MAKE_BASE=TRUE

R5202[1] 8.2K 5% 1/16W MF LF 402 2
[1]R5203 8.2K 5% 1/16W MF LF 2 402

THIS PAGE DIFFERENT BETWEEN K60 AND K62.

SMC SLAVE SMBUS "2" CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 2 ONLY (NO CONNECTIONS, JUST PULLUP)

6 =PP3V3_S0_SMBUS_SMC_BSA

SMC
U4900
(SLAVE)

46 SMB_BSA_CLK — 94 SMBUS_SMC_BSA_SCL
MAKE_BASE=TRUE
46 SMB_BSA_DATA — 94 SMBUS_SMC_BSA_SDA
MAKE_BASE=TRUE

R5280[1] 100K 5% 1/16W MF LF 402 2
[1]R5281 100K 5% 1/16W MF LF 2 402

SMC "B" SMBUS CONNECTIONS

BUS B CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K60/62 CHOOSES 0

6 =PP3V3_S0_SMBUS_SMC_B

SMC
U4900
(MASTER)

46 SMB_B_S0_CLK — 94 SMBUS_SMC_B_S0_SCL
MAKE_BASE=TRUE
46 SMB_B_S0_DATA — 94 SMBUS_SMC_B_S0_SDA
MAKE_BASE=TRUE

R5260[1] 2.0K 5% 1/16W MF LF 402 2
[1]R5261 2.0K 5% 1/16W MF LF 2 402

AC/DC PS TEMPS
EMC1403-[1,2] : ACDC THRU J600
(WRITE 0X98 OR 0X9A READ 0X99 OR 0X9B)
3 SENSE POINTS PRIMARY SECONDARY AMB
=SMB_ACDC_SCL 6
=SMB_ACDC_SDA 6

AC/DC PS POWER
INA219: ACDC THRU J600
(WRITE 0X80 READ 0X81)
OUTPUT VOLTAGE CURRENT POWER

SMC "0" SMBUS CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 0 ONLY

6 =PP3V3_S0_SMBUS_SMC_0

SMC
U4900
(MASTER)

46 SMB_0_S0_CLK — 94 SMBUS_SMC_0_S0_SCL
MAKE_BASE=TRUE
46 SMB_0_S0_DATA — 94 SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE

R5250[1] 2.2K 5% 1/16W MF LF 402 2
[1]R5251 2.2K 5% 1/16W MF LF 2 402

Also reserve 0x56 and 0x32 per spec

MXM TEMP
GPU ON CARD - J8400
NV INSIDE (WRITE: 0X9E READ: 0X9F)
EMC1402 ON AMD MXM CARD (WRITE 0X98 READ 0X99)
=SMB_MXM_THRM_SCL 76
=SMB_MXM_THRM_SDA 76

EMC1414: U5520
DEV: CPU D,CPU HTSK
(WRITE: 0X78 READ: 0X79)

EMC1428: U5500
PROD: AMB L-SKIN,R-SKIN,ODD,
LCD,CPU PROX,MXM TEMPS
(WRITE: 0X92 READ:0X93)
=SMB_SNS1_SCL 52
=SMB_SNS1_SDA 52

PCIE MINI-CARD
X18 WI-FI MODULE
TMP106: J3400
(WRITE: 0X90 READ: 0X91)
=SMB_MINI_SCL 33
=SMB_MINI_SDA 33

PCH "SML 1" CONNECTIONS

49 6 =PP3V3_S0_SMBUS

PCH (FOR TEMP)
U1800
(SLAVE)
(WRITE: 0X86 READ: 0X89)

94 18 SML_PCH_1_CLK
MAKE_BASE=TRUE
94 18 SML_PCH_1_DATA
MAKE_BASE=TRUE

NOSTUFF R5204[1] 8.2K 5% 1/16W MF LF 402 2
NOSTUFF [1]R5205 8.2K 5% 1/16W MF LF 2 402

R5206 0 5% 1/10W MF-LF 402
R5207 0 5% 1/10W MF-LF 402

THE PCH address is user programmable by SPI ROM

SMC "A" SMBUS CONNECTIONS

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE
BUS A CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K74 CHOOSES 1

6 =PP3V3_S3_SMBUS_SMC_A

SMC
U4900
(MASTER)

46 SMB_A_S3_CLK — 94 SMBUS_SMC_A_S3_SCL
MAKE_BASE=TRUE
46 SMB_A_S3_DATA — 94 SMBUS_SMC_A_S3_SDA
MAKE_BASE=TRUE

R5270[1] 4.7K 5% 1/16W MF-LF 402 2
[1]R5271 4.7K 5% 1/16W MF-LF 2 402

ALS
(WRITE: 0X52 READ: 0X53)
=SMB_ALS_SCL 44
=SMB_ALS_SDA 44

SMC "MANAGEMENT" SMBUS (BUS 1)

USES INTERNAL SMC CONTROLLER CHANNEL 1 ONLY

6 =PP3V3_S0_SMBUS_SMC_MGMT

SMC
U4900
(MASTER)

46 SMB_MGMT_CLK — 94 SMBUS_SMC_MGMT_SCL
MAKE_BASE=TRUE
46 SMB_MGMT_DATA — 94 SMBUS_SMC_MGMT_SDA
MAKE_BASE=TRUE

R5290[1] 2.2K 5% 1/16W MF LF 402 2
[1]R5291 2.2K 5% 1/16W MF LF 2 402

PANEL TEMP SENSOR
TMP421 ON TCON BOARD VIA J9002
(SLAVE)
(WRITE: 0X9E READ: 0X9F)
SMB_DP_TCON_SLA_SCL 81
SMB_DP_TCON_SLA_SDA 81

DISPLAY TCON
PARADE ON TCON BOARD VIA J9002
(SLAVE)
(TBD WRITE: 0X1A READ: 0X1B)
(TO READ VENDOR ID AND PANEL ID)
TCON ALSO HAS MASTER BUS TO LUT ROM AND EDID ROM

DISPLAY TCON TO SPTX OR O2M BLC

49 6 =PP3V3_S0_SMBUS

DISPLAY TCON
VIA J9002
(MASTER)

=SMB_DP_TCON_SDA — MAKE_BASE=TRUE
=SMB_DP_TCON_SCL — MAKE_BASE=TRUE

R5210[1] 2.2K 5% 1/16W MF LF 402 2
[1]R5211 2.2K 5% 1/16W MF LF 2 402

BLC MICRO
VIA J602
(SLAVE)
(WRITE: 0X6E READ: 0X6F)
SMB_BLC_TCON_SDA 84 (MUX) 81
SMB_BLC_TCON_SCL 84 (MUX) 81

NOTE: DISPLAY TCON HAS 4.7K PU.
NOTE: SPTX BLC HAS 4.7K PU.
NOTE: O2Micro BLC HAS NO PU.

T29 I2C CONNECTIONS

6 =PP3V3_S0_T29I2C

I2C BUS PULL-UP RAIL MUST REFLECT WHEN USB POWER (VBUS) IS VALID.

T29 IC
U9700
(MASTER)

96 86 I2C_T29_SCL
MAKE_BASE=TRUE
96 86 I2C_T29_SDA
MAKE_BASE=TRUE

T29 R5230[1] 4.7K 5% 1/16W MF LF 402 2
T29 [1]R5231 4.7K 5% 1/16W MF LF 2 402

T29 PORT A MCU
U9330
(WRITE: 0X26 READ: 0X27)
=I2C_T29AMCU_SCL 84
=I2C_T29AMCU_SDA 84

SYNC_MASTER=K60_MARK SYNC_DATE=01/06/2011

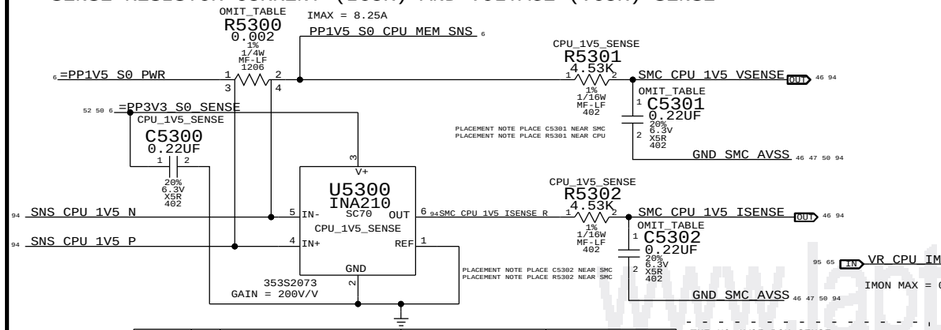
PAGE TITLE
SMBUS CONNECTIONS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 52 OF 110
SHEET 49 OF 98

CPU VDD 1.5V

SENSE RESISTOR CURRENT (IC5R) AND VOLTAGE (VC5R) SENSE

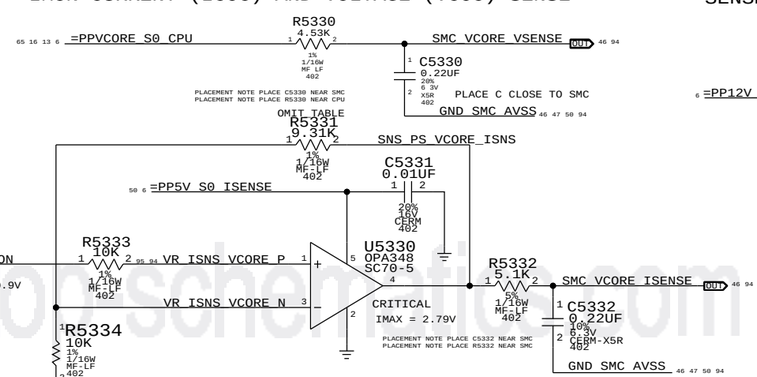


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5300	CPU_1V5_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5300	NO_CPU_1V5_SENSE
132S0080	2	CAP,0.22UF,402	C5301,C5302	CPU_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5301,C5302	NO_CPU_1V5_SENSE

THE NO_1V05_PCH_SENSE, NO_CPU_VCCSA_SENSE, AND NO_CPU_1V5_SENSE CONFIGURATIONS SHOULD IDEALLY NEVER BE USED AS TOTAL CPU POWER SENSING REQUIRES ALL 3 SENSORS.

CPU VCC (VCORE)

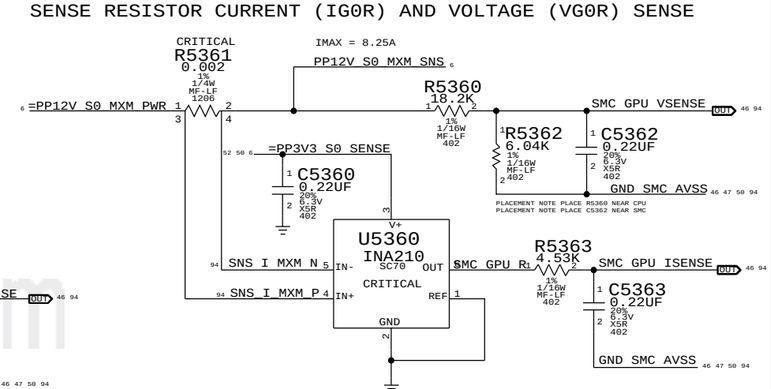
IMON CURRENT (IC0C) AND VOLTAGE (VC0C) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0312	1	RES,MTL FILM,1/16W,9.31K,0402	R5331	CPUVCORE-3PH
114S0345	1	RES,MTL FILM,1/16W,21K,0402	R5331	CPUVCORE-4PH

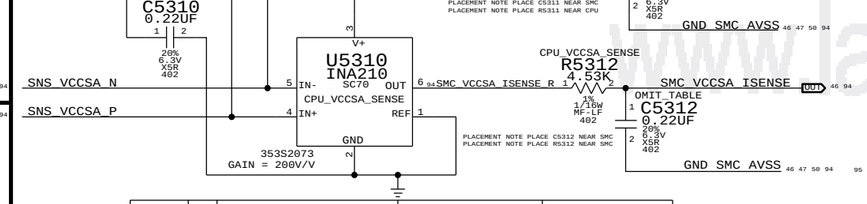
GPU MXM

SENSE RESISTOR CURRENT (IG0R) AND VOLTAGE (VG0R) SENSE



CPU VCCSA

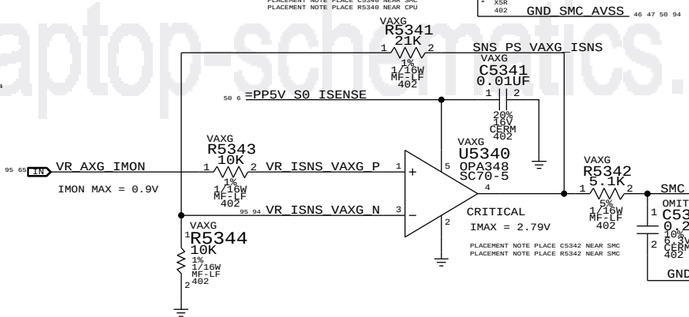
SENSE RESISTOR CURRENT (ICSR) AND VOLTAGE (VCSR) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5310	CPU_VCCSA_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5310	NO_CPU_VCCSA_SENSE
132S0080	2	CAP,0.22UF,402	C5311,C5312	CPU_VCCSA_SENSE
116S0004	2	RES,0 OHM,402	C5311,C5312	NO_CPU_VCCSA_SENSE

CPU VAXG

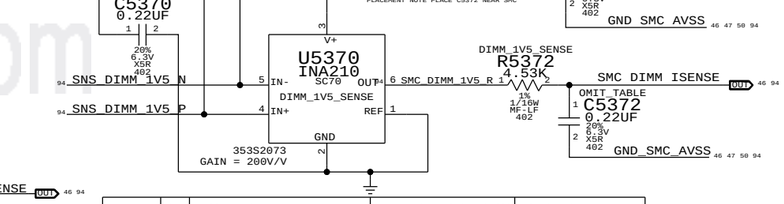
IMON CURRENT (IC0G) AND VOLTAGE (VC0G) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5340,C5342	VAXG
116S0004	2	RES,0 OHM,402	C5340,C5342	NO_VAXG

DIMM VDD 1.5V (LIKELY DEVELOPMENT ONLY)

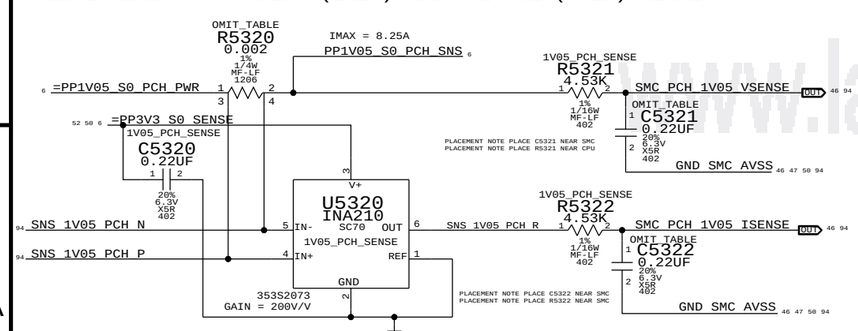
SENSE RESISTOR CURRENT (IM0R) AND VOLTAGE (VM0R) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5371,C5372	DIMM_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5371,C5372	PRODUCTION

PCH 1.05V

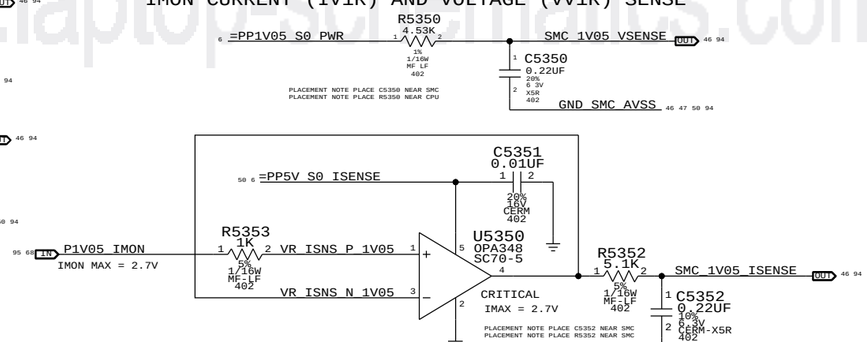
SENSE RESISTOR CURRENT (IN1R) AND VOLTAGE (VN1R) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5320	1V05_PCH_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5320	NO_1V05_PCH_SENSE
132S0080	2	CAP,0.22UF,402	C5321,C5322	1V05_PCH_SENSE
116S0004	2	RES,0 OHM,402	C5321,C5322	NO_1V05_PCH_SENSE

1.05V FOR CPU VCCIO, CPU VCCSA & PCH 1.05V

IMON CURRENT (IV1R) AND VOLTAGE (VV1R) SENSE

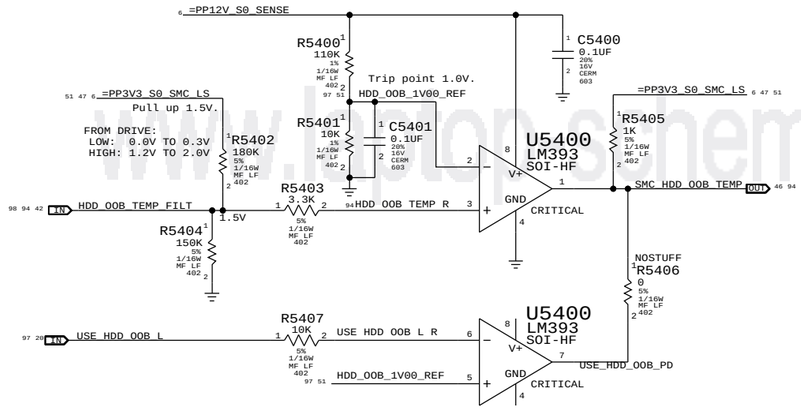


NOTE: TOTAL CPU POWER = VC0C*IC0C + VCSR*ICSR + VCSC*ICSC + VC0G*IC0G + VV1R*ICIR

where ICIR = IV1R - IN1R - ICSR

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE: CPU/PCH/GPU POWER SENSE	
Apple Inc.	DRAWING NUMBER: 051-8115 SIZE: D
	REVISION: 11.1.0
	BRANCH:
	PAGE: 53 OF 110
	SHEET: 50 OF 98

HDD OOB TEMPERATURE SENSING



DRIVE ACTIVE = VALID SIGNAL PROTOCOL BETWEEN 0-2.0V.
DRIVE ASLEEP = HDD DRIVES HDD_OOB_TEMP LOW
DRIVE ABSENT = OOB IS PULLED HIGH UNLESS PCH DETERMINES SSD PRESENT AND DRIVES USE_HDD_OOB_L LOW WHICH THEN PULLS HDD_OOB_TEMP LOW.

NOTE: WILL BE CONNECTED TO SATA PWR CONNECTOR PIN 11
THIS PIN IS ORIGINALLY INTENDED FOR HDD LED OUTPUT,
AND ALSO FOR HDD STAGGERED PIN UP (FLOATING) OR IMMEDIATE SPIN-UP (GROUND).
BOTH FUNCTIONS NOT USED.

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE: HDD OOB SENSE

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

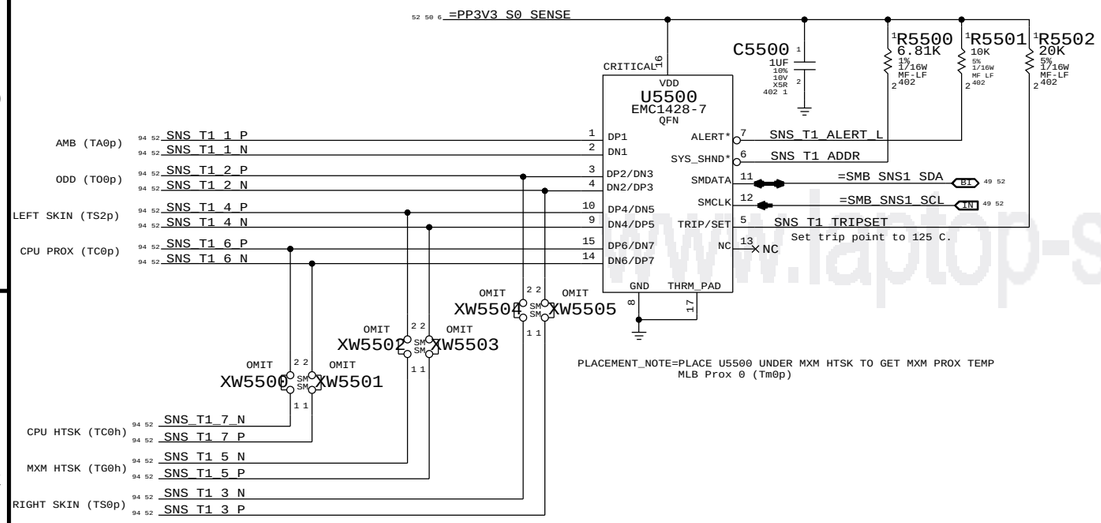
REVISION: 11.1.0

BRANCH:

PAGE: 54 OF 110

SHEET: 51 OF 98

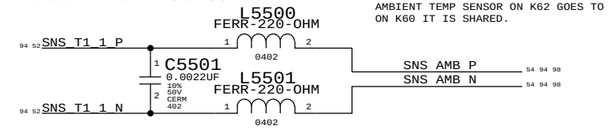
SNS T1: PRODUCTION TEMP SENSOR IC



PLACEMENT_NOTE=PLACE U5500 UNDER MXM HTSK TO GET MXM PROX TEMP
MLB Prox 0 (Tm0p)

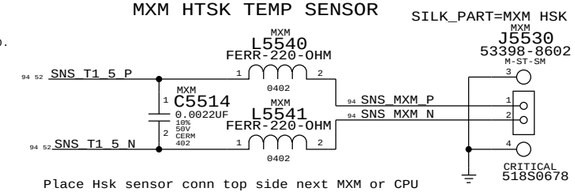
EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

AMBIENT TEMP SENSOR



AMBIENT TEMP SENSOR ON K62 GOES TO J5500.
ON K60 IT IS SHARED.

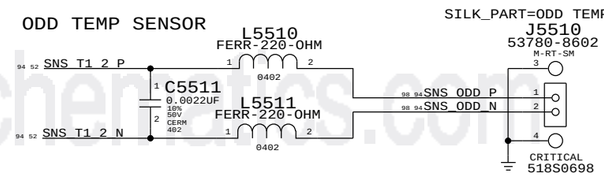
MXM HTSK TEMP SENSOR



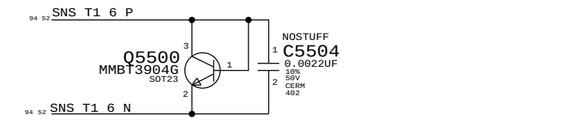
Place Hsk sensor conn top side next MXM or CPU

518S0677

ODD TEMP SENSOR

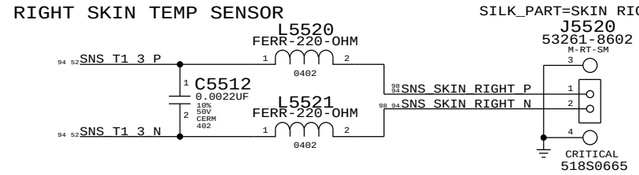


CPU PROXIMITY TEMP SENSOR

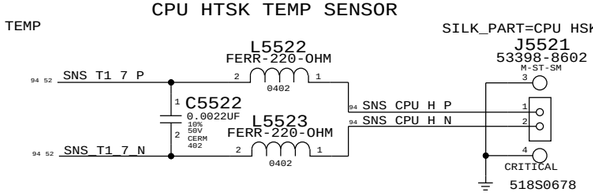


Place Q5500 (CPU Proximity Sensor) at the solder side
at edge near backer plate of CPU to replace HeatSink Temp Sensor

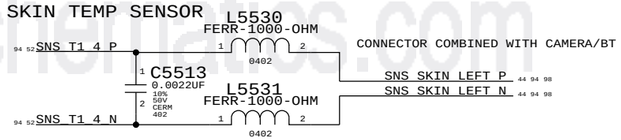
RIGHT SKIN TEMP SENSOR



CPU HTSK TEMP SENSOR



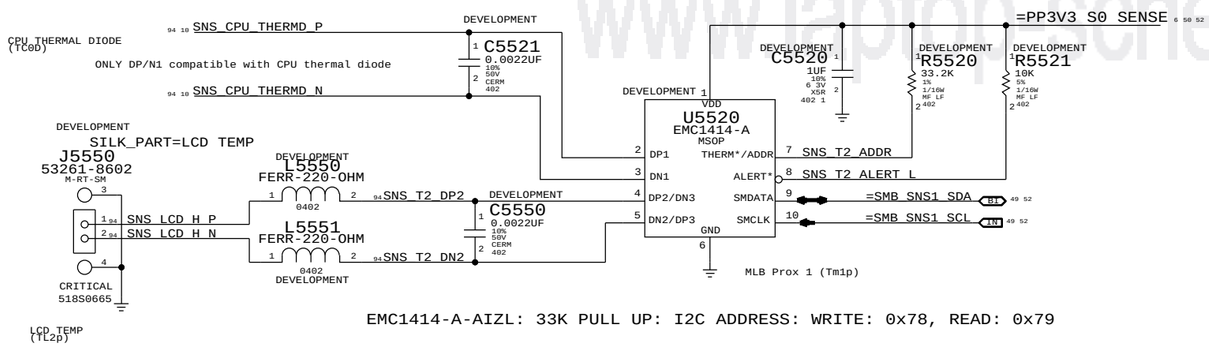
LEFT SKIN TEMP SENSOR



CONNECTOR COMBINED WITH CAMERA/BT

THIS PAGE DIFFERENT BETWEEN K60 AND K62.

SNS T2: DEVELOPMENT TEMP SENSOR IC



MLB Prox 1 (Tm1p)

EMC1414-A-AIZL: 33K PULL UP: I2C ADDRESS: WRITE: 0x78, READ: 0x79

SYNC MASTER=K60 MARK	SYNC DATE=01/06/2011
PAGE TITLE: TEMP SENSORS	
Apple Inc.	DRAWING NUMBER: 051-8115 SIZE: D
	REVISION: 11.1.0
	BRANCH:
	PAGE: 55 OF 110
	SHEET: 52 OF 98

FAN 0

=PP12V_S0_FAN

R5602 1.5K 5% 1/10W MF-LF 1206

=PP3V3_S0_FAN

R5606 10K 5% 1/10W MF-LF 402

SMC_FAN_0_CTL

Q5602 2N7002 SOT23-HF1

F0_VOLTAGE8R5

R5605 3.9K 5% 1/8W MF-LF 805

F0_GATESLOWDN

R5603 1.5K 5% 1/8W MF-LF 805

C5601 0.47UF 10% 16V X7R 805

CRITICAL Q5600 NTHS5443T1H 1206A-03-HF

C5606 4.7UF 20% 16V CERM 1206-1

C5607 0.01UF 20% 16V CERM 402

CRITICAL L5610 220-OHM-1.4A 0603

PP12V_S0_FAN0_L

MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=12V

D5600 MMBD914XG SOT23

C5602 100UF 20% 16V TANT 6.3X5.5-SM1-HF

MIN_NECK_WIDTH=0.25MM
MIN_LINE_WIDTH=0.5MM

FAN_0_PWR

CRITICAL L5620 220-OHM-1.4A 0603

MIN_NECK_WIDTH=0.25MM
MIN_LINE_WIDTH=0.5MM

FAN_0_PWR_L

FAN_TACH0_L

=PP3V3_S0_FAN

R5600 10K 5% 1/16W MF-LF 402

R5699 47K 5% 1/16W MF-LF 402

SMC_FAN_0_TACH

FAN_TACH0

NOTE: ADDED TO PROTECT SMC

CRITICAL L5600 FERR-220-OHM 0402

CRITICAL J5600 53780-8604 M-RT-SM

1 MOTOR CONTROL
2 TACH
3 GND
4 12V DC
6 518S0730

FAN_0_GND
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

R5620 0 5% 1/10W MF-LF 603

PLACEMENT_NOTE=PLACE R5620 CLOSE TO J5600 Pin3

FAN 1

=PP12V_S0_FAN

R5610 1.5K 5% 1/8W MF-LF 1206

=PP3V3_S0_FAN

R5611 10K 5% 1/10W MF-LF 402

SMC_FAN_1_CTL

Q5605 2N7002 SOT23-HF1

F1_VOLTAGE8R5

R5609 3.9K 5% 1/8W MF-LF 805

F1_GATESLOWDN

R5607 1.5K 5% 1/8W MF-LF 805

C5603 0.47UF 10% 16V X7R 805

CRITICAL Q5603 NTHS5443T1H 1206A-03-HF

C5608 2.2UF 10% 16V X5R 603

C5628 2.2UF 10% 16V X5R 603

C5609 0.01UF 20% 16V CERM 402

CRITICAL L5630 220-OHM-1.4A 0603

PP12V_S0_FAN1_L

MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=12V

D5601 MMBD914XG SOT23

C5605 100UF 20% 16V TANT D-HF

MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

FAN_1_PWR

CRITICAL L5640 220-OHM-1.4A 0603

MIN_NECK_WIDTH=0.25MM
MIN_LINE_WIDTH=0.5MM

FAN_1_PWR_L

FAN_TACH1_L

=PP3V3_S0_FAN

R5601 10K 5% 1/16W MF-LF 402

R5698 47K 5% 1/16W MF-LF 402

SMC_FAN_1_TACH

FAN_TACH1

C5605 IS POLY-TANT BECAUSE IT MUST BE PLACED ON THE BOTTOM

CRITICAL L5601 FERR-220-OHM 0402

CRITICAL J5601 53780-8604 M-RT-SM

1 MOTOR CONTROL
2 TACH
3 GND
4 12V DC
6 518S0730

FAN_1_GND
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

R5630 0 5% 1/10W MF-LF 603

PLACEMENT_NOTE=PLACE R5630 CLOSE TO J5601 Pin3

ODD FAN

HD FAN

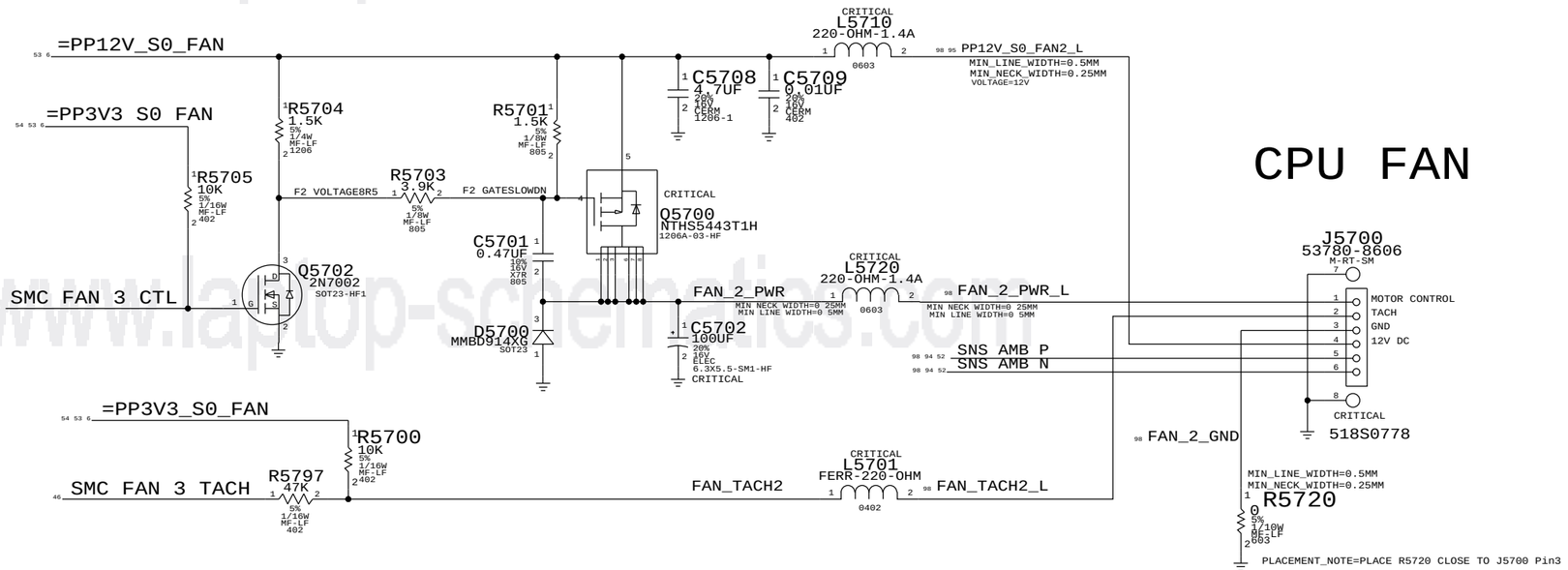
SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: HD AND OD FAN

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 56 OF 110
SHEET: 53 OF 98

SMC'S FAN3 OUTPUT CONTROL FAN 2



CPU FAN

FAN 3 SMC CONTROL (UNUSED)

SYNC MASTER=K60 JERRY SYNC DATE=01/06/2011

PAGE TITLE: CPU FAN

Apple Inc.

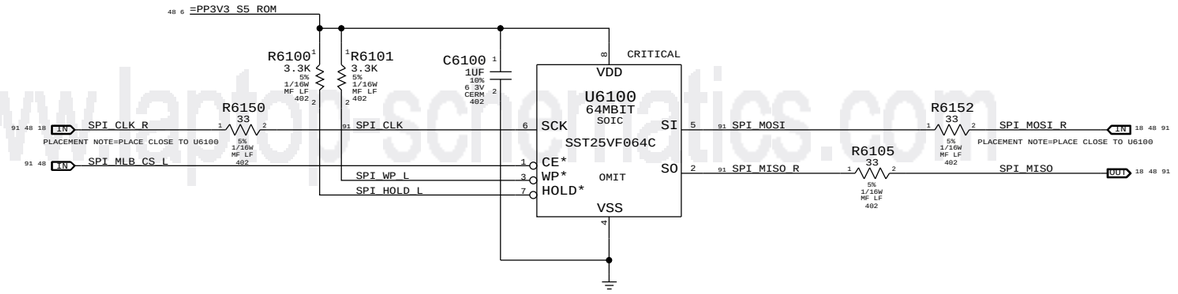
DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 57 OF 110

SHEET: 54 OF 98



SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE

SPI ROM

Apple Inc.

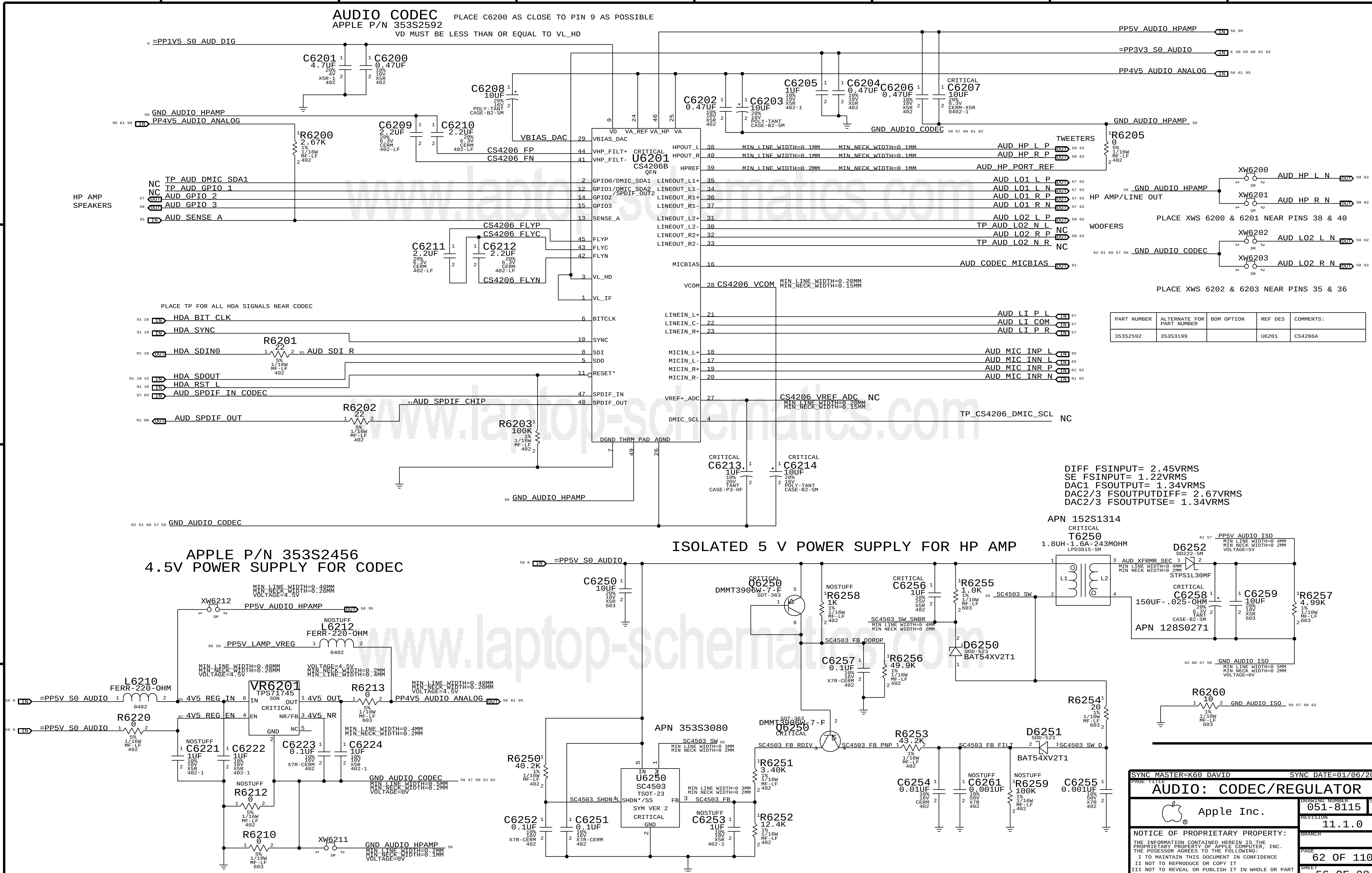
DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

BRANCH

PAGE 61 OF 110

SHEET 55 OF 98



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S2592	353S3199		U6201	CS4206A

SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

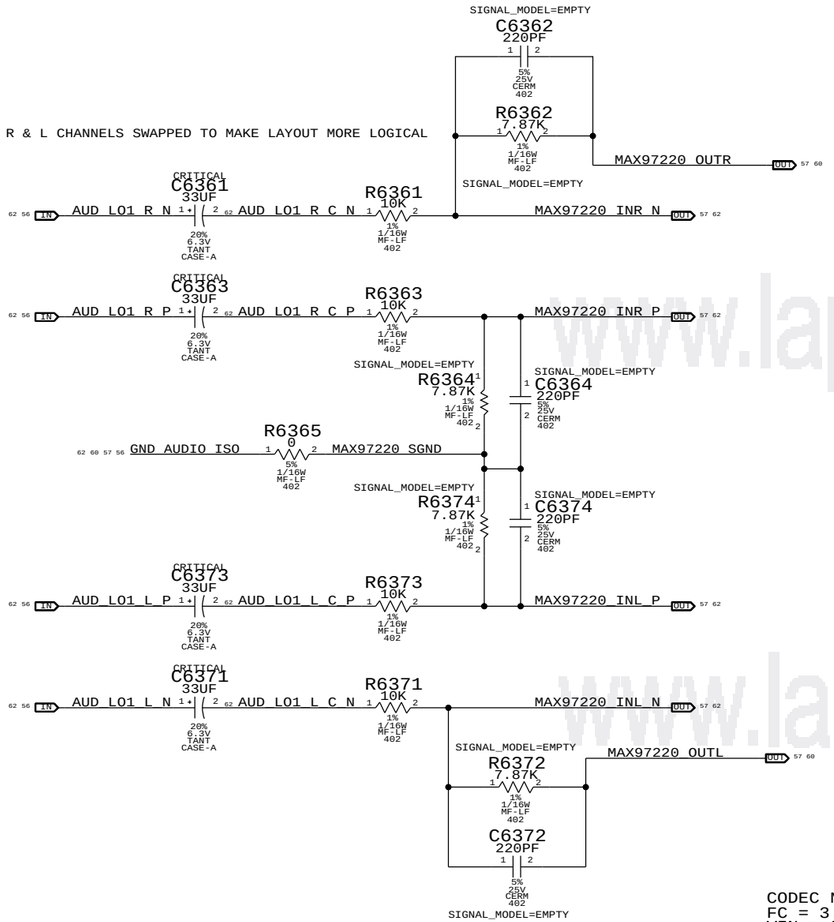
PAGE TITLE
AUDIO: CODEC/REGULATOR

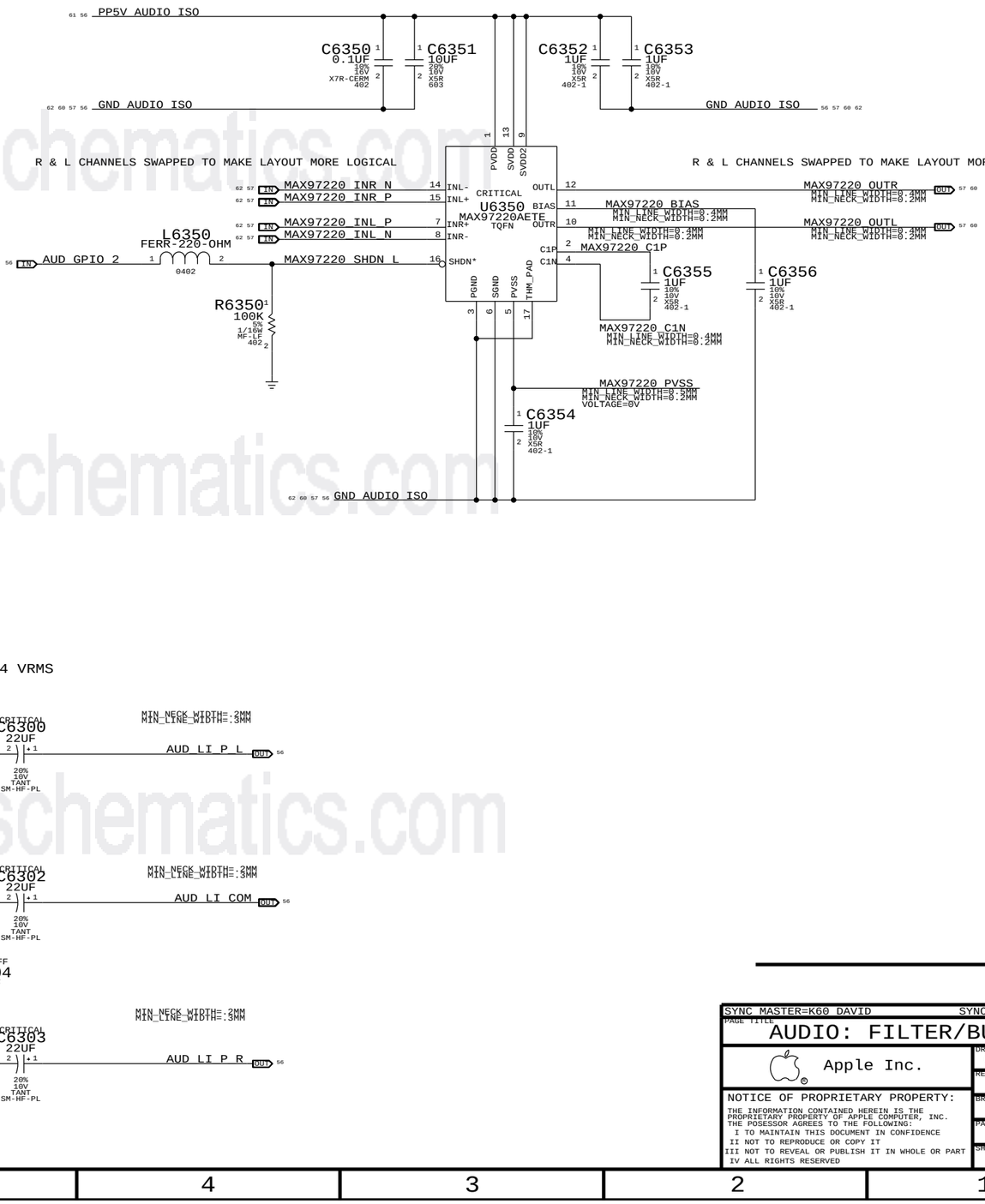
Apple Inc.

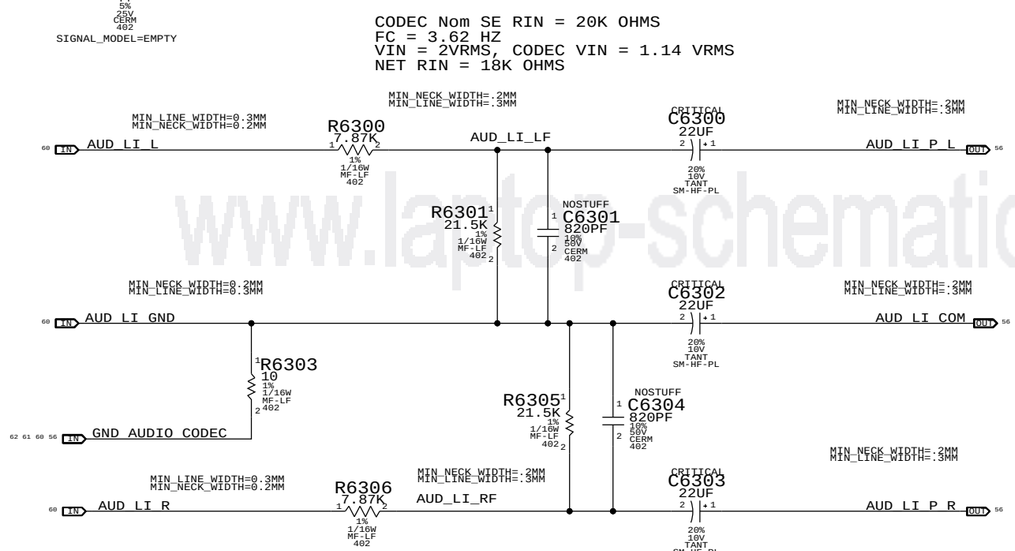
DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

BRANCH







SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE

AUDIO: FILTER/BUFFER

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

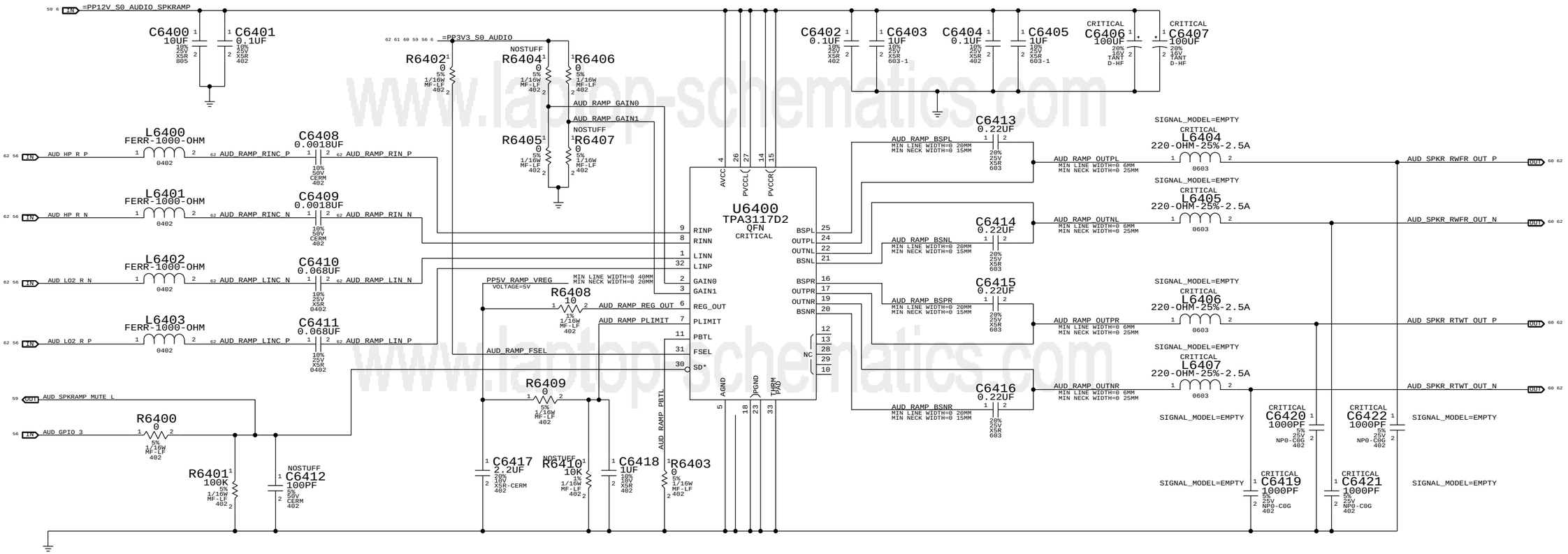
BRANCH

PAGE 63 OF 110

SHEET 57 OF 98

RIGHT CH SPEAKER AMP
APPLE P/N 353S3069

R6402 = HIGH = 400 KHZ
SPEAKER AMP GAIN = +15.2 DB
SPEAKER AMP RIN = 104K NOMINAL W/ +15.2 DB GAIN
FC_HPF, TWEETERS = ~850 HZ (0.0018 UF)
FC_HPF, WOOFERS = ~22.5 HZ (0.068 UF)



SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

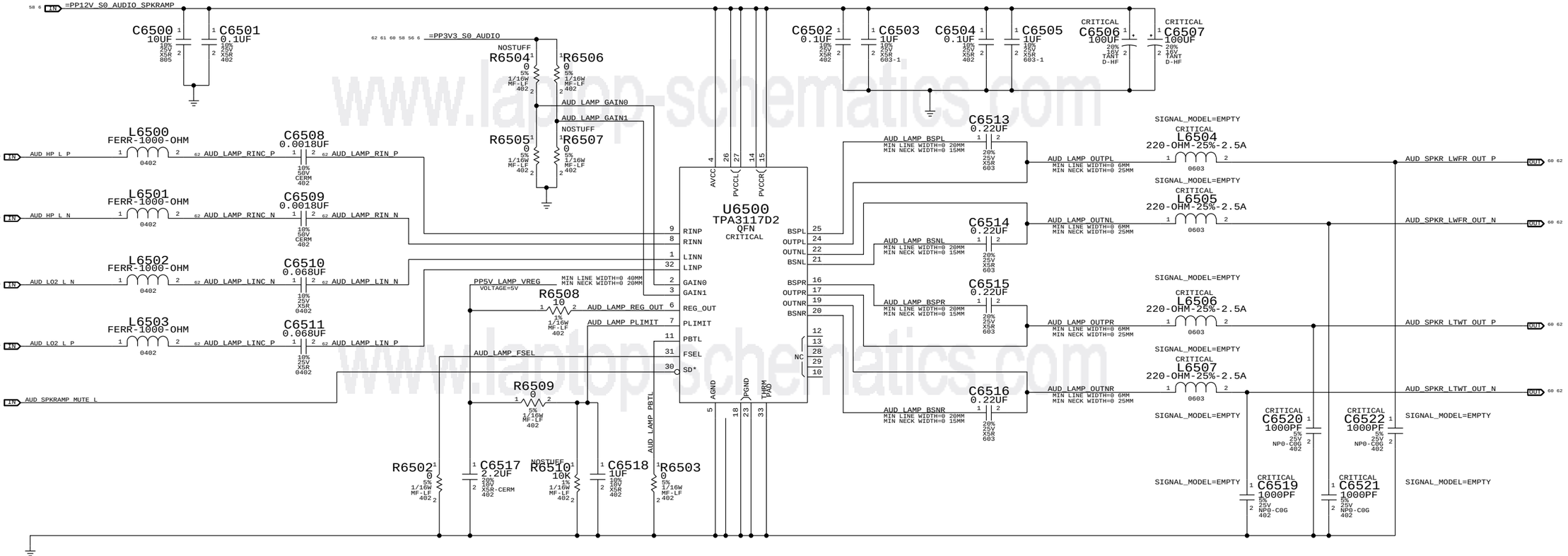
PAGE TITLE
AUDIO: SPEAKER AMP 1

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 64 OF 110
SHEET 58 OF 98

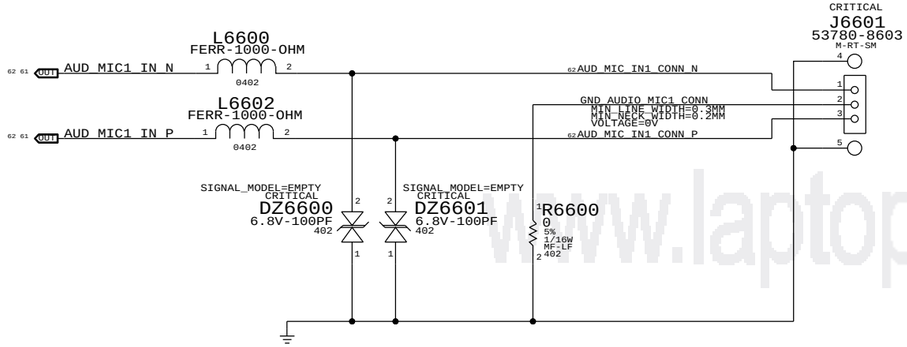
LEFT CH SPEAKER AMP
APPLE P/N 353S3069

R6502 = LOW = 300 KHZ
SPEAKER AMP GAIN = +15.2 DB
SPEAKER AMP RIN = 104K NOMINAL W/ +15.2 DB GAIN
FC_HPF, TWEETERS = ~850 HZ (0.0018 UF)
FC_HPF, WOOFERS = ~22.5 HZ (0.068 UF)

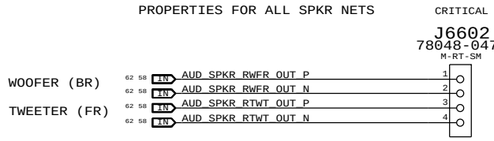


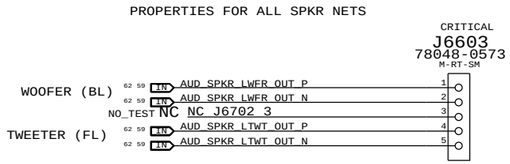
SYNC MASTER=K60 DAVID	SYNC DATE=01/06/2011
PAGE TITLE: AUDIO: SPEAKER AMP	
Apple Inc.	DRAWING NUMBER: 051-8115 SIZE: D
	REVISION: 11.1.0
	BRANCH:
	PAGE: 65 OF 110
	SHEET: 59 OF 98

INTERNAL MIC CON
APPLE P/N 518S0677

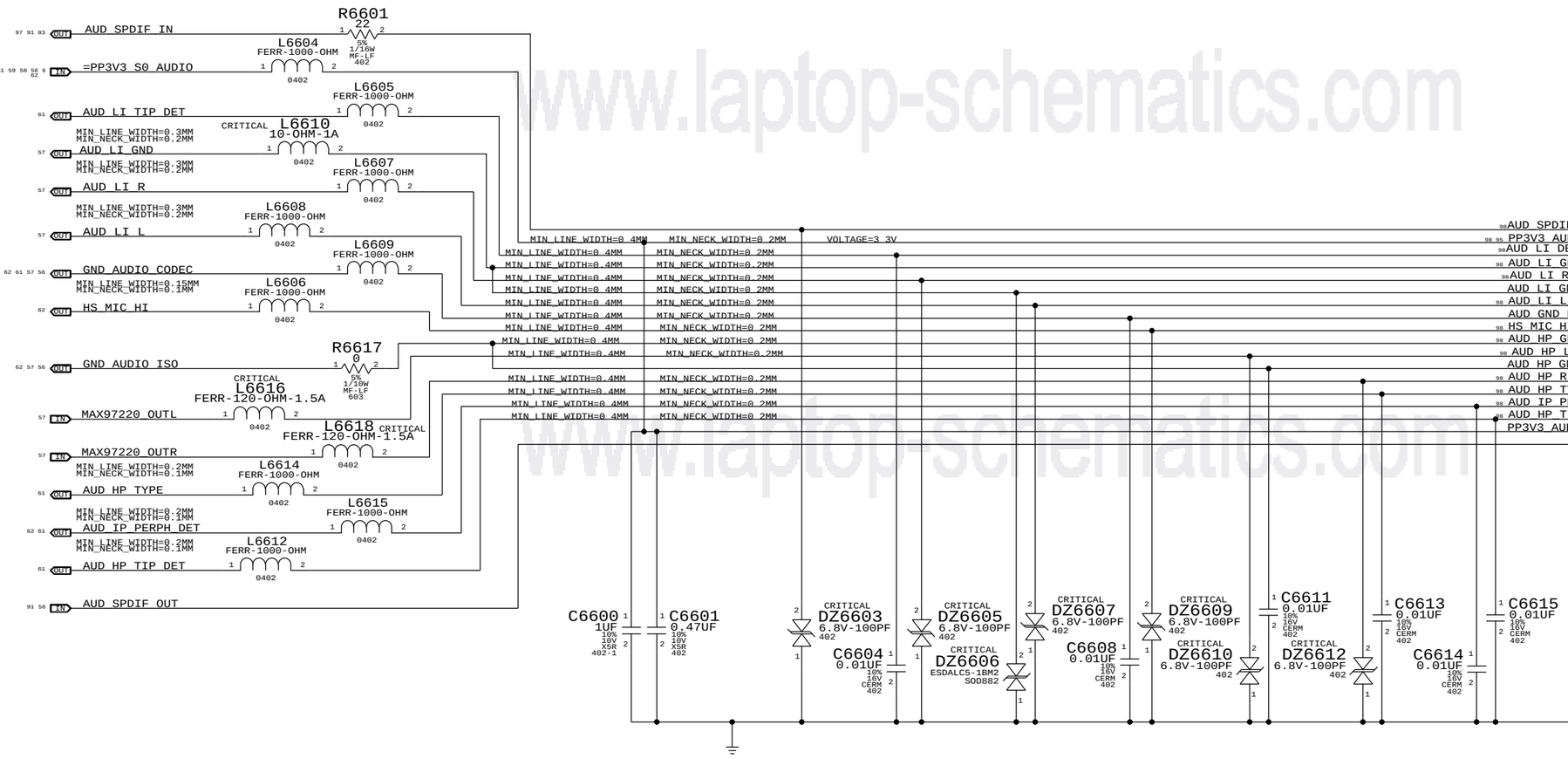


SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656





REMOTE I/O CONNECTOR
APPLE P/N 518S0723



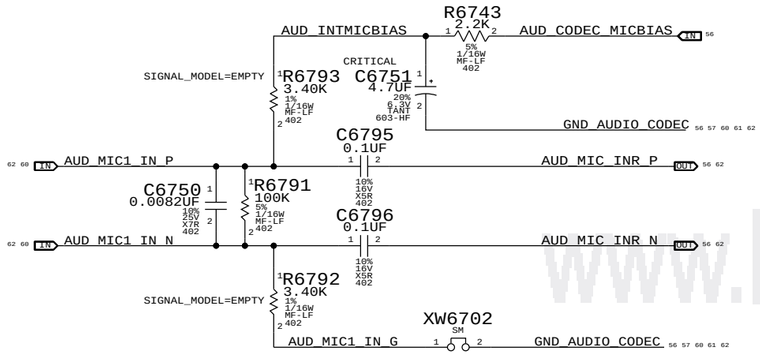
SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE
Audio: MLB to I/O Conn.

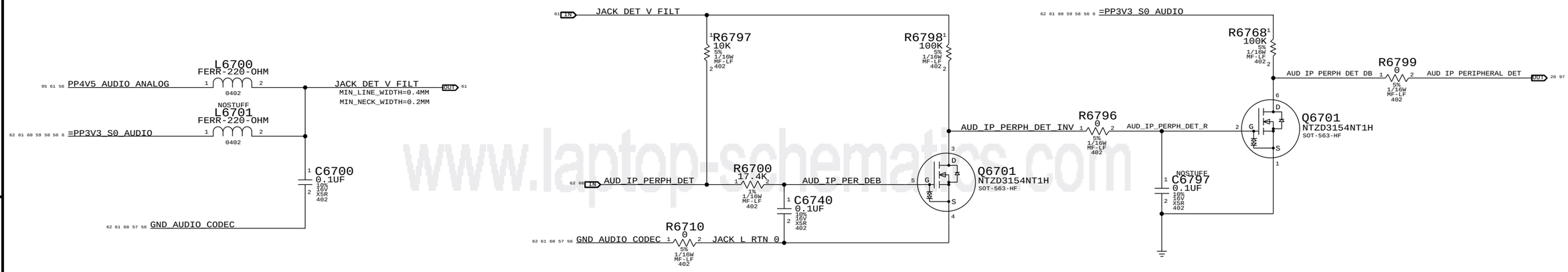
Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 66 OF 110
SHEET 60 OF 98

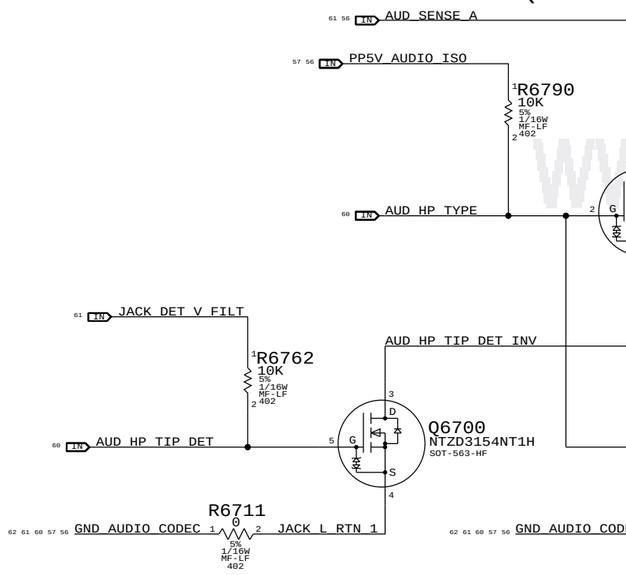
Internal Microphone Impedance Matching



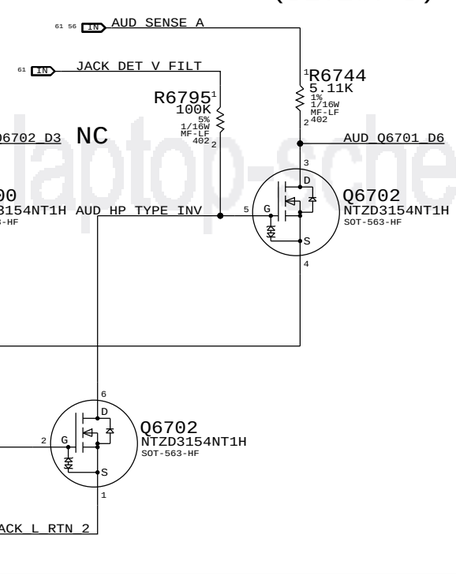
IPHS HS Detect Debounce CKT



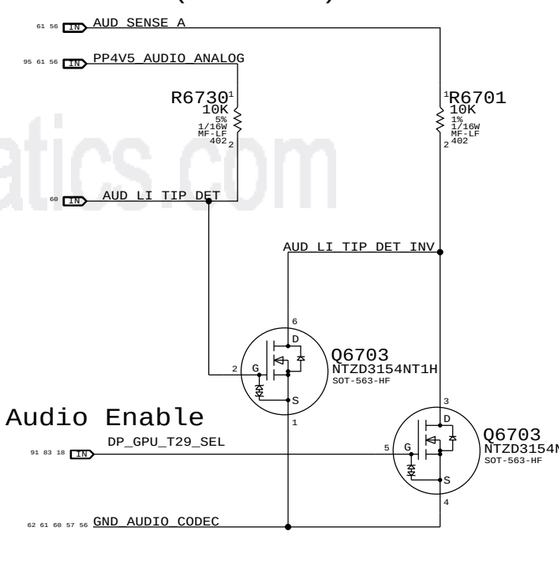
Digital Out (DETECT B)



Headphone Out (DETECT D)



LI Insert Detect (DETECT C)



SYNC MASTER=K60 DAVID SYNC DATE=11/24/2010

PAGE TITLE
AUDIO: Detects/Grounding

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 67 OF 110
SHEET 61 OF 98

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	0X0A (D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X02 (2)	0X02 (2)	0X09 (09)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0E (14,LEFT & RIGHT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	COUGAR POINT GPIO 16	COUGAR POINT GPIO 5 (PCVR_INT) COUGAR POINT GPIO 3 (PERIPH_DET)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0 1 MM	?
SPKROUT	*	0 2 MM	?

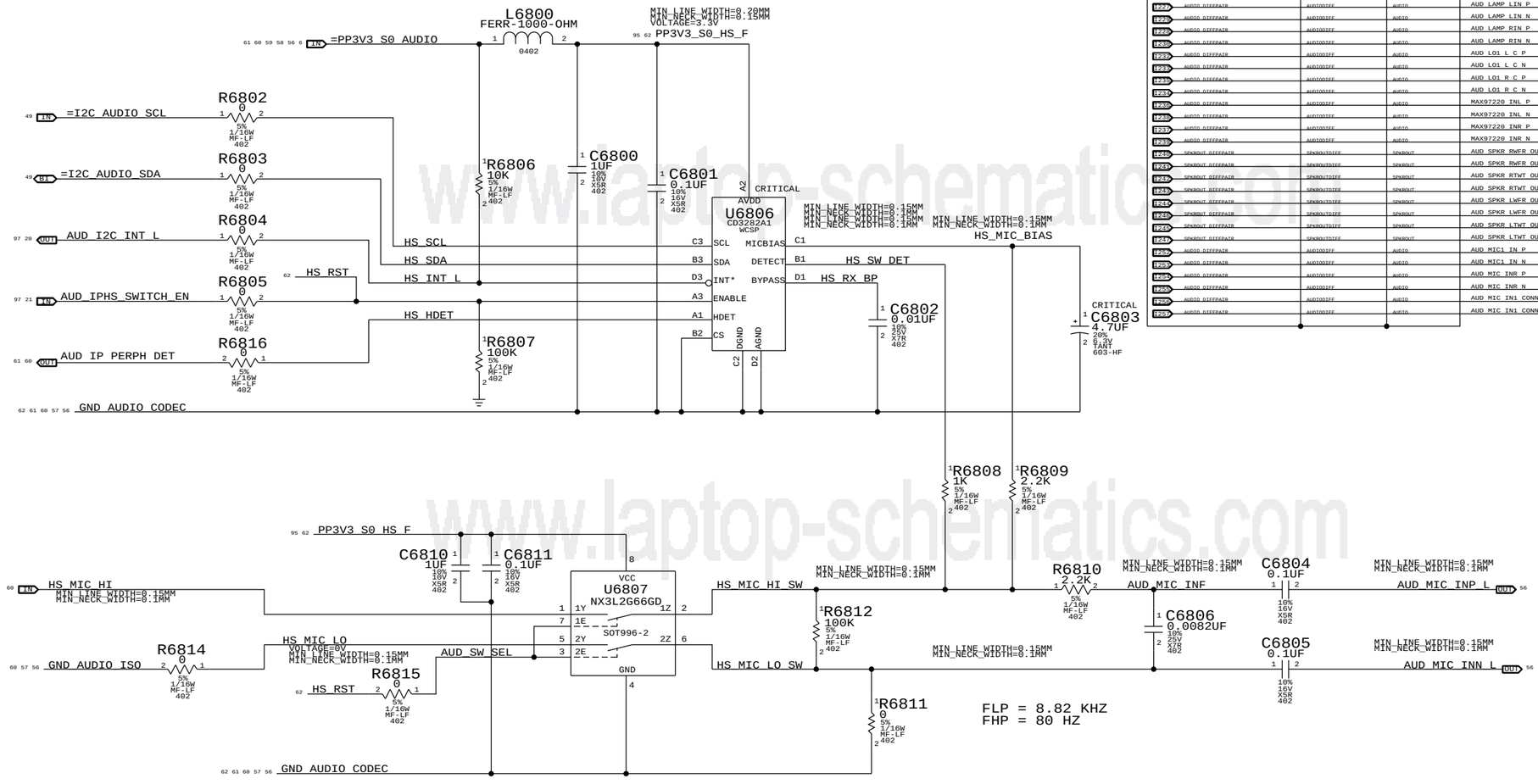
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0 1 MM	0 1 MM	10 MM	0 1 MM	0 1 MM
SPKROUTDIFF	*	Y	0 6 MM	0 25 MM	10 MM	0 2 MM	0 2 MM

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_L_P	56 59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_L_N	56 59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_R_P	56 58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_R_N	56 58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	56 57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	56 57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	56 57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	56 59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	56 58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	58
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	59
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	57
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	57
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	58 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	58 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	58 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	58 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	59 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	59 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	59 60
SPKROUT DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	59 60
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC1_IN_P	60 61
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC1_IN_N	60 61
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_P	56 61
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_N	56 61
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_IN1_CONN_P	60
AUDIO DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_IN1_CONN_N	60

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2640



SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE: AUDIO: Mikey

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 68 OF 110

SHEET: 62 OF 98

SLP_S4 ENABLES

MEMVTT_EN SEQUENCE

=PP3V3_S0_PWRCTL
R6951 10K 5% 1/16W MF-LF 402
R6952 10K 5% 1/16W MF-LF 402
NOSTUFF C6951 100PF 5% 50V CERM 402
PM_EN_DDRVTT_S0_REG
NOSTUFF C6953 0.1UF 10% 10V X5R 402
VTT_REG_PGOOD_L
Q6911 MMDT3904-X-G SOT 363 LF
R6950 10K 5% 1/16W MF-LF 402
PM_PGOOD_P1V05_S0_REG
CPUVTT_REG_PGOOD_R
NOSTUFF C6952 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S5_PWRCTL
PM_SLP_S5_L
R6971 0 5% 1/16W MF-LF 402
NOSTUFF R6972 0 5% 1/16W MF-LF 402
PM_SLP_S4_L
PM_SLP_S4_1_L_R
74LVC08 TSSOP-HF U6900 08
S4_ENABLES

C6910 0.1UF 20% 10V CERM 402

R6911 33 5% 1/16W MF-LF 402
PM_EN_P3V3_S3_FET
Enable FET
R6912 33 5% 1/16W MF-LF 402
PM_EN_P5V_S3_REG
ENABLE REGULATOR

NOSTUFF C6920 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6921 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S5_PWRCTL
R6916 100K 5% 1/16W MF-LF 402
R6915 10K 5% 1/16W MF-LF 402
CPU_SKTOCC
CPU_SKTOCC_L
Q6910 2N7002 SOT23-HF1
NOSTUFF R6917 10K 5% 1/16W MF-LF 402

PLACE TOP SIDE
REWORK TO POWER UP WITH NO CPU

PM_PGOOD_P5V_S3_REG
R6970 0 5% 1/16W MF-LF 402
PM_EN_USB_PWR
NOSTUFF C6924 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S5_PWRCTL
PM_SLP_S4_L
74LVC08 TSSOP-HF U6900 08
PM_EN_DDR1V5_S3_REG
PM_PGOOD_P5V_S3_REG

NOSTUFF R6931 33 5% 1/16W MF-LF 402
PM_PGOOD_P3V3_S0_FET
PM_EN_P1V5_S0_FET

SLP_S3 ENABLES

=PP3V3_S5_PWRCTL
R6955 10K 5% 1/16W MF LF 402
P3V3_S5_PWRCTL_U6900_R
PGOOD_P12V_S0
74LVC08 TSSOP-HF U6900 08

NOSTUFF R6946 33 5% 1/16W MF-LF 402
PM_EN_P3V3_S0_FET
Enable FET
NOSTUFF R6947 33 5% 1/16W MF-LF 402
PM_EN_P5V_S0_FET
Enable FET

OTHER RAILS ENABLED BY P3V3_S0 AND P5V_S0:
PP1V8_S0 VREG (CPU PLL)

NOSTUFF R6944 33 5% 1/16W MF LF 402
NOSTUFF R6941 10K 5% 1/16W MF LF 402

PM_SLP_S3_BUF_L
Enable FET
PM_EN_P1V5_S0_FET
PM_EN_DDRVTT_S0_REG
Enable regulator

=PP12V_S0_PWRCTL
R6934 82K 5% 1/16W MF-LF 402
PM_PGOOD_P5V_S0_FET
R6935 33K 5% 1/16W MF-LF 402

=PM_SLP_S3_L
PM_PGOOD_DDR1V5_S3_REG
74LVC08 TSSOP-HF U6900 08
PM_EN_P12V_S0_FET

OPTION TO DELAY 1V8
R6932 33 5% 1/16W MF-LF 402
PM_PGOOD_P3V3_S0_FET
NOSTUFF R6990 33 5% 1/16W MF-LF 402
PM_PGOOD_P5V_S0_FET
PM_EN_P1V8_S0_REG
NOSTUFF C6994 0.47UF 10% 6.3V CERM-X5R 402

NOSTUFF C6947 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6944 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6941 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6945 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6946 0.47UF 10% 6.3V CERM-X5R 402

OPTIONAL SEQUENCE TO DELAY 3V,1V5
R6930 33 5% 1/16W MF-LF 402
PM_PGOOD_P5V_S0_FET
PM_EN_P3V3_S0_FET
R6933 33 5% 1/16W MF-LF 402
PM_PGOOD_P5V_S0_FET
PM_EN_P1V5_S0_FET

NOSTUFF R6942 33 5% 1/16W MF-LF 402
Enable regulator
PM_EN_P1V05_S0_REG
NOSTUFF C6942 1UF 10% 6.3V CERM 402
R6936 33 5% 1/16W MF-LF 402
PM_PGOOD_P3V3_S0_FET
OPTION TO DELAY 1V05

CPUVTT_VREG/ PCH CORE
NOTE: PM_PGOOD_P1V05_S0_REG ENABLES VCCSA REGULATOR CIRCUIT ON PAGE 70
PM_PGOOD_P1V05_S0_REG = =PM_EN_VCCSA_S0_CPU
MAKE_BASE=TRUE

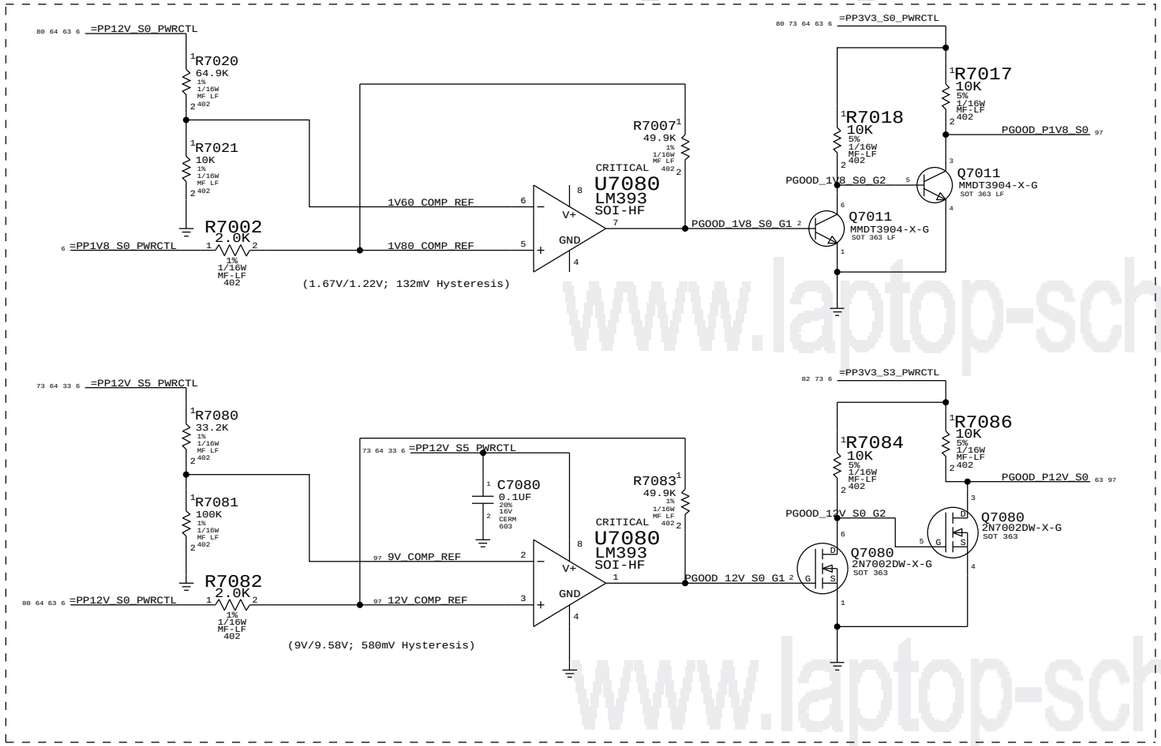
VCCSA REGULATOR
PM_PGOOD_PVCCSA_S0_REG = Enable regulator PM_EN_PVCORE_CPU
MAKE_BASE=TRUE
TO ENABLE OF CPU VCORE

SYNC_MASTER=K62 SYNC_DATE=01/06/2011
PAGE TITLE
POWER SEQUENCING ENABLES

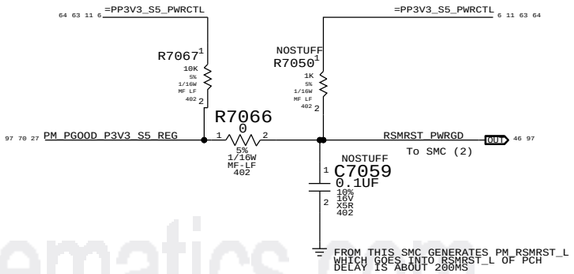
Apple Inc.

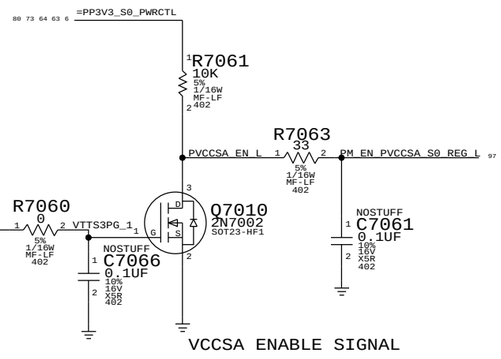
DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 69 OF 110
SHEET 63 OF 98

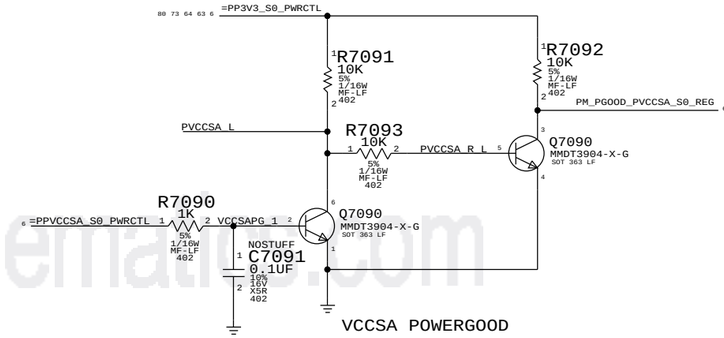
PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0

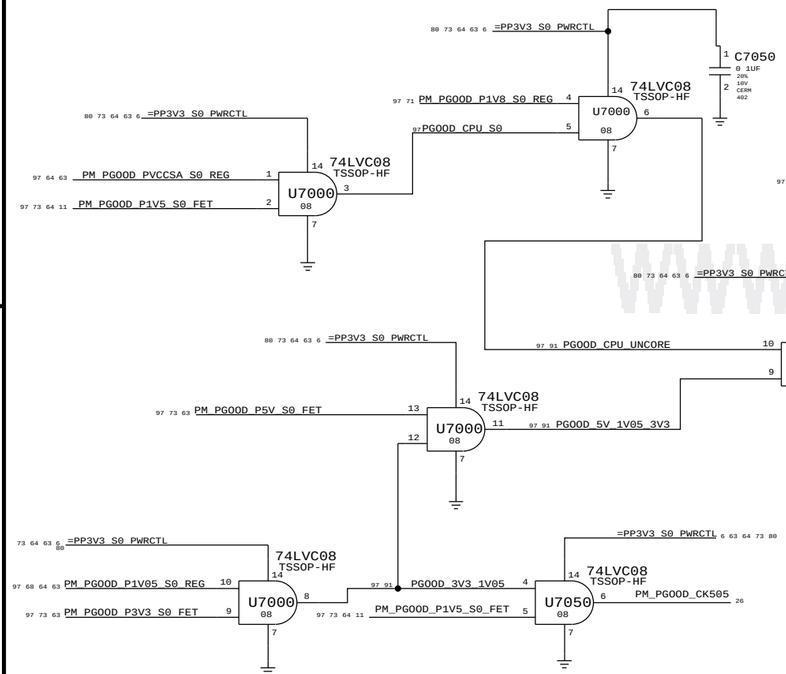


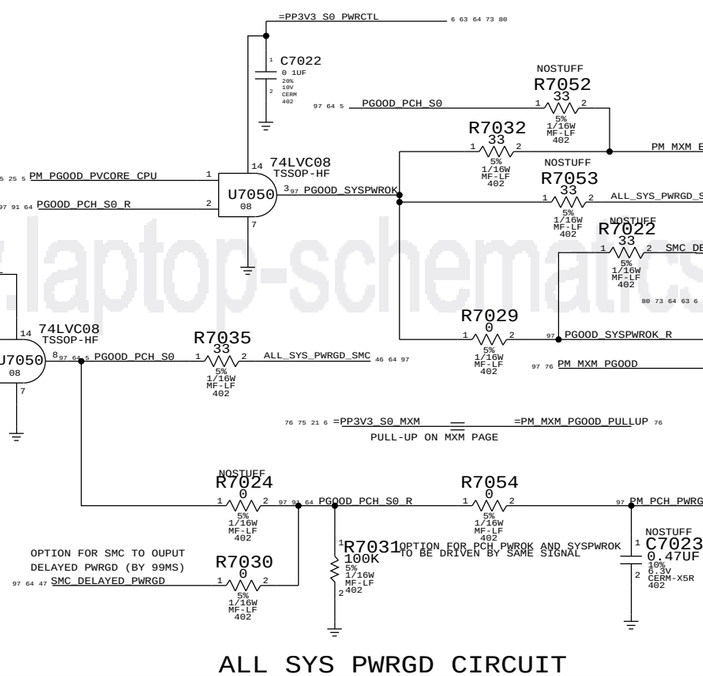
S0 RAILS PGOOD











ALL SYS PWRGD CIRCUIT

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: POWER SEQUENCING PGOOD

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DRAWING NUMBER: 051-8115 SIZE: D

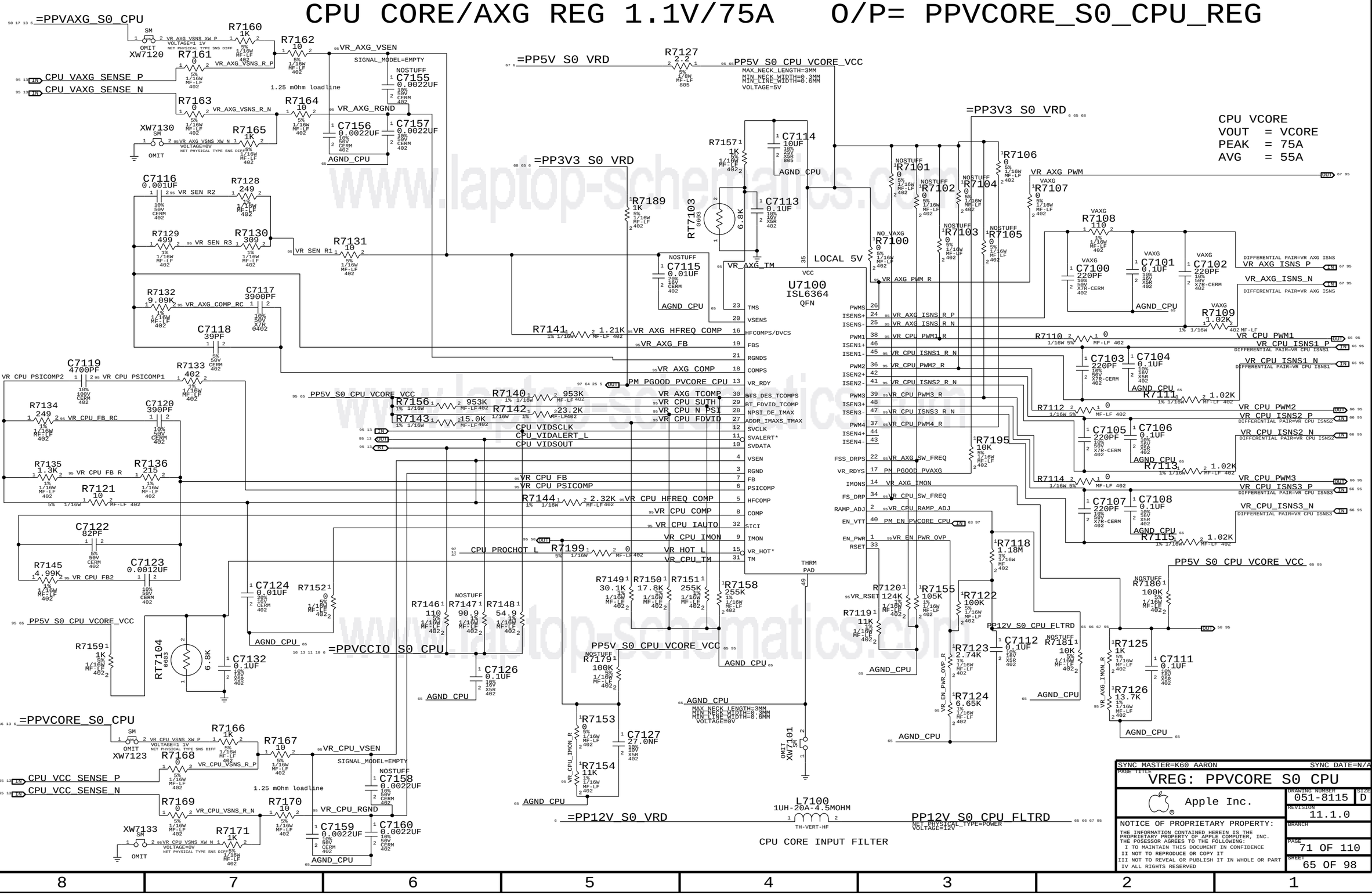
REVISION: 11.1.0

BRANCH:

PAGE: 70 OF 110

SHEET: 64 OF 98

CPU CORE/AXG REG 1.1V/75A O/P= PPVCORE_S0_CPU_REG



PHASE 1

PP12V_S0_CPU_FLTRD
NET_SPACING_TYPE=POWER
CRITICAL C7272 220UF 20% 16V ALUM-POLY 8X7-TH
CRITICAL C7270 220UF 20% 16V ALUM-POLY 8X7-TH
CRITICAL C7271 220UF 20% 16V ALUM-POLY 8X7-TH
R7202 10 5% 1/10W MF-LF 603
R7205 0 5% 1/10W MF-LF 603
NOSTUFF R7201 10 5% 1/10W MF-LF 603
VR_CPU_DRV1_VCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
VR_CPU_DRV1_UVCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
VR_CPU_DRV1_PVCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
C7201 1UF 10% 16V X5R 603
U7201 ISL6622 DFN
VCC UVCC LVCC
GDSEL BOOT UGATE PHASE LGATE PWM GND THRML PAD
C7202 1UF 10% 16V X5R 603
C7200 1UF 10% 16V X5R 603
NOSTUFF R7207 0 5% 1/10W MF-LF 603
VR_CPU_DRV1_GDSEL
VR_CPU_PWM1
R7204 0 5% 1/10W MF-LF 603
VR_CPU_BOOT1_RC
NET_PHYSICAL_TYPE=VR_CTL_PHY NET_SPACING_TYPE=VR_CONTROL DIDT=TRUE NO_TEST=TRUE
C7203 0.22UF 10% 16V X7R 603
VR_CPU_DRV1_BOOT
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL NO_TEST=TRUE
VR_CPU_DRV1_UGATE
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_PHASE1
NET_PHYSICAL_TYPE=POWER DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
VR_CPU_DRV1_LGATE
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
376S0772
CRITICAL Q7201 IRF6710 S1
SWITCH_NODE=TRUE
CRITICAL L7201 0.24UH+/-20%-0.000420HM-40A SDP1108M-TH
PPVCORE_S0_CPU_REG1
CRITICAL C7205 220UF 20% 16V ALUM-POLY 8X7-TH
CRITICAL C7206 10UF 10% 16V X5R-CERM 0805
CRITICAL C7215 10UF 10% 16V X5R-CERM 0805
C7207 1UF 10% 16V X5R 603
C7281 1UF 10% 16V X5R 603
C7210 0.001UF 10% 50V X7R 402
C7211 1UF 10% 25V X5R 402
THESE TWO CAPS ARE FOR EMC
CRITICAL R7208 0.0005 1% 1W MF 0612
PPVCORE_S0_CPU_REG
NOSTUFF R7206 2.2 5% 1/8W MF-LF 805
VR_CPU_PH1_SNUB
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
CRITICAL Q7202 IRF6795 DIRECTFET-MX
C7208 0.001UF 10% 50V CERM 402 NOSTUFF
376S0771
VR_CPU_ISNS1_P
VR_CPU_ISNS1_N

PHASE 2

R7222 10 5% 1/10W MF-LF 603
NOSTUFF R7225 0 5% 1/10W MF-LF 603
R7221 10 5% 1/10W MF-LF 603
VR_CPU_DRV2_VCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
VR_CPU_DRV2_UVCC
NET_PHYSICAL_TYPE=POWER
VR_CPU_DRV2_PVCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
C7221 1UF 10% 16V X5R 603
U7221 ISL6612 QFN1
VCC PVCC
PWM BOOT UGATE PHASE LGATE NC NC GND THRML PAD
C7222 1UF 10% 16V X5R 603
NOSTUFF C7220 1UF 10% 16V X5R 603
VR_CPU_PWM2
VR_CPU_DRV2_GDSEL
NOSTUFF R7227 0 5% 1/10W MF-LF 603
R7224 0 5% 1/10W MF-LF 603
VR_CPU_BOOT2_RC
NET_PHYSICAL_TYPE=VR_CTL_PHY NET_SPACING_TYPE=VR_CONTROL DIDT=TRUE NO_TEST=TRUE
C7223 0.22UF 10% 16V X7R 603
VR_CPU_DRV2_BOOT
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL NO_TEST=TRUE
VR_CPU_DRV2_UGATE
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_PHASE2
NET_PHYSICAL_TYPE=POWER DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
VR_CPU_DRV2_LGATE
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
376S0772
CRITICAL Q7221 IRF6710 S1
SWITCH_NODE=TRUE
CRITICAL L7221 0.24UH+/-20%-0.000420HM-40A SDP1108M-TH 152-0118
PPVCORE_S0_CPU_REG2
CRITICAL C7225 220UF 20% 16V ALUM-POLY 8X7-TH
CRITICAL C7226 10UF 10% 16V X5R-CERM 0805
CRITICAL C7229 10UF 10% 16V X5R-CERM 0805
C7282 1UF 10% 16V X5R 603
C7227 1UF 10% 16V X5R 603
C7230 0.001UF 10% 50V X7R 402
C7231 1UF 10% 25V X5R 402
THESE TWO CAPS ARE FOR EMC
CRITICAL R7228 0.0005 1% 1W MF 0612
PPVCORE S0 CPU REG
NOSTUFF R7226 2.2 5% 1/8W MF-LF 805
VR_CPU_PH2_SNUB
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
CRITICAL Q7222 IRF6795 DIRECTFET-MX
C7228 0.001UF 10% 50V CERM 402 NOSTUFF
376S0771
VR_CPU_ISNS2_P
VR_CPU_ISNS2_N

PHASE 3

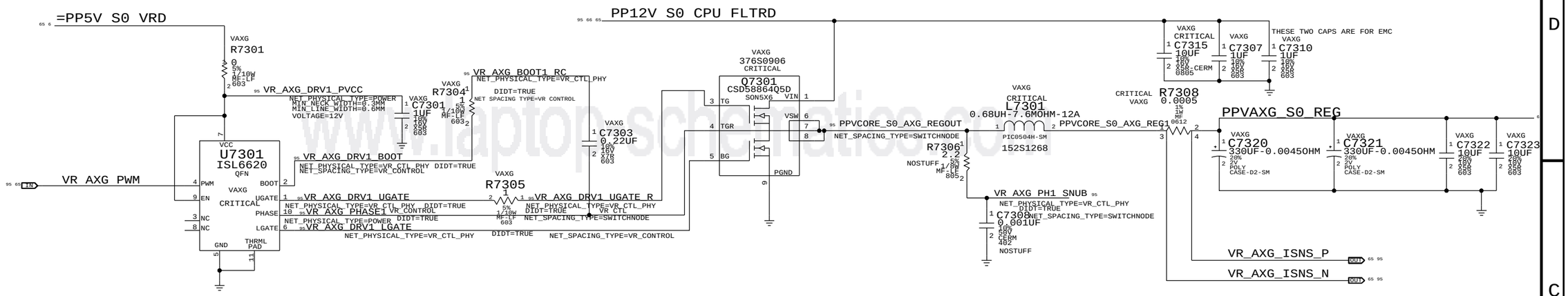
376S0772
R7242 10 5% 1/10W MF-LF 603
NOSTUFF R7245 0 5% 1/10W MF-LF 603
R7241 10 5% 1/10W MF-LF 603
VR_CPU_DRV3_VCC
NO_TEST=TRUE NET_PHYSICAL_TYPE=POWER
VR_CPU_DRV3_UVCC
NET_PHYSICAL_TYPE=POWER
VR_CPU_DRV3_PVCC
NET_PHYSICAL_TYPE=POWER NO_TEST=TRUE
C7241 1UF 10% 16V X5R 603
U7241 ISL6612 QFN1
VCC PVCC
PWM BOOT UGATE PHASE LGATE NC NC GND THRML PAD
C7242 1UF 10% 16V X5R 603
NOSTUFF C7240 1UF 10% 16V X5R 603
VR_CPU_PWM3
VR_CPU_DRV3_GDSEL
NOSTUFF R7247 0 5% 1/10W MF-LF 603
R7244 0 5% 1/10W MF-LF 603
VR_CPU_BOOT3_RC
NET_PHYSICAL_TYPE=VR_CTL_PHY NET_SPACING_TYPE=VR_CONTROL DIDT=TRUE NO_TEST=TRUE
C7243 0.22UF 10% 16V X7R 603
VR_CPU_DRV3_BOOT
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_DRV3_UGATE
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
VR_CPU_PHASE3
NET_PHYSICAL_TYPE=POWER DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
VR_CPU_DRV3_LGATE
NO_TEST=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
CRITICAL Q7241 IRF6710 S1
SWITCH_NODE=TRUE
CRITIICAL L7241 0.24UH+/-20%-0.000420HM-40A SDP1108M-TH 152-0118
PPVCORE_S0_CPU_REG3
CRITICAL C7245 220UF 20% 16V ALUM-POLY 8X7-TH
CRITICAL C7246 10UF 10% 16V X5R-CERM 0805
CRITICAL C7249 10UF 10% 16V X5R-CERM 0805
C7283 1UF 10% 16V X5R 603
C7247 1UF 10% 16V X5R 603
C7250 0.001UF 10% 50V X7R 402
C7251 1UF 10% 25V X5R 402
THESE TWO CAPS ARE FOR EMC
CRITICAL R7248 0.0005 1% 1W MF 0612
PPVCORE_S0_CPU_REG
NOSTUFF R7246 2.2 5% 1/8W MF-LF 805
VR_CPU_PH3_SNUB
NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE NET_SPACING_TYPE=SWITCHNODE
CRITICAL Q7242 IRF6795 DIRECTFET-MX
C7248 0.001UF 10% 50V CERM 402 NOSTUFF
376S0771
VR_CPU_ISNS3_P
VR_CPU_ISNS3_N

OUTPUT BULK DECOUPLING:

128S0209
PPVCORE S0 CPU REG
75A MAX
C7260 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7261 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7262 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7263 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7264 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7265 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

SYNC MASTER=K62 SYNC DATE=01/06/2011
PAGE TITLE
VREG: CPU CORE - PHASES 1-3
Apple Inc.
DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 72 OF 110
SHEET 66 OF 98

AXG PHASE (MAX 15A)



SYNC MASTER=K60_AARON SYNC DATE=N/A

PAGE TITLE
VREG:AXG PHASE/CORE - CAPS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

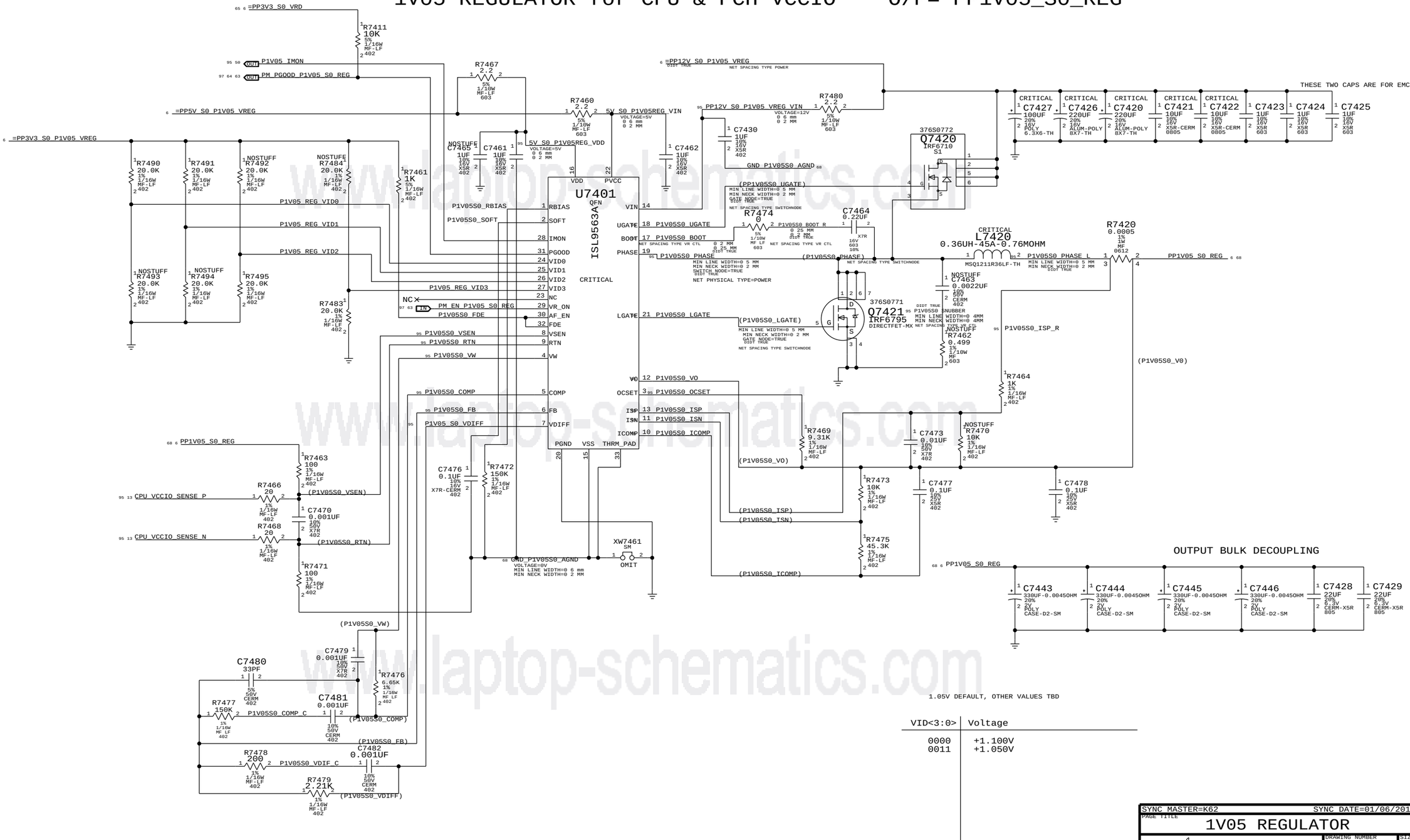
REVISION 11.1.0

BRANCH

PAGE 73 OF 110

SHEET 67 OF 98

1V05 REGULATOR for CPU & PCH VCCIO O/P= PP1V05_S0_REG



1.05V DEFAULT, OTHER VALUES TBD

VID<3:0>	Voltage
0000	+1.100V
0011	+1.050V

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: 1V05 REGULATOR

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

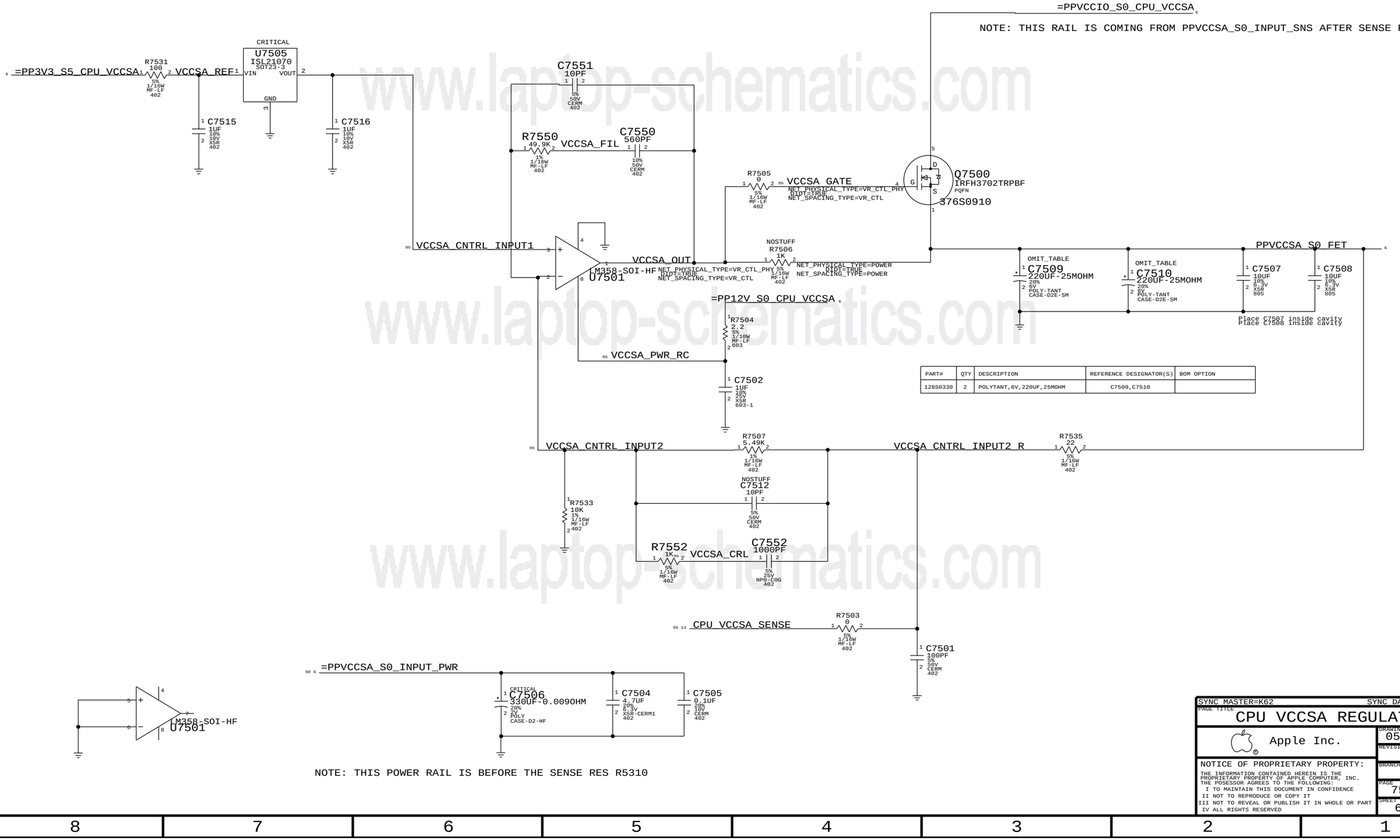
REVISION: 11.1.0

BRANCH:

PAGE: 74 OF 110

SHEET: 68 OF 98

CPU VCCSA 0.925V (8.8A MAX)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0330	2	POLYTANT,6V,220UF,25MOHM	C7509,C7510	

NOTE: THIS POWER RAIL IS BEFORE THE SENSE RES R5310

SYNC MASTER=K62 SYNC DATE=11/15/2010

PAGE TITLE

CPU VCCSA REGULATOR

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

BRANCH

PAGE 75 OF 110

SHEET 69 OF 98

3V3 S5 REGULATOR

5V S3 REGULATOR

Power Rating ?

3V3 OUTPUT

5V OUTPUT

=PP12V_S5_P5VS3_VREG

NET SPACING TYPE=POWER

EMC CAPS
PLACE CLOSE TO FET

C7718 100UF 20% 16V POLY 6 3X6 TH
C7712 10UF 10% 16V X5R CERM 0805
C7710 10UF 10% 16V X5R CERM 0805
C7711 1UF 10% 16V X5R 603
C7722 1UF 10% 16V X5R 603

NET_PHYSICAL_TYPE=POWER
DIDT TRUE

C7719 100UF 20% 16V POLY 6 3X6 TH
C7766 100UF 20% 16V POLY 6 3X6 TH
C7767 100UF 20% 16V POLY 6 3X6 TH
C7768 100UF 20% 16V POLY 6 3X6 TH
C7758 10UF 10% 16V X5R CERM 0805
C7765 10UF 10% 16V X5R CERM 0805

=PP3V3_S5_VRD 6

R7726 20K 5% 1/16W MF-LF 402

=PP12V_S5_P5VS3_VREG 6 70

NOSTUFF
R7725 20K 5% 1/16W MF-LF 402

PP5V_S5_LDO 6

EMC: C7753-C7755
PLACE AT Q7330

C7754 1UF 10% 16V X5R 603
C7755 1UF 10% 16V X5R 603

PP3V3_S5_REG

R7776 0.002 1% 1206 1/4W MF LF

CRITICAL
L7710 2.2UH-14A MMD06CZ-SM

PP3V3_S5_REG_R
NET_PHYSICAL_TYPE=POWER

C7790 0.01UF 16V CERM 402
R7790 15.8K 1% 1/16W MF LF 402
R7791 15.8K 1% 1/16W MF LF 402

Q7710
RJK0384DPA
WPAK
376S0801

D1
G1 1 (P3V3S5 UGATE)
MIN NECK WIDTH=0.2MM
MIN LINE WIDTH=0.6MM
GATE NODE=TRUE
NET SPACING TYPE=VR CONTROL

S1/D2 7
G2 6 (P3V3S5_LGATE)
MIN NECK WIDTH=0.2MM
MIN LINE WIDTH=0.6MM
GATE NODE=TRUE
NET SPACING TYPE=VR CONTROL

S2

C7730 1000PF 5% 25V NP0-C0G 402 NOSTUFF
R7730 0.499 1% 1/10W MF 603
NET SPACING TYPE=VR CTL NOSTUFF

P3V3S5 REG SNUB
DIDT TRUE

C7714 0.1UF 10% 50V X7R 603

P3V3S5_REG_BOOT_R
MIN NECK WIDTH=0.2MM
MIN LINE WIDTH=0.6MM
DIDT TRUE
NET SPACING TYPE=VR CONTROL
(P3V3S5 PHASE)

R7710 0 5% 1/10W MF LF 603

NET SPACING TYPE=VR CONTROL
MIN NECK WIDTH=0.2MM
MIN LINE WIDTH=0.6MM
NET SPACING TYPE=SWITCHNODE
NET PHYSICAL TYPE=POWER

PM_PGOOD_P3V3_S5_REG
P3V3S5_REG_UGATE
P3V3S5_REG_BOOT
P3V3S5_REG_PHASE
P3V3S5_REG_LGATE
P3V3S5_REG_ISEN
P3V3S5_REG_OCSET
P3V3S5_REG_VOUT1
P3V3S5_REG_FB

U7700
ISL62383
QFN
CRITICAL

PGOOD1 7
UGATE1 14
BOOT1 15
PHASE1 13
LGATE1 16
ISEN1 10
OCSET1 11
VOUT1 9
FB1 8
FSET1 6
EN1 12

VCC1 5
VCC2 4
LDO5 18
VIN 17
FCCM 3
PGOOD2 1
UGATE2 22
BOOT2 21
PHASE2 23
LGATE2 20
ISEN2 26
OCSET2 25
VOUT2 27
FB2 28
FSET2 2
EN2 24
THRM PAD 29
PGND 19

TP_P5VS3_REG_FCCM
P5VS3_REG_UGATE
P5VS3_REG_BOOT
P5VS3_REG_PHASE
P5VS3_REG_LGATE
P5VS3_REG_ISEN
P5VS3_REG_OCSET
P5VS3_REG_VOUT2
P5VS3_REG_FB
P5VS3_REG_FSET2

PM_EN_P3V3_S5_REG

NET_PHYSICAL_TYPE=POWER
C7742 4.7UF 20% 6.3V CERM 603
R7740 2.2 5% 1/8W MF-LF 805
R7741 1 5% 1/8W MF-LF 805
P5V_S5_LDO_R

P5V_S5_VCC1
C7740 1UF 10% 16V X5R 603
C7741 1UF 10% 16V X5R 603
C7743 1UF 10% 16V X5R 603

VIN_5V_S5_REG_RC

PM_PGOOD_P5V_S3_REG
MIN LINE WIDTH=0.6MM
NET_SPACING_TYPE=VR_CONTROL

CRITICAL
Q7750
FDMS0346
POWER56
376S0875

R7750 0 5% 1/10W MF-LF 603
P5VS3_REG_BOOT_R
MIN NECK WIDTH=0.2MM
MIN LINE WIDTH=0.6MM
NET_SPACING_TYPE=VR_CONTROL

C7756 0.1UF 10% 25V X5R 402

NET SPACING TYPE=SWITCHNODE
NET_PHYSICAL_TYPE=POWER

NOSTUFF
C7757 0.001UF 10% 50V CERM 402

5V SNUBBER
DIDT TRUE
MIN LINE WIDTH=0.4MM
MIN NECK WIDTH=0.2MM
NET SPACING TYPE=SWITCHNODE
R7752 0.499 1% 1/10W MF 603 NOSTUFF

CRITICAL
Q7751
FDMS0355S
POWER56
376S0917

EMC: C7763-C7764
PLACE AT L7750.2

C7763 0.001UF 10% 50V X7R 402
C7764 0.001UF 10% 50V X7R 402

PP5V_S3_REG

R7775 0.002 1% 1206 1/4W MF LF

CRITICAL
L7750 2.2UH+/-20%-0.0069OHM-16A PIC1005H-SM

PP5V_S3_REG_R
NET_PHYSICAL_TYPE=POWER

R7770 9.76K 1% 1/16W MF-LF 402
C7770 27.0NF 10% 10V X5R 402
R7771 9.76K 1% 1/16W MF LF 402

OUTPUT BULK DECOUPLING:

C7760 10UF 20% 6.3V CERM 805-1
C7769 10UF 20% 6.3V CERM 805-1

CRITICAL
C7761 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

CRITICAL
C7762 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

SM XW7751 OMIT

OUTPUT BULK DECOUPLING:

PLACEMENT NOTE=PLACE NEXT TO C7716

128S0237
CRITICAL
C7721 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

C7715 10UF 10% 16V X5R CERM 0805
C7717 10UF 10% 16V X5R CERM 0805

SM XW7716 OMIT

R7720 45.3K 1% 1/16W MF-LF 402 <Ra>
R7721 10.0K 0.5% 1/16W MF 402 <Rb>

R7724 976 1% 1/10W MF-LF 402
P3V3S5_REG_FB_R

C7720 1000PF 5% 25V NP0 C0G 402

R7722 68K 5% 1/16W MF-LF 402
R7723 33K 5% 1/16W MF-LF 402

C7723 0.1UF 20% 16V CERM 603
C7716 0.1UF 20% 16V CERM 603

EMC CAPS
PLACE CLOSE
TO L

Vout = 0.6V * (1 + Ra / Rb)

P3V3S5_REG_FSET1
C7701 0.01UF 10% 16V CERM 402
R7701 16.5K 1% 1/16W MF-LF 402

PM_EN_P5V_S3_REG

C7747 0.01UF 10% 16V CERM 402
R7747 16.5K 1% 1/16W MF-LF 402

NOSTUFF
C7777 0.001UF 10% 50V CERM 402

R7759 976 1% 1/16W MF-LF 402
P5VS5_REG_FB_R
C7759 1000PF 5% 25V NP0-C0G 402

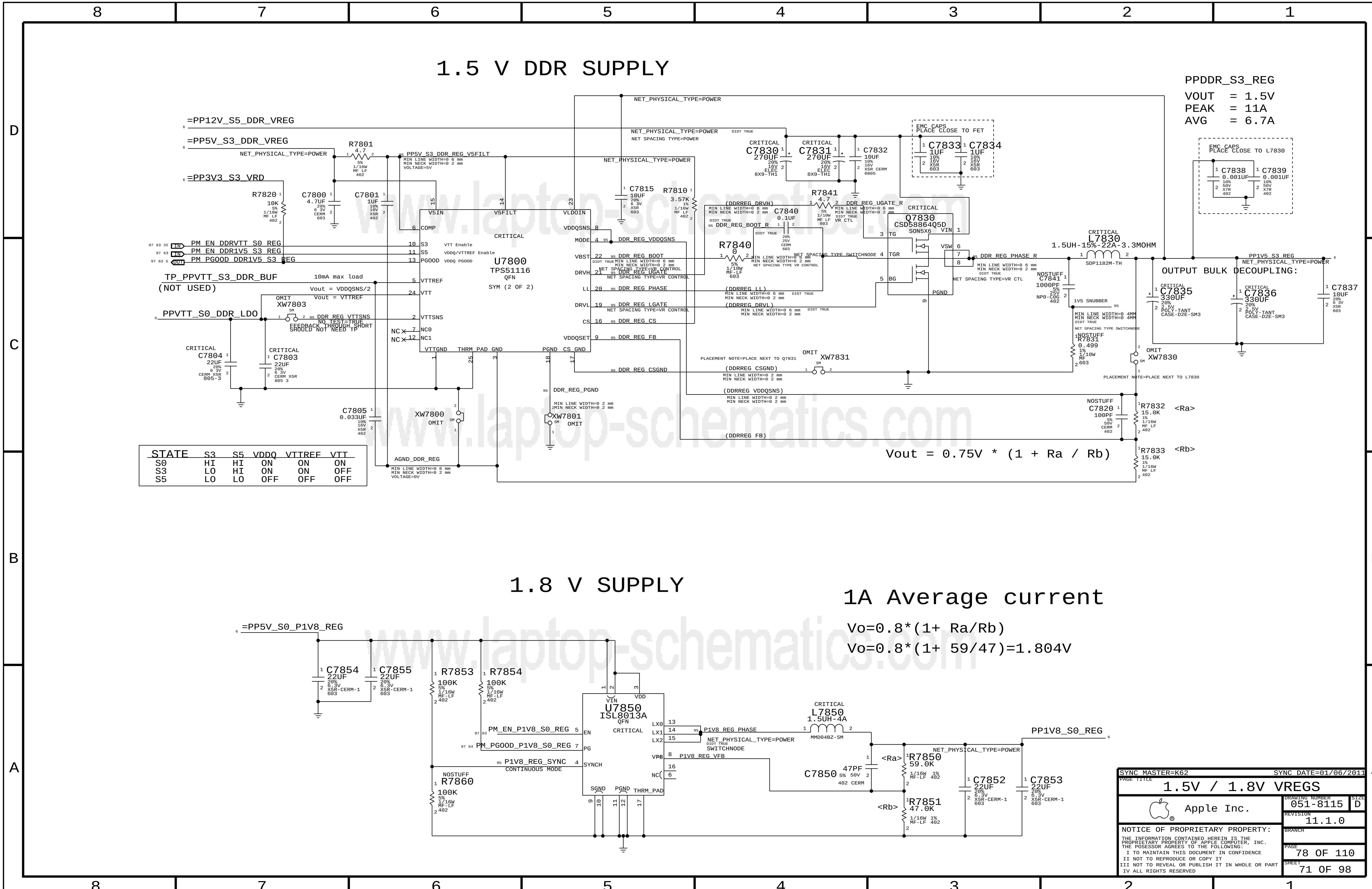
R7755 75K 1% 1/16W MF-LF 402 RA
R7756 10K 1% 1/16W MF LF 402 RB

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: 5V S3 / 3V3 S5 VREGS

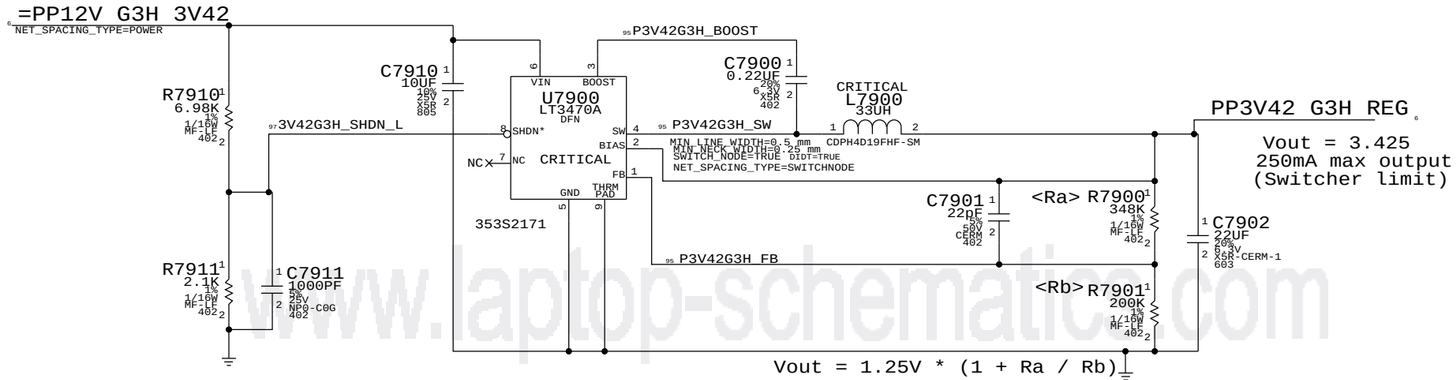
Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 77 OF 110
SHEET: 70 OF 98



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE: 3.42 G3HOT SUPPLY

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

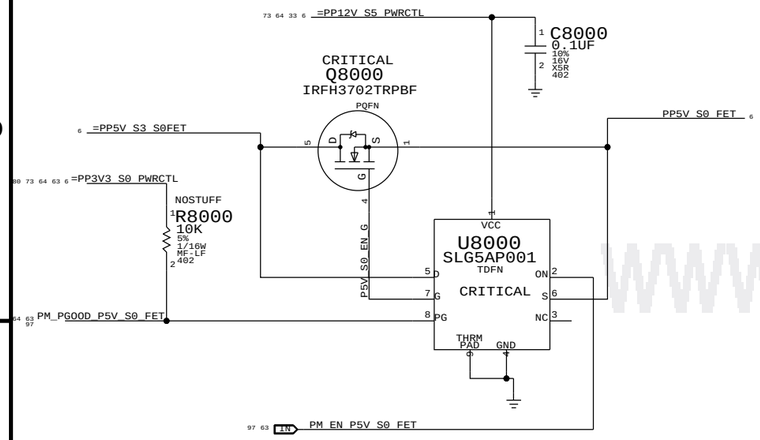
REVISION: 11.1.0

BRANCH:

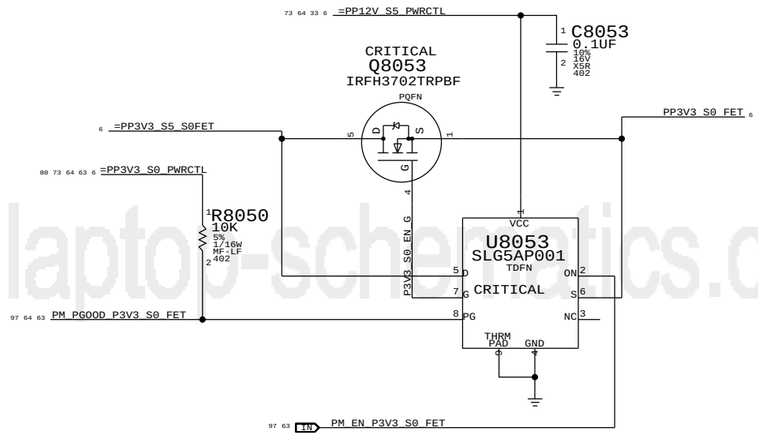
PAGE: 79 OF 110

SHEET: 72 OF 98

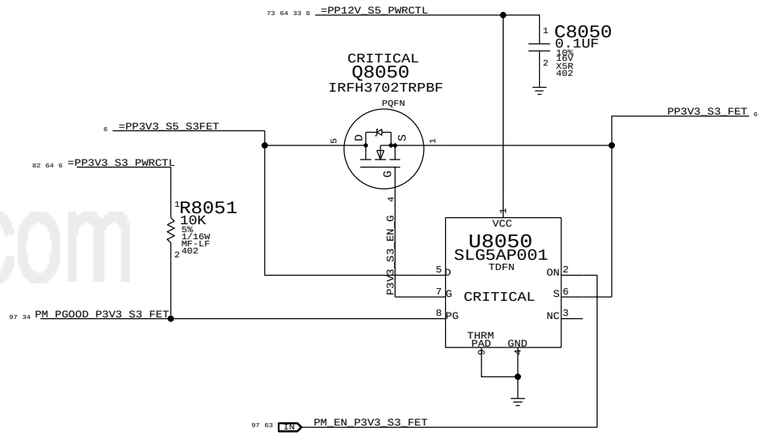
5V S0 FET (6.6A PK/3.1A AVG)



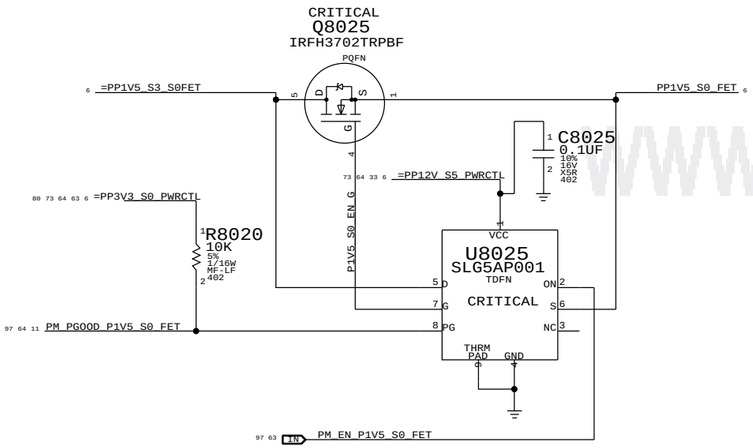
3.3V S0 FET (2.9APK / 2.0A AVG)



3.3V S3 FET (3.4A PK / 1.6A AVG)



1.5V S0 FET (4.8A PK / 4.8A AVG)



SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE: S3+S0 FETS

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

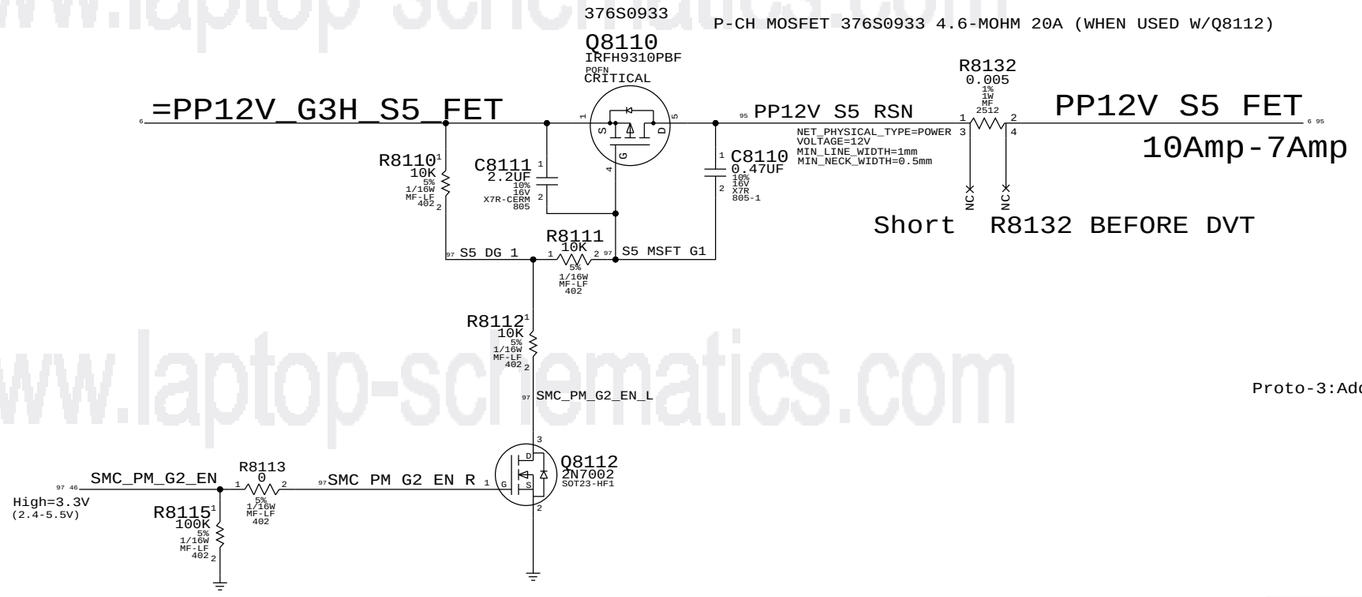
REVISION: 11.1.0

BRANCH:

PAGE: 80 OF 110

SHEET: 73 OF 98

376S0933
Q8110
IRFH9310PBF
P-CH MOSFET 376S0933 4.6-MOHM 20A (WHEN USED W/Q8112)



Short R8132 BEFORE DVT

Proto-3:Add C8111

SYNC MASTER=K60 JERRY SYNC DATE=01/06/2011

PAGE TITLE
12V S0 & 12V S5 switch

Apple Inc.

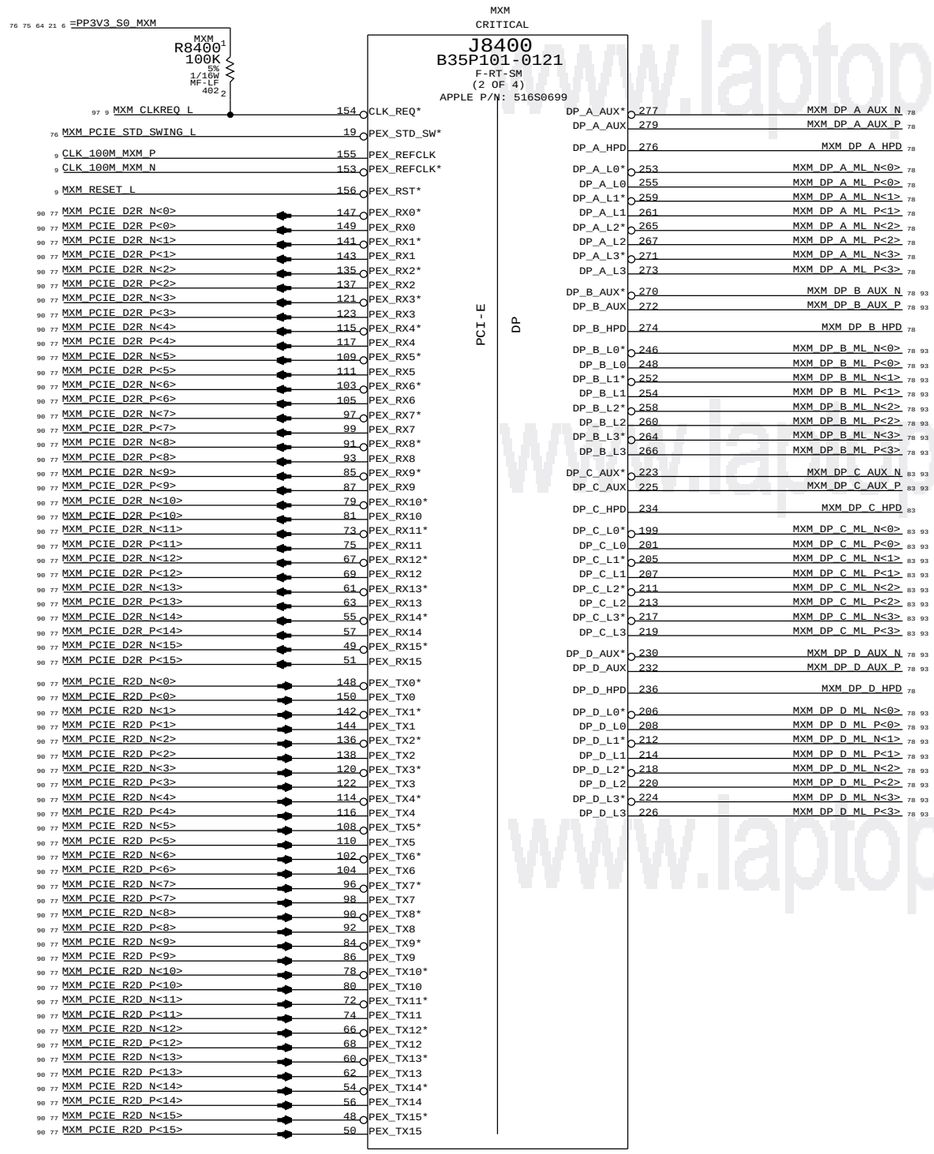
DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 81 OF 110
SHEET 74 OF 98

Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM



MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

MXM DP PORT ROUTING

	K62	K60
DP A	EXT DP1	EXT DP1
DP B	T29 DP2	T29 DP2
DP C	INT DP	INT DP
DP D	T29 DP1	T29 DP1
DP E	EXT DP2	

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 84 OF 110
SHEET 75 OF 98

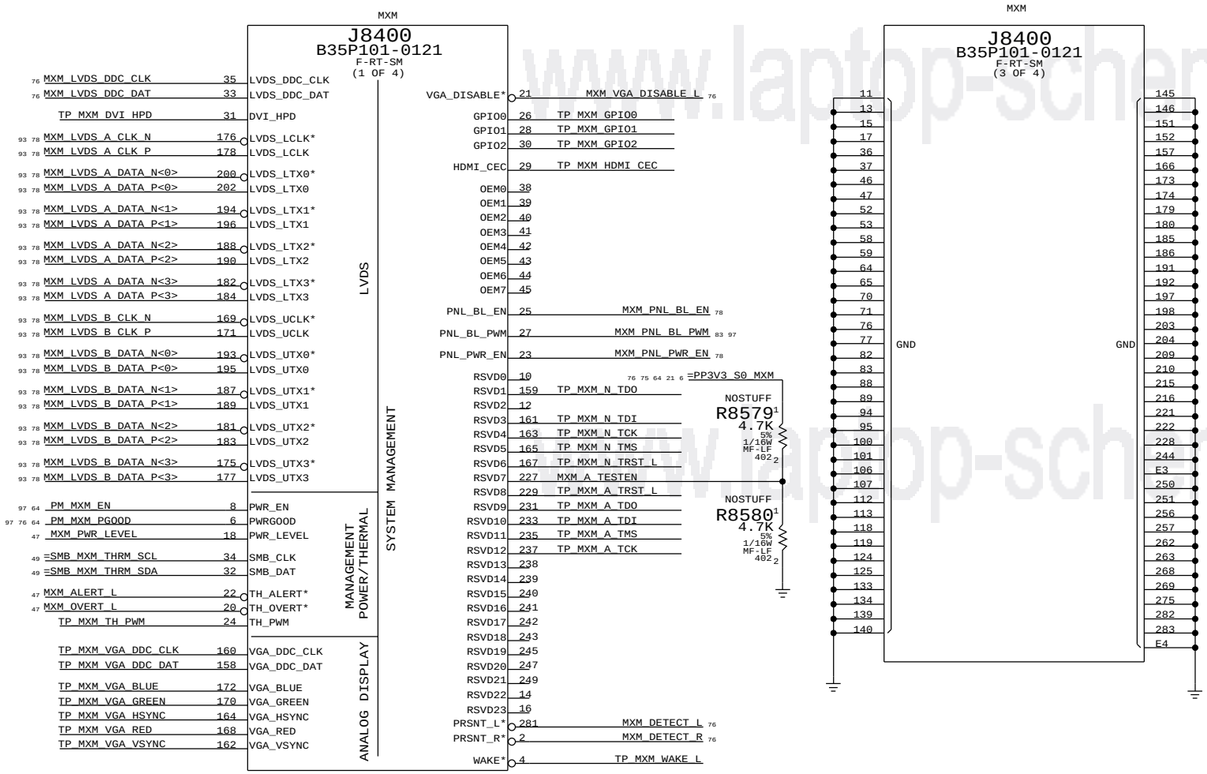
Page Notes

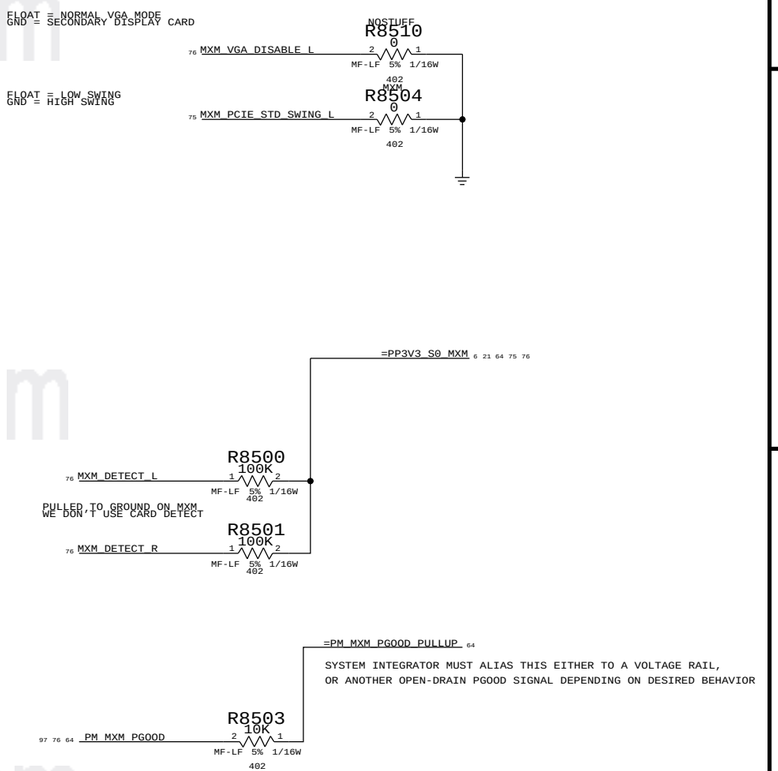
Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

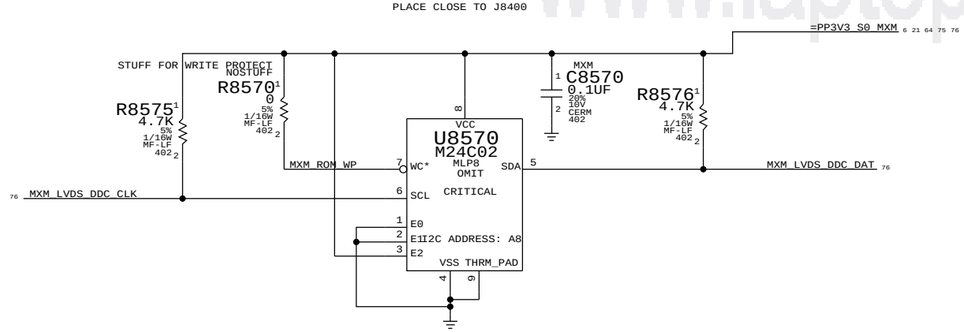
PULLUPS & PULLDOWNS AT MXM CONNECTOR





MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



SYNC MASTER=K60 MASTER	SYNC DATE=N/A
PAGE TITLE	MXM I/O
Apple Inc.	DRAWING NUMBER 051-8115 · SIZE D
	REVISION 11.1.0
	BRANCH
	PAGE 85 OF 110
	SHEET 76 OF 98

MXM TX CAPS

PEG_R2D_C_P<0>	MXM	C8600	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>		
PEG_R2D_C_N<0>	MXM	C8601	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<15>		
PEG_R2D_C_N<1>	MXM	C8602	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<14>		
PEG_R2D_C_P<1>	MXM	C8603	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<14>		
PEG_R2D_C_N<2>	MXM	C8604	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<13>		
PEG_R2D_C_P<2>	MXM	C8605	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<13>		
PEG_R2D_C_P<3>	MXM	C8606	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<12>		
PEG_R2D_C_N<3>	MXM	C8607	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<12>		
PEG_R2D_C_N<4>	MXM	C8608	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<11>		
PEG_R2D_C_P<4>	MXM	C8609	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<11>		
PEG_R2D_C_N<5>	MXM	C8610	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<10>		
PEG_R2D_C_P<5>	MXM	C8611	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<10>		
PEG_R2D_C_P<6>	MXM	C8612	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<9>		
PEG_R2D_C_N<6>	MXM	C8613	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<9>		
PEG_R2D_C_N<7>	MXM	C8614	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<8>		
PEG_R2D_C_P<7>	MXM	C8615	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<8>		
PEG_R2D_C_P<8>	MXM	C8616	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<7>		
PEG_R2D_C_N<8>	MXM	C8617	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<7>		
PEG_R2D_C_P<9>	MXM	C8618	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<6>		
PEG_R2D_C_N<9>	MXM	C8619	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<6>		
PEG_R2D_C_N<10>	MXM	C8620	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<5>		
PEG_R2D_C_P<10>	MXM	C8621	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<5>		
PEG_R2D_C_N<11>	MXM	C8622	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<4>		
PEG_R2D_C_P<11>	MXM	C8623	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<4>		
PEG_R2D_C_P<12>	MXM	C8624	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<3>		
PEG_R2D_C_N<12>	MXM	C8625	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<3>		
PEG_R2D_C_N<13>	MXM	C8626	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<2>		
PEG_R2D_C_P<13>	MXM	C8627	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<2>		
PEG_R2D_C_P<14>	MXM	C8628	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<1>		
PEG_R2D_C_N<14>	MXM	C8629	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<1>		
PEG_R2D_C_N<15>	MXM	C8630	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<0>		
PEG_R2D_C_P<15>	MXM	C8631	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<0>		

MXM RX CAPS

MXM_PCIE_D2R_P<15>	MXM	C8632	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<0>		
MXM_PCIE_D2R_N<15>	MXM	C8633	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<0>		
MXM_PCIE_D2R_P<14>	MXM	C8634	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<1>		
MXM_PCIE_D2R_N<14>	MXM	C8635	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<1>		
MXM_PCIE_D2R_P<13>	MXM	C8636	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<2>		
MXM_PCIE_D2R_N<13>	MXM	C8637	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<2>		
MXM_PCIE_D2R_P<12>	MXM	C8638	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<3>		
MXM_PCIE_D2R_N<12>	MXM	C8639	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<3>		
MXM_PCIE_D2R_P<11>	MXM	C8640	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<4>		
MXM_PCIE_D2R_N<11>	MXM	C8641	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<4>		
MXM_PCIE_D2R_P<10>	MXM	C8642	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<5>		
MXM_PCIE_D2R_N<10>	MXM	C8643	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<5>		
MXM_PCIE_D2R_P<9>	MXM	C8644	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<6>		
MXM_PCIE_D2R_N<9>	MXM	C8645	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<6>		
MXM_PCIE_D2R_P<8>	MXM	C8646	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<7>		
MXM_PCIE_D2R_N<8>	MXM	C8647	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<7>		
MXM_PCIE_D2R_P<7>	MXM	C8648	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<8>		
MXM_PCIE_D2R_N<7>	MXM	C8649	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<8>		
MXM_PCIE_D2R_P<6>	MXM	C8650	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<9>		
MXM_PCIE_D2R_N<6>	MXM	C8651	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<9>		
MXM_PCIE_D2R_P<5>	MXM	C8652	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<10>		
MXM_PCIE_D2R_N<5>	MXM	C8653	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<10>		
MXM_PCIE_D2R_P<4>	MXM	C8654	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<11>		
MXM_PCIE_D2R_N<4>	MXM	C8655	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<11>		
MXM_PCIE_D2R_P<3>	MXM	C8656	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<12>		
MXM_PCIE_D2R_N<3>	MXM	C8657	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<12>		
MXM_PCIE_D2R_P<2>	MXM	C8658	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<13>		
MXM_PCIE_D2R_N<2>	MXM	C8659	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<13>		
MXM_PCIE_D2R_P<1>	MXM	C8662	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<14>		
MXM_PCIE_D2R_N<1>	MXM	C8663	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<14>		
MXM_PCIE_D2R_P<0>	MXM	C8660	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<15>		
MXM_PCIE_D2R_N<0>	MXM	C8661	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<15>		

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 86 OF 110

SHEET: 77 OF 98

Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MXM ALIAS

75	MXM_DP_A_ML_P<0..3>	==	DP_EXTA_ML_C_P<0..3>	84 93	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
75	MXM_DP_A_ML_N<0..3>	==	DP_EXTA_ML_C_N<0..3>	84 93	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
75	MXM_DP_A_AUX_P	==	DP_EXTA_AUXCH_C_P	78 84 93	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
75	MXM_DP_A_AUX_N	==	DP_EXTA_AUXCH_C_N	78 84 93	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
75	MXM_DP_A_HPD	==	DP_EXTA_HPD	84	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		

T29 CONN POWER CONTROL ALIAS

95 84	PP3V3_SW_DPAPWR	==	=PP3V3_SW_DPAPWR	6	
97 36 33 19	PCIE_WAKE_L	==	=T29_WAKE_L	84	

Unused MXM Interfaces

93 76	MXM_LVDS_A_CLK_N	==	NC_MXM_LVDS_A_CLK_N		
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 76	MXM_LVDS_A_CLK_P	==	NC_MXM_LVDS_A_CLK_P		
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 76	MXM_LVDS_A_DATA_N<3..0>	==	NC_MXM_LVDS_A_DATA_N<3..0>		
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 76	MXM_LVDS_A_DATA_P<3..0>	==	NC_MXM_LVDS_A_DATA_P<3..0>		
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 76	MXM_LVDS_B_CLK_N	==	NC_MXM_LVDS_B_CLK_N		
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 76	MXM_LVDS_B_CLK_P	==	NC_MXM_LVDS_B_CLK_P		
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 76	MXM_LVDS_B_DATA_N<3..0>	==	NC_MXM_LVDS_B_DATA_N<3..0>		
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 76	MXM_LVDS_B_DATA_P<3..0>	==	NC_MXM_LVDS_B_DATA_P<3..0>		
		==	MAKE_BASE=TRUE NO_TEST=TRUE		

T29 MXM DP ALIAS

93 75	MXM_DP_D_ML_P<0..3>	==	DP_T29SNK0_ML_C_P<0..3>	86 96	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 75	MXM_DP_D_ML_N<0..3>	==	DP_T29SNK0_ML_C_N<0..3>	86 96	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 75	MXM_DP_D_AUX_P	==	DP_T29SNK0_AUXCH_C_P	86 96	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 75	MXM_DP_D_AUX_N	==	DP_T29SNK0_AUXCH_C_N	86 96	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
75	MXM_DP_D_HPD	==	DP_T29SNK0_HPD	86	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 75	MXM_DP_B_ML_P<0..3>	==	DP_T29SNK1_ML_C_P<0..3>	86 96	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 75	MXM_DP_B_ML_N<0..3>	==	DP_T29SNK1_ML_C_N<0..3>	86 96	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 75	MXM_DP_B_AUX_P	==	DP_T29SNK1_AUXCH_C_P	86 96	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
93 75	MXM_DP_B_AUX_N	==	DP_T29SNK1_AUXCH_C_N	86 96	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
75	MXM_DP_B_HPD	==	DP_T29SNK1_HPD	86	
		==	MAKE_BASE=TRUE NO_TEST=TRUE		

Unused T29 Interfaces

96 86	T29_D2R_N<2..3>	==	NC_T29_D2R_N<2..3>				
		==	MAKE_BASE=TRUE NO_TEST=TRUE				
96 86	T29_D2R_P<2..3>	==	NC_T29_D2R_P<2..3>				
		==	MAKE_BASE=TRUE NO_TEST=TRUE				
96 86	T29_R2D_C_N<2..3>	==	NC_T29_R2D_C_N<2..3>				
		==	MAKE_BASE=TRUE NO_TEST=TRUE				
96 86	T29_R2D_C_P<2..3>	==	NC_T29_R2D_C_P<2..3>				
		==	MAKE_BASE=TRUE NO_TEST=TRUE				
86	T29_LSEO<3>	==	T29_LSEO_LSOE3	==	T29_LSOE<3>	86	
		==	MAKE_BASE=TRUE NO_TEST=TRUE	==			
86	T29_LSEO<2>	==	T29_LSEO_LSEO2	==	T29_LSOE<2>	86	
		==	MAKE_BASE=TRUE NO_TEST=TRUE	==			

UNUSED MXM CONTROL SIGNALS

76	MXM_PNL_BL_EN	==	NC_MXM_PNL_BL_EN		
		==	MAKE_BASE=TRUE NO_TEST=TRUE		
76	MXM_PNL_PWR_EN	==	NC_MXM_PNL_PWR_EN		
		==	MAKE_BASE=TRUE NO_TEST=TRUE		

DDC/AUX ALIAS

93 84 78	DP_EXTA_AUXCH_C_P	==	DP_EXTA_DDC_CLK	84	
	MAKE_BASE=TRUE	==			
93 84 78	DP_EXTA_AUXCH_C_N	==	DP_EXTA_DDC_DATA	84	
	MAKE_BASE=TRUE	==			

SYNC_MASTER=K60_AARON SYNC_DATE=07/18/2010

PAGE TITLE
DP ALIAS AND CONTROL

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 87 OF 110
SHEET 78 OF 98

System RTC Power Source & 32kHz / 25MHz Clock Generator

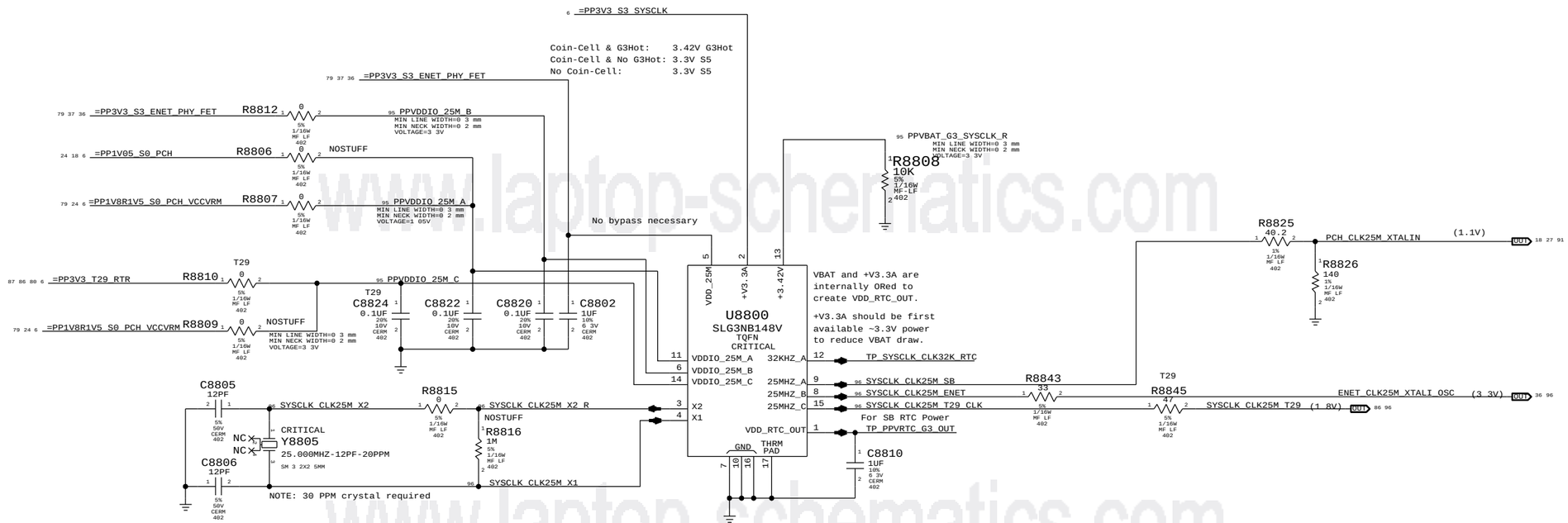
GreenCLK Implementation Notes:

VBAT: Alias as appropriate (see note below & Desktop Example)
+V3.3A: Alias as appropriate (see note below)
VDD_25M: 3.3V matching 'highest' VDDIO power state (ENET)

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

For Cougar Point Desktop: VDDIO = VCCVRM (1.8V), Vclk = 1.1V Max, Divider: 604 / 1000
For Cougar Point Mobile: VDDIO = VCCVRM (1.5V), Vclk = 1.1V Max, Divider: 332 / 1000
For Caesar-IV (BCM57765): VDDIO = XTALVDDH (3.3V), Vclk = 3.3V Max. No Divider Necessary



SYNC MASTER=K62 SYNC DATE=01/06/2013

PAGE TITLE

GREEN CLOCK

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 88 OF 110
SHEET 79 OF 98

Page Notes

Power aliases required by this page:
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- T29_RESET_L

BOM options provided by this page:
(NONE)

Supervisor & CLKREQ# Isolation

=PP3V3_S0_T29PWRCTL

R8906 10K 5% 1/16W MF LF 402

C8900 0.1UF 10% 25V X5R 402

U8900 SLG4AP016V TDFN — T29 CRITICAL

VDD

=PP3V3_T29_RTR

R8907 100K 5% 1/16W MF LF 402

=PP1V05_T29

SENSE 0.7V

Platform (PCIe) Reset

T29_RESET_L

R8903 10K 5% 1/16W MF LF 402

Open-Drain GPIO

T29_SW_RESET_L

MR*

DLY

RESET*

T29_RESET_RTR_L

DLY = 60 ms +/- 20%

EN

OUT (GD)

IN

=T29_CLKREQ_L

T29_CLKREQ_ISOL_L

MAKE BASE=TRUE

GND

THRM PAD

T29 CLKREQ# ISOLATION

=PP3V3_T29_RTR

R8904 10K 5% 1/16W MF LF 402

Q8950 SSM3K15FV SOD-VESM-HF

T29_CLKREQ_L

T29_CLKREQ_FET_L

Pull-up provided by SB page.

3.3V T29 Switch

=PP3V3_S0_P3V3T29FET

U8910 TPS22924 CSP — T29 CRITICAL

VIN VOUT ON GND

PP3V3_T29_FET

Max Current = 1.7A (85C)

C8910 1UF 10% 6.3V CERM 402

U8910

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.05V T29 Switch

=PP12V_S0_PWRCTL

C8930 0.1UF 10% 16V X5R 402

CRITICAL Q8930 BSZ035N03MSG P-TSDSON-8 — T29

=PP1V05_S0_P1V05T29FET

PP1V05_T29_FET

=PP3V3_S0_PWRCTL

R8930 10K 5% 1/16W MF-LF 402

P1V05_S0_T29_EN

U8930 SLG5AP001 TDFN — T29 CRITICAL

VCC D G PG ON S NC THRM PAD GND

PM_PGOOD_P1V05_S0_T29_FET

T29_PWR_EN

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE	T29 POWER
Apple Inc.	DRAWING NUMBER 051-8115 SIZE D
	REVISION 11.1.0
	BRANCH
	PAGE 89 OF 110
	SHEET 80 OF 98

Page Notes

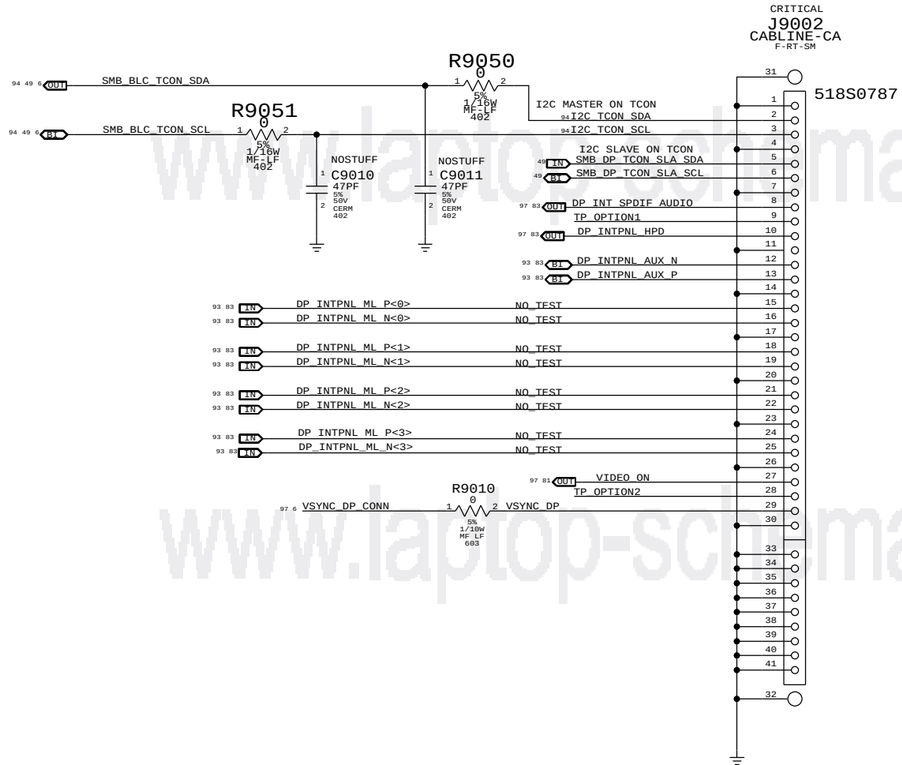
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

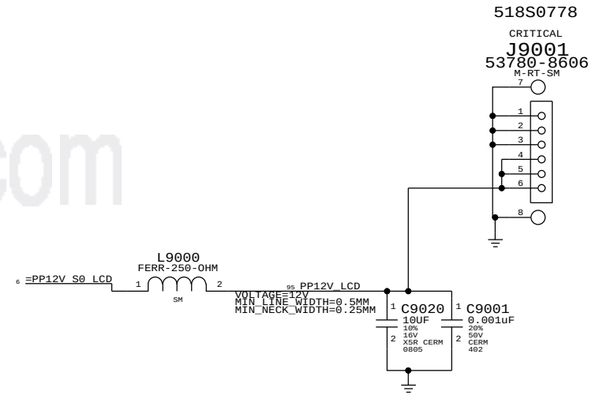
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

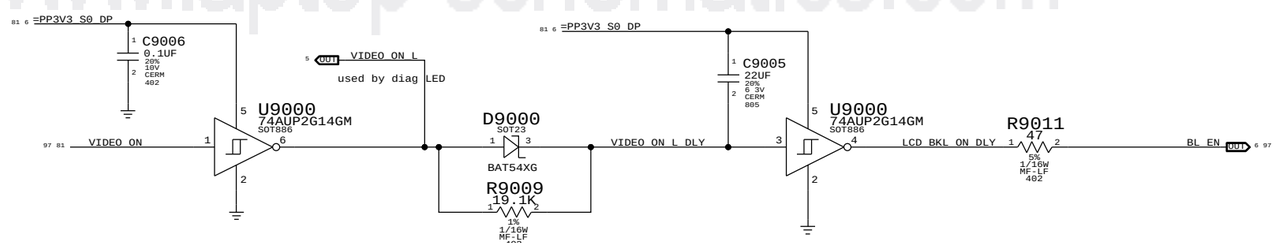


INTERNAL DP POWER



BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

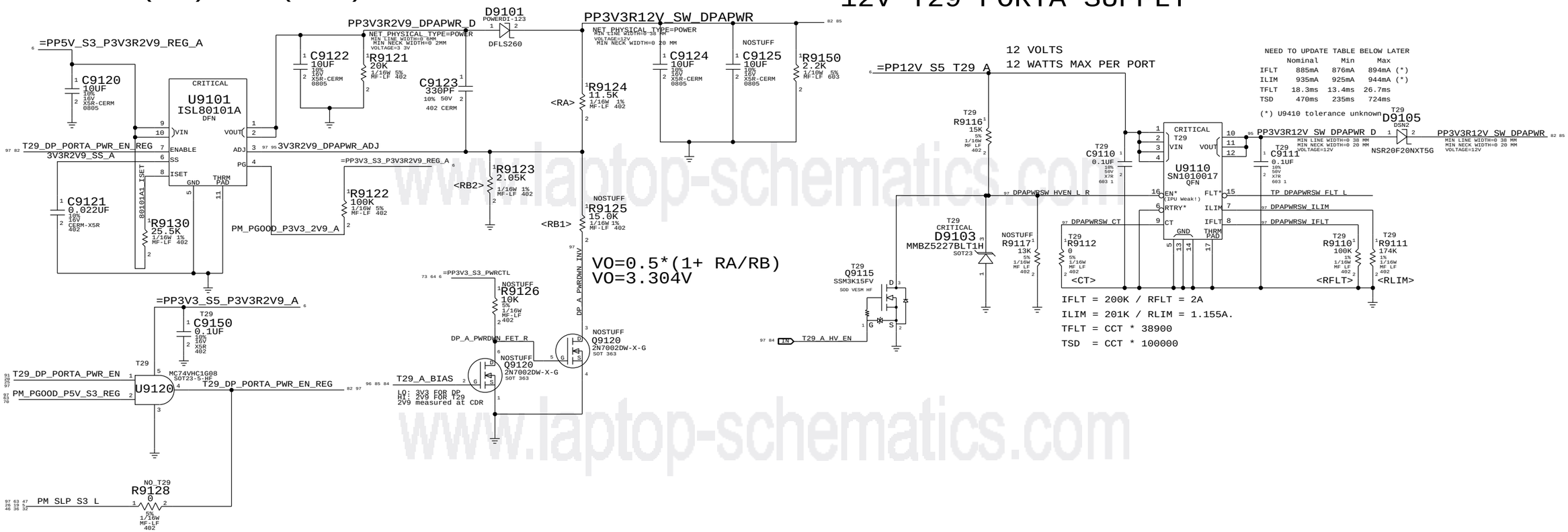
PAGE TITLE
Display: Int DP Connector

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 90 OF 110
SHEET 81 OF 98

3V3(DP)/2V9(T29) PORTA SUPPLY

12V T29 PORTA SUPPLY



NEED TO UPDATE TABLE BELOW LATER

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance unknown

SYNC MASTER=K62 SYNC DATE=11/14/2010

PAGE TITLE: 2V9/3V3/12V POWER SWITCH

Apple Inc.

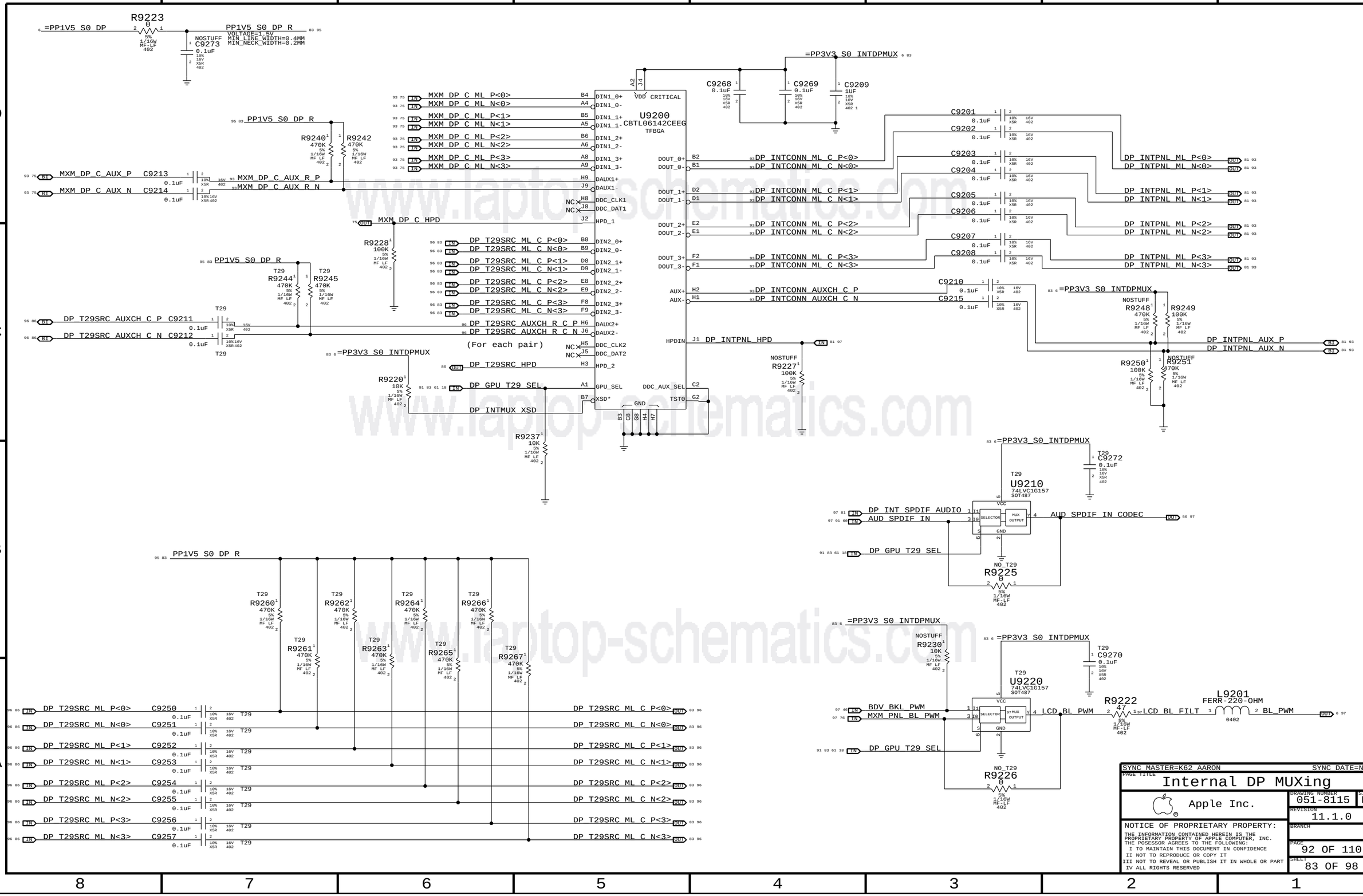
DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 91 OF 110

SHEET: 82 OF 98



T29 A High-Speed Signals

DP_EXTA_ML_C_P<0> C9300 0.1uF DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1uF DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1uF DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1uF DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1uF DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1uF DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1uF DP_EXTA_ML_P<3>
DP_EXTA_ML_C_N<3> C9307 0.1uF DP_EXTA_ML_N<3>
DP_EXTA_AUXCH_C_P C9308 0.1uF DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1uF DP_EXTA_AUXCH_N

=PP3V3_S0_DPSDRVA
R9309 1M 5% MF-LF 1/16W 402 DP_EXTA_AUXCH_P
R9308 1M 5% MF-LF 1/16W 402 DP_EXTA_AUXCH_N

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

T29_D2R_N<0>
T29_D2R_P<0>
OVERSIZE_PAD=0.875 mm^2 (Both L's)
L9372 1.0NH+/-0.1NH 0201-1 T29
L9373 1.0NH+/-0.1NH 0201-1 T29
T29_R2D_C_P<0>
T29_R2D_C_N<0>
T29_R2D_C_F_N<0>
T29_R2D_C_F_P<0>

T29 A BIAS R2D P0 VOLTAGE=3.3V
GND_VOID=TRUE (C9370/C9371)
C9370 0.47UF 20% 4V CERM-X5R-1 201 T29
C9371 0.47UF 20% 4V CERM-X5R-1 201 T29
(C9372.2) GND_VOID=TRUE
C9372 0.47UF 20% 4V CERM-X5R-1 201 T29
C9373 0.47UF 20% 4V CERM-X5R-1 201 T29
(C9373.2) GND_VOID=TRUE
T29 A BIAS R2D N0 VOLTAGE=3.3V

R9372 1.5K 5% 1/20W MF 201 GND_VOID=TRUE T29 SIGNAL_MODEL=EMPTY
R9373 1.5K 5% 1/20W MF 201 GND_VOID=TRUE T29 SIGNAL_MODEL=EMPTY

T29 signals are P/N-swapped after AC caps to improve layout.

(All 4 L's)

T29 Path Biasing

T29_D2R_P<1>
T29_D2R_N<1>
OVERSIZE_PAD=0.875 mm^2 (Both L's)
L9382 1.0NH+/-0.1NH 0201-1 T29
L9383 1.0NH+/-0.1NH 0201-1 T29
T29_R2D_C_N<1>
T29_R2D_C_P<1>
T29_R2D_C_F_N<1>
T29_R2D_C_F_P<1>

T29 A BIAS R2D P1 VOLTAGE=3.3V
GND_VOID=TRUE (C9380/C9381)
C9380 0.47UF 20% 4V CERM-X5R-1 201 T29
C9381 0.47UF 20% 4V CERM-X5R-1 201 T29
(C9383.2) GND_VOID=TRUE
C9382 0.47UF 20% 4V CERM-X5R-1 201 T29
C9383 0.47UF 20% 4V CERM-X5R-1 201 T29
(C9383.2) GND_VOID=TRUE
T29 A BIAS R2D N1 VOLTAGE=3.3V

R9382 1.5K 5% 1/20W MF 201 GND_VOID=TRUE T29 SIGNAL_MODEL=EMPTY
R9383 1.5K 5% 1/20W MF 201 GND_VOID=TRUE T29 SIGNAL_MODEL=EMPTY

T29_D2R_C_P<0> T29_D2R_C_N<0>
D9364 D9372 D9373 D9365 BAR90-02LRH TSLP-2-7
GND_VOID=TRUE (D9364.2)
T29: TX_0
T29DPA_ML_C_P<0> T29DPA_ML_C_N<0>
GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY
R9374 1.5K 5% 1/20W MF 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
R9375 1.5K 5% 1/20W MF 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
T29_D2R_C_P<1> T29_D2R_C_N<1>
D9360 D9382 D9383 D9361 BAR90-02LRH TSLP-2-7
GND_VOID=TRUE (D9360.2)
T29: TX_1
T29DPA_ML_C_P<2> T29DPA_ML_C_N<2>
GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)
R9384 1.5K 5% 1/20W MF 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
R9385 1.5K 5% 1/20W MF 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY

DP Path Biasing

DP_SDRVA_ML_R_P<0> DP_SDRVA_ML_R_N<0>
DP_SDRVA_ML_R_P<2> DP_SDRVA_ML_R_N<2>
R9354 22 5% 1/20W MF 201
R9355 22 5% 1/20W MF 201
R9350 22 5% 1/20W MF 201
R9351 22 5% 1/20W MF 201
DP_SDRVA_ML_P<0> DP_SDRVA_ML_N<0>
DP_SDRVA_ML_P<2> DP_SDRVA_ML_N<2>
C9364 0.22UF 20% 6.3V X5R 0201
C9365 0.22UF 20% 6.3V X5R 0201
C9360 0.22UF 20% 6.3V X5R 0201
C9361 0.22UF 20% 6.3V X5R 0201

R9370 390 5% 1/20W MF 201
R9371 390 5% 1/20W MF 201
R9352 390 5% 1/20W MF 201
R9353 390 5% 1/20W MF 201

DP_A_BIAS_N_2 R9361 1.5K 5% 1/20W MF 201 R9362 51 5% 1/20W MF 201 VOLTAGE=3.3V
DP_A_BIAS_P_2 R9360 1.5K 5% 1/20W MF 201 R9363 51 5% 1/20W MF 201 VOLTAGE=3.3V
DP_A_BIAS_N_0 R9365 1.5K 5% 1/20W MF 201 R9366 51 5% 1/20W MF 201 VOLTAGE=3.3V
DP_A_BIAS_P_0 R9364 1.5K 5% 1/20W MF 201 R9367 51 5% 1/20W MF 201 VOLTAGE=3.3V
Both R's: C9358 0.1UF 10% 16V X5R-CERM 0201

DP A Super-Driver

=PP3V3_S0_DPSDRVA
C9310 2.2UF 20% 6.3V CERM 402-LF
C9311 0.1UF 20% 10V CERM 402
C9312 0.1UF 20% 10V CERM 402

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NO STUFF R9311 1K 5% 1/16W MF-LF 402
R9310 1K 5% 1/16W MF-LF 402
R9312 1K 5% 1/16W MF-LF 402

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL

DP_EXTA_ML_P<0>	IN_D0P	OUT_D0P	DP_SDRVA_ML_C_P<0>
DP_EXTA_ML_N<0>	IN_D0N	OUT_D0N	DP_SDRVA_ML_C_N<0>
DP_EXTA_ML_P<1>	IN_D1P	OUT_D1P	DP_SDRVA_ML_C_P<1>
DP_EXTA_ML_N<1>	IN_D1N	OUT_D1N	DP_SDRVA_ML_C_N<1>
DP_EXTA_ML_P<2>	IN_D2P	OUT_D2P	DP_SDRVA_ML_C_P<2>
DP_EXTA_ML_N<2>	IN_D2N	OUT_D2N	DP_SDRVA_ML_C_N<2>
DP_EXTA_ML_P<3>	IN_D3P	OUT_D3P	DP_SDRVA_ML_C_P<3>
DP_EXTA_ML_N<3>	IN_D3N	OUT_D3N	DP_SDRVA_ML_C_N<3>
DP_EXTA_DDC_CLK	IN_SCL	AC_AUXP	DP_SDRVA_AUXCH_C_P
DP_EXTA_DDC_DATA	IN_SDA	AC_AUXN	DP_SDRVA_AUXCH_C_N
DP_EXTA_AUXCH_P	IN_AUXP	OUT_AUXP_SCL	(DP_SDRVA_AUXCH_P)
DP_EXTA_AUXCH_N	IN_AUXN	OUT_AUXN_SDA	(DP_SDRVA_AUXCH_N)
DP_EXTA_HPD	IN_HPD	(IPD) OUT_HPD	(DP_SDRVA_HPD)
DPSDRVA_I2C_CTL_EN	I2C_CTL_EN (IPU)	CA_DET	DP_A_CA_DET
DPSDRVA_I2C_ADDR0	I2C_ADDR0 (IPD)	CEXT	DPSDRVA_CEXT
DPSDRVA_I2C_ADDR1	I2C_ADDR1 (IPD)		
=I2C_DPSDRVA_SCL	SCL_CTL		
=I2C_DPSDRVA_SDA	SDA_CTL		
DPSDRVA_REXT	REXT		
DP_AUXCH_ISOL	AUXDDC_OFF (IPD)		
DP_A_PWRDWN_R	PD (IPD)		

GND THMPAD

C9319 2.2UF 20% 6.3V CERM 402-LF

SDRV_PD R9318 0 5% 1/16W MF-LF 402
R9319 4.02K 1% 1/16W MF-LF 402

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

AUXCH Snoop Port, used by PS8301 during training.

C9363 0.1UF 10% 16V X5R-CERM 0201
C9362 0.1UF 10% 16V X5R-CERM 0201
C9367 0.1UF 10% 16V X5R-CERM 0201
C9366 0.1UF 10% 16V X5R-CERM 0201
C9369 0.1UF 10% 16V X5R 402
C9368 0.1UF 10% 16V X5R 402

IC supports input high while Vcc = 0V.

=PP3V3_S0_DPSDRVA
C9359 0.1UF 10% 16V X5R 402
DP_A_PWRDWN
CRITICAL U9359 74LVC1G04DBDCK SC70
DP_A_BIAS

DP/T29 A Low-Speed MUX

PP3V3_SW_DPAPWR Must be 3.3V DP A port power

C9390 0.1UF 10% 16V X5R-CERM 0201
C9391 0.1UF 10% 16V X5R-CERM 0201
R9399 100K 5% 1/16W MF-LF 402

U9390 CBTL04DP081 HVQFN OMIT CRITICAL

DP_SDRVA_ML_N<3>	DIN1_0+	DOUT_0+	T29DPA_ML_N<3>
DP_SDRVA_ML_P<3>	DIN1_0-	DOUT_0-	T29DPA_ML_P<3>
DP_SDRVA_ML_N<1>	DIN1_1+		T29: Unused
DP_SDRVA_ML_P<1>	DIN1_1-		
DP_SDRVA_AUXCH_P	AUX1+	DOUT_1+	T29DPA_ML_N<1>
DP_SDRVA_AUXCH_N	AUX1-	DOUT_1-	T29DPA_ML_P<1>
DP_SDRVA_HPD	HPD_1		T29: LSX_A_R2P/P2R (P/N)
T29_A_RSVD_N	DIN2_0+	AUX+	DP_A_EXT_AUXCH_P
T29_A_RSVD_P	DIN2_0-	AUX-	DP_A_EXT_AUXCH_N
(T29_A_LSX_P2R)	DIN2_1+		T29: RX_1 Bias Sink
(T29_A_LSX_R2P)	DIN2_1-		
T29_D2R1_BIASP	AUX2+	HPD_IN	DP_A_EXT_HPD
T29_D2R1_BIASN	AUX2-		
NC	HPD_2		
DP_A_PWRDWN	GPU_SEL		
T29_A_BIAS	AUX_SEL		
NC	NC		

LO=Port A HI=Port B

THMPAD GND

SIGNAL_MODEL=T29DP_MUX

T29 R9392 51 5% 1/16W MF-LF 402
T29 R9393 51 5% 1/16W MF-LF 402
T29 R9396 1K 5% 1/16W MF-LF 402
T29 R9397 1K 5% 1/16W MF-LF 402
R9398 100K 5% 1/16W MF-LF 402

CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

Port A MCU

PP3V3_SW_DPAPWR Must be 3.3V DP A port power

C9330 0.1UF 20% 16V CERM 402
C9331 0.1UF 20% 16V CERM 402

U9330 LPC1112A HVQFN25 CRITICAL

DP_A_CA_DET	RESET#/PIO0_0	R/PIO1_0/AD1	T29DPA_CONFIG1_RC
T29_LSEO<0>	PIO0_1/CLKOUT	R/PIO1_1/AD2	T29DPA_CONFIG2_RC
	PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3	T29_A_HV_EN_R
=I2C_T29AMCU_SCL	PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4	T29_A_UC_ADDR
=I2C_T29AMCU_SDA	PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP	DP_A_EXT_HPD
T29DPA_HPD	PIO0_6/SCK	PIO1_6/RXD	T29_A_LSX_P2R (P2R = PLUG TO RECEPTACLE)
T29_A_BIAS	PIO0_7/CTS#	PIO1_7/TXD	T29_A_LSX_R2P (R2P = RECEPTACLE TO PLUG)
T29_LSOE<0>	PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0	T29_LSEO<1>
T29_LSOE<1>	PIO0_9/MOSI/CT16B0_MAT1		
T29_MCU_INT_L	SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)		
	R/PIO0_11/AD0 (OD)	XTALIN	
	VSS	THRM PAD	

T29 R9334 10K 5% 1/16W MF-LF 402
T29 R9338 10K 5% 1/16W MF-LF 402
T29 R9335 1K 5% 1/16W MF-LF 402
T29 R9336 10K 5% 1/16W MF-LF 402

I2C Addr: 0x26/0x27 (Wr/Rd)

T29 A HV EN
T29_A_BIAS 0 5% MF 1/20W 201 NO_T29 R9378
T29DPA_CONFIG1_RC 0 5% MF 1/20W 201 DP_A_CA_DET NO_T29 R9380
T29DPA_HPD 0 5% MF 1/20W 201 DP_A_EXT_HPD NO_T29 R9379
DP_A_PWRDWN 0 5% MF 1/20W 201 NO_T29 R9381

T29 R9339 1M 5% 1/16W MF-LF 402

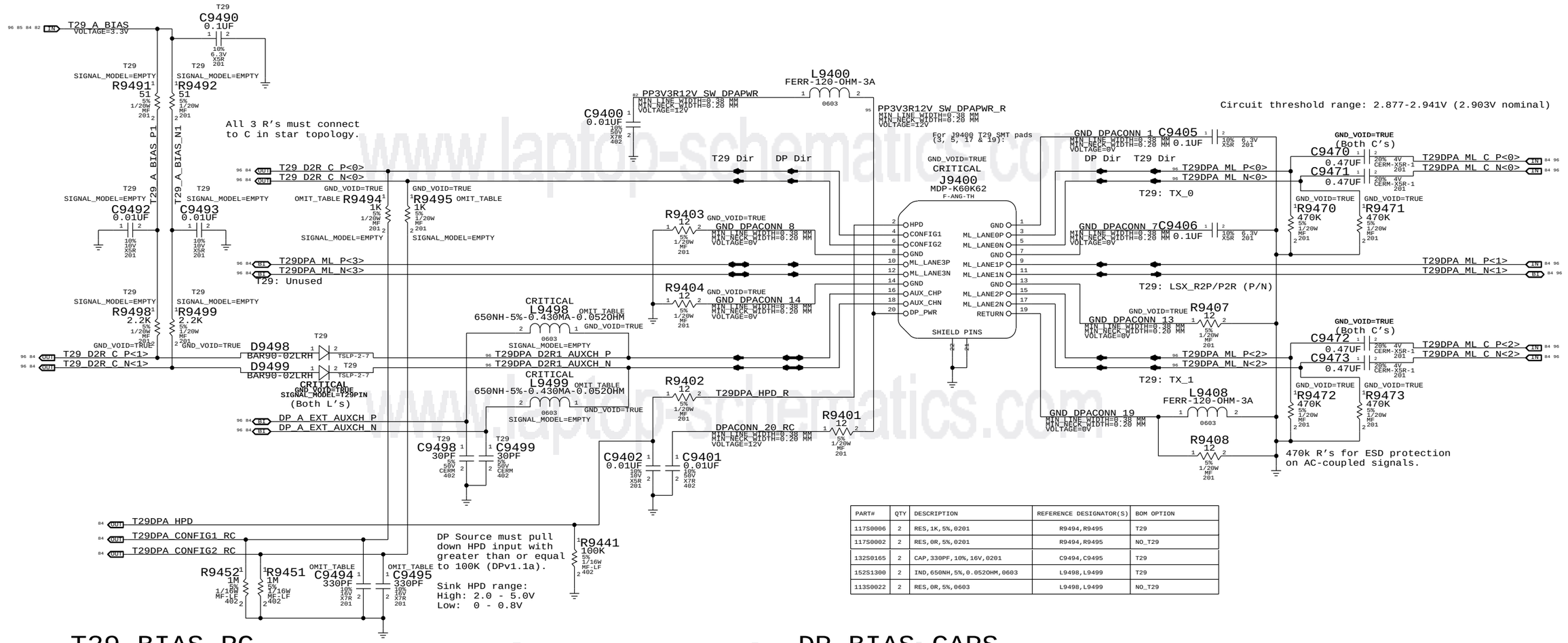
=T29_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#

=T29_WAKE_L
OMIT R9330 0 5% 1/16W MF-LF 402 SWCLK SWDIO
T29_A_UC_ADDR

R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

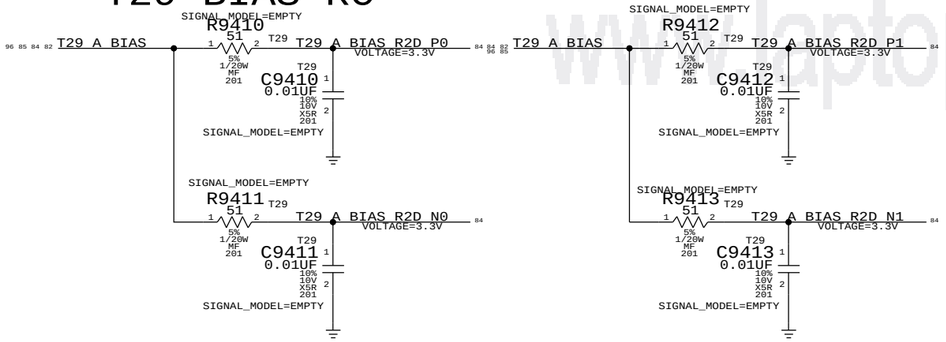
SYNC_MASTER=K62 SYNC_DATE=11/14/2016
PAGE TITLE: DisplayPort/T29 A MUXing
Apple Inc.
DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 93 OF 110
SHEET: 84 OF 98

DisplayPort/T29 A Connector

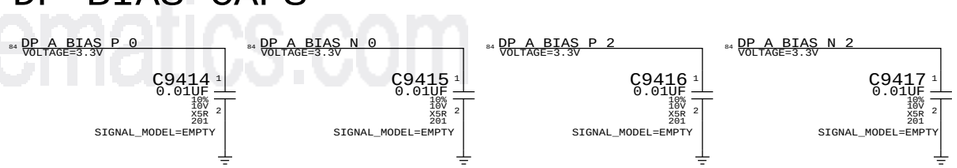


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0006	2	RES,1K,5%,0201	R9494,R9495	T29
117S0002	2	RES,0R,5%,0201	R9494,R9495	NO_T29
132S0165	2	CAP,330PF,10%,16V,0201	C9494,C9495	T29
152S1300	2	IND,650NH,5%,0.052OHM,0603	L9498,L9499	T29
113S0022	2	RES,0R,5%,0603	L9498,L9499	NO_T29

T29 BIAS RC



DP BIAS CAPS



SYNC MASTER=(MASTER) SYNC DATE=(MASTER)

PAGE TITLE: DisplayPort/T29 A Connector

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 94 OF 110

SHEET: 85 OF 98

CRITICAL
OMIT
U9700
T29
FCBGA
(SYM 1 OF 2)

PCIE GEN2

RECEIVE

PCIE_T29_R2D_C_P<0>	C9700 0.1uF	PCIE_T29_R2D_P<0>
PCIE_T29_R2D_C_N<0>	C9701 0.1uF	PCIE_T29_R2D_N<0>
PCIE_T29_R2D_C_P<1>	C9702 0.1uF	PCIE_T29_R2D_P<1>
PCIE_T29_R2D_C_N<1>	C9703 0.1uF	PCIE_T29_R2D_N<1>
PCIE_T29_R2D_C_P<2>	C9704 0.1uF	PCIE_T29_R2D_P<2>
PCIE_T29_R2D_C_N<2>	C9705 0.1uF	PCIE_T29_R2D_N<2>
PCIE_T29_R2D_C_P<3>	C9706 0.1uF	PCIE_T29_R2D_P<3>
PCIE_T29_R2D_C_N<3>	C9707 0.1uF	PCIE_T29_R2D_N<3>

PER_0_P (V19), PER_0_N (T19), PER_1_P (P19), PER_1_N (M19), PER_2_P (K19), PER_2_N (H19), PER_3_P (F19), PER_3_N (D19)

TRANSMIT

PCIE_T29_D2R_C_P<0>	C9740 0.1uF	T29PCIE_T29_D2R_P<0>
PCIE_T29_D2R_C_N<0>	C9741 0.1uF	T29PCIE_T29_D2R_N<0>
PCIE_T29_D2R_C_P<1>	C9742 0.1uF	T29PCIE_T29_D2R_P<1>
PCIE_T29_D2R_C_N<1>	C9743 0.1uF	T29PCIE_T29_D2R_N<1>
PCIE_T29_D2R_C_P<2>	C9744 0.1uF	T29PCIE_T29_D2R_P<2>
PCIE_T29_D2R_C_N<2>	C9745 0.1uF	T29PCIE_T29_D2R_N<2>
PCIE_T29_D2R_C_P<3>	C9746 0.1uF	T29PCIE_T29_D2R_P<3>
PCIE_T29_D2R_C_N<3>	C9747 0.1uF	T29PCIE_T29_D2R_N<3>

PET_0_P (V21), PET_0_N (T21), PET_1_P (P21), PET_1_N (M21), PET_2_P (K21), PET_2_N (H21), PET_3_P (F21), PET_3_N (D21)

NOSTUFF R9710 0 — TP_T29_MONDC0 — T29_MONDC0 — MONDC0
DEBUG For monitoring current/voltage
NOSTUFF R9711 0 — TP_T29_MONDC1 — T29_MONDC1 — MONDC1

C9715 0.1uF — TP_T29_MONOBSP — T29_MONOBSP — MONOBSP
DEBUG For monitoring clock
C9716 0.1uF — TP_T29_MONOBSN — T29_MONOBSN — MONOBSN

=PP3V3_T29_RTR

WAKE* F1 — T29_PCIE_WAKE_L — R9751 10K (=PP3V3_T29_RTR)
PERST* E6 — T29_RESET_RTR_L (IN 80 97)
RSENSE E14 — T29_RSENSE
R9755 1.0K — RBIAS E16 — T29_RBIAS

MISC

POWER ON RESET

Not used in host mode.

PCIE_RST_0* K1	TP_T29_PCIE_RESET0_L
PCIE_RST_1* J2	TP_T29_PCIE_RESET1_L
PCIE_RST_2* K3	TP_T29_PCIE_RESET2_L
PCIE_RST_3* J4	TP_T29_PCIE_RESET3_L

JTAG

TDI T3	JTAG_T29_TDI
TMS R4	JTAG_T29_TMS
TCK R2	JTAG_T29_TCK
TDO T1	JTAG_T29_TDO

CLOCKS

REFCLK_100_IN_P H17	PCIE_CLK100M_T29_P (IN 18 96)
REFCLK_100_IN_N G16	PCIE_CLK100M_T29_N (IN 18 96)
XTAL_25_IN P17	SYSCLK_CLK25M_T29_R
XTAL_25_OUT R16	TP_T29_XTAL25OUT
TMU_CLK_OUT U2	T29_TMU_CLK_OUT
TMU_CLK_IN E2	T29_TMU_CLK_IN

SYSCLK_CLK25M_T29_R — R9795 64.9 — SYSCLK_CLK25M_T29 (IN 79 96)
R9796 150 — =PP3V3_T29_RTR
NOSTUFF R9799 10K — =PP3V3_T29_RTR
R9798 10K — =PP3V3_T29_RTR

J9700 78171-6006 M-RT-SM — =PP3V3_T29_RTR

CLK REQUEST

=T29_CLKREQ_L (OUT 80)	PCIE_CLKREQ_0* P3
T29_GPIO<1>	PCIE_CLKREQ_1* N4
T29_GPIO<2>	PCIE_CLKREQ_2* M3
T29_RSVD	PCIE_CLKREQ_3* L4

EEPROM

T29_SPI_MOSI	EE_DI P1
T29_SPI_MISO	EE_DO M1
T29_SPI_CS_L	EE_CS* N2
T29_SPI_CLK	EE_CLK L2

TEST PORT

THERM_DP A2 — TP_T29_THERM_DP — Use B1 GND ball for THERM DN
TEST_EN E4 — T29_TEST_EN
TEST_POINT_0 P5 — TP_T29_TEST_POINT_0
TEST_POINT_1 N6 — TP_T29_TEST_POINT_1
TEST_POINT_2 M5 — TP_T29_TEST_POINT_2
TEST_POINT_3 L6 — TP_T29_TEST_POINT_3

R9725 0 — T29_SPI_MOSI

R9729 0 — DP_T29SNK0_ML_P<3> (AA4), DP_T29SNK0_ML_N<3> (Y3), DP_T29SNK0_ML_P<2> (AA6), DP_T29SNK0_ML_N<2> (Y5), DP_T29SNK0_ML_P<1> (AA8), DP_T29SNK0_ML_N<1> (Y7), DP_T29SNK0_ML_P<0> (AA10), DP_T29SNK0_ML_N<0> (Y9), DP_T29SNK0_AUXCH_P (V1), DP_T29SNK0_AUXCH_N (W2), DP_T29SNK0_HPD (V5)

R9730 100K — DP_T29SNK1_ML_P<3> (V9), DP_T29SNK1_ML_N<3> (U8), DP_T29SNK1_ML_P<2> (V11), DP_T29SNK1_ML_N<2> (U10), DP_T29SNK1_ML_P<1> (V13), DP_T29SNK1_ML_N<1> (U12), DP_T29SNK1_ML_P<0> (V15), DP_T29SNK1_ML_N<0> (U14), DP_T29SNK1_AUXCH_P (V7), DP_T29SNK1_AUXCH_N (U6), DP_T29SNK1_HPD (U4)

R9731 100K

DISPLAY

SOURCE PORT 0

DPSRC0_ML_LANE_3P	DP_T29SRC_ML_P<3> (AA18)
DPSRC0_ML_LANE_3N	DP_T29SRC_ML_N<3> (Y17)
DPSRC0_ML_LANE_2P	DP_T29SRC_ML_P<2> (AA16)
DPSRC0_ML_LANE_2N	DP_T29SRC_ML_N<2> (Y15)
DPSRC0_ML_LANE_1P	DP_T29SRC_ML_P<1> (AA14)
DPSRC0_ML_LANE_1N	DP_T29SRC_ML_N<1> (Y13)
DPSRC0_ML_LANE_0P	DP_T29SRC_ML_P<0> (AA12)
DPSRC0_ML_LANE_0N	DP_T29SRC_ML_N<0> (Y11)
DPSRC0_AUX_CHP	DP_T29SRC_AUXCH_C_P (W16)
DPSRC0_AUX_CHN	DP_T29SRC_AUXCH_C_N (U16)
DPSRC0_HOT_PLUG_DET	DP_T29SRC_HPD (V3)

DP_ATEST Y19 — T29_DP_ATEST
DP_RES_0 Y21
DP_RES_1 AA20 — T29_DP_RES

R9785 14.0K — R9732 100K — C9785 100PF — C9786 0.01UF

100pF SRF > 40MHz
BYPASS=U3600.Y19::2mm
BYPASS=U3600.Y19::5.08mm

R9741 100K — NOSTUFF — DP_T29SNK0_AUXCH_N, DP_T29SNK0_AUXCH_P
R9742 100K — NOSTUFF
=PP3V3_T29_RTR
R9743 100K — NOSTUFF — DP_T29SNK1_AUXCH_N, DP_T29SNK1_AUXCH_P
R9744 100K — NOSTUFF

PORTS

PORT0

T29_R2D_C_P<0> (OUT 96 84)	PRT0_T29T_P A6
T29_R2D_C_N<0> (OUT 96 84)	PRT0_T29T_N A4
T29_D2R_P<0> (IN 96 84)	PRT0_T29R_P C4
T29_D2R_N<0> (IN 96 84)	PRT0_T29R_N C2
T29_LSEO<0> (OUT 84)	T29_0_LSEO J6
T29_LSOE<0> (IN 84)	T29_0_LSOE K5

PORT1

T29_R2D_C_P<1> (OUT 96 84)	PRT1_T29T_P A10
T29_R2D_C_N<1> (OUT 96 84)	PRT1_T29T_N A8
T29_D2R_P<1> (IN 96 84)	PRT1_T29R_P C8
T29_D2R_N<1> (IN 96 84)	PRT3_T29R_N C6
T29_LSEO<1> (OUT 84)	T29_1_LSEO G6
T29_LSOE<1> (IN 84)	T29_1_LSOE H5

I2C_T29_SDA (BI 96 49) — F3 — T29_SDA
I2C_T29_SCL (OUT 96 49) — F5 — T29_SCL

PORT2

PRT2_T29T_P	T29_R2D_C_P<2> (A14) (OUT 78 96)
PRT2_T29T_N	T29_R2D_C_N<2> (A12) (OUT 78 96)
PRT2_T29R_P	T29_D2R_P<2> (C12) (IN 78 96)
PRT2_T29R_N	T29_D2R_N<2> (C10) (IN 78 96)
T29_2_LSEO	T29_LSEO<2> (G4) (OUT 78)
T29_2_LSOE	T29_LSOE<2> (H3) (IN 78)

PORT3

PRT3_T29T_P	T29_R2D_C_P<3> (A18) (OUT 78 96)
PRT3_T29T_N	T29_R2D_C_N<3> (A16) (OUT 78 96)
PRT3_T29R_P	T29_D2R_P<3> (C16) (IN 78 96)
PRT3_T29R_N	T29_D2R_N<3> (C14) (IN 78 96)
T29_3_LSEO	T29_LSEO<3> (G2) (OUT 78)
T29_3_LSOE	T29_LSOE<3> (H1) (IN 78)

NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).

SNK0 AC Coupling

DP_T29SNK0_ML_C_P<0>	C9720 0.1uF	DP_T29SNK0_ML_P<0>
DP_T29SNK0_ML_C_N<0>	C9721 0.1uF	DP_T29SNK0_ML_N<0>
DP_T29SNK0_ML_C_P<1>	C9722 0.1uF	DP_T29SNK0_ML_P<1>
DP_T29SNK0_ML_C_N<1>	C9723 0.1uF	DP_T29SNK0_ML_N<1>
DP_T29SNK0_ML_C_P<2>	C9724 0.1uF	DP_T29SNK0_ML_P<2>
DP_T29SNK0_ML_C_N<2>	C9725 0.1uF	DP_T29SNK0_ML_N<2>
DP_T29SNK0_ML_C_P<3>	C9726 0.1uF	DP_T29SNK0_ML_P<3>
DP_T29SNK0_ML_C_N<3>	C9727 0.1uF	DP_T29SNK0_ML_N<3>
DP_T29SNK0_AUXCH_C_P	C9728 0.1uF	DP_T29SNK0_AUXCH_P
DP_T29SNK0_AUXCH_C_N	C9729 0.1uF	DP_T29SNK0_AUXCH_N

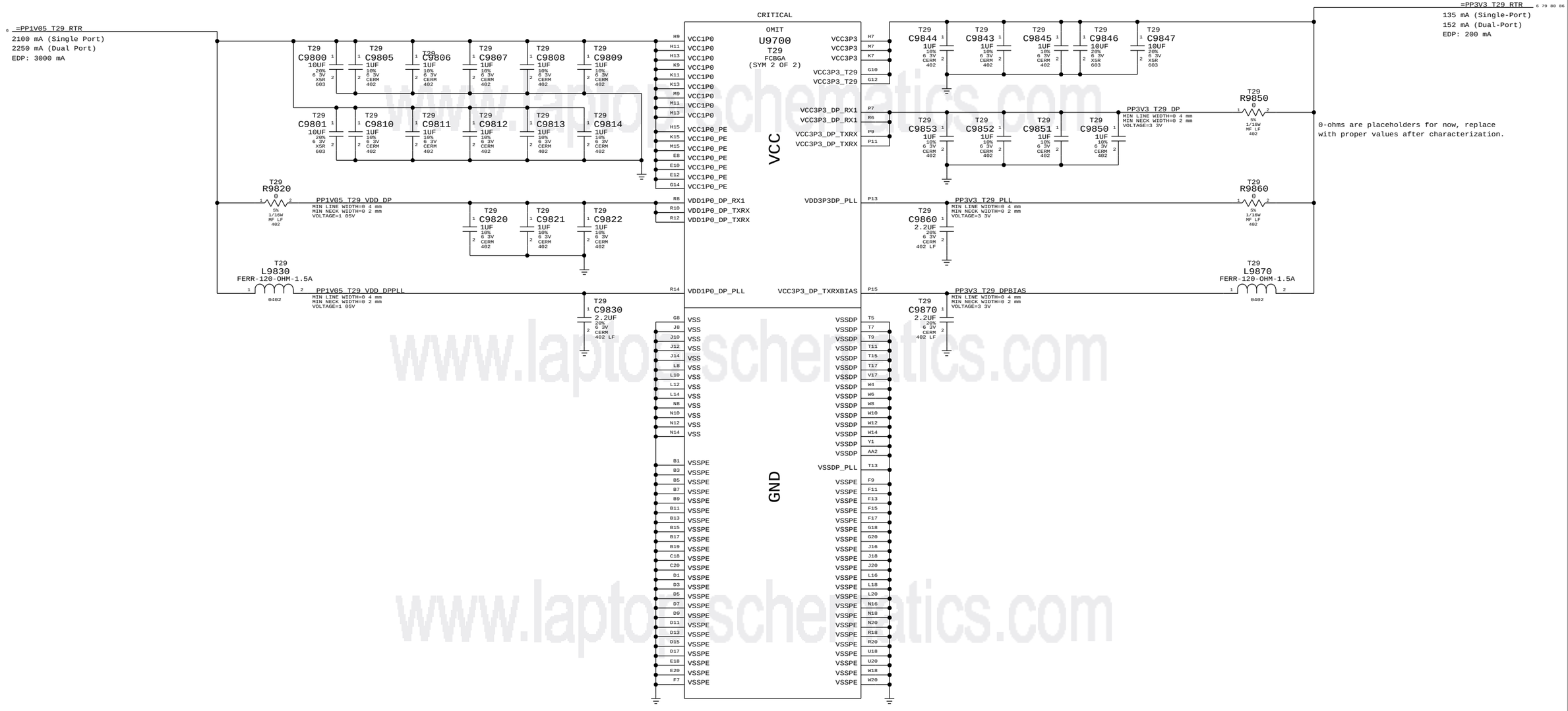
SNK1 AC Coupling

DP_T29SNK1_ML_C_P<0>	C9730 0.1uF	DP_T29SNK1_ML_P<0>
DP_T29SNK1_ML_C_N<0>	C9731 0.1uF	DP_T29SNK1_ML_N<0>
DP_T29SNK1_ML_C_P<1>	C9732 0.1uF	DP_T29SNK1_ML_P<1>
DP_T29SNK1_ML_C_N<1>	C9733 0.1uF	DP_T29SNK1_ML_N<1>
DP_T29SNK1_ML_C_P<2>	C9734 0.1uF	DP_T29SNK1_ML_P<2>
DP_T29SNK1_ML_C_N<2>	C9735 0.1uF	DP_T29SNK1_ML_N<2>
DP_T29SNK1_ML_C_P<3>	C9736 0.1uF	DP_T29SNK1_ML_P<3>
DP_T29SNK1_ML_C_N<3>	C9737 0.1uF	DP_T29SNK1_ML_N<3>
DP_T29SNK1_AUXCH_C_P	C9738 0.1uF	DP_T29SNK1_AUXCH_P
DP_T29SNK1_AUXCH_C_N	C9739 0.1uF	DP_T29SNK1_AUXCH_N

R9790 3.3K — R9791 3.3K — C9790 1UF — R9792 3.3K — R9793 3.3K — R9723 10K — R9722 10K — R9721 10K — =PP3V3_T29_RTR

CRITICAL
OMIT_TABLE
U9790 M95320-RMB6TG MLP
VCC, VSS, THM PAD
(T29_SPI_MOSI), (T29_SPI_CLK), (T29_SPI_CS_L), T29ROM_WP_L, T29ROM_HOLD_L
(T29_SPI_MISO)

SYNC_MASTER=K62	SYNC_DATE=01/06/2013
PAGE TITLE	T29 Host (1 of 2)
Apple Inc.	DRAWING NUMBER 051-8115 · SIZE D
	REVISION 11.1.0
	BRANCH
	PAGE 97 OF 110
	SHEET 86 OF 98



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: T29 Host (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 98 OF 110

SHEET: 87 OF 98

K60/62 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP ISL2 ISL3 ISL4 ISL5 ISL6 ISL7 BOTTOM	NO TYPE BGA BGA P1MM	MM	15 5 1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50 OHM SE	=50 OHM SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12 7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34 OHM SE	TOP BOTTOM	Y	0 21 MM	0 090 MM	=STANDARD		
34 OHM SE	*	Y	0 19 MM	0 090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39 OHM SE	TOP BOTTOM	Y	0 175 MM	0 090 MM	=STANDARD		
39 OHM SE	*	Y	0 159 MM	0 090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42 OHM SE	TOP BOTTOM	Y	0 151 MM	0 090 MM	=STANDARD		
42 OHM SE	*	Y	0 135 MM	0 090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50 OHM SE	TOP BOTTOM	Y	0 1 MM	0 085 MM	15 MM		
50 OHM SE	*	Y	0 1 MM	0 085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55 OHM SE	TOP BOTTOM	Y	0 085 MM	0 085 MM	=STANDARD		
55 OHM SE	*	Y	0 076 MM	0 076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
68 OHM DIFF	ISL3 ISL6	Y	0 16 MM	0 090 MM	=STANDARD	0 13 MM	0 1 MM
68 OHM DIFF	TOP BOTTOM	Y	0 165 MM	0 090 MM	=STANDARD	0 13 MM	0 1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85 OHM DIFF	ISL3 ISL6	Y	0 115 MM	0 085 MM	=STANDARD	0 2 MM	0 1 MM
85 OHM DIFF	TOP BOTTOM	Y	0 125 MM	0 085 MM	=STANDARD	0 2 MM	0 1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90 OHM DIFF	ISL3 ISL6	Y	0 099 MM	0 085 MM	12 MM	0 2 MM	0 1 MM
90 OHM DIFF	TOP BOTTOM	Y	0 110 MM	0 085 MM	=STANDARD	0 2 MM	0 1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100 OHM DIFF	ISL3 ISL6	Y	0 081 MM	0 081 MM	=STANDARD	0 25 MM	0 1 MM
100 OHM DIFF	TOP BOTTOM	Y	0 091 MM	0 085 MM	=STANDARD	0 25 MM	0 1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110 OHM DIFF	ISL3 ISL6	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110 OHM DIFF	TOP BOTTOM	Y	0 075 MM	0 075 MM	=STANDARD	0 320 MM	0 15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1 1 DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0 1 MM	0 085 MM
POWER WIDTH	*	Y	0 600 MM	0 200 MM	3 0 MM	=STANDARD	=STANDARD
POWER CTL	*	Y	0 300 MM	0 200 MM	3 0 MM	=STANDARD	=STANDARD

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0 1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2 1 SPACING	*	0 2 MM	?
2 5 1 SPACING	*	0 25 MM	?
3 1 SPACING	*	0 3 MM	?
3 5 1 SPACING	*	0 35 MM	?
4 1 SPACING	*	0 4 MM	?
5 1 SPACING	*	0 5 MM	?
6 1 SPACING	*	0 6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X DIELECTRIC	*	0 155 MM	?
2X DIELECTRIC	TOP BOTTOM	0 145 MM	?
3X DIELECTRIC	*	0 230 MM	?
3X DIELECTRIC	TOP BOTTOM	0 215 MM	?
4X DIELECTRIC	*	0 305 MM	?
4X DIELECTRIC	TOP BOTTOM	0 285 MM	?
5X DIELECTRIC	*	0 380 MM	?
5X DIELECTRIC	TOP BOTTOM	0 355 MM	?
7X DIELECTRIC	*	0 532 MM	?
7X DIELECTRIC	TOP BOTTOM	0 497 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND P2MM	*	0 2 MM	1000
PWR P2MM	*	0 2 MM	1000
SWITCHNODE	*	0 8 MM	1000

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA P1MM	*	=DEFAULT	?
BGA P1P5MM	*	0 15 MM	?
BGA P2MM	*	0 2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA P1MM	BGA P1MM
*	*	BGA	BGA P1MM
MEM CLK	*	BGA	BGA P1P5MM
CLK PCIE	*	BGA	BGA P1MM
CLK LPC	*	BGA	BGA P1MM
CLK PCI	*	BGA	BGA P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR CONTROL	*	*	SWITCHNODE
VR CONTROL	VR CONTROL	*	STANDARD
VR CONTROL	SWITCHNODE	*	STANDARD
VR CONTROL	GND	*	STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

BOARD STACK-UP

TOP	HALF OZ	SIGNAL
	0.071	PREPREG
2	TWO OZ	GND
	0.076	PREPREG
3	ONE OZ	SIGNAL
	0.370	PREPREG
4	TWO OZ	POWER
	0.101	CORE
5	TWO OZ	POWER
	0.370	PREPREG
6	ONE OZ	SIGNAL
	0.076	PREPREG
7	TWO OZ	GND
	0.071	PREPREG
BOTTOM	HALF OZ	SIGNAL

BOARD THICKNESS = 62 MIL (1.5748 mm)

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE: K60/K62 RULE DEFINITIONS

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 100 OF 110

SHEET: 88 OF 98

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD
MEM 42S	*	=42 OHM SE	=42 OHM SE	=42 OHM SE	=42 OHM SE	=STANDARD	=STANDARD
MEM 39S	*	=39 OHM SE	=39 OHM SE	=39 OHM SE	=39 OHM SE	=STANDARD	=STANDARD
MEM 34S	*	=34 OHM SE	=34 OHM SE	=34 OHM SE	=34 OHM SE	=STANDARD	=STANDARD
MEM 68D	*	=68 OHM DIFF	=68 OHM DIFF	=68 OHM DIFF	=68 OHM DIFF	=68 OHM DIFF	=68 OHM DIFF
MEM 42S D	*	=42 OHM SE	=42 OHM SE	=42 OHM SE	=42 OHM SE	0 1016 MM	0 1016 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM CLK2MEM	*	=4 1 SPACING	?
MEM CTRL2CTRL	*	=2 5 1 SPACING	?
MEM CTRL2MEM	*	=3 1 SPACING	?
MEM CMD2CMD	*	=2 1 SPACING	?
MEM CMD2MEM	*	=3 1 SPACING	?
MEM DQ SAMEBYTE	*	=3 1 SPACING	?
MEM DQ DIFFBYTE	*	=5 1 SPACING	?
MEM DATA2MEM	*	=4 1 SPACING	?
MEM DQS2MEM	*	=4 1 SPACING	?
MEM 2OTHER	*	=5 1 SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM CLK	MEM CLK	*	MEM CLK2MEM
MEM CLK	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM CMD	MEM CTRL	*	MEM CMD2MEM
MEM CMD	MEM CMD	*	MEM CMD2CMD
MEM CMD	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM CTRL	MEM CTRL	*	MEM CTRL2CTRL
MEM CTRL	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQS	MEM CTRL	*	MEM DQS2MEM
MEM DQS	MEM CMD	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE0	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE1	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE2	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE3	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE4	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE5	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE6	*	MEM DQS2MEM
MEM DQS	MEM DQ BYTE7	*	MEM DQS2MEM
MEM DQS	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE5	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE5	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE5	MEM DQ BYTE5	*	MEM DQ SAMEBYTE
MEM DQ BYTE5	MEM DQ BYTE6	*	MEM DQ DIFFBYTE
MEM DQ BYTE5	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE5	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE6	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE6	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE6	MEM DQ BYTE6	*	MEM DQ SAMEBYTE
MEM DQ BYTE6	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE6	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE7	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE7	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE7	MEM DQ BYTE7	*	MEM DQ SAMEBYTE
MEM DQ BYTE7	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE0	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE0	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE0	MEM DQ BYTE0	*	MEM DQ SAMEBYTE
MEM DQ BYTE0	MEM DQ BYTE1	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	MEM DQ BYTE2	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	MEM DQ BYTE3	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	MEM DQ BYTE4	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	MEM DQ BYTE5	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	MEM DQ BYTE6	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE0	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE1	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE1	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE1	MEM DQ BYTE1	*	MEM DQ SAMEBYTE
MEM DQ BYTE1	MEM DQ BYTE2	*	MEM DQ DIFFBYTE
MEM DQ BYTE1	MEM DQ BYTE3	*	MEM DQ DIFFBYTE
MEM DQ BYTE1	MEM DQ BYTE4	*	MEM DQ DIFFBYTE
MEM DQ BYTE1	MEM DQ BYTE5	*	MEM DQ DIFFBYTE
MEM DQ BYTE1	MEM DQ BYTE6	*	MEM DQ DIFFBYTE
MEM DQ BYTE1	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE1	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE2	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE2	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE2	MEM DQ BYTE2	*	MEM DQ SAMEBYTE
MEM DQ BYTE2	MEM DQ BYTE3	*	MEM DQ DIFFBYTE
MEM DQ BYTE2	MEM DQ BYTE4	*	MEM DQ DIFFBYTE
MEM DQ BYTE2	MEM DQ BYTE5	*	MEM DQ DIFFBYTE
MEM DQ BYTE2	MEM DQ BYTE6	*	MEM DQ DIFFBYTE
MEM DQ BYTE2	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE2	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE3	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE3	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE3	MEM DQ BYTE3	*	MEM DQ SAMEBYTE
MEM DQ BYTE3	MEM DQ BYTE4	*	MEM DQ DIFFBYTE
MEM DQ BYTE3	MEM DQ BYTE5	*	MEM DQ DIFFBYTE
MEM DQ BYTE3	MEM DQ BYTE6	*	MEM DQ DIFFBYTE
MEM DQ BYTE3	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE3	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQ BYTE4	MEM CTRL	*	MEM DATA2MEM
MEM DQ BYTE4	MEM CMD	*	MEM DATA2MEM
MEM DQ BYTE4	MEM DQ BYTE4	*	MEM DQ SAMEBYTE
MEM DQ BYTE4	MEM DQ BYTE5	*	MEM DQ DIFFBYTE
MEM DQ BYTE4	MEM DQ BYTE6	*	MEM DQ DIFFBYTE
MEM DQ BYTE4	MEM DQ BYTE7	*	MEM DQ DIFFBYTE
MEM DQ BYTE4	*	*	MEM 2OTHER

Memory Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	MEM 68D	MEM CLK	MEM_A_CLK_P<3..0>	12 32
	MEM 68D	MEM CLK	MEM_A_CLK_N<3..0>	12 32
	MEM 39S	MEM CTRL	MEM_A_CKE<3..0>	12 30
	MEM 39S	MEM CTRL	MEM_A_CS_L<3..0>	12 30
	MEM 39S	MEM CTRL	MEM_A_ODT<3..0>	12 30
	MEM 34S	MEM CMD	MEM_A_A<15..0>	12 30
	MEM 34S	MEM CMD	MEM_A_BA<2..0>	12 30
	MEM 34S	MEM CMD	MEM_A_RAS_L	12 30
	MEM 34S	MEM CMD	MEM_A_CAS_L	12 30
	MEM 34S	MEM CMD	MEM_A_WE_L	12 30
	MEM 42S	MEM DQ BYTE0	MEM_A_DQ<7..0>	12 32
	MEM 42S	MEM DQ BYTE1	MEM_A_DQ<15..8>	12 32
	MEM 42S	MEM DQ BYTE2	MEM_A_DQ<23..16>	12 32
	MEM 42S	MEM DQ BYTE3	MEM_A_DQ<31..24>	12 32
	MEM 42S	MEM DQ BYTE4	MEM_A_DQ<39..32>	12 32
	MEM 42S	MEM DQ BYTE5	MEM_A_DQ<47..40>	12 32
	MEM 42S	MEM DQ BYTE6	MEM_A_DQ<55..48>	12 32
	MEM 42S	MEM DQ BYTE7	MEM_A_DQ<63..56>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<0>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<0>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<1>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<1>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<2>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<2>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<3>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<3>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<4>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<4>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<5>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<5>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<6>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<6>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_P<7>	12 32
	MEM 42S D	MEM DQS	MEM_A_DQS_N<7>	12 32
H17	MEM 50S	PM	MEM_RESET_L	30 31 32 97

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	MEM 68D	MEM CLK	MEM_B_CLK_P<3..0>	12 32
	MEM 68D	MEM CLK	MEM_B_CLK_N<3..0>	12 32
	MEM 39S	MEM CTRL	MEM_B_CKE<3..0>	12 31
	MEM 39S	MEM CTRL	MEM_B_CS_L<3..0>	12 31
	MEM 39S	MEM CTRL	MEM_B_ODT<3..0>	12 31
	MEM 34S	MEM CMD	MEM_B_A<15..0>	12 31
	MEM 34S	MEM CMD	MEM_B_BA<2..0>	12 31
	MEM 34S	MEM CMD	MEM_B_RAS_L	12 31
	MEM 34S	MEM CMD	MEM_B_CAS_L	12 31
	MEM 34S	MEM CMD	MEM_B_WE_L	12 31
	MEM 42S	MEM DQ BYTE0	MEM_B_DQ<7..0>	12 32
	MEM 42S	MEM DQ BYTE1	MEM_B_DQ<15..8>	12 32
	MEM 42S	MEM DQ BYTE2	MEM_B_DQ<23..16>	12 32
	MEM 42S	MEM DQ BYTE3	MEM_B_DQ<31..24>	12 32
	MEM 42S	MEM DQ BYTE4	MEM_B_DQ<39..32>	12 32
	MEM 42S	MEM DQ BYTE5	MEM_B_DQ<47..40>	12 32
	MEM 42S	MEM DQ BYTE6	MEM_B_DQ<55..48>	12 32
	MEM 42S	MEM DQ BYTE7	MEM_B_DQ<63..56>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<0>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<0>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<1>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<1>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<2>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<2>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<3>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<3>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<4>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<4>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<5>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<5>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<6>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<6>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_P<7>	12 32
	MEM 42S D	MEM DQS	MEM_B_DQS_N<7>	12 32

MEMORY MISC PROPERTIES

VOLTAGE	NET TYPE PHYSICAL	NET TYPE SPACING	VOLTAGE		
	MEM POWER PHY	MEM POWER		CPU_DIMM_VREF_A	
	MEM POWER PHY	MEM POWER		CPU_DIMM_VREF_B	
H167	MEM POWER PHY	MEM POWER		CPU_DDR_VREF	11 28
H168	MEM POWER PHY	MEM POWER		VREFMARGIN_DIMMA_DACOUT	28
H169	MEM POWER PHY	MEM POWER		VREFMARGIN_DIMMA_OPFB	28
H170	MEM POWER PHY	MEM POWER		VREFMARGIN_DIMMA_DQ	28
H173	MEM POWER PHY	MEM POWER		CPU_DIMM_VREF_A_SW	
H174	MEM POWER PHY	MEM POWER		VREFMARGIN_DIMMB_DACOUT	28
H175	MEM POWER PHY	MEM POWER		VREFMARGIN_DIMMB_OPFB	28
H176	MEM POWER PHY	MEM POWER		VREFMARGIN_DIMMB_DQ	28
H178	MEM POWER PHY	MEM POWER		CPU_DIMM_VREF_B_SW	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	=3:1_SPACING	?

SYNC_MASTER=K60_ROSITA SYNC_DATE=01/06/2011

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 101 OF 110

SHEET: 89 OF 98

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE 85D	*	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF
CLK PCIE 90D	*	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X DIELECTRIC	?
CLK PCIE	*	0 5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP BOTTOM	=4 1 SPACING	?

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD
CPU RCOMP PHY	*	Y	0 254 MM	0 200 MM	3 0 MM	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU ITP	*	0 2 MM	?
CPU RCOMP	*	0 2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA 90D	*	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=6 1 SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP BOTTOM	=6 1 SPACING	?

NET TYPE

ELECTRICAL CONSTRAINT SET	PHYSICAL	SPACING		
SATA				
H50	SATA 90D	SATA	SATA_SSD_R2D_C_P	18 42
H49	SATA 90D	SATA	SATA_SSD_R2D_C_N	18 42
H51	SATA 90D	SATA	SATA_SSD_R2D_P	42
H52	SATA 90D	SATA	SATA_SSD_R2D_N	42
H53	SATA 90D	SATA	SATA_SSD_D2R_P	18 42
H54	SATA 90D	SATA	SATA_SSD_D2R_N	18 42
H55	SATA 90D	SATA	SATA_SSD_D2R_C_P	42
H56	SATA 90D	SATA	SATA_SSD_D2R_C_N	42
PCIE				
H31	PCIE 85D	PCIE	PCIE_USB3_1_R2D_P	
H32	PCIE 85D	PCIE	PCIE_USB3_1_R2D_N	
H21	PCIE 85D	PCIE	PCIE_USB3_1_R2D_C_P	
H22	PCIE 85D	PCIE	PCIE_USB3_1_R2D_C_N	
H23	PCIE 85D	PCIE	PCIE_USB3_1_D2R_P	
H24	PCIE 85D	PCIE	PCIE_USB3_1_D2R_N	
H25	PCIE 85D	PCIE	PCIE_USB3_1_D2R_C_P	
H26	PCIE 85D	PCIE	PCIE_USB3_1_D2R_C_N	
H27	PCIE 85D	PCIE	PCIE_USB3_2_R2D_P	
H28	PCIE 85D	PCIE	PCIE_USB3_2_R2D_N	
H29	PCIE 85D	PCIE	PCIE_USB3_2_R2D_C_P	
H30	PCIE 85D	PCIE	PCIE_USB3_2_R2D_C_N	
H32	PCIE 85D	PCIE	PCIE_USB3_2_D2R_P	
H33	PCIE 85D	PCIE	PCIE_USB3_2_D2R_N	
H34	PCIE 85D	PCIE	PCIE_USB3_2_D2R_C_P	
H35	PCIE 85D	PCIE	PCIE_USB3_2_D2R_C_N	
CPU ITP				
H43	CPU 50S	CPU ITP	XDP_BPM_L<7..0>	11 25
H45	CPU 50S	CPU ITP	CPU_CFG<17..0>	10 15 25
H44	CPU 50S	CPU ITP	XDP_OBSDATA_B<3..0>	25
H46	CPU 50S	CPU ITP	XDP_CPU_CFG<0>	25
H48	CPU 50S	CPU ITP	XDP_CPU_TDO	11 25
H47	CPU 50S	CPU ITP	XDP_CPU_TDI	11 25
H49	CPU 50S	CPU ITP	XDP_CPU_TMS	11 25
H50	CPU 50S	CPU ITP	XDP_CPU_TCK	11 25
H51	CPU 50S	CPU ITP	XDP_CPU_TRST_L	11 25
CPU_MISC				
	CPU RCOMP PHY	CPU RCOMP	CPU_PEG_COMP	10

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

NET TYPE

ELECTRICAL CONSTRAINT SET	PHYSICAL	SPACING		
PCIE GRAPHICS				
	PCIE 85D	PCIE	PEG_R2D_C_P<15..0>	9 77
	PCIE 85D	PCIE	PEG_R2D_C_N<15..0>	9 77
	PCIE 85D	PCIE	PEG_D2R_P<15..0>	9 77
	PCIE 85D	PCIE	PEG_D2R_N<15..0>	9 77
	PCIE 85D	PCIE	MXM_PCIE_R2D_P<7..0>	75 77
	PCIE 85D	PCIE	MXM_PCIE_R2D_N<7..0>	75 77
	PCIE 85D	PCIE	MXM_PCIE_D2R_P<7..0>	75 77
	PCIE 85D	PCIE	MXM_PCIE_D2R_N<7..0>	75 77
PCIE I/O				
	PCIE 85D	PCIE	PCIE_MINI_R2D_P	33
	PCIE 85D	PCIE	PCIE_MINI_R2D_N	33
	PCIE 85D	PCIE	PCIE_MINI_R2D_C_P	18 33
	PCIE 85D	PCIE	PCIE_MINI_R2D_C_N	18 33
	PCIE 85D	PCIE	PCIE_MINI_D2R_P	18 33
	PCIE 85D	PCIE	PCIE_MINI_D2R_N	18 33
	PCIE 85D	PCIE	PCIE_FW_R2D_P	39
	PCIE 85D	PCIE	PCIE_FW_R2D_N	39
	PCIE 85D	PCIE	PCIE_FW_R2D_C_P	18 39
	PCIE 85D	PCIE	PCIE_FW_R2D_C_N	18 39
	PCIE 85D	PCIE	PCIE_FW_D2R_P	18 39
	PCIE 85D	PCIE	PCIE_FW_D2R_N	18 39
	PCIE 85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE 85D	PCIE	PCIE_FW_D2R_C_N	39
DMI				
H41	CLK PCIE 90D	CLK PCIE	DMI_MIDBUS_CLK100M_N	
H42	CLK PCIE 90D	CLK PCIE	DMI_MIDBUS_CLK100M_P	
H39	CLK PCIE 90D	CLK PCIE	DMI_CLK100M_CPU_N	11 18
H37	CLK PCIE 90D	CLK PCIE	DMI_CLK100M_CPU_P	11 18
	PCIE 85D	PCIE	DMI_S2N_P<3..0>	10 19
	PCIE 85D	PCIE	DMI_S2N_N<3..0>	10 19
	PCIE 85D	PCIE	DMI_N2S_P<3..0>	10 19
	PCIE 85D	PCIE	DMI_N2S_N<3..0>	10 19
PCIE REF CLOCKS				
	CLK PCIE 90D	CLK PCIE	GPU_CLK100M_PCIE_P	9
	CLK PCIE 90D	CLK PCIE	GPU_CLK100M_PCIE_N	9
	CLK PCIE 90D	CLK PCIE	PCIE_CLK100M_MINI_P	18 33
	CLK PCIE 90D	CLK PCIE	PCIE_CLK100M_MINI_N	18 33
	CLK PCIE 90D	CLK PCIE	PCIE_CLK100M_FW_P	18 39
	CLK PCIE 90D	CLK PCIE	PCIE_CLK100M_FW_N	18 39
	ENET 100D	ENET MII	PCIE_CLK100M_ENET_P	18 37
	ENET 100D	ENET MII	PCIE_CLK100M_ENET_N	18 37
SATA				
	SATA 90D	SATA	SATA_HDD_R2D_C_P	18 42
	SATA 90D	SATA	SATA_HDD_R2D_C_N	18 42
	SATA 90D	SATA	SATA_HDD_R2D_P	42
	SATA 90D	SATA	SATA_HDD_R2D_N	42
	SATA 90D	SATA	SATA_HDD_D2R_P	18 42
	SATA 90D	SATA	SATA_HDD_D2R_N	18 42
	SATA 90D	SATA	SATA_HDD_D2R_C_P	42
	SATA 90D	SATA	SATA_HDD_D2R_C_N	42
	SATA 90D	SATA	SATA_ODD_R2D_C_P	18 42
	SATA 90D	SATA	SATA_ODD_R2D_C_N	18 42
	SATA 90D	SATA	SATA_ODD_R2D_P	42
	SATA 90D	SATA	SATA_ODD_R2D_N	42
	SATA 90D	SATA	SATA_ODD_D2R_P	18 42
	SATA 90D	SATA	SATA_ODD_D2R_N	18 42
	SATA 90D	SATA	SATA_ODD_D2R_C_P	42
	SATA 90D	SATA	SATA_ODD_D2R_C_N	42
CLOCKS				
	CLK PCIE 90D	CLK PCIE	PCH_CLK100M_DMI_P	18 26
	CLK PCIE 90D	CLK PCIE	PCH_CLK100M_DMI_N	18 26
	CLK PCIE 90D	CLK PCIE	PCH_CLK96M_DOT_P	18 26
	CLK PCIE 90D	CLK PCIE	PCH_CLK96M_DOT_N	18 26
	CLK PCIE 90D	CLK PCIE	PCH_CLK100M_SATA_P	18 26
	CLK PCIE 90D	CLK PCIE	PCH_CLK100M_SATA_N	18 26
	CLK PCIE 90D	CLK PCIE	ITPXDP_CLK100M_N	18 25
	CLK PCIE 90D	CLK PCIE	ITPXDP_CLK100M_P	18 25
	CLK PCIE 90D	CLK PCIE	ITPCPU_CLK100M_N	11 18
	CLK PCIE 90D	CLK PCIE	ITPCPU_CLK100M_P	11 18
H37	CLK PCIE 90D	CLK PCIE	XDP_CPU_CLK100M_P	25
H38	CLK PCIE 90D	CLK PCIE	XDP_CPU_CLK100M_N	25
UNUSED CLOCKS				
H35	CLK PCIE 90D	CLK PCIE	TP_CLK133M_PCH_N	26
H36	CLK PCIE 90D	CLK PCIE	TP_CLK133M_PCH_P	26
UNUSED PCIE				
H38	PCIE 85D	PCIE	MXM_PCIE_R2D_P<8..15>	75 77
H46	PCIE 85D	PCIE	MXM_PCIE_R2D_N<8..15>	75 77
H42	PCIE 85D	PCIE	MXM_PCIE_D2R_P<8..15>	75 77
H43	PCIE 85D	PCIE	MXM_PCIE_D2R_N<8..15>	75 77

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

PCIE/DMI/FDI/SATA CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

BRANCH

PAGE 102 OF 110

SHEET 90 OF 98

PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD
CLK PCH 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK PCH	*	=4 1 SPACING	?
COMP PCH	*	0 2 MM	?
ITP PCH	*	0 2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD
CLK PCI 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK PCI	*	0 2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD
CLK LPC 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0 15 MM	?
CLK LPC	*	0 2 MM	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x DIELECTRIC	?

SPI Interface Constraints

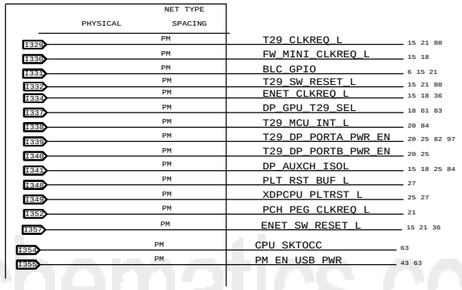
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

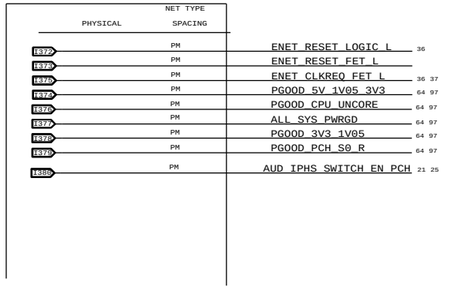
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0 2 MM	?

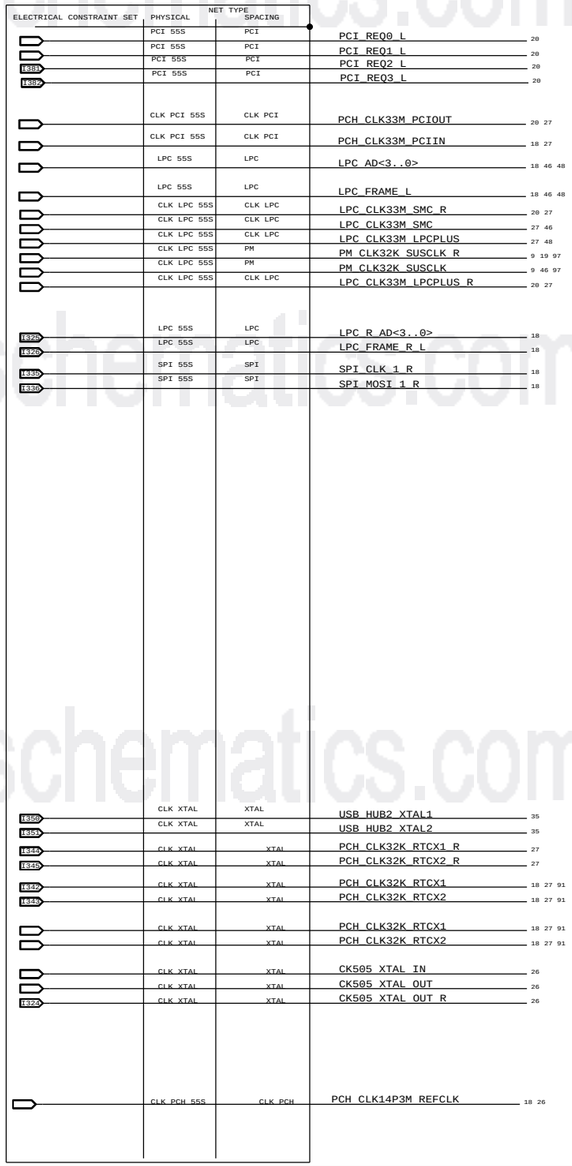
XTAL Constraints

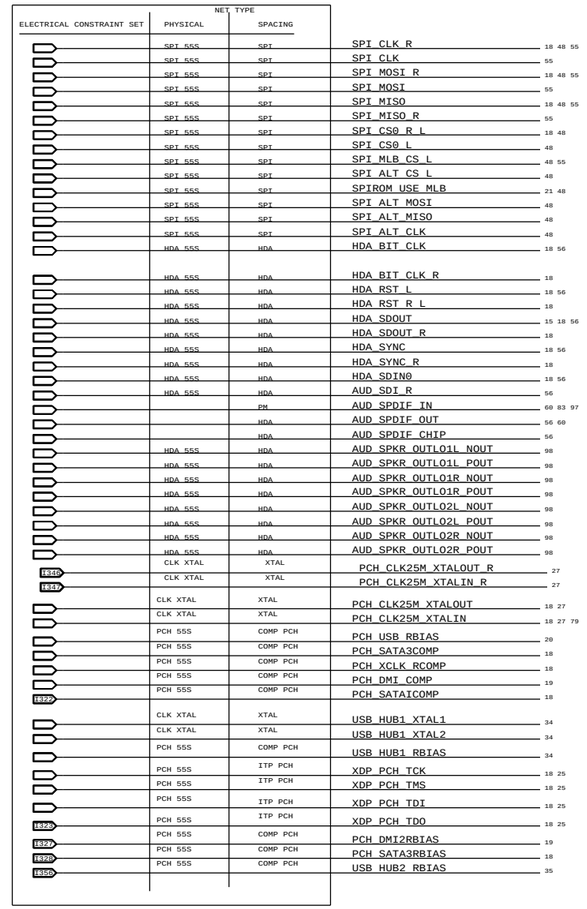
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK XTAL	*	100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X DIELECTRIC	?









SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

IBEX PEAK CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

BRANCH

PAGE 103 OF 110

SHEET 91 OF 98

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET MII	*	0 3 MM	?
ENET SE	*	=STANDARD	?

SOURCE:BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET 100D	*	100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET DIFF	*	0 6 MM	?
ENET DIFF2DIFF	*	=3 1 SPACING	?
ENET 2OTHER	*	=50MIL SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
50MIL SPACING	*	1 27 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET DIFF	ENET DIFF	*	ENET DIFF2DIFF
ENET DIFF T	*	*	ENET 2OTHER

CAESAR IV (SD) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD	*	=3 1 SPACING	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW 110D	*	110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF

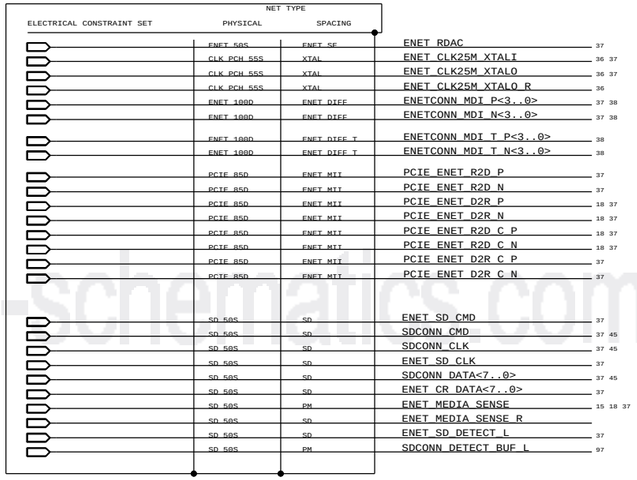
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW TP	*	=3 1 SPACING	?

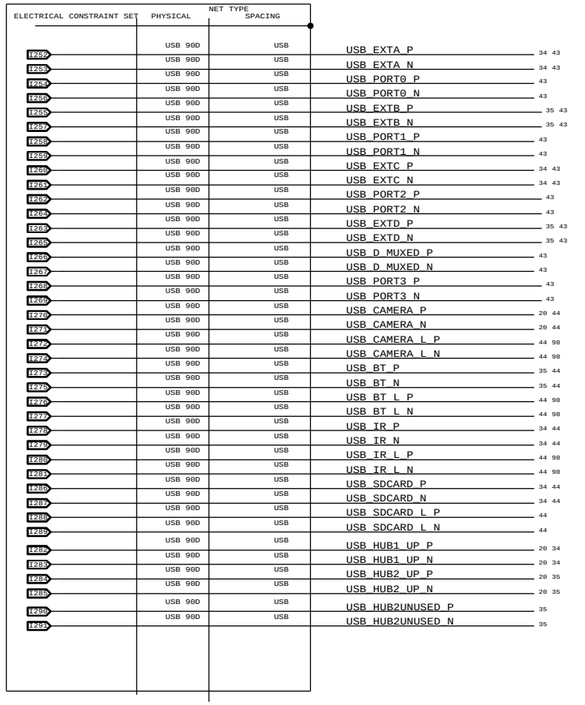
USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB 90D	*	90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

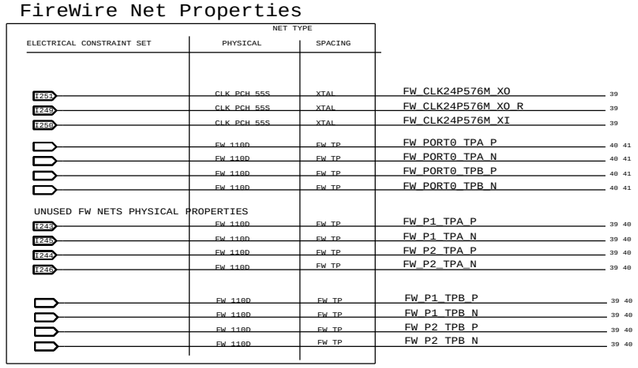
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=3 1 SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP BOTTOM	=4x DIELECTRIC	?





FireWire Net Properties



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
USB/ENET/SD/FW/AUD CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 104 OF 110
SHEET 92 OF 98

GRAPHICS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP 85D	*	85 OHM DIFF	=85 OHM DIFF	0 08MM	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3 1 SPACING	?

USE 5X_DIELECTRIC IN K62

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL CONSTRAINT SET
ASSINGED IN CONT. MGR. NET TYPE

	PHYSICAL	SPACING		
I160	DP 85D	DISPLAYPORT	DP_INTCONN_ML_C_P<3..0>	83
I174	DP 85D	DISPLAYPORT	DP_INTCONN_ML_C_N<3..0>	83
	DP 85D	DISPLAYPORT	DP_INTCONN_AUXCH_C_P	83
	DP 85D	DISPLAYPORT	DP_INTCONN_AUXCH_C_N	83
I153	DP 85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	81 83
I154	DP 85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	81 83
	DP 85D	DISPLAYPORT	DP_INTPNL_AUX_P	81 83
	DP 85D	DISPLAYPORT	DP_INTPNL_AUX_N	81 83
I181	DP 85D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	84
I180	DP 85D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	84
I183	DP 85D	DISPLAYPORT	DP_EXTA_AUXCH_P	84
I182	DP 85D	DISPLAYPORT	DP_EXTA_AUXCH_N	84
I172	DP 85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	78 84
I173	DP 85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	78 84
I177	DP 85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	78 84
I176	DP 85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	78 84
I191	DP 85D	DISPLAYPORT	DP_EXTB_ML_P<3..0>	
I192	DP 85D	DISPLAYPORT	DP_EXTB_ML_N<3..0>	
I193	DP 85D	DISPLAYPORT	DP_EXTB_AUXCH_P	
I194	DP 85D	DISPLAYPORT	DP_EXTB_AUXCH_N	
I195	DP 85D	DISPLAYPORT	DP_EXTB_ML_C_P<3..0>	
I196	DP 85D	DISPLAYPORT	DP_EXTB_ML_C_N<3..0>	
I189	DP 85D	DISPLAYPORT	DP_EXTB_AUXCH_C_P	
I190	DP 85D	DISPLAYPORT	DP_EXTB_AUXCH_C_N	
P199	DP 85D	DISPLAYPORT	MXM_DP_B_ML_P<3..0>	75 78
P200	DP 85D	DISPLAYPORT	MXM_DP_B_ML_N<3..0>	75 78
P203	DP 85D	DISPLAYPORT	MXM_DP_B_AUX_P	75 78
P202	DP 85D	DISPLAYPORT	MXM_DP_B_AUX_N	75 78
P205	DP 85D	DISPLAYPORT	MXM_DP_C_ML_P<3..0>	75 83
P206	DP 85D	DISPLAYPORT	MXM_DP_C_ML_N<3..0>	75 83
P209	DP 85D	DISPLAYPORT	MXM_DP_C_AUX_P	75 83
P208	DP 85D	DISPLAYPORT	MXM_DP_C_AUX_N	75 83
P211	DP 85D	DISPLAYPORT	MXM_DP_C_AUX_R_P	83
P212	DP 85D	DISPLAYPORT	MXM_DP_C_AUX_R_N	83
P207	DP 85D	DISPLAYPORT	MXM_DP_D_ML_P<3..0>	75 78
P208	DP 85D	DISPLAYPORT	MXM_DP_D_ML_N<3..0>	75 78
P201	DP 85D	DISPLAYPORT	MXM_DP_D_AUX_P	75 78
P210	DP 85D	DISPLAYPORT	MXM_DP_D_AUX_N	75 78

UNUSED VIDEO NET PHYSICAL CONSTRAINTS

DP 85D	DISPLAYPORT	MXM_LVDS_A_CLK_P	76 78
DP 85D	DISPLAYPORT	MXM_LVDS_A_CLK_N	76 78
DP 85D	DISPLAYPORT	MXM_LVDS_B_CLK_P	76 78
DP 85D	DISPLAYPORT	MXM_LVDS_B_CLK_N	76 78
DP 85D	DISPLAYPORT	MXM_LVDS_A_DATA_P<3..0>	76 78
DP 85D	DISPLAYPORT	MXM_LVDS_A_DATA_N<3..0>	76 78
DP 85D	DISPLAYPORT	MXM_LVDS_B_DATA_P<3..0>	76 78
DP 85D	DISPLAYPORT	MXM_LVDS_B_DATA_N<3..0>	76 78

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
GRAPHICS CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 105 OF 110
SHEET 93 OF 98

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	49
	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	49
	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	49
	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	49
	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	49
	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	49
	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	49
	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	49
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	49 94
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	49 94
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	49 94
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	49 94
	SMB_5SS	SMB	SMBUS_PCH_CLK	18 49
	SMB_5SS	SMB	SMBUS_PCH_DATA	18 49
	SMB_5SS	SMB	SML_PCH_0_CLK	18 49
	SMB_5SS	SMB	SML_PCH_0_DATA	18 49
	SMB_5SS	SMB	SML_PCH_1_CLK	18 49
	SMB_5SS	SMB	SML_PCH_1_DATA	18 49
	CLK_XTAL	XTAL	SMC_EXTAL	46 47
	CLK_XTAL	XTAL	SMC_XTAL	46 47
I254	SMB_5SS	SMB	I2C_VREFMRGN_DIMMA_SCL	28
I253	SMB_5SS	SMB	I2C_VREFMRGN_DIMMA_SDA	28
I255	SMB_5SS	SMB	I2C_VREFMRGN_DIMMB_SCL	28
I254	SMB_5SS	SMB	I2C_VREFMRGN_DIMMB_SDA	28
I265	SMB_5SS	SMB	SMB_BLC_TCON_SCL	6 49 81
I264	SMB_5SS	SMB	SMB_BLC_TCON_SDA	6 49 81
I268	SMB_5SS	SMB	I2C_TCON_SCL	81
I269	SMB_5SS	SMB	I2C_TCON_SDA	81
I266	SMB_5SS	SMB	SMB_BLC_PCH_SCL_R	6
I267	SMB_5SS	SMB	SMB_BLC_PCH_SDA_R	6

SMC THERMAL NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	THERM_DIFF	THERMAL	SNS_T1_1_P	52
	THERM_DIFF	THERMAL	SNS_T1_1_N	52
	THERM_DIFF	THERMAL	SNS_T2_DP2	52
	THERM_DIFF	THERMAL	SNS_T2_DN2	52
I209	THERM_DIFF	THERMAL	SNS_T1_2_P	52
I208	THERM_DIFF	THERMAL	SNS_T1_2_N	52
I207	THERM_DIFF	THERMAL	SNS_T1_3_P	52
I206	THERM_DIFF	THERMAL	SNS_T1_3_N	52
I211	THERM_DIFF	THERMAL	SNS_T1_4_P	52
I212	THERM_DIFF	THERMAL	SNS_T1_4_N	52
I213	THERM_DIFF	THERMAL	SNS_T1_5_P	52
I214	THERM_DIFF	THERMAL	SNS_T1_5_N	52
I215	THERM_DIFF	THERMAL	SNS_T1_6_P	52
I216	THERM_DIFF	THERMAL	SNS_T1_6_N	52
I217	THERM_DIFF	THERMAL	SNS_T1_7_P	52
I218	THERM_DIFF	THERMAL	SNS_T1_7_N	52
I224	THERM_DIFF	THERMAL	SNS_CPU_THERMD_P	10 52
I225	THERM_DIFF	THERMAL	SNS_CPU_THERMD_N	10 52
I219	THERM_DIFF	THERMAL	SNS_LCD_H_P	52
I210	THERM_DIFF	THERMAL	SNS_LCD_H_N	52
	THERM_DIFF	THERMAL	SNS_ODD_P	52 98
	THERM_DIFF	THERMAL	SNS_ODD_N	52 98
	THERM_DIFF	THERMAL	SNS_CPU_H_P	52
	THERM_DIFF	THERMAL	SNS_CPU_H_N	52
I222	THERM_DIFF	THERMAL	SNS_SKIN_RIGHT_P	52 98
I223	THERM_DIFF	THERMAL	SNS_SKIN_RIGHT_N	52 98
	THERM_DIFF	THERMAL	SNS_SKIN_LEFT_P	44 52 98
	THERM_DIFF	THERMAL	SNS_SKIN_LEFT_N	44 52 98
	THERM_DIFF	THERMAL	SNS_AMB_P	52 54 98
	THERM_DIFF	THERMAL	SNS_AMB_N	52 54 98
	THERM_DIFF	THERMAL	SNS_MXM_P	52
	THERM_DIFF	THERMAL	SNS_MXM_N	52
		THERMAL	HDD_OOB_TEMP_FILT	42 51 98
		THERMAL	HDD_OOB_TEMP_FB	42
		THERMAL	HDD_OOB_TEMP_R	51
		THERMAL	SMC_HDD_OOB_TEMP	46 51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	THERM_DIFF	THERMAL	SNS_I_MXM_P	50
	THERM_DIFF	THERMAL	SNS_I_MXM_N	50
	THERM_DIFF	THERMAL	SNS_DIMM_1V5_P	50
	THERM_DIFF	THERMAL	SNS_DIMM_1V5_N	50
	SNS_DIFF	THERMAL	VR_ISNS_VCORE_P	50 95
	SNS_DIFF	THERMAL	VR_ISNS_VCORE_N	50 95
	SNS_DIFF	THERMAL	VR_ISNS_VAXG_P	50 95
	SNS_DIFF	THERMAL	VR_ISNS_VAXG_N	50 95
I243	SNS_DIFF	THERMAL	VR_ISNS_1V05_P	95
I244	SNS_DIFF	THERMAL	VR_ISNS_1V05_N	95
I245	THERM_DIFF	THERMAL	SNS_CPU_1V5_P	50
I246	THERM_DIFF	THERMAL	SNS_CPU_1V5_N	50
I247	THERM_DIFF	THERMAL	SNS_VCCSA_P	50
I248	THERM_DIFF	THERMAL	SNS_VCCSA_N	50
I251	THERM_DIFF	THERMAL	SNS_1V05_PCH_P	50
I252	THERM_DIFF	THERMAL	SNS_1V05_PCH_N	50
I230		THERMAL	GND_SMC_AVSS	46 47 50 94
I241		THERMAL	SMC_CPU_1V5_ISENSE	46 50
I240		THERMAL	SMC_CPU_1V5_ISENSE_R	50
I242		THERMAL	SMC_CPU_1V5_VSENSE	46 50
I230		THERMAL	GND_SMC_AVSS	46 47 50 94
I238		THERMAL	SMC_DIMM_ISENSE	46 50
I239		THERMAL	SMC_DIMM_1V5_R	50
I231		THERMAL	SMC_DIMM_VSENSE	46 50
I230		THERMAL	GND_SMC_AVSS	46 47 50 94
I276		THERMAL	SMC_VCCSA_ISENSE	46 50
I275		THERMAL	SMC_VCCSA_ISENSE_R	50
I227		THERMAL	SMC_VCCSA_VSENSE	46 50
		THERMAL	GND_SMC_AVSS	46 47 50 94
		THERMAL	SMC_PCH_1V05_ISENSE	46 50
		THERMAL	SMC_VAXG_VSENSE	46 50
		THERMAL	SMC_PCH_1V05_VSENSE	46 50
I230		THERMAL	GND_SMC_AVSS	46 47 50 94
I235		THERMAL	SMC_1V05_ISENSE	46 50
I237		THERMAL	SMC_VAXG_ISENSE	46 50
I233		THERMAL	SMC_1V05_VSENSE	46 50
I236		THERMAL	SMC_GPU_ISENSE	46 50
		THERMAL	SMC_GPU_VSENSE	46 50
		THERMAL	SMC_VCORE_ISENSE	46 50
I234		THERMAL	SMC_VCORE_VSENSE	46 50
I232		THERMAL	SMC_CPU_VSENSE	

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: SMC Constraints

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 106 OF 110

SHEET: 94 OF 98

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

	NET TYPE PHYSICAL	SPACING	VOLTAGE	
U25	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE1 66
U29	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE2 66
U33	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE3 66
U27	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE4
U37	POWER	SWITCHNODE	1.5V	VR_AXG_PHASE1 67
U32	POWER	SWITCHNODE	3.3V	P3V3S5_REG_PHASE 70
U33	POWER	SWITCHNODE	5V	P5VS3_REG_PHASE 70
U34	POWER	SWITCHNODE	1.05V	P1V05S0_PHASE 68
U35	POWER	SWITCHNODE	1.05V	P1V05_REG_PHASE
U42	POWER	SWITCHNODE	3.4V	P3V42G3H_SW 72
U43	POWER	SWITCHNODE	3.3V	ENET_3V3_S3_SR_IN 37
U37	POWER	SWITCHNODE	1.2V	ENET_SR_LX 36 37
U33	POWER	SWITCHNODE	1.5V	DDR_REG_PHASE 71
U14	POWER	SWITCHNODE	1.8V	P1V8_REG_PHASE 71
U19	POWER	POWER	0.75V	PP0V75_S3_MEM_VREFCA_A 28 30
U42	POWER	POWER	0.75V	PP0V75_S3_MEM_VREFCA_B 28 31
U44	POWER	POWER	0.75V	PP0V75_S3_MEM_VREFDQ_A 28 30
U54	POWER	POWER	0.75V	PP0V75_S3_MEM_VREFDQ_B 28 31
U14	POWER	POWER	12V	PP12V_S0 6
U15	POWER	POWER	12V	PP12V_S0_CPU_FLTRD 65 66 67
U17	POWER	POWER	12V	PP12V_S0_FAN0_L 53 98
U17	POWER	POWER	12V	PP12V_S0_FAN1_L 53 98
U17	POWER	POWER	12V	PP12V_S0_FAN2_L 54 98
U27	POWER	POWER	12V	VR_CPU_DRV1_PVCC 66
U27	POWER	POWER	12V	VR_CPU_DRV1_UVCC 66
U27	POWER	POWER	12V	VR_CPU_DRV2_PVCC 66
U27	POWER	POWER	12V	VR_CPU_DRV2_UVCC 66
U27	POWER	POWER	12V	VR_CPU_DRV3_PVCC 66
U27	POWER	POWER	12V	VR_CPU_DRV3_UVCC 66
U27	POWER	POWER	12V	VR_CPU_DRV4_PVCC
U27	POWER	POWER	12V	VR_CPU_DRV4_UVCC
U27	POWER	POWER	12V	VR_AXG_DRV1_PVCC 67
U27	POWER	POWER	12V	VR_AXG_DRV1_UVCC
U59	POWER	POWER	12V	VR_CPU_DRV1_VCC 66
U68	POWER	POWER	12V	VR_CPU_DRV2_VCC 66
U89	POWER	POWER	12V	VR_CPU_DRV3_VCC 66
U60	POWER	POWER	12V	VR_CPU_DRV4_VCC
U65	POWER	POWER	12V	PP12V_S0_VG_OK 41
U65	POWER	POWER	12V	P12V_FW_R 41
U65	POWER	POWER	12V	P12V_FW_CL 41
U65	POWER	POWER	12V	P12V_FW_D 41
U26	POWER	POWER	12V	FW_PORT0_VP 41
U27	POWER	POWER	12V	FW_PORT0_VP_F 41
U54	POWER	POWER	12V	PPVP_FW_PHY_CPS 39 41
U68	POWER	POWER	12V	PP12V_S0_P1V05_VREG_VIN 68
U76	POWER	POWER	12V	VCCSA_PWR_RC 69
U77	POWER	POWER	12V	PP12V_S0_BL_R
U77	POWER	POWER	12V	PP12V_S5_FET 6 74
U78	POWER	POWER	12V	PP12V_LCD 81
U68	POWER	POWER	12V	PP12V_G3H 6
U77	POWER	POWER	12V	PP12V_S5 6
U77	POWER	POWER	12V	PP12V_S5_RSN 74
U26	POWER	POWER	0.75V	PPVTT_S0_DDR 6
U61	POWER	POWER	0.75V	PP0V75_S0 6
U70	POWER	POWER	0.925V	PPVCCSA_S0_CPU 6
U55	POWER	POWER	1.0V	PP1V0_FW_FWPHY_AVDD 39
U57	POWER	POWER	1.0V	PP1V0_S0_FW_VDD 40
U25	POWER	POWER	1.05V	PP1V05_S0_T29 6
U74	POWER	POWER	1.05V	PP1V05_S0_INPUT_VCCSA 6
U71	POWER	POWER	1.05V	PPVAXG_S0 6
U17	POWER	POWER	1.05V	PP1V05_S0 6
U74	POWER	POWER	1.05V	PP1V05_S0_PCH 6
U71	POWER	POWER	1.05V	PP1V05_S0_CK505_F 26
U77	POWER	POWER	1.05V	PPVOUT_S5_PCH_DCPSUS 22
U19	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA_F 17 22
U18	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F 17 22
U18	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_EXP_F 22 24
U23	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLLDMI2_F 22 24
U18	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_SATA_F 22 24
U25	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCCLKDMI_F 22 24
U75	POWER	POWER	1.1V	PPVCORE_S0_AXG_REG1 67
U75	POWER	POWER	1.1V	PPVCORE_S0_AXG_REGOUT 67
U29	POWER	POWER	1.1V	PPVCORE_S0_CPU 6
U29	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG1 66
U29	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG2 66
U66	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG3 66
U70	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG4
U55	VR_CTL_PHY	VR_CTL	1.2V	PP1V2_S3_ENET_INTREG 36
U66	POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_AVDDL 37
U65	POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_PCIEPLL 37
U65	POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_GPHYPLL 37
U19	POWER	POWER	1.5V	PP1V5_S0 6
U19	POWER	POWER	1.5V	PP1V5_S0_CK505_F 26
U68	POWER	POWER	1.5V	PP1V5_S0_CK505_R 26
U71	POWER	POWER	1.5V	PP1V5_S0_CPU_MEM 6
U75	POWER	POWER	1.5V	PP1V5_S0_CPU_SNS 6
U21	POWER	POWER	1.5V	PP1V5_S3 6
U74	POWER	POWER	1.5V	PP1V5_S3_MEM 6

POWER NET PROPERTIES

	NET TYPE PHYSICAL	SPACING	VOLTAGE	
U56	POWER	POWER	12V	PP12V_S0_MXM 6
U29	POWER	POWER	12V	PP12V_SLG1
U88	POWER	POWER	12V	PP3V3R12V_SW_DPAPWR_1
U89	POWER	POWER	12V	PP3V3R12V_SW_DPBPWR_1
U73	POWER	POWER	1.8V	USB_HUB2_VDD1V8 35
U75	POWER	POWER	1.8V	USB_HUB2_VDD1V8PLL 35
U74	POWER	POWER	1.8V	PP1V8_S0 6
U74	POWER	POWER	1.8V	PP1V8R1V5_S0_PCH_VCCVRM_F 22 24
U76	POWER	POWER	1.8V	USB_HUB1_VDD1V8 34
U75	POWER	POWER	1.8V	USB_HUB1_VDD1V8PLL 34
U82	POWER	POWER	1.8V	PP3V3R1V8_ENET_LR_OUT_REG 37
U78	POWER	POWER	3.3V	PPVBAT_G3_SYSCLK_R 79
U68	POWER	POWER	3.3V	USB_HUB1_VDDPLL3V3 34
U68	POWER	POWER	3.3V	USB_HUB1_VDDA3V3 34
U79	POWER	POWER	3.3V	USB_HUB2_VDDPLL3V3 35
U79	POWER	POWER	3.3V	USB_HUB2_VDDA3V3 35
U21	POWER	POWER	3.3V	PP3V3R1V5_PCH_VCCSUSHDA 22 24
U21	POWER	POWER	3.3V	PP3V3_S0_CK505_F 26
U22	POWER	POWER	3.3V	PP3V3_S0_HS_F 62
U68	POWER	POWER	3.3V	PP3V3_S0_SW_SD_PWR 45
U22	POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC_F 17 22
U33	POWER	POWER	3.3V	PP3V3_S0 6
U21	POWER	POWER	3.3V	PP3V3_SMCUSBMUX 43
U22	POWER	POWER	3.3V	PP3V3_S3 6 98
U66	POWER	POWER	3.3V	PP3V3_S3_BT_FLT 44
U57	POWER	POWER	3.3V	PP3V3_S3_MINI_CONN 33
U26	POWER	POWER	3.3V	PP3V3_S3_SDCARD_FLT 44
U74	POWER	SWITCHNODE	3.3V	PP3V3_S3_ENET_PHY_FET 36
U66	POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_XTALVDDH 37
U66	POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_BIASVDDH 37
U66	POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_AVDDH 37
U74	POWER	POWER	3.3V	ENET_XTALVDDH 37
U23	POWER	POWER	3.3V	PP3V3_S5 6
U76	POWER	POWER	3.3V	PP3V3_S5_REG_R 70
U27	POWER	POWER	3.3V	PPVOUT_S0_PCH_DCPSST 22
U26	POWER	POWER	3.3V	PPVOUT_PCH_DCPSUSBYP 22
U26	POWER	POWER	3.3V	PPVOUT_G3_PCH_DCPRTC 22
U27	POWER	POWER	3.3V	PPVBATT_G3_RTC 27
U26	POWER	POWER	3.3V	PPVBATT_G3_RTC_R 27
U20	POWER	POWER	3.3V	PP3V3_AUDIO_SPDIF_JACK 60 98
U20	POWER	POWER	3.3V	PP3V3_FW_FWPHY_VDDA 39
U20	POWER	POWER	3.3V	PP3V3_FW_FWPHY_VP25 39
U37	POWER	POWER	3.3V	PP3V3_S0_T29 6
U19	POWER	POWER	3.3V	PP3V3_SW_DPAPWR 78 84
U82	POWER	POWER	3.3V	PP3V3_SW_DPBPWR
U82	POWER	POWER	3.3V	PP3V3_G3H_RTC 18 19 22 27
U23	POWER	POWER	3.3V	PP3V3_G3H_AVREF_SMC 46 47
U28	POWER	POWER	3.4V	PP3V3_G3H_SMC_AVCC 46
U60	POWER	POWER	3.42V	PP3V42_G3H 6
U72	POWER	POWER	4.5V	4V5_REG_IN 56
U84	POWER	POWER	4.5V	PP4V5_AUDIO_ANALOG 56 61
U47	POWER	POWER	4.5V	PP5V_AUDIO_HPAMP 56
U80	POWER	POWER	5V	PP5V_LAMP_VREG 56 59
U81	POWER	POWER	5V	PP5V_RAMP_VREG 58
U28	POWER	POWER	5V	PP5V_S0 6 98
U28	POWER	POWER	5V	PP5V_S0_CPU_VCORE_VCC 65
U38	POWER	POWER	5V	PP5V_S0_PCH_V5REF 24
U60	POWER	POWER	5V	PP5V_S0_SATA_FET 42
U60	POWER	POWER	5V	5V_S0_P1V05REG_VIN 68
U76	POWER	POWER	5V	5V_S0_P1V05REG_VDD 68
U24	POWER	POWER	5V	PP5V_S3 6 98
U23	POWER	POWER	5V	PP5V_S3_VREFMRGN_A 28
U25	POWER	POWER	5V	PP5V_S3_VREFMRGN_B 28
U24	POWER	POWER	5V	PP5V_S3_DDR_REG_V5FILT 71
U24	POWER	POWER	5V	PP5V_S3_CAMERA_FLT 44
U26	POWER	POWER	5V	PP5V_S3_REG_R 70
U24	POWER	POWER	5V	PP5V_S3_IR_FLT 44 98
U76	POWER	POWER	5V	PP5V_S5 6
U24	POWER	POWER	5V	PP5V_S5_PCH_V5REFSUS 24
U24	POWER	POWER	5V	PP5V_USB_PORT0 43
U26	POWER	POWER	5V	PP5V_USB_PORT0_F 43
U24	POWER	POWER	5V	PP5V_USB_PORT1 43
U24	POWER	POWER	5V	PP5V_USB_PORT1_F 43
U24	POWER	POWER	5V	PP5V_USB_PORT2 43
U26	POWER	POWER	5V	PP5V_USB_PORT2_F 43
U26	POWER	POWER	5V	PP5V_USB_PORT3 43
U26	POWER	POWER	5V	PP5V_USB_PORT3_F 43
U25	POWER	POWER		DDR_REG_PGND 71
U24	POWER	POWER		DDR_REG_CSGND 71
U33	POWER	POWER	3.3V	PPVDDIO_25M_B 79
U34	POWER	POWER	1.05V	PPVDDIO_25M_A 79
U30	POWER	POWER	3.3V	PPVDDIO_25M_C 79
U35	POWER	POWER	12V	PP3V3R12V_SW_DPAPWR_R 85
U37	POWER	POWER	12V	PP3V3R12V_SW_DPAPWR_D 82
U38	POWER	POWER	1.5V	PP1V5_S0_DP_R 83

SENSING NET PROPERTIES

	NET TYPE PHYSICAL	SPACING	
U95	SNS DIFF	THERMAL	VR_CPU_ISNS1_P 65 66
U95	SNS DIFF	THERMAL	VR_CPU_ISNS1_N 65 66
U95	SNS DIFF	THERMAL	VR_CPU_ISNS1_R_N 65
U96	SNS DIFF	THERMAL	VR_CPU_ISNS2_P 65 66
U96	SNS DIFF	THERMAL	VR_CPU_ISNS2_N 65 66
U96	SNS DIFF	THERMAL	VR_CPU_ISNS2_R_N 65
U98	SNS DIFF	THERMAL	VR_CPU_ISNS3_P 65 66
U98	SNS DIFF	THERMAL	VR_CPU_ISNS3_N 65 66
U98	SNS DIFF	THERMAL	VR_CPU_ISNS3_R_N 65
U88	SNS DIFF	THERMAL	VR_CPU_ISNS4_P
U88	SNS DIFF	THERMAL	VR_CPU_ISNS4_N
U88	SNS DIFF	THERMAL	VR_CPU_ISNS4_R_N
U68	SNS DIFF	THERMAL	P1V05S0_ISN 68
U68	SNS DIFF	THERMAL	P1V05S0_ISP 68
U92	SNS DIFF	THERMAL	VR_AXG_ISNS_R_P 65
U92	SNS DIFF	THERMAL	VR_AXG_ISNS_R_N 65
U92	SNS DIFF	THERMAL	VR_AXG_ISNS_N 65 67
U92	SNS DIFF	THERMAL	VR_AXG_ISNS_P 65 67
U69	SNS DIFF	THERMAL	VR_ISNS_1V05_N 94
U69	SNS DIFF	THERMAL	VR_ISNS_1V05_P 94
U69	SNS DIFF	THERMAL	VR_ISNS_VAXG_N 50 94
U69	SNS DIFF	THERMAL	VR_ISNS_VAXG_P 50 94
U48	SNS DIFF	THERMAL	VR_ISNS_VCORE_N 50 94
U69	SNS DIFF	THERMAL	VR_ISNS_VCORE_P 50 94
U72	SNS DIFF		CPU_VAXG_SENSE_P 13 65
U74	SNS DIFF		CPU_VAXG_SENSE_N 13 65
U88	SNS DIFF		VR_AXG_VSNS_R_N 65
U48	SNS DIFF		VR_AXG_VSNS_R_P 65
U58	SNS DIFF		VR_AXG_VSEN 65
U59	SNS DIFF		VR_AXG_RGND 65
U71	SNS DIFF		VR_AXG_VSNS_XW_N 65
U45	SNS DIFF		VR_AXG_VSNS_XW_P 65
U61	SNS DIFF		CPU_VCC_SENSE_N 13 65
U61	SNS DIFF		CPU_VCC_SENSE_P 13 65
U61	SNS DIFF		VR_CPU_VSEN 65
U71	SNS DIFF		VR_CPU_RGND 65
U72	SNS DIFF		VR_CPU_VSNS_R_N 65
U62	SNS DIFF		VR_CPU_VSNS_R_P 65
U63	SNS DIFF		VR_CPU_VSNS_XW_P 65
U64	SNS DIFF		VR_CPU_VSNS_XW_N 65
T66	SNS DIFF		CPU_VCCIO_SENSE_P 13 68
T67	SNS DIFF		CPU_VCCIO_SENSE_N 13 68
U45	SNS DIFF		P1V05S0_VSEN 68
U45	SNS DIFF		P1V05S0_RTN 68

VR CTRL NET PROPERTIES

	NET TYPE PHYSICAL	SPACING	
U27	VR CTL PHY	SWITCHNODE	VR_CPU_PH1_SNUB 66
U31	VR CTL PHY	SWITCHNODE	VR_CPU_PH2_SNUB 66
U33	VR CTL PHY	SWITCHNODE	VR_CPU_PH3_SNUB 66
U35	VR CTL PHY	SWITCHNODE	VR_CPU_PH4_SNUB
U95	VR CTL PHY	VR CTL	VR_CPU_COMP 65
U69	VR CTL PHY	VR CTL	VR_AXG_TM 65
U92	VR CTL PHY	VR CTL	VR_AXG_PWM_R 65
U61	VR CTL PHY	VR CTL	VR_AXG_PWM 65 67
U62	VR CTL PHY	VR CTL	VR_CPU_PWM2 65 66
U62	VR CTL PHY	VR CTL	VR_CPU_PWM1 65 66
U84	VR CTL PHY	VR CTL	VR_CPU_PWM1_R 65
U34	VR CTL PHY	VR CTL	VR_CPU_PWM2_R 65
U34	VR CTL PHY	VR CTL	VR_CPU_PWM3 65 66
U34	VR CTL PHY	VR CTL	VR_CPU_PWM3_R 65
U35	VR CTL PHY	VR CTL	VR_CPU_PWM4
U35	VR CTL PHY	VR CTL	VR_CPU_PWM4_R 65
U41	VR CTL PHY	VR CTL	VR_AXG_SW_FREQ 65
U41	VR CTL PHY	VR CTL	VR_EN_PWR_OVP 65
U39	VR CTL PHY	VR CTL	VR_RSET 65
U39	VR CTL PHY	VR CTL	VR_EN_PWR_OVP_R 65
U39	VR CTL PHY	VR CONTROL	VR_CPU_BOOT1_RC 66
U35	VR CTL PHY	VR CONTROL	VR_CPU_BOOT2_RC 66
U36	VR CTL PHY	VR CONTROL	VR_CPU_BOOT3_RC 66
U69	VR CTL PHY	VR CONTROL	VR_AXG_BOOT1_RC 67
U35	VR CTL PHY	VR CTL	VR_CPU_BOOT4_RC
U35	VR CTL PHY	VR CONTROL	VR_CPU_DRV1_BOOT 66
U36	VR CTL PHY	VR CTL	VR_CPU_DRV1_GDSEL 66
U36	VR CTL PHY	VR CONTROL	VR_CPU_DRV1_LGATE 66
U36	VR CTL PHY	VR CONTROL	VR_CPU_DRV1_UGATE 66
U36	VR CTL PHY	VR CONTROL	VR_CPU_DRV2_BOOT 66
U36	VR CTL PHY	VR CTL	VR_CPU_DRV2_GDSEL 66
U36	VR CTL PHY	VR CONTROL	VR_CPU_DRV2_LGATE 66
U36	VR CTL PHY	VR CONTROL	VR_CPU_DRV2_UGATE 66
U37	VR CTL PHY	VR CONTROL	VR_CPU_DRV3_BOOT 66
U37	VR CTL PHY	VR CTL	VR_CPU_DRV3_GDSEL 66
U37	VR CTL PHY	VR CONTROL	VR_CPU_DRV3_LGATE 66
U37	VR CTL PHY	VR CONTROL	VR_CPU_DRV3_UGATE 66
U38	VR CTL PHY	VR CTL	VR_CPU_DRV4_BOOT
U38	VR CTL PHY	VR CTL	VR_CPU_DRV4_GDSEL
U38	VR CTL PHY	VR CONTROL	VR_CPU_DRV4_LGATE
U38	VR CTL PHY	VR CONTROL	VR_CPU_DRV4_UGATE
U69	VR CTL PHY	VR CONTROL	VR_AXG_DRV1_BOOT 67
U69	VR CTL PHY	VR CTL	VR_AXG_DRV1_UGATE_R 67
U69	VR CTL PHY	VR CONTROL	VR_AXG_DRV1_LGATE 67
U69	VR CTL PHY	VR CONTROL	VR_AXG_DRV1_UGATE 67
U38	VR CTL PHY	VR CTL	VR_CPU_SW_FREQ 65
U38	VR CTL PHY	VR CTL	VR_CPU_FB 65
U38	VR CTL PHY	VR CTL	VR_CPU_FB_R 65
U38	VR CTL PHY	VR CTL	VR_CPU_RAMP_ADJ 65
U39	VR CTL PHY	VR CTL	VR_CPU_IMON 50 65
U63	VR CTL PHY	VR CTL	VR_CPU_SUTH 65
U37	VR CTL PHY	VR CTL	VR_CPU_N_PSI 65
U38	VR CTL PHY	VR CTL	VR_CPU_FDVID 65
U43	VR CTL PHY	VR CTL	VR_CPU_PSICOMP 65
U39	VR CTL PHY	VR CTL	VR_CPU_IAUTO 65
U64	VR CTL PHY	VR CTL	VR_CPU_PSICOMP1 65
U64	VR CTL PHY	VR CTL	VR_CPU_PSICOMP2 65
U64	VR CTL PHY	VR CTL	VR_CPU_FB_RC 65
U64	VR CTL PHY	VR CTL	VR_CPU_FB2 65
U64	VR CTL PHY	VR CTL	VR_CPU_IMON_R 65
U64	VR CTL PHY	VR CTL	VR_CPU_HFREQ_COMP 65
U68	VR CTL PHY	SWITCHNODE	VR_AXG_PH1_SNUB 67
U92	VR CTL PHY	VR CTL	VR_AXG_IMON 50 65
U65	VR CTL PHY	VR CTL	VR_AXG_IMON_R 65
U62	VR CTL PHY	VR CTL	VR_AXG_HFREQ_COMP 65
U63	VR CTL PHY	VR CTL	VR_AXG_FB 65
U62	VR CTL PHY	VR CTL	VR_SEN_R1 65
U62	VR CTL PHY	VR CTL	VR_SEN_R2 65
U63	VR CTL PHY	VR CTL	VR_SEN_R3 65
U63	VR CTL PHY	VR CTL	VR_AXG_COMP_RC 65
U63	VR CTL PHY	VR CTL	VR_AXG_COMP 65
U63	VR CTL PHY	VR CTL	VR_AXG_TCOMP 65
U38	VR CTL PHY	SWITCHNODE	P1V05S0_UGATE 68
U39	VR CTL PHY	SWITCHNODE	P1V05S0_LGATE 68
U39	VR CTL PHY	VR CTL	P1V05S0_BOOT 68
U40	VR CTL PHY	VR CTL	P1V05S0_BOOT_R 68
U71	VR CTL PHY	VR CTL	P1V05_IMON 50 68
U42	VR CTL PHY	VR CTL	P1V05S0_FB 68
U39	VR CTL PHY	VR CTL	P1V05S0_PHASE_L 68
U59	VR CTL PHY	VR CTL	P1V05S0_VW 68
U40	VR CTL PHY	VR CTL	P1V05S0_COMP 68
U40	VR CTL PHY	VR CTL	P1V05S0_ICOMP 68
U40	VR CTL PHY	VR CTL	P1V05_S0_VDIFF 68
U40	VR CTL PHY	VR CTL	P1V05S0_COMP_C 68
U40	VR CTL PHY	VR CTL	P1V05S0_VDIF_C 68
U40	VR CTL PHY	VR CTL	P1V05S0_VO 68
U40	VR CTL PHY	VR CTL	P1V05S0_OCSET 68
U40	VR CTL PHY	VR CTL	P1V05S0_SNUBBER 68
U73	VR CTL PHY	VR CTL	P1V05_REG_VFB
U76	VR CTL PHY	VR CTL	ENET_SR_VFB 36 37
U76	VR CTL PHY	VR CTL	P1V05S0_ISP_R 68
U80	VR CTL PHY	VR CTL	VCCSA_CNTRL_INPUT2_R 69 95
U80	VR CTL PHY	VR CTL	T29BST_FBX
U67	VR CTL PHY	VR CTL	P3V42G3H_BOOST 72
U68	VR CTL PHY	VR CTL	P3V42G3H_FB 72

VR CTRL NET PROPERTIES

	NET TYPE PHYSICAL	SPACING	
U37	VR CTL PHY	VR CTL	DDR_REG_CS 71
U38	VR CTL PHY	VR CTL	DDR_REG_FB 71
U38	VR CTL PHY	VR CONTROL	DDR_REG_LGATE 71
U39	VR CTL PHY	VR CONTROL	DDR_REG_UGATE 71
U44	VR CTL PHY	VR CONTROL	DDR_REG_BOOT 71
U42	VR CTL PHY	VR CTL	DDR_REG_BOOT_R 71
U42	VR CTL PHY	VR CTL	DDR_REG_VDDQSNS 71
U44	VR CTL PHY	VR CTL	DDR_REG_VTTSNS 71
U24	VR CTL PHY	VR CTL	DDR_REG_PHASE_R 71
U27	VR CTL PHY	VR CTL	DDR_REG_UGATE_R 71
U25	VR CTL PHY	SWITCHNODE	1V5_SNUBBER 71
U42	VR CTL PHY	VR CTL	P1V8_REG_VFB 71
U27	VR CTL PHY	VR CTL	P1V8_REG_SYNC 71
U45	VR CTL PHY	VR CONTROL	P3V3S5_REG_BOOT 70
U45	VR CTL PHY	VR CONTROL	P3V3S5_REG_BOOT_R 70
U45	VR CTL PHY	VR CTL	P3V3S5_REG_FB 70
U45	VR CTL PHY	VR CTL	P3V3S5_REG_ISEN 70
U45	VR CTL PHY	VR CONTROL	P3V3S5_REG_LGATE 70
U45	VR CTL PHY	VR CTL	P3V3S5_REG_OCSET 70
U45	VR CTL PHY	VR CONTROL	P3V3S5_REG_VOUT1 70
U47	VR CTL PHY	VR CONTROL	P3V3S5_REG_FSET1 70
U45	VR CTL PHY	VR CONTROL	P3V3S5_REG_UGATE 70
U45	VR CTL PHY	VR CTL	P3V3S5_REG_SNUB 70
U45	VR CTL PHY	VR CONTROL	P5VS3_REG_BOOT 70
U46	VR CTL PHY	VR CTL	P5VS3_REG_FB 70
U46	VR CTL PHY	VR CTL	P5VS3_REG_ISEN 70
U46	VR CTL PHY	VR CONTROL	P5VS3_REG_LGATE 70
U46	VR CTL PHY	VR CTL	P5VS3_REG_OCSET 70
U46	VR CTL PHY	VR CTL	P5VS3_REG_FSET2 70
U46	VR CTL PHY	VR CONTROL	P5VS3_REG_UGATE 70
U47	VR CTL PHY	VR CONTROL	P5VS3_REG_VOUT2 70
U41	VR CTL PHY	VR CTL	VCCSA_CNTRL_INPUT1 69
U41	VR CTL PHY	VR CTL	VCCSA_CNTRL_INPUT2 69
U75	VR CTL PHY	VR CTL	VCCSA_CNTRL_INPUT2_R 69 95
U22	VR CTL PHY	VR CTL	VCCSA_OUT 69
U22	VR CTL PHY	VR CTL	VCCSA_GATE 69
U30	VR CTL PHY	VR CTL	VCCSA_REF 69
U31	VR CTL PHY	VR CTL	VCCSA_CRL 69
U22	VR CTL PHY	VR CTL	CPU_VCCSA_SENSE 13 69
U79	VR CTL PHY	VR CTL	VR_CPU_TM 65
U32	VR CTL PHY	PM	3V3R2V9_DPAPWR_ADJ 82 97

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VID_PHY	*	50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL	*	0.35MM	?

VR VID NET PROPERTIES

	NET TYPE PHYSICAL	SPACING	
U72	VID PHY	VR CTL VIDS	CPU_VIDSCLK_R 13
U72	VID PHY	VR CTL VIDS	CPU_VIDALERT_L_R 13
U74	VID PHY	VR CTL VIDS	CPU_VIDSOUT_R 13
U49	VID PHY	VR CTL VIDS	CPU_VIDSCLK 13 65
U49	VID PHY	VR CTL VIDS	CPU_VIDALERT_L 13 65
U50	VID PHY	VR CTL VIDS	CPU_VIDSOUT 13 65

PULL UP STUB < 1 INCH
VID LENGTH SKEW < 1 INCH
VID LENGTH RANGE< 1 TO 15 INCH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_VIDS	*	=4X_DIELECTRIC	?

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE: POWER CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 107 OF 110
SHEET 95 OF 98

T29 ELECTRICAL ROUTES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29 90D	*	90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	*	=5X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	TOP BOTTOM	=7X DIELECTRIC	?

T29 PCI-EXPRESS (SAME RULE AS PCIE)

T29 SPI INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29 SPI 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29 SPI	*	0 2 MM	?

T29 XTAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29 XTAL 100D	*	100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29 XTAL	*	=4X DIELECTRIC	?

T29 SMBUS INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29 SMB 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29 SMB	*	=2x DIELECTRIC	?

GREEN CLOCK CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK 25M 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK 25M	*	=5X DIELECTRIC	?

T29 BIAS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29 COMP	*	0 2 MM	?

T29 NET PROPERTIES

ELECTRICAL CONSTRAINT SET	PHYSICAL (NET TYPE)	SPACING (NET TYPE)	
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_P<3..0> 78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_N<3..0> 78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_D2R_C_P<3..0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29_D2R_C_N<3..0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29_R2D_P<3..0> 84
NO_TEST=TRUE	T29_90D	T29	T29_R2D_N<3..0> 84
NO_TEST=TRUE	T29_90D	T29	T29_D2R_P<3..0> 78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_D2R_N<3..0> 78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_F_P<3..0> 84
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_F_N<3..0> 84
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_P<3..0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_N<3..0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_P<3..0>
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_N<3..0>
NO_TEST=TRUE	T29_90D	T29	DP_A_EXT_AUXCH_P 84 85
NO_TEST=TRUE	T29_90D	T29	DP_A_EXT_AUXCH_N 84 85
NO_TEST=TRUE	T29_90D	T29	DP_SDRVA_AUXCH_C_P 84
NO_TEST=TRUE	T29_90D	T29	DP_SDRVA_AUXCH_C_N 84
NO_TEST=TRUE	T29_90D	T29	DP_SDRVB_AUXCH_C_P
NO_TEST=TRUE	T29_90D	T29	DP_SDRVB_AUXCH_C_N
NO_TEST=TRUE	T29_90D	T29	DP_B_EXT_AUXCH_P
NO_TEST=TRUE	T29_90D	T29	DP_B_EXT_AUXCH_N
NO_TEST=TRUE	T29_90D	T29	T29DPA_D2R1_AUXCH_P 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_D2R1_AUXCH_N 85
NO_TEST=TRUE	T29_90D	T29	T29DPB_D2R3_AUXCH_P
NO_TEST=TRUE	T29_90D	T29	T29DPB_D2R3_AUXCH_N
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_N<0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_P<0> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_N<2> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_P<2> 84 85
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_N<0>
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_P<0>
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_N<2>
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_P<2>
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0> 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0> 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0> 18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0> 18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0> 18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0> 18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0> 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0> 86
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P 18 86
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N 18 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0> 83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0> 83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_P<3..0> 83 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_N<3..0> 83 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0> 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0> 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0> 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0> 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0> 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0> 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0> 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0> 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N 78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_R_C_P 83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_R_C_N 83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P 83 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N 83 86
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_AUXCH_P 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_AUXCH_N 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_AUXCH_P
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_AUXCH_N
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_C_P<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_C_N<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_P<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_N<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_R_P<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_R_N<3..0> 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_C_P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_C_N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_R_P<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_R_N<3..0>
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_A_RSVD_N 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_A_RSVD_P 84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_B_RSVD_N
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_B_RSVD_P

T29 NET PROPERTIES

ELECTRICAL CONSTRAINT SET	PHYSICAL (NET TYPE)	SPACING (NET TYPE)	
	T29_SPI_55S	T29_SPI	JTAG_T29_TDI 15 21 86
	T29_SPI_55S	T29_SPI	JTAG_T29_TMS 15 18 86
	T29_SPI_55S	T29_SPI	JTAG_T29_TCK 15 21 25 86
	T29_SPI_55S	T29_SPI	JTAG_T29_TDO 15 21 86
L43J	T29_SPI_55S	T29_SPI	T29_SPI_MOSI 86
L43H	T29_SPI_55S	T29_SPI	T29_SPI_MISO 86
L43G	T29_SPI_55S	T29_SPI	T29_SPI_CS_L 86
L44D	T29_SPI_55S	T29_SPI	T29_SPI_CLK 86
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29 79 86 96
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R 86 96
	T29_SMB_55S	T29_SMB	I2C_T29_SDA 49 86
	T29_SMB_55S	T29_SMB	I2C_T29_SCL 49 86
L42J	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB 79
L42G	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET 79
L42E	CLK_25M_55S	CLK_25M	ENET_CLK25M_XTALI_OSC 36 79
L42A	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_CLK 79
L43K	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29 79 86 96
L42C	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R 86 96
L42C	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X2 79
L42D	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X2_R 79
L42F	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X1 79
L43L	T29_55S	T29_COMP	T29_RSENSE 86
L43C	T29_55S	T29_COMP	T29_RBIAS 86
L43E		T29_COMP	T29_A_BIAS 82 84 85
L43F		T29_COMP	T29_B_BIAS
L42H		T29_COMP	DP_A_BIAS 84

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

T29 CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

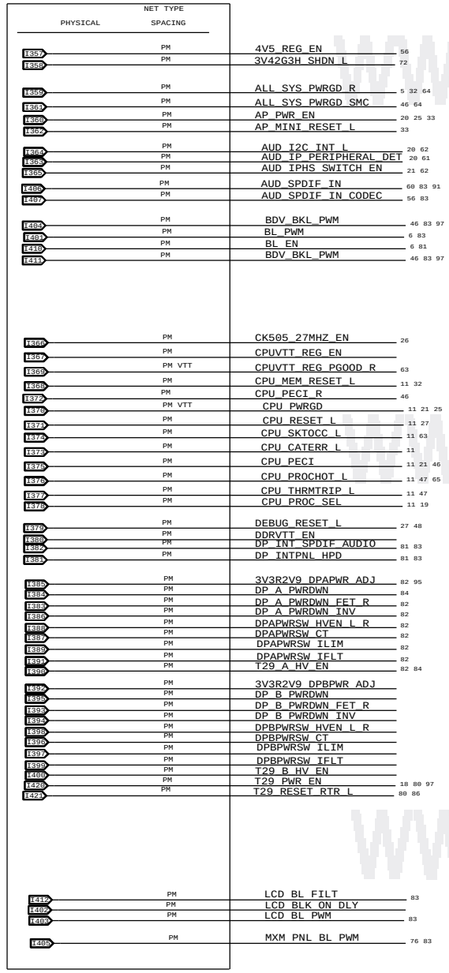
BRANCH

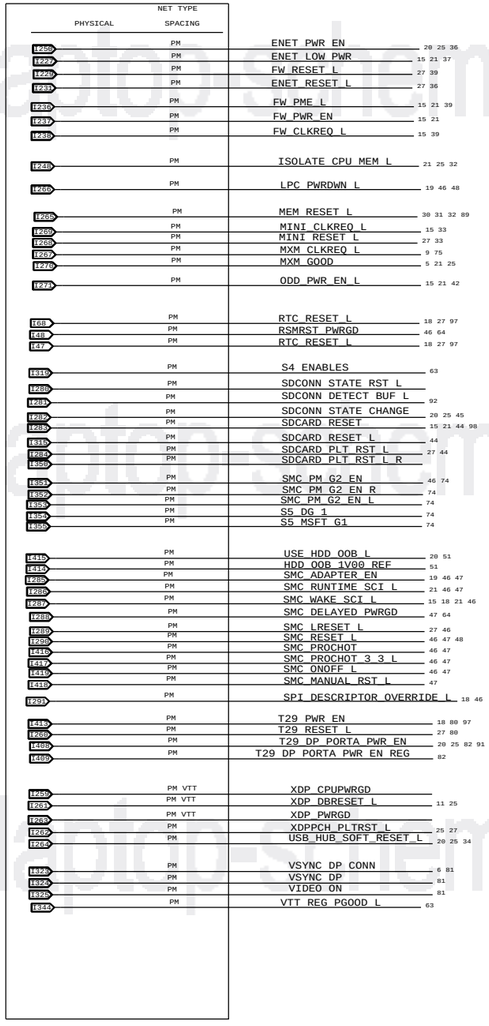
PAGE 108 OF 110

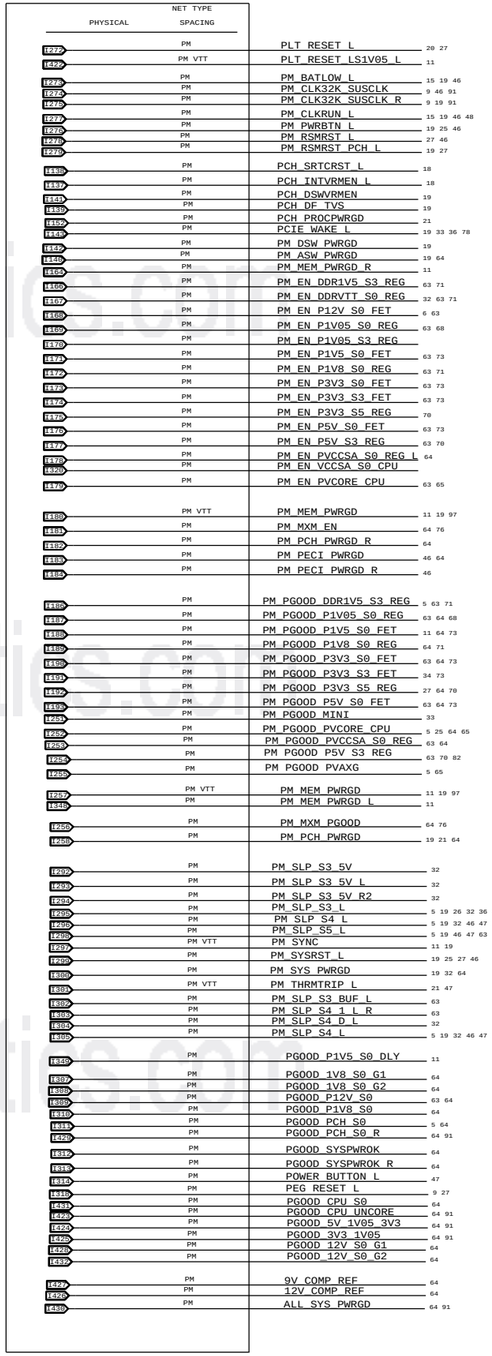
SHEET 96 OF 98

PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2 1 SPACING
PM VTT	PM VTT	*	2 1 SPACING
PM VTT	*	*	3 1 SPACING
PM VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT







SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
PM RESETS ENABLES PGOOD CONST

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 109 OF 110
SHEET 97 OF 98

FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

95 6 IN PP5V_S3 FUNC_TEST_TRUE
MIN ALLOWED TPS=1
92 44 IN USB_CAMERA_L_P FUNC_TEST=TRUE
92 44 IN USB_CAMERA_L_N FUNC_TEST=TRUE

92 44 IN USB_BT_L_P FUNC_TEST_TRUE
92 44 IN USB_BT_L_N FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
1 PP3V3_S3 TESTPOINT NEAR J4700
6 GROUND TESTPOINTS NEAR J4700

J4750 USB CARD READER

97 44 21 15 IN SDCARD_RESET FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4780 IR BOARD

92 44 IN USB_IR_L_P FUNC_TEST_TRUE
92 44 IN USB_IR_L_N FUNC_TEST=TRUE

95 44 IN PP5V_S3_IR_FLT FUNC_TEST_TRUE

1 GROUND TESTPOINT NEAR J4780

J4520 SATA ODD (HIGH SPEED)

46 42 IN SMC_ODD_DETECT FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
1 GROUND TESTPOINTS NEAR J4520

J5551 ODD TEMP SENSOR

94 52 IN SNS_ODD_P FUNC_TEST_TRUE
94 52 IN SNS_ODD_N FUNC_TEST_TRUE

J5600 ODD FAN

53 IN FAN_0_PWR_L FUNC_TEST_TRUE
53 IN FAN_TACH0_L FUNC_TEST_TRUE
95 53 IN PP12V_S0_FAN0_L FUNC_TEST_TRUE
53 IN FAN_0_GND FUNC_TEST=TRUE

J5700 CPU FAN

54 IN FAN_2_PWR_L FUNC_TEST_TRUE
54 IN FAN_TACH2_L FUNC_TEST=TRUE
95 54 IN PP12V_S0_FAN2_L FUNC_TEST=TRUE
54 IN FAN_2_GND FUNC_TEST=TRUE

94 54 52 IN SNS_AMB_P FUNC_TEST_TRUE
94 54 52 IN SNS_AMB_N FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J5700

J5601 HD FAN

53 IN FAN_1_PWR_L FUNC_TEST=TRUE
53 IN FAN_TACH1_L FUNC_TEST=TRUE
95 53 IN PP12V_S0_FAN1_L FUNC_TEST=TRUE
53 IN FAN_1_GND FUNC_TEST_TRUE

J5400 HDD TEMP SENSOR

94 51 42 IN HDD_OOB_TEMP_FILT FUNC_TEST=TRUE

1 GROUND TESTPOINTS NEAR J5400

J5560 SKIN TEMP SENSOR

94 52 44 IN SNS_SKIN_LEFT_P FUNC_TEST_TRUE
94 52 44 IN SNS_SKIN_LEFT_N FUNC_TEST_TRUE

94 52 IN SNS_SKIN_RIGHT_P FUNC_TEST_TRUE
94 52 IN SNS_SKIN_RIGHT_N FUNC_TEST_TRUE

J6602 AUDIO RIGHT SPEAKER

91 IN AUD_SPKR_OUTL02R_POUT FUNC_TEST_TRUE
91 IN AUD_SPKR_OUTL02R_NOUT FUNC_TEST_TRUE
91 IN AUD_SPKR_OUTL01R_POUT FUNC_TEST_TRUE
91 IN AUD_SPKR_OUTL01R_NOUT FUNC_TEST_TRUE

J6603 AUDIO LEFT SPEAKER

91 IN AUD_SPKR_OUTL02L_POUT FUNC_TEST_TRUE
91 IN AUD_SPKR_OUTL02L_NOUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTL01L_POUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTL01L_NOUT FUNC_TEST=TRUE

J6600 AUDIO AUXILIARY CONNECTOR

2 TP'S
95 60 IN PP3V3_AUDIO_SPDIF_JACK FUNC_TEST=TRUE
MIN ALLOWED TPS=2

60 IN AUD_LI_DET_JACK FUNC_TEST_TRUE

60 IN AUD_LI_R_JACK FUNC_TEST=TRUE
60 IN AUD_LI_GND_JACK FUNC_TEST=TRUE
60 IN AUD_LI_L_JACK FUNC_TEST=TRUE

60 IN HS_MIC_HI_JACK FUNC_TEST_TRUE

60 IN AUD_HP_L_JACK FUNC_TEST=TRUE
60 IN AUD_HP_GND_JACK FUNC_TEST=TRUE
60 IN AUD_HP_R_JACK FUNC_TEST=TRUE
60 IN AUD_HP_TYPEDET_JACK FUNC_TEST=TRUE
60 IN AUD_IP_PERPH_JACK FUNC_TEST=TRUE
60 IN AUD_HP_TIPDET_JACK FUNC_TEST=TRUE

60 IN AUD_SPDIFIN_JACK FUNC_TEST=TRUE

4 GROUND TESTPOINTS NEAR J6600

GND 17 TP'S FUNC_TEST_TRUE
MIN ALLOWED TPS=17

95 6 IN PP3V3_S3 2 TP'S FUNC_TEST_TRUE
MIN ALLOWED TPS=2

95 6 IN PP5V_S0 FUNC_TEST_TRUE
MIN ALLOWED TPS=1

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: K60/K62 ICT/FCT

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D
REVISION: 11.1.0
BRANCH:
PAGE: 110 OF 110
SHEET: 98 OF 98