1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0002265654	ENGINEERING RELEASED	2013-08-22

SCHEM,MLB_KEPLER,J45G

8/22/2013 DVT

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0675	1	SCHEM,MLB_KEPLER,J45G	SCH	CRITICAL	
820-3787	1	PCBF,MLB_KEPLER,J45G	PCB	CRITICAL	

DRAWING

TITLE=MLB
ABBREV=ABBREV
LAST MODIFIED=Thu Aug 22 12:19:14 2013

DRAWING TITLE: SCHEM,MLB,KEPLER,J45G

Apple Inc.

DRAWING NUMBER: 051-0675 | SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0177	COMMON PARTS,MLB,KEPLER,J45	J45G_COMMON
985-0181	DEV,MLB,KEPLER,J45	J45G_DEVEL:DVT
639-5245	PCBA,MLB,KEPLER,CRW_BEST,8G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600_S,FB_2G_HYNIX_A_DIE
639-5246	PCBA,MLB,KEPLER,CRW_BEST,8G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600_S,FB_2G_ELPIDA
639-5247	PCBA,MLB,KEPLER,CRW_BSET,8G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600_S,FB_2G_HYNIX_A_DIE
639-5248	PCBA,MLB,KEPLER,CRW_BEST,8G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600_S,FB_2G_ELPIDA
639-5249	PCBA,MLB,KEPLER,CRW_BEST,8G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600_S,FB_2G_HYNIX_A_DIE
639-5250	PCBA,MLB,KEPLER,CRW_BEST,8G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600_S,FB_2G_ELPIDA
639-5251	PCBA,MLB,KEPLER,CRW_BEST,16G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600,FB_2G_HYNIX_A_DIE
639-5252	PCBA,MLB,KEPLER,CRW_BEST,16G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600,FB_2G_ELPIDA
639-5253	PCBA,MLB,KEPLER,CRW_BEST,16G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600,FB_2G_HYNIX_A_DIE
639-5254	PCBA,MLB,KEPLER,CRW_BEST,16G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600,FB_2G_ELPIDA
639-5255	PCBA,MLB,KEPLER,CRW_BEST,16G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600,FB_2G_HYNIX_A_DIE
639-5256	PCBA,MLB,KEPLER,CRW_BEST,16G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600,FB_2G_ELPIDA
-> 639-5257	PCBA,MLB,KEPLER,CRW_CTO,8G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600_S,FB_2G_HYNIX_A_DIE
639-5258	PCBA,MLB,KEPLER,CRW_CTO,8G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600_S,FB_2G_ELPIDA
639-5259	PCBA,MLB,KEPLER,CRW_CTO,8G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600_S,FB_2G_HYNIX_A_DIE
639-5260	PCBA,MLB,KEPLER,CRW_CTO,8G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600_S,FB_2G_ELPIDA
639-5261	PCBA,MLB,KEPLER,CRW_CTO,8G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600_S,FB_2G_HYNIX_A_DIE
639-5262	PCBA,MLB,KEPLER,CRW_CTO,8G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600_S,FB_2G_ELPIDA
639-5263	PCBA,MLB,KEPLER,CRW_CTO,16G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600,FB_2G_HYNIX_A_DIE
639-5264	PCBA,MLB,KEPLER,CRW_CTO,16G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600,FB_2G_ELPIDA
639-5265	PCBA,MLB,KEPLER,CRW_CTO,16G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600,FB_2G_HYNIX_A_DIE
639-5266	PCBA,MLB,KEPLER,CRW_CTO,16G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600,FB_2G_ELPIDA
639-5267	PCBA,MLB,KEPLER,CRW_CTO,16G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600,FB_2G_HYNIX_A_DIE
639-5268	PCBA,MLB,KEPLER,CRW_CTO,16G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600,FB_2G_ELPIDA
-> 639-5478	PCBA,MLB,KEPLER,CRW_BEST,8G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600_S,FB_4G_HYNIX
639-5479	PCBA,MLB,KEPLER,CRW_BEST,8G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600_S,FB_4G_HYNIX
639-5480	PCBA,MLB,KEPLER,CRW_BEST,8G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600_S,FB_4G_HYNIX
639-5481	PCBA,MLB,KEPLER,CRW_BEST,16G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600,FB_4G_HYNIX
639-5482	PCBA,MLB,KEPLER,CRW_BEST,16G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600,FB_4G_HYNIX
639-5483	PCBA,MLB,KEPLER,CRW_BEST,16G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600,FB_4G_HYNIX
639-5484	PCBA,MLB,KEPLER,CRW_CTO,8G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600_S,FB_4G_HYNIX
639-5485	PCBA,MLB,KEPLER,CRW_CTO,8G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600_S,FB_4G_HYNIX
639-5486	PCBA,MLB,KEPLER,CRW_CTO,8G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600_S,FB_4G_HYNIX
639-5487	PCBA,MLB,KEPLER,CRW_CTO,16G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600,FB_4G_HYNIX
639-5488	PCBA,MLB,KEPLER,CRW_CTO,16G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600,FB_4G_HYNIX
639-5489	PCBA,MLB,KEPLER,CRW_CTO,16G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600,FB_4G_HYNIX

J45G BOM Groups

BOM GROUP	BOM OPTIONS
J45G_COMMON	ALTERNATE,COMMON,J45G_COMMON1,J45G_COMMON2,J45G_PROGPARTS,GFX_BM,ACAPS:A2
J45G_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,CPUPEG:X8X8,S2_PWR:S0
J45G_COMMON2	EDP:YES,LPCPLUS_CONN:YES,LPCPLUS_R:YES,XDP,RIO_PWR:1V5,SPI:DUAL_IO,SSD_PWR_EN:GPIO,CAM_WAKE:NO
J45G_PVT	BKLT:PROD,SENSOR_NONPROD:N
J45G_PROGPARTS	SMC_PROG:PROTO4,BOOTROM_PROG:PROTO4,TBTROM:PROG,TPAD_PSOC:PROG,GFX_PROGPARTS
GFX_PROGPARTS	DPMUXMCU:PROG
J45G_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,DDRVREF_DAC,SENSOR_NONPROD:Y,BKLT:ENG,DBGLED,CAM_XTAL:YES,DPMUX_DEBUG
J45G_DEVEL:DVT	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,DBGLED
GFX_BM	GK107:GX,DPMUX:HOCO
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4599	1	IC,CPU,CRW,PRQ,C0,2.0,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BETTER
337S4600	1	IC,CPU,CRW,PRQ,C0,2.3,47W,4+3E,6M,BGA1364	U0500	CRITICAL	CPU_CRW:BEST
337S4624	1	IC,CPU,CRW,PRQ,C0,2.6,47W,4+3E,6M,BGA1364	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,PCH,LPT-M, HM87,C2,SR199,PRQ,20x20mm,PCBGA	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC, PCBGA288	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CMRA,8X8,208PCBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GDMKA,96B FBGA	U4000	CRITICAL	
333S0667	16	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	4Gb_HYNIX_1600_S
333S0624	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	4Gb_SAMSUNG_1600_S
333S0703	16	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	4Gb_ELPIDA_1600_S
333S0660	16	IC,SDRAM,4GBIT,DDR3L-1600,V8GA,78P,FBGA		CRITICAL	4Gb_MICRON_1600_S
333S0667	32	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	4Gb_HYNIX_1600
333S0624	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	4Gb_SAMSUNG_1600
333S0703	32	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	4Gb_ELPIDA_1600
333S0660	32	IC,SDRAM,4GBIT,DDR3L-1600,V8GA,78P,FBGA		CRITICAL	4Gb_MICRON_1600
337S4256	1	IC,GPU,GK107-GT A2,BGA908	U8400	CRITICAL	GK107:GT
337S4427	1	IC,GPU,107GX,924MHZ,1.0375V,1.5V,FBGA908	U8400	CRITICAL	GK107:GX
337S4616	1	IC,GPU,CK107-762,A2,940MHz,5GBPS,1.2V,1.5V908BG	U8400	CRITICAL	GK107:GX2
333S0630	4	IC,SDRAM,GDDR5,64MX32,A-DIE,HYNIX	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_HYNIX_A_DIE
333S0631	4	IC,SDRAM,GDDR5,64MX32,D-DIE,SAMSUNG	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_SAMSUNG
333S0695	4	IC,SDRAM,GDDR5,2GBIT,5GBPS,170FBGA	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_ELPIDA
333S0701	4	IC,SDRAM,GDDR5,2GBIT,5GBPS,170FBGA,EDW2032BBBG-6A-F	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_ELPIDA_29nm
333S0734	4	IC,SDRAM,GDDR5,64MX3,HYNIX,H5GC2H24BFR-T2C	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_HYNIX_29nm
333S0685	4	IC,SDRAM,GDDR5,64MX3,HYNIX,H5GC4H24MFP-T2C	U8800,U8850,U8900,U8950	CRITICAL	FB_4G_HYNIX

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:2Gb_HYNIX_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM:2Gb_SAMSUNG_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM:2Gb_ELPIDA_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM:2Gb_MICRON_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM:4Gb_HYNIX_1600_S	4Gb_HYNIX_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:4Gb_SAMSUNG_1600_S	4Gb_SAMSUNG_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM:4Gb_ELPIDA_1600_S	4Gb_ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM:4Gb_MICRON_1600_S	4Gb_MICRON_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM:4Gb_HYNIX_1600	4Gb_HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM:4Gb_SAMSUNG_1600	4Gb_SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM:4Gb_ELPIDA_1600	4Gb_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM:4Gb_MICRON_1600	4Gb_MICRON_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H

Development/Base BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0177	1	J45G MLB,KEPLER BASE BOM	BASE	CRITICAL	BASE_BOM
985-0181	1	J45G MLB,KEPLER, DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SYNC MASTER=J15 REFERENCE SYNC DATE=07/31/2012

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Programmables - All builds

341S3920	1	IC,EEPROM,FALCON RIDGE (V13.1),J44/J45	U2890	CRITICAL	TBTROM:PROG
335S0915	1	EEPROM,SPI FLASH ROM,4MBit,50MHZ,USON8	U2890	CRITICAL	TBTROM:BLANK
335S0852	1	IC,GPUROM,D2,BLANK	U9101	CRITICAL	GPUROM:BLANK
341S3565	1	IC,EDP MUX-95C,(RENESAS) V3.2.8,DVB,D2	U9600	CRITICAL	DPMUXMCU:PROG
337S4313	1	IC,MCU,H8S/2113,9X9MM,TLP-145V	U9600	CRITICAL	DPMUXMCU:BLANK
341S3856	1	IC,TRKPD/KYBD CNTRLR,CU only,V225,J45	U4801	CRITICAL	TPAD_PSOC:PROG
337S4587	1	IC,TP PSOC,QFN,BLANK	U4801	CRITICAL	TPAD_PSOC:BLANK

SMC

338S1214	1	IC,SMC-A3,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BASE
341S3901	1	IC,SMC-B1,SCPL,EXT,V2.16Q13,PROTO4,J45G	U5000	CRITICAL	SMC_PROG:PROTO4
341S3741	1	IC,SMC-A3,SCPL,EXT,VXXXX,PVT,J15	U5000	CRITICAL	SMC_PROG:PVT

EFI ROM

335S0807	1	IC,SPI SRL 50MHZ FLASH,64MBIT,8SOP,FUSE,L	U6100	CRITICAL	BOOTROM_PROG:BLANK
335S0812	1	64MBIT SPI SRL DUAL I/O FLSH,SOIC8,Z	U6100	CRITICAL	BOOTROM_PROG:BLANK2
341S3712	1	IC,EFI ROM(V0008)PROTO 0,J15	U6100	CRITICAL	BOOTROM_PROG:PROTO
341S3742	1	IC,EFI ROM(V0013) PROTO 1,J15	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3890	1	IC,EFI ROM(V0100) PROTO 3-J45 & EVT-J45	U6100	CRITICAL	BOOTROM_PROG:PROTO3
341S3904	1	IC,EFI ROM(V0106) PROTO 4,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO4

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
376S1053	376S0604		ALL	Diodes alt to Fairchild	
128S0311	128S0329		ALL	NMC alt to Sanyo	
138S0739	138S0706		ALL	Samsung alt to Murata	
197S0481	197S0480		ALL	EPSON Alt to NDK	
371S0713	371S0558		ALL	ODM alt to PT	
152S0461	152S1645		ALL	Cystec alt to Vishay	
376S1080	376S0820		ALL	Diodes alt to On Semi	
155S0667	155S0583		ALL	Panasonic alt to TDK	
376S1032	376S0855		ALL	Toshiba alt to Diodes	
376S1129	376S0855		ALL	NXP alt to Diodes	
376S1089	376S1128		ALL	NXP alt to Diodes	
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung	
128S0371	128S0376		ALL	Kemet alt to Sanyo	
333S0629	333S0703		ALL	Spida Alt die	
138S0803	138S0639		ALL	Samsung Alt to Murata	
138S0843	138S0674		ALL	Samsung Alt to Murata	
138S0846	138S0811		ALL	Samsung Alt to Murata	
127S0164	127S0162		ALL	Rcmb Alt to Vishay	
138S0732	138S0715		ALL	Rcmb Alt to Vishay	
128S0364	128S0264		ALL	Kemet alt to Sanyo	
333S0704	333S0700		ALL	ELPIDA to HYNIX D6400	
353S3527	353S3528		ALL	Pericom eDP MUX	FROM J15
353S3526	353S3528		ALL	TI eDP MUX	FROM J15
197S0466	197S0464		ALL	Epson alt to NDK	FROM J15
311S0649	311S0541		ALL	ON alt to Toshiba (U2930,U7000)	
197S0479	197S0478		ALL	Epson alt to NDK	

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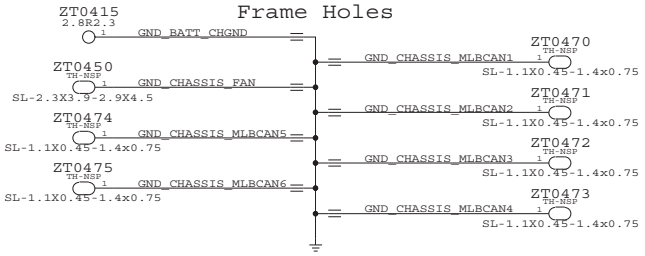
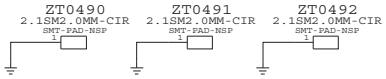
Frame Holes



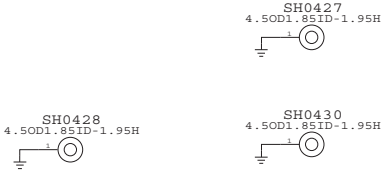
SMT GND TEST PONTS



APN 806-2247
BR0401
MLB-MTG-BRKT-J5

J45 THERMAL MODULE STANDOFF

GPU BOSS APN 860-4772



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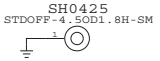

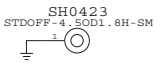

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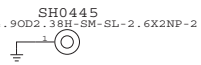
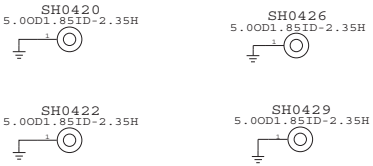
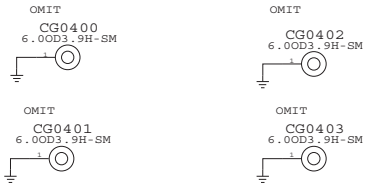
APN 817-0741



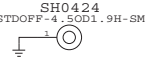
CPU BOSS APN 860-2931



Thermal Module gaskets APN 875-9290



APN 860-1328



APN 817-4517

PD parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	

APN 806-9391

SHLD-MLB-USB-J45

APN 806-6192

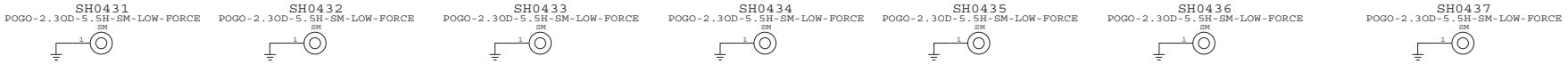
SHLD-J45-CAN-FENCE1-MDP

APN 806-6194

SHLD-J45-CAN-FENCE2-MDP

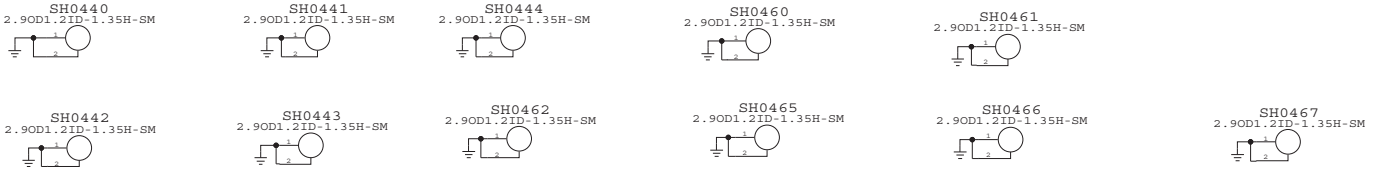
J45 POGO PINS

APN 870-2451



J45 STANDOFF

APN 860-1448



SYNC MASTER=CLEAN J45 SYNC DATE=05/03/2013

PAGE TITLE: PD Parts

Apple Inc.

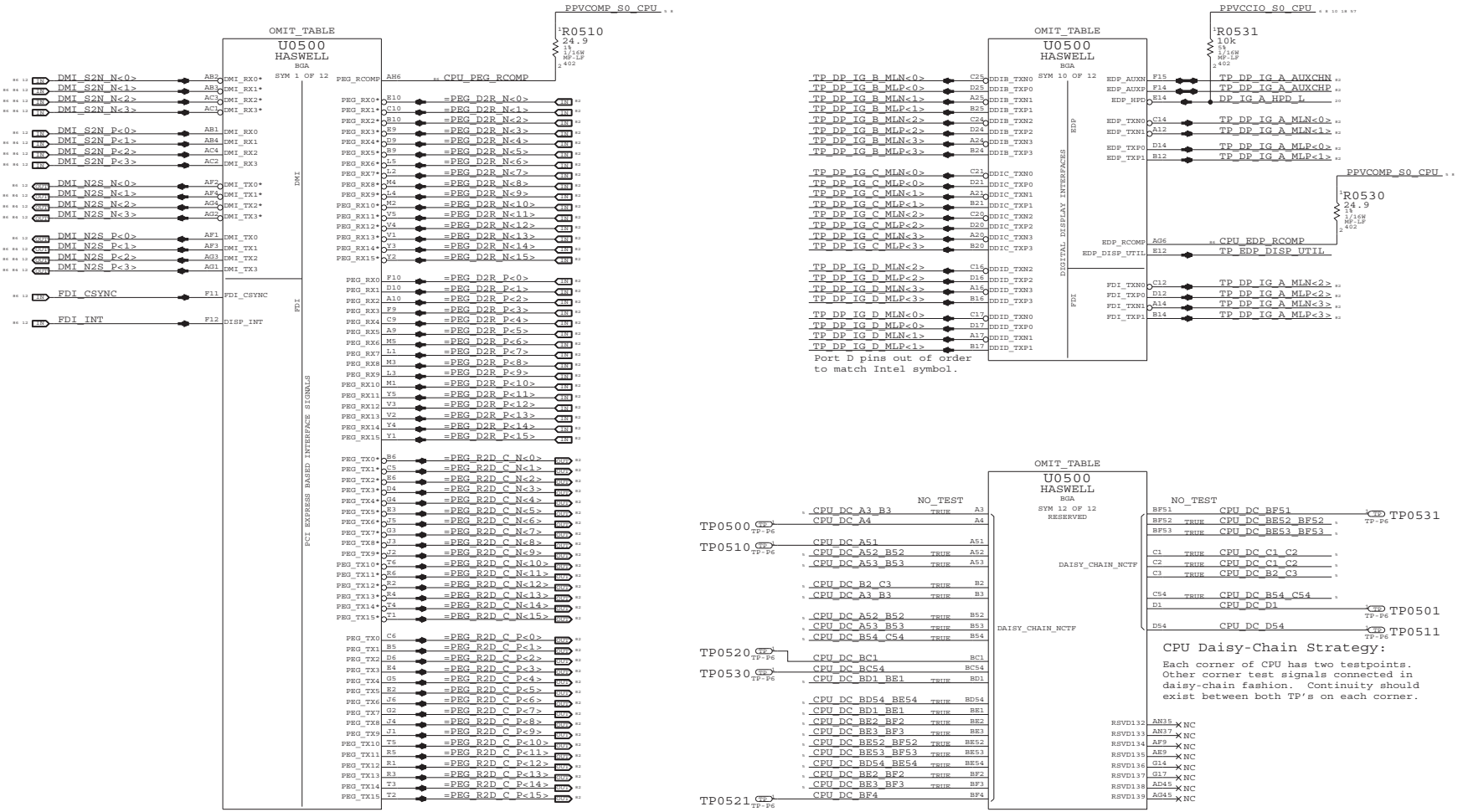
DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

PAGE: 4 OF 119

SHEET: 4 OF 94



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE

CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D

REVISION 6.0.0

BRANCH dvt

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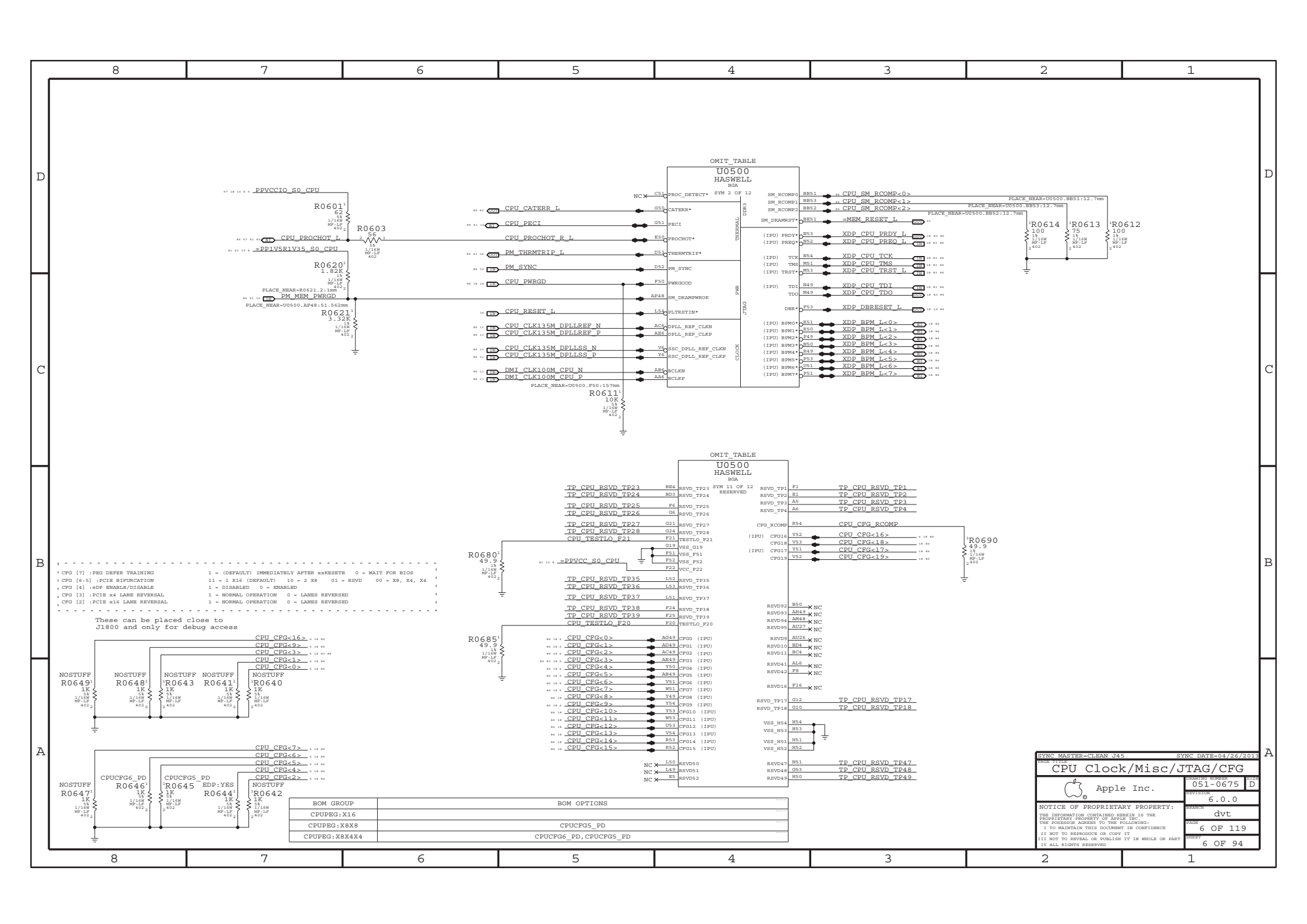
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U0500
HASWELL
BGA
SYM 2 OF 12
PROC_DETECT*
CATERR*
PECI
PROCHOT*
THERMTRIP*
PM_SYNC
PWRGOOD
SM_DRAMPWROK
PLTRSTIN*
DPLL_REF_CLKN
DPLL_REF_CLKP
SSC_DPLL_REF_CLKN
SSC_DPLL_REF_CLKP
BCLKN
BCLKP
THERMAL
DDR3
PWR
JTAG
CLOCK
PPVCCIO_S0_CPU
R0601 62
R0603 56
R0620 1.82K
R0621 3.32K
CPU_PROCHOT_L
=PP1V5R1V35_S0_CPU
PM_MEM_PWRGD
CPU_CATERR_L
CPU_PECI
CPU_PROCHOT_R_L
PM_THRMTRIP_L
PM_SYNC
CPU_PWRGD
CPU_RESET_L
CPU_CLK135M_DPLLREF_N
CPU_CLK135M_DPLLREF_P
CPU_CLK135M_DPLLSS_N
CPU_CLK135M_DPLLSS_P
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
R0611 10K
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
SM_DRAMRST*
(IPU) PRDY*
(IPU) PREQ*
(IPD) TCK
(IPU) TMS
(IPU) TRST*
(IPU) TDI
TDO
DBR*
(IPU) BPM0*
(IPU) BPM1*
(IPU) BPM2*
(IPU) BPM3*
(IPU) BPM4*
(IPU) BPM5*
(IPU) BPM6*
(IPU) BPM7*
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CPU_SM_RCOMP<2>
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XDP_CPU_TRST_L
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XDP_BPM_L<7>
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PLACE_NEAR=U0500.BB52:12.7mm
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R0613 75
R0612 100
OMIT_TABLE
U0500
HASWELL
BGA
SYM 11 OF 12
RESERVED
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TP_CPU_RSVD_TP24
TP_CPU_RSVD_TP25
TP_CPU_RSVD_TP26
TP_CPU_RSVD_TP27
TP_CPU_RSVD_TP28
CPU_TESTLO_F21
TP_CPU_RSVD_TP35
TP_CPU_RSVD_TP36
TP_CPU_RSVD_TP37
TP_CPU_RSVD_TP38
TP_CPU_RSVD_TP39
CPU_TESTLO_F20
TP_CPU_RSVD_TP1
TP_CPU_RSVD_TP2
TP_CPU_RSVD_TP3
TP_CPU_RSVD_TP4
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CPU_CFG<17>
CPU_CFG<19>
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R0680 49.9
=PPVCC_S0_CPU
R0685 49.9
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CPU_CFG<10>
CPU_CFG<11>
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>
TP_CPU_RSVD_TP17
TP_CPU_RSVD_TP18
TP_CPU_RSVD_TP47
TP_CPU_RSVD_TP48
TP_CPU_RSVD_TP49
CFG [7] :PEG DEFER TRAINING 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
These can be placed close to J1800 and only for debug access
NOSTUFF R0649 1K
R0648 1K
R0643 1K
NOSTUFF R0641 1K
R0640 1K
CPUCFG6_PD R0646 1K
CPUCFG5_PD R0645 1K
EDP:YES R0644 1K
NOSTUFF R0642 1K
NOSTUFF R0647 1K
BOM GROUP
BOM OPTIONS
CPUPEG:X16
CPUCFG5_PD
CPUPEG:X8X8
CPUPEG:X8X4X4
CPUCFG6_PD,CPUCFG5_PD
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
PAGE TITLE
CPU Clock/Misc/JTAG/CFG
Apple Inc.
DRAWING NUMBER 051-0675
SIZE D
REVISION 6.0.0
BRANCH dvt
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SHEET 6 OF 94
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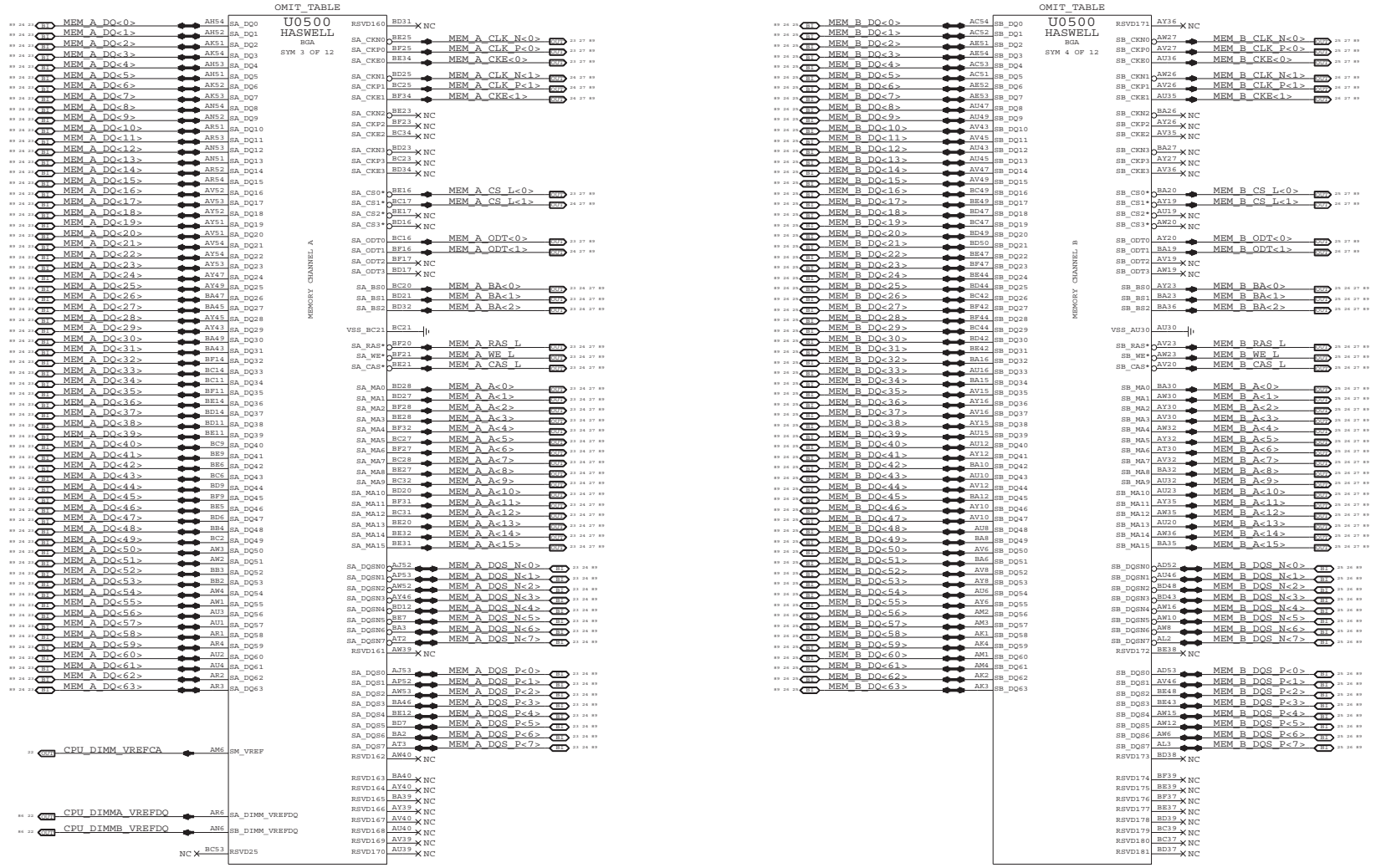
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BGA
SYM 3 OF 12
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SYM 4 OF 12
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SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
PAGE TITLE
CPU DDR3 Interfaces
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
PAGE
7 OF 119
SHEET
7 OF 94
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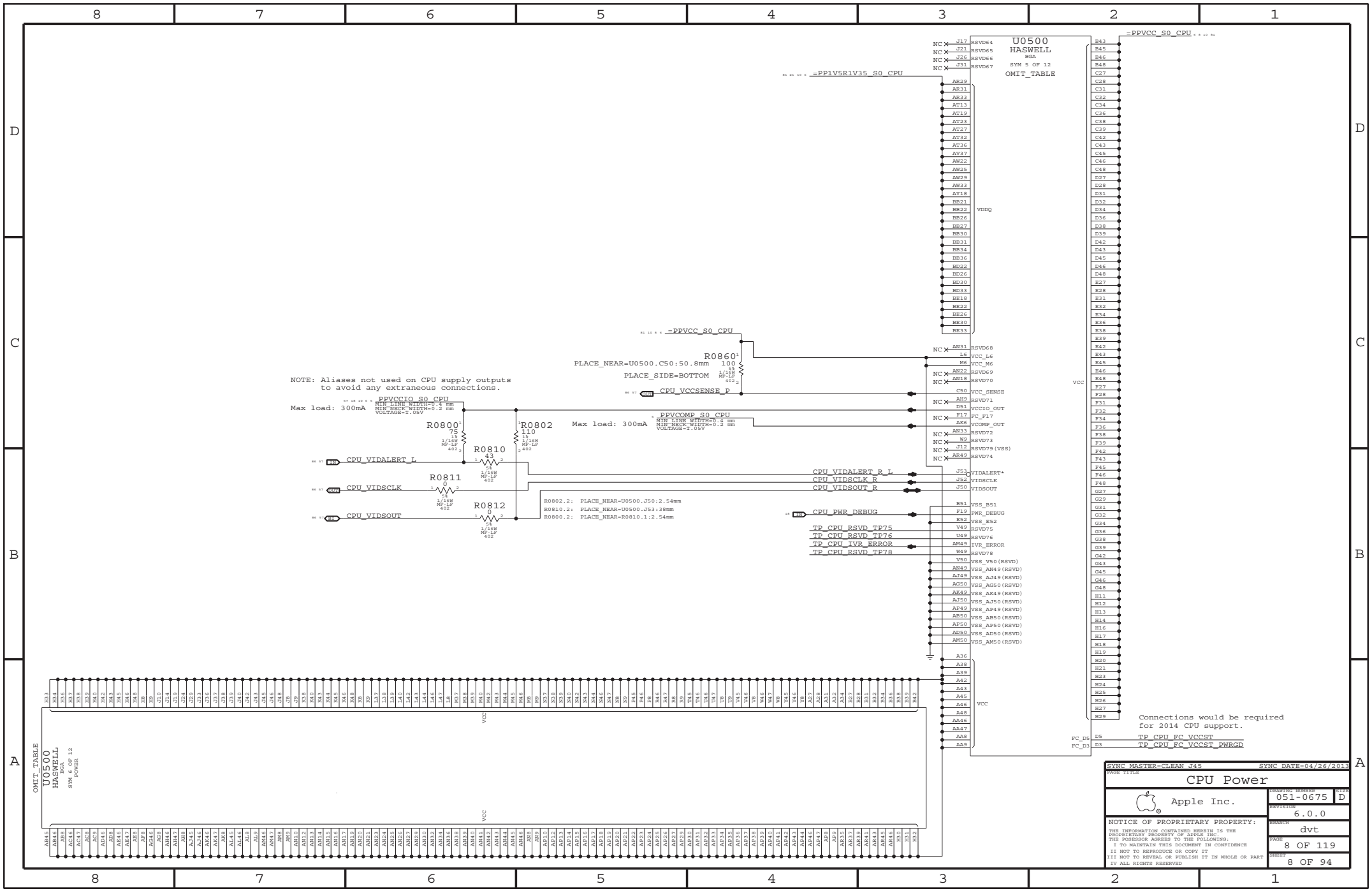
U0500
HASWELL
BGA
SYM 5 OF 12
OMIT_TABLE
=PP1V5R1V35_S0_CPU
=PPVCC_S0_CPU
VDDQ
VCC
R0860
PLACE_NEAR=U0500.C50:50.8mm
PLACE_SIDE=BOTTOM
100
CPU_VCCSENSE_P
VCC_SENSE
NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.
PPVCCIO_S0_CPU
Max load: 300mA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
R0800
75
R0802
110
R0810
43
R0811
0
R0812
0
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
PPVCOMP_S0_CPU
Max load: 300mA
VCCIO_OUT
VCOMP_OUT
R0802.2: PLACE_NEAR=U0500.J50:2.54mm
R0810.2: PLACE_NEAR=U0500.J53:38mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_PWR_DEBUG
TP_CPU_RSVD_TP75
TP_CPU_RSVD_TP76
TP_CPU_IVR_ERROR
TP_CPU_RSVD_TP78
TP_CPU_FC_VCCST
TP_CPU_FC_VCCST_PWRGD
Connections would be required
for 2014 CPU support.
OMIT_TABLE
U0500
HASWELL
BGA
SYM 6 OF 12
POWER
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
PAGE TITLE
CPU Power
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
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dvt
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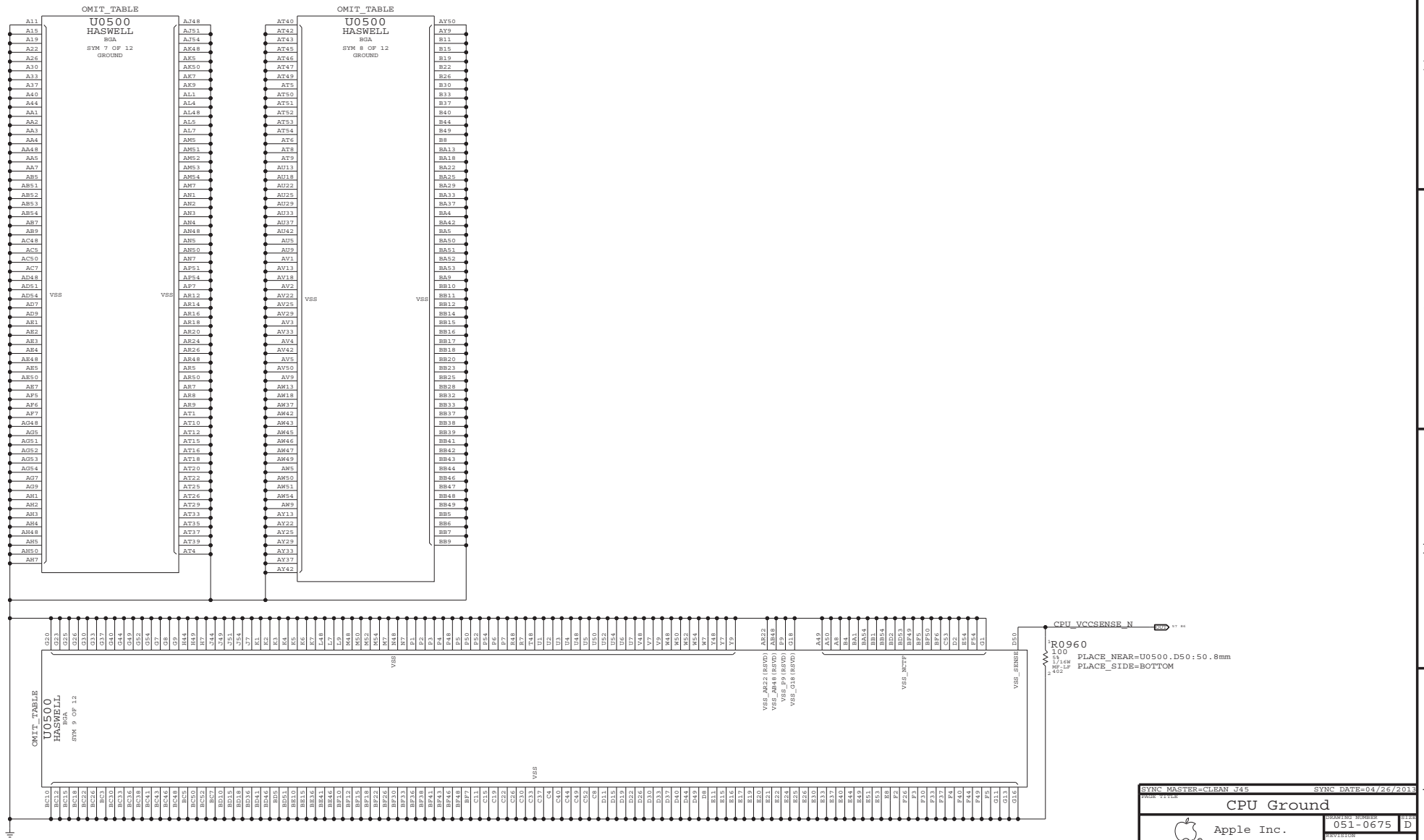

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE

CPU Ground

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D

REVISION 6.0.0

BRANCH dvt

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CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 9x 210uF 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

=PPVCC_S0_CPU

PLACEMENT_NOTE (C1000-C1019):
Place on bottom side of U0500

C1000 1UF 10% 10V X6S-CERM 0402
C1001 1UF 10% 10V X6S-CERM 0402
C1002 1UF 10% 10V X6S-CERM 0402
C1003 1UF 10% 10V X6S-CERM 0402
C1004 1UF 10% 10V X6S-CERM 0402
C1005 1UF 10% 10V X6S-CERM 0402
C1006 1UF 10% 10V X6S-CERM 0402
C1007 1UF 10% 10V X6S-CERM 0402
C1008 1UF 10% 10V X6S-CERM 0402
C1009 1UF 10% 10V X6S-CERM 0402
C1010 1UF 10% 10V X6S-CERM 0402
C1011 1UF 10% 10V X6S-CERM 0402
C1012 1UF 10% 10V X6S-CERM 0402
C1013 1UF 10% 10V X6S-CERM 0402
C1014 1UF 10% 10V X6S-CERM 0402
C1015 1UF 10% 10V X6S-CERM 0402
C1016 1UF 10% 10V X6S-CERM 0402
C1017 1UF 10% 10V X6S-CERM 0402
C1018 1UF 10% 10V X6S-CERM 0402
C1019 1UF 10% 10V X6S-CERM 0402

NO STUFF NO STUFF NO STUFF

PLACEMENT_NOTE (C1020-C1023):
Place near U0500 on bottom side

C1020 20UF 20% 4V XSR-CERM 0402-2
C1021 20UF 20% 4V XSR-CERM 0402-2
C1022 20UF 20% 4V XSR-CERM 0402-2
C1023 20UF 20% 4V XSR-CERM 0402-2

NO STUFF NO STUFF NO STUFF

ACAPS:A2
CAPS for Acoustic Control (C109A to C102D)
ACAPS:A2

NO STUFF
CRITICAL C109A 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C109B 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C109C 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C109D 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A1
CRITICAL C109E 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A1
CRITICAL C109F 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A1
CRITICAL C101A 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A1
CRITICAL C101B 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A1
CRITICAL C101C 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C101D 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A1
CRITICAL C101E 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C101F 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C102A 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C102B 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C102C 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C102D 20UF 20% 4V XSR-CERM 0402-2

ACAPS:A2

NO STUFF NO STUFF NO STUFF

PLACEMENT_NOTE (C1024-C1045):
Place near inductors on bottom side.

NO STUFF
CRITICAL C1024 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1025 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1026 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1027 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1028 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1029 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1030 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1031 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1032 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1033 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1034 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1035 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1036 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1037 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1038 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1039 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1040 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1041 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1042 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1043 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1044 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1045 20UF 20% 4V XSR-CERM 0402-2

ACAPS:A2

PLACEMENT_NOTE (C1046-C1067):
Place near inductors on bottom side.

ACAPS:A1
CRITICAL C1046 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1047 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1048 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A2
CRITICAL C1049 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1050 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A1
CRITICAL C1051 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A1
CRITICAL C1052 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A2
CRITICAL C1053 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A2
CRITICAL C1054 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A1
CRITICAL C1055 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A2
CRITICAL C1056 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C1057 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1058 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A2
CRITICAL C1059 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A2
CRITICAL C1060 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1061 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1062 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1063 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A1
CRITICAL C1064 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1065 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A1
CRITICAL C1066 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C1067 20UF 20% 4V XSR-CERM 0402-2

NO STUFF NO STUFF NO STUFF

PLACEMENT_NOTE (C1068-C1076):
Place near inductors on bottom side.

CRITICAL C1068 210UF 20% 2V POLY-TANT CASE-B2S
CRITICAL C1069 210UF 20% 2V POLY-TANT CASE-B2S
CRITICAL C1070 210UF 20% 2V POLY-TANT CASE-B2S
CRITICAL C1071 210UF 20% 2V POLY-TANT CASE-B2S
CRITICAL C1072 210UF 20% 2V POLY-TANT CASE-B2S
CRITICAL C1073 210UF 20% 2V POLY-TANT CASE-B2S
CRITICAL C1074 210UF 20% 2V POLY-TANT CASE-B2S
CRITICAL C1075 210UF 20% 2V POLY-TANT CASE-B2S
NO STUFF
CRITICAL C1076 210UF 20% 2V POLY-TANT CASE-B2S
NO STUFF
CRITICAL C1077 330UF-9MOHM 20% 2V POLY-TANT D15T-1

CAPS for Acoustic Control (C102E to C103F)
ACAPS:A2
NO STUFF
CRITICAL C102E 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C102F 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C103A 20UF 20% 4V XSR-CERM 0402-2
NO STUFF
CRITICAL C103B 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C103C 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C103D 20UF 20% 4V XSR-CERM 0402-2
ACAPS:A2
CRITICAL C103E 20UF 20% 4V XSR-CERM 0402-2
CRITICAL C103F 20UF 20% 4V XSR-CERM 0402-2

CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402

=PP1V5R1V35_S0_CPU

PLACEMENT_NOTE (C1080-C1089):
Place on bottom side of U0500

C1080 1UF 10% 10V X6S-CERM 0402
C1081 1UF 10% 10V X6S-CERM 0402
C1082 1UF 10% 10V X6S-CERM 0402
C1083 1UF 10% 10V X6S-CERM 0402
C1084 1UF 10% 10V X6S-CERM 0402
C1085 1UF 10% 10V X6S-CERM 0402
C1086 1UF 10% 10V X6S-CERM 0402
C1087 1UF 10% 10V X6S-CERM 0402
C1088 1UF 10% 10V X6S-CERM 0402
C1089 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1090-C1097):
Place near U0500 on bottom side

C1090 10UF 20% 4V X6S-CERM 0603
C1091 10UF 20% 4V X6S-CERM 0603
C1092 10UF 20% 4V X6S-CERM 0603
C1093 10UF 20% 4V X6S-CERM 0603
C1094 10UF 20% 4V X6S-CERM 0603
C1095 10UF 20% 4V X6S-CERM 0603
C1096 10UF 20% 4V X6S-CERM 0603
C1097 10UF 20% 4V X6S-CERM 0603

PLACEMENT_NOTE (C1098-C1099):

CRITICAL C1098 330UF-6MOHM 20% 2.0V POLY-TANT D15T-ECQLT-COMBO
CRITICAL C1099 330UF-6MOHM 20% 2.0V POLY-TANT D15T-ECQLT-COMBO

(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

CPU VCCIO Decoupling

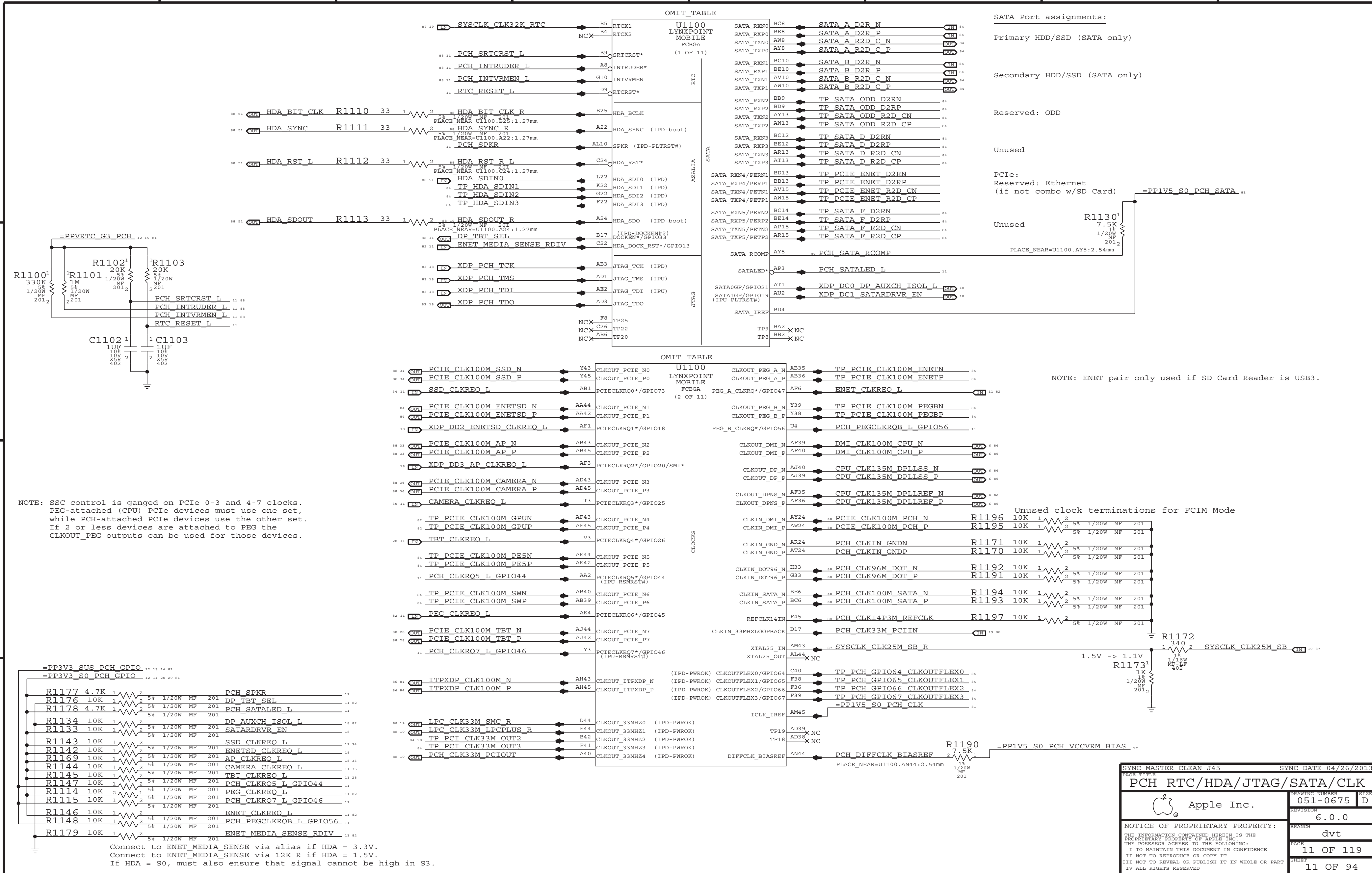
Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

PPVCCIO_S0_CPU

C1079 0.01UF 10% 16V X7R-CERM 0402

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

SYNC MASTER=CLEAN J15 SYNC DATE=05/02/2013
PAGE TITLE: CPU Decoupling
Apple Inc.
DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
PAGE: 10 OF 119
SHEET: 10 OF 94



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

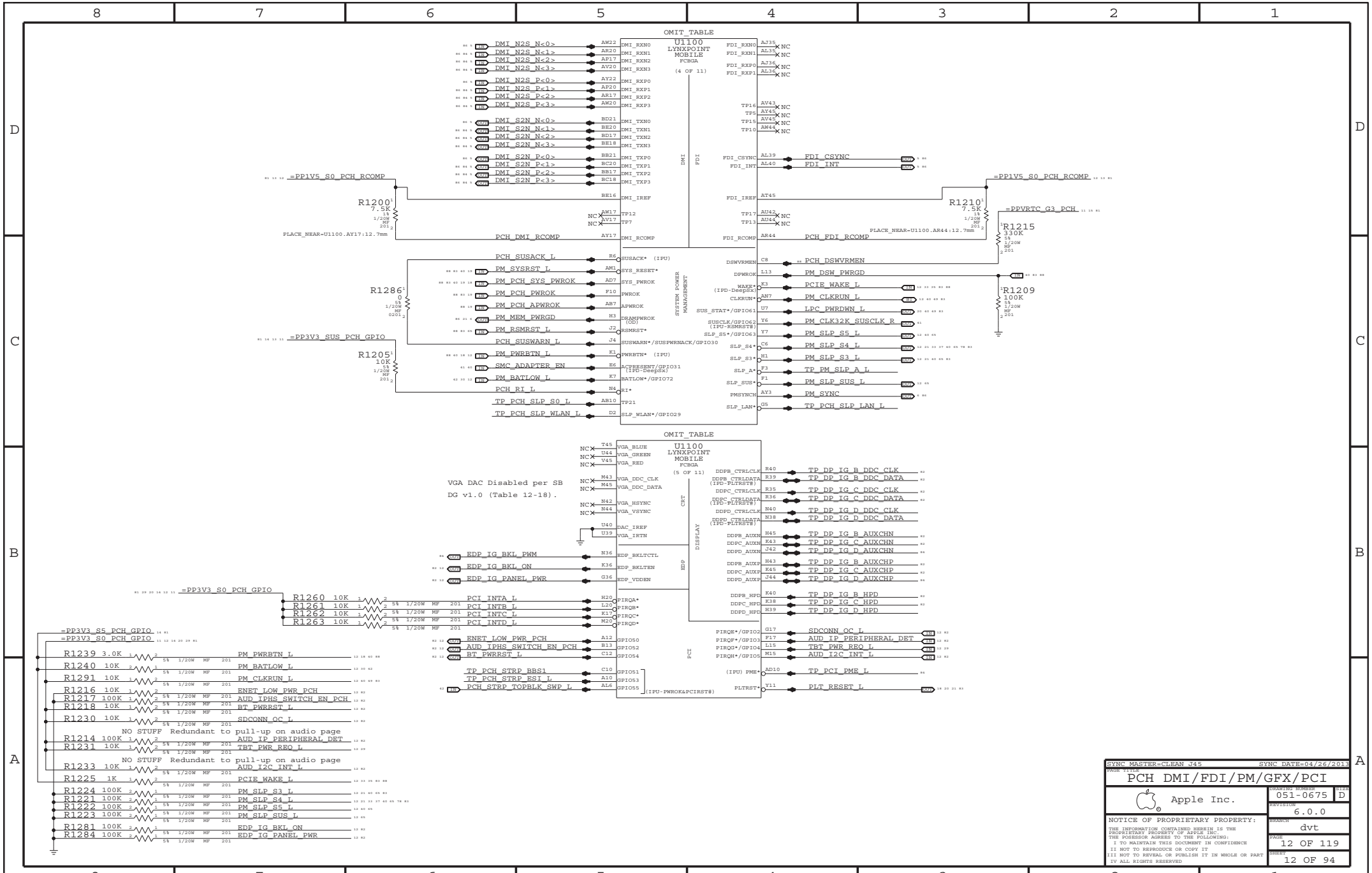
PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D

REVISION 6.0.0

BRANCH dvt


OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(4 OF 11)
DMI_N2S_N<0>
DMI_N2S_N<1>
DMI_N2S_N<2>
DMI_N2S_N<3>
DMI_N2S_P<0>
DMI_N2S_P<1>
DMI_N2S_P<2>
DMI_N2S_P<3>
DMI_S2N_N<0>
DMI_S2N_N<1>
DMI_S2N_N<2>
DMI_S2N_N<3>
DMI_S2N_P<0>
DMI_S2N_P<1>
DMI_S2N_P<2>
DMI_S2N_P<3>
=PP1V5_S0_PCH_RCOMP
R1200 7.5K
PLACE_NEAR=U1100.AY17:12.7mm
PCH_DMI_RCOMP
FDI_CSYNC
FDI_INT
FDI_RCOMP
PCH_FDI_RCOMP
PLACE_NEAR=U1100.AR44:12.7mm
R1210 7.5K
=PP1V5_S0_PCH_RCOMP
=PPVRTC_G3_PCH
R1215 330K
R1209 100K
PCH_SUSACK_L
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PM_PCH_APWROK
PM_MEM_PWRGD
PM_RSMRST_L
PCH_SUSWARN_L
PM_PWRBTN_L
SMC_ADAPTER_EN
PM_BATLOW_L
PCH_RI_L
TP_PCH_SLP_S0_L
TP_PCH_SLP_WLAN_L
R1286 0
=PP3V3_SUS_PCH_GPIO
R1205 10K
PCH_DSWVRMEN
PM_DSW_PWRGD
PCIE_WAKE_L
PM_CLKRUN_L
LPC_PWRDWN_L
PM_CLK32K_SUSCLK_R
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PM_SLP_A_L
PM_SLP_SUS_L
PM_SYNC
TP_PCH_SLP_LAN_L
SYSTEM POWER MANAGEMENT
DMI
FDI
OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(5 OF 11)
VGA DAC Disabled per SB
DG v1.0 (Table 12-18).
VGA_BLUE
VGA_GREEN
VGA_RED
VGA_DDC_CLK
VGA_DDC_DATA
VGA_HSYNC
VGA_VSYNC
DAC_IREF
VGA_IRTN
CRT
DISPLAY
EDP_IG_BKL_PWM
EDP_IG_BKL_ON
EDP_IG_PANEL_PWR
EDP
=PP3V3_S0_PCH_GPIO
R1260 10K
R1261 10K
R1262 10K
R1263 10K
PCI_INTA_L
PCI_INTB_L
PCI_INTC_L
PCI_INTD_L
ENET_LOW_PWR_PCH
AUD_IPHS_SWITCH_EN_PCH
BT_PWRRST_L
TP_PCH_STRP_BBS1
TP_PCH_STRP_ESI_L
PCH_STRP_TOPBLK_SWP_L
(IPU-PWROK&PCIRST#)
PCI
DDPB_CTRLCLK
DDPB_CTRLDATA
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPD_CTRLCLK
DDPD_CTRLDATA
TP_DP_IG_B_DDC_CLK
TP_DP_IG_B_DDC_DATA
TP_DP_IG_C_DDC_CLK
TP_DP_IG_C_DDC_DATA
TP_DP_IG_D_DDC_CLK
TP_DP_IG_D_DDC_DATA
TP_DP_IG_B_AUXCHN
TP_DP_IG_C_AUXCHN
TP_DP_IG_D_AUXCHN
TP_DP_IG_B_AUXCHP
TP_DP_IG_C_AUXCHP
TP_DP_IG_D_AUXCHP
TP_DP_IG_B_HPD
TP_DP_IG_C_HPD
TP_DP_IG_D_HPD
SDCONN_OC_L
AUD_IP_PERIPHERAL_DET
TBT_PWR_REQ_L
AUD_I2C_INT_L
TP_PCI_PME_L
PLT_RESET_L
=PP3V3_S5_PCH_GPIO
=PP3V3_S0_PCH_GPIO
R1239 3.0K PM_PWRBTN_L
R1240 10K PM_BATLOW_L
R1291 10K PM_CLKRUN_L
R1216 10K ENET_LOW_PWR_PCH
R1217 100K AUD_IPHS_SWITCH_EN_PCH
R1218 10K BT_PWRRST_L
R1230 10K SDCONN_OC_L
NO STUFF Redundant to pull-up on audio page
R1214 100K AUD_IP_PERIPHERAL_DET
R1231 10K TBT_PWR_REQ_L
NO STUFF Redundant to pull-up on audio page
R1233 10K AUD_I2C_INT_L
R1225 1K PCIE_WAKE_L
R1224 100K PM_SLP_S3_L
R1221 100K PM_SLP_S4_L
R1222 100K PM_SLP_S5_L
R1223 100K PM_SLP_SUS_L
R1281 100K EDP_IG_BKL_ON
R1284 100K EDP_IG_PANEL_PWR
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
PAGE TITLE
PCH DMI/FDI/PM/GFX/PCI
Apple Inc.
DRAWING NUMBER 051-0675
SIZE D
REVISION 6.0.0
BRANCH dvt
PAGE 12 OF 119
SHEET 12 OF 94
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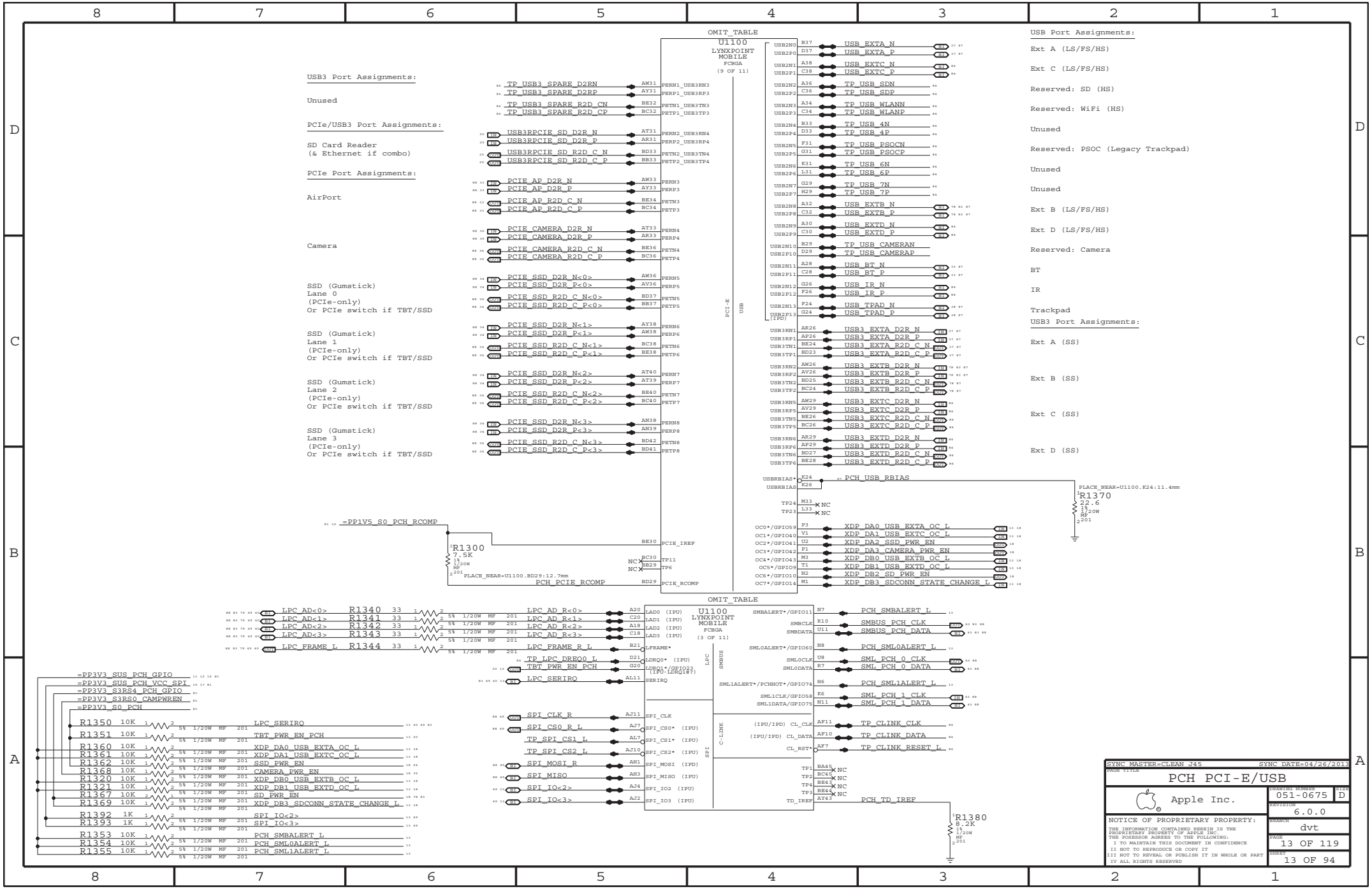
USB3 Port Assignments:
Unused
PCIe/USB3 Port Assignments:
SD Card Reader
(& Ethernet if combo)
PCIe Port Assignments:
AirPort
Camera
SSD (Gumstick)
Lane 0
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 1
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 2
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 3
(PCIe-only)
Or PCIe switch if TBT/SSD
OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(9 OF 11)
PCI-E
USB
USB Port Assignments:
Ext A (LS/FS/HS)
Ext C (LS/FS/HS)
Reserved: SD (HS)
Reserved: WiFi (HS)
Unused
Reserved: PSOC (Legacy Trackpad)
Unused
Unused
Ext B (LS/FS/HS)
Ext D (LS/FS/HS)
Reserved: Camera
BT
IR
Trackpad
USB3 Port Assignments:
Ext A (SS)
Ext B (SS)
Ext C (SS)
Ext D (SS)
PCH_USB_RBIAS
PLACE_NEAR=U1100.K24:11.4mm
R1370
22.6
=PP1V5_S0_PCH_RCOMP
R1300
7.5K
PLACE_NEAR=U1100.BD29:12.7mm
PCH_PCIE_RCOMP
OMIT_TABLE
LPC
SMBUS
C-LINK
SPI
R1340
R1341
R1342
R1343
R1344
LPC_FRAME_L
TP_LPC_DREQ0_L
TBT_PWR_EN_PCH
LPC_SERIRQ
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
TP_SPI_CS2_L
SPI_MOSI_R
SPI_MISO
SPI_IO<2>
SPI_IO<3>
PCH_SMBALERT_L
PCH_SML0ALERT_L
PCH_SML1ALERT_L
TP_CLINK_CLK
TP_CLINK_DATA
TP_CLINK_RESET_L
PCH_TD_IREF
R1380
8.2K
=PP3V3_SUS_PCH_GPIO
=PP3V3_SUS_PCH_VCC_SPI
=PP3V3_S3RS4_PCH_GPIO
=PP3V3_S3RS0_CAMPWREN
=PP3V3_S0_PCH
R1350
R1351
R1360
R1361
R1362
R1368
R1320
R1321
R1367
R1369
R1392
R1393
R1353
R1354
R1355
XDP_DA0_USB_EXTA_OC_L
XDP_DA1_USB_EXTC_OC_L
SSD_PWR_EN
CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L
XDP_DB1_USB_EXTD_OC_L
SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
PAGE TITLE
PCH PCI-E/USB
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
PAGE
13 OF 119
SHEET
13 OF 94
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Pull-up/down on chipset support page (depends on TBT controller)
Redwood Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

OMIT_TABLE

U1100
LYNXPOINT
MOBILE
FCBGA
(6 OF 11)

=PP3V3_S0_PCH_GPIO

RAMCFG0:H R1475[1] 10K 5% 1/20W MF 201 2
RAMCFG1:H R1474[1] 10K 5% 1/20W MF 201 2
RAMCFG2:H R1473[1] 10K 5% 1/20W MF 201 2
RAMCFG3:H R1472[1] 10K 5% 1/20W MF 201 2

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

=PP3V3_S5_PCH_GPIO
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO

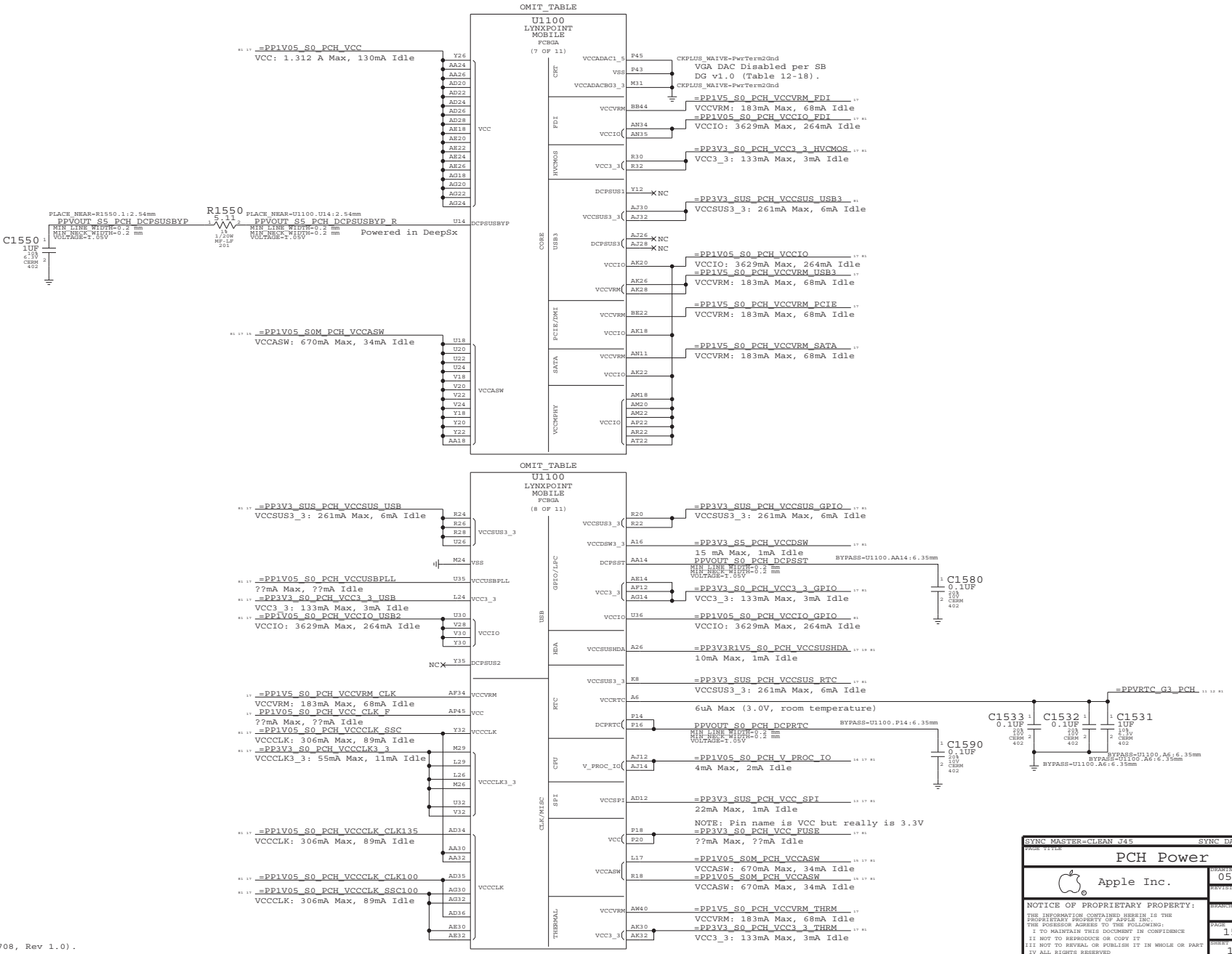
NOTE: GPIO0 pull-up/down on project-specific page

R1485	10K	5%	1/20W	MF	201		FW_PME_L
R1411	20K	5%	1/20W	MF	201		DPMUX_UC_IRQ
R1496	10K	5%	1/20W	MF	201		SMC_RUNTIME_SCI_L
R1494	10K	5%	1/20W	MF	201		WOL_EN
R1489	10K	5%	1/20W	MF	201		MEM_VDD_SEL_1V5_L
R1495	100K	5%	1/20W	MF	201		XDP_DD0_SSD_PCIE_SEL_L
R1490	100K	5%	1/20W	MF	201		LPCPLUS_GPIO
R1412	10K	5%	1/20W	MF	201		JTAG_TBT_TMS_PCH
R1492	10K	5%	1/20W	MF	201		TBT_GO2SX_BIDIR
R1491	10K	5%	1/20W	MF	201		SMC_WAKE_SCI_L
R1498	10K	5%	1/20W	MF	201		ODD_PWR_EN_L
R1413	10K	5%	1/20W	MF	201		JTAG_ISP_TCK
R1486	10K	5%	1/20W	MF	201		JTAG_ISP_TDO
R1499	10K	5%	1/20W	MF	201		JTAG_ISP_TDI
R1484	10K	5%	1/20W	MF	201		FW_PWR_EN_PCH
R1493	100K	5%	1/20W	MF	201		SPIROM_USE_MLB

NOTE: GPIO70 pull-up/down on project-specific page

R1450	10K	5%	1/20W	MF	201		PCH_A20GATE
R1455	10K	5%	1/20W	MF	201		PCH_RCIN_L

SYNC MASTER=CLEAN J45	SYNC DATE=04/26/2013
PAGE TITLE	PCH GPIO/MISC/NCTF
Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
	REVISION 6.0.0
	BRANCH dvt
	PAGE 14 OF 119
	SHEET 14 OF 94


OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(7 OF 11)
=PP1V05_S0_PCH_VCC
VCC: 1.312 A Max, 130mA Idle
VCC
VCCASW
=PP1V05_S0M_PCH_VCCASW
VCCASW: 670mA Max, 34mA Idle
R1550
5.11
1/20W
MF-LF
201
PLACE_NEAR=R1550.1:2.54mm
PPVOUT_S5_PCH_DCPSUSBYP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
PLACE_NEAR=U1100.U14:2.54mm
PPVOUT_S5_PCH_DCPSUSBYP_R
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
Powered in DeepSx
C1550
1UF
6.3V
CERM
402
DCPSUSBYP
CORE
VCCADAC1_5
VSS
VCCADACBG3_3
CRT
CKPLUS_WAIVE=PwrTerm2Gnd
VGA DAC Disabled per SB
DG v1.0 (Table 12-18).
VCCVRM
VCCIO
FDI
=PP1V5_S0_PCH_VCCVRM_FDI
VCCVRM: 183mA Max, 68mA Idle
=PP1V05_S0_PCH_VCCIO_FDI
VCCIO: 3629mA Max, 264mA Idle
VCC3_3
HVCMOS
=PP3V3_S0_PCH_VCC3_3_HVCMOS
VCC3_3: 133mA Max, 3mA Idle
DCPSUS1
NC
VCCSUS3_3
USB3
=PP3V3_SUS_PCH_VCCSUS_USB3
VCCSUS3_3: 261mA Max, 6mA Idle
DCPSUS3
=PP1V05_S0_PCH_VCCIO
VCCIO: 3629mA Max, 264mA Idle
=PP1V5_S0_PCH_VCCVRM_USB3
VCCVRM: 183mA Max, 68mA Idle
=PP1V5_S0_PCH_VCCVRM_PCIE
VCCVRM: 183mA Max, 68mA Idle
PCIE/DMI
SATA
=PP1V5_S0_PCH_VCCVRM_SATA
VCCVRM: 183mA Max, 68mA Idle
VCCMPHY
OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(8 OF 11)
=PP3V3_SUS_PCH_VCCSUS_USB
VCCSUS3_3: 261mA Max, 6mA Idle
=PP1V05_S0_PCH_VCCUSBPLL
??mA Max, ??mA Idle
=PP3V3_S0_PCH_VCC3_3_USB
VCC3_3: 133mA Max, 3mA Idle
=PP1V05_S0_PCH_VCCIO_USB2
VCCIO: 3629mA Max, 264mA Idle
VCCUSBPLL
VCC3_3
VCCIO
VSS
DCPSUS2
=PP1V5_S0_PCH_VCCVRM_CLK
VCCVRM: 183mA Max, 68mA Idle
=PP1V05_S0_PCH_VCC_CLK_F
??mA Max, ??mA Idle
=PP1V05_S0_PCH_VCCCLK_SSC
VCCCLK: 306mA Max, 89mA Idle
=PP3V3_S0_PCH_VCCCLK3_3
VCCCLK3_3: 55mA Max, 11mA Idle
VCCVRM
VCC
VCCCLK
VCCCLK3_3
=PP1V05_S0_PCH_VCCCLK_CLK135
VCCCLK: 306mA Max, 89mA Idle
=PP1V05_S0_PCH_VCCCLK_CLK100
=PP1V05_S0_PCH_VCCCLK_SSC100
VCCCLK: 306mA Max, 89mA Idle
VCCCLK
USB
GPIO/LPC
HDA
RTC
CPU
SPI
CLK/MISC
=PP3V3_SUS_PCH_VCCSUS_GPIO
VCCSUS3_3: 261mA Max, 6mA Idle
=PP3V3_S5_PCH_VCCDSW
15 mA Max, 1mA Idle
DCPSST
PPVOUT_S0_PCH_DCPSST
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
BYPASS=U1100.AA14:6.35mm
C1580
0.1UF
=PP3V3_S0_PCH_VCC3_3_GPIO
VCC3_3: 133mA Max, 3mA Idle
=PP1V05_S0_PCH_VCCIO_GPIO
VCCIO: 3629mA Max, 264mA Idle
=PP3V3R1V5_S0_PCH_VCCSUSHDA
10mA Max, 1mA Idle
=PP3V3_SUS_PCH_VCCSUS_RTC
VCCSUS3_3: 261mA Max, 6mA Idle
=PPVRTC_G3_PCH
6uA Max (3.0V, room temperature)
DCPRTC
PPVOUT_S0_PCH_DCPRTC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
BYPASS=U1100.P14:6.35mm
C1590
0.1UF
C1533
0.1UF
C1532
0.1UF
C1531
1UF
6.3V
BYPASS=U1100.A6:6.35mm
=PP1V05_S0_PCH_V_PROC_IO
4mA Max, 2mA Idle
=PP3V3_SUS_PCH_VCC_SPI
22mA Max, 1mA Idle
NOTE: Pin name is VCC but really is 3.3V
=PP3V3_S0_PCH_VCC_FUSE
??mA Max, ??mA Idle
=PP1V05_S0M_PCH_VCCASW
VCCASW: 670mA Max, 34mA Idle
=PP1V05_S0M_PCH_VCCASW
VCCASW: 670mA Max, 34mA Idle
=PP1V5_S0_PCH_VCCVRM_THRM
VCCVRM: 183mA Max, 68mA Idle
=PP3V3_S0_PCH_VCC3_3_THRM
VCC3_3: 133mA Max, 3mA Idle
THERMAL
Current data from LPT EDS (doc #486708, Rev 1.0).
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
PAGE TITLE
PCH Power
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
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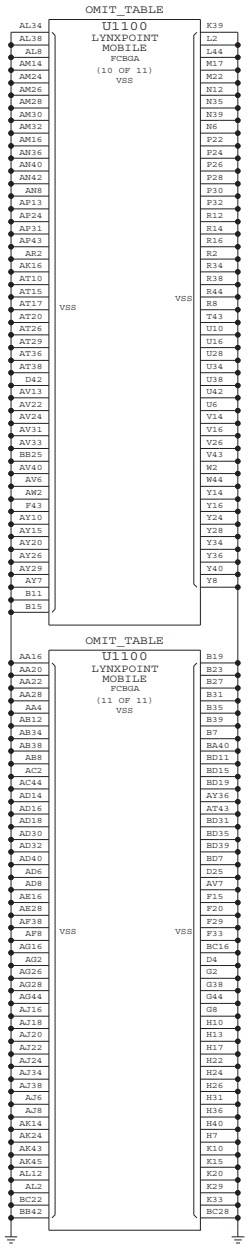

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE

PCH Grounds

Apple Inc.

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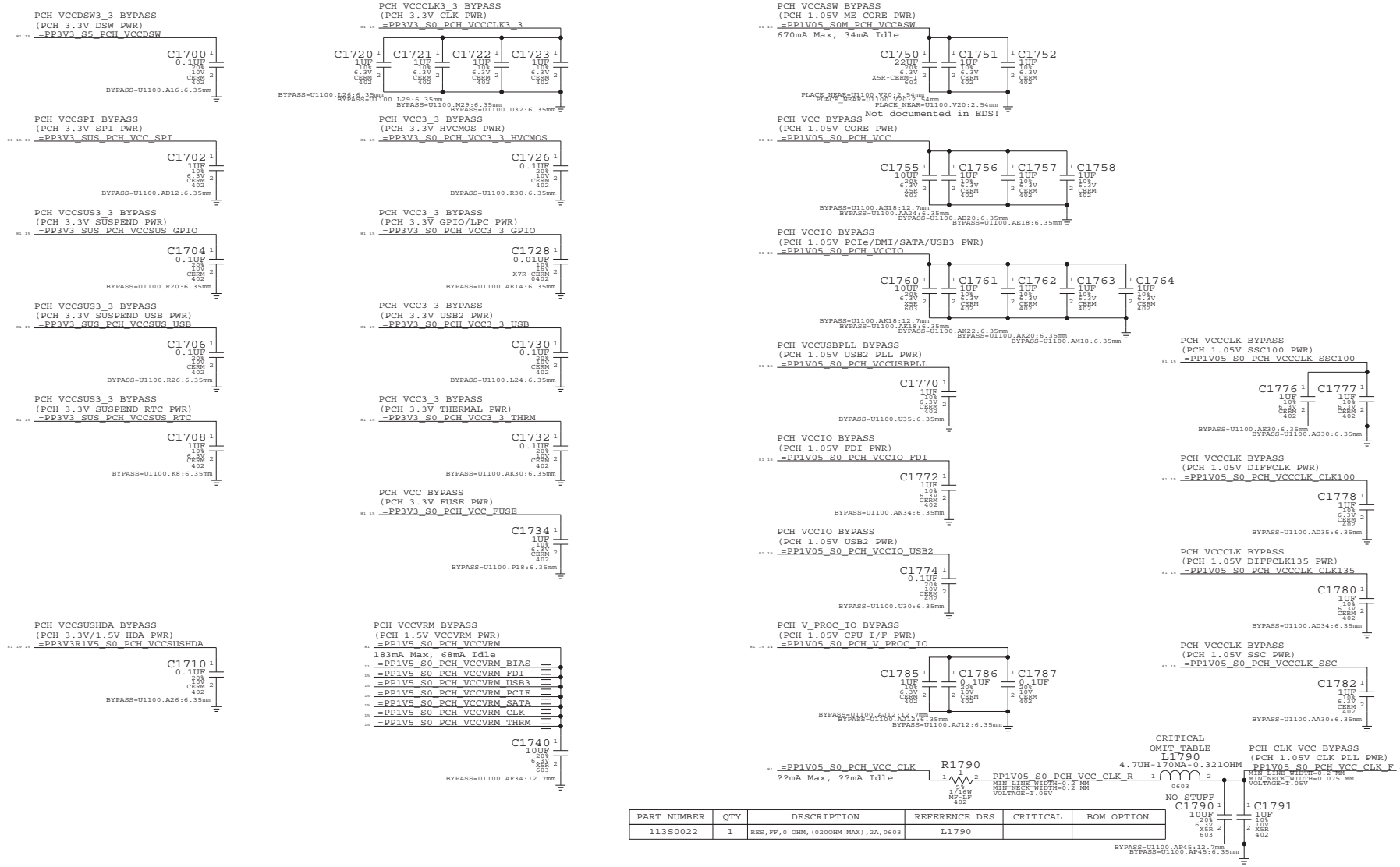

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(0220HM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE

PCH DECOUPLING

Apple Inc.

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Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

Merged (CPU/PCH) Micro2-XDP

PPVCCIO_S0_CPU
=PP1V05_S0_CPU_JTAG
R1830 150 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

XDP_CPU_PREQ_L	OBSFN_A0	OBSFN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSFN_A1	OBSFN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSFN_B0	OBSFN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSFN_B1	OBSFN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
XDP_SYS_PWROK	HOOK3	RESET#/HOOK6	XDP_CPURST_L
		DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_CPU_TDO
=SMBUS_XDP_SCL	SCL	TRST#	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_CPU_TDI
	TCK0	TMS	XDP_CPU_TMS
		XDP_PRESENT#	XDP_CPU_PRESENT_L

518S0847

CPU_PWRGD → R1800 1K 5% 1/20W MF 201 PLACE_NEAR=U0500.F50:2.54mm
PM_PWRBTN_L → R1802 0 5% 1/20W MF 0201 PLACE_NEAR=U0500.J3:2.54mm
PM_PCH_SYS_PWROK → R1804 0 5% 1/16W MF-LF 402
XDP_CPU_TCK

C1804 0.1UF 10% 6.3V CERM-X5R 0201
R1831 1K 5% 1/16W MF-LF 402
C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
C1806 0.1UF 10% 6.3V CERM-X5R 0201

=PP1V05_S0_CPU_JTAG
XDP_CPU_TDO → R1820 51 5% 1/20W MF 201 PLACE_NEAR=U0500.M49:28mm
XDP_CPU_TCK → R1823 51 5% 1/20W MF 201 PLACE_NEAR=U0500.N54:28mm
XDP_CPU_TRST_L → R1824 51 5% 1/20W MF 201 PLACE_NEAR=U0500.M53:28mm

TDI and TMS are terminated in CPU.

R1805 1K 5% 1/20W MF 201 PLACE_NEAR=U0500.AG7:2.54mm
PLT_RESET_L
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS

CRITICAL Q1840 DMN5L06VK-7 SOT-563 — PLACE_NEAR=J1800.51:28mm — XDP_CPU_TDO
CRITICAL Q1840 DMN5L06VK-7 SOT-563 — PLACE_NEAR=J1800.53:28mm — XDP_CPUPCH_TRST_L, MAKE_BASE=TRUE, XDP_CPU_TRST_L
CRITICAL Q1842 DMN5L06VK-7 SOT-563 — PLACE_NEAR=J1800.55:28mm — XDP_CPU_TDI
CRITICAL Q1842 DMN5L06VK-7 SOT-563 — PLACE_NEAR=J1800.57:28mm — XDP_CPU_TMS

PCH/XDP Signals

OMIT (All 10 R's)

				Non-XDP Signals
XDP_DA0_USB_EXTA_OC_L	R1890	SHORT		USB_EXTA_OC_L
XDP_DA2_SSD_PWR_EN	R1895	SHORT		SSD_PWR_EN
XDP_DA3_CAMERA_PWR_EN	R1893	SHORT		CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L	R1894	SHORT		USB_EXTB_OC_L
XDP_DB2_SD_PWR_EN	R1896	SHORT		SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L	R1897	SHORT		SDCONN_STATE_CHANGE_L
XDP_DC0_DP_AUXCH_ISOL_L	R1872	SHORT		DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN		MAKE_BASE=TRUE		SATARDRVR_EN
XDP_DC2_ODD_PWR_EN_L		MAKE_BASE=TRUE		ODD_PWR_EN_L
XDP_DC3_JTAG_ISP_TCK	R1875	SHORT		JTAG_ISP_TCK
XDP_DD0_SSD_PCIE_SEL_L	R1876	SHORT		SSD_PCIE_SEL_L
XDP_DD1_MLB_RAMCFG1		MAKE_BASE=TRUE		MLB_RAMCFG1
XDP_DD2_ENETSD_CLKREQ_L		MAKE_BASE=TRUE		ENETSD_CLKREQ_L
XDP_DD3_AP_CLKREQ_L	R1879	SHORT		AP_CLKREQ_L

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

XDP_DA1_USB_EXTC_OC_L → TP1810
XDP_DB1_USB_EXTD_OC_L → TP1811
XDP_FC0_HDD_PWR_EN → TP1812
XDP_FC1_GPU_GOOD → TP1813

CPU JTAG Isolation

=PP5V_S0_XDPJTAGISOL
=PP3V3_S5_XDPJTAGISOL
C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

=PP1V05_SUS_PCH_JTAG
XDP_PCH_TDO → R1860 51 5% 1/20W MF 201 PLACE_NEAR=U1100.AD3:28mm
XDP_PCH_TDI → R1861 51 5% 1/20W MF 201 PLACE_NEAR=U1100.AE2:28mm
XDP_PCH_TMS → R1862 51 5% 1/20W MF 201 PLACE_NEAR=U1100.AD1:28mm
XDP_PCH_TCK → R1866 51 5% 1/20W MF 201 PLACE_NEAR=U1100.AB3:28mm

SYNC_MASTER=CLEAN J45 SYNC_DATE=04/26/2013

PAGE TITLE: CPU & PCH XDP

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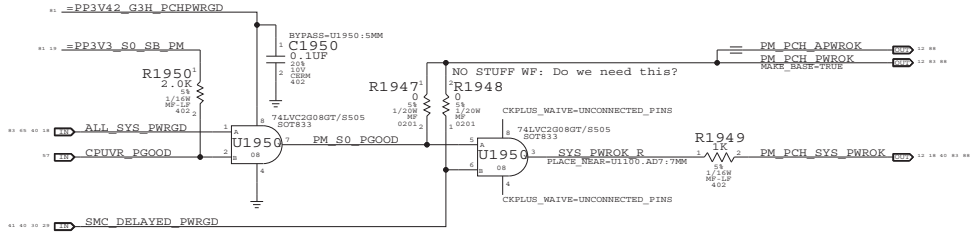
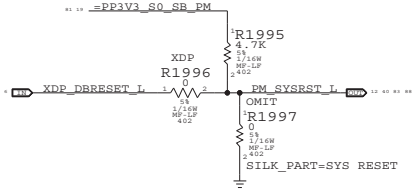
PCH PWROK Generation



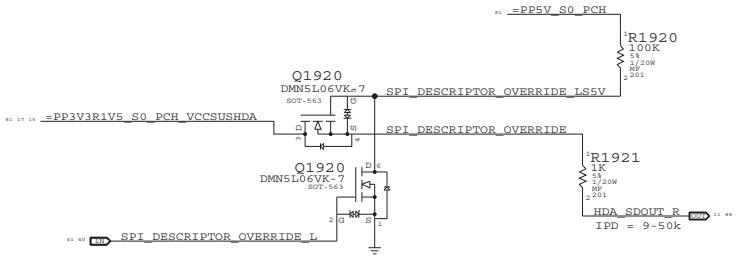
NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

PCH Reset Button

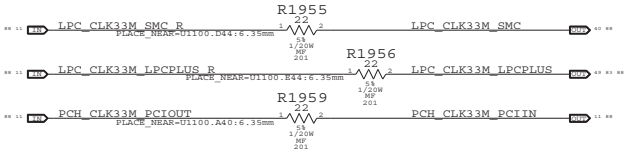


PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



PCH 33MHz Clocks



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

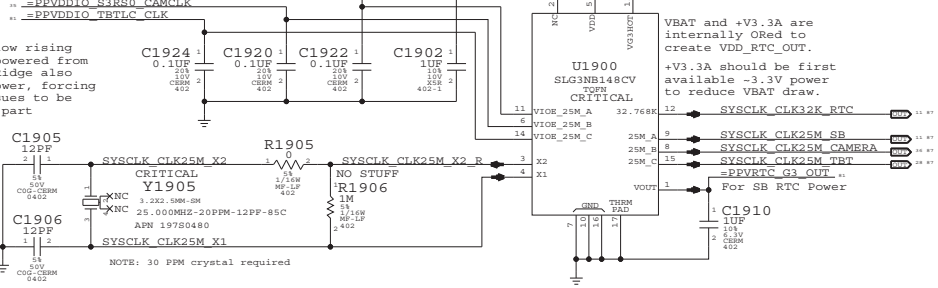
NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

=PPVBAT_G3_SYSCLK
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

=PP3V3_S5_SYSCLK
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary

GreenClk 25MHz Power =PP3V3_S4_SYSCLK
SB XTAL Power =PPVDDIO_S0_SBCLK
Camera XTAL Power =PPVDDIO_S3RS0_CAMCLK
TBT XTAL Power =PPVDDIO_TBTLC_CLK

NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Redwood Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).



VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.

NOTE: 30 PPM crystal required

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE: Chipset Support

Apple Inc.

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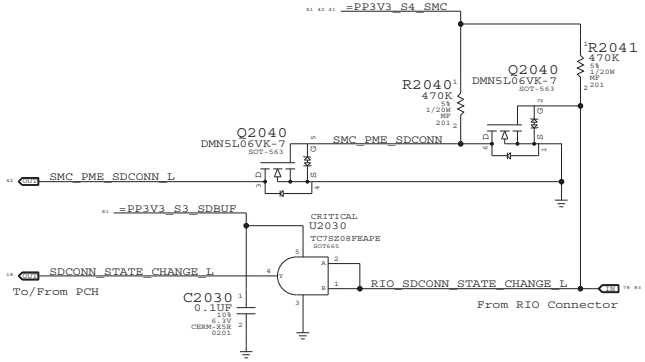
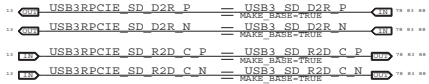
RIO SD Card Reader Support



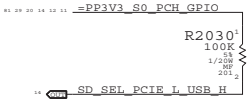
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.



Flexible I/O Configuration Strap

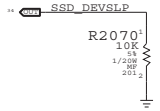
Must pull signal correctly even if always USB or PCIe



PCH 33MHz Clock for DPMUX

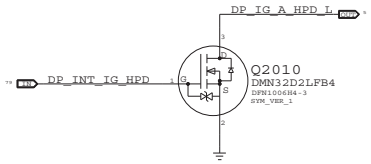
GS3 Connector Support

DEVSLP not supported on LPT-H

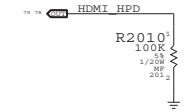


LCD HPD Inverter

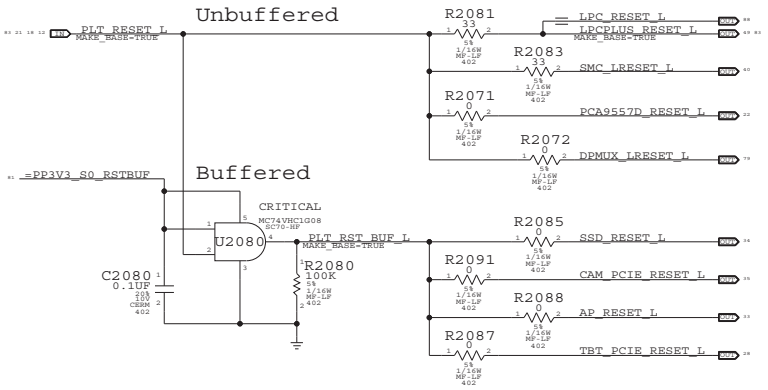
(Pull-Up on CPU Page)



HDMI HPD pull-down

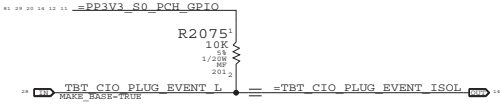


Platform Reset Connections



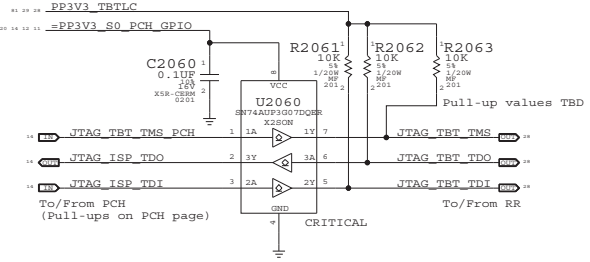
Redwood Ridge Support

RR output is open-drain, no isolation necessary

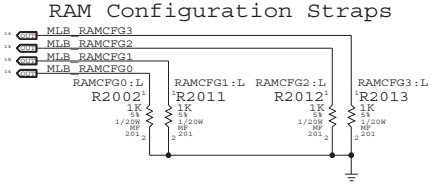


Redwood Ridge JTAG Isolation

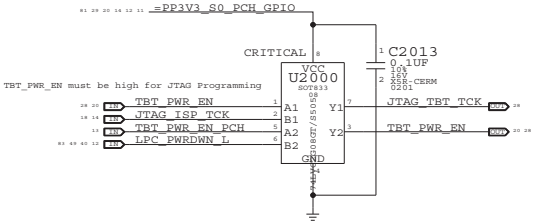
TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V



RAM Configuration Straps



GPIO Glitch Prevention



SYNC MASTER=CLEAN J45	SYNC DATE=04/26/2013
PAGE TITLE: Project Chipset Support	
Apple Inc.	DRAWING NUMBER: 051-0675 SIZE: D
	REVISION: 6.0.0
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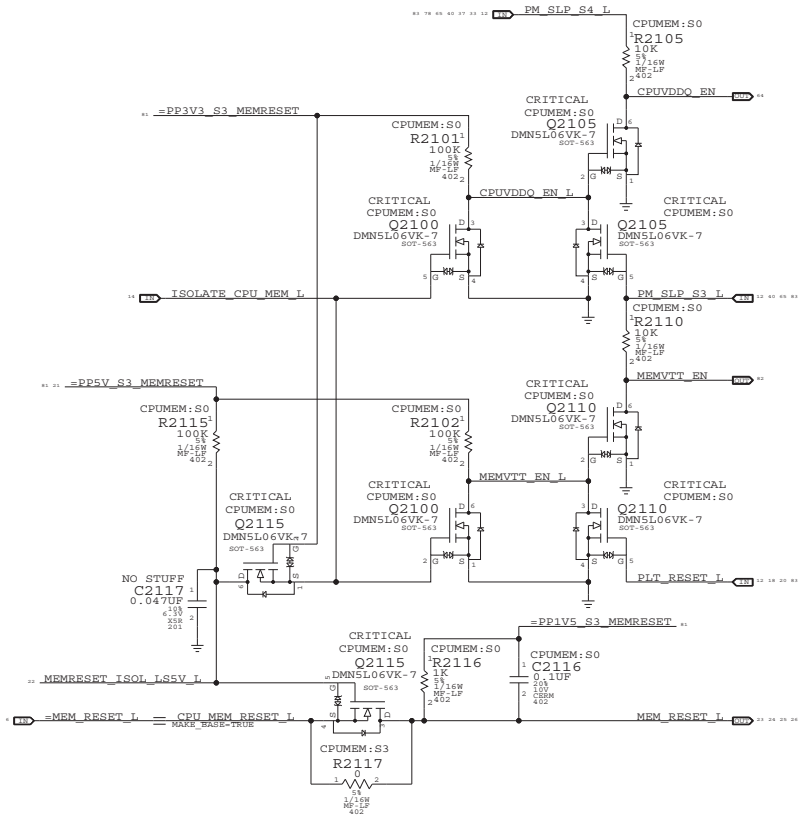
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



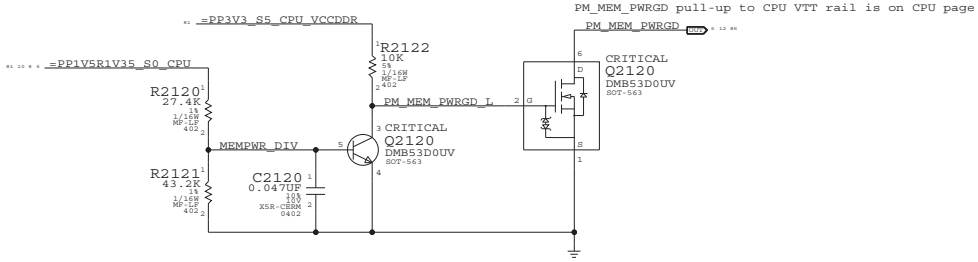
Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0 0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to 1	0	1	1	1	1	1	1	1
S3 2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
to 5	0	1	1	1	0 (*)	1	1	1
S0 6	0	1	1	1	1	1	1	1
7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

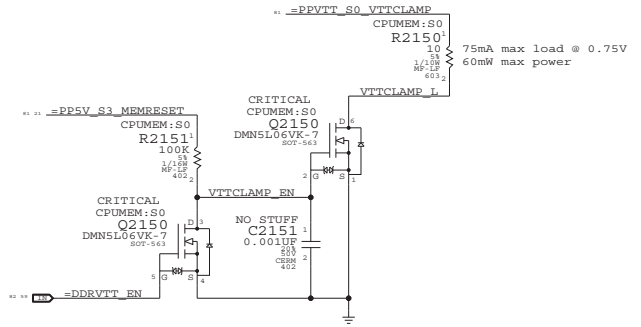
MEM S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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SHEET: 21 OF 94

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during S3

MEMRESET_ISOL_LS5V_L
CPU_DIMMA_VREFDQ
CPU_DIMMB_VREFDQ
CPU_DIMM_VREFCA

CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563
CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563

CPU_MEM_VREFDQ_A_ISOL
CPU_MEM_VREFDQ_B_ISOL
CPU_MEM_VREFCA_A_ISOL
CPU_MEM_VREFCA_B_ISOL

EN RC's to avoid drain glitches

VREFMRGN_DQ_A_EN_RC
VREFMRGN_DQ_B_EN_RC
VREFMRGN_CA_A_EN_RC
VREFMRGN_CA_B_EN_RC

DDRVREF_DAC R2225 100K 1% 1/16W MF-LF 402
DDRVREF_DAC R2245 100K 1% 1/16W MF-LF 402
DDRVREF_DAC R2265 100K 1% 1/16W MF-LF 402
DDRVREF_DAC R2285 100K 1% 1/16W MF-LF 402

DDRVREF_DAC R2201 100K 5% 1/20W MF 201
DDRVREF_DAC R2202 100K 5% 1/20W MF 201
DDRVREF_DAC R2207 100K 5% 1/20W MF 201
DDRVREF_DAC R2208 100K 5% 1/20W MF 201

DDRVREF_DAC C2225 0.1UF 20% 10V CERM 402
DDRVREF_DAC C2245 0.1UF 20% 10V CERM 402
DDRVREF_DAC C2265 0.1UF 20% 10V CERM 402
DDRVREF_DAC C2285 0.1UF 20% 10V CERM 402

CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563

Q2225 pin 6: PLACE_NEAR=Q2220.6:2.54mm
Q2265 pin 6: PLACE_NEAR=Q2260.6:2.54mm

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.

VRef Dividers

Always used, regardless of margining option.

=PPDDR_S3_MEMVREF

R2223 2 5% 1/20W MF 201
R2243 2 5% 1/20W MF 201
R2263 2 5% 1/20W MF 201
R2283 2 5% 1/20W MF 201

R2221 1K 1% 1/16W MF-LF 402
R2222 1K 1% 1/16W MF-LF 402
R2241 1K 1% 1/16W MF-LF 402
R2242 1K 1% 1/16W MF-LF 402
R2261 1K 1% 1/16W MF-LF 402
R2262 1K 1% 1/16W MF-LF 402
R2281 1K 1% 1/16W MF-LF 402
R2282 1K 1% 1/16W MF-LF 402

R2220 24.9 1% 1/20W MF 201
R2240 24.9 1% 1/20W MF 201
R2260 24.9 1% 1/20W MF 201
R2280 24.9 1% 1/20W MF 201

C2220 0.022UF 10% 6.3V X5R-CERM 0201
C2240 0.022UF 10% 6.3V X5R-CERM 0201
C2260 0.022UF 10% 6.3V X5R-CERM 0201
C2280 0.022UF 10% 6.3V X5R-CERM 0201

MEM_VREFDQ_A_RC
MEM_VREFDQ_B_RC
MEM_VREFCA_A_RC
MEM_VREFCA_B_RC

PPVREF_S3_MEM_VREFDQ_A
PPVREF_S3_MEM_VREFDQ_B
PPVREF_S3_MEM_VREFCA_A
PPVREF_S3_MEM_VREFCA_B

MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

=PP3V3_S3_VREFMRGN
OMIT R2218 SHORT
PP3V3_S3_VREFMRGN
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC U2200 DAC5574 MSOP
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA
Addr=0x98(WR)/0x99(RD)

VREFMRGN_DQ_A
VREFMRGN_DQ_B
VREFMRGN_CA_AB
VREFMRGN_MEMVREG_FBVREF

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

(All 4 R's) DDRVREF_DAC
R2226 332 1% 1/16W MF-LF 402 VREFMRGN_DQ_A_RDIV
R2246 332 1% 1/16W MF-LF 402 VREFMRGN_DQ_B_RDIV
R2266 332 1% 1/16W MF-LF 402 VREFMRGN_CA_A_RDIV
R2286 332 1% 1/16W MF-LF 402 VREFMRGN_CA_B_RDIV

R22x6 pin 2:
PLACE_NEAR=Q2225.1:2.54mm
PLACE_NEAR=Q2225.4:2.54mm
PLACE_NEAR=Q2265.1:2.54mm
PLACE_NEAR=Q2265.4:2.54mm

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC U2201 PCA9557 QFN (OD)
Addr=0x30(WR)/0x31(RD)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA

VREFMRGN_DQ_A_EN
VREFMRGN_DQ_B_EN
VREFMRGN_CA_A_EN
VREFMRGN_CA_B_EN
VREFMRGN_MEMVREG_EN
VREFMRGN_FRAMEBUF_EN

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PCA9557D_RESET_L

=PP3V3_S3_VREFMRGN
DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC U2204 MAX4253 UCSP
VREFMRGN_MEMVREG_BUF
DDRVREF_DAC R2214 33.2K 1% 1/16W MF-LF 402
DDRREG_FB

DDRVREF_DAC R2213 100K 1% 1/20W MF 201
CRITICAL DDRVREF_DAC U2204 MAX4253 UCSP
VREFMRGN_FRAMEBUF_BUF
DDRVREF_DAC R2217 1M 1% 1/16W MF-LF 402

DDRVREF_DAC R2215 100K 1% 1/20W MF 201

Pins B1 & B4:
CKPLUS_WAIVE=unconnected_pins

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	DDR3 (1.5V)		DDR3L (1.35V)		DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output	3.923mV / step @ output

NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE: DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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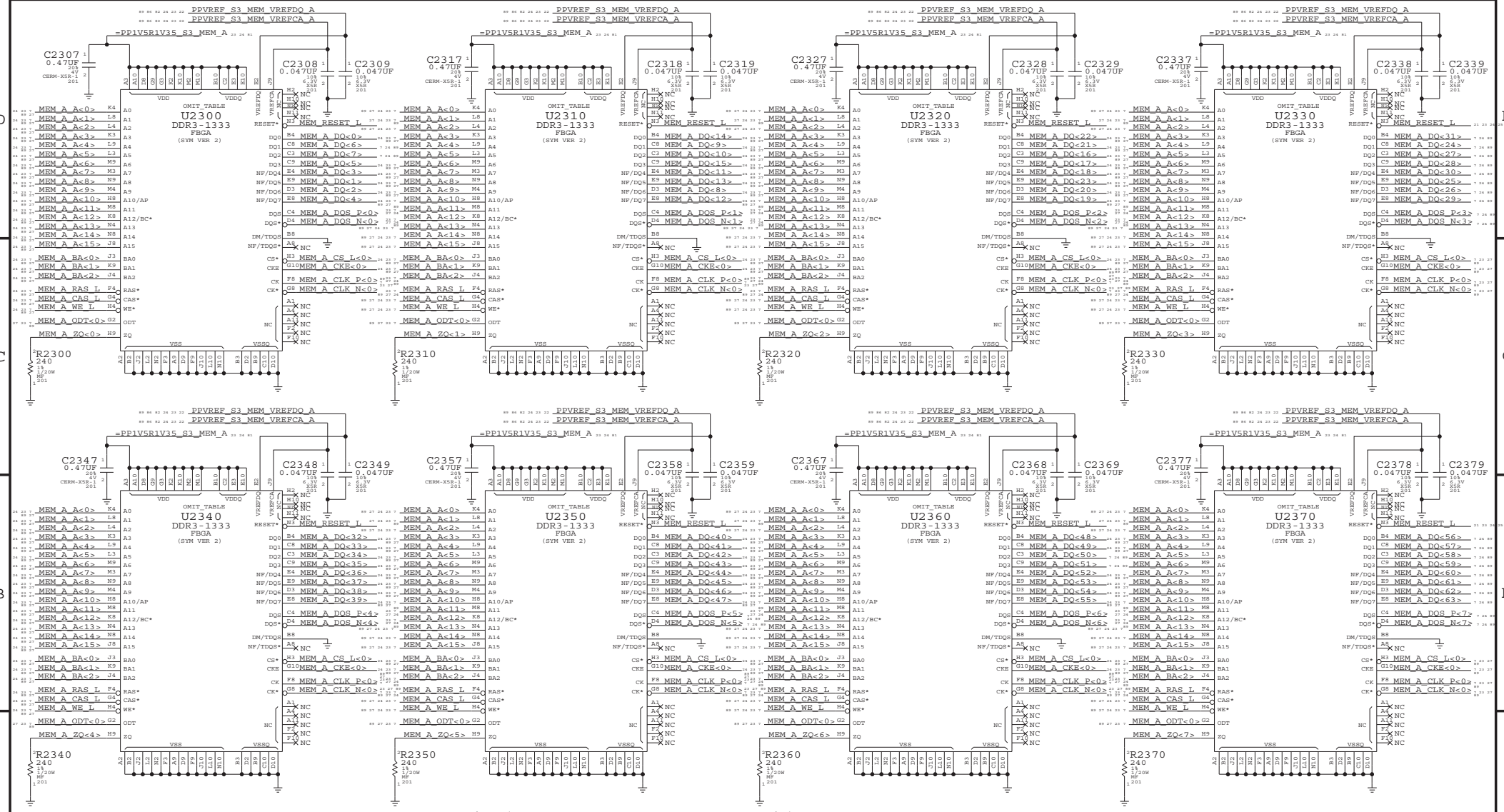
U2300
U2310
U2320
U2330
U2340
U2350
U2360
U2370
DDR3-1333
FBGA
(SYM VER 2)
OMIT_TABLE
SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
PAGE TITLE
DDR3 SDRAM Bank A (1 OF 2)
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
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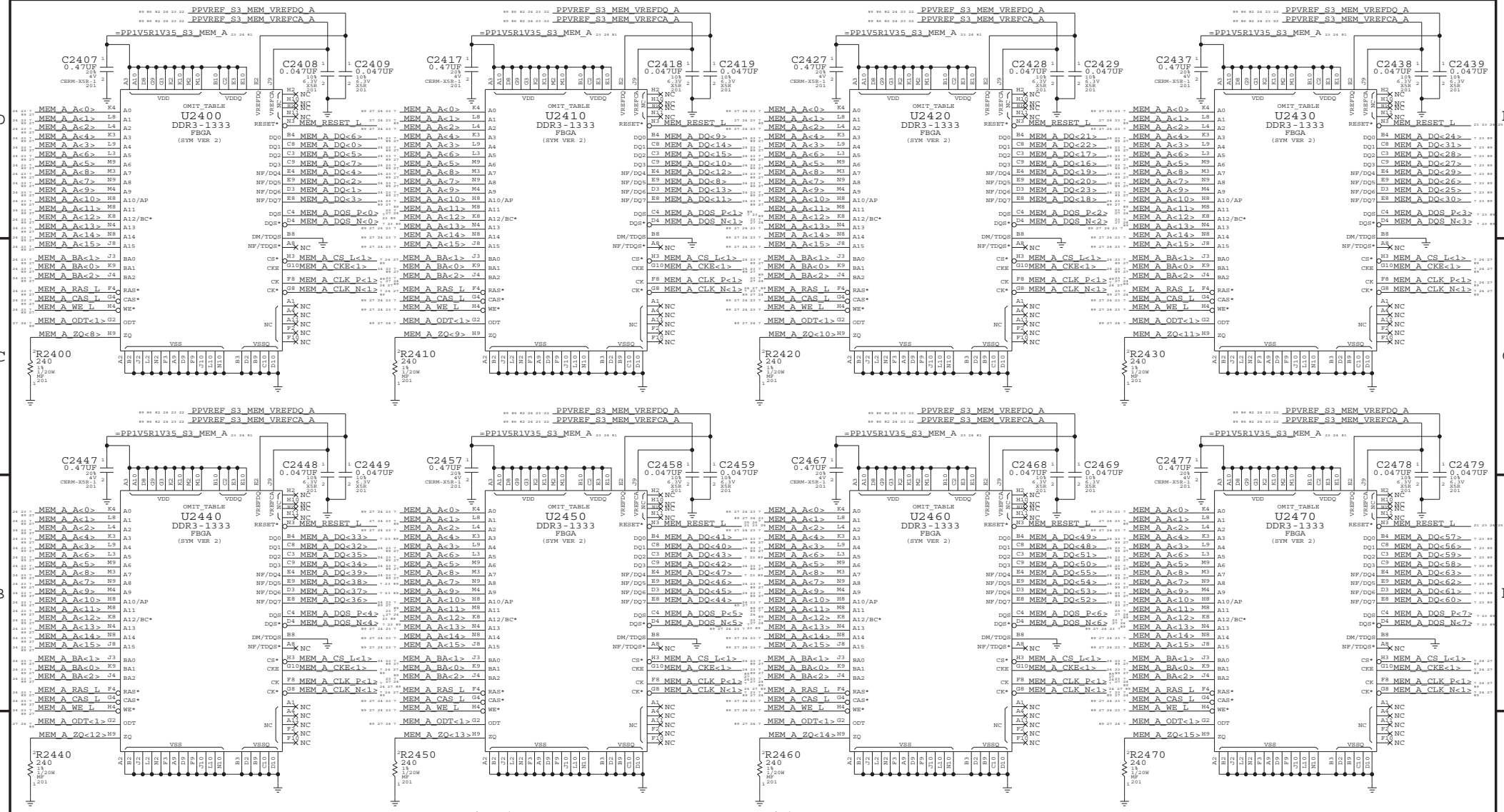

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PAGE TITLE
DDR3 SDRAM Bank A (2 OF 2)

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REVISION 6.0.0

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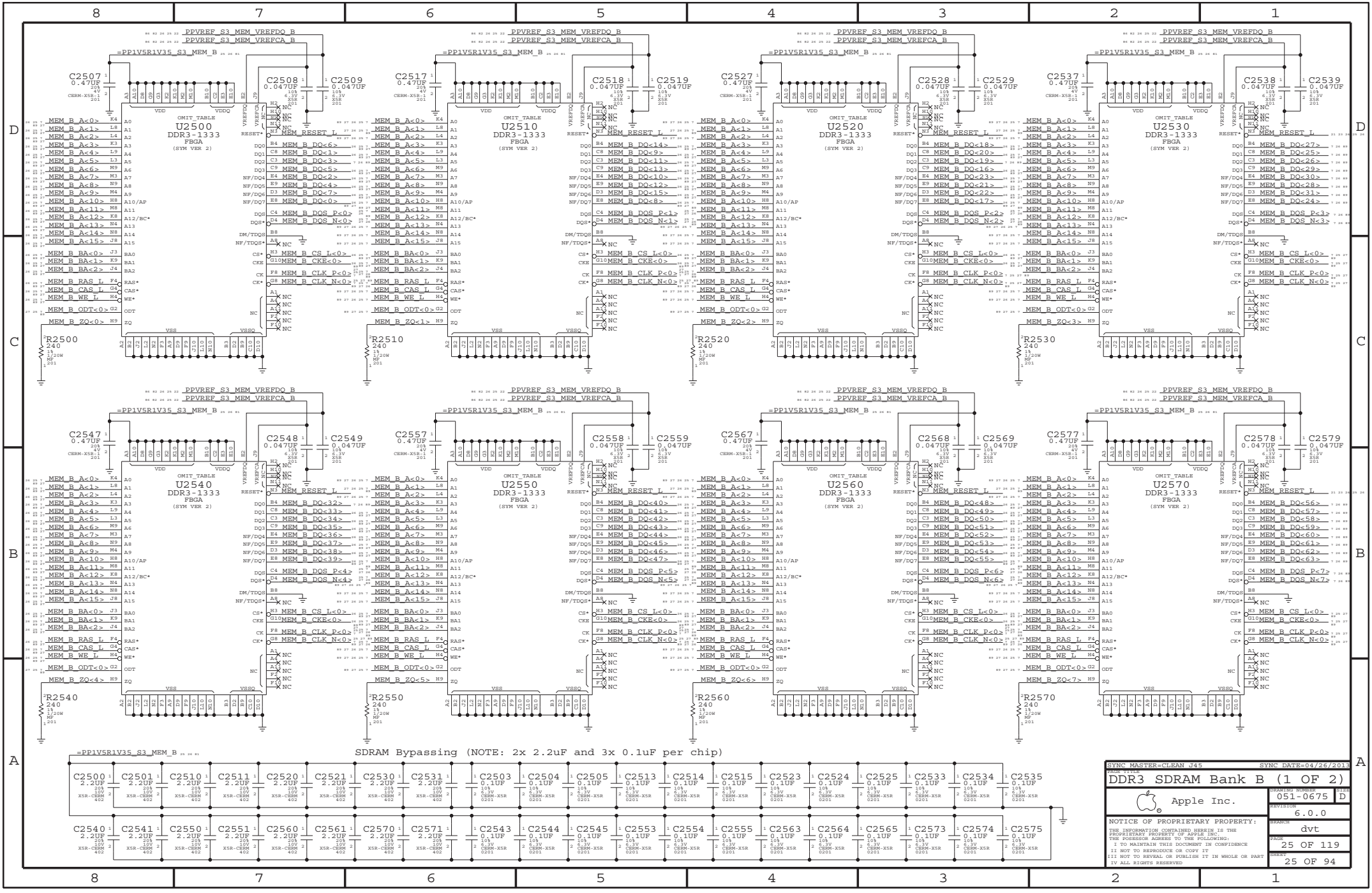
U2500
U2510
U2520
U2530
U2540
U2550
U2560
U2570
DDR3-1333
FBGA
(SYM VER 2)
OMIT_TABLE
=PP1V5R1V35_S3_MEM_B
PPVREF_S3_MEM_VREFDQ_B
PPVREF_S3_MEM_VREFCA_B
MEM_RESET_L
MEM_B_CS_L<0>
MEM_B_CKE<0>
MEM_B_CLK_P<0>
MEM_B_CLK_N<0>
MEM_B_RAS_L
MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<0>
SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
PAGE TITLE
DDR3 SDRAM Bank B (1 OF 2)
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
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PAGE
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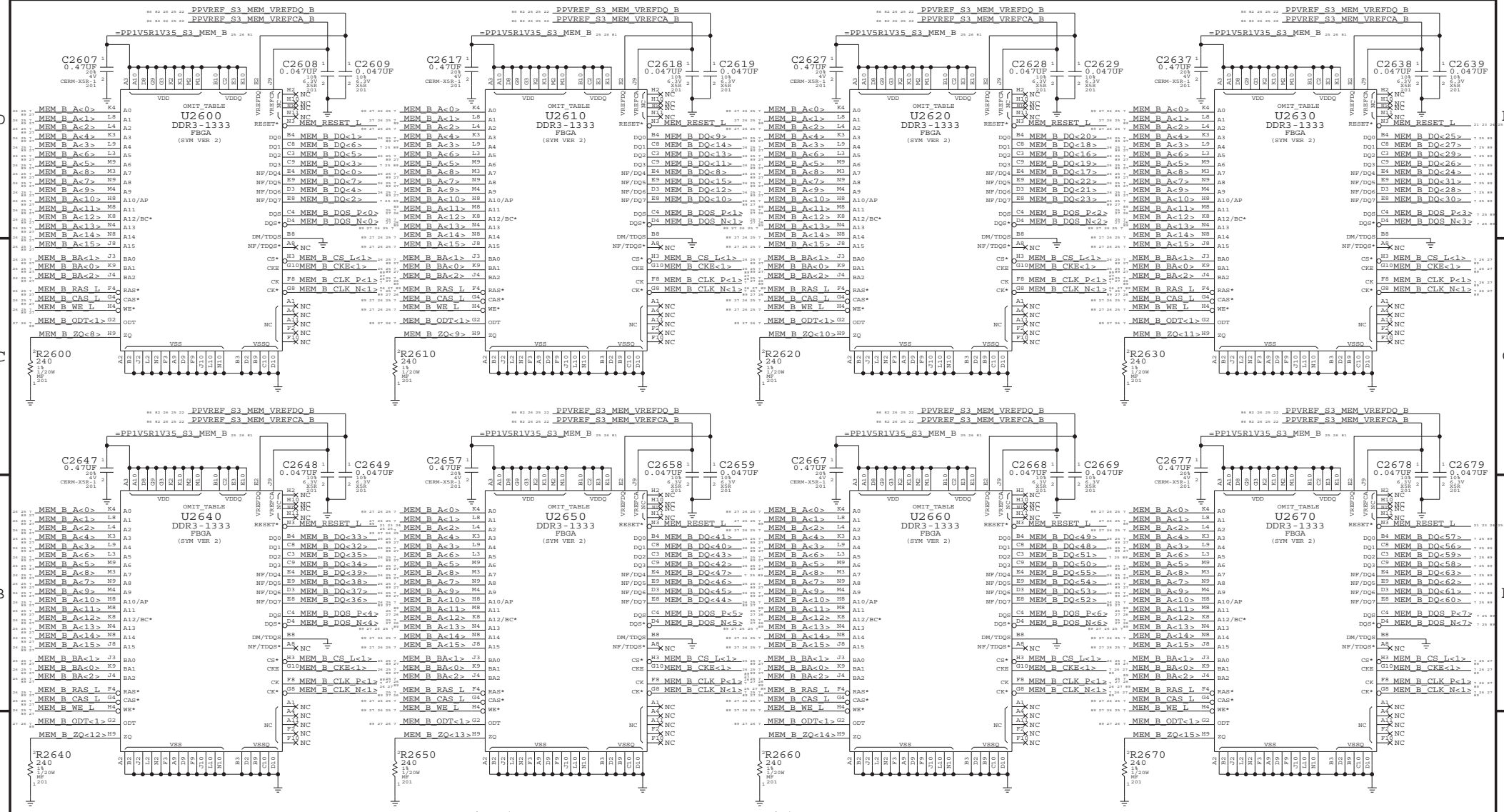

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE
DDR3 SDRAM Bank B (2 OF 2)

Apple Inc.

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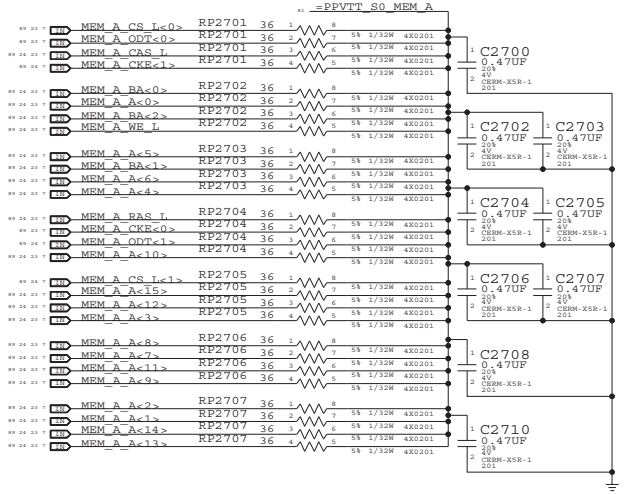
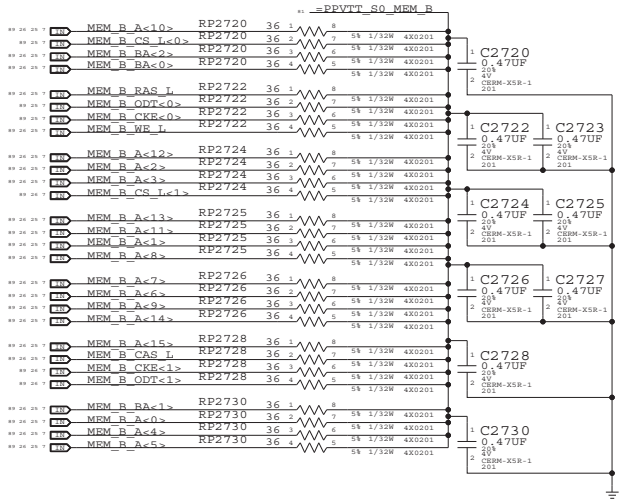
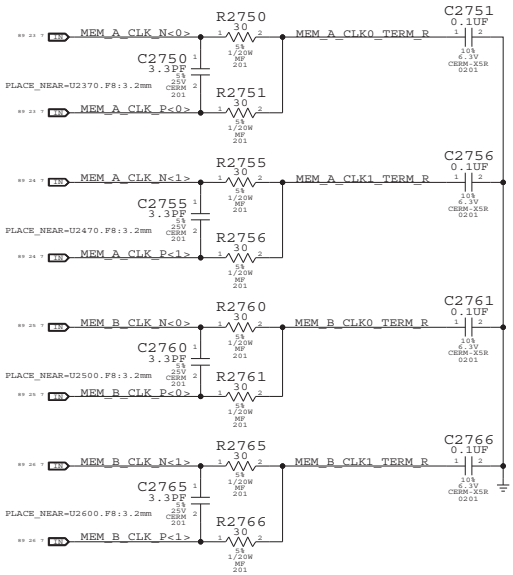
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC MASTER=CLEAN_J45 SYNC DATE=04/26/2013

PAGE TITLE

DDR3 Termination

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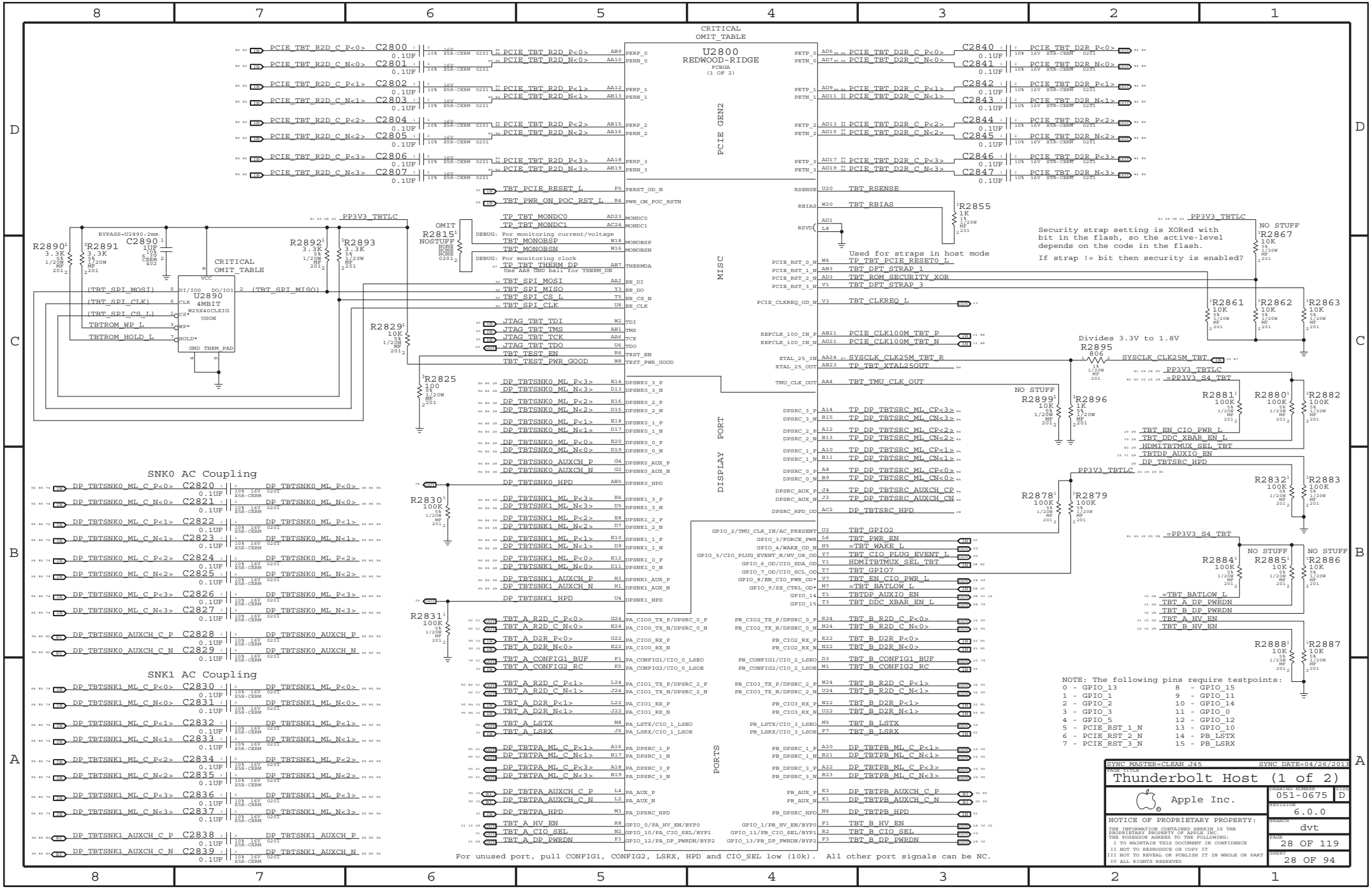
CRITICAL
OMIT_TABLE
U2800
REDWOOD-RIDGE
FCBGA
(1 OF 2)
PCIE GEN2
MISC
DISPLAY PORT
PORTS
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_P<0>
PCIE_TBT_R2D_N<0>
PCIE_TBT_R2D_P<1>
PCIE_TBT_R2D_N<1>
PCIE_TBT_R2D_P<2>
PCIE_TBT_R2D_N<2>
PCIE_TBT_R2D_P<3>
PCIE_TBT_R2D_N<3>
PCIE_TBT_D2R_C_P<0>
PCIE_TBT_D2R_C_N<0>
PCIE_TBT_D2R_C_P<1>
PCIE_TBT_D2R_C_N<1>
PCIE_TBT_D2R_C_P<2>
PCIE_TBT_D2R_C_N<2>
PCIE_TBT_D2R_C_P<3>
PCIE_TBT_D2R_C_N<3>
PCIE_TBT_D2R_P<0>
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<1>
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_P<2>
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<3>
PCIE_TBT_D2R_N<3>
TBT_PCIE_RESET_L
TBT_PWR_ON_POC_RST_L
TP_TBT_MONDC0
TP_TBT_MONDC1
TBT_MONOBSP
TBT_MONOBSN
TP_TBT_THERM_DP
TBT_SPI_MOSI
TBT_SPI_MISO
TBT_SPI_CS_L
TBT_SPI_CLK
JTAG_TBT_TDI
JTAG_TBT_TMS
JTAG_TBT_TCK
JTAG_TBT_TDO
TBT_TEST_EN
TBT_TEST_PWR_GOOD
TBT_RSENSE
TBT_RBIAS
TP_TBT_PCIE_RESET0_L
TBT_DFT_STRAP_1
TBT_ROM_SECURITY_XOR
TBT_DFT_STRAP_3
TBT_CLKREQ_L
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
SYSCLK_CLK25M_TBT_R
TP_TBT_XTAL25OUT
TBT_TMU_CLK_OUT
TP_DP_TBTSRC_ML_CP<3>
TP_DP_TBTSRC_ML_CN<3>
TP_DP_TBTSRC_ML_CP<2>
TP_DP_TBTSRC_ML_CN<2>
TP_DP_TBTSRC_ML_CP<1>
TP_DP_TBTSRC_ML_CN<1>
TP_DP_TBTSRC_ML_CP<0>
TP_DP_TBTSRC_ML_CN<0>
TP_DP_TBTSRC_AUXCH_CP
TP_DP_TBTSRC_AUXCH_CN
DP_TBTSRC_HPD
TBT_GPIO2
TBT_PWR_EN
=TBT_WAKE_L
TBT_CIO_PLUG_EVENT_L
HDMITBTMUX_SEL_TBT
TBT_GPIO7
TBT_EN_CIO_PWR_L
=TBT_BATLOW_L
TBTDP_AUXIO_EN
TBT_DDC_XBAR_EN_L
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_A_CONFIG1_BUF
TBT_A_CONFIG2_RC
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
TBT_A_LSTX
TBT_A_LSRX
TBT_A_HV_EN
TBT_A_CIO_SEL
TBT_A_DP_PWRDN
TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
TBT_B_D2R_P<0>
TBT_B_D2R_N<0>
TBT_B_CONFIG1_BUF
TBT_B_CONFIG2_RC
TBT_B_R2D_C_P<1>
TBT_B_R2D_C_N<1>
TBT_B_D2R_P<1>
TBT_B_D2R_N<1>
TBT_B_LSTX
TBT_B_LSRX
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
DP_TBTPB_AUXCH_C_P
DP_TBTPB_AUXCH_C_N
DP_TBTPB_HPD
TBT_B_HV_EN
TBT_B_CIO_SEL
TBT_B_DP_PWRDN
PP3V3_TBTLC
CRITICAL
OMIT_TABLE
BYPASS=U2890:2mm
U2890
4MBIT
W25X40CLXIG
USON
GND THRM PAD
(TBT_SPI_MOST)
(TBT_SPI_CLK)
(TBT_SPI_CS_L)
TBTROM_WP_L
TBTROM_HOLD_L
(TBT_SPI_MISO)
R2890 3.3K
R2891 3.3K
R2892 3.3K
R2893 3.3K
C2890 1UF
R2815 NOSTUFF
R2829 10K
R2825 100
Used for straps in host mode
Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.
If strap != bit then security is enabled?
Divides 3.3V to 1.8V
R2895 806
R2896 1K
R2899 NOSTUFF 10K
R2855 1K
R2861 10K
R2862 10K
R2863 10K
R2867 NOSTUFF 10K
R2878 100K
R2879 100K
R2880 100K
R2881 100K
R2882 100K
R2883 100K
R2884 100K
R2885 NOSTUFF 10K
R2886 NOSTUFF 10K
R2887 10K
R2888 10K
R2830 100K
R2831 100K
TBT_EN_CIO_PWR_L
TBT_DDC_XBAR_EN_L
HDMITBTMUX_SEL_TBT
TBTDP_AUXIO_EN
DP_TBTSRC_HPD
=TBT_BATLOW_L
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN
=PP3V3_S4_TBT
SNK0 AC Coupling
SNK1 AC Coupling
DP_TBTSNK0_ML_C_P<0> C2820
DP_TBTSNK0_ML_C_N<0> C2821
DP_TBTSNK0_ML_C_P<1> C2822
DP_TBTSNK0_ML_C_N<1> C2823
DP_TBTSNK0_ML_C_P<2> C2824
DP_TBTSNK0_ML_C_N<2> C2825
DP_TBTSNK0_ML_C_P<3> C2826
DP_TBTSNK0_ML_C_N<3> C2827
DP_TBTSNK0_AUXCH_C_P C2828
DP_TBTSNK0_AUXCH_C_N C2829
DP_TBTSNK1_ML_C_P<0> C2830
DP_TBTSNK1_ML_C_N<0> C2831
DP_TBTSNK1_ML_C_P<1> C2832
DP_TBTSNK1_ML_C_N<1> C2833
DP_TBTSNK1_ML_C_P<2> C2834
DP_TBTSNK1_ML_C_N<2> C2835
DP_TBTSNK1_ML_C_P<3> C2836
DP_TBTSNK1_ML_C_N<3> C2837
DP_TBTSNK1_AUXCH_C_P C2838
DP_TBTSNK1_AUXCH_C_N C2839
0.1UF 10% 16V XSR-CERM 0201
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER 051-0675
SIZE D
REVISION 6.0.0
BRANCH dvt
PAGE 28 OF 119
SHEET 28 OF 94
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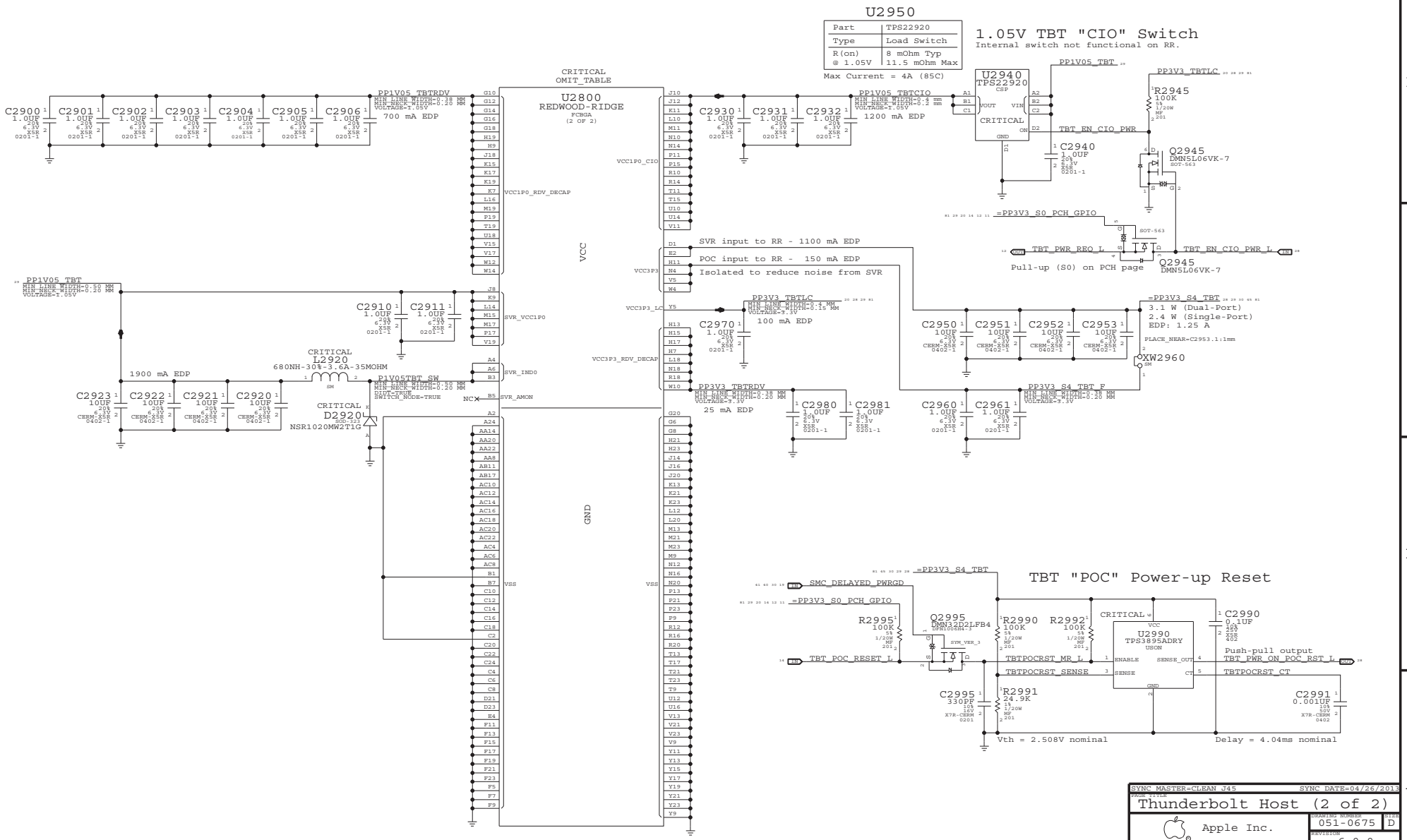

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE
Thunderbolt Host (2 of 2)

Apple Inc.

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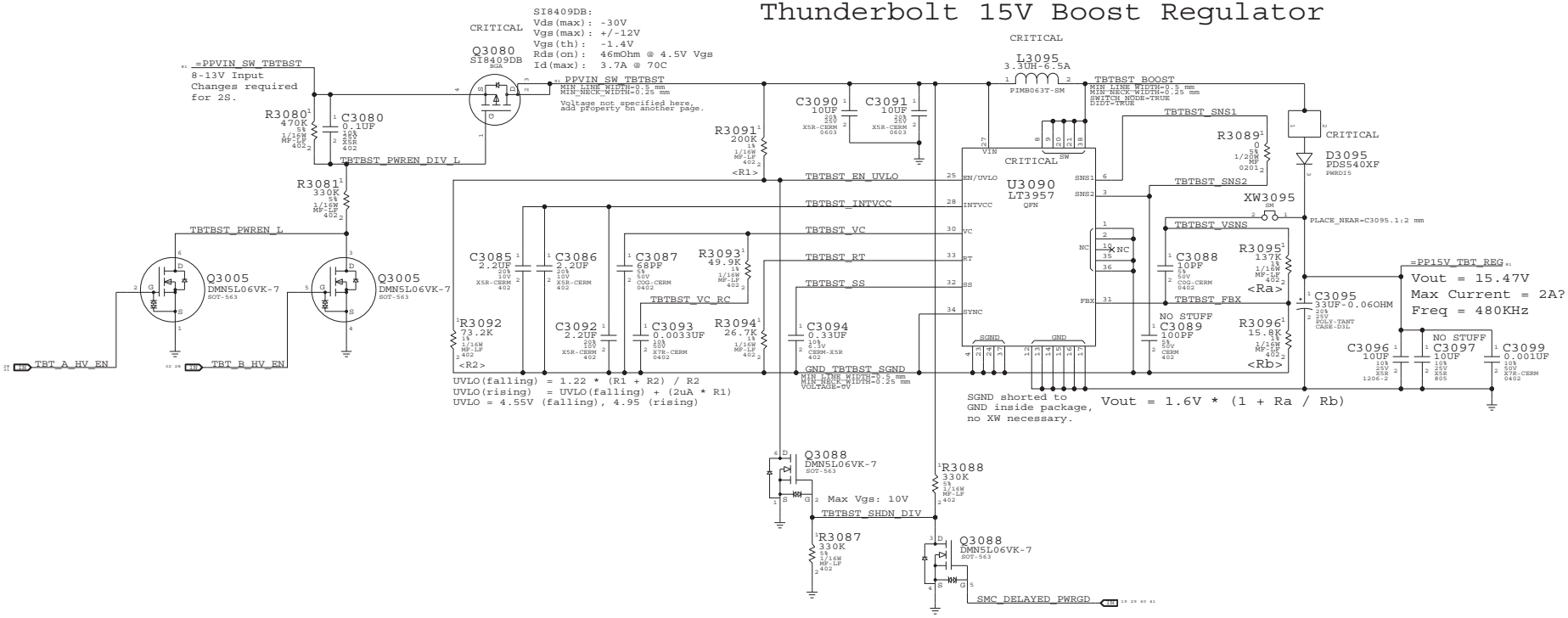
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

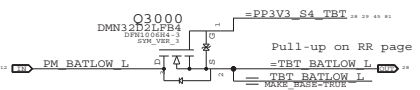
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator



BATLOW# Isolation



SYNC MASTER=CLEAN_J45 SYNC DATE=04/26/2013

PAGE TITLE: Thunderbolt Mobile Support

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

<RHVS3> <RHVS0> ILIM = 40000 / RISET

<RV3P3>

Thunderbolt Connector A

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

470k R's for ESD protection on AC-coupled signals.

514-0876

SYNC MASTER=CLEAN J45	SYNC DATE=04/26/2013
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Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTBPWRSW

CRITICAL C3387 100UF 20% 16V POLY-TANT CASE-B2-SM; C3380 22UF 20% 6.3V X5R-CERM 603; C3381 0.1UF 10% 16V X5R-CERM 0201

=PPHV_S4SW_TBTBPWRSW 15.75V Max

C3315 4.7UF 10% 25V X5R-CERM 0603; C3310 0.1UF 10% 25V X5R 402

CRITICAL U3310 CD3211A0RGPR QFN

C3385 0.1UF 10% 16V X5R-CERM 0201; C3386 10UF 20% 6.3V CERM-X5R 402; C3311 0.1UF 10% 25V X5R 402

PP3V3_S4_TBTBPWR MIN LINE WIDTH=0.38 MM MIN NECK WIDTH=0.20 MM VOLTAGE=3.3V

PP3V3RHV_S4_TBTBPWR MIN LINE WIDTH=0.38 MM MIN NECK WIDTH=0.20 MM VOLTAGE=15V

=TBTBPWRSW_EN

TBT_B_HV_EN

=TBT_S0_EN

TBTBPWRSW_ISET_V3P3

TBTBPWRSW_ISET_S0

TBTBPWRSW_ISET_S3

GND THRM PAD

TBTHV:P15V 12V: See below R3310 22.6K 1% 1/20W MF 201; TBTHV:P15V R3311 22.6K 1% 1/20W MF 201; R3312 36.5K 1% 1/20W MF 201 <RV3P3>

TBTBPWRSW_ISET_S3_R

TBTBPWRSW_ISET_S0_R

TBTHV:P15V R3313 22.6K 1% 1/20W MF 201 <RHVS3>; TBTHV:P15V R3314 22.6K 1% 1/20W MF 201 <RHVS0>

Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

PP3V3_S4_TBTBPWR

C3320 0.1UF 10% 16V X5R-CERM 0201

CRITICAL U3320 CBTL05024 HVQFN24-COMBO SIGNAL_MODEL=TBT_MUX

GND_VOID-TRUE (Both C's)

TBT_B_D2R_N<1> C3377 0.47UF 20% 4V CERM-X5R-1 TBT_B_D2R_C_N<1>

TBT_B_D2R_P<1> C3376 0.47UF 20% 4V CERM-X5R-1 TBT_B_D2R_C_P<1>

DP_TBTPB_AUXCH_C_N C3330 0.1UF 20% 16V X5R-CERM 0201 DP_TBTPB_AUXCH_N

DP_TBTPB_AUXCH_C_P C3331 0.1UF 10% 16V X5R-CERM 0201 DP_TBTPB_AUXCH_P

DP_TBTPB_DDC_DATA

DP_TBTPB_DDC_CLK

TBT_B_CONFIG1_BUF

DP_TBTPB_ML_C_P<1> C3332 0.22UF 20% 6.3V X5R 0201 DP_TBTPB_ML_P<1>

DP_TBTPB_ML_C_N<1> C3333 0.22UF 20% 6.3V X5R 0201 DP_TBTPB_ML_N<1>

TBT_B_LSTX

TBT_B_LSRX

DP_TBTPB_HPD

TB_ENA TBT_B_CIO_SEL

AUXIO_EN TBTDP_AUXIO_EN

DP_PD TBT_B_DP_PWRDN

(IPU) AUXIO- TBT_B_D2R1_AUXDDC_N

(IPD) AUXIO+ TBT_B_D2R1_AUXDDC_P

TBT: RX_1

DDC_DAT DDC_CLK

CA_DETOUT CA_DET TBT_B_CONFIG1_RC

DP+ DP- DPMLO+ TBT_B_LSX_ML_P<1> DPMLO- TBT_B_LSX_ML_N<1>

TBT: LSX_A_R2P/P2R (P/N)

LSTX (IPU) LSRX (IPD) HPDOUT HPD TBT_B_HPD

GND THRMPAD

Thunderbolt Connector B

CRITICAL L3300 FERR-120-OHM-3A 0603

PP3V3RHV_S4_TBTBPWR_F MIN LINE WIDTH=0.38 MM MIN NECK WIDTH=0.20 MM VOLTAGE=15V

C3300 0.01UF 10% 50V X7R-CERM 0402; C3301 0.01UF 10% 50V X7R-CERM 0402

TBTBCONN_20_RC MIN LINE WIDTH=0.38 MM MIN NECK WIDTH=0.20 MM VOLTAGE=18V

R3301 12 5% 1/20W MF 201

TBT Dir DP Dir

TBT: RX_0

GND_VOID-TRUE (Both C's)

TBT_B_D2R_P<0> C3374 0.47UF 20% 4V CERM-X5R-1 TBT_B_D2R_C_P<0>

TBT_B_D2R_N<0> C3375 0.47UF 20% 4V CERM-X5R-1 TBT_B_D2R_C_N<0>

R3394 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE; R3395 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE

DP_TBTPB_ML_C_P<3> C3378 0.22UF 20% 6.3V X5R 0201 DP_TBTPB_ML_P<3>

DP_TBTPB_ML_C_N<3> C3379 0.22UF 20% 6.3V X5R 0201 DP_TBTPB_ML_N<3>

TBT: Unused

R3379 470K 5% 1/20W MF 201; R3378 470K 5% 1/20W MF 201

TBT_B_D2R1_AUXDDC_P

TBT_B_D2R1_AUXDDC_N

TBT: RX_1

TBT_B_HPD

TBT_B_CONFIG1_RC

TBT_B_CONFIG2_RC

R3352 1M 5% 1/20W MF 201; R3351 1M 5% 1/20W MF 201; C3394 330PF 10% 16V X7R-CERM 0201; C3395 330PF 10% 16V X7R-CERM 0201; R3341 100K 5% 1/20W MF 201

C3302 0.01UF 10% 50V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

CRITICAL

J3200 MDP-J44 F-RT-TH SHIELD PINS PORT A

HPD CONFIG1 CONFIG2 GND2 ML_LANE3P ML_LANE3N GND4 AUX_CHP AUX_CHN DP_PWR

ML_LANE0P ML_LANE0N GND1 ML_LANE1P ML_LANE1N GND3 ML_LANE2P ML_LANE2N RETURN

514-0876

TBTBCONN_1_C MIN LINE WIDTH=0.38 MM MIN NECK WIDTH=0.20 MM VOLTAGE=18.9V (0-18.9V)

C3305 0.01UF 10% 25V X5R-CERM 0201

TBTBCONN_7_C MIN LINE WIDTH=0.38 MM MIN NECK WIDTH=0.20 MM VOLTAGE=18.9V (0-18.9V)

C3306 0.01UF 10% 25V X5R-CERM 0201

DP Dir TBT Dir

TBT_B_R2D_P<0> TBT_B_R2D_N<0>

TBT: TX_0

DP_B_LSX_ML_P<1> DP_B_LSX_ML_N<1>

TBT: LSX_R2P/P2R (P/N)

GND_VOID-TRUE (Both C's)

C3370 0.22UF 20% 6.3V X5R 0201 TBT_B_R2D_C_P<0>

C3371 0.22UF 20% 6.3V X5R 0201 TBT_B_R2D_C_N<0>

R3370 470K 5% 1/20W MF 201; R3371 470K 5% 1/20W MF 201

TBT_B_R2D_P<1> TBT_B_R2D_N<1>

TBT: TX_1

GND_VOID-TRUE (Both C's)

C3372 0.22UF 20% 6.3V X5R 0201 TBT_B_R2D_C_P<1>

C3373 0.22UF 20% 6.3V X5R 0201 TBT_B_R2D_C_N<1>

R3372 470K 5% 1/20W MF 201; R3373 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

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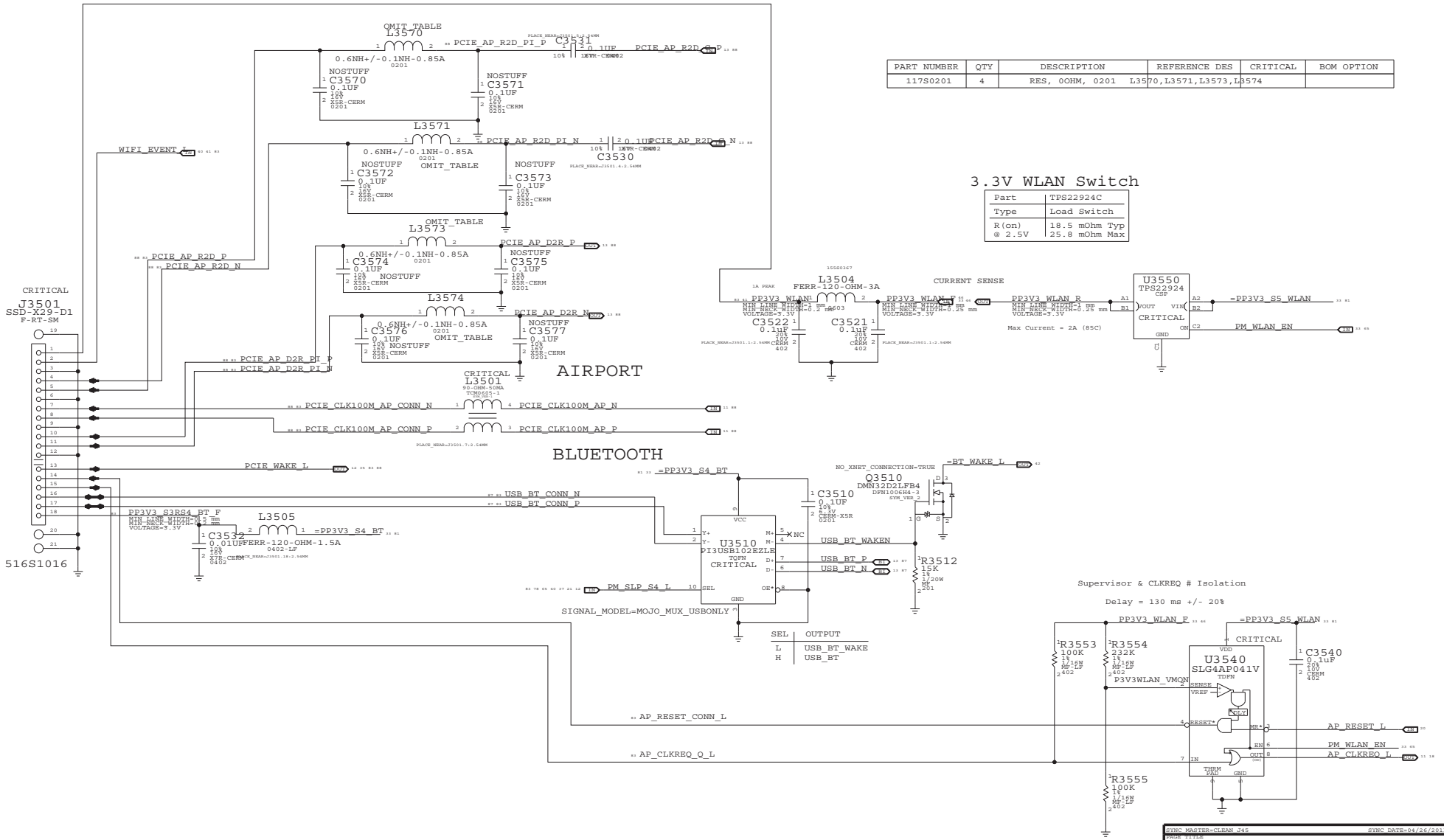

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 0OHM, 0201	L3570,L3571,L3573,L3574		

SYNC MASTER-CLEAN J45 SYNC DATE-04/26/2013

PAGE TITLE: X29C CONNECTOR

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REVISION: 6.0.0

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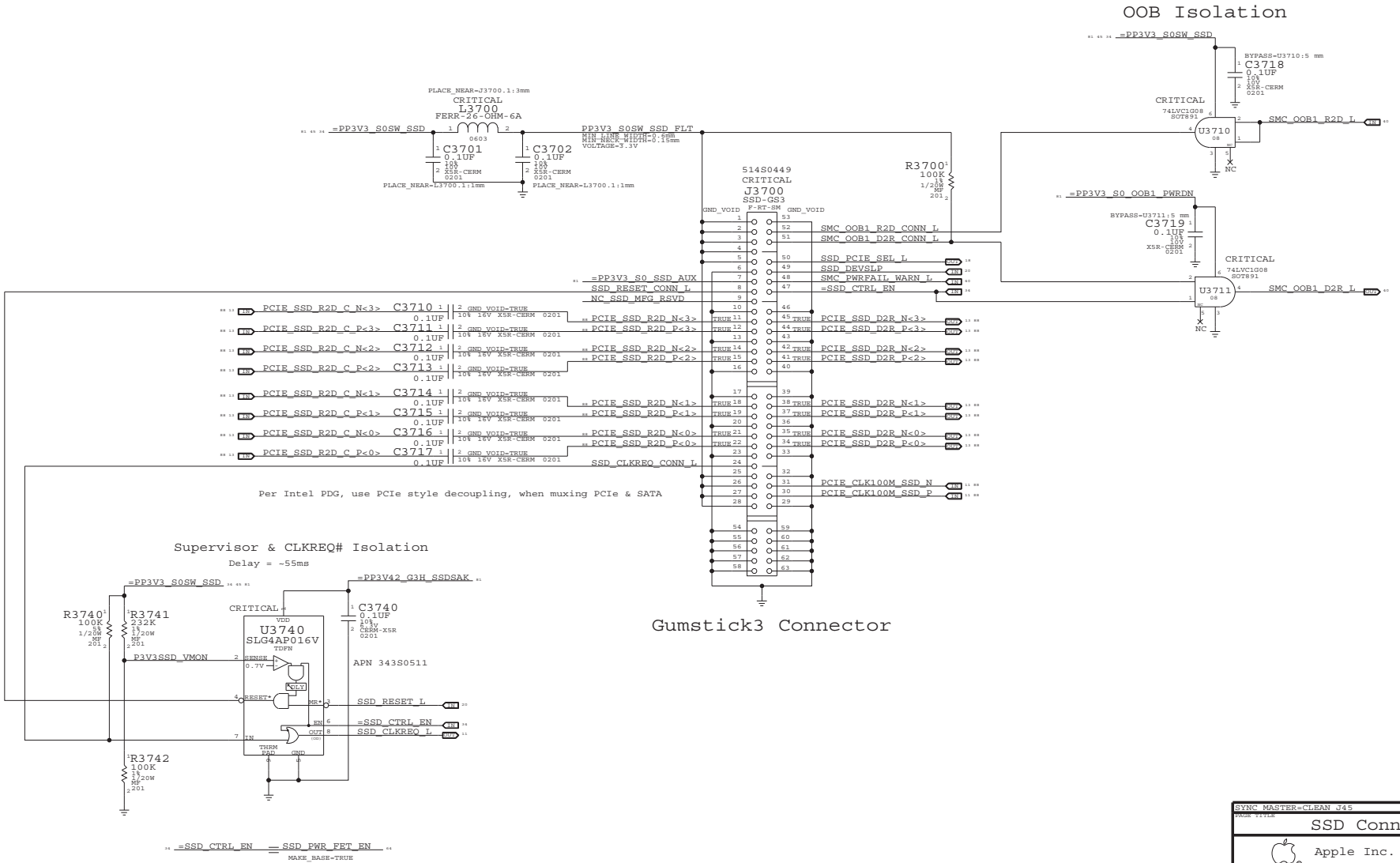

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PAGE TITLE

SSD Connector

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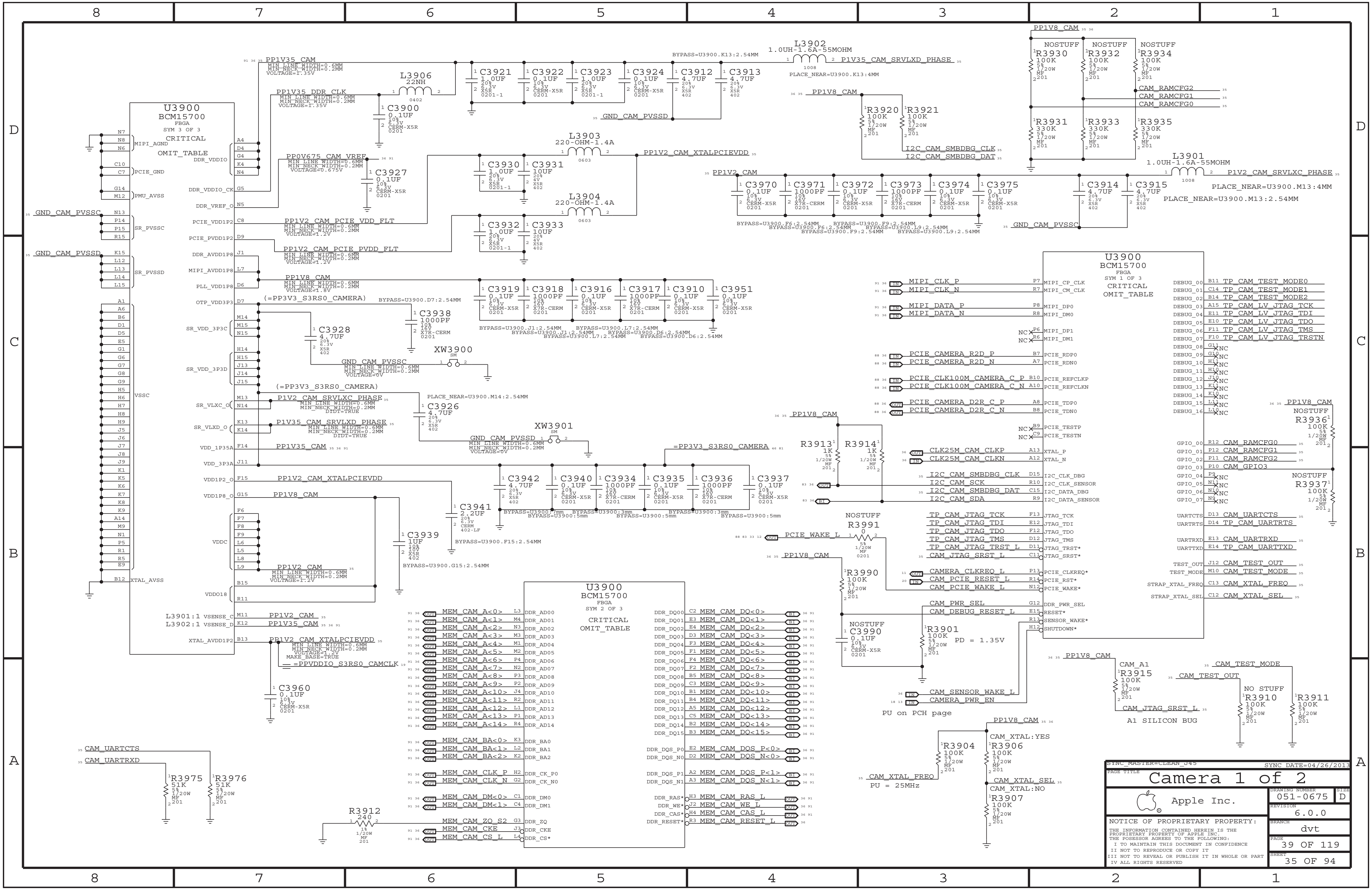

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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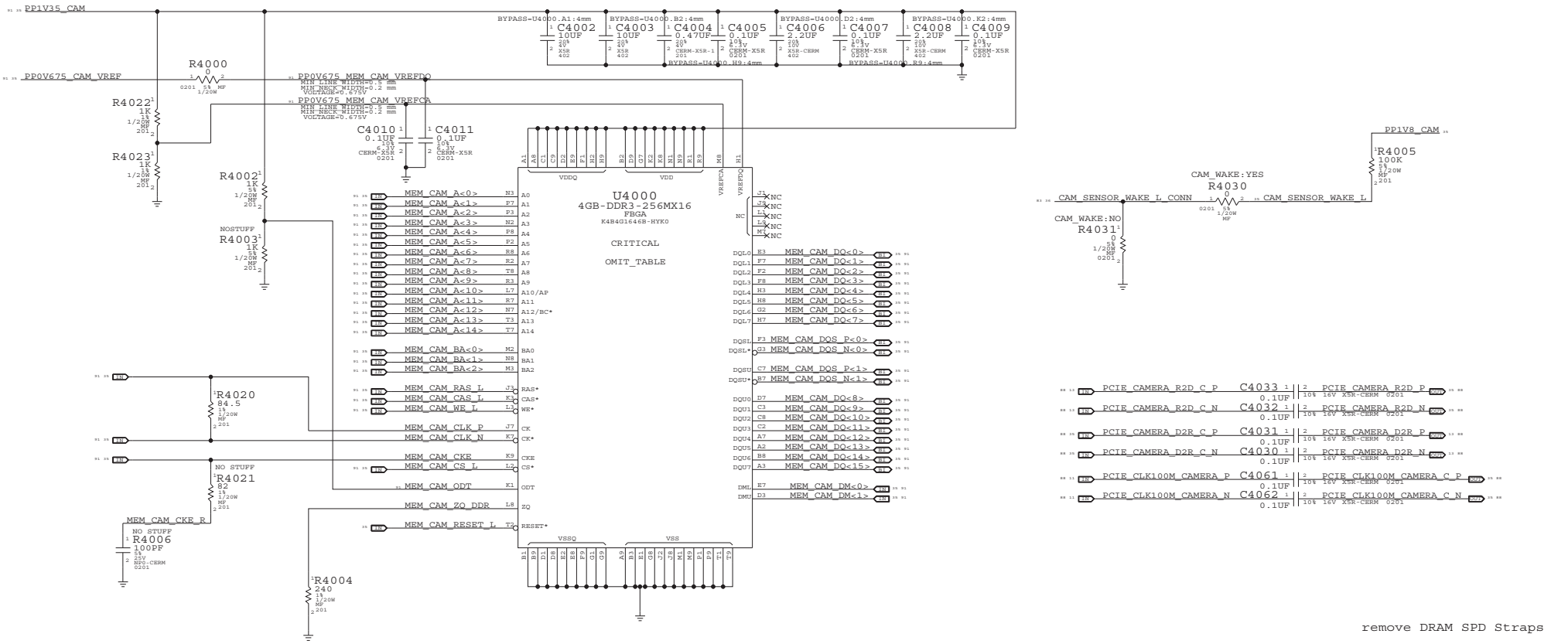
PP1V35_CAM
PP0V675_CAM_VREF
R4000
PP0V675_MEM_CAM_VREFDQ
PP0V675_MEM_CAM_VREFCA
R4022
R4023
R4002
R4003
NOSTUFF
C4010
C4011
C4002
C4003
C4004
C4005
C4006
C4007
C4008
C4009
U4000
4GB-DDR3-256MX16
FBGA
K4B4G1646B-HYK0
CRITICAL
OMIT_TABLE
MEM_CAM_A<0>
MEM_CAM_A<1>
MEM_CAM_A<2>
MEM_CAM_A<3>
MEM_CAM_A<4>
MEM_CAM_A<5>
MEM_CAM_A<6>
MEM_CAM_A<7>
MEM_CAM_A<8>
MEM_CAM_A<9>
MEM_CAM_A<10>
MEM_CAM_A<11>
MEM_CAM_A<12>
MEM_CAM_A<13>
MEM_CAM_A<14>
MEM_CAM_BA<0>
MEM_CAM_BA<1>
MEM_CAM_BA<2>
MEM_CAM_RAS_L
MEM_CAM_CAS_L
MEM_CAM_WE_L
MEM_CAM_CLK_P
MEM_CAM_CLK_N
MEM_CAM_CKE
MEM_CAM_CS_L
MEM_CAM_ODT
MEM_CAM_ZQ_DDR
MEM_CAM_RESET_L
MEM_CAM_DQ<0>
MEM_CAM_DQ<1>
MEM_CAM_DQ<2>
MEM_CAM_DQ<3>
MEM_CAM_DQ<4>
MEM_CAM_DQ<5>
MEM_CAM_DQ<6>
MEM_CAM_DQ<7>
MEM_CAM_DQS_P<0>
MEM_CAM_DQS_N<0>
MEM_CAM_DQS_P<1>
MEM_CAM_DQS_N<1>
MEM_CAM_DQ<8>
MEM_CAM_DQ<9>
MEM_CAM_DQ<10>
MEM_CAM_DQ<11>
MEM_CAM_DQ<12>
MEM_CAM_DQ<13>
MEM_CAM_DQ<14>
MEM_CAM_DQ<15>
MEM_CAM_DM<0>
MEM_CAM_DM<1>
R4020
R4021
R4006
R4004
MEM_CAM_CKE_R
PP1V8_CAM
R4005
CAM_WAKE:YES
R4030
CAM_WAKE:NO
R4031
CAM_SENSOR_WAKE_L_CONN
CAM_SENSOR_WAKE_L
PCIE_CAMERA_R2D_C_P
PCIE_CAMERA_R2D_C_N
PCIE_CAMERA_D2R_C_P
PCIE_CAMERA_D2R_C_N
PCIE_CLK100M_CAMERA_P
PCIE_CLK100M_CAMERA_N
C4033
C4032
C4031
C4030
C4061
C4062
remove DRAM SPD Straps
CAMERA SENSOR
J4002
CCR20-AK7100-1
MIPI_CLK_CONN_N
MIPI_CLK_CONN_P
CAM_SENSOR_WAKE_L_CONN
MIPI_DATA_CONN_N
MIPI_DATA_CONN_P
=I2C_ALS_SDA
=I2C_ALS_SCL
I2C_CAM_SCK
I2C_CAM_SDA
PP5V_S3RS0_ALSCAM_P
ALS
518S0892
L4009
L4007
L4010
L4011
MIPI_CLK_N
MIPI_CLK_P
MIPI_DATA_N
MIPI_DATA_P
=PP5V_S0_ALSCAM
=PP5V_S3_ALSCAM
C4013
77.2 mA nominal max
96.2 mA peak
SYSCLK_CLK25M_CAMERA
CLK25M_CAM_CLKP
C4015
C4014
Y4000
25.000MHZ-20PPM-12PF-85C
CLK25M_CAM_XTALP
CLK25M_CAM_XTALN
CLK25M_CAM_XTALP_R
R4007
R4008
R4009
R4012
R4010
CLK25M_CAM_CLKN
C4016
NOTE: TBD PPM crystal required
NO STUFF
DRAM CFG Chart
VENDOR
CFG 1
CFG 0
HYNIX
SAMSUNG
MICRON
ELPIDA
DIE REV
CFG 2
A
B
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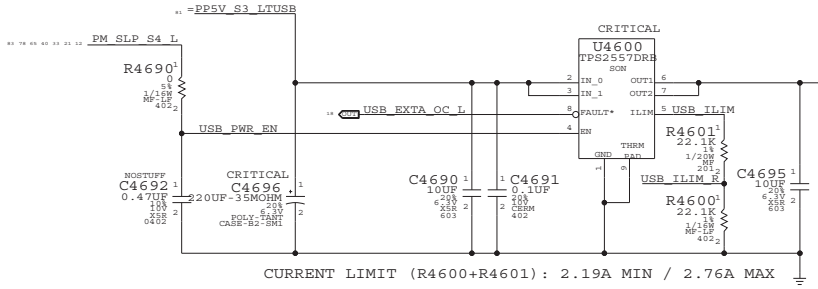
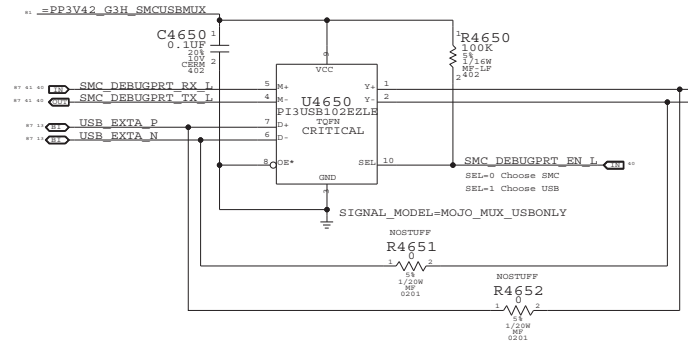
USB Port Power Switch



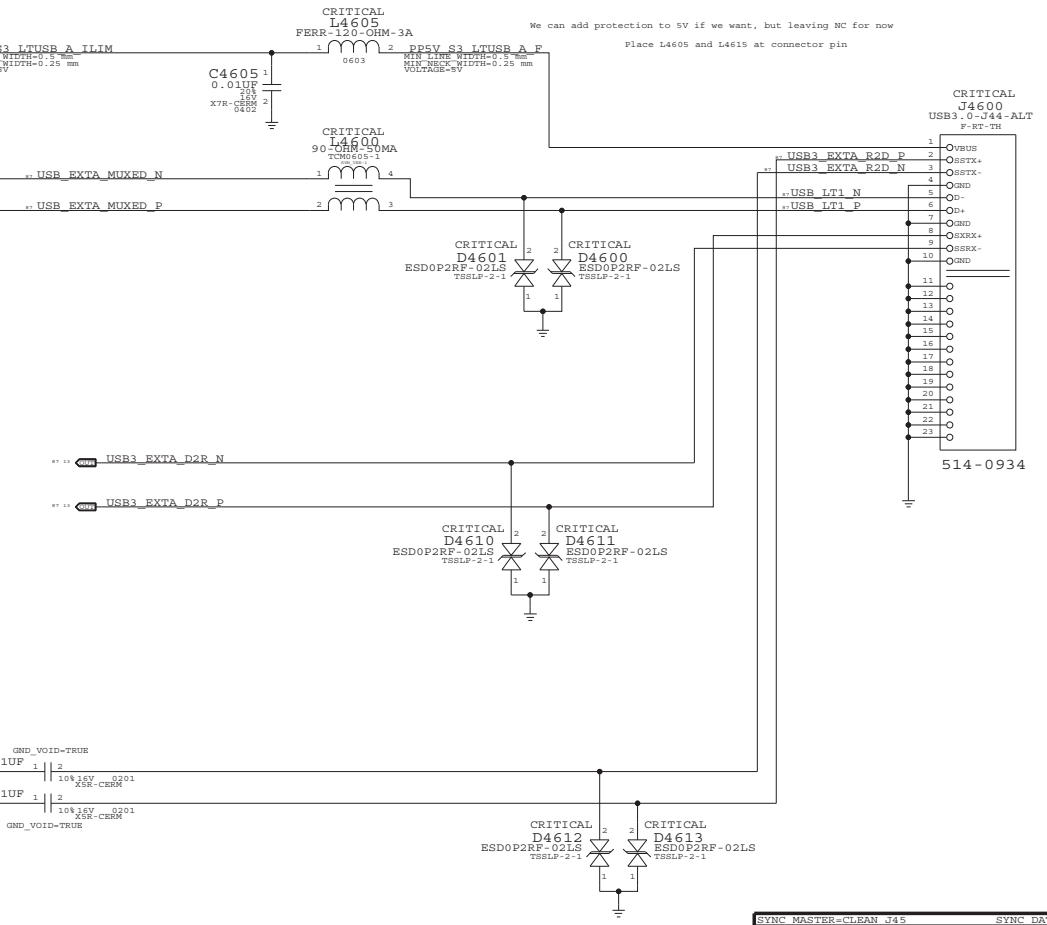
USB/SMC Debug Mux



Left USB Port A

We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

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USB 3.0 CONNECTORS

Apple Inc.

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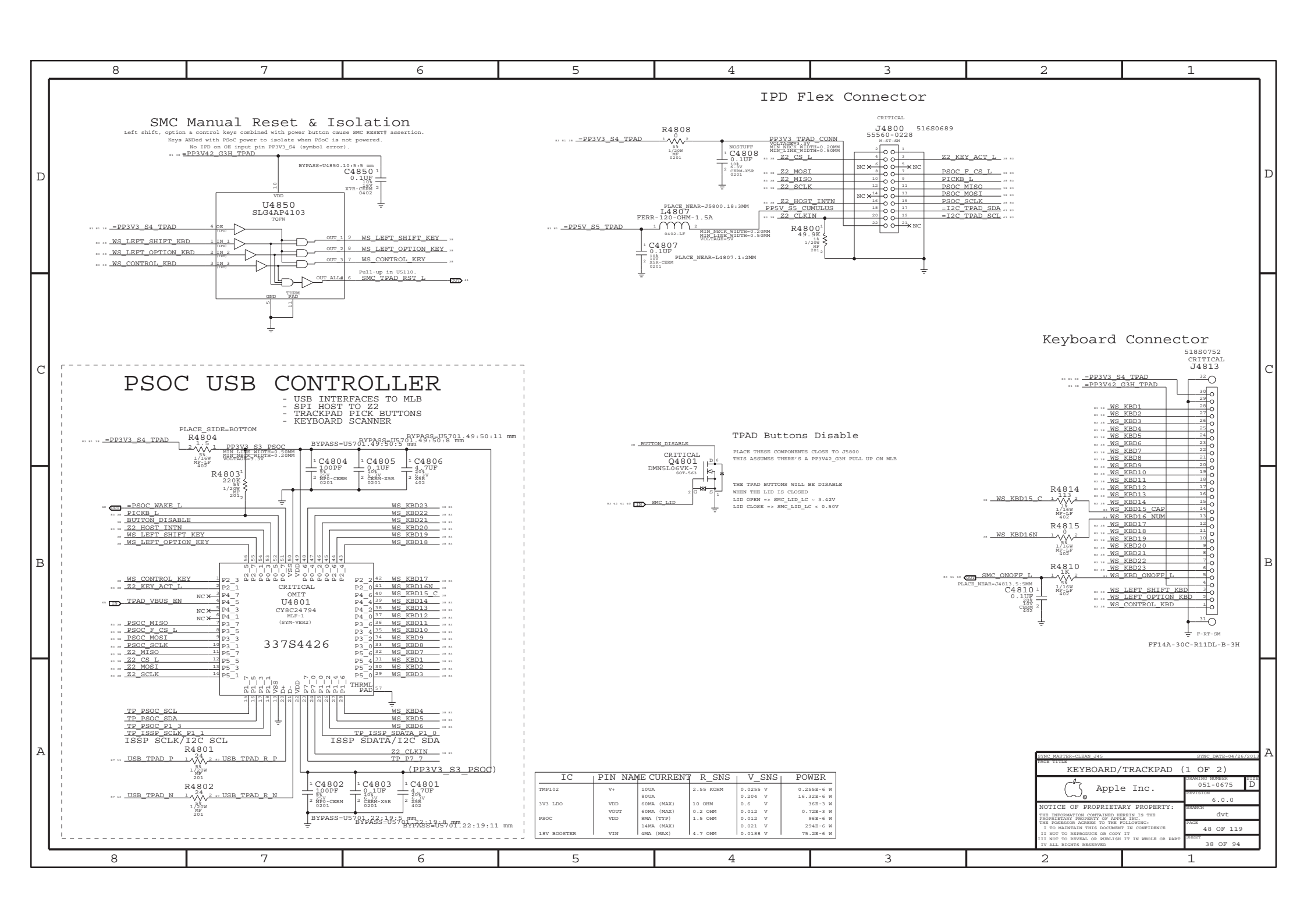
SMC Manual Reset & Isolation
Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).
=PP3V42_G3H_TPAD
BYPASS=U4850.10:5:5 mm
C4850 0.1UF 10% 16V X7R-CERM 0402
U4850
SLG4AP4103
TQFN
=PP3V3_S4_TPAD
WS_LEFT_SHIFT_KBD
WS_LEFT_OPTION_KBD
WS_CONTROL_KBD
WS_LEFT_SHIFT_KEY
WS_LEFT_OPTION_KEY
WS_CONTROL_KEY
Pull-up in U5110.
SMC_TPAD_RST_L
IPD Flex Connector
CRITICAL
J4800 516S0689
55560-0228
M-ST-SM
R4808 0 1/20W MF 0201
PP3V3_TPAD_CONN
C4808 0.1UF 10% 16V CERM-X5R 0201
Z2_CS_L
Z2_MOSI
Z2_MISO
Z2_SCLK
Z2_HOST_INTN
PP5V_S5_CUMULUS
Z2_CLKIN
Z2_KEY_ACT_L
PSOC_F_CS_L
PICKB_L
PSOC_MISO
PSOC_MOSI
PSOC_SCLK
=I2C_TPAD_SDA
=I2C_TPAD_SCL
PLACE_NEAR=J5800.18:3MM
L4807 FERR-120-OHM-1.5A 0402-LF
=PP5V_S5_TPAD
C4807 0.1UF 10% 16V X5R-CERM 0201
PLACE_NEAR=L4807.1:2MM
R4800 49.9K 1% 1/20W MF 201
PSOC USB CONTROLLER
- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER
PLACE_SIDE=BOTTOM
R4804 1.5 1/16W MF-LF 402
PP3V3_S3_PSOC
R4803 220K 1% 1/20W MF 201
C4804 100PF 5% 25V NP0-CERM 0201
C4805 0.1UF 10% 6.3V X5R-CERM 0201
C4806 4.7UF 20% 6.3V X5R 402
=PSOC_WAKE_L
PICKB_L
BUTTON_DISABLE
Z2_HOST_INTN
WS_LEFT_SHIFT_KEY
WS_LEFT_OPTION_KEY
WS_CONTROL_KEY
Z2_KEY_ACT_L
TPAD_VBUS_EN
PSOC_MISO
PSOC_F_CS_L
PSOC_MOSI
PSOC_SCLK
Z2_MISO
Z2_CS_L
Z2_MOSI
Z2_SCLK
CRITICAL
OMIT
U4801
CY8C24794
MLF-1
(SYM-VER2)
337S4426
THRML PAD
WS_KBD23
WS_KBD22
WS_KBD21
WS_KBD20
WS_KBD19
WS_KBD18
WS_KBD17
WS_KBD16N
WS_KBD15_C
WS_KBD14
WS_KBD13
WS_KBD12
WS_KBD11
WS_KBD10
WS_KBD9
WS_KBD8
WS_KBD7
WS_KBD1
WS_KBD2
WS_KBD3
WS_KBD4
WS_KBD5
WS_KBD6
TP_PSOC_SCL
TP_PSOC_SDA
TP_PSOC_P1_3
TP_ISSP_SCLK_P1_1
ISSP SCLK/I2C SCL
TP_ISSP_SDATA_P1_0
ISSP SDATA/I2C SDA
Z2_CLKIN
TP_P7_7
R4801 24 1/16W MF 201
USB_TPAD_P
USB_TPAD_R_P
R4802 24 1/16W MF 201
USB_TPAD_N
USB_TPAD_R_N
(PP3V3_S3_PSOC)
C4802 100PF 5% 25V NP0-CERM 0201
C4803 0.1UF 10% 6.3V X5R-CERM 0201
C4801 4.7UF 20% 6.3V X5R 402
BYPASS=U5701.49:50:5 mm
BYPASS=U5701.49:50:8 mm
BYPASS=U5701.49:50:11 mm
BYPASS=U5701.22:19:8 mm
BYPASS=U5701.22:19:11 mm
TPAD Buttons Disable
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB
THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V
BUTTON_DISABLE
CRITICAL
Q4801
DMN5L06VK-7
SOT-563
SMC_LID
Keyboard Connector
518S0752
CRITICAL
J4813
=PP3V3_S4_TPAD
=PP3V42_G3H_TPAD
WS_KBD1
WS_KBD2
WS_KBD3
WS_KBD4
WS_KBD5
WS_KBD6
WS_KBD7
WS_KBD8
WS_KBD9
WS_KBD10
WS_KBD11
WS_KBD12
WS_KBD13
WS_KBD14
WS_KBD15_CAP
WS_KBD16_NUM
WS_KBD17
WS_KBD18
WS_KBD19
WS_KBD20
WS_KBD21
WS_KBD22
WS_KBD23
WS_KBD_ONOFF_L
WS_LEFT_SHIFT_KBD
WS_LEFT_OPTION_KBD
WS_CONTROL_KBD
R4814 113 1/16W MF-LF 402
WS_KBD15_C
R4815 0 1/16W MF-LF 402
WS_KBD16N
R4810 1K 1/16W MF-LF 402
SMC_ONOFF_L
PLACE_NEAR=J4813.5:5MM
C4810 0.1UF 20% 10V CERM 402
F-RT-SM
FF14A-30C-R11DL-B-3H
IC | PIN NAME | CURRENT | R_SNS | V_SNS | POWER
TMP102 | V+ | 10UA | 2.55 KOHM | 0.0255 V | 0.255E-6 W
 | | 80UA | | 0.204 V | 16.32E-6 W
3V3 LDO | VDD | 60MA (MAX) | 10 OHM | 0.6 V | 36E-3 W
 | VOUT | 60MA (MAX) | 0.2 OHM | 0.012 V | 0.72E-3 W
PSOC | VDD | 8MA (TYP) | 1.5 OHM | 0.012 V | 96E-6 W
 | | 14MA (MAX) | | 0.021 V | 294E-6 W
18V BOOSTER | VIN | 4MA (MAX) | 4.7 OHM | 0.0188 V | 75.2E-6 W
SYNC MASTER-CLEAN J45
SYNC DATE=04/26/2013
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KEYBOARD/TRACKPAD (1 OF 2)
Apple Inc.
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SIZE D
REVISION 6.0.0
BRANCH dvt
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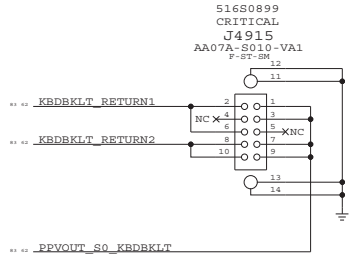
Keyboard Backlight Connector



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

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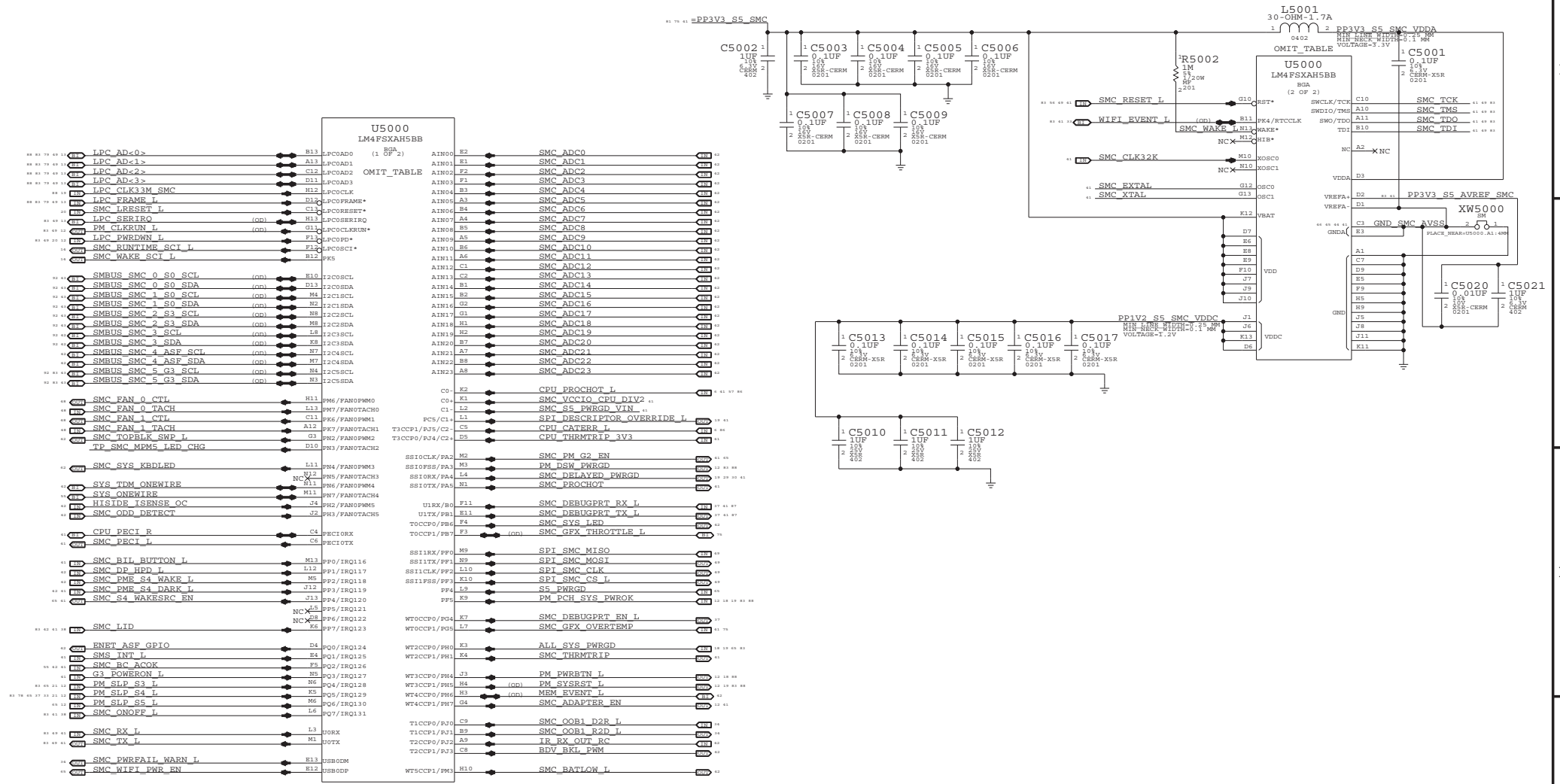
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

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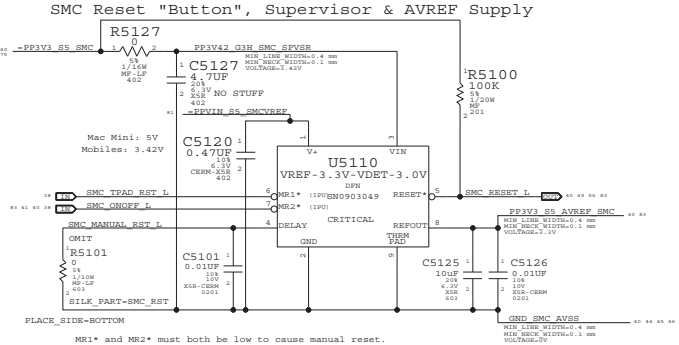
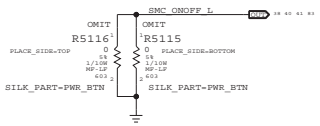
SMC Reset "Button", Supervisor & AVREF Supply



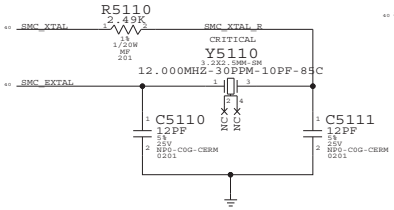
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

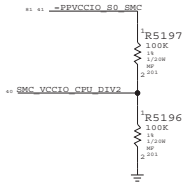
Debug Power "Buttons"



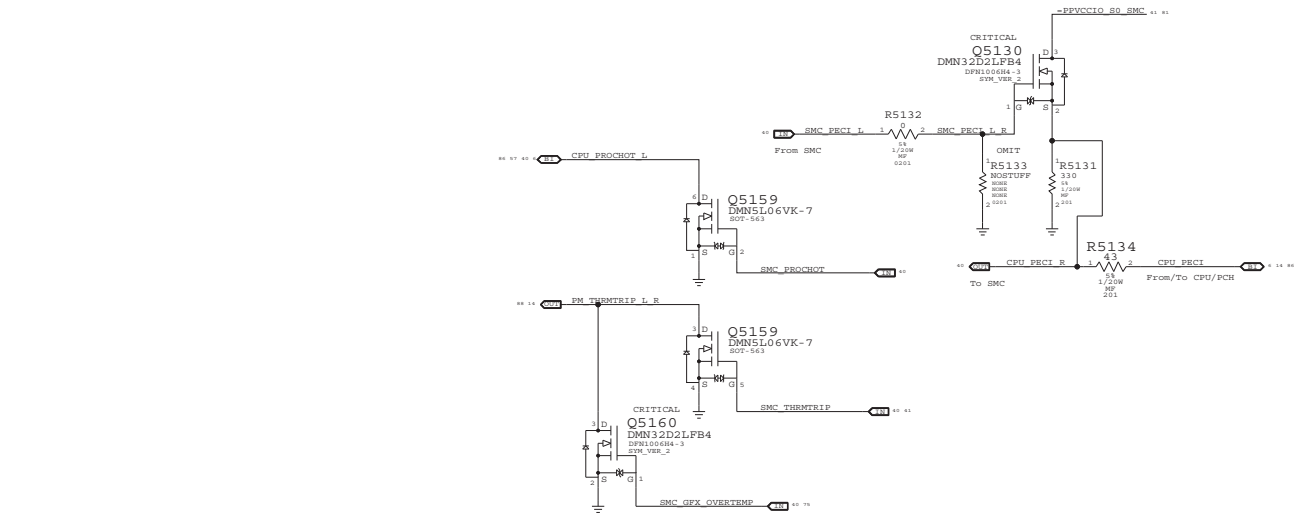
SMC Crystal Circuit

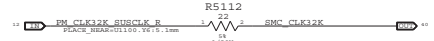


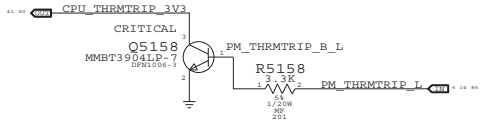
SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

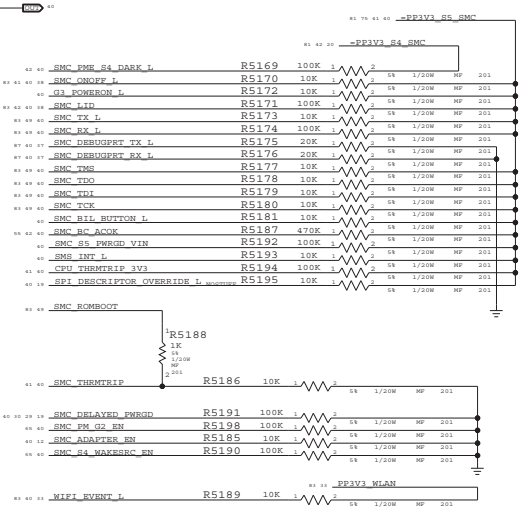


SMC12 PECI SUPPORT









SYNC MASTER=CLEAN_J45 SYNC DATE=04/26/2013

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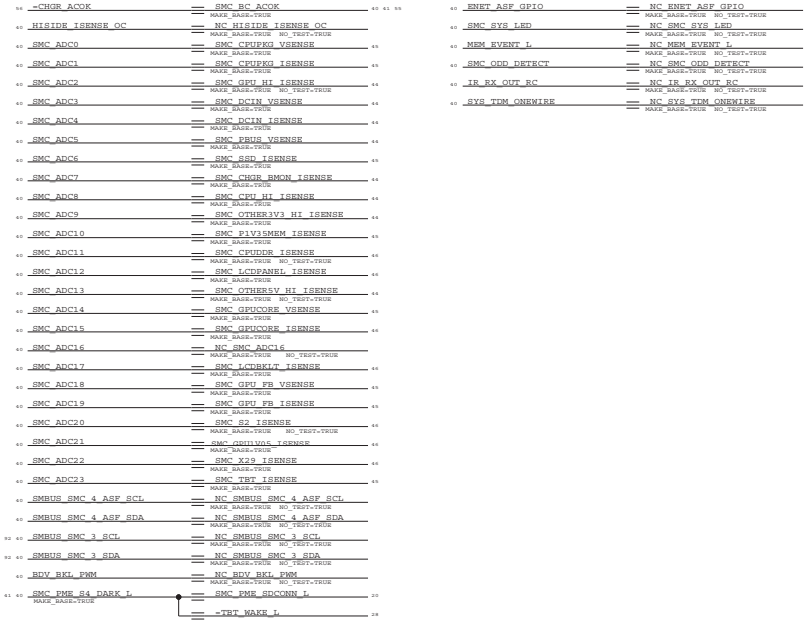
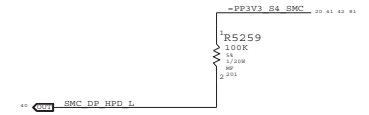
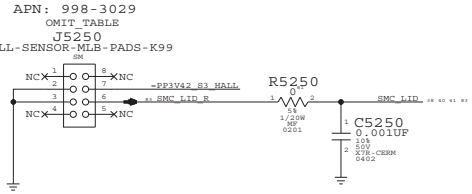


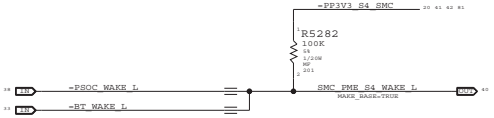
Spare S4 IRQ

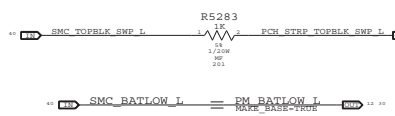


Hall Effect pads



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	





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PCH SMBus "0" Connections

=PP3V3_S0_SMBUS_PCH

R5300 1K 5% 1/16W MF-LF 402
R5301 1K 5% 1/16W MF-LF 402

Lynx Point
U1100
(MASTER)
SMBUS_PCH_CLK — MAKE_BASE=TRUE
SMBUS_PCH_DATA — MAKE_BASE=TRUE

VRef DACs
U2200
(Write: 0x98 Read: 0x99)
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA

Margin Control
U2201
(Write: 0x30 Read: 0x31)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA

XDP Connectors
J1800 & J1850
(MASTER)
=SMBUS_XDP_SCL
=SMBUS_XDP_SDA

R5390 0 5% 1/16W MF-LF 402
R5391 0 5% 1/16W MF-LF 402

HDMI Redriver (on RIO)
J9510 -> U9700
(WRITE: 0xCC READ: 0xCD)
I2C_HDMIRDRV_SCL
I2C_HDMIRDRV_SDA

NO STUFF
R5392 0 5% 1/16W MF-LF 402
R5393 0 5% 1/16W MF-LF 402

HDMI Redriver (on RIO)
J9510 -> U9700
(WRITE: 0xCC READ: 0xCD)
I2C_DPMUX_A_SCL
I2C_DPMUX_A_SDA
I2C_HDMIRDRV_SCL
I2C_HDMIRDRV_SDA

NO STUFF

PCH "SMLink 0" Connections

=PP3V3_S0_SMBUS_PCH

R5310 8.2K 5% 1/16W MF-LF 402
R5311 8.2K 5% 1/16W MF-LF 402

Lynx Point
U1100
(MASTER)
SML_PCH_0_CLK — MAKE_BASE=TRUE
SML_PCH_0_DATA — MAKE_BASE=TRUE

PCH "SMLink 1" Connections

=PP3V3_S0_SMBUS_PCH

NO STUFF
R5320 8.2K 5% 1/20W MF 201
NO STUFF
R5321 8.2K 5% 1/20W MF 201

R5323 0 5% 1/20W MF 0201
R5322 0 5% 1/20W MF 0201

Lynx Point
U1100
(Write: 0x88 Read: 0x89)
SML_PCH_1_CLK — MAKE_BASE=TRUE
SML_PCH_1_DATA — MAKE_BASE=TRUE

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

R5350 2.0K 5% 1/16W MF-LF 402
R5351 2.0K 5% 1/16W MF-LF 402

SMC
U5000
(MASTER)
SMB_0_S0_CLK — SMBUS_SMC_0_S0_SCL — MAKE_BASE=TRUE
SMB_0_S0_DATA — SMBUS_SMC_0_S0_SDA — MAKE_BASE=TRUE

L&R Fin Stack Temp
EMC1414-A: U5850
(Write: 0x98 Read: 0x99)
=SMBUS_GPUTHMSNS_SCL
=SMBUS_GPUTHMSNS_SDA

J4002
ALS
(Write: 0x72 Read: 0x73)
=I2C_ALS_SCL
=I2C_ALS_SDA

Need to check with SMC team

GPU Temp (Int)
GK107: U8400
(Write: 0x9E Read: 0x9F)
GPU_SMB_CLK_R
GPU_SMB_DAT_R

SMC "2" SMBUS CONNECTIONS

NOTE: SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_2_S3

R5370 1K 5% 1/20W MF 201
R5371 1K 5% 1/20W MF 201

SMC
U5000
(MASTER)
SMB_2_S3_CLK — SMBUS_SMC_2_S3_SCL — MAKE_BASE=TRUE
SMB_2_S3_DATA — SMBUS_SMC_2_S3_SDA — MAKE_BASE=TRUE

Trackpad
J4801
(Write: 0x90 Read: 0x91)
=I2C_TPAD_SCL
=I2C_TPAD_SDA

SMC "1" SMBUS CONNECTIONS

=PP3V3_S0_SMBUS_SMC_1_S0

R5360 1K 5% 1/20W MF 201
R5361 1K 5% 1/20W MF 201

SMC
U5000
(MASTER)
SMB_1_S0_CLK — SMBUS_SMC_1_S0_SCL — MAKE_BASE=TRUE
SMB_1_S0_DATA — SMBUS_SMC_1_S0_SDA — MAKE_BASE=TRUE

CPU/DDR3/PCH/AIRFLOW TEMP
EMC1414-A: U5870
(Write: 0x98 Read: 0x99)
=I2C_CPUTHMSNS_SCL
=I2C_CPUTHMSNS_SDA

X29 TEMP
TMP105: U5823
(WRITE: 0X92 READ: 0X93)
=I2C_X29THMSNS_SCL
=I2C_X29THMSNS_SDA

SMC "5" SMBUS CONNECTIONS

=PP3V42_G3H_SMBUS_SMC_5

R5380 2.0K 5% 1/20W MF 201
R5381 2.0K 5% 1/20W MF 201

SMC
U5000
(MASTER)
SMB_5_CLK — SMBUS_SMC_5_G3_SCL — MAKE_BASE=TRUE
SMB_5_DATA — SMBUS_SMC_5_G3_SDA — MAKE_BASE=TRUE

Battery Charger
ISL6258 - U7100
(Write: 0x12 Read: 0x13)
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA

Battery
J7050
(Write: 0x16 Read: 0x17)
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA

SMC "4" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

SMC "3" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

=PP3V3_S0_DPMUXI2C

R5336 4.7K 5% 1/16W MF-LF 402
R5337 4.7K 5% 1/16W MF-LF 402

DPMUX IC
U9100
(MASTER)
=I2C_DPMUX_A_SCL — I2C_DPMUX_A_SCL — MAKE_BASE=TRUE
=I2C_DPMUX_A_SDA — I2C_DPMUX_A_SDA — MAKE_BASE=TRUE

LED BACKLIGHT SMBUS CONNECTION

=PP3V3_S0_DPMUXI2C

R5334 4.7K 5% 1/20W MF 201
R5335 4.7K 5% 1/20W MF 201

DPMUX IC
U9100
(MASTER)
=I2C_DPMUX_UC_SCL — I2C_DPMUX_UC_SCL — MAKE_BASE=TRUE
=I2C_DPMUX_UC_SDA — I2C_DPMUX_UC_SDA — MAKE_BASE=TRUE

LED BACKLIGHT
U7100
(WRITE: 0x58 READ: 0x59)
=I2C_BKL_1_SCL
=I2C_BKL_1_SDA

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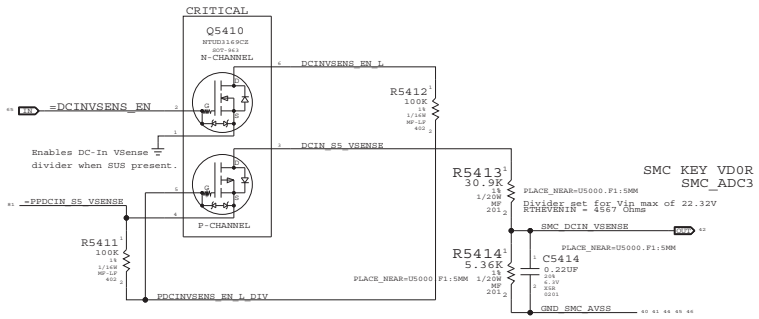
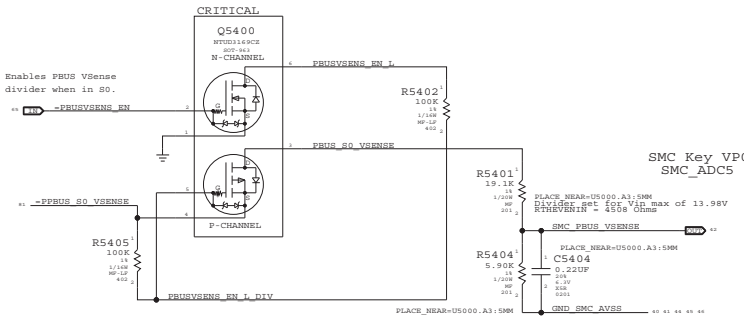
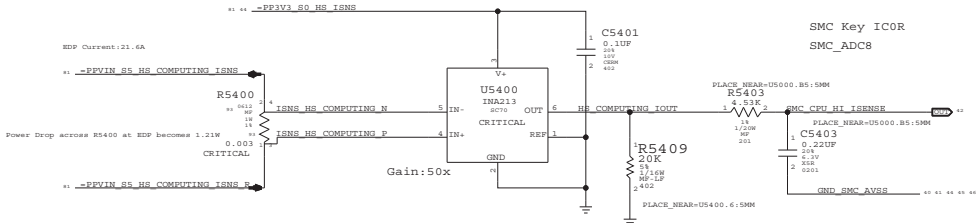
DC-In Voltage Sense Enable & Filter



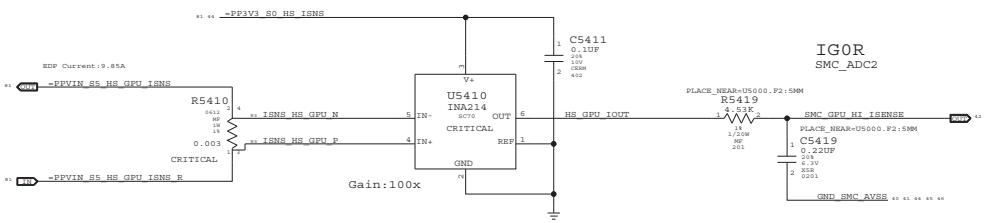
PBUS Voltage Sense Enable & Filter



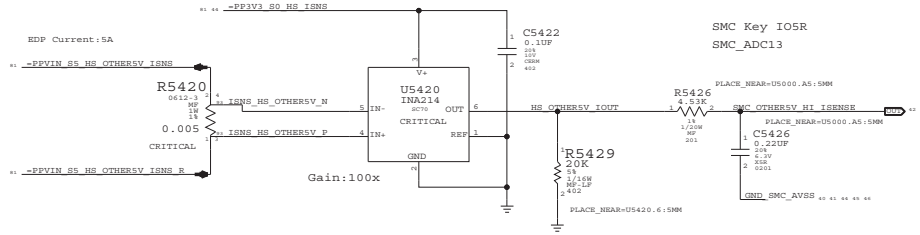
COMPUTING High Side Current Sense / Filter



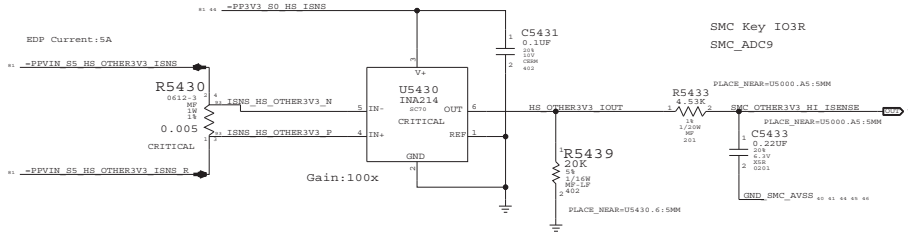
GRAPHICS High Side Current Sense / Filter



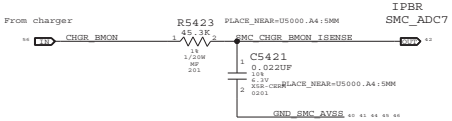
OTHERS (5V) High Side Current Sense / Filter



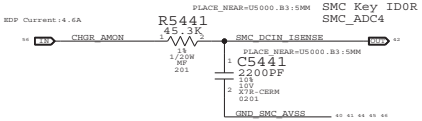
OTHERS (3.3V) High Side Current Sense / Filter



CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



SYNC MASTER=CLEAN_J45 SYNC DATE=04/26/2013

PAGE TITLE: High Side Voltage and Current Sensing

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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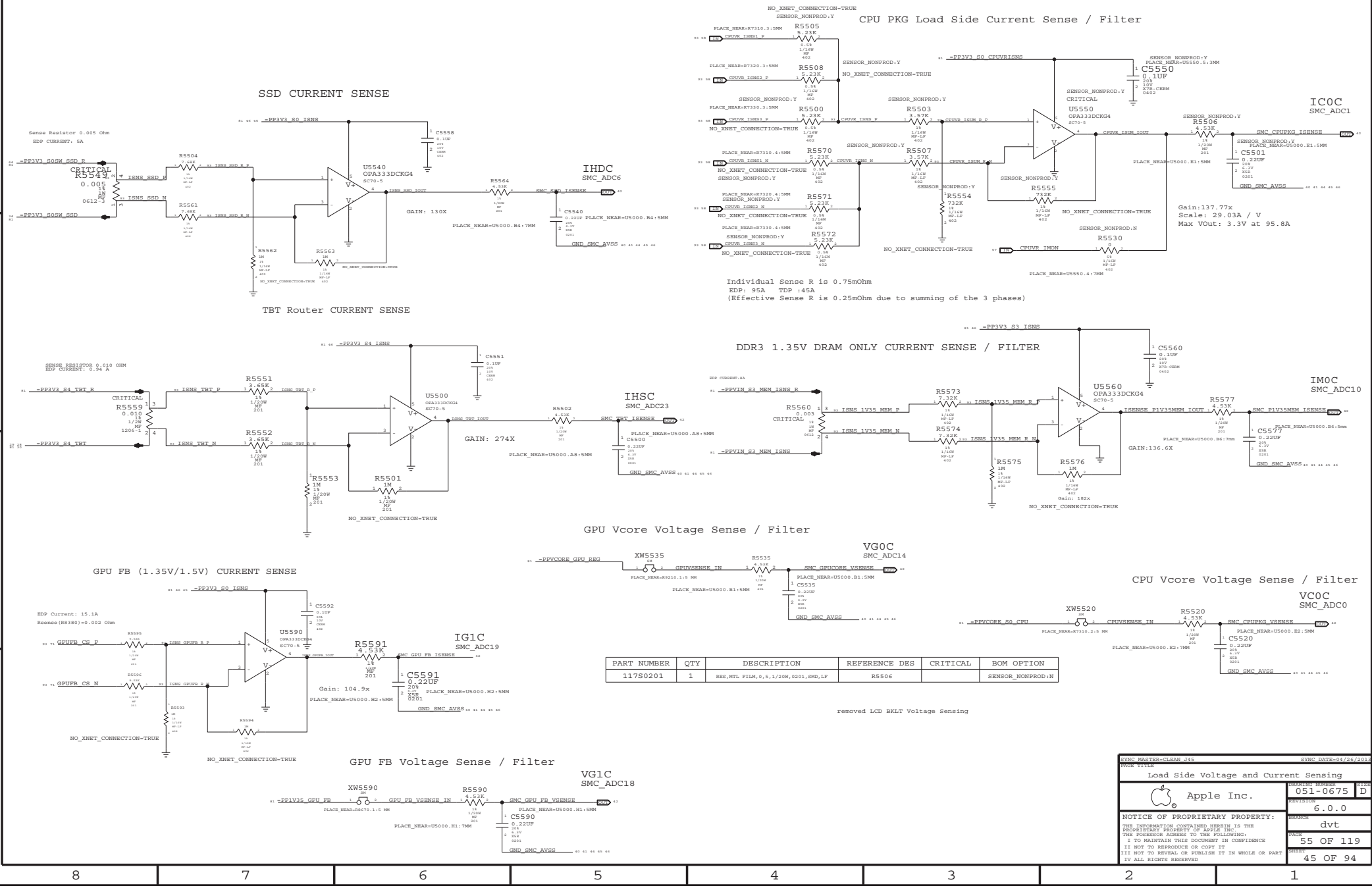

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	1	RES,MTL FILM,0,5,1/20W,0201,SMD,LF	R5506		SENSOR_NONPROD:N

removed LCD BKLT Voltage Sensing

SYNC MASTER-CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE: Load Side Voltage and Current Sensing

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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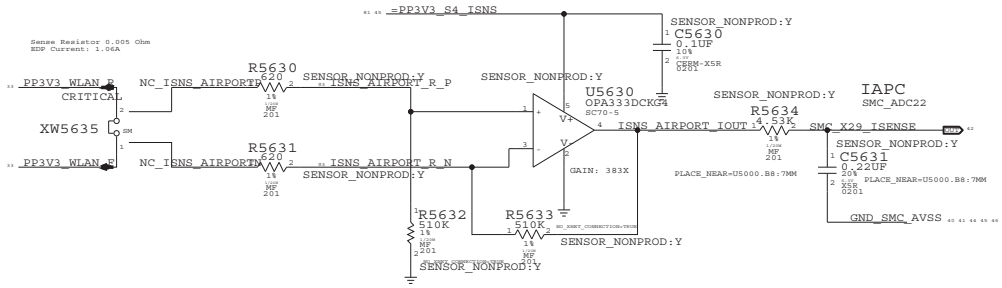
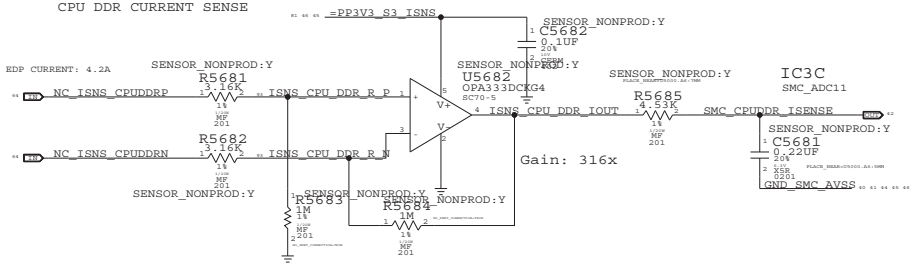
X29 AIRPORT CURRENT SENSE



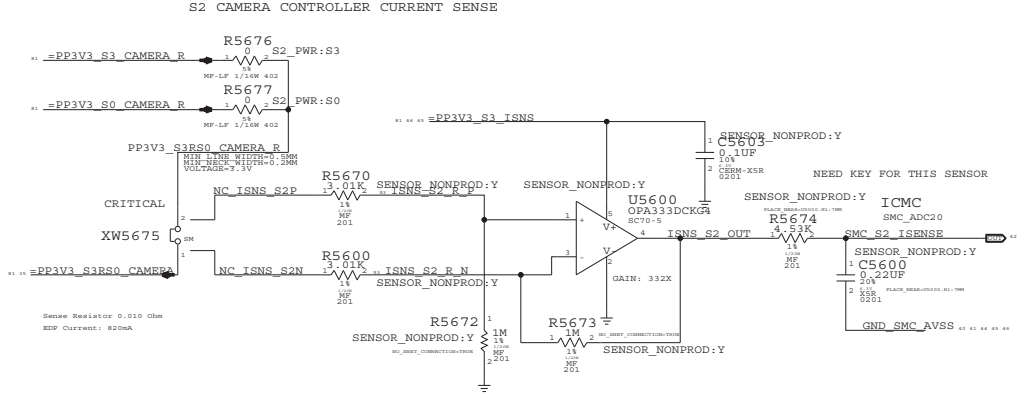
C5601,C5631,C5600,C5681,C5671,C5618,C5642

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	7	RES,MTL FILM,100K,5,1/20W,0201,SMD,LF			SENSOR_NONPROD:N

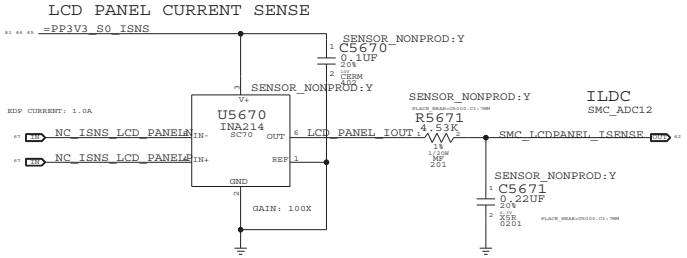
CPU DDR CURRENT SENSE



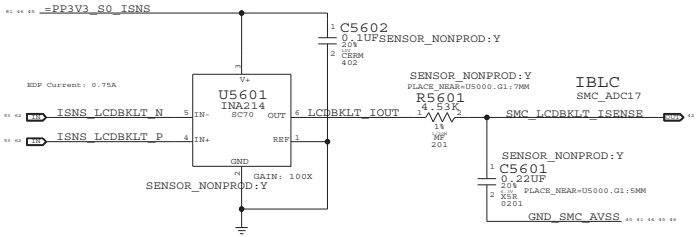
S2 CAMERA CONTROLLER CURRENT SENSE



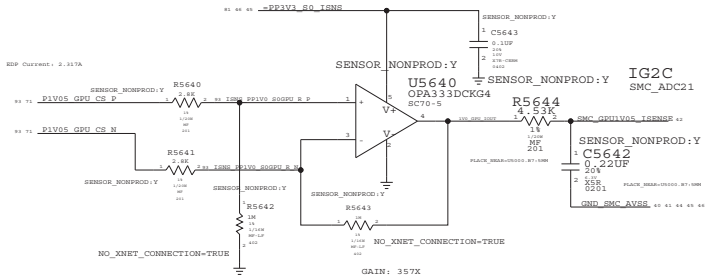
LCD PANEL CURRENT SENSE



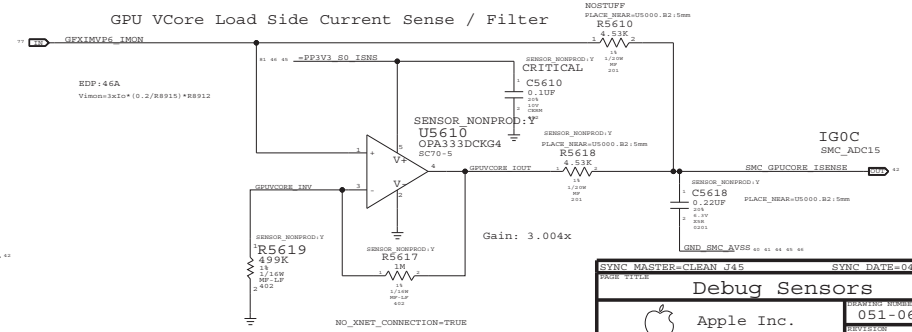
LCD BKLT Current Sense



GPU 1.05V CURRENT SENSE



GPU VCore Load Side Current Sense / Filter



SYNC MASTER=CLEAN_J45 SYNC DATE=04/26/2013

PAGE TITLE

Debug Sensors

Apple Inc.

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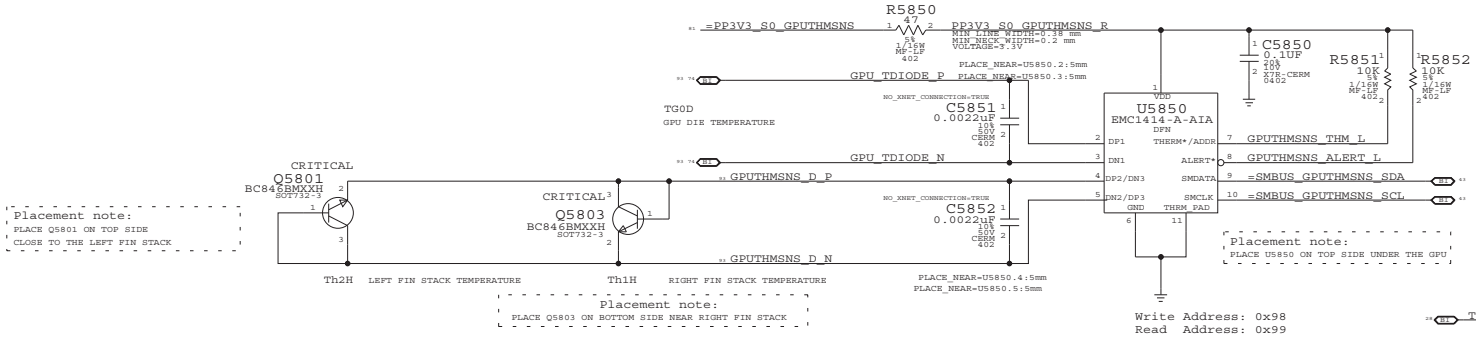
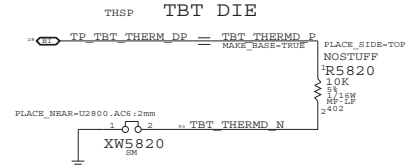
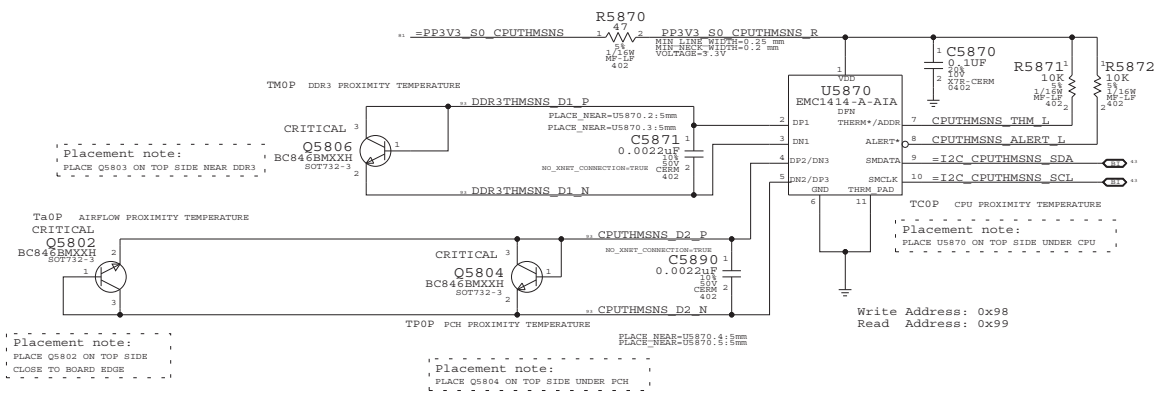
GPU PROXIMITY/GPU DIE/LEFT FIN STACK/RIGHT FIN STACK



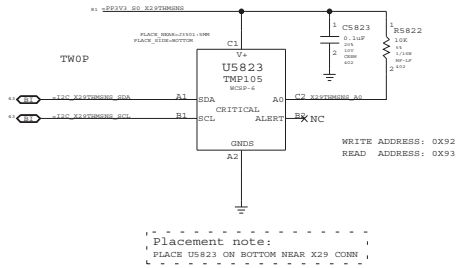
TBT DIE



DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY



X29 PROXIMITY



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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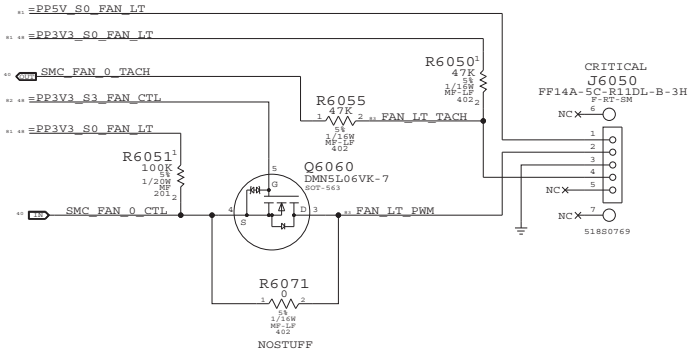
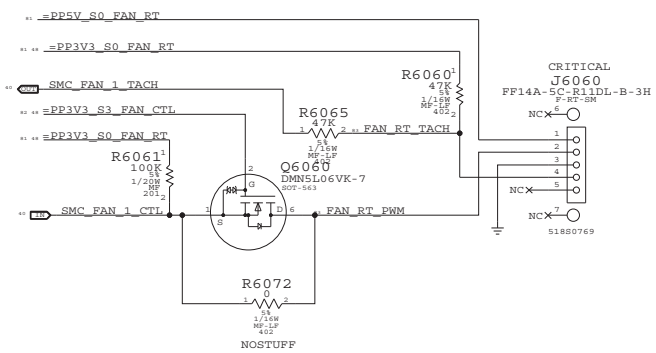
Left Fan



Right Fan



SYNC MASTER=CLEAN J45 SYNC DATE=06/23/2013

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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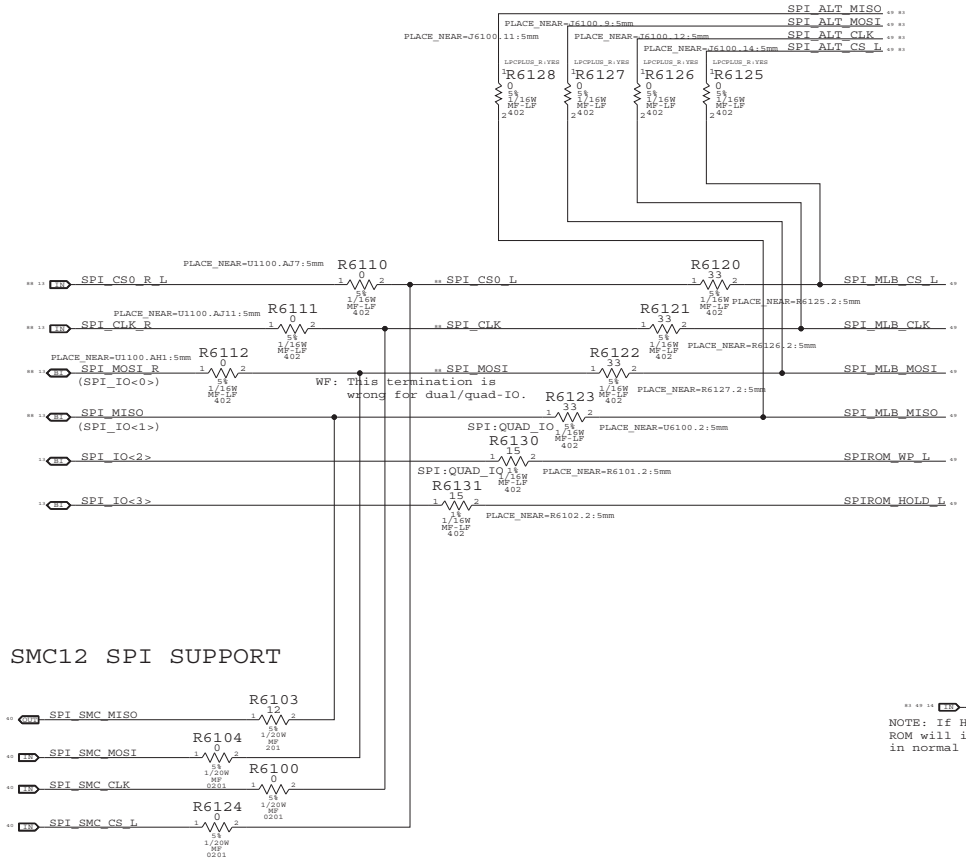
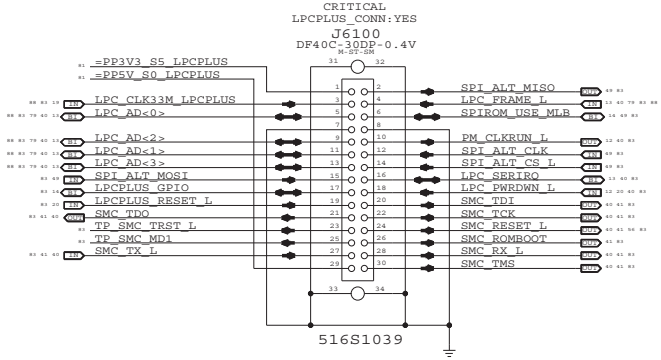
SPI Bus Series Termination

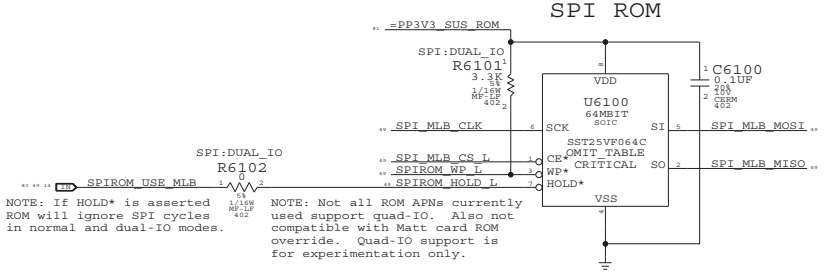


SMC12 SPI SUPPORT

LPC+SPI Connector



SPI ROM



NOTE: If HOLD* is asserted ROM will ignore SPI cycles in normal and dual-IO modes.

NOTE: Not all ROM APNs currently used support quad-IO. Also not compatible with Matt card ROM override. Quad-IO support is for experimentation only.

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE: SPI ROM / LPC+SPI Conn.

Apple Inc.

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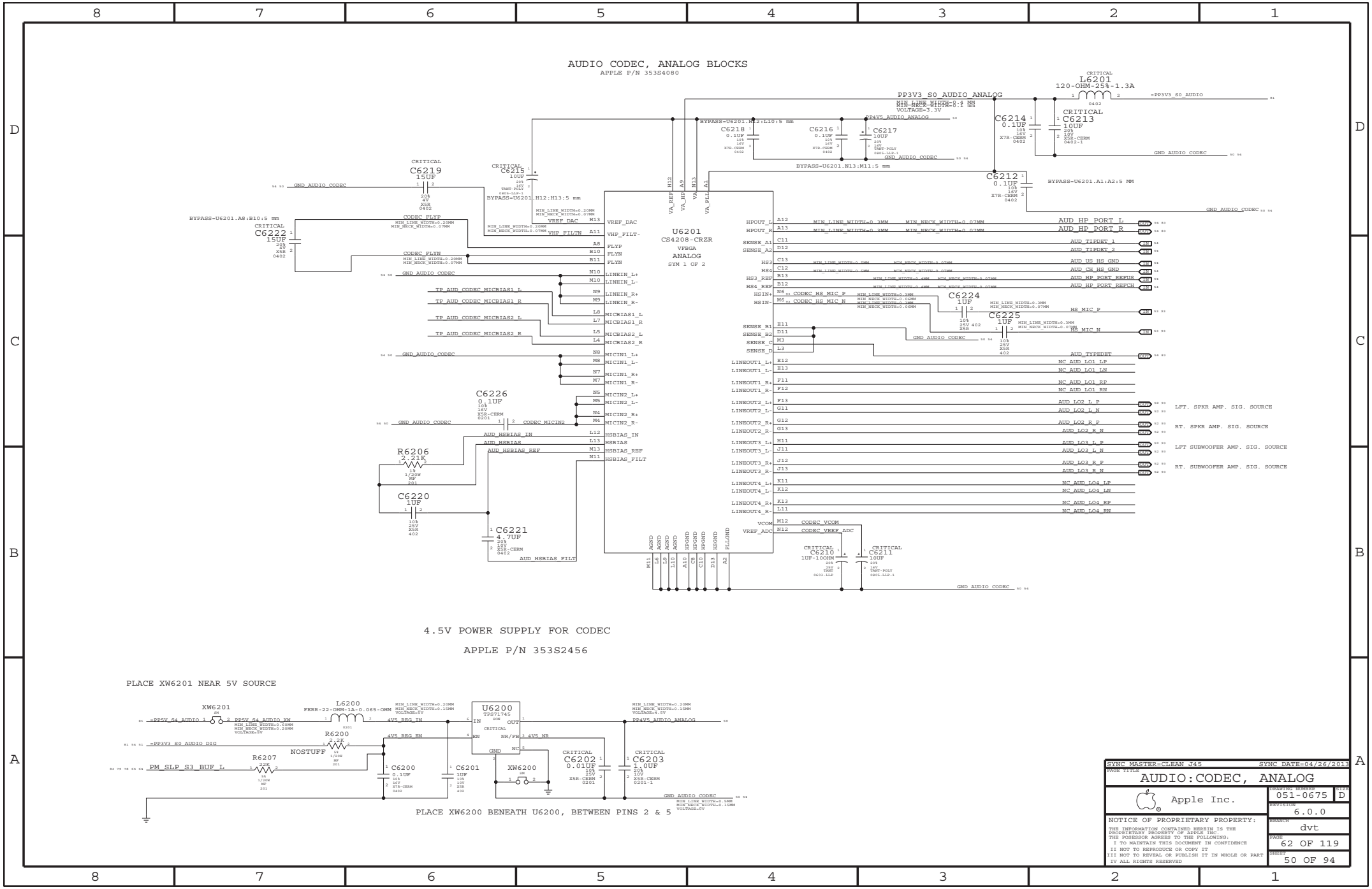
AUDIO CODEC, ANALOG BLOCKS
APPLE P/N 353S4080
U6201
CS4208-CRZR
VFBGA
ANALOG
SYM 1 OF 2
4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456
PLACE XW6201 NEAR 5V SOURCE
PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
AUDIO:CODEC, ANALOG
Apple Inc.
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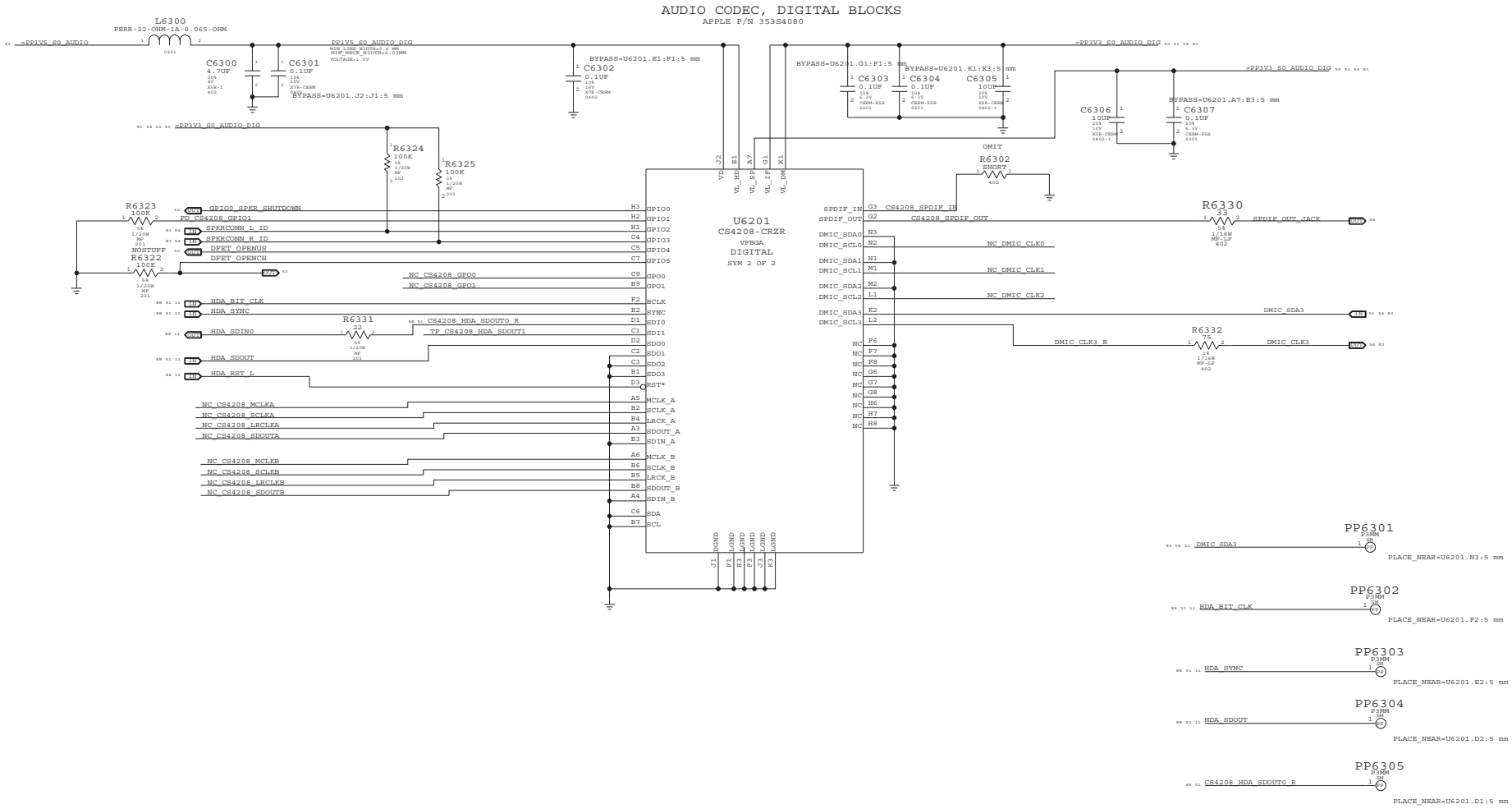

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE
AUDIO:CODEC, DIGITAL

Apple Inc.

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REVISION 6.0.0

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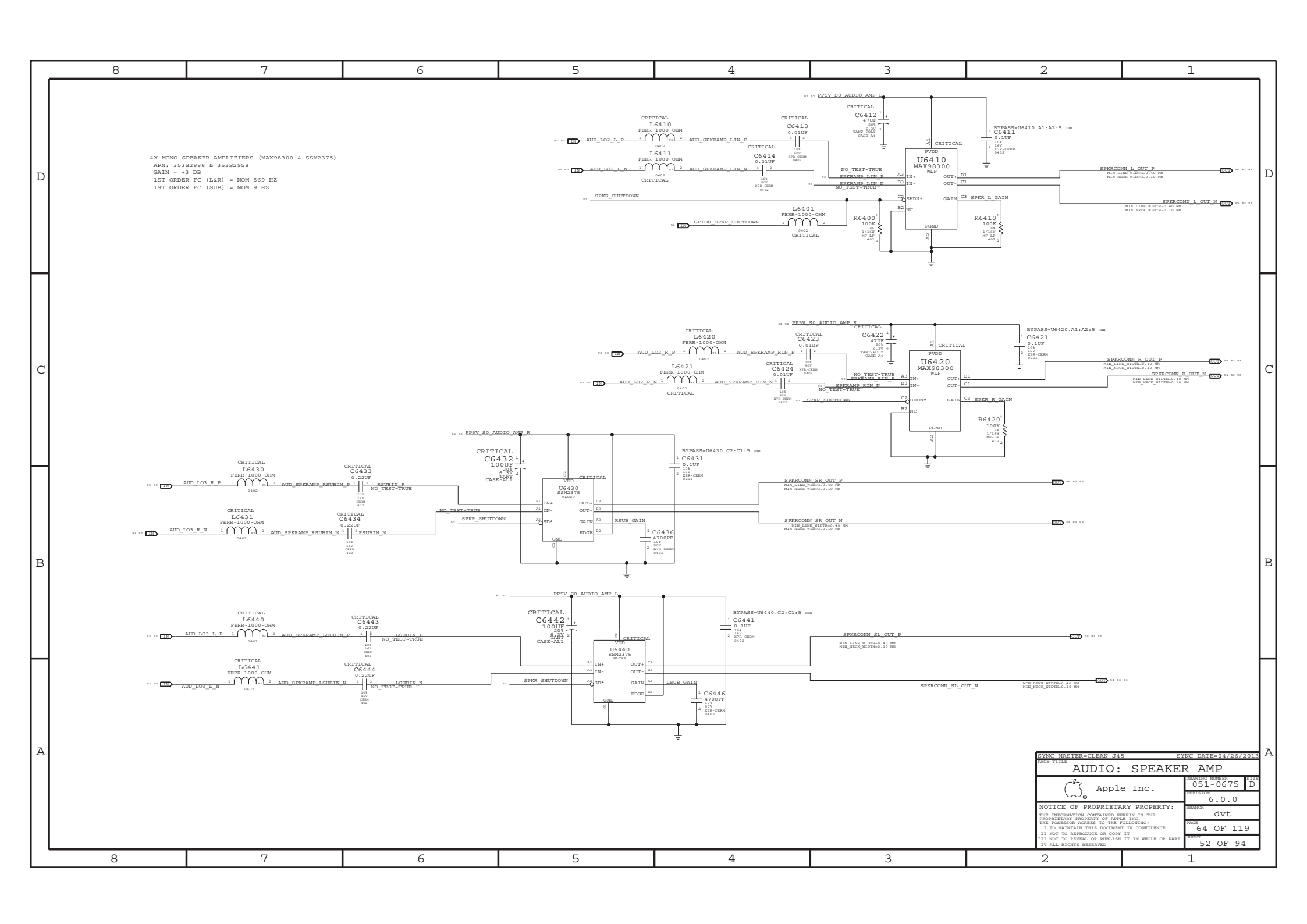
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ
PP5V_S0_AUDIO_AMP_L
PP5V_S0_AUDIO_AMP_R
U6410 MAX98300 WLP
U6420 MAX98300 WLP
U6430 SSM2375 WLCSP
U6440 SSM2375 WLCSP
AUD_LO2_L_P
AUD_LO2_L_N
AUD_LO2_R_P
AUD_LO2_R_N
AUD_LO3_R_P
AUD_LO3_R_N
AUD_LO3_L_P
AUD_LO3_L_N
SPKR_SHUTDOWN
GPIO0_SPKR_SHUTDOWN
NO_TEST=TRUE
SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
SPKRCONN_SR_OUT_P
SPKRCONN_SR_OUT_N
SPKRCONN_SL_OUT_P
SPKRCONN_SL_OUT_N
SYNC MASTER=CLEAN_J45
SYNC DATE=04/26/2013
PAGE TITLE
AUDIO: SPEAKER AMP
Apple Inc.
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REVISION 6.0.0
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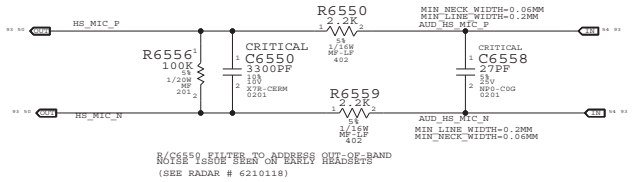

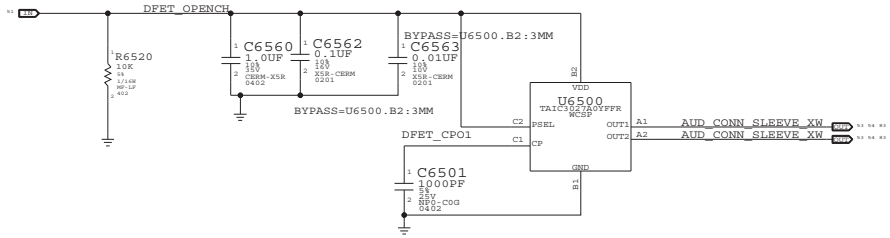

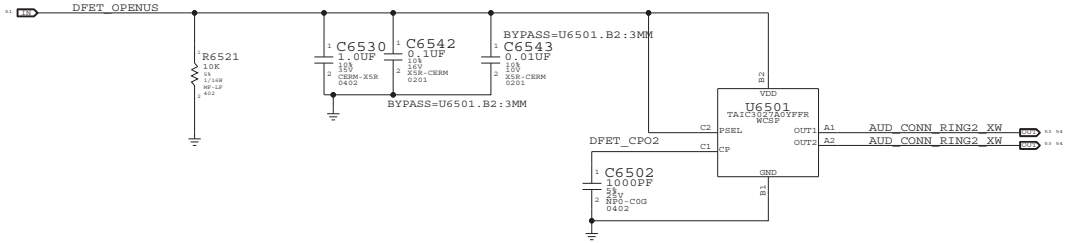

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

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AUDIO: JACK

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2	INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN

2-MIC CONNECTOR
APN: 518S0769

J6601
FF14A-5C-R11DL-B-3H
F-RT-SM

SPEAKER CONNECTOR HP=80HZ
APN: 518S0672

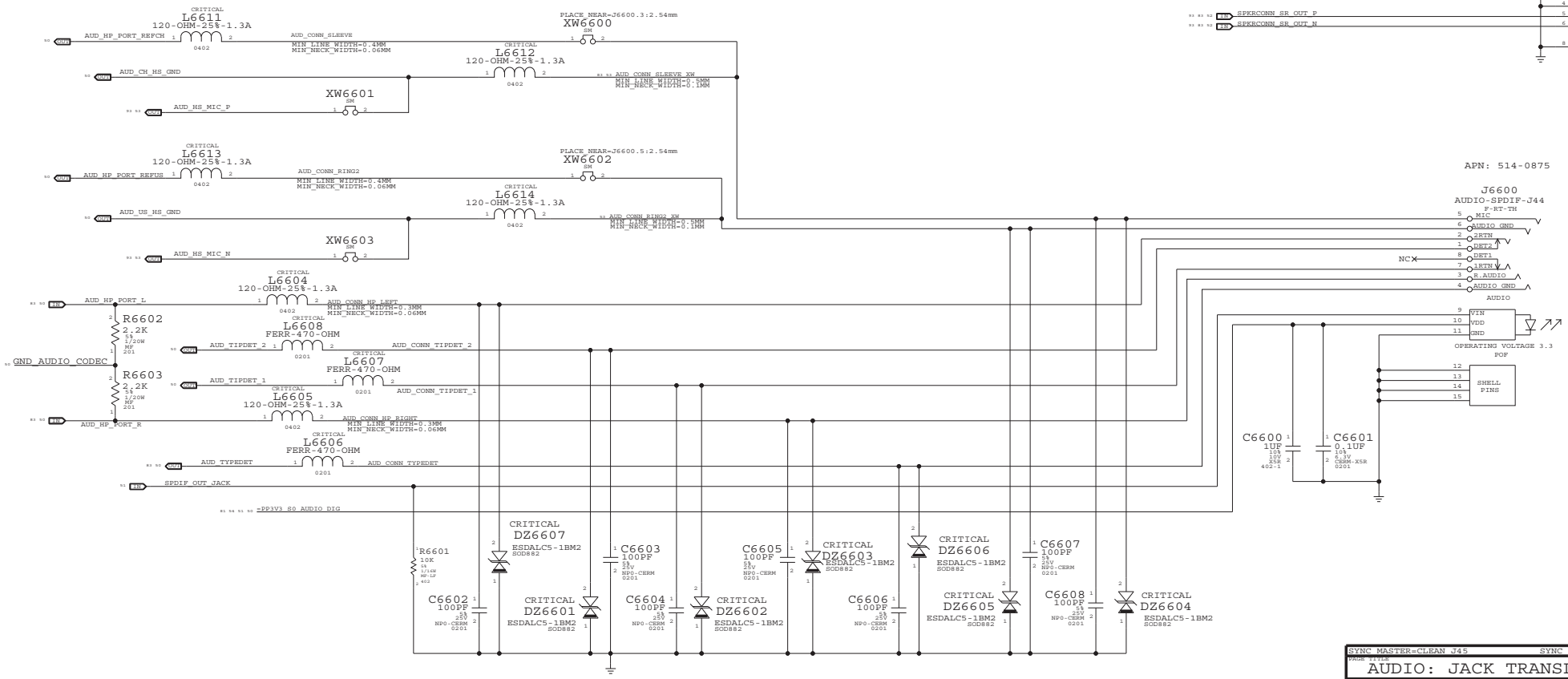
J6602
78171-6006
M-RT-SM

J6603
78171-6006
M-RT-SM

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH

OPERATING VOLTAGE 3.3
POF



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

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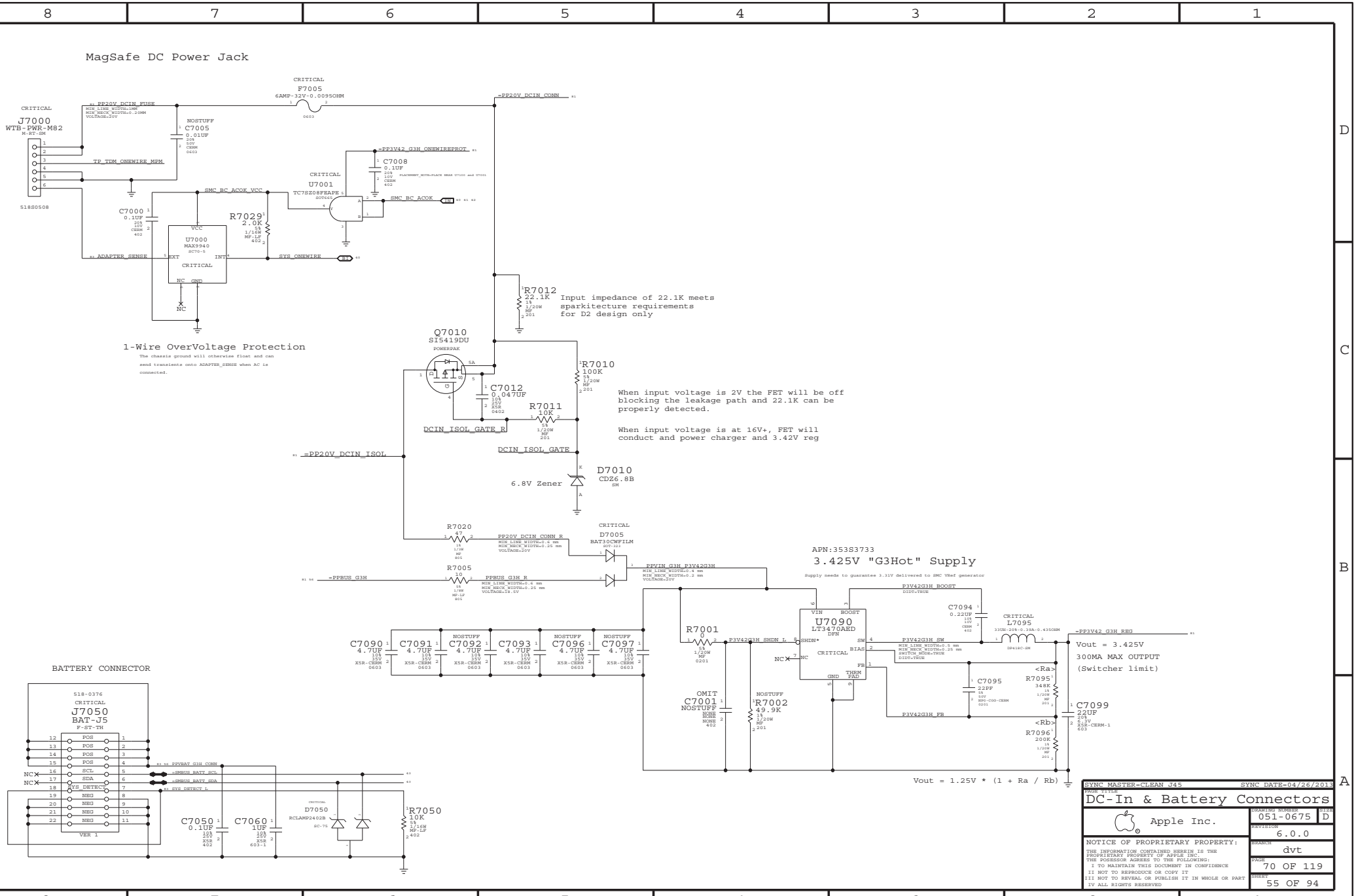
MagSafe DC Power Jack
J7000
WTB-PWR-M82
F7005
6AMP-32V-0.0095OHM
C7005
0.01UF
C7008
0.1UF
U7001
TC7SZ08FEAPE
C7000
0.1UF
R7029
2.0K
U7000
MAX9940
1-Wire OverVoltage Protection
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.
R7012
22.1K
Input impedance of 22.1K meets sparkitecture requirements for D2 design only
Q7010
SI5419DU
POWERPAK
R7010
100K
C7012
0.047UF
R7011
10K
When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.
When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg
DCIN_ISOL_GATE_R
DCIN_ISOL_GATE
=PP20V_DCIN_ISOL
D7010
CDZ6.8B
6.8V Zener
R7020
47
PP20V_DCIN_CONN_R
D7005
BAT30CWFILM
R7005
10
PPBUS_G3H_R
=PPBUS_G3H
APN:353S3733
3.425V "G3Hot" Supply
Supply needs to guarantee 3.31V delivered to SMC VRef generator
PPVIN_G3H_P3V42G3H
P3V42G3H_BOOST
U7090
LT3470AED
DFN
C7094
0.22UF
L7095
33UH-20%-0.39A-0.435OHM
DP414C-SM
-PP3V42_G3H_REG
Vout = 3.425V
300MA MAX OUTPUT
(Switcher limit)
R7001
0
P3V42G3H_SHDN_L
P3V42G3H_SW
P3V42G3H_FB
C7095
22PF
R7095
348K
<Ra>
C7099
22UF
R7096
200K
<Rb>
Vout = 1.25V * (1 + Ra / Rb)
C7090
4.7UF
C7091
4.7UF
C7092
4.7UF
C7093
4.7UF
C7096
4.7UF
C7097
4.7UF
NOSTUFF
OMIT
C7001
NOSTUFF
R7002
49.9K
BATTERY CONNECTOR
J7050
BAT-J5
F-ST-TH
VER 1
C7050
0.1UF
C7060
1UF
D7050
RCLAMP2402B
R7050
10K
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
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DC-In & Battery Connectors
Apple Inc.
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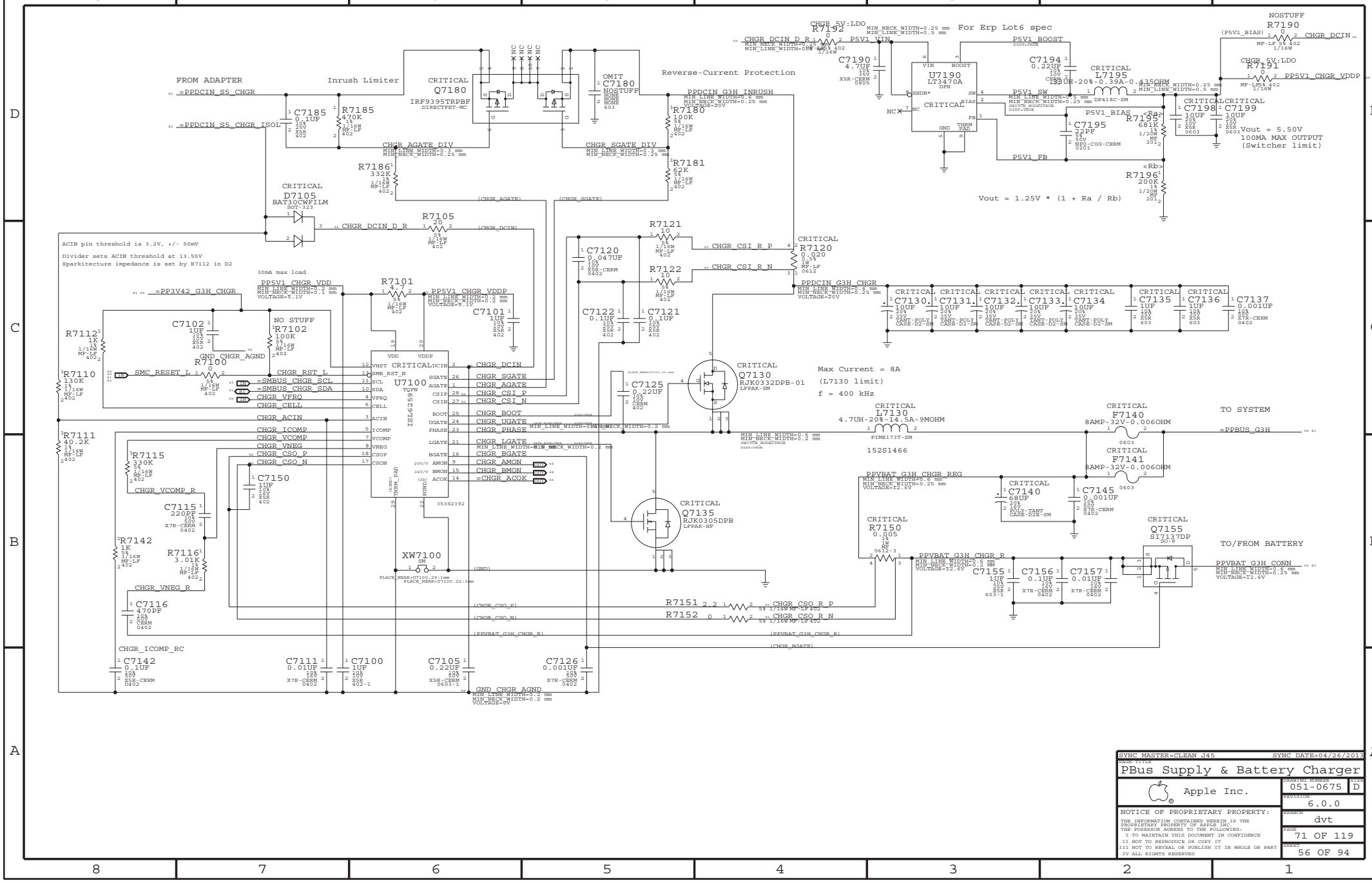
FROM ADAPTER
Inrush Limiter
Reverse-Current Protection
CRITICAL Q7180 IRF9395TRPBF DIRECTFET-MC
OMIT C7180 NOSTUFF
=PPDCIN_S5_CHGR
=PPDCIN_S5_CHGR_ISOL
C7185 0.1UF
R7185 470K
R7180 100K
R7186 332K
R7181 62K
CHGR_AGATE_DIV
CHGR_SGATE_DIV
PPDCIN_G3H_INRUSH
CRITICAL D7105 BAT30CWFILM SOT-323
R7105 20
CHGR_DCIN_D_R
ACIN pin threshold is 3.2V, +/- 50mV
Divider sets ACIN threshold at 13.55V
Sparkitecture impedance is set by R7112 in D2
30mA max load
=PP3V42_G3H_CHGR
PP5V1_CHGR_VDD
PP5V1_CHGR_VDDP
R7101 4.7
C7101 1UF
C7102 1UF
NO STUFF R7102 100K
R7112 1K
R7100 0
GND_CHGR_AGND
R7110 130K
R7111 40.2K
SMC_RESET_L
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA
CHGR_VFRQ
CHGR_CELL
CHGR_ACIN
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
CHGR_CSO_P
CHGR_CSO_N
U7100 ISL6255 TQFN
CHGR_RST_L
SMB_RST_N
CHGR_DCIN
CHGR_AGATE
CHGR_CSI_P
CHGR_CSI_N
CHGR_BOOT
CHGR_UGATE
CHGR_PHASE
CHGR_LGATE
CHGR_BGATE
CHGR_AMON
CHGR_BMON
=CHGR_ACOK
R7115 330K
C7150 1UF
C7115 220PF
R7142 1K
R7116 3.01K
CHGR_VCOMP_R
CHGR_VNEG_R
C7116 470PF
XW7100 SM
C7120 0.047UF
R7121 10
R7122 10
CHGR_CSI_R_P
CHGR_CSI_R_N
C7122 0.1UF
C7121 0.1UF
C7125 0.22UF
CRITICAL Q7130 RJK0332DPB-01 LFPAK-SM
CRITICAL Q7135 RJK0305DPB LFPAK-HF
CRITICAL R7120 0.020
PPDCIN_G3H_CHGR
Max Current = 8A
(L7130 limit)
f = 400 kHz
CRITICAL L7130 4.7UH-20%-14.5A-9MOHM PIME173T-SM
152S1466
CRITICAL P7140 8AMP-32V-0.006OHM
CRITICAL P7141 8AMP-32V-0.006OHM
TO SYSTEM
=PPBUS_G3H
PPVBAT_G3H_CHGR_REG
CRITICAL C7140 68UF
C7145 0.001UF
CRITICAL R7150 0.005
PPVBAT_G3H_CHGR_R
C7155 1UF
C7156 0.1UF
C7157 0.01UF
CRITICAL Q7155 SI7137DP SO-8
TO/FROM BATTERY
PPVBAT_G3H_CONN
R7151 2.2
R7152 0
CHGR_CSO_R_P
CHGR_CSO_R_N
CHGR_ICOMP_RC
C7142 0.1UF
C7111 0.01UF
C7100 1UF
C7105 0.22UF
C7126 0.001UF
GND_CHGR_AGND
CHGR_5V:LDO
R7192 0
P5V1_VIN
C7190 4.7UF
U7190 LT3470A DFN
P5V1_BOOST
C7194 0.22UF
CRITICAL L7195 4.7UH-20%-0.39A-0.435OHM DP418C-SM
P5V1_SW
P5V1_BIAS
P5V1_FB
C7195 22PF
<Ra> R7195 681K
<Rb> R7196 200K
Vout = 1.25V * (1 + Ra / Rb)
NOSTUFF R7190 0
CHGR_DCIN
CHGR_5V:LDO R7191 0
PP5V1_CHGR_VDDP
CRITICAL C7198 10UF
C7199 10UF
Vout = 5.50V
100MA MAX OUTPUT
(Switcher limit)
CRITICAL C7130 10UF
C7131 10UF
C7132 10UF
C7133 10UF
C7134 10UF
C7135 1UF
C7136 1UF
C7137 0.001UF
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
PAGE TITLE
PBus Supply & Battery Charger
Apple Inc.
DRAWING NUMBER 051-0675
SIZE D
REVISION 6.0.0
BRANCH dvt
PAGE 71 OF 119
SHEET 56 OF 94
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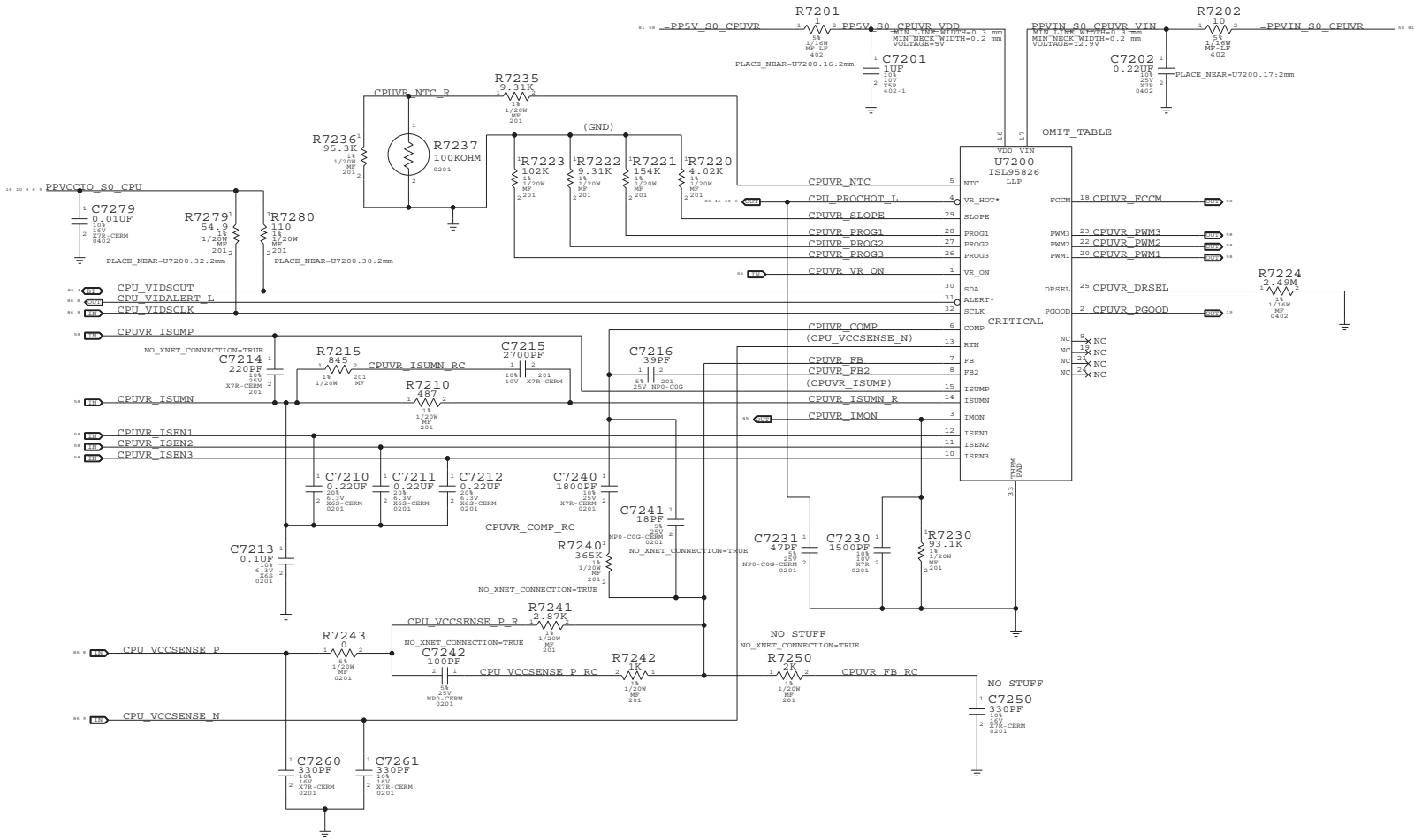
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC,ISL95826IRZ200,PWM,PGOOD,SCREEN,32P,QFN	U7200	CRITICAL	

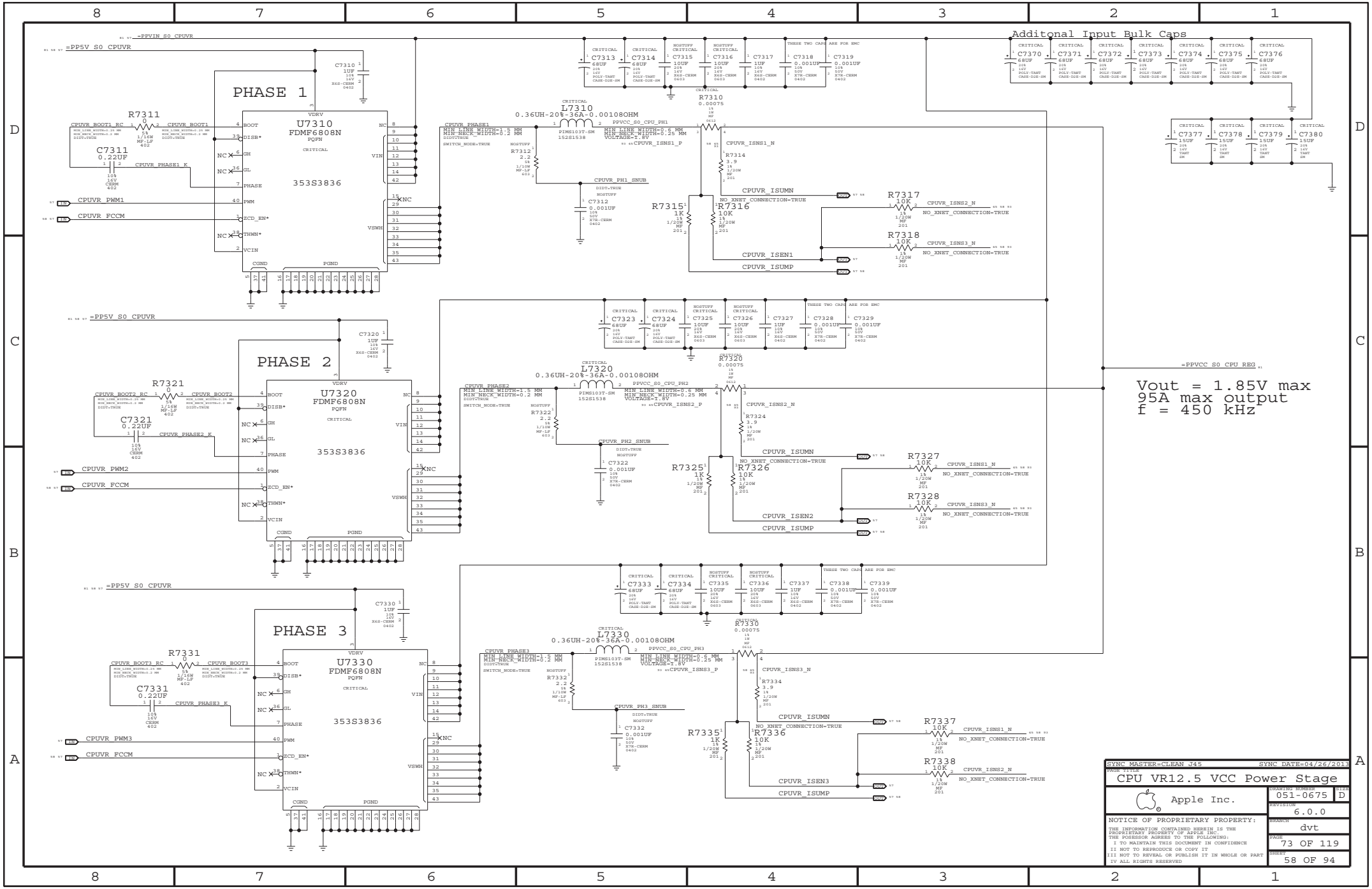


SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE
CPU VR12.5 VCC Regulator IC

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D
REVISION 6.0.0
BRANCH dvt
PAGE 72 OF 119
SHEET 57 OF 94


PHASE 1
PHASE 2
PHASE 3
U7310
FDMF6808N
PQFN
CRITICAL
353S3836
VDRV
BOOT
DISB*
GH
GL
PHASE
PWM
ZCD_EN*
THWN*
VCIN
VIN
VSWH
NC
CGND
PGND
R7311
0
C7311
0.22UF
CPUVR_BOOT1_RC
CPUVR_BOOT1
CPUVR_PHASE1_K
CPUVR_PWM1
CPUVR_FCCM
U7320
R7321
C7321
CPUVR_BOOT2_RC
CPUVR_BOOT2
CPUVR_PHASE2_K
CPUVR_PWM2
U7330
R7331
C7331
CPUVR_BOOT3_RC
CPUVR_BOOT3
CPUVR_PHASE3_K
CPUVR_PWM3
=PPVIN_S0_CPUVR
=PP5V_S0_CPUVR
C7310
1UF
C7320
C7330
L7310
0.36UH-20%-36A-0.00108OHM
L7320
L7330
PIMS103T-SM
152815138
CPUVR_PHASE1
CPUVR_PHASE2
CPUVR_PHASE3
PPVCC_S0_CPU_PH1
PPVCC_S0_CPU_PH2
PPVCC_S0_CPU_PH3
R7312
R7322
R7332
CPUVR_PH1_SNUB
CPUVR_PH2_SNUB
CPUVR_PH3_SNUB
C7312
C7322
C7332
R7310
R7320
R7330
CPUVR_ISNS1_P
CPUVR_ISNS2_P
CPUVR_ISNS3_P
CPUVR_ISNS1_N
CPUVR_ISNS2_N
CPUVR_ISNS3_N
R7314
R7324
R7334
CPUVR_ISUMN
CPUVR_ISUMP
CPUVR_ISEN1
CPUVR_ISEN2
CPUVR_ISEN3
R7315
R7325
R7335
R7316
R7326
R7336
R7317
R7327
R7337
R7318
R7328
R7338
NO_XNET_CONNECTION=TRUE
C7313
C7314
C7315
C7316
C7317
C7318
C7319
C7323
C7324
C7325
C7326
C7327
C7328
C7329
C7333
C7334
C7335
C7336
C7337
C7338
C7339
THESE TWO CAPS ARE FOR EMC
Additonal Input Bulk Caps
C7370
C7371
C7372
C7373
C7374
C7375
C7376
C7377
C7378
C7379
C7380
=PPVCC_S0_CPU_REG
Vout = 1.85V max
95A max output
f = 450 kHz
SYNC MASTER=CLEAN_J45
SYNC DATE=04/26/2013
PAGE TITLE
CPU VR12.5 VCC Power Stage
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
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58 OF 94
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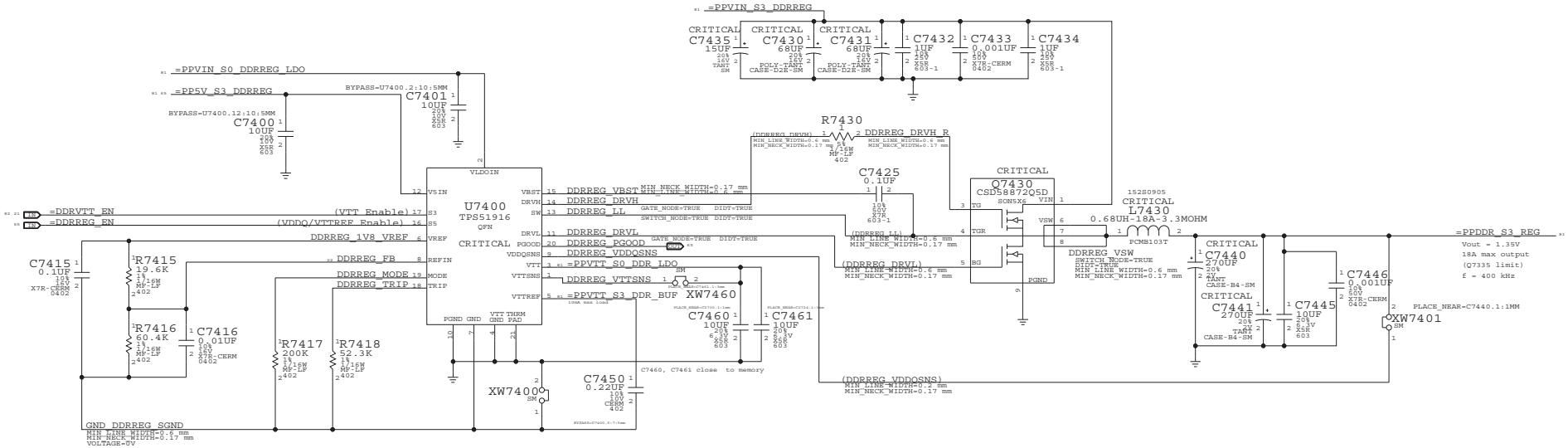
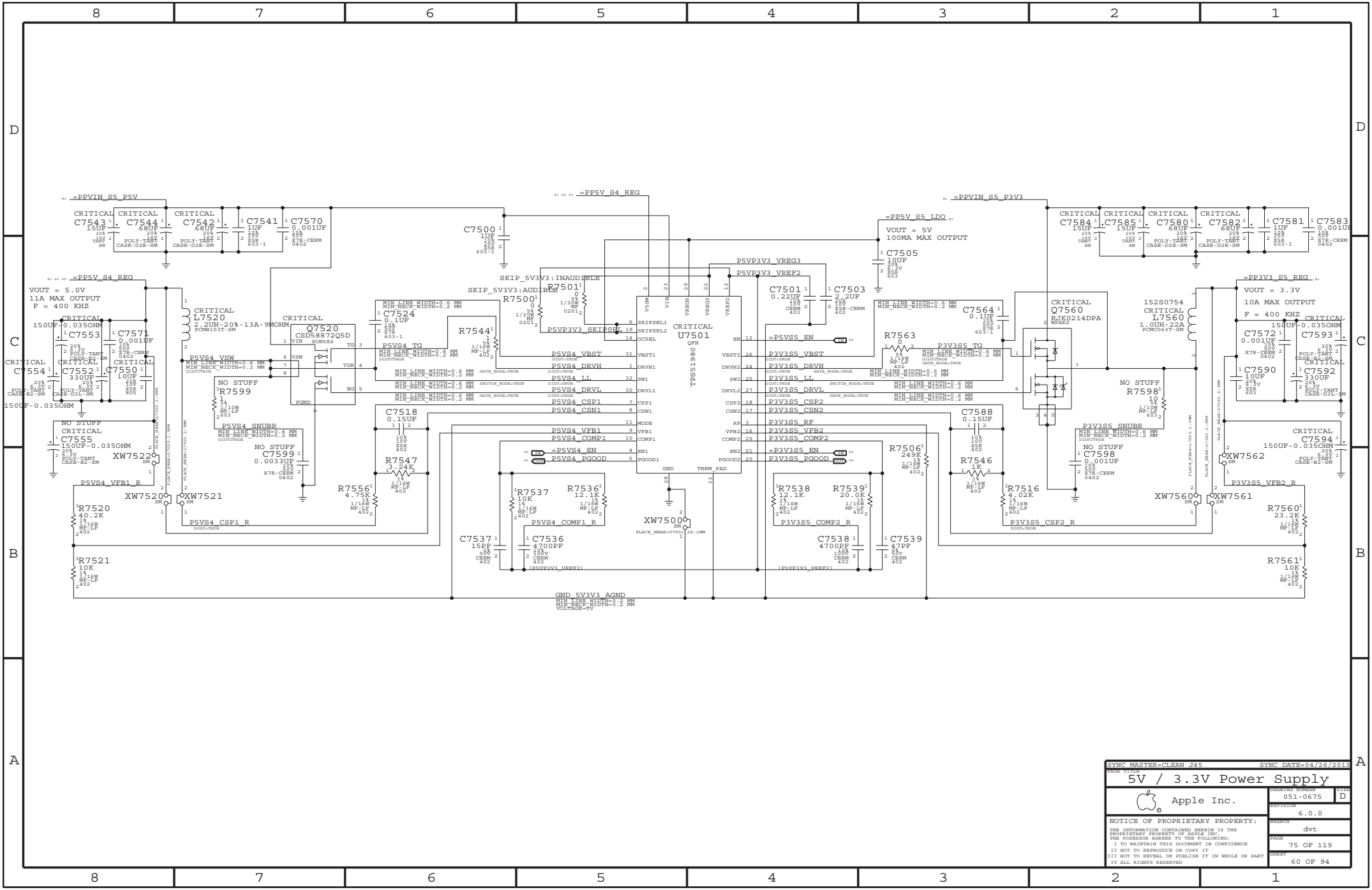
DDR3L (1V35 S3) REGULATOR



SYNC MASTER=CLEAN J45	SYNC DATE=04/26/2013
PAGE TITLE	1.35V DDR3L SUPPLY
Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
	REVISION 6.0.0
	BRANCH dvt
	PAGE 74 OF 119
	SHEET 59 OF 94


=PPVIN_S5_P5V
=PP5V_S4_REG
=PP5V_S5_LDO
VOUT = 5V
100MA MAX OUTPUT
=PPVIN_S5_P3V3
=PP5V_S4_REG
VOUT = 5.0V
11A MAX OUTPUT
F = 400 KHZ
=PP3V3_S5_REG
VOUT = 3.3V
10A MAX OUTPUT
F = 400 KHZ
SKIP_5V3V3:INAUDIBLE
SKIP_5V3V3:AUDIBLE
P5VP3V3_VREG3
P5VP3V3_VREF2
P5VP3V3_SKIPSEL
TPS51980
U7501
QFN
THRM_PAD
GND_5V3V3_AGND
MIN LINE WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
P5VS4_VSW
P5VS4_TG
P5VS4_VBST
P5VS4_DRVH
P5VS4_LL
P5VS4_DRVL
P5VS4_CSP1
P5VS4_CSN1
P5VS4_VFB1
P5VS4_COMP1
P5VS4_PGOOD
P5VS4_SNUBR
P5VS4_VFB1_R
P5VS4_CSP1_R
P5VS4_COMP1_R
P3V3S5_TG
P3V3S5_VBST
P3V3S5_DRVH
P3V3S5_LL
P3V3S5_DRVL
P3V3S5_CSP2
P3V3S5_CSN2
P3V3S5_RF
P3V3S5_VFB2
P3V3S5_COMP2
P3V3S5_PGOOD
P3V3S5_SNUBR
P3V3S5_VFB2_R
P3V3S5_COMP2_R
P3V3S5_CSP2_R
=P5VS5_EN
=P3V3S5_EN
NO STUFF
CRITICAL
Q7520
CSD58872Q5D
Q7560
RJK0214DPA
L7520
2.2UH-20%-13A-9MOHM
L7560
1.0UH-22A
152S0754
XW7522
XW7521
XW7562
XW7561
XW75200
XW75600
XW75000
C7500
C7501
C7503
C7505
C7518
C7524
C7537
C7536
C7538
C7539
C7564
C7588
C7598
C7599
R7500
R7501
R7520
R7521
R7537
R7536
R7538
R7539
R7544
R7547
R7556
R7563
R7598
R7506
R7546
R7516
R7560
R7561
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
PAGE TITLE
5V / 3.3V Power Supply
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
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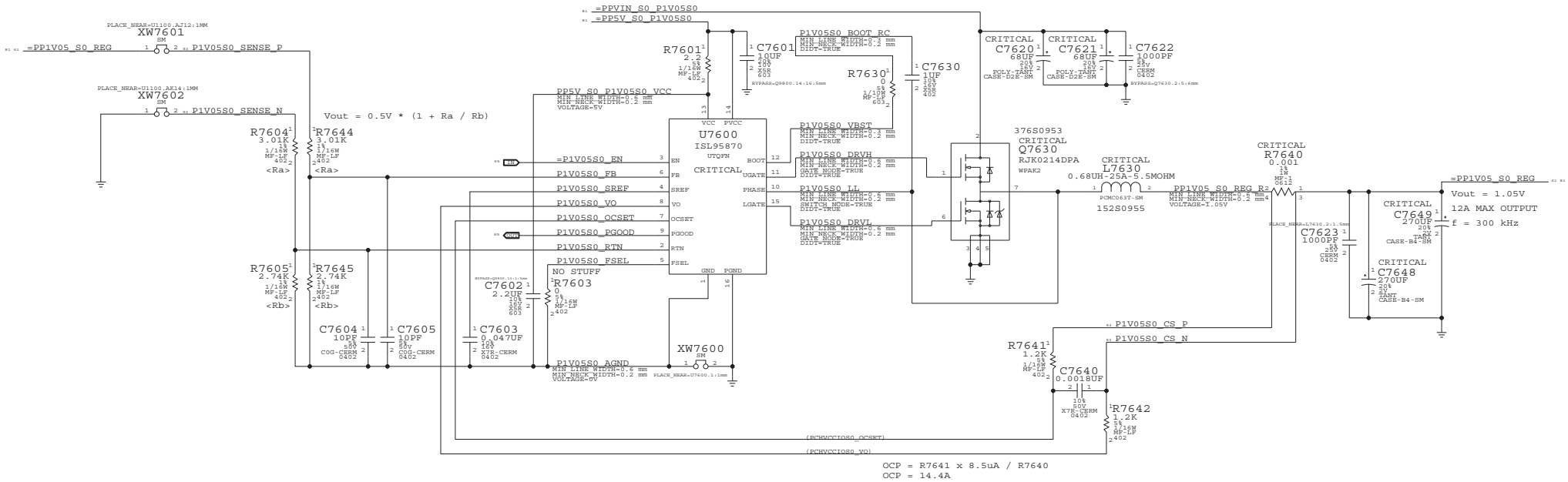
1V05 S0 REGULATOR



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE: 1V05V POWER SUPPLY

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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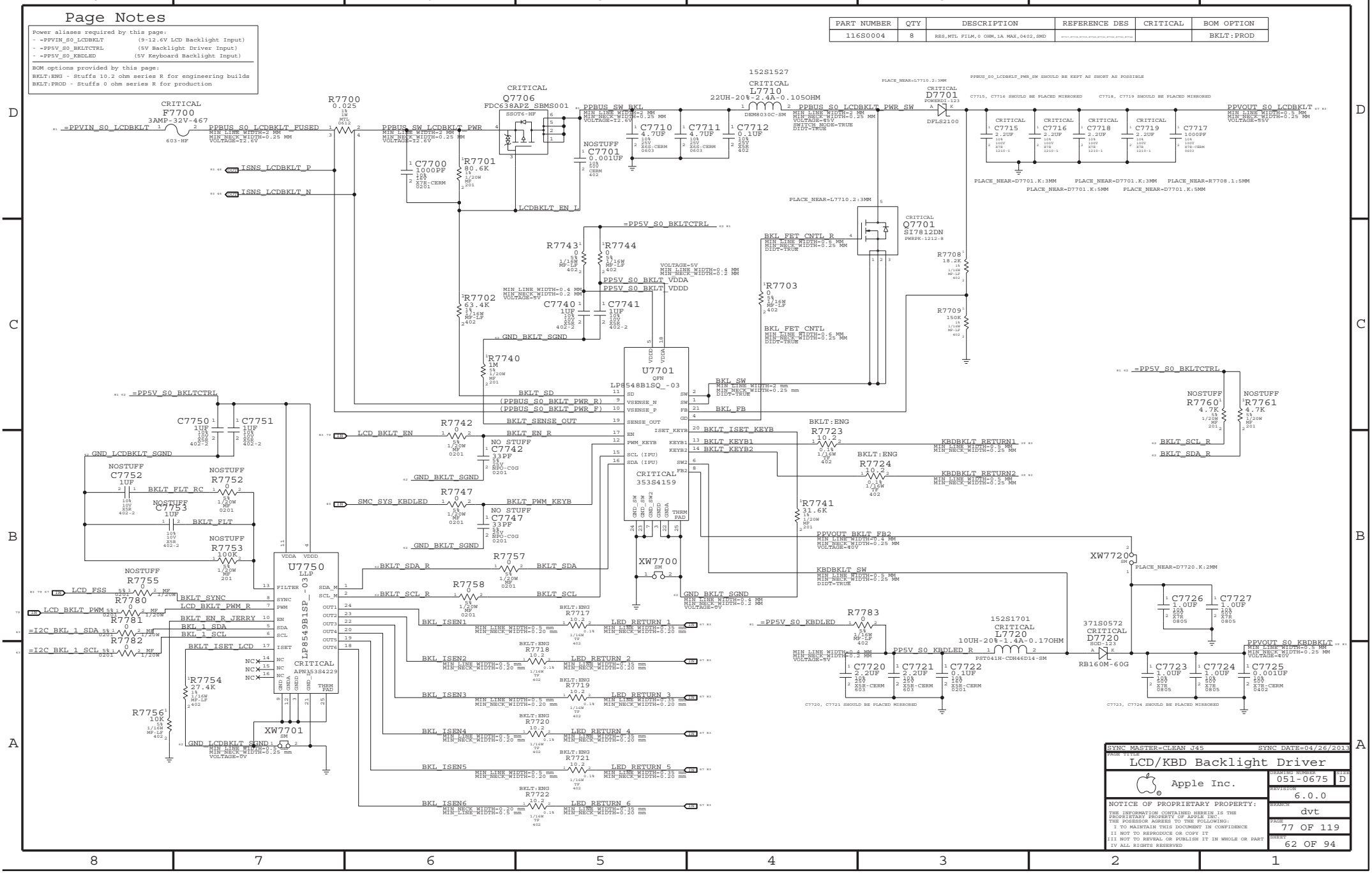
SHEET: 61 OF 94

Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	8	RES,MTL FILM,0 OHM,1A MAX,0402,SMD			BKLT:PROD



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE
LCD/KBD Backlight Driver

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D
REVISION 6.0.0
BRANCH dvt
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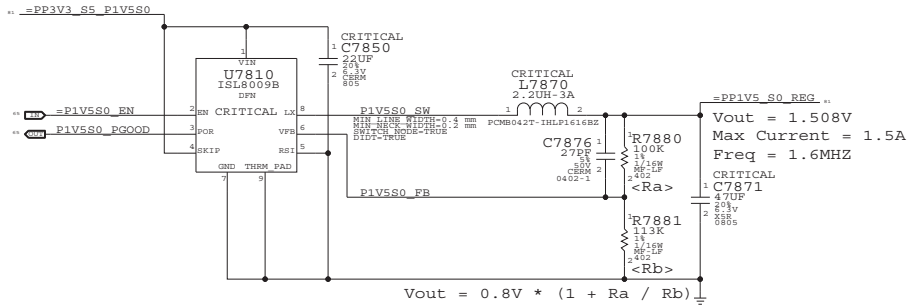
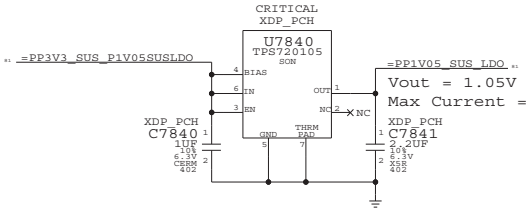
1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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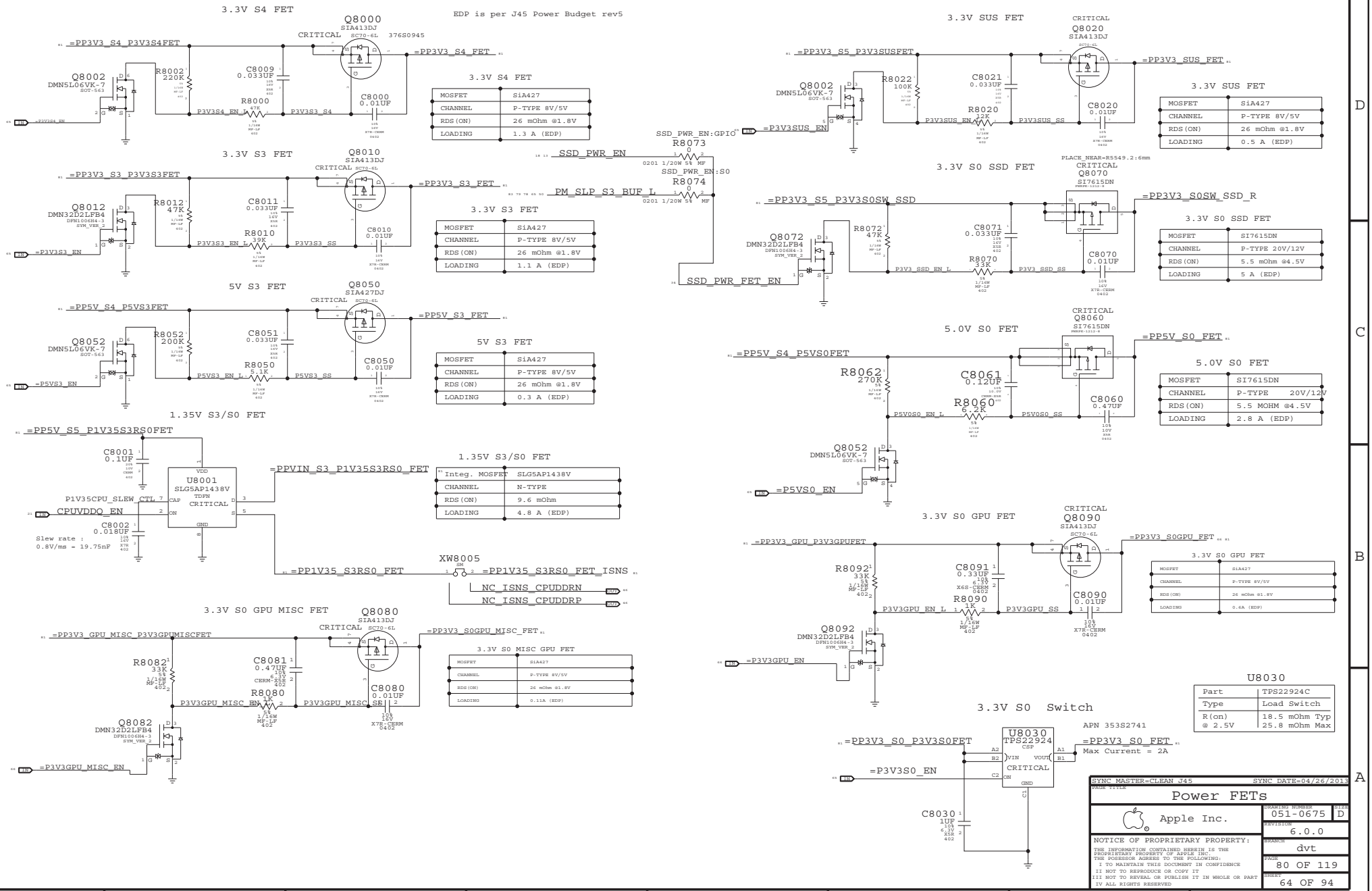
3.3V S4 FET
EDP is per J45 Power Budget rev5
Q8000
SIA413DJ
CRITICAL
SC70-6L
376S0945
=PP3V3_S4_P3V3S4FET
=PP3V3_S4_FET
Q8002
DMN5L06VK-7
SOT-563
R8002
220K
C8009
0.033UF
R8000
47K
C8000
0.01UF
P3V3S4_EN_L
P3V3S3_S4
=P3V3S4_EN
3.3V S4 FET
MOSFET SiA427
CHANNEL P-TYPE 8V/5V
RDS(ON) 26 mOhm @1.8V
LOADING 1.3 A (EDP)
3.3V S3 FET
Q8010
SIA413DJ
=PP3V3_S3_P3V3S3FET
=PP3V3_S3_FET
Q8012
DMN32D2LFB4
R8012
47K
C8011
0.033UF
R8010
39K
C8010
0.01UF
P3V3S3_EN_L
P3V3S3_SS
=P3V3S3_EN
3.3V S3 FET
MOSFET SiA427
CHANNEL P-TYPE 8V/5V
RDS(ON) 26 mOhm @1.8V
LOADING 1.1 A (EDP)
5V S3 FET
Q8050
SIA427DJ
=PP5V_S4_P5VS3FET
=PP5V_S3_FET
Q8052
DMN5L06VK-7
R8052
200K
C8051
0.033UF
R8050
5.1K
C8050
0.01UF
P5VS3_EN_L
P5VS3_SS
=P5VS3_EN
5V S3 FET
MOSFET SiA427
CHANNEL P-TYPE 8V/5V
RDS(ON) 26 mOhm @1.8V
LOADING 0.3 A (EDP)
1.35V S3/S0 FET
=PP5V_S5_P1V35S3RS0FET
U8001
SLG5AP1438V
TDFN
CRITICAL
VDD
CAP
ON
GND
C8001
0.1UF
C8002
0.018UF
P1V35CPU_SLEW_CTL
CPUVDDQ_EN
Slew rate :
0.8V/ms = 19.75nF
=PPVIN_S3_P1V35S3RS0_FET
=PP1V35_S3RS0_FET
1.35V S3/S0 FET
Integ. MOSFET SLG5AP1438V
CHANNEL N-TYPE
RDS(ON) 9.6 mOhm
LOADING 4.8 A (EDP)
XW8005
=PP1V35_S3RS0_FET_ISNS
NC_ISNS_CPUDDRN
NC_ISNS_CPUDDRP
3.3V S0 GPU MISC FET
Q8080
SIA413DJ
=PP3V3_GPU_MISC_P3V3GPUMISCFET
=PP3V3_S0GPU_MISC_FET
R8082
33K
C8081
0.47UF
R8080
1K
C8080
0.01UF
P3V3GPU_MISC_EN
P3V3GPU_MISC_SS
Q8082
DMN32D2LFB4
=P3V3GPU_MISC_EN
3.3V S0 MISC GPU FET
MOSFET SiA427
CHANNEL P-TYPE 8V/5V
RDS(ON) 26 mOhm @1.8V
LOADING 0.11A (EDP)
SSD_PWR_EN
SSD_PWR_EN:GPIO
R8073
0
SSD_PWR_EN:S0
R8074
0
PM_SLP_S3_BUF_L
SSD_PWR_FET_EN
3.3V SUS FET
Q8020
SIA413DJ
CRITICAL
SC70-6L
=PP3V3_S5_P3V3SUSFET
=PP3V3_SUS_FET
Q8002
DMN5L06VK-7
R8022
100K
C8021
0.033UF
R8020
12K
C8020
0.01UF
P3V3SUS_EN_L
P3V3SUS_SS
=P3V3SUS_EN
3.3V SUS FET
MOSFET SiA427
CHANNEL P-TYPE 8V/5V
RDS(ON) 26 mOhm @1.8V
LOADING 0.5 A (EDP)
3.3V S0 SSD FET
PLACE_NEAR=R5549.2:6mm
Q8070
SI7615DN
CRITICAL
=PP3V3_S5_P3V3S0SW_SSD
=PP3V3_S0SW_SSD_R
Q8072
DMN32D2LFB4
R8072
47K
C8071
0.033UF
R8070
33K
C8070
0.01UF
P3V3_SSD_EN_L
P3V3_SSD_SS
3.3V S0 SSD FET
MOSFET SI7615DN
CHANNEL P-TYPE 20V/12V
RDS(ON) 5.5 mOhm @4.5V
LOADING 5 A (EDP)
5.0V S0 FET
Q8060
SI7615DN
CRITICAL
=PP5V_S4_P5VS0FET
=PP5V_S0_FET
R8062
270K
C8061
0.12UF
R8060
6.2K
C8060
0.47UF
P5V0S0_EN_L
P5V0S0_SS
Q8052
DMN5L06VK-7
=P5VS0_EN
5.0V S0 FET
MOSFET SI7615DN
CHANNEL P-TYPE 20V/12V
RDS(ON) 5.5 MOHM @4.5V
LOADING 2.8 A (EDP)
3.3V S0 GPU FET
Q8090
SIA413DJ
CRITICAL
SC70-6L
=PP3V3_GPU_P3V3GPUFET
=PP3V3_S0GPU_FET
R8092
33K
C8091
0.33UF
R8090
1K
C8090
0.01UF
P3V3GPU_EN_L
P3V3GPU_SS
Q8092
DMN32D2LFB4
=P3V3GPU_EN
3.3V S0 GPU FET
MOSFET SiA427
CHANNEL P-TYPE 8V/5V
RDS(ON) 26 mOhm @1.8V
LOADING 0.6A (EDP)
3.3V S0 Switch
APN 353S2741
U8030
TPS22924
CSP
CRITICAL
=PP3V3_S0_P3V3S0FET
=PP3V3_S0_FET
Max Current = 2A
=P3V3S0_EN
C8030
1UF
U8030
Part TPS22924C
Type Load Switch
R(on) @ 2.5V 18.5 mOhm Typ 25.8 mOhm Max
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
PAGE TITLE
Power FETs
Apple Inc.
DRAWING NUMBER 051-0675
SIZE D
REVISION 6.0.0
BRANCH dvt
PAGE 80 OF 119
SHEET 64 OF 94
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Power State Debug LEDs
(For development only)

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

S4 Power Enable

S3 ENABLE

CPUVCORE ENABLE

S0 ENABLE

3.3V SUS Enable

PM_SLP_SUS_L: 100K pull down on PCH page

S0 Rail PGOOD (BJT Version)

3.3V SUS Detect

S0 Rail PGOOD Circuitry
(ISL Version in development)

S5 Rail Enables & PGOOD

WLAN Enable Generation

"WLAN" = ("S4" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S4 term is guaranteed by S4 pull-up on open-drain AP_PWR_EN signal.

1V5 S0 "PGOOD" Delay

CHGR_VFRQ Generation

VFRQ High: Variable Frequency
VFRQ LOW: Fix Frequency

Unused PGOOD signals

SYNC MASTER=CLEAN_J45	SYNC DATE=06/23/2013	
PAGE TITLE: Power Control 1/ENABLE		
Apple Inc.	DRAWING NUMBER: 051-0675	SIZE: D
	REVISION: 6.0.0	
	BRANCH: dvt	
	PAGE: 81 OF 119	
	SHEET: 65 OF 94	

GPU Rail Sequencing

KEPLER GPU REQUIRES RAILS TO COME up in the following order:

1) GPU_1.3V
2) IPPX IOVDD - 1.8V
3) GPUVCORE
4) PRVDDQ/GDDR5 1.35V
5) PEXVDD/Q OR IPPV IOVDD - 1.05V

EG_RAIL1_EN	P3V3GPU_EN	=P3V3GPU_MISC_EN	
	MAKE_BASE=TRUE		
EG_RAIL2_EN	P1V8GPU_EN	=P3V3GPU_EN	
	MAKE_BASE=TRUE		
EG_RAIL3_EN	GPUVCORE_EN	=P1V8GPU_EN	
	MAKE_BASE=TRUE		
EG_RAIL4_EN	P1V35GPUFB_EN	=GPUVCORE_EN	
	MAKE_BASE=TRUE		
EG_RAIL5_EN	P1V05_S0GPU_EN	=P1V35FB_EN	
	MAKE_BASE=TRUE		
		=P1V05_GPU_EN	

NOTE: 1V8 MAY NOT BE REQUIRED FOR KEPLER IF THERE IS NO LVDS

EXT GPU PWRGD Pullup

=PP3V3_S0_PWRCTL

R8200 R8201 R8202
100K 5% 1/20W MF 201

=PP3V3_S0GPU_FET	GPU_PGOOD1	
TP_GPU_PGOOD2	GPU_PGOOD2	
MAKE_BASE=TRUE		
GPUVCORE_PGOOD	GPU_PGOOD3	
MAKE_BASE=TRUE		
GPUFB_PGOOD	GPU_PGOOD4	
MAKE_BASE=TRUE		
P1V05_S0GPU_PGOOD	PM_ALL_GPU_PGOOD	
MAKE_BASE=TRUE		

NOTE: NO PU ON 3V3 AND 1V8 PGOODS SINCE THEY ARE SYNTHETIC.

NOTE 2: CHECK IF 1V8 IS READ AS LOGIC HIGH BY GMUX

PCIE TEST STRUCTURES (FOR LAB USE)

PEG_R2D_P<0> — R8210 82 5% 1/20W MF 201 — NOSTUFF — PEG_R2D_N<0>

PEG_R2D_P<5> — R8215 82 5% 1/20W MF 201 — NOSTUFF — PEG_R2D_N<5>

PEG_R2D_P<3> — R8213 82 5% 1/20W MF 201 — NOSTUFF — PEG_R2D_N<3>

PEG_R2D_P<7> — R8217 82 5% 1/20W MF 201 — NOSTUFF — PEG_R2D_N<7>

PLACE R8210 - R8217 CLOSE TO U8000

PEG_D2R_P<0> — R8220 82 5% 1/20W MF 201 — NOSTUFF — PEG_D2R_N<0>

PEG_D2R_P<4> — R8224 82 5% 1/20W MF 201 — NOSTUFF — PEG_D2R_N<4>

PEG_D2R_P<7> — R8227 82 5% 1/20W MF 201 — NOSTUFF — PEG_D2R_N<7>

PLACE R8220 - R8227 CLOSE TO U1000

SYNC MASTER-D2 KEPLER — SYNC DATE-01/13/2012

PAGE TITLE: Power Sequencing EG/PCH S0

Apple Inc.

DRAWING NUMBER: 051-0675 — SIZE: D

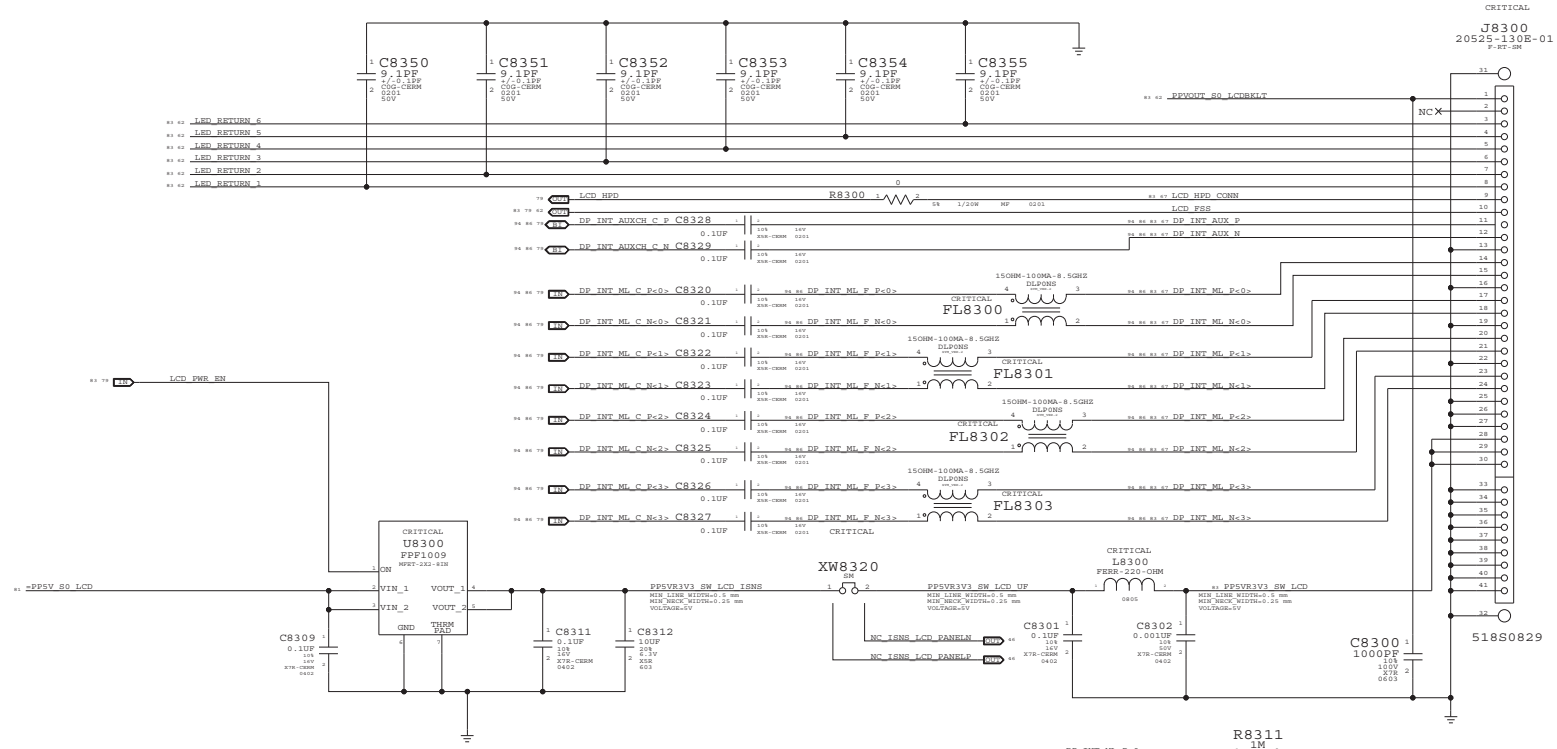
REVISION: 6.0.0

BRANCH: dvt

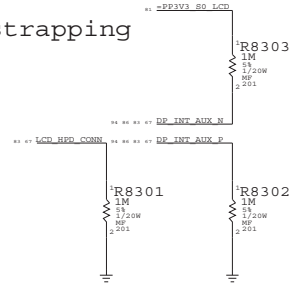
PAGE: 82 OF 119

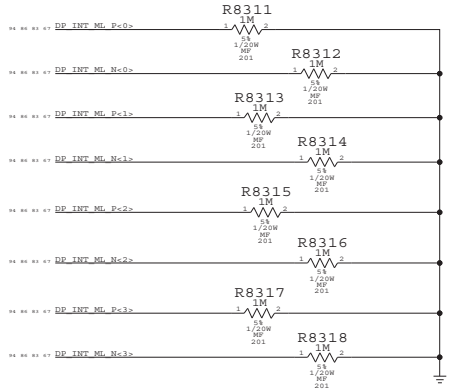
SHEET: 66 OF 94

LCD PANEL INTERFACE (eDP)



LCD Panel HPD & AUX strapping





SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

PAGE: 83 OF 119

SHEET: 67 OF 94

Page Notes

Power aliases required by this page:

- +PP3V3_GPU_VDD33

Signal aliases required by this page:

(NONE)

ROM options provided by this page:

(NONE)

C8420 0.22UF PEG_R2D_C_P<0> — PEG_R2D_P<0>
C8421 0.22UF PEG_R2D_C_N<0> — PEG_R2D_N<0>
C8422 0.22UF PEG_R2D_C_P<1> — PEG_R2D_P<1>
C8423 0.22UF PEG_R2D_C_N<1> — PEG_R2D_N<1>
C8424 0.22UF PEG_R2D_C_P<2> — PEG_R2D_P<2>
C8425 0.22UF PEG_R2D_C_N<2> — PEG_R2D_N<2>
C8426 0.22UF PEG_R2D_C_P<3> — PEG_R2D_P<3>
C8427 0.22UF PEG_R2D_C_N<3> — PEG_R2D_N<3>
C8428 0.22UF PEG_R2D_C_P<4> — PEG_R2D_P<4>
C8429 0.22UF PEG_R2D_C_N<4> — PEG_R2D_N<4>
C8430 0.22UF PEG_R2D_C_P<5> — PEG_R2D_P<5>
C8431 0.22UF PEG_R2D_C_N<5> — PEG_R2D_N<5>
C8432 0.22UF PEG_R2D_C_P<6> — PEG_R2D_P<6>
C8433 0.22UF PEG_R2D_C_N<6> — PEG_R2D_N<6>
C8434 0.22UF PEG_R2D_C_P<7> — PEG_R2D_P<7>
C8435 0.22UF PEG_R2D_C_N<7> — PEG_R2D_N<7>

C8455 0.22UF PEG_D2R_C_P<0> — PEG_D2R_P<0>
C8456 0.22UF PEG_D2R_C_N<0> — PEG_D2R_N<0>
C8457 0.22UF PEG_D2R_C_P<1> — PEG_D2R_P<1>
C8458 0.22UF PEG_D2R_C_N<1> — PEG_D2R_N<1>
C8459 0.22UF PEG_D2R_C_P<2> — PEG_D2R_P<2>
C8460 0.22UF PEG_D2R_C_N<2> — PEG_D2R_N<2>
C8461 0.22UF PEG_D2R_C_P<3> — PEG_D2R_P<3>
C8462 0.22UF PEG_D2R_C_N<3> — PEG_D2R_N<3>
C8463 0.22UF PEG_D2R_C_P<4> — PEG_D2R_P<4>
C8464 0.22UF PEG_D2R_C_N<4> — PEG_D2R_N<4>
C8465 0.22UF PEG_D2R_C_P<5> — PEG_D2R_P<5>
C8466 0.22UF PEG_D2R_C_N<5> — PEG_D2R_N<5>
C8467 0.22UF PEG_D2R_C_P<6> — PEG_D2R_P<6>
C8468 0.22UF PEG_D2R_C_N<6> — PEG_D2R_N<6>
C8469 0.22UF PEG_D2R_C_P<7> — PEG_D2R_P<7>
C8470 0.22UF PEG_D2R_C_N<7> — PEG_D2R_N<7>

OMIT_TABLE

U8400
NV-GK107
BGA
(1 OF 10)

PEG_R2D_P<0>	AN12 PEX_RX0	PEX_TX0 AK14	PEG_D2R_C_P<0>
PEG_R2D_N<0>	AM12 PEX_RX0*	PEX_TX0* AJ14	PEG_D2R_C_N<0>
PEG_R2D_P<1>	AN14 PEX_RX1	PEX_TX1 AH14	PEG_D2R_C_P<1>
PEG_R2D_N<1>	AM14 PEX_RX1*	PEX_TX1* AG14	PEG_D2R_C_N<1>
PEG_R2D_P<2>	AP14 PEX_RX2	PEX_TX2 AK15	PEG_D2R_C_P<2>
PEG_R2D_N<2>	AP15 PEX_RX2*	PEX_TX2* AJ15	PEG_D2R_C_N<2>
PEG_R2D_P<3>	AN15 PEX_RX3	PEX_TX3 AL16	PEG_D2R_C_P<3>
PEG_R2D_N<3>	AM15 PEX_RX3*	PEX_TX3* AK16	PEG_D2R_C_N<3>
PEG_R2D_P<4>	AN17 PEX_RX4	PEX_TX4 AK17	PEG_D2R_C_P<4>
PEG_R2D_N<4>	AM17 PEX_RX4*	PEX_TX4* AJ17	PEG_D2R_C_N<4>
PEG_R2D_P<5>	AP17 PEX_RX5	PEX_TX5 AH17	PEG_D2R_C_P<5>
PEG_R2D_N<5>	AP18 PEX_RX5*	PEX_TX5* AG17	PEG_D2R_C_N<5>
PEG_R2D_P<6>	AN18 PEX_RX6	PEX_TX6 AK18	PEG_D2R_C_P<6>
PEG_R2D_N<6>	AM18 PEX_RX6*	PEX_TX6* AJ18	PEG_D2R_C_N<6>
PEG_R2D_P<7>	AN20 PEX_RX7	PEX_TX7 AL19	PEG_D2R_C_P<7>
PEG_R2D_N<7>	AM20 PEX_RX7*	PEX_TX7* AK19	PEG_D2R_C_N<7>
NC	AP20 PEX_RX8	PEX_TX8 AK20	NC
NC	AP21 PEX_RX8*	PEX_TX8* AJ20	NC
NC	AN21 PEX_RX9	PEX_TX9 AH20	NC
NC	AM21 PEX_RX9*	PEX_TX9* AG20	NC
NC	AN23 PEX_RX10	PEX_TX10 AK21	NC
NC	AM23 PEX_RX10*	PEX_TX10* AJ21	NC
NC	AP23 PEX_RX11	PEX_TX11 AL22	NC
NC	AP24 PEX_RX11*	PEX_TX11* AK22	NC
NC	AN24 PEX_RX12	PEX_TX12 AK23	NC
NC	AM24 PEX_RX12*	PEX_TX12* AJ23	NC
NC	AN26 PEX_RX13	PEX_TX13 AH23	NC
NC	AM26 PEX_RX13*	PEX_TX13* AG23	NC
NC	AP26 PEX_RX14	PEX_TX14 AK24	NC
NC	AP27 PEX_RX14*	PEX_TX14* AJ24	NC
NC	AN27 PEX_RX15	PEX_TX15 AL25	NC
NC	AM27 PEX_RX15*	PEX_TX15* AK25	NC

PEG_CLK100M_P — AL13 PEX_REFCLK
PEG_CLK100M_N — AK13 PEX_REFCLK*
PEX_TSTCLK_OUT AJ26
PEX_TSTCLK_OUT* AK26
GPU_RESET_L — R8400 0 — GPU_RESET_R_L — AJ12 PEX_RST*
PEX_TERMP AP29
PEX_CLKREQ_L_R — AK12 PEX_CLKREQ*
AJ11 PEX_WAKE*
PEX_SVDD_3V3 AG12

-PP3V3_GPU_VDD33 — R8401 10K 1% 1/20W MF 201 — PEX_CLKREQ_L_R
PEX_TSTCLK_O_P — NOSTUFF R8402 200 1% 1/20W MF 201 — PEX_TSTCLK_O_N
GPU_PEX_TERMP — R8405 2.49K 1% 1/20W MF 201
PP3V3_GPU_PEX_PLL_HVDD

SYNC MASTER-D2 MLB — SYNC DATE-07/31/2012

PAGE TITLE: KEPLER PCI-E

Apple Inc.

DRAWING NUMBER: 051-0675 — SIZE: D
REVISION: 6.0.0
BRANCH: dvt
PAGE: 84 OF 119
SHEET: 68 OF 94

Page Notes

Power aliases required by this page:

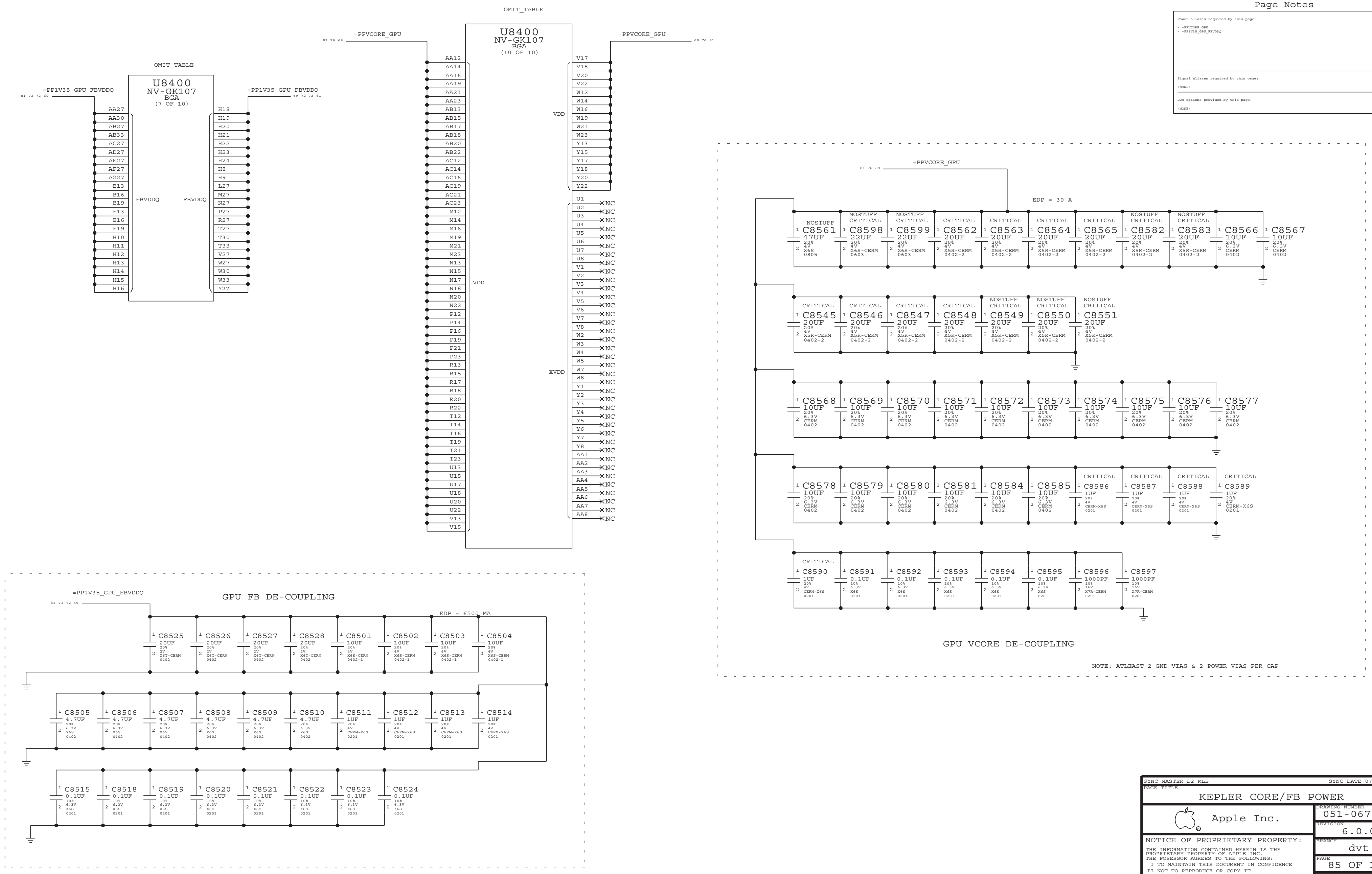
- =PPVCORE_GPU
- =PP1V35_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



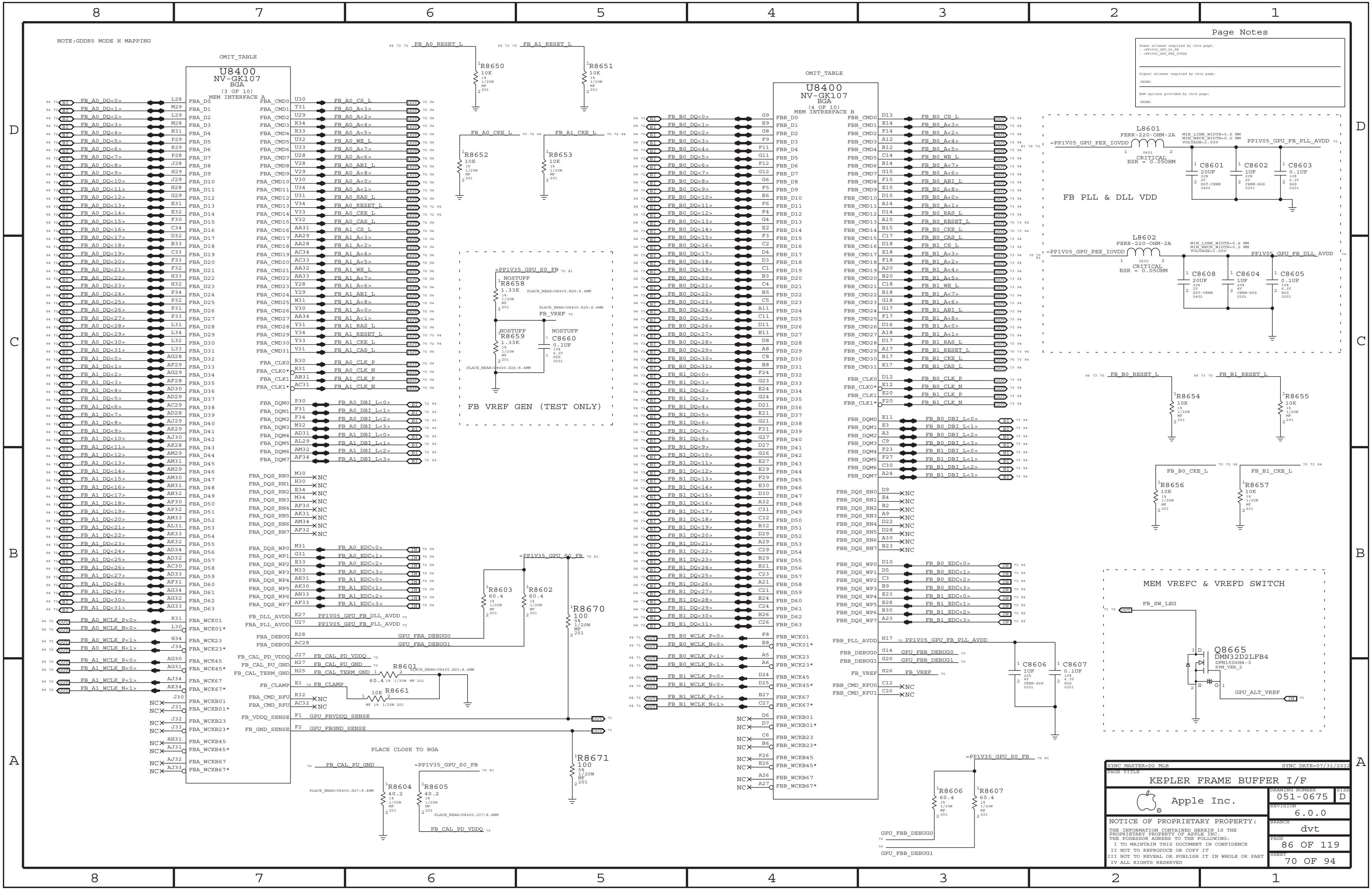
SYNC_MASTER=D2_MLB SYNC_DATE=07/31/2012

PAGE TITLE

KEPLER CORE/FB POWER

Apple Inc.

DRAWING NUMBER	051-0675
SIZE	D
REVISION	6.0.0
BRANCH	dvt
PAGE	85 OF 119
SHEET	69 OF 94



SYNC_MASTER=D2_MLB SYNC_DATE=07/31/2012

PAGE TITLE

KEPLER FRAME BUFFER I/F

Apple Inc.

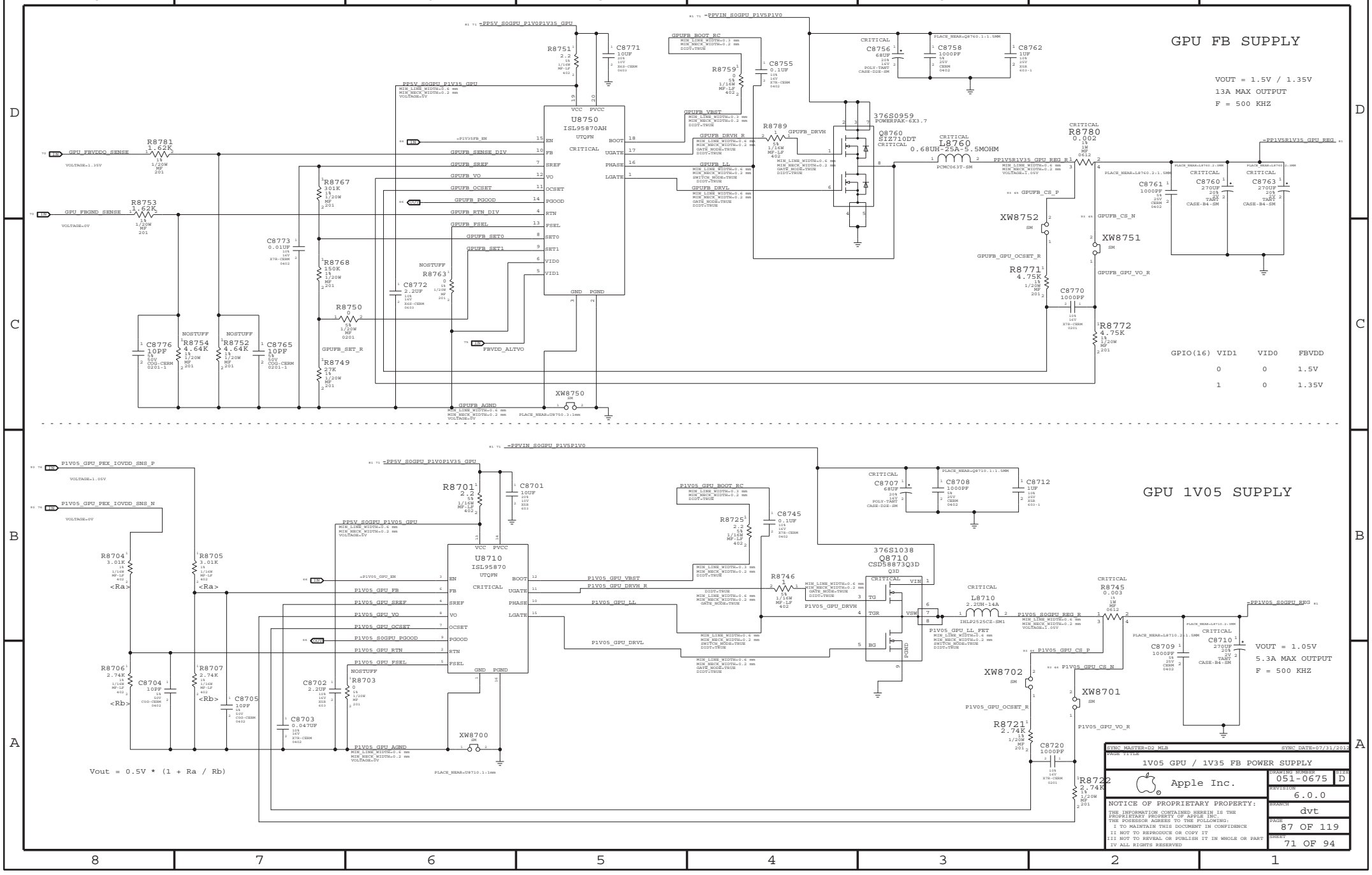
DRAWING NUMBER 051-0675 SIZE D

REVISION 6.0.0

BRANCH dvt

PAGE 86 OF 119

SHEET 70 OF 94


GPU FB SUPPLY
VOUT = 1.5V / 1.35V
13A MAX OUTPUT
F = 500 KHZ
GPIO(16) VID1 VID0 FBVDD
0 0 1.5V
1 0 1.35V
U8750
ISL95870AH
UTQFN
CRITICAL
GPU_FBVDDQ_SENSE
GPU_FBGND_SENSE
GPUFB_SENSE_DIV
GPUFB_SREF
GPUFB_VO
GPUFB_OCSET
GPUFB_PGOOD
GPUFB_RTN_DIV
GPUFB_FSEL
GPUFB_SET0
GPUFB_SET1
GPUFB_BOOT_RC
GPUFB_VBST
GPUFB_DRVH_R
GPUFB_LL
GPUFB_DRVL
GPUFB_DRVH
GPUFB_AGND
GPUFB_SET_R
GPUFB_GPU_OCSET_R
GPUFB_GPU_VO_R
GPUFB_CS_P
GPUFB_CS_N
PP1V5R1V35_GPU_REG_R
=PP1V5R1V35_GPU_REG
=PPVIN_S0GPU_P1V5P1V0
=PP5V_S0GPU_P1V0P1V35_GPU
PP5V_S0GPU_P1V35_GPU
=P1V35PB_EN
FBVDD_ALTVO
Q8760
SI2710DT
376S0959
POWERPAK-6X3.7
L8760
0.68UH-25A-5.5MOHM
PCMC063T-SM
XW8750
XW8751
XW8752
NOSTUFF
P1V05 GPU LL FET
P1V05_GPU_BOOT_RC
P1V05_GPU_VBST
P1V05_GPU_DRVH_R
P1V05_GPU_LL
P1V05_GPU_DRVL
P1V05_GPU_DRVH
P1V05_GPU_AGND
P1V05_GPU_SREF
P1V05_GPU_VO
P1V05_GPU_OCSET
P1V05_GPU_RTN
P1V05_GPU_FSEL
P1V05_S0GPU_PGOOD
P1V05_GPU_EN
P1V05_GPU_CS_P
P1V05_GPU_CS_N
P1V05_GPU_VO_R
P1V05_GPU_OCSET_R
P1V05_S0GPU_REG_R
=PP1V05_S0GPU_REG
Q8710
CSD58873Q3D
Q3D
L8710
2.2UH-14A
IHLP2525CZ-SM1
U8710
ISL95870
VOUT = 1.05V
5.3A MAX OUTPUT
F = 500 KHZ
Vout = 0.5V * (1 + Ra / Rb)
<Ra>
<Rb>
SYNC MASTER=D2 MLB
SYNC DATE=07/31/2012
PAGE TITLE
1V05 GPU / 1V35 FB POWER SUPPLY
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
PAGE
87 OF 119
SHEET
71 OF 94
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Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_PP_VDD

Signal aliases required by this page:
(NONE)

ROM options provided by this page:

CK TERMINATION - A0

CK TERMINATION - A1

U8800
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
(2 OF 2)
OMIT_TABLE

U8850
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
(2 OF 2)
OMIT_TABLE

PLACE CLOSE TO U8800
PLACE CLOSE TO U8850

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 mm

SYNC MASTER=D2_MLB	SYNC DATE=07/31/2012
PAGE TITLE: GDDR5 Frame Buffer A	
Apple Inc.	DRAWING NUMBER: 051-0675 SIZE: D
	REVISION: 6.0.0
	BRANCH: dvt
	PAGE: 88 OF 119
	SHEET: 72 OF 94

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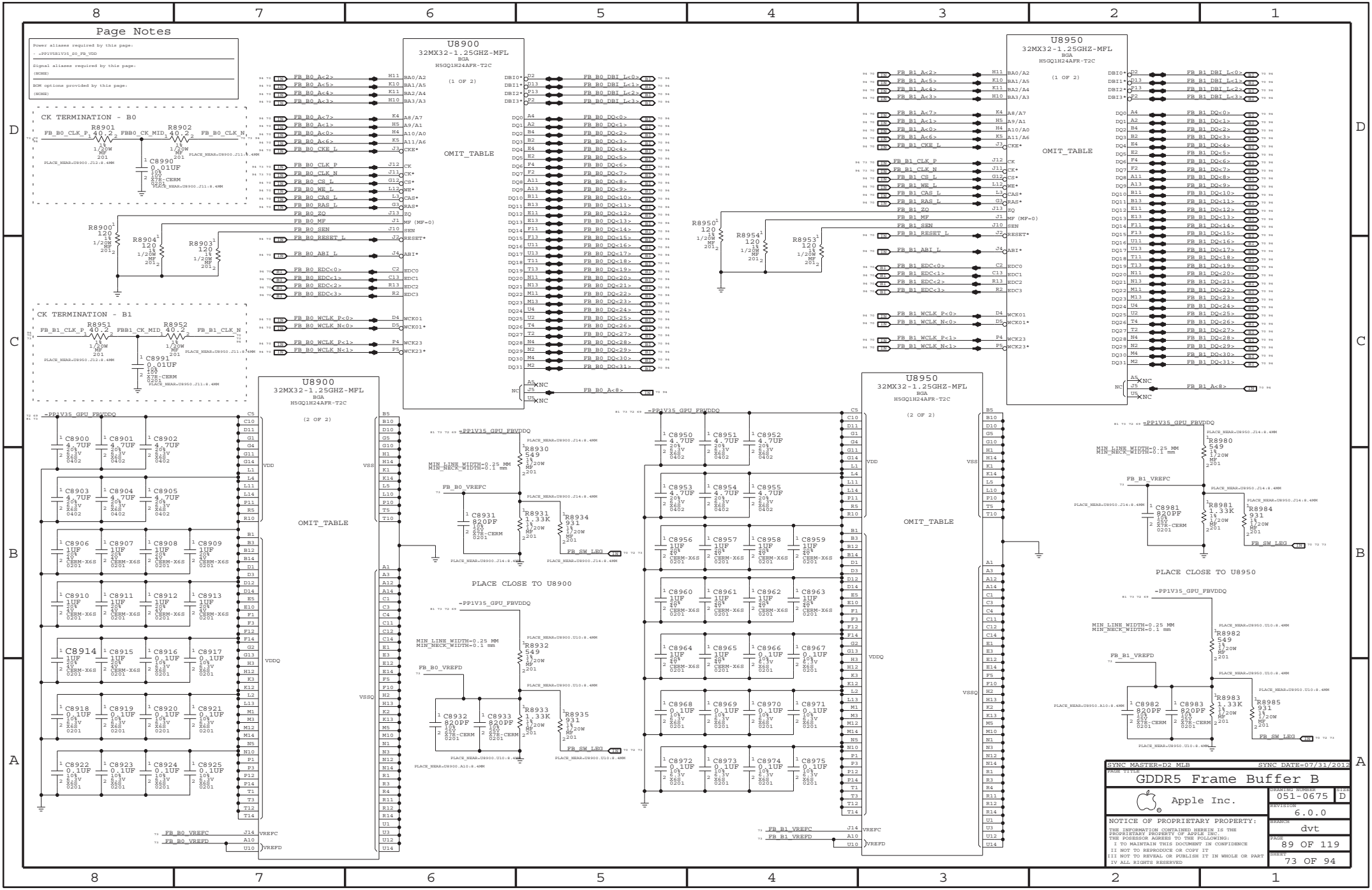
Page Notes
Power aliases required by this page:
- +PP1V5R1V35_S0_PB_VDD
Signal aliases required by this page:
(NONE)
ROM options provided by this page:
(NONE)
CK TERMINATION - B0
CK TERMINATION - B1
U8900
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
(2 OF 2)
U8950
OMIT_TABLE
PLACE CLOSE TO U8900
PLACE CLOSE TO U8950
SYNC MASTER=D2 MLB
SYNC DATE=07/31/2012
PAGE TITLE
GDDR5 Frame Buffer B
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
PAGE
89 OF 119
SHEET
73 OF 94
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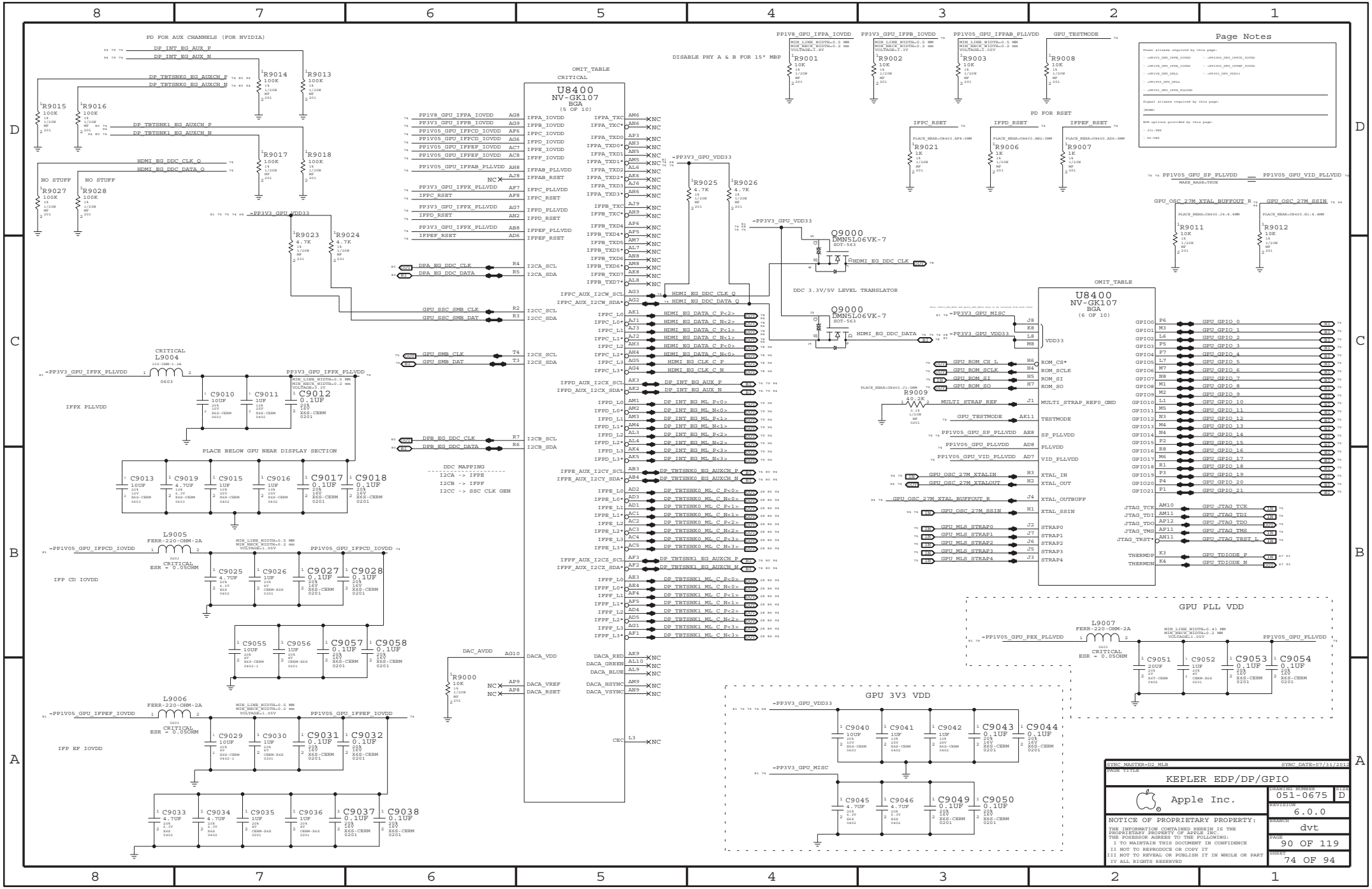
Page Notes
U8400
NV-GK107
BGA
(5 OF 10)
(6 OF 10)
OMIT_TABLE
CRITICAL
PD FOR AUX CHANNELS (FOR NVIDIA)
PD FOR RSET
DISABLE PHY A & B FOR 15" MBP
DDC 3.3V/5V LEVEL TRANSLATOR
DDC MAPPING
I2CA -> IFPE
I2CB -> IFPF
I2CC -> SSC CLK GEN
IFPX PLLVDD
IFP CD IOVDD
IFP EF IOVDD
GPU PLL VDD
GPU 3V3 VDD
Q9000
DMN5L06VK-7
SOT-563
R9009
40.2K
L9004
L9005
L9006
L9007
FERR-220-OHM-2A
C9010
C9011
C9012
0.1UF
C9013
C9019
C9015
C9016
C9017
C9018
C9025
C9026
C9027
C9028
C9055
C9056
C9057
C9058
C9029
C9030
C9031
C9032
C9033
C9034
C9035
C9036
C9037
C9038
C9040
C9041
C9042
C9043
C9044
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C9046
C9049
C9050
C9051
C9052
C9053
C9054
R9000
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R9003
R9008
R9014
R9013
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R9017
R9018
R9027
R9028
R9023
R9024
R9025
R9026
R9021
R9006
R9007
R9011
R9012
GPU_TESTMODE
IFPC_RSET
IFPD_RSET
IFPEF_RSET
GPU_OSC_27M_XTAL_BUFFOUT_R
GPU_OSC_27M_SSIN
DP_TBTSNK0_EG_AUXCH_P
DP_TBTSNK0_EG_AUXCH_N
DP_TBTSNK1_EG_AUXCH_P
DP_TBTSNK1_EG_AUXCH_N
HDMI_EG_DDC_CLK_Q
HDMI_EG_DDC_DATA_Q
NO STUFF
DPA_EG_DDC_CLK
DPA_EG_DDC_DATA
GPU_SSC_SMB_CLK
GPU_SSC_SMB_DAT
GPU_SMB_CLK
GPU_SMB_DAT
DPB_EG_DDC_CLK
DPB_EG_DDC_DATA
HDMI_EG_DDC_DATA
GPU_ROM_CS_L
GPU_ROM_SCLK
GPU_ROM_SI
GPU_ROM_SO
MULTI_STRAP_REF
GPU_MLS_STRAP0
GPU_MLS_STRAP1
GPU_MLS_STRAP2
GPU_MLS_STRAP3
GPU_MLS_STRAP4
GPU_JTAG_TCK
GPU_JTAG_TDI
GPU_JTAG_TDO
GPU_JTAG_TMS
GPU_JTAG_TRST_L
GPU_TDIODP_P
GPU_TDIODN_N
SYNC MASTER-D2 MLB
SYNC DATE-07/31/2012
PAGE TITLE
KEPLER EDP/DP/GPIO
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
PAGE
90 OF 119
SHEET
74 OF 94
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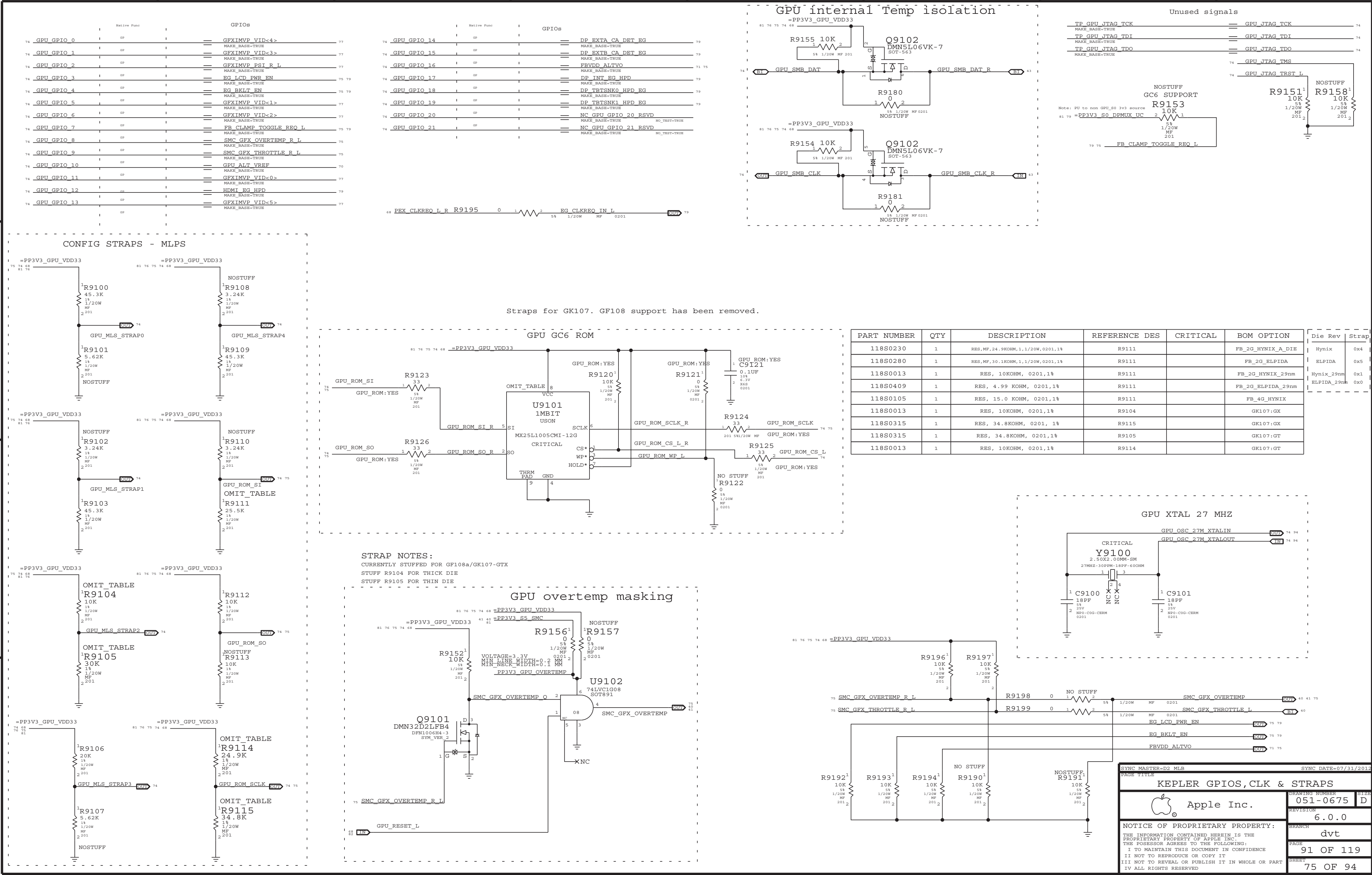

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0230	1	RES,MF,24.9KOHM,1,1/20W,0201,1%	R9111		FB_2G_HYNIX_A_DIE
118S0280	1	RES,MF,30.1KOHM,1,1/20W,0201,1%	R9111		FB_2G_ELPIDA
118S0013	1	RES, 10KOHM, 0201,1%	R9111		FB_2G_HYNIX_29nm
118S0409	1	RES, 4.99 KOHM, 0201,1%	R9111		FB_2G_ELPIDA_29nm
118S0105	1	RES, 15.0 KOHM, 0201,1%	R9111		FB_4G_HYNIX
118S0013	1	RES, 10KOHM, 0201,1%	R9104		GK107:GX
118S0315	1	RES, 34.8KOHM, 0201, 1%	R9115		GK107:GX
118S0315	1	RES, 34.8KOHM, 0201,1%	R9105		GK107:GT
118S0013	1	RES, 10KOHM, 0201,1%	R9114		GK107:GT

Die Rev	Strap
Hynix	0x4
ELPIDA	0x5
Hynix_29nm	0x1
ELPIDA_29nm	0x0

SYNC MASTER=D2 MLB SYNC DATE=07/31/2012

PAGE TITLE

KEPLER GPIOS,CLK & STRAPS

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D

REVISION 6.0.0

BRANCH dvt

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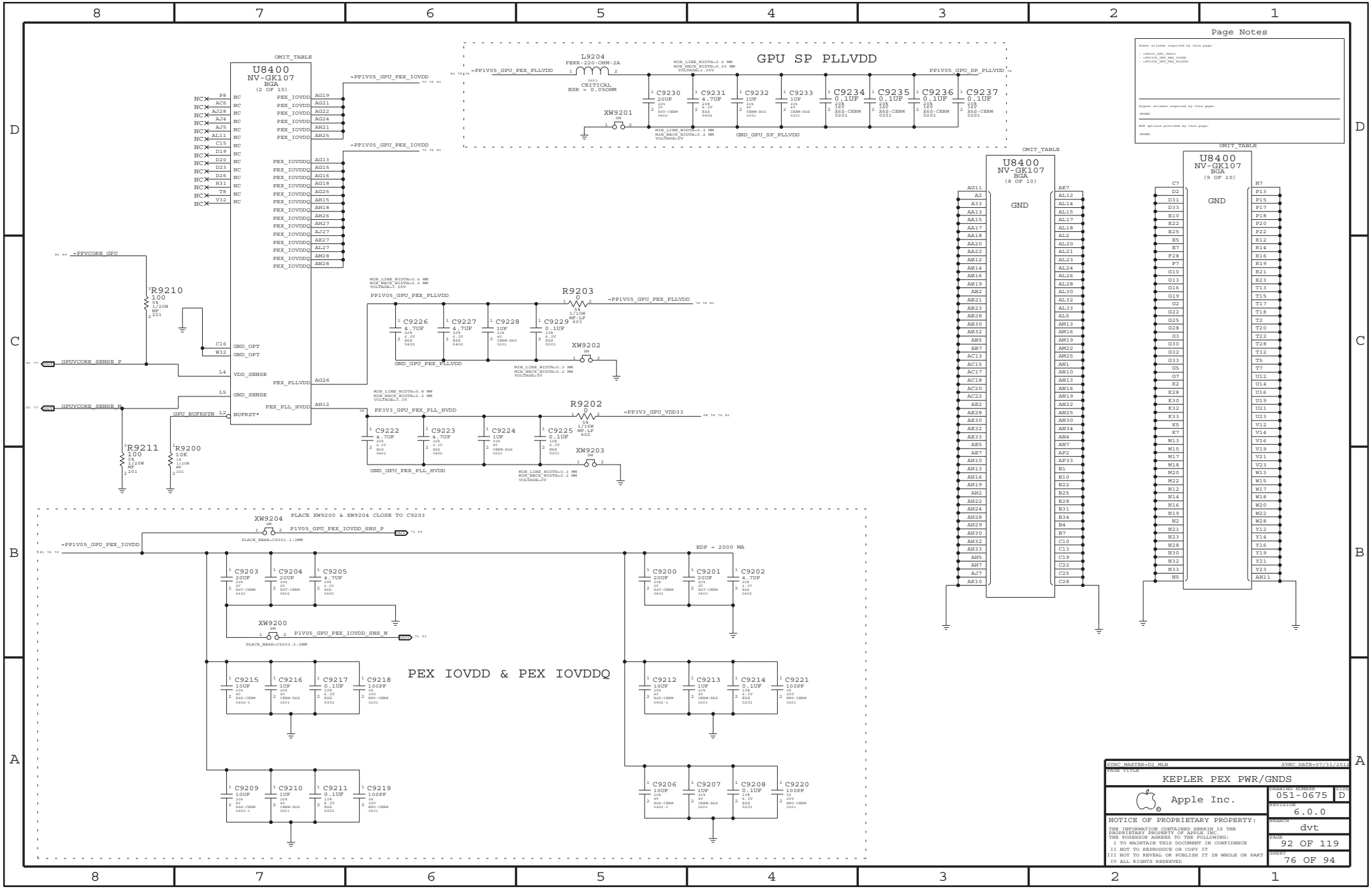
SHEET 75 OF 94


GPU SP PLLVDD
PEX IOVDD & PEX IOVDDQ
U8400
NV-GK107
BGA
(2 OF 10)
(8 OF 10)
(9 OF 10)
GND
OMIT_TABLE
L9204
FERR-220-OHM-2A
CRITICAL
ESR = 0.05OHM
R9210
R9211
R9200
R9203
R9202
XW9201
XW9202
XW9203
XW9204
XW9200
PLACE XW9200 & XW9204 CLOSE TO C9203
EDP = 2000 MA
=PPVCORE_GPU
=PP1V05_GPU_PEX_IOVDD
=PP1V05_GPU_PEX_PLLVDD
=PP1V05_GPU_SP_PLLVDD
=PP3V3_GPU_VDD33
GPUVCORE_SENSE_P
GPUVCORE_SENSE_N
GPU_BUFRSTN
GND_GPU_SP_PLLVDD
GND_GPU_PEX_PLLVDD
GND_GPU_PEX_PLL_HVDD
Page Notes
KEPLER PEX PWR/GNDS
Apple Inc.
051-0675
6.0.0
dvt
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SYNC MASTER-D2 MLB
SYNC DATE-07/31/2012
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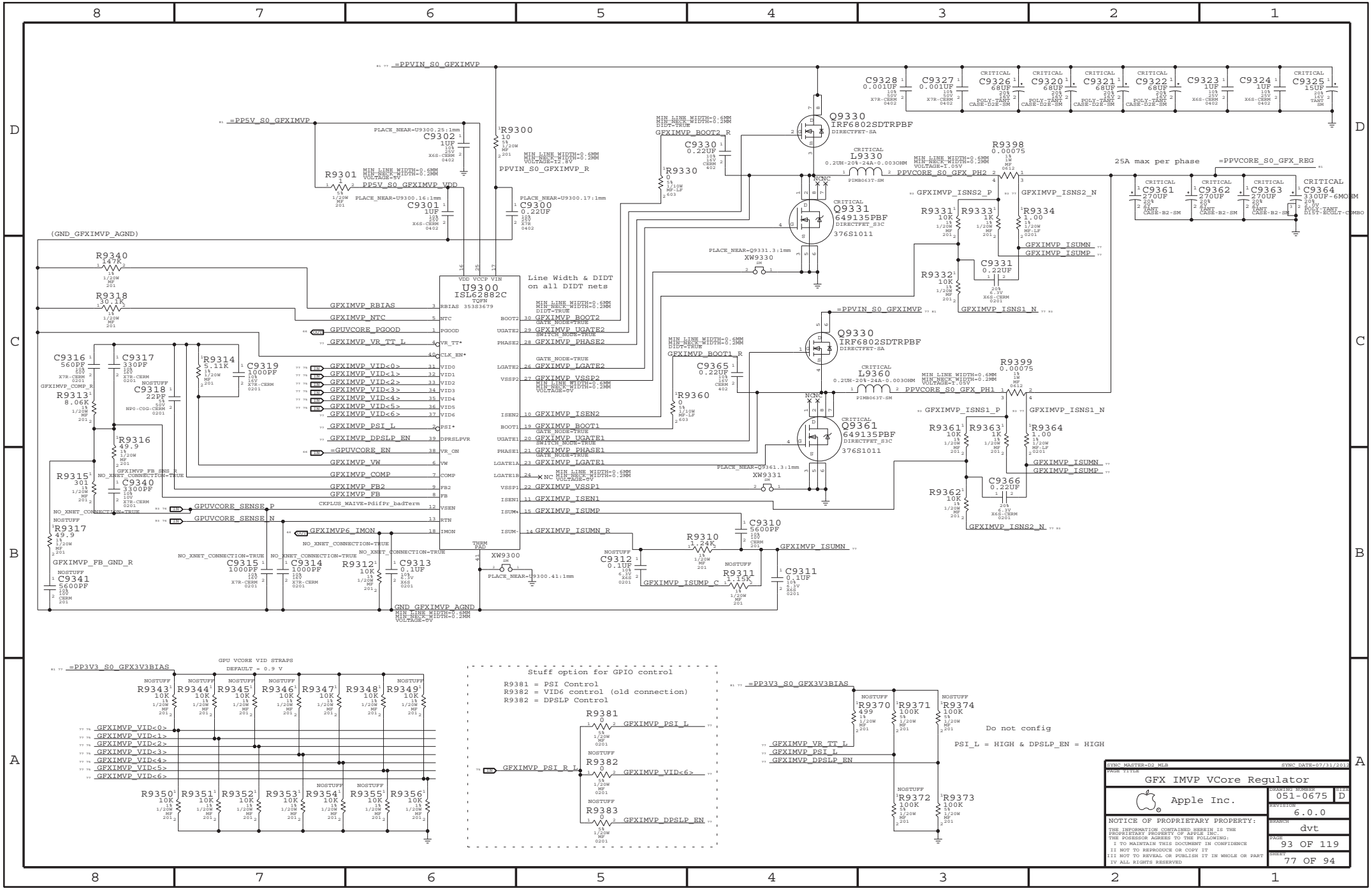
=PPVIN_S0_GFXIMVP
=PP5V_S0_GFXIMVP
PP5V_S0_GFXIMVP_VDD
PPVIN_S0_GFXIMVP_R
(GND_GFXIMVP_AGND)
U9300
ISL62882C
TQFN
Line Width & DIDT on all DIDT nets
GFXIMVP_RBIAS
GFXIMVP_NTC
GPUVCORE_PGOOD
GFXIMVP_VR_TT_L
GFXIMVP_VID<0>
GFXIMVP_VID<1>
GFXIMVP_VID<2>
GFXIMVP_VID<3>
GFXIMVP_VID<4>
GFXIMVP_VID<5>
GFXIMVP_VID<6>
GFXIMVP_PSI_L
GFXIMVP_DPSLP_EN
=GPUVCORE_EN
GFXIMVP_VW
GFXIMVP_COMP
GFXIMVP_FB2
GFXIMVP_FB
GPUVCORE_SENSE_P
GPUVCORE_SENSE_N
GFXIMVP6_IMON
GFXIMVP_BOOT2
GFXIMVP_UGATE2
GFXIMVP_PHASE2
GFXIMVP_LGATE2
GFXIMVP_VSSP2
GFXIMVP_BOOT1
GFXIMVP_UGATE1
GFXIMVP_PHASE1
GFXIMVP_LGATE1
GFXIMVP_VSSP1
GFXIMVP_ISEN2
GFXIMVP_ISEN1
GFXIMVP_ISUMP
GFXIMVP_ISUMN_R
GFXIMVP_ISUMN
GFXIMVP_ISUMP
Q9330
IRF6802SDTRPBF
DIRECTFET-SA
Q9331
649135PBF
DIRECTFET_S3C
376S1011
Q9361
L9330
L9360
0.2UH-20%-24A-0.003OHM
PIMB063T-SM
PPVCORE_S0_GFX_PH2
PPVCORE_S0_GFX_PH1
25A max per phase
=PPVCORE_S0_GFX_REG
GFXIMVP_ISNS2_P
GFXIMVP_ISNS2_N
GFXIMVP_ISNS1_N
GFXIMVP_ISNS1_P
GFXIMVP_FB_GND_R
GFXIMVP_ISUMP_C
GND_GFXIMVP_AGND
=PP3V3_S0_GFX3V3BIAS
GPU VCORE VID STRAPS
DEFAULT = 0.9 V
Stuff option for GPIO control
R9381 = PSI Control
R9382 = VID6 control (old connection)
R9382 = DPSLP Control
GFXIMVP_PSI_R_L
Do not config
PSI_L = HIGH & DPSLP_EN = HIGH
SYNC MASTER-D2 MLB
SYNC DATE-07/31/2012
PAGE TITLE
GFX IMVP VCore Regulator
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
PAGE
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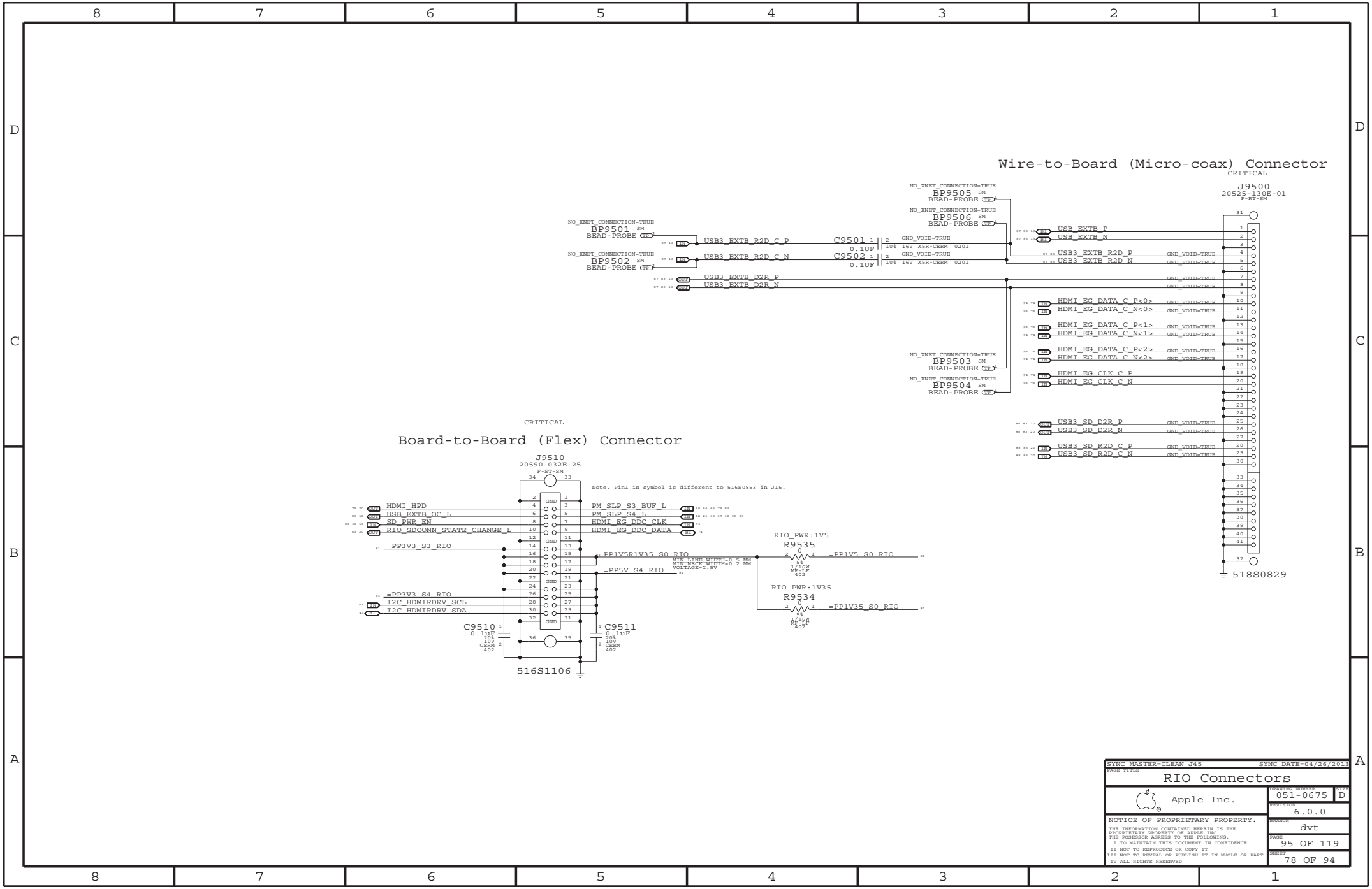

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE

RIO Connectors

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D

REVISION 6.0.0

BRANCH dvt

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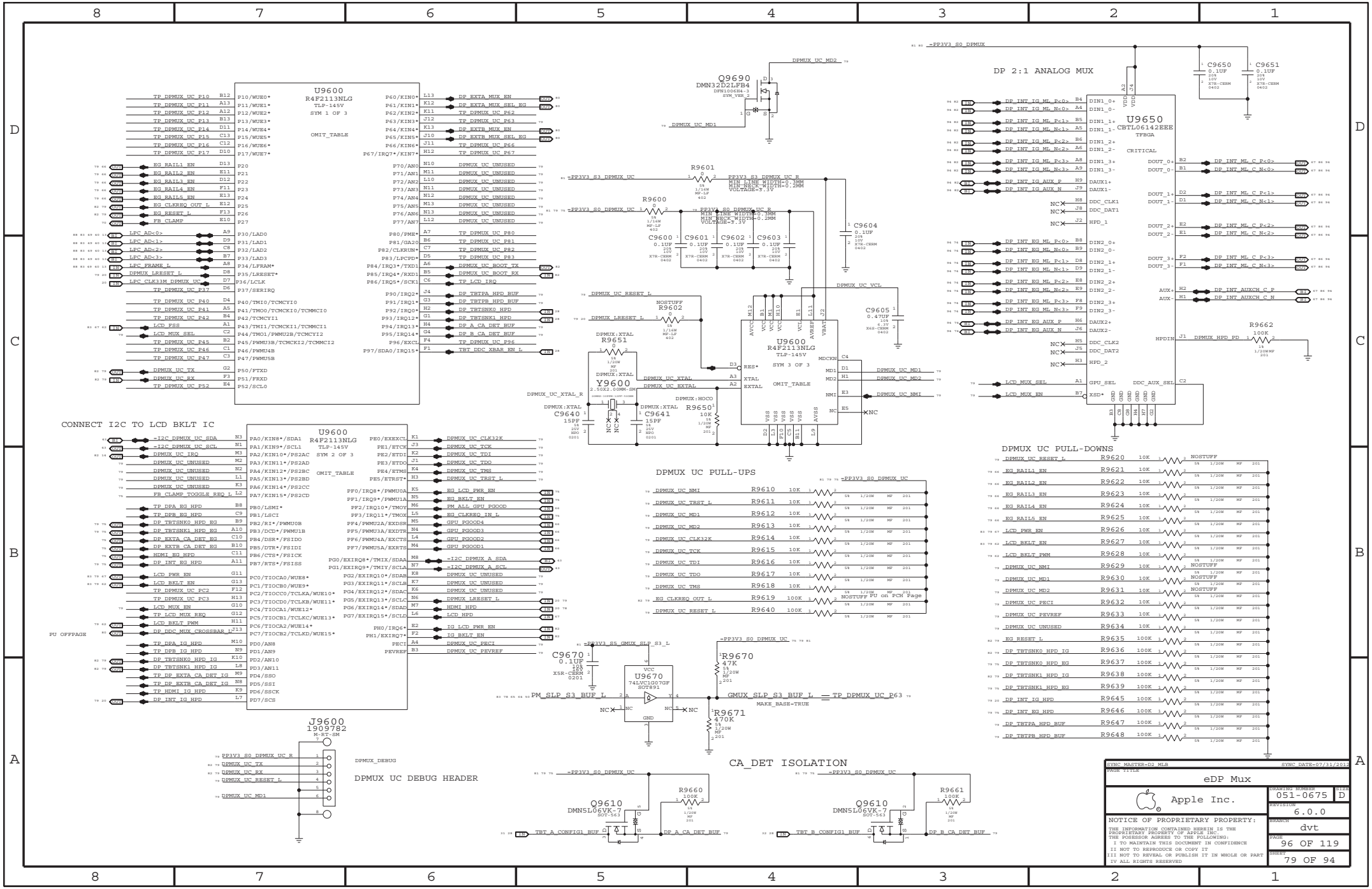
U9600
R4F2113NLG
TLP-145V
SYM 1 OF 3
OMIT_TABLE
U9600
R4F2113NLG
TLP-145V
SYM 2 OF 3
OMIT_TABLE
U9600
R4F2113NLG
TLP-145V
SYM 3 OF 3
OMIT_TABLE
DP 2:1 ANALOG MUX
U9650
CBTL06142EEE
TFBGA
CRITICAL
CONNECT I2C TO LCD BKLT IC
DPMUX UC PULL-UPS
DPMUX UC PULL-DOWNS
CA_DET ISOLATION
DPMUX UC DEBUG HEADER
J9600
1909782
M-RT-SM
Q9690
DMN32D2LFB4
Q9610
DMN5L06VK-7
U9670
74LVC1G07GF
Y9600
R9601
R9602
R9651
R9650
R9660
R9661
R9662
C9650
C9651
C9604
C9605
C9640
C9641
C9670
PU OFFPAGE
MAKE_BASE=TRUE
NOSTUFF
eDP Mux
Apple Inc.
SYNC MASTER-D2 MLB
SYNC DATE-07/31/2012
DRAWING NUMBER
051-0675
REVISION
6.0.0
BRANCH
dvt
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79 OF 94
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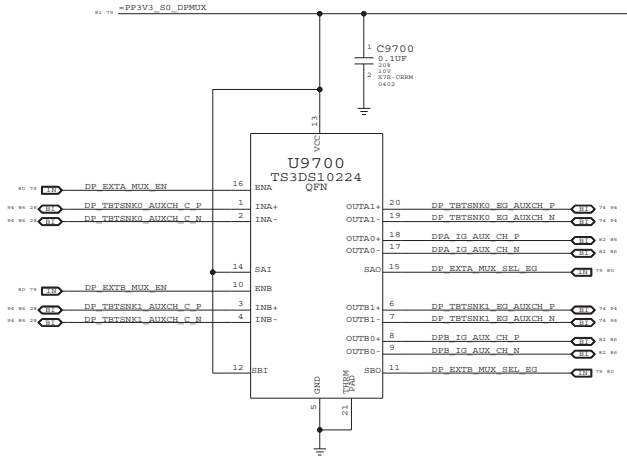
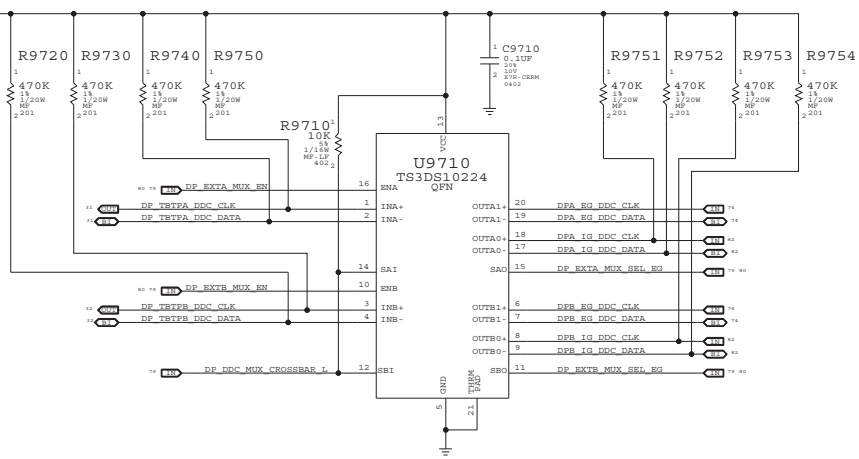
DP A & DP B AUX MUX



DP A & DP B DDC MUX



MUX TRUTH TABLE

SAI/SBI	SAO	SBO	INA	INB
0	0	0	OUTB0	OUTA0
0	0	1	OUTB1	OUTA0
0	1	0	OUTB0	OUTA1
0	1	1	OUTB1	OUTA1
1	0	0	OUTA0	OUTB0
1	0	1	OUTA0	OUTB1
1	1	0	OUTA1	OUTB0
1	1	1	OUTA1	OUTB1

SYNC MASTER-CLEAN_D2 SYNC DATE=08/14/2012

PAGE TITLE: eDP Muxed Graphics Support

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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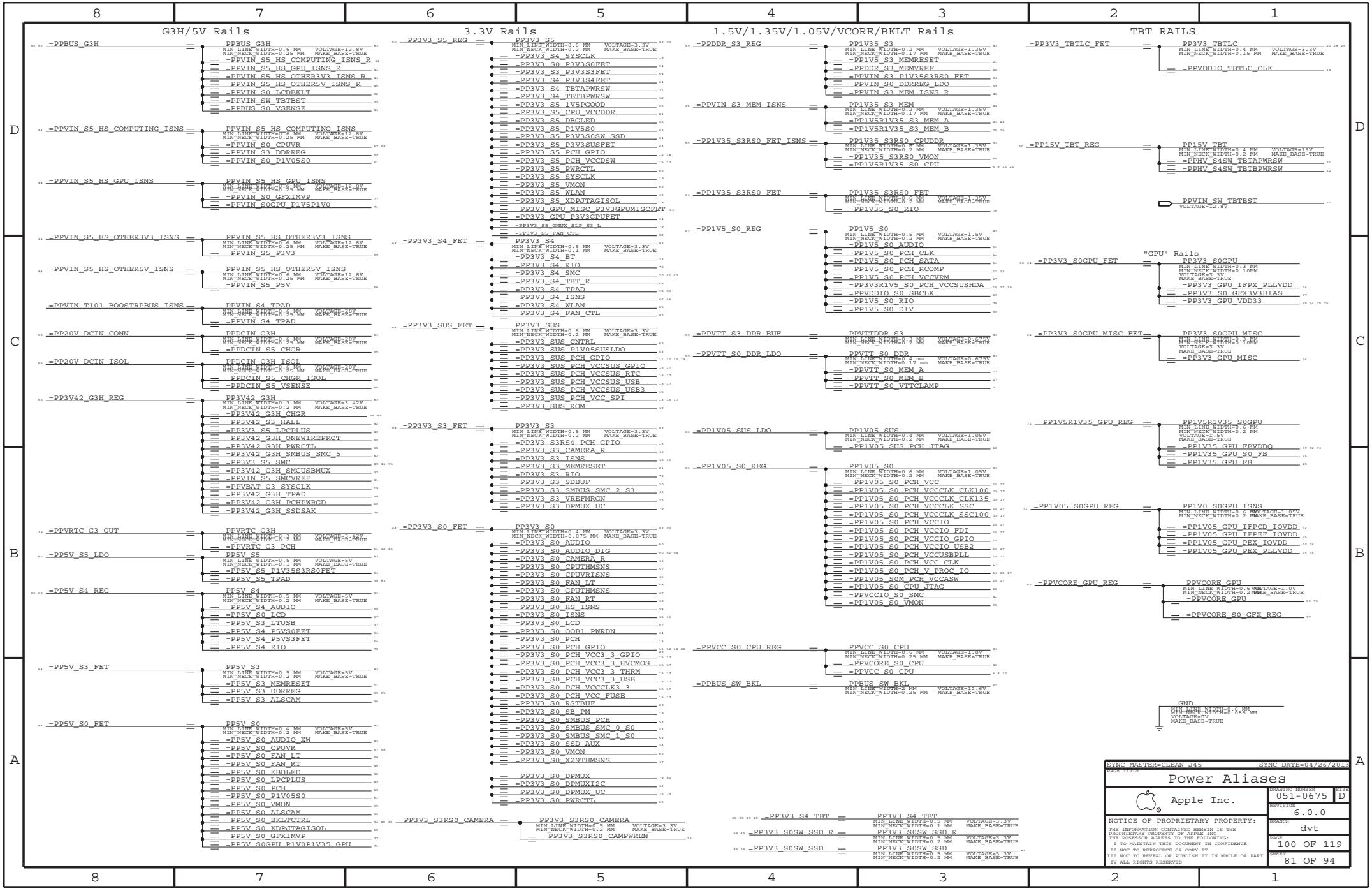
G3H/5V Rails
3.3V Rails
1.5V/1.35V/1.05V/VCORE/BKLT Rails
TBT RAILS
=PPBUS_G3H
PPBUS_G3H
=PPVIN_S5_HS_COMPUTING_ISNS_R
=PPVIN_S5_HS_GPU_ISNS_R
=PPVIN_S5_HS_OTHER3V3_ISNS_R
=PPVIN_S5_HS_OTHER5V_ISNS_R
=PPVIN_S0_LCDBKLT
=PPVIN_SW_TBTBST
=PPBUS_S0_VSENSE
=PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
=PPVIN_S0_CPUVR
=PPVIN_S3_DDRREG
=PPVIN_S0_P1V05S0
=PPVIN_S5_HS_GPU_ISNS
PPVIN_S5_HS_GPU_ISNS
=PPVIN_S0_GFXIMVP
=PPVIN_S0GPU_P1V5P1V0
=PPVIN_S5_HS_OTHER3V3_ISNS
PPVIN_S5_HS_OTHER3V3_ISNS
=PPVIN_S5_P3V3
=PPVIN_S5_HS_OTHER5V_ISNS
PPVIN_S5_HS_OTHER5V_ISNS
=PPVIN_S5_P5V
=PPVIN_T101_BOOSTRPBUS_ISNS
PPVIN_S4_TPAD
=PPVIN_S4_TPAD
=PP20V_DCIN_CONN
PPDCIN_G3H
=PPDCIN_S5_CHGR
=PP20V_DCIN_ISOL
PPDCIN_G3H_ISOL
=PPDCIN_S5_CHGR_ISOL
=PPDCIN_S5_VSENSE
=PP3V42_G3H_REG
PP3V42_G3H
=PP3V42_G3H_CHGR
=PP3V42_S3_HALL
=PP3V3_S5_LPCPLUS
=PP3V42_G3H_ONEWIREPROT
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_SMBUS_SMC_5
=PP3V3_S5_SMC
=PP3V42_G3H_SMCUSBMUX
=PPVIN_S5_SMCVREF
=PPVBAT_G3_SYSCLK
=PP3V42_G3H_TPAD
=PP3V42_G3H_PCHPWRGD
=PP3V42_G3H_SSDSAK
=PPVRTC_G3_OUT
PPVRTC_G3H
=PPVRTC_G3_PCH
=PP5V_S5_LDO
PP5V_S5
=PP5V_S5_P1V35S3RS0FET
=PP5V_S5_TPAD
=PP5V_S4_REG
PP5V_S4
=PP5V_S4_AUDIO
=PP5V_S0_LCD
=PP5V_S3_LCDLB
=PP5V_S4_P5VS0FET
=PP5V_S4_P5VS3FET
=PP5V_S4_RIO
=PP5V_S3_FET
PP5V_S3
=PP5V_S3_MEMRESET
=PP5V_S3_DDRREG
=PP5V_S3_ALSCAM
=PP5V_S0_FET
PP5V_S0
=PP5V_S0_AUDIO_XW
=PP5V_S0_CPUVR
=PP5V_S0_FAN_LT
=PP5V_S0_FAN_RT
=PP5V_S0_KBDLED
=PP5V_S0_LPCPLUS
=PP5V_S0_PCH
=PP5V_S0_P1V05S0
=PP5V_S0_VMON
=PP5V_S0_ALSCAM
=PP5V_S0_BKLTCTRL
=PP5V_S0_XDPJTAGISOL
=PP5V_S0_GFXIMVP
=PP5V_S0GPU_P1V0P1V35_GPU
=PP3V3_S5_REG
PP3V3_S5
=PP3V3_S4_SYSCLK
=PP3V3_S0_P3V3S0FET
=PP3V3_S3_P3V3S3FET
=PP3V3_S4_P3V3S4FET
=PP3V3_S4_TBTAPWRSW
=PP3V3_S4_TBTBPWRSW
=PP3V3_S5_1V5PGOOD
=PP3V3_S5_CPU_VCCDDR
=PP3V3_S5_DBGLED
=PP3V3_S5_P1V5S0
=PP3V3_S5_P3V3S0SW_SSD
=PP3V3_S5_P3V3SUSPET
=PP3V3_S5_PCH_GPIO
=PP3V3_S5_PCH_VCCDSW
=PP3V3_S5_PWRCTL
=PP3V3_S5_SYSCLK
=PP3V3_S5_VMON
=PP3V3_S5_WLAN
=PP3V3_S5_XDPJTAGISOL
=PP3V3_GPU_MISC_P3V3GPUMISCFET
=PP3V3_GPU_P3V3GPUFET
=PP3V3_S4_FET
PP3V3_S4
=PP3V3_S4_BT
=PP3V3_S4_RIO
=PP3V3_S4_SMC
=PP3V3_S4_TBT_R
=PP3V3_S4_TPAD
=PP3V3_S4_ISNS
=PP3V3_S4_WLAN
=PP3V3_S4_FAN_CTL
=PP3V3_SUS_FET
PP3V3_SUS
=PP3V3_SUS_CNTRL
=PP3V3_SUS_P1V05SUSLDO
=PP3V3_SUS_PCH_GPIO
=PP3V3_SUS_PCH_VCCSUS_GPIO
=PP3V3_SUS_PCH_VCCSUS_RTC
=PP3V3_SUS_PCH_VCCSUS_USB
=PP3V3_SUS_PCH_VCCSUS_USB3
=PP3V3_SUS_PCH_VCC_SPI
=PP3V3_SUS_ROM
=PP3V3_S3_FET
PP3V3_S3
=PP3V3_S3RS4_PCH_GPIO
=PP3V3_S3_CAMERA_R
=PP3V3_S3_ISNS
=PP3V3_S3_MEMRESET
=PP3V3_S3_RIO
=PP3V3_S3_SDBUF
=PP3V3_S3_SMBUS_SMC_2_S3
=PP3V3_S3_VREFMRGN
=PP3V3_S3_DPMUX_UC
=PP3V3_S0_FET
PP3V3_S0
=PP3V3_S0_AUDIO
=PP3V3_S0_AUDIO_DIG
=PP3V3_S0_CAMERA_R
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_CPUVRISNS
=PP3V3_S0_FAN_LT
=PP3V3_S0_GPUTHMSNS
=PP3V3_S0_FAN_RT
=PP3V3_S0_HS_ISNS
=PP3V3_S0_ISNS
=PP3V3_S0_LCD
=PP3V3_S0_OOB1_PWRDN
=PP3V3_S0_PCH
=PP3V3_S0_PCH_GPIO
=PP3V3_S0_PCH_VCC3_3_GPIO
=PP3V3_S0_PCH_VCC3_3_HVCMOS
=PP3V3_S0_PCH_VCC3_3_THRM
=PP3V3_S0_PCH_VCC3_3_USB
=PP3V3_S0_PCH_VCCCLK3_3
=PP3V3_S0_PCH_VCC_FUSE
=PP3V3_S0_RSTBUP
=PP3V3_S0_SB_PM
=PP3V3_S0_SMBUS_PCH
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_1_S0
=PP3V3_S0_SSD_AUX
=PP3V3_S0_VMON
=PP3V3_S0_X29THMSNS
=PP3V3_S0_DPMUX
=PP3V3_S0_DPMUXI2C
=PP3V3_S0_DPMUX_UC
=PP3V3_S0_PWRCTL
=PP3V3_S3RS0_CAMERA
PP3V3_S3RS0_CAMERA
=PP3V3_S3RS0_CAMPWREN
=PPDDR_S3_REG
PP1V35_S3
=PP1V5_S3_MEMRESET
=PPDDR_S3_MEMVREF
=PPVIN_S3_P1V35S3RS0_FET
=PPVIN_S0_DDRREG_LDO
=PPVIN_S3_MEM_ISNS_R
=PPVIN_S3_MEM_ISNS
PP1V35_S3_MEM
=PP1V5R1V35_S3_MEM_A
=PP1V5R1V35_S3_MEM_B
=PP1V35_S3RS0_FET_ISNS
PP1V35_S3RS0_CPUDDR
=PP1V35_S3RS0_VMON
=PP1V5R1V35_S0_CPU
=PP1V35_S3RS0_FET
PP1V35_S3RS0_FET
=PP1V35_S0_RIO
=PP1V5_S0_REG
PP1V5_S0
=PP1V5_S0_AUDIO
=PP1V5_S0_PCH_CLK
=PP1V5_S0_PCH_SATA
=PP1V5_S0_PCH_RCOMP
=PP1V5_S0_PCH_VCCVRM
=PP3V3R1V5_S0_PCH_VCCSUSHDA
=PPVDDIO_S0_SBCLK
=PP1V5_S0_RIO
=PP1V5_S0_DIV
=PPVTT_S3_DDR_BUF
PPVTTDDR_S3
=PPVTT_S0_DDR_LDO
PPVTT_S0_DDR
=PPVTT_S0_MEM_A
=PPVTT_S0_MEM_B
=PPVTT_S0_VTTCLAMP
=PP1V05_SUS_LDO
PP1V05_SUS
=PP1V05_SUS_PCH_JTAG
=PP1V05_S0_REG
PP1V05_S0
=PP1V05_S0_PCH_VCC
=PP1V05_S0_PCH_VCCCLK_CLK100
=PP1V05_S0_PCH_VCCCLK_CLK135
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=PP1V05_S0_PCH_VCCIO
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=PP1V05_S0_PCH_VCCIO_GPIO
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=PP1V05_S0_PCH_VCCUSBPLL
=PP1V05_S0_PCH_VCC_CLK
=PP1V05_S0_PCH_V_PROC_IO
=PP1V05_S0M_PCH_VCCASW
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=PPVCCIO_S0_SMC
=PP1V05_S0_VMON
=PPVCC_S0_CPU_REG
PPVCC_S0_CPU
=PPVCORE_S0_CPU
=PPVCC_S0_CPU
=PPBUS_SW_BKL
PPBUS_SW_BKL
=PP3V3_S4_TBT
PP3V3_S4_TBT
=PP3V3_S0SW_SSD_R
PP3V3_S0SW_SSD_R
=PP3V3_S0SW_SSD
PP3V3_S0SW_SSD
=PP3V3_TBTLC_FET
PP3V3_TBTLC
=PPVDDIO_TBTLC_CLK
=PP15V_TBT_REG
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=PPHV_S4SW_TBTAPWRSW
=PPHV_S4SW_TBTBPWRSW
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VOLTAGE=12.6V
"GPU" Rails
=PP3V3_S0GPU_FET
PP3V3_S0GPU
=PP3V3_GPU_IFPX_PLLVDD
=PP3V3_S0_GFX3V3BIAS
=PP3V3_GPU_VDD33
=PP3V3_S0GPU_MISC_FET
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=PP3V3_GPU_MISC
=PP1V5R1V35_GPU_REG
PP1V5R1V35_S0GPU
=PP1V35_GPU_FBVDDQ
=PP1V35_GPU_S0_FB
=PP1V35_GPU_FB
=PP1V05_S0GPU_REG
PP1V0_S0GPU_ISNS
=PP1V05_GPU_IFPCD_IOVDD
=PP1V05_GPU_IFPEF_IOVDD
=PP1V05_GPU_PEX_IOVDD
=PP1V05_GPU_PEX_PLLVDD
=PPVCORE_GPU_REG
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MIN_NECK_WIDTH=0.085 MM
VOLTAGE=0V
MAKE_BASE=TRUE
SYNC MASTER=CLEAN J45
SYNC DATE=04/26/2013
PAGE TITLE
Power Aliases
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
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Display Aliases

EDP_IG_PANEL_PWR = IG_LCD_PWR_EN
EDP_IG_BKL_ON = IG_BKLT_EN

DP_INT_IG_ML_P<3..0> = TP_DP_IG_A_MLP<3..0>
DP_INT_IG_ML_N<3..0> = TP_DP_IG_A_MLN<3..0>
DP_INT_IG_AUX_P = TP_DP_IG_A_AUXCHP
DP_INT_IG_AUX_N = TP_DP_IG_A_AUXCHN

DPA_IG_AUX_CH_P = TP_DP_IG_B_AUXCHP
DPA_IG_AUX_CH_N = TP_DP_IG_B_AUXCHN
DPB_IG_AUX_CH_P = TP_DP_IG_C_AUXCHP
DPB_IG_AUX_CH_N = TP_DP_IG_C_AUXCHN
DPA_IG_DDC_CLK = TP_DP_IG_B_DDC_CLK
DPA_IG_DDC_DATA = TP_DP_IG_B_DDC_DATA
DPB_IG_DDC_CLK = TP_DP_IG_C_DDC_CLK
DPB_IG_DDC_DATA = TP_DP_IG_C_DDC_DATA
DP_TBTSNK0_HPD_IG = TP_DP_IG_B_HPD
DP_TBTSNK1_HPD_IG = TP_DP_IG_C_HPD
DPMUX_UC_RX = DPMUX_UC_BOOT_RX
DPMUX_UC_TX = DPMUX_UC_BOOT_TX

EG_RESET_L = GPU_RESET_L
PEG_CLKREQ_L = EG_CLKREQ_OUT_L

DP_AUXCH_ISOL_L = DP_AUXIO_EN

CPU signals

MEMVTT_EN = =DDRVTT_EN

PEG_D2R_P<7..0> = =PEG_D2R_P<7..0>
PEG_D2R_N<7..0> = =PEG_D2R_N<7..0>
PEG_R2D_C_P<7..0> = =PEG_R2D_C_P<7..0>
PEG_R2D_C_N<7..0> = =PEG_R2D_C_N<7..0>

NC_PCIE_PEG_D2RP<15..12> = =PEG_D2R_P<15..12>
NC_PCIE_PEG_D2RN<15..12> = =PEG_D2R_N<15..12>
NC_PCIE_PEG_R2D_CP<15..12> = =PEG_R2D_C_P<15..12>
NC_PCIE_PEG_R2D_CN<15..12> = =PEG_R2D_C_N<15..12>

Thunderbolt Signals Through PEG

PCIE_TBT_D2R_P<3..0> = =PEG_D2R_P<11..8>
PCIE_TBT_D2R_N<3..0> = =PEG_D2R_N<11..8>
PCIE_TBT_R2D_C_P<3..0> = =PEG_R2D_C_P<11..8>
PCIE_TBT_R2D_C_N<3..0> = =PEG_R2D_C_N<11..8>

PEG_CLK100M_N = TP_PCIE_CLK100M_GPUN
PEG_CLK100M_P = TP_PCIE_CLK100M_GPUP

=PP3V3_S3_FAN_CTL = PP3V3_S3_FAN_CTL
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

RA201
0
5%
1/20W
MF
0201
=PP3V3_S5_FAN_CTL
RA202
0
5%
1/20W
MF
0201
=PP3V3_S4_FAN_CTL
NOSTUFF

TP_P1V8GPU_EN = =P1V8GPU_EN

Unused signals

BT_PWRRST_L
MEM_VDD_SEL_1V5_L
FW_PWR_EN_PCH
WOL_EN
FW_PME_L
DP_TBT_SEL
ENET_MEDIA_SENSE_RDIV
AUD_IPHS_SWITCH_EN_PCH
AUD_IP_PERIPHERAL_DET
AUD_I2C_INT_L
TBT_GO2SX_BIDIR
DPMUX_UC_IRQ
PEG_CLKREQ_L
ENET_CLKREQ_L
ENET_LOW_PWR_PCH
HDMITBTMUX_SEL_TBT
SDCONN_OC_L

VOLTAGE MAKE_BASE

PPVREF_S3_MEM_VREFDQ_A = 0.675V TRUE PP0V75_S3_MEM_VREFDQ_A
PPVREF_S3_MEM_VREFDQ_B = 0.675V TRUE PP0V75_S3_MEM_VREFDQ_B
PPVREF_S3_MEM_VREFCA_A = 0.675V TRUE PP0V75_S3_MEM_VREFCA_A
PPVREF_S3_MEM_VREFCA_B = 0.675V TRUE PP0V75_S3_MEM_VREFCA_B

=PP5V_S0_AUDIO_XW
XWA202
SM
PP5V_S0_AUDIO_AMP_L
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
XWA203
SM
PP5V_S0_AUDIO_AMP_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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Signal Aliases

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Functional Test Points

J3501 - airport

FUNC_TEST		
TRUE	AP_CLKREQ_Q_L	33
TRUE	AP_RESET_CONN_L	33
TRUE	PCIE_AP_D2R_PI_N	33 88
TRUE	PCIE_AP_D2R_PI_P	33 88
TRUE	PCIE_AP_R2D_N	33 88
TRUE	PCIE_AP_R2D_P	33 88
TRUE	PCIE_CLK100M_AP_CONN_N	33 88
TRUE	PCIE_CLK100M_AP_CONN_P	33 88
TRUE	PCIE_WAKE_L	12 33 35 88
TRUE	PP3V3_S3RS4_BT_F	33
TRUE	PP3V3_WLAN	33 61
TRUE	USB_BT_CONN_N	33 87
TRUE	USB_BT_CONN_P	33 87
TRUE	WIFI_EVENT_L	33 40 41
TRUE	GND	4X

J4002 - Camera

TRUE	MIPI_CLK_CONN_N	36 91
TRUE	MIPI_CLK_CONN_P	36 91
TRUE	CAM_SENSOR_WAKE_L_CONN	36
TRUE	MIPI_DATA_CONN_N	36 91
TRUE	MIPI_DATA_CONN_P	36 91
TRUE	=I2C_ALS_SDA	36 63
TRUE	=I2C_ALS_SCL	36 63
TRUE	I2C_CAM_SCK	35 36
TRUE	I2C_CAM_SDA	35 36
TRUE	PP5V_S3RS0_ALSCAM_F	36
TRUE	GND	

J9500 - rio coax

TRUE	HDMI_CLK_N	86
TRUE	HDMI_CLK_P	86
TRUE	HDMI_DATA_N<0>	86
TRUE	HDMI_DATA_N<1>	86
TRUE	HDMI_DATA_N<2>	86
TRUE	HDMI_DATA_P<0>	86
TRUE	HDMI_DATA_P<1>	86
TRUE	HDMI_DATA_P<2>	86

TRUE	USB3_SD_D2R_N	20 78 88
TRUE	USB3_SD_D2R_P	20 78 88
TRUE	USB3_SD_R2D_C_N	20 78 88
TRUE	USB3_SD_R2D_C_P	20 78 88
TRUE	USB3_EXTB_D2R_N	13 78 87
TRUE	USB3_EXTB_D2R_P	13 78 87
TRUE	USB3_EXTB_R2D_N	78 87
TRUE	USB3_EXTB_R2D_P	78 87
TRUE	USB_EXTB_N	13 78 87
TRUE	USB_EXTB_P	13 78 87
TRUE	GND	19X

J9510 - rio flex

TRUE	SD_PWR_EN	13 18 78
TRUE	PP1V5R1V35_S0_RIO	78
TRUE	HDMI_DDC_CLK	
TRUE	HDMI_DDC_DATA	
TRUE	HDMI_HPD_L	
TRUE	SMBUS_PCH_CLK	13 63 88
TRUE	SMBUS_PCH_DATA	13 63 88
TRUE	PM_SLP_S3_BUF_L	50 64 65 78 79
TRUE	PM_SLP_S4_L	12 21 33 37 40 65 78
TRUE	PP3V3_S3	3X 81 83
TRUE	PP3V3_S4	81 83
TRUE	PP5V_S4	5X 81
TRUE	RIO_SDCONN_STATE_CHANGE_L	20 78
TRUE	USB_EXTB_OC_L	18 78
TRUE	GND	10X

J5150 - hall effect

TRUE	PP3V42_G3H	81 83
TRUE	SMC_LID_R	42
TRUE	GND	

J6050 - left fan

TRUE	FAN_LT_PWM	48
TRUE	FAN_LT_TACH	48
TRUE	PP5V_S0	3X 81 83
TRUE	GND	5X

J6060 - right fan

TRUE	FAN_RT_PWM	48
TRUE	FAN_RT_TACH	48
TRUE	PP5V_S0	3X 81 83
TRUE	GND	5X

J6100 - lpc + spi

FUNC_TEST		
TRUE	LPCPLUS_GPIO	14 69
TRUE	LPCPLUS_RESET_L	20 69
TRUE	LPC_AD<0>	13 60 69 79 88
TRUE	LPC_AD<1>	13 60 69 79 88
TRUE	LPC_AD<2>	13 60 69 79 88
TRUE	LPC_AD<3>	13 60 69 79 88
TRUE	LPC_CLK33M_LPCPLUS	19 69 88
TRUE	LPC_FRAME_L	13 60 69 79 88
TRUE	LPC_PWRDWN_L	12 20 60 69
TRUE	LPC_SERIRQ	13 60 69
TRUE	PM_CLKRUN_L	12 60 69
TRUE	PP5V_S0	81 83
TRUE	SMC_RESET_L	40 61 69 96
TRUE	SMC_ROMBOOT	61 69
TRUE	SMC_RX_L	40 61 69
TRUE	SMC_TCK	40 61 69
TRUE	SMC_TDI	40 61 69
TRUE	SMC_TDO	40 61 69
TRUE	SMC_TMS	40 61 69
TRUE	SMC_TX_L	40 61 69
TRUE	SPIROM_USE_MLB	14 69
TRUE	SPI_ALT_CLK	69
TRUE	SPI_ALT_CS_L	69
TRUE	SPI_ALT_MISO	69
TRUE	SPI_ALT_MOSI	69
TRUE	TP_SMC_MD1	69
TRUE	TP_SMC_TRST_L	69
TRUE	GND	2X

J4800 - ipd flex

TRUE	Z2_CS_L	38
TRUE	Z2_MOSI	38
TRUE	Z2_MISO	38
TRUE	Z2_SCLK	38
TRUE	Z2_HOST_INTN	38
TRUE	Z2_CLKIN	38
TRUE	Z2_KEY_ACT_L	38
TRUE	PSOC_F_CS_L	38
TRUE	PICKB_L	38
TRUE	PSOC_MOSI	38
TRUE	PSOC_MISO	38
TRUE	PSOC_SCLK	38
TRUE	=I2C_TPAD_SCL	38 63
TRUE	=I2C_TPAD_SDA	38 63
TRUE	SMC_LID	38 40 61 62
TRUE	SMC_T101_COM_1	
TRUE	=PP3V3_S4_TPAD	38 81
TRUE	=PP5V_S5_TPAD	38 81
TRUE	GND	2X

J4813 - keyboard

TRUE	PP3V3_S4	81 83
TRUE	PP3V42_G3H	81 83
TRUE	WS_CONTROL_KBD	38
TRUE	WS_KBD1	38
TRUE	WS_KBD10	38
TRUE	WS_KBD11	38
TRUE	WS_KBD12	38
TRUE	WS_KBD13	38
TRUE	WS_KBD14	38
TRUE	WS_KBD15_CAP	38
TRUE	WS_KBD16_NUM	38
TRUE	WS_KBD17	38
TRUE	WS_KBD18	38
TRUE	WS_KBD19	38
TRUE	WS_KBD2	38
TRUE	WS_KBD20	38
TRUE	WS_KBD21	38
TRUE	WS_KBD22	38
TRUE	WS_KBD23	38
TRUE	WS_KBD3	38
TRUE	WS_KBD4	38
TRUE	WS_KBD5	38
TRUE	WS_KBD6	38
TRUE	WS_KBD7	38
TRUE	WS_KBD8	38
TRUE	WS_KBD9	38
TRUE	WS_KBD_ONOFF_L	38
TRUE	WS_LEFT_OPTION_KBD	38
TRUE	WS_LEFT_SHIFT_KBD	38
TRUE	GND	2X

J4915 - kbd bklt

TRUE	KBDBKLT_RETURN1	2X 39 62
TRUE	KBDBKLT_RETURN2	2X 39 62
TRUE	PPVOUT_S0_KBDBKLT	39 62
TRUE	GND	4X

J6701 - audio flex

FUNC_TEST		
TRUE	AUD_HP_PORT_L	50 54
TRUE	AUD_HP_PORT_R	50 54
TRUE	AUD_SPDIF_OUT_JACK	
TRUE	AUD_TIPDET_INV	
TRUE	AUD_TYPEDET	50 54
TRUE	AUD_CONN_MIC_XW	4X
TRUE	CH_HS_MIC	
TRUE	PP3V3_S0	81 83 93
TRUE	AUD_CONN_SLEEVE_XW	4X 53 54
TRUE	US_HS_MIC	
TRUE	GND	2X GND

J6601 - mic

TRUE	DMIC_CLK3	91 94
TRUE	PP3V3_S0	81 83 93
TRUE	DMIC_SDA2	94
TRUE	DMIC_SDA3	91 94
TRUE	GND	

J6602 - L speaker

TRUE	SPKRCONN_L_ID	91 94
TRUE	SPKRCONN_L_OUT_N	92 94 93
TRUE	SPKRCONN_L_OUT_P	92 94 93
TRUE	SPKRCONN_SL_OUT_N	92 94 93
TRUE	SPKRCONN_SL_OUT_P	92 94 93
TRUE	GND	

J6603 - R speaker

TRUE	SPKRCONN_R_ID	91 94
TRUE	SPKRCONN_R_OUT_N	92 94 93
TRUE	SPKRCONN_R_OUT_P	92 94 93
TRUE	SPKRCONN_SR_OUT_N	92 94 93
TRUE	SPKRCONN_SR_OUT_P	92 94 93
TRUE	GND	

J7000 - DC PWR

TRUE	ADAPTER_SENSE	95
TRUE	PP20V_DCIN_FUSE	2X 95
TRUE	GND	2X

J7050 - battery

TRUE	PPVBAT_G3H_CONN	8X 95 96
TRUE	SMBUS_SMC_5_G3_SCL	40 63 92
TRUE	SMBUS_SMC_5_G3_SDA	40 63 92
TRUE	SYS_DETECT_L	95
TRUE	GND	8X

J8300 - eDP

TRUE	DP_INT_AUX_N	67 86 96
TRUE	DP_INT_AUX_P	67 86 96
TRUE	DP_INT_ML_N<0>	67 86 96
TRUE	DP_INT_ML_N<1>	67 86 96
TRUE	DP_INT_ML_N<2>	67 86 96
TRUE	DP_INT_ML_N<3>	67 86 96
TRUE	DP_INT_ML_P<0>	67 86 96
TRUE	DP_INT_ML_P<1>	67 86 96
TRUE	DP_INT_ML_P<2>	67 86 96
TRUE	DP_INT_ML_P<3>	67 86 96
TRUE	LCD_FSS	42 67 79
TRUE	LCD_HPD_CONN	67
TRUE	LED_RETURN_1	42 67
TRUE	LED_RETURN_2	42 67
TRUE	LED_RETURN_3	42 67
TRUE	LED_RETURN_4	42 67
TRUE	LED_RETURN_5	42 67
TRUE	LED_RETURN_6	42 67
TRUE	PP5VR3V3_SW_LCD	3X 67
TRUE	PPVOUT_S0_LCDBKLT	42 67
TRUE	GND	16X

Power Rails

TRUE	PM_SLP_S3_L	12 21 40 65
TRUE	PPVTT_S0_DDR	81
TRUE	PP3V3_S0	81 83 93
TRUE	PP3V3_S3	81 83
TRUE	PP3V3_S5	81 93
TRUE	PP3V3_S5_AVREF_SMC	40 61
TRUE	PP3V42_G3H	81 83
TRUE	PP5V_S0	81 83
TRUE	PP5V_S3	81
TRUE	PP5V_S5	81
TRUE	PPBUS_G3H	81
TRUE	PPDCIN_G3H	81
TRUE	PPVCC_S0_CPU	81
TRUE	PPVTTDDR_S3	81
TRUE	PP3V3_S0SW_SSD	81
TRUE	PP1V5_S0	81
TRUE	PP1V35_S3	81

XDP

FUNC_TEST		
TRUE	XDP_CPU_TCK	6 18 86
TRUE	XDP_PCH_TCK	11 18
TRUE	XDP_CPU_TDI	6 18 86
TRUE	XDP_CPU_TDO	6 18 86
TRUE	XDP_CPU_TRST_L	6 18 86
TRUE	XDP_CPU_TMS	6 18 86
TRUE	XDP_PCH_TMS	11 18
TRUE	XDP_PCH_TDI	11 18
TRUE	XDP_PCH_TDO	11 18
TRUE	XDP_CPU_PREQ_L	6 18 86
TRUE	XDP_CPU_PRDY_L	6 18 86
TRUE	PM_RSMRST_L	12 65 88
TRUE	PM_PCH_PWROK	12 19 88
TRUE	PM_SYSRST_L	12 19 40 88
TRUE	CPU_CFG<3>	6 18 86
TRUE	PP1V05_S0	81
TRUE	GND	2X GND

Power Sequence

FUNC_TEST		
TRUE	SMC_ONOFF_L	38 40 41
TRUE	PM_DSW_PWRGD	12 40 88
TRUE	ALL_SYS_PWRGD	18 19 40 65
TRUE	PM_PCH_SYS_PWROK	12 19 19 40 88
TRUE	PLT_RESET_L	12 18 20 21
TRUE	LCD_PWR_EN	47 79
TRUE	LCD_BKLT_EN	62 79

TPA401 A — TP-PG
TPA402 A — TP-PG

	PEG_CLK100M_P	88 92 98
	PEG_CLK100M_N	88 92 98

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NC NO_TESTs

PCH

	NO_TEST	MAKE_BASE	
TP_USB3_SPARE_D2RN	TRUE	TRUE	NC_USB3_SPARE_D2RN
TP_USB3_SPARE_D2RP	TRUE	TRUE	NC_USB3_SPARE_D2RP
TP_USB3_SPARE_R2D_CN	TRUE	TRUE	NC_USB3_SPARE_R2D_CN
TP_USB3_SPARE_R2D_CP	TRUE	TRUE	NC_USB3_SPARE_R2D_CP
USB3_EXTC_D2R_N	TRUE	TRUE	NC_USB3_EXTC_D2RN
USB3_EXTC_D2R_P	TRUE	TRUE	NC_USB3_EXTC_D2RP
USB3_EXTC_R2D_C_N	TRUE	TRUE	NC_USB3_EXTC_R2D_CN
USB3_EXTC_R2D_C_P	TRUE	TRUE	NC_USB3_EXTC_R2D_CP
USB3_EXTD_D2R_N	TRUE	TRUE	NC_USB3_EXTD_D2RN
USB3_EXTD_D2R_P	TRUE	TRUE	NC_USB3_EXTD_D2RP
USB3_EXTD_R2D_C_N	TRUE	TRUE	NC_USB3_EXTD_R2D_CN
USB3_EXTD_R2D_C_P	TRUE	TRUE	NC_USB3_EXTD_R2D_CP
PCIE_ENET_D2RN	TRUE	TRUE	NC_PCIE_ENET_D2RN
PCIE_ENET_D2RP	TRUE	TRUE	NC_PCIE_ENET_D2RP
PCIE_ENET_R2D_CN	TRUE	TRUE	NC_PCIE_ENET_R2D_CN
PCIE_ENET_R2D_CP	TRUE	TRUE	NC_PCIE_ENET_R2D_CP
SATA_A_D2R_N	TRUE	TRUE	NC_SATA_A_D2RN
SATA_A_D2R_P	TRUE	TRUE	NC_SATA_A_D2RP
SATA_A_R2D_C_N	TRUE	TRUE	NC_SATA_A_R2D_CN
SATA_A_R2D_C_P	TRUE	TRUE	NC_SATA_A_R2D_CP
SATA_B_D2R_N	TRUE	TRUE	NC_SATA_B_D2RN
SATA_B_D2R_P	TRUE	TRUE	NC_SATA_B_D2RP
SATA_B_R2D_C_N	TRUE	TRUE	NC_SATA_B_R2D_CN
SATA_B_R2D_C_P	TRUE	TRUE	NC_SATA_B_R2D_CP
TP_SATA_ODD_D2RN	TRUE	TRUE	NC_SATA_ODD_D2RN
TP_SATA_ODD_D2RP	TRUE	TRUE	NC_SATA_ODD_D2RP
TP_SATA_ODD_R2D_CN	TRUE	TRUE	NC_SATA_ODD_R2D_CN
TP_SATA_ODD_R2D_CP	TRUE	TRUE	NC_SATA_ODD_R2D_CP
TP_SATA_D_D2RN	TRUE	TRUE	NC_SATA_D_D2RN
TP_SATA_D_D2RP	TRUE	TRUE	NC_SATA_D_D2RP
TP_SATA_D_R2D_CN	TRUE	TRUE	NC_SATA_D_R2D_CN
TP_SATA_D_R2D_CP	TRUE	TRUE	NC_SATA_D_R2D_CP
TP_SATA_F_D2RN	TRUE	TRUE	NC_SATA_F_D2RN
TP_SATA_F_D2RP	TRUE	TRUE	NC_SATA_F_D2RP
TP_SATA_F_R2D_CN	TRUE	TRUE	NC_SATA_F_R2D_CN
TP_SATA_F_R2D_CP	TRUE	TRUE	NC_SATA_F_R2D_CP
USB_EXTC_N	TRUE	TRUE	NC_USB_EXTCN
USB_EXTC_P	TRUE	TRUE	NC_USB_EXTCP
TP_USB_SDN	TRUE	TRUE	NC_USB_SDN
TP_USB_SDP	TRUE	TRUE	NC_USB_SDP
TP_USB_WLANN	TRUE	TRUE	NC_USB_WLANN
TP_USB_WLANP	TRUE	TRUE	NC_USB_WLANP
TP_USB_6N	TRUE	TRUE	NC_USB_6N
TP_USB_6P	TRUE	TRUE	NC_USB_6P
TP_USB_7N	TRUE	TRUE	NC_USB_7N
TP_USB_7P	TRUE	TRUE	NC_USB_7P
USB_EXTD_N	TRUE	TRUE	NC_USB_EXTDN
USB_EXTD_P	TRUE	TRUE	NC_USB_EXTDP
TP_USB_PSOCN	TRUE	TRUE	NC_USB_PSOCN
TP_USB_PSOCP	TRUE	TRUE	NC_USB_PSOCP
USB_IR_N	TRUE	TRUE	NC_USB_IRN
USB_IR_P	TRUE	TRUE	NC_USB_IRP
ITPXDP_CLK100M_N	TRUE	TRUE	NC_ITPXDP_CLK100MN
ITPXDP_CLK100M_P	TRUE	TRUE	NC_ITPXDP_CLK100MP
TP_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L
TP_PCI_CLK33M_OUT2	TRUE	TRUE	NC_PCI_CLK33M_OUT2
TP_PCI_CLK33M_OUT3	TRUE	TRUE	NC_PCI_CLK33M_OUT3
TP_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1
TP_HDA_SDIN2	TRUE	TRUE	NC_HDA_SDIN2
TP_HDA_SDIN3	TRUE	TRUE	NC_HDA_SDIN3
TP_LPC_DREQ0_L	TRUE	TRUE	NC_LPC_DREQ0_L
TP_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK
TP_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA
TP_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L
EDP_IG_BKL_PWM	TRUE	TRUE	NC_EDP_IG_BKL_PWM
USB_SMC_P	TRUE	TRUE	NC_USB_SMCP
USB_SMC_N	TRUE	TRUE	NC_USB_SMCN
SMC_INTERFACE_2	TRUE	TRUE	NC_SMC_INTERFACE_2

Thunderbolt

	NO_TEST	MAKE_BASE	
TP_TBT_XTAL25OUT	TRUE	TRUE	NC_TBT_XTAL25OUT
TP_DP_TBTSRC_ML_CP<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>
TP_DP_TBTSRC_ML_CN<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>
TP_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP
TP_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN
TP_DP_IG_D_AUXCHN	TRUE	TRUE	NC_DP_IG_D_AUXCHN
TP_DP_IG_D_AUXCHP	TRUE	TRUE	NC_DP_IG_D_AUXCHP
TP_PCIE_CLK100M_PE5N	TRUE	TRUE	NC_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P	TRUE	TRUE	NC_PCIE_CLK100M_PE5P
PCIE_CLK100M_ENETSD_N	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN
PCIE_CLK100M_ENETSD_P	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP
TP_PCIE_CLK100M_ENETN	TRUE	TRUE	NC_PCIE_CLK100M_ENETN
TP_PCIE_CLK100M_ENETP	TRUE	TRUE	NC_PCIE_CLK100M_ENETP
TP_PCIE_CLK100M_PEGBN	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN
TP_PCIE_CLK100M_PEGBP	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP
TP_PCIE_CLK100M_SWN	TRUE	TRUE	NC_PCIE_CLK100M_SWN
TP_PCIE_CLK100M_SWP	TRUE	TRUE	NC_PCIE_CLK100M_SWP
TP_PCH_GPIO64_CLKOUTFLEX0	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3
TP_USB_4N	TRUE	TRUE	NC_USB_4N
TP_USB_4P	TRUE	TRUE	NC_USB_4P

TRUE	PCIE_TBT_R2D_P<3..0>
TRUE	PCIE_TBT_R2D_N<3..0>
TRUE	PCIE_TBT_D2R_C_P<3..0>
TRUE	PCIE_TBT_D2R_C_N<3..0>
TRUE	DMI_S2N_P<3..1>
TRUE	DMI_S2N_N<3..1>
TRUE	DMI_N2S_P<3..1>
TRUE	DMI_N2S_N<3..1>

PLACEABLE BEAD-PROBES FOR TBT

TBT_A_R2D_C_P<1>	CTDSM	BEAD-PROBE	BPA535 NO_XNET_CONNECTION=TRUE
TBT_A_D2R_P<1>	CTDSM	BEAD-PROBE	BPA531 NO_XNET_CONNECTION=TRUE
TBT_A_D2R_N<1>	CTDSM	BEAD-PROBE	BPA532 NO_XNET_CONNECTION=TRUE

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J15 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE_ADJ	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE_ADJ	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL8,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL8,ISL10	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL8,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL8,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL1,ISL4,ISL9,ISL12	0.053 MM	?
1X_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_2794S	*	=2794_OHM_SE	=2794_OHM_SE	=2794_OHM_SE	=2794_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2CLK	*	=7x_DIELECTRIC	?
HDMICLK_2DP	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
DMI_S2N	CPU_8SD	DMI_S2N	DMI_S2N_P<3:0>
DMI_S2N	CPU_8SD	DMI_S2N	DMI_S2N_N<3:0>
DMI_N2S	CPU_8SD	DMI_N2S	DMI_N2S_P<3:0>
DMI_N2S	CPU_8SD	DMI_N2S	DMI_N2S_N<3:0>
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT
FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC
DMI_CLK	CPU_8SD	CLK_DMI	DMI_CLK100M_CPU_P
DMI_CLK	CPU_8SD	CLK_DMI	DMI_CLK100M_CPU_N
CPU_CLK135_PLL	CPU_8SD	CLK_PCIE	CPU_CLK135M_DPLLREF_N
CPU_CLK135_PLL	CPU_8SD	CLK_PCIE	CPU_CLK135M_DPLLREF_P
CPU_CLK135_PLL	CPU_8SD	CLK_PCIE	CPU_CLK135M_DPLLSS_N
CPU_CLK135_PLL	CPU_8SD	CLK_PCIE	CPU_CLK135M_DPLLSS_P
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP
CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>
XDP_CLK_ECH	CLK_PCIE_8SD	CLK_PCIE	ITPXDP_CLK100M_P
XDP_CLK_ECH	CLK_PCIE_8SD	CLK_PCIE	ITPXDP_CLK100M_N
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPU_TRST_L
XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>
XDP_DBRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L
CPU_PECI	CPU_45S	CPU_VID	CPU_PECI
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD
PM_THRMTRIP_L	CPU_45S	CPU_SM1L	PM_THRMTRIP_L
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK
CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N
CPU_MEM_VREF		CPU_VREF	CPU_DIMMA_VREFDQ
CPU_MEM_VREF		CPU_VREF	CPU_DIMMB_VREFDQ
CPU_MEM_VREF		MEM_PWR	PPVREF_S3_MEM_VREFDQ_A
CPU_MEM_VREF		CPU_VREF	PPVREF_S3_MEM_VREFDQ_B
CPU_MEM_VREF		MEM_PWR	PPVREF_S3_MEM_VREFCA_A
CPU_MEM_VREF		CPU_VREF	PPVREF_S3_MEM_VREFCA_B
PEG_D2R	PEG_80D	PEG_D2R	PEG_D2R_P<7..0>
PEG_D2R	PEG_80D	PEG_D2R	PEG_D2R_N<7..0>
	PEG_80D	PEG_D2R	PEG_D2R_C_P<7..0>
	PEG_80D	PEG_D2R	PEG_D2R_C_N<7..0>
	PEG_80D	PEG_R2D	PEG_R2D_P<7..0>
	PEG_80D	PEG_R2D	PEG_R2D_N<7..0>
PEG_R2D	PEG_80D	PEG_R2D	PEG_R2D_C_P<7..0>
PEG_R2D	PEG_80D	PEG_R2D	PEG_R2D_C_N<7..0>
PEG_D2R_TBT	CPU_8SD	PEG_D2R	PCIE_TBT_D2R_P<3..0>
PEG_D2R_TBT	CPU_8SD	PEG_D2R	PCIE_TBT_D2R_N<3..0>
	CPU_8SD	PEG_D2R	PCIE_TBT_D2R_C_P<3..0>
	CPU_8SD	PEG_D2R	PCIE_TBT_D2R_C_N<3..0>
PEG_R2D_TBT	CPU_8SD	PEG_R2D	PCIE_TBT_R2D_P<3..0>
PEG_R2D_TBT	CPU_8SD	PEG_R2D	PCIE_TBT_R2D_N<3..0>
	CPU_8SD	PEG_R2D	PCIE_TBT_R2D_C_P<3..0>
	CPU_8SD	PEG_R2D	PCIE_TBT_R2D_C_N<3..0>

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_P_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_P_N<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_P
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_N
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_P
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_N
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_P
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_N

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_P<2..0>
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_N<2..0>
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_P
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_N
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N
	DP_85D		DP_TBTSNK0_AUXCH_C_P
	DP_85D		DP_TBTSNK0_AUXCH_C_N
TBTSNK1_AUXCH1	DP_85D		DP_TBTSNK1_AUXCH_P
TBTSNK1_AUXCH1	DP_85D		DP_TBTSNK1_AUXCH_N
	DP_85D		DP_TBTSNK1_AUXCH_C_P
	DP_85D		DP_TBTSNK1_AUXCH_C_N

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_7XRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_7XRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_7XRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_7XRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_7XRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_7XRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	84
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	84
P37	SATA_85D	SATA_D2R	NC_SATA_A_D2RP	84
P32	SATA_85D	SATA_D2R	NC_SATA_A_D2RN	84
P35	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	84
P40	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	84
P30	SATA_85D	SATA_D2R	NC_SATA_B_D2RP	84
P28	SATA_85D	SATA_D2R	NC_SATA_B_D2RN	84
P81	PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
	USB_EXTA	USB_85D	USB	USB_EXTA_P	13 37
	USB_EXTA	USB_85D	USB	USB_EXTA_N	13 37
P43	USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	37
P41	USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_N	37
P46	USB_EXTA	USB_85D	USB	USB_LT1_P	37
P44	USB_EXTA	USB_85D	USB	USB_LT1_N	37
	USB_MC	USB_85D	USB	NC_USB_EXTCP	84
	USB_MC	USB_85D	USB	NC_USB_EXTCN	84
P31	USB_MC	USB_85D	USB	NC_USB_SDP	84
P29	USB_MC	USB_85D	USB	NC_USB_SDN	84
P26		CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	37 40 41
P24		CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	37 40 41
	USB_SMC	USB_85D	USB	USB_SMC_P	84
	USB_SMC	USB_85D	USB	USB_SMC_N	84
P33	USB_MC	USB_85D	USB	NC_USB_6P	84
P45	USB_MC	USB_85D	USB	NC_USB_6N	84
P39	USB_MC	USB_85D	USB	NC_USB_7P	84
P38	USB_MC	USB_85D	USB	NC_USB_7N	84
	USB_EXTB	USB_85D	USB	USB_EXTB_P	13 78 83
	USB_EXTB	USB_85D	USB	USB_EXTB_N	13 78 83
P36	USB_MC	USB_85D	USB	NC_USB_EXTDP	84
P34	USB_MC	USB_85D	USB	NC_USB_EXTDN	84
	USB_BT	USB_85D	USB	USB_BT_P	13 33
	USB_BT	USB_85D	USB	USB_BT_N	13 33
		USB_85D	USB	USB_BT_CONN_P	83 83
		USB_85D	USB	USB_BT_CONN_N	83 83
P27	USB_MC	USB_85D	USB	NC_USB_IRP	84
P25	USB_MC	USB_85D	USB	NC_USB_IRN	84
P23	USB_TPAD	USB_85D	USB	USB_TPAD_P	13 38
P21	USB_TPAD	USB_85D	USB	USB_TPAD_N	13 38
P20		USB_85D	USB	USB_TPAD_R_P	38
P19		USB_85D	USB	USB_TPAD_R_N	38
	PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
P99	USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 37
P97	USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 37
P103		USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
P101		USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
P93	USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	37
P91	USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	37
P96		USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 37
P94		USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 37
P89	USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 78 83
P87	USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 78 83
P85		USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
P83		USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
P77	USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	78 83
P75	USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	78 83
P80		USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 78
P78		USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 78
P102	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	84
P100	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	84
P95		USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	84
P92		USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	84
P90	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	84
P88	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	84
P82		USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	84
P79		USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	84

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
P109	SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
P105	SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
P106		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
P104	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 36
P108	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
P107		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	-	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L
LPC_RESET_L	LPC_45S	LPC	LPC_RESET_L
SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK
SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA
SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK
SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA
SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK
SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK
	HDA_45S	HDA	HDA_BIT_CLK_R
HDA_SYNC	HDA_45S	HDA	HDA_SYNC
	HDA_45S	HDA	HDA_SYNC_R
	HDA_45S	HDA	HDA_RST_R_L
HDA_RST_L	HDA_45S	HDA	HDA_RST_L
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0
HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT
	HDA_45S	HDA	HDA_SDOUT_R
	SPI_45S	SPI	SPI_CLK_R
SPI_CLK	SPI_45S	SPI	SPI_CLK
	SPI_45S	SPI	SPI_MOSI_R
SPI_MOSI	SPI_45S	SPI	SPI_MOSI
SPI_MISO	SPI_45S	SPI	SPI_MISO
	SPI_45S	SPI	SPI_CS0_R_L
SPI_CS0	SPI_45S	SPI	SPI_CS0_L
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N
	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P
	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N
PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N
	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P
	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N
PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P
PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N
	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P
	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R
PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIIN
PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK
PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIOUT
PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P
PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N
PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P
PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N
PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P
PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N
PEG_CLK100M	PEG_80D	CLK_PCIE	PEG_CLK100M_P
PEG_CLK100M	PEG_80D	CLK_PCIE	PEG_CLK100M_N
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N
	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P
	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N
	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P
	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N
PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P
	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N

PCH Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTRUDER_L
PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTVRMEN_L
PCH_PM_NET	PCH_45S	PCH_SE	PCH_DSWVRMEN
PCH_PM_NET	PCH_45S	PCH_SE	PCH_SRTCRST_L
PCH_PM_NET	PCH_45S	PCH_SE	PM_RSMRST_L
PCH_PM_NET	PCH_45S	PCH_SE	PM_SYSRST_L
PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK
PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_APWROK
PCH_PM_NET	PCH_45S	PCH_SE	PM_DSW_PWRGD
PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_SYS_PWROK
PCH_PM_NET	PCH_45S	PCH_SE	PM_PWRBTN_L
PCH_PM_NET	PCH_45S	PCH_SE	PM_THRMTRIP_L_R
PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE_WAKE_L
PCH_PM_NET	PCH_45S	PCH_SE	PCH_RCIN_L
PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_P<3..0>
PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_N<3..0>
PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_P<3..0>
PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_N<3..0>
	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_P<3..0>
	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_N<3..0>

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	-5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	-5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	-5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	-5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	-5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	-8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	-8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	-4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	-4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	-10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0>
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0>
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1>
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1>
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0>
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1>
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0>
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1>
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0>
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1>
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0>
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8>
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16>
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24>
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32>
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40>
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48>
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56>
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0>
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0>
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1>
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1>
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2>
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2>
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3>
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3>
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4>
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4>
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5>
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5>
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6>
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6>
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7>
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7>
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0>
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0>
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1>
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1>
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0>
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1>
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0>
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1>
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0>
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1>
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0>
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8>
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16>
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24>
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32>
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40>
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48>
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56>
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0>
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0>
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1>
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1>
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2>
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2>
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3>
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3>
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4>
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4>
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5>
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5>
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6>
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6>
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7>
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7>
		MEM_PWR	PPVREF_S3_MEM_VREFDQ_A
		MEM_PWR	PPVREF_S3_MEM_VREFCA_A
		MEM_PWR	PP1V35_S3_MEM

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0>
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0>
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0>
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0>
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0>
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0>
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0>
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1>
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1>
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1>
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1>
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0>
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0>
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0>
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0>
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0>
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0>
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0>
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1>
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1>
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1>
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1>
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L

Only used on hosts supporting Thunderbolt video-in

SYNC MASTER=CLEAN_J45 SYNC DATE=04/26/2013

PAGE TITLE: Thunderbolt Constraints

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L
	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N
		S2_MEM_PWR	PP1V35_CAM
		S2_MEM_PWR	PP0V675_CAM_VREF
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
SMBUS_SMC_2_S3_SCL	SMB_455	SMB	SMBUS_SMC_2_S3_SCL	40 43
SMBUS_SMC_2_S3_SDA	SMB_455	SMB	SMBUS_SMC_2_S3_SDA	40 43
SMBUS_SMC_1_S0_SCL	SMB_455	SMB	SMBUS_SMC_1_S0_SCL	40 43
SMBUS_SMC_1_S0_SDA	SMB_455	SMB	SMBUS_SMC_1_S0_SDA	40 43
SMBUS_SMC_0_S0_SCL	SMB_455	SMB	SMBUS_SMC_0_S0_SCL	40 43
SMBUS_SMC_0_S0_SDA	SMB_455	SMB	SMBUS_SMC_0_S0_SDA	40 43
SMBUS_SMC_5_SCL	SMB_455	SMB	SMBUS_SMC_5_G3_SCL	40 43 83
SMBUS_SMC_5_SDA	SMB_455	SMB	SMBUS_SMC_5_G3_SDA	40 43 83
SMBUS_SMC_3_SCL	SMB_455	SMB	SMBUS_SMC_3_SCL	40 42
SMBUS_SMC_3_SDA	SMB_455	SMB	SMBUS_SMC_3_SDA	40 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	56
	1TO1_DIFFPAIR		CHGR_CSI_N	56
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	56
	1TO1_DIFFPAIR		CHGR_CSO_N	56

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_90S	*	=1:1_DIFFPAIR	=90_OHM_SE	=90_OHM_SE	=90_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_90S	*	=1:1_DIFFPAIR	=90_OHM_SE	=90_OHM_SE	=90_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.2 MM	0.2 MM
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMSH	*	=2X_DIELECTRIC	7
THMSH	*	=2X_DIELECTRIC	7
AUDIO	*	=2X_DIELECTRIC	7

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_CORE	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	7

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_N
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPUTHMSNS_D_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPUTHMSNS_D_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_GPUFB_R_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_GPUFB_R_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUFB_CS_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUFB_CS_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V05S_GPU_CS_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V05S_GPU_CS_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_P
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_N
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_P
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_N
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_P
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_N
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS2_P
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS2_N
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS1_P
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS1_N
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_N
SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_P
SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P
	AUDIODIFF	AUDIO	ISNS_TBT_R_N
	AUDIODIFF	AUDIO	ISNS_TBT_R_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P
	THERM_1TO1_45S	THERM	ISNS_SSD_N
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P
	THERM_1TO1_45S	THERM	ISNS_SSD_R_N
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P
	THERM_1TO1_45S	THERM	P1V05S0_CS_N
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE_P
	THERM_1TO1_45S	THERM	P1V05S0_SENSE_N
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P
	THERM_1TO1_45S	THERM	TBT_THERMD_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P
	AUDIODIFF	AUDIO	CHGR_CSI_R_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P
	AUDIODIFF	AUDIO	CHGR_CSO_R_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_N

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)	
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N
	AUDIODIFF	AUDIO	RSUBIN_P
	AUDIODIFF	AUDIO	RSUBIN_N
	AUDIODIFF	AUDIO	LSUBIN_P
	AUDIODIFF	AUDIO	LSUBIN_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N
	AUDIODIFF	AUDIO	SPKRAMP_RIN_P
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N
	AUDIODIFF	AUDIO	SPKRAMP_LIN_P
	AUDIODIFF	AUDIO	SPKRAMP_LIN_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P
	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N
	DIFFPAIR	AUDIO	AUD_HS_MIC_P
	DIFFPAIR	AUDIO	AUD_HS_MIC_N
	DIFFPAIR	AUDIO	HS_MIC_P
	DIFFPAIR	AUDIO	HS_MIC_N
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N
		SB_POWER	PP3V3_S5
		SB_POWER	PP3V3_S0
		SB_POWER	PP1V35_S3RS0_CPUDDR
		GND	GND

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE_ADJ	=45_OHM_SE_ADJ	=45_OHM_SE_ADJ	=45_OHM_SE_ADJ	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	TOP,BOTTOM	=5x_DIELECTRIC	?

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_A<8..0>
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_A<8..0>
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_ABI_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_ABI_L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_RAS_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_RAS_L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CAS_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CAS_L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_WE_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_WE_L
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_CKE_L
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_CKE_L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CS_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CS_L
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>
FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>
FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>
FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>
FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>
FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>
FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>
FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>
FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>
FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>
FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>
FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>
FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>
FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_RESET_L
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_RESET_L

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_A<8..0>
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_A<8..0>
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_ABI_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_ABI_L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_RAS_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_RAS_L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CAS_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CAS_L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_WE_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_WE_L
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_CKE_L
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_CKE_L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CS_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CS_L
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>
FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>
FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>
FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>
FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>
FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>
FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>
FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>
FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>
FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>
FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>
FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_RESET_L
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_RESET_L

MUXGFX & DP AUX MUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_P
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_N
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_P
	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_N
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_IG_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_IG_ML_N<3..0>
DP_INT_EG_AUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N
DP_INT_EG_ML	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>
DP_INT_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_P
DP_INT_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_N
DP_INT_EG_AUX1	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_P
DP_INT_EG_AUX1	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_N
TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P
TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N
TBTSNK1_AUXCH1	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P
TBTSNK1_AUXCH1	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>

Kepler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_XTALIN
GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_XTALOUT
GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_XTAL_BUFFOUT_R
GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_SSIN
	1TO1_DIFFPAIR		PEX_TSTCLK_O_P
	1TO1_DIFFPAIR		PEX_TSTCLK_O_N
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_EG_DATA_C_P<2..0>
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_EG_DATA_C_N<2..0>
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_EG_CLK_C_P
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_EG_CLK_C_N

SYNC MASTER-SIDLE J15 — SYNC DATE-09/02/2012

PAGE TITLE: GPU (Kepler) Constraints

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