1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,J45

DVT 8/6/2013

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0456	1	SCHEM MLB J45	SCH	CRITICAL	
820-3662	1	PCBF MLB J45	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST MODIFIED=Tue Aug 6 17 09 28 2013

DRAWING TITLE: <PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 1 OF 118
SHEET: 1 OF 81

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0067	COMMON PARTS,MLB,J45	J45_COMMON
985-0045	DEV BOM,MLB,J45	J45_DEVEL:ENG
639-4822	PCBA,MLB,BETTER,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600_S
639-4823	PCBA,MLB,BETTER,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600
639-4828	PCBA,MLB,BETTER,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600_S
639-4829	PCBA,MLB,BETTER,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600
639-4834	PCBA,MLB,BETTER,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600_S
639-4835	PCBA,MLB,BETTER,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600
639-4840	PCBA,MLB,BEST,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600_S
639-4841	PCBA,MLB,BEST,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600
639-4846	PCBA,MLB,BEST,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600_S
639-4847	PCBA,MLB,BEST,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600
639-4852	PCBA,MLB,BEST,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600_S
639-4853	PCBA,MLB,BEST,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600
639-4858	PCBA,MLB,CTO,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600_S
639-4859	PCBA,MLB,CTO,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600
639-4864	PCBA,MLB,CTO,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600_S
639-4865	PCBA,MLB,CTO,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600
639-4870	PCBA,MLB,CTO,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600_S
639-4871	PCBA,MLB,CTO,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600

J45 BOM Groups

BOM GROUP	BOM OPTIONS
J45_COMMON	ALTERNATE,COMMON,J45_COMMON1,J45_COMMON2,J45_PROGPARTS
J45_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,CPUPEG:X16,S2_PWR:S0
J45_COMMON2	EDP:YES,LPCPLUS_CONN:YES,LPCPLUS_R:YES,XDP,RIO_PWR:1V5,SPI:DUAL_IO,SSD_PWR_EN:GPIO,CAM_WAKE:NO
J45_PVB	BKLT:PROD,SENSOR_NONPROD:N
J45_PROGPARTS	SMC_PROG:EVT,BOOTROM_PROG:DVT,TBTROM:PROG,TPAD_PSOC:PROG
J45_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,DDRVREF_DAC,SENSOR_NONPROD:Y,SENSOR_NONPROD_R,BKLT:ENG,DBGLED,CAM_XTAL:YES
J45_DEVEL:FSB	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,SENSOR_NONPROD_R
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4599	1	CRW SR18J PRQ C0 2 0 47W 4+3E 6M BGA	U0500	CRITICAL	CPU_CRW:BETTER
337S4600	1	CRW SR18H PRQ C0 2 3 47W 4+3E 6M BGA	U0500	CRITICAL	CPU_CRW:BEST
337S4624	1	CRW SR1BS PRQ C0 2 6 47W 4+3E 6M BGA	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC QEWV LPT M HM87 C2 SR199 PRQ FCBGA	U1100	CRITICAL	
338S1247	1	IC TBT FR 4C A0 PRQ CIO SR1JC FCBGA288	U2800	CRITICAL	
338S1186	1	IC BCM15700A2 S2 PCIE CMRA 8X8 208FCBGA	U3900	CRITICAL	
333S0700	1	IC SDRAM 4GBIT DDR3L 1600 GEMMA 96B FBGA	U4000	CRITICAL	
333S0667	16	IC SDRAM 4GBIT DDR3L 1600 HUMA 78P FBGA		CRITICAL	HYNIX_1600_S
333S0624	16	IC SDRAM DDR3 1600 512MX8 78FBGA C DIE SAMSUNG		CRITICAL	SAMSUNG_1600_S
333S0703	16	IC SDRAM 4GBIT DDR3L 1600 F DIE RS 78P		CRITICAL	ELPIDA_1600_S
333S0660	16	IC SDRAM 4GBIT DDR3L 1600 V80A 78P FBGA		CRITICAL	MICRON_1600_S
333S0667	32	IC SDRAM 4GBIT DDR3L 1600 HUMA 78P FBGA		CRITICAL	HYNIX_1600
333S0624	32	IC SDRAM DDR3 1600 512MX8 78FBGA C DIE SAMSUNG		CRITICAL	SAMSUNG_1600
333S0703	32	IC SDRAM 4GBIT DDR3L 1600 F DIE RS 78P		CRITICAL	ELPIDA_1600
333S0660	32	IC SDRAM 4GBIT DDR3L 1600 V80A 78P FBGA		CRITICAL	MICRON_1600

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1600_S	HYNIX_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:SAMSUNG_1600_S	SAMSUNG_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM:ELPIDA_1600_S	ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM:MICRON_1600_S	MICRON_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM:HYNIX_1600	HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM:SAMSUNG_1600	SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM:ELPIDA_1600	ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM:MICRON_1600	MICRON_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H

COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0067	1	J45 MLB BASE BOM	BASE	CRITICAL	BASE_BOM
985-0045	1	J45 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SYNC MASTER=J15 MLB SYNC DATE=10/25/2012

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 2 OF 118

SHEET: 2 OF 81

Programmables - All builds

335S0915	1	IC,SERIAL SPI FLASH ROM,4MBIT,50MHZ,USON	U2890	CRITICAL	TBTROM:BLANK
341S3919	1	IC,EPROM,Falcon RIDGE(V13.9)J44/45	U2890	CRITICAL	TBTROM:PROG
337S4587	1	IC,TP PSOC, QFN,BLANK	U4801	CRITICAL	TPAD_PSOC:BLANK
341S3856	1	IC,TRKPD/KYBD,PSOC(V225)	U4801	CRITICAL	TPAD_PSOC:PROG

SMC

338S1214	1	IC,SMC-B1,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BASE
341S3902	1	IC,SMC-B1,EXT,V2.12A54,EVT,J45	U5000	CRITICAL	SMC_PROG:EVT
341S3741	1	IC,SMC-A3,SCPL,EXT,VXXXX,PVT,J15	U5000	CRITICAL	SMC_PROG:PVT

EFI ROM

335S0807	1	IC SPI SRL 50MHZ FLASH 64MBIT 8SOP FUSE=1	U6100	CRITICAL	BOOTROM_BLANK:MACRONIX
335S0812	1	IC SPI SRL 50MHZ FLASH 64MBIT SOIC8	U6100	CRITICAL	BOOTROM_BLANK:NUMONYX
341S3763	1	IC,EFI ROM(VXXXX)PROTO 0,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S3780	1	IC,EFI ROM(V0035)PRE-PROTO 1,J45	U6100	CRITICAL	BOOTROM PROG PRE PROTO1
341S3793	1	IC,EFI ROM(V0041)PROTO 1,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3811	1	IC,EFI ROM(V00xx)PROTO 2,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S3890	1	IC,EFI ROM(V0100)PROTO3-J45 &EVT-J45	U6100	CRITICAL	BOOTROM_PROG:EVT
341S3929	1	IC,EFI ROM(Vxxxx)DVT-J45	U6100	CRITICAL	BOOTROM_PROG:DVT

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7845	1	MBP BARCODE LABEL	LABEL	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson Alt to NDK
197S0478	197S0479		ALL	NDK Alt to Epson
371S0713	371S0558		ALL	DDS alt to ST
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
107S0232	107S0241		ALL	Cyntec alt to TFT
376S1032	376S0855		ALL	Toshiba alt to Diodes
376S1129	376S0855		ALL	NXP alt to Diodes
376S1089	376S1128		ALL	NXP alt to Diodes
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung
128S0371	128S0376		ALL	Kemet alt to Sanyo
333S0629	333S0703		ALL	Elpida F die alt
138S0803	138S0639		ALL	Samsung alt to Murata
138S0843	138S0674		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
127S0164	127S0162		ALL	Rohm alt to Vishay
138S0732	138S0715		ALL	Rohm alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HYNIX U4000
311S0649	311S0541		ALL	ON alt to Toshiba (U2030 U7001)

SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

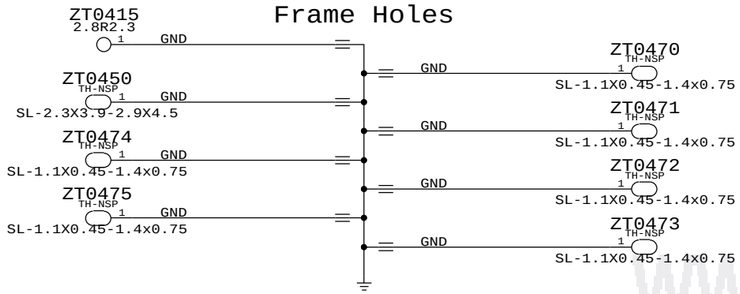
REVISION: <E4LABEL>

BRANCH: <BRANCH>

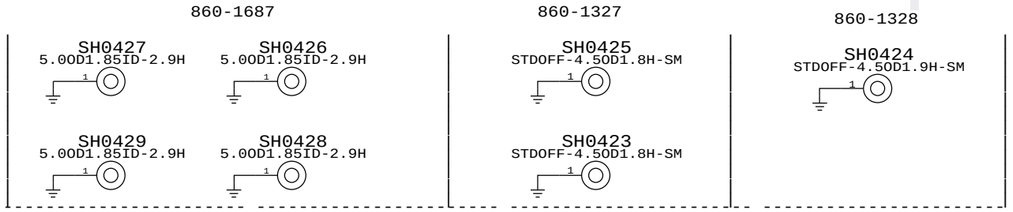
PAGE: 3 OF 118

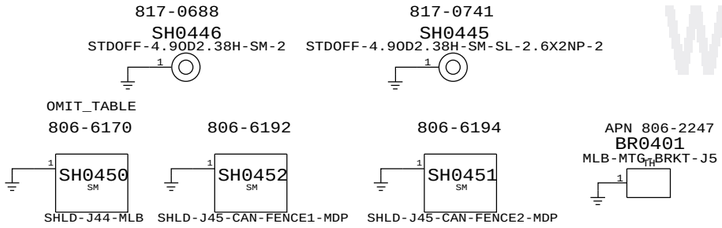
SHEET: 3 OF 81

Frame Holes

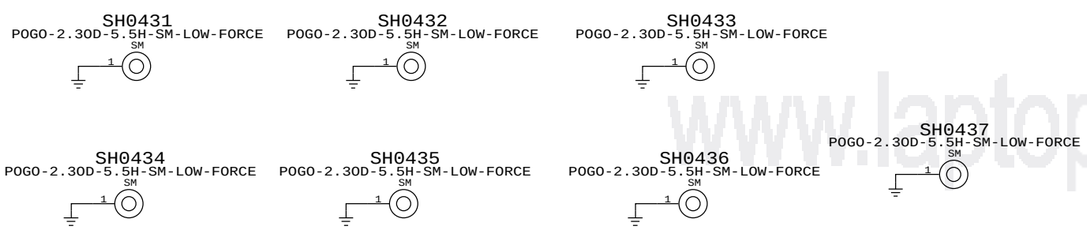


J45 THERMAL MODULE STANDOFF

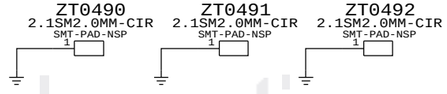




J45 POGO PINS

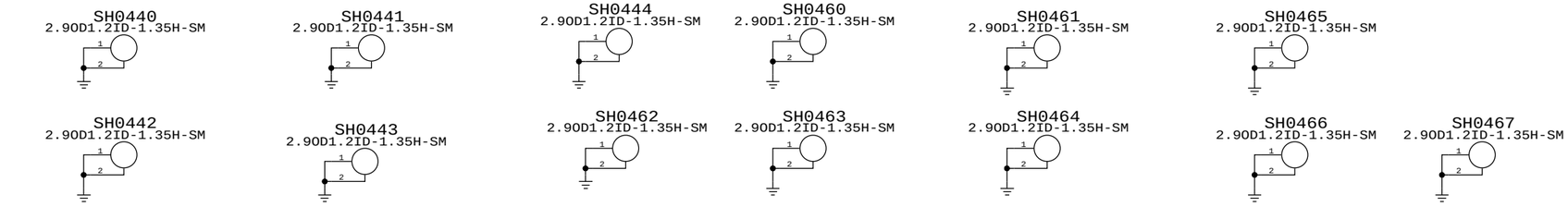


SMT GND TEST PONTS



J45 StAND OFF

860-1448



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
725-1807	1	INSULATOR,REAR,MLB,J45	REAR_INSULATOR	CRITICAL	
725-1877	1	INSULATOR,CPU,J45	CPU_INSULATOR	CRITICAL	
725-1787	1	INSULATOR,PCH,J15	PCH_INSULATOR	CRITICAL	
806-6193	2	CAN COVER,mDP	CAN_COVER1, CAN_COVER2	CRITICAL	
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	
806-9391	1	SHIELD CAN, USB,J45	SH0450	CRITICAL	

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: PD Parts

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 4 OF 118

SHEET: 4 OF 81

DMI / FDI

OMIT_TABLE
U0500
HASWELL
BGA
SYM 1 OF 12

DMI_RX0*	AB2	DMI S2N N<0>	IN
DMI_RX1*	AB3	DMI S2N N<1>	IN
DMI_RX2*	AC3	DMI S2N N<2>	IN
DMI_RX3*	AC1	DMI S2N N<3>	IN
DMI_RX0	AB1	DMI S2N P<0>	IN
DMI_RX1	AB4	DMI S2N P<1>	IN
DMI_RX2	AC4	DMI S2N P<2>	IN
DMI_RX3	AC2	DMI S2N P<3>	IN
DMI_TX0*	AF2	DMI N2S N<0>	OUT
DMI_TX1*	AF4	DMI N2S N<1>	OUT
DMI_TX2*	AG4	DMI N2S N<2>	OUT
DMI_TX3*	AG2	DMI N2S N<3>	OUT
DMI_TX0	AF1	DMI N2S P<0>	OUT
DMI_TX1	AF3	DMI N2S P<1>	OUT
DMI_TX2	AG3	DMI N2S P<2>	OUT
DMI_TX3	AG1	DMI N2S P<3>	OUT
FDI_CSYNC	F11	FDI CSYNC	IN
DISP_INT	F12	FDI INT	IN

PPVCOMP_S0_CPU
R0510 24.9 1% 1/16W MF-LF 402
PEG_RCOMP AH6 — CPU_PEG_RCOMP

PCI EXPRESS BASED INTERFACE SIGNALS

PEG_RX0	E10	PCIE_TBT_D2R_N<0>	IN
PEG_RX1	C10	PCIE_TBT_D2R_N<1>	IN
PEG_RX2	B10	PCIE_TBT_D2R_N<2>	IN
PEG_RX3	E9	PCIE_TBT_D2R_N<3>	IN
PEG_RX4	D9	TP_PEG_D2RN<4>	IN
PEG_RX5	B9	TP_PEG_D2RN<5>	IN
PEG_RX6	L5	TP_PEG_D2RN<6>	IN
PEG_RX7	L2	TP_PEG_D2RN<7>	IN
PEG_RX8	M4	TP_PEG_D2RN<8>	IN
PEG_RX9	L4	TP_PEG_D2RN<9>	IN
PEG_RX10	M2	TP_PEG_D2RN<10>	IN
PEG_RX11	V5	TP_PEG_D2RN<11>	IN
PEG_RX12	V4	TP_PEG_D2RN<12>	IN
PEG_RX13	V1	TP_PEG_D2RN<13>	IN
PEG_RX14	Y3	TP_PEG_D2RN<14>	IN
PEG_RX15	Y2	TP_PEG_D2RN<15>	IN
PEG_RX0	F10	PCIE_TBT_D2R_P<0>	IN
PEG_RX1	D10	PCIE_TBT_D2R_P<1>	IN
PEG_RX2	A10	PCIE_TBT_D2R_P<2>	IN
PEG_RX3	F9	PCIE_TBT_D2R_P<3>	IN
PEG_RX4	C9	TP_PEG_D2RP<4>	IN
PEG_RX5	A9	TP_PEG_D2RP<5>	IN
PEG_RX6	M5	TP_PEG_D2RP<6>	IN
PEG_RX7	L1	TP_PEG_D2RP<7>	IN
PEG_RX8	M3	TP_PEG_D2RP<8>	IN
PEG_RX9	L3	TP_PEG_D2RP<9>	IN
PEG_RX10	M1	TP_PEG_D2RP<10>	IN
PEG_RX11	Y5	TP_PEG_D2RP<11>	IN
PEG_RX12	V3	TP_PEG_D2RP<12>	IN
PEG_RX13	V2	TP_PEG_D2RP<13>	IN
PEG_RX14	Y4	TP_PEG_D2RP<14>	IN
PEG_RX15	Y1	TP_PEG_D2RP<15>	IN
PEG_TX0*	B6	PCIE_TBT_R2D_C_N<0>	OUT
PEG_TX1*	C5	PCIE_TBT_R2D_C_N<1>	OUT
PEG_TX2*	E6	PCIE_TBT_R2D_C_N<2>	OUT
PEG_TX3*	D4	PCIE_TBT_R2D_C_N<3>	OUT
PEG_TX4*	G4	TP_PEG_R2D_CN<4>	OUT
PEG_TX5*	E3	TP_PEG_R2D_CN<5>	OUT
PEG_TX6*	J5	TP_PEG_R2D_CN<6>	OUT
PEG_TX7*	G3	TP_PEG_R2D_CN<7>	OUT
PEG_TX8*	J3	TP_PEG_R2D_CN<8>	OUT
PEG_TX9*	J2	TP_PEG_R2D_CN<9>	OUT
PEG_TX10*	T6	TP_PEG_R2D_CN<10>	OUT
PEG_TX11*	R6	TP_PEG_R2D_CN<11>	OUT
PEG_TX12*	R2	TP_PEG_R2D_CN<12>	OUT
PEG_TX13*	R4	TP_PEG_R2D_CN<13>	OUT
PEG_TX14*	T4	TP_PEG_R2D_CN<14>	OUT
PEG_TX15*	T1	TP_PEG_R2D_CN<15>	OUT
PEG_TX0	C6	PCIE_TBT_R2D_C_P<0>	OUT
PEG_TX1	B5	PCIE_TBT_R2D_C_P<1>	OUT
PEG_TX2	D6	PCIE_TBT_R2D_C_P<2>	OUT
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PEG_TX4	G5	TP_PEG_R2D_CP<4>	OUT
PEG_TX5	E2	TP_PEG_R2D_CP<5>	OUT
PEG_TX6	J6	TP_PEG_R2D_CP<6>	OUT
PEG_TX7	G2	TP_PEG_R2D_CP<7>	OUT
PEG_TX8	J4	TP_PEG_R2D_CP<8>	OUT
PEG_TX9	J1	TP_PEG_R2D_CP<9>	OUT
PEG_TX10	T5	TP_PEG_R2D_CP<10>	OUT
PEG_TX11	R5	TP_PEG_R2D_CP<11>	OUT
PEG_TX12	R1	TP_PEG_R2D_CP<12>	OUT
PEG_TX13	R3	TP_PEG_R2D_CP<13>	OUT
PEG_TX14	T3	TP_PEG_R2D_CP<14>	OUT
PEG_TX15	T2	TP_PEG_R2D_CP<15>	OUT

EDP / DDIB / DDIC / DDID

OMIT_TABLE
U0500
HASWELL
BGA
SYM 10 OF 12

DDIB_TXN0	C25	DP_TBTSNK0_ML_C_N<0>	
DDIB_TXP0	D25	DP_TBTSNK0_ML_C_P<0>	
DDIB_TXN1	A25	DP_TBTSNK0_ML_C_N<1>	
DDIB_TXP1	B25	DP_TBTSNK0_ML_C_P<1>	
DDIB_TXN2	C24	DP_TBTSNK0_ML_C_N<2>	
DDIB_TXP2	D24	DP_TBTSNK0_ML_C_P<2>	
DDIB_TXN3	A24	DP_TBTSNK0_ML_C_N<3>	
DDIB_TXP3	B24	DP_TBTSNK0_ML_C_P<3>	
DDIC_TXN0	C21	DP_TBTSNK1_ML_C_N<0>	
DDIC_TXP0	D21	DP_TBTSNK1_ML_C_P<0>	
DDIC_TXN1	A21	DP_TBTSNK1_ML_C_N<1>	
DDIC_TXP1	B21	DP_TBTSNK1_ML_C_P<1>	
DDIC_TXN2	C20	DP_TBTSNK1_ML_C_N<2>	
DDIC_TXP2	D20	DP_TBTSNK1_ML_C_P<2>	
DDIC_TXN3	A20	DP_TBTSNK1_ML_C_N<3>	
DDIC_TXP3	B20	DP_TBTSNK1_ML_C_P<3>	
DDID_TXN2	C16	TP_DP_IG_D_MLN<2>	
DDID_TXP2	D16	TP_DP_IG_D_MLP<2>	
DDID_TXN3	A16	HDMI_CLK_N	
DDID_TXP3	B16	HDMI_CLK_P	
DDID_TXN0	C17	TP_DP_IG_D_MLN<0>	
DDID_TXP0	D17	TP_DP_IG_D_MLP<0>	
DDID_TXN1	A17	TP_DP_IG_D_MLN<1>	
DDID_TXP1	B17	TP_DP_IG_D_MLP<1>	

Port D pins out of order to match Intel symbol.

PPVCCIO_S0_CPU
R0531 10k 5% 1/16W MF-LF 402

EDP_AUXN	F15	DP_INT_AUXCH_C_N	
EDP_AUXP	F14	DP_INT_AUXCH_C_P	
EDP_HPD	E14	DP_IG_A_HPD_L	
EDP_TXN0	C14	DP_INT_ML_C_N<0>	
EDP_TXN1	A12	DP_INT_ML_C_N<1>	
EDP_TXP0	D14	DP_INT_ML_C_P<0>	
EDP_TXP1	B12	DP_INT_ML_C_P<1>	

PPVCOMP_S0_CPU
R0530 24.9 1% 1/16W MF-LF 402
EDP_RCOMP AG6 — CPU_EDP_RCOMP
EDP_DISP_UTIL E12 — TP_EDP_DISP_UTIL

FDI_TXN0	C12	DP_INT_ML_C_N<2>	
FDI_TXP0	D12	DP_INT_ML_C_P<2>	
FDI_TXN1	A14	DP_INT_ML_C_N<3>	
FDI_TXP1	B14	DP_INT_ML_C_P<3>	

CPU DC / TP / RSVD

OMIT_TABLE
U0500
HASWELL
BGA
SYM 12 OF 12
RESERVED

TP0500 (TP-P6 1)
TP0510 (TP-P6 1)
TP0520 (TP-P6 1)
TP0530 (TP-P6 1)
TP0521 (TP-P6 1)

CPU_DC_A3_B3	NO_TEST	A3	
CPU_DC_A4		A4	
CPU_DC_A51		A51	
CPU_DC_A52_B52	TRUE	A52	
CPU_DC_A53_B53	TRUE	A53	
CPU_DC_B2_C3	TRUE	B2	
CPU_DC_A3_B3	TRUE	B3	
CPU_DC_A52_B52	TRUE	B52	
CPU_DC_A53_B53	TRUE	B53	
CPU_DC_B54_C54	TRUE	B54	
CPU_DC_BC1		BC1	
CPU_DC_BC54		BC54	
CPU_DC_BD1_BE1	TRUE	BD1	
CPU_DC_BD54_BE54	TRUE	BD54	
CPU_DC_BD1_BE1	TRUE	BE1	
CPU_DC_BE2_BF2	TRUE	BE2	
CPU_DC_BE3_BF3	TRUE	BE3	
CPU_DC_BE52_BF52	TRUE	BE52	
CPU_DC_BE53_BF53	TRUE	BE53	
CPU_DC_BD54_BE54	TRUE	BE54	
CPU_DC_BE2_BF2	TRUE	BF2	
CPU_DC_BE3_BF3	TRUE	BF3	
CPU_DC_BF4		BF4	

DAISY_CHAIN_NCTF
DAISY_CHAIN_NCTF

NO_TEST

BF51		CPU_DC_BF51	TP0531 (TP-P6)
BF52	TRUE	CPU_DC_BE52_BF52	
BF53	TRUE	CPU_DC_BE53_BF53	
C1	TRUE	CPU_DC_C1_C2	
C2	TRUE	CPU_DC_C1_C2	
C3	TRUE	CPU_DC_B2_C3	
C54	TRUE	CPU_DC_B54_C54	
D1		CPU_DC_D1	TP0501 (TP-P6)
D54		CPU_DC_D54	TP0511 (TP-P6)

CPU Daisy-Chain Strategy:

Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.

RSVD132	AN35	NC
RSVD133	AN37	NC
RSVD134	AF9	NC
RSVD135	AE9	NC
RSVD136	G14	NC
RSVD137	G17	NC
RSVD138	AD45	NC
RSVD139	AG45	NC

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

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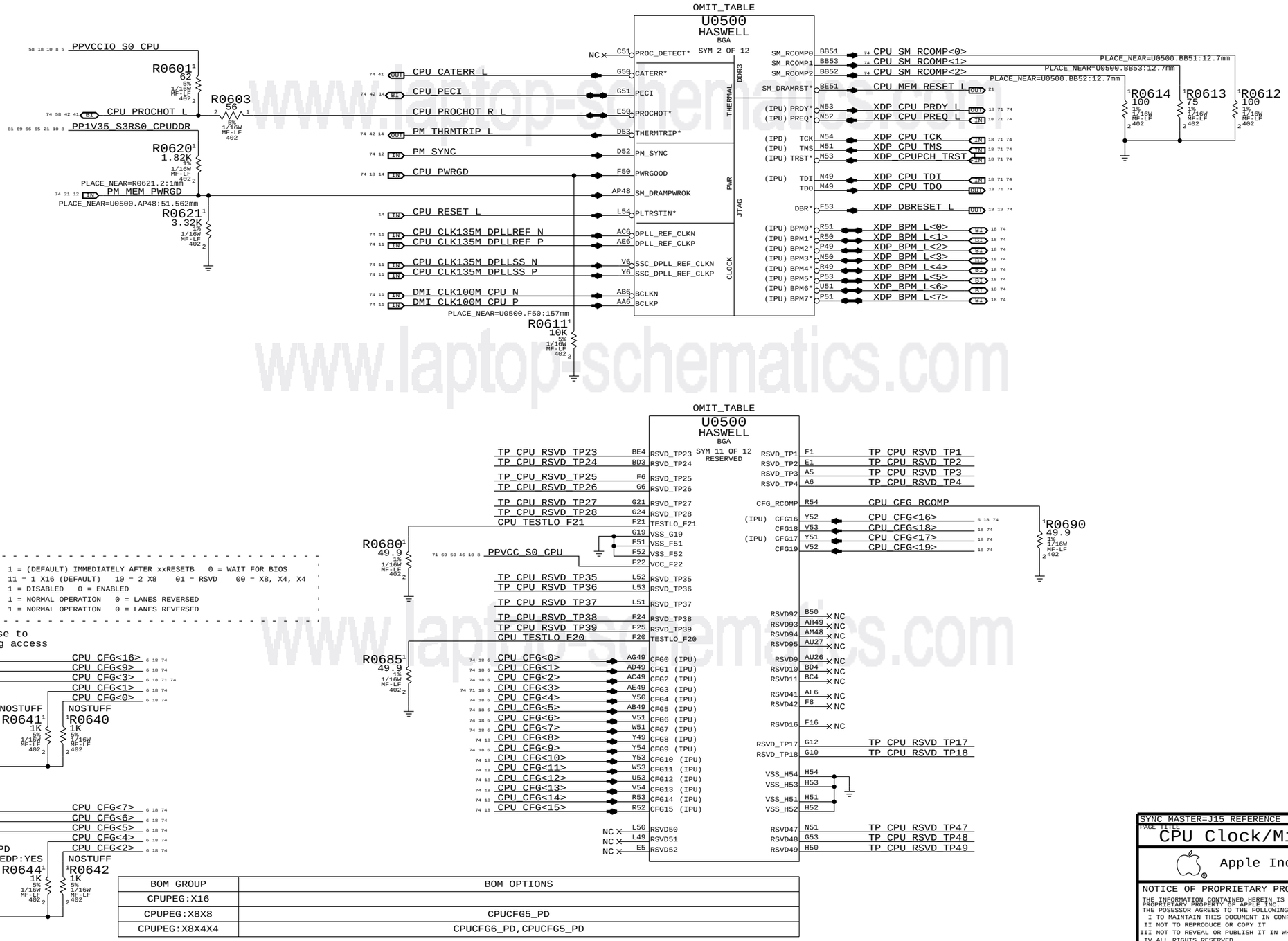
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 5 OF 118
SHEET: 5 OF 81



BOM GROUP	BOM OPTIONS
CPUPEG:X16	
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

SYNC_MASTER=J15 REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

CPU Clock/Misc/JTAG/CFG

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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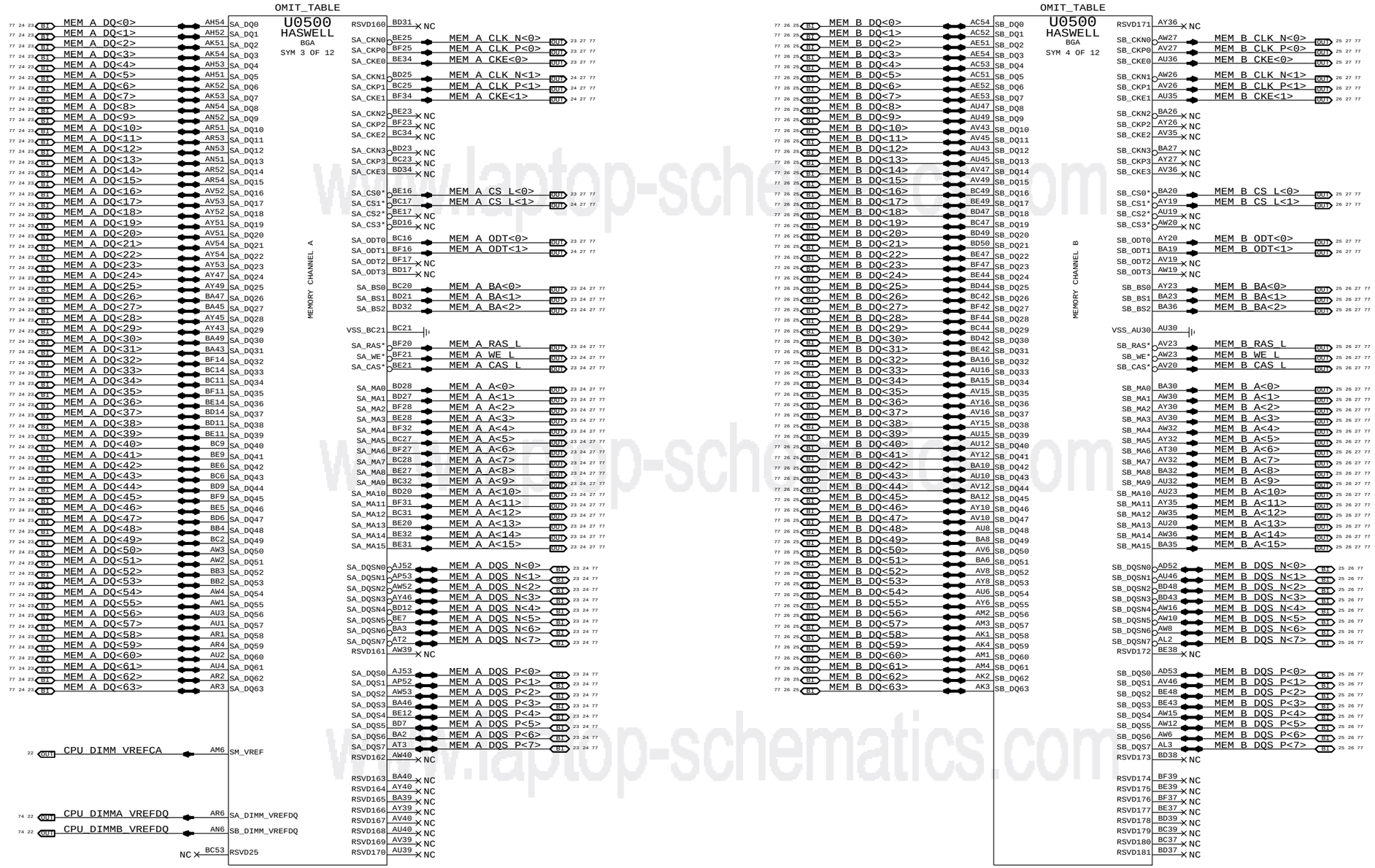
PAGE 6 OF 118

SHEET 6 OF 81



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PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

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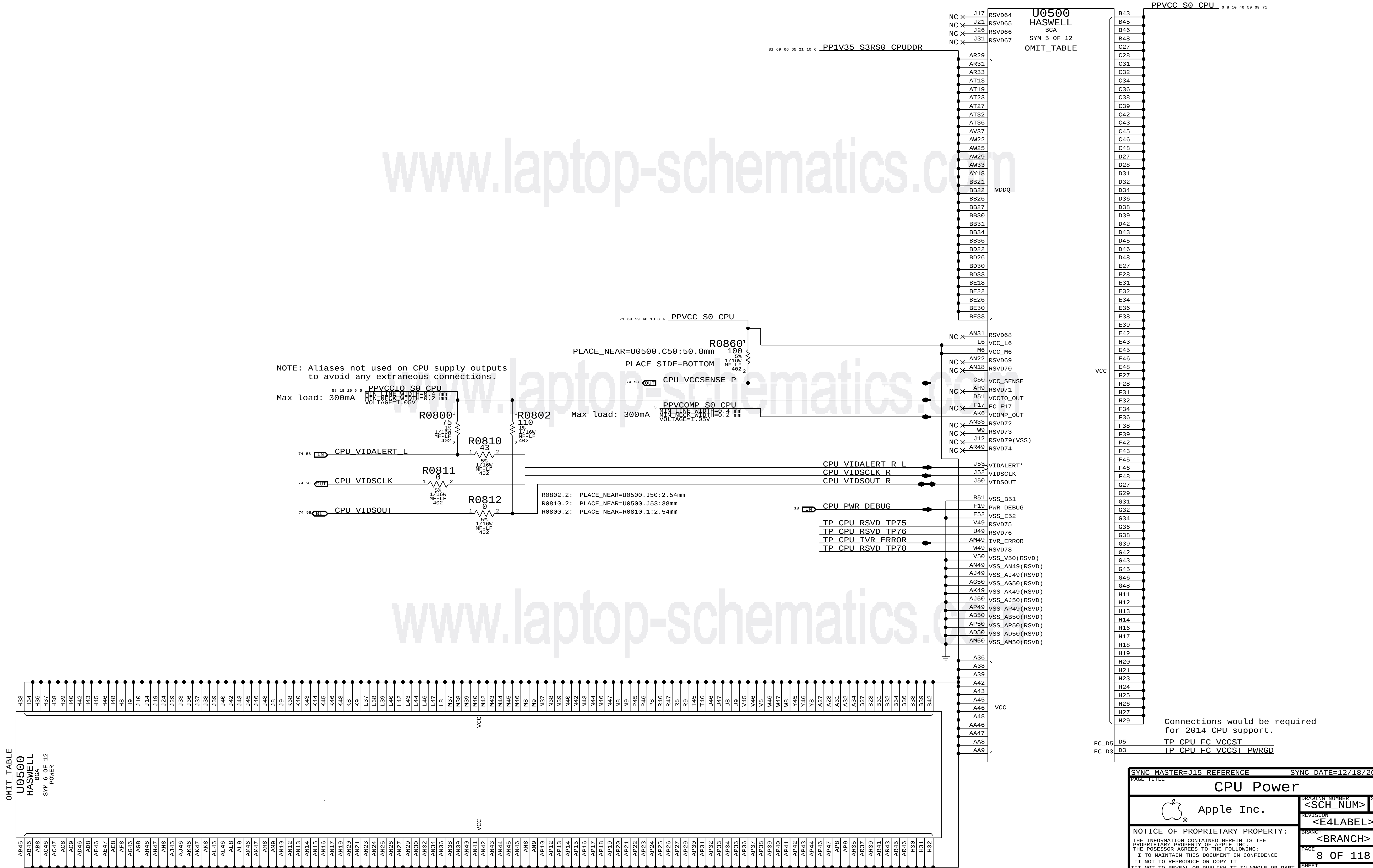
PAGE 7 OF 118

SHEET 7 OF 81



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Apple Inc.

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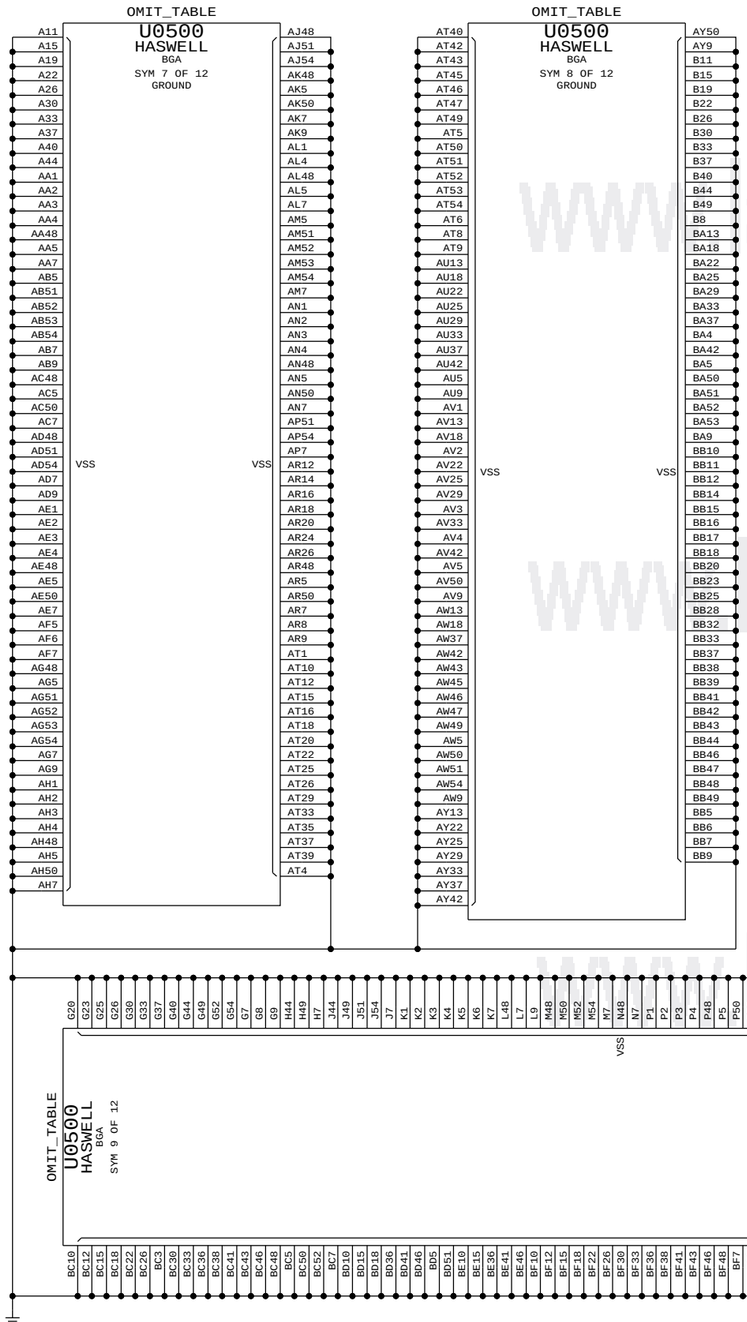

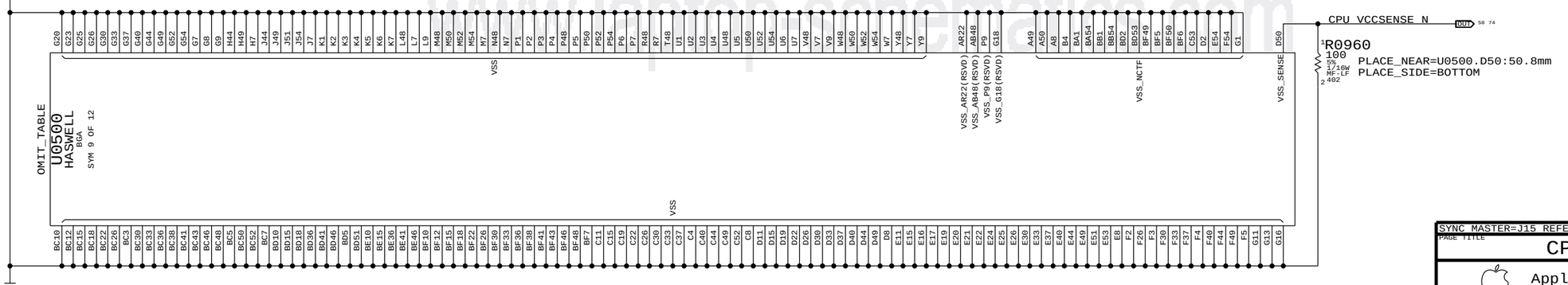

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PAGE TITLE

CPU Ground

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DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 9 OF 118

SHEET 9 OF 81

CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 8x 210uF(2x nostuff) 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

PPVCC_S0_CPU

PLACEMENT_NOTE (C1000-C1019):
Place on bottom side of U0500

C1000 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1001 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1002 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1003 1UF 10% 10V X6S-CERM 0402
C1004 1UF 10% 10V X6S-CERM 0402
C1005 1UF 10% 10V X6S-CERM 0402
C1006 1UF 10% 10V X6S-CERM 0402
C1007 1UF 10% 10V X6S-CERM 0402
C1008 1UF 10% 10V X6S-CERM 0402
C1009 1UF 10% 10V X6S-CERM 0402
C1010 1UF 10% 10V X6S-CERM 0402
C1011 1UF 10% 10V X6S-CERM 0402
C1012 1UF 10% 10V X6S-CERM 0402
C1013 1UF 10% 10V X6S-CERM 0402
C1014 1UF 10% 10V X6S-CERM 0402
C1015 1UF 10% 10V X6S-CERM 0402
C1016 1UF 10% 10V X6S-CERM 0402
C1017 1UF 10% 10V X6S-CERM 0402
C1018 1UF 10% 10V X6S-CERM 0402
C1019 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1020-C1023):
CAPs for Acoustic control (C109A-C102D)
Place near U0500 on bottom side

C1020 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C1021 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C1022 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C1023 20UF 20% 4V X5R-CERM 0402-2
C109A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109D 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109E 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C109F 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101D 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101E 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C101F 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102D 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF

PLACEMENT_NOTE (C1024-C1045):
Place near inductors on bottom side.

CRITICAL C1024 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1025 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1026 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1027 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1028 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1029 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1030 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1031 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1032 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1033 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1034 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1035 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1036 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1037 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1038 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1039 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1040 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1041 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1042 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1043 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1044 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1045 20UF 20% 4V X5R-CERM 0402-2

PLACEMENT_NOTE (C1046-C1067):
Place near inductors on bottom side.

CRITICAL C1046 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1047 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1048 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1049 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1050 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1051 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1052 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1053 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1054 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1055 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1056 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1057 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1058 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1059 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1060 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1061 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1062 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1063 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1064 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1065 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1066 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1067 20UF 20% 4V X5R-CERM 0402-2

PLACEMENT_NOTE (C1068-C1076:
CAPs for Acoustic control (C102E-C103F)

CRITICAL C1068 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1069 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1070 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1071 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1072 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1073 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1074 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1075 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1076 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1077 210UF 20% 2.5V POLY-TANT CASE-B2S

C102E 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C102F 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103D 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103E 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C103F 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF

CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402

PP1V35_S3RS0_CPUDDR

PLACEMENT_NOTE (C1080-C1089):
Place on bottom side of U0500

C1080 1UF 10% 10V X6S-CERM 0402
C1081 1UF 10% 10V X6S-CERM 0402
C1082 1UF 10% 10V X6S-CERM 0402
C1083 1UF 10% 10V X6S-CERM 0402
C1084 1UF 10% 10V X6S-CERM 0402
C1085 1UF 10% 10V X6S-CERM 0402
C1086 1UF 10% 10V X6S-CERM 0402
C1087 1UF 10% 10V X6S-CERM 0402
C1088 1UF 10% 10V X6S-CERM 0402
C1089 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1090-C1097):
Place near U0500 on bottom side

C1090 10UF 20% 4V X6S-CERM 0603
C1091 10UF 20% 4V X6S-CERM 0603
C1092 10UF 20% 4V X6S-CERM 0603
C1093 10UF 20% 4V X6S-CERM 0603
C1094 10UF 20% 4V X6S-CERM 0603
C1095 10UF 20% 4V X6S-CERM 0603
C1096 10UF 20% 4V X6S-CERM 0603
C1097 10UF 20% 4V X6S-CERM 0603

PLACEMENT_NOTE (C1098-C1099):

CRITICAL C1098 330UF-6MOHM 20% 2.5V POLY-TANT D1ST-ECGLT-COMBO
CRITICAL C1099 330UF-6MOHM 20% 2.5V POLY-TANT D1ST-ECGLT-COMBO
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

CPU VCCIO Decoupling

Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

PPVCCIO_S0_CPU

C1079 0.01UF 10% 10V X7R-CERM 0402

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

SYNC MASTER=J15 REFERENCE — SYNC DATE=12/18/2012

PAGE TITLE: CPU Decoupling

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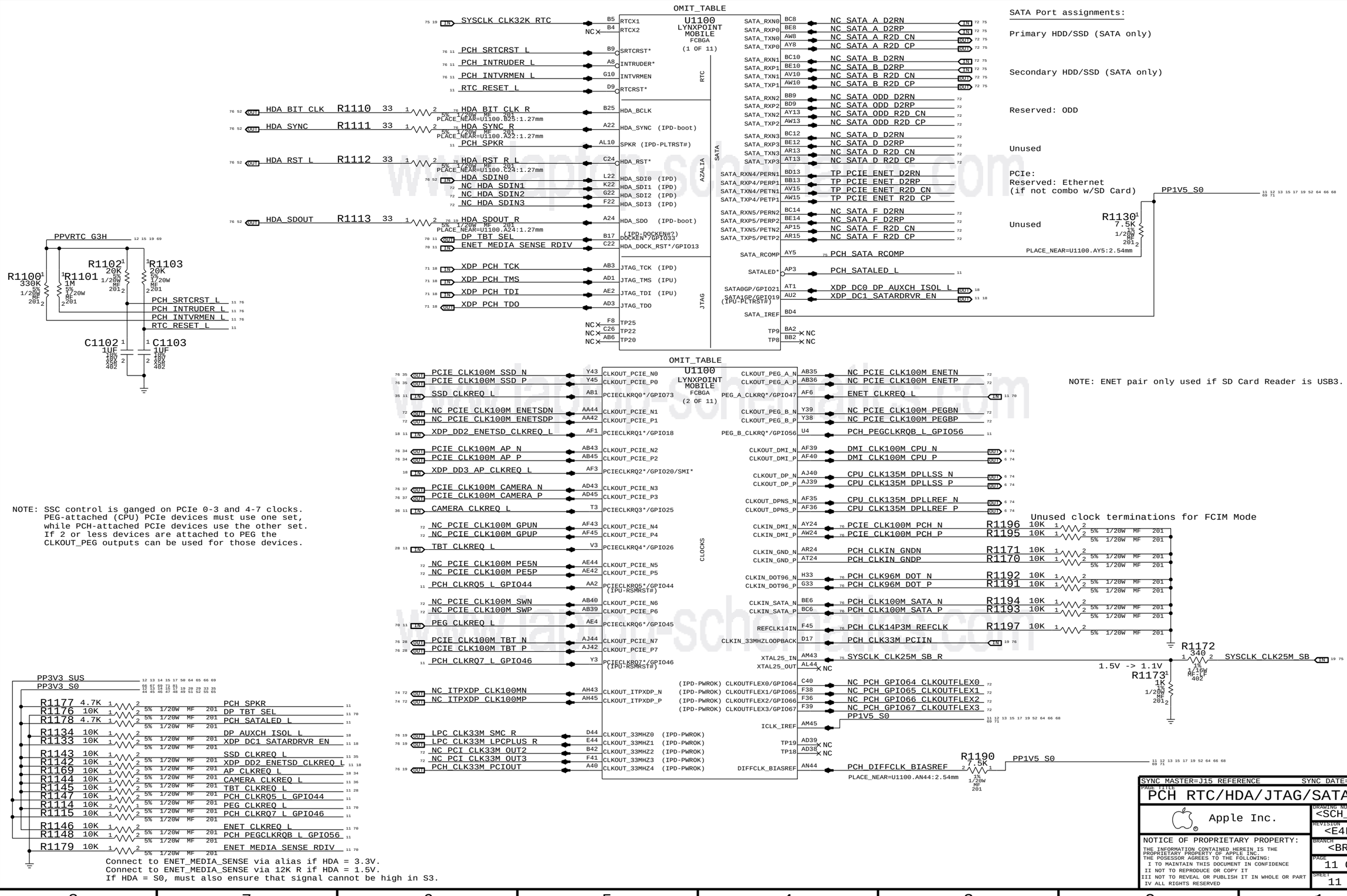
BRANCH: <BRANCH>
PAGE: 10 OF 118
SHEET: 10 OF 81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U1100
LYNXPOINT MOBILE
FCBGA
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SYSCLK_CLK32K_RTC
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
HDA_BIT_CLK
HDA_SYNC
HDA_RST_L
HDA_SDOUT
R1110 33
R1111 33
R1112 33
R1113 33
HDA_BIT_CLK_R
HDA_SYNC_R
HDA_RST_R_L
HDA_SDOUT_R
PLACE_NEAR=U1100.B25:1.27mm
PLACE_NEAR=U1100.A22:1.27mm
PLACE_NEAR=U1100.C24:1.27mm
PLACE_NEAR=U1100.A24:1.27mm
PCH_SPKR
HDA_SDIN0
NC_HDA_SDIN1
NC_HDA_SDIN2
NC_HDA_SDIN3
DP_TBT_SEL
ENET_MEDIA_SENSE_RDIV
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
RTC
AZALIA
JTAG
SATA
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
SATA_RXN2
SATA_RXP2
SATA_TXN2
SATA_TXP2
SATA_RXN3
SATA_RXP3
SATA_TXN3
SATA_TXP3
SATA_RXN4/PERN1
SATA_RXP4/PERP1
SATA_TXN4/PETN1
SATA_TXP4/PETP1
SATA_RXN5/PERN2
SATA_RXP5/PERP2
SATA_TXN5/PETN2
SATA_TXP5/PETP2
SATA_RCOMP
SATALED*
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA_IREF
NC_SATA_A_D2RN
NC_SATA_A_D2RP
NC_SATA_A_R2D_CN
NC_SATA_A_R2D_CP
NC_SATA_B_D2RN
NC_SATA_B_D2RP
NC_SATA_B_R2D_CN
NC_SATA_B_R2D_CP
NC_SATA_ODD_D2RN
NC_SATA_ODD_D2RP
NC_SATA_ODD_R2D_CN
NC_SATA_ODD_R2D_CP
NC_SATA_D_D2RN
NC_SATA_D_D2RP
NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP
TP_PCIE_ENET_D2RN
TP_PCIE_ENET_D2RP
TP_PCIE_ENET_R2D_CN
TP_PCIE_ENET_R2D_CP
NC_SATA_F_D2RN
NC_SATA_F_D2RP
NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP
PCH_SATA_RCOMP
PCH_SATALED_L
XDP_DC0_DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN
SATA Port assignments:
Primary HDD/SSD (SATA only)
Secondary HDD/SSD (SATA only)
Reserved: ODD
Unused
PCIe:
Reserved: Ethernet
(if not combo w/SD Card)
Unused
PP1V5_S0
R1130 7.5K
PLACE_NEAR=U1100.AY5:2.54mm
OMIT_TABLE
U1100
LYNXPOINT MOBILE
FCBGA
(2 OF 11)
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
SSD_CLKREQ_L
NC_PCIE_CLK100M_ENETSDN
NC_PCIE_CLK100M_ENETSDP
XDP_DD2_ENETSD_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
XDP_DD3_AP_CLKREQ_L
PCIE_CLK100M_CAMERA_N
PCIE_CLK100M_CAMERA_P
CAMERA_CLKREQ_L
NC_PCIE_CLK100M_GPUN
NC_PCIE_CLK100M_GPUP
TBT_CLKREQ_L
NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P
PCH_CLKRQ5_L_GPIO44
NC_PCIE_CLK100M_SWN
NC_PCIE_CLK100M_SWP
PEG_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
PCH_CLKRQ7_L_GPIO46
NC_ITPXDP_CLK100MN
NC_ITPXDP_CLK100MP
LPC_CLK33M_SMC_R
LPC_CLK33M_LPCPLUS_R
NC_PCI_CLK33M_OUT2
NC_PCI_CLK33M_OUT3
PCH_CLK33M_PCIOUT
CLOCKS
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
PCIECLKRQ0*/GPIO73
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
PCIECLKRQ1*/GPIO18
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
PCIECLKRQ2*/GPIO20/SMI*
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
PCIECLKRQ3*/GPIO25
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
PCIECLKRQ4*/GPIO26
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
PCIECLKRQ6*/GPIO45
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_33MHZ0 (IPD-PWROK)
CLKOUT_33MHZ1 (IPD-PWROK)
CLKOUT_33MHZ2 (IPD-PWROK)
CLKOUT_33MHZ3 (IPD-PWROK)
CLKOUT_33MHZ4 (IPD-PWROK)
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
PEG_A_CLKRQ*/GPIO47
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ*/GPIO56
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKOUT_DPNS_N
CLKOUT_DPNS_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND_N
CLKIN_GND_P
CLKIN_DOT96_N
CLKIN_DOT96_P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_33MHZLOOPBACK
XTAL25_IN
XTAL25_OUT
(IPD-PWROK) CLKOUTFLEX0/GPIO64
(IPD-PWROK) CLKOUTFLEX1/GPIO65
(IPD-PWROK) CLKOUTFLEX2/GPIO66
(IPD-PWROK) CLKOUTFLEX3/GPIO67
ICLK_IREF
DIFFCLK_BIASREF
NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3
PP1V5_S0
ENET_CLKREQ_L
NC_PCIE_CLK100M_ENETN
NC_PCIE_CLK100M_ENETP
NC_PCIE_CLK100M_PEGBN
NC_PCIE_CLK100M_PEGBP
PCH_PEGCLKRQB_L_GPIO56
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
CPU_CLK135M_DPLLSS_N
CPU_CLK135M_DPLLSS_P
CPU_CLK135M_DPLLREF_N
CPU_CLK135M_DPLLREF_P
PCH_CLKIN_GNDN
PCH_CLKIN_GNDP
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
SYSCLK_CLK25M_SB_R
SYSCLK_CLK25M_SB
1.5V -> 1.1V
R1173 1K
R1172 340
PCH_DIFFCLK_BIASREF
R1190 7.5K
PLACE_NEAR=U1100.AN44:2.54mm
Unused clock terminations for FCIM Mode
R1196 10K
R1195 10K
R1171 10K
R1170 10K
R1192 10K
R1191 10K
R1194 10K
R1193 10K
R1197 10K
NOTE: ENET pair only used if SD Card Reader is USB3.
PPVRTC_G3H
R1100 330K
R1101 1M
R1102 20K
R1103 20K
C1102 1UF
C1103 1UF
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.
PP3V3_SUS
PP3V3_S0
R1177 4.7K PCH_SPKR
R1176 10K DP_TBT_SEL
R1178 4.7K PCH_SATALED_L
R1134 10K DP_AUXCH_ISOL_L
R1133 10K XDP_DC1_SATARDRVR_EN
R1143 10K SSD_CLKREQ_L
R1142 10K XDP_DD2_ENETSD_CLKREQ_L
R1169 10K AP_CLKREQ_L
R1144 10K CAMERA_CLKREQ_L
R1145 10K TBT_CLKREQ_L
R1147 10K PCH_CLKRQ5_L_GPIO44
R1114 10K PEG_CLKREQ_L
R1115 10K PCH_CLKRQ7_L_GPIO46
R1146 10K ENET_CLKREQ_L
R1148 10K PCH_PEGCLKRQB_L_GPIO56
R1179 10K ENET_MEDIA_SENSE_RDIV
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.
SYNC_MASTER=J15_REFERENCE
SYNC_DATE=12/18/2012
PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
11 OF 118
SHEET
11 OF 81
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OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(4 OF 11)

DMI_RXN0 AW22 ← DMI N2S N<0>
DMI_RXN1 AR20 ← DMI N2S N<1>
DMI_RXN2 AP17 ← DMI N2S N<2>
DMI_RXN3 AV20 ← DMI N2S N<3>
DMI_RXP0 AY22 ← DMI N2S P<0>
DMI_RXP1 AP20 ← DMI N2S P<1>
DMI_RXP2 AR17 ← DMI N2S P<2>
DMI_RXP3 AW20 ← DMI N2S P<3>
DMI_TXN0 BD21 → DMI S2N N<0>
DMI_TXN1 BE20 → DMI S2N N<1>
DMI_TXN2 BD17 → DMI S2N N<2>
DMI_TXN3 BE18 → DMI S2N N<3>
DMI_TXP0 BB21 → DMI S2N P<0>
DMI_TXP1 BC20 → DMI S2N P<1>
DMI_TXP2 BB17 → DMI S2N P<2>
DMI_TXP3 BC18 → DMI S2N P<3>
DMI_IREF BE16 ← PP1V5_S0 via R1200 7.5K 1% 1/20W MF 201 (PLACE_NEAR=U1100.AY17:12.7mm)
TP12 AW17 → NC
TP7 AV17 → NC
DMI_RCOMP AY17 ← PCH_DMI_RCOMP

FDI_RXN0 AJ35 → NC
FDI_RXN1 AL35 → NC
FDI_RXP0 AJ36 → NC
FDI_RXP1 AL36 → NC
TP16 AV43 → NC
TP5 AY45 → NC
TP15 AV45 → NC
TP10 AW44 → NC
FDI_CSYNC AL39 ← FDI_CSYNC (OUT)
FDI_INT AL40 ← FDI_INT (OUT)
FDI_IREF AT45 ← PP1V5_S0 via R1210 7.5K 1% 1/20W MF 201 (PLACE_NEAR=U1100.AR44:12.7mm)
TP17 AU42 → NC
TP13 AU44 → NC
FDI_RCOMP AR44 ← PCH_FDI_RCOMP

PPVRTC_G3H → R1215 330K 5% 1/20W MF 201

DMI
FDI

SYSTEM POWER MANAGEMENT

PCH_SUSACK_L → SUSACK* (IPU) R6
PM_SYSRST_L ← SYS_RESET* AM1
PM_PCH_SYS_PWROK ← SYS_PWROK AD7
PM_PCH_PWROK ← PWROK F10
PM_PCH_PWROK ← APWROK AB7
PM_MEM_PWRGD → DRAMPWROK (OD) H3
PM_RSMRST_L ← RSMRST* J2
PCH_SUSWARN_L → SUSWARN*/SUSPWRNACK/GPIO30 J4
PM_PWRBTN_L ← PWRBTN* (IPU) K1
SMC_ADAPTER_EN ← ACPRESENT/GPIO31 (IPD-DeepSx) E6
PM_BATLOW_L ← BATLOW*/GPIO72 K7
PCH_RI_L ← RI* N4
TP_PCH_SLP_S0_L ← TP21 AB10
TP_PCH_SLP_WLAN_L ← SLP_WLAN*/GPIO29 D2

R1286 0 5% 1/20W MF 0201
R1205 10K 5% 1/20W MF 201
PP3V3_SUS

DSWVRMEN C8 ← PCH_DSWVRMEN
DPWROK L13 ← PM_DSW_PWRGD
WAKE* (IPD-DeepSx) K3 ↔ PCIE_WAKE_L
CLKRUN* AN7 ↔ PM_CLKRUN_L
SUS_STAT*/GPIO61 U7 → LPC_PWRDWN_L
SUSCLK/GPIO62 (IPU-RSMRST#) Y6 → PM_CLK32K_SUSCLK_R
SLP_S5*/GPIO63 Y7 → PM_SLP_S5_L
SLP_S4* C6 → PM_SLP_S4_L
SLP_S3* H1 → PM_SLP_S3_L
SLP_A* F3 → TP_PM_SLP_A_L
SLP_SUS* F1 → PM_SLP_SUS_L
PMSYNCH AY3 → PM_SYNC
SLP_LAN* G5 → TP_PCH_SLP_LAN_L

R1209 100K 5% 1/20W MF 201

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(5 OF 11)

VGA_BLUE T45 → NC
VGA_GREEN U44 → NC
VGA_RED V45 → NC
VGA_DDC_CLK M43 → NC
VGA_DDC_DATA M45 → NC
VGA_HSYNC N42 → NC
VGA_VSYNC N44 → NC
DAC_IREF U40 ← R1260 10K 1% 1/20W MF 201 (VGA DAC Disabled per SB DG v1.0 (Table 12-18).)
VGA_IRTN U39 → PP3V3_S0

CRT
DISPLAY
EDP

EDP_BKLTCTL N36 ← EDP_IG_BKL_PWM (OUT)
EDP_BKLTEN K36 ← EDP_IG_BKL_ON (OUT)
EDP_VDDEN G36 ← EDP_IG_PANEL_PWR (OUT)

DDPB_CTRLCLK R40 → DP_TBTSNK0_DDC_CLK
DDPB_CTRLDATA (IPD-PLTRST#) R39 → DP_TBTSNK0_DDC_DATA
DDPC_CTRLCLK R35 → DP_TBTSNK1_DDC_CLK
DDPC_CTRLDATA (IPD-PLTRST#) R36 → DP_TBTSNK1_DDC_DATA
DDPD_CTRLCLK N40 → HDMI_DDC_CLK
DDPD_CTRLDATA (IPD-PLTRST#) N38 → HDMI_DDC_DATA
DDPB_AUXN H45 → DP_TBTSNK0_AUXCH_C_N
DDPC_AUXN K43 → DP_TBTSNK1_AUXCH_C_N
DDPD_AUXN J42 → NC_DP_IG_D_AUXCHN
DDPB_AUXP H43 → DP_TBTSNK0_AUXCH_C_P
DDPC_AUXP K45 → DP_TBTSNK1_AUXCH_C_P
DDPD_AUXP J44 → NC_DP_IG_D_AUXCHP
DDPB_HPD K40 ← DP_TBTSNK0_HPD
DDPC_HPD K38 ← DP_TBTSNK1_HPD
DDPD_HPD H39 ← HDMI_HPD

PCI

PIRQA* H20 ← PCI_INTA_L
PIRQB* L20 ← PCI_INTB_L
PIRQC* K17 ← PCI_INTC_L
PIRQD* M20 ← PCI_INTD_L
GPIO50 A12 ↔ ENET_LOW_PWR_PCH
GPIO52 B13 ↔ AUD_IPHS_SWITCH_EN_PCH
GPIO54 C12 ↔ BT_PWRRST_L
GPIO51 C10 ← TP_PCH_STRP_BBS1
GPIO53 A10 ← TP_PCH_STRP_ESI_L
GPIO55 AL6 ← PCH_STRP_TOPBLK_SWP_L
PIRQE*/GPIO2 G17 ↔ SDCONN_OC_L
PIRQF*/GPIO3 F17 ↔ AUD_IP_PERIPHERAL_DET
PIRQG*/GPIO4 L15 ↔ TBT_PWR_REQ_L
PIRQH*/GPIO5 M15 ↔ AUD_I2C_INT_L
(IPU) PME* AD10 → NC_PCI_PME_L
PLTRST* Y11 → PLT_RESET_L (OUT)
(IPU-PWROK&PCIRST#)

R1260 10K 5% 1/20W MF 201
R1261 10K 5% 1/20W MF 201
R1262 10K 5% 1/20W MF 201
R1263 10K 5% 1/20W MF 201
PP3V3_S0

PP3V3_S5
PP3V3_S0

R1239 3.0K 5% 1/20W MF 201 — PM_PWRBTN_L
R1240 10K 5% 1/20W MF 201 — PM_BATLOW_L
R1291 10K 5% 1/20W MF 201 — PM_CLKRUN_L
R1216 10K 5% 1/20W MF 201 — ENET_LOW_PWR_PCH
R1217 100K 5% 1/20W MF 201 — AUD_IPHS_SWITCH_EN_PCH
R1218 10K 5% 1/20W MF 201 — BT_PWRRST_L
R1230 10K 5% 1/20W MF 201 — SDCONN_OC_L

NO STUFF Redundant to pull-up on audio page

R1214 100K 5% 1/20W MF 201 — AUD_IP_PERIPHERAL_DET
R1231 10K 5% 1/20W MF 201 — TBT_PWR_REQ_L

NO STUFF Redundant to pull-up on audio page

R1233 10K 5% 1/20W MF 201 — AUD_I2C_INT_L
R1225 1K 5% 1/20W MF 201 — PCIE_WAKE_L
R1224 100K 5% 1/20W MF 201 — PM_SLP_S3_L
R1221 100K 5% 1/20W MF 201 — PM_SLP_S4_L
R1222 100K 5% 1/20W MF 201 — PM_SLP_S5_L
R1223 100K 5% 1/20W MF 201 — PM_SLP_SUS_L
R1281 100K 5% 1/20W MF 201 — EDP_IG_BKL_ON
R1284 100K 5% 1/20W MF 201 — EDP_IG_PANEL_PWR

SYNC_MASTER=J15 REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: PCH DMI/FDI/PM/GFX/PCI

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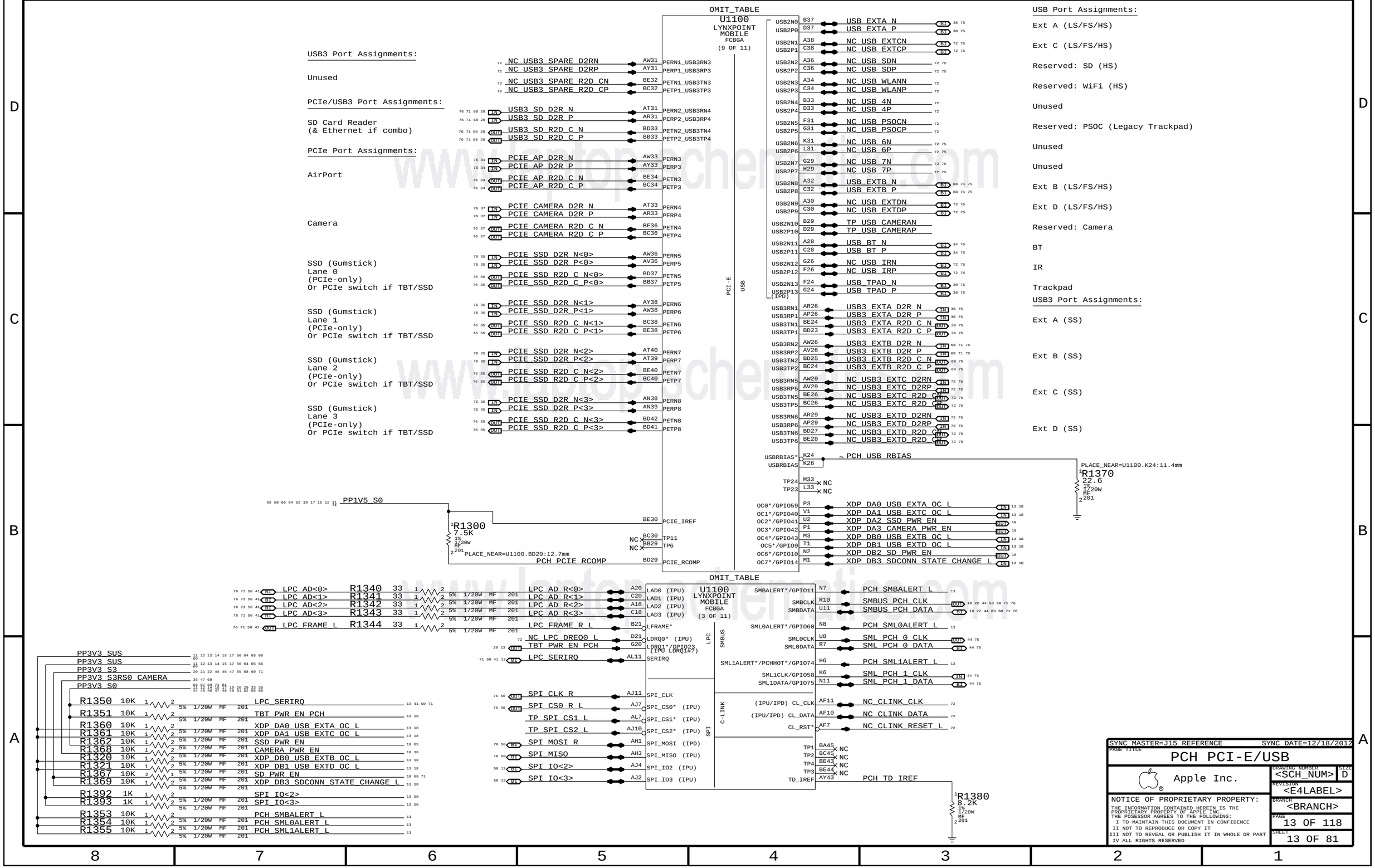
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 12 OF 118
SHEET: 12 OF 81


OMIT_TABLE
U1100
LYNXPOINT MOBILE
FCBGA
(9 OF 11)
PCI-E
USB
USB3 Port Assignments:
Unused
PCIe/USB3 Port Assignments:
SD Card Reader
(& Ethernet if combo)
PCIe Port Assignments:
AirPort
Camera
SSD (Gumstick)
Lane 0
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 1
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 2
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 3
(PCIe-only)
Or PCIe switch if TBT/SSD
NC_USB3_SPARE_D2RN
NC_USB3_SPARE_D2RP
NC_USB3_SPARE_R2D_CN
NC_USB3_SPARE_R2D_CP
USB3_SD_D2R_N
USB3_SD_D2R_P
USB3_SD_R2D_C_N
USB3_SD_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_CAMERA_D2R_N
PCIE_CAMERA_D2R_P
PCIE_CAMERA_R2D_C_N
PCIE_CAMERA_R2D_C_P
PCIE_SSD_D2R_N<0>
PCIE_SSD_D2R_P<0>
PCIE_SSD_R2D_C_N<0>
PCIE_SSD_R2D_C_P<0>
PCIE_SSD_D2R_N<1>
PCIE_SSD_D2R_P<1>
PCIE_SSD_R2D_C_N<1>
PCIE_SSD_R2D_C_P<1>
PCIE_SSD_D2R_N<2>
PCIE_SSD_D2R_P<2>
PCIE_SSD_R2D_C_N<2>
PCIE_SSD_R2D_C_P<2>
PCIE_SSD_D2R_N<3>
PCIE_SSD_D2R_P<3>
PCIE_SSD_R2D_C_N<3>
PCIE_SSD_R2D_C_P<3>
PP1V5_S0
R1300 7.5K 1% 1/20W MF 201
PLACE_NEAR=U1100.BD29:12.7mm
PCH_PCIE_RCOMP
PCIE_IREF
TP11
TP6
PCIE_RCOMP
USB Port Assignments:
Ext A (LS/FS/HS)
Ext C (LS/FS/HS)
Reserved: SD (HS)
Reserved: WiFi (HS)
Unused
Reserved: PSOC (Legacy Trackpad)
Unused
Unused
Ext B (LS/FS/HS)
Ext D (LS/FS/HS)
Reserved: Camera
BT
IR
Trackpad
USB3 Port Assignments:
Ext A (SS)
Ext B (SS)
Ext C (SS)
Ext D (SS)
USB_EXTA_N
USB_EXTA_P
NC_USB_EXTCN
NC_USB_EXTCP
NC_USB_SDN
NC_USB_SDP
NC_USB_WLANN
NC_USB_WLANP
NC_USB_4N
NC_USB_4P
NC_USB_PSOCN
NC_USB_PSOCP
NC_USB_6N
NC_USB_6P
NC_USB_7N
NC_USB_7P
USB_EXTB_N
USB_EXTB_P
NC_USB_EXTDN
NC_USB_EXTDP
TP_USB_CAMERAN
TP_USB_CAMERAP
USB_BT_N
USB_BT_P
NC_USB_IRN
NC_USB_IRP
USB_TPAD_N
USB_TPAD_P
USB3_EXTA_D2R_N
USB3_EXTA_D2R_P
USB3_EXTA_R2D_C_N
USB3_EXTA_R2D_C_P
USB3_EXTB_D2R_N
USB3_EXTB_D2R_P
USB3_EXTB_R2D_C_N
USB3_EXTB_R2D_C_P
NC_USB3_EXTC_D2RN
NC_USB3_EXTC_D2RP
NC_USB3_EXTC_R2D_GN
NC_USB3_EXTC_R2D_GP
NC_USB3_EXTD_D2RN
NC_USB3_EXTD_D2RP
NC_USB3_EXTD_R2D_GN
NC_USB3_EXTD_R2D_GP
PCH_USB_RBIAS
PLACE_NEAR=U1100.K24:11.4mm
R1370 22.6 1% 1/20W MF 201
XDP_DA0_USB_EXTA_OC_L
XDP_DA1_USB_EXTC_OC_L
XDP_DA2_SSD_PWR_EN
XDP_DA3_CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L
XDP_DB1_USB_EXTD_OC_L
XDP_DB2_SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L
OMIT_TABLE
U1100
LYNXPOINT MOBILE
FCBGA
(3 OF 11)
LPC
SMBUS
C-LINK
SPI
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_FRAME_L
R1340 33 5% 1/20W MF 201
R1341 33 5% 1/20W MF 201
R1342 33 5% 1/20W MF 201
R1343 33 5% 1/20W MF 201
R1344 33 5% 1/20W MF 201
LPC_AD_R<0>
LPC_AD_R<1>
LPC_AD_R<2>
LPC_AD_R<3>
LPC_FRAME_R_L
NC_LPC_DREQ0_L
TBT_PWR_EN_PCH
LPC_SERIRQ
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
TP_SPI_CS2_L
SPI_MOSI_R
SPI_MISO
SPI_IO<2>
SPI_IO<3>
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
(IPD) CL_CLK
(IPD) CL_DATA
CL_RST*
TD_IREF
PCH_SMBALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
PCH_SML0ALERT_L
SML_PCH_0_CLK
SML_PCH_0_DATA
PCH_SML1ALERT_L
SML_PCH_1_CLK
SML_PCH_1_DATA
NC_CLINK_CLK
NC_CLINK_DATA
NC_CLINK_RESET_L
PCH_TD_IREF
R1380 8.2K 1% 1/20W MF 201
PP3V3_SUS
PP3V3_SUS
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0
R1350 10K
R1351 10K
R1360 10K
R1361 10K
R1362 10K
R1368 10K
R1320 10K
R1321 10K
R1367 10K
R1369 10K
R1392 1K
R1393 1K
R1353 10K
R1354 10K
R1355 10K
LPC_SERIRQ
TBT_PWR_EN_PCH
XDP_DA0_USB_EXTA_OC_L
XDP_DA1_USB_EXTC_OC_L
SSD_PWR_EN
CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L
XDP_DB1_USB_EXTD_OC_L
SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L
SPI_IO<2>
SPI_IO<3>
PCH_SMBALERT_L
PCH_SML0ALERT_L
PCH_SML1ALERT_L
SYNC MASTER=J15 REFERENCE
SYNC DATE=12/18/2012
PAGE TITLE
PCH PCI-E/USB
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
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REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
13 OF 118
SHEET
13 OF 81
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Pull-up/down on chipset support page (depends on TBT controller)
Redwood Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(6 OF 11)

CPU/MISC
GPIO

TBT_CIO_PLUG_EVENT_L	AT8	BMBUSY*/GPIO0	
FW_PME_L	F13	TACH1/GPIO1	
DPMUX_UC_IRQ	A14	TACH2/GPIO6	
SMC_RUNTIME_SCI_L	G15	TACH3/GPIO7	
XDP_FC0_HDD_PWR_EN	Y1	GPIO8 (IPU-RSMRST#)	
WOL_EN	K13	LAN_PHY_PWR_CTRL/GPIO12	
MEM_VDD_SEL_1V5_L	AB11	GPIO15	
XDP_DD0_SSD_PCIE_SEL_L	AN2	SATA4GP/GPIO16 (IPU-BOOT/SATA4GP?)	
LPCPLUS_GPIO	C14	TACH0/GPIO17	
JTAG_TBT_TMS_PCH	BB4	SCLOCK/GPIO22	
TBT_GO2SX_BIDIR	Y10	GPIO24	
SMC_WAKE_SCI_L	R11	GPIO27 (IPU-DeepSx)	
ISOLATE_CPU_MEM_L	AD11	GPIO28	
TBT_POC_RESET_L	AN6	GPIO34	
XDP_FC1_GPU_GOOD	AP1	GPIO35/NMI*	
XDP_DC2_ODD_PWR_EN_L	AT3	SATA2GP/GPIO36 (IPD-PLTRST#)	
XDP_DC3_JTAG_ISP_TCK	AK1	SATA3GP/GPIO37 (IPD-PLTRST#)	
JTAG_ISP_TDO	AT7	SLOAD/GPIO38	
JTAG_ISP_TDI	AM3	SDATAOUT0/GPIO39	
FW_PWR_EN_PCH	AN4	SDATAOUT1/GPIO48	
XDP_DD1_MLB_RAMCFG1	AK3	SATA5GP/GPIO49 (IPU-BOOT/SATA5GP?)	
SPIROM_USE_MLB	U12	GPIO57	
MLB_RAMCFG3	C16	TACH4/GPIO68	
MLB_RAMCFG2	D13	TACH5/GPIO69	
SD_SEL_PCIE_L_USB_H	G13	TACH6/GPIO70 (IPU-BOOT?)	
MLB_RAMCFG0	H15	TACH7/GPIO71 (IPU-BOOT?)	
	BE41		
	BE5		
VSS	C45		
	A5		

PCH_A20GATE	AN10	TP14	
PCH_PECI	AY1	(IPD) PECI	
PCH_RCIN_L	AT6	RCIN*	
PCH_PROCPWRGD	AV3	PROCPWRGD	
PM_THRMTRIP_L_R	AV1	THRMTRIP*	
CPU_RESET_L	AU4	PLTRST_PROC*	
	N10	VSS	
	A2		
	A41		
	A43		
	A44		
	B1		
	B2		
	B44		
	B45		
	BA1		
	BC1		
	BD1		
	BD2		
	BD44	VSS	
	BD45		
	BE2		
	BE3		
	D1		
	E1		
	E45		
	A4		

PP3V3_S0

RAMCFG0:H R1475 10K 5% 1/20W MF 201
RAMCFG1:H R1474 10K 5% 1/20W MF 201
RAMCFG2:H R1473 10K 5% 1/20W MF 201
RAMCFG3:H R1472 10K 5% 1/20W MF 201

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

PP1V05_S0
NO STUFF
R1457 1K 5% 1/16W MF-LF 402

NO STUFF
R1470 43 5% 1/20W MF 201 — CPU_PECI
R1440 0 5% 1/20W MF 0201 — CPU_PWRGD
R1456 390 5% 1/20W MF 201 — PM_THRMTRIP_L

PP3V3_S5
PP3V3_SUS
PP3V3_S0

NOTE: GPIO0 pull-up/down on project-specific page

R1485	10K	FW_PME_L	
R1411	20K	DPMUX_UC_IRQ	
R1496	10K	SMC_RUNTIME_SCI_L	
R1494	10K	WOL_EN	
R1489	10K	MEM_VDD_SEL_1V5_L	
R1495	100K	XDP_DD0_SSD_PCIE_SEL_L	
R1490	100K	LPCPLUS_GPIO	
R1412	10K	JTAG_TBT_TMS_PCH	
R1492	10K	TBT_GO2SX_BIDIR	
R1491	10K	SMC_WAKE_SCI_L	
R1498	10K	XDP_DC2_ODD_PWR_EN_L	
R1413	10K	JTAG_ISP_TCK	
R1486	10K	JTAG_ISP_TDO	
R1499	10K	JTAG_ISP_TDI	
R1484	10K	FW_PWR_EN_PCH	
R1493	100K	SPIROM_USE_MLB	

NOTE: GPIO70 pull-up/down on project-specific page

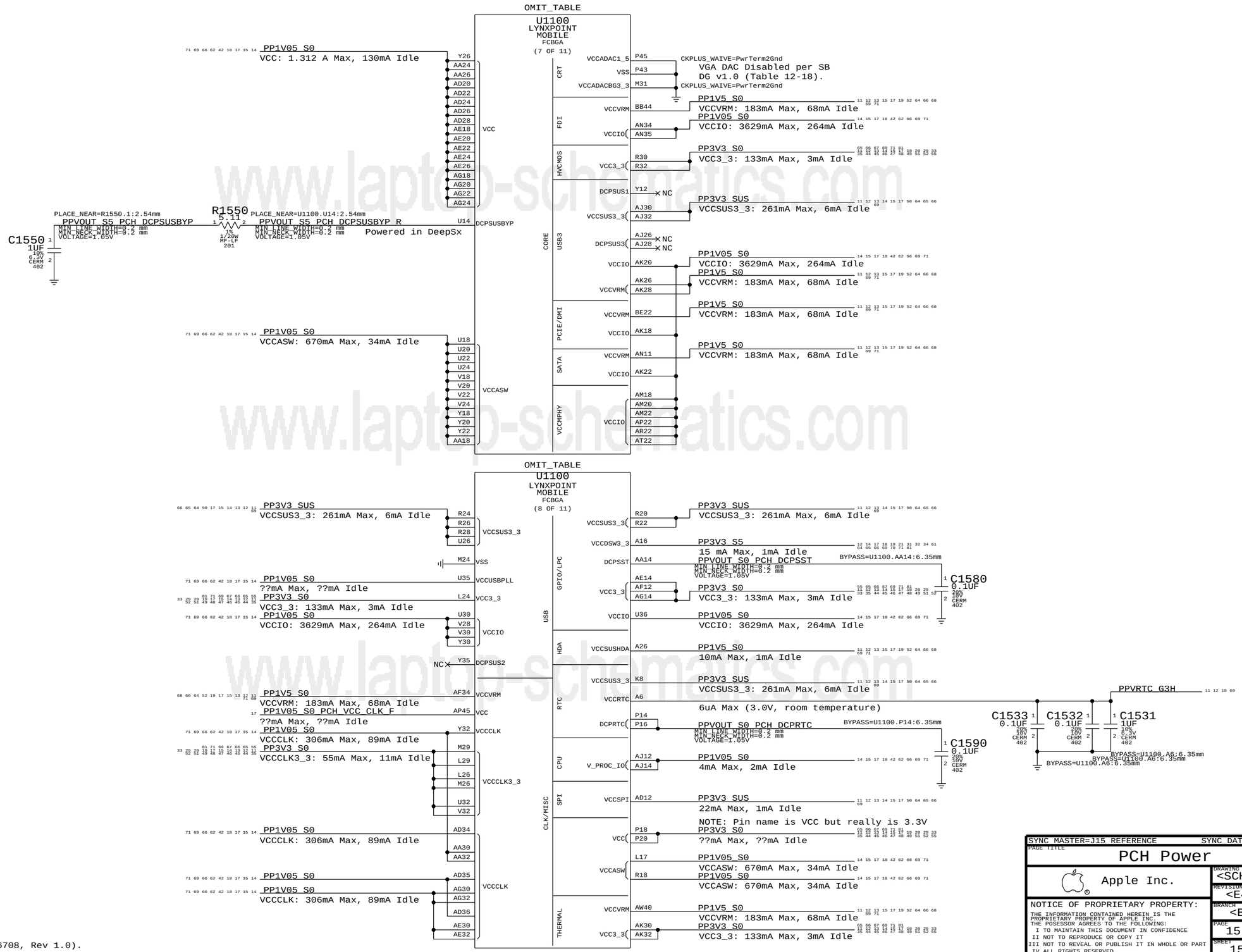
R1450	10K	PCH_A20GATE	
R1455	10K	PCH_RCIN_L	

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: PCH GPIO/MISC/NCTF

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 14 OF 118
SHEET: 14 OF 81



Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

PCH Power

Apple Inc.

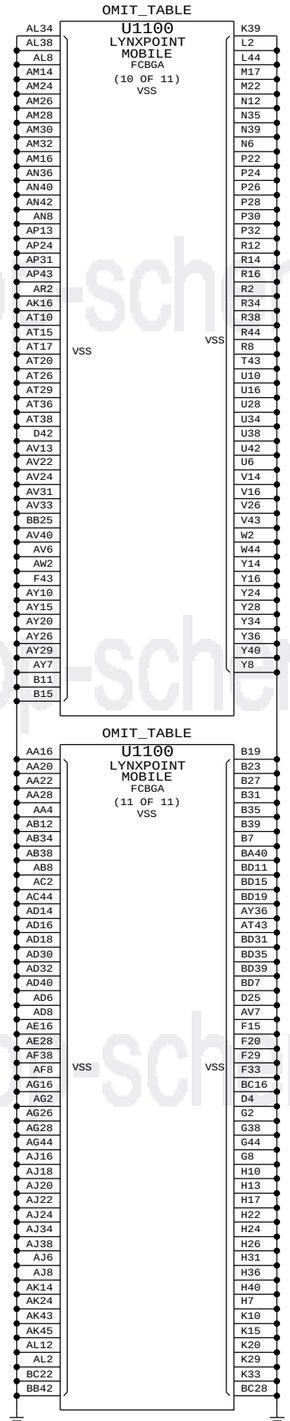
DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 15 OF 118

SHEET 15 OF 81



SYNC MASTER=J15 REFERENCE SYNC DATE=12/18/2012

PAGE TITLE

PCH Grounds

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DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 16 OF 118

SHEET 16 OF 81

PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5

C1700 0.1UF 20% 10V CERM 402
BYPASS=U1100.A16:6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS

C1702 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD12:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS

C1704 0.1UF 10% 16V CERM 402
BYPASS=U1100.R20:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR)
PP3V3_SUS

C1706 0.1UF 10% 16V CERM 402
BYPASS=U1100.R26:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS

C1708 1UF 10% 6.3V CERM 402
BYPASS=U1100.K8:6.35mm

PCH VCCCLK3_3 BYPASS
(PCH 3.3V CLK PWR)
PP3V3_S0

C1720 1UF 10% 6.3V CERM 402
C1721 1UF 10% 6.3V CERM 402
C1722 1UF 10% 6.3V CERM 402
C1723 1UF 10% 6.3V CERM 402
BYPASS=U1100.L26:6.35mm
BYPASS=U1100.L29:6.35mm
BYPASS=U1100.M29:6.35mm
BYPASS=U1100.U32:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR)
PP3V3_S0

C1726 0.1UF 20% 10V CERM 402
BYPASS=U1100.R30:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0

C1728 0.01UF 10% 16V X7R-CERM 0402
BYPASS=U1100.AE14:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR)
PP3V3_S0

C1730 0.1UF 20% 10V CERM 402
BYPASS=U1100.L24:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0

C1732 0.1UF 20% 10V CERM 402
BYPASS=U1100.AK30:6.35mm

PCH VCC BYPASS
(PCH 3.3V FUSE PWR)
PP3V3_S0

C1734 1UF 10% 6.3V CERM 402
BYPASS=U1100.P18:6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
670mA Max, 34mA Idle

C1750 22UF 20% 6.3V X5R-CERM-1 603
C1751 1UF 10% 6.3V CERM 402
C1752 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
Not documented in EDS!

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0

C1755 10UF 20% 6.3V X5R 603
C1756 1UF 10% 6.3V CERM 402
C1757 1UF 10% 6.3V CERM 402
C1758 1UF 10% 6.3V CERM 402
BYPASS=U1100.AG18:12.7mm
BYPASS=U1100.AG22:6.35mm
BYPASS=U1100.AD20:6.35mm
BYPASS=U1100.AE18:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR)
PP1V05_S0

C1760 10UF 20% 6.3V X5R 603
C1761 1UF 10% 6.3V CERM 402
C1762 1UF 10% 6.3V CERM 402
C1763 1UF 10% 6.3V CERM 402
C1764 1UF 10% 6.3V CERM 402
BYPASS=U1100.AK18:12.7mm
BYPASS=U1100.AG18:6.35mm
BYPASS=U1100.AK22:6.35mm
BYPASS=U1100.AK20:6.35mm
BYPASS=U1100.AM18:6.35mm

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR)
PP1V05_S0

C1770 1UF 10% 6.3V CERM 402
BYPASS=U1100.U35:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR)
PP1V05_S0

C1772 1UF 10% 6.3V CERM 402
BYPASS=U1100.AN34:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0

C1774 0.1UF 20% 10V CERM 402
BYPASS=U1100.U30:6.35mm

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR)
PP1V05_S0

C1785 1UF 10% 6.3V CERM 402
C1786 0.1UF 20% 10V CERM 402
C1787 0.1UF 20% 10V CERM 402
BYPASS=U1100.AJ12:12.7mm
BYPASS=U1100.AJ12:6.35mm
BYPASS=U1100.AJ12:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR)
PP1V05_S0

C1776 1UF 10% 6.3V CERM 402
C1777 1UF 10% 6.3V CERM 402
BYPASS=U1100.AE30:6.35mm
BYPASS=U1100.AG30:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR)
PP1V05_S0

C1778 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD35:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR)
PP1V05_S0

C1780 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD34:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR)
PP1V05_S0

C1782 1UF 10% 6.3V CERM 402
BYPASS=U1100.AA30:6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0

C1710 0.1UF 20% 10V CERM 402
BYPASS=U1100.A26:6.35mm

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR)
PP1V5_S0
183mA Max, 68mA Idle
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0

C1740 10UF 20% 6.3V X5R 603
BYPASS=U1100.AF34:12.7mm

PP1V5_S0
??mA Max, ??mA Idle
R1790 1 5% 1/10W MF-LF 402
PP1V5_S0_PCH_VCC_CLK_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
OMIT_TABLE
L1790 4.7UH-170MA-0.321OHM 0603

PCH CLK VCC BYPASS
(PCH 1.05V CLK PLL PWR)
PP1V05_S0_PCH_VCC_CLK_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V

NO STUFF
C1790 10UF 20% 6.3V X5R 603
C1791 1UF 10% 10V X5R 402
BYPASS=U1100.AP45:12.7mm
BYPASS=U1100.AP45:6.35mm

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(020OHM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15 REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE
PCH DECOUPLING

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 17 OF 118
SHEET 17 OF 81

Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

(TP-P6)

Merged (CPU/PCH) Micro2-XDP

PPVCCIO_S0_CPU

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

PP1V05_S0 → R1830 150 5% 1/16W MF-LF 402

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

518S0847

XDP_CPU_PRESENT_L

C1804 0.1UF 10% 6.3V CERM-X5R 0201
R1831 1K 5% 1/16W MF-LF 402
C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
C1806 0.1UF 10% 6.3V CERM-X5R 0201

CPU_PWRGD → R1800 1K 5% 1/20W MF 201 → PLT_RESET_L
PLACE_NEAR=U0500.F50:2.54mm
PLACE_NEAR=U0500.A67:2.54mm

PM_PWRBTN_L → R1802 0 5% 1/20W MF 0201
PLACE_NEAR=U5000.J3:2.54mm

PM_PCH_SYS_PWROK → R1804 0 5% 1/16W MF-LF 402

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_CPU_TCK

R1805 1K 5% 1/20W MF 201

PP1V05_S0 → R1820 51 5% 1/20W MF 201 → XDP_CPU_TDO
PLACE_NEAR=U0500.M49:28mm

R1823 51 → XDP_CPU_TCK
PLACE_NEAR=U0500.N54:28mm

R1824 51 → XDP_CPUPCH_TRST_L
PLACE_NEAR=U0500.M53:28mm

TDI and TMS are terminated in CPU.

CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563
PLACE_NEAR=J1800.51:28mm → XDP_CPU_TDO

CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563
PLACE_NEAR=J1800.53:28mm → XDP_CPUPCH_TRST_L
MAKE_BASE=TRUE

CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563
PLACE_NEAR=J1800.55:28mm → XDP_CPU_TDI

CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563
PLACE_NEAR=J1800.57:28mm → XDP_CPU_TMS

PCH/XDP Signals

OMIT (All 10 R's)

XDP_DA0_USB_EXTA_OC_L	R1890 SHORT		NONE NONE NONE 201
XDP_DA2_SSD_PWR_EN	R1895 SHORT		NONE NONE NONE 201
XDP_DA3_CAMERA_PWR_EN	R1893 SHORT		NONE NONE NONE 201
XDP_DB0_USB_EXTB_OC_L	R1894 SHORT		NONE NONE NONE 201
XDP_DB2_SD_PWR_EN	R1896 SHORT		NONE NONE NONE 201
XDP_DB3_SDCONN_STATE_CHANGE_L	R1897 SHORT		NONE NONE NONE 201
XDP_DC0_DP_AUXCH_ISOL_L	R1872 SHORT		NONE NONE NONE 201
XDP_DC1_SATARDRVR_EN	MAKE_BASE=TRUE		
XDP_DC2_ODD_PWR_EN_L	MAKE_BASE=TRUE		
XDP_DC3_JTAG_ISP_TCK	R1875 SHORT		NONE NONE NONE 201
XDP_DD0_SSD_PCIE_SEL_L	R1876 SHORT		NONE NONE NONE 201
XDP_DD1_MLB_RAMCFG1	MAKE_BASE=TRUE		
XDP_DD2_ENETSD_CLKREQ_L	MAKE_BASE=TRUE		
XDP_DD3_AP_CLKREQ_L	R1879 SHORT		NONE NONE NONE 201

Non-XDP Signals

USB_EXTA_OC_L	XDP_DA0_USB_EXTA_OC_L
SSD_PWR_EN	XDP_DA2_SSD_PWR_EN
CAMERA_PWR_EN	XDP_DA3_CAMERA_PWR_EN
USB_EXTB_OC_L	XDP_DB0_USB_EXTB_OC_L
SD_PWR_EN	XDP_DB2_SD_PWR_EN
SDCONN_STATE_CHANGE_L	XDP_DB3_SDCONN_STATE_CHANGE_L
DP_AUXCH_ISOL_L	XDP_DC0_DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN	XDP_DC1_SATARDRVR_EN
XDP_DC2_ODD_PWR_EN_L	XDP_DC2_ODD_PWR_EN_L
JTAG_ISP_TCK	XDP_DC3_JTAG_ISP_TCK
SSD_PCIE_SEL_L	XDP_DD0_SSD_PCIE_SEL_L
XDP_DD1_MLB_RAMCFG1	XDP_DD1_MLB_RAMCFG1
XDP_DD2_ENETSD_CLKREQ_L	XDP_DD2_ENETSD_CLKREQ_L
AP_CLKREQ_L	XDP_DD3_AP_CLKREQ_L

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
ALL_SYS_PWRGD

C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, GND, NC, NC, A, Y)
R1845 330K 5% 1/20W MF 201

XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

R1860 51 → XDP_PCH_TDO
PLACE_NEAR=U1100.AD3:28mm

R1861 51 → XDP_PCH_TDI
PLACE_NEAR=U1100.AE2:28mm

R1862 51 → XDP_PCH_TMS
PLACE_NEAR=U1100.AD1:28mm

R1866 51 → XDP_PCH_TCK
PLACE_NEAR=U1100.AB3:28mm

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

XDP_DA1_USB_EXTC_OC_L → TP1810
XDP_DB1_USB_EXTD_OC_L → TP1811
XDP_FC0_HDD_PWR_EN → TP1812
XDP_FC1_GPU_GOOD → TP1813

(TP-P6)

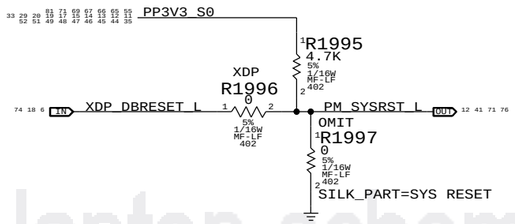
SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012

PAGE TITLE: CPU & PCH XDP

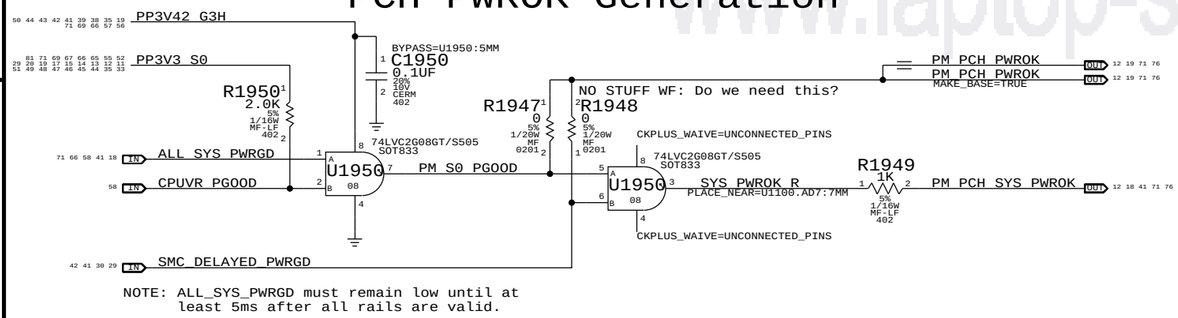
Apple Inc.

DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 18 OF 118
SHEET: 18 OF 81

PCH Reset Button

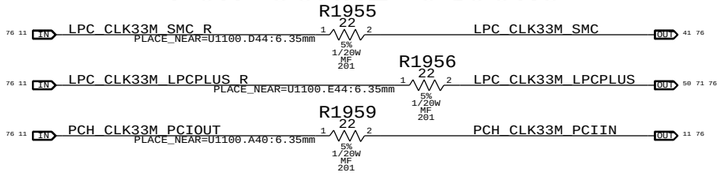


PCH PWROK Generation



NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

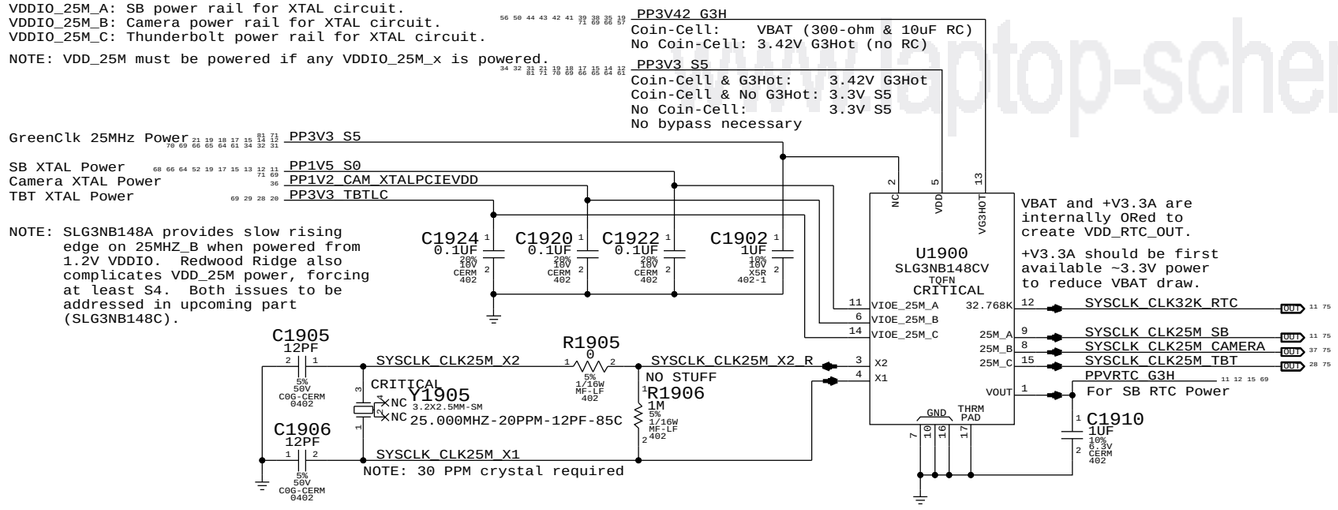
PCH 33MHz Clocks



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

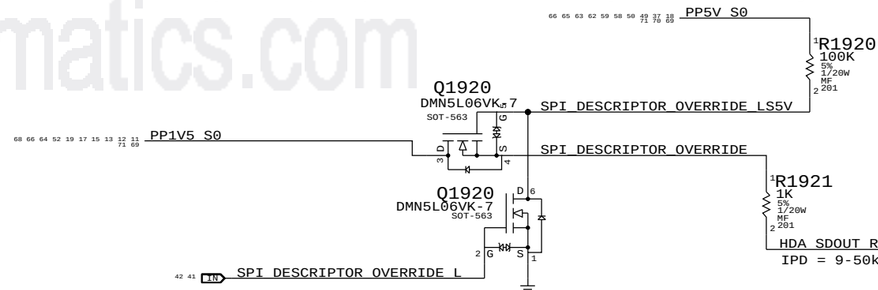


NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Redwood Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).

NOTE: 30 PPM crystal required

PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



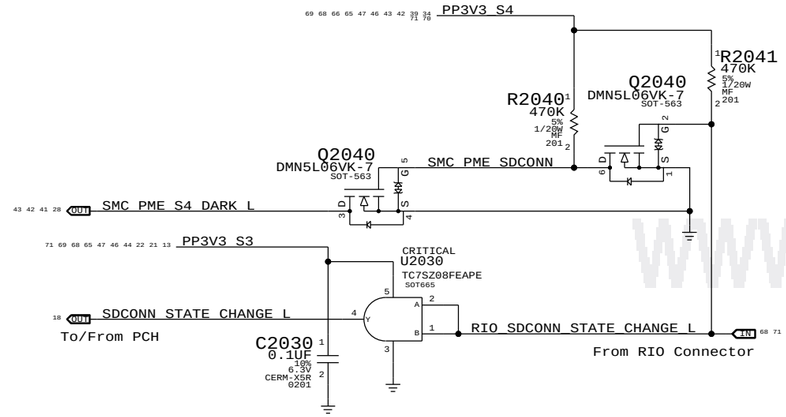
SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: Chipset Support

Apple Inc.

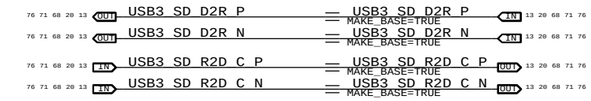
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 19 OF 118
SHEET: 19 OF 81

RIO SD Card Reader Support



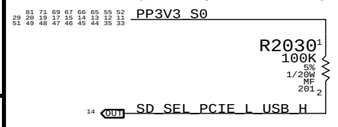
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.



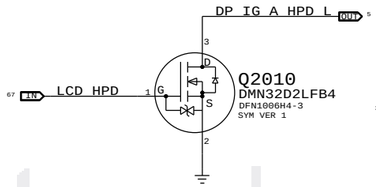
Flexible I/O Configuration Strap

Must pull signal correctly even if always USB or PCIe

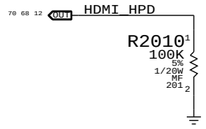


LCD HPD Inverter

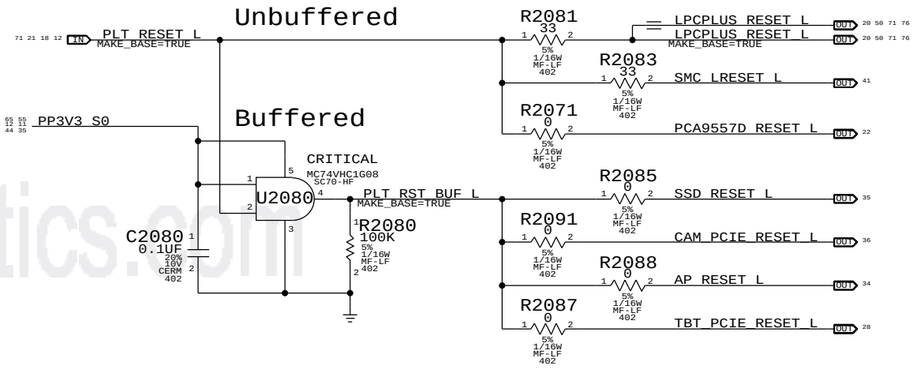
(Pull-Up on CPU Page)



HDMI HPD pull-down

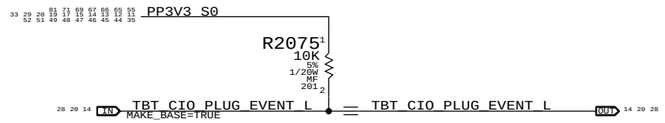


Platform Reset Connections



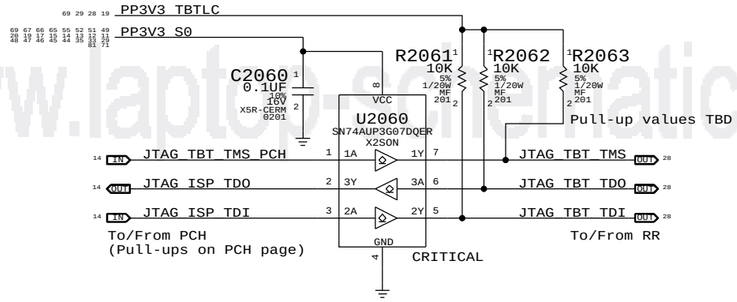
Redwood Ridge Support

RR output is open-drain, no isolation necessary



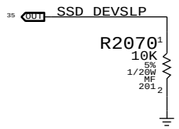
Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V

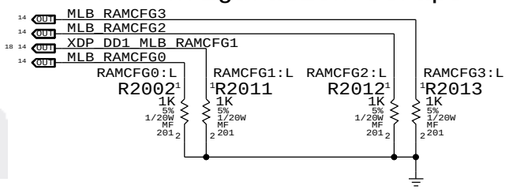


GS3 Connector Support

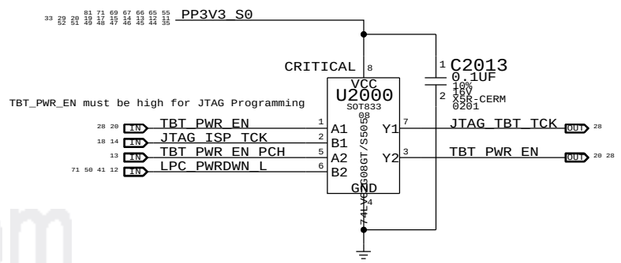
DEVSLP not supported on LPT-H



RAM Configuration Straps



GPIO Glitch Prevention



SYNC_MASTER=J15_REFERENCE SYNC_DATE=01/14/2013

PAGE TITLE: Project Chipset Support

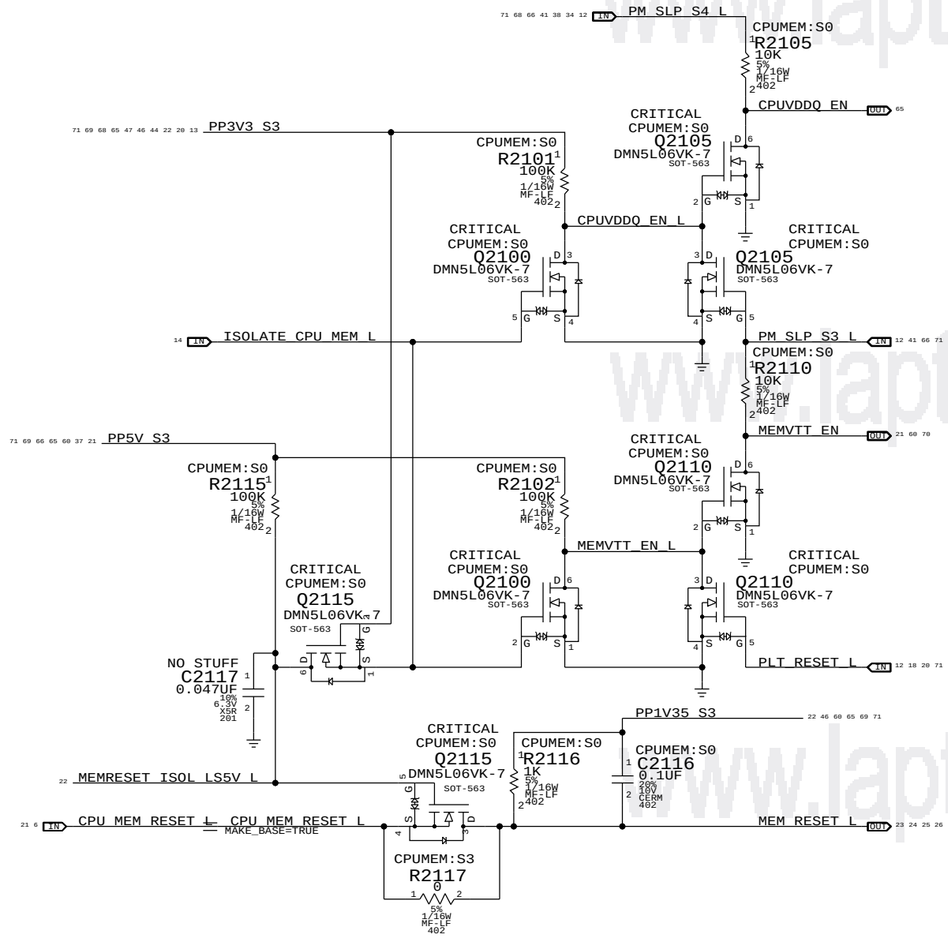
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 20 OF 118
SHEET: 20 OF 81

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

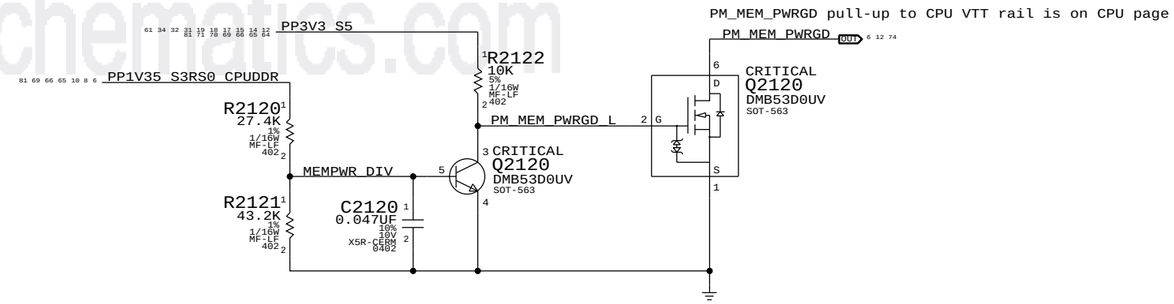
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



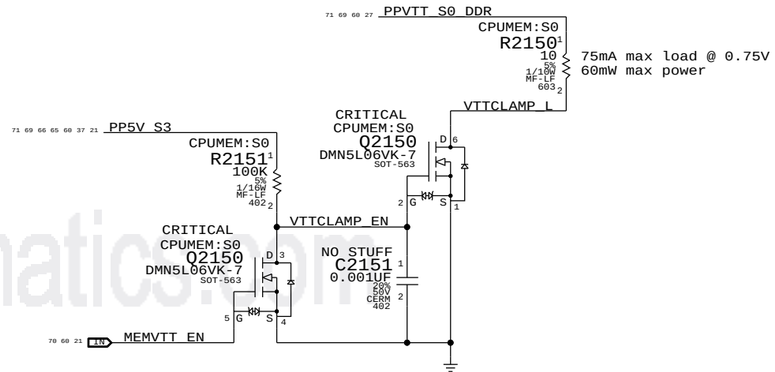
MEM S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 21 OF 118
SHEET: 21 OF 81

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during S3

21 IN MEMRESET_ISOL_LS5V_L
74 7 IN CPU_DIMMA_VREFDQ
74 7 IN CPU_DIMMB_VREFDQ
7 IN CPU_DIMM_VREFCA

CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563
CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.

CPU_MEM_VREFDQ_A_ISOL
DDRVREF_DAC R2225 100K 5% 1/10W MF-LF 402
VREFMRGN_DQ_A_EN_RC
DDRVREF_DAC R2201 100K 5% 1/20W MF 201
DDRVREF_DAC C2225 0.1UF 20% 10V CERM 402
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
Q2225 pin 6: PLACE_NEAR=Q2220.6:2.54mm

CPU_MEM_VREFDQ_B_ISOL
DDRVREF_DAC R2245 100K 5% 1/10W MF-LF 402
VREFMRGN_DQ_B_EN_RC
DDRVREF_DAC R2202 100K 5% 1/20W MF 201
DDRVREF_DAC C2245 0.1UF 20% 10V CERM 402
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
Q2265 pin 6: PLACE_NEAR=Q2260.6:2.54mm

CPU_MEM_VREFCA_A_ISOL
DDRVREF_DAC R2265 100K 5% 1/10W MF-LF 402
VREFMRGN_CA_A_EN_RC
DDRVREF_DAC R2207 100K 5% 1/20W MF 201
DDRVREF_DAC C2265 0.1UF 20% 10V CERM 402
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563

CPU_MEM_VREFCA_B_ISOL
DDRVREF_DAC R2285 100K 5% 1/10W MF-LF 402
VREFMRGN_CA_B_EN_RC
DDRVREF_DAC R2208 100K 5% 1/20W MF 201
DDRVREF_DAC C2285 0.1UF 20% 10V CERM 402
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563

(All 4 R's) DDRVREF_DAC
R2226 332 1% 1/16W MF-LF 402 VREFMRGN_DQ_A_RDIV
R2246 332 1% 1/16W MF-LF 402 VREFMRGN_DQ_B_RDIV
R2266 332 1% 1/16W MF-LF 402 VREFMRGN_CA_A_RDIV
R2286 332 1% 1/16W MF-LF 402 VREFMRGN_CA_B_RDIV

R22x6 pin 2:
PLACE_NEAR=Q2225.1:2.54mm
PLACE_NEAR=Q2225.4:2.54mm
PLACE_NEAR=Q2265.1:2.54mm
PLACE_NEAR=Q2265.4:2.54mm

VRef Dividers

Always used, regardless of margining option.

PP1V35_S3 21 46 60 65 69 71

PLACE_NEAR=C2220.1:2mm
R2223 2 5% 1/20W MF 201
PLACE_NEAR=C2220.6:2mm
C2220 0.022UF 10% 6.3V X5R-CERM 0201
MEM_VREFDQ_A_RC
PLACE_NEAR=R2221.2:1mm
R2222 1K 1% 1/16W MF-LF 402
R2220 24.9 1% 1/20W MF 201
PLACE_NEAR=R2223.2:1mm
PP0V75_S3_MEM_VREFDQ_A 23 24 70 74 77
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

PLACE_NEAR=C2240.1:2mm
R2243 2 5% 1/20W MF 201
PLACE_NEAR=C2240.6:2mm
C2240 0.022UF 10% 6.3V X5R-CERM 0201
MEM_VREFDQ_B_RC
PLACE_NEAR=R2241.2:1mm
R2242 1K 1% 1/16W MF-LF 402
R2240 24.9 1% 1/20W MF 201
PLACE_NEAR=R2243.2:1mm
PP0V75_S3_MEM_VREFDQ_B 23 26 70 74
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

PLACE_NEAR=C2260.1:2mm
R2263 2 5% 1/20W MF 201
PLACE_NEAR=C2260.3:2mm
C2260 0.022UF 10% 6.3V X5R-CERM 0201
MEM_VREFCA_A_RC
PLACE_NEAR=R2261.2:1mm
R2262 1K 1% 1/16W MF-LF 402
R2260 24.9 1% 1/20W MF 201
PLACE_NEAR=R2263.2:1mm
PP0V75_S3_MEM_VREFCA_A 23 24 70 74 77
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

PLACE_NEAR=C2280.1:2mm
R2283 2 5% 1/20W MF 201
PLACE_NEAR=C2280.3:2mm
C2280 0.022UF 10% 6.3V X5R-CERM 0201
MEM_VREFCA_B_RC
PLACE_NEAR=R2281.2:1mm
R2282 1K 1% 1/16W MF-LF 402
R2280 24.9 1% 1/20W MF 201
PLACE_NEAR=R2283.2:1mm
PP0V75_S3_MEM_VREFCA_B 25 26 70 74
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

R2241 1K 1% 1/16W MF-LF 402
R2261 1K 1% 1/16W MF-LF 402
R2281 1K 1% 1/16W MF-LF 402

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

47 46 44 22 71 20 18 13 PP3V3_S3
OMIT R2218 SHORT NONE NONE NONE NONE 402
PP3V3_S3_VREFMRGN MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC
U2200 MSOP DAC5574
VDD 8
SMBUS_PCH_CLK 44 22 18 13 IN → SCL 6
SMBUS_PCH_DATA 44 22 18 13 BI → SDA 7
A0 9
A1 10
GND 3
VOUTA 1 VREFMRGN_DQ_A
VOUTB 2 VREFMRGN_DQ_B
VOUTC 4 VREFMRGN_CA_AB
VOUTD 5 VREFMRGN_MEMVREG_FBVREF
Addr=0x98(WR)/0x99(RD)

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC
U2201 PCA9557 QFN (OD)
VCC 16
Addr=0x30(WR)/0x31(RD)
A0 3
A1 4
A2 5
SMBUS_PCH_CLK 76 71 68 63 44 22 18 13 IN → SCL 1
SMBUS_PCH_DATA 76 71 68 63 44 22 18 13 BI → SDA 2
THRM PAD 17
GND 8
P0 6 NC
P1 7 VREFMRGN_DQ_A_EN
P2 9 VREFMRGN_DQ_B_EN
P3 10 VREFMRGN_CA_A_EN
P4 11 VREFMRGN_CA_B_EN
P5 12 VREFMRGN_MEMVREG_EN
P6 13 VREFMRGN_FRAMEBUF_EN
P7 14 NC
RESET* 15
20 IN PCA9557D_RESET_L

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PP3V3_S3 13 20 21 22 44 46 47 65 68 69 71
DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_MEMVREG_BUF
DDRVREF_DAC R2214 33.2K 1% 1/16W MF-LF 402
DDRREG_FB OUT 60

DDRVREF_DAC R2213 100K 5% 1/20W MF 201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_FRAMEBUF_BUF
DDRVREF_DAC R2217 1M 5% 1/10W MF-LF 402

Pins B1 & B4:
CKPLUS_WAIVE=unconnected_pins

DDRVREF_DAC R2215 100K 5% 1/20W MF 201

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	DDR3 (1.5V)		DDR3L (1.35V)		DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output	3.923mV / step @ output

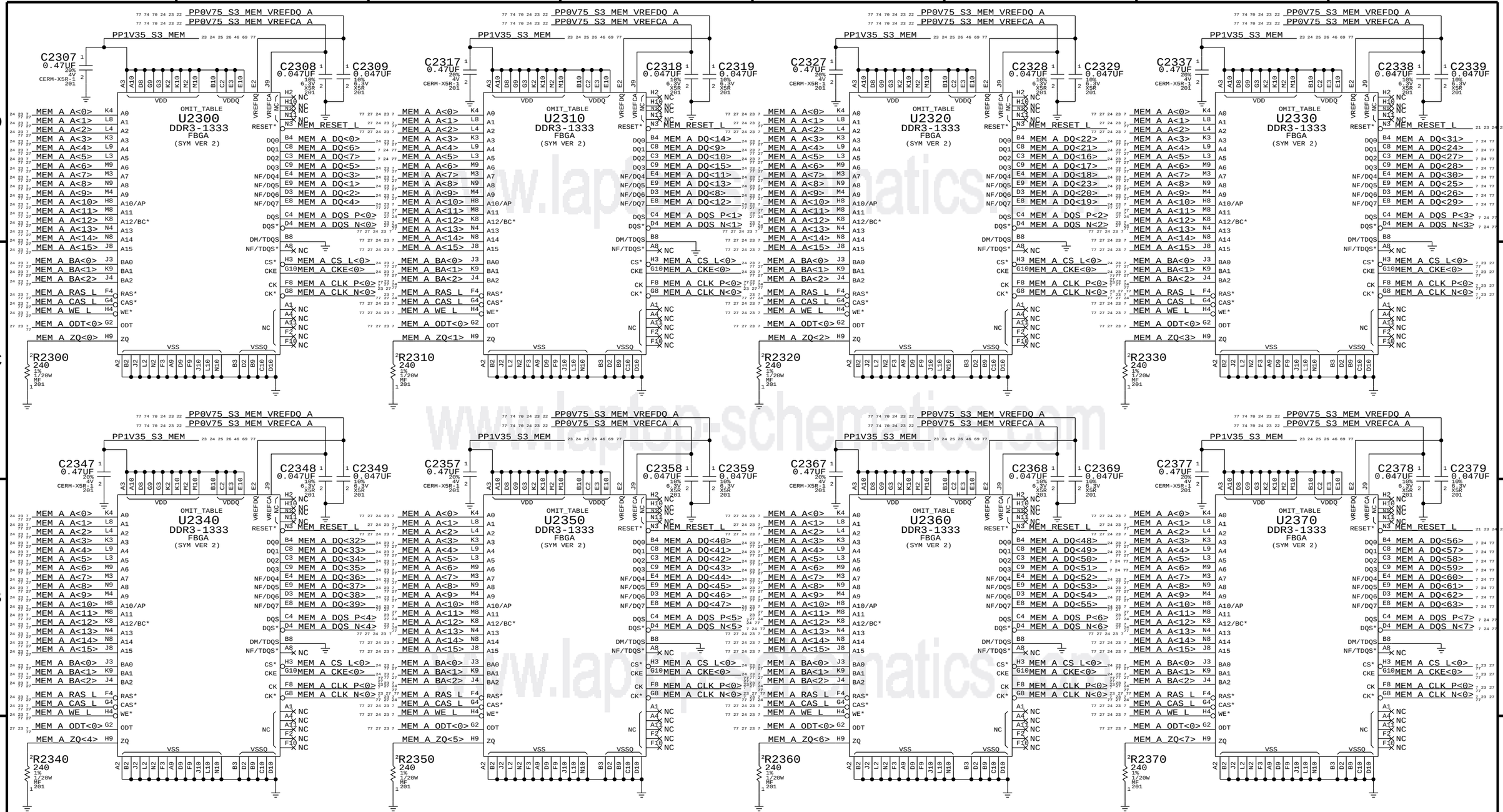
NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 22 OF 118
SHEET: 22 OF 81

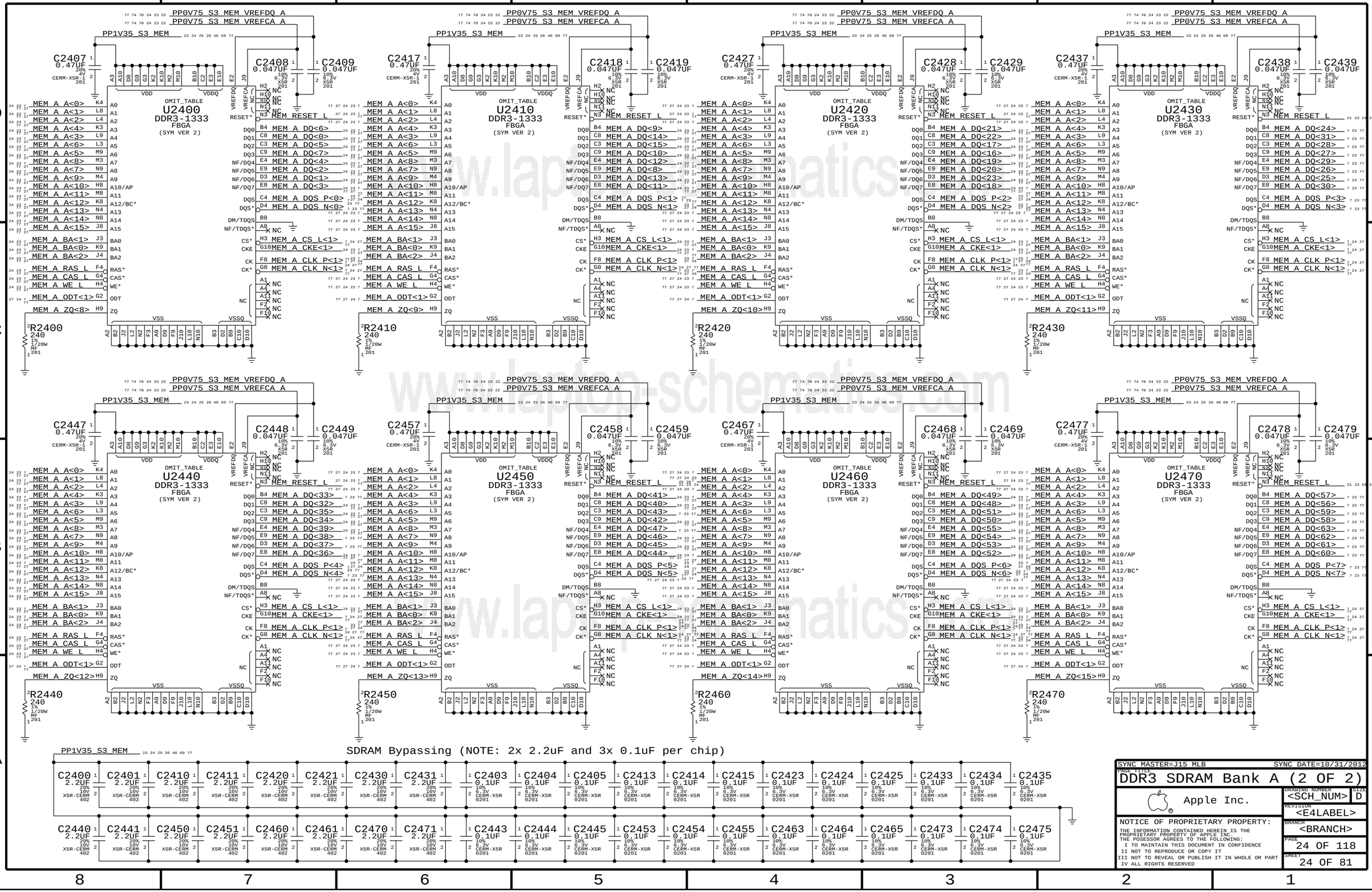


SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
DDR3 SDRAM Bank A (1 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 23 OF 118
SHEET 23 OF 81



PP1V35_S3_MEM

C2507 0.47UF 20% 4V CERM-X5R-1 201
C2508 0.047UF 10% 6.3V X5R 201
C2509 0.047UF 10% 6.3V X5R 201

U2500 DDR3-1333 FBGA (SYM VER 2) — OMIT_TABLE

PP0V75_S3_MEM_VREFDQ_B
PP0V75_S3_MEM_VREFCA_B

MEM_B_A<0>
MEM_B_A<1>
MEM_B_A<2>
MEM_B_A<3>
MEM_B_A<4>
MEM_B_A<5>
MEM_B_A<6>
MEM_B_A<7>
MEM_B_A<8>
MEM_B_A<9>
MEM_B_A<10>
MEM_B_A<11>
MEM_B_A<12>
MEM_B_A<13>
MEM_B_A<14>
MEM_B_A<15>
MEM_B_BA<0>
MEM_B_BA<1>
MEM_B_BA<2>
MEM_B_RAS_L
MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<0>

MEM_RESET_L

MEM_B_DQ<6>
MEM_B_DQ<1>
MEM_B_DQ<3>
MEM_B_DQ<5>
MEM_B_DQ<2>
MEM_B_DQ<4>
MEM_B_DQ<7>
MEM_B_DQ<0>
MEM_B_DQS_P<0>
MEM_B_DQS_N<0>
MEM_B_CS_L<0>
MEM_B_CKE<0>
MEM_B_CLK_P<0>
MEM_B_CLK_N<0>

R2500 240 1% 1/20W MF 201

C2517 0.47UF 20% 4V CERM-X5R-1 201
C2518 0.047UF 10% 6.3V X5R 201
C2519 0.047UF 10% 6.3V X5R 201

U2510 DDR3-1333 FBGA (SYM VER 2) — OMIT_TABLE

MEM_B_A<0>
MEM_B_A<1>
MEM_B_A<2>
MEM_B_A<3>
MEM_B_A<4>
MEM_B_A<5>
MEM_B_A<6>
MEM_B_A<7>
MEM_B_A<8>
MEM_B_A<9>
MEM_B_A<10>
MEM_B_A<11>
MEM_B_A<12>
MEM_B_A<13>
MEM_B_A<14>
MEM_B_A<15>
MEM_B_BA<0>
MEM_B_BA<1>
MEM_B_BA<2>
MEM_B_RAS_L
MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<1>

MEM_RESET_L

MEM_B_DQ<14>
MEM_B_DQ<9>
MEM_B_DQ<11>
MEM_B_DQ<13>
MEM_B_DQ<10>
MEM_B_DQ<12>
MEM_B_DQ<15>
MEM_B_DQ<8>
MEM_B_DQS_P<1>
MEM_B_DQS_N<1>
MEM_B_CS_L<0>
MEM_B_CKE<0>
MEM_B_CLK_P<0>
MEM_B_CLK_N<0>

R2510 240 1% 1/20W MF 201

C2527 0.47UF 20% 4V CERM-X5R-1 201
C2528 0.047UF 10% 6.3V X5R 201
C2529 0.047UF 10% 6.3V X5R 201

U2520 DDR3-1333 FBGA (SYM VER 2) — OMIT_TABLE

MEM_B_A<0>
MEM_B_A<1>
MEM_B_A<2>
MEM_B_A<3>
MEM_B_A<4>
MEM_B_A<5>
MEM_B_A<6>
MEM_B_A<7>
MEM_B_A<8>
MEM_B_A<9>
MEM_B_A<10>
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MEM_B_A<12>
MEM_B_A<13>
MEM_B_A<14>
MEM_B_A<15>
MEM_B_BA<0>
MEM_B_BA<1>
MEM_B_BA<2>
MEM_B_RAS_L
MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<2>

MEM_RESET_L

MEM_B_DQ<18>
MEM_B_DQ<20>
MEM_B_DQ<19>
MEM_B_DQ<16>
MEM_B_DQ<23>
MEM_B_DQ<21>
MEM_B_DQ<22>
MEM_B_DQ<17>
MEM_B_DQS_P<2>
MEM_B_DQS_N<2>
MEM_B_CS_L<0>
MEM_B_CKE<0>
MEM_B_CLK_P<0>
MEM_B_CLK_N<0>

R2520 240 1% 1/20W MF 201

C2537 0.47UF 20% 4V CERM-X5R-1 201
C2538 0.047UF 10% 6.3V X5R 201
C2539 0.047UF 10% 6.3V X5R 201

U2530 DDR3-1333 FBGA (SYM VER 2) — OMIT_TABLE

MEM_B_A<0>
MEM_B_A<1>
MEM_B_A<2>
MEM_B_A<3>
MEM_B_A<4>
MEM_B_A<5>
MEM_B_A<6>
MEM_B_A<7>
MEM_B_A<8>
MEM_B_A<9>
MEM_B_A<10>
MEM_B_A<11>
MEM_B_A<12>
MEM_B_A<13>
MEM_B_A<14>
MEM_B_A<15>
MEM_B_BA<0>
MEM_B_BA<1>
MEM_B_BA<2>
MEM_B_RAS_L
MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<3>

MEM_RESET_L

MEM_B_DQ<27>
MEM_B_DQ<25>
MEM_B_DQ<26>
MEM_B_DQ<29>
MEM_B_DQ<30>
MEM_B_DQ<28>
MEM_B_DQ<31>
MEM_B_DQ<24>
MEM_B_DQS_P<3>
MEM_B_DQS_N<3>
MEM_B_CS_L<0>
MEM_B_CKE<0>
MEM_B_CLK_P<0>
MEM_B_CLK_N<0>

R2530 240 1% 1/20W MF 201

PP1V35_S3_MEM

C2547 0.47UF 20% 4V CERM-X5R-1 201
C2548 0.047UF 10% 6.3V X5R 201
C2549 0.047UF 10% 6.3V X5R 201

U2540 DDR3-1333 FBGA (SYM VER 2) — OMIT_TABLE

PP0V75_S3_MEM_VREFDQ_B
PP0V75_S3_MEM_VREFCA_B

MEM_B_A<0>
MEM_B_A<1>
MEM_B_A<2>
MEM_B_A<3>
MEM_B_A<4>
MEM_B_A<5>
MEM_B_A<6>
MEM_B_A<7>
MEM_B_A<8>
MEM_B_A<9>
MEM_B_A<10>
MEM_B_A<11>
MEM_B_A<12>
MEM_B_A<13>
MEM_B_A<14>
MEM_B_A<15>
MEM_B_BA<0>
MEM_B_BA<1>
MEM_B_BA<2>
MEM_B_RAS_L
MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<4>

MEM_RESET_L

MEM_B_DQ<32>
MEM_B_DQ<33>
MEM_B_DQ<34>
MEM_B_DQ<35>
MEM_B_DQ<36>
MEM_B_DQ<37>
MEM_B_DQ<38>
MEM_B_DQ<39>
MEM_B_DQS_P<4>
MEM_B_DQS_N<4>
MEM_B_CS_L<0>
MEM_B_CKE<0>
MEM_B_CLK_P<0>
MEM_B_CLK_N<0>

R2540 240 1% 1/20W MF 201

C2557 0.47UF 20% 4V CERM-X5R-1 201
C2558 0.047UF 10% 6.3V X5R 201
C2559 0.047UF 10% 6.3V X5R 201

U2550 DDR3-1333 FBGA (SYM VER 2) — OMIT_TABLE

MEM_B_A<0>
MEM_B_A<1>
MEM_B_A<2>
MEM_B_A<3>
MEM_B_A<4>
MEM_B_A<5>
MEM_B_A<6>
MEM_B_A<7>
MEM_B_A<8>
MEM_B_A<9>
MEM_B_A<10>
MEM_B_A<11>
MEM_B_A<12>
MEM_B_A<13>
MEM_B_A<14>
MEM_B_A<15>
MEM_B_BA<0>
MEM_B_BA<1>
MEM_B_BA<2>
MEM_B_RAS_L
MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<5>

MEM_RESET_L

MEM_B_DQ<40>
MEM_B_DQ<41>
MEM_B_DQ<42>
MEM_B_DQ<43>
MEM_B_DQ<44>
MEM_B_DQ<45>
MEM_B_DQ<46>
MEM_B_DQ<47>
MEM_B_DQS_P<5>
MEM_B_DQS_N<5>
MEM_B_CS_L<0>
MEM_B_CKE<0>
MEM_B_CLK_P<0>
MEM_B_CLK_N<0>

R2550 240 1% 1/20W MF 201

C2567 0.47UF 20% 4V CERM-X5R-1 201
C2568 0.047UF 10% 6.3V X5R 201
C2569 0.047UF 10% 6.3V X5R 201

U2560 DDR3-1333 FBGA (SYM VER 2) — OMIT_TABLE

MEM_B_A<0>
MEM_B_A<1>
MEM_B_A<2>
MEM_B_A<3>
MEM_B_A<4>
MEM_B_A<5>
MEM_B_A<6>
MEM_B_A<7>
MEM_B_A<8>
MEM_B_A<9>
MEM_B_A<10>
MEM_B_A<11>
MEM_B_A<12>
MEM_B_A<13>
MEM_B_A<14>
MEM_B_A<15>
MEM_B_BA<0>
MEM_B_BA<1>
MEM_B_BA<2>
MEM_B_RAS_L
MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<6>

MEM_RESET_L

MEM_B_DQ<48>
MEM_B_DQ<49>
MEM_B_DQ<50>
MEM_B_DQ<51>
MEM_B_DQ<52>
MEM_B_DQ<53>
MEM_B_DQ<54>
MEM_B_DQ<55>
MEM_B_DQS_P<6>
MEM_B_DQS_N<6>
MEM_B_CS_L<0>
MEM_B_CKE<0>
MEM_B_CLK_P<0>
MEM_B_CLK_N<0>

R2560 240 1% 1/20W MF 201

C2577 0.47UF 20% 4V CERM-X5R-1 201
C2578 0.047UF 10% 6.3V X5R 201
C2579 0.047UF 10% 6.3V X5R 201

U2570 DDR3-1333 FBGA (SYM VER 2) — OMIT_TABLE

MEM_B_A<0>
MEM_B_A<1>
MEM_B_A<2>
MEM_B_A<3>
MEM_B_A<4>
MEM_B_A<5>
MEM_B_A<6>
MEM_B_A<7>
MEM_B_A<8>
MEM_B_A<9>
MEM_B_A<10>
MEM_B_A<11>
MEM_B_A<12>
MEM_B_A<13>
MEM_B_A<14>
MEM_B_A<15>
MEM_B_BA<0>
MEM_B_BA<1>
MEM_B_BA<2>
MEM_B_RAS_L
MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<7>

MEM_RESET_L

MEM_B_DQ<56>
MEM_B_DQ<57>
MEM_B_DQ<58>
MEM_B_DQ<59>
MEM_B_DQ<60>
MEM_B_DQ<61>
MEM_B_DQ<62>
MEM_B_DQ<63>
MEM_B_DQS_P<7>
MEM_B_DQS_N<7>
MEM_B_CS_L<0>
MEM_B_CKE<0>
MEM_B_CLK_P<0>
MEM_B_CLK_N<0>

R2570 240 1% 1/20W MF 201

SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)

PP1V35_S3_MEM

C2500 C2501 C2510 C2511 C2520 C2521 C2530 C2531 2.2UF 20% 10V X5R-CERM 402
C2503 C2504 C2505 C2513 C2514 C2515 C2523 C2524 C2525 C2533 C2534 C2535 0.1UF 10% 6.3V CERM-X5R 0201
C2540 C2541 C2550 C2551 C2560 C2561 C2570 C2571 2.2UF 20% 10V X5R-CERM 402
C2543 C2544 C2545 C2553 C2554 C2555 C2563 C2564 C2565 C2573 C2574 C2575 0.1UF 10% 6.3V CERM-X5R 0201

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SYNC_DATE=10/31/2012

PAGE_TITLE: DDR3 SDRAM Bank B (1 OF 2)

Apple Inc.

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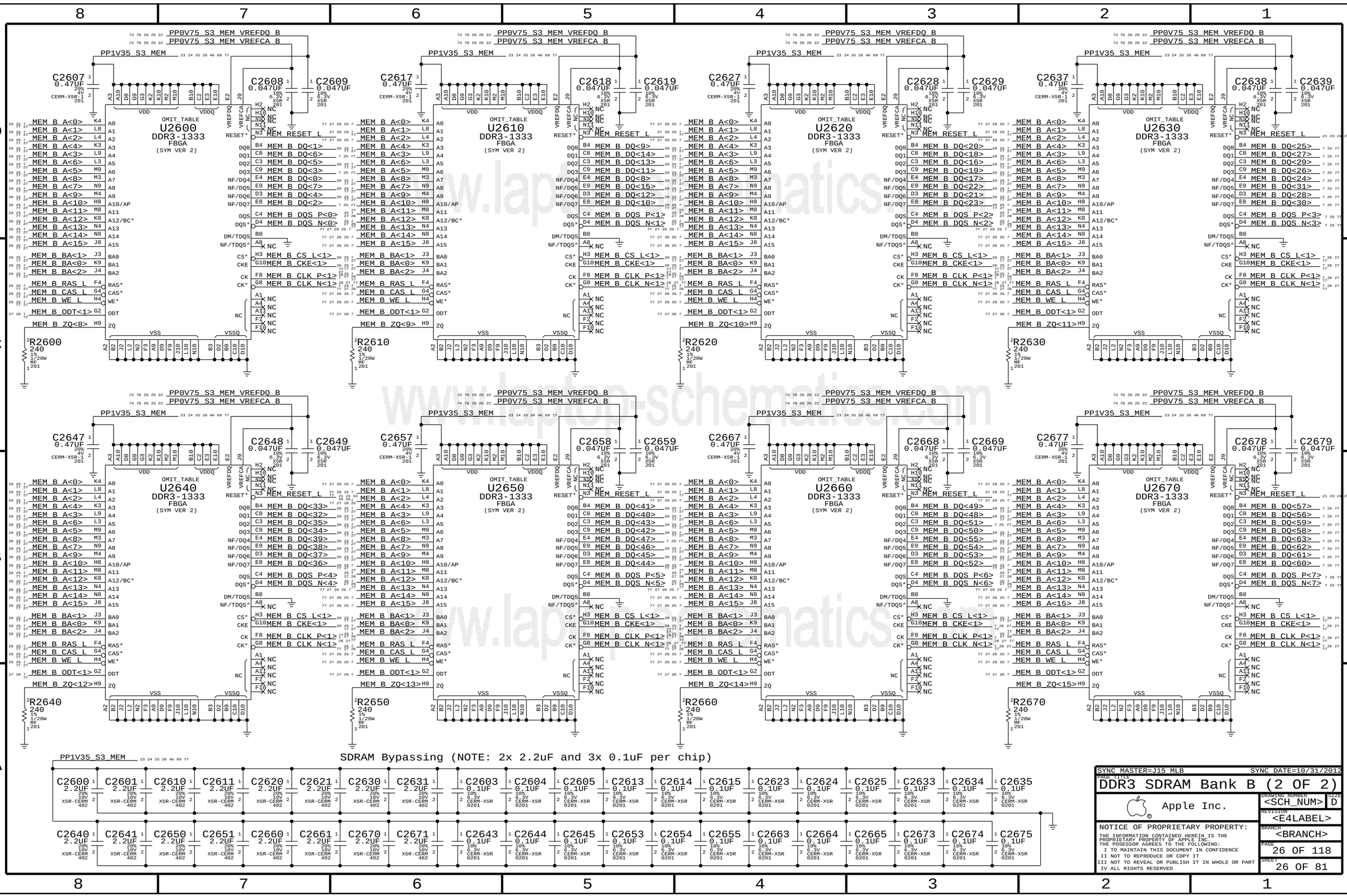
PAGE: 25 OF 118
SHEET: 25 OF 81


PP0V75_S3_MEM_VREFDQ_B
PP0V75_S3_MEM_VREFCA_B
PP1V35_S3_MEM
C2607 0.47UF
C2608 0.047UF
C2609 0.047UF
U2600
DDR3-1333
FBGA
(SYM VER 2)
OMIT_TABLE
R2600 240
C2617 0.47UF
C2618 0.047UF
C2619 0.047UF
U2610
DDR3-1333
FBGA
(SYM VER 2)
OMIT_TABLE
R2610 240
C2627 0.47UF
C2628 0.047UF
C2629 0.047UF
U2620
DDR3-1333
FBGA
(SYM VER 2)
OMIT_TABLE
R2620 240
C2637 0.47UF
C2638 0.047UF
C2639 0.047UF
U2630
DDR3-1333
FBGA
(SYM VER 2)
OMIT_TABLE
R2630 240
C2647 0.47UF
C2648 0.047UF
C2649 0.047UF
U2640
DDR3-1333
FBGA
(SYM VER 2)
OMIT_TABLE
R2640 240
C2657 0.47UF
C2658 0.047UF
C2659 0.047UF
U2650
DDR3-1333
FBGA
(SYM VER 2)
OMIT_TABLE
R2650 240
C2667 0.47UF
C2668 0.047UF
C2669 0.047UF
U2660
DDR3-1333
FBGA
(SYM VER 2)
OMIT_TABLE
R2660 240
C2677 0.47UF
C2678 0.047UF
C2679 0.047UF
U2670
DDR3-1333
FBGA
(SYM VER 2)
OMIT_TABLE
R2670 240
MEM_B_RESET_L
MEM_B_ZQ
MEM_B_BA
MEM_B_RAS_L
MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT
MEM_B_CS_L
MEM_B_CKE
MEM_B_CLK_P
MEM_B_CLK_N
SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)
C2600 2.2UF
C2603 0.1UF
C2604 0.1UF
C2605 0.1UF
C2613 0.1UF
C2614 0.1UF
C2615 0.1UF
C2623 0.1UF
C2624 0.1UF
C2625 0.1UF
C2633 0.1UF
C2634 0.1UF
C2635 0.1UF
C2640 2.2UF
C2643 0.1UF
C2644 0.1UF
C2645 0.1UF
C2653 0.1UF
C2654 0.1UF
C2655 0.1UF
C2663 0.1UF
C2664 0.1UF
C2665 0.1UF
C2673 0.1UF
C2674 0.1UF
C2675 0.1UF
SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012
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DDR3 SDRAM Bank B (2 OF 2)
Apple Inc.
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PAGE
26 OF 118
SHEET
26 OF 81
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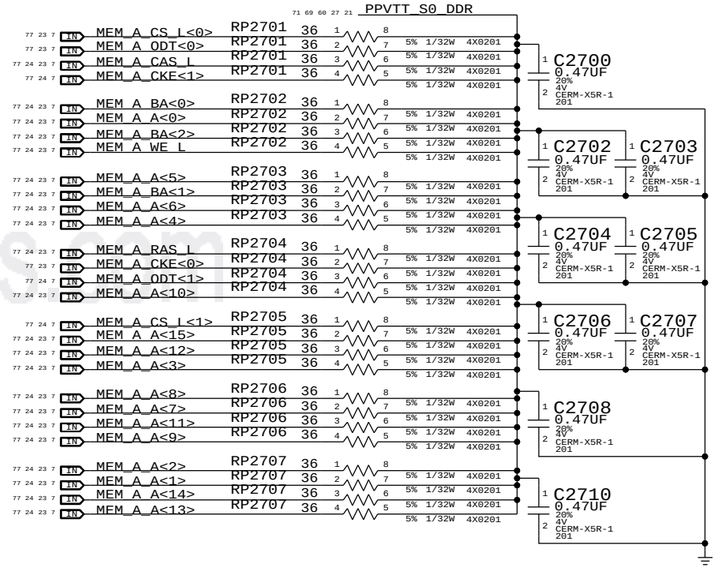
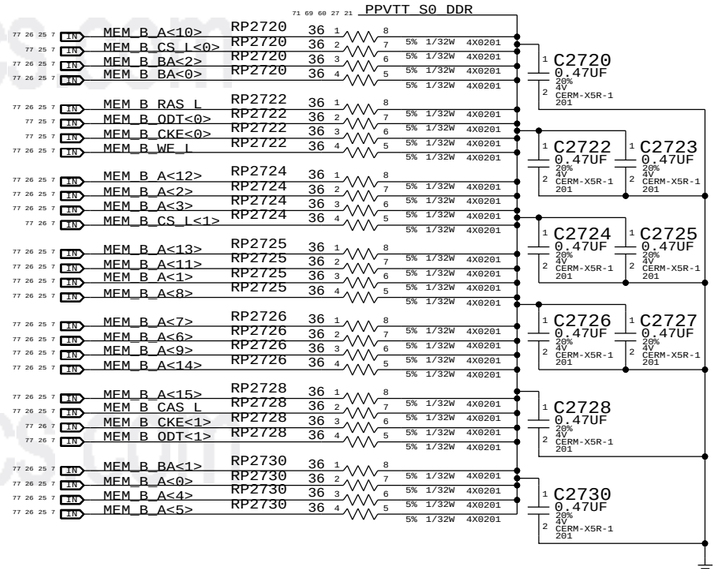
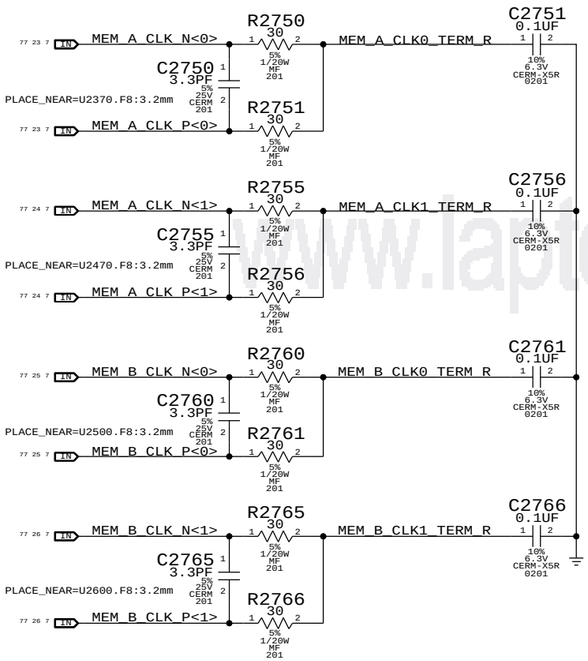
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



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PAGE TITLE: DDR3 Termination

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DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 27 OF 118
SHEET: 27 OF 81

CRITICAL
OMIT_TABLE

U2800
REDWOOD-RIDGE
FCBGA
(1 OF 2)

PCIE GEN2

PCIE_TBT_R2D_C_P<0>	C2800 0.1UF	PCIE_TBT_R2D_P<0>	AB9	PERP_0	
PCIE_TBT_R2D_C_N<0>	C2801 0.1UF	PCIE_TBT_R2D_N<0>	AA10	PERN_0	
PCIE_TBT_R2D_C_P<1>	C2802 0.1UF	PCIE_TBT_R2D_P<1>	AA12	PERP_1	
PCIE_TBT_R2D_C_N<1>	C2803 0.1UF	PCIE_TBT_R2D_N<1>	AB13	PERN_1	
PCIE_TBT_R2D_C_P<2>	C2804 0.1UF	PCIE_TBT_R2D_P<2>	AB15	PERP_2	
PCIE_TBT_R2D_C_N<2>	C2805 0.1UF	PCIE_TBT_R2D_N<2>	AA16	PERN_2	
PCIE_TBT_R2D_C_P<3>	C2806 0.1UF	PCIE_TBT_R2D_P<3>	AA18	PERP_3	
PCIE_TBT_R2D_C_N<3>	C2807 0.1UF	PCIE_TBT_R2D_N<3>	AB19	PERN_3	
		TBT_PCIE_RESET_L	P5	PERST_OD_N	
		TBT_PWR_ON_POC_RST_L	R4	PWR_ON_POC_RSTN	

PETP_0	AD5	PCIE_TBT_D2R_C_P<0>	C2840 0.1UF → PCIE_TBT_D2R_P<0>
PETN_0	AD7	PCIE_TBT_D2R_C_N<0>	C2841 0.1UF → PCIE_TBT_D2R_N<0>
PETP_1	AD9	PCIE_TBT_D2R_C_P<1>	C2842 0.1UF → PCIE_TBT_D2R_P<1>
PETN_1	AD11	PCIE_TBT_D2R_C_N<1>	C2843 0.1UF → PCIE_TBT_D2R_N<1>
PETP_2	AD13	PCIE_TBT_D2R_C_P<2>	C2844 0.1UF → PCIE_TBT_D2R_P<2>
PETN_2	AD15	PCIE_TBT_D2R_C_N<2>	C2845 0.1UF → PCIE_TBT_D2R_N<2>
PETP_3	AD17	PCIE_TBT_D2R_C_P<3>	C2846 0.1UF → PCIE_TBT_D2R_P<3>
PETN_3	AD19	PCIE_TBT_D2R_C_N<3>	C2847 0.1UF → PCIE_TBT_D2R_N<3>

MISC

		TBT_RSENSE	U20	RSENSE
		TBT_RBIAS	W20	RBIAS
			AD1	RSVD
			L8	RSVD

R2855 1K 1% 1/20W MF 201

Used for straps in host mode

PCIE_RST_0_N	W6	TP_TBT_PCIE_RESET0_L	
PCIE_RST_1_N	AB3	TBT_DFT_STRAP_1	
PCIE_RST_2_N	AD3	TBT_ROM_SECURITY_XOR	
PCIE_RST_3_N	V1	TBT_DFT_STRAP_3	
PCIE_CLKREQ_OD_N	V3	TBT_CLKREQ_L	OUT 11
REFCLK_100_IN_P	AB21	PCIE_CLK100M_TBT_P	IN 11 76
REFCLK_100_IN_N	AD21	PCIE_CLK100M_TBT_N	IN 11 76
XTAL_25_IN	AA24 75	SYSCLK_CLK25M_TBT_R	
XTAL_25_OUT	AB23	NC_TBT_XTAL25OUT	72
TMU_CLK_OUT	AA4	TBT_TMU_CLK_OUT	

Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.

If strap != bit then security is enabled?

PP3V3_TBTLC → NO STUFF R2867 10K 5% 1/20W MF 201

R2861 10K, R2862 10K, R2863 10K — 5% 1/20W MF 201

Divides 3.3V to 1.8V

R2895 806 1% 1/20W MF 201 — SYSCLK_CLK25M_TBT (IN 19 75)

NO STUFF R2899 10K 5% 1/20W MF 201

R2896 1K 5% 1/20W MF 201

PP3V3_TBTLC (69 29 28 20 19), PP3V3_S4_TBT (69 46 30 29 28)

R2881 100K, R2880 100K, R2882 100K — 5% 1/20W MF 201

		TBT_EN_CIO_PWR_L	29 28
		TBT_DDC_XBAR_EN_L	33 28
		HDMITBTMUX_SEL_TBT	70 28
		TBTDP_AUXIO_EN	32 31 28
		DP_TBTSRC_HPD	28

PP3V3_TBTLC (19 20 28 29 69)

R2878 100K, R2879 100K — 5% 1/20W MF 201

R2832 100K, R2883 100K — 5% 1/20W MF 201

PP3V3_S4_TBT (69 46 30 29 28)

NO STUFF R2884 100K 5% 1/20W MF 201

NO STUFF R2885 10K 5% 1/20W MF 201

R2886 10K 5% 1/20W MF 201

		TBT_BATLOW_L	30 28
		TBT_A_DP_PWRDN	31 28
		TBT_B_DP_PWRDN	32 28
		TBT_A_HV_EN	31 30 28
		TBT_B_HV_EN	33 32 28

R2888 10K, R2887 10K — 5% 1/20W MF 201

R2890 3.3K 5% 1/20W MF 201

R2891 3.3K 5% 1/20W MF 201

C2890 1UF 10% 6.3V CERM 402

BYPASS=U2890:2mm

CRITICAL
OMIT_TABLE

U2890 4MBIT W25X40CLXIG USON

VCC

(TBT_SPI_MOSI)	5	DI/IO0	
(TBT_SPI_CLK)	6	CLK	
(TBT_SPI_CS_L)	1	CS*	
TBTROM_WP_L	3	WP*	
TBTROM_HOLD_L	7	HOLD*	
(TBT_SPI_MISO)	2	DO/IO1	
	4	GND	
	9	THRM_PAD	

R2892 3.3K 5% 1/20W MF 201

R2893 3.3K 5% 1/20W MF 201

R2829 10K 5% 1/20W MF 201

R2825 100 5% 1/20W MF 201

OMIT
R2815 NOSTUFF NONE NONE NONE 0201

DEBUG: For monitoring current/voltage
TBT_MONOBSP W18 MONOBSP
TBT_MONOBSN W16 MONOBSN

DEBUG: For monitoring clock
TBT_THERMD_P AB7 THERMDA
Use AA8 GND ball for THERM_DN

		TP_TBT_MONDC0	AD23 MONDC0
		TP_TBT_MONDC1	AC24 MONDC1
		TBT_SPI_MOSI	AA2 EE_DI
		TBT_SPI_MISO	Y3 EE_DO
		TBT_SPI_CS_L	T5 EE_CS_N
		TBT_SPI_CLK	U8 EE_CLK
		JTAG_TBT_TDI	W2 TDI
		JTAG_TBT_TMS	AB1 TMS
		JTAG_TBT_TCK	AA6 TCK
		JTAG_TBT_TDO	U6 TDO
		TBT_TEST_EN	R6 TEST_EN
		TBT_TEST_PWR_GOOD	W8 TEST_PWR_GOOD

PORTS

DP_TBTSNK0_ML_P<3>	E14	DPSNK0_3_P	DPSRC_3_P	A14 NC_DP_TBTSRC_ML_CP<3>
DP_TBTSNK0_ML_N<3>	D13	DPSNK0_3_N	DPSRC_3_N	B15 NC_DP_TBTSRC_ML_CN<3>
DP_TBTSNK0_ML_P<2>	E16	DPSNK0_2_P	DPSRC_2_P	A12 NC_DP_TBTSRC_ML_CP<2>
DP_TBTSNK0_ML_N<2>	D15	DPSNK0_2_N	DPSRC_2_N	B13 NC_DP_TBTSRC_ML_CN<2>
DP_TBTSNK0_ML_P<1>	E18	DPSNK0_1_P	DPSRC_1_P	A10 NC_DP_TBTSRC_ML_CP<1>
DP_TBTSNK0_ML_N<1>	D17	DPSNK0_1_N	DPSRC_1_N	B11 NC_DP_TBTSRC_ML_CN<1>
DP_TBTSNK0_ML_P<0>	E20	DPSNK0_0_P	DPSRC_0_P	A8 NC_DP_TBTSRC_ML_CP<0>
DP_TBTSNK0_ML_N<0>	D19	DPSNK0_0_N	DPSRC_0_N	B9 NC_DP_TBTSRC_ML_CN<0>
DP_TBTSNK0_AUXCH_P	G4	DPSNK0_AUX_P	DPSRC_AUX_P	J4 NC_DP_TBTSRC_AUXCH_CP
DP_TBTSNK0_AUXCH_N	G2	DPSNK0_AUX_N	DPSRC_AUX_N	J2 NC_DP_TBTSRC_AUXCH_CN
DP_TBTSNK0_HPD	AB5	DPSNK0_HPD	DPSRC_HPD_OD	AC2 DP_TBTSRC_HPD
DP_TBTSNK1_ML_P<3>	E6	DPSNK1_3_P		
DP_TBTSNK1_ML_N<3>	D5	DPSNK1_3_N		
DP_TBTSNK1_ML_P<2>	E8	DPSNK1_2_P		
DP_TBTSNK1_ML_N<2>	D7	DPSNK1_2_N		
DP_TBTSNK1_ML_P<1>	E10	DPSNK1_1_P		
DP_TBTSNK1_ML_N<1>	D9	DPSNK1_1_N		
DP_TBTSNK1_ML_P<0>	E12	DPSNK1_0_P		
DP_TBTSNK1_ML_N<0>	D11	DPSNK1_0_N		
DP_TBTSNK1_AUXCH_P	H3	DPSNK1_AUX_P		
DP_TBTSNK1_AUXCH_N	H1	DPSNK1_AUX_N		
DP_TBTSNK1_HPD	U4	DPSNK1_HPD		

R2830 100K 5% 1/20W MF 201

R2831 100K 5% 1/20W MF 201

		TBT_A_R2D_C_P<0>	G24	PA_CIO0_TX_P/DPSRC_0_P
		TBT_A_R2D_C_N<0>	E24	PA_CIO0_TX_N/DPSRC_0_N
		TBT_A_D2R_P<0>	G22	PA_CIO0_RX_P
		TBT_A_D2R_N<0>	E22	PA_CIO0_RX_N
		TBT_A_CONFIG1_BUF	P1	PA_CONFIG1/CIO_0_LSEO
		TBT_A_CONFIG2_RC	K5	PA_CONFIG2/CIO_0_LSOE
		TBT_A_R2D_C_P<1>	L24	PA_CIO1_TX_P/DPSRC_2_P
		TBT_A_R2D_C_N<1>	J24	PA_CIO1_TX_N/DPSRC_2_N
		TBT_A_D2R_P<1>	L22	PA_CIO1_RX_P
		TBT_A_D2R_N<1>	J22	PA_CIO1_RX_N
		TBT_A_LSTX	N8	PA_LSTX/CIO_1_LSEO
		TBT_A_LSRX	J6	PA_LSRX/CIO_1_LSOE
		TBT_A_HPD	M3	PA_DPSRC_HPD
		TBT_A_HV_EN	R8	GPIO_0/PA_HV_EN/BYP0
		TBT_A_CIO_SEL	N2	GPIO_10/PA_CIO_SEL/BYP1
		TBT_A_DP_PWRDN	P3	GPIO_12/PA_DP_PWRDN/BYP2
		TBT_A_AUXCH_C_P	L4	PA_AUX_P
		TBT_A_AUXCH_C_N	L2	PA_AUX_N

GPIO_2/TMU_CLK_IN/AC_PRESENT	U2	TBT_GPIO2		
GPIO_3/FORCE_PWR	L6	TBT_PWR_EN	IN	20
GPIO_4/WAKE_OD_N	H5	SMC_PME_S4_DARK_L	OUT	20 41 42 43
GPIO_5/CIO_PLUG_EVENT_N/HV_OK_OD	Y7	TBT_CIO_PLUG_EVENT_L	OUT	14 20
GPIO_6_OD/CIO_SDA_OD	Y1	HDMITBTMUX_SEL_TBT	IN	28 70
GPIO_7_OD/CIO_SCL_OD	T7	TBT_GPIO7		
GPIO_8/EN_CIO_PWR_OD*	V7	TBT_EN_CIO_PWR_L	OUT	28 29
GPIO_9/SX_CTRL_OD*	M7	TBT_BATLOW_L	IN	28 30
GPIO_14	T1	TBTDP_AUXIO_EN	OUT	28 31 32
GPIO_15	T3	TBT_DDC_XBAR_EN_L	OUT	28 33
PB_CIO2_TX_P/DPSRC_0_P	R24	TBT_B_R2D_C_P<0>	OUT	32 78
PB_CIO2_TX_N/DPSRC_0_N	N24	TBT_B_R2D_C_N<0>	OUT	32 78
PB_CIO2_RX_P	R22	TBT_B_D2R_P<0>	IN	32 78
PB_CIO2_RX_N	N22	TBT_B_D2R_N<0>	IN	32 78
PB_CONFIG1/CIO_2_LSEO	D3	TBT_B_CONFIG1_BUF	OUT	32
PB_CONFIG2/CIO_2_LSOE	M1	TBT_B_CONFIG2_RC	IN	32
PB_CIO3_TX_P/DPSRC_2_P	W24	TBT_B_R2D_C_P<1>	OUT	32 78
PB_CIO3_TX_N/DPSRC_2_N	U24	TBT_B_R2D_C_N<1>	OUT	32 78
PB_CIO3_RX_P	W22	TBT_B_D2R_P<1>	IN	32 78
PB_CIO3_RX_N	U22	TBT_B_D2R_N<1>	IN	32 78
PB_LSTX/CIO_3_LSEO	M5	TBT_B_LSTX	OUT	32
PB_LSRX/CIO_3_LSOE	P7	TBT_B_LSRX	IN	32
PB_DPSRC_1_P	A20	DP_TBTPB_ML_C_P<1>	OUT	32 78
PB_DPSRC_1_N	B21	DP_TBTPB_ML_C_N<1>	OUT	32 78
PB_DPSRC_3_P	A22	DP_TBTPB_ML_C_P<3>	OUT	32 78
PB_DPSRC_3_N	B23	DP_TBTPB_ML_C_N<3>	OUT	32 78
PB_AUX_P	K3	DP_TBTPB_AUXCH_C_P	B1	32 78
PB_AUX_N	K1	DP_TBTPB_AUXCH_C_N	B1	32 78
PB_DPSRC_HPD	N6	DP_TBTPB_HPD	IN	32
GPIO_1/PB_HV_EN/BYP0	F1	TBT_B_HV_EN	OUT	28 32 33
GPIO_11/PB_CIO_SEL/BYP1	R2	TBT_B_CIO_SEL	OUT	32
GPIO_13/PB_DP_PWRDN/BYP2	F3	TBT_B_DP_PWRDN	OUT	28 32

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C2820 0.1UF	DP_TBTSNK0_ML_P<0>	28 74
DP_TBTSNK0_ML_C_N<0>	C2821 0.1UF	DP_TBTSNK0_ML_N<0>	28 74
DP_TBTSNK0_ML_C_P<1>	C2822 0.1UF	DP_TBTSNK0_ML_P<1>	28 74
DP_TBTSNK0_ML_C_N<1>	C2823 0.1UF	DP_TBTSNK0_ML_N<1>	28 74
DP_TBTSNK0_ML_C_P<2>	C2824 0.1UF	DP_TBTSNK0_ML_P<2>	28 74
DP_TBTSNK0_ML_C_N<2>	C2825 0.1UF	DP_TBTSNK0_ML_N<2>	28 74
DP_TBTSNK0_ML_C_P<3>	C2826 0.1UF	DP_TBTSNK0_ML_P<3>	28 74
DP_TBTSNK0_ML_C_N<3>	C2827 0.1UF	DP_TBTSNK0_ML_N<3>	28 74
DP_TBTSNK0_AUXCH_C_P	C2828 0.1UF	DP_TBTSNK0_AUXCH_P	28 74
DP_TBTSNK0_AUXCH_C_N	C2829 0.1UF	DP_TBTSNK0_AUXCH_N	28 74

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C2830 0.1UF	DP_TBTSNK1_ML_P<0>	28 74
DP_TBTSNK1_ML_C_N<0>	C2831 0.1UF	DP_TBTSNK1_ML_N<0>	28 74
DP_TBTSNK1_ML_C_P<1>	C2832 0.1UF	DP_TBTSNK1_ML_P<1>	28 74
DP_TBTSNK1_ML_C_N<1>	C2833 0.1UF	DP_TBTSNK1_ML_N<1>	28 74
DP_TBTSNK1_ML_C_P<2>	C2834 0.1UF	DP_TBTSNK1_ML_P<2>	28 74
DP_TBTSNK1_ML_C_N<2>	C2835 0.1UF	DP_TBTSNK1_ML_N<2>	28 74
DP_TBTSNK1_ML_C_P<3>	C2836 0.1UF	DP_TBTSNK1_ML_P<3>	28 74
DP_TBTSNK1_ML_C_N<3>	C2837 0.1UF	DP_TBTSNK1_ML_N<3>	28 74
DP_TBTSNK1_AUXCH_C_P	C2838 0.1UF	DP_TBTSNK1_AUXCH_P	28 74
DP_TBTSNK1_AUXCH_C_N	C2839 0.1UF	DP_TBTSNK1_AUXCH_N	28 74

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

SYNC_MASTER=T29_RR SYNC_DATE=01/14/2013

PAGE TITLE: Thunderbolt Host (1 of 2)

Apple Inc.

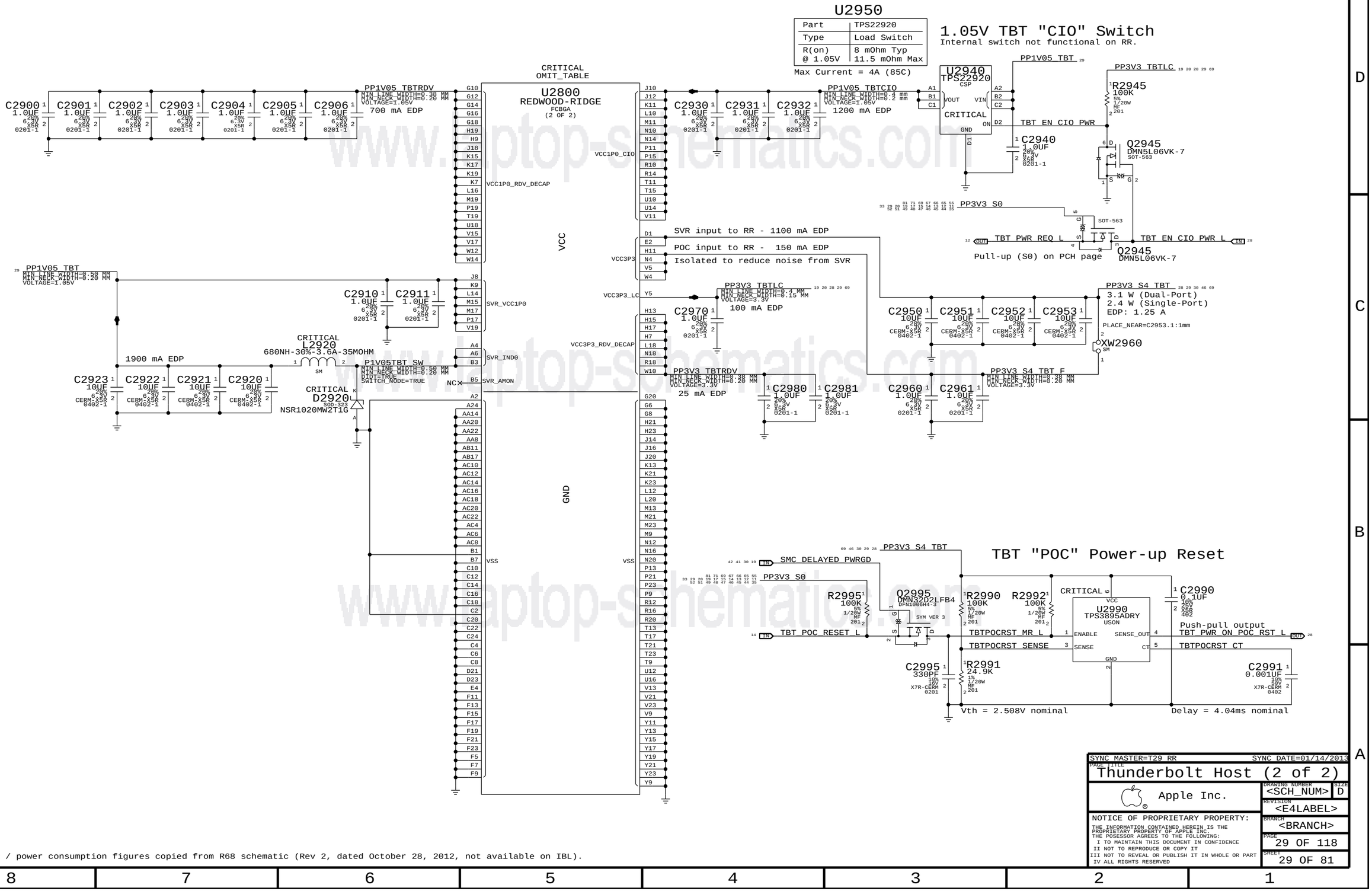
DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 28 OF 118

SHEET: 28 OF 81



Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator

PPBUS_G3H
8-13V Input
Changes required
for 2S.

R3080 470K 5% 1/16W MF-LF 402
C3080 0.1UF 10% 25V X5R 402
TBTBST_PWREN_DIV_L
R3081 330K 5% 1/16W MF-LF 402
TBTBST_PWREN_L

Q3005 DMN32D2LFB4 DFN1006H4-3 SYM VER 2
TBT_A_HV_EN
Second FET needed for dual-port designs.

CRITICAL
Q3080 SI8409DB BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here,
add property on another page.

R3091 200K 1% 1/10W MF-LF 402 <R1>
R3092 73.2K 1% 1/10W MF-LF 402 <R2>

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603

CRITICAL
L3095 3.3UH-6.5A PIMB063T-SM
TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
U3090 LT3957 QFN

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
TBTBST_SNS1
TBTBST_SNS2
TBTBST_VSNS
TBTBST_FBX

C3085 2.2UF 20% 10V X5R-CERM 402
C3086 2.2UF 20% 10V X5R-CERM 402
C3087 68PF 5% 50V C0G-CERM 0402
R3093 49.9K 1% 1/10W MF-LF 402
C3092 2.2UF 20% 10V X5R-CERM 402
C3093 0.0033UF 10% 50V X7R-CERM 0402
R3094 26.7K 1% 1/10W MF-LF 402
C3094 0.33UF 10% 6.3V CERM-X5R 402

GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

SGND shorted to
GND inside package,
no XW necessary.

R3089 0 5% 1/20W MF 0201
CRITICAL
D3095 PDS540XF PWRDI5
XW3095 SM
PLACE_NEAR=C3095.1:2 mm

C3088 10PF 5% 50V C0G-CERM 0402
R3095 137K 1% 1/10W MF-LF 402 <Ra>
NO STUFF
C3089 100PF 5% 50V CERM 402
R3096 15.8K 1% 1/10W MF-LF 402 <Rb>

Vout = 1.6V * (1 + Ra / Rb)

PP15V_TBT
Vout = 15.47V
Max Current = 2A?
Freq = 480KHz

C3095 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L
C3096 10UF 10% 25V X5R 1206-2
NO STUFF
C3097 10UF 10% 25V X5R 805
C3099 0.001UF 10% 50V X7R-CERM 0402

Q3088 DMN5L06VK-7 SOT-563
Max Vgs: 10V
R3088 330K 5% 1/10W MF-LF 402
TBTBST_SHDN_DIV
R3087 330K 5% 1/10W MF-LF 402
Q3088 DMN5L06VK-7 SOT-563
SMC_DELAYED_PWRGD

BATLOW# Isolation

Q3000 DMN32D2LFB4 DFN1006H4-3 SYM VER 3
PP3V3_S4_TBT
Pull-up on RR page
PM_BATLOW_L
TBT_BATLOW_L
TBT_BATLOW_L
MAKE_BASE=TRUE

SYNC_MASTER=T29_RR SYNC_DATE=01/14/2013

PAGE TITLE: Thunderbolt Mobile Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 30 OF 118
SHEET: 30 OF 81

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
PP15V_TBT 15.75V Max
CRITICAL C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3280 22UF 20% 6.3V X5R-CERM 603
C3281 0.1UF 10% 16V X5R-CERM 0201
C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 16V X5R 402
CRITICAL U3210 CD3211A0RGPR QFN
V3P3 V3P3OUT VHV OUT ENHVU FAULTZ EN ISET_V3P3 HV_EN ISET_S0 S0 ISET_S3 GND THRM PAD
C3285 0.1UF 10% 16V X5R-CERM 0201
C3286 10UF 20% 6.3V CERM-X5R 0402
C3211 0.1UF 10% 25V X5R 402
PP3V3_S4_TBTAPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V)
PP3V3RHV_S4_TBTAPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)
S4_PWR_EN
TBT_A_HV_EN
PM_SLP_S3_R_L
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTHV:P15V R3210 22.6K 1% 1/20W MF 2012 (12V: See below)
TBTHV:P15V R3211 22.6K 1% 1/20W MF 2012
R3212 36.5K 1% 1/20W MF 2012 <RV3P3>
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
TBTHV:P15V R3213 22.6K 1% 1/20W MF 2012 <RHVS3>
TBTHV:P15V R3214 22.6K 1% 1/20W MF 2012 <RHVS0>
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

PP3V3_S4_TBTAPWR
C3220 0.1UF 10% 16V X5R-CERM 0201
CRITICAL U3220 CBTL05024 HVQFN24-COMBO
SIGNAL_MODEL=TBT_MUX
GND_VOID=TRUE (Both C's)
C3277 0.47UF 20% 4V_201 CERM-X5R-1
C3276 0.47UF 20% 4V_201 CERM-X5R-1
C3230 0.1UF 10% 16V X5R-CERM 0201
C3231 0.1UF 10% 16V X5R-CERM 0201
C3232 0.22UF 20% 6.3V X5R 0201
C3233 0.22UF 20% 6.3V X5R 0201
TBT_A_D2R_N<1> / TBT_A_D2R_P<1>
TBT_A_D2R_C_N<1> / TBT_A_D2R_C_P<1>
DP_TBTPA_AUXCH_C_N / DP_TBTPA_AUXCH_C_P
DP_TBTPA_AUXCH_N / DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA / DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1> / DP_TBTPA_ML_C_N<1>
DP_TBTPA_ML_P<1> / DP_TBTPA_ML_N<1>
TBT_A_LSTX / TBT_A_LSRX
DP_TBTPA_HPD
TBT_A_CIO_SEL
TBTDP_AUXIO_EN
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N / TBT_A_D2R1_AUXDDC_P
TBT: RX_1
TBT_A_CONFIG1_RC
TBT_A_HPD
TBT_A_LSX_ML_P<1> / TBT_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)

Thunderbolt Connector A

CRITICAL L3200 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTAPWR_F (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)
C3200 0.01UF 10% 50V X7R-CERM 0402
R3201 12 5% 1/20W MF 201
TBTACONN_20_RC (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V)
C3201 0.01UF 10% 50V X7R-CERM 0402
TBTACONN_1_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V)
C3205 0.01UF 10% 25V X5R-CERM 0201 (0-18.9V)
TBTACONN_7_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V)
C3206 0.01UF 10% 25V X5R-CERM 0201 (0-18.9V)
GND_VOID=TRUE (Both C's)
C3274 0.47UF 20% 4V_201 CERM-X5R-1
C3275 0.47UF 20% 4V_201 CERM-X5R-1
C3278 0.22UF 20% 6.3V X5R 0201
C3279 0.22UF 20% 6.3V X5R 0201
C3270 0.22UF 20% 6.3V X5R 0201
C3271 0.22UF 20% 6.3V X5R 0201
C3272 0.22UF 20% 6.3V X5R 0201
C3273 0.22UF 20% 6.3V X5R 0201
R3294 1K 5% 1/20W MF 201
R3295 1K 5% 1/20W MF 201
R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
TBT_A_D2R_P<0> / TBT_A_D2R_N<0>
TBT_A_D2R_C_P<0> / TBT_A_D2R_C_N<0>
DP_TBTPA_ML_C_P<3> / DP_TBTPA_ML_C_N<3>
DP_TBTPA_ML_P<3> / DP_TBTPA_ML_N<3>
TBT_A_D2R_C_P<1> / TBT_A_D2R_C_N<1>
TBT_A_D2R_P<1> / TBT_A_D2R_N<1>
TBT_A_D2R_C_P<0> / TBT_A_D2R_C_N<0>
TBT_A_D2R_P<0> / TBT_A_D2R_N<0>
TBT Dir / DP Dir
TBT: RX_0
TBT: TX_0
TBT: Unused
TBT: TX_1
TBT: RX_1
DP_A_LSX_ML_P<1> / DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R-CERM 0201
C3295 330PF 10% 16V X7R-CERM 0201
R3241 100K 5% 1/20W MF 201
C3202 0.01UF 10% 16V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
CRITICAL J3200 MDP-J44 F-RT-TH GND0 (514-0876)
SHIELD PINS
PORT B
SHIELD PINS
470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 32 OF 118
SHEET: 31 OF 81

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
CRITICAL C3387 100UF 20% 6.3V POLY-TANT CASE-B2-SM; C3380 22UF 20% 6.3V X5R-CERM 0603; C3381 0.1UF 10% 16V X5R-CERM 0201
PP15V_TBT 15.75V Max
C3315 4.7UF 10% 25V X5R-CERM 0603; C3310 0.1UF 10% 16V X5R 402
CRITICAL U3310 CD3211A0RGPR QFN
V3P3 (19,20) V3P3OUT (18) PP3V3_S4_TBTBPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V)
VHV (6,7) OUT (12,14) PP3V3RHV_S4_TBTBPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)
C3385 0.1UF 10% 16V X5R-CERM 0201; C3386 10UF 20% 6.3V CERM-X5R 0402; C3311 0.1UF 10% 25V X5R 402
ENHVU (16)
EN (5) ← S4_PWR_EN
HV_EN (11) ← TBT_B_HV_EN
S0 (17) ← PM_SLP_S3_R_L
FAULTZ (4)
ISET_V3P3 (8) ← TBTBPWRSW_ISET_V3P3
ISET_S0 (10) ← TBTBPWRSW_ISET_S0
ISET_S3 (9) ← TBTBPWRSW_ISET_S3
GND (1,2,3,13,15) THRM PAD (21)
TBTHV:P15V R3310 22.6K 1% 1/20W MF 201; TBTHV:P15V R3311 22.6K 1% 1/20W MF 201; R3312 36.5K 1% 1/20W MF 201 <RV3P3>
12V: See below
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
TBTHV:P15V R3313 22.6K 1% 1/20W MF 201 <RHVS3>; TBTHV:P15V R3314 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

PP3V3_S4_TBTBPWR
C3320 0.1UF 10% 16V X5R-CERM 0201
CRITICAL U3320 CBTL05024 HVQFN24-COMBO
VDD (3) ← SIGNAL_MODEL=TBT_MUX
GND_THMPAD (9,21,25)

TB- (7)	← TBT_B_D2R_C_N<1>	TB_ENA (15)	→ TBT_B_CIO_SEL
TB+ (8)	← TBT_B_D2R_C_P<1>	AUXIO_EN (24)	→ TBTDP_AUXIO_EN
		DP_PD (6)	← TBT_B_DP_PWRDN
AUX- (1)	← DP_TBTPB_AUXCH_C_N	(IPU) AUXIO- (23)	→ TBT_B_D2R1_AUXDDC_N
AUX+ (2)	← DP_TBTPB_AUXCH_P	(IPD) AUXIO+ (22)	→ TBT_B_D2R1_AUXDDC_P
			TBT: RX_1
DDC_DAT (4)	← DP_TBTPB_DDC_DATA		
DDC_CLK (5)	← DP_TBTPB_DDC_CLK		
CA_DETOUT (16)	→ TBT_B_CONFIG1_BUF	CA_DET (18)	→ TBT_B_CONFIG1_RC
DP+ (11)	← DP_TBTPB_ML_P<1>		
DP- (10)	← DP_TBTPB_ML_N<1>		
		DPML0+ (19)	→ DP_B_LSX_ML_P<1>
LSTX (IPU) (14)	← TBT_B_LSTX	DPML0- (20)	→ DP_B_LSX_ML_N<1>
LSRX (IPD) (13)	→ TBT_B_LSRX		TBT: LSX_A_R2P/P2R (P/N)
HPDOUT (12)	→ DP_TBTPB_HPD	HPD (17)	→ TBT_B_HPD

GND_VOID=TRUE (Both C's)
C3377 0.47UF 20% 4V 201 CERM-X5R-1; C3376 0.47UF 20% 4V 201 CERM-X5R-1
TBT_B_D2R_N<1> → TBT_B_D2R_C_N<1>
TBT_B_D2R_P<1> → TBT_B_D2R_C_P<1>
C3330 0.1UF 10% 16V X5R-CERM 0201; C3331 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPB_AUXCH_C_N → DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P → DP_TBTPB_AUXCH_C_P
C3332 0.22UF 20% 6.3V X5R 0201; C3333 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_C_P<1> → DP_TBTPB_ML_P<1>
DP_TBTPB_ML_C_N<1> → DP_TBTPB_ML_N<1>

Thunderbolt Connector B

CRITICAL L3300 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTBPWR_F (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)
C3300 0.01UF 10% 50V X7R-CERM 0402
R3301 12 5% 1/20W MF 201
TBTBCONN_20_RC (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V)
C3301 0.01UF 10% 50V X7R-CERM 0402
C3302 0.01UF 10% 16V X5R-CERM 0201

GND_VOID=TRUE (Both C's)
C3374 0.47UF 20% 4V 201 CERM-X5R-1; C3375 0.47UF 20% 4V 201 CERM-X5R-1
TBT_B_D2R_P<0> → TBT_B_D2R_C_P<0>
TBT_B_D2R_N<0> → TBT_B_D2R_C_N<0>
GND_VOID=TRUE R3394 1K 5% 1/20W MF 201; R3395 1K 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
C3378 0.22UF 20% 6.3V X5R 0201; C3379 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_C_P<3> → DP_TBTPB_ML_P<3>
DP_TBTPB_ML_C_N<3> → DP_TBTPB_ML_N<3>
R3379 470K 5% 1/20W MF 201; R3378 470K 5% 1/20W MF 201
TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N
TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC
R3352 1M 5% 1/20W MF 201; R3351 1M 5% 1/20W MF 201; C3394 330PF 10% 16V X7R-CERM 0201; C3395 330PF 10% 16V X7R-CERM 0201; R3341 100K 5% 1/20W MF 201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

CRITICAL
SHIELD PINS (S5,S4,S3,S2,S1)
J3200 MDP-J44 F-RT-TH
PORT A SHIELD PINS (S23,S11,S10,S9,S8,S7,S6)
514-0876

A2	HPD	GND0	A1
A4	CONFIG1	ML_LANE0P	A3
A6	CONFIG2	ML_LANE0N	A5
A8	GND2	GND1	A7
A10	ML_LANE3P	ML_LANE1P	A9
A12	ML_LANE3N	ML_LANE1N	A11
A14	GND4	GND3	A13
A16	AUX_CHP	ML_LANE2P	A15
A18	AUX_CHN	ML_LANE2N	A17
A20	DP_PWR	RETURN	A19

TBT Dir DP Dir
TBT: RX_0
TBT: Unused
TBT: RX_1

TBTBCONN_1_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V) (0-18.9V)
C3305 0.01UF 10% 25V X5R-CERM 0201
TBTBCONN_7_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V) (0-18.9V)
C3306 0.01UF 10% 25V X5R-CERM 0201
DP Dir TBT Dir
TBT_B_R2D_P<0> → TBT_B_R2D_C_P<0>
TBT_B_R2D_N<0> → TBT_B_R2D_C_N<0>
TBT: TX_0
TBT_B_R2D_P<1> → TBT_B_R2D_C_P<1>
TBT_B_R2D_N<1> → TBT_B_R2D_C_N<1>
TBT: TX_1

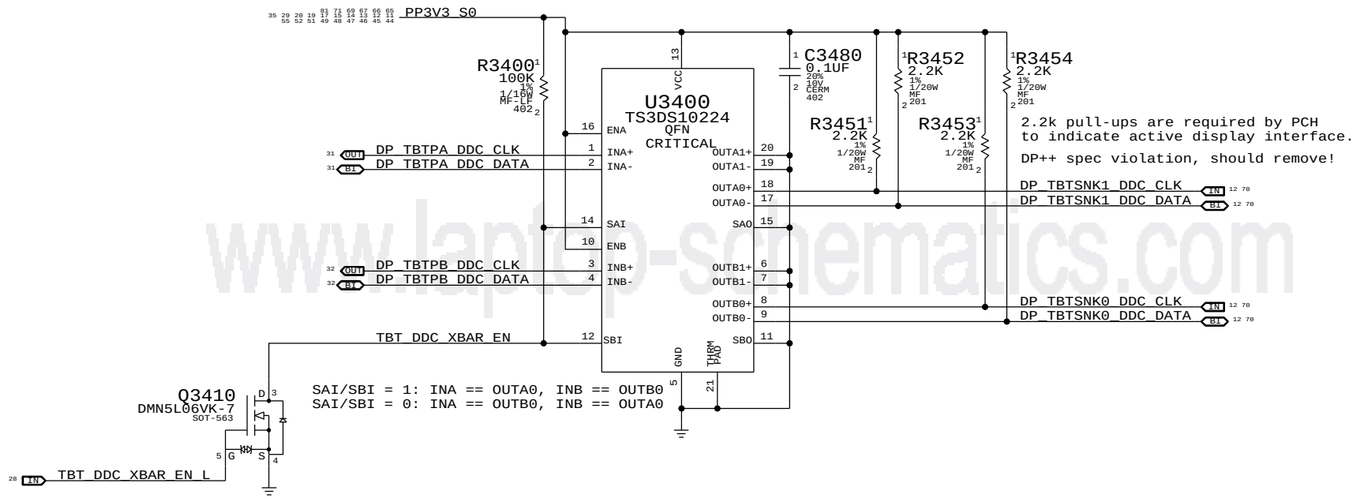
GND_VOID=TRUE (Both C's)
C3370 0.22UF 20% 6.3V X5R 0201; C3371 0.22UF 20% 6.3V X5R 0201
R3370 470K 5% 1/20W MF 201; R3371 470K 5% 1/20W MF 201
C3372 0.22UF 20% 6.3V X5R 0201; C3373 0.22UF 20% 6.3V X5R 0201
R3372 470K 5% 1/20W MF 201; R3373 470K 5% 1/20W MF 201
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)

470k R's for ESD protection on AC-coupled signals.

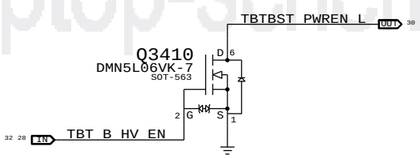
SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012
PAGE TITLE: Thunderbolt Connector B
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 33 OF 118
SHEET: 32 OF 81

DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!



Second TBT Port HV Boost Enable



SYNC MASTER=J15 REFERENCE	SYNC DATE=11/16/2012
PAGE TITLE	DDC Crossbar
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 34 OF 118
	SHEET 33 OF 81

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 0OHM, 0201	L3570,L3571,L3573,L3574		

3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

AIRPORT

BLUETOOTH

Supervisor & CLKREQ # Isolation

Delay = 130 ms +/- 20%

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: X29C CONNECTOR

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

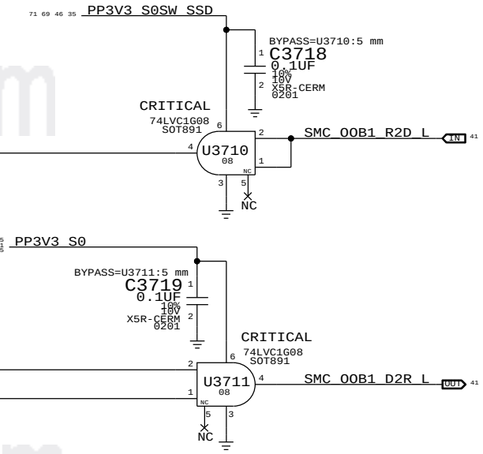
REVISION: <E4LABEL>

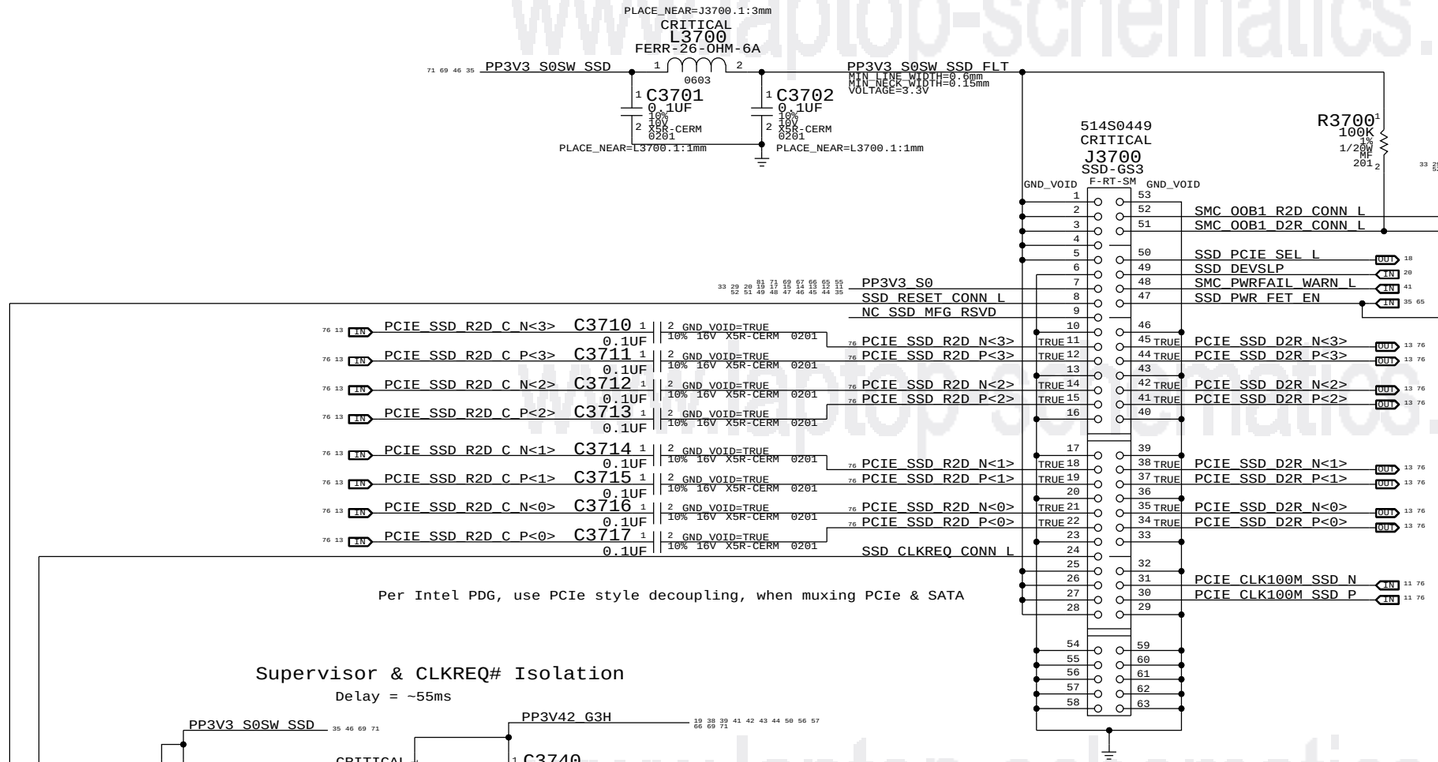
BRANCH: <BRANCH>

PAGE: 35 OF 118

SHEET: 34 OF 81

OOB Isolation

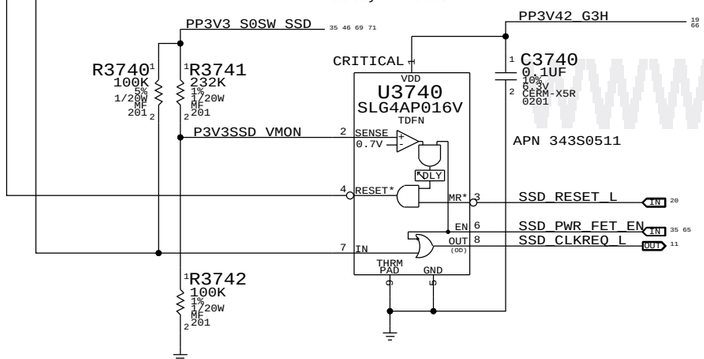




Per Intel PDG, use PCIe style decoupling, when muxing PCIe & SATA

Supervisor & CLKREQ# Isolation

Delay = ~55ms



SSD_PWR_FET_EN = SSD_PWR_FET_EN

MAKE_BASE=TRUE

Gumstick3 Connector

SYNC_MASTER=CLEAN_MLB_KEPLER	SYNC_DATE=06/08/2013
PAGE TITLE: SSD Connector	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 37 OF 118
	SHEET: 35 OF 81

U3900 BCM15700 FBGA SYM 3 OF 3 CRITICAL OMIT_TABLE

U3900 BCM15700 FBGA SYM 2 OF 3 CRITICAL OMIT_TABLE

U3900 BCM15700 FBGA SYM 1 OF 3 CRITICAL OMIT_TABLE

L3902 1.0UH-1.6A-55MOHM 1008 — P1V35 CAM SRVLXD PHASE

L3901 1.0UH-1.6A-55MOHM 1008 — P1V2 CAM SRVLXC PHASE

L3906 22NH 0402

L3903 220-OHM-1.4A 0603

L3904 220-OHM-1.4A 0603

XW3900 SM

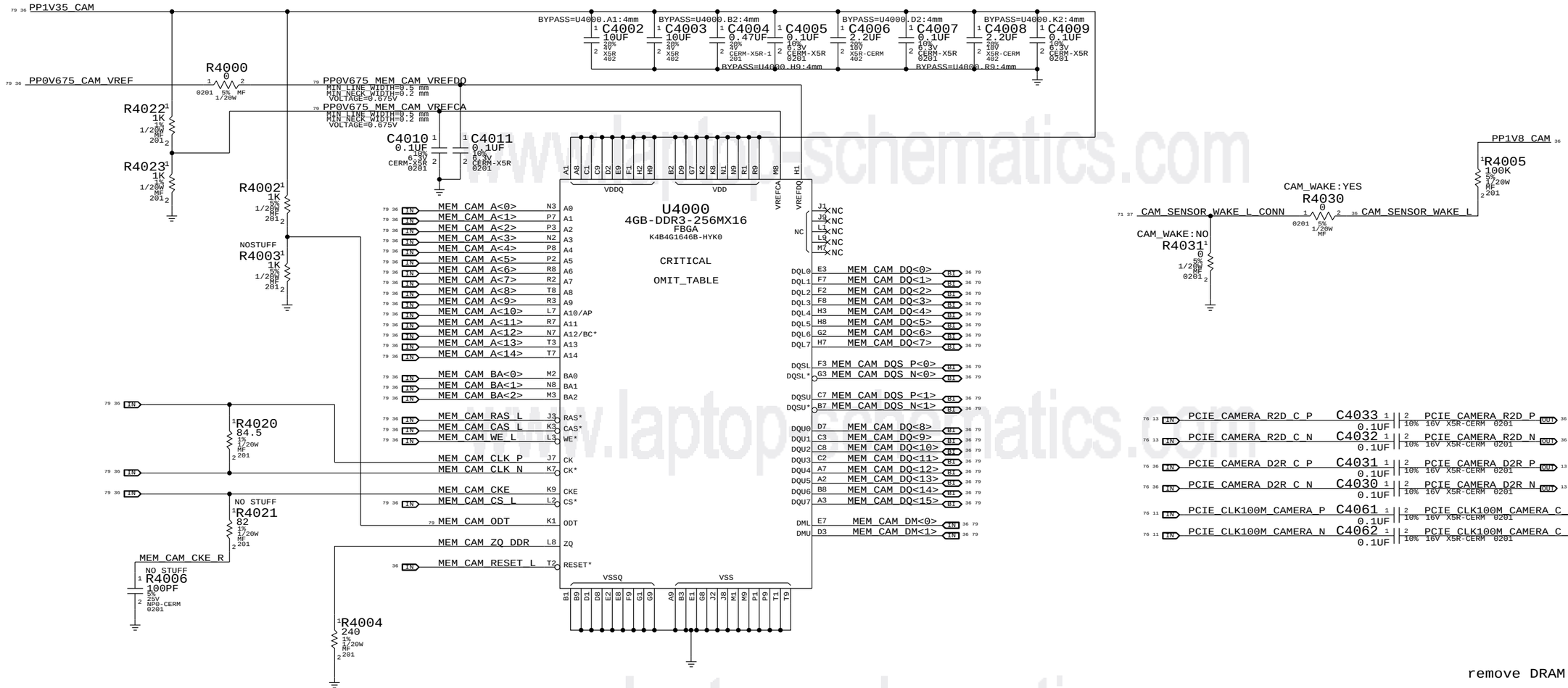
XW3901 SM

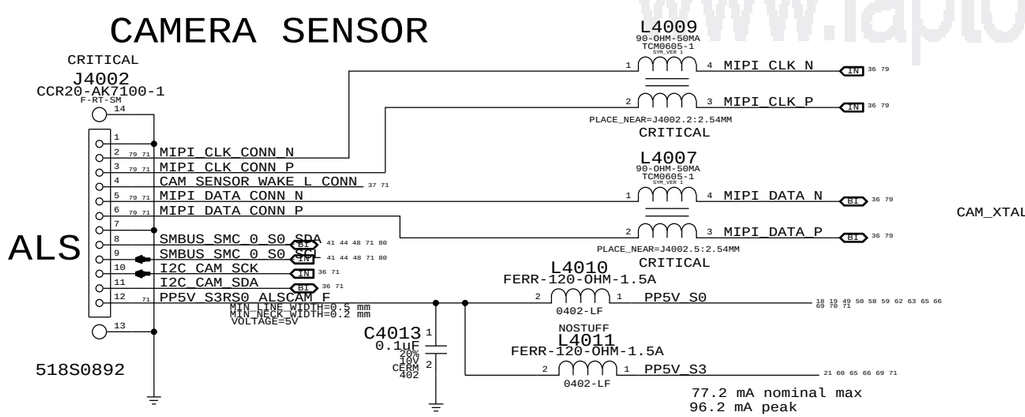
R3912 240 1% 1/20W MF 201

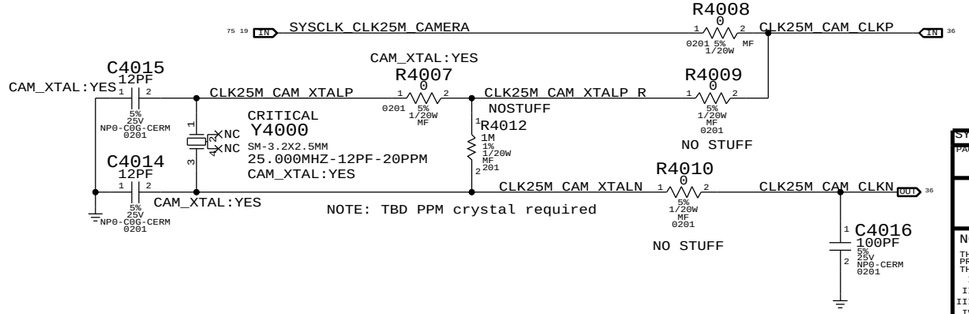
PU on PCH page

A1 SILICON BUG

SYNC_MASTER=CLEAN_MLB_REPLER	SYNC DATE=06/13/2013
PAGE TITLE	Camera 1 of 2
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 39 OF 118
	SHEET 36 OF 81







remove DRAM SPD Straps

DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

SYNC_MASTER=CLEAN_MLB_KEPLER
SYNC_DATE=06/13/2013
PAGE TITLE
Camera 2 of 2
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 40 OF 118
SHEET 37 OF 81

USB Port Power Switch

PP5V_S4

PM_SLP_S4_L

R4690 0 5% 1/16W MF-LF 402

USB_PWR_EN

USB_EXTA_OC_L (OUT)

CRITICAL U4600 TPS2557DRB SON

IN_0, IN_1, FAULT*, EN, OUT1, OUT2, ILIM, GND, THRM PAD

USB_ILIM

R4601 22.1K 1% 1/20W MF 201

USB_ILIM_R

R4600 22.1K 1% 1/16W MF-LF 402

NOSTUFF C4692 0.47UF 10% 10V X5R 0402

CRITICAL C4696 220UF-35MOHM 20% 6.3V POLY-TANT CASE-B2-SM1

C4690 10UF 20% 6.3V X5R 603

C4691 0.1UF 10% 10V X5R CERM 402

C4695 10UF 20% 6.3V X5R 603

PP5V_S3_LTUSB_A_ILIM
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

CURRENT LIMIT (R4600+R4601): 2.19A MIN / 2.76A MAX

Left USB Port A

We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin

CRITICAL L4605 FERR-120-OHM-3A 0603

PP5V_S3_LTUSB_A_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

C4605 0.01UF 10% 16V X7R-CERM 0402

CRITICAL L4600 90-OHM-50MA TCM0605-1

USB_EXTA_MUXED_N

USB_EXTA_MUXED_P

CRITICAL D4601 ESD0P2RF-02LS TSSLP-2-1

CRITICAL D4600 ESD0P2RF-02LS TSSLP-2-1

CRITICAL J4600 USB3.0-J44-ALT F-RT-TH

VBUS, SSTX+, SSTX-, GND, D-, D+, GND, SSRX+, SSRX-, GND

USB3_EXTA_R2D_P

USB3_EXTA_R2D_N

USB_LT1_N

USB_LT1_P

514-0934

USB/SMC Debug Mux

PP3V42_G3H

C4650 0.1UF 20% 10V CERM 402

R4650 100K 5% 1/16W MF-LF 402

SMC_DEBUGPRT_RX_L (IN)

SMC_DEBUGPRT_TX_L (OUT)

U4650 PI3USB102EZLE TQFN CRITICAL

M+, M-, D+, D-, OE*, SEL, VCC, GND, Y+, Y-

USB_EXTA_P (B1)

USB_EXTA_N (B1)

SMC_DEBUGPRT_EN_L (IN)

SEL=0 Choose SMC

SEL=1 Choose USB

SIGNAL_MODEL=MOJO_MUX_USBONLY

NOSTUFF R4651 0 5% 1/20W MF 0201

NOSTUFF R4652 0 5% 1/20W MF 0201

USB3_EXTA_D2R_N (OUT)

USB3_EXTA_D2R_P (OUT)

CRITICAL D4610 ESD0P2RF-02LS TSSLP-2-1

CRITICAL D4611 ESD0P2RF-02LS TSSLP-2-1

GND_VOID=TRUE

USB3_EXTA_R2D_C_N (IN) C4610 0.1UF 10%16V X5R-CERM 0201

USB3_EXTA_R2D_C_P (IN) C4611 0.1UF 10%16V X5R-CERM 0201

GND_VOID=TRUE

CRITICAL D4612 ESD0P2RF-02LS TSSLP-2-1

CRITICAL D4613 ESD0P2RF-02LS TSSLP-2-1

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: USB 3.0 CONNECTORS

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

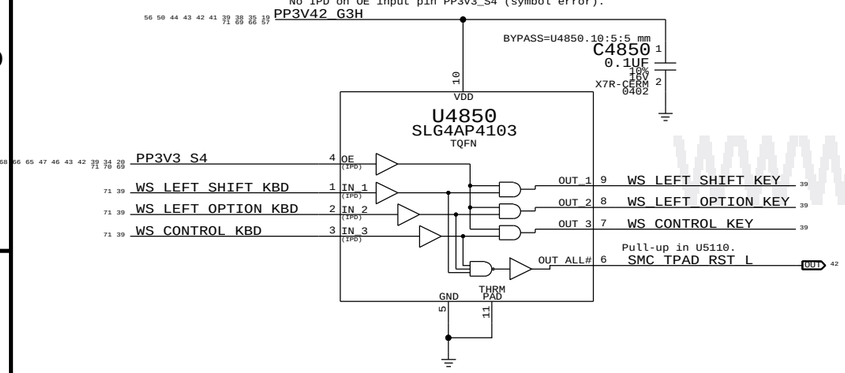
BRANCH: <BRANCH>

PAGE: 46 OF 118

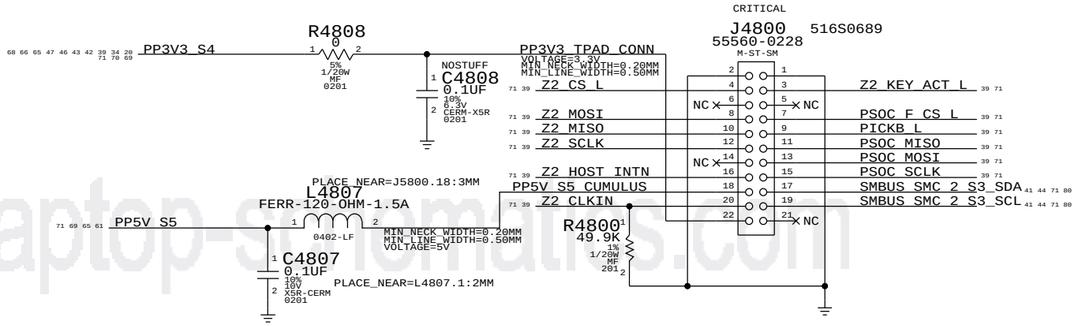
SHEET: 38 OF 81

SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

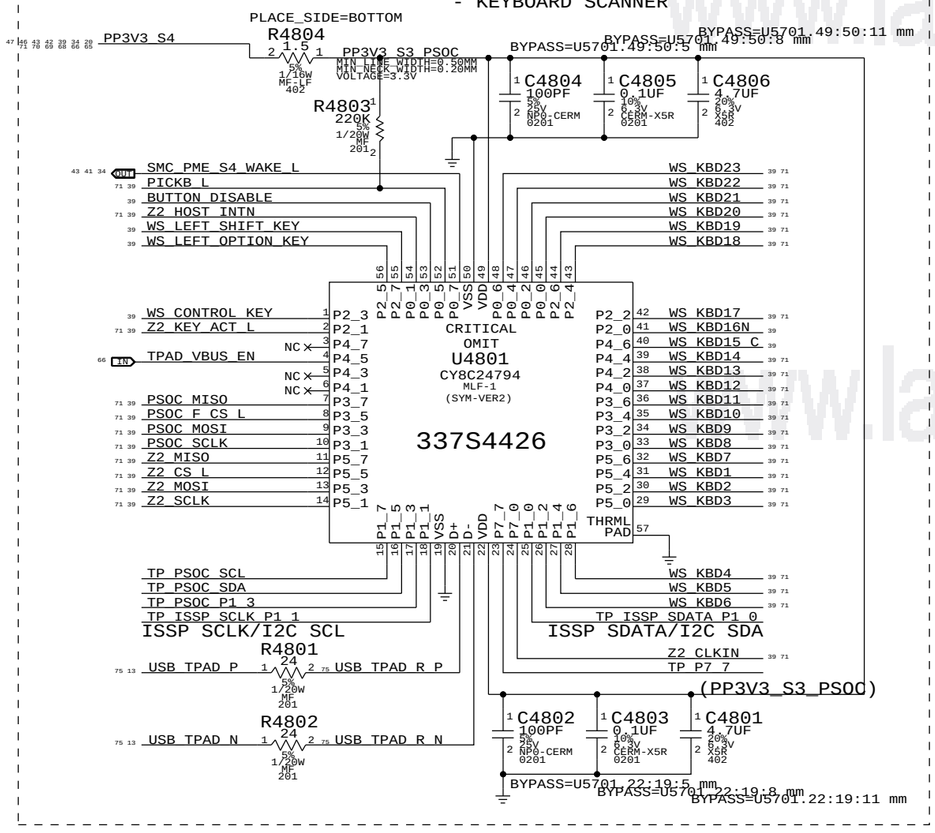


IPD Flex Connector



PSOC USB CONTROLLER

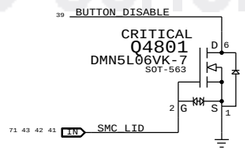
- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



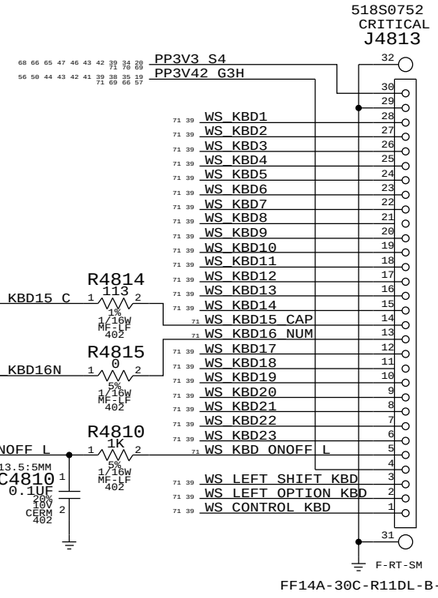
TPAD Buttons Disable

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V



Keyboard Connector



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

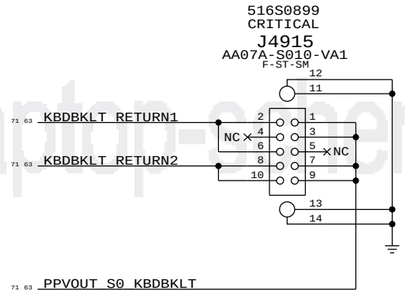
SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 48 OF 118
SHEET: 39 OF 81

Keyboard Backlight Connector



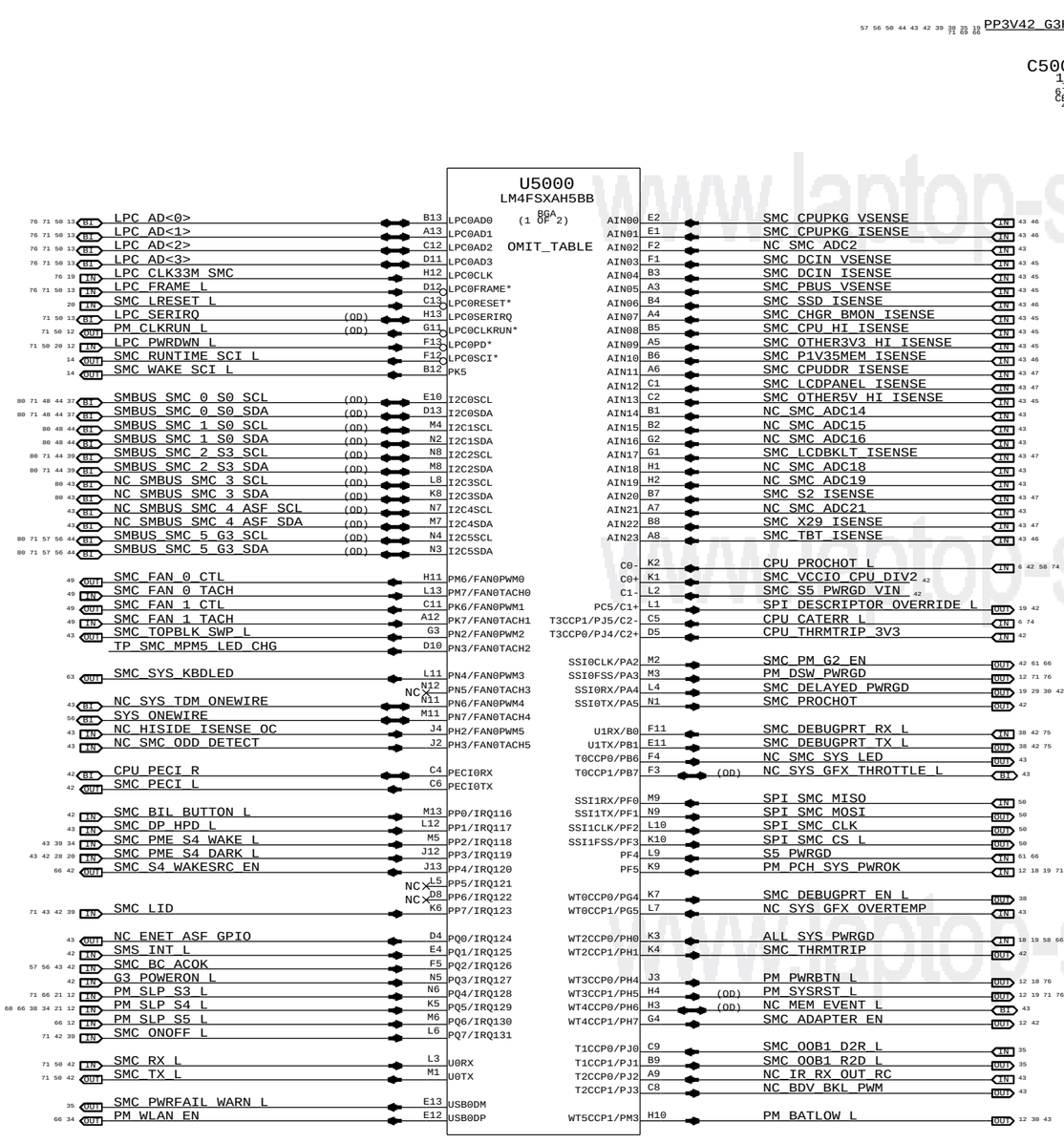
SYNC_MASTER=CHANG J45 SYNC_DATE=03/15/2013

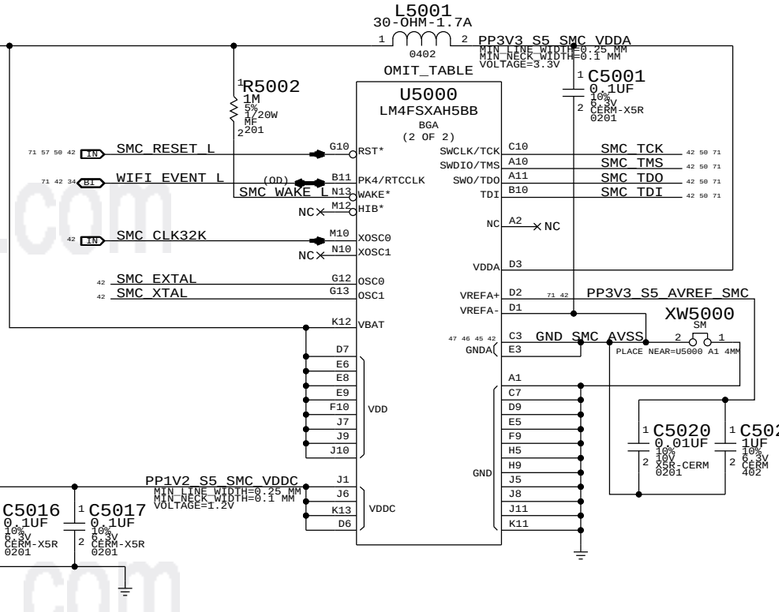
PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 49 OF 118
SHEET 40 OF 81

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=CHANG J45 SYNC_DATE=03/15/2013

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

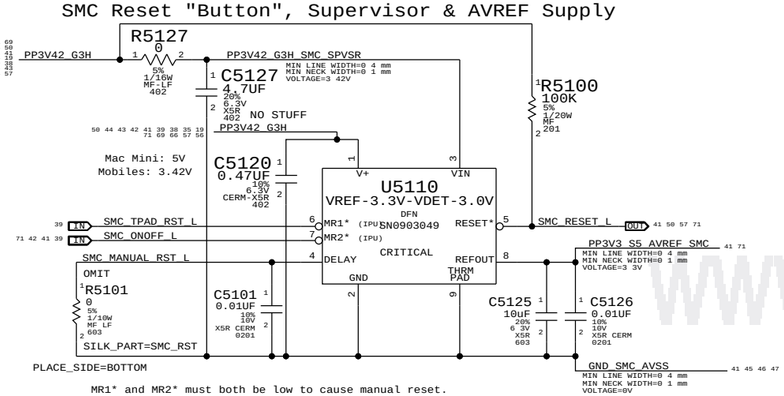
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 50 OF 118

SHEET: 41 OF 81

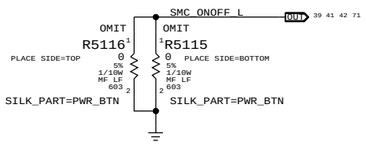
SMC Reset "Button", Supervisor & AVREF Supply



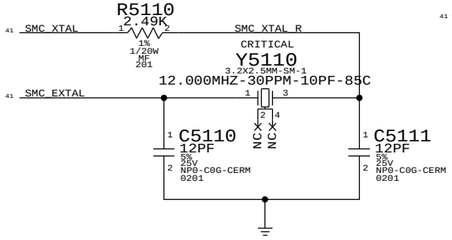
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

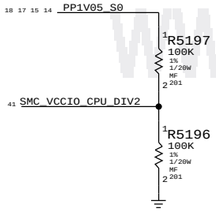
Debug Power "Buttons"



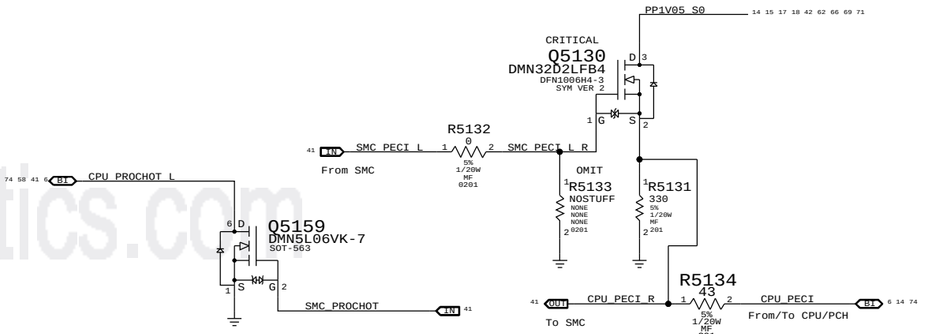
SMC Crystal Circuit

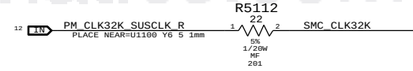


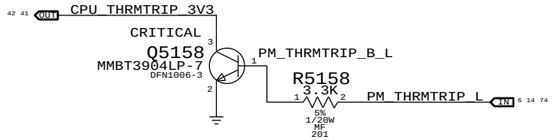
SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

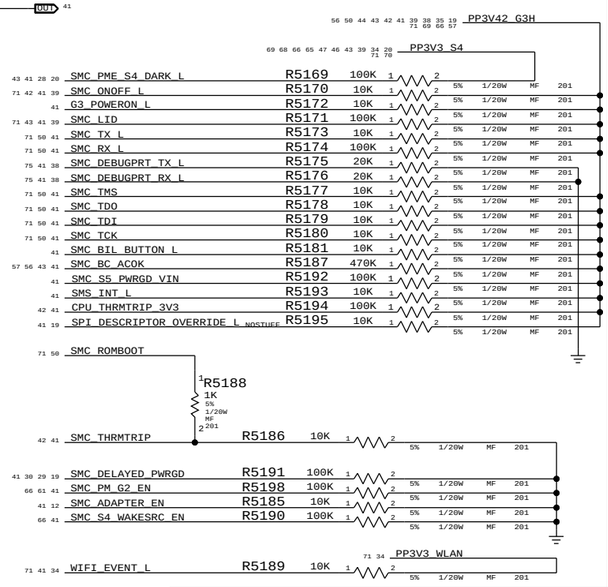


SMC12 PECI SUPPORT









SYNC_MASTER=CHANG_J45 SYNC_DATE=11/12/2012

PAGE TITLE: SMC Shared Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

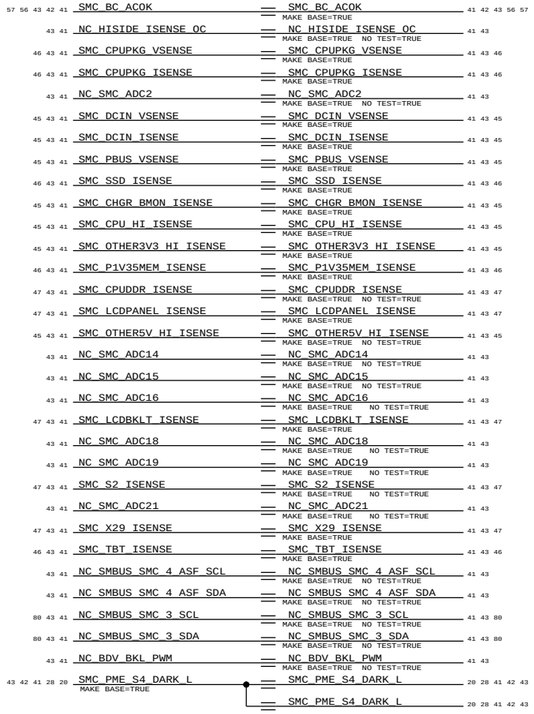
REVISION: <E4LABEL>

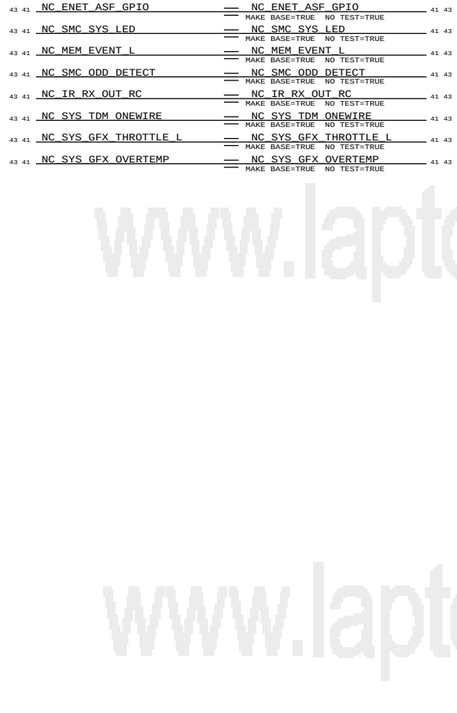
BRANCH: <BRANCH>

PAGE: 51 OF 118

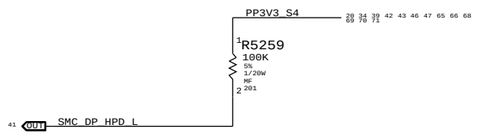
SHEET: 42 OF 81

8	7	6	5	4	3	2	1

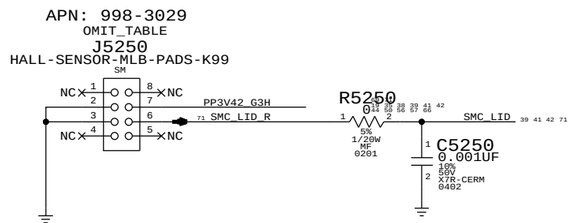




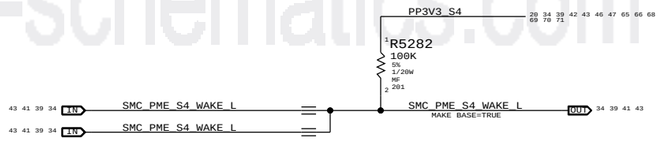
Spare S4 IRQ

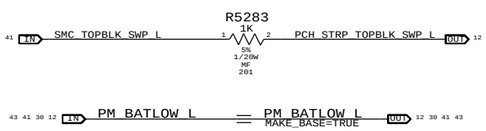


Hall Effect pads



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	





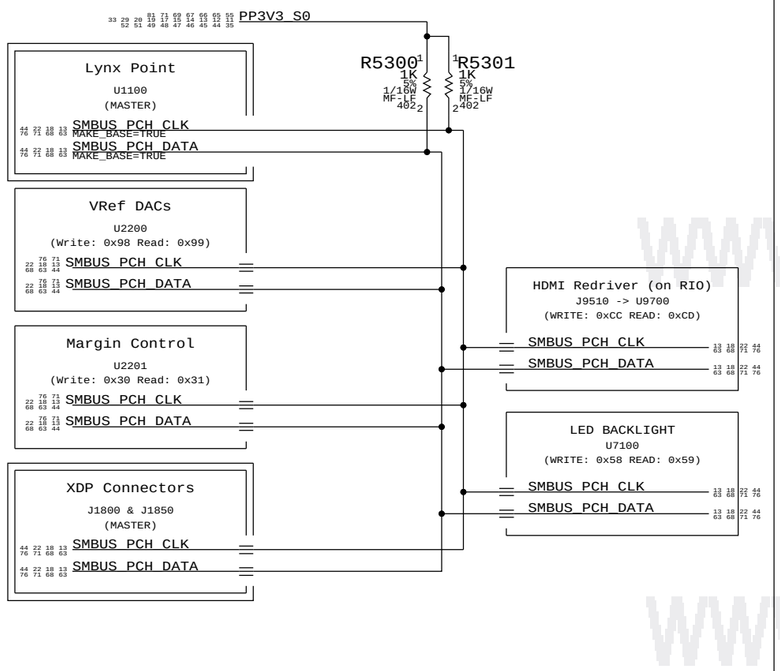
PAGE TITLE
SMC Project Support

Apple Inc.

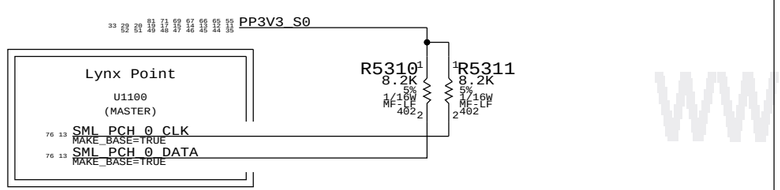
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 52 OF 118
SHEET 43 OF 81

8	7	6	5	4	3	2	1

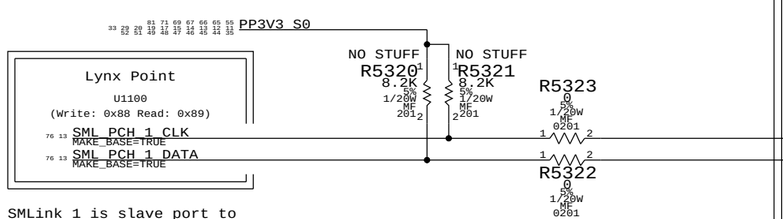
PCH SMBus "0" Connections



PCH "SMLink 0" Connections

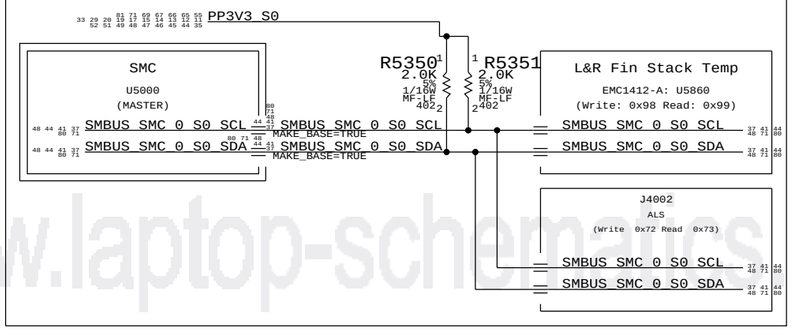


PCH "SMLink 1" Connections



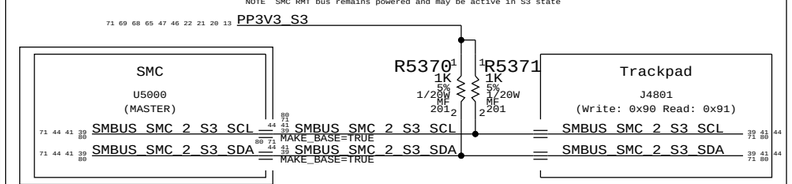
SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

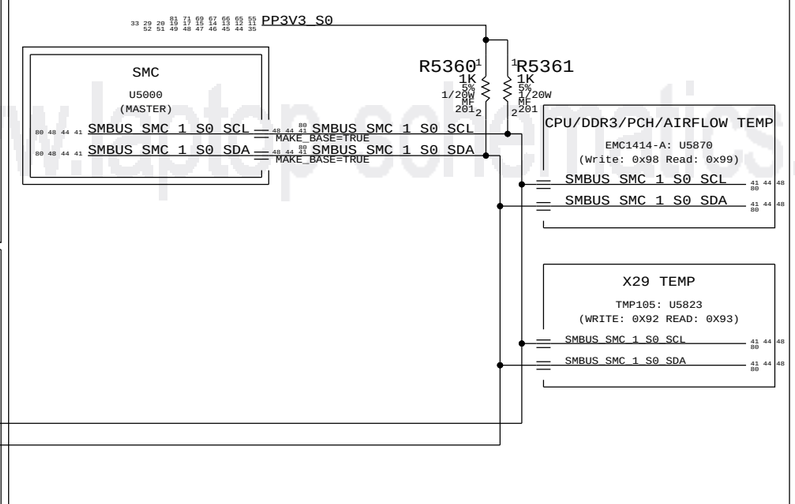


SMC "2" SMBUS CONNECTIONS

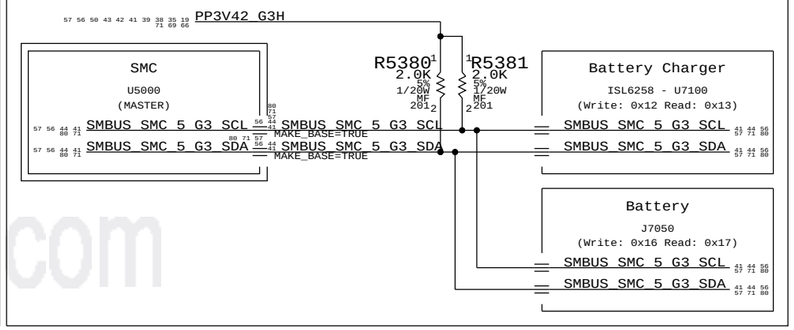
NOTE SMC RMT bus remains powered and may be active in S3 state



SMC "1" SMBUS CONNECTIONS



SMC "5" SMBUS CONNECTIONS



SMC "4" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

SMC "3" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

SYNC MASTER=CHANG J45 SYNC DATE=11/26/2012

PAGE TITLE: SMBus Connections

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

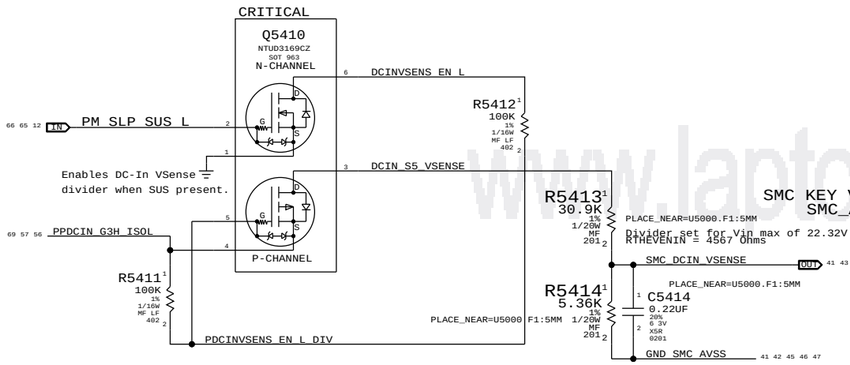
REVISION: <E4LABEL>

BRANCH: <BRANCH>

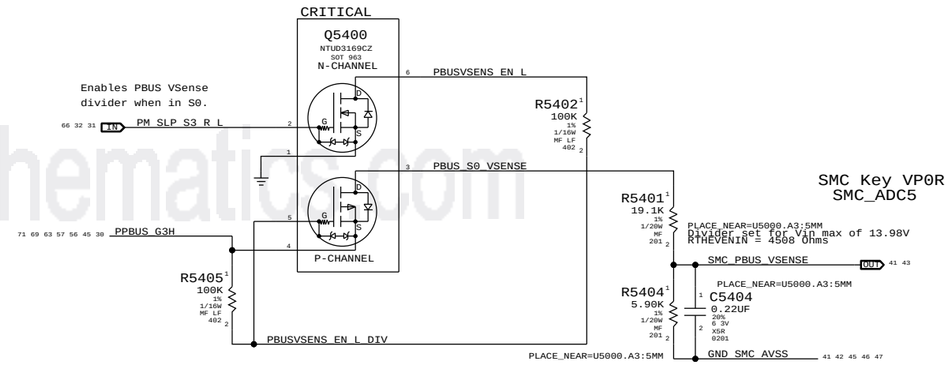
PAGE: 53 OF 118

SHEET: 44 OF 81

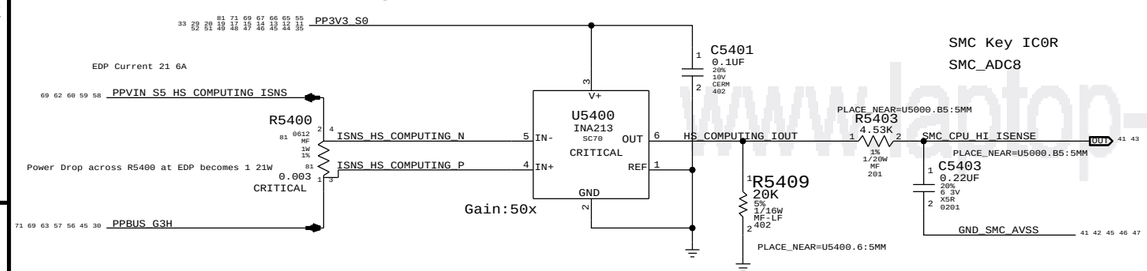
DC-In Voltage Sense Enable & Filter



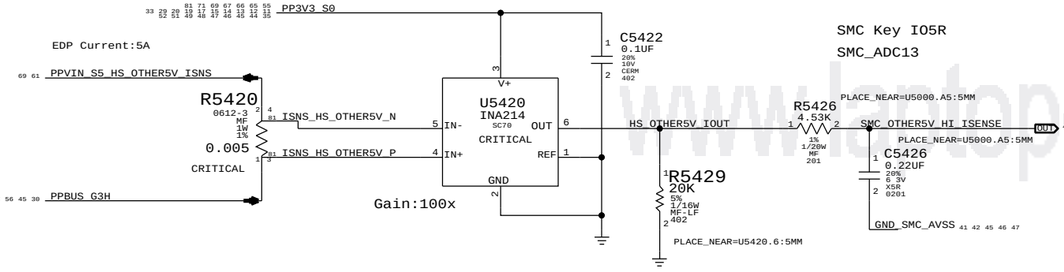
PBUS Voltage Sense Enable & Filter



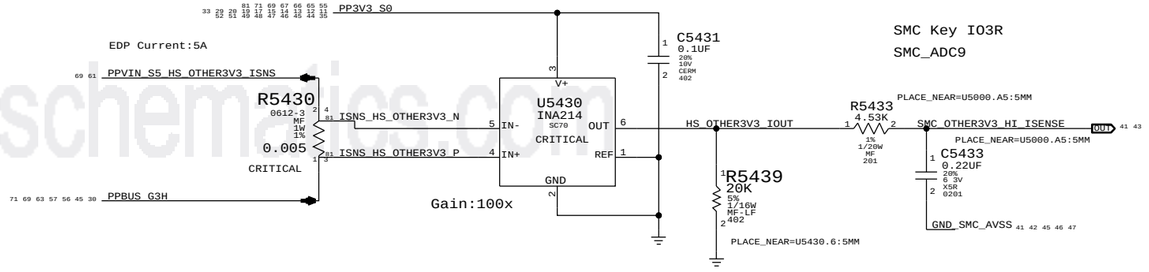
COMPUTING High Side Current Sense / Filter



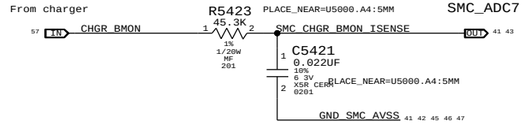
OTHERS (5V) High Side Current Sense / Filter



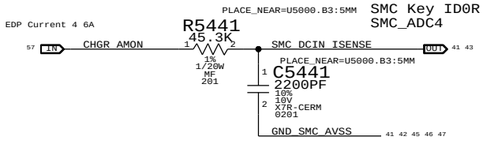
OTHERS (3.3V) High Side Current Sense / Filter



CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



SYNC_MASTER=CHANG J45 SYNC_DATE=12/21/2012

PAGE TITLE: High Side Voltage and Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

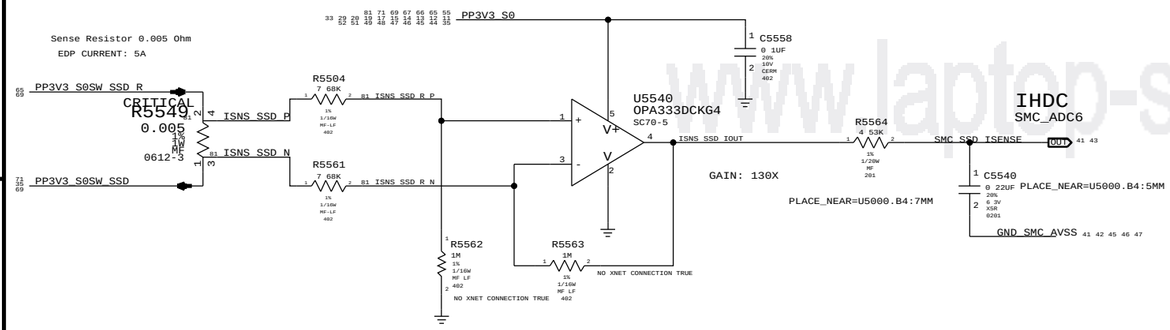
REVISION: <E4LABEL>

BRANCH: <BRANCH>

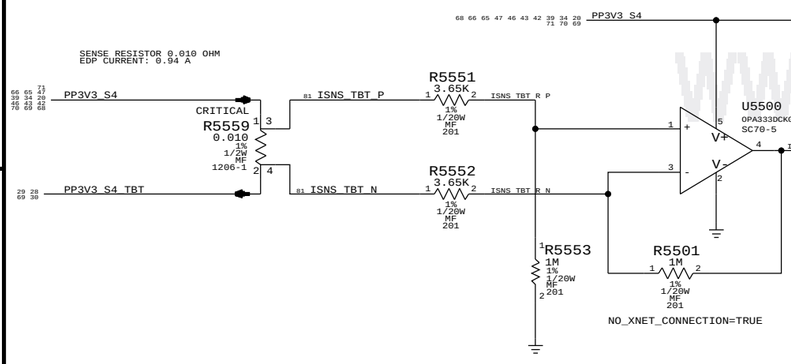
PAGE: 54 OF 118

SHEET: 45 OF 81

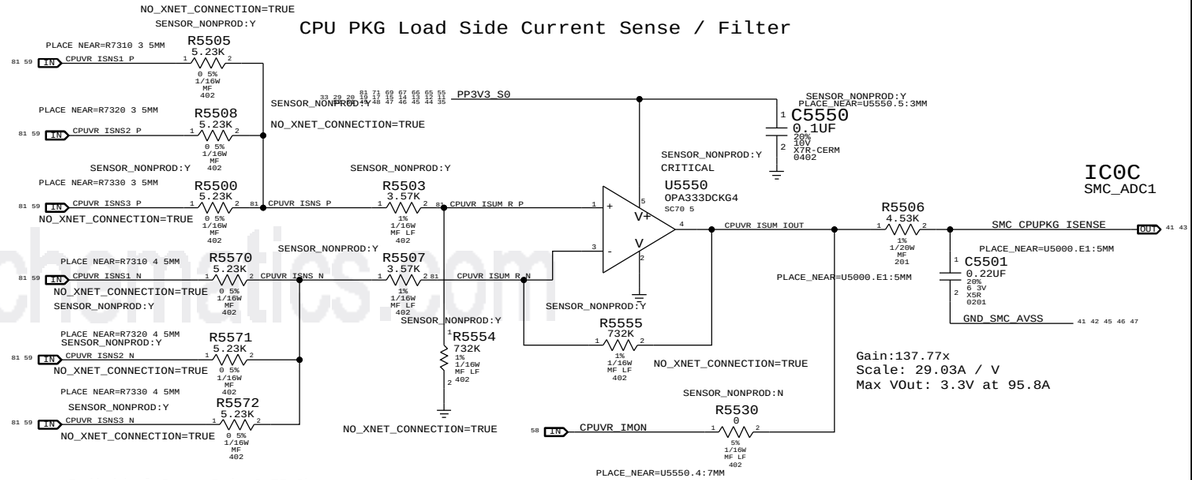
SSD CURRENT SENSE



TBT Router CURRENT SENSE

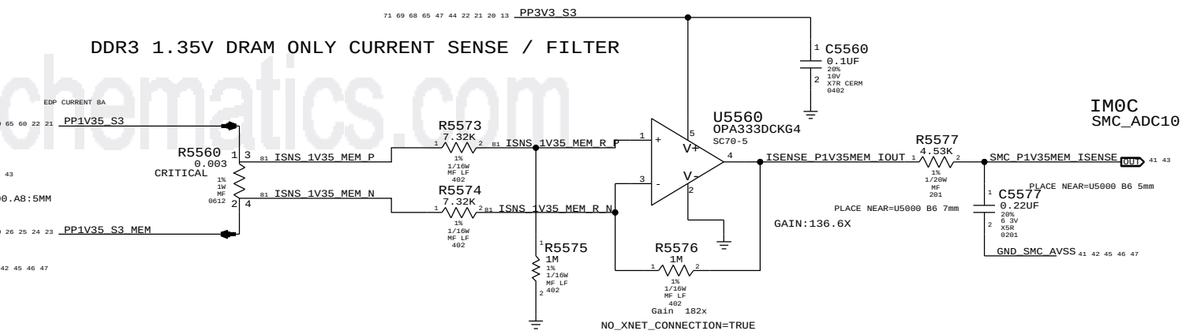


CPU PKG Load Side Current Sense / Filter

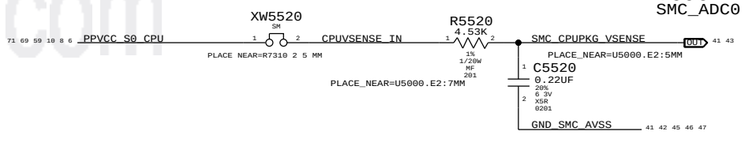


Individual Sense R is 0.75mOhm
EDP: 95A TDP :45A
(Effective Sense R is 0.25mOhm due to summing of the 3 phases)

DDR3 1.35V DRAM ONLY CURRENT SENSE / FILTER

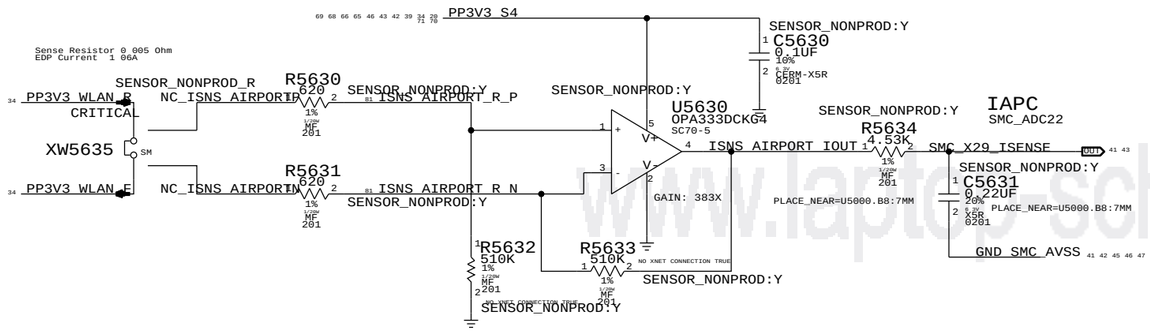


CPU Vcore Voltage Sense / Filter



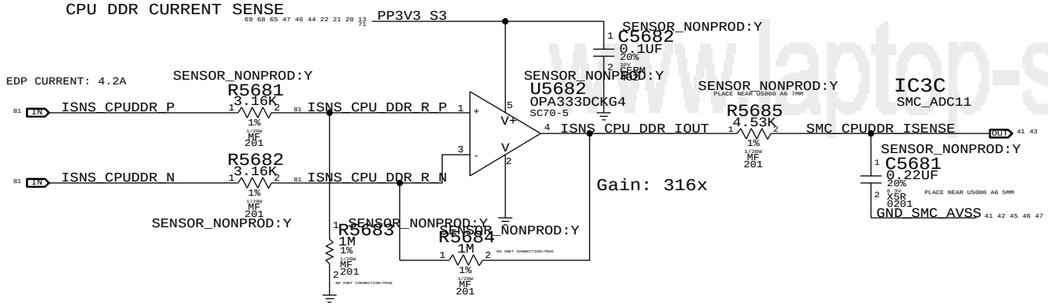
SYNC_MASTER=CHANG_J45	SYNC_DATE=03/15/2013
PAGE TITLE: Load Side Voltage and Current Sensing	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 55 OF 118
	SHEET: 46 OF 81

X29 AIRPORT CURRENT SENSE

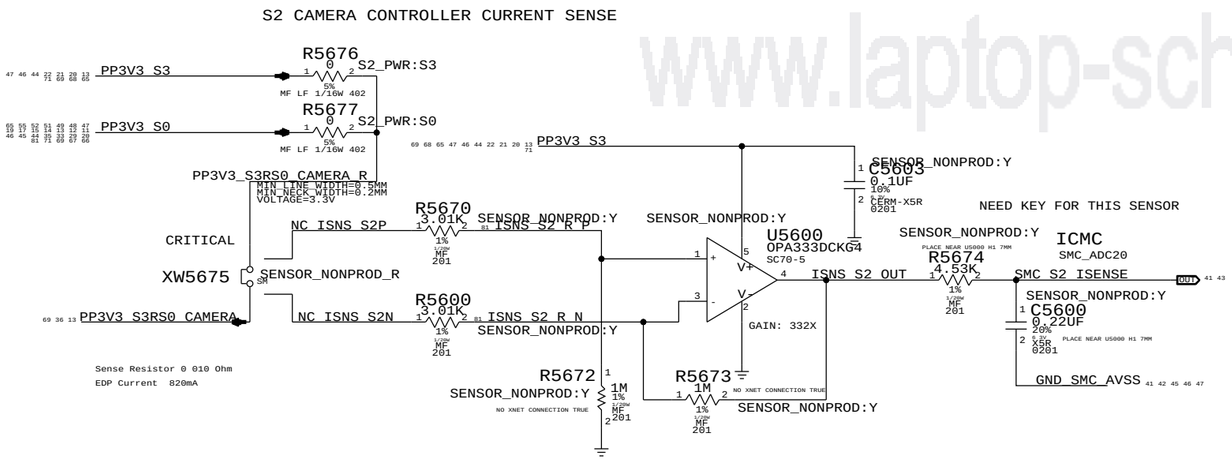


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	7	RES MTL FILM 100K 5 1/20W 0201 SMD LF	C5601 C5631 C5660 C5661 C5671 C5610		SENSOR_NONPROD:N

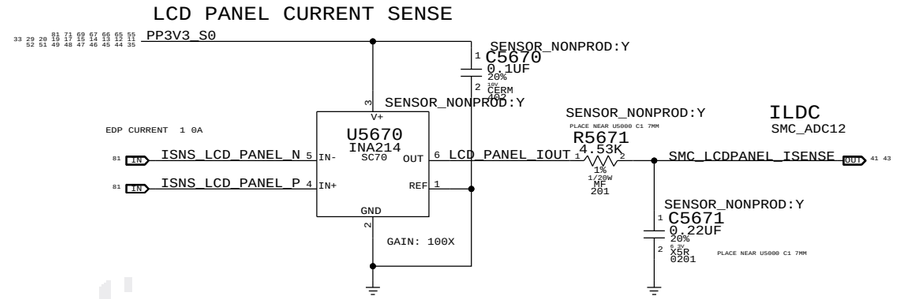
CPU DDR CURRENT SENSE



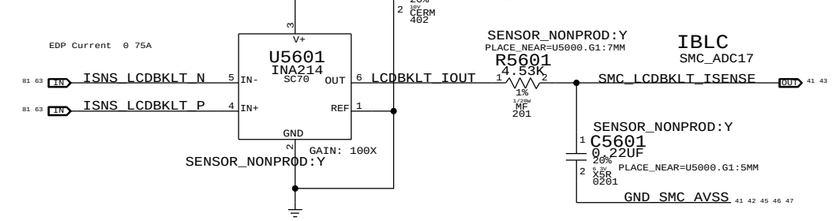
S2 CAMERA CONTROLLER CURRENT SENSE



LCD PANEL CURRENT SENSE



LCD BKLT Current Sense



SYNC MASTER=CHANG J45 SYNC DATE=12/21/2012

PAGE TITLE

Debug Sensors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

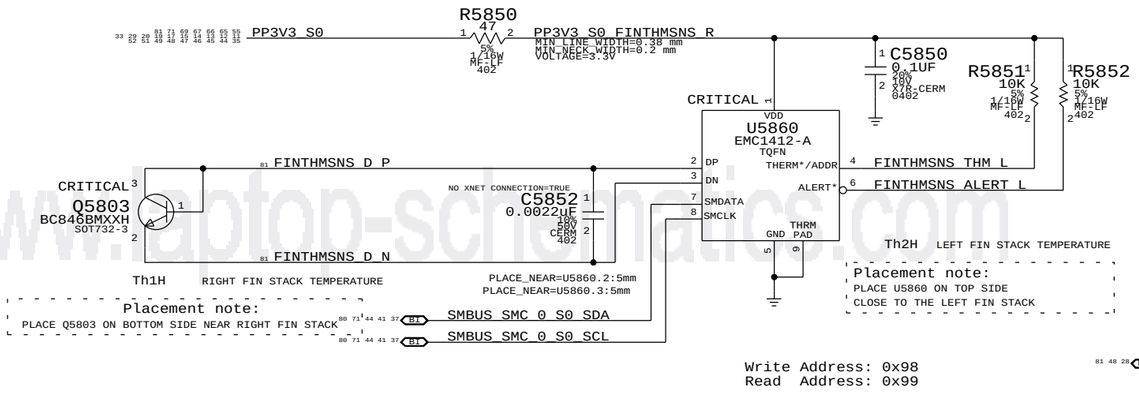
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 56 OF 118

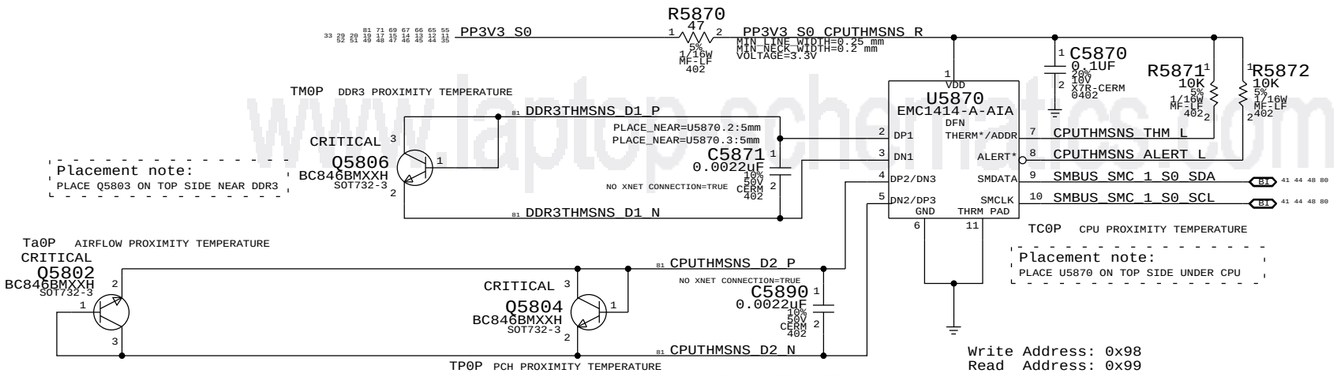
SHEET 47 OF 81

LEFT FIN STACK/RIGHT FIN STACK



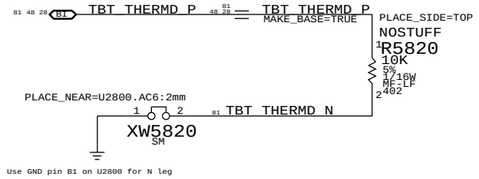
Write Address: 0x98
Read Address: 0x99

DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY

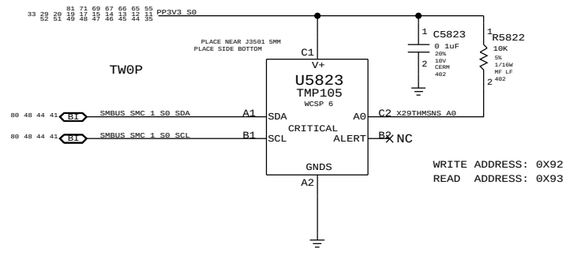


Write Address: 0x98
Read Address: 0x99

THSP TBT DIE



X29 PROXIMITY



WRITE ADDRESS: 0X92
READ ADDRESS: 0X93

SYNC MASTER=CHANG J45 SYNC DATE=11/26/2012

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

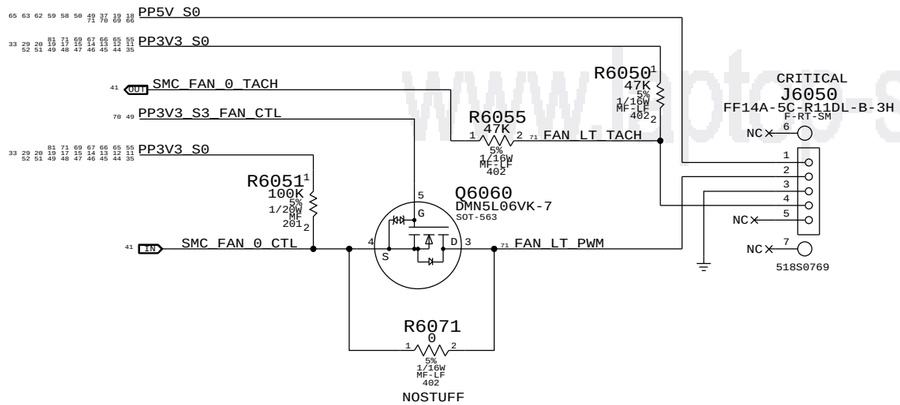
REVISION: <E4LABEL>

BRANCH: <BRANCH>

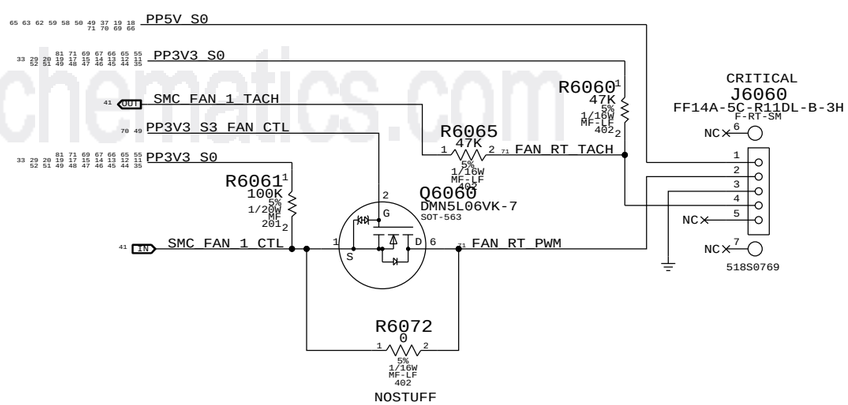
PAGE: 58 OF 118

SHEET: 48 OF 81

Left Fan



Right Fan



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

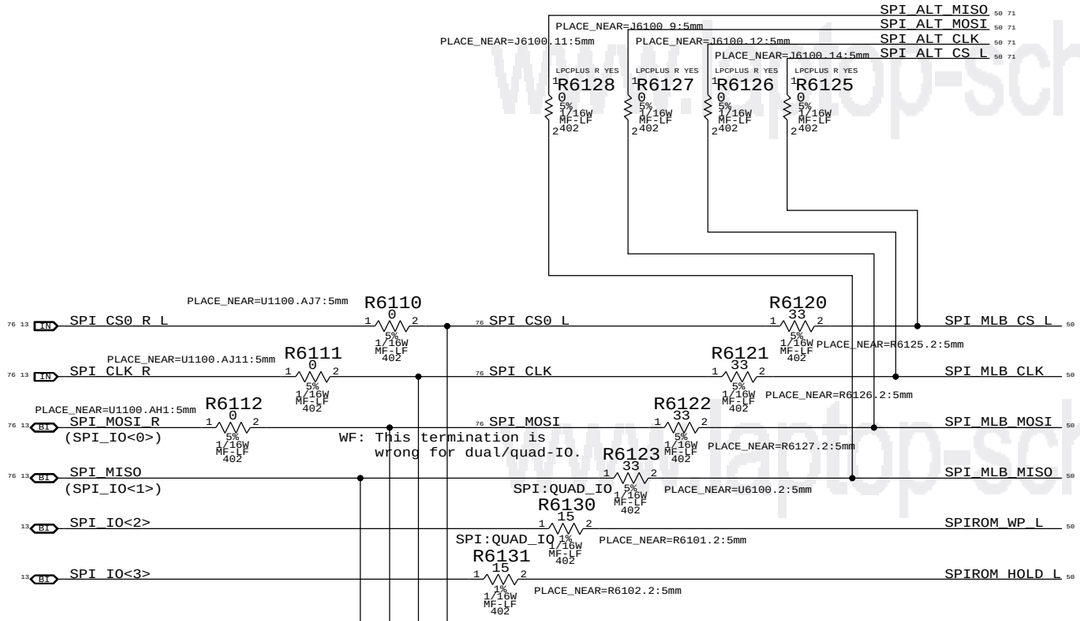
REVISION: <E4LABEL>

BRANCH: <BRANCH>

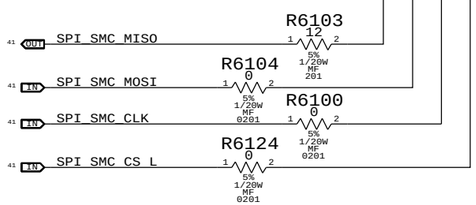
PAGE: 60 OF 118

SHEET: 49 OF 81

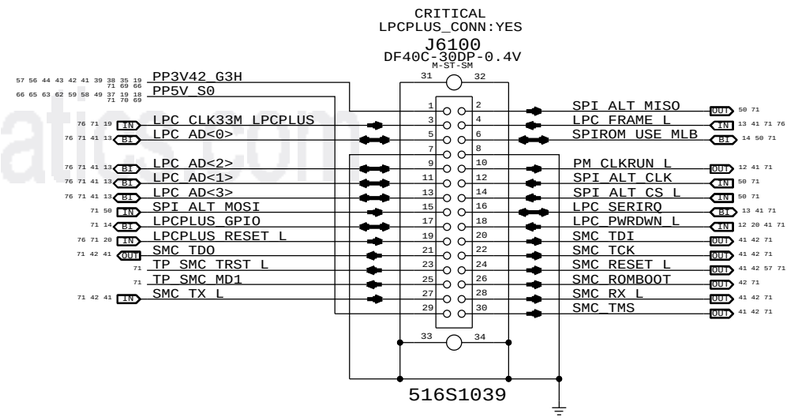
SPI Bus Series Termination



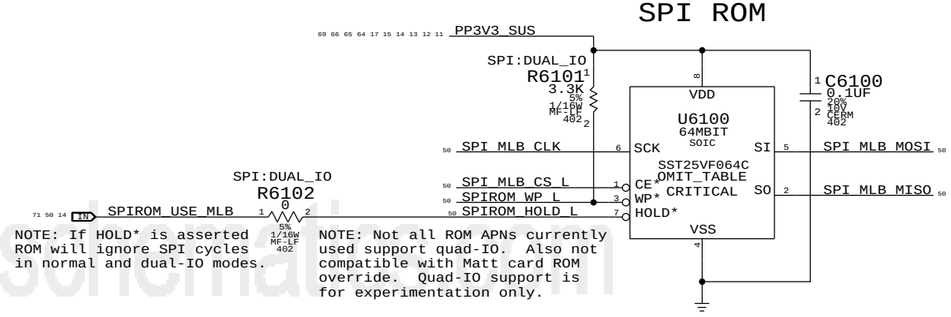
SMC12 SPI SUPPORT



LPC+SPI Connector



SPI ROM



NOTE: If HOLD* is asserted ROM will ignore SPI cycles in normal and dual-IO modes.

NOTE: Not all ROM APNs currently used support quad-IO. Also not compatible with Matt card ROM override. Quad-IO support is for experimentation only.

SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE: SPI ROM / LPC+SPI Conn.

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

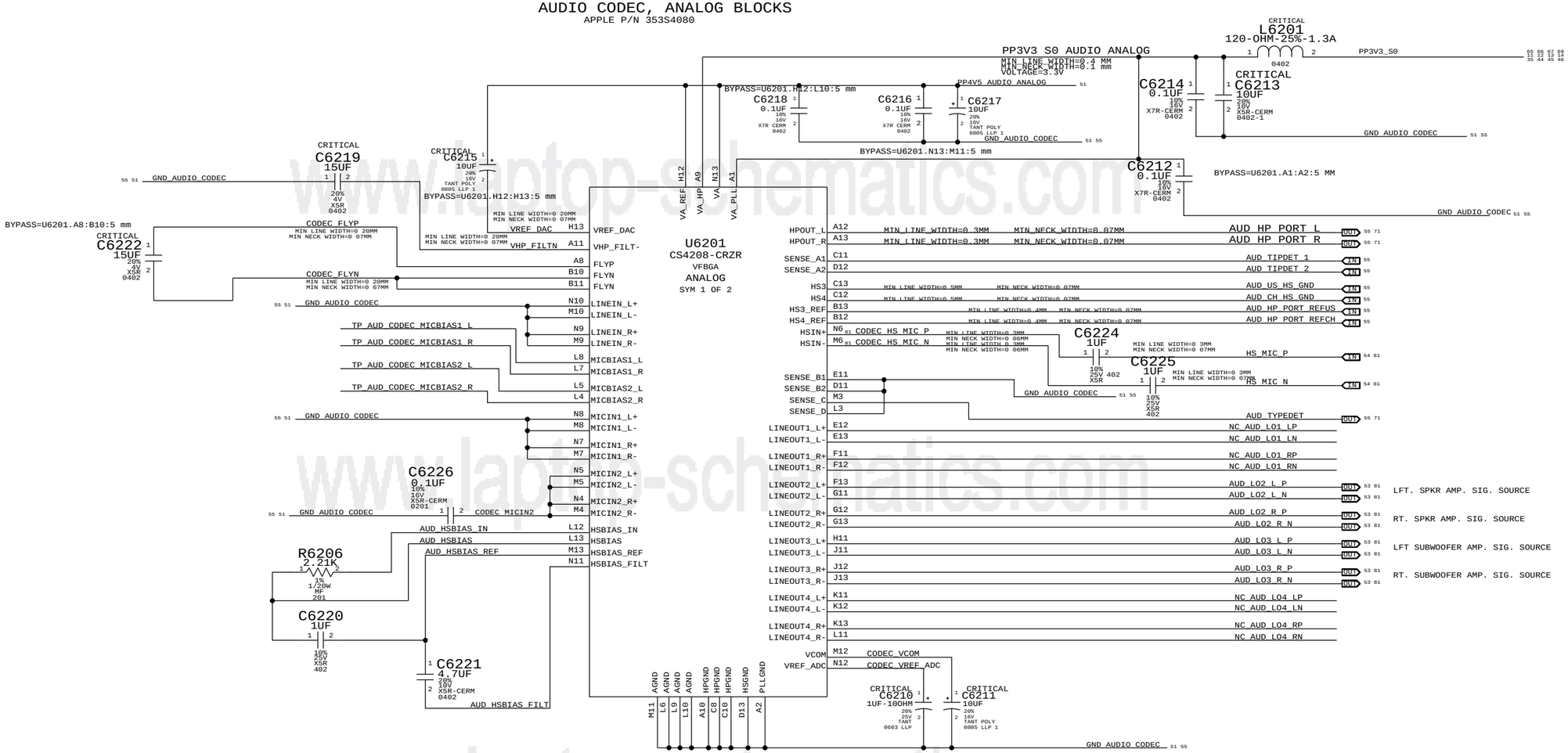
BRANCH: <BRANCH>

PAGE: 61 OF 118

SHEET: 50 OF 81

AUDIO CODEC, ANALOG BLOCKS

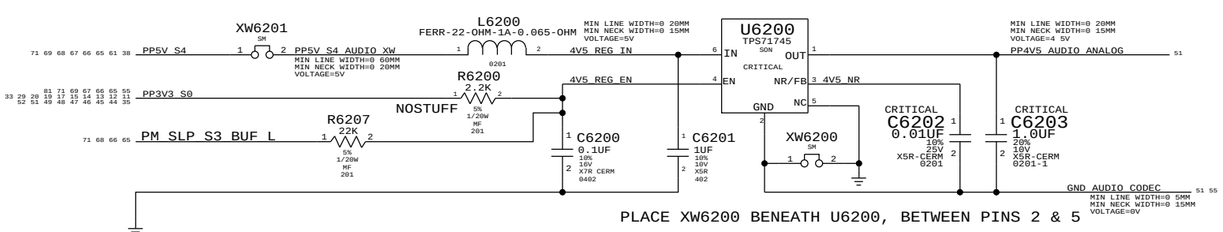
APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456

PLACE XW6201 NEAR 5V SOURCE



SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE: AUDIO:CODEC, ANALOG

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

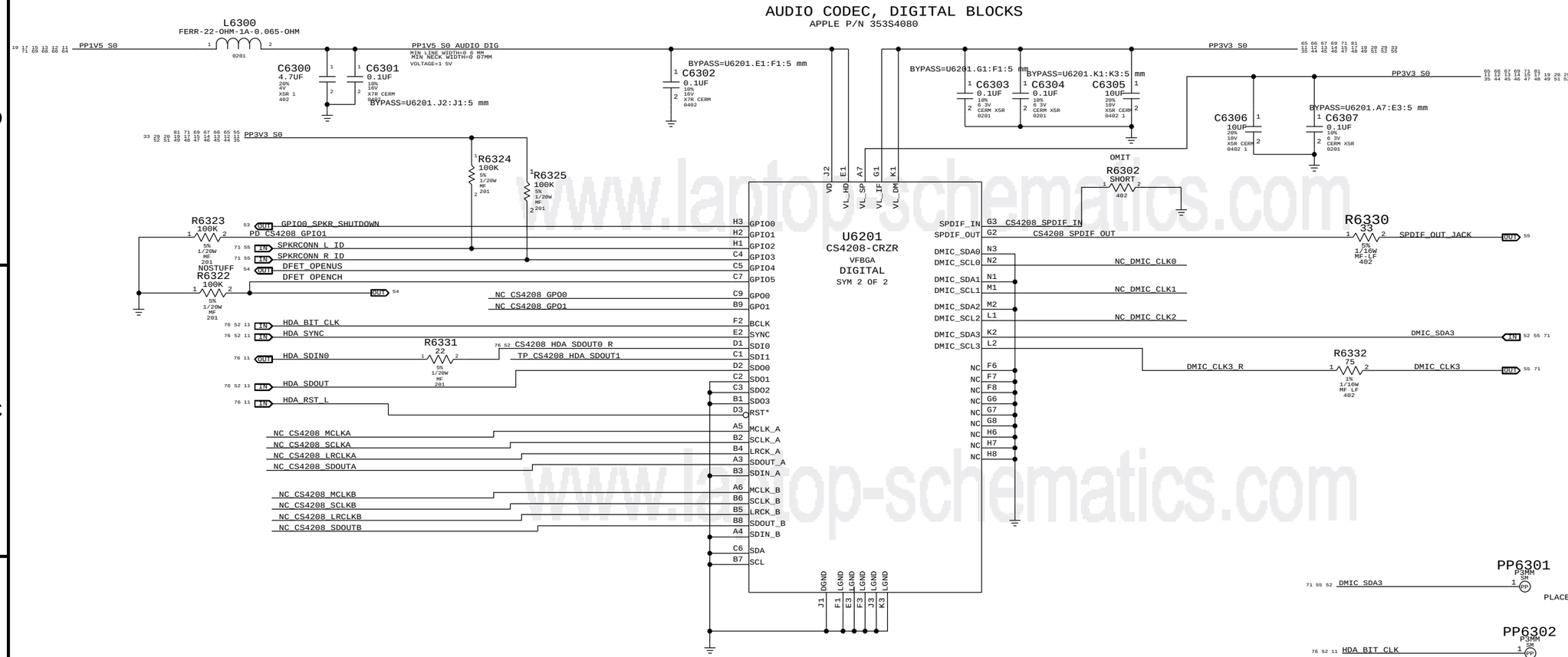
BRANCH: <BRANCH>

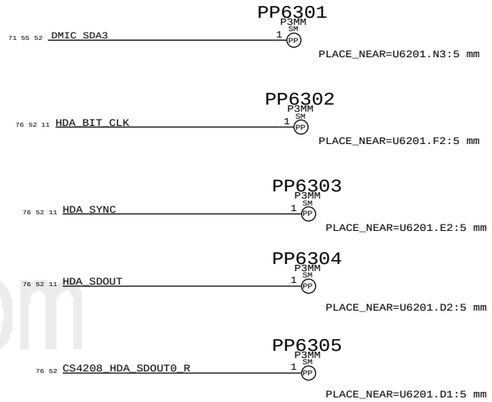
PAGE: 62 OF 118

SHEET: 51 OF 81

AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080





SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE: AUDIO:CODEC, DIGITAL

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

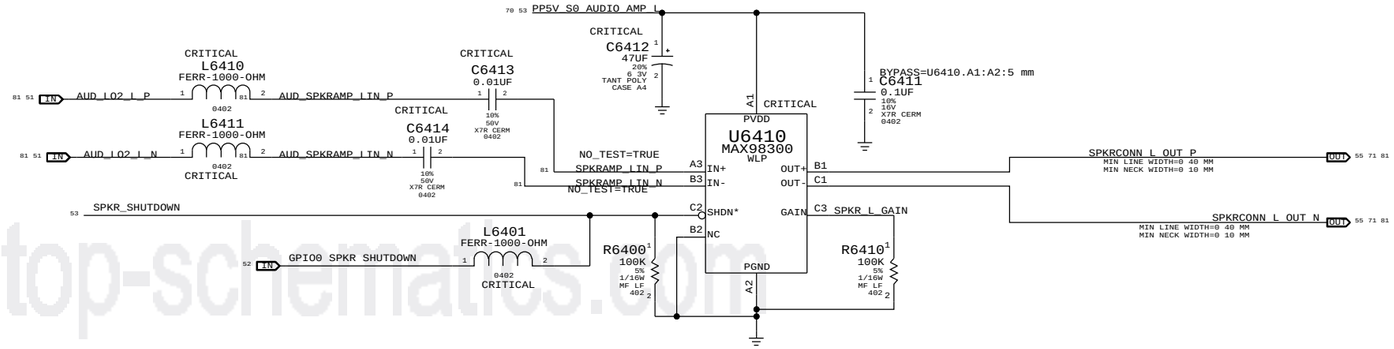
REVISION: <E4LABEL>

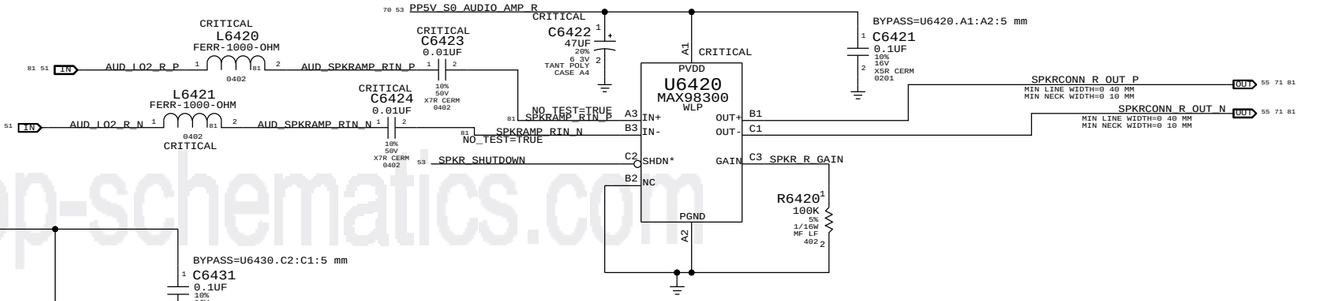
BRANCH: <BRANCH>

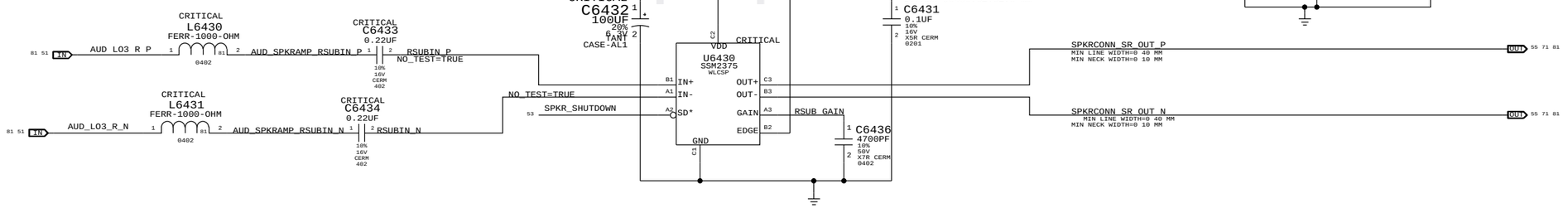
PAGE: 63 OF 118

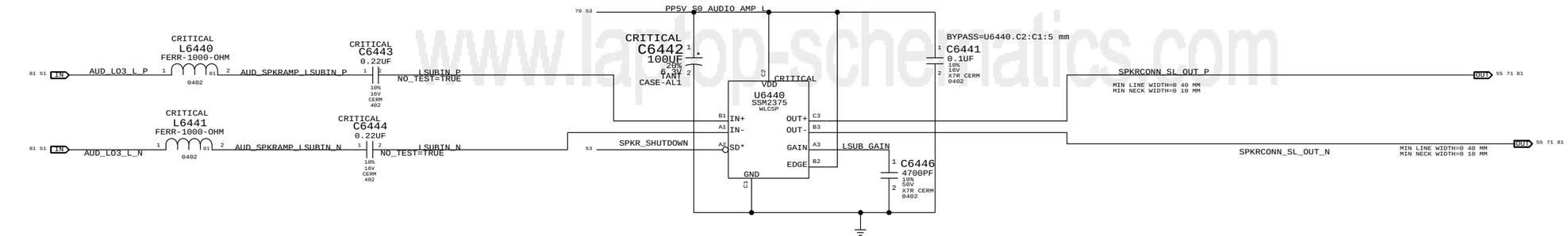
SHEET: 52 OF 81

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ







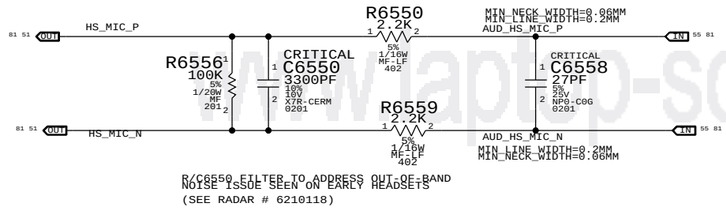


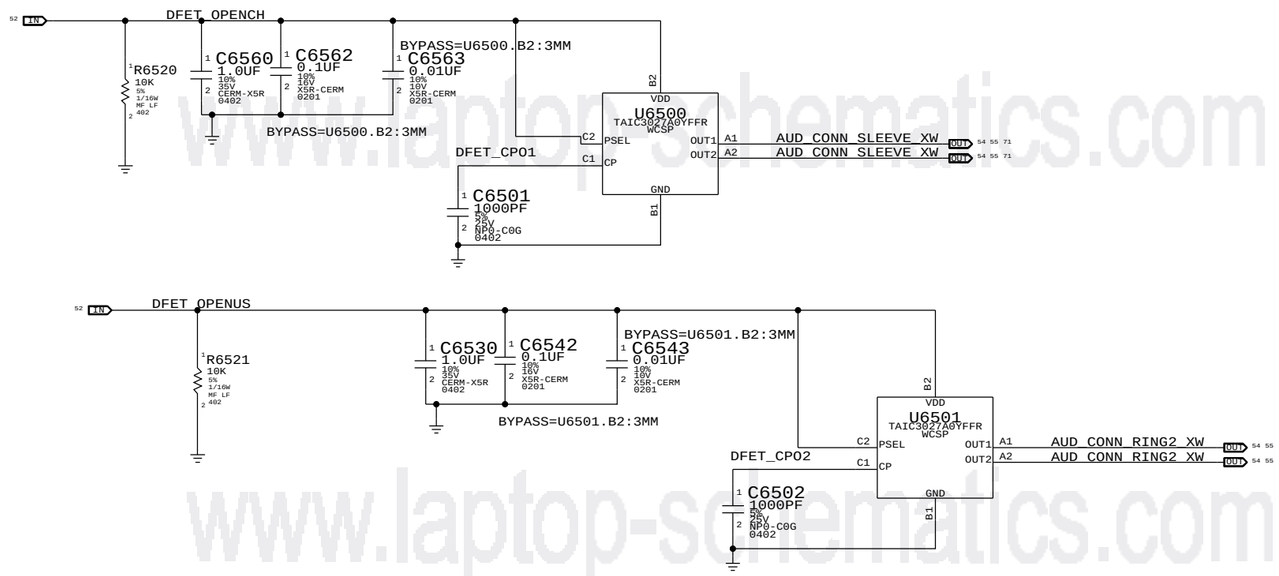
SYNC MASTER=JOE J45 SYNC DATE=07/30/2013

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 64 OF 118
SHEET 53 OF 81





SYNC MASTER=JOE J45 SYNC DATE=07/30/2013

PAGE TITLE

AUDIO: JACK

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 65 OF 118

SHEET 54 OF 81

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3 3V
DMIC 2	0X09 (9)	0X1C (28)	3 3V
HEADSET MIC	0X07 (7)	0X18 (24)	2 7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2 INPUT	HIGH = FG	LOW = MERRY
RIGHT SPEAKER ID	GPIO3 INPUT	HIGH = FG	LOW = MERRY
DFET CONTROL	GPIO4 OUTPUT	HIGH = DFETs OPEN	

2-MIC CONNECTOR
APN: 518S0769

J6601
FF14A-5C-R11DL-B-3H
F-RT-SM

PP3V3_S0
DMIC_SDA3
DMIC_CLK3
OMIT
R6680
SHORT
402
DMIC_SDA2

SPEAKER CONNECTOR HP=80HZ
APN: 518S0672

J6602
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
SPKRCONN_L_ID
SPKRCONN_SL_OUT_P
SPKRCONN_SL_OUT_N

J6603
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
SPKRCONN_R_ID
SPKRCONN_SR_OUT_P
SPKRCONN_SR_OUT_N

L6611 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_REFCH
AUD_CONN_SLEEVE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM

L6612 120-OHM-25%-1.3A 0402 CRITICAL
AUD_CH_HS_GND
AUD_CONN_SLEEVE_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM

XW6600 SM PLACE_NEAR=J6600.3:2.54mm
XW6601 SM
AUD_HS_MIC_P

L6613 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_REFUS
AUD_CONN_RING2
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM

L6614 120-OHM-25%-1.3A 0402 CRITICAL
AUD_US_HS_GND
AUD_CONN_RING2_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM

XW6602 SM PLACE_NEAR=J6600.5:2.54mm
XW6603 SM
AUD_HS_MIC_N

L6604 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_L
AUD_CONN_HP_LEFT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM

L6608 FERR-470-OHM 0201 CRITICAL
AUD_TIPDET_2
AUD_CONN_TIPDET_2

L6607 FERR-470-OHM 0201 CRITICAL
AUD_TIPDET_1
AUD_CONN_TIPDET_1

L6605 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_R
AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM

L6606 FERR-470-OHM 0201 CRITICAL
AUD_TYPEDET
AUD_CONN_TYPEDET

R6602 2.2K 5% 1/20W MF 201
R6603 2.2K 5% 1/20W MF 201
GND_AUDIO_CODEC
SPDIF_OUT_JACK

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH

MIC
AUDIO GND
2RTN
DET2
DET1
1RTN
R.AUDIO
AUDIO GND
AUDIO
NC

VIN
VDD
GND
OPERATING VOLTAGE 3.3
POF

SHELL PINS

C6600 1UF 10% 10V X5R 402-1
C6601 0.1UF 10% 6.3V CERM-X5R 0201

R6601 10K 5% 1/16W MF-LF 402

DZ6607 ESDALC5-1BM2 SOD882 CRITICAL
C6603 100PF 5% 25V NP0-CERM 0201
DZ6601 ESDALC5-1BM2 SOD882 CRITICAL
C6602 100PF 5% 25V NP0-CERM 0201
DZ6602 ESDALC5-1BM2 SOD882 CRITICAL
C6604 100PF 5% 25V NP0-CERM 0201
DZ6603 ESDALC5-1BM2 SOD882 CRITICAL
C6605 100PF 5% 25V NP0-CERM 0201
DZ6606 ESDALC5-1BM2 SOD882 CRITICAL
C6606 100PF 5% 25V NP0-CERM 0201
DZ6605 ESDALC5-1BM2 SOD882 CRITICAL
C6607 100PF 5% 25V NP0-CERM 0201
DZ6604 ESDALC5-1BM2 SOD882 CRITICAL
C6608 100PF 5% 25V NP0-CERM 0201

SYNC_MASTER=JOE J45 SYNC_DATE=07/30/2013
PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

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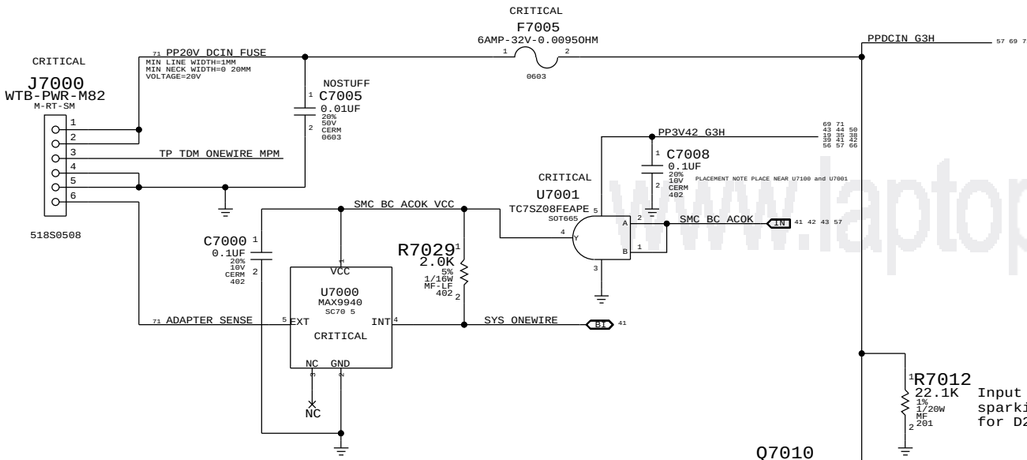
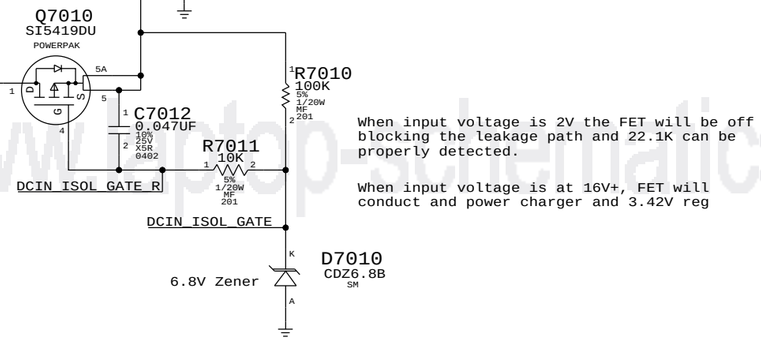
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 66 OF 118
SHEET 55 OF 81

MagSafe DC Power Jack



1-Wire OverVoltage Protection

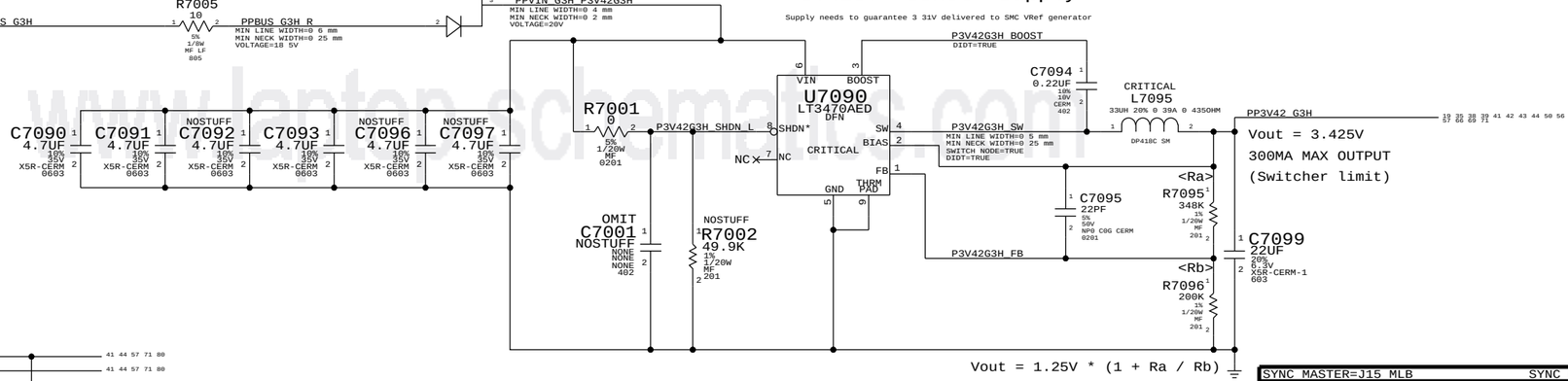
The chassis ground will otherwise float and can send transients onto ADAPTER SENSE when AC is connected



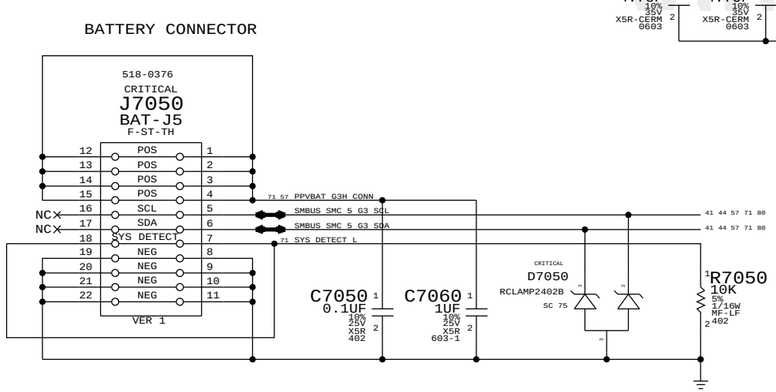
APN:353S3733

3.425V "G3Hot" Supply

Supply needs to guarantee 3 31V delivered to SMC VRef generator



BATTERY CONNECTOR

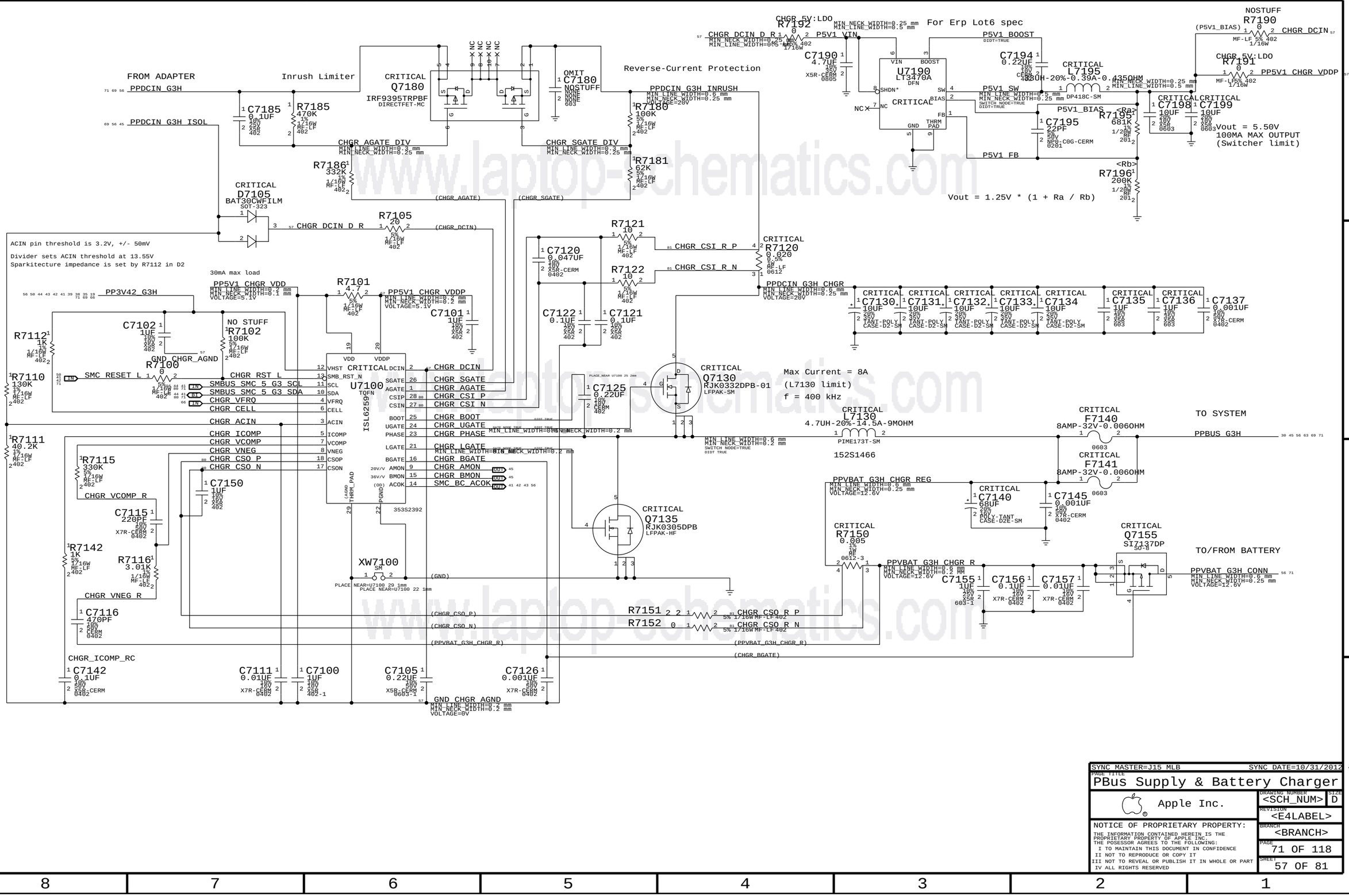


SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 70 OF 118
SHEET 56 OF 81



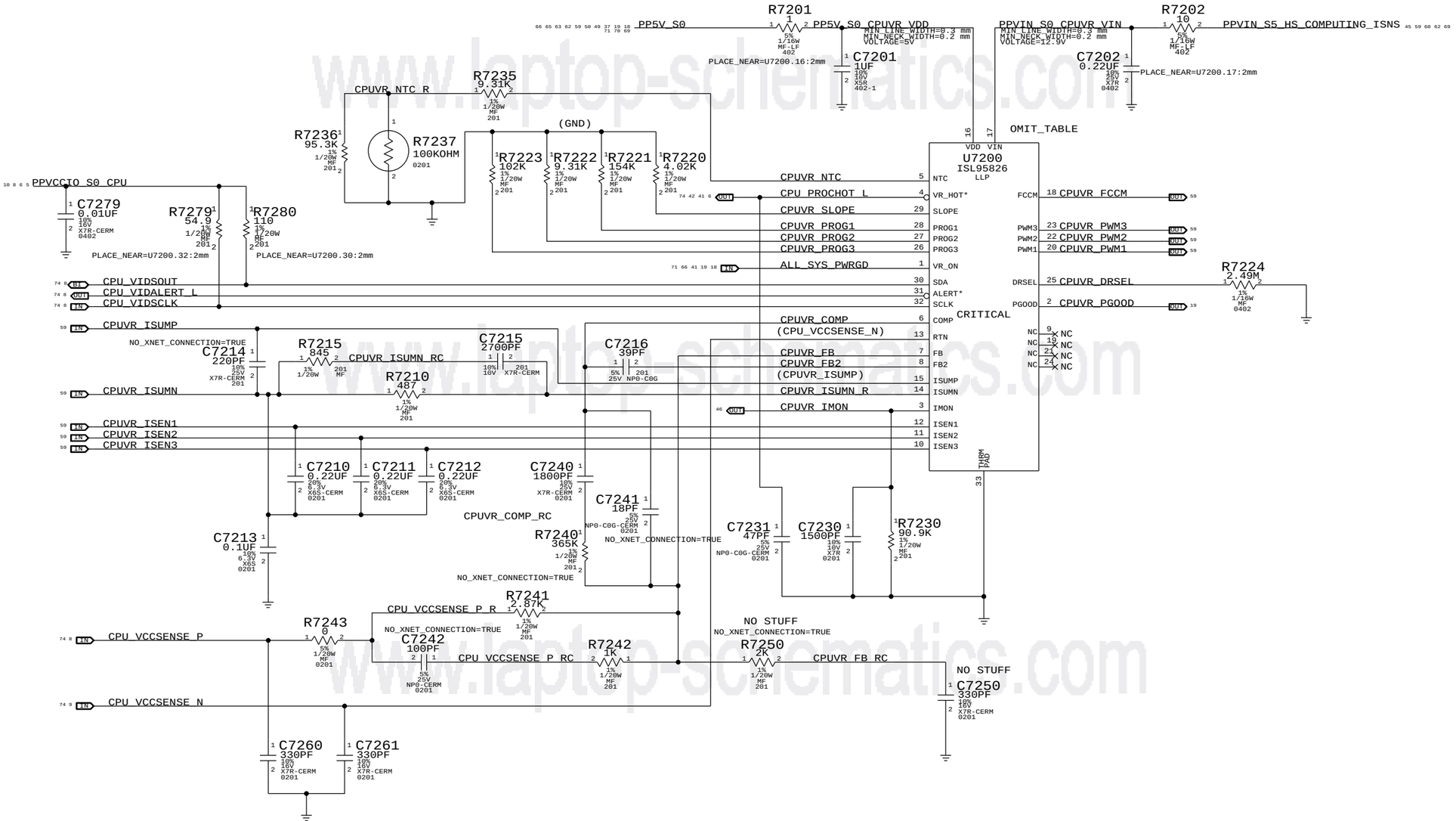
SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 71 OF 118
SHEET 57 OF 81

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC ISL95826R6200 PWM PGOOD SCREEN 32P QFN	U7200	CRITICAL	



SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE
CPU VR12.5 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 72 OF 118
SHEET 58 OF 81

PP5V_S0

PPVIN_S5_HS_COMPUTING_ISNS

PHASE 1

U7310 FDMF6808N PQFN CRITICAL 353S3836

R7311 0 5% 1/10W MF-LF 402 — CPUVR_BOOT1_RC — CPUVR_BOOT1

C7311 0.22UF 10% 16V CERM 402 — CPUVR_PHASE1_K

CPUVR_PWM1

CPUVR_FCCM

C7310 1UF 10% 16V X6S CERM 0402

L7310 0.36UH-20%-36A-0.001080HM CRITICAL — PIMS103T-SM 152S1538

CPUVR_PHASE1 — MIN_LINE_WIDTH=1.5 MM — MIN_NECK_WIDTH=0.2 MM — DIDT=TRUE — SWITCH NODE=TRUE

PPVCC_S0_CPU_PH1 — MIN_LINE_WIDTH=0.6 MM — MIN_NECK_WIDTH=0.25 MM — VOLTAGE=1.8V

R7310 0.00075 1% 1W MF 0612 CRITICAL

R7312 2.2 5% 1/10W MF LF 603 NOSTUFF — CPUVR_PH1_SNUB — C7312 0.001UF 10% 50V X7R CERM 0402 DIDT=TRUE NOSTUFF

CPUVR_ISNS1_P — CPUVR_ISNS1_N

R7314 3.9 1% 1/20W MF 201

R7315 1K 1% 1/20W MF 201

R7316 10K 1% 1/20W MF 201 — CPUVR_ISUMN — NO_XNET_CONNECTION=TRUE

CPUVR_ISEN1

CPUVR_ISUMP

R7317 10K 1% 1/20W MF 201 — CPUVR_ISNS2_N — NO_XNET_CONNECTION=TRUE

R7318 10K 1% 1/20W MF 201 — CPUVR_ISNS3_N — NO_XNET_CONNECTION=TRUE

C7313 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7314 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7315 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL

C7316 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL

C7317 1UF 10% 16V X6S CERM 0402

C7318 0.001UF 10% 50V X7R CERM 0402 THESE TWO CAPS ARE FOR EMC

C7319 0.001UF 10% 50V X7R CERM 0402

Additonal Input Bulk Caps

C7370 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7371 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7372 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7373 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7374 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7375 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7376 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7377 15UF 20% 16V TANT SM CRITICAL

C7378 15UF 20% 16V TANT SM CRITICAL

C7379 15UF 20% 16V TANT SM CRITICAL

C7380 15UF 20% 16V TANT SM CRITICAL

C7381 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7382 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7383 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7384 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

PHASE 2

U7320 FDMF6808N PQFN CRITICAL 353S3836

R7321 0 5% 1/10W MF-LF 402 — CPUVR_BOOT2_RC — CPUVR_BOOT2

C7321 0.22UF 10% 16V CERM 402 — CPUVR_PHASE2_K

CPUVR_PWM2

CPUVR_FCCM

C7320 1UF 10% 16V X6S CERM 0402

L7320 0.36UH-20%-36A-0.001080HM CRITICAL — PIMS103T-SM 152S1538

CPUVR_PHASE2 — MIN_LINE_WIDTH=1.5 MM — MIN_NECK_WIDTH=0.2 MM — DIDT=TRUE — SWITCH NODE=TRUE

PPVCC_S0_CPU_PH2 — MIN_LINE_WIDTH=0.6 MM — MIN_NECK_WIDTH=0.25 MM — VOLTAGE=1.8V

R7320 0.00075 1% 1W MF 0612 CRITICAL

R7322 2.2 5% 1/10W MF LF 603 NOSTUFF — CPUVR_PH2_SNUB — C7322 0.001UF 10% 50V X7R CERM 0402 DIDT=TRUE NOSTUFF

CPUVR_ISNS2_P — CPUVR_ISNS2_N

R7324 3.9 1% 1/20W MF 201

R7325 1K 1% 1/20W MF 201

R7326 10K 1% 1/20W MF 201 — CPUVR_ISUMN — NO_XNET_CONNECTION=TRUE

CPUVR_ISEN2

CPUVR_ISUMP

R7327 10K 1% 1/20W MF 201 — CPUVR_ISNS1_N — NO_XNET_CONNECTION=TRUE

R7328 10K 1% 1/20W MF 201 — CPUVR_ISNS3_N — NO_XNET_CONNECTION=TRUE

C7323 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7324 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7325 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL

C7326 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL

C7327 1UF 10% 16V X6S CERM 0402

C7328 0.001UF 10% 50V X7R CERM 0402 THESE TWO CAPS ARE FOR EMC

C7329 0.001UF 10% 50V X7R CERM 0402

PHASE 3

U7330 FDMF6808N PQFN CRITICAL 353S3836

R7331 0 5% 1/10W MF-LF 402 — CPUVR_BOOT3_RC — CPUVR_BOOT3

C7331 0.22UF 10% 16V CERM 402 — CPUVR_PHASE3_K

CPUVR_PWM3

CPUVR_FCCM

C7330 1UF 10% 16V X6S CERM 0402

L7330 0.36UH-20%-36A-0.001080HM CRITICAL — PIMS103T-SM 152S1538

CPUVR_PHASE3 — MIN_LINE_WIDTH=1.5 MM — MIN_NECK_WIDTH=0.2 MM — DIDT=TRUE — SWITCH NODE=TRUE

PPVCC_S0_CPU_PH3 — MIN_LINE_WIDTH=0.6 MM — MIN_NECK_WIDTH=0.25 MM — VOLTAGE=1.8V

R7330 0.00075 1% 1W MF 0612 CRITICAL

R7332 2.2 5% 1/10W MF LF 603 NOSTUFF — CPUVR_PH3_SNUB — C7332 0.001UF 10% 50V X7R CERM 0402 DIDT=TRUE NOSTUFF

CPUVR_ISNS3_P — CPUVR_ISNS3_N

R7334 3.9 1% 1/20W MF 201

R7335 1K 1% 1/20W MF 201

R7336 10K 1% 1/20W MF 201 — CPUVR_ISUMN — NO_XNET_CONNECTION=TRUE

CPUVR_ISEN3

CPUVR_ISUMP

R7337 10K 1% 1/20W MF 201 — CPUVR_ISNS1_N — NO_XNET_CONNECTION=TRUE

R7338 10K 1% 1/20W MF 201 — CPUVR_ISNS2_N — NO_XNET_CONNECTION=TRUE

C7333 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7334 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

C7335 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL

C7336 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL

C7337 1UF 10% 16V X6S CERM 0402

C7338 0.001UF 10% 50V X7R CERM 0402 THESE TWO CAPS ARE FOR EMC

C7339 0.001UF 10% 50V X7R CERM 0402

PPVCC_S0_CPU

Vout = 1.85V max
95A max output
f = 450 kHz

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: CPU VR12.5 VCC Power Stage

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

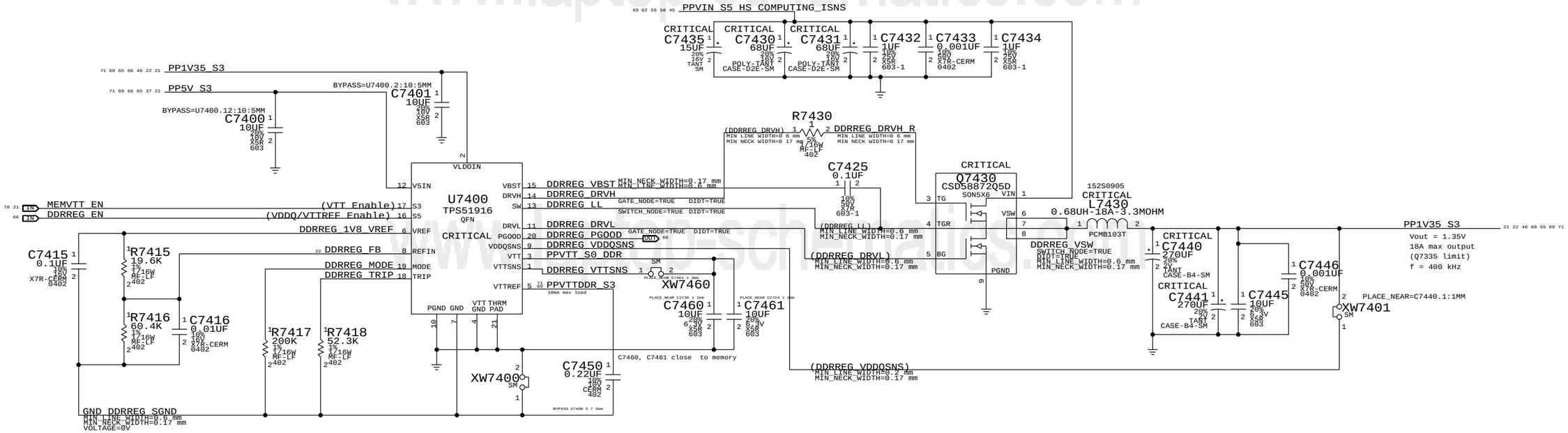
REVISION: <E4LABEL>

BRANCH: <BRANCH>

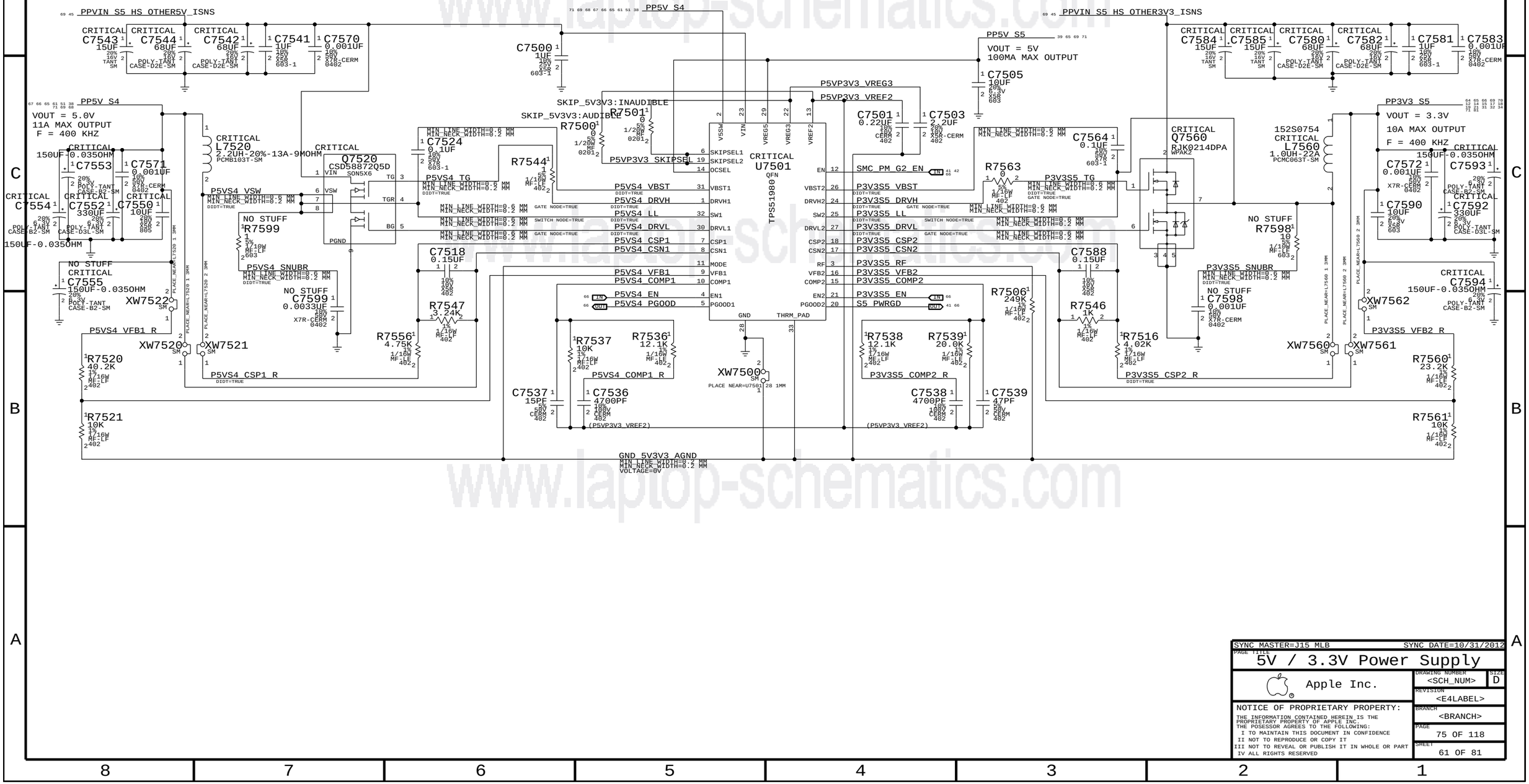
PAGE: 73 OF 118

SHEET: 59 OF 81

DDR3L (1V35 S3) REGULATOR



SYNC MASTER=J15 MLB	SYNC DATE=10/31/2012
PAGE TITLE	1.35V DDR3L SUPPLY
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 74 OF 118
	SHEET 60 OF 81



SYNC MASTER=J15 MLB	SYNC DATE=10/31/2012
PAGE TITLE: 5V / 3.3V Power Supply	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
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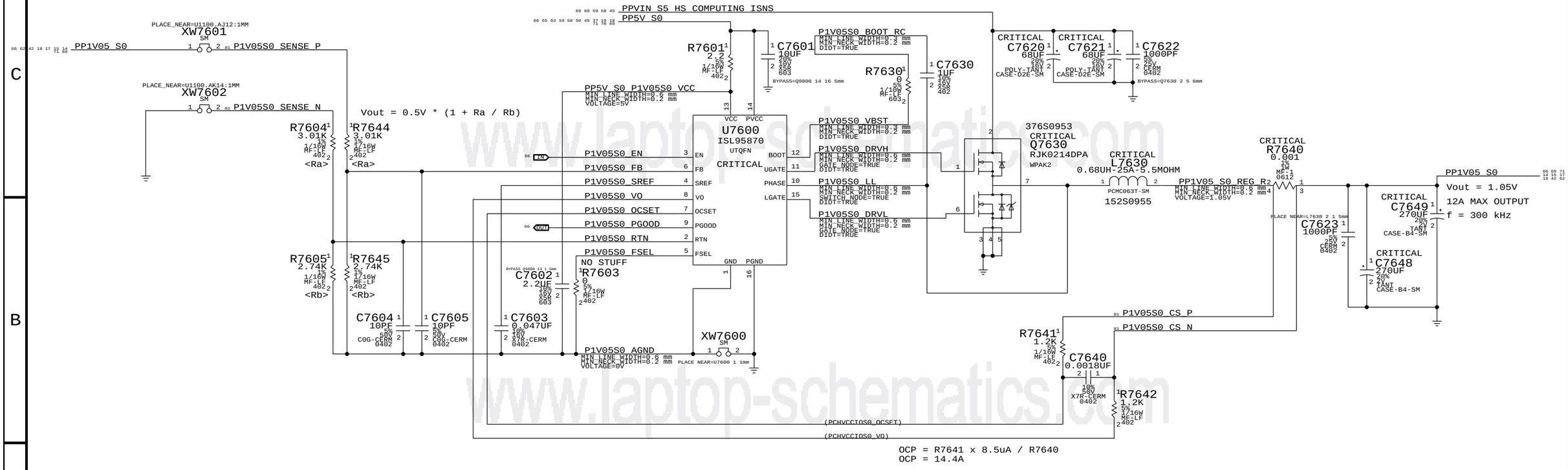
1V05 S0 REGULATOR



SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE
1V05V POWER SUPPLY

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 76 OF 118
SHEET 62 OF 81

Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	8	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7717 R7718 R7719 R7720 R7721 R7722 R7723 R7724		BKLT:PROD

PPBUS_G3H → CRITICAL F7700 3AMP-32V-467 (603-HF) → PPBUS_S0_LCDBKLT_FUSED → R7700 0.025 1% 1W MTL 0612 → PPBUS_SW_LCDBKLT_PWR

CRITICAL Q7706 FDC638APZ SBMS001 (SSOT6-HF)

PPBUS_SW_BKL → C7700 1000PF → R7701 80.6K → ISNS_LCDBKLT_P / ISNS_LCDBKLT_N

NOSTUFF C7701 0.001UF

152S1527 CRITICAL L7710 22UH-20%-2.4A-0.105OHM (DEM8030C-SM)

PPBUS_S0_LCDBKLT_PWR_SW → C7710 4.7UF, C7711 4.7UF, C7712 0.1UF

CRITICAL D7701 POWERDI-123 (DFLS2100)

PPBUS S0 LCDBKLT PWR SW SHOULD BE KEPT AS SHORT AS POSSIBLE

C7715 C7716 SHOULD BE PLACED MIRRORED C7718 C7719 SHOULD BE PLACED MIRRORED

CRITICAL C7715 2.2UF, C7716 2.2UF, C7718 2.2UF, C7719 2.2UF, C7717 1000PF

PPVOUT_S0_LCDBKLT

PLACE_NEAR=L7710 2 3MM

PLACE_NEAR=D7701.K:3MM PLACE_NEAR=D7701.K:3MM PLACE_NEAR=R7708.1:5MM
PLACE_NEAR=D7701.K:5MM PLACE_NEAR=D7701.K:5MM

PLACE_NEAR=L7710.2:3MM

CRITICAL Q7701 SI7812DN (PWRPK-1212-8)

BKL_FET_CNTL_R → R7703 0 → BKL_FET_CNTL

R7708 18.2K, R7709 150K

PP5V_S0 → R7743 0, R7744 0

PP5V_S0_BKLT_VDDA / PP5V_S0_BKLT_VDDD

R7702 63.4K

C7740 1UF, C7741 1UF

GND_BKLT_SGND

R7740 1M

U7701 LLP LP8548B1SQ-03

BKL_SW → BKL_FB

BKLT_SD
(PPBUS_S0_BKLT_PWR_R)
(PPBUS_S0_BKLT_PWR_F)
BKLT_SENSE_OUT
BKLT_EN_R
BKLT_ISET_KEYB

R7742 0 ← EDP_IG_BKL_ON → NO STUFF C7742 33PF

R7747 0 ← SMC_SYS_KBDLED → NO STUFF C7747 33PF

BKLT:ENG R7723 10.2 → KBDBKLT_RETURN1
BKLT:ENG R7724 10.2 → KBDBKLT_RETURN2

R7741 31.6K → PPVOUT_BKLT_FB

CRITICAL 353S4159 (SSOT-24)

XW7700 SM

KBDBKLT_SW

GND_BKLT_SGND

R7757 0 BKLT_SDA

R7758 0 BKLT_SCL

U7750 LLP LP8549B1SP-03

LCD_FSS, EDP_IG_BKL_PWM, SMBUS_PCH_DATA, SMBUS_PCH_CLK

BKLT_SYNC, LCD_BKLT_PWM_R, BKL_1_EN_R_JERRY, BKL_1_SDA, BKL_1_SCL, BKLT_ISET_LCD

R7780 0, R7781 0, R7782 0

CRITICAL APN353S4229

R7754 27.4K, R7756 10K

XW7701 SM

GND_LCDBKLT_SGND

BKL_ISEN1 → LED_RETURN_1
BKL_ISEN2 → LED_RETURN_2
BKL_ISEN3 → LED_RETURN_3
BKL_ISEN4 → LED_RETURN_4
BKL_ISEN5 → LED_RETURN_5
BKL_ISEN6 → LED_RETURN_6

R7717 10.2, R7718 10.2, R7719 10.2, R7720 10.2, R7721 10.2, R7722 10.2

R7783 0 ← PP5V_S0

152S1701 CRITICAL L7720 10UH-20%-1.4A-0.17OHM (PST041H-CDH46D14-SM)

C7720 2.2UF, C7721 2.2UF, C7722 0.1UF

C7720 C7721 SHOULD BE PLACED MIRRORED

371S0572 CRITICAL D7720 SOD-123 (RB160M-60G)

XW7720 SM

C7726 1.0UF, C7727 1.0UF, C7723 1.0UF, C7724 1.0UF, C7725 0.001UF

C7723 C7724 SHOULD BE PLACED MIRRORED

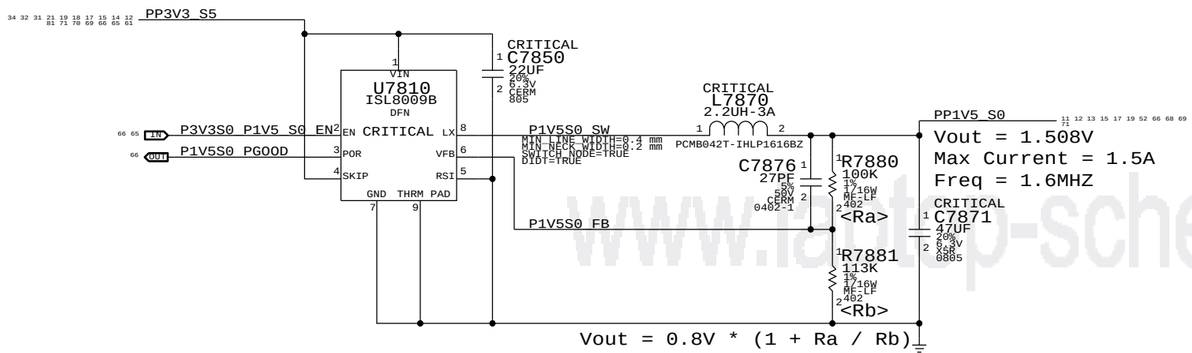
PPVOUT_S0_KBDBKLT

R7760 4.7K, R7761 4.7K

BKLT_SCL_R, BKLT_SDA_R

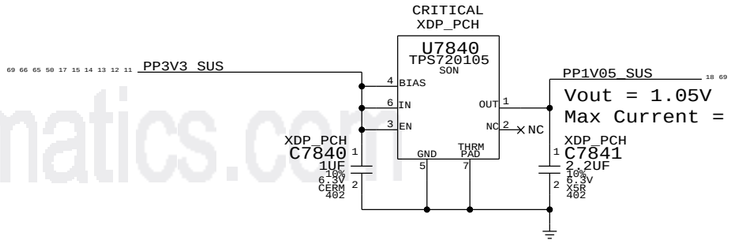
SYNC_MASTER=CLEAN_MLB_KEPLER	SYNC_DATE=06/13/2013
PAGE TITLE	LCD/KBD Backlight Driver
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 77 OF 118
	SHEET 63 OF 81

1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 78 OF 118

SHEET: 64 OF 81

3.3V S4 FET

376S0945
CRITICAL
Q8000
SIA413DJ
SC70-6L

EDP is per J45 Power Budget rev5

PP3V3_S5 → R8002 220K → P3V3S4_EN_L → R8000 47K → P3V3S3_S4
C8009 0.033UF (P3V3S4_EN_L)
C8000 0.01UF (P3V3S3_S4)
Q8002 DMN5L06VK-7 SOT-563 (D 6, G 2, S 1)
EN ← S4_PWR_EN
PP3V3_S4 → C8000 0.01UF

3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

3.3V S3 FET

CRITICAL
Q8010
SIA413DJ
SC70-6L

PP3V3_S5 → R8012 47K → P3V3S3_EN_L → R8010 39K → P3V3S3_SS
C8011 0.033UF (P3V3S3_EN_L)
C8010 0.01UF (P3V3S3_SS)
Q8012 DMN32D2LFB4 DFN1006H4-3 SYM VER 2 (D 3, G 1, S 2)
EN ← P3V3S3_EN
PP3V3_S3 → C8010 0.01UF

SSD_PWR_EN:GPIO
SSD_PWR_EN ← R8073 0 0201 1/20W 5% MF ← SSD_PWR_EN
SSD_PWR_EN → R8074 0 0201 1/20W 5% MF → SSD_PWR_FET_EN
PM_SLP_S3_BUF_L → Q8072 DMN32D2LFB4 DFN1006H4-3 SYM VER 2 (D 3, G 1, S 2)

3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

5V S3 FET

CRITICAL
Q8050
SIA427DJ
SC70-6L

PP5V_S4 → R8052 200K → P5VS3_EN_L → R8050 5.1K → P5VS3_SS
C8051 0.033UF (P5VS3_EN_L)
C8050 0.01UF (P5VS3_SS)
Q8052 DMN5L06VK-7 SOT-563 (D 6, G 2, S 1)
EN ← P5VS3_EN
PP5V_S3 → C8050 0.01UF

5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

1.35V S3/S0 FET

PP5V_S5 → C8001 0.1UF → U8001 SLG5AP1438V TDFN CRITICAL (VDD 1, CAP 7, ON 2, GND 8, D 3, S 5)
C8002 0.018UF (GND)
P1V35CPU_SLEW_CTL → CAP
CPUVDDQ_EN ← EN ← ON
Slew rate : 0.8V/ms = 19.75nF
PP1V35_S3 ← D, S
PP1V35_S3RS0_FET → XW8005 SM → PP1V35_S3RS0_CPUDDR
NC_ISNS_CPUDDRN (DIFF)
NC_ISNS_CPUDDRP (DIFF)

1.35V S3/S0 FET	
Integ. MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

SENSOR_NONPROD_R

3.3V SUS FET

CRITICAL
Q8020
SIA413DJ
SC70-6L

PP3V3_S5 → R8022 100K → P3V3SUS_EN → R8020 12K → P3V3SUS_SS
C8021 0.033UF (P3V3SUS_EN)
C8020 0.01UF (P3V3SUS_SS)
Q8002 DMN5L06VK-7 SOT-563 (D 3, G 5, S 4)
EN ← PM_SLP_SUS
PP3V3_SUS → C8020 0.01UF

3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

3.3V S0 SSD FET

PLACE_NEAR=R5549.2:6mm

CRITICAL
Q8070
SI7615DN
PWRPK 1212 8

PP3V3_S5 → R8072 47K → P3V3_SSD_EN_L → R8070 33K → P3V3_SSD_SS
C8071 0.033UF (P3V3_SSD_EN_L)
C8070 0.01UF (P3V3_SSD_SS)
Q8072 DMN32D2LFB4 DFN1006H4-3 SYM VER 2 (D 3, G 1, S 2)
SSD_PWR_FET_EN
PP3V3_S0SW_SSD_R

3.3V S0 SSD FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET

CRITICAL
Q8060
SI7615DN
PWRPK 1212 8

PP5V_S4 → R8062 270K → P5V0S0_EN_L → R8060 6.2K → P5V0S0_SS
C8061 0.12UF (P5V0S0_EN_L)
C8060 0.47UF (P5V0S0_SS)
Q8052 DMN5L06VK-7 SOT-563 (D 3, G 5, S 4)
EN ← P5VS0_EN
PP5V_S0

5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

3.3V S0 Switch

U8030
TPS22924
CSP
CRITICAL
APN 353S2741

PP3V3_S5 → A2 VIN, B2 VIN
P3V3S0_P1V5_S0_EN ← EN ← C2 ON
A1 VOUT, B1 VOUT → PP3V3_S0
Max Current = 2A
GND
C8030 1UF

U8030	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 80 OF 118
SHEET: 65 OF 81

Power State Debug LEDs
(For development only)

PP3V3_S5 → R8194 0 (5% 1/16W MF-LF 402) → DBGLED (PLACE_SIDE=BOTTOM, PP3V3_S5_DBGLED: MIN_NECK_WIDTH=0.1 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=3.3V)

DBGLED_S5	DBGLED_S4	DBGLED_S3	DBGLED_S0
R8190 20K (5% 1/20W MF 201)	R8191 20K	R8192 20K	R8193 20K
D8190	D8191	D8192	D8193
GREEN-56MCD-2MA-2.65V LTQH9G-SM (PLACE_SIDE=BOTTOM, SILK_PART=S5_ON)	GREEN-56MCD-2MA-2.65V LTQH9G-SM (PLACE_SIDE=BOTTOM, SILK_PART=S4_ON)	GREEN-56MCD-2MA-2.65V LTQH9G-SM (PLACE_SIDE=BOTTOM, SILK_PART=S3_ON)	GREEN-56MCD-2MA-2.65V LTQH9G-SM (PLACE_SIDE=BOTTOM, SILK_PART=S0_ON)
DBGLED_S4_D	DBGLED_S3_D	DBGLED_S0_D	
Q8190 DMN5L06VK-7 SOT-563	Q8190 DMN5L06VK-7 SOT-563	Q8191 DMN32D2LFB4 DFN1006H4-3 SYM VER 2	

S4_PWR_EN, PM_SLP_S4_L, PM_SLP_S3_BUF_L

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

S4 Power Enable

PP3V3_S5 → C8170 0.1uF (20% 10V CERM 402) → PM_SLP_S5_L (PM SLP S5 L 100K pull down on PCH page) → U8170 74LVC1G32 SOT891 (SMC_S4_WAKESRC_EN, NC)

S4_PWR_EN (MAKE_BASE=TRUE) → D8174 (SOD-523 BAT54XV2T1) → R8174 43K (5% 1/16W MF-LF 402) → P5VS4_EN (MAKE_BASE=TRUE)

P5VS4_EN_D → R8175 240 (5% 1/10W MF-LF 402) → C8174 2.2UF (10% 6.3V X5R 402)

S4_PWR_EN (OUT) ×3

S3 ENABLE

PM_SLP_S4_L (IN) — PM SLP S4 L 100K pull down in PCH page

R8111 5.1K (5% 1/16W MF-LF 402)	R8112 0 (5% 1/16W MF-LF 402)	R8113 0 (5% 1/16W MF-LF 402)	R8114 3.3K (5% 1/20W MF 201)
C8110 0.47UF (10% 6.3V CERM-X5R 402)	C8112 0.47UF (10% 6.3V CERM-X5R 402)	C8113 0.47UF (10% 6.3V CERM-X5R 402)	C8114 0.47UF (10% 6.3V CERM-X5R 402)
	NO STUFF	NO STUFF	NO STUFF

TPAD_VBUS_EN (OUT)
P5VS3_EN — P5VS3_EN (MAKE_BASE=TRUE) (OUT)
P3V3S3_EN — P3V3S3_EN (MAKE_BASE=TRUE) (OUT)
DDRREG_EN — DDRREG_EN (MAKE_BASE=TRUE) (OUT)

CPUVCORE ENABLE

ALL_SYS_PWRGD — ALL_SYS_PWRGD (MAKE_BASE=TRUE) (OUT)

S0 ENABLE

PP3V3_S5 → C8180 0.1uF (20% 10V CERM 402) → U8180 MC74VHC1G08 SC70-HF

PM_SLP_S3_L (IN) → R8178 100 (5% 1/16W MF-LF 402) → PM_SLP_S3_R_L (MAKE_BASE=TRUE)
PM SLP S3 L 100K pull down in PCH page

(PM_SLP_S3_BUF_L) → NO STUFF R8180 100K (5% 1/16W MF-LF 402) → D8185 (SOD-523 BAT54XV2T1)

P1V05_EN_D → R8138 820 (5% 1/10W MF-LF 402)

D8185 → R8185 130K (5% 1/16W MF-LF 402) → C8185 0.82UF (10% 6.3V X5R 402)

PM_SLP_S3_BUF_L (OUT)
R8186 20K (5% 1/16W MF-LF 402) → C8186 0.68UF (10% 6.3V CERM 402)
R8187 0 (5% 1/16W MF-LF 402) → C8187 0.68UF (10% 6.3V CERM 402) NO STUFF

MAKE_BASE=TRUE
P5VS0_EN — P5VS0_EN (OUT)
P3V3S0_P1V5_S0_EN — P3V3S0_P1V5_S0_EN (OUT)
P3V3S0_P1V5_S0_EN — P1V05S0_EN (OUT)
P1V05S0_EN (MAKE_BASE=TRUE)

PM_SLP_S3_R_L (OUT) ×2

3.3V SUS Enable

PM_SLP_SUS_L (IN) — PM_SLP_SUS_L (MAKE_BASE=TRUE) (OUT) ×2

PM_SLP_SUS_L: 100K pull down on PCH page

S0 Rail PGOOD (BJT Version)

PP5V_S0 → R8151 54.9K (1% 1/16W MF-LF 402) → VMON_5V_DIV
5.0V Divider:1.07V
R8152 15.0K (1% 1/16W MF-LF 402)

PP3V3_S5 → R8156 150K (1% 1/16W MF-LF 402) → S0PGD_C

ALL_SYS_PWRGD

R8153 1K (5% 1/16W MF-LF 402) → VMON_Q2_BASE
R8154 1K → VMON_Q3_BASE
R8155 1K → VMON_Q4_BASE

Q8150 (ASMCC0179, DFN2015H4-8, 353S2809): Q1, Q2, Q3 CRITICAL, Q4

PP1V35_S3RS0_CPUDDR
PP3V3_S0
VMON_3V_DIV
3V3 Divider:1.07V
R8158 15.0K (1% 1/16W MF-LF 402)
R8159 7.15K (1% 1/16W MF-LF 402)

S0PGD_BJT_GND_R
R8157 100 (5% 1/16W MF-LF 402)

Vbe 0.7V max @2mA
Vce(sat) 0.1V max @1mA
Q1 Vth 0.7~1V @Id 250uA

3.3V SUS Detect

PP3V3_S5 → C8130 0.1uF (20% 10V CERM 402)

PP3V3_SUS → R8133 100K (5% 1/16W MF-LF 402)

U8130 TPS3808G33DBVRG4 SOT23 6 (CRITICAL)
SENSE, VDD, RESET* → PM_RSMRST_L (PM RSMRST L goes to U1100 C21)
CT → SUS_PGOOD_CT → C8131 0.001UF (20% 50V CERM 402) NO STUFF
MR* → TP_SUS_PGOOD_MR_L
GND

S5 Rail Enables & PGOOD

SMC_PM_G2_EN (IN) — MAKE_BASE=TRUE → R8140 100 (5% 1/16W MF-LF 402) → P3V3S5_EN — P3V3S5_EN (MAKE_BASE=TRUE) (OUT)
SMC_PM_G2_EN (OUT)
C8142 0.0033UF (10% 50V X7R CERM 402) NO STUFF

PP3V42_G3H → R8141 100K (5% 1/16W MF-LF 402)
S5_PWRGD-->SMC
SMC-->PM_DSW_PWRGD
S5_PWRGD — S5_PWRGD (MAKE_BASE=TRUE) (OUT)

WLAN Enable Generation

"WLAN" = ("S4" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S4 term is guaranteed by S4 pull-up on open-drain AP_PWR_EN signal.

PP3V3_S4 → R8125 330K (5% 1/20W MF 201) → PM_WLAN_EN — PM_WLAN_EN (MAKE_BASE=TRUE) (OUT)
PM_WLAN_EN (IN)

S0 Rail PGOOD Circuitry
(ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V3MON: 2.814V-3.099V
V5MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

keep R8171 DDRCPU 1 35V only

PP3V3_S0 → C8162 0.1UF (20% 10V X7R CERM 0402) NOSTUFF → R8195 10 (5% 1/16W MF 402) → PP3V3_S0_VMON_P2
C8160 0.1UF (20% 10V X7R CERM 0402) S0PGOOD_ISL

PP3V3_S0 → C8163 0.1UF (20% 10V X7R CERM 0402) NOSTUFF → R8196 10 (1% 1/16W MF LF 402) → PP3V3_S0_VMON_P7
C8161 0.1UF (20% 10V X7R CERM 0402) S0PGOOD_ISL

PP3V3_S0_VMON_P7 → R8197 100K (5% 1/16W MF-LF 402) NOSTUFF → VMON_MR

PP5V_S0
PP1V35_S3RS0_CPUDDR
PP1V05_S0

R8160 6.04K (1% 1/16W MF-LF 402) S0PGOOD_ISL
P5V_VMON divider
3.16V @4.5V

R8170 10K (1% 1/16W MF-LF 402) S0PGOOD_ISL
P5V_DIV_VMON

R8172 6.04K (1% 1/16W MF-LF 402) S0PGOOD_ISL
P1V05_DIV_VMON

R8161 15.0K (1% 1/16W MF-LF 402) S0PGOOD_ISL
1V35_VMON divider
@ 732V @1.31V

R8171 12.4K (1% 1/16W MF-LF 402)
P1V05_VID_VMON

R8173 15.0K (1% 1/16W MF-LF 402) S0PGOOD_ISL
1V05_VMON divider
@ 716V @1.02V

U8160 ISL88042IRTEZ TDFN (CRITICAL)
VDD, V2MON, V3MON, V4MON, GND, THRM_PAD
RST* → 1VMON_MR

S0PGOOD_ISL R8162 330 (5% 1/16W MF-LF 402) → ALL_SYS_PWRGD

PM_SLP_S3_BUF_L → R8167 10K (5% 1/16W MF-LF 402) → P1V5S0_PGOOD
R8168 100 (5% 1/16W MF-LF 402)
R8169 100 (5% 1/16W MF-LF 402) → P1V05S0_PGOOD

1V5 S0 "PGOOD" Delay

PP3V3_S5 → R8136 23.7K (1% 1/16W MF-LF 402) → C8134 2.2UF (10% 6.3V X5R 402)
PM_1V5_PGD_L

R8137 100 (5% 1/16W MF-LF 402) DELAY_1V5S0_PGD_L → ALL_SYS_PWRGD (OUT)

CRITICAL Q8151 DMB53D0UV SOT-563
Vgs:0.7V~1.0V

R8139 2.0K (1% 1/16W MF-LF 402) → PM_1V5_PGD_L_R
R8135 54.9K (1% 1/16W MF-LF 402)
R8134 61.9K (1% 1/16W MF-LF 402) → PM_1V5_PGD_DIV

CRITICAL Q8151 DMB53D0UV SOT-563
VBEon: 0.58~0.7V
1V5 Divider:0.75~0.85V

PM_SLP_S3_R_L

CHGR VFRQ Generation

VFRQ High: Variable Frequency
VFRQ Low: Fix Frequency

PP3V42_G3H → R8131 100K (5% 1/16W MF-LF 402) → CHGR_VFRQ (OUT)

Unused PGOOD signals

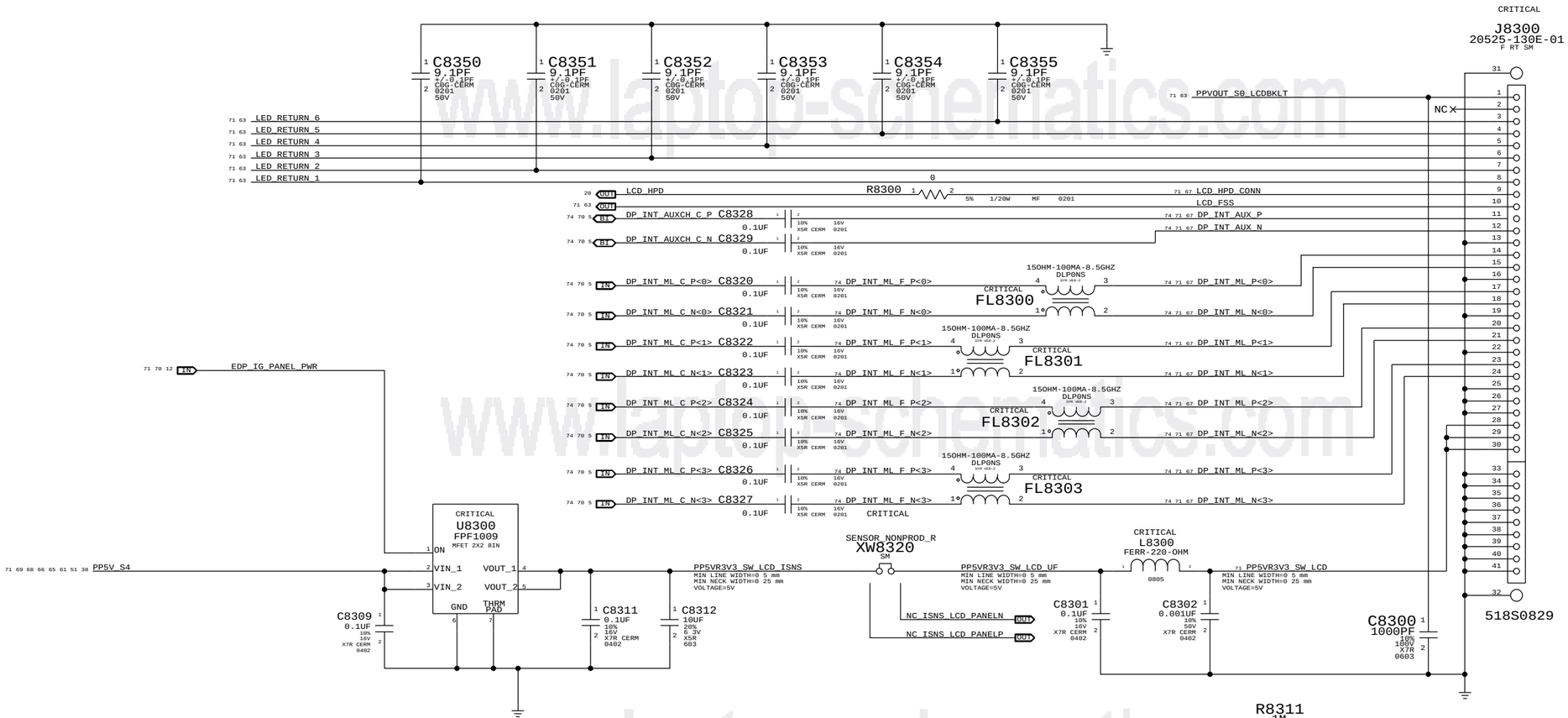
Q8131 DMN32D2LFB4 DFN1006H4-3 SYM VER 2

PP5V_S3 → R8120 470K (5% 1/20W MF 201) → PP5V_S4 → R8165 470K (5% 1/16W MF-LF 402)

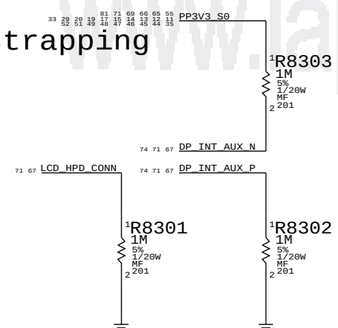
DDRREG_PGOOD (IN)
P5VS4_PGOOD (IN)

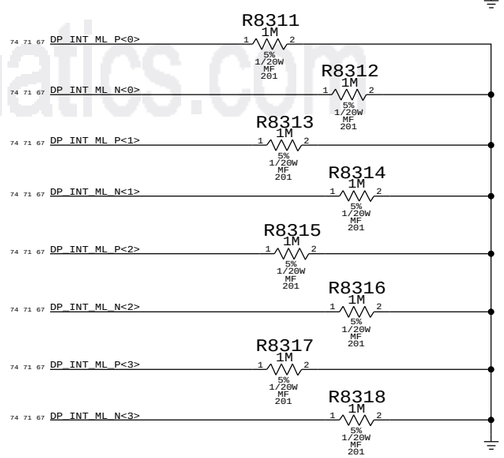
SYNC_MASTER=CHANG_J45	SYNC_DATE=03/15/2013
PAGE TITLE	Power Control 1/ENABLE
Apple Inc.	DRAWING NUMBER <SCH_NUM> D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 81 OF 118
	SHEET 66 OF 81

LCD PANEL INTERFACE (eDP)



LCD Panel HPD & AUX strapping





SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 83 OF 118
SHEET: 67 OF 81

Wire-to-Board (Micro-coax) Connector

NO_XNET_CONNECTION=TRUE
BP9501 SM
BEAD-PROBE TP 1

NO_XNET_CONNECTION=TRUE
BP9502 SM
BEAD-PROBE TP 1

75 13 IN USB3_EXTB_R2D_C_P
75 13 IN USB3_EXTB_R2D_C_N

C9501 1 2 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE
C9502 1 2 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE

75 71 13 OUT USB3_EXTB_D2R_P
75 71 13 OUT USB3_EXTB_D2R_N

NO_XNET_CONNECTION=TRUE
BP9505 SM
BEAD-PROBE TP 1

NO_XNET_CONNECTION=TRUE
BP9506 SM
BEAD-PROBE TP 1

75 71 13 BI USB_EXTB_P
75 71 13 BI USB_EXTB_N
75 71 USB3_EXTB_R2D_P GND_VOID=TRUE
75 71 USB3_EXTB_R2D_N GND_VOID=TRUE

74 71 70 IN HDMI_DATA_P<0> GND_VOID=TRUE
74 71 70 IN HDMI_DATA_N<0> GND_VOID=TRUE
74 71 70 IN HDMI_DATA_P<1> GND_VOID=TRUE
74 71 70 IN HDMI_DATA_N<1> GND_VOID=TRUE
74 71 70 IN HDMI_DATA_P<2> GND_VOID=TRUE
74 71 70 IN HDMI_DATA_N<2> GND_VOID=TRUE

NO_XNET_CONNECTION=TRUE
BP9503 SM
BEAD-PROBE TP 1

NO_XNET_CONNECTION=TRUE
BP9504 SM
BEAD-PROBE TP 1

74 71 70 5 IN HDMI_CLK_P
74 71 70 5 IN HDMI_CLK_N

76 71 20 13 OUT USB3_SD_D2R_P GND_VOID=TRUE
76 71 20 13 OUT USB3_SD_D2R_N GND_VOID=TRUE
76 71 20 13 IN USB3_SD_R2D_C_P GND_VOID=TRUE
76 71 20 13 IN USB3_SD_R2D_C_N GND_VOID=TRUE

J9500
20525-130E-01
F-RT-SM

518S0829

Board-to-Board (Flex) Connector

J9510
20590-032E-25
F-ST-SM

Note. Pin1 in symbol is different to 516S0853 in J15.

70 20 12 OUT HDMI_HPD
71 18 OUT USB_EXTB_OC_L
71 18 13 IN SD_PWR_EN
71 20 OUT RIO_SDCONN_STATE_CHANGE_L

PM_SLP_S3_BUF_L IN 51 65 66 71
PM_SLP_S4_L IN 12 21 34 38 41 66 71
HDMI_DDC_CLK IN 12 70 71
HDMI_DDC_DATA BI 12 70 71

71 69 65 47 46 44 22 21 20 13 PP3V3_S3
PP1V5R1V35_S0_RIO MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.5V 38 51 61 65 66 67 69 71
PP5V_S4

69 66 65 47 46 43 42 39 34 20 73 70 PP3V3_S4
76 71 63 44 22 18 13 IN SMBUS_PCH_CLK
76 71 63 44 22 18 13 BI SMBUS_PCH_DATA

C9510 1 2 0.1uF 20% 16V X5R CERM 402
C9511 1 2 0.1uF 20% 16V X5R CERM 402

516S1106

RIO_PWR:1V5
R9535 0 5% 1/10W MF-LF 402
2 1 PP1V5_S0 11 12 13 15 17 19 52 64 66 69 71

RIO_PWR:1V35
R9534 0 5% 1/10W MF-LF 402
2 1 PP1V35_S3RS0_FET 65 69

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
RIO Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 95 OF 118
SHEET 68 OF 81

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

Power Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 100 OF 118

SHEET 69 OF 81

Display Aliases

71 70 67 12	EDP_IG_PANEL_PWR	MAKE_BASE=TRUE	=	EDP_IG_PANEL_PWR	12 67 70 71
71 70 63 12	EDP_IG_BKL_ON	MAKE_BASE=TRUE	=	EDP_IG_BKL_ON	12 63 70 71
70 63 12	EDP_IG_BKL_PWM	MAKE_BASE=TRUE	=	EDP_IG_BKL_PWM	12 63 70
74 67 5	DP_INT_ML_C_P<3..0>	MAKE_BASE=TRUE	=	TP_DP_IG_A_MLP<3..0>	
74 67 5	DP_INT_ML_C_N<3..0>	MAKE_BASE=TRUE	=	TP_DP_IG_A_MLN<3..0>	
74 70 67 5	DP_INT_AUXCH_C_P	MAKE_BASE=TRUE	=	DP_INT_AUXCH_C_P	5 67 70 74
74 70 67 5	DP_INT_AUXCH_C_N	MAKE_BASE=TRUE	=	DP_INT_AUXCH_C_N	5 67 70 74
70 28 12	DP_TBTSNK0_HPD	MAKE_BASE=TRUE	=	DP_TBTSNK0_HPD	12 28 70
74 28 5	DP_TBTSNK0_ML_C_P<3..0>	MAKE_BASE=TRUE	=	TP_DP_IG_B_MLP<3..0>	
74 28 5	DP_TBTSNK0_ML_C_N<3..0>	MAKE_BASE=TRUE	=	TP_DP_IG_B_MLN<3..0>	
74 70 28 12	DP_TBTSNK0_AUXCH_C_P	MAKE_BASE=TRUE	=	DP_TBTSNK0_AUXCH_C_P	12 28 70 74
74 70 28 12	DP_TBTSNK0_AUXCH_C_N	MAKE_BASE=TRUE	=	DP_TBTSNK0_AUXCH_C_N	12 28 70 74
70 33 12	DP_TBTSNK0_DDC_DATA	MAKE_BASE=TRUE	=	DP_TBTSNK0_DDC_DATA	12 33 70
70 33 12	DP_TBTSNK0_DDC_CLK	MAKE_BASE=TRUE	=	DP_TBTSNK0_DDC_CLK	12 33 70
70 28 12	DP_TBTSNK1_HPD	MAKE_BASE=TRUE	=	DP_TBTSNK1_HPD	12 28 70
74 28 5	DP_TBTSNK1_ML_C_P<3..0>	MAKE_BASE=TRUE	=	TP_DP_IG_C_MLP<3..0>	
74 28 5	DP_TBTSNK1_ML_C_N<3..0>	MAKE_BASE=TRUE	=	TP_DP_IG_C_MLN<3..0>	
74 70 28 12	DP_TBTSNK1_AUXCH_C_P	MAKE_BASE=TRUE	=	DP_TBTSNK1_AUXCH_C_P	12 28 70 74
74 70 28 12	DP_TBTSNK1_AUXCH_C_N	MAKE_BASE=TRUE	=	DP_TBTSNK1_AUXCH_C_N	12 28 70 74
70 33 12	DP_TBTSNK1_DDC_DATA	MAKE_BASE=TRUE	=	DP_TBTSNK1_DDC_DATA	12 33 70
70 33 12	DP_TBTSNK1_DDC_CLK	MAKE_BASE=TRUE	=	DP_TBTSNK1_DDC_CLK	12 33 70
70 68 20 12	HDMI_HPD	MAKE_BASE=TRUE	=	HDMI_HPD	12 20 68 70
74 71 68	HDMI_DATA_P<0..2>	MAKE_BASE=TRUE	=	TP_DP_IG_D_MLP<2..0>	5
74 71 68	HDMI_DATA_N<0..2>	MAKE_BASE=TRUE	=	TP_DP_IG_D_MLN<2..0>	5
74 71 70 68 5	HDMI_CLK_P	MAKE_BASE=TRUE	=	HDMI_CLK_P	5 68 70 71 74
74 71 70 68 5	HDMI_CLK_N	MAKE_BASE=TRUE	=	HDMI_CLK_N	5 68 70 71 74
71 70 68 12	HDMI_DDC_CLK	MAKE_BASE=TRUE	=	HDMI_DDC_CLK	12 68 70 71
71 70 68 12	HDMI_DDC_DATA	MAKE_BASE=TRUE	=	HDMI_DDC_DATA	12 68 70 71

CPU signals

70 60 21	MEMVTT_EN	MAKE_BASE=TRUE	=	MEMVTT_EN	21 60 70

Thunderbolt Signals Through PEG

74 28 5	PCIE_TBT_D2R_P<3..0>	MAKE_BASE=TRUE	=	=PEG_D2R_P<3..0>	OUT
74 28 5	PCIE_TBT_D2R_N<3..0>	MAKE_BASE=TRUE	=	=PEG_D2R_N<3..0>	OUT
74 28 5	PCIE_TBT_R2D_C_P<3..0>	MAKE_BASE=TRUE	=	=PEG_R2D_C_P<3..0>	IN
74 28 5	PCIE_TBT_R2D_C_N<3..0>	MAKE_BASE=TRUE	=	=PEG_R2D_C_N<3..0>	IN

Unused PEG Lanes

5	TP_PEG_D2RP<15..4>	MAKE_BASE=TRUE	=	=PEG_D2R_P<15..4>	
5	TP_PEG_D2RN<15..4>	MAKE_BASE=TRUE	=	=PEG_D2R_N<15..4>	
5	TP_PEG_R2D_CP<15..4>	MAKE_BASE=TRUE	=	=PEG_R2D_C_P<15..4>	
5	TP_PEG_R2D_CN<15..4>	MAKE_BASE=TRUE	=	=PEG_R2D_C_N<15..4>	

70 49	PP3V3_S3_FAN_CTL		=	PP3V3_S3_FAN_CTL	MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM VOLTAGE=3.3V MAKE_BASE=TRUE	49 70
	RA201 0 1/20W MF 0201 5%	1 2	=	PP3V3_S5		12 14 15 17 18 19 21 31 32 34 61 64 65 66 69 71 81
	RA202 0 1/20W MF 0201 5% NOSTUFF	1 2	=	PP3V3_S4		20 34 39 42 43 46 47 65 66 68 69 71

Unused signals

12	BT_PWRRST_L
14	MEM_VDD_SEL_1V5_L
14	FW_PWR_EN_PCH
14	WOL_EN
14	FW_PME_L
11	DP_TBT_SEL
11	ENET_MEDIA_SENSE_RDIV
12	AUD_IPHS_SWITCH_EN_PCH
12	AUD_IP_PERIPHERAL_DET
12	AUD_I2C_INT_L
14	TBT_GO2SX_BIDIR
14	DPMUX_UC_IRQ
11	PEG_CLKREQ_L
11	ENET_CLKREQ_L
12	ENET_LOW_PWR_PCH
28	HDMITBTMUX_SEL_TBT
12	SDCONN_OC_L

		VOLTAGE	MAKE_BASE		
77 74 70 24 23 22	PP0V75_S3_MEM_VREFDQ_A	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_A	22 23 24 70 74 77
74 70 26 25 22	PP0V75_S3_MEM_VREFDQ_B	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_B	22 25 26 70 74
77 74 70 24 23 22	PP0V75_S3_MEM_VREFCA_A	0.675V	TRUE	PP0V75_S3_MEM_VREFCA_A	22 23 24 70 74 77
74 70 26 25 22	PP0V75_S3_MEM_VREFCA_B	0.675V	TRUE	PP0V75_S3_MEM_VREFCA_B	22 25 26 70 74

65 63 62 59 58 50 49 37 19 18 71 69 66	PP5V_S0				
	XWA202 SM 1 2	=	PP5V_S0_AUDIO_AMP_L	MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V	53
	XWA203 SM 1 2	=	PP5V_S0_AUDIO_AMP_R	MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V	53

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 102 OF 118

SHEET: 70 OF 81

Functional Test Points

J3501 - airport

FUNC_TEST		
TRUE	AP_CLKREQ_Q_L	34
TRUE	AP_RESET_CONN_L	34
TRUE	PCIE_AP_D2R_PI_N	34 76
TRUE	PCIE_AP_D2R_PI_P	34 76
TRUE	PCIE_AP_R2D_N	34 76
TRUE	PCIE_AP_R2D_P	34 76
TRUE	PCIE_CLK100M_AP_CONN_N	34 76
TRUE	PCIE_CLK100M_AP_CONN_P	34 76
TRUE	PCIE_WAKE_L	12 34 36 76
TRUE	PP3V3_S3RS4_BT_F	34
TRUE	PP3V3_WLAN	34 42
TRUE	USB_BT_CONN_N	34 75
TRUE	USB_BT_CONN_P	34 75
TRUE	WIFI_EVENT_L	34 41 42
TRUE	GND	4X

J4002 - Camera

TRUE	MIPI_CLK_CONN_N	37 79
TRUE	MIPI_CLK_CONN_P	37 79
TRUE	CAM_SENSOR_WAKE_L_CONN	37
TRUE	MIPI_DATA_CONN_N	37 79
TRUE	MIPI_DATA_CONN_P	37 79
TRUE	SMBUS_SMC_0_S0_SDA	37 41 44 48 80
TRUE	SMBUS_SMC_0_S0_SCL	37 41 44 48 80
TRUE	I2C_CAM_SCK	36 37
TRUE	I2C_CAM_SDA	36 37
TRUE	PP5V_S3RS0_ALSCAM_F	37
TRUE	GND	

J9500 - rio coax

TRUE	HDMI_CLK_N	5 68 70 74
TRUE	HDMI_CLK_P	5 68 70 74
TRUE	HDMI_DATA_N<0>	68 70 74
TRUE	HDMI_DATA_N<1>	68 70 74
TRUE	HDMI_DATA_N<2>	68 70 74
TRUE	HDMI_DATA_P<0>	68 70 74
TRUE	HDMI_DATA_P<1>	68 70 74
TRUE	HDMI_DATA_P<2>	68 70 74
TRUE	USB3_SD_D2R_N	13 20 68 76
TRUE	USB3_SD_D2R_P	13 20 68 76
TRUE	USB3_SD_R2D_C_N	13 20 68 76
TRUE	USB3_SD_R2D_C_P	13 20 68 76
TRUE	USB3_EXTB_D2R_N	13 68 75
TRUE	USB3_EXTB_D2R_P	13 68 75
TRUE	USB3_EXTB_R2D_N	68 75
TRUE	USB3_EXTB_R2D_P	68 75
TRUE	USB_EXTB_N	13 68 75
TRUE	USB_EXTB_P	13 68 75
TRUE	GND	19X

J9510 - rio flex

TRUE	SD_PWR_EN	13 18 68
TRUE	PP1V5R1V35_S0_RIO	68
TRUE	HDMI_DDC_CLK	12 68 70
TRUE	HDMI_DDC_DATA	12 68 70
TRUE	HDMI_HPD_L	
TRUE	SMBUS_PCH_CLK	13 18 22 44 63 68 76
TRUE	SMBUS_PCH_DATA	13 18 22 44 63 68 76
TRUE	PM_SLP_S3_BUF_L	51 65 66 68
TRUE	PM_SLP_S4_L	12 21 34 38 41 66 68
TRUE	PP3V3_S3	3X 13 20 21 22 44 46 47 65 68 69 71
TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP5V_S4	5X 38 51 61 65 66 67 68 69
TRUE	RIO_SDCONN_STATE_CHANGE_L	20 68
TRUE	USB_EXTB_OC_L	18 68
TRUE	GND	10X

J5150 - hall effect

TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	SMC_LID_R	43
TRUE	GND	

J6050 - left fan

TRUE	FAN_LT_PWM	49
TRUE	FAN_LT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	GND	5X

J6060 - right fan

TRUE	FAN_RT_PWM	49
TRUE	FAN_RT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	GND	5X

J6100 - lpc + spi

FUNC_TEST		
TRUE	LPCPLUS_GPIO	14 50
TRUE	LPCPLUS_RESET_L	20 50 76
TRUE	LPC_AD<0>	13 41 50 76
TRUE	LPC_AD<1>	13 41 50 76
TRUE	LPC_AD<2>	13 41 50 76
TRUE	LPC_AD<3>	13 41 50 76
TRUE	LPC_CLK33M_LPCPLUS	19 50 76
TRUE	LPC_FRAME_L	13 41 50 76
TRUE	LPC_PWRDWN_L	12 20 41 50
TRUE	LPC_SERIRQ	13 41 50
TRUE	PM_CLKRUN_L	12 41 50
TRUE	PP5V_S0	18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	SMC_RESET_L	41 42 50 57
TRUE	SMC_ROMBOOT	42 50
TRUE	SMC_RX_L	41 42 50
TRUE	SMC_TCK	41 42 50
TRUE	SMC_TDI	41 42 50
TRUE	SMC_TDO	41 42 50
TRUE	SMC_TMS	41 42 50
TRUE	SMC_TX_L	41 42 50
TRUE	SPIROM_USE_MLB	14 50
TRUE	SPI_ALT_CLK	50
TRUE	SPI_ALT_CS_L	50
TRUE	SPI_ALT_MISO	50
TRUE	SPI_ALT_MOSI	50
TRUE	TP_SMC_MD1	50
TRUE	TP_SMC_TRST_L	50
TRUE	GND	2X

J4800 - ipd flex

TRUE	Z2_CS_L	39
TRUE	Z2_MOSI	39
TRUE	Z2_MISO	39
TRUE	Z2_SCLK	39
TRUE	Z2_HOST_INTN	39
TRUE	Z2_CLKIN	39
TRUE	Z2_KEY_ACT_L	39
TRUE	PSOC_F_CS_L	39
TRUE	PICKB_L	39
TRUE	PSOC_MOSI	39
TRUE	PSOC_MISO	39
TRUE	PSOC_SCLK	39
TRUE	SMBUS_SMC_2_S3_SCL	39 41 44 80
TRUE	SMBUS_SMC_2_S3_SDA	39 41 44 80
TRUE	SMC_LID	39 41 42 43
TRUE	SMC_T101_COM_1	
TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP5V_S5	39 61 65 69 71
TRUE	GND	2X

J4813 - keyboard

TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	WS_CONTROL_KBD	39
TRUE	WS_KBD1	39
TRUE	WS_KBD10	39
TRUE	WS_KBD11	39
TRUE	WS_KBD12	39
TRUE	WS_KBD13	39
TRUE	WS_KBD14	39
TRUE	WS_KBD15_CAP	39
TRUE	WS_KBD16_NUM	39
TRUE	WS_KBD17	39
TRUE	WS_KBD18	39
TRUE	WS_KBD19	39
TRUE	WS_KBD2	39
TRUE	WS_KBD20	39
TRUE	WS_KBD21	39
TRUE	WS_KBD22	39
TRUE	WS_KBD23	39
TRUE	WS_KBD3	39
TRUE	WS_KBD4	39
TRUE	WS_KBD5	39
TRUE	WS_KBD6	39
TRUE	WS_KBD7	39
TRUE	WS_KBD8	39
TRUE	WS_KBD9	39
TRUE	WS_KBD_ONOFF_L	39
TRUE	WS_LEFT_OPTION_KBD	39
TRUE	WS_LEFT_SHIFT_KBD	39
TRUE	GND	2X

J4915 - kbd bklt

TRUE	KBDBKLT_RETURN1	2X 40 63
TRUE	KBDBKLT_RETURN2	2X 40 63
TRUE	PPVOUT_S0_KBDBKLT	40 63
TRUE	GND	4X

J6701 - audio flex

FUNC_TEST		
TRUE	AUD_HP_PORT_L	51 55
TRUE	AUD_HP_PORT_R	51 55
TRUE	AUD_SPDIF_OUT_JACK	
TRUE	AUD_TIPDET_INV	
TRUE	AUD_TYPEDET	51 55
TRUE	AUD_CONN_MIC_XW	4X
TRUE	CH_HS_MIC	
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	AUD_CONN_SLEEVE_XW	4X 54 55
TRUE	US_HS_MIC	
TRUE	GND	2X GND

J6601 - mic

TRUE	DMIC_CLK3	52 55
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	DMIC_SDA2	55
TRUE	DMIC_SDA3	52 55
TRUE	GND	

J6602 - L speaker

TRUE	SPKRCONN_L_ID	52 55
TRUE	SPKRCONN_L_OUT_N	53 55 81
TRUE	SPKRCONN_L_OUT_P	53 55 81
TRUE	SPKRCONN_SL_OUT_N	53 55 81
TRUE	SPKRCONN_SL_OUT_P	53 55 81
TRUE	GND	

J6603 - R speaker

TRUE	SPKRCONN_R_ID	52 55
TRUE	SPKRCONN_R_OUT_N	53 55 81
TRUE	SPKRCONN_R_OUT_P	53 55 81
TRUE	SPKRCONN_SR_OUT_N	53 55 81
TRUE	SPKRCONN_SR_OUT_P	53 55 81
TRUE	GND	

J7000 - DC PWR

TRUE	ADAPTER_SENSE	56
TRUE	PP20V_DCIN_FUSE	2X 56
TRUE	GND	2X

J7050 - battery

TRUE	PPVBAT_G3H_CONN	8X 56 57
TRUE	SMBUS_SMC_5_G3_SCL	41 44 56 57 80
TRUE	SMBUS_SMC_5_G3_SDA	41 44 56 57 80
TRUE	SYS_DETECT_L	56
TRUE	GND	8X

J8300 - eDP

TRUE	DP_INT_AUX_N	67 74
TRUE	DP_INT_AUX_P	67 74
TRUE	DP_INT_ML_N<0>	67 74
TRUE	DP_INT_ML_N<1>	67 74
TRUE	DP_INT_ML_N<2>	67 74
TRUE	DP_INT_ML_N<3>	67 74
TRUE	DP_INT_ML_P<0>	67 74
TRUE	DP_INT_ML_P<1>	67 74
TRUE	DP_INT_ML_P<2>	67 74
TRUE	DP_INT_ML_P<3>	67 74
TRUE	LCD_FSS	63 67
TRUE	LCD_HPD_CONN	67
TRUE	LED_RETURN_1	63 67
TRUE	LED_RETURN_2	63 67
TRUE	LED_RETURN_3	63 67
TRUE	LED_RETURN_4	63 67
TRUE	LED_RETURN_5	63 67
TRUE	LED_RETURN_6	63 67
TRUE	PP5VR3V3_SW_LCD	3X 67
TRUE	PPVOUT_S0_LCDBKLT	63 67
TRUE	GND	16X

Power Rails

TRUE	PM_SLP_S3_L	12 21 41 66
TRUE	PPVTT_S0_DDR	21 27 60 69
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	PP3V3_S3	13 20 21 22 44 46 47 65 68 69 71
TRUE	PP3V3_S5	12 14 15 17 18 19 21 31 32 34 61 64 65 66 69 70 81
TRUE	PP3V3_S5_AVREF_SMC	41 42
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	PP5V_S0	18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	PP5V_S3	21 37 60 65 66 69
TRUE	PP5V_S5	39 61 65 69 71
TRUE	PPBUS_G3H	30 45 56 57 63 69
TRUE	PPDCIN_G3H	56 57 69
TRUE	PPVCC_S0_CPU	6 8 10 46 59 69
TRUE	PPVTTDDR_S3	60 69
TRUE	PP3V3_S0SW_SSD	35 46 69
TRUE	PP1V5_S0	11 12 13 15 17 19 52 64 66 68 69
TRUE	PP1V35_S3	21 22 46 60 65 69

XDP

FUNC_TEST		
TRUE	XDP_CPU_TCK	6 18 74
TRUE	XDP_PCH_TCK	11 18
TRUE	XDP_CPU_TDI	6 18 74
TRUE	XDP_CPU_TDO	6 18 74
TRUE	XDP_CPUPCH_TRST_L	6 18 74
TRUE	XDP_CPU_TMS	6 18 74
TRUE	XDP_PCH_TMS	11 18
TRUE	XDP_PCH_TDI	11 18
TRUE	XDP_PCH_TDO	11 18
TRUE	XDP_CPU_PREQ_L	6 18 74
TRUE	XDP_CPU_PRDY_L	6 18 74
TRUE	PM_RSMRST_L	12 66 76
TRUE	PM_PCH_PWROK	12 19 76
TRUE	PM_SYSRST_L	12 19 41 76
TRUE	CPU_CFG<3>	6 18 74
TRUE	PP1V05_S0	14 15 17 18 42 62 66 69
TRUE	GND	2X GND

Power Sequence

FUNC_TEST		
TRUE	SMC_ONOFF_L	39 41 42
TRUE	PM_DSW_PWRGD	12 41 76
TRUE	ALL_SYS_PWRGD	18 19 41 58 66
TRUE	PM_PCH_SYS_PWROK	12 18 19 41 76
TRUE	PLT_RESET_L	12 18 20 21
TRUE	EDP_IG_PANEL_PWR	12 67 70
TRUE	EDP_IG_BKL_ON	12 63 70

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Functional Test Points

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DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 104 OF 118

SHEET: 71 OF 81

NC NO_TESTs

PCH

	NO_TEST	MAKE_BASE	
NC_USB3_SPARE_D2RN	TRUE	TRUE	NC_USB3_SPARE_D2RN
NC_USB3_SPARE_D2RP	TRUE	TRUE	NC_USB3_SPARE_D2RP
NC_USB3_SPARE_R2D_CN	TRUE	TRUE	NC_USB3_SPARE_R2D_CN
NC_USB3_SPARE_R2D_CP	TRUE	TRUE	NC_USB3_SPARE_R2D_CP
NC_USB3_EXTC_D2RN	TRUE	TRUE	NC_USB3_EXTC_D2RN
NC_USB3_EXTC_D2RP	TRUE	TRUE	NC_USB3_EXTC_D2RP
NC_USB3_EXTC_R2D_CN	TRUE	TRUE	NC_USB3_EXTC_R2D_CN
NC_USB3_EXTC_R2D_CP	TRUE	TRUE	NC_USB3_EXTC_R2D_CP
NC_USB3_EXTD_D2RN	TRUE	TRUE	NC_USB3_EXTD_D2RN
NC_USB3_EXTD_D2RP	TRUE	TRUE	NC_USB3_EXTD_D2RP
NC_USB3_EXTD_R2D_CN	TRUE	TRUE	NC_USB3_EXTD_R2D_CN
NC_USB3_EXTD_R2D_CP	TRUE	TRUE	NC_USB3_EXTD_R2D_CP
NC_PCIE_ENET_D2RN	TRUE	TRUE	NC_PCIE_ENET_D2RN
NC_PCIE_ENET_D2RP	TRUE	TRUE	NC_PCIE_ENET_D2RP
NC_PCIE_ENET_R2D_CN	TRUE	TRUE	NC_PCIE_ENET_R2D_CN
NC_PCIE_ENET_R2D_CP	TRUE	TRUE	NC_PCIE_ENET_R2D_CP
NC_SATA_A_D2RN	TRUE	TRUE	NC_SATA_A_D2RN
NC_SATA_A_D2RP	TRUE	TRUE	NC_SATA_A_D2RP
NC_SATA_A_R2D_CN	TRUE	TRUE	NC_SATA_A_R2D_CN
NC_SATA_A_R2D_CP	TRUE	TRUE	NC_SATA_A_R2D_CP
NC_SATA_B_D2RN	TRUE	TRUE	NC_SATA_B_D2RN
NC_SATA_B_D2RP	TRUE	TRUE	NC_SATA_B_D2RP
NC_SATA_B_R2D_CN	TRUE	TRUE	NC_SATA_B_R2D_CN
NC_SATA_B_R2D_CP	TRUE	TRUE	NC_SATA_B_R2D_CP
NC_SATA_ODD_D2RN	TRUE	TRUE	NC_SATA_ODD_D2RN
NC_SATA_ODD_D2RP	TRUE	TRUE	NC_SATA_ODD_D2RP
NC_SATA_ODD_R2D_CN	TRUE	TRUE	NC_SATA_ODD_R2D_CN
NC_SATA_ODD_R2D_CP	TRUE	TRUE	NC_SATA_ODD_R2D_CP
NC_SATA_D_D2RN	TRUE	TRUE	NC_SATA_D_D2RN
NC_SATA_D_D2RP	TRUE	TRUE	NC_SATA_D_D2RP
NC_SATA_D_R2D_CN	TRUE	TRUE	NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP	TRUE	TRUE	NC_SATA_D_R2D_CP
NC_SATA_F_D2RN	TRUE	TRUE	NC_SATA_F_D2RN
NC_SATA_F_D2RP	TRUE	TRUE	NC_SATA_F_D2RP
NC_SATA_F_R2D_CN	TRUE	TRUE	NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP	TRUE	TRUE	NC_SATA_F_R2D_CP
NC_USB_EXTCN	TRUE	TRUE	NC_USB_EXTCN
NC_USB_EXTCP	TRUE	TRUE	NC_USB_EXTCP
NC_USB_SDN	TRUE	TRUE	NC_USB_SDN
NC_USB_SDP	TRUE	TRUE	NC_USB_SDP
NC_USB_WLANN	TRUE	TRUE	NC_USB_WLANN
NC_USB_WLANP	TRUE	TRUE	NC_USB_WLANP
NC_USB_6N	TRUE	TRUE	NC_USB_6N
NC_USB_6P	TRUE	TRUE	NC_USB_6P
NC_USB_7N	TRUE	TRUE	NC_USB_7N
NC_USB_7P	TRUE	TRUE	NC_USB_7P
NC_USB_EXTDN	TRUE	TRUE	NC_USB_EXTDN
NC_USB_EXTDP	TRUE	TRUE	NC_USB_EXTDP
NC_USB_PSOCN	TRUE	TRUE	NC_USB_PSOCN
NC_USB_PSOCP	TRUE	TRUE	NC_USB_PSOCP
NC_USB_IRN	TRUE	TRUE	NC_USB_IRN
NC_USB_IRP	TRUE	TRUE	NC_USB_IRP
NC_ITPXDP_CLK100MN	TRUE	TRUE	NC_ITPXDP_CLK100MN
NC_ITPXDP_CLK100MP	TRUE	TRUE	NC_ITPXDP_CLK100MP
NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L
NC_PCI_CLK33M_OUT2	TRUE	TRUE	NC_PCI_CLK33M_OUT2
NC_PCI_CLK33M_OUT3	TRUE	TRUE	NC_PCI_CLK33M_OUT3
NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1
NC_HDA_SDIN2	TRUE	TRUE	NC_HDA_SDIN2
NC_HDA_SDIN3	TRUE	TRUE	NC_HDA_SDIN3
NC_LPC_DREQ0_L	TRUE	TRUE	NC_LPC_DREQ0_L
NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK
NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA
NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L
NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP
NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN
NC_SMC_INTERFACE_2	TRUE	TRUE	NC_SMC_INTERFACE_2

Thunderbolt

	NO_TEST	MAKE_BASE	
NC_TBT_XTAL25OUT	TRUE	TRUE	NC_TBT_XTAL25OUT
TP_DP_TBTSRC_ML_CP<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>
TP_DP_TBTSRC_ML_CN<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>
NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN
NC_DP_IG_D_AUXCHN	TRUE	TRUE	NC_DP_IG_D_AUXCHN
NC_DP_IG_D_AUXCHP	TRUE	TRUE	NC_DP_IG_D_AUXCHP
NC_PCIE_CLK100M_GPUN	TRUE	TRUE	NC_PCIE_CLK100M_GPUN
NC_PCIE_CLK100M_GPUP	TRUE	TRUE	NC_PCIE_CLK100M_GPUP
NC_PCIE_CLK100M_PE5N	TRUE	TRUE	NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P	TRUE	TRUE	NC_PCIE_CLK100M_PE5P
NC_PCIE_CLK100M_ENETSDN	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN
NC_PCIE_CLK100M_ENETSDP	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP
NC_PCIE_CLK100M_ENETN	TRUE	TRUE	NC_PCIE_CLK100M_ENETN
NC_PCIE_CLK100M_ENETP	TRUE	TRUE	NC_PCIE_CLK100M_ENETP
NC_PCIE_CLK100M_PEGBN	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN
NC_PCIE_CLK100M_PEGBP	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP
NC_PCIE_CLK100M_SWN	TRUE	TRUE	NC_PCIE_CLK100M_SWN
NC_PCIE_CLK100M_SWP	TRUE	TRUE	NC_PCIE_CLK100M_SWP
NC_PCH_GPIO64_CLKOUTFLEX0	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3
NC_USB_4N	TRUE	TRUE	NC_USB_4N
NC_USB_4P	TRUE	TRUE	NC_USB_4P

TRUE	PCIE_TBT_R2D_P<3..0>	
TRUE	PCIE_TBT_R2D_N<3..0>	
TRUE	PCIE_TBT_D2R_C_P<3..0>	
TRUE	PCIE_TBT_D2R_C_N<3..0>	
TRUE	DMI_S2N_P<3..1>	
TRUE	DMI_S2N_N<3..1>	
TRUE	DMI_N2S_P<3..1>	
TRUE	DMI_N2S_N<3..1>	

PLACEABLE BEAD-PROBES FOR TBT

TBT_A_R2D_C_P<1>	1	SM	BEAD-PROBE BPA535 NO_XNET_CONNECTION=TRUE
TBT_A_R2D_P<1>	1	SM	BEAD-PROBE BPA531 NO_XNET_CONNECTION=TRUE
TBT_A_R2D_N<1>	1	SM	BEAD-PROBE BPA532 NO_XNET_CONNECTION=TRUE

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: NC & No Test

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 105 OF 118

SHEET: 72 OF 81

J15 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	·	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3 ISL4 ISL9 ISL10	0.053 MM	?
1x_DIELECTRIC	ISL5 ISL6 ISL7 ISL8 ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65 BGA

SYNC MASTER=SIDLE J45 SYNC DATE=12/10/2012

PAGE TITLE: PCB Rule Definitions

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DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 110 OF 118

SHEET: 73 OF 81

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD
CPU 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD
CPU 27P4S	*	=27P4 OHM SE	=27P4 OHM SE	=27P4 OHM SE	=27P4 OHM SE	7 MIL	7 MIL
CPU 85D	*	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU AGTL	*	=STANDARD	?
CPU 8MIL	*	8 MIL	?
CPU COMP	*	20 MIL	?
CPU ITP	*	=2 1 SPACING	?
CPU VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU AGTL	TOP BOTTOM	=2x DIELECTRIC	?
CPU VID	*	0 457 MM	?
CPU VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG 80D	*	80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG 2SAME	*	=3X DIELECTRIC	?
PEG TXRX	*	=6X DIELECTRIC	?
PEG 2OTHER	*	=4X DIELECTRIC	?
PEG 2CLK	*	=7X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG 2SAME	TOP BOTTOM	=4X DIELECTRIC	?
PEG TXRX	TOP BOTTOM	=10X DIELECTRIC	?
PEG 2OTHER	TOP BOTTOM	=6X DIELECTRIC	?
PEG 2CLK	TOP BOTTOM	=10X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP 85D	*	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP 2SAME	*	=3x DIELECTRIC	?
DP 2OTHER	*	=4x DIELECTRIC	?
HDMICLK 2CLK	*	=7x DIELECTRIC	?
HDMICLK 2DP	*	=4x DIELECTRIC	?
HDMICLK 2OTHER	*	=7x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP 2SAME	TOP BOTTOM	=4x DIELECTRIC	?
DP 2OTHER	TOP BOTTOM	=6x DIELECTRIC	?
HDMICLK 2CLK	TOP BOTTOM	=10x DIELECTRIC	?
HDMICLK 2DP	TOP BOTTOM	=6x DIELECTRIC	?
HDMICLK 2OTHER	TOP BOTTOM	=10x DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra pair matching should be 0 127mm Inter pair matching should be within 2 54cm Max Length 241 3mm
DIsplayPort AUX CH intra pair matching should be 0 127mm Max length 330 2mm
SOURCE Calpella SFF DG Rev 1 5 (407364) and Family GPU DG 04202 001 v04
MAX LENGTH OF DISPLAYPORT/TMDS TRACES 13 INCHES

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N P<3:0>	5 12 72
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N N<3:0>	5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S P<3:0>	5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S N<3:0>	5 12 72
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC	5 12
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_P	6 11
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP	5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP	5
CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>	6 18 71
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MP	11 72
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MN	11 72
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 18 71
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 18 71
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 18 71
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 18 71
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 18 71
XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	6 18
XDP_BDRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L	6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 18 71
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 18 71
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 41
CPU_PECI	CPU_45S	CPU_VID	CPU_PECI	6 14 42
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 41 42 58
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_8MTI	PM_THRMTRIP_L	6 14 42
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	6
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 58
CPU_MEM_VREF		CPU_VREF	CPU_DIMMA_VREFDQ	7 22
CPU_MEM_VREF		CPU_VREF	CPU_DIMMB_VREFDQ	7 22
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 70 77
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	22 25 26 70
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	22 23 24 70 77
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	22 25 26 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_P<3..0>	5 28 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_N<3..0>	5 28 70
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_P<3..0>	28 72
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_N<3..0>	28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_P<3..0>	28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_N<3..0>	28 72
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_P<3..0>	5 28 70
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_N<3..0>	5 28 70

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	5 67 70
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	5 67 70
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 71 74
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 71 74
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	67
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	67
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 71 74
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 71 74
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	5 67 70
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	5 67 70
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	67 71
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	67 71

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_P<2..0>	68 70 71
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_N<2..0>	68 70 71
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_P	5 68 70 71
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_N	5 68 70 71
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	5 28 70
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	5 28 70
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	5 28 70
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	5 28 70
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	28
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	28
	DP_85D		DP_TBTSNK0_AUXCH_C_P	12 28 70
	DP_85D		DP_TBTSNK0_AUXCH_C_N	12 28 70
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P	28
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N	28
	DP_85D		DP_TBTSNK1_AUXCH_C_P	12 28 70
	DP_85D		DP_TBTSNK1_AUXCH_C_N	12 28 70

SYNC MASTER=SIDLE J45 SYNC DATE=12/10/2012

PAGE TITLE: CPU Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 111 OF 118
SHEET: 74 OF 81

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF
SATA 37SE	*	37 OHM SE	=37 OHM SE	=37 OHM SE	=37 OHM SE	=37 OHM SE	=37 OHM SE
SATA 45SE	*	45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA 2SAME	*	=3X DIELECTRIC	?
SATA TXRX	*	=6X DIELECTRIC	?
SATA 2OTHER	*	=4X DIELECTRIC	?
SATA RCOMP	*	=6X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA 2SAME	TOP BOTTOM	=4x DIELECTRIC	?
SATA TXRX	TOP BOTTOM	=10X DIELECTRIC	?
SATA 2OTHER	TOP BOTTOM	=6X DIELECTRIC	?
SATA RCOMP	TOP BOTTOM	=10X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH USB RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X DIELECTRIC	?
USB RBIAS	*	=6X DIELECTRIC	?
BT WAKE	*	=4X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP BOTTOM	=6X DIELECTRIC	?
USB RBIAS	TOP BOTTOM	=10X DIELECTRIC	?
BT WAKE	TOP BOTTOM	=6X DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3 2SAME	*	=3X DIELECTRIC	?
USB3 TXRX	*	=6X DIELECTRIC	?
USB3 2OTHER	*	=4X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3 2SAME	TOP BOTTOM	=4x DIELECTRIC	?
USB3 TXRX	TOP BOTTOM	=10X DIELECTRIC	?
USB3 2OTHER	TOP BOTTOM	=6X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	11 72
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	11 72
T27	SATA_85D	SATA_D2R	NC_SATA_A_D2RP	11 72
T27	SATA_85D	SATA_D2R	NC_SATA_A_D2RN	11 72
T29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	11 72
T29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	11 72
T30	SATA_85D	SATA_D2R	NC_SATA_B_D2RP	11 72
T30	SATA_85D	SATA_D2R	NC_SATA_B_D2RN	11 72
T213 PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
	USB_85D	USB	USB_EXTA_P	13 38
	USB_85D	USB	USB_EXTA_N	13 38
T24	USB_85D	USB	USB_EXTA_MUXED_P	38
T24	USB_85D	USB	USB_EXTA_MUXED_N	38
T24	USB_85D	USB	USB_LT1_P	38
T24	USB_85D	USB	USB_LT1_N	38
	USB_85D	USB	NC_USB_EXTCP	13 72
	USB_85D	USB	NC_USB_EXTCN	13 72
T23	USB_85D	USB	NC_USB_SDP	13 72
T23	USB_85D	USB	NC_USB_SDN	13 72
T27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	38 41 42
T27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	38 41 42
	USB_SMC	USB_85D	USB	NC_USB_SMCP	72
	USB_SMC	USB_85D	USB	NC_USB_SMCN	72
T28	USB_85D	USB	NC_USB_6P	13 72
T28	USB_85D	USB	NC_USB_6N	13 72
T28	USB_85D	USB	NC_USB_7P	13 72
T28	USB_85D	USB	NC_USB_7N	13 72
	USB_85D	USB	USB_EXTB_P	13 68 71
	USB_85D	USB	USB_EXTB_N	13 68 71
T26	USB_85D	USB	NC_USB_EXTDP	13 72
T25	USB_85D	USB	NC_USB_EXTDN	13 72
	USB_85D	USB	USB_BT_P	13 34
	USB_85D	USB	USB_BT_N	13 34
	USB_85D	USB	USB_BT_CONN_P	34 71
	USB_85D	USB	USB_BT_CONN_N	34 71
T28	USB_85D	USB	NC_USB_IRP	13 72
T28	USB_85D	USB	NC_USB_IRN	13 72
T28	USB_85D	USB	USB_TPAD_P	13 39
T28	USB_85D	USB	USB_TPAD_N	13 39
T30	USB_85D	USB	USB_TPAD_R_P	39
T30	USB_85D	USB	USB_TPAD_R_N	39
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
T22 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 38
T23 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 38
T26	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
T26	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
T23 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	38
T22 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	38
T26	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 38
T26	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 38
T22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 68 71
T22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 68 71
T26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
T26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
T22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	68 71
T22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	68 71
T26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 68
T26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 68
T26 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	13 72
T26 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	13 72
T26	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	13 72
T26	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	13 72
T25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	13 72
T25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	13 72
T25	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	13 72
T25	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	13 72

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
T25 SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
T25 SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
T25	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
T25 SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 37
T25 SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
T25	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

SYNC_MASTER=SIDLE J45 SYNC_DATE=12/10/2012

PAGE TITLE: PCH Constraints 1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 112 OF 118

SHEET: 75 OF 81

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD
CLK LPC 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH SE	*	=2x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH SE	TOP BOTTOM	=3x DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF
CLK PCIE 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE 2SAME	*	=2X DIELECTRIC	?
PCIE TXRX	*	=6X DIELECTRIC	?
PCIE 2OTHER	*	=4X DIELECTRIC	?
PCIE 2CLK	*	=7X DIELECTRIC	?
PCIECLK 2OTHER	*	=7X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE 2SAME	TOP BOTTOM	=4X DIELECTRIC	?
PCIE TXRX	TOP BOTTOM	=10X DIELECTRIC	?
PCIE 2OTHER	TOP BOTTOM	=6X DIELECTRIC	?
PCIE 2CLK	TOP BOTTOM	=10X DIELECTRIC	?
PCIECLK 2OTHER	TOP BOTTOM	=10X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	13 41 50 71
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	13 41 50 71
LPC_RESET_L	LPC_45S	LPC	LPCPLUS_RESET_L	20 50 71
SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	13 18 22 44 63 68 71
SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	13 18 22 44 63 68 71
SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	13 44
SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	13 44
SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK	13 44
SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA	13 44
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	11 52
	HDA_45S	HDA	HDA_BIT_CLK_R	11
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	11 52
	HDA_45S	HDA	HDA_SYNC_R	11
	HDA_45S	HDA	HDA_RST_R_L	11
HDA_RST_L	HDA_45S	HDA	HDA_RST_L	11 52
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	11 52
HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	52
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	11 52
	HDA_45S	HDA	HDA_SDOUT_R	11 19
	SPI_45S	SPI	SPI_CLK_R	13 50
SPI_CLK	SPI_45S	SPI	SPI_CLK	50
	SPI_45S	SPI	SPI_MOSI_R	13 50
SPI_MOSI	SPI_45S	SPI	SPI_MOSI	50
SPI_MISO	SPI_45S	SPI	SPI_MISO	13 50
	SPI_45S	SPI	SPI_CS0_R_L	13 50
SPI_CS0	SPI_45S	SPI	SPI_CS0_L	50
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P	13 20 68 71
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N	13 20 68 71
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P	13 20 68 71
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N	13 20 68 71
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P	34 71
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N	34 71
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P	13 34
[1804]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N	13 34
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P	34
[1805]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N	34
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P	13 34
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N	13 34
[1276]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P	34 71
[1276]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N	34 71
[1825] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P	36 37
[1826] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N	36 37
[1827]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P	13 37
[1828]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N	13 37
[1829] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P	13 37
[1830] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N	13 37
[1831]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P	36 37
[1832]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N	36 37
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	11 19
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	19 41
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	19 50 71
[1833]	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	11 19
[1834] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIIN	11 19
[1835] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	11
[1836] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIOUT	11 19
[1853] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P	11
[1854] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N	11
[1855] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
[1856] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
[1857] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P	11
[1858] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N	11
[1859] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P	11
[1860] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N	11
PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_P	
PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_N	
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	11 34
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	11 34
[1838]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	34 71
[1839]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	34 71
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	11 37
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	11 37
[1840]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	36 37
[1841]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	36 37
[2481] PCIE_CLK100M_FW	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11 35
[2482]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11 35

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
[1813] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTRUDER_L	11
[1814] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTVRMEN_L	11
[1815] PCH_PM_NET	PCH_45S	PCH_SE	PCH_DSWVRMEN	12
[1816] PCH_PM_NET	PCH_45S	PCH_SE	PCH_SRTCRST_L	11
[1808] PCH_PM_NET	PCH_45S	PCH_SE	PM_RSMRST_L	12 66 71
[1807] PCH_PM_NET	PCH_45S	PCH_SE	PM_SYSRST_L	12 19 41 71
[1818] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 71 76
[1817] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 71 76
[1820] PCH_PM_NET	PCH_45S	PCH_SE	PM_DSW_PWRGD	12 41 71
[1819] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_SYS_PWROK	12 18 19 41 71
[1809] PCH_PM_NET	PCH_45S	PCH_SE	PM_PWRBTN_L	12 18 41
[1806] PCH_PM_NET	PCH_45S	PCH_SE	PM_THRMTRIP_L_R	14 42
[1824] PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE_WAKE_L	12 34 36 71
[1821] PCH_PM_NET	PCH_45S	PCH_SE	PCH_RCIN_L	14
[1835] PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_P<3..0>	13 35
[1836] PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_N<3..0>	13 35
[1838] PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_P<3..0>	13 35
[1837] PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_N<3..0>	13 35
[1839]	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_P<3..0>	35
[1840]	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_N<3..0>	35

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: PCH Constraints 2

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DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 113 OF 118

SHEET: 76 OF 81

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0> 7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0> 7 23 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1> 7 24 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1> 7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0> 7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8> 7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16> 7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24> 7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32> 7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40> 7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48> 7 23 24
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7> 7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0> 7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0> 7 25 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1> 7 26 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1> 7 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0> 7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8> 7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16> 7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24> 7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32> 7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40> 7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48> 7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7> 7 25 26
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A 22 23 24 70 74
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A 22 23 24 70 74
		MEM_PWR	PP1V35_S3_MEM 23 24 25 26 46 69

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: Memory Constraints

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DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 114 OF 118
SHEET: 77 OF 81

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP 2SAME	*	=3X DIELECTRIC	?
TBTDP TXRX	*	=6X DIELECTRIC	?
TBTDP 2OTHER	*	=4X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP 2SAME	TOP BOTTOM	=4x DIELECTRIC	?
TBTDP TXRX	TOP BOTTOM	=10X DIELECTRIC	?
TBTDP 2OTHER	TOP BOTTOM	=6X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING	
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0> 28 31 72
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0> 28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0> 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0> 28 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0> 28 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1> 28 31 72
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1> 28 31 72
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N 31
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0> 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0> 28 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N 32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 28

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: Thunderbolt Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 115 OF 118

SHEET: 78 OF 81

MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI 2OTHER	*	=4X DIELECTRIC	?
MIPI 2CLK	*	=6X DIELECTRIC	?
MIPICLK 2OTHER	*	=7X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI 2OTHER	TOP BOTTOM	=6X DIELECTRIC	?
MIPI 2CLK	TOP BOTTOM	=8X DIELECTRIC	?
MIPICLK 2OTHER	TOP BOTTOM	=10X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L
	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N
		S2_MEM_PWR	PP1V35_CAM
		S2_MEM_PWR	PP0V675_CAM_VREF
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ

SYNC MASTER=SIDLE J45 SYNC DATE=12/10/2012

PAGE TITLE: Camera Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 116 OF 118

SHEET: 79 OF 81

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	SPACING		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	39 41 44 71
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	39 41 44 71
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	41 44 48
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	41 44 48
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	37 41 44 48 71
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	37 41 44 48 71
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_G3_SCL	41 44 56 57 71
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	41 44 56 57 71
SMBUS_SMC_3_SCL	SMB_45S	SMB	NC_SMBUS_SMC_3_SCL	41 43
SMBUS_SMC_3_SDA	SMB_45S	SMB	NC_SMBUS_SMC_3_SDA	41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	57
	1TO1_DIFFPAIR		CHGR_CSI_N	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	57
	1TO1_DIFFPAIR		CHGR_CSO_N	57

SYNC MASTER=SIDLE J45 SYNC DATE=12/10/2012

PAGE TITLE: SMC Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 117 OF 118

SHEET: 80 OF 81

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE 1TO1 50S	*	1 1_DIFFPAIR	50 OHM SE	50 OHM SE	50 OHM SE	1 1 DIFFPAIR	1 1 DIFFPAIR
THERM 1TO1 50S	*	1 1_DIFFPAIR	50 OHM SE	50 OHM SE	50 OHM SE	1 1 DIFFPAIR	1 1 DIFFPAIR
DIFFPAIR	*	1 1 DIFFPAIR			1 1 DIFFPAIR	1 1 DIFFPAIR	1 1 DIFFPAIR
AUDIODIFF	*	1 1_DIFFPAIR	0 1 MM	0 1 MM	10 MM	0 1 MM	0 1 MM
THERM 45S CPUVRISNS1	*	1 1_DIFFPAIR	45 OHM SE	45 OHM SE	45 OHM SE	0 2 MM	0 2 MM
THERM 1TO1 45S	*	1 1_DIFFPAIR	45 OHM SE	45 OHM SE	45 OHM SE	1 1 DIFFPAIR	1 1 DIFFPAIR
SENSE 1TO1 45S	*	1 1_DIFFPAIR	45 OHM SE	45 OHM SE	45 OHM SE	1 1 DIFFPAIR	1 1 DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	2X DIELECTRIC	?
THERM	*	2X DIELECTRIC	?
AUDIO	*	2X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU COMP	GND	*	GND P2MM
CPU VCCSENSE	GND	*	GND P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK PCIE	GND	*	GND P2MM
GND	PCIE *	*	GND P2MM
GND	SATA *	*	GND P2MM
USB	GND	*	GND P2MM
CLK PCIE	SB POWER	*	PWR P2MM
SB POWER	SATA *	*	PWR P2MM
USB	SB POWER	*	PWR P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND P2MM	*	0 20 MM	1000
PWR P2MM	*	0 20 MM	1000

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	NET TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N	47
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P	47
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_P	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_N	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_N	48
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P	47
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	47 63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	47 63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	45
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P	46
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_N	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_N	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_N	46 59
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	81
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	81
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	81
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	81
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	46
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P	46
	AUDIODIFF	AUDIO	ISNS_TBT_R_N	46
	AUDIODIFF	AUDIO	ISNS_TBT_R_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P	46
	THERM_1TO1_45S	THERM	ISNS_SSD_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P	46
	THERM_1TO1_45S	THERM	ISNS_SSD_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P	62
	THERM_1TO1_45S	THERM	P1V05S0_CS_N	62
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE_P	62
	THERM_1TO1_45S	THERM	P1V05S0_SENSE_N	62
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P	28 48
	THERM_1TO1_45S	THERM	TBT_THERMD_N	48
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P	57
	AUDIODIFF	AUDIO	CHGR_CSI_R_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P	57
	AUDIODIFF	AUDIO	CHGR_CSO_R_N	57
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_P	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_N	47

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
	AUDIODIFF	AUDIO	RSUBIN_P	53
	AUDIODIFF	AUDIO	RSUBIN_N	53
	AUDIODIFF	AUDIO	LSUBIN_P	53
	AUDIODIFF	AUDIO	LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	53 55 71
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	53 55 71
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	53 55 71
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	53 55 71
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	53 55 71
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_P	51
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_N	51
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P	
	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N	
	DIFFPAIR	AUDIO	AUD_HS_MIC_P	54 55
	DIFFPAIR	AUDIO	AUD_HS_MIC_N	54 55
	DIFFPAIR	AUDIO	HS_MIC_P	51 54
	DIFFPAIR	AUDIO	HS_MIC_N	51 54
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P	
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N	51 53
		SB_POWER	PP3V3_S5	12 14 15 17 18 19 21 31 32 34 61 64 65 66 69 70 71
		SB_POWER	PP3V3_S0	60 66 67 11 12 13 14 15 17 19 20 23 33 35 44 45 46 47 48 49 51 52 55 69 71 8 10 21 65 66 69
		SB_POWER	PP1V35_S3RS0_CPUDDR	
		GND	GND	

SYNC_MASTER=SIDLE J45 SYNC_DATE=12/10/2012

PAGE TITLE: Project Specific Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 118 OF 118

SHEET: 81 OF 81