1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# J16 MLB_IG

| REV | ECN | DESCRIPTION OF REVISION | CK APPD / DATE |
|---|---|---|---|
| | | | 2013-03-22 |

LAST_MODIFIED=Fri Mar 22 11:24:26 2013


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DRAWING
TITLE=J16 MLB_IG
ABBREV=DRAWING
LAST_MODIFIED=Fri Mar 22 11:24:26 2013

DRAWING TITLE: SCHEM,MLB IG,J16

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DRAWING NUMBER: 051-0164 | SIZE: D
REVISION: 12.4.0
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## Main BOM Variants

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|---|---|---|
| 985-0052 | PCBA,MLB_IG,DEV,J16 | DEVELOPMENT,J16_DEVEL |
| 639-4515 | PCBA,MLB_IG,J16 | J16,J16_COMMON,CPU:GOOD,SSD:Y,EEEE:FF3T |
| 639-4704 | PCBA,MLB_IG,BETTER,J16 | J16,J16_COMMON,CPU:BETTER,SSD:Y,EEEE:FGWY |
| 639-4705 | PCBA,MLB_IG,CTO,J16 | J16,J16_COMMON,CPU:CTO,SSD:Y,EEEE:FGY0 |

## BOM Groups

| BOM GROUP | BOM OPTIONS |
|---|---|
| J16_COMMON | COMMON,ALTERNATE,J16_COMMON1,J16_COMMON2,J16_PROGPARTS |
| J16_COMMON1 | XDP,SPEAKERID,TBTHV:P12V,CPUVCC:3PHASE |
| J16_COMMON2 | VDDQ:P1V35 |
| J16_PROGPARTS | SMC:PROG,BOOTROM:PROG,T29ROM:PROG,CIVROM:PROG,CAMROM:PROG |
| J16_DEVEL | XDP_CONN,LPCPLUS,DDRVREF_DAC,DEVEL_SENSORS,DEVEL_AUDIO |
| DEVEL_SENSORS | AP_ISNS:Y,HDD_IVSNS:Y,TEMPSNSDEV |
| J16_PRODUCTION | AP_ISNS:N,HDD_IVSNS:N |

ADD 'J16_PRODUCTION' AT REVA RELEASE

## CPUs

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 337S4515 | 1 | CRW,QEUZ,EEU2,C0,2.7G,65W,4+3,1.15,4M,BGA | U0500 | CRITICAL | CPU:GOOD |
| 337S4516 | 1 | CRW,QEUY,EEU2,C0,3.0G,65W,4+3,1.13,4M,BGA | U0500 | CRITICAL | CPU:BETTER |
| 337S4517 | 1 | CRW,QEUX,EEU2,C0,3.2G,65W,4+3,1.3,6M,BGA | U0500 | CRITICAL | CPU:CTO |

## ASIC Parts

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 337S4483 | 1 | LYNX POINT MOBILE,C1,QS,QE99,FCBGA695 | U1100 | CRITICAL | |
| 338S1113 | 1 | IC,TBT,CR-4C,B1,PRQ,CIO,28B 12X12 FC-CSP | U2800 | CRITICAL | |
| 343S0616 | 1 | IC,BCM57766A,CIV+,A0,8X8 | U3900 | CRITICAL | |
| 353S3908 | 1 | IC,LP85G1,LED BLKT CTLR,LLP24,B0-F | U8100 | CRITICAL | |

## Programmable Parts

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 341S3783 | 1 | IC,EFI,V0039,J16 | U5210 | CRITICAL | BOOTROM:PROG |
| 335S0807 | 1 | IC,64 MBIT SPI SERIAL FLASH | U5210 | CRITICAL | BOOTROM:BLANK |
| 341S3781 | 1 | IC,SMC,PROGRMD,V2.12A30,J16 | U5000 | CRITICAL | SMC:PROG |
| 338S1159 | 1 | IC,SMC12-A3,40MHZ/50MIPS,SCPL FW,157BGA | U5000 | CRITICAL | SMC:BLANK |
| 341S3734 | 1 | IC,EEPROM,CR,V16.2,J16 | U2890 | CRITICAL | T29ROM:PROG |
| 335S0865 | 1 | IC,EEPROM,SERIAL,256KB,MLP8 | U2890 | CRITICAL | T29ROM:BLANK |
| 341S3735 | 1 | IC,ENET SPI ROM,NYMONYX,V1.13,D7/D7I | U3990 | CRITICAL | CIVROM:PROG |
| 335S0862 | 1 | IC,SERIAL FLASH,2MBIT,2.7V,REV F | U3990 | CRITICAL | CIVROM:BLANK |
| 341S3778 | 1 | IC,CAMERA,FLASH,V7229,J16 | U4202 | CRITICAL | CAMROM:PROG |
| 335S0852 | 1 | IC,FLASH,SPI,1MBIT,3V3 | U4202 | CRITICAL | CAMROM:BLANK |

## Bar Code Labels / EEEE #'s

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 825-7896 | 1 | MLB LABEL,2D | EEEE_FF3T | CRITICAL | EEEE:FF3T |
| 825-7896 | 1 | MLB LABEL,2D | EEEE_FGY0 | CRITICAL | EEEE:FGY0 |
| 825-7896 | 1 | MLB LABEL,2D | EEEE_FGWY | CRITICAL | EEEE:FGWY |

## Schematic / PCB #'s

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 051-0164 | 1 | SCH,MLB_IG,J16 | SCH | CRITICAL | J16 |
| 820-3588 | 1 | PCBF,MLB_IG,J16 | PCB | CRITICAL | J16 |

## Alternates

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: | |
|---|---|---|---|---|---|
| 377S0147 | 377S0126 | | ALL | USB2 diodes | |
| 377S0155 | 377S0104 | | ALL | USB3 diodes | |
| 377S0124 | 377S0057 | | ALL | TVS | |
| 376S0975 | 376S1081 | | ALL | P/NCh dual FET | |
| 157S0084 | 157S0058 | | ALL | Enet magnetics | |
| 155S0578 | 155S0367 | | ALL | 120OHM EMI BEAD | |
| 128S0368 | 128S0365 | | ALL | 150UF AL POLY | |
| 138S0681 | 138S0638 | | ALL | Taiyo 10uf 805 alt | |
| 197S0479 | 197S0478 | | Y4200 | 12 MHz Cam. Xtal | |
| 341S3747 | 341S3735 | | U3990 | Enet ROM | |
| 107S0251 | 107S0249 | | ALL | Sense resistor | R5400,R5520,R5530 |
| 102S0880 | 102S0879 | | ALL | Sense resistor | R5430 |
| 197S0481 | 197S0480 | | ALL | 25MHz Xtal | |
| 138S0860 | 138S0775 | | ALL | Single-source 1uF 402 | |
| 138S0859 | 138S0788 | | ALL | Single-source 10uF | |
| 138S0706 | 138S0739 | | ALL | Single-source 1uF 201 | |

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PAGE TITLE: BOM Configuration

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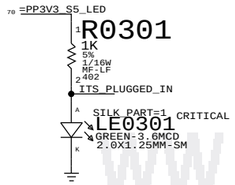
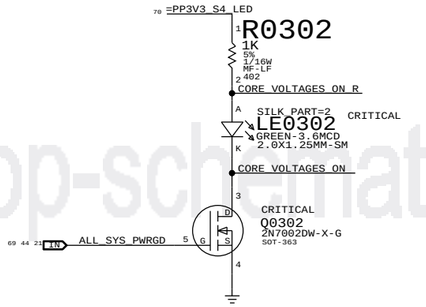
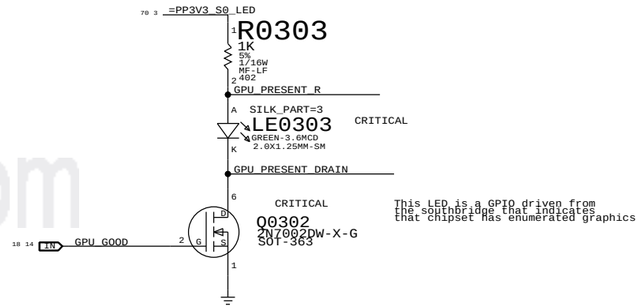
## S5 Led



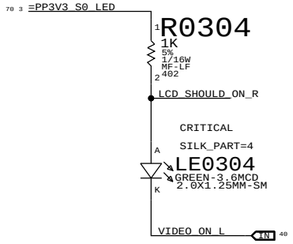

## ALL_SYS_PWRGD Led




## GPU GOOD Led




## VIDEO ON Led

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SYNC_MASTER=J16_MAX SYNC_DATE=02/11/2013

PAGE TITLE: DEBUG LEDS

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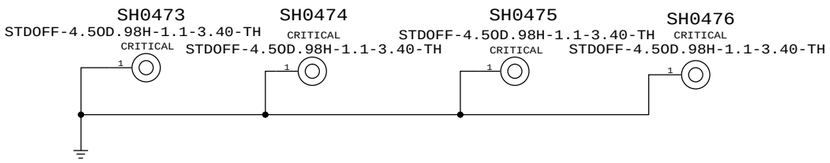
## CPU HEATSINK MOUNTING FEATURES

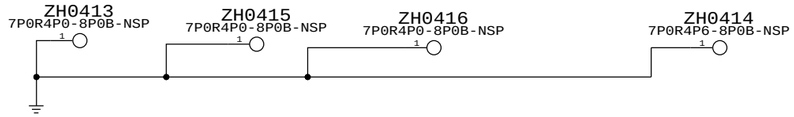



## HEATSINK STABILITY MOUNTING FEATURES

(860-1532)

## Rear Cover

998-4559 (Plated holes, 4mm inner diameter, 8mm pad)
998-5089 (ZH0414) near BLC has slightly larger hole to allow for grommet

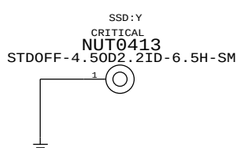



## WIRELESS CARD MTG HOLES

998-4560 (Plated holes, 2.3mm inner diameter, 4.3mm pad)

## SSD STANDOFF

APN: 860-1624

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PAGE TITLE: Holes/PD parts

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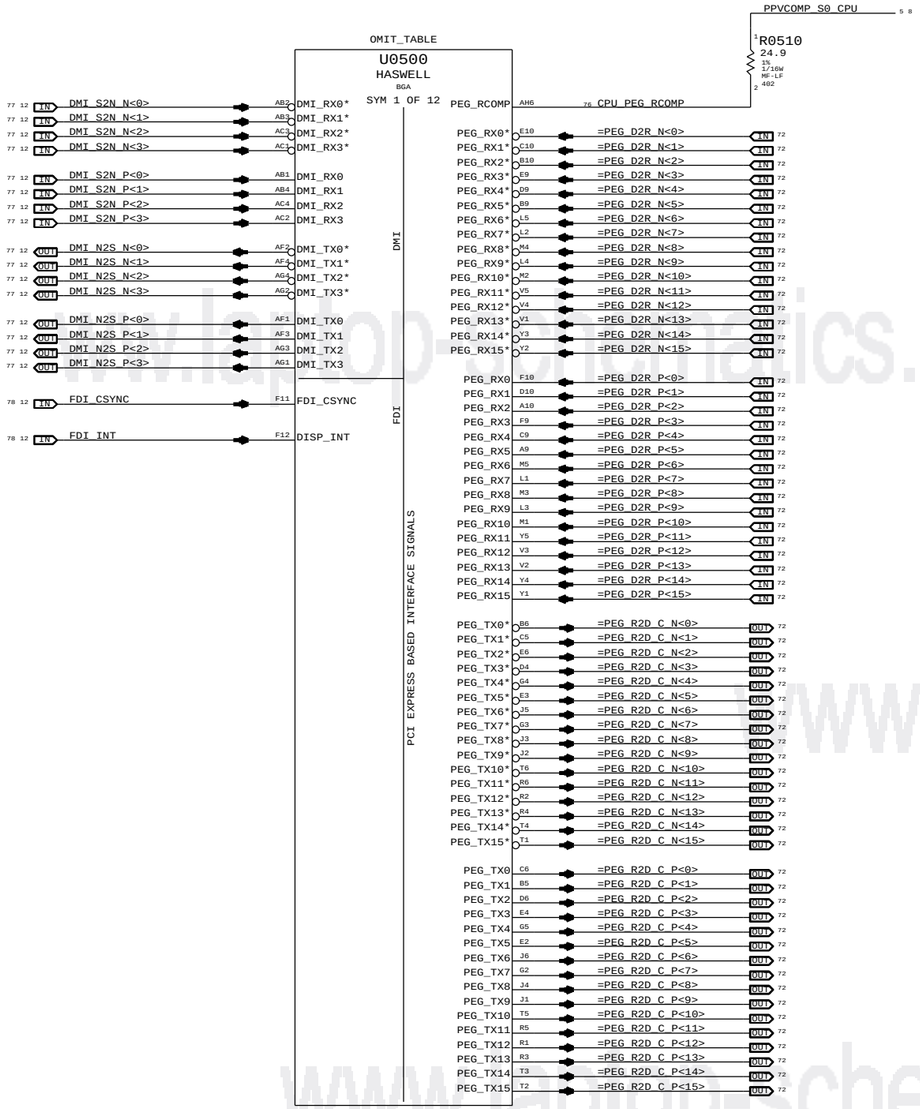


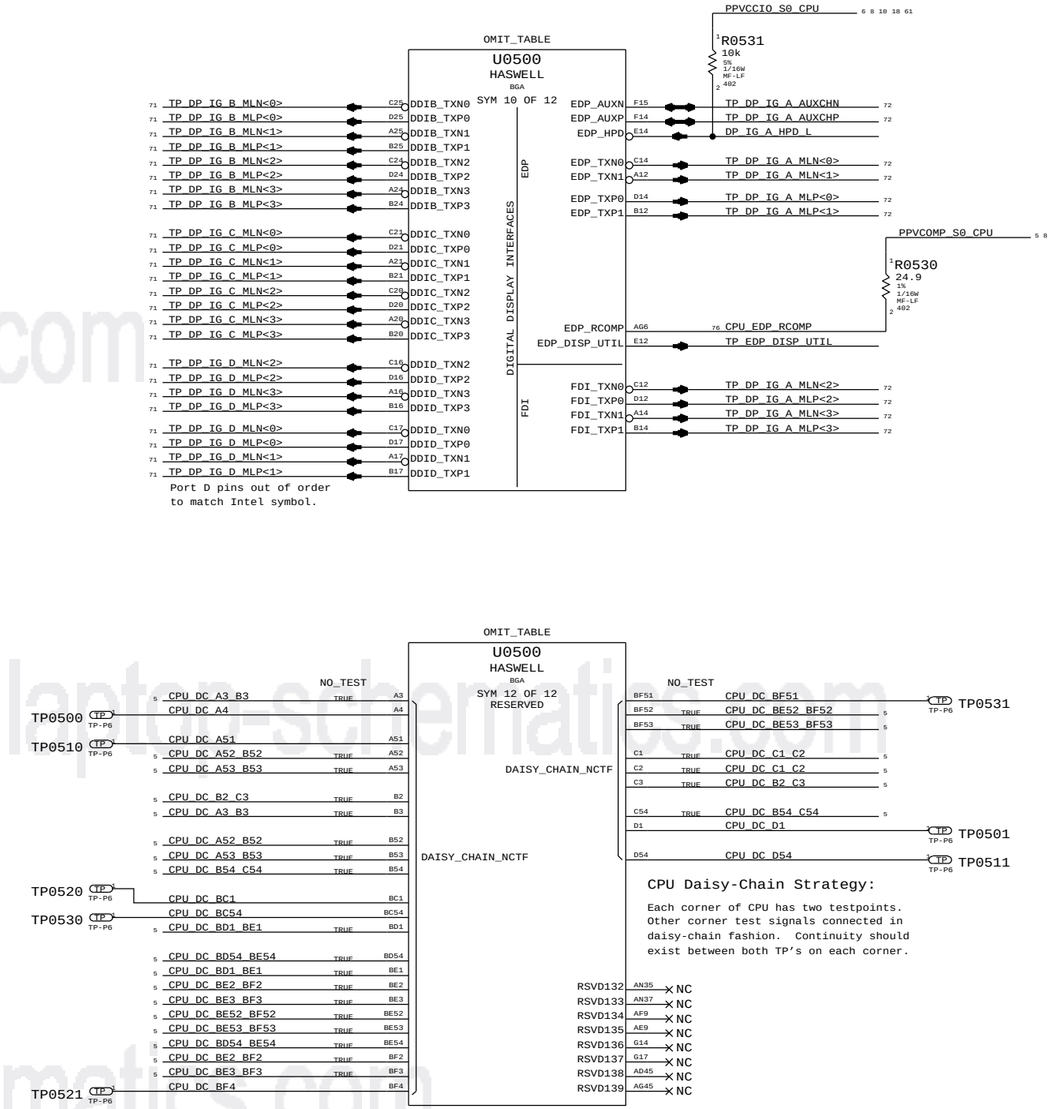


Port D pins out of order
to match Intel symbol.




### CPU Daisy-Chain Strategy:

Each corner of CPU has two testpoints.
Other corner test signals connected in
daisy-chain fashion. Continuity should
exist between both TP's on each corner.

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PAGE TITLE

# CPU DMI/PEG/FDI/RSVD

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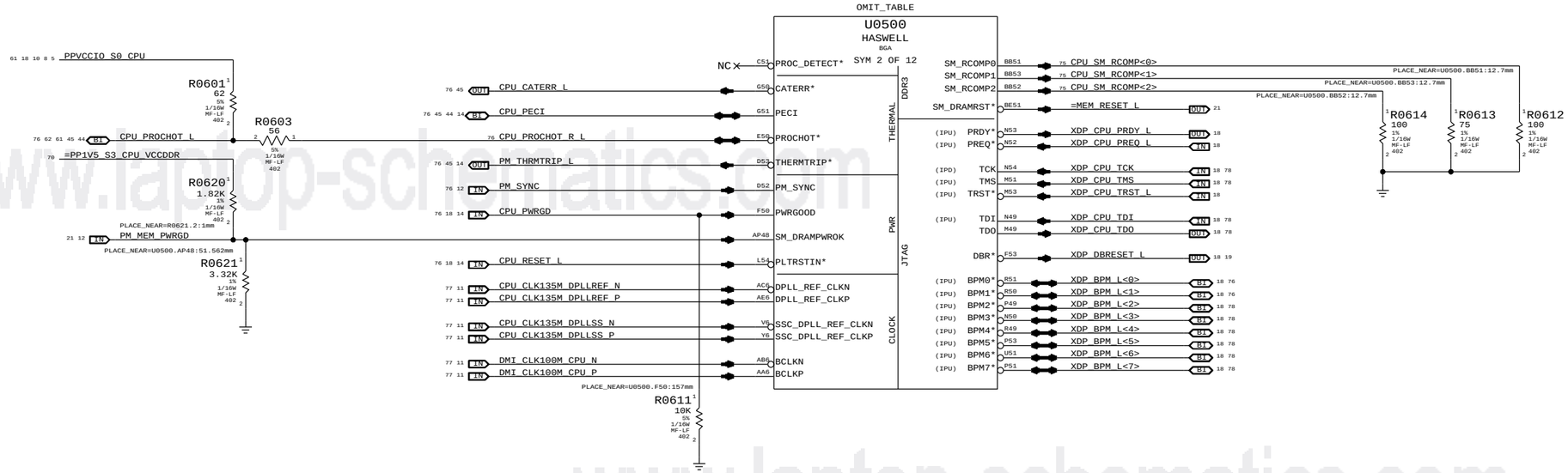
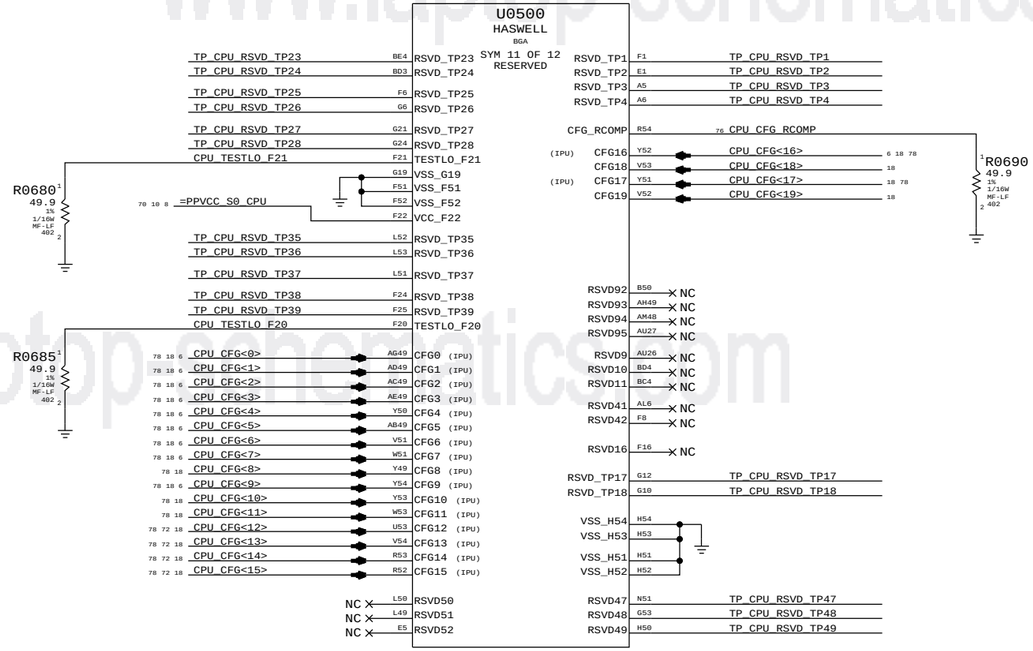
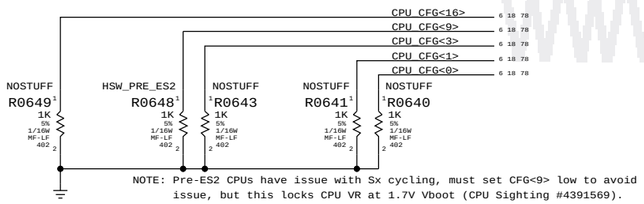


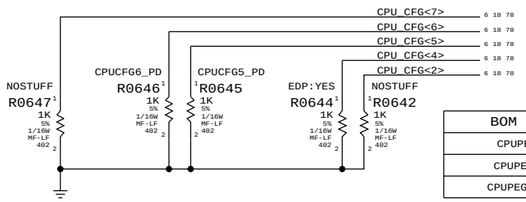




CFG [7] :PEG DEFER TRAINING — 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB  0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION — 11 = 1 X16 (DEFAULT)  10 = 2 X8  01 = RSVD  00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE — 1 = DISABLED  0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL — 1 = NORMAL OPERATION  0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL — 1 = NORMAL OPERATION  0 = LANES REVERSED

These can be placed close to J1800 and only for debug access




NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).




| BOM GROUP | BOM OPTIONS |
|---|---|
| CPUPEG:X16 | |
| CPUPEG:X8X8 | CPUCFG5_PD |
| CPUPEG:X8X4X4 | CPUCFG6_PD,CPUCFG5_PD |

SYNC MASTER=J16_DINI  SYNC_DATE=01/14/2013
PAGE TITLE: CPU Clock/Misc/JTAG/CFG

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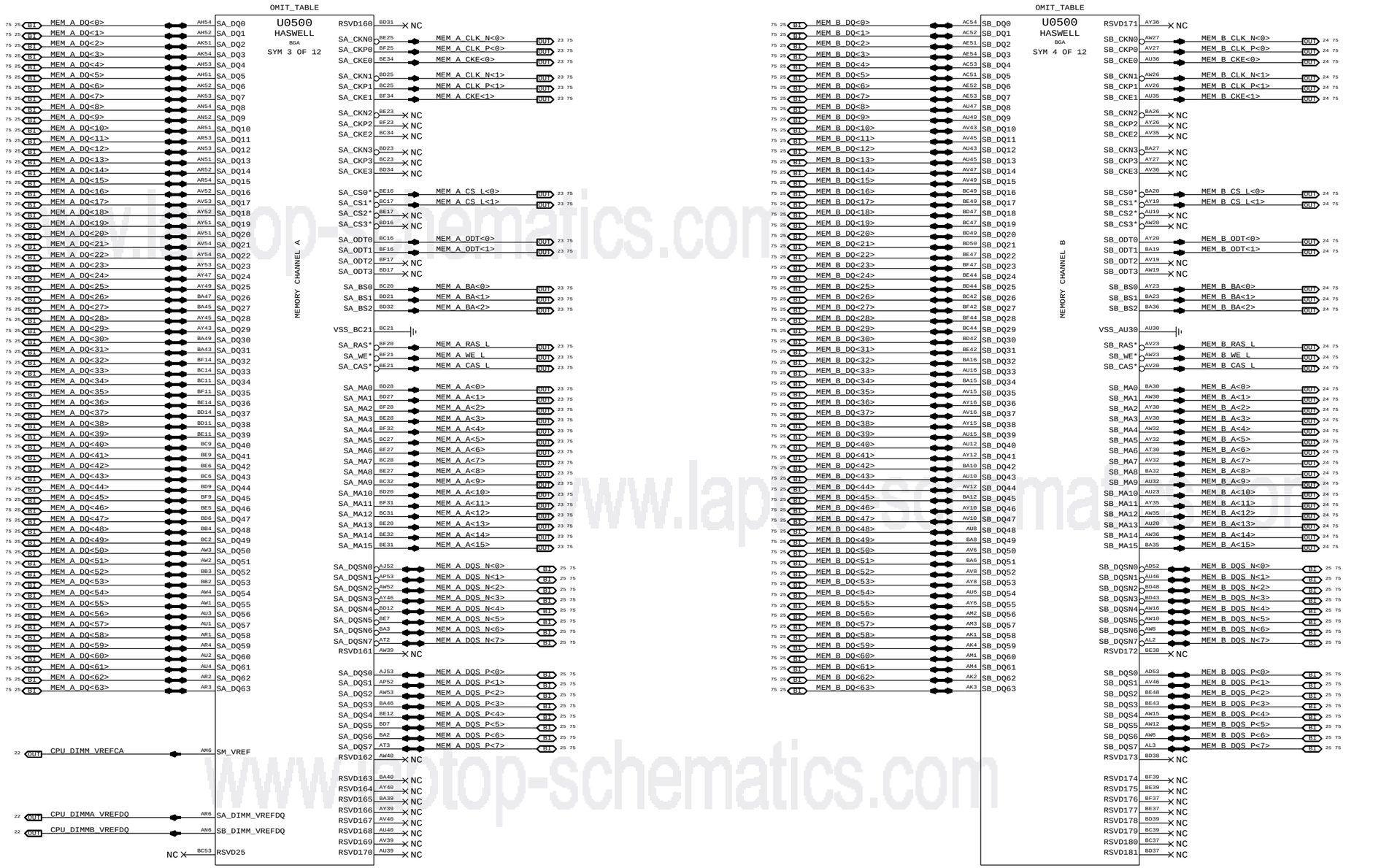


SYNC_MASTER=J16_DINI SYNC_DATE=01/14/2013

PAGE TITLE

# CPU DDR3 Interfaces

Apple Inc.

DRAWING NUMBER 051-0164 SIZE D

REVISION 12.4.0

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NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.

61 18 10 6 5 PPVCCIO_S0_CPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
Max load: 300mA

R0800 1 75 1% 1/16W MF-LF 402 2
R0802 1 110 1% 1/16W MF-LF 402 2

5 PPVCOMP_S0_CPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
Max load: 300mA

83 61 IN CPU_VIDALERT_L
R0810 1 43 5% 1/16W MF-LF 402 2
83 61 OUT CPU_VIDSCLK
R0811 1 0 5% 1/16W MF-LF 402 2
83 61 IN CPU_VIDSOUT
R0812 1 0 5% 1/16W MF-LF 402 2

R0802.2: PLACE_NEAR=U0500.J50:2.54mm
R0810.2: PLACE_NEAR=U0500.J53:38mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm

70 10 =PP1V5R1V35_S0_CPU

70 10 8 6 =PPVCC_S0_CPU
R0860 1 100 5% 1/16W MF-LF 402 2
PLACE_NEAR=U0500.C50:50.8mm
PLACE_SIDE=BOTTOM
83 61 OUT CPU_VCCSENSE_P

U0500
HASWELL
BGA
SYM 5 OF 12
OMIT_TABLE

| | | |
|---|---|---|
| NC | J17 | RSVD64 |
| NC | J21 | RSVD65 |
| NC | J26 | RSVD66 |
| NC | J31 | RSVD67 |
| | AR29 | VDDQ |
| | AR31 | |
| | AR33 | |
| | AT13 | |
| | AT19 | |
| | AT23 | |
| | AT27 | |
| | AT32 | |
| | AT36 | |
| | AV37 | |
| | AW22 | |
| | AW25 | |
| | AW29 | |
| | AW33 | |
| | AY18 | |
| | BB21 | |
| | BB22 | |
| | BB26 | |
| | BB27 | |
| | BB30 | |
| | BB31 | |
| | BB34 | |
| | BB36 | |
| | BD22 | |
| | BD26 | |
| | BD30 | |
| | BD33 | |
| | BE18 | |
| | BE22 | |
| | BE26 | |
| | BE30 | |
| | BE33 | |
| NC | AN31 | RSVD68 |
| | L6 | VCC_L6 |
| | M6 | VCC_M6 |
| NC | AN22 | RSVD69 |
| NC | AN18 | RSVD70 |
| | C50 | VCC_SENSE |
| NC | AH9 | RSVD71 |
| | D51 | VCCIO_OUT |
| NC | F17 | FC_F17 |
| | AK6 | VCOMP_OUT |
| NC | AN33 | RSVD72 |
| NC | W9 | RSVD73 |
| NC | J12 | RSVD79(VSS) |
| NC | AR49 | RSVD74 |
| | J53 | VIDALERT* |
| | J52 | VIDSCLK |
| | J50 | VIDSOUT |
| | B51 | VSS_B51 |
| 18 IN | F19 | PWR_DEBUG |
| | E52 | VSS_E52 |
| TP_CPU_RSVD_TP75 | V49 | RSVD75 |
| TP_CPU_RSVD_TP76 | U49 | RSVD76 |
| TP_CPU_IVR_ERROR | AM49 | IVR_ERROR |
| TP_CPU_RSVD_TP78 | W49 | RSVD78 |
| | V50 | VSS_V50(RSVD) |
| | AN49 | VSS_AN49(RSVD) |
| | AJ49 | VSS_AJ49(RSVD) |
| | AG50 | VSS_AG50(RSVD) |
| | AK49 | VSS_AK49(RSVD) |
| | AJ50 | VSS_AJ50(RSVD) |
| | AP49 | VSS_AP49(RSVD) |
| | AB50 | VSS_AB50(RSVD) |
| | AP50 | VSS_AP50(RSVD) |
| | AD50 | VSS_AD50(RSVD) |
| | AM50 | VSS_AM50(RSVD) |
| | A36 | VCC |
| | A38 | |
| | A39 | |
| | A42 | |
| | A43 | |
| | A45 | |
| | A46 | |
| | A48 | |
| | AA46 | |
| | AA47 | |
| | AA8 | |
| | AA9 | |

=PPVCC_S0_CPU 6 8 10 70

| | | |
|---|---|---|
| | B43 | VCC |
| | B45 | |
| | B46 | |
| | B48 | |
| | C27 | |
| | C28 | |
| | C31 | |
| | C32 | |
| | C34 | |
| | C36 | |
| | C38 | |
| | C39 | |
| | C42 | |
| | C43 | |
| | C45 | |
| | C46 | |
| | C48 | |
| | D27 | |
| | D28 | |
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| | F27 | |
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| | G46 | |
| | G48 | |
| | H11 | |
| | H12 | |
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| | H14 | |
| | H16 | |
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| | H20 | |
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| | H24 | |
| | H25 | |
| | H26 | |
| | H27 | |
| | H29 | |

Connections would be required
for 2014 CPU support.

FC_D5 D5 TP_CPU_FC_VCCST
FC_D3 D3 TP_CPU_FC_VCCST_PWRGD

OMIT_TABLE
U0500
HASWELL
BGA
SYM 6 OF 12
POWER

| | | |
|---|---|---|
| | H33 | VCC |
| | H34 | |
| | H36 | |
| | H37 | |
| | H38 | |
| | H39 | |
| | H40 | |
| | H42 | |
| | H43 | |
| | H45 | |
| | H46 | |
| | H48 | |
| | H8 | |
| | H9 | |
| | J10 | |
| | J14 | |
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| | K38 | |
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| | M27 | |
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| | N46 | |
| | N47 | |
| | N8 | |
| | N9 | |
| | P45 | |
| | P46 | |
| | P8 | |
| | R46 | |
| | R47 | |
| | R8 | |
| | R9 | |
| | T45 | |
| | T46 | |
| | U46 | |
| | U47 | |
| | U8 | |
| | U9 | |
| | V45 | |
| | V46 | |
| | V8 | |
| | W46 | |
| | W47 | |
| | W8 | |
| | Y45 | |
| | Y46 | |
| | Y8 | |
| | Y9 | |
| | AJ27 | |
| | AJ28 | |
| | AJ31 | |
| | AJ32 | |
| | AJ34 | |
| | B27 | |
| | B28 | |
| | B31 | |
| | B32 | |
| | B34 | |
| | B36 | |
| | B38 | |
| | B39 | |
| | B42 | |
| | AB45 | VCC |
| | AB46 | |
| | AB8 | |
| | AC45 | |
| | AC46 | |
| | AC47 | |
| | AD45 | |
| | AD46 | |
| | AD47 | |
| | AE45 | |
| | AE46 | |
| | AE47 | |
| | AE48 | |
| | AF8 | |
| | AG45 | |
| | AG46 | |
| | AG47 | |
| | AG48 | |
| | AH8 | |
| | AH45 | |
| | AH46 | |
| | AH47 | |
| | AH48 | |
| | AJ8 | |
| | AJ45 | |
| | AJ46 | |
| | AJ47 | |
| | AK45 | |
| | AK46 | |
| | AK47 | |
| | AK8 | |
| | AL45 | |
| | AL46 | |
| | AL8 | |
| | AL9 | |
| | AM45 | |
| | AM46 | |
| | AM47 | |
| | AM8 | |
| | AM9 | |
| | AN10 | |
| | AN12 | |
| | AN13 | |
| | AN14 | |
| | AN15 | |
| | AN16 | |
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| | AN43 | |
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| | AP10 | |
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| | AP43 | |
| | AP44 | |
| | AP46 | |
| | AP47 | |
| | AP8 | |
| | AP9 | |
| | AR35 | |
| | AR37 | |
| | AR38 | |
| | AR41 | |
| | AR43 | |
| | AR45 | |
| | AR46 | |
| | H30 | |
| | H31 | |
| | H32 | |

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CPU Power

Apple Inc.

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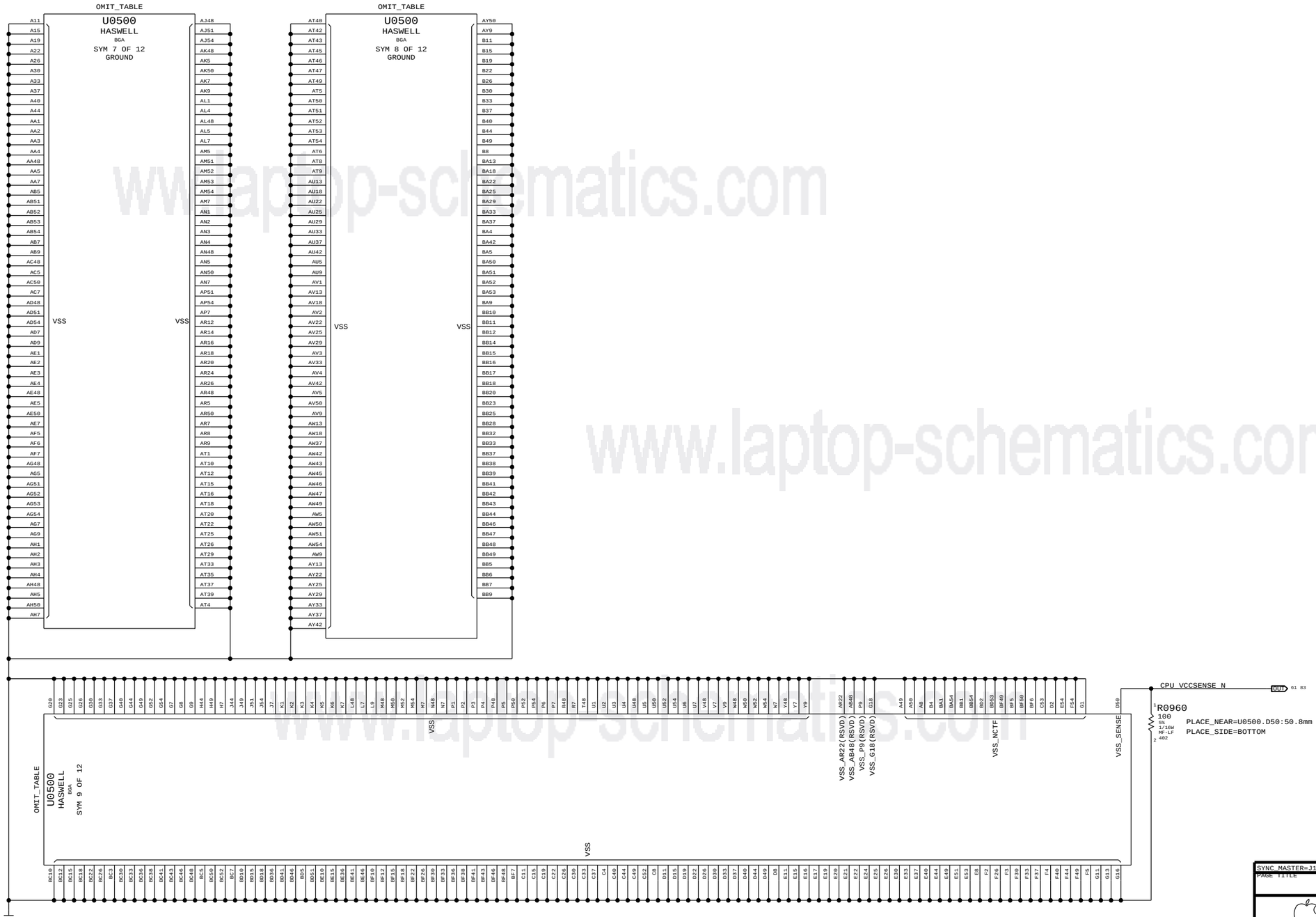


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PAGE TITLE

# CPU Ground

Apple Inc.

DRAWING NUMBER 051-0164 SIZE D

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## CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 9x 210uF 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

70 8 6 =PPVCC_S0_CPU

PLACEMENT_NOTE (C1000-C1019):
**Place on bottom side of U0500**

C1000 1UF 10% 10V X6S-CERM 0402
C1001 1UF 10% 10V X6S-CERM 0402
C1002 1UF 10% 10V X6S-CERM 0402
C1003 1UF 10% 10V X6S-CERM 0402
C1004 1UF 10% 10V X6S-CERM 0402
C1005 1UF 10% 10V X6S-CERM 0402
C1006 1UF 10% 10V X6S-CERM 0402
C1007 1UF 10% 10V X6S-CERM 0402
C1008 1UF 10% 10V X6S-CERM 0402
C1009 1UF 10% 10V X6S-CERM 0402
C1010 1UF 10% 10V X6S-CERM 0402
C1011 1UF 10% 10V X6S-CERM 0402
C1012 1UF 10% 10V X6S-CERM 0402
C1013 1UF 10% 10V X6S-CERM 0402
C1014 1UF 10% 10V X6S-CERM 0402
C1015 1UF 10% 10V X6S-CERM 0402
C1016 1UF 10% 10V X6S-CERM 0402
C1017 1UF 10% 10V X6S-CERM 0402
C1018 1UF 10% 10V X6S-CERM 0402
C1019 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1020-C1023):
**Place near U0500 on bottom side**

C1020 10UF 20% 4V X6S 0402
C1021 10UF 20% 4V X6S 0402
C1022 10UF 20% 4V X6S 0402
C1023 10UF 20% 4V X6S 0402

For noise floor mitigation of DP (C1070-C1075):

C1070 1.5PF +/-0.1PF 25V NP0-C0G 201
C1071 1.5PF +/-0.1PF 25V NP0-C0G 201
C1072 1.5PF +/-0.1PF 25V NP0-C0G 201
C1073 1.5PF +/-0.1PF 25V NP0-C0G 201
C1074 1.5PF +/-0.1PF 25V NP0-C0G 201
C1075 1.5PF +/-0.1PF 25V NP0-C0G 201

PLACEMENT_NOTE (C1024-C1045):
**Place near inductors on bottom side.**

CRITICAL C1024 10UF 20% 4V X6S 0402
CRITICAL C1025 10UF 20% 4V X6S 0402
CRITICAL C1026 10UF 20% 4V X6S 0402
CRITICAL C1027 10UF 20% 4V X6S 0402
CRITICAL C1028 10UF 20% 4V X6S 0402
CRITICAL C1029 10UF 20% 4V X6S 0402
CRITICAL C1030 10UF 20% 4V X6S 0402
CRITICAL C1031 10UF 20% 4V X6S 0402
CRITICAL C1032 10UF 20% 4V X6S 0402
CRITICAL C1033 10UF 20% 4V X6S 0402
CRITICAL C1034 10UF 20% 4V X6S 0402
CRITICAL C1035 10UF 20% 4V X6S 0402
CRITICAL C1036 10UF 20% 4V X6S 0402
CRITICAL C1037 10UF 20% 4V X6S 0402
CRITICAL C1038 10UF 20% 4V X6S 0402
CRITICAL C1039 10UF 20% 4V X6S 0402
CRITICAL C1040 10UF 20% 4V X6S 0402
CRITICAL C1041 10UF 20% 4V X6S 0402
CRITICAL C1042 10UF 20% 4V X6S 0402
CRITICAL C1043 10UF 20% 4V X6S 0402
CRITICAL C1044 10UF 20% 4V X6S 0402
CRITICAL C1045 10UF 20% 4V X6S 0402

PLACEMENT_NOTE (C1046-C1067):
**Place near inductors on bottom side.**

CRITICAL C1046 10UF 20% 4V X6S 0402
CRITICAL C1047 10UF 20% 4V X6S 0402
CRITICAL C1048 10UF 20% 4V X6S 0402
CRITICAL C1049 10UF 20% 4V X6S 0402
CRITICAL C1050 10UF 20% 4V X6S 0402
CRITICAL C1051 10UF 20% 4V X6S 0402
CRITICAL C1052 10UF 20% 4V X6S 0402
CRITICAL C1053 10UF 20% 4V X6S 0402
CRITICAL C1054 10UF 20% 4V X6S 0402
CRITICAL C1055 10UF 20% 4V X6S 0402
CRITICAL C1056 10UF 20% 4V X6S 0402
CRITICAL C1057 10UF 20% 4V X6S 0402
CRITICAL C1058 10UF 20% 4V X6S 0402
CRITICAL C1059 10UF 20% 4V X6S 0402
CRITICAL C1060 10UF 20% 4V X6S 0402
CRITICAL C1061 10UF 20% 4V X6S 0402
CRITICAL C1062 10UF 20% 4V X6S 0402
CRITICAL C1063 10UF 20% 4V X6S 0402
CRITICAL C1064 10UF 20% 4V X6S 0402
CRITICAL C1065 10UF 20% 4V X6S 0402
CRITICAL C1066 10UF 20% 4V X6S 0402
CRITICAL C1067 10UF 20% 4V X6S 0402

BULK CAPS ON REGULATOR PAGE

## CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402

70 8 =PP1V5R1V35_S0_CPU

PLACEMENT_NOTE (C1080-C1089):
**Place on bottom side of U0500**

C1080 1UF 10% 10V X6S-CERM 0402
C1081 1UF 10% 10V X6S-CERM 0402
C1082 1UF 10% 10V X6S-CERM 0402
C1083 1UF 10% 10V X6S-CERM 0402
C1084 1UF 10% 10V X6S-CERM 0402
C1085 1UF 10% 10V X6S-CERM 0402
C1086 1UF 10% 10V X6S-CERM 0402
C1087 1UF 10% 10V X6S-CERM 0402
C1088 1UF 10% 10V X6S-CERM 0402
C1089 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1090-C1097):
**Place near U0500 on bottom side**

C1090 10UF 20% 4V X6S-CERM 0603
C1091 10UF 20% 4V X6S-CERM 0603
C1092 10UF 20% 4V X6S-CERM 0603
C1093 10UF 20% 4V X6S-CERM 0603
C1094 10UF 20% 4V X6S-CERM 0603
C1095 10UF 20% 4V X6S-CERM 0603
C1096 10UF 20% 4V X6S-CERM 0603
C1097 10UF 20% 4V X6S-CERM 0603

BULK CAPS ON REGULATOR PAGE

## CPU VCCIO Decoupling

Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

61 18 8 6 5 PPVCCIO_S0_CPU

C1079 0.01UF 10% 16V X7R-CERM 0402

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

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OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(1 OF 11)

RTC
SATA
AZALIA
JTAG

PCH_CLK32K_RTCX1 — RTCX1 B5
PCH_CLK32K_RTCX2 — RTCX2 B4
PCH_SRTCRST_L — SRTCRST* B9
PCH_INTRUDER_L — INTRUDER* A8
PCH_INTVRMEN_L — INTVRMEN G10
RTC_RESET_L — RTCRST* D9

HDA_BIT_CLK — R1110 33 — HDA_BIT_CLK_R — HDA_BCLK B25
HDA_SYNC — R1111 33 — HDA_SYNC_R — HDA_SYNC A22 (IPD-boot)
PCH_SPKR — SPKR AL10 (IPD-PLTRST#)
HDA_RST_L — R1112 33 — HDA_RST_R_L — HDA_RST* C24
HDA_SDIN0 — HDA_SDI0 L22 (IPD)
TP_HDA_SDIN1 — HDA_SDI1 K22 (IPD)
TP_HDA_SDIN2 — HDA_SDI2 G22 (IPD)
TP_HDA_SDIN3 — HDA_SDI3 F22 (IPD)
HDA_SDOUT — R1113 33 — HDA_SDOUT_R — HDA_SDO A24 (IPD-boot)
DP_TBT_SEL — DOCKEN*/GPIO33 B17 (IPD-DOCKENB#)
ENET_MEDIA_SENSE — HDA_DOCK_RST*/GPIO13 C22

XDP_PCH_TCK — JTAG_TCK AB3 (IPD)
XDP_PCH_TMS — JTAG_TMS AD1 (IPU)
XDP_PCH_TDI — JTAG_TDI AE2 (IPU)
XDP_PCH_TDO — JTAG_TDO AD3
NC — TP25 F8
NC — TP22 C26
NC — TP20 A86

SATA_RXN0 BC8 — SATA_HDD_D2R_N — 33 78
SATA_RXP0 BE8 — SATA_HDD_D2R_P — 33 78
SATA_TXN0 AW8 — SATA_HDD_R2D_C_N — 33 78
SATA_TXP0 AY8 — SATA_HDD_R2D_C_P — 33 78
SATA_RXN1 BC10 — NC
SATA_RXP1 BE10 — NC
SATA_TXN1 AV10 — NC
SATA_TXP1 AW10 — NC
SATA_RXN2 BB9 — NC
SATA_RXP2 BD9 — NC
SATA_TXN2 AY13 — NC
SATA_TXP2 AW13 — NC
SATA_RXN3 BC12 — NC
SATA_RXP3 BE12 — NC
SATA_TXN3 AR13 — NC
SATA_TXP3 AT13 — NC

SATA_RXN4/PERN1 BD13 — SSD_D2R_N<0> — 33 78
SATA_RXP4/PERP1 BB13 — SSD_D2R_P<0> — 33 78
SATA_TXN4/PETN1 AV15 — SSD_R2D_N<0> — 33 78
SATA_TXP4/PETP1 AW15 — SSD_R2D_P<0> — 33 78
SATA_RXN5/PERN2 BC14 — SSD_D2R_N<1> — 33 78
SATA_RXP5/PERP2 BE14 — SSD_D2R_P<1> — 33 78
SATA_TXN5/PETN2 AP15 — SSD_R2D_N<1> — 33 78
SATA_TXP5/PETP2 AR15 — SSD_R2D_P<1> — 33 78
SATA_RCOMP AY5 — PCH_SATA_RCOMP — 78
SATALED* AP3 — PCH_SATALED_L — 11 33
SATA0GP/GPIO21 AT1 — DP_AUXIO_EN — 11 18 29 30
SATA1GP/GPIO19 (IPU-PLTRST#) AU2 — SATARDRVR_EN — 11 18
SATA_IREF BD4
TP9 BA2 — NC
TP8 BB2 — NC

SATA Port assignments:

PRIMARY HDD

SSD

=PP1V5_S0_PCH_SATA — R1130 7.5K 1% 1/20W MF 201 — PLACE_NEAR=U1100.AY5:2.54mm

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(2 OF 11)

CLOCKS

PCIE_CLK100M_SSD_N — CLKOUT_PCIE_N0 Y43
PCIE_CLK100M_SSD_P — CLKOUT_PCIE_P0 Y45
SSD_CLKREQ_L — PCIECLKRQ0*/GPIO73 AB1
PCIE_CLK100M_ENET_N — CLKOUT_PCIE_N1 AA44
PCIE_CLK100M_ENET_P — CLKOUT_PCIE_P1 AA42
ENET_CLKREQ_L — PCIECLKRQ1*/GPIO18 AF1
PCIE_CLK100M_AP_N — CLKOUT_PCIE_N2 AB43
PCIE_CLK100M_AP_P — CLKOUT_PCIE_P2 AB45
AP_CLKREQ_L — PCIECLKRQ2*/GPIO20/SMI* AF3
PCIE_CLK100M_TBT_N — CLKOUT_PCIE_N3 AD43
PCIE_CLK100M_TBT_P — CLKOUT_PCIE_P3 AD45
PCH_CLKRQ3_L_GPIO25 — PCIECLKRQ3*/GPIO25 T3
NC — CLKOUT_PCIE_N4 AF43
NC — CLKOUT_PCIE_P4 AF45
TBT_CLKREQ_L — PCIECLKRQ4*/GPIO26 V3
NC — CLKOUT_PCIE_N5 AE44
NC — CLKOUT_PCIE_P5 AE42
PCH_CLKRQ5_L_GPIO44 — PCIECLKRQ5*/GPIO44 AA2 (IPU-RSMRST#)
NC — CLKOUT_PCIE_N6 AB40
NC — CLKOUT_PCIE_P6 AB39
PEG_CLKREQ_L — PCIECLKRQ6*/GPIO45 AE4
NC — CLKOUT_PCIE_N7 AJ44
NC — CLKOUT_PCIE_P7 AJ42
PCH_CLKRQ7_L_GPIO46 — PCIECLKRQ7*/GPIO46 Y3 (IPU-RSMRST#)
NC — CLKOUT_ITPXDP_N AH43 (IPD-PWROK)
NC — CLKOUT_ITPXDP_P AH45 (IPD-PWROK)
LPC_CLK33M_SMC_R — CLKOUT_33MHZ0 D44 (IPD-PWROK)
LPC_CLK33M_LPCPLUS_R — CLKOUT_33MHZ1 E44 (IPD-PWROK)
TP_PCI_CLK33M_OUT2 — CLKOUT_33MHZ2 B42 (IPD-PWROK)
TP_PCI_CLK33M_OUT3 — CLKOUT_33MHZ3 F41 (IPD-PWROK)
PCH_CLK33M_PCIOUT — CLKOUT_33MHZ4 A40 (IPD-PWROK)

CLKOUT_PEG_A_N AB35 — NC
CLKOUT_PEG_A_P AB36 — NC
PEG_A_CLKRQ*/GPIO47 AF6 — PCH_PEGCLKRQA_L_GPIO47 — 11
CLKOUT_PEG_B_N Y39 — NC
CLKOUT_PEG_B_P Y38 — NC
PEG_B_CLKRQ*/GPIO56 U4 — PCH_PEGCLKRQB_L_GPIO56 — 11
CLKOUT_DMI_N AF39 — DMI_CLK100M_CPU_N — 6 77
CLKOUT_DMI_P AF40 — DMI_CLK100M_CPU_P — 6 77
CLKOUT_DP_N AJ40 — CPU_CLK135M_DPLLSS_N — 6 77
CLKOUT_DP_P AJ39 — CPU_CLK135M_DPLLSS_P — 6 77
CLKOUT_DPNS_N AF35 — CPU_CLK135M_DPLLREF_N — 6 77
CLKOUT_DPNS_P AF36 — CPU_CLK135M_DPLLREF_P — 6 77
CLKIN_DMI_N AY24 — PCIE_CLK100M_PCHN — R1196 10K
CLKIN_DMI_P AW24 — PCIE_CLK100M_PCHP — R1195 10K
CLKIN_GND_N AR24 — PCH_CLKIN_GNDN — R1171 10K
CLKIN_GND_P AT24 — PCH_CLKIN_GNDP — R1170 10K
CLKIN_DOT96_N H33 — PCH_CLK96M_DOTN — R1192 10K
CLKIN_DOT96_P G33 — PCH_CLK96M_DOTP — R1191 10K
CLKIN_SATA_N BE6 — PCH_CLK100M_SATAN — R1194 10K
CLKIN_SATA_P BC6 — PCH_CLK100M_SATAP — R1193 10K
REFCLK14IN F45 — PCH_CLK14P3M_REFCLK — R1197 10K
CLKIN_33MHZLOOPBACK D17 — PCH_CLK33M_PCIIN — 19 79
XTAL25_IN AM43 — SYSCLK_CLK25M_SB_R — 79
XTAL25_OUT AL44 — NC
CLKOUTFLEX0/GPIO64 C40 — TP_PCH_GPIO64_CLKOUTFLEX0 — 72
CLKOUTFLEX1/GPIO65 F38 — TP_PCH_GPIO65_CLKOUTFLEX1 — 72
CLKOUTFLEX2/GPIO66 F36 — TP_PCH_GPIO66_CLKOUTFLEX2 — 72
CLKOUTFLEX3/GPIO67 F39 — TP_PCH_GPIO67_CLKOUTFLEX3 — 72
ICLK_IREF AM45 — =PP1V5_S0_PCH_CLK — 19 70
TP19 AD39 — NC
TP18 AD38 — NC
DIFFCLK_BIASREF AN44 — PCH_DIFFCLK_BIASREF — R1190 7.5K 1% 1/20W MF 201 — =PP1V5_S0_VCCVRM_BIAS — 17
PLACE_NEAR=U1100.AN44:2.54mm

Unused clock terminations for FCIM Mode

R1172 340 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_SB — 19 79
1.5V -> 1.1V
R1173 1K 1% 1/20W MF 201

=PPVRTC_G3_PCH — 12 15 70
R1100 330K 5% 1/20W MF 201
R1101 1M 5% 1/20W MF 201
R1102 20K 5% 1/20W MF 201
R1103 20K 5% 1/20W MF 201
PCH_SRTCRST_L — 11
PCH_INTRUDER_L — 11
PCH_INTVRMEN_L — 11
RTC_RESET_L — 11 19 45
C1102 1UF 10% 10V X5R 402
C1103 1UF 10% 10V X5R 402

=PP3V3_SUS_PCH_GPIO — 12 13 14 70
=PP3V3_S0_PCH_GPIO — 12 14 28 70

R1177 4.7K — PCH_SPKR — 11
R1176 10K — DP_TBT_SEL — 11 41 58
R1178 4.7K — PCH_SATALED_L — 11 33
R1134 10K — DP_AUXIO_EN — 11 18 29 30
R1133 10K — SATARDRVR_EN — 11 18
R1143 10K — SSD_CLKREQ_L — 11 33
R1142 10K — ENET_CLKREQ_L — 11 18 35
R1169 10K — AP_CLKREQ_L — 11 18 32
R1144 10K — PCH_CLKRQ3_L_GPIO25 — 11
R1145 10K — TBT_CLKREQ_L — 11 28
R1147 10K — PCH_CLKRQ5_L_GPIO44 — 11
R1114 10K — PEG_CLKREQ_L — 11
R1115 10K — PCH_CLKRQ7_L_GPIO46 — 11
R1146 10K — PCH_PEGCLKRQA_L_GPIO47 — 11
R1148 10K — PCH_PEGCLKRQB_L_GPIO56 — 11
R1179 10K — ENET_MEDIA_SENSE — 11 35 80

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.

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PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK

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OMIT_TABLE

U1100 LYNXPOINT MOBILE FCBGA (4 OF 11)

DMI_RXN0 AW22 ← DMI_N2S_N<0> (77 5 IN)
DMI_RXN1 AR20 ← DMI_N2S_N<1> (77 5 IN)
DMI_RXN2 AP17 ← DMI_N2S_N<2> (77 5 IN)
DMI_RXN3 AV20 ← DMI_N2S_N<3> (77 5 IN)
DMI_RXP0 AY22 ← DMI_N2S_P<0> (77 5 IN)
DMI_RXP1 AP20 ← DMI_N2S_P<1> (77 5 IN)
DMI_RXP2 AR17 ← DMI_N2S_P<2> (77 5 IN)
DMI_RXP3 AW20 ← DMI_N2S_P<3> (77 5 IN)
DMI_TXN0 BD21 → DMI_S2N_N<0> (77 5 OUT)
DMI_TXN1 BE20 → DMI_S2N_N<1> (77 5 OUT)
DMI_TXN2 BD17 → DMI_S2N_N<2> (77 5 OUT)
DMI_TXN3 BE18 → DMI_S2N_N<3> (77 5 OUT)
DMI_TXP0 BB21 → DMI_S2N_P<0> (77 5 OUT)
DMI_TXP1 BC20 → DMI_S2N_P<1> (77 5 OUT)
DMI_TXP2 BB17 → DMI_S2N_P<2> (77 5 OUT)
DMI_TXP3 BC18 → DMI_S2N_P<3> (77 5 OUT)
DMI_IREF BE16 ← =PP1V5_S0_PCH_RCOMP (70 13 12); R1200 7.5K 1% 1/20W MF 201; PLACE_NEAR=U1100.AY17:12.7mm
TP12 AW17 — NC
TP7 AV17 — NC
DMI_RCOMP AY17 ← PCH_DMI_RCOMP (77)

FDI_RXN0 AJ35 — NC
FDI_RXN1 AL35 — NC
FDI_RXP0 AJ36 — NC
FDI_RXP1 AL36 — NC
TP16 AV43 — NC
TP5 AY45 — NC
TP15 AV45 — NC
TP10 AW44 — NC
FDI_CSYNC AL39 → FDI_CSYNC (OUT 5 78)
FDI_INT AL40 → FDI_INT (OUT 5 78)
FDI_IREF AT45 ← =PP1V5_S0_PCH_RCOMP (12 13 70); R1210 7.5K 1% 1/20W MF 201; PLACE_NEAR=U1100.AR44:12.7mm
FDI_RCOMP AR44 ← PCH_FDI_RCOMP (78)

DMI
FDI

SUSACK* R6 ← PCH_SUSACK_L (IPU)
SYS_RESET* AM1 ← PM_SYSRST_L (44 19 IN)
SYS_PWROK AD7 ← PM_PCH_SYS_PWROK (69 45 18 IN)
PWROK F10 ← PM_PCH_PWROK (69 39 20 18 IN)
APWROK AB7 ← PM_PCH_APWROK (69 IN)
DRAMPWROK H3 ← PM_MEM_PWRGD (21 6 OUT)
RSMRST* J2 ← PM_RSMRST_PCH_L (69 18 12 IN)
SUSWARN*/SUSPWRNACK/GPIO30 J4 ← PCH_SUSWARN_L
PWRBTN* K1 ← PM_PWRBTN_L (44 18 12 IN) (IPU)
ACPRESENT/GPIO31 E6 ← PCH_GPIO31 (12) (IPD-DeepSx)
BATLOW*/GPIO72 K7 ← PCH_GPIO72 (12 IN)
RI* N4 ← PCH_RI_L; R1205 10K 5% 1/20W MF 201 ← =PP3V3_SUS_PCH_GPIO (70 14 13 11)
TP21 AB10 — NC
SLP_WLAN*/GPIO29 D2 ← TP_PCH_SLP_WLAN_L

SYSTEM POWER MANAGEMENT

DSWVRMEN C8 ← PCH_DSWVRMEN
DPWROK L13 ← PM_RSMRST_PCH_L (IN 12 18 69)
WAKE* K3 (IPD-DeepSx) ← PCIE_WAKE_L (IN 12 32 36)
CLKRUN* AN7 ↔ PM_CLKRUN_L (BI 12 44 45 46)
SUS_STAT*/GPIO61 U7 → LPC_PWRDWN_L (OUT 20 44 46)
SUSCLK/GPIO62 (IPU-RSMRST#) Y6 → PM_CLK32K_SUSCLK_R (OUT 45 79)
SLP_S5*/GPIO63 Y7 → PM_SLP_S5_L (OUT 12 32 44 68)
SLP_S4* C6 → PM_SLP_S4_L (OUT 12 44 68)
SLP_S3* H1 → PM_SLP_S3_L (OUT 12 21 36 44 45 68 69)
SLP_A* E3 → TP_PM_SLP_A_L
SLP_SUS* F1 → PM_SLP_SUS_L (OUT 12)
PMSYNCH AY3 ← PM_SYNC (OUT 6 76)
SLP_LAN* G5 → TP_PCH_SLP_LAN_L

R1286 0 5% 1/20W MF 0201 ← PM_PCH_PWROK
R1209 10K 5% 1/20W MF 201 ← PCH_DSWVRMEN
R1215 330K 5% 1/20W MF 201 ← =PPVRTC_G3_PCH (11 15 70)

OMIT_TABLE

U1100 LYNXPOINT MOBILE FCBGA (5 OF 11)

VGA_BLUE T45 — NC
VGA_GREEN U44 — NC
VGA_RED V45 — NC
VGA_DDC_CLK M43 — NC
VGA_DDC_DATA M45 — NC
VGA_HSYNC N42 — NC
VGA_VSYNC N44 — NC
DAC_IREF U40
VGA_IRTN U39

VGA DAC Disabled per SB DG v1.0 (Table 12-18).

CRT
DISPLAY

DDPB_CTRLCLK R40 → TP_DP_IG_B_DDC_CLK (71)
DDPB_CTRLDATA R39 (IPD-PLTRST#) → TP_DP_IG_B_DDC_DATA (71)
DDPC_CTRLCLK R35 → TP_DP_IG_C_DDC_CLK (71)
DDPC_CTRLDATA R36 (IPD-PLTRST#) → TP_DP_IG_C_DDC_DATA (71)
DDPD_CTRLCLK N40 → TP_DP_IG_D_DDC_CLK (71)
DDPD_CTRLDATA N38 (IPD-PLTRST#) → TP_DP_IG_D_DDC_DATA (71)
DDPB_AUXN H45 → TP_DP_IG_B_AUXCHN (71)
DDPC_AUXN K43 → TP_DP_IG_C_AUXCHN (71)
DDPD_AUXN J42 → TP_DP_IG_D_AUXCHN (71)
DDPB_AUXP H43 → TP_DP_IG_B_AUXCHP (71)
DDPC_AUXP K45 → TP_DP_IG_C_AUXCHP (71)
DDPD_AUXP J44 → TP_DP_IG_D_AUXCHP (71)
DDPB_HPD K40 → TP_DP_IG_B_HPD (71)
DDPC_HPD K38 → TP_DP_IG_C_HPD (71)
DDPD_HPD H39 → TP_DP_IG_D_HPD (71)

EDP

EDP_BKLTCTL N36 — NC
EDP_BKLTEN K36 — NC
EDP_VDDEN G36 — NC

PCI

PIRQA* H20 ← PCI_INTA_L; R1260 10K
PIRQB* L20 ← PCI_INTB_L; R1261 10K
PIRQC* K17 ← PCI_INTC_L; R1262 10K
PIRQD* M20 ← PCI_INTD_L; R1263 10K
PIRQE*/GPIO2 G17 → SDCONN_OC_L (IN 12 37)
PIRQF*/GPIO3 F17 → AUD_IP_PERIPHERAL_DET (IN 12 58)
PIRQG*/GPIO4 L15 → TBT_PWR_REQ_L (IN 12 26)
PIRQH*/GPIO5 M15 → AUD_I2C_INT_L (IN 12 56)
PME* AD10 (IPU) → TP_PCI_PME_L
PLTRST* Y11 → PLT_RESET_L (OUT 20)
(IPU-PWROK&PCIRST#)

GPIO50 A12 → ENET_LOW_PWR_PCH (20 12 OUT)
GPIO52 B13 → AUD_IPHS_SWITCH_EN_PCH (20 12 OUT)
GPIO54 C12 → BT_PWR_RST_L (32 12 OUT)
GPIO51 C10 ← TP_PCH_STRP_BBS1
GPIO53 A10 ← TP_PCH_STRP_ESI_L
GPIO55 AL6 ← PCH_STRP_TOPBLK_SWP_L (45 IN)

=PP3V3_S0_PCH_GPIO (70 28 14 12 11)
=PP3V3_S5_PCH_GPIO (70)
=PP3V3_S0_PCH_GPIO (11 12 14 28 70)

R1226 10K — PCH_GPIO31 (12)
R1239 3.0K — PM_PWRBTN_L (12 18 44)
R1240 10K — PCH_GPIO72 (12)
R1291 10K NO STUFF — PM_CLKRUN_L (12 44 45 46)
R1216 10K — ENET_LOW_PWR_PCH (12 20)
R1217 100K — AUD_IPHS_SWITCH_EN_PCH (12 20)
R1218 10K — BT_PWR_RST_L (12 32)
R1230 10K — SDCONN_OC_L (12 37)
NO STUFF Redundant to pull-up on audio page
R1214 100K — AUD_IP_PERIPHERAL_DET (12 58)
R1231 10K — TBT_PWR_REQ_L (12 26)
NO STUFF Redundant to pull-up on audio page
R1233 10K — AUD_I2C_INT_L (12 56)
R1225 1K — PCIE_WAKE_L (IN 12 32 36); MAKE_BASE=TRUE — =TBT_WAKE_L (IN 26)
R1224 100K — PM_SLP_S3_L (12 21 36 44 45 68 69)
R1221 100K — PM_SLP_S4_L (12 44 68)
R1222 100K — PM_SLP_S5_L (12 32 44 68)
R1223 100K — PM_SLP_SUS_L (12)

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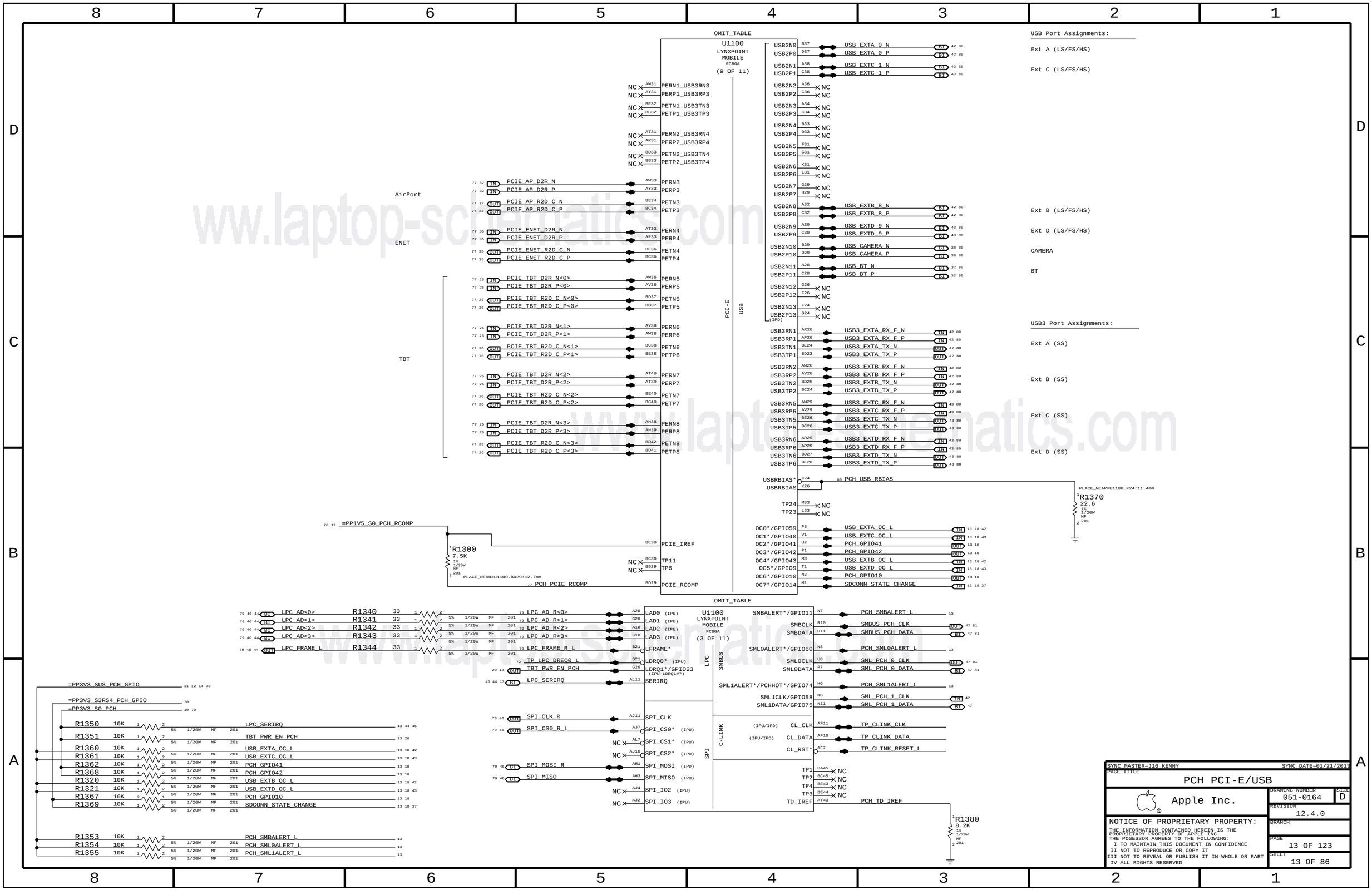

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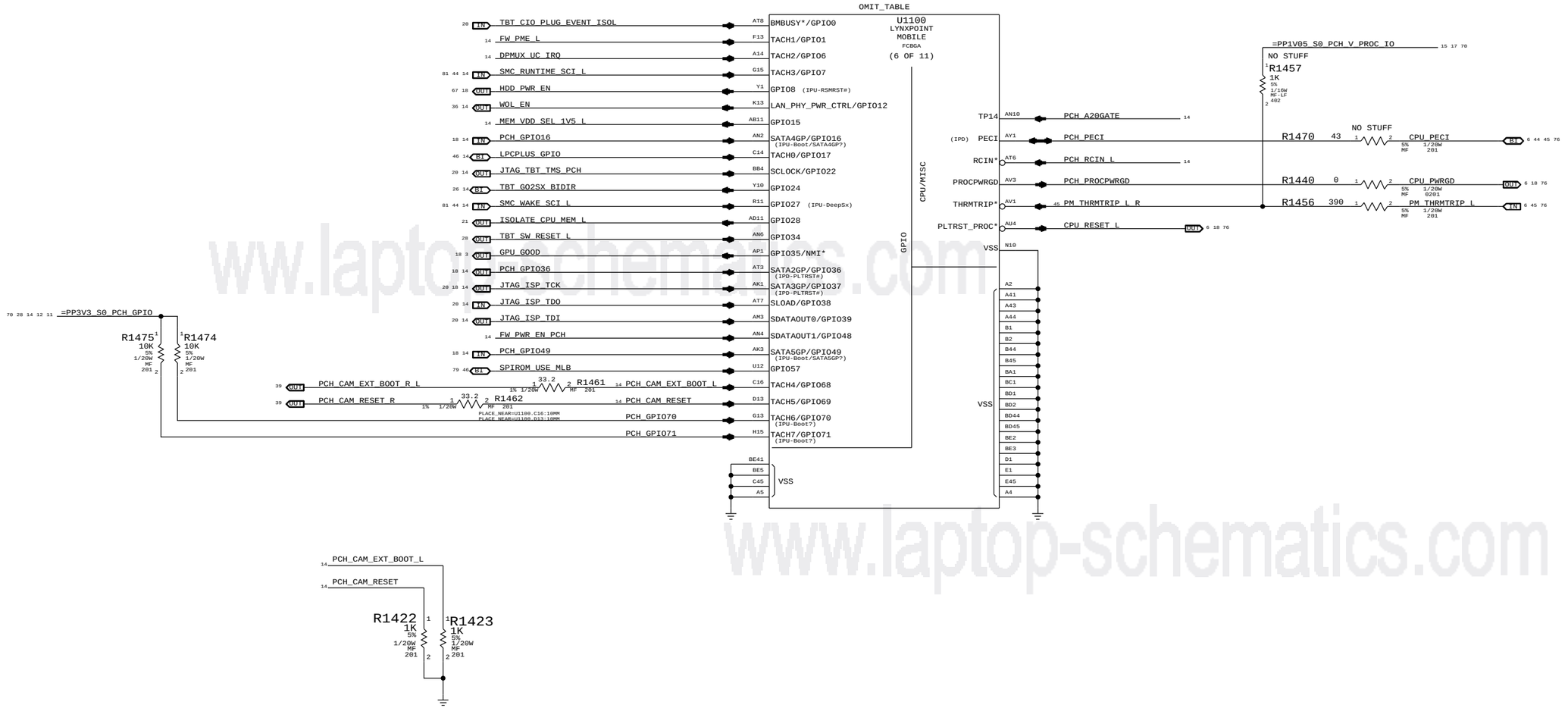


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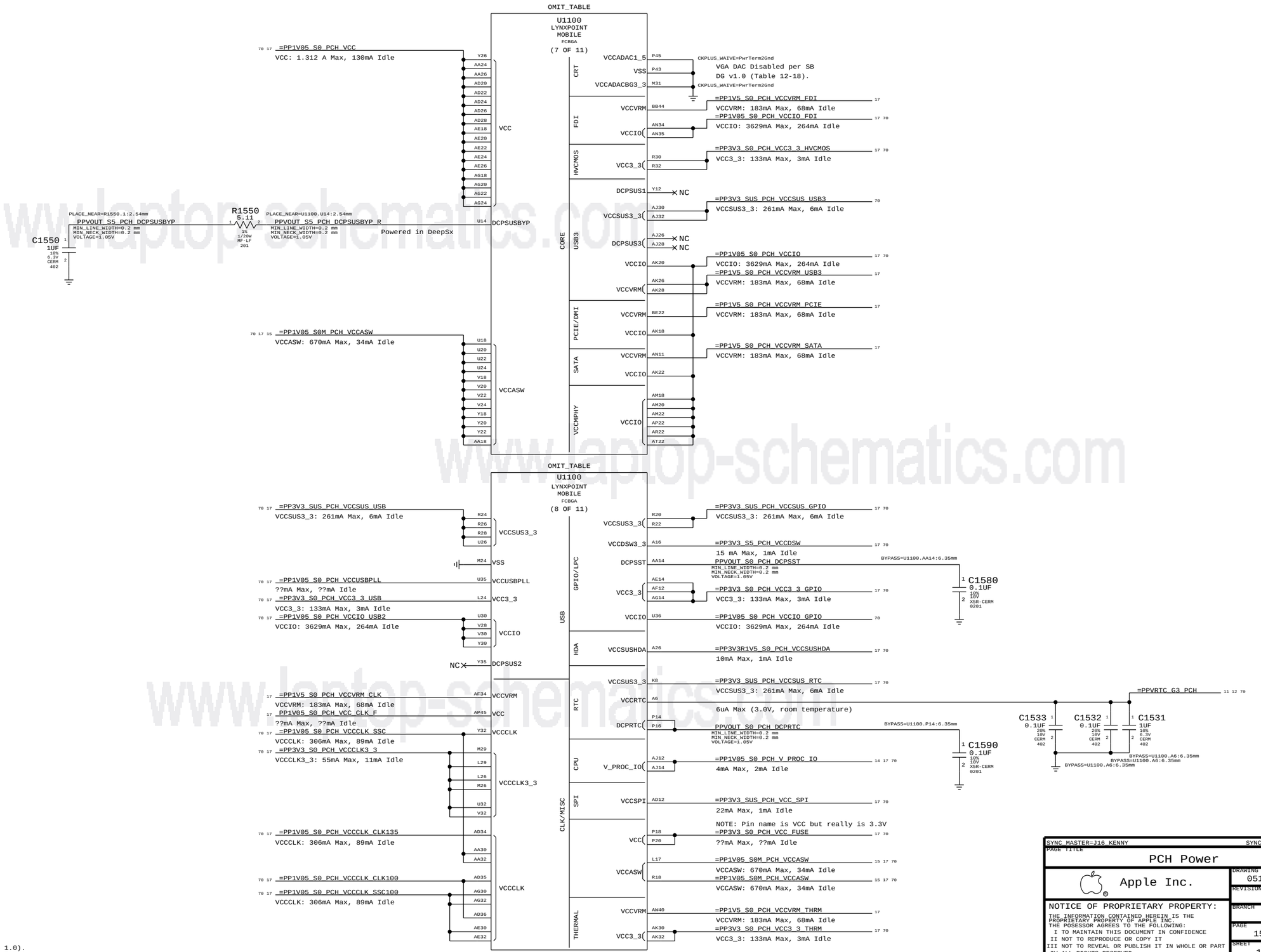


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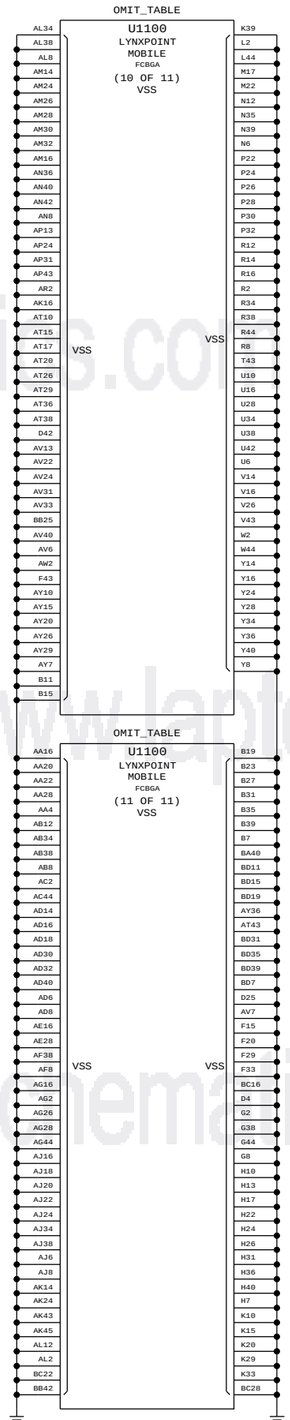


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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
70 15 =PP3V3_S5_PCH_VCCDSW
C1700 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.A16:6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
70 15 =PP3V3_SUS_PCH_VCC_SPI
C1702 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AD12:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
70 15 =PP3V3_SUS_PCH_VCCSUS_GPIO
C1704 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.R20:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR)
70 15 =PP3V3_SUS_PCH_VCCSUS_USB
C1706 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.R26:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
70 15 =PP3V3_SUS_PCH_VCCSUS_RTC
C1708 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.K8:6.35mm

PCH VCCCLK3_3 BYPASS
(PCH 3.3V CLK PWR)
70 15 =PP3V3_S0_PCH_VCCCLK3_3
C1720 1UF 20% 10V X5R 0201
C1721 1UF 20% 10V X5R 0201
C1722 1UF 20% 10V X5R 0201
C1723 1UF 20% 10V X5R 0201
BYPASS=U1100.L26:6.35mm
BYPASS=U1100.L29:6.35mm
BYPASS=U1100.M29:6.35mm
BYPASS=U1100.U32:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR)
70 15 =PP3V3_S0_PCH_VCC3_3_HVCMOS
C1726 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.R30:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
70 15 =PP3V3_S0_PCH_VCC3_3_GPIO
C1728 0.01UF 10% 10V X7R-CERM 0201
BYPASS=U1100.AE14:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR)
70 15 =PP3V3_S0_PCH_VCC3_3_USB
C1730 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.L24:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
70 15 =PP3V3_S0_PCH_VCC3_3_THRM
C1732 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.AK30:6.35mm

PCH VCC BYPASS
(PCH 3.3V FUSE PWR)
70 15 =PP3V3_S0_PCH_VCC_FUSE
C1734 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.P18:6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
70 15 =PP1V05_S0M_PCH_VCCASW
670mA Max, 34mA Idle
C1750 20UF 20% 4V X5R-CERM 0402
C1751 1.0UF 20% 6.3V X5R 0201-1
C1752 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
Not documented in EDS!

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
70 15 =PP1V05_S0_PCH_VCC
C1755 10UF 20% 10V X5R-CERM 0402-1
C1756 1.0UF 20% 6.3V X5R 0201-1
C1757 1.0UF 20% 6.3V X5R 0201-1
C1758 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AG18:12.7mm
BYPASS=U1100.AA24:6.35mm
BYPASS=U1100.AD20:6.35mm
BYPASS=U1100.AE18:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR)
70 15 =PP1V05_S0_PCH_VCCIO
C1760 10UF 20% 10V X5R-CERM 0402-1
C1761 1.0UF 20% 6.3V X5R 0201-1
C1762 1.0UF 20% 6.3V X5R 0201-1
C1763 1.0UF 20% 6.3V X5R 0201-1
C1764 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AK18:12.7mm
BYPASS=U1100.AK18:6.35mm
BYPASS=U1100.AK22:6.35mm
BYPASS=U1100.AK20:6.35mm
BYPASS=U1100.AM18:6.35mm

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR)
70 15 =PP1V05_S0_PCH_VCCUSBPLL
C1770 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U1100.U35:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR)
70 15 =PP1V05_S0_PCH_VCCIO_FDI
C1772 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AN34:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
70 15 =PP1V05_S0_PCH_VCCIO_USB2
C1774 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U1100.U30:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR)
70 15 =PP1V05_S0_PCH_VCCCLK_SSC100
C1776 1.0UF 20% 6.3V X5R 0201-1
C1777 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AE30:6.35mm
BYPASS=U1100.AG30:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR)
70 15 =PP1V05_S0_PCH_VCCCLK_CLK100
C1778 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AD35:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR)
70 15 =PP1V05_S0_PCH_VCCCLK_CLK135
C1780 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AD34:6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
70 15 =PP3V3R1V5_S0_PCH_VCCSUSHDA
C1710 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U1100.A26:6.35mm

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR)
70 =PP1V5_S0_PCH_VCCVRM
183mA Max, 68mA Idle
11 =PP1V5_S0_PCH_VCCVRM_BIAS
15 =PP1V5_S0_PCH_VCCVRM_FDI
15 =PP1V5_S0_PCH_VCCVRM_USB3
15 =PP1V5_S0_PCH_VCCVRM_PCIE
15 =PP1V5_S0_PCH_VCCVRM_SATA
15 =PP1V5_S0_PCH_VCCVRM_CLK
15 =PP1V5_S0_PCH_VCCVRM_THRM
C1740 10UF 20% 10V X5R-CERM 0402-1
BYPASS=U1100.AF34:12.7mm

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR)
70 15 14 =PP1V05_S0_PCH_V_PROC_IO
C1785 1.0UF 20% 6.3V X5R 0201-1
C1786 0.1UF 10% 6.3V CERM-X5R 0201
C1787 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U1100.AJ12:6.35mm
BYPASS=U1100.AJ12:12.7mm
BYPASS=U1100.AJ12:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR)
70 15 =PP1V05_S0_PCH_VCCCLK_SSC
C1782 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AA30:6.35mm

70 =PP1V05_S0_PCH_VCC_CLK
??mA Max, ??mA Idle
R1790 1 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_CLK_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
OMIT_TABLE
L1790 4.7UH-170MA-0.321OHM 0603
PCH CLK VCC BYPASS
(PCH 1.05V CLK PLL PWR)
PP1V05_S0_PCH_VCC_CLK_F 15
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
NO STUFF
C1790 10UF 20% 10V X5R-CERM 0402-1
C1791 1.0UF 20% 6.3V X5R 0201-1
BYPASS=U1100.AP45:12.7mm
BYPASS=U1100.AP45:6.35mm

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 113S0022 | 1 | RES,FF,0 OHM,(0200HM MAX),2A,0603 | L1790 | | |

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J16_KENNY SYNC_DATE=01/21/2013

PAGE TITLE
PCH DECOUPLING

Apple Inc.

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## Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807
(TP-P6)

## CPU Micro2-XDP

PPVCCIO_S0_CPU
=PP1V05_S0_XDP → R1830 150 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM
998-2516

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

| | | | |
|---|---|---|---|
| XDP_CPU_PREQ_L | OBSEN_A0 | OBSEN_C0 | CPU_CFG<17> |
| XDP_CPU_PRDY_L | OBSEN_A1 | OBSEN_C1 | CPU_CFG<16> |
| CPU_CFG<0> | OBSDATA_A0 | OBSDATA_C0 | CPU_CFG<8> |
| CPU_CFG<1> | OBSDATA_A1 | OBSDATA_C1 | CPU_CFG<9> |
| CPU_CFG<2> | OBSDATA_A2 | OBSDATA_C2 | CPU_CFG<10> |
| CPU_CFG<3> | OBSDATA_A3 | OBSDATA_C3 | CPU_CFG<11> |
| XDP_BPM_L<0> | OBSEN_B0 | OBSEN_D0 | CPU_CFG<19> |
| XDP_BPM_L<1> | OBSEN_B1 | OBSEN_D1 | CPU_CFG<18> |
| CPU_CFG<4> | OBSDATA_B0 | OBSDATA_D0 | CPU_CFG<12> |
| CPU_CFG<5> | OBSDATA_B1 | OBSDATA_D1 | CPU_CFG<13> |
| CPU_CFG<6> | OBSDATA_B2 | OBSDATA_D2 | CPU_CFG<14> |
| CPU_CFG<7> | OBSDATA_B3 | OBSDATA_D3 | CPU_CFG<15> |
| XDP_CPU_PWRGD | PWRGD/HOOK0 | ITPCLK/HOOK4 | NC |
| XDP_CPU_PWRBTN_L | HOOK1 | ITPCLK#/HOOK5 | NC |
| | VCC_OBS_AB | VCC_OBS_CD | |
| CPU_PWR_DEBUG | HOOK2 | RESET#/HOOK6 | XDP_CPURST_L |
| XDP_VR_READY | HOOK3 | DBR#/HOOK7 | XDP_DBRESET_L |
| =SMBUS_XDP_SDA | SDA | TDO | XDP_CPU_TDO |
| =SMBUS_XDP_SCL | SCL | TRSTn | XDP_CPU_TRST_L |
| XDP_CPU_TCK | TCK1 | TDI | XDP_CPU_TDI |
| | TCK0 | TMS | XDP_CPU_TMS |
| | | XDP_PRESENT# | |

NC per Intel DPDG.
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_CPU_PRESENT_L

XDP C1804 0.1UF 20% 10V CERM 402
XDP C1800 0.1UF 20% 10V CERM 402
XDP C1801 0.1UF 20% 10V CERM 402
XDP C1806 0.1UF 20% 10V CERM 402
XDP R1831 1K 5% 1/16W MF-LF 402

=PP1V05_S0_XDP
XDP_CPU_TDO → R1820 51 5% 1/20W MF 201 PLACE_NEAR=J1800.51:5MM
XDP_CPU_TCK → R1823 51 5% 1/20W MF 201
XDP_CPU_TRST_L → R1824 51 5% 1/20W MF 201

TDI and TMS are terminated in CPU.

CPU_PWRGD → R1800 1K 5% 1/20W MF 201 PLACE_NEAR=U0500.AB35:16.5mm
PM_PWRBTN_L → R1802 0 5% 1/20W MF 0201
PM_PCH_SYS_PWROK → R1804 220 5% 1/20W MF 201

WF: SB DPDG says HOOK1 is BP_PWRGD_RST#

CPU_RESET_L → R1805 1K 5% 1/20W MF 201

## CPU-PCH JTAG Chain Support

To link CPU and PCH JTAG pull ICT_JTAG_EN to 5V (must be in S0)

TP1845
ICT_JTAG_EN
XDP_CPU_TMS → XDP_PCH_TMS
TP1840
XDP_CPU_TCK → XDP_PCH_TCK
TP1841
XDP_CPU_TDO → XDP_CPU_TDO_PCH_TDI → XDP_PCH_TDI

Q1840 DMN5L06VK-7 SOT-563
Q1846 DMN5L06VK-7 SOT-563
Q1842 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
Q1848 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3

R1842 1M 5% 1/20W MF 201
R1841 1M 5% 1/20W MF 201
R1840 1M 5% 1/20W MF 201
R1845 1K 5% 1/20W MF 201

R1892 0 5% 1/16W MF-LF 402 NOSTUFF
=PP3V3_S5_XDP → PP3V3_S5_XDP_R
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
MAX_NECK_LENGTH=3MM

XDP_PCH_TDO → J1850.51:2.54mm
XDP_PCH_TDI → U1100.W39:4mm
XDP_PCH_TMS → U1100.W40:3.5mm
XDP_PCH_TCK

R1860 210 1% 1/20W MF 201
R1861 210 1% 1/20W MF 201
R1862 210 1% 1/20W MF 201
R1867 100 5% 1/20W MF 201 J1850.51:5mm
R1868 100 5% 1/20W MF 201 U1100.W39:21MM
R1869 100 5% 1/20W MF 201 U1100.W40:20MM
R1866 51 5% 1/20W MF 201

## XDP SIGNALS

### PCH SIGNALS

OMIT (All 18 R's)

| | | | |
|---|---|---|---|
| USB_EXTA_OC_L | R1890 | XDP_DA0_USB_EXTA_OC_L | |
| USB_EXTC_OC_L | R1893 | XDP_DA1_USB_EXTC_OC_L | |
| PCH_GPIO41 | R1894 | XDP_DA2_PCH_GPIO41 | |
| PCH_GPIO42 | R1895 | XDP_DA3_PCH_GPIO42 | |
| USB_EXTB_OC_L | R1880 | XDP_DB0_USB_EXTB_OC_L | |
| USB_EXTD_OC_L | R1881 | XDP_DB1_USB_EXTD_OC_L | |
| PCH_GPIO10 | R1896 | XDP_DB2_PCH_GPIO10 | |
| SDCONN_STATE_CHANGE | R1897 | XDP_DB3_SDCONN_STATE_CHANGE_L | |
| DP_AUXIO_EN | R1872 | XDP_DC0_DP_AUXCH_ISOL_L | |
| SATARDRVR_EN | R1873 | XDP_DC1_SATARDRVR_EN | |
| PCH_GPIO36 | R1874 | XDP_DC2_PCH_GPIO36 | |
| JTAG_ISP_TCK | R1875 | XDP_DC3_JTAG_ISP_TCK | |
| PCH_GPIO16 | R1878 | XDP_DD0_PCH_GPIO16 | |
| PCH_GPIO49 | R1879 | XDP_DD1_PCH_GPIO49 | |
| ENET_CLKREQ_L | R1882 | XDP_DD2_ENET_CLKREQ_L | |
| AP_CLKREQ_L | R1883 | XDP_DD3_AP_CLKREQ_L | |
| HDD_PWR_EN | R1886 | XDP_FC0_HDD_PWR_EN | |
| GPU_GOOD | R1887 | XDP_FC1_GPU_GOOD | |

All: SHORT 1 2 NONE NONE NONE 402

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

## PCH Micro2-XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J1850
DF40RC-60DP-0.4V
M-ST-SM
998-2516

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

| | | | |
|---|---|---|---|
| OBSFN_A0 | OBSFN_C0 | XDP_FC0_HDD_PWR_EN | |
| OBSFN_A1 | OBSFN_C1 | XDP_FC1_GPU_GOOD | |
| XDP_DA0_USB_EXTA_OC_L | OBSDATA_A0 | OBSDATA_C0 | XDP_DC0_DP_AUXCH_ISOL_L |
| XDP_DA1_USB_EXTC_OC_L | OBSDATA_A1 | OBSDATA_C1 | XDP_DC1_SATARDRVR_EN |
| XDP_DA2_PCH_GPIO41 | OBSDATA_A2 | OBSDATA_C2 | XDP_DC2_PCH_GPIO36 |
| XDP_DA3_PCH_GPIO42 | OBSDATA_A3 | OBSDATA_C3 | XDP_DC3_JTAG_ISP_TCK |
| | OBSFN_B0 | OBSFN_D0 | |
| | OBSFN_B1 | OBSFN_D1 | |
| XDP_DB0_USB_EXTB_OC_L | OBSDATA_B0 | OBSDATA_D0 | XDP_DD0_PCH_GPIO16 |
| XDP_DB1_USB_EXTD_OC_L | OBSDATA_B1 | OBSDATA_D1 | XDP_DD1_PCH_GPIO49 |
| XDP_DB2_PCH_GPIO10 | OBSDATA_B2 | OBSDATA_D2 | XDP_DD2_ENET_CLKREQ_L |
| XDP_DB3_SDCONN_STATE_CHANGE_L | OBSDATA_B3 | OBSDATA_D3 | XDP_DD3_AP_CLKREQ_L |
| XDP_PCH_S5_PWRGD | PWRGD/HOOK0 | ITPCLK/HOOK4 | |
| XDP_PCH_PWRBTN_L | HOOK1 | ITPCLK#/HOOK5 | |
| | VCC_OBS_AB | VCC_OBS_CD | |
| | HOOK2 | RESET#/HOOK6 | XDP_PM_PCH_PWROK |
| | HOOK3 | DBR#/HOOK7 | XDP_DBRESET_L |
| =SMBUS_XDP_SDA | SDA | TDO | XDP_PCH_TDO |
| =SMBUS_XDP_SCL | SCL | TRSTn | TP_XDP_PCH_TRST_L |
| XDP_PCH_TCK | TCK1 | TDI | XDP_PCH_TDI |
| | TCK0 | TMS | XDP_PCH_TMS |
| | | XDP_PRESENT# | |

NC
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

PM_RSMRST_PCH_L → R1884 1K 5% 1/20W MF 201 PLACE_NEAR=J1850.40:2.54mm
PM_PWRBTN_L → R1885 0 5% 1/20W MF 0201 PLACE_NEAR=U5000.J3:2.54mm

R1870 1K 5% 1/20W MF 201 PM_PCH_PWROK

XDP C1880 0.1UF 20% 10V CERM 402
XDP C1881 0.1UF 20% 10V CERM 402

SYNC_MASTER=J16_KENNY SYNC_DATE=03/18/2013

PAGE TITLE: CPU & PCH XDP

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## System 25MHz Clock Generator

VDD must be powered if any VDDIO is.
ENET > S0 > TBT, so ENET is used here.

GreenClk 25MHz Power — 70 =PP3V3_ENET_SYSCLK
Ethernet XTAL Power — 70 =PPVDDIO_ENET_CLK
SB XTAL Power — 70 11 =PP1V5_S0_PCH_CLK
TBT XTAL Power — 70 =PPVDDIO_TBT_CLK

C1924 0.1UF 20% 10V CERM 402
C1922 0.1UF 20% 10V CERM 402
C1920 0.1UF 20% 10V CERM 402
C1902 1UF 10% 6.3V CERM 402

U1900
SLG3NB146V
TDFN
CRITICAL

VDD, VDDIO_A, VDDIO_B, VDDIO_C, GND, THRM PAD

C1905 12PF 5% 50V C0G-CERM 0402
C1906 12PF 5% 50V C0G-CERM 0402
NC
NC
CRITICAL
Y1905
25.000MHZ-20PPM-12PF-85C
3.2X2.5MM-SM

R1905 0 5% 1/16W MF-LF 402
NOSTUFF
R1906 1M 5% 1/16W MF-LF 402

70 SYSCLK_CLK25M_X2
70 SYSCLK_CLK25M_X2_R
79 SYSCLK_CLK25M_X1
XOUT
XIN

25MHZ_A — SYSCLK_CLK25M_SB — OUT 11 79
25MHZ_B — SYSCLK_CLK25M_ENET_R — OUT 19 79
25MHZ_C — SYSCLK_CLK25M_TBT — OUT 26 79

NOTE: 30 PPM crystal required

## RTC Power Sources

Coin-Cell Holder
J1900
BB10201-C1403-7H
SM
511S0054

PPVBATT_G3_RTC
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R1902 1K 5% 1/16W MF-LF 402

70 =PP3V3_G3H_RTC_D
PPVBATT_G3_RTC_R
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

D1900
BAT54DW-X-G
SOT-363
NC
NC
NC
NC

PP3V3_G3_RTC
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V

TP1900
1.97X2.02MM-NSP
SMT-PAD
OMIT

TP1901
1.97X2.02MM-NSP
SMT-PAD
OMIT

Place TP1901-TP1903 on bottom side

TP1902
1.4-SQ-NSP
SM-PAD
OMIT

TP1903
1.4-SQ-NSP
SM-PAD
OMIT

45 11 RTC_RESET_L

## PCH RTC Crystal

PLACE_NEAR=Y1910.4:2MM

79 11 IN PCH_CLK32K_RTCX2
R1910 0 5% 1/16W MF-LF 402
79 PCH_CLK32K_RTCX2_R
C1910 12PF 5% 50V C0G-CERM 0402
R1911 10M 5% 1/16W MF-LF 402
CRITICAL
Y1910
32.768K-12.5PF
SM-HF
C1911 12PF 5% 50V C0G-CERM 0402
79 11 OUT PCH_CLK32K_RTCX1

PLACE_NEAR=Y1910.1:2MM

## Clock series termination

79 11 IN LPC_CLK33M_SMC_R — PLACE_NEAR=U1100:10MM — R1955 33 5% 1/16W MF-LF 402 — LPC_CLK33M_SMC — OUT 44 79
79 11 IN LPC_CLK33M_LPCPLUS_R — PLACE_NEAR=U1100:10MM — R1956 33 5% 1/16W MF-LF 402 — LPC_CLK33M_LPCPLUS — OUT 46 79
79 11 IN PCH_CLK33M_PCIOUT — PLACE_NEAR=U1100:13MM — R1959 33 5% 1/16W MF-LF 402 — PCH_CLK33M_PCIIN — OUT 11 79
79 19 SYSCLK_CLK25M_ENET_R — PLACE_NEAR=U1900.4:10MM — R1958 33 5% 1/16W MF-LF 402 — SYSCLK_CLK25M_ENET — OUT 35 79

## PCH Reset Button

70 13 =PP3V3_S0_PCH
R1995 4.7K 5% 1/16W MF-LF 402
XDP
R1996 0 5% 1/16W MF-LF 402
18 6 IN XDP_DBRESET_L
PM_SYSRST_L — OUT 12 44
OMIT
R1997 0 5% 1/16W MF-LF 402
SILK_PART=SYS RESET

## PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.

70 20 =PP3V3_S5_PCH
44 IN SPI_DESCRIPTOR_OVERRIDE_L
Q1920 NTR1P02L SOT23-3-HF

PLACE_NEAR=R1113.2:15MM
SPI_DESCRIPTOR_OVERRIDE_R — 330 5% — R1921 1/16W MF-LF 402 — HDA_SDOUT_R — OUT 11 79

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SYNC_DATE=01/21/2013
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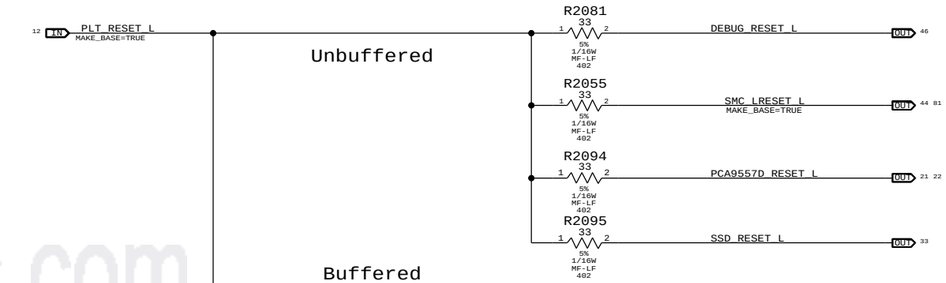
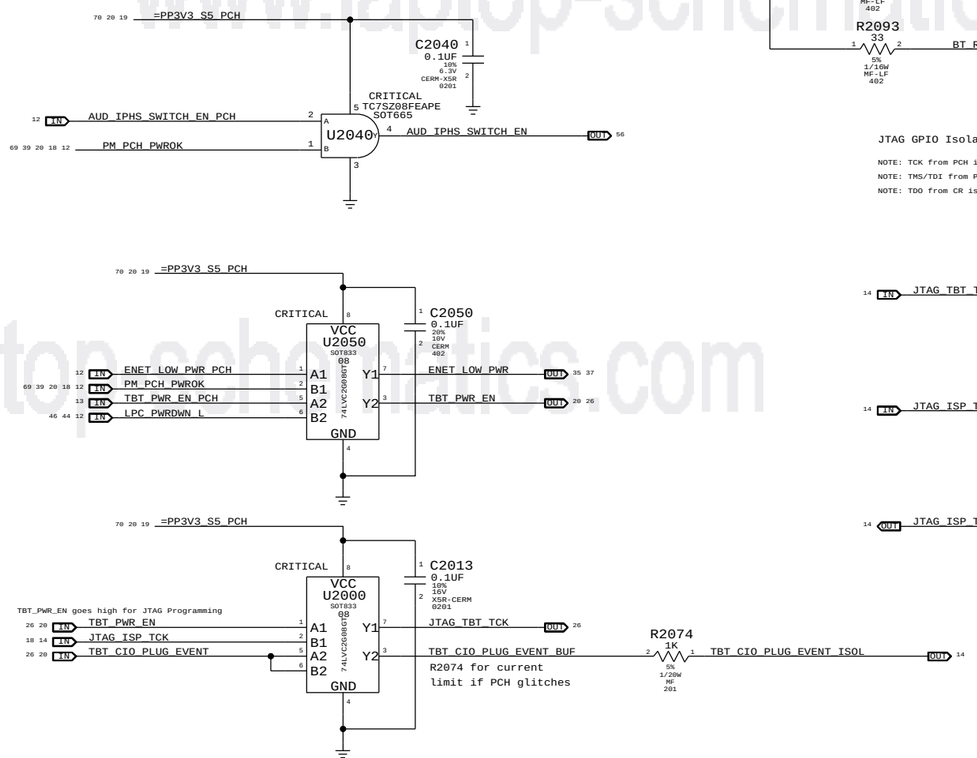
## Platform Reset Connections

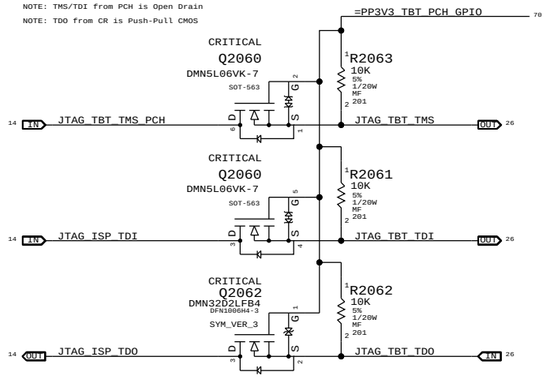



## GPIO Glitch Prevention




## JTAG GPIO Isolation due to glitch in and out of sleep

NOTE: TCK from PCH is Push-Pull CMOS
NOTE: TMS/TDI from PCH is Open Drain
NOTE: TDO from CR is Push-Pull CMOS

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SYNC_MASTER=J16_KENNY SYNC_DATE=01/21/2013

PAGE TITLE: Project Chipset Support

Apple Inc.

DRAWING NUMBER: 051-0164 SIZE: D
REVISION: 12.4.0
BRANCH:
PAGE: 20 OF 123
SHEET: 20 OF 86

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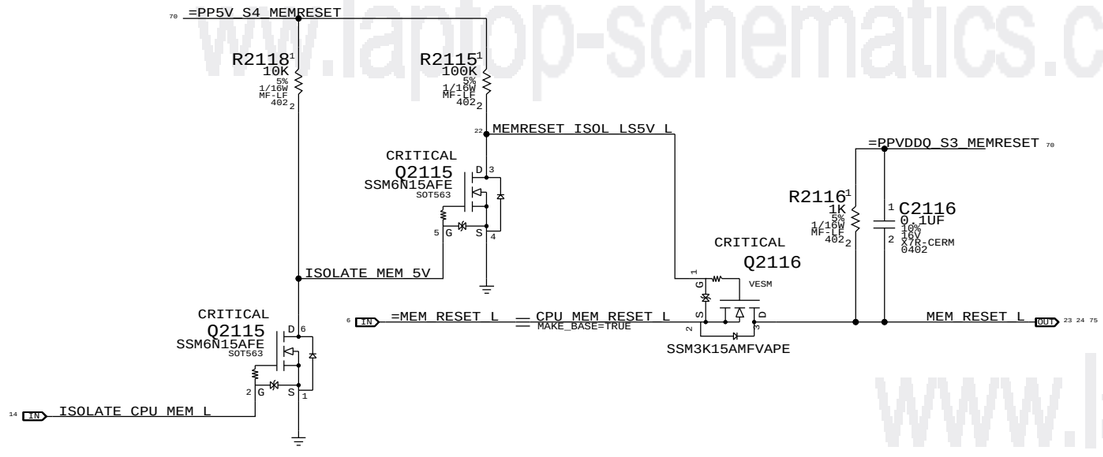
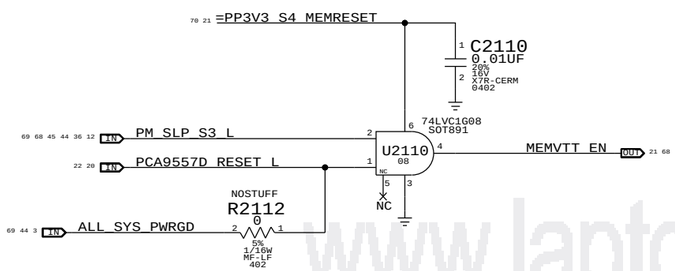
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

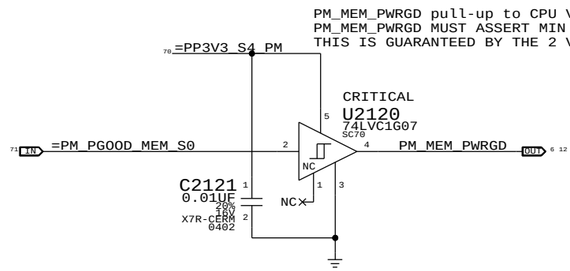
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

MEMVTT_EN = PLT_RESET_L * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



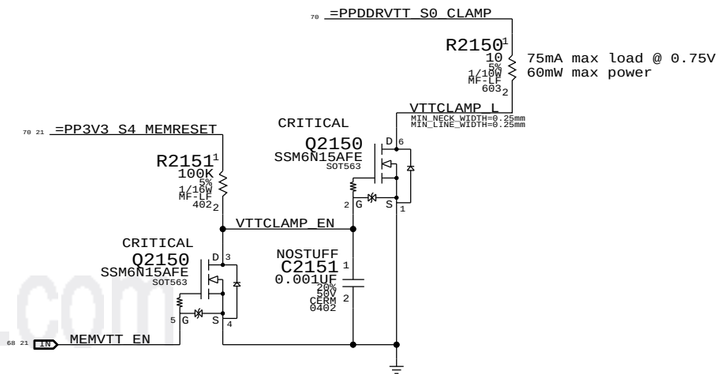




# MEM S0 "PGOOD" FOR CPU




# MEMVTT Clamp

Ensures CKE signals are held low in S3




| | Step | ISOLATE_CPU_MEM_L | PLT_RESET_L | PM_SLP_S3_L | CPU_MEM_RESET_L | MEM_RESET_L | MEMVTT_EN |
|---|---|---|---|---|---|---|---|
| S0 | 0 | 1 | 1 | 1 | 1 | CPU_MEM_RESET_L | 1 |
| | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| to | 2 | 0 | 0 | 1 | 1 | 1 | 0 |
| S3 | 3 | 0 | 0 | 0 | X | 1 | 0 |
| | 4 | 0 | 0 | 1 | X | 1 | 0 |
| to | 5 | 0 | 1 | 1 | 0 (*) | 1 | 1 |
| | 6 | 0 | 1 | 1 | 1 | 1 | 1 |
| S0 | 7 | 1 | 1 | 1 | 1 | CPU_MEM_RESET_L | 1 |

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J16_NICK SYNC_DATE=12/11/2012

PAGE TITLE
CPU Memory S3 Support

Apple Inc.

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## Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

# CPU-Based Margining

FETs for CPU isolation during S3

21 IN MEMRESET_ISOL_LS5V_L
7 IN CPU_DIMMA_VREFDQ
7 IN CPU_DIMMB_VREFDQ
7 IN CPU_DIMM_VREFCA

CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563
CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.

CPU_MEM_VREFDQ_A_ISOL
CPU_MEM_VREFDQ_B_ISOL
CPU_MEM_VREFCA_A_ISOL
CPU_MEM_VREFCA_B_ISOL

EN RC's to avoid drain glitches

DDRVREF_DAC R2225 100K 5% 1/16W MF-LF 402
DDRVREF_DAC R2201 100K 5% 1/20W MF 201
DDRVREF_DAC C2225 0.1UF 20% 10V CERM 402
VREFMRGN_DQ_A_EN_RC
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
Q2225 pin 6: PLACE_NEAR=Q2220.6:5mm

DDRVREF_DAC R2245 100K 5% 1/16W MF-LF 402
DDRVREF_DAC R2202 100K 5% 1/20W MF 201
DDRVREF_DAC C2245 0.1UF 20% 10V CERM 402
VREFMRGN_DQ_B_EN_RC
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
Q2265 pin 6: PLACE_NEAR=Q2260.6:5mm

DDRVREF_DAC R2265 100K 5% 1/16W MF-LF 402
DDRVREF_DAC R2207 100K 5% 1/20W MF 201
DDRVREF_DAC C2265 0.1UF 20% 10V CERM 402
VREFMRGN_CA_A_EN_RC
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563

DDRVREF_DAC R2285 100K 5% 1/16W MF-LF 402
DDRVREF_DAC R2208 100K 5% 1/20W MF 201
DDRVREF_DAC C2285 0.1UF 20% 10V CERM 402
VREFMRGN_CA_B_EN_RC
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563

(All 4 R's) DDRVREF_DAC
R2226 332 1% 1/16W MF-LF 402 VREFMRGN_DQ_A_RDIV
R2246 332 1% 1/16W MF-LF 402 VREFMRGN_DQ_B_RDIV
R2266 332 1% 1/16W MF-LF 402 VREFMRGN_CA_A_RDIV
R2286 332 1% 1/16W MF-LF 402 VREFMRGN_CA_B_RDIV
R22x6 pin 2: PLACE_NEAR=Q2225.1:5.5mm / PLACE_NEAR=Q2265.4:5.5mm / PLACE_NEAR=Q2225.1:5.5mm / PLACE_NEAR=Q2265.4:5.5mm

# VRef Dividers

Always used, regardless of margining option.

=PPDDR_S3_MEMVREF 70

R2223 2 5% 1/20W MF 201 PLACE_NEAR=Q2220.1:2mm
R2221 1K 1% 1/16W MF-LF 402 PLACE_NEAR=R2223.2:1.5MM
PPVREF_S3_MEM_VREFDQ_A MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm 23
C2220 0.022UF 10% 6.3V XSR-CERM 0201 PLACE_NEAR=Q2220.6:2mm
R2222 1K 1% 1/16W MF-LF 402 PLACE_NEAR=R2221.2:1mm
MEM_VREFDQ_A_RC
R2220 24.9 1% 1/20W MF 201

R2243 2 5% 1/20W MF 201 PLACE_NEAR=Q2240.1:2mm
R2241 1K 1% 1/16W MF-LF 402 PLACE_NEAR=R2243.2:1mm
PPVREF_S3_MEM_VREFDQ_B MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm 24
C2240 0.022UF 10% 6.3V XSR-CERM 0201 PLACE_NEAR=Q2260.6:4MM
R2242 1K 1% 1/16W MF-LF 402 PLACE_NEAR=R2241.2:1mm
MEM_VREFDQ_B_RC
R2240 24.9 1% 1/20W MF 201

R2263 2 5% 1/20W MF 201 PLACE_NEAR=Q2260.1:2mm
R2261 1K 1% 1/16W MF-LF 402 PLACE_NEAR=R2263.2:1mm
PPVREF_S3_MEM_VREFCA_A MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm 23
C2260 0.022UF 10% 6.3V XSR-CERM 0201 PLACE_NEAR=Q2220.3:2mm
R2262 1K 1% 1/16W MF-LF 402 PLACE_NEAR=R2261.2:1mm
MEM_VREFCA_A_RC
R2260 24.9 1% 1/20W MF 201

R2283 2 5% 1/20W MF 201 PLACE_NEAR=Q2280.1:2mm
R2281 1K 1% 1/16W MF-LF 402 PLACE_NEAR=R2283.2:1.5MM
PPVREF_S3_MEM_VREFCA_B MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm 24
C2280 0.022UF 10% 6.3V XSR-CERM 0201 PLACE_NEAR=Q2260.3:2mm
R2282 1K 1% 1/16W MF-LF 402 PLACE_NEAR=R2281.2:1mm
MEM_VREFCA_B_RC
R2280 24.9 1% 1/20W MF 201

# DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

70 22 =PP3V3_S3_VREFMRGN
OMIT R2218 SHORT NONE NONE NONE 402
PP3V3_S3_VREFMRGN MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-XSR 0201

CRITICAL DDRVREF_DAC
U2200 MSOP DAC5574 VDD VOUTA VOUTB VOUTC VOUTD SCL SDA A0 A1 GND
47 IN =I2C_VREFDACS_SCL
47 BI =I2C_VREFDACS_SDA
Addr=0x98(WR)/0x99(RD)
VREFMRGN_DQ_A
VREFMRGN_DQ_B
VREFMRGN_CA_AB
VREFMRGN_MEMVREG_FBVREF

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-XSR 0201
CRITICAL DDRVREF_DAC
U2201 PCA9557 QFN VCC P0 P1 P2 P3 P4 P5 P6 P7 SCL SDA A0 A1 A2 RESET THRM PAD GND
Addr=0x30(WR)/0x31(RD)
P0 NC
P1 VREFMRGN_DQ_A_EN
P2 VREFMRGN_DQ_B_EN
P3 VREFMRGN_CA_A_EN
P4 VREFMRGN_CA_B_EN
P5 VREFMRGN_MEMVREG_EN
P6 VREFMRGN_FRAMEBUF_EN
P7 NC
47 IN =I2C_PCA9557D_SCL
47 BI =I2C_PCA9557D_SDA
RESET* 15
21 20 IN PCA9557D_RESET_L

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

=PP3V3_S3_VREFMRGN 22 70
DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-XSR 0201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_MEMVREG_BUF
DDRVREF_DAC R2214 33.2K 1% 1/16W MF-LF 402
DDRREG_FB OUT 63

DDRVREF_DAC R2213 100K 5% 1/20W MF 201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_FRAMEBUF_BUF
DDRVREF_DAC R2217 1M 5% 1/16W MF-LF 402
Pins B1 & B4: **CKPLUS_WAIVE=unconnected_pins**

DDRVREF_DAC R2215 100K 5% 1/20W MF 201

NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

| | MEM A VREF DQ | MEM B VREF DQ | MEM A VREF CA | MEM B VREF CA | MEM VREG | |
|---|---|---|---|---|---|---|
| DAC Channel: | A | B | C | C | D | |
| PCA9557D Pin: | 1 | 2 | 3 | 4 | 5 | |
| | DDR3 (1.5V) | | DDR3L (1.35V) | | DDR3 (1.5V) | DDR3L (1.35V) |
| Nominal value | 0.750V (DAC: 0x3A = 0.747mV) | | 0.675V (DAC: 0x34 = 0.670mV) | | 1.500V (DAC: 0x74 = 1.495V) | 1.343V (DAC: 0x68 = 1.341V) |
| Margined target: | 0.300V - 1.200V (+/- 450mV) | | 0.275V - 1.075V (+/- 400mV) | | 1.200V - 1.800V (+/- 300mV) | 0.950V - 1.750V (+/- 400mV) |
| DAC range: | 0.000V - 1.508V (0x00 - 0x75) | | 0.000V - 1.354V (0x00 - 0x69) | | 0.000V - 3.004V (0x00 - 0xE9) | 0.000V - 2.707V (0x00 - 0xD2) |
| Margined range: | 0.299V - 1.206V (+/- 453mV) | | 0.269V - 1.083V (+/- 406mV) | | 1.199V - 1.801V (+/- 301mV) | 0.932V - 1.760V (+/- 414mV) |
| VRef current: | +901uA - -911uA (- = sourced) | | +811uA - -816uA (- = sourced) | | +36uA - -36uA (- = sourced) | +28uA - -29uA (- = sourced) |
| DAC step size: | 7.68mV / step @ output | | 7.67mV / step @ output | | 2.575mV / step @ output | 3.923mV / step @ output |

SYNC_MASTER=J16_NICK SYNC_DATE=01/10/2013
PAGE TITLE: DDR3 VREF MARGINING
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22 =PPVREF_S3_MEM_VREFDQ_A
VOLTAGE=0.75V

C2330 2.2UF 20% 6.3V CERM 402-LF
C2331 0.1UF 20% 10V CERM 402

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

70 23 =PPVDDQ_S3_MEM_A

C2310 0.1UF 20% 10V CERM 402
C2311 0.1UF 20% 10V CERM 402
C2312 0.1UF 20% 10V CERM 402
C2313 0.1UF 20% 10V CERM 402
C2314 0.1UF 20% 10V CERM 402
C2315 0.1UF 20% 10V CERM 402
C2316 0.1UF 20% 10V CERM 402
C2317 0.1UF 20% 10V CERM 402
C2302 0.1UF 20% 10V CERM 402

=PPVDDQ_S3_MEM_A 23 70

C2300 10UF 20% 6.3V X5R 603
C2301 10UF 20% 6.3V X5R 603
C2318 0.1UF 20% 10V CERM 402
C2319 0.1UF 20% 10V CERM 402
C2320 0.1UF 20% 10V CERM 402
C2321 0.1UF 20% 10V CERM 402
C2322 0.1UF 20% 10V CERM 402
C2323 0.1UF 20% 10V CERM 402
C2324 0.1UF 20% 10V CERM 402

23 MEM_A_SA<1>
23 MEM_A_SA<0>
70 23 =PPSPD_S0_MEM_A

C2340 2.2UF 20% 6.3V CERM 402-LF
R2340 10K 5% 1/16W MF-LF 402
R2341 10K 5% 1/16W MF-LF 402

70 23 =PPDDRVTT_S0_MEM_A

J2300 CRITICAL
F-RT-SM
2-20133310-1

| | | | |
|---|---|---|---|
| 1 | VREFDQ | VSS_0 | 2 |
| 3 | VSS_1 | DQ4 | 4 =MEM_A_DQ<4> |
| 5 | DQ0 | DQ5 | 6 =MEM_A_DQ<5> |
| 7 | DQ1 | VSS_2 | 8 |
| 9 | VSS_3 | DQS0* | 10 =MEM_A_DQS_N<0> |
| 11 | DM0 | DQS0 | 12 =MEM_A_DQS_P<0> |
| 13 | VSS_4 | VSS_5 | 14 |
| 15 | DQ2 | DQ6 | 16 =MEM_A_DQ<6> |
| 17 | DQ3 | DQ7 | 18 =MEM_A_DQ<7> |
| 19 | VSS_6 | VSS_7 | 20 |
| 21 | DQ8 | DQ12 | 22 =MEM_A_DQ<12> |
| 23 | DQ9 | DQ13 | 24 =MEM_A_DQ<13> |
| 25 | VSS_8 | VSS_9 | 26 |
| 27 | DQS1* | DM1 | 28 |
| 29 | DQS1 | RESET* | 30 MEM_RESET_L IN 21 24 75 |
| 31 | VSS_10 | VSS_11 | 32 |
| 33 | DQ10 | DQ14 | 34 =MEM_A_DQ<14> |
| 35 | DQ11 | DQ15 | 36 =MEM_A_DQ<15> |
| 37 | VSS_12 | VSS_13 | 38 |
| 39 | DQ16 | DQ20 | 40 =MEM_A_DQ<20> |
| 41 | DQ17 | DQ21 | 42 =MEM_A_DQ<21> |
| 43 | VSS_14 | VSS_15 | 44 |
| 45 | DQS2* | DM2 | 46 |
| 47 | DQS2 | VSS_16 | 48 |
| 49 | VSS_17 | DQ22 | 50 =MEM_A_DQ<22> |
| 51 | DQ18 | DQ23 | 52 =MEM_A_DQ<23> |
| 53 | DQ19 | VSS_18 | 54 |
| 55 | VSS_19 | DQ28 | 56 =MEM_A_DQ<28> |
| 57 | DQ24 | DQ29 | 58 =MEM_A_DQ<29> |
| 59 | DQ25 | VSS_20 | 60 |
| 61 | VSS_21 | DQS3* | 62 =MEM_A_DQS_N<3> |
| 63 | DM3 | DQS3 | 64 =MEM_A_DQS_P<3> |
| 65 | VSS_22 | VSS_23 | 66 |
| 67 | DQ26 | DQ30 | 68 =MEM_A_DQ<30> |
| 69 | DQ27 | DQ31 | 70 =MEM_A_DQ<31> |
| 71 | VSS_24 | VSS_25 | 72 |
| 73 | CKE0 | CKE1 | 74 MEM_A_CKE<1> LN 7 75 |
| 75 | VDD_0 | VDD_1 | 76 |
| 77 | NC_0 | A15 | 78 MEM_A_A<15> LN 7 75 |
| 79 | BA2 | A14 | 80 MEM_A_A<14> LN 7 75 |
| 81 | VDD_2 | VDD_3 | 82 |
| 83 | A12/BC* | A11 | 84 MEM_A_A<11> LN 7 75 |
| 85 | A9 | A7 | 86 MEM_A_A<7> LN 7 75 |
| 87 | VDD_4 | VDD_5 | 88 |
| 89 | A8 | A6 | 90 MEM_A_A<6> LN 7 75 |
| 91 | A5 | A4 | 92 MEM_A_A<4> LN 7 75 |
| 93 | VDD_6 | VDD_7 | 94 |
| 95 | A3 | A2 | 96 MEM_A_A<2> LN 7 75 |
| 97 | A1 | A0 | 98 MEM_A_A<0> LN 7 75 |
| 99 | VDD_8 | VDD_9 | 100 |
| 101 | CK0 | CK1 | 102 MEM_A_CLK_P<1> LN 7 75 |
| 103 | CK0* | CK1* | 104 MEM_A_CLK_N<1> LN 7 75 |
| 105 | VDD_10 | VDD_11 | 106 |
| 107 | A10_AP | BA1 | 108 MEM_A_BA<1> LN 7 75 |
| 109 | BA0 | RAS* | 110 MEM_A_RAS_L LN 7 75 |
| 111 | VDD_12 | VDD_13 | 112 |
| 113 | WE* | S0* | 114 MEM_A_CS_L<0> LN 7 75 |
| 115 | CAS* | ODT0 | 116 MEM_A_ODT<0> LN 7 75 |
| 117 | VDD_14 | VDD_15 | 118 |
| 119 | A13 | ODT1 | 120 MEM_A_ODT<1> LN 7 75 |
| 121 | S1* | NC_1 | 122 NC |
| 123 | VDD_16 | VDD_17 | 124 |
| 125 | TEST | VREFCA | 126 |
| 127 | VSS_26 | VSS_27 | 128 |
| 129 | DQ32 | DQ36 | 130 =MEM_A_DQ<36> |
| 131 | DQ33 | DQ37 | 132 =MEM_A_DQ<37> |
| 133 | VSS_28 | VSS_29 | 134 |
| 135 | DQS4* | DM4 | 136 |
| 137 | DQS4 | VSS_30 | 138 |
| 139 | VSS_31 | DQ38 | 140 =MEM_A_DQ<38> |
| 141 | DQ34 | DQ39 | 142 =MEM_A_DQ<39> |
| 143 | DQ35 | VSS_32 | 144 |
| 145 | VSS_33 | DQ44 | 146 =MEM_A_DQ<44> |
| 147 | DQ40 | DQ45 | 148 =MEM_A_DQ<45> |
| 149 | DQ41 | VSS_34 | 150 |
| 151 | VSS_35 | DQS5* | 152 =MEM_A_DQS_N<5> |
| 153 | DM5 | DQS5 | 154 =MEM_A_DQS_P<5> |
| 155 | VSS_36 | VSS_37 | 156 |
| 157 | DQ42 | DQ46 | 158 =MEM_A_DQ<46> |
| 159 | DQ43 | DQ47 | 160 =MEM_A_DQ<47> |
| 161 | VSS_38 | VSS_39 | 162 |
| 163 | DQ48 | DQ52 | 164 =MEM_A_DQ<52> |
| 165 | DQ49 | DQ53 | 166 =MEM_A_DQ<53> |
| 167 | VSS_40 | VSS_41 | 168 |
| 169 | DQS6* | DM6 | 170 |
| 171 | DQS6 | VSS_42 | 172 |
| 173 | VSS_43 | DQ54 | 174 =MEM_A_DQ<54> |
| 175 | DQ50 | DQ55 | 176 =MEM_A_DQ<55> |
| 177 | DQ51 | VSS_44 | 178 |
| 179 | VSS_45 | DQ60 | 180 =MEM_A_DQ<60> |
| 181 | DQ56 | DQ61 | 182 =MEM_A_DQ<61> |
| 183 | DQ57 | VSS_46 | 184 |
| 185 | VSS_47 | DQS7* | 186 =MEM_A_DQS_N<7> |
| 187 | DM7 | DQS7 | 188 =MEM_A_DQS_P<7> |
| 189 | VSS_48 | VSS_49 | 190 |
| 191 | DQ58 | DQ62 | 192 =MEM_A_DQ<62> |
| 193 | DQ59 | DQ63 | 194 =MEM_A_DQ<63> |
| 195 | VSS_50 | VSS_51 | 196 |
| 197 | SA0 | EVENT* | 198 MEM_EVENT_L OUT 24 44 45 |
| 199 | VDDSPD | SDA | 200 =I2C_SODIMMA_SDA BI 47 |
| 201 | SA1 | SCL | 202 =I2C_SODIMMA_SCL IN 47 |
| 203 | VTT_0 | VTT_1 | 204 |
| 205 | MTG_PIN | MTG_PIN | 206 |

KEY

75 7 =MEM_A_CKE<0>
75 7 =MEM_A_BA<2>
75 7 =MEM_A_A<12>
75 7 =MEM_A_A<9>
75 7 =MEM_A_A<8>
75 7 =MEM_A_A<5>
75 7 =MEM_A_A<3>
75 7 =MEM_A_A<1>
75 7 =MEM_A_CLK_P<0>
75 7 =MEM_A_CLK_N<0>
75 7 =MEM_A_A<10>
75 7 =MEM_A_BA<0>
75 7 =MEM_A_WE_L
75 7 =MEM_A_CAS_L
75 7 =MEM_A_A<13>
75 7 =MEM_A_CS_L<1>

NC

23 =MEM_A_SA<0>
70 23 =PPSPD_S0_MEM_A
23 =MEM_A_SA<1>

C2335 2.2UF 20% 6.3V CERM 402-LF
C2336 0.1UF 20% 10V CERM 402

PPVREF_S3_MEM_VREFCA_A 22
VOLTAGE=0.75V

=PPDDRVTT_S0_MEM_A 23 70

C2350 1UF 10% 10V X6S-CERM 0402
C2351 1UF 10% 10V X6S-CERM 0402
C2352 1UF 10% 10V X6S-CERM 0402
C2353 1UF 10% 10V X6S-CERM 0402

SYNC_MASTER=J16_NICK SYNC_DATE=01/10/2013

PAGE TITLE
DDR3 SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER 051-0164 SIZE D
REVISION 12.4.0
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22 PPVREF_S3_MEM_VREFDQ_B
VOLTAGE=0.75V

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 0.1UF 20% 10V CERM 402

CRITICAL
J2500
F-RT-SM
2-2013289-1

| | | | |
|---|---|---|---|
| 1 | VREFDQ | VSS_0 | 2 |
| 3 | VSS_1 | DQ4 | 4 |
| 5 | DQ0 | DQ5 | 6 |
| 7 | DQ1 | VSS_2 | 8 |
| 9 | VSS_3 | DQS0* | 10 |
| 11 | DM0 | DQS0 | 12 |
| 13 | VSS_4 | VSS_5 | 14 |
| 15 | DQ2 | DQ6 | 16 |
| 17 | DQ3 | DQ7 | 18 |
| 19 | VSS_6 | VSS_7 | 20 |
| 21 | DQ8 | DQ12 | 22 |
| 23 | DQ9 | DQ13 | 24 |
| 25 | VSS_8 | VSS_9 | 26 |
| 27 | DQS1* | DM1 | 28 |
| 29 | DQS1 | RESET* | 30 |
| 31 | VSS_10 | VSS_11 | 32 |
| 33 | DQ10 | DQ14 | 34 |
| 35 | DQ11 | DQ15 | 36 |
| 37 | VSS_12 | VSS_13 | 38 |
| 39 | DQ16 | DQ20 | 40 |
| 41 | DQ17 | DQ21 | 42 |
| 43 | VSS_14 | VSS_15 | 44 |
| 45 | DQS2* | DM2 | 46 |
| 47 | DQS2 | VSS_16 | 48 |
| 49 | VSS_17 | DQ22 | 50 |
| 51 | DQ18 | DQ23 | 52 |
| 53 | DQ19 | VSS_18 | 54 |
| 55 | VSS_19 | DQ28 | 56 |
| 57 | DQ24 | DQ29 | 58 |
| 59 | DQ25 | VSS_20 | 60 |
| 61 | VSS_21 | DQS3* | 62 |
| 63 | DM3 | DQS3 | 64 |
| 65 | VSS_22 | VSS_23 | 66 |
| 67 | DQ26 | DQ30 | 68 |
| 69 | DQ27 | DQ31 | 70 |
| 71 | VSS_24 | VSS_25 | 72 |
| | KEY | | |
| 73 | CKE0 | CKE1 | 74 |
| 75 | VDD_0 | VDD_1 | 76 |
| 77 | NC_0 | A15 | 78 |
| 79 | BA2 | A14 | 80 |
| 81 | VDD_2 | VDD_3 | 82 |
| 83 | A12/BC* | A11 | 84 |
| 85 | A9 | A7 | 86 |
| 87 | VDD_4 | VDD_5 | 88 |
| 89 | A8 | A6 | 90 |
| 91 | A5 | A4 | 92 |
| 93 | VDD_6 | VDD_7 | 94 |
| 95 | A3 | A2 | 96 |
| 97 | A1 | A0 | 98 |
| 99 | VDD_8 | VDD_9 | 100 |
| 101 | CK0 | CK1 | 102 |
| 103 | CK0* | CK1* | 104 |
| 105 | VDD_10 | VDD_11 | 106 |
| 107 | A10_AP | BA1 | 108 |
| 109 | BA0 | RAS* | 110 |
| 111 | VDD_12 | VDD_13 | 112 |
| 113 | WE* | S0* | 114 |
| 115 | CAS* | ODT0 | 116 |
| 117 | VDD_14 | VDD_15 | 118 |
| 119 | A13 | ODT1 | 120 |
| 121 | S1* | NC_1 | 122 |
| 123 | VDD_16 | VDD_17 | 124 |
| 125 | TEST | VREFCA | 126 |
| 127 | VSS_26 | VSS_27 | 128 |
| 129 | DQ32 | DQ36 | 130 |
| 131 | DQ33 | DQ37 | 132 |
| 133 | VSS_28 | VSS_29 | 134 |
| 135 | DQS4* | DM4 | 136 |
| 137 | DQS4 | VSS_30 | 138 |
| 139 | VSS_31 | DQ38 | 140 |
| 141 | DQ34 | DQ39 | 142 |
| 143 | DQ35 | VSS_32 | 144 |
| 145 | VSS_33 | DQ44 | 146 |
| 147 | DQ40 | DQ45 | 148 |
| 149 | DQ41 | VSS_34 | 150 |
| 151 | VSS_35 | DQS5* | 152 |
| 153 | DM5 | DQS5 | 154 |
| 155 | VSS_36 | VSS_37 | 156 |
| 157 | DQ42 | DQ46 | 158 |
| 159 | DQ43 | DQ47 | 160 |
| 161 | VSS_38 | VSS_39 | 162 |
| 163 | DQ48 | DQ52 | 164 |
| 165 | DQ49 | DQ53 | 166 |
| 167 | VSS_40 | VSS_41 | 168 |
| 169 | DQS6* | DM6 | 170 |
| 171 | DQS6 | VSS_42 | 172 |
| 173 | VSS_43 | DQ54 | 174 |
| 175 | DQ50 | DQ55 | 176 |
| 177 | DQ51 | VSS_44 | 178 |
| 179 | VSS_45 | DQ60 | 180 |
| 181 | DQ56 | DQ61 | 182 |
| 183 | DQ57 | VSS_46 | 184 |
| 185 | VSS_47 | DQS7* | 186 |
| 187 | DM7 | DQS7 | 188 |
| 189 | VSS_48 | VSS_49 | 190 |
| 191 | DQ58 | DQ62 | 192 |
| 193 | DQ59 | DQ63 | 194 |
| 195 | VSS_50 | VSS_51 | 196 |
| 197 | SA0 | EVENT* | 198 |
| 199 | VDDSPD | SDA | 200 |
| 201 | SA1 | SCL | 202 |
| 203 | VTT_0 | VTT_1 | 204 |
| 205 | MTG_PIN | MTG_PIN | 206 |

=MEM_B_DQ<0>
=MEM_B_DQ<1>
=MEM_B_DQ<2>
=MEM_B_DQ<3>
=MEM_B_DQ<8>
=MEM_B_DQ<9>
=MEM_B_DQS_N<1>
=MEM_B_DQS_P<1>
=MEM_B_DQ<10>
=MEM_B_DQ<11>
=MEM_B_DQ<16>
=MEM_B_DQ<17>
=MEM_B_DQS_N<2>
=MEM_B_DQS_P<2>
=MEM_B_DQ<18>
=MEM_B_DQ<19>
=MEM_B_DQ<24>
=MEM_B_DQ<25>
=MEM_B_DQ<26>
=MEM_B_DQ<27>
=MEM_B_DQ<32>
=MEM_B_DQ<33>
=MEM_B_DQS_N<4>
=MEM_B_DQS_P<4>
=MEM_B_DQ<34>
=MEM_B_DQ<35>
=MEM_B_DQ<40>
=MEM_B_DQ<41>
=MEM_B_DQ<42>
=MEM_B_DQ<43>
=MEM_B_DQ<48>
=MEM_B_DQ<49>
=MEM_B_DQS_N<6>
=MEM_B_DQS_P<6>
=MEM_B_DQ<50>
=MEM_B_DQ<51>
=MEM_B_DQ<56>
=MEM_B_DQ<57>
=MEM_B_DQ<58>
=MEM_B_DQ<59>

=MEM_B_DQ<4>
=MEM_B_DQ<5>
=MEM_B_DQS_N<0>
=MEM_B_DQS_P<0>
=MEM_B_DQ<6>
=MEM_B_DQ<7>
=MEM_B_DQ<12>
=MEM_B_DQ<13>
MEM_RESET_L
=MEM_B_DQ<14>
=MEM_B_DQ<15>
=MEM_B_DQ<20>
=MEM_B_DQ<21>
=MEM_B_DQ<22>
=MEM_B_DQ<23>
=MEM_B_DQ<28>
=MEM_B_DQ<29>
=MEM_B_DQS_N<3>
=MEM_B_DQS_P<3>
=MEM_B_DQ<30>
=MEM_B_DQ<31>
=MEM_B_DQ<36>
=MEM_B_DQ<37>
=MEM_B_DQ<38>
=MEM_B_DQ<39>
=MEM_B_DQ<44>
=MEM_B_DQ<45>
=MEM_B_DQS_N<5>
=MEM_B_DQS_P<5>
=MEM_B_DQ<46>
=MEM_B_DQ<47>
=MEM_B_DQ<52>
=MEM_B_DQ<53>
=MEM_B_DQ<54>
=MEM_B_DQ<55>
=MEM_B_DQ<60>
=MEM_B_DQ<61>
=MEM_B_DQS_N<7>
=MEM_B_DQS_P<7>
=MEM_B_DQ<62>
=MEM_B_DQ<63>
MEM_EVENT_L
=I2C_SODIMMB_SDA
=I2C_SODIMMB_SCL

75 7 IN MEM_B_CKE<0>
75 7 IN MEM_B_CKE<1>
NC
75 7 IN MEM_B_BA<2>
75 7 IN MEM_B_A<12>
75 7 IN MEM_B_A<9>
75 7 IN MEM_B_A<8>
75 7 IN MEM_B_A<5>
75 7 IN MEM_B_A<3>
75 7 IN MEM_B_A<1>
75 7 IN MEM_B_CLK_P<0>
75 7 IN MEM_B_CLK_N<0>
75 7 IN MEM_B_A<10>
75 7 IN MEM_B_BA<0>
75 7 IN MEM_B_WE_L
75 7 IN MEM_B_CAS_L
75 7 IN MEM_B_A<13>
75 7 IN MEM_B_CS_L<1>
NC
75 7 IN MEM_B_A<15>
75 7 IN MEM_B_A<14>
75 7 IN MEM_B_A<11>
75 7 IN MEM_B_A<7>
75 7 IN MEM_B_A<6>
75 7 IN MEM_B_A<4>
75 7 IN MEM_B_A<2>
75 7 IN MEM_B_A<0>
75 7 IN MEM_B_CLK_P<1>
75 7 IN MEM_B_CLK_N<1>
75 7 IN MEM_B_BA<1>
75 7 IN MEM_B_RAS_L
75 7 IN MEM_B_CS_L<0>
75 7 IN MEM_B_ODT<0>
75 7 IN MEM_B_ODT<1>
NC
OUT MEM_EVENT_L 23 44 45
BI =I2C_SODIMMB_SDA 47
IN =I2C_SODIMMB_SCL 47

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

70 24 =PPVDDQ_S3_MEM_B

C2510 C2511 C2512 C2513 C2514 C2515 C2516 C2517 C2502 0.1UF 20% 10V CERM 402

=PPVDDQ_S3_MEM_B 24 70

C2500 10UF 20% 6.3V X5R 603
C2501 10UF 20% 6.3V X5R 603
C2518 C2519 C2520 C2521 C2522 C2523 C2524 0.1UF 20% 10V CERM 402

70 24 =PPSPD_S0_MEM_B

R2541 10K 5% 1/16W MF-LF 402
R2540 10K 5% 1/16W MF-LF 402

24 MEM_B_SA<1>
24 MEM_B_SA<0>

70 24 =PPSPD_S0_MEM_B

C2540 2.2UF 20% 6.3V CERM 402-LF

70 24 =PPDDRVTT_S0_MEM_B

PPVREF_S3_MEM_VREFCA_B 22
VOLTAGE=0.75V

C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_B 24 70

C2550 C2551 C2552 C2553 1UF 10% 10V X6S-CERM 0402

| | |
|---|---|
| SYNC_MASTER=J16_NICK | SYNC_DATE=01/10/2013 |
| PAGE TITLE | DDR3 SO-DIMM CONNECTOR B |
| Apple Inc. | DRAWING NUMBER 051-0164 SIZE D |
| | REVISION 12.4.0 |
| | BRANCH |
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THERE ARE NO PIN SWAPS

| | | | |
|---|---|---|---|
| MEM_A_DQS_N<0> | MAKE_BASE=TRUE | =MEM_A_DQS_N<0> | MEM_B_DQS_N<0> |
| MEM_A_DQS_P<0> | MAKE_BASE=TRUE | =MEM_A_DQS_P<0> | MEM_B_DQS_P<0> |
| MEM_A_DQ<7> | MAKE_BASE=TRUE | =MEM_A_DQ<7> | MEM_B_DQ<7> |
| MEM_A_DQ<6> | MAKE_BASE=TRUE | =MEM_A_DQ<6> | MEM_B_DQ<6> |
| MEM_A_DQ<5> | MAKE_BASE=TRUE | =MEM_A_DQ<5> | MEM_B_DQ<5> |
| MEM_A_DQ<4> | MAKE_BASE=TRUE | =MEM_A_DQ<4> | MEM_B_DQ<4> |
| MEM_A_DQ<3> | MAKE_BASE=TRUE | =MEM_A_DQ<3> | MEM_B_DQ<3> |
| MEM_A_DQ<2> | MAKE_BASE=TRUE | =MEM_A_DQ<2> | MEM_B_DQ<2> |
| MEM_A_DQ<1> | MAKE_BASE=TRUE | =MEM_A_DQ<1> | MEM_B_DQ<1> |
| MEM_A_DQ<0> | MAKE_BASE=TRUE | =MEM_A_DQ<0> | MEM_B_DQ<0> |
| MEM_A_DQS_N<1> | MAKE_BASE=TRUE | =MEM_A_DQS_N<1> | MEM_B_DQS_N<1> |
| MEM_A_DQS_P<1> | MAKE_BASE=TRUE | =MEM_A_DQS_P<1> | MEM_B_DQS_P<1> |
| MEM_A_DQ<15> | MAKE_BASE=TRUE | =MEM_A_DQ<15> | MEM_B_DQ<15> |
| MEM_A_DQ<14> | MAKE_BASE=TRUE | =MEM_A_DQ<14> | MEM_B_DQ<14> |
| MEM_A_DQ<13> | MAKE_BASE=TRUE | =MEM_A_DQ<13> | MEM_B_DQ<13> |
| MEM_A_DQ<12> | MAKE_BASE=TRUE | =MEM_A_DQ<12> | MEM_B_DQ<12> |
| MEM_A_DQ<11> | MAKE_BASE=TRUE | =MEM_A_DQ<11> | MEM_B_DQ<11> |
| MEM_A_DQ<10> | MAKE_BASE=TRUE | =MEM_A_DQ<10> | MEM_B_DQ<10> |
| MEM_A_DQ<9> | MAKE_BASE=TRUE | =MEM_A_DQ<9> | MEM_B_DQ<9> |
| MEM_A_DQ<8> | MAKE_BASE=TRUE | =MEM_A_DQ<8> | MEM_B_DQ<8> |
| MEM_A_DQS_N<2> | MAKE_BASE=TRUE | =MEM_A_DQS_N<2> | MEM_B_DQS_N<2> |
| MEM_A_DQS_P<2> | MAKE_BASE=TRUE | =MEM_A_DQS_P<2> | MEM_B_DQS_P<2> |
| MEM_A_DQ<23> | MAKE_BASE=TRUE | =MEM_A_DQ<23> | MEM_B_DQ<23> |
| MEM_A_DQ<22> | MAKE_BASE=TRUE | =MEM_A_DQ<22> | MEM_B_DQ<22> |
| MEM_A_DQ<21> | MAKE_BASE=TRUE | =MEM_A_DQ<21> | MEM_B_DQ<21> |
| MEM_A_DQ<20> | MAKE_BASE=TRUE | =MEM_A_DQ<20> | MEM_B_DQ<20> |
| MEM_A_DQ<19> | MAKE_BASE=TRUE | =MEM_A_DQ<19> | MEM_B_DQ<19> |
| MEM_A_DQ<18> | MAKE_BASE=TRUE | =MEM_A_DQ<18> | MEM_B_DQ<18> |
| MEM_A_DQ<17> | MAKE_BASE=TRUE | =MEM_A_DQ<17> | MEM_B_DQ<17> |
| MEM_A_DQ<16> | MAKE_BASE=TRUE | =MEM_A_DQ<16> | MEM_B_DQ<16> |
| MEM_A_DQS_N<3> | MAKE_BASE=TRUE | =MEM_A_DQS_N<3> | MEM_B_DQS_N<3> |
| MEM_A_DQS_P<3> | MAKE_BASE=TRUE | =MEM_A_DQS_P<3> | MEM_B_DQS_P<3> |
| MEM_A_DQ<31> | MAKE_BASE=TRUE | =MEM_A_DQ<31> | MEM_B_DQ<31> |
| MEM_A_DQ<30> | MAKE_BASE=TRUE | =MEM_A_DQ<30> | MEM_B_DQ<30> |
| MEM_A_DQ<29> | MAKE_BASE=TRUE | =MEM_A_DQ<29> | MEM_B_DQ<29> |
| MEM_A_DQ<28> | MAKE_BASE=TRUE | =MEM_A_DQ<28> | MEM_B_DQ<28> |
| MEM_A_DQ<27> | MAKE_BASE=TRUE | =MEM_A_DQ<27> | MEM_B_DQ<27> |
| MEM_A_DQ<26> | MAKE_BASE=TRUE | =MEM_A_DQ<26> | MEM_B_DQ<26> |
| MEM_A_DQ<25> | MAKE_BASE=TRUE | =MEM_A_DQ<25> | MEM_B_DQ<25> |
| MEM_A_DQ<24> | MAKE_BASE=TRUE | =MEM_A_DQ<24> | MEM_B_DQ<24> |
| MEM_A_DQS_N<4> | MAKE_BASE=TRUE | =MEM_A_DQS_N<4> | MEM_B_DQS_N<4> |
| MEM_A_DQS_P<4> | MAKE_BASE=TRUE | =MEM_A_DQS_P<4> | MEM_B_DQS_P<4> |
| MEM_A_DQ<39> | MAKE_BASE=TRUE | =MEM_A_DQ<39> | MEM_B_DQ<39> |
| MEM_A_DQ<38> | MAKE_BASE=TRUE | =MEM_A_DQ<38> | MEM_B_DQ<38> |
| MEM_A_DQ<37> | MAKE_BASE=TRUE | =MEM_A_DQ<37> | MEM_B_DQ<37> |
| MEM_A_DQ<36> | MAKE_BASE=TRUE | =MEM_A_DQ<36> | MEM_B_DQ<36> |
| MEM_A_DQ<35> | MAKE_BASE=TRUE | =MEM_A_DQ<35> | MEM_B_DQ<35> |
| MEM_A_DQ<34> | MAKE_BASE=TRUE | =MEM_A_DQ<34> | MEM_B_DQ<34> |
| MEM_A_DQ<33> | MAKE_BASE=TRUE | =MEM_A_DQ<33> | MEM_B_DQ<33> |
| MEM_A_DQ<32> | MAKE_BASE=TRUE | =MEM_A_DQ<32> | MEM_B_DQ<32> |
| MEM_A_DQS_N<5> | MAKE_BASE=TRUE | =MEM_A_DQS_N<5> | MEM_B_DQS_N<5> |
| MEM_A_DQS_P<5> | MAKE_BASE=TRUE | =MEM_A_DQS_P<5> | MEM_B_DQS_P<5> |
| MEM_A_DQ<47> | MAKE_BASE=TRUE | =MEM_A_DQ<47> | MEM_B_DQ<47> |
| MEM_A_DQ<46> | MAKE_BASE=TRUE | =MEM_A_DQ<46> | MEM_B_DQ<46> |
| MEM_A_DQ<45> | MAKE_BASE=TRUE | =MEM_A_DQ<45> | MEM_B_DQ<45> |
| MEM_A_DQ<44> | MAKE_BASE=TRUE | =MEM_A_DQ<44> | MEM_B_DQ<44> |
| MEM_A_DQ<43> | MAKE_BASE=TRUE | =MEM_A_DQ<43> | MEM_B_DQ<43> |
| MEM_A_DQ<42> | MAKE_BASE=TRUE | =MEM_A_DQ<42> | MEM_B_DQ<42> |
| MEM_A_DQ<41> | MAKE_BASE=TRUE | =MEM_A_DQ<41> | MEM_B_DQ<41> |
| MEM_A_DQ<40> | MAKE_BASE=TRUE | =MEM_A_DQ<40> | MEM_B_DQ<40> |
| MEM_A_DQS_N<6> | MAKE_BASE=TRUE | =MEM_A_DQS_N<6> | MEM_B_DQS_N<6> |
| MEM_A_DQS_P<6> | MAKE_BASE=TRUE | =MEM_A_DQS_P<6> | MEM_B_DQS_P<6> |
| MEM_A_DQ<55> | MAKE_BASE=TRUE | =MEM_A_DQ<55> | MEM_B_DQ<55> |
| MEM_A_DQ<54> | MAKE_BASE=TRUE | =MEM_A_DQ<54> | MEM_B_DQ<54> |
| MEM_A_DQ<53> | MAKE_BASE=TRUE | =MEM_A_DQ<53> | MEM_B_DQ<53> |
| MEM_A_DQ<52> | MAKE_BASE=TRUE | =MEM_A_DQ<52> | MEM_B_DQ<52> |
| MEM_A_DQ<51> | MAKE_BASE=TRUE | =MEM_A_DQ<51> | MEM_B_DQ<51> |
| MEM_A_DQ<50> | MAKE_BASE=TRUE | =MEM_A_DQ<50> | MEM_B_DQ<50> |
| MEM_A_DQ<49> | MAKE_BASE=TRUE | =MEM_A_DQ<49> | MEM_B_DQ<49> |
| MEM_A_DQ<48> | MAKE_BASE=TRUE | =MEM_A_DQ<48> | MEM_B_DQ<48> |
| MEM_A_DQS_N<7> | MAKE_BASE=TRUE | =MEM_A_DQS_N<7> | MEM_B_DQS_N<7> |
| MEM_A_DQS_P<7> | MAKE_BASE=TRUE | =MEM_A_DQS_P<7> | MEM_B_DQS_P<7> |
| MEM_A_DQ<63> | MAKE_BASE=TRUE | =MEM_A_DQ<63> | MEM_B_DQ<63> |
| MEM_A_DQ<62> | MAKE_BASE=TRUE | =MEM_A_DQ<62> | MEM_B_DQ<62> |
| MEM_A_DQ<61> | MAKE_BASE=TRUE | =MEM_A_DQ<61> | MEM_B_DQ<61> |
| MEM_A_DQ<60> | MAKE_BASE=TRUE | =MEM_A_DQ<60> | MEM_B_DQ<60> |
| MEM_A_DQ<59> | MAKE_BASE=TRUE | =MEM_A_DQ<59> | MEM_B_DQ<59> |
| MEM_A_DQ<58> | MAKE_BASE=TRUE | =MEM_A_DQ<58> | MEM_B_DQ<58> |
| MEM_A_DQ<57> | MAKE_BASE=TRUE | =MEM_A_DQ<57> | MEM_B_DQ<57> |
| MEM_A_DQ<56> | MAKE_BASE=TRUE | =MEM_A_DQ<56> | MEM_B_DQ<56> |

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SYNC_MASTER=J16_NICK SYNC_DATE=01/10/2013

PAGE TITLE
DDR3 ALIASES AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-0164 SIZE D

REVISION 12.4.0

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## SNK0 AC Coupling

| | | | | |
|---|---|---|---|---|
| DP_TBTSNK0_ML_C_P<0> | C2820 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK0_ML_P<0> |
| DP_TBTSNK0_ML_C_N<0> | C2821 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK0_ML_N<0> |
| DP_TBTSNK0_ML_C_P<1> | C2822 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK0_ML_P<1> |
| DP_TBTSNK0_ML_C_N<1> | C2823 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK0_ML_N<1> |
| DP_TBTSNK0_ML_C_P<2> | C2824 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK0_ML_P<2> |
| DP_TBTSNK0_ML_C_N<2> | C2825 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK0_ML_N<2> |
| DP_TBTSNK0_ML_C_P<3> | C2826 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK0_ML_P<3> |
| DP_TBTSNK0_ML_C_N<3> | C2827 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK0_ML_N<3> |
| DP_TBTSNK0_AUXCH_C_P | C2828 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK0_AUXCH_P |
| DP_TBTSNK0_AUXCH_C_N | C2829 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK0_AUXCH_N |

## SNK1 AC Coupling

| | | | | |
|---|---|---|---|---|
| DP_TBTSNK1_ML_C_P<0> | C2830 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK1_ML_P<0> |
| DP_TBTSNK1_ML_C_N<0> | C2831 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK1_ML_N<0> |
| DP_TBTSNK1_ML_C_P<1> | C2832 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK1_ML_P<1> |
| DP_TBTSNK1_ML_C_N<1> | C2833 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK1_ML_N<1> |
| DP_TBTSNK1_ML_C_P<2> | C2834 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK1_ML_P<2> |
| DP_TBTSNK1_ML_C_N<2> | C2835 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK1_ML_N<2> |
| DP_TBTSNK1_ML_C_P<3> | C2836 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK1_ML_P<3> |
| DP_TBTSNK1_ML_C_N<3> | C2837 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK1_ML_N<3> |
| DP_TBTSNK1_AUXCH_C_P | C2838 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK1_AUXCH_P |
| DP_TBTSNK1_AUXCH_C_N | C2839 | 0.1UF | 10% 16V X5R-CERM 0201 | DP_TBTSNK1_AUXCH_N |

## PCIE GEN2

CRITICAL
OMIT_TABLE
U2800
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)

| | | | | |
|---|---|---|---|---|
| PCIE_TBT_R2D_C_P<0> | C2800 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_R2D_P<0> |
| PCIE_TBT_R2D_C_N<0> | C2801 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_R2D_N<0> |
| PCIE_TBT_R2D_C_P<1> | C2802 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_R2D_P<1> |
| PCIE_TBT_R2D_C_N<1> | C2803 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_R2D_N<1> |
| PCIE_TBT_R2D_C_P<2> | C2804 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_R2D_P<2> |
| PCIE_TBT_R2D_C_N<2> | C2805 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_R2D_N<2> |
| PCIE_TBT_R2D_C_P<3> | C2806 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_R2D_P<3> |
| PCIE_TBT_R2D_C_N<3> | C2807 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_R2D_N<3> |

RECEIVE: PERP_0, PERN_0, PERP_1, PERN_1, PERP_2, PERN_2, PERP_3, PERN_3

| | | | | |
|---|---|---|---|---|
| PCIE_TBT_D2R_C_P<0> | C2840 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_D2R_P<0> |
| PCIE_TBT_D2R_C_N<0> | C2841 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_D2R_N<0> |
| PCIE_TBT_D2R_C_P<1> | C2842 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_D2R_P<1> |
| PCIE_TBT_D2R_C_N<1> | C2843 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_D2R_N<1> |
| PCIE_TBT_D2R_C_P<2> | C2844 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_D2R_P<2> |
| PCIE_TBT_D2R_C_N<2> | C2845 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_D2R_N<2> |
| PCIE_TBT_D2R_C_P<3> | C2846 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_D2R_P<3> |
| PCIE_TBT_D2R_C_N<3> | C2847 | 0.1UF | 10% 16V X5R-CERM 0201 | PCIE_TBT_D2R_N<3> |

TRANSMIT: PETP_0, PETN_0, PETP_1, PETN_1, PETP_2, PETN_2, PETP_3, PETN_3

## MISC

| | | |
|---|---|---|
| PERST_N | TBT_PCIE_RESET_L | R6 |
| PWR_ON_POC_RST_L | TBT_PWR_ON_POC_RST_L | J2 |
| MONDC0 | TP_TBT_MONDC0 | AD23 |
| MONDC1 | TP_TBT_MONDC1 | AC24 |
| MONOBS_P | TBT_MONOBSP | W18 |
| MONOBS_N | TBT_MONOBSN | W16 |
| THERMDA | TP_TBT_THERM_DP | Y7 |
| EE_DI | TBT_SPI_MOSI | R4 |
| EE_DO | TBT_SPI_MISO | P5 |
| EE_CS_N | TBT_SPI_CS_L | AD3 |
| EE_CLK | TBT_SPI_CLK | W4 |

EEPROM

| | | |
|---|---|---|
| TDI | JTAG_TBT_TDI | V1 |
| TMS | JTAG_TBT_TMS | AB3 |
| TCK | JTAG_TBT_TCK | AA6 |
| TDO | JTAG_TBT_TDO | R2 |
| TEST_EN | TBT_TEST_EN | N4 |
| TEST_PWR_GOOD | TBT_TEST_PWR_GOOD | AB5 |

JTAG/TEST PORT

| | | |
|---|---|---|
| RSENSE | TBT_RSENSE | U20 |
| RBIAS | TBT_RBIAS | W20 |
| NC | NC | U4 |

R2855 1K 1% 1/20W MF 201

Not used in host mode.

PCIE RESET

| | | |
|---|---|---|
| PCIE_RST_0_N | TP_TBT_PCIE_RESET0_L | N6 |
| PCIE_RST_1_N | TP_TBT_PCIE_RESET1_L | T1 |
| PCIE_RST_2_N | TP_TBT_PCIE_RESET2_L | Y5 |
| PCIE_RST_3_N | TP_TBT_PCIE_RESET3_L | U2 |

| | | |
|---|---|---|
| PCIE_CLKREQ_OD_N | =TBT_CLKREQ_L | W6 |
| EN_LC_PWR | TBT_EN_LC_PWR | K5 |

CLOCKS

| | | |
|---|---|---|
| REFCLK_100_IN_P | PCIE_CLK100M_TBT_P | AB21 |
| REFCLK_100_IN_N | PCIE_CLK100M_TBT_N | AD21 |
| XTAL_25_IN | SYSCLK_CLK25M_TBT_R | AA24 |
| XTAL_25_OUT | TP_TBT_XTAL25OUT | AB23 |
| TMU_CLK_OUT | TBT_TMU_CLK_OUT | AA4 |
| TMU_CLK_IN | TBT_TMU_CLK_IN | Y3 |

R2898 10K 5% 1/16W MF-LF 402
R2895 806 1% 1/16W MF-LF 402
SYSCLK_CLK25M_TBT
Divides 3.3V to 1.8V

R2897 100K 5% 1/16W MF-LF 402
NO STUFF R2899 10K 5% 1/16W MF-LF 402
R2896 1K 5% 1/16W MF-LF 402

R2880 10K 5% 1/16W MF-LF 402

TBT_DDC_XBAR_EN_L
TBT_GO2SX_BIDIR
R2881 FOR CYA, allows separation of GPIO_2/GPIO_9 if necessary. STUFF ONE OF R2881/2.
R2881 0 5% 1/16W MF-LF 402
TBT_GPIO_9
TBT_GPIO_14
NO STUFF R2883 10K 5% 1/16W MF-LF 402
R2882 10K 5% 1/16W MF-LF 402

NOTE: The following pins require testpoints:

| | |
|---|---|
| 0 - GPIO_13 | 8 - GPIO_15 |
| 1 - GPIO_1 | 9 - GPIO_11 |
| 2 - GPIO_2 | 10 - GPIO_14 |
| 3 - GPIO_3 | 11 - GPIO_0 |
| 4 - GPIO_5 | 12 - GPIO_12 |
| 5 - PCIE_RST_1_N | 13 - GPIO_10 |
| 6 - PCIE_RST_2_N | 14 - PB_LSTX |
| 7 - PCIE_RST_3_N | 15 - PB_LSRX |

## DISPLAYPORT

SINK PORT 0: DPSNK0_3_P, DPSNK0_3_N, DPSNK0_2_P, DPSNK0_2_N, DPSNK0_1_P, DPSNK0_1_N, DPSNK0_0_P, DPSNK0_0_N, DPSNK0_AUX_P, DPSNK0_AUX_N, DPSNK0_HPD

R2830 100K 5% 1/16W MF-LF 402

SINK PORT 1: DPSNK1_3_P, DPSNK1_3_N, DPSNK1_2_P, DPSNK1_2_N, DPSNK1_1_P, DPSNK1_1_N, DPSNK1_0_P, DPSNK1_0_N, DPSNK1_AUX_P, DPSNK1_AUX_N, DPSNK1_HPD

R2831 100K 5% 1/16W MF-LF 402

SOURCE PORT 0

| | | |
|---|---|---|
| DPSRC_3_P | TP_DP_TBTSRC_ML_CP<3> | A14 |
| DPSRC_3_N | TP_DP_TBTSRC_ML_CN<3> | B15 |
| DPSRC_2_P | TP_DP_TBTSRC_ML_CP<2> | A12 |
| DPSRC_2_N | TP_DP_TBTSRC_ML_CN<2> | B13 |
| DPSRC_1_P | TP_DP_TBTSRC_ML_CP<1> | A10 |
| DPSRC_1_N | TP_DP_TBTSRC_ML_CN<1> | B11 |
| DPSRC_0_P | TP_DP_TBTSRC_ML_CP<0> | A8 |
| DPSRC_0_N | TP_DP_TBTSRC_ML_CN<0> | B9 |
| DPSRC_AUX_P | TP_DP_TBTSRC_AUXCH_CP | C2 |
| DPSRC_AUX_N | TP_DP_TBTSRC_AUXCH_CN | D3 |
| DPSRC_HPD_OD | DP_TBTSRC_HPD | V3 |

R2832 100K 5% 1/16W MF-LF 402

| | | |
|---|---|---|
| GPIO_2/GO2SX | TBT_GO2SX_BIDIR | Y1 |
| (FORCE_PWR) GPIO_3 | TBT_PWR_EN | W2 |
| GPIO_4/WAKE_N_OD | =TBT_WAKE_L | J4 |
| GPIO_5/CIO_PLUG_EVENT | TBT_CIO_PLUG_EVENT | AA2 |
| GPIO_6/CIO_SDA_OD | I2C_TBTRTR_SDA | AB1 |
| GPIO_7/CIO_SCL_OD | I2C_TBTRTR_SCL | AC2 |
| GPIO_8/EN_CIO_PWR_OD* | (TBT_EN_CIO_PWR_L) | P3 |
| GPIO_9/OK2GO2SX_OD* | TBT_GPIO_9 | M5 |
| GPIO_14 | TBT_GPIO_14 | T3 |
| GPIO_15 | TBT_DDC_XBAR_EN_L | V5 |

TBT_PWR_REQ_L
TBT_EN_CIO_PWR_L
MAKE_BASE=TRUE

I2C_TBTRTR_SDA
I2C_TBTRTR_SCL

R2889 3.3K 5% 1/16W MF-LF 402
R2894 3.3K 5% 1/16W MF-LF 402

R2885 10K 5% 1/16W MF-LF 402
R2886 10K 5% 1/16W MF-LF 402

TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN

R2888 10K 5% 1/16W MF-LF 402
R2887 10K 5% 1/16W MF-LF 402

PORT0: PA_CIO0_TX_P/DP_SRC_0_P, PA_CIO0_TX_N/DP_SRC_0_N, PA_CIO0_RX_P, PA_CIO0_RX_N, PA_CONFIG1/CIO_0_LSEO, PA_CONFIG2/CIO_0_LSOE

PORT2: PB_CIO2_TX_P/DP_SRC_0_P, PB_CIO2_TX_N/DP_SRC_0_N, PB_CIO2_RX_P, PB_CIO2_RX_N, PB_CONFIG1/CIO_2_LSEO, PB_CONFIG2/CIO_2_LSOE

PORT1: PA_CIO1_TX_P/DP_SRC_2_P, PA_CIO1_TX_N/DP_SRC_2_N, PA_CIO1_RX_P, PA_CIO1_RX_N, PA_LSTX/CIO_3_LSEO, PA_LSRX/CIO_3_LSOE

PORT3: PB_CIO3_TX_P/DP_SRC_2_P, PB_CIO3_TX_N/DP_SRC_2_N, PB_CIO3_RX_P, PB_CIO3_RX_N, PB_LSTX/CIO_3_LSEO, PB_LSRX/CIO_3_LSOE

| | | |
|---|---|---|
| PA_DPSRC_1_P | DP_TBTPB_ML_C_P<1> | A20 |
| PA_DPSRC_1_N | DP_TBTPB_ML_C_N<1> | B21 |
| PA_DPSRC_3_P | DP_TBTPB_ML_C_P<3> | A22 |
| PA_DPSRC_3_N | DP_TBTPB_ML_C_N<3> | B23 |
| PA_AUX_P | DP_TBTPA_AUXCH_C_P | F3 |
| PA_AUX_N | DP_TBTPA_AUXCH_C_N | F1 |
| PA_DPSRC_HPD | DP_TBTPA_HPD | H1 |
| GPIO_0/PA_HV_EN/BYP0 | TBT_A_HV_EN | G2 |
| GPIO_10/PA_CIO_SEL/BYP1 | TBT_A_CIO_SEL | M3 |
| GPIO_12/PA_DP_PWRDN/BYP2 | TBT_A_DP_PWRDN | H3 |
| PB_DPSRC_1_P | DP_TBTPB_ML_C_P<1> | A20 |
| PB_DPSRC_1_N | DP_TBTPB_ML_C_N<1> | B21 |
| PB_DPSRC_3_P | DP_TBTPB_ML_C_P<3> | A22 |
| PB_DPSRC_3_N | DP_TBTPB_ML_C_N<3> | B23 |
| PB_AUX_P | DP_TBTPB_AUXCH_C_P | D1 |
| PB_AUX_N | DP_TBTPB_AUXCH_C_N | E2 |
| PB_DPSRC_HPD | DP_TBTPB_HPD | K3 |
| GPIO_1/PB_HV_EN/BYP0 | TBT_B_HV_EN | M1 |
| GPIO_11/PB_CIO_SEL/BYP1 | TBT_B_CIO_SEL | L2 |
| GPIO_13/PB_DP_PWRDN/BYP2 | TBT_B_DP_PWRDN | L4 |

## PORTS

| | | |
|---|---|---|
| PB_CIO2_TX_P/DP_SRC_0_P | TBT_B_R2D_C_P<0> | R24 |
| PB_CIO2_TX_N/DP_SRC_0_N | TBT_B_R2D_C_N<0> | N24 |
| PB_CIO2_RX_P | TBT_B_D2R_P<0> | R22 |
| PB_CIO2_RX_N | TBT_B_D2R_N<0> | N22 |
| PB_CONFIG1/CIO_2_LSEO | TBT_B_CONFIG1_BUF | P1 |
| PB_CONFIG2/CIO_2_LSOE | TBT_B_CONFIG2_RC | H5 |
| PB_CIO3_TX_P/DP_SRC_2_P | TBT_B_R2D_C_P<1> | W24 |
| PB_CIO3_TX_N/DP_SRC_2_N | TBT_B_R2D_C_N<1> | U24 |
| PB_CIO3_RX_P | TBT_B_D2R_P<1> | W22 |
| PB_CIO3_RX_N | TBT_B_D2R_N<1> | U22 |
| PB_LSTX/CIO_3_LSEO | TBT_B_LSTX | L6 |
| PB_LSRX/CIO_3_LSOE | TBT_B_LSRX | G6 |

| | | |
|---|---|---|
| PA_CIO0_TX_P/DP_SRC_0_P | TBT_A_R2D_C_P<0> | G24 |
| PA_CIO0_TX_N/DP_SRC_0_N | TBT_A_R2D_C_N<0> | E24 |
| PA_CIO0_RX_P | TBT_A_D2R_P<0> | G22 |
| PA_CIO0_RX_N | TBT_A_D2R_N<0> | E22 |
| PA_CONFIG1/CIO_0_LSEO | TBT_A_CONFIG1_BUF | K1 |
| PA_CONFIG2/CIO_0_LSOE | TBT_A_CONFIG2_RC | G4 |
| PA_CIO1_TX_P/DP_SRC_2_P | TBT_A_R2D_C_P<1> | L24 |
| PA_CIO1_TX_N/DP_SRC_2_N | TBT_A_R2D_C_N<1> | J24 |
| PA_CIO1_RX_P | TBT_A_D2R_P<1> | L22 |
| PA_CIO1_RX_N | TBT_A_D2R_N<1> | J22 |
| PA_LSTX/CIO_1_LSEO | TBT_A_LSTX | N2 |
| PA_LSRX/CIO_1_LSOE | TBT_A_LSRX | J6 |

R2825 0 5% 1/16W MF-LF 402
R2829 0 5% 1/16W MF-LF 402

| | | |
|---|---|---|
| DPSNK0_3_P | DP_TBTSNK0_ML_P<3> | E14 |
| DPSNK0_3_N | DP_TBTSNK0_ML_N<3> | D13 |
| DPSNK0_2_P | DP_TBTSNK0_ML_P<2> | E16 |
| DPSNK0_2_N | DP_TBTSNK0_ML_N<2> | D15 |
| DPSNK0_1_P | DP_TBTSNK0_ML_P<1> | E18 |
| DPSNK0_1_N | DP_TBTSNK0_ML_N<1> | D17 |
| DPSNK0_0_P | DP_TBTSNK0_ML_P<0> | E20 |
| DPSNK0_0_N | DP_TBTSNK0_ML_N<0> | D19 |
| DPSNK0_AUX_P | DP_TBTSNK0_AUXCH_P | A6 |
| DPSNK0_AUX_N | DP_TBTSNK0_AUXCH_N | B5 |
| DPSNK0_HPD | DP_TBTSNK0_HPD | U6 |
| DPSNK1_3_P | DP_TBTSNK1_ML_P<3> | E6 |
| DPSNK1_3_N | DP_TBTSNK1_ML_N<3> | D5 |
| DPSNK1_2_P | DP_TBTSNK1_ML_P<2> | E8 |
| DPSNK1_2_N | DP_TBTSNK1_ML_N<2> | D7 |
| DPSNK1_1_P | DP_TBTSNK1_ML_P<1> | E10 |
| DPSNK1_1_N | DP_TBTSNK1_ML_N<1> | D9 |
| DPSNK1_0_P | DP_TBTSNK1_ML_P<0> | E12 |
| DPSNK1_0_N | DP_TBTSNK1_ML_N<0> | D11 |
| DPSNK1_AUX_P | DP_TBTSNK1_AUXCH_P | A4 |
| DPSNK1_AUX_N | DP_TBTSNK1_AUXCH_N | B3 |
| DPSNK1_HPD | DP_TBTSNK1_HPD | T5 |

R2801 0 5% 1/20W MF 0201

OMIT R2815 NOSTUFF NONE NONE NONE 402

DEBUG: For monitoring current/voltage
DEBUG: For monitoring clock
Use AA8 GND ball for THERM_DN

NO STUFF C2810 0.1UF 10% 16V X7R-CERM 0402

R2890 3.3K 5% 1/16W MF-LF 402
R2891 3.3K 5% 1/16W MF-LF 402
C2890 1UF 10% 6.3V CERM 402
R2892 3.3K 5% 1/16W MF-LF 402
R2893 3.3K 5% 1/16W MF-LF 402

CRITICAL
OMIT_TABLE
U2890 M95256-RMC6XG MLP
VCC, D, C, S*, W*, HOLD*, VSS, THM PAD, Q

(TBT_SPI_MOSI), (TBT_SPI_CLK), (TBT_SPI_CS_L), TBTROM_WP_L, TBTROM_HOLD_L, (TBT_SPI_MISO)

R2810 47K 5% 1/16W MF-LF 402

=PP3V3_S4_TBT
=PP3V3_TBTLC_RTR
TBT_SPI_CLK_RES

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

SYNC_MASTER=J16_MAX SYNC_DATE=02/11/2013

PAGE TITLE: Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER: 051-0164 SIZE: D
REVISION: 12.4.0
BRANCH:
PAGE: 28 OF 123
SHEET: 26 OF 86

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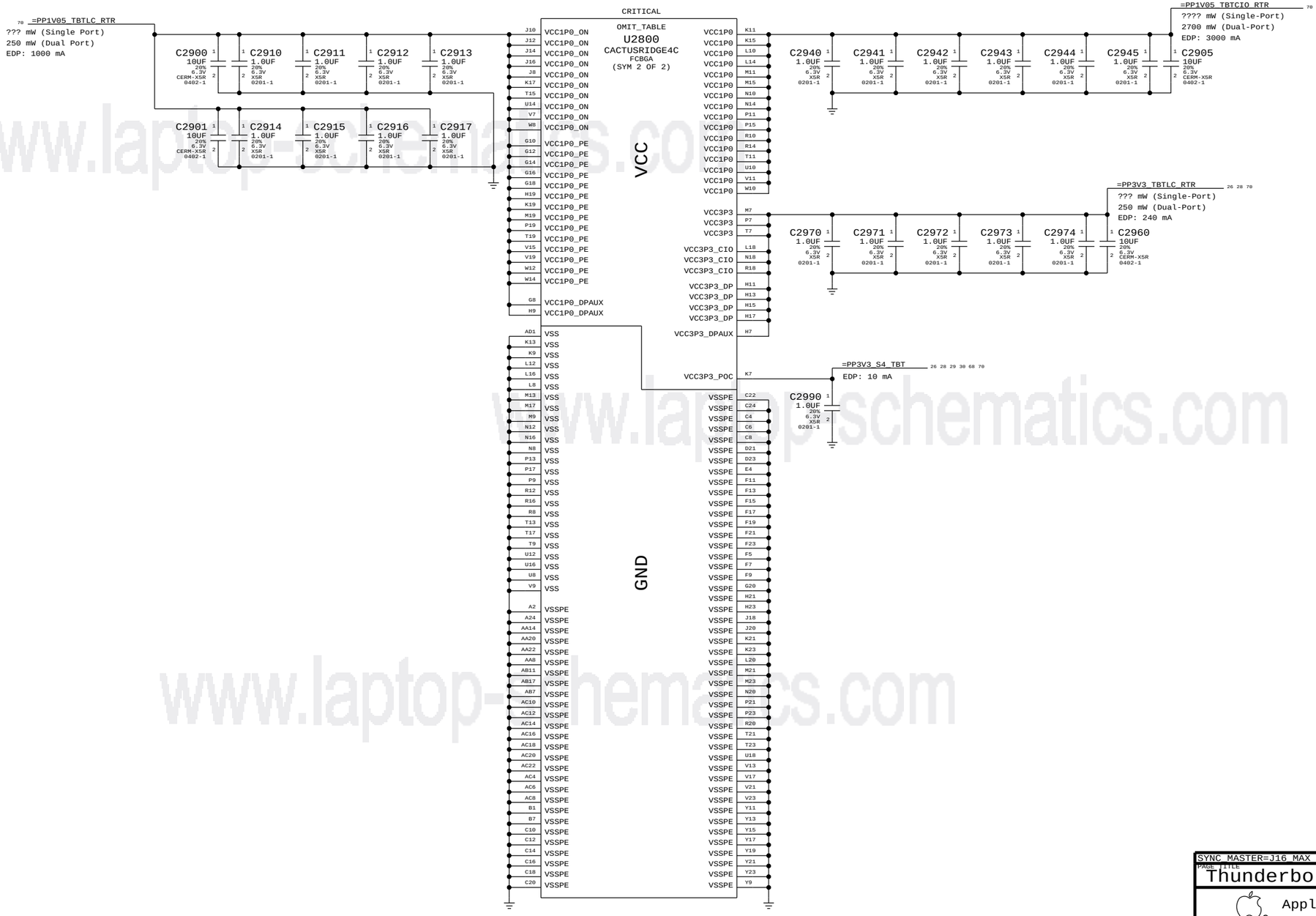


EDP current / power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC_MASTER=J16_MAX SYNC_DATE=02/11/2013

PAGE TITLE
Thunderbolt Host (2 of 2)

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## Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

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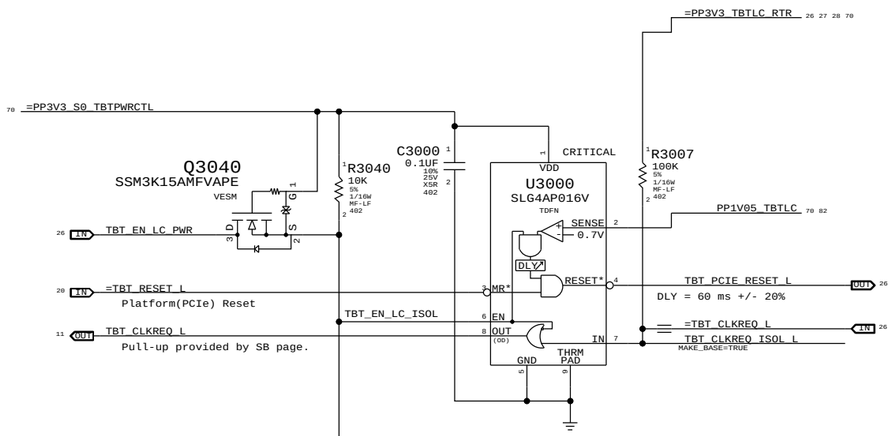
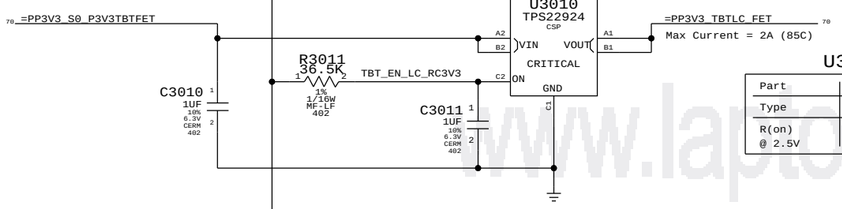
### Supervisor & CLKREQ# Isolation

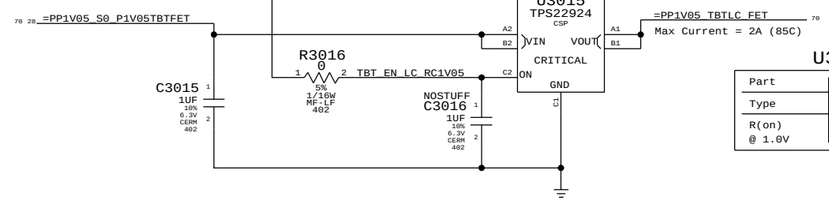



### 3.3V TBT "LC" Switch




| U3010 | |
|---|---|
| Part | TPS22924C |
| Type | Load Switch |
| R(on) @ 2.5V | 18.5 mOhm Typ<br>25.8 mOhm Max |

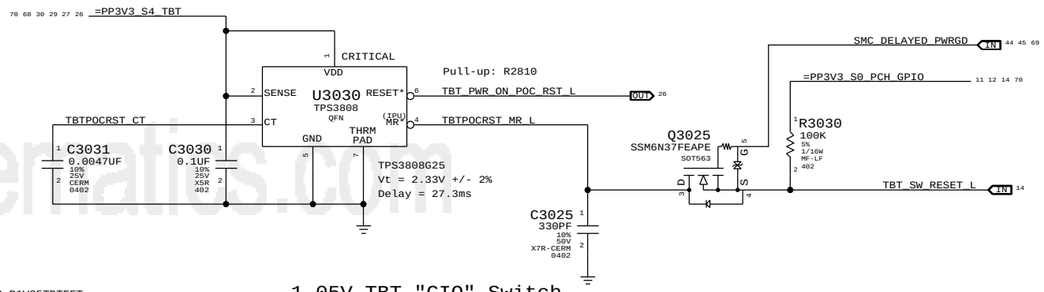
### 1.05V TBT "LC" Switch



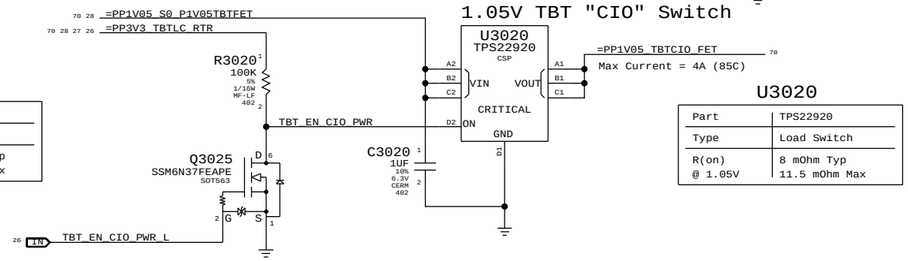

| U3015 | |
|---|---|
| Part | TPS22924C |
| Type | Load Switch |
| R(on) @ 1.0V | 20.3 mOhm Typ<br>28.6 mOhm Max |

### TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.




### 1.05V TBT "CIO" Switch




| U3020 | |
|---|---|
| Part | TPS22920 |
| Type | Load Switch |
| R(on) @ 1.05V | 8 mOhm Typ<br>11.5 mOhm Max |

SYNC_MASTER=J16_MAX SYNC_DATE=02/11/2013

PAGE TITLE
# Thunderbolt Power Support

Apple Inc.

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# 3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

| | Nominal | Min | Max |
|---|---|---|---|
| IV3P3 | 1100mA | 1030mA | 1200mA |
| IHVS0 | 890mA | 830mA | 930mA (assumes 15V, 12W minimum) |
| IHVS3 | 890mA | 830mA | 930mA (assumes 3S, 9-12.6V, 7.5-11.7W) |

=PP3V3_S4_TBTAPWRSW
CRITICAL C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C3280 22UF 20% 6.3V X5R-CERM-1 603
C3281 0.1UF 20% 10V CERM 402
=PPHV_SW_TBTAPWRSW
18.9V Max
C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 50V X7R 603-1
CRITICAL U3210 CD3210A0RGP QFN
V3P3
VHV
V3P3OUT
OUT
NC
RSVD
EN
HV_EN
S0
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN
PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C3211 0.1UF 10% 50V X7R 603-1
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
12V: See below
TBTHV:P15V
R3210 22.6K 1% 1/16W MF-LF 402
R3211 22.6K 1% 1/16W MF-LF 402
R3212 36.5K 1% 1/16W MF-LF 402
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R3213 22.6K 1% 1/16W MF-LF 402
R3214 22.6K 1% 1/16W MF-LF 402
Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

For 12V systems:

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 114S0338 | 2 | RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF | R3210,R3213 | | TBTHV:P12V |
| 114S0338 | 2 | RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF | R3211,R3214 | | TBTHV:P12V |

| | Nominal | Min | Max |
|---|---|---|---|
| IHVS0/S3 | 1120mA | 1090mA | 1170mA (12W minimum) |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 311S0596 | 311S0593 | | ALL | TI Alternate |
| 128S0398 | 128S0220 | | ALL | 3.3V INPUT CAP |

=PP3V3_S4_TBT
C3220 0.1UF 10% 6.3V CERM-X5R 0201
C3221 0.1UF 10% 6.3V CERM-X5R 0201
R3227 10K 5% 1/20W MF 201
R3229 100K 5% 1/20W MF 201
VDD
CRITICAL U3220 CBTL05023 HVQFN
TBT_A_BIAS VOLTAGE=3.3V
C3225 0.1UF 10% 6.3V CERM-X5R 0201
TBT_A_CIO_SEL
DP_AUXIO_EN
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
C3230 0.1UF 10% 6.3V CERM-X5R 0201
C3231 0.1UF 10% 6.3V CERM-X5R 0201
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
C3232 0.22UF 20% 6.3V X5R 0201
C3233 0.22UF 20% 6.3V X5R 0201
TBT_A_LSTX
TBT_A_LSRX_UNBUF
DP_TBTPA_HPD
BIASIN
AUXIO_EN
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX
LSRX
DP_PD
HPDOUT
BIASOUT
AUXIO-
AUXIO+
CA_DET
DPMLO+
DPMLO-
HPD
GND_THMPAD
DP_A_AUXCH_DDC_N
DP_A_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD
R3226 1M 5% 1/20W MF 201
R3228 100K 5% 1/20W MF 201
=PP3V3_S4_TBT
CRITICAL U3260 74AUP1T97GM SOT886
TBT_A_LSRX
C3260 0.1UF 10% 16V X5R-CERM 0201

# Thunderbolt Connector A

L3200 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C3200 0.01UF 10% 50V X7R-CERM 0402
R3201 12 5% 1/20W MF 201
TBTACONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
C3201 0.01UF 10% 50V X7R-CERM 0402
TBT Dir
DP Dir
C3205 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
DP Dir
TBT Dir
TBT: TX_0
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
GND_VOID=TRUE (Both C's)
C3270 0.22UF 20% 6.3V X5R 0201
C3271 0.22UF 20% 6.3V X5R 0201
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
C3206 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
TBT: LSX_R2P/P2R (P/N)
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_1
C3272 0.22UF 20% 6.3V X5R 0201
C3273 0.22UF 20% 6.3V X5R 0201
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201
TBT_A_R2D_C_N<1>
TBT_A_R2D_C_P<1>
NOTE: Polarity Swapped for layout!
470k R's for ESD protection on AC-coupled signals.
CRITICAL J3200 DUAL-MDP-K70 F-ANG-TH
SHLD
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
PORT A SHLD
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
J16:514-0824 / J17:514-0831
TBT_A_D2R_N<0>
TBT_A_D2R_P<0>
C3274 0.47UF 20% 4V CERM-X5R-1 201
C3275 0.47UF 20% 4V CERM-X5R-1 201
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
NOTE: Polarity Swapped for layout!
R3294 1K 5% 1/20W MF 201
R3295 1K 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
C3278 0.22UF 20% 6.3V X5R 0201
C3279 0.22UF 20% 6.3V X5R 0201
TBT: Terminated
R3278 470K 5% 1/20W MF 201
R3279 470K 5% 1/20W MF 201
TBT_A_BIAS
R3298 2.2K 5% 1/20W MF 201
R3299 2.2K 5% 1/20W MF 201
TBT_A_D2R_N<1>
TBT_A_D2R_P<1>
C3276 0.47UF 20% 4V CERM-X5R-1 201
C3277 0.47UF 20% 4V CERM-X5R-1 201
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>
NOTE: Polarity Swapped for layout!
CRITICAL D3298 BAR90-02LRH TSLP-2-7
CRITICAL D3299 BAR90-02LRH TSLP-2-7
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
CRITICAL L3298 650NH-5%-0.430MA-0.52OHM 0603
CRITICAL L3299 650NH-5%-0.430MA-0.52OHM 0603
DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N
C3298 30PF 5% 50V C0G-NP0 0402
C3299 30PF 5% 50V C0G-NP0 0402
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R-CERM 0201
C3295 330PF 10% 16V X7R-CERM 0201
R3241 100K 5% 1/20W MF 201
C3202 0.01UF 10% 25V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

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SYNC_MASTER=J16_MAX SYNC_DATE=02/11/2013
PAGE TITLE: Thunderbolt Connector A
Apple Inc.
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# 3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

=PP3V3_S4_TBTBPWRSW

| | Nominal | Min | Max |
|---|---|---|---|
| IV3P3 | 1100mA | 1030mA | 1200mA |
| IHVS0 | 890mA | 830mA | 930mA (assumes 15V, 12W minimum) |
| IHVS3 | 890mA | 830mA | 930mA (assumes 3S, 9-12.6V, 7.5-11.7W) |

CRITICAL C3387 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C3380 22UF 20% 6.3V X5R-CERM-1 603
C3381 0.1UF 20% 10V CERM 402

=PPHV_SW_TBTBPWRSW
18.9V Max

C3315 4.7UF 10% 25V X5R-CERM 0603
C3310 0.1UF 10% 50V X7R 603-1

CRITICAL U3310 CD3210A0RGP QFN

V3P3 V3P3OUT NC
VHV OUT PPHV_SW_TBTBPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C3311 0.1UF 10% 50V X7R 603-1

RSVD RSVD
EN ISET_V3P3 TBTBPWRSW_ISET_V3P3
=TBTBPWRSW_EN
HV_EN ISET_S0 TBTBPWRSW_ISET_S0
TBT_B_HV_EN
S0 ISET_S3 TBTBPWRSW_ISET_S3
=TBT_S0_EN
GND THRM PAD

12V: See below

TBTHV:P15V
R3310 22.6K 1% 1/16W MF-LF 402
R3311 22.6K 1% 1/16W MF-LF 402
R3312 36.5K 1% 1/16W MF-LF 402

TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
TBTHV:P15V
R3313 22.6K 1% 1/16W MF-LF 402
R3314 22.6K 1% 1/16W MF-LF 402
Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

For 12V systems:

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 114S0338 | 2 | RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF | R3310,R3313 | | TBTHV:P12V |
| 114S0338 | 2 | RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF | R3311,R3314 | | TBTHV:P12V |

| | Nominal | Min | Max |
|---|---|---|---|
| IHVS0/S3 | 1120mA | 1090mA | 1170mA (12W minimum) |

# Thunderbolt Connector B

=PP3V3_S4_TBT

C3320 0.1UF 10% 6.3V CERM-X5R 0201
C3321 0.1UF 10% 6.3V CERM-X5R 0201
R3327 10K 5% 1/20W MF 201
R3329 100K 5% 1/20W MF 201

CRITICAL U3320 CBTL05023 HVQFN VDD

TBT_B_BIAS VOLTAGE=3.3V
C3325 0.1UF 10% 6.3V CERM-X5R 0201

TBT_B_CIO_SEL → BIASIN
DP_AUXIO_EN → AUXIO_EN
DP_TBTPB_AUXCH_C_N → C3330 0.1UF → AUX-
DP_TBTPB_AUXCH_C_P → C3331 0.1UF → AUX+
DP_TBTPB_DDC_DATA → DDC_DAT
DP_TBTPB_DDC_CLK → DDC_CLK
TBT_B_CONFIG1_BUF → CA_DETOUT
DP_TBTPB_ML_C_P<1> → C3332 0.22UF → DP+
DP_TBTPB_ML_C_N<1> → C3333 0.22UF → DP-
TBT_B_LSTX → LSTX
TBT_B_LSRX_UNBUF → LSRX
TBT_B_DP_PWRDN → DP_PD
DP_TBTPB_HPD → HPDOUT

BIASOUT → C3325
AUXIO- → DP_B_AUXCH_DDC_N
AUXIO+ → DP_B_AUXCH_DDC_P
TBT: RX_1 Bias Sink
CA_DET → TBT_B_CONFIG1_RC
DPMLO+ → DP_B_LSX_ML_P<1>
DPMLO- → DP_B_LSX_ML_N<1>
TBT: LSX_B_R2P/P2R (P/N)
HPD → TBT_B_HPD

GND_THMPAD

=PP3V3_S4_TBT
CRITICAL U3360 74AUP1T97GM SOT886
TBT_B_LSRX
C3360 0.1UF 10% 16V X5R-CERM 0201

R3326 1M 5% 1/20W MF 201
R3328 100K 5% 1/20W MF 201

L3300 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTBPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C3300 0.01UF 10% 50V X7R-CERM 0402
R3301 12 5% 1/20W MF 201
TBTBCONN_20_RC
C3301 0.01UF 10% 50V X7R-CERM 0402

C3305 0.01UF 10% 25V X5R-CERM 0201
TBTBCONN_1_C
(0-18.9V)
DP Dir TBT Dir
TBT: TX_0

GND_VOID=TRUE (Both C's)
C3370 0.22UF 20% 6.3V X5R 0201
C3371 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
R3370 470K 5% 1/20W MF 201
R3371 470K 5% 1/20W MF 201

C3306 0.01UF 10% 25V X5R-CERM 0201
TBTBCONN_7_C
(0-18.9V)
TBT: LSX_R2P/P2R (P/N)
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>

NOTE: Polarity Swapped for Layout!

GND_VOID=TRUE (Both C's)
C3372 0.22UF 20% 6.3V X5R 0201
C3373 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_N<1>
TBT_B_R2D_C_P<1>
R3372 470K 5% 1/20W MF 201
R3373 470K 5% 1/20W MF 201

TBT: TX_1

470k R's for ESD protection on AC-coupled signals.

CRITICAL J3200 DUAL-MDP-K70 F-ANG-TH SHLD PORT B SHLD

| | | | |
|---|---|---|---|
| 22 HPD | | GND0 | 21 |
| 24 CONFIG1 | | ML_LANE0P | 23 |
| 26 CONFIG2 | | ML_LANE0N | 25 |
| 28 GND2 | | GND1 | 27 |
| 30 ML_LANE3P | | ML_LANE1P | 29 |
| 32 ML_LANE3N | | ML_LANE1N | 31 |
| 34 GND4 | | GND3 | 33 |
| 36 AUX_CHP | | ML_LANE2P | 35 |
| 38 AUX_CHN | | ML_LANE2N | 37 |
| 40 DP_PWR | | RETURN | 39 |

65 64 63 62 61 60 59

TBT_B_D2R_N<0> → C3374 0.47UF → TBT_B_D2R_C_P<0>
TBT_B_D2R_P<0> → C3375 0.47UF → TBT_B_D2R_C_N<0>
R3394 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3395 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE

NOTE: Polarity Swapped for Layout!

DP_TBTPB_ML_C_P<3> → C3378 0.22UF → DP_TBTPB_ML_P<3>
DP_TBTPB_ML_C_N<3> → C3379 0.22UF → DP_TBTPB_ML_N<3>
R3378 470K 5% 1/20W MF 201
R3379 470K 5% 1/20W MF 201
TBT: Terminated

TBT_B_BIAS
R3398 2.2K 5% 1/20W MF 201
R3399 2.2K 5% 1/20W MF 201

TBT_B_D2R_N<1> → C3376 0.47UF → TBT_B_D2R_C_P<1>
TBT_B_D2R_P<1> → C3377 0.47UF → TBT_B_D2R_C_N<1>

CRITICAL
D3398 BAR90-02LRH TSLP-2-7 → TBT_B_D2R1_AUXDDC_P
D3399 BAR90-02LRH TSLP-2-7 → TBT_B_D2R1_AUXDDC_N

CRITICAL L3398 650NH-5%-0.430MA-0.52OHM 0603 NO_XNET_CONNECTION=TRUE
CRITICAL L3399 650NH-5%-0.430MA-0.52OHM 0603 NO_XNET_CONNECTION=TRUE

DP_B_AUXCH_DDC_P
DP_B_AUXCH_DDC_N
C3398 30PF 5% 50V C0G-NP0 0402
C3399 30PF 5% 50V C0G-NP0 0402

TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC
R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
C3394 330PF 10% 16V X7R-CERM 0201
C3395 330PF 10% 16V X7R-CERM 0201
R3341 100K 5% 1/20W MF 201

C3302 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

J16:514-0824 / J17:514-0831

SYNC_MASTER=J16_MAX SYNC_DATE=02/11/2013

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

DRAWING NUMBER 051-0164 SIZE D
REVISION 12.4.0
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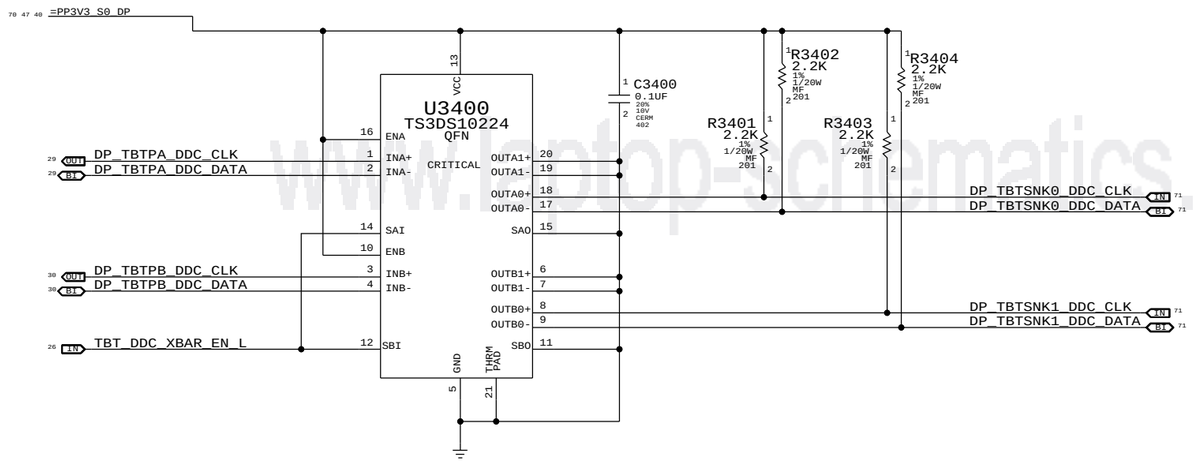
# Dual-Port Host DDC Crossbar

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SYNC_MASTER=J16_MAX SYNC_DATE=02/11/2013

PAGE TITLE: TBT DDC Crossbar

Apple Inc.

DRAWING NUMBER: 051-0164 SIZE: D

REVISION: 12.4.0

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# AIRPORT BLUETOOTH

AP & BT Load Switch

| | |
|---|---|
| SWITCH | TPS22924B |
| CHANNEL | N-TYPE |
| RDS(ON) | 18.4 MOHM @3.3V |
| LOADING | 2 A (EDP) |

=PP3V3_S4_AP → U3510 TPS22924 CSP (A2/B2 VIN, A1/B1 VOUT, C2 ON, GND, CRITICAL, C1) → PP3V3_S4_AP_FET
MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V

AP_PWR_EN (EN) → C2

CRITICAL L3502 FERR-220-OHM-2.5A 0603 → PP3V3_S4_AP_FLT
MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V

C3502 0.1UF 10% 16V X7R-CERM 0402
C3503 0.1UF 10% 16V X7R-CERM 0402
C3504 10UF 20% 6.3V X5R 603

C3505 0.1UF 0201 10V CERM-X5R (PLACE_NEAR=J3500.4:7mm)
C3506 0.1UF 0201 10V CERM-X5R (PLACE_NEAR=J3500.5:7mm)

PCIE_AP_R2D_C_N (EN) → C3505
PCIE_AP_R2D_C_P (EN) → C3506

514S0335 CRITICAL
J3500 SSD-K99 F-RT-SM1

| | |
|---|---|
| 1 | |
| 2 | AP_EVENT_L (BI) |
| 3 | |
| 4 | PCIE_AP_R2D_N |
| 5 | PCIE_AP_R2D_P |
| 6 | |
| 7 | PCIE_CLK100M_AP_N (IN) |
| 8 | PCIE_CLK100M_AP_P (IN) |
| 9 | |
| 10 | PCIE_AP_D2R_P (OUT) |
| 11 | PCIE_AP_D2R_N (OUT) |
| 12 | |
| 13 | AP_WAKE_L |
| 14 | AP_RESET_CONN_L |
| 15 | AP_CLKREQ_Q_L |
| 16 | USB_BT_MUX_N |
| 17 | USB_BT_MUX_P |
| 18 | |
| 19 | |
| 20 | |
| 21 | |

=PP3V3_G3H_BT → U3540 TPS22924B CSP (A2/B2 VIN, A1/B1 VOUT, C2 ON, GND, CRITICAL, C1) → PP3V3_G3H_BT_FET
VOLTAGE=3.3V, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM

CRITICAL L3501 FERR-220-OHM-2.5A 0603 → PP3V3_G3H_BT_FLT
VOLTAGE=3.3V, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM

C3507 0.1UF 10% 16V X7R-CERM 0402
C3508 10UF 20% 6.3V X5R 603

BT_RESET_MASK_L

BT_RESET_MASK_L GATES BT_PWR_RST_L
until after S0 GPIO is guranteed stable

CRITICAL Q3540 DMC2400UV SOT563 (P-CHN, D, S, G)

BT_PWR_RST_L (IN)

SMC_G3_WAKESRC_EN → R3542 10K 5% 1/16W MF-LF 402 → BT_PWR_EN

Q3540 DMC2400UV SOT563 (P-CHN)

BT_PWR_RST → R3543 10K 5% 1/16W MF-LF 402
BT_PWR_RST → C3541 0.01UF 20% 16V CERM 402

Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%

PP3V3_S4_AP_FLT → R3530 100K 1% 1/16W MF-LF 402
PP3V3_S4_AP_FLT → R3531 232K 1% 1/16W MF-LF 402
P3V3AP_VMON
R3532 100K 1% 1/16W MF-LF 402

=PP3V3_S4_AP → C3530 0.1UF 20% 16V CERM 402

CRITICAL U3530 SLG4AP041V TDFN (VDD, SENSE, VREF, DLY, RESET*, MR*, EN, IN, OUT (OD), THRM PAD, GND)

AP_RESET_CONN_L → RESET*
AP_CLKREQ_Q_L → IN
MR* → AP_RESET_L (IN)
EN ← AP_PWR_EN (IN)
OUT (OD) → AP_CLKREQ_L (OUT)

Wake from BT in G3H circuit

SMC_PME_S4_WAKE_L (OUT) → CRITICAL Q3501 SSM3K15AMFVAPE VESM (D, S, G)

=PP3V3_G3H_BT → C3500 0.1UF 20% 16V CERM 402

CRITICAL U3501 USB3740 DFN

| | |
|---|---|
| USB_BT_N (BI) | DP_2 |
| USB_BT_P (BI) | DM_2 |
| USB_BT_WAKEN | DP_1 |
| NC | DM_1 |
| | OE* |
| PM_SLP_S5_L (IN) | S |
| | GND |
| DP | USB_BT_MUX_N |
| DM | USB_BT_MUX_P |

R3501 15K 1% 1/20W MF 201

SIGNAL_MODEL=SWI_USB3740_DFN_USB3740_MOJO

Q3570 SSM3K15AMFVAPE VESM CRITICAL
PP3V3_S4_AP_FLT → R3570 10K 5% 1/16W MF-LF 402
PCIE_WAKE_L → Q3570 → AP_WAKE_L

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| | |
|---|---|
| SYNC_MASTER=J16_FIYIN | SYNC_DATE=01/11/2013 |
| PAGE TITLE | AIRPORT/BT |
| Apple Inc. | DRAWING NUMBER 051-0164 |
| | SIZE D |
| | REVISION 12.4.0 |
| | BRANCH |
| | PAGE 35 OF 123 |
| | SHEET 32 OF 86 |

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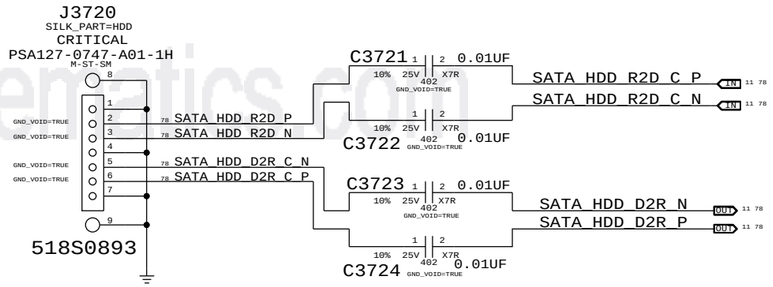
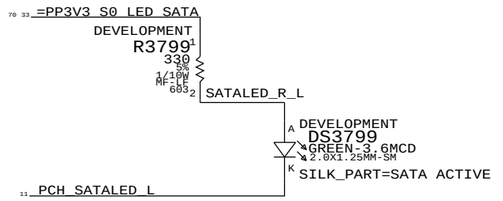
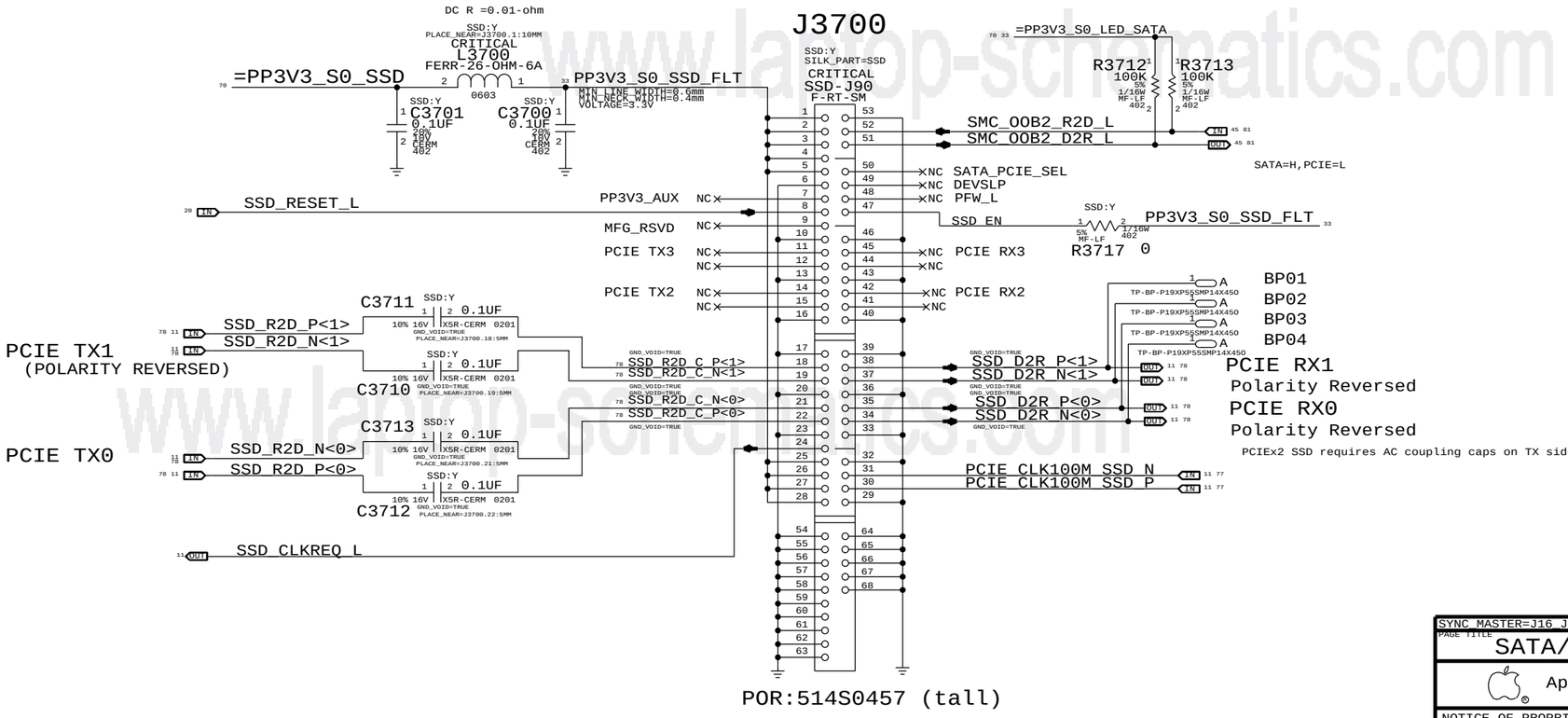
## HDD SIGNAL CONNECTOR




## SATA Activity LED




## GS3 SSD




POR:514S0457 (tall)

| | |
|---|---|
| SYNC_MASTER=J16_JERRY | SYNC_DATE=01/07/2013 |
| PAGE TITLE | SATA/SSD Connectors |
| Apple Inc. | DRAWING NUMBER 051-0164 · SIZE D |
| | REVISION 12.4.0 |
| | BRANCH |
| | PAGE 37 OF 123 |
| | SHEET 33 OF 86 |

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# HDD POWER/OOB CONNECTOR

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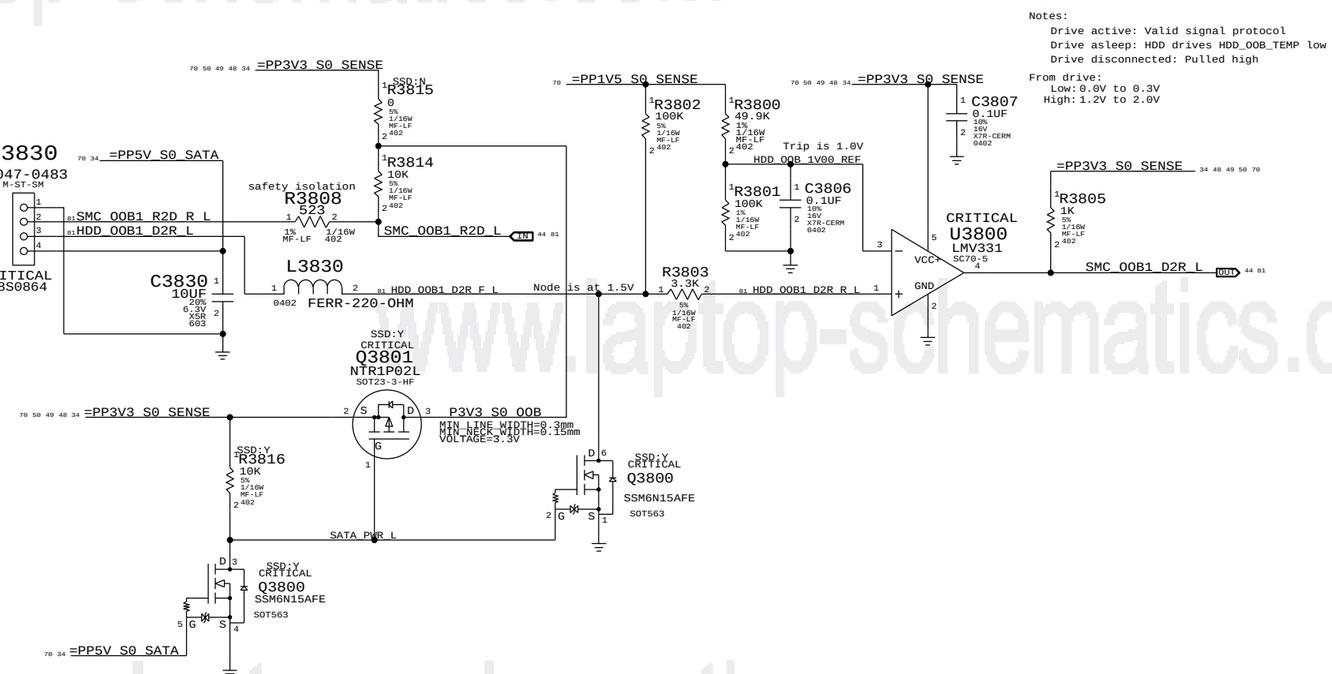
## HDD Out-of-Band Temperature Sensing

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SYNC_MASTER=J16_JERRY SYNC_DATE=01/07/2013

PAGE TITLE: HDD Connector

Apple Inc.

DRAWING NUMBER: 051-0164 SIZE: D

REVISION: 12.4.0

BRANCH:

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

70 36 35 =PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
36 =PP3V3R1V8_CR_VDDIO

ENET_SR_LX 36
=ENET_SR_VFB 36
Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY 36
396mA (1000base-T, Caesar II)

CRITICAL L3900 FERR-600-OHM-300MA-0.85OHM 0402
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C3900 0.1UF 10% 16V X5R-CERM 0201
ENET_XTALVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

CRITICAL L3905 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_ENET_PHY_BIASVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_ENET_PHY_AVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3920 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_AVDDL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3925 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_PCIEPLL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_GPHYPLL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.15 mm VOLTAGE=1.2V
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM1 402
C3916 0.1UF 10% 16V X5R-CERM 0201

AVDDH BIASVDDH XTALVDDH VDDO SR_VDD SR_VDDP SR_LX SR_VFB AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

70 =PP3V3_S0_ENET
R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

C3950 0.1UF 10% 16V X5R-CERM 0201
C3951 0.1UF 10% 16V X5R-CERM 0201
C3955 0.1UF 10% 16V X5R-CERM 0201
C3956 0.1UF 10% 16V X5R-CERM 0201

77 13 OUT PCIE_ENET_D2R_N
77 13 OUT PCIE_ENET_D2R_P
77 13 IN PCIE_ENET_R2D_C_P
77 13 IN PCIE_ENET_R2D_C_N
36 OUT =ENET_WAKE_L (See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT
77 PCIE_ENET_D2R_C_N
77 PCIE_ENET_D2R_C_P
77 PCIE_ENET_R2D_P
77 PCIE_ENET_R2D_N
77 11 IN PCIE_CLK100M_ENET_P
77 11 IN PCIE_CLK100M_ENET_N
37 IN ENET_RESET_L
18 11 OUT ENET_CLKREQ_L
OUT ENET_WAKE*
37 20 IN ENET_LOW_PWR
SMB_ENET_SCL
SMB_ENET_SDA
80 35 BI ENET_SCLK
80 35 IN ENET_MISO
80 35 BI ENET_MOSI
80 35 BI ENET_CS_L
36 OUT ENET_TRAFFICLED_L
79 19 IN SYSCLK_CLK25M_ENET
80 ENET_RDAC

OMIT_TABLE
U3900 BCM57766C0KMLG QFN-8X8

58 VMAIN_PRSNT (IPD-ENET)
27 PCIE_TXD_N
28 PCIE_TXD_P
33 PCIE_RXD_P
34 PCIE_RXD_N
31 PCIE_REFCLK_P
30 PCIE_REFCLK_N
11 PERST* (IPD)
12 CLKREQ* (OD)
3 WAKE* (OD)
4 LOW_PWR (IPD)
6 SMB_CLK
10 SMB_DATA (IPD-ENETM)
66 SCLK_SPD1000LED*
64 SI/EEDATA
65 SO_LINKLED*
63 CS*/EECLK (IPU)
2 SPD100LED*/SERIAL_DO (OD)
67 TRAFFICLED*/SERIAL_DI (OD)
18 XTALI
19 XTALO
38 RDAC
69 THRM_PAD

R3965 1.24K 1% 1/16W MF-LF 402

TRD0_P 40 ENETCONN_MDI_P<0>
TRD0_N 41 ENETCONN_MDI_N<0>
TRD1_P 44 ENETCONN_MDI_P<1>
TRD1_N 43 ENETCONN_MDI_N<1>
TRD2_P 46 ENETCONN_MDI_P<2>
TRD2_N 47 ENETCONN_MDI_N<2>
TRD3_P 50 ENETCONN_MDI_P<3>
TRD3_N 49 ENETCONN_MDI_N<3>
84 36 80

PP3V3R1V8_ENET_LR_OUT 36
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.15 mm VOLTAGE=3.3V

(IPD) GPIO_0/CR_ACT_LED* 5 NC
GPIO_1/LR_OUT 8
GPIO_2/MEDIA_SENSE 9 ENET_MEDIA_SENSE OUT 11 80

NOTE: "IPx" == Programmable pull-up/down
(IPx-ENET) SD_DETECT 1 ENET_SD_DETECT_L IN 37 80
SD_DETECT can only be used active low due to errata.

(IPU-ENET)
CR_CMD 26 80 ENET_SD_CMD R3961 33 1% 1/20W MF 201 SDCONN_CMD IN 37 80
CR_CLK 21 80 ENET_SD_CLK R3979 33 1% 1/20W MF 201 SDCONN_CLK OUT 37 80
CR_DATA0 25 80 ENET_CR_DATA<0> R3971 33 1% 1/20W MF 201 SDCONN_DATA<0> BI 37 80
CR_DATA1 24 80 ENET_CR_DATA<1> R3972 33 1% 1/20W MF 201 SDCONN_DATA<1> BI 37 80
CR_DATA2 23 80 ENET_CR_DATA<2> R3973 33 1% 1/20W MF 201 SDCONN_DATA<2> BI 37 80
CR_DATA3 22 80 ENET_CR_DATA<3> R3974 33 1% 1/20W MF 201 SDCONN_DATA<3> BI 37 80
CR_DATA4 52 80 ENET_CR_DATA<4> R3975 33 1% 1/20W MF 201 SDCONN_DATA<4> BI 37 80
CR_DATA5 53 80 ENET_CR_DATA<5> R3976 33 1% 1/20W MF 201 SDCONN_DATA<5> BI 37 80
CR_DATA6 54 80 ENET_CR_DATA<6> R3977 33 1% 1/20W MF 201 SDCONN_DATA<6> BI 37 80
CR_DATA7 55 80 ENET_CR_DATA<7> R3978 33 1% 1/20W MF 201 SDCONN_DATA<7> BI 37 80

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

(IPU-ENET) MS_INS* 59 NC
(IPU-ENET) CR_LED*/CR_BUS_PWR 60 ENET_CR_PWREN OUT 37
(IPU-ENET) CR_WP* 57 SDCONN_WP IN 37
(NO IPU OR IPD-ENET) SR_DISABLE 68 ENET_SR_DISABLE R3981 1K 5% 1/16W MF-LF 402

(See note)
ENET 1.2V SR IS ENABLED IF FLOATING.

ENET supports both active-levels for WP.

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE
If ENET switching regulator is used, this pin should have a 1K pull-down to GND

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900

## PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup. (Required ROM size 1 Mbit)

70 36 35 =PP3V3_ENET_PHY
C3990 0.1UF 10% 16V X5R-CERM 0201
U3990 AT45DB011D SOIC-8S1 OMIT_TABLE
VCC SCK CS* WP* RESET* SI SO GND
80 35 IN ENET_SCLK
80 35 IN ENET_CS_L
ENET_MOSI IN 35 80
ENET_MISO OUT 35 80
NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=J16_MAX SYNC_DATE=02/11/2013
PAGE TITLE: ETHERNET PHY (CAESAR IV)
Apple Inc.
DRAWING NUMBER 051-0164 SIZE D
REVISION 12.4.0
BRANCH
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## CAESAR IV 1.2V INT.VR CMPTS

Power decoupling

C4010 4.7UF 20% 6.3V X5R-CERM1 402
C4011 0.1UF 10% 16V X7R-CERM 0402

=PP3V3_ENET_PHY

CRITICAL
L4010 4.7UH-0.8A PCAA031B-SM

ENET_SR_LX
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
SWITCH_NODE=TRUE
DIDT=TRUE

C4012 10UF 20% 6.3V X5R 603
C4013 0.1UF 10% 16V X7R-CERM 0402

PP1V2_ENET_INTREG
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V

Feedback loop

PP1V2_ENET_INTREG
MAKE_BASE=TRUE
=PP1V2_ENET_PHY
=ENET_SR_VFB

## ENET Enable Generation

"ENET" = "S0" || ("S4" && "WOL_EN")

=PP3V3_S4_FET_ENET

R4020 10K 5% 1/16W MF-LF 402

CRITICAL
Q4021 2N7002DW-X-G SOT-363

WOL_EN
PM_SLP_S3_L

CRITICAL
Q4021 2N7002DW-X-G SOT-363

PM_EN_ENET_L

R4021 100K 5% 1/16W MF-LF 402

C4020 0.033UF 10% 16V X5R 402

## 3.3V ENET FET

CRITICAL
Q4020 NTR4101P SOT-23-HF

P3V3ENET_SS

C4021 0.01UF 10% 50V X7R-CERM 0402

PP3V3_ENET_FET

## CAESAR IV ACTIVITY LED

=PP3V3_ENET_PHY

DEVELOPMENT
R4050 330 5% 1/16W MF-LF 402

ENET_ACT

DEVELOPMENT
LED4050 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:ENET ACT

ENET_TRAFFICLED_L

## CAESAR IV WAKE# ISOLATION

=PP3V3_ENET_PHY

Q4070 SSM3K15AMFVAPE VESM

R4070 10K 5% 1/16W MF-LF 402

PCIE_WAKE_L

ENET_WAKE_L
MAKE_BASE=TRUE

=ENET_WAKE_L

PP3V3R1V8_ENET_LR_OUT
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.15 mm

=PP3V3R1V8_CR_VDDIO

C4030 4.7UF 20% 6.3V X5R-CERM1 402
C4031 0.1UF 10% 16V X5R-CERM 0201
C4032 0.1UF 10% 16V X5R-CERM 0201

157S0058
CRITICAL
T4000 SM

ENETCONN_MDI_P<1>
ENETCONN_MDI_N<1>
ENETCONN_MDI_P<3>
ENETCONN_MDI_N<3>
ENETCONN_MDI_T_P<1>
ENETCONN_MDI_T_N<1>
ENETCONN_MDI_T_N<3>
ENETCONN_MDI_T_P<3>

TX →
LFE8904CF
← RX

ENETCONN_MCT1
ENETCONN_MCT3

CRITICAL
T4010 SM

ENETCONN_MDI_N<2>
ENETCONN_MDI_P<2>
ENETCONN_MDI_N<0>
ENETCONN_MDI_P<0>
ENETCONN_MDI_T_N<2>
ENETCONN_MDI_T_P<2>
ENETCONN_MDI_T_N<0>
ENETCONN_MDI_T_P<0>

TX →
LFE8904CF
← RX

ENETCONN_MCT2
ENETCONN_MCT0

ENETCONN_TCT

C4001 0.1UF 20% 10V CERM 402
C4002 0.1UF 20% 10V CERM 402
C4003 0.1UF 20% 10V CERM 402
C4004 0.1UF 20% 10V CERM 402

R4000 75 5% 1/16W MF-LF 402
R4001 75 5% 1/16W MF-LF 402
R4002 75 5% 1/16W MF-LF 402
R4003 75 5% 1/16W MF-LF 402

ENETCONN_MCT_BS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm

NOSTUFF
C4000 1000PF 10% 2KV CERM 1206

514-0822
CRITICAL
J4000 K70-K72 F-ANG-TH

ENET_MDI
ENET_MDI_TRAN3-
ENET_MDI_TRAN3+
ENET_MDI_TRAN1-
ENET_MDI_TRAN2-
ENET_MDI_TRAN2+
ENET_MDI_TRAN1+
ENET_MDI_TRAN0-
ENET_MDI_TRAN0+

SHIELD PINS

SYNC_MASTER=J16_MAX SYNC_DATE=02/11/2013

PAGE TITLE
Ethernet Support & Connector

Apple Inc.

DRAWING NUMBER 051-0164
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REVISION 12.4.0
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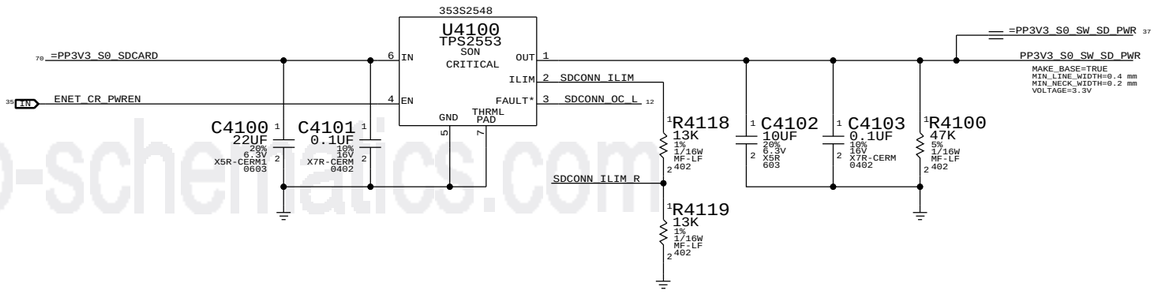
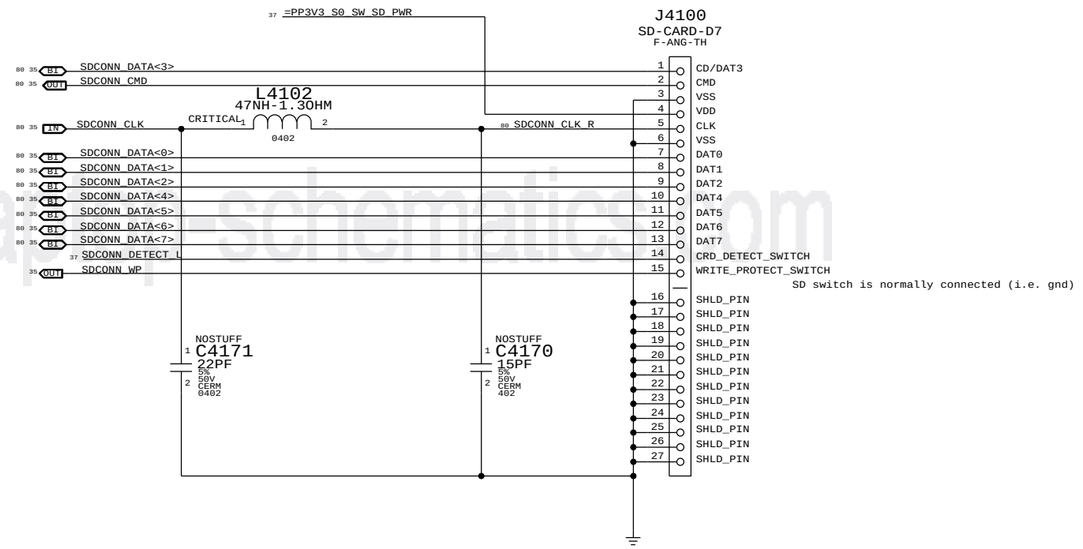
# SD CARD 3.3V OVERCURRENT PROTECTION CHIP



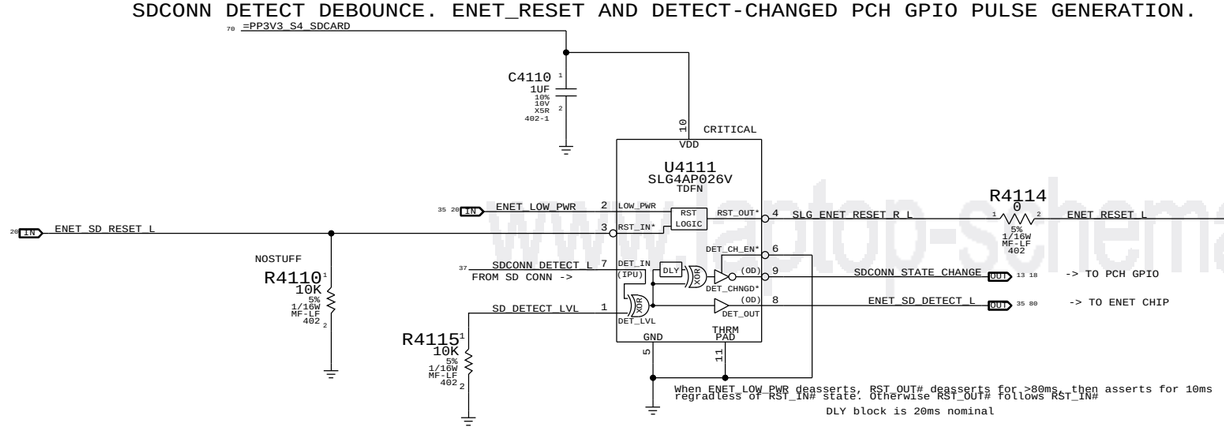

J16:516-0249 / J17:512-0038

## SD CARD CONNECTOR

J4100
SD-CARD-D7
F-ANG-TH




## SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.

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SYNC_MASTER=J16 MAX SYNC_DATE=02/11/2013

PAGE TITLE
**SD READER CONNECTOR**

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DRAWING NUMBER 051-0164 SIZE D
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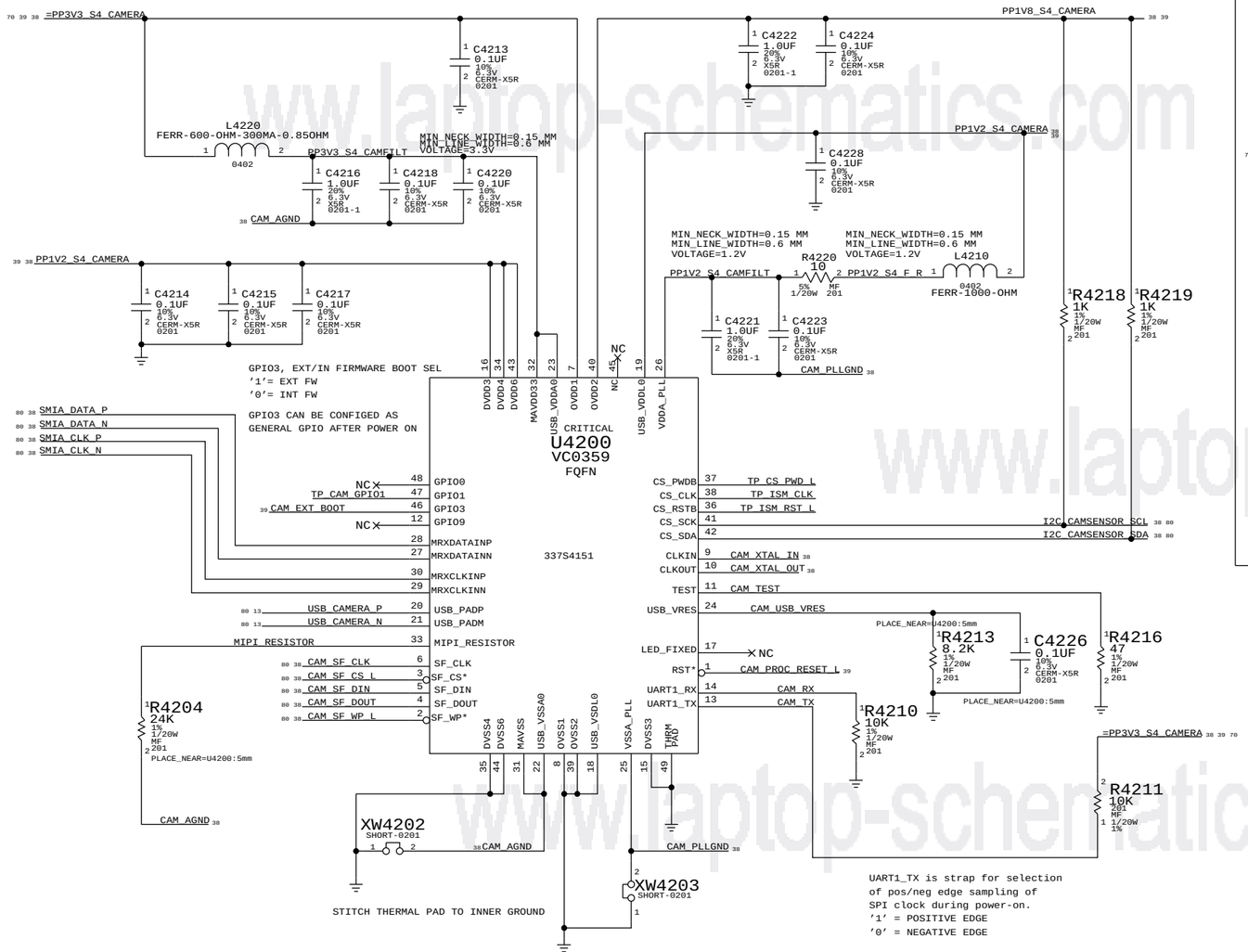
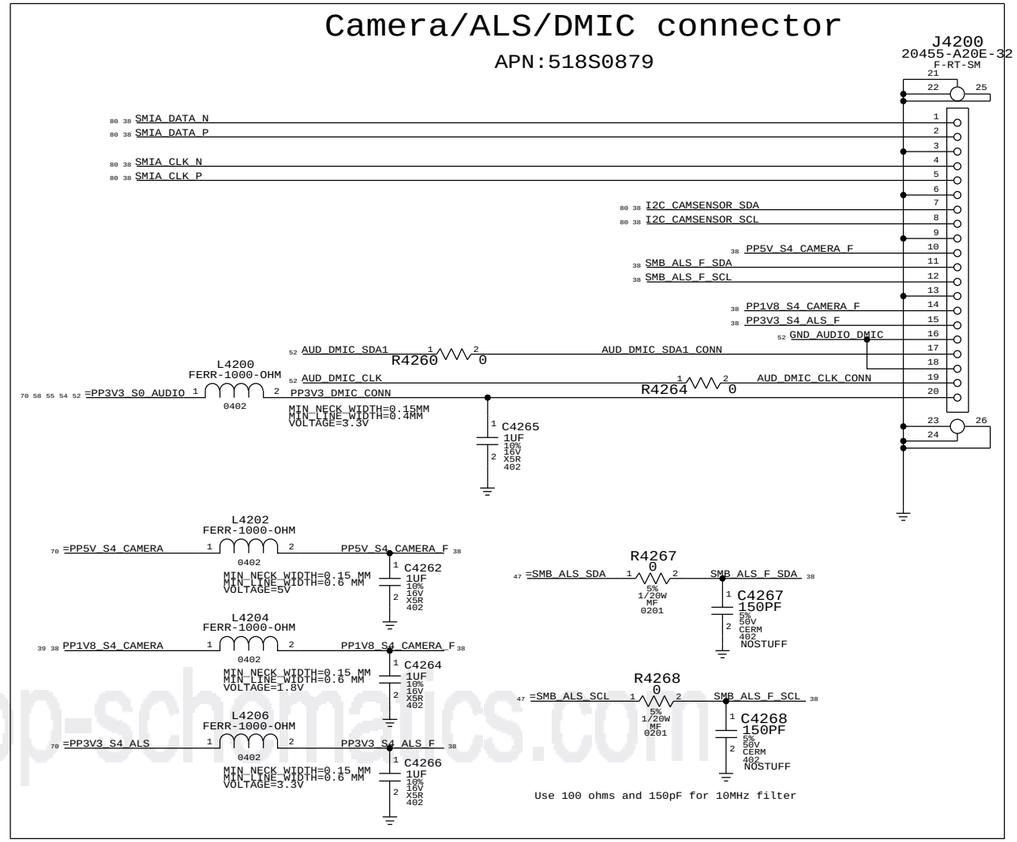
# USB CAMERA CONTROLLER

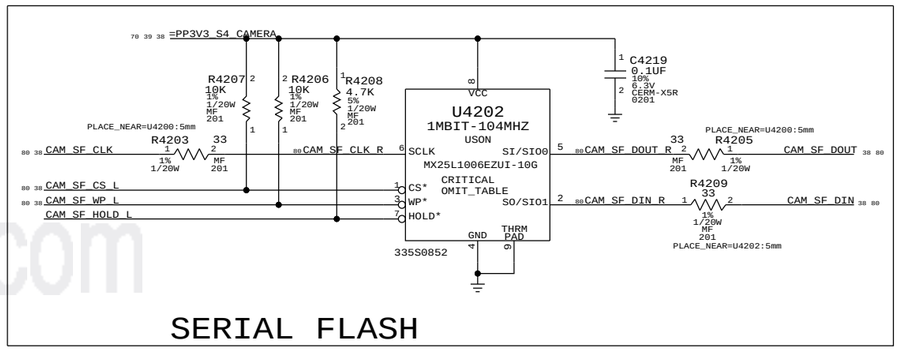



## Camera/ALS/DMIC connector

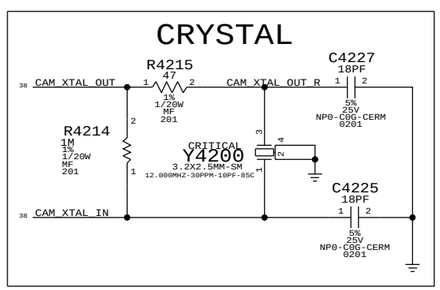
APN:518S0879




## SERIAL FLASH




## CRYSTAL




| | |
|---|---|
| SYNC_MASTER=J16_MAX | SYNC_DATE=02/11/2013 |
| PAGE TITLE | Camera Controller |
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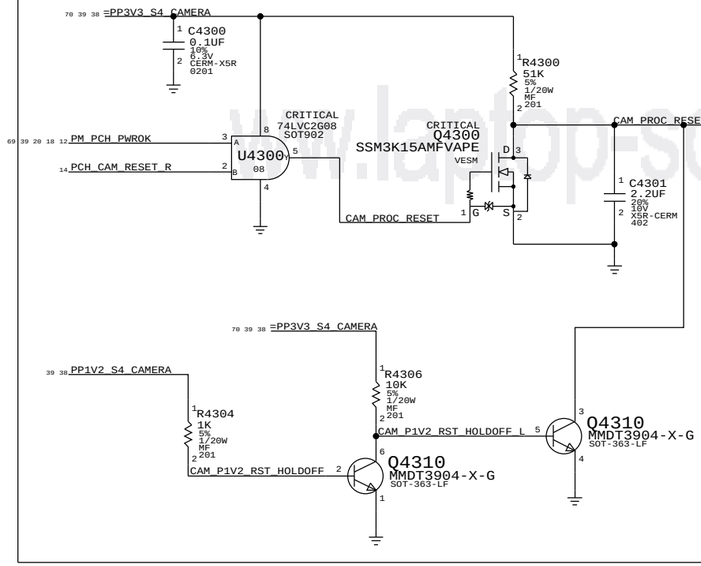
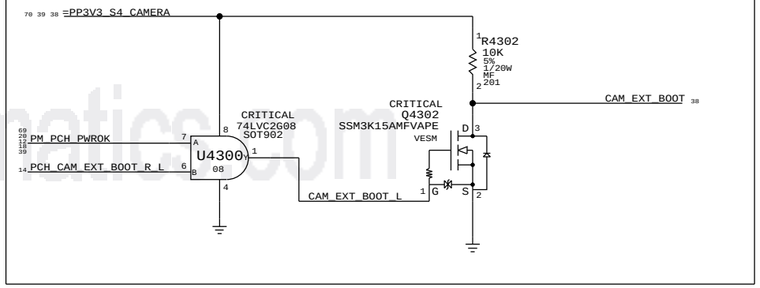
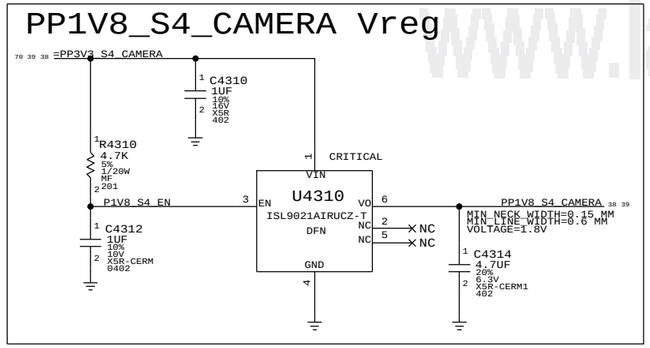
## Camera Processor Reset



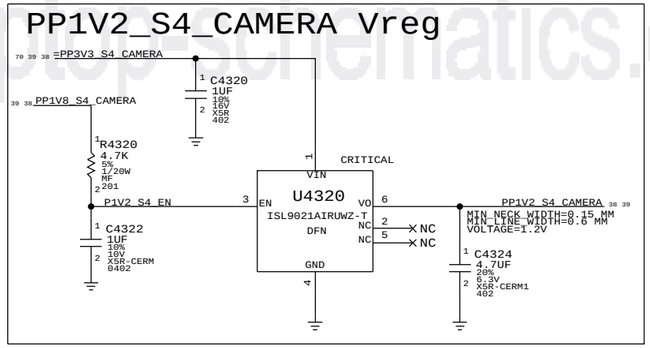

## Camera Processor ExtBoot Cntl




## PP1V8_S4_CAMERA Vreg




## PP1V2_S4_CAMERA Vreg

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SYNC_MASTER=J16_MAX SYNC_DATE=02/11/2013

PAGE TITLE
# Camera Controller Support

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## Internal DP Connector

518S0829

CRITICAL

J4400
20525-130E-01
F-RT-SM

=PP12V_S0_LCD → F4400 3AMP-32V-467 (603-HF) → PP12V_LCD_F → L4400 FERR-220-OHM (0805) → PP12V_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm

C4420 10UF 10% 16V X5R-CERM 0805
C4401 0.001UF 20% 50V CERM 0402

| | | | |
|---|---|---|---|
| Display TCon Master | 81 47 | BI | SMB_DP_TCON_SDA |
| | 81 47 | OUT | SMB_DP_TCON_SCL |
| Display TCon Slave | 47 | BI | SMB_DP_TCON_SLA_SDA |
| | 47 | IN | SMB_DP_TCON_SLA_SCL |
| | 85 52 | OUT | DP_INT_SPDIF_AUDIO |
| | 43 | OUT | DP_INTPNL_HPD |
| | 85 41 | BI | DP_INTPNL_AUX_N |
| | 85 41 | BI | DP_INTPNL_AUX_P |
| | 85 41 | IN | DP_INTPNL_ML_P<0> |
| | 85 41 | IN | DP_INTPNL_ML_N<0> |
| | 85 41 | IN | DP_INTPNL_ML_P<1> |
| | 85 41 | IN | DP_INTPNL_ML_N<1> |
| | 40 | | VIDEO_ON |
| | 66 | OUT | BKLT_VSYNC |

## Backlight Control

Delay applies only on a L->H transition on VIDEO_ON. This guarantees video is valid before the backlight is enabled.
On a H->L transition, output follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video

70 47 31 =PP3V3_S0_DP

C4450 0.1UF 10% 6.3V CERM-X5R 0201
C4451 10UF 20% 6.3V CERM-X5R 0402-1

U4450 74AUP2G14GM SOT886
D4450 SOD-523 BAT54XV2T1
U4450 74AUP2G14GM SOT886

40 VIDEO_ON → R4451 100K 5% 1/20W MF 201 → U4450 pin 1
U4450 pin 6 → D4450 A
D4450 K → VIDEO_ON_L_DLY → U4450 pin 3
D4450 K → R4450 30.1K 1% 1/20W MF 201 → VIDEO_ON_L (OUT 3) To Diag LED
U4450 pin 4 → BKLT_EN (OUT 66) To BLC

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## TP to DP aliases

26 IN TP_DP_TBTSRC_ML_CP<0> — DP_TBTSRC_ML_P<0> 41 85 MAKE_BASE=TRUE
26 IN TP_DP_TBTSRC_ML_CN<0> — DP_TBTSRC_ML_N<0> 41 85 MAKE_BASE=TRUE

26 IN TP_DP_TBTSRC_ML_CP<1> — DP_TBTSRC_ML_P<1> 41 85 MAKE_BASE=TRUE
26 IN TP_DP_TBTSRC_ML_CN<1> — DP_TBTSRC_ML_N<1> 41 85 MAKE_BASE=TRUE

26 BI TP_DP_TBTSRC_AUXCH_CP — DP_TBTSRC_AUXCH_P 41 85 MAKE_BASE=TRUE
26 BI TP_DP_TBTSRC_AUXCH_CN — DP_TBTSRC_AUXCH_N 41 85 MAKE_BASE=TRUE

## NC aliases

26 IN TP_DP_TBTSRC_ML_CP<2> — NC_DP_TBTSRC_ML_P<2> NO_TEST=TRUE MAKE_BASE=TRUE
26 IN TP_DP_TBTSRC_ML_CN<2> — NC_DP_TBTSRC_ML_N<2> NO_TEST=TRUE MAKE_BASE=TRUE

26 IN TP_DP_TBTSRC_ML_CP<3> — NC_DP_TBTSRC_ML_P<3> NO_TEST=TRUE MAKE_BASE=TRUE
26 IN TP_DP_TBTSRC_ML_CN<3> — NC_DP_TBTSRC_ML_N<3> NO_TEST=TRUE MAKE_BASE=TRUE

73 IN DP_INT_ML_P<2> — NC_DP_INT_ML_P<2> NO_TEST=TRUE MAKE_BASE=TRUE
73 IN DP_INT_ML_N<2> — NC_DP_INT_ML_N<2> NO_TEST=TRUE MAKE_BASE=TRUE

73 IN DP_INT_ML_P<3> — NC_DP_INT_ML_P<3> NO_TEST=TRUE MAKE_BASE=TRUE
73 IN DP_INT_ML_N<3> — NC_DP_INT_ML_N<3> NO_TEST=TRUE MAKE_BASE=TRUE

71 41 DP_INT_HPD
R4500 100K 5% 1/20W MF 201

=PP3V3_S0_INTDPMUX 41 70
C4568 0.1UF 10% 6.3V CERM-X5R 0201
C4569 0.1UF 10% 6.3V CERM-X5R 0201

U4500 PI3VEDP212 TQFN CRITICAL

| | | | |
|---|---|---|---|
| 85 71 IN | DP_INT_ML_P<0> | 31 | D0+A |
| 85 71 IN | DP_INT_ML_N<0> | 30 | D0-A |
| 85 71 IN | DP_INT_ML_P<1> | 27 | D1+A |
| 85 71 IN | DP_INT_ML_N<1> | 26 | D1-A |
| 85 BI | DP_INT_AUX_C_P | 19 | AUX+A |
| 85 BI | DP_INT_AUX_C_N | 18 | AUX-A |
| 71 41 OUT | DP_INT_HPD | 17 | HPD_A |
| 85 41 | DP_TBTSRC_ML_C_P<0> | 25 | D0+B |
| 85 41 | DP_TBTSRC_ML_C_N<0> | 24 | D0-B |
| 85 41 | DP_TBTSRC_ML_C_P<1> | 23 | D1+B |
| 85 41 | DP_TBTSRC_ML_C_N<1> | 22 | D1-B |
| 85 BI | DP_TBTSRC_AUX_C_P | 15 | AUX+B |
| 85 BI | DP_TBTSRC_AUX_C_N | 14 | AUX-B |
| 26 OUT | DP_TBTSRC_HPD | 13 | HPD_B |
| 58 11 IN | DP_TBT_SEL | 10 | SEL |
| | | 32 | AUX_SEL |
| | | 11 | HPD_SEL |

VDD: 29 20 16 12 9 6
THMPAD_GND: 33 28 21

PD is on the CR page

C4508 0.1UF 20% 6.3V X5R 0201
C4509 0.1UF 20% 6.3V X5R 0201
C4510 0.1UF 20% 6.3V X5R 0201
C4511 0.1UF 20% 6.3V X5R 0201

| | | | |
|---|---|---|---|
| D0+ | 1 85 | DP_INTPNL_ML_C_P<0> | DP_INTPNL_ML_P<0> OUT 40 85 |
| D0- | 2 85 | DP_INTPNL_ML_C_N<0> | DP_INTPNL_ML_N<0> OUT 40 85 |
| D1+ | 4 85 | DP_INTPNL_ML_C_P<1> | DP_INTPNL_ML_P<1> OUT 40 85 |
| D1- | 5 85 | DP_INTPNL_ML_C_N<1> | DP_INTPNL_ML_N<1> OUT 40 85 |
| AUX+ | 6 | DP_INTPNL_AUX_P | BI 40 85 |
| AUX- | 7 | DP_INTPNL_AUX_N | BI 40 85 |
| HPD | 8 | DP_INTPNL_HPD | IN 40 |

C4500 0.15UF 20% 6.3V X5R 0201
C4501 0.15UF 20% 6.3V X5R 0201
C4502 0.15UF 20% 6.3V X5R 0201
C4503 0.15UF 20% 6.3V X5R 0201

R4502 100K 5% 1/20W MF 201
R4503 100K 5% 1/20W MF 201
=PP3V3_S0_INTDPMUX 41 70

70 41 =PP3V3_S0_INTDPMUX
R4504 2.2K 1% 1/20W MF 201
R4505 2.2K 1% 1/20W MF 201

DP_INT_DDC_DATA BI 71
DP_INT_DDC_CLK IN 71

85 71 BI DP_INT_AUX_P
85 71 BI DP_INT_AUX_N

85 41 BI DP_TBTSRC_AUXCH_P
85 41 BI DP_TBTSRC_AUXCH_N

85 41 IN DP_TBTSRC_ML_P<0> — C4512 0.22UF 20% 6.3V X5R 0201 — DP_TBTSRC_ML_C_P<0> 41 85
85 41 IN DP_TBTSRC_ML_N<0> — C4513 0.22UF 20% 6.3V X5R 0201 — DP_TBTSRC_ML_C_N<0> 41 85
85 41 IN DP_TBTSRC_ML_P<1> — C4514 0.22UF 20% 6.3V X5R 0201 — DP_TBTSRC_ML_C_P<1> 41 85
85 41 IN DP_TBTSRC_ML_N<1> — C4515 0.22UF 20% 6.3V X5R 0201 — DP_TBTSRC_ML_C_N<1> 41 85

R4512 2.7K 5% 1/20W MF 201
R4513 2.7K 5% 1/20W MF 201
R4514 2.7K 5% 1/20W MF 201
R4515 2.7K 5% 1/20W MF 201

SYNC_MASTER=J16_MAX SYNC_DATE=02/11/2013

PAGE TITLE: Internal DP MUXing

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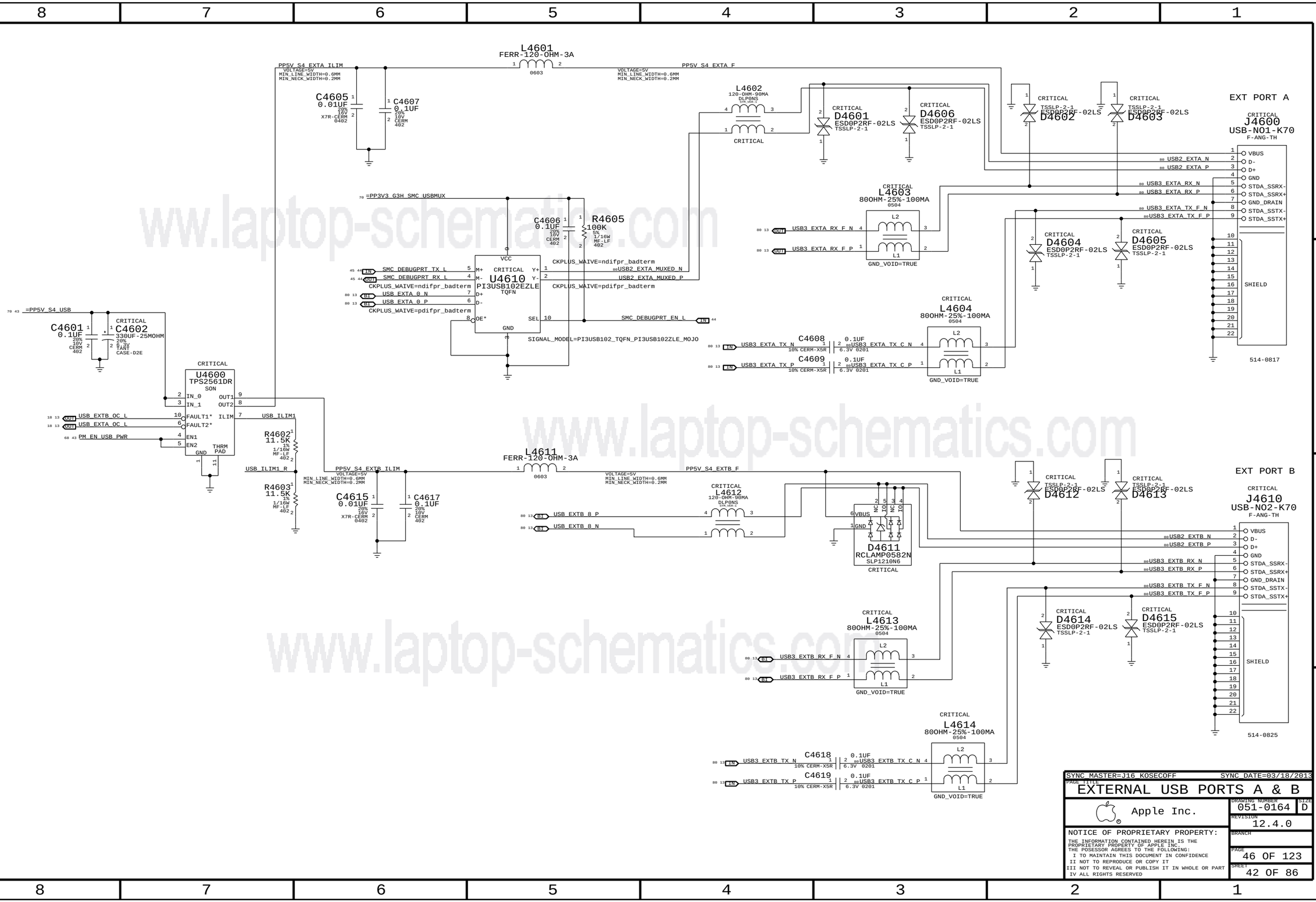


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SYNC_MASTER=J16_KOSECOFF SYNC_DATE=03/18/2013

PAGE TITLE
EXTERNAL USB PORTS A & B

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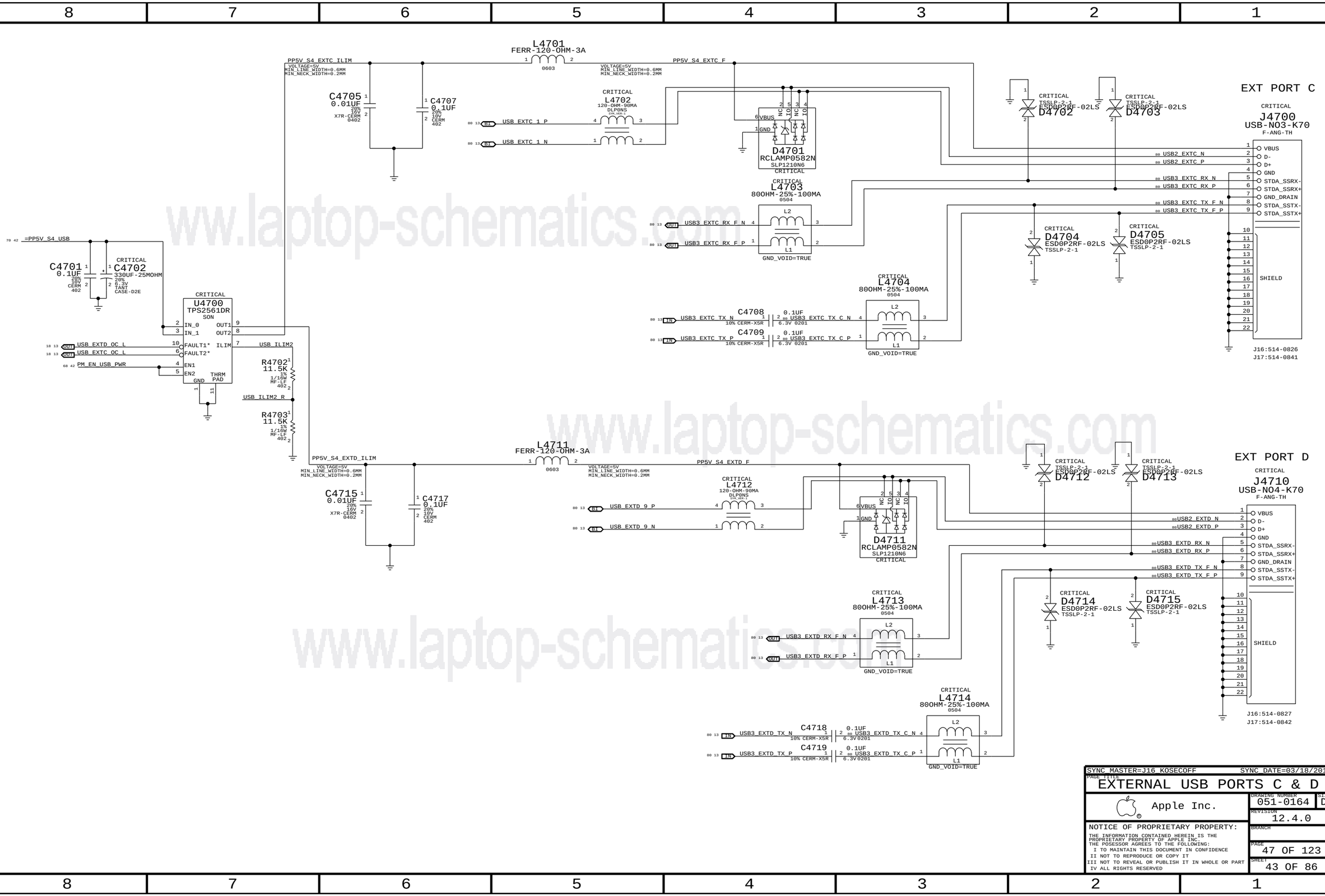


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PAGE TITLE
# EXTERNAL USB PORTS C & D

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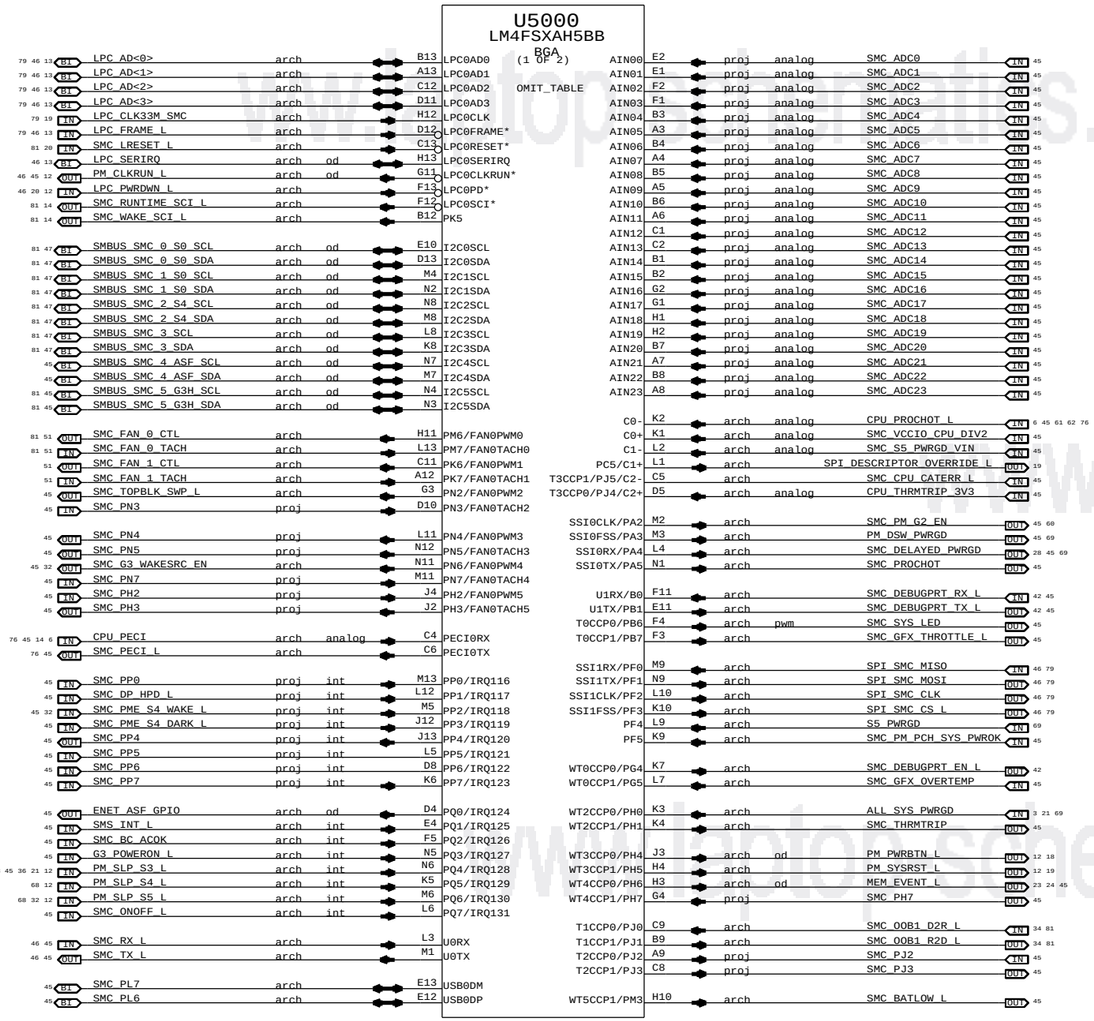
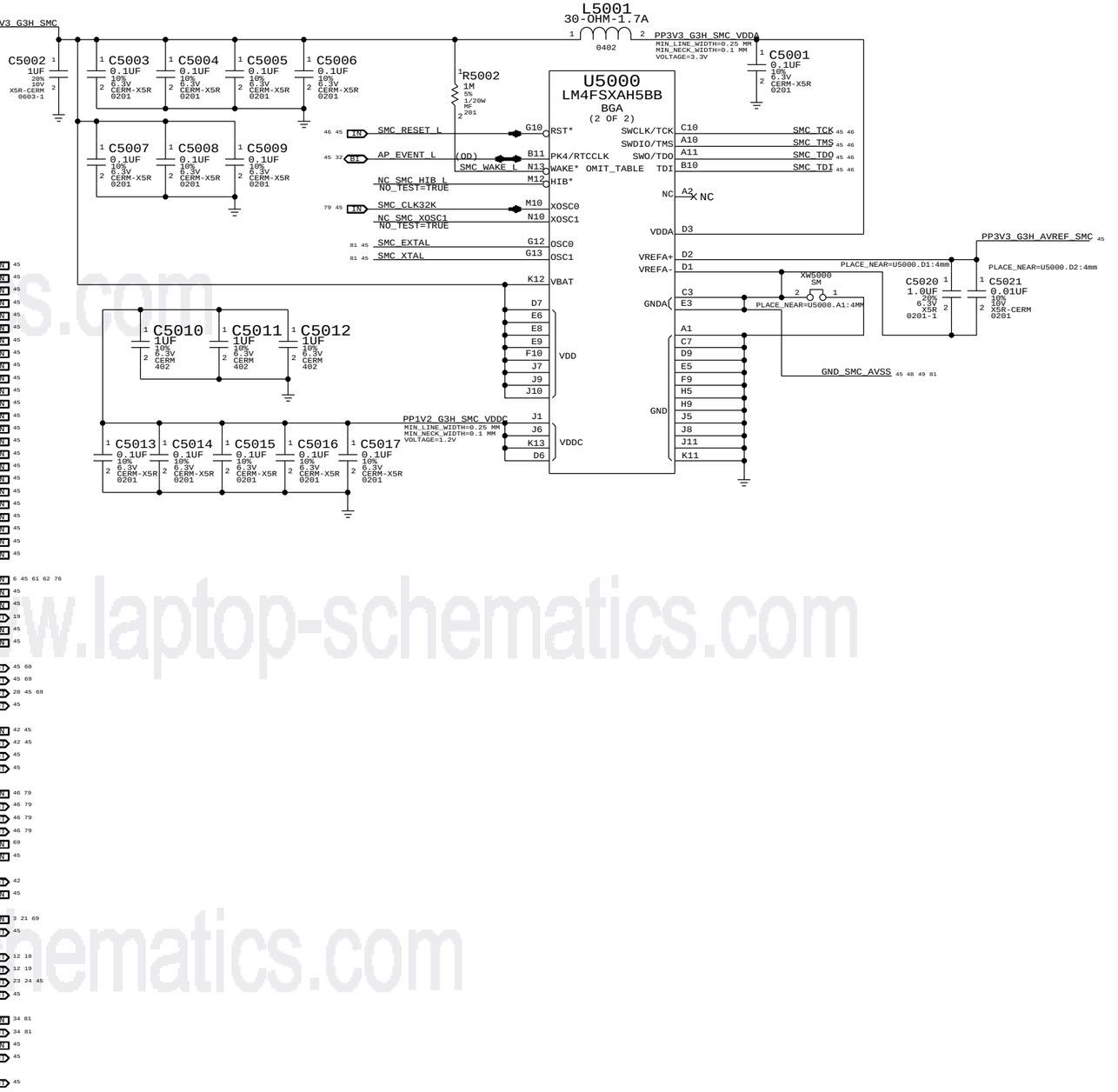
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.







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PAGE TITLE: SMC

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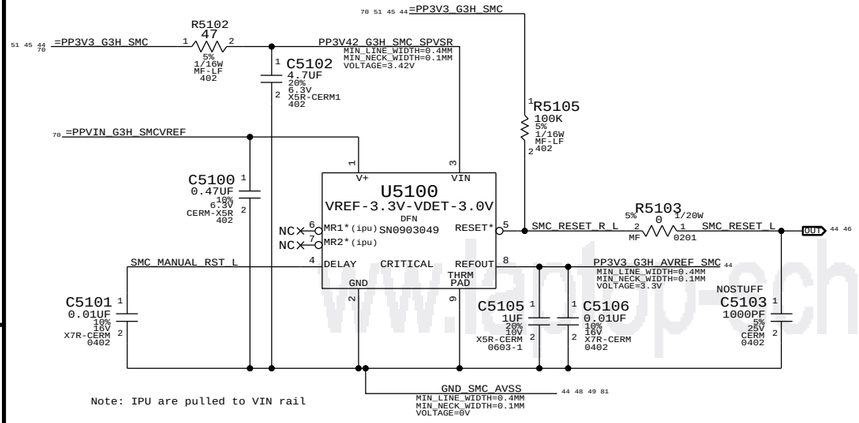
## SMC Supervisor and AVREF Supply




Note: IPU are pulled to VIN rail

## ADC Channel Aliases

| | | | |
|---|---|---|---|
| SMC_ADC0 | VSNS_P12VG3H | MAKE_BASE=TRUE | 48 81 |
| SMC_ADC1 | ISNS_P12VG3H | MAKE_BASE=TRUE | 48 81 |
| SMC_ADC4 | VSNS_PVDDQS0 | MAKE_BASE=TRUE | 49 81 |
| SMC_ADC5 | ISNS_PVDDQS0 | MAKE_BASE=TRUE | 49 81 |
| SMC_ADC6 | VSNS_VDDQS3_DDR | MAKE_BASE=TRUE | 49 81 |
| SMC_ADC7 | ISNS_VDDQS3_DDR | MAKE_BASE=TRUE | 49 81 |
| SMC_ADC10 | VSNS_CPUVCC | MAKE_BASE=TRUE | 48 81 |
| SMC_ADC11 | ISNS_CPUVCC | MAKE_BASE=TRUE | 48 81 |
| SMC_ADC14 | VSNS_HDDS0 | MAKE_BASE=TRUE | 48 81 |
| SMC_ADC15 | ISNS_HDDS0 | MAKE_BASE=TRUE | 48 81 |
| SMC_ADC17 | VSNS_P1V05S0_PCH | MAKE_BASE=TRUE | 48 81 |
| SMC_ADC19 | ISNS_P3V3S4_AP | MAKE_BASE=TRUE | 48 81 |
| SMC_ADC20 | ISNS_SSDS0 | MAKE_BASE=TRUE | 49 81 |
| SMC_ADC21 | VSNS_P3V3S5 | MAKE_BASE=TRUE | 49 81 |

## Unused ADC Channels

| | | | |
|---|---|---|---|
| SMC_PH3 | NC_SMC_PH3 | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_ADC2 | NC_VSNS_P12VS0_GPUCORE | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_ADC3 | NC_ISNS_P12VS0_GPUCORE | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_ADC8 | NC_VSNS_P12VS0_FBVDDQ | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_ADC9 | NC_ISNS_P12VS0_FBVDDQ | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_ADC12 | NC_VSNS_GPUCORE_ALT | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_ADC13 | NC_ISNS_GPUCORE_ALT | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_ADC16 | NC_SMC_ADC16 | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_ADC18 | NC_SMC_ADC18 | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_ADC22 | NC_SMC_ADC22 | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_ADC23 | NC_SMC_ADC23 | MAKE_BASE=TRUE | NO_TEST=TRUE |

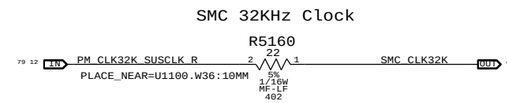
## Project-specific Aliases

| | | | |
|---|---|---|---|
| SMC_PN5 | ACDC_BURST_EN_L | MAKE_BASE=TRUE | 45 |
| SMC_PJ3 | SMC_OOB2_R2D_L | MAKE_BASE=TRUE | 33 81 |
| SMC_PJ2 | SMC_OOB2_D2R_L | MAKE_BASE=TRUE | 33 81 |
| SMC_PP0 | SMC_ACDC_ID | MAKE_BASE=TRUE | 60 |
| SMC_PH2 | SMC_ASSERT_RTCRST | MAKE_BASE=TRUE | 45 |
| SMC_PL6 | SMC_WIFI_PWR_EN | MAKE_BASE=TRUE | 45 |

## Unused Project-specific

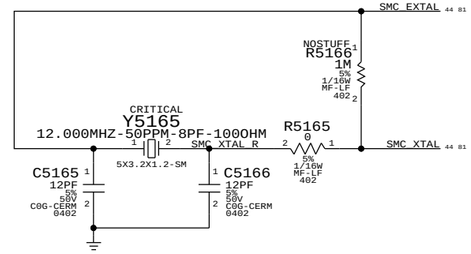
| | | | |
|---|---|---|---|
| SMC_S5_PWRGD_VIN | NC_SMC_S5_PWRGD_VIN | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_PL7 | NC_SMC_PL7 | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_PN3 | NC_SMC_PN3 | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_PN4 | NC_SMC_PN4 | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_PP4 | NC_SMC_S4_WAKESRC_EN | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_PN7 | NC_SMC_PN7 | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_PP5 | NC_SMC_PP5 | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_PP6 | NC_SMC_PP6 | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_PP7 | NC_SMC_PP7 | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_DP_HPD_L | NC_SMC_DP_HPD_L | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_PME_S4_DARK_L | NC_SMC_PME_S4_DARK_L | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_PH7 | TP_SMC_PH7 | MAKE_BASE=TRUE | NO_TEST=TRUE |
| TP for access if ZPB re-intstated | | | |
| SMBUS_SMC_4_ASF_SCL | NC_SMBUS_SMC_4_ASF_SCL | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMBUS_SMC_4_ASF_SDA | NC_SMBUS_SMC_4_ASF_SDA | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMBUS_SMC_5_G3H_SCL | NC_SMBUS_SMC_5_G3H_SCL | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMBUS_SMC_5_G3H_SDA | NC_SMBUS_SMC_5_G3H_SDA | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_BATLOW_L | NC_SMC_BATLOW_L | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_GFX_THROTTLE_L | NC_SMC_GFX_THROTTLE_L | MAKE_BASE=TRUE | NO_TEST=TRUE |
| SMC_GFX_OVERTEMP | NC_SMC_GFX_OVERTEMP | MAKE_BASE=TRUE | NO_TEST=TRUE |

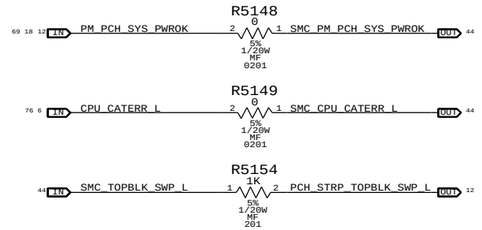
## SMC 32KHz Clock



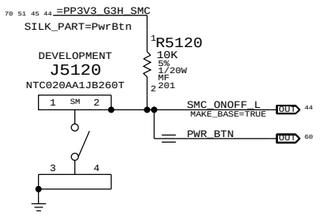

## SMC Crystal

NOTE: SMC team wants 12MHz for this Xtal



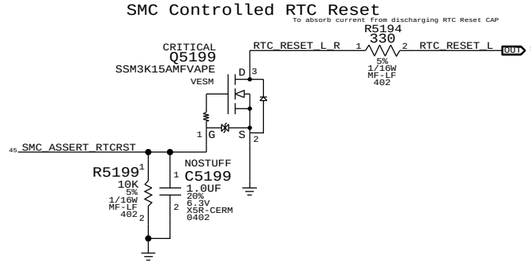




## Power Button

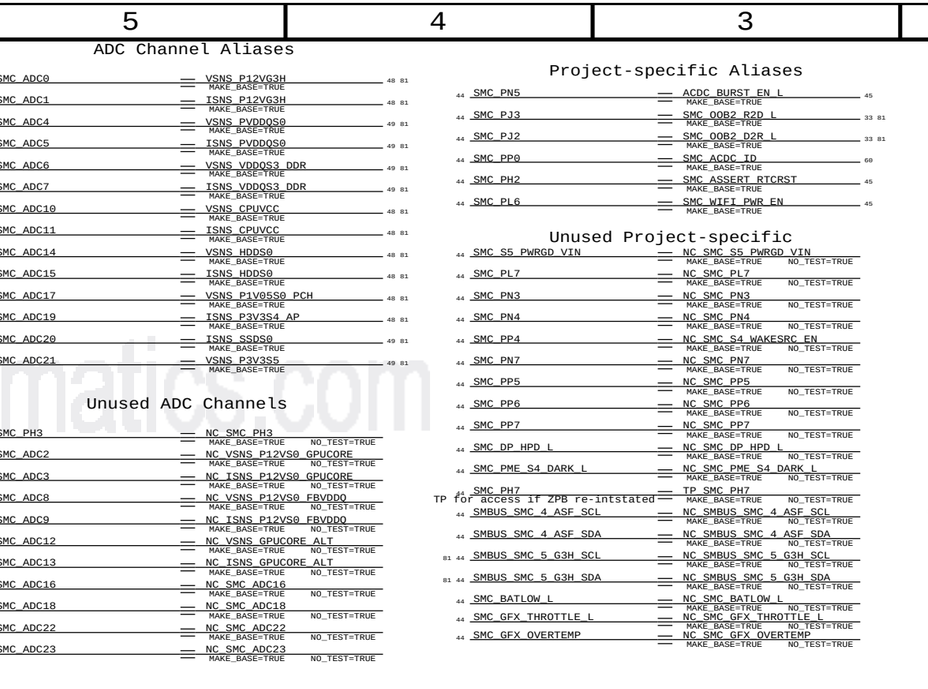



## SMC Controlled RTC Reset

To absorb current from discharging RTC Reset CAP




## Platform Thermal Control

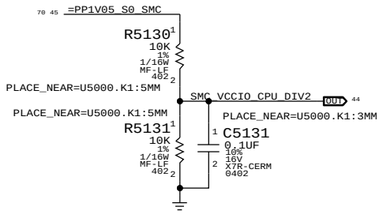



## Arch Pull Up/Down

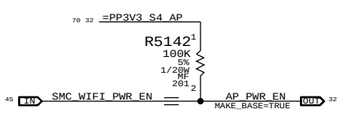
| | | | | | |
|---|---|---|---|---|---|
| | | | =PP3V3_S0_SMC | | |
| MEM_EVENT_L | R5170 | 10K | 5% | 1/20W MF | 201 |
| PM_CLKRUN_L | R5171 | 10K | 5% | 1/20W MF | 201 |
| | | | =PP3V3_G3H_SMC | | |
| ENET_ASF_GPIO | R5175 | 10K | 5% | 1/20W MF | 201 |
| G3_POWERON_L | R5176 | 10K | 5% | 1/20W MF | 201 |
| SMC_BC_ACOK | R5178 | 100K | 5% | 1/20W MF | 201 |
| SMC_SYS_LED (NOSTUFF) | R5179 | 100K | 5% | 1/20W MF | 201 |
| SMS_INT_L | R5180 | 10K | 5% | 1/20W MF | 201 |
| SMC_PME_S4_WAKE_L | R5181 | 10K | 5% | 1/20W MF | 201 |
| | | | PP3V3_S4_AP_FET | | |
| AP_EVENT_L | R5185 | 10K | 5% | 1/20W MF | 201 |
| SMC_G3_WAKESRC_EN | R5118 | 100K | 5% | 1/20W MF | 201 |
| SMC_DELAYED_PWRGD | R5186 | 100K | 5% | 1/16W MF-LF | 402 |
| PM_DSW_PWRGD | R5184 | 100K | 5% | 1/16W MF-LF | 402 |
| SMC_PM_G2_EN | R5187 | 100K | 5% | 1/20W MF | 201 |

Note:

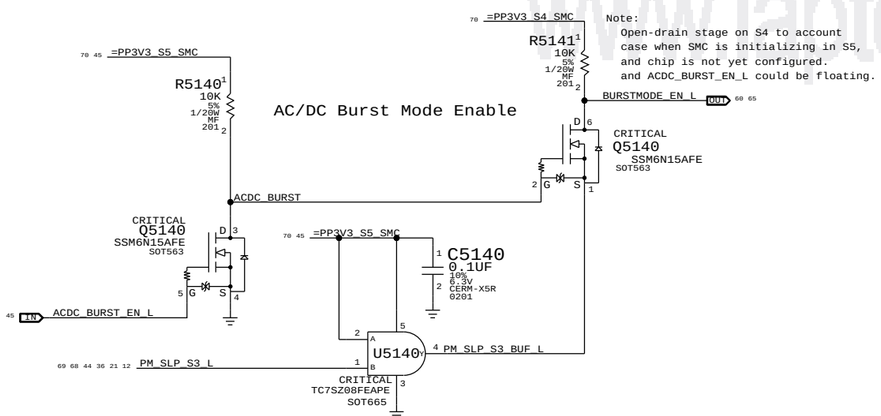
## Comparator Reference




## SMC control for AirPort power

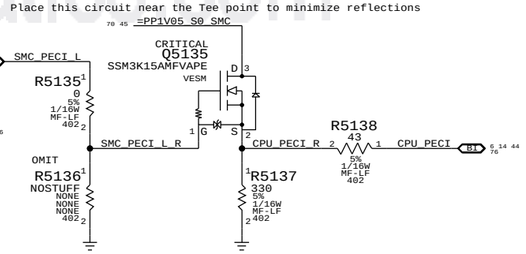



## AC/DC Burst Mode Enable



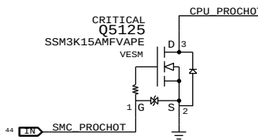

## PECI Support

Level-shifter that allows SMC to drive PECI
Place this circuit near the Tee point to minimize reflections




## PROCHOT Support

Level-shifter that allows SMC to drive PROCHOT




## Serial/JTAG Interface Pull-ups

| | | | | | |
|---|---|---|---|---|---|
| | | | =PP3V3_G3H_SMC | | |
| SMC_TX_L | R5190 | 10K | 5% | 1/20W MF | 201 |
| SMC_RX_L | R5191 | 100K | 5% | 1/20W MF | 201 |
| SMC_DEBUGPRT_TX_L | R5192 | 20K | 5% | 1/20W MF | 201 |
| SMC_DEBUGPRT_RX_L | R5193 | 20K | 5% | 1/20W MF | 201 |
| SMC_TCK | R5195 | 10K | 5% | 1/20W MF | 201 |
| SMC_TDI | R5196 | 10K | 5% | 1/20W MF | 201 |
| SMC_TDO | R5197 | 10K | 5% | 1/20W MF | 201 |
| SMC_TMS | R5198 | 10K | 5% | 1/20W MF | 201 |

SYNC_MASTER=J16_TONY SYNC_DATE=03/13/2013

PAGE TITLE: SMC Support

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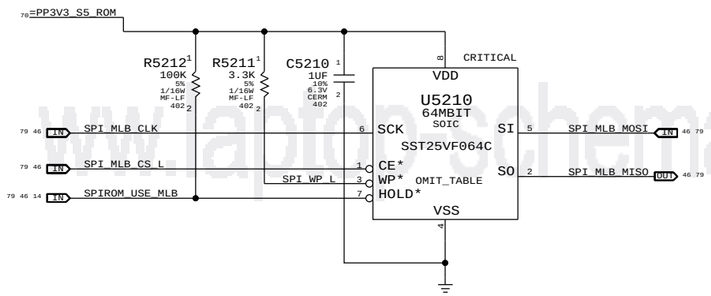
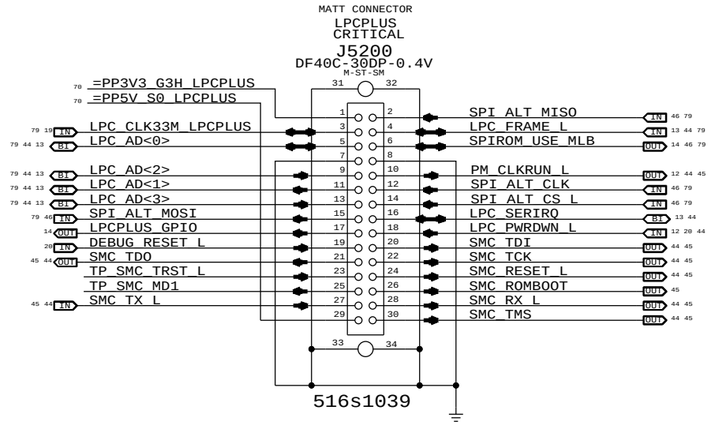
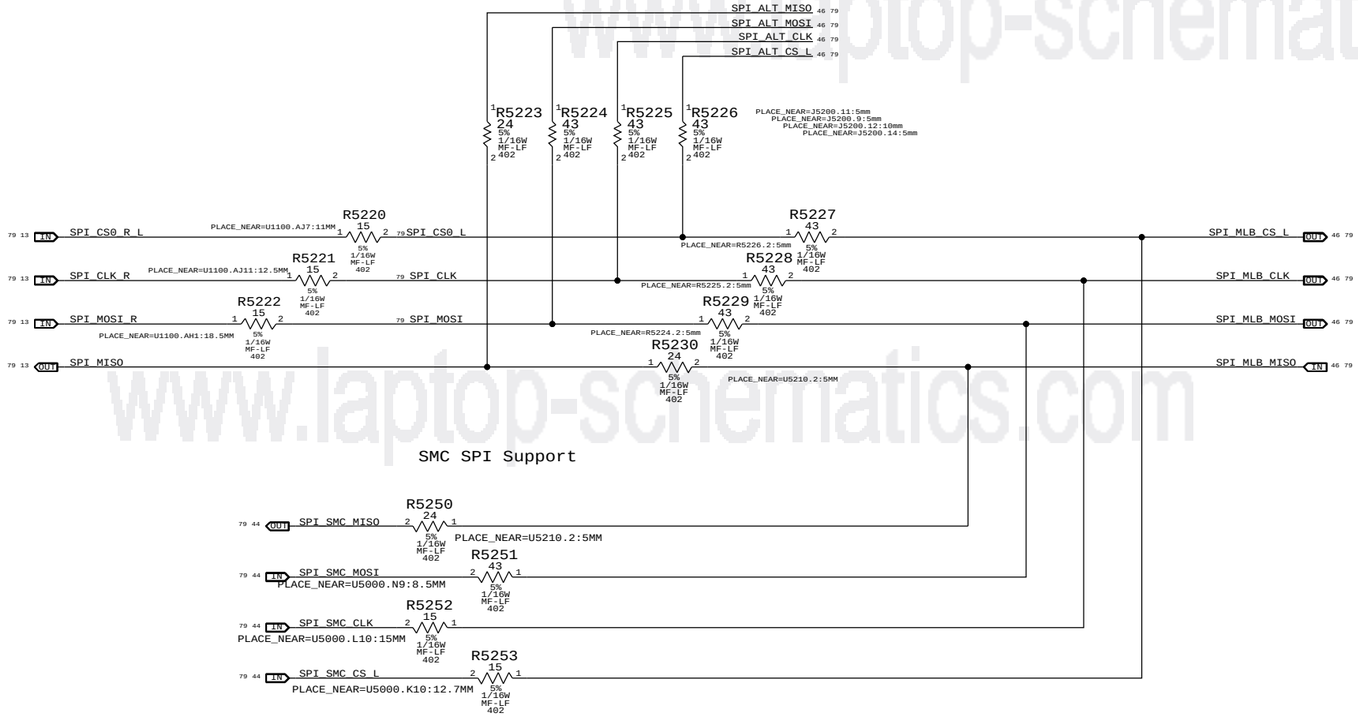
## SPI BootROM




## LPC+SPI Connector




## SPI Series Termination




## SMC SPI Support

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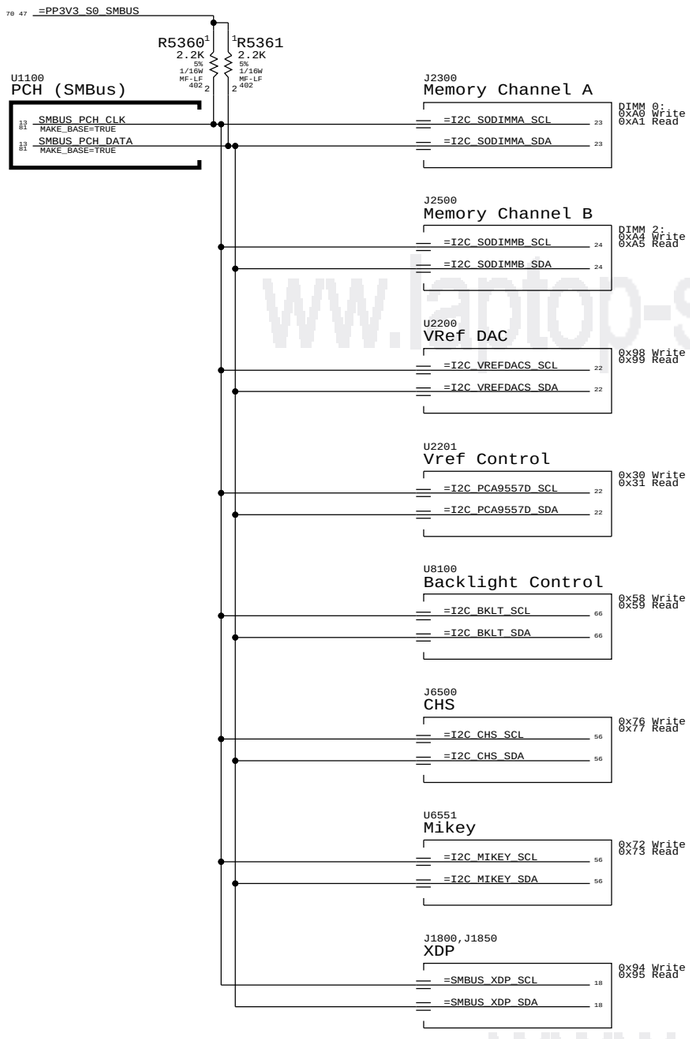
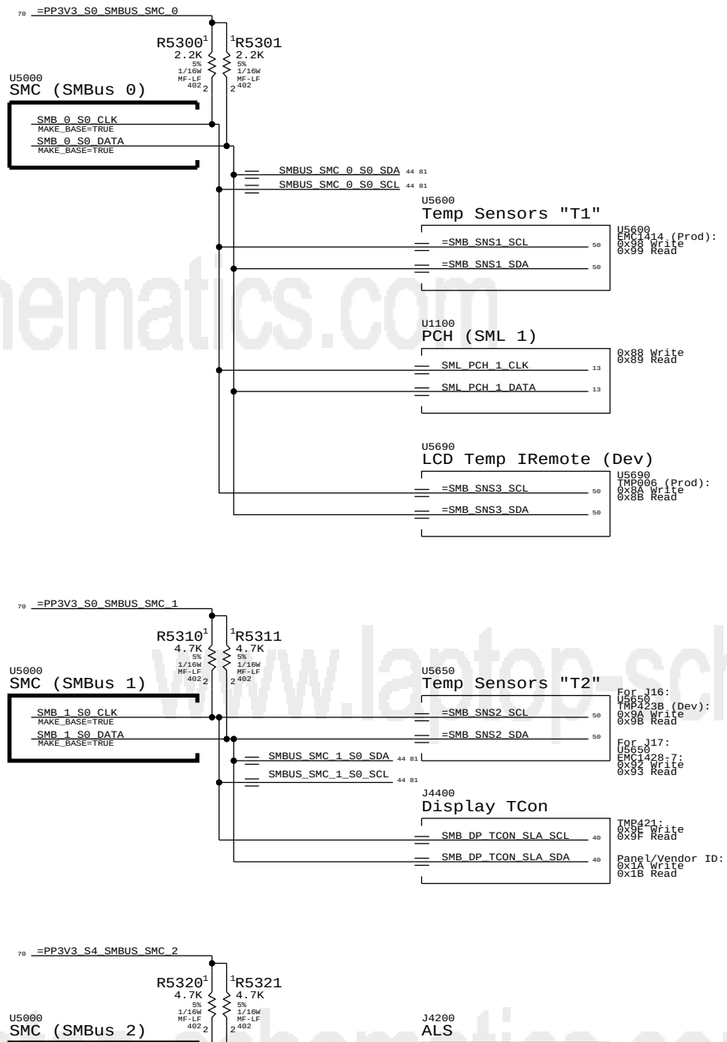
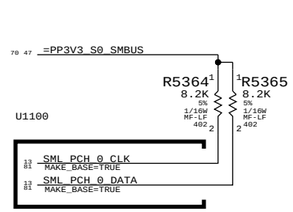
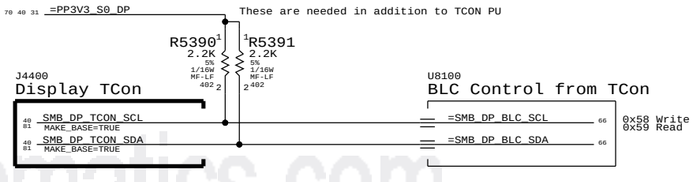



SMC multi-master experiment




Unused PCH SM Link




Line Legend
- Master
- Slave
- Mux

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# SMBus Connections

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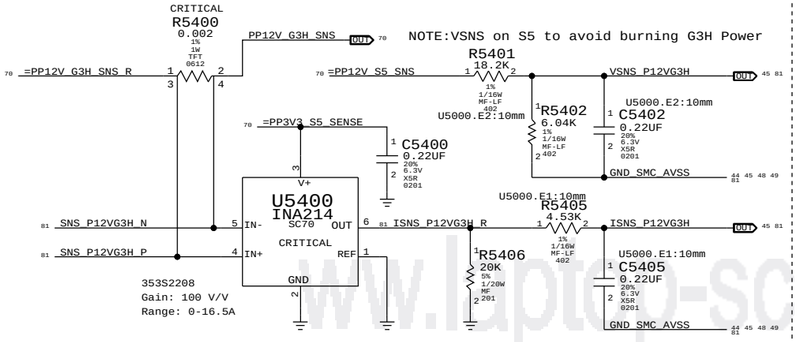
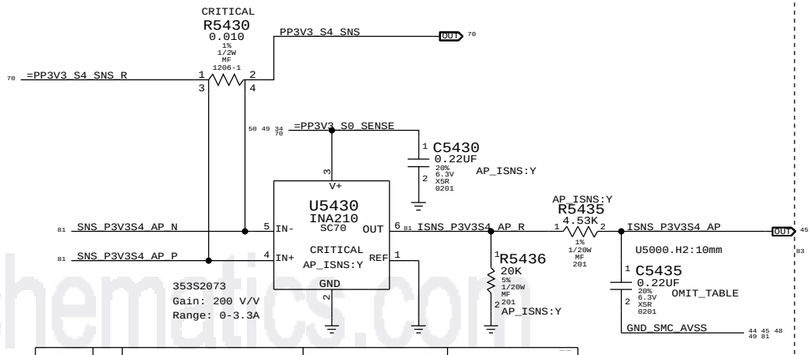
## 12V G3H (VD2R:ADC0/ID2R:ADC1) AC/DC lowside sense (System total)



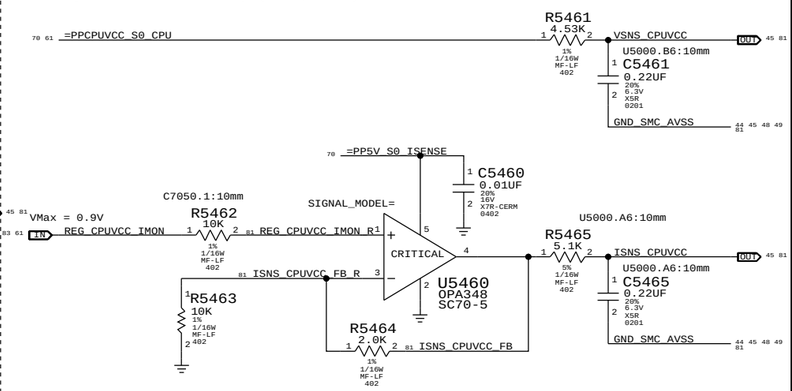

## PP3V3_S4_AP (IW0R:ADC19) Airport supply current sense




| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 132S0304 | 1 | CAP,0.22uF,201 | C5435 | AP_ISNS:Y |
| 117S0002 | 1 | RES,0 ohm,201 | C5435 | AP_ISNS:N |

## CPU Core (VC0C:ADC10/IC0C:ADC11)

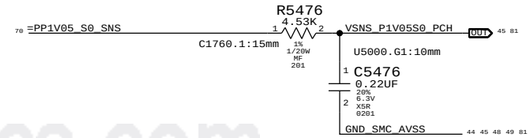
Voltage sense and IMON amp (VC0C, IC0C)




## PP1V05_S0_PCH (VN1R:ADC17)

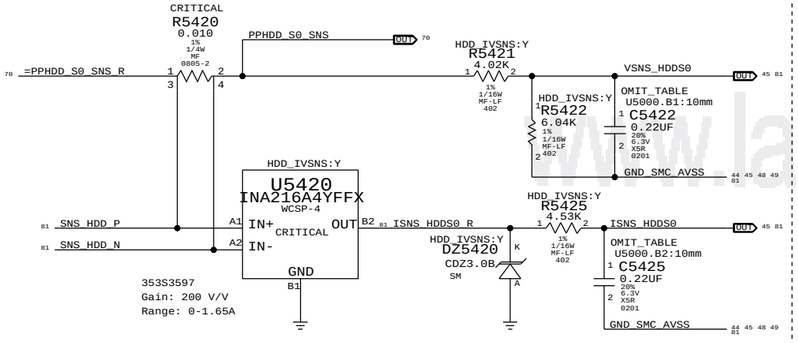
I/V-sense for PP1V05_S0_PCH

Place R5476 over PP1V05_S0 power plane shape.




## HDD S0 (VH05:ADC14/IH05:ADC15)

I/V-sense for HDD (Development, but need R5420)




| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 132S0304 | 2 | CAP,0.22UF,201 | C5422,C5425 | HDD_IVSNS:Y |
| 117S0002 | 2 | RES,0 OHM,201 | C5422,C5425 | HDD_IVSNS:N |

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PAGE TITLE: I and V Sense

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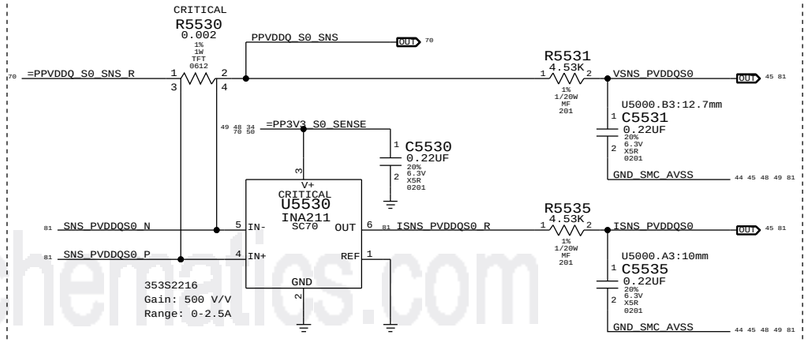
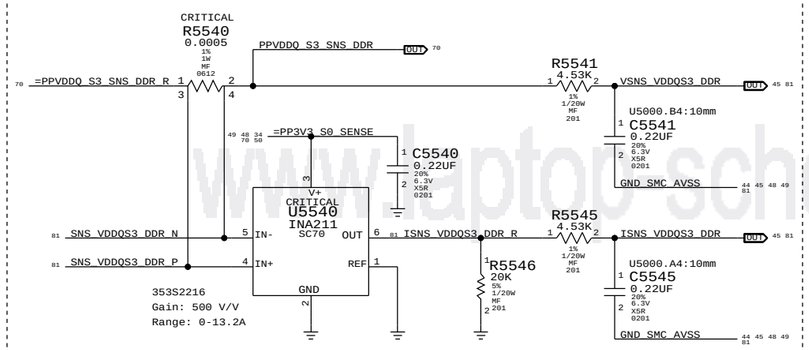
## PPVDDQ_S0 (VC0M:ADC4/IC0M:ADC5)

lowside sense for CPU mem rail (2.5A max draw, 3.3A max sense capability)

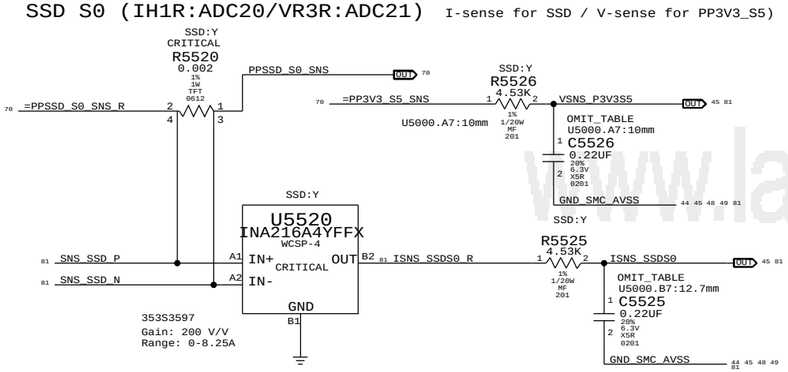



## VDDQ S3 (VM0R:ADC6/IM0R:ADC7)

VDDQ lowside sense for SO-DIMM modules




## SSD S0 (IH1R:ADC20/VR3R:ADC21) I-sense for SSD / V-sense for PP3V3_S5)




| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 132S0304 | 2 | CAP,0.22UF,201 | C5525,C5526 | SSD:Y |
| 117S0002 | 2 | RES,0 OHM,201 | C5525,C5526 | SSD:N |

SYNC_MASTER=J16 TONY SYNC_DATE=03/13/2013

PAGE TITLE: I and V Sense(Continued)

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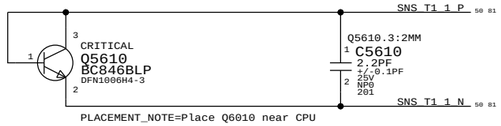
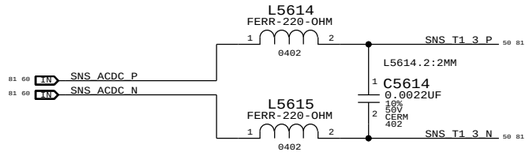
# Temperature Sensor T1

### MLB Proximity

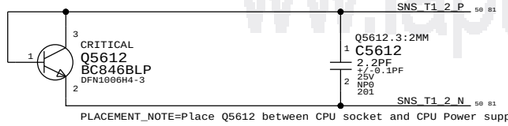



PLACEMENT_NOTE=Place Q6010 near CPU

### AC/DC Diode on supply

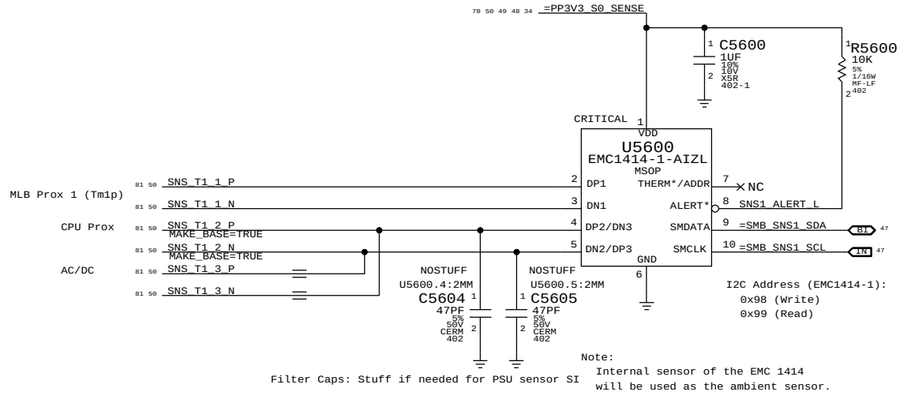



### CPU Proximity



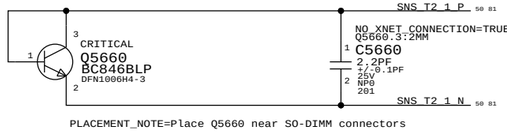

PLACEMENT_NOTE=Place Q5612 between CPU socket and CPU Power supply components

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 372S0186 | 372S0185 | | ALL | Alternate Temp Diode |



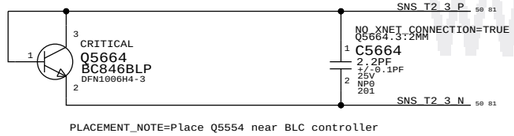

# Temperature Sensor T2

### SO-DIMM Proximity



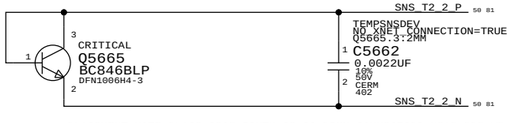

PLACEMENT_NOTE=Place Q5660 near SO-DIMM connectors

### BLC Proximity

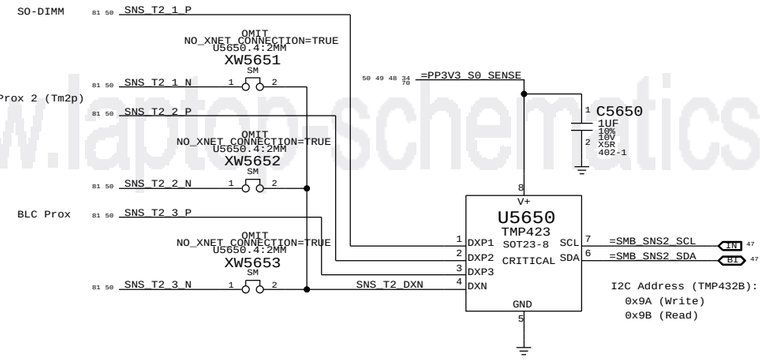



PLACEMENT_NOTE=Place Q5554 near BLC controller

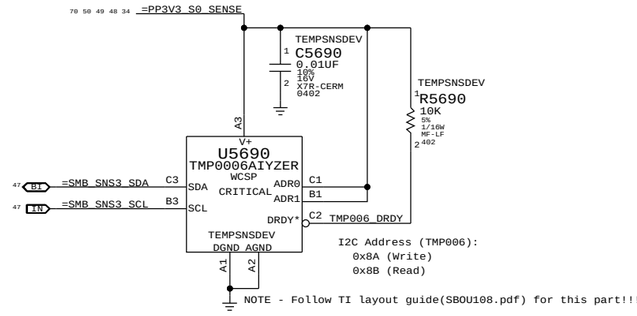
### MLB Proximity




PLACEMENT_NOTE=PLACE Q565 SOUTH OF SO-DIMM CONNECTORS NEAR DDR VR




# Temperature Sensor T3: LCD Remote Sensor(Dev Only)




This PD part is a rubber bumper to protect TMP006
Added to board BOM (DEV only) to clean up PD BOM

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 875-6433 | 1 | BUMPER,U5690,D7 | BUMPER_U5690 | TEMPSNSDEV |

SYNC_MASTER=J16_FIYIN SYNC_DATE=01/11/2013

PAGE TITLE: Temperature Sensors

Apple Inc.

DRAWING NUMBER: 051-0164 SIZE: D
REVISION: 12.4.0
BRANCH:
PAGE: 56 OF 123
SHEET: 50 OF 86

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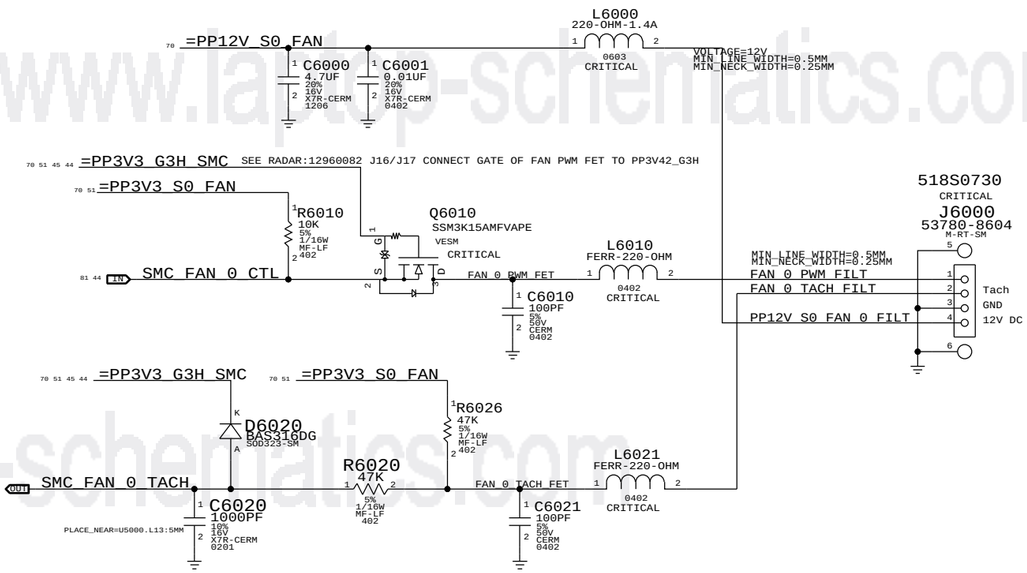
# SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).




Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

# SMC Fan 1 (Unused)

SYNC_MASTER=J16_JERRY SYNC_DATE=01/07/2013

PAGE TITLE: System Fan

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DRAWING NUMBER: 051-0164 SIZE: D

REVISION: 12.4.0

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# AUDIO CODEC

APPLE P/N 353S2592

PLACE C6100 AS CLOSE TO PIN 9 AS POSSIBLE

VD MUST BE LESS THAN OR EQUAL TO VL_HD

=PP1V5_S0_AUD_DIG

C6101 4.7UF 20% 4V X5R-1 402

C6100 0.47UF 10% 10V X5R 0402

GND_AUDIO_CODEC

PP4V5_AUDIO_ANALOG

R6100 2.67K 1% 1/16W MF-LF 402

C6109 2.2UF 20% 6.3V CERM 402-LF

C6110 2.2UF 20% 6.3V CERM 402-LF

C6108 10UF 20% 16V POLY-TANT CASE-B2-SM

VBIAS_DAC

CS4206_FP

CS4206_FN

U6101 CS4206B QFN

VD VA_REF VA_HP VA

PP5V_AUDIO_HPAMP

=PP3V3_S0_AUDIO

PP4V5_AUDIO_ANALOG

C6105 1UF 10% 10V X5R 402-1

C6104 0.47UF 10% 10V X5R 0402

C6106 0.47UF 10% 10V X5R 0402

C6107 CRITICAL 10UF 20% 10V X5R-CERM 0402-1

C6102 0.47UF 10% 10V X5R 0402

C6103 CRITICAL 10UF 20% 16V POLY-TANT CASE-B2-SM

GND_AUDIO_CODEC

R6105 0 5% 1/16W MF-LF 402

DMICS 1 & 2 — AUD_DMIC_SDA1

NC — TP_DMIC_SDA2

HP AMP CNTRL — AUD_GPIO_2

MAC SPKR AMP CNTRL — AUD_CODEC_MICBIAS

D6100 SOD-523 BAT54XV2T1

WIN SPKR AMP CNTRL — AUD_GPIO_3

AUD_SENSE_A

R6106 100K 1% 1/16W MF-LF 402

C6111 2.2UF 20% 6.3V CERM 402-LF

C6112 CRITICAL 2.2UF 20% 6.3V CERM 402-LF

CS4206_FLYP

CS4206_FLYC

CS4206_FLYN

GPIO0/DMIC_SDA1

GPIO1/DMIC_SCL/SPDIF_OUT2

GPIO2

GPIO3

SENSE_A

FLYP

FLYC

FLYN

VL_HD

VL_IF

HPOUT_L — TP_AUD_HP_L NC

HPOUT_R — TP_AUD_HP_R NC

HPREF — CS4206_HPREF

MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM

MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM

HP AMP/LINE OUT — RESERVE SPACE FOR POSSIBLE LATCH CIRCUIT

TWEETERS

LINEOUT_L1+ — AUD_LO1_L_P

LINEOUT_L1- — AUD_LO1_L_N

LINEOUT_R1+ — AUD_LO1_R_P

LINEOUT_R1- — AUD_LO1_R_N

WOOFERS

LINEOUT_L2+ — AUD_LO2_L_P

LINEOUT_L2- — AUD_LO2_L_N

LINEOUT_R2+ — AUD_LO2_R_P

LINEOUT_R2- — AUD_LO2_R_N

MICBIAS — AUD_CODEC_MICBIAS

VCOM — CS4206_VCOM

MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

LINEIN_L+ — AUD_LI_P_L NC

LINEIN_C- — AUD_LI_COM NC

LINEIN_R+ — AUD_LI_P_R NC

NO_TEST=TRUE

MICIN_L+ — AUD_MIC_INL_P

MICIN_L- — AUD_MIC_INL_N

MICIN_R+ — AUD_MIC_INP_R NC

MICIN_R- — AUD_MIC_INN_R NC

VREF+_ADC — CS4206_VREF_ADC NC

R6104 0 5% 1/16W MF-LF 402

DMIC_SCL — CS4206_DMIC_SCL

AUD_DMIC_CLK

Q6170 P S / P G — DEVEL_AUDIO CRITICAL Q6170 DMC2400UV SOT563 — R6170 0 5% 1/16W MF-LF 402

Q6170 N G / N S — DEVEL_AUDIO CRITICAL Q6170 DMC2400UV SOT563 — R6171 0 5% 1/16W MF-LF 402

Q6171 P S / P G — DEVEL_AUDIO CRITICAL Q6171 DMC2400UV SOT563 — R6172 0 5% 1/16W MF-LF 402

Q6171 N G / N S — DEVEL_AUDIO CRITICAL Q6171 DMC2400UV SOT563 — R6173 0 5% 1/16W MF-LF 402

PLACE TP FOR ALL HDA SIGNALS NEAR CODEC

HDA_BIT_CLK

HDA_SYNC

HDA_SDIN0

R6101 22 5% 1/16W MF-LF 402

AUD_SDI_R

HDA_SDOUT

HDA_RST_L

DP_INT_SPDIF_AUDIO

AUD_SPDIF_CHIP

AUD_SPDIF_OUT

R6102 22 5% 1/16W MF-LF 402

BITCLK

SYNC

SDI

SDO

RESET*

SPDIF_IN

SPDIF_OUT

DGND THRM_PAD AGND

R6103 100K 1% 1/16W MF-LF 402

DMICS SHOULD HAVE OWN GND ON CONNECTOR SHARED WITH CAMERA

GND_AUDIO_DMIC

MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM VOLTAGE=0V

XW6100 SM

C6113 CRITICAL 1UF 10% 25V TANT CASE-P3-HF

C6114 CRITICAL 10UF 20% 16V POLY-TANT CASE-B2-SM

C6115 0.47UF 10% 10V X5R 0402

R6107 100K 1% 1/16W MF-LF 402

R6108 100K 1% 1/16W MF-LF 402

R6109 100K 1% 1/16W MF-LF 402

R6110 100K 1% 1/16W MF-LF 402

R6111 100K 1% 1/16W MF-LF 402

GND_AUDIO_CODEC

## APPLE P/N 353S2456
## 4.5V POWER SUPPLY FOR CODEC

L6111 FERR-220-OHM 0402

MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM VOLTAGE=4.5V

PP5V_AUDIO_HPAMP

L6110 FERR-220-OHM 0402

=PP5V_S0_AUDIO

VR6101 TPS71745 SON CRITICAL

4V5_REG_IN

4V5_REG_EN

4V5_NR

PP4V5_AUDIO_ANALOG

MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.15MM VOLTAGE=4.5V

R6120 0 5% 1/16W MF-LF 402

=PP3V3_S0_AUDIO

C6122 1UF 10% 10V X5R 402-1

XW6110 SM

C6123 0.1UF 10% 16V X7R-CERM 0402

C6124 1UF 10% 10V X5R 402-1

MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM

GND_AUDIO_CODEC

MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

XW6111 SM

GND_AUDIO_HPAMP

MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

PLACE XW6110 BENEATH U6101, BETWEEN PINS 2 & 5

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=J16_DIRK SYNC_DATE=03/07/2013

PAGE TITLE: AUDIO: CODEC/REGULATORS

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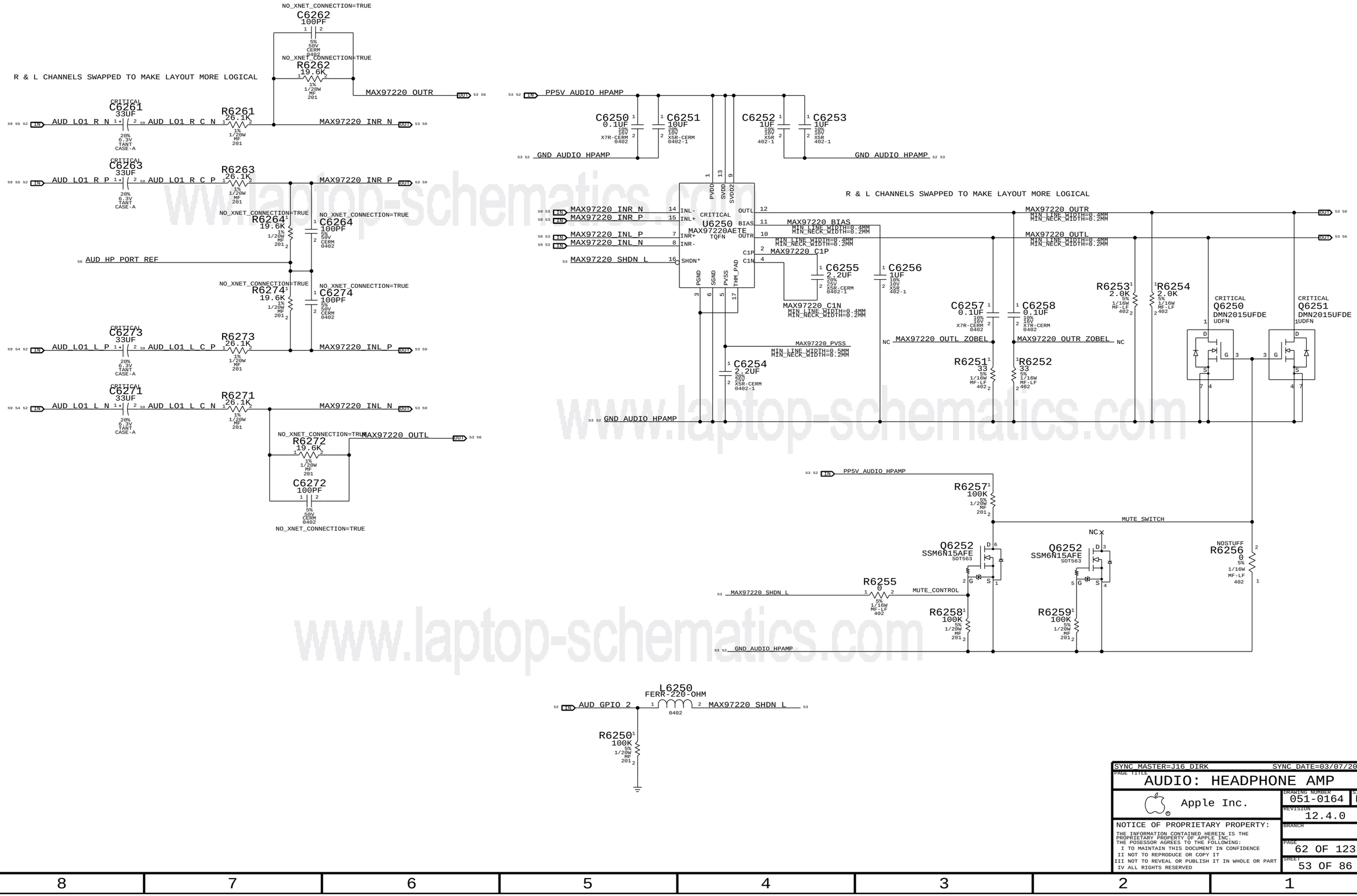


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SYNC_MASTER=J16_DIRK SYNC_DATE=03/07/2013

PAGE TITLE
# AUDIO: HEADPHONE AMP

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# LEFT CH SPEAKER AMP
## APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

=PP12V_S0_AUDIO_SPKRAMP

C6300 10UF 10% 25V X5R 805
C6301 10UF 10% 25V X5R 805
C6302 0.1UF 10% 25V X5R 402
C6303 1UF 10% 25V X5R 603-1
C6304 0.1UF 10% 25V X5R 402
C6305 1UF 10% 25V X5R 603-1
CRITICAL C6306 470UF 20% 16V POLY SM

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6303 FERR-1000-OHM 0402 — AUD_LO1_L_N — AUD_LAMP_RINC_P — C6308 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_LAMP_RIN_P
L6302 FERR-1000-OHM 0402 — AUD_LO1_L_P — AUD_LAMP_RINC_N — C6309 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_LAMP_RIN_N
L6300 FERR-1000-OHM 0402 — AUD_LO2_L_N — AUD_LAMP_LINC_P — C6310 1UF 10% 25V X5R 0402 — AUD_LAMP_LIN_P
L6301 FERR-1000-OHM 0402 — AUD_LO2_L_P — AUD_LAMP_LINC_N — C6311 1UF 10% 25V X5R 0402 — AUD_LAMP_LIN_N

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

=PP3V3_S0_AUDIO

CRITICAL U6300 SSM3302 LFCSP

| | |
|---|---|
| PVDD | 34, 35, 36, 37 |
| INR+ | 20 |
| INR- | 19 |
| SDNR* | 22 |
| MONO | 16 |
| SDNL* | 9 |
| INL+ | 11 |
| INL- | 12 |
| GAIN | 21 |
| VREG/AVDD | 8 |
| REGEN | 23 |
| AGND | 7, 24 |
| THRM_PAD | 41 |
| PGND | 31, 32, 33, 38, 39, 40 |
| THERM | 17 |
| BOOTR+ | 30 |
| OUTR+ | 28, 29 |
| OUTR- | 26, 27 |
| BOOTR- | 25 |
| EDGE | 10 |
| BOOTL+ | 1 |
| OUTL+ | 2, 3 |
| OUTL- | 4, 5 |
| BOOTL- | 6 |
| NC | 18, 13 |
| TEST | 14, 15 |

WOOFERS & TWEETERS ON UNDER MAC OS — AUD_SPKRAMP_MAC_SHDN_L
ONLY WOOFERS ON UNDER WINDOWS — AUD_SPKRAMP_WIN_SHDN_L
AUD_LAMP_MONO
AUD_LAMP_GAIN
AUD_LAMP_AVDD — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V

C6317 2.2UF 20% 10V X5R-CERM 402

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

TP_AUD_LAMP_THERM — NC

C6313 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTRP — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM
C6314 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTRN — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM
C6315 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTLP — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM
C6316 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTLN — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM

AUD_LAMP_EDGE

AUD_LAMP_OUTPR — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
AUD_LAMP_OUTNR — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
AUD_LAMP_OUTPL — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
AUD_LAMP_OUTNL — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM

NO_XNET_CONNECTION=TRUE
CRITICAL L6305 110-OHM-3A DLY5ATN111SQ2
CRITICAL L6307 110-OHM-3A DLY5ATN111SQ2

AUD_SPKR_LTWT_OUT_P — NO_XNET_CONNECTION=TRUE — CRITICAL C6323 1000PF 5% 25V CERM 0402 — AUD_SPKR_LTWT_OUT_N
AUD_SPKR_LWFR_OUT_N — NO_XNET_CONNECTION=TRUE — CRITICAL C6324 1000PF 5% 25V CERM 0402 — AUD_SPKR_LWFR_OUT_P

CRITICAL C6320 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE
CRITICAL C6322 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE
CRITICAL C6319 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE
CRITICAL C6321 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE

L6308 FERR-1000-OHM 0402 — AUD_CODEC_MICBIAS — AUD_SPKRAMP_MAC_SHDN_L
R6301 100K 5% 1/16W MF-LF 402 — NOSTUFF C6312 100PF 5% 50V CERM 0402

R6308 0 5% 1/16W MF-LF 402 — AUD_GPIO_3 — AUD_SPKRAMP_WIN_SHDN_L
R6309 100K 5% 1/16W MF-LF 402 — NOSTUFF C6318 100PF 5% 50V CERM 0402

| EDGE RATE CONTROL | R6304 | R6305 |
|---|---|---|
| ON | 0 OHM | NOSTUFF |
| OFF | NOSTUFF | 0 OHM |

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

| GAIN | R6306 | R6307 |
|---|---|---|
| +9 DB | NOSTUFF | 0 OHM |
| +12 DB | NOSTUFF | 47 KOHM |
| +15 DB | NOSTUFF | NOSTUFF |
| +18 DB | 47 KOHM | NOSTUFF |
| +24 DB | 0 OHM | NOSTUFF |

AUD_LAMP_AVDD
R6304 0 5% 1/16W MF-LF 402 — AUD_LAMP_EDGE
NOSTUFF R6305 0 5% 1/16W MF-LF 402
R6303 0 5% 1/16W MF-LF 402 — AUD_LAMP_MONO
NOSTUFF R6306 0 5% 1/16W MF-LF 402 — AUD_LAMP_GAIN
R6307 47K 5% 1/16W MF-LF 402

SYNC_MASTER=J16_DIRK SYNC_DATE=03/07/2013
PAGE TITLE: AUDIO: LEFT SPKR AMP

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# RIGHT CH SPEAKER AMP
## APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

=PP12V_S0_AUDIO_SPKRAMP

C6400 10UF 10% 25V X5R 805
C6401 10UF 10% 25V X5R 805
C6402 0.1UF 10% 25V X5R 402
C6403 1UF 10% 25V X5R 603-1
C6404 0.1UF 10% 25V X5R 402
C6405 1UF 10% 25V X5R 603-1
CRITICAL C6406 470UF 20% 16V POLY SM

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6400 FERR-1000-OHM 0402 — AUD_LO2_R_N — AUD_RAMP_RINC_P — C6408 1UF 10% 25V X5R 0402 — AUD_RAMP_RIN_P
L6401 FERR-1000-OHM 0402 — AUD_LO2_R_P — AUD_RAMP_RINC_N — C6409 1UF 10% 25V X5R 0402 — AUD_RAMP_RIN_N
L6402 FERR-1000-OHM 0402 — AUD_LO1_R_P — AUD_RAMP_LINC_P — C6410 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_RAMP_LIN_P
L6403 FERR-1000-OHM 0402 — AUD_LO1_R_N — AUD_RAMP_LINC_N — C6411 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_RAMP_LIN_N

=PP3V3_S0_AUDIO

CRITICAL U6400 SSM3302 LFCSP

| | | |
|---|---|---|
| 34,35,36,37 | PVDD | |
| 20 | INR+ | |
| 19 | INR- | |
| 54 EN | AUD_SPKRAMP_WIN_SHDN_L | ONLY WOOFERS ON UNDER WINDOWS |
| 22 | SDNR* | |
| 55 | AUD_RAMP_MONO | |
| 16 | MONO | |
| 54 EN | AUD_SPKRAMP_MAC_SHDN_L | WOOFERS & TWEETERS ON UNDER MAC OS |
| 9 | SDNL* | |
| 11 | INL+ | |
| 12 | INL- | |
| 55 | AUD_RAMP_GAIN | |
| 21 | GAIN | |
| 55 | AUD_RAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V) | |
| 8 | VREG/AVDD | |
| 23 | REGEN | |
| 7,24,41 | AGND | |
| 31,32,33,38,39,40 | PGND | |
| | THRM_PAD | |
| | C6417 2.2UF 20% 10V X5R-CERM 402 | |

| | | |
|---|---|---|
| THERM 17 | TP_AUD_RAMP_THERM | NC |
| BOOTR+ 30 | AUD_RAMP_BOOTRP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) | C6413 0.22UF 20% 25V X5R 603 |
| OUTR+ 28,29 | AUD_RAMP_OUTRP (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) | NO_XNET_CONNECTION=TRUE; CRITICAL L6405 110-OHM-3A DLY5ATN111SQ2; AUD_SPKR_RWFR_OUT_P; NO_XNET_CONNECTION=TRUE; CRITICAL C6423 1000PF 5% 25V CERM 0402; AUD_SPKR_RWFR_OUT_N |
| OUTR- 26,27 | AUD_RAMP_OUTRN (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) | |
| BOOTR- 25 | AUD_RAMP_BOOTRN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) | C6414 0.22UF 20% 25V X5R 603 |
| EDGE 10 | AUD_RAMP_EDGE | |
| BOOTL+ 1 | AUD_RAMP_BOOTLP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) | C6415 0.22UF 20% 25V X5R 603 |
| OUTL+ 2,3 | AUD_RAMP_OUTLP (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) | NO_XNET_CONNECTION=TRUE; CRITICAL L6407 110-OHM-3A DLY5ATN111SQ2; AUD_SPKR_RTWT_OUT_P; NO_XNET_CONNECTION=TRUE; CRITICAL C6424 1000PF 5% 25V CERM 0402; AUD_SPKR_RTWT_OUT_N |
| OUTL- 4,5 | AUD_RAMP_OUTLN (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) | |
| BOOTL- 6 | AUD_RAMP_BOOTLN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) | C6416 0.22UF 20% 25V X5R 603 |
| NC 18 | NC | |
| NC 13 | NC | |
| TEST 14,15 | | |

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

CRITICAL C6420 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE
CRITICAL C6422 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE
CRITICAL C6419 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE
CRITICAL C6421 1000PF 5% 25V CERM 0402 — NO_XNET_CONNECTION=TRUE

EDGE RATE CONTROL

| | R6404 | R6405 |
|---|---|---|
| ON | 0 OHM | NOSTUFF |
| OFF | NOSTUFF | 0 OHM |

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

| GAIN | R6406 | R6407 |
|---|---|---|
| +9 DB | NOSTUFF | 0 OHM |
| +12 DB | NOSTUFF | 47 KOHM |
| +15 DB | NOSTUFF | NOSTUFF |
| +18 DB | 47 KOHM | NOSTUFF |
| +24 DB | 0 OHM | NOSTUFF |

AUD_RAMP_AVDD
R6404 0 5% 1/16W MF-LF 402 — AUD_RAMP_EDGE
NOSTUFF R6405 0 5% 1/16W MF-LF 402
R6403 0 5% 1/16W MF-LF 402 — AUD_RAMP_MONO
NOSTUFF R6406 0 5% 1/16W MF-LF 402 — AUD_RAMP_GAIN
R6407 47K 5% 1/16W MF-LF 402

SYNC_MASTER=J16_DIRK SYNC_DATE=03/07/2013

PAGE TITLE: AUDIO: RIGHT SPKR AMP

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# MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2640

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=10.63KHZ

MIKEY 1A
APN:353S2640
MIKEY ADDRESS: WRITE=72H, READ=73H

I2C ADDRESSES

| | | | |
|---|---|---|---|
| MIKEY | READ | 0111 0011 | 0X73 |
| MIKEY | WRITE | 0111 0010 | 0X72 |
| CHS | READ | 0111 0111 | 0X77 |
| CHS | WRITE | 0111 0110 | 0X76 |

AUDIO JACK: HP CONNECTOR WITH MIKEY
PLACE XWS 6500 & 6501 AT J6500 PINS

I2C PULLUPS ON SOUTHBRIDGE PAGE

PP4V5_AUDIO_ANALOG
=PP3V3_S0_AUDIO_DIG
R6562 10K 5% 1/20W MF 201
CRITICAL C6555 4.7UF 20% 10V X5R-CERM 0402
C6560 0.1UF 10% 16V X7R-CERM 0402
U6551 CD3285A0 MQFN-RSV
AVDD
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA
AUD_I2C_INT_L
AUD_IPHS_SWITCH_EN
SCL
SDA
INT*
ENABLE
HDET
CS
DGND AGND
MICBIAS
DETECT
BYPASS
HS_MIC_BIAS
HS_SW_DET
HS_RX_BP
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.20MM
NO_XNET_CONNECTION=TRUE
R6554 1K 5% 1/10W MF-LF 402
NOSTUFF R6561 47K 5% 1/16W MF-LF 402
HS_HDET
AUD_PORTD_DET_L
R6555 100K 5% 1/20W MF 201
C6556 0.01UF 10% 25V X7R 402
GND_AUDIO_CODEC
C6552 0.1UF 10% 16V X7R-CERM 0402
AUD_MIC_INL_P
R6550 2.2K 5% 1/10W MF-LF 402
AUD_HS_MIC_RC_P
AUD_HS_MIC_P
R6556 100K 5% 1/20W MF 201
CRITICAL C6550 0.0082UF 10% 25V X7R-CERM 0402
CRITICAL C6558 27PF 5% 50V CERM 0402-1
C6553 0.1UF 10% 16V X7R-CERM 0402
AUD_MIC_INL_N
R6551 0 5% 1/10W MF-LF 402
AUD_HS_MIC_RC_N
AUD_HS_MIC_N
R/C6750 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210118)
NOSTUFF R6553 1K 5% 1/10W MF-LF 402
L6500 FERR-1000-OHM 0402
AUD_TYPEDET_R
L6501 FERR-1000-OHM 0402
L6502 FERR-1000-OHM 0402
CRITICAL L6503 FERR-120-OHM-2.0A 0402
L6511 FERR-120-OHM-2.0A 0402
=PP3V3_S4_AUDIO_DIG
L6505 FERR-1000-OHM 0402
AUD_TIPDET2_R
R6506 0 5% 1/10W MF-LF 402
VOLTAGE=0V
NOSTUFF DZ6500 ESDALC5-1BM2 SOD882
NOSTUFF DZ6501 ESDALC5-1BM2 SOD882
NOSTUFF DZ6502 ESDALC5-1BM2 SOD882
POLARITY INTENTIONALLY OPPOSIDE

APN 516S0687

CRITICAL
NO_XNET_CONNECTION=TRUE
J6500 54722-0224 F-ST-SM
AUD_J1_TYPEDET_R
AUD_J1_MIC_N
AUD_J1_MIC_P
AUD_J1_MIC_BIAS
AUD_J1_PP3V3_S0
=I2C_CHS_SDA
AUD_J1_TIPDET2_R
AUD_J1_HP_OUTL
AUD_J1_HP_PORT_REF
AUD_J1_HP_OUTR
=I2C_CHS_SCL
AUD_SPDIF_OUT
AUD_J1_TIPDET1_R
AUD_J1_GND_ANALOG
CRITICAL L6507 FERR-120-OHM-2.0A 0402
MAX97220_OUTL
CRITICAL L6508 FERR-120-OHM-2.0A 0402
AUD_HP_PORT_REF
CRITICAL L6509 FERR-120-OHM-2.0A 0402
MAX97220_OUTR
L6510 FERR-1000-OHM 0402
AUD_TIPDET1_R
NOSTUFF DZ6503 ESDALC5-1BM2 SOD882
NOSTUFF DZ6504 ESDALC5-1BM2 SOD882
NOSTUFF DZ6505 ESDALC5-1BM2 SOD882

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SYNC_MASTER=J16_DIRK SYNC_DATE=03/07/2013

PAGE TITLE
AUDIO: Jack, Mikey, CHS Switch

Apple Inc.

DRAWING NUMBER 051-0164 SIZE D
REVISION 12.4.0
BRANCH
PAGE 65 OF 123
SHEET 56 OF 86

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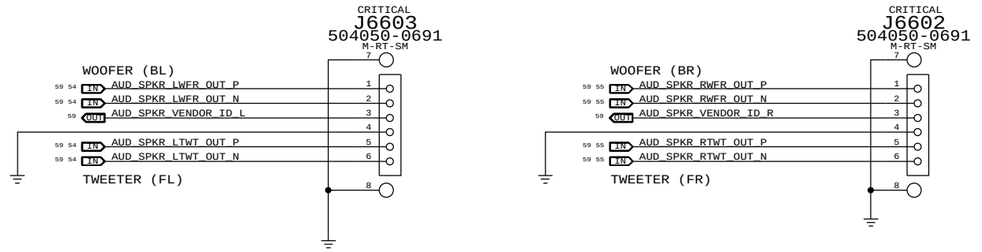
# SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862

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SYNC_MASTER=J16_DIRK SYNC_DATE=03/07/2013

PAGE TITLE: Audio: Spkr/Mic Conn.

Apple Inc.

DRAWING NUMBER: 051-0164 SIZE: D

REVISION: 12.4.0

BRANCH:

PAGE: 66 OF 123

SHEET: 57 OF 86

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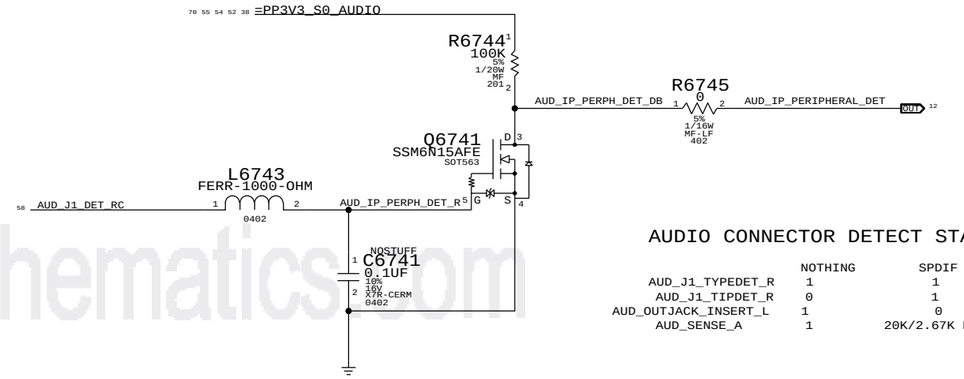
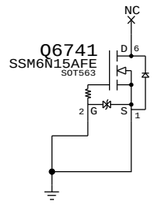
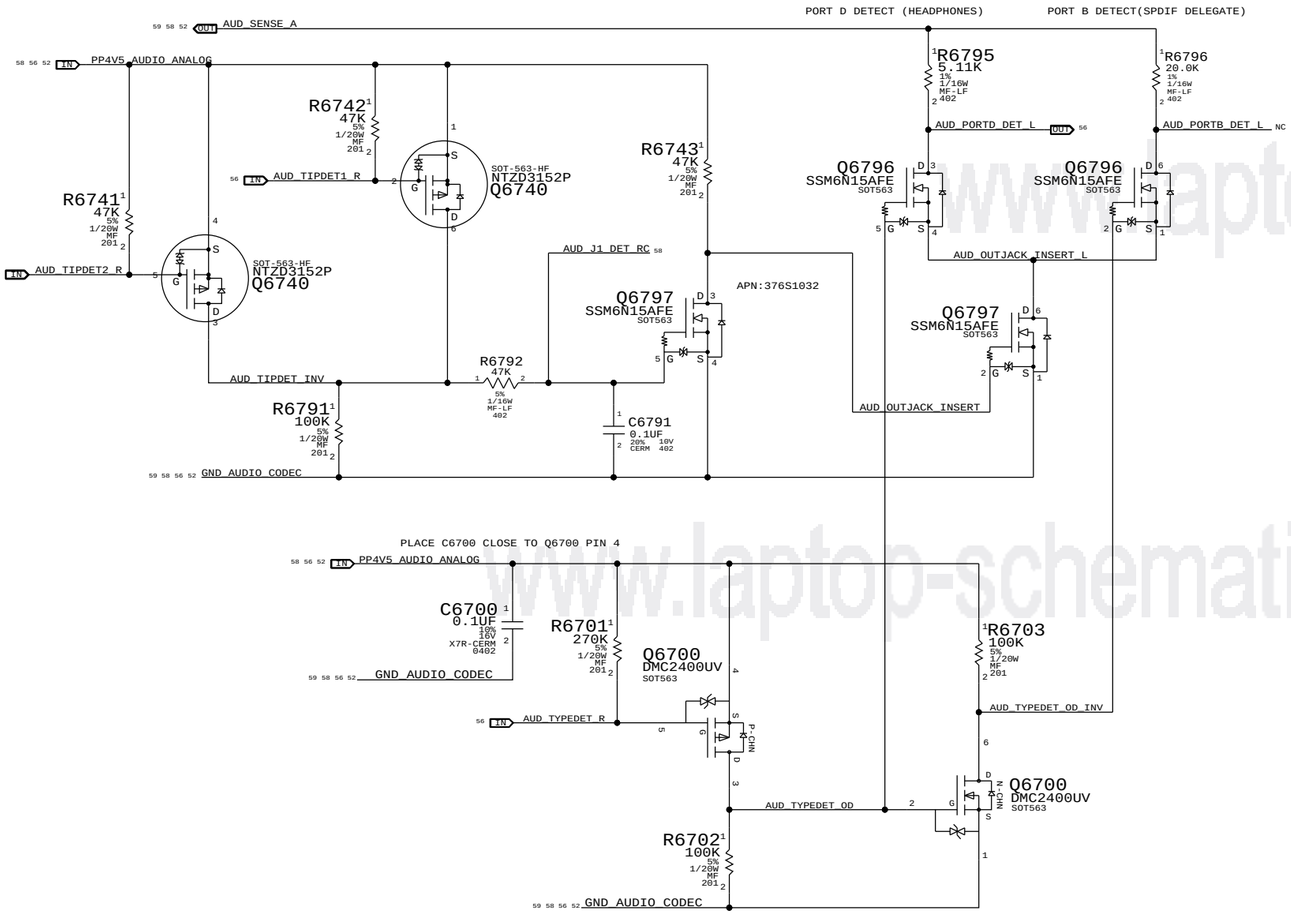
# IPHS HS Detect Debounce CKT




## AUDIO CONNECTOR DETECT STATES

| | NOTHING | SPDIF | HEADPHONE |
|---|---|---|---|
| AUD_J1_TYPEDET_R | 1 | 1 | 0 |
| AUD_J1_TIPDET_R | 0 | 1 | 1 |
| AUD_OUTJACK_INSERT_L | 1 | 0 | 0 |
| AUD_SENSE_A | 1 | 20K/2.67K RDIV | 39.2K/2.67K RDIV |



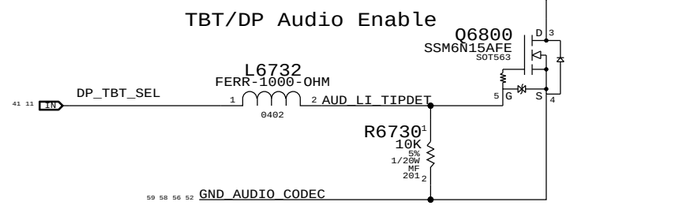




## Target Display Mode Detect




## TBT/DP Audio Enable

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SYNC_MASTER=J16_DIRK SYNC_DATE=03/07/2013

PAGE TITLE
AUDIO: Detects/Grounding

Apple Inc.

DRAWING NUMBER 051-0164 SIZE D
REVISION 12.4.0
BRANCH
PAGE 67 OF 123
SHEET 58 OF 86

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## CODEC OUTPUT SIGNAL PATHS

| FUNCTION | VOLUME/MUTE | CONVERTER | PIN COMPLEX | MAC SHDN | WIN SHDN | DET ASSIGNMENT |
|---|---|---|---|---|---|---|
| HP/LINE OUT | 0X03 (3) | 0X03 (3) | 0X0A (10,D) | GPIO_2 | GPIO_2 | 0X0A (DET D) |
| PRIMARY SPKRS (WFR) | 0X04 (4) | 0X04 (4) | 0X0B (11) | MICBIAS | GPIO_3 | N/A |
| SECONDARY SPKRS (TWT) | 0X03 (3) | 0X03 (3) | 0X0A (10,V24) | MICBIAS | N/A | N/A |
| SPDIF OUT | N/A | 0X08 (8) | 0x10 (16) | N/A | N/A | 0X0D (DET B) |

## CODEC INPUT SIGNAL PATHS

| FUNCTION | CONVERTER | PIN COMPLEX | ENABLE/CONTROL | DET ASSIGNMENT |
|---|---|---|---|---|
| SPDIF IN | 0X07 (7) | 0x0F (15) | N/A | 0X09 (DET A) |
| INTERNAL MIC ARRAY | 0X06 (6)<br>0X05 (5) | 0X0E (14,LEFT & RIGHT)<br>0X12 (18,LEFT) | N/A | N/A |
| EXTERNAL MIC | 0X06 (6) | 0X0D (13,V22,B,LEFT) | Lynx POINT GPIO 16 | Lynx POINT GPIO 5 (RCVR INT)<br>Lynx POINT GPIO 3 (PERIPH DET) |

## OTHER DETECT

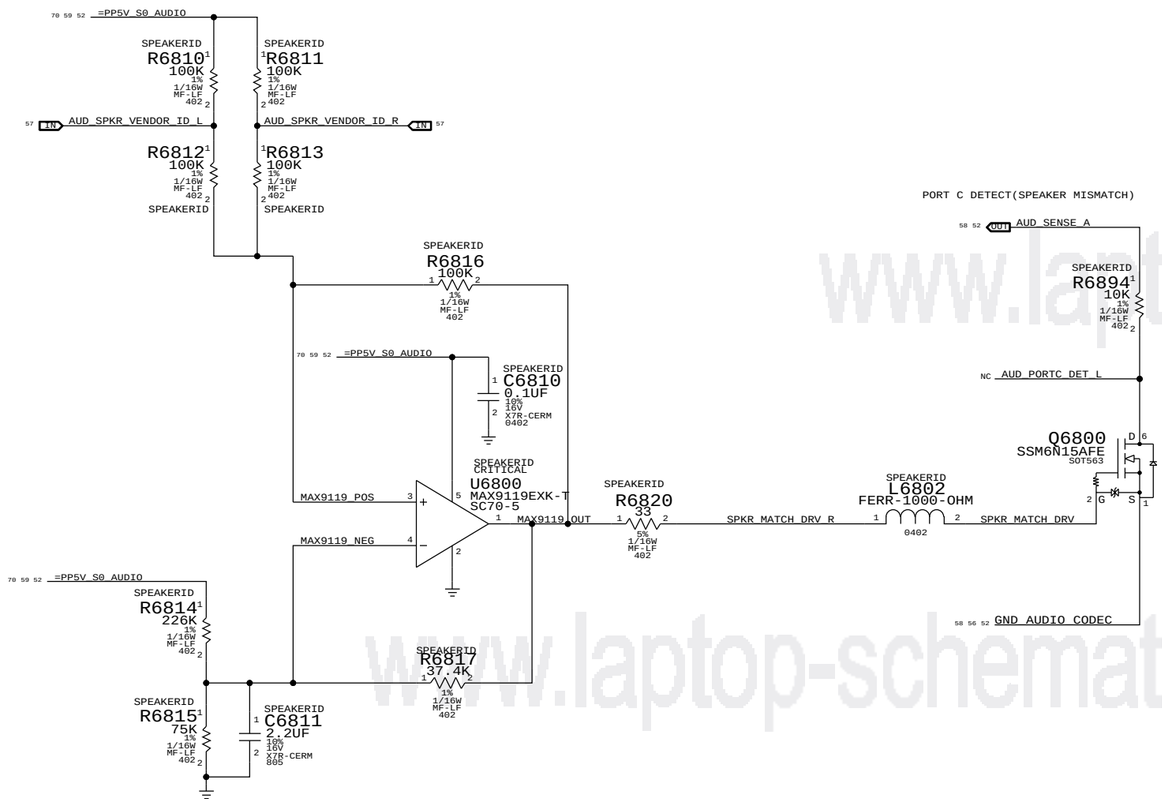
| FUNCTION | CONVERTER | PIN COMPLEX | ENABLE/CONTROL | DET ASSIGNMENT |
|---|---|---|---|---|
| MULTIPLE SPKR VENDORS | N/A | N/A | N/A | 0X0C (DET C) |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| AUDIO | * | 0.1 MM | ? |
| SPKROUT | * | 0.2 MM | ? |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| AUDIODIFF | * | AUDIODIFF |
| SPKROUTDIFF | * | SPKROUTDIFF |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| AUDIODIFF | * | Y | 0.1 MM | 0.1 MM | 10 MM | 0.1 MM | 0.1 MM |
| SPKROUTDIFF | * | Y | 0.6 MM | 0.25 MM | 10 MM | 0.2 MM | 0.2 MM |

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE: PHYSICAL | NET_TYPE: SPACING | | |
|---|---|---|---|---|
| 1535 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_L_P | 52 53 54 |
| 1536 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_L_N | 52 53 54 |
| 1537 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_L_C_P | 53 |
| 1538 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_L_C_N | 53 |
| 1539 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_R_P | 52 53 55 |
| 1540 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_R_N | 52 53 55 |
| 1541 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_R_C_P | 53 |
| 1542 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_R_C_N | 53 |
| 1543 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO2_L_P | 52 54 |
| 1544 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO2_L_N | 52 54 |
| 1545 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO2_R_P | 52 55 |
| 1546 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO2_R_N | 52 55 |
| 1547 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_LINC_P | 55 |
| 1548 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_LINC_N | 55 |
| 1549 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_RINC_P | 55 |
| 1550 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_RINC_N | 55 |
| 1551 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_LIN_P | 55 |
| 1552 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_LIN_N | 55 |
| 1553 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_RIN_P | 55 |
| 1554 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_RIN_N | 55 |
| 1555 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_LINC_P | 54 |
| 1556 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_LINC_N | 54 |
| 1557 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_RINC_P | 54 |
| 1558 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_RINC_N | 54 |
| 1559 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_LIN_P | 54 |
| 1560 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_LIN_N | 54 |
| 1561 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_RIN_P | 54 |
| 1562 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_RIN_N | 54 |
| 1563 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | MAX9722D_INL_P | 53 |
| 1564 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | MAX9722D_INL_N | 53 |
| 1565 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | MAX9722D_INR_P | 53 |
| 1566 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | MAX9722D_INR_N | 53 |
| 1567 SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_RWFR_OUT_P | 55 57 |
| 1568 SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_RWFR_OUT_N | 55 57 |
| 1569 SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_RTWT_OUT_P | 55 57 |
| 1570 SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_RTWT_OUT_N | 55 57 |
| 1571 SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_LWFR_OUT_P | 54 57 |
| 1572 SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_LWFR_OUT_N | 54 57 |
| 1573 SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_LTWT_OUT_P | 54 57 |
| 1574 SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_LTWT_OUT_N | 54 57 |
| 1575 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_MIC_INL_P | 52 56 |
| 1576 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_MIC_INL_N | 52 56 |
| 1577 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_HS_MIC_RC_P | 56 |
| 1578 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_HS_MIC_RC_N | 56 |
| 1579 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_HS_MIC_P | 56 |
| 1580 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_HS_MIC_N | 56 |
| 1581 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_J1_MIC_P | 56 |
| 1582 AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_J1_MIC_N | 56 |

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SYNC_MASTER=J16_DIRK SYNC_DATE=03/07/2013

PAGE TITLE: AUDIO: Speaker ID

Apple Inc.

DRAWING NUMBER: 051-0164 SIZE: D

REVISION: 12.4.0

BRANCH:

PAGE: 68 OF 123

SHEET: 59 OF 86

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# 3.425V "G3Hot" Regulator

Switching freq: 409 kHz = $\frac{13.5}{L6901}$

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 138S0676 | 138S0691 | | C6905 | |

## MLB to AC-DC Connector

CRITICAL
J6900
43650-0603
F-RT-TH

PP12V_G3H_ACDC 70

C6911 10UF 10% 16V X5R-CERM 0805 — J6900.4:3mm
C6912 1000PF 5% 25V CERM 0402 — EMC — J6900.5:3mm
C6913 1000PF 5% 25V CERM 0402 — EMC — J6900.4:4mm

## MLB to AC-DC Supplemental Signal Connector

SILK_PART=PwrSig
CRITICAL
J6901
53780-8606
M-RT-SM

PWR_BTN 45 OUT
R6911 100 5% 1/16W MF-LF 402
C6914 1UF 10% 6.3V CERM 402
D6911 6.8V-100PF 402
PWR_BTN_R
SNS_ACDC_N 81 50 OUT
SNS_ACDC_P 81 50 OUT
BURSTMODE_EN_R_L
SMC_ACDC_ID 60 45 OUT

BURSTMODE_EN_L 65 45 IN
R6912 1K 5% 1/16W MF-LF 402
C6915 0.1UF 10% 16V X7R-CERM 0402
D6912 6.8V-100PF 402

=PP3V3_S0_VRD 70 64 61
R6913 10K 5% 1/16W MF-LF 402
SMC_ACDC_ID 60 45
C6916 1UF 10% 6.3V CERM 402

## 12V S5 FET

CRITICAL
Q6970
IRFH3702TRPBF
PQFN

=PP12V_G3H_FET_P12V_S5 70
C6970 0.1UF 10% 16V X7R-CERM 0402
PP12V_S5_FET OUT 70
FET_EN_P12V_S5_R
R6972 49.9K 1% 1/16W MF-LF 402

U6970
SLG5AP022-200030V
TDFN
VCC
ON
NC
GND
THRM PAD
D
G
S
PG

SMC_PM_G2_EN 45 44 IN
Input: 2.4V to 5.5V
FET_EN_P12V_S5
PM_PGOOD_FET_P12V_S5 OUT 68

SMC_PM_G2_EN IS PULLED DOWN ON SMC PAGE

## 3.425V "G3Hot" Regulator

=PP12V_G3H_REG_3V42_G3H 70
C6906 1UF 10% 25V X6S-CERM 0402
C6907 1UF 10% 25V X6S-CERM 0402
C6902 10UF 10% 16V X6S 0805
R6901 150K 1% 1/16W MF-LF 402
P3V42G3H_SHDN_L 84
R6902 49.9K 1% 1/16W MF-LF 402
NOSTUFF
C6901 1000PF 5% 25V CERM 0402

U6900
LT3470AEDFN
CRITICAL
VIN
SHDN*
NC
BOOST
SW
BIAS
FB
GND
THRM PAD

P3V42G3H_BOOST 84
C6903 0.22UF 10% 16V CERM 402
CRITICAL
L6901 33UH
CDPH4D19FHF-SM
P3V42G3H_SW 84
C6904 22PF 5% 50V CERM 0402
P3V42G3H_FB 84
R6903 348K 1% 1/16W MF-LF 402 <Ra>
R6904 200K 1% 1/16W MF-LF 402 <Rb>
C6905 22UF 20% 6.3V X5R-CERM1 0603
PP3V42_G3H_REG 70
Vout = 3.425
250mA max output
(Switcher limit)

Vout = 1.25V * (1 + Ra / Rb)

| | |
|---|---|
| SYNC_MASTER=J16_ROSSANA | SYNC_DATE=03/04/2013 |
| PAGE TITLE: Power Connectors / VReg G3Hot | |
| Apple Inc. | DRAWING NUMBER: 051-0164 SIZE: D |
| | REVISION: 12.4.0 |
| | BRANCH |
| | PAGE: 69 OF 123 |
| | SHEET: 60 OF 86 |

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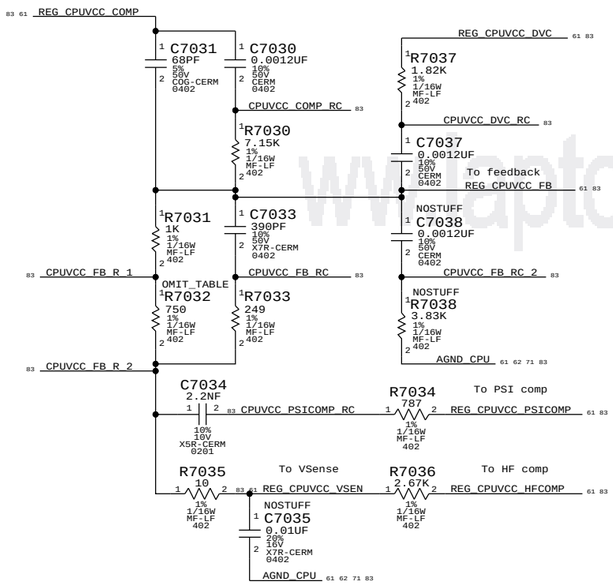
# CPU VCC S0 Regulator

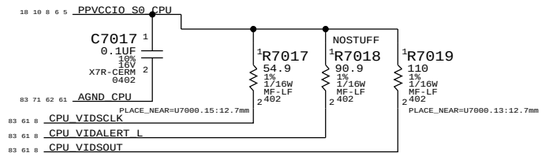
OC trip point: 114 A

Switching freq: 403 kHz = $\frac{5\ E10}{R7003}$

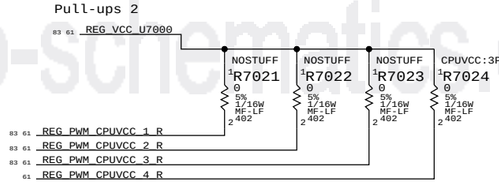
Compensation and feedback

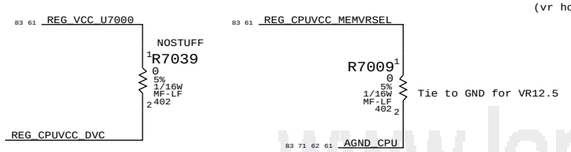


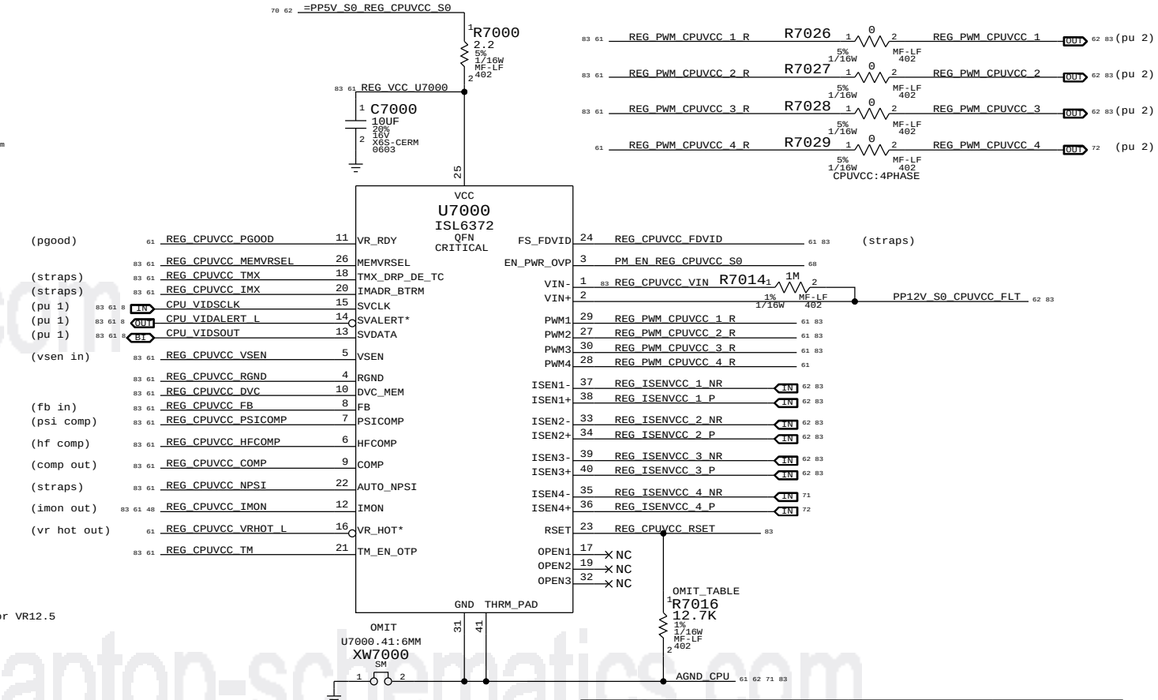

Pull-ups 1




Pull-ups 2



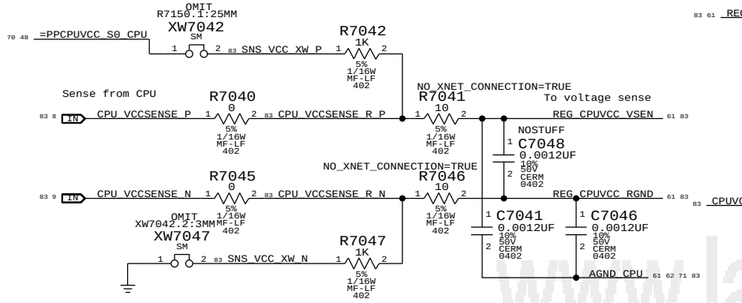





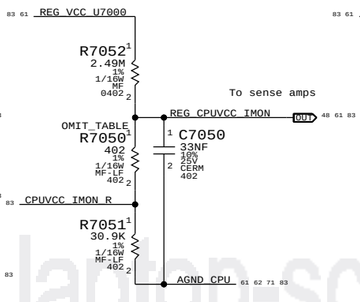


| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 114S0324 | 1 | RES,12.7K,402 | R7016 | CPUVCC:3PHASE |
| 114S0316 | 1 | RES,10.2K,402 | R7016 | CPUVCC:4PHASE |

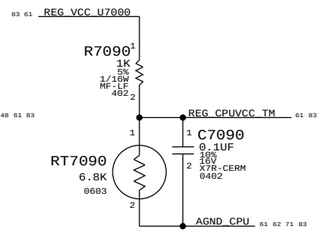
Voltage sense input



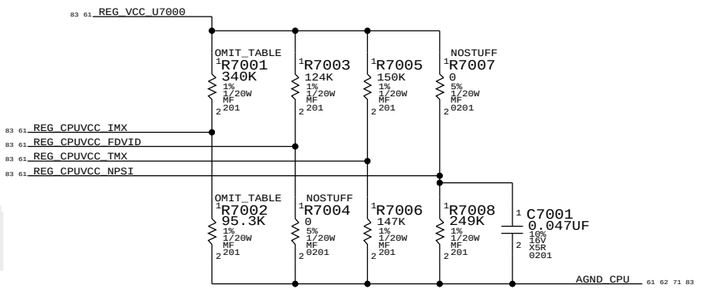

IMON output



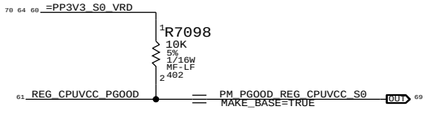

Temp measurement



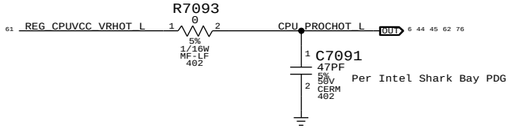

Straps




Power goods




VRHot to ProcHot




J16: 3PHASE
J17: 4PHASE

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 118S0311 | 1 | RES,340K,201 | R7001 | CPUVCC:3PHASE |
| 118S0116 | 1 | RES,158K,201 | R7001 | CPUVCC:4PHASE |
| 118S0575 | 1 | RES,95.3K,201 | R7002 | CPUVCC:3PHASE |
| 118S0380 | 1 | RES,44.2K,201 | R7002 | CPUVCC:4PHASE |
| 114S0206 | 1 | RES,750 OHM,402 | R7032 | CPUVCC:3PHASE |
| 114S0211 | 1 | RES,845 OHM,402 | R7032 | CPUVCC:4PHASE |
| 114S0179 | 1 | RES,402 OHM,402 | R7050 | CPUVCC:3PHASE |
| 114S0184 | 1 | RES,453 OHM,402 | R7050 | CPUVCC:4PHASE |

SYNC_MASTER=J16_ROSSANA SYNC_DATE=03/21/2013

PAGE TITLE: VReg CPU VCC Cntl

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REVISION: 12.4.0

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## CPU Phase 1

=PP5V_S0_REG_CPUVCC_S0

R7116 0 5% 1/10W MF-LF 603

C7116 0.22UF 10% 25V X7R 0603

REG_BOOT_CPUVCC_1_RC

REG_BOOT_CPUVCC_1

REG_PHASE_CPUVCC_1

REG_PWM_CPUVCC_1 (IN)

NOSTUFF R7115 0 5% 1/20W MF 0201

CPU_PROCHOT_L (OUT)

U7110.3:3MM C7125 1.0UF 10% 16V X7R 0603

PP12V_S0_CPUVCC_FLT

U7110 FDMF6808N PQFN CRITICAL

VDRV, BOOT, DISB*, GH, GL, PHASE, PWM, ZCD_EN*, THWN*, VCIN, VIN, VSWH, CGND, PGND, NC

REG_THWN_1

## CPU Phase 2

=PP5V_S0_REG_CPUVCC_S0

R7136 0 5% 1/10W MF-LF 603

C7136 0.22UF 10% 25V X7R 0603

REG_BOOT_CPUVCC_2_RC

REG_BOOT_CPUVCC_2

REG_PHASE_CPUVCC_2

REG_PWM_CPUVCC_2 (IN)

NOSTUFF R7135 0 5% 1/20W MF 0201

U7130.3:3MM C7145 1.0UF 10% 16V X7R 0603

U7130 FDMF6808N PQFN CRITICAL

REG_THWN_2

## CPU Phase 3

=PP5V_S0_REG_CPUVCC_S0

R7156 0 5% 1/10W MF-LF 603

C7156 0.22UF 10% 25V X7R 0603

REG_BOOT_CPUVCC_3_RC

REG_BOOT_CPUVCC_3

REG_PHASE_CPUVCC_3

REG_PWM_CPUVCC_3 (IN)

NOSTUFF R7155 0 5% 1/20W MF 0201

U7150.3:3MM C7165 1.0UF 10% 16V X7R 0603

U7150 FDMF6808N PQFN CRITICAL

REG_THWN_3

=PP5V_S0_REG_CPUVCC_S0

R7180 1K 1% 1/16W MF-LF 402

NOSTUFF R7181 1K 1% 1/16W MF-LF 402

REG_ZCDEN

## CPU Output Decoupling

PPCPUVCC_S0_REG

C7180 270UF-0.006OHM 20% 2.5V TANT CASE-D2

C7181 270UF-0.006OHM 20% 2.5V TANT CASE-D2

C7182 270UF-0.006OHM 20% 2.5V TANT CASE-D2

C7183 270UF-0.006OHM 20% 2.5V TANT CASE-D2

C7184 270UF-0.006OHM 20% 2.5V TANT CASE-D2

C7185 270UF-0.006OHM 20% 2.5V TANT CASE-D2

## Filtered 12V Rail

CRITICAL L7100 0.36UH-30A-0.6MOHM SDP110808MR36MF-TH

=PP12V_S0_REG_CPUVCC_S0 — PP12V_S0_CPUVCC_FLT

## Acoustics E-noise Components

EMC U7110.11:3MM C7118 1000PF 5% 25V CERM 0402

EMC U7110.11:3MM C7119 1000PF 5% 25V CERM 0402

CRITICAL C7110 180UF 20% 16V POLY TH1

CRITICAL C7111 180UF 20% 16V POLY TH1

CRITICAL C7112 10UF 20% 16V X6S-CERM 0603

CRITICAL C7113 10UF 20% 16V X6S-CERM 0603

EMC CRITICAL U7110.11:3MM C7114 1UF 10% 16V X6S-CERM 0402

EMC CRITICAL U7110.11:3MM C7115 1UF 10% 16V X6S-CERM 0402

REG_PHASE_CPUVCC1

CRITICAL L7110 230NH-10%-45A-0.00031OHM CTX01-SM

PPCPUVCC_S0_SENSE_1

NOSTUFF C7117 0.0022UF 10% 50V CERM 402

REG_SNUBBER_CPUVCC_1

NOSTUFF R7117 1 5% 1/8W MF-LF 805

CRITICAL R7110 0.0005 1% 1W MF 0612

PPCPUVCC_S0_REG (OUT 62 70)

REG_ISENVCC_1_P (OUT 61 83)

NO_XNET_CONNECTION=TRUE U7000.38:3MM

C7121 220PF 10% 50V X7R-CERM 0402

NO_XNET_CONNECTION=TRUE C7121.2:2MM

R7121 1.02K 1% 1/16W MF-LF 402

REG_ISENVCC_1_N — REG_ISENVCC_1_NR (OUT 61 83)

NO_XNET_CONNECTION=TRUE C7121.1:2MM

C7120 0.1UF 10% 16V X7R-CERM 0402

AGND_CPU 61 62 71 83

EMC U7130.11:3MM C7138 1000PF 5% 25V CERM 0402

EMC U7130.11:3MM C7139 1000PF 5% 25V CERM 0402

CRITICAL C7130 180UF 20% 16V POLY TH1

CRITICAL C7131 180UF 20% 16V POLY TH1

CRITICAL C7132 10UF 20% 16V X6S-CERM 0603

CRITICAL C7133 10UF 20% 16V X6S-CERM 0603

EMC CRITICAL U7130.11:3MM C7134 1UF 10% 16V X6S-CERM 0402

EMC CRITICAL U7130.11:3MM C7135 1UF 10% 16V X6S-CERM 0402

REG_PHASE_CPUVCC2

CRITICAL L7130 230NH-10%-45A-0.00031OHM CTX01-SM

PPCPUVCC_S0_SENSE_2

NOSTUFF C7137 0.0022UF 10% 50V CERM 402

REG_SNUBBER_CPUVCC_2

NOSTUFF R7137 1 5% 1/8W MF-LF 805

CRITICAL R7130 0.0005 1% 1W MF 0612

PPCPUVCC_S0_REG (OUT 62 70)

REG_ISENVCC_2_P (OUT 61 83)

NO_XNET_CONNECTION=TRUE U7000.34:3MM

C7141 220PF 10% 50V X7R-CERM 0402

NO_XNET_CONNECTION=TRUE C7141.2:2MM

R7141 1.02K 1% 1/16W MF-LF 402

REG_ISENVCC_2_N — REG_ISENVCC_2_NR (OUT 61 83)

NO_XNET_CONNECTION=TRUE C7141.1:2MM

C7140 0.1UF 10% 16V X7R-CERM 0402

AGND_CPU 61 62 71 83

EMC U7150.11:3MM C7158 1000PF 5% 25V CERM 0402

EMC U7150.11:3MM C7159 1000PF 5% 25V CERM 0402

CRITICAL C7150 180UF 20% 16V POLY TH1

CRITICAL C7151 180UF 20% 16V POLY TH1

CRITICAL C7152 10UF 20% 16V X6S-CERM 0603

CRITICAL C7153 10UF 20% 16V X6S-CERM 0603

EMC CRITICAL U7150.11:3MM C7154 1UF 10% 16V X6S-CERM 0402

EMC CRITICAL U7150.11:3MM C7155 1UF 10% 16V X6S-CERM 0402

REG_PHASE_CPUVCC3

CRITICAL L7150 230NH-10%-45A-0.00031OHM CTX01-SM

PPCPUVCC_S0_SENSE_3

NOSTUFF C7157 0.0022UF 10% 50V CERM 402

REG_SNUBBER_CPUVCC_3

NOSTUFF R7157 1 5% 1/8W MF-LF 805

CRITICAL R7150 0.0005 1% 1W MF 0612

PPCPUVCC_S0_REG (OUT 62 70)

REG_ISENVCC_3_P (OUT 61 83)

NO_XNET_CONNECTION=TRUE U7000.40:3MM

C7161 220PF 10% 50V X7R-CERM 0402

NO_XNET_CONNECTION=TRUE C7161.2:2MM

R7161 1.02K 1% 1/16W MF-LF 402

REG_ISENVCC_3_N — REG_ISENVCC_3_NR (OUT 61 83)

NO_XNET_CONNECTION=TRUE C7161.1:2MM

C7160 0.1UF 10% 16V X7R-CERM 0402

AGND_CPU 61 62 71 83

SYNC_MASTER=J16_ROSSANA SYNC_DATE=03/21/2013

PAGE TITLE: VReg CPU VCC Phases

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DRAWING NUMBER: 051-0164 SIZE: D

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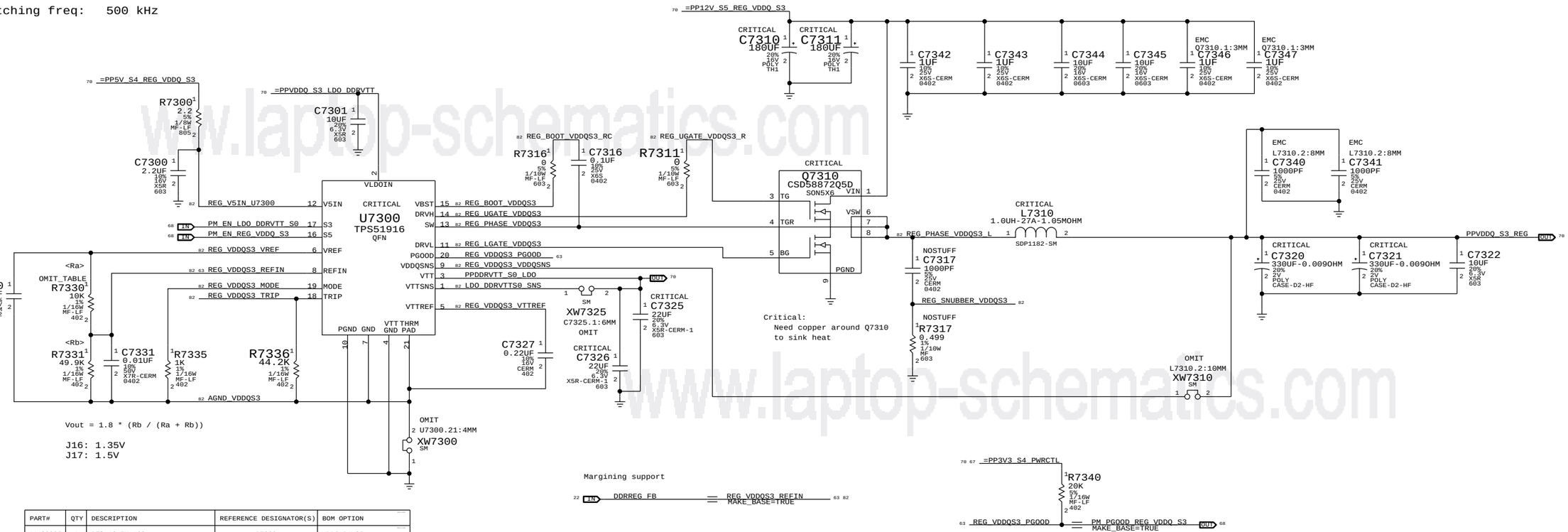
# VDDQ (1.5V / 1.35V) S3 Regulator

OC trip point: 30.4 A VDDQ = $\frac{R7336}{8\ E5\ *\ Rds(Q7310)} + \frac{0.65625}{L7310\ *\ f(switch)}$

3 A VTT (FIXED)
10 mA VTTREF (FIXED)

Switching freq: 500 kHz




| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 114S0335 | 1 | RES,16.5K,402 | R7330 | VDDQ:P1V35 |
| 114S0315 | 1 | RES,10K,402 | R7330 | VDDQ:P1V5 |

Margining support







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PAGE TITLE: VReg VDDQ S3

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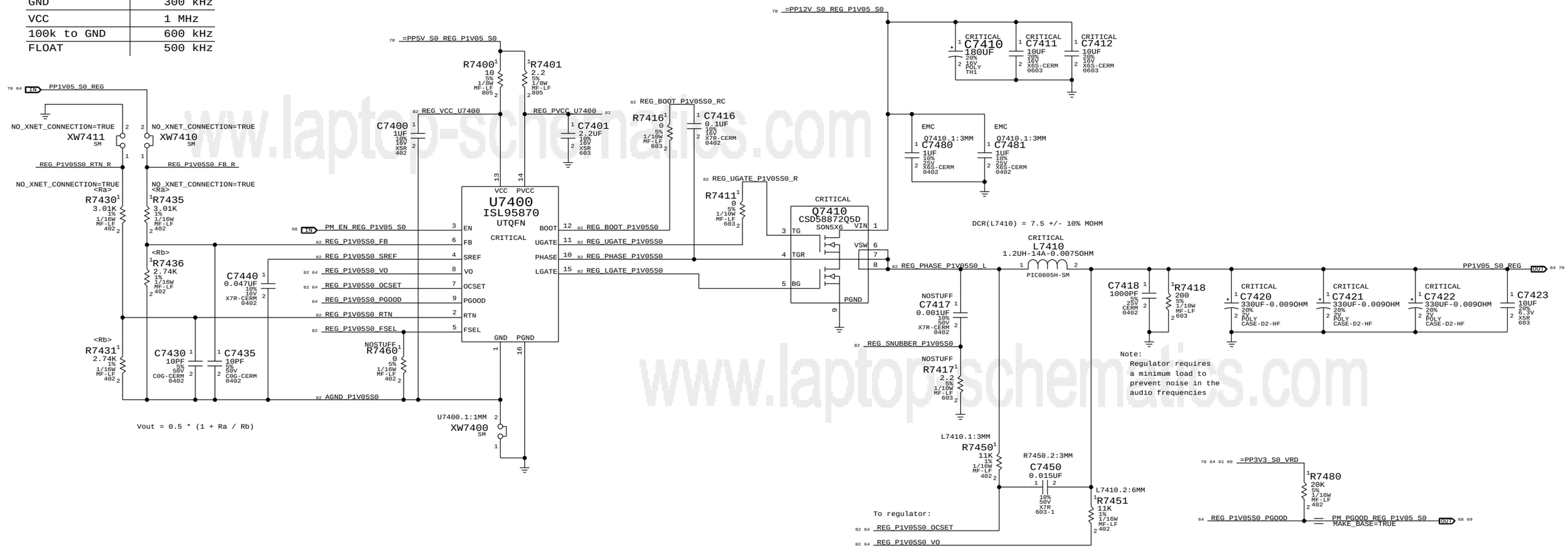
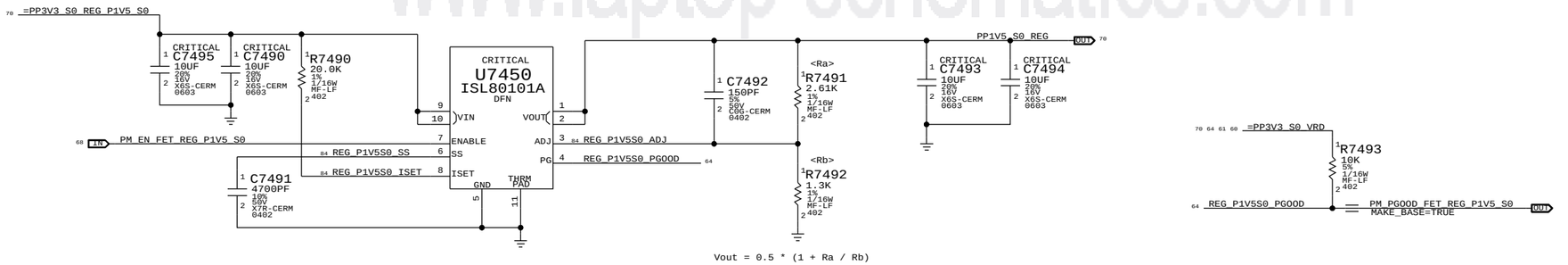
# PCH/TBT (1.05V) S0 REGULATOR

Switching freq: 500 kHz OC trip point: 12.4 A = $\frac{\text{R7450} * 8.5\ \text{E-6}}{\text{DCR(L7410)}}$

| FSEL STRAP | SW FREQ |
|---|---|
| GND | 300 kHz |
| VCC | 1 MHz |
| 100k to GND | 600 kHz |
| FLOAT | 500 kHz |




# 1.5V S0 REGULATOR

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PAGE TITLE: VREG 1V05 S0 / 1V5 S0

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## 3.3V S5 Regulator

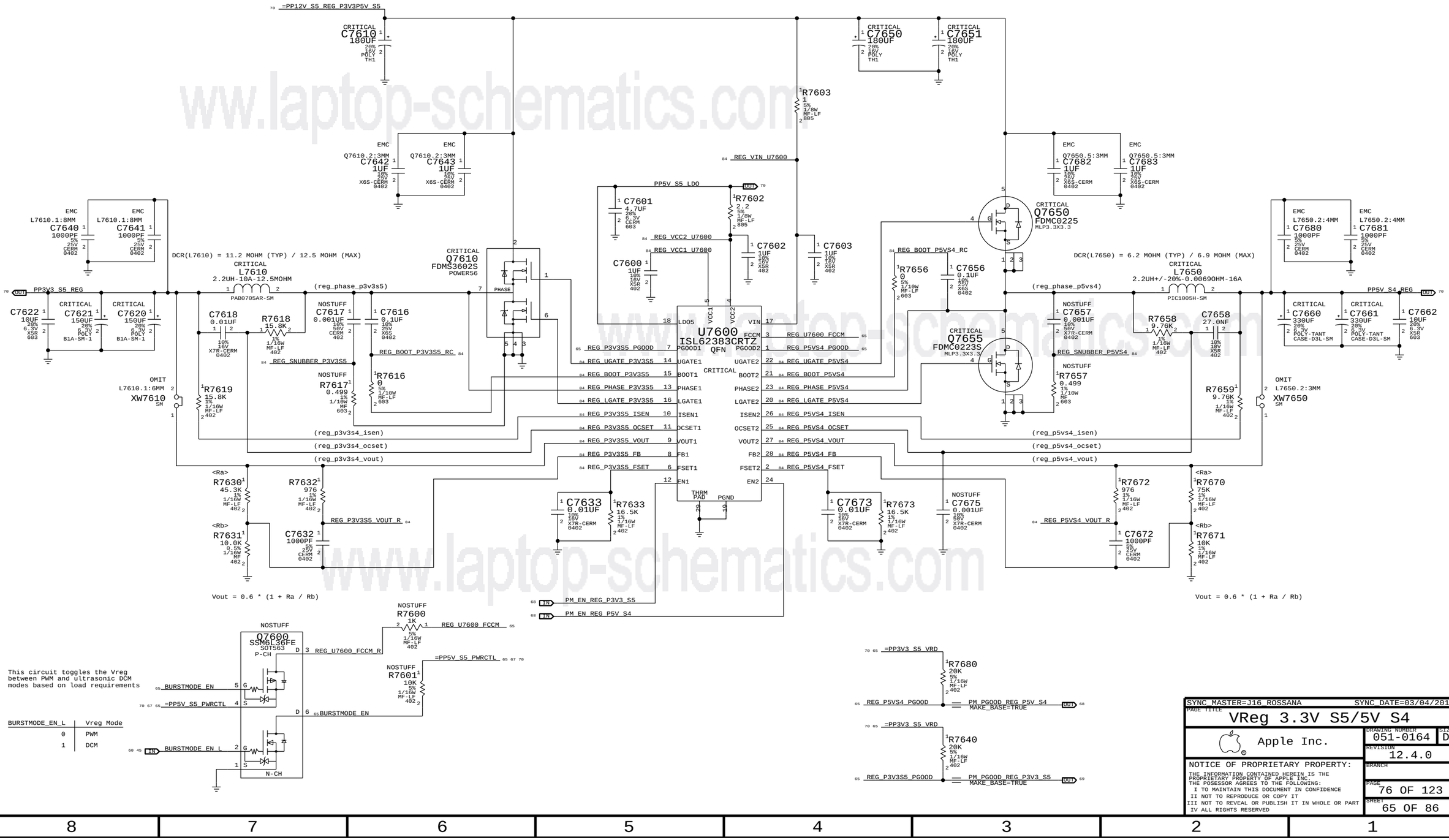
OC trip point: 12.5 A = $\frac{\text{R7618 * 10 E-6}}{\text{DCR(L7610)}}$

Switching freq: 356 kHz = $\frac{1}{\text{170 E-12 * R7633}}$

## 5V S4 Regulator

OC trip point: 14.1 A = $\frac{\text{R7658 * 10 E-6}}{\text{DCR(L7650)}}$

Switching freq: 356 kHz = $\frac{1}{\text{170 E-12 * R7673}}$

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PAGE TITLE: VReg 3.3V S5/5V S4

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| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 152S1668 | 1 | IND,PWR,33UH,20%,10A,35MOHM | L8100 | CRITICAL | |

OMIT/table L8100 due to late sourcing change, did not want footprint change
Add 152s1668 (Cyntec) directly for next program

OMIT_TABLE
CRITICAL
L8100
33UH-20%-10A-0.03510HM
THLB87A7GZ-IHLP4040DZ11-SM
NOSTUFF

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 371S0648 | 371S0694 | | D8100 | BLC Switch Diode |

ACOUSTICS E-NOISE COMPONENTS

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 138S0810 | 138S0745 | | 2.2UF_CAP | BLC OUTPUT CAPS |
| 138S0839 | 138S0745 | | 2.2UF_CAP | BLC OUTPUT CAPS |
| 371S0748 | 371S0731 | | D8101 | INPUT DIODE |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 376S1071 | 376S1073 | | ALL | Short Protection FET |
| 155S0831 | 155S0797 | | ALL | FB8100 to FB8107 |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 376S1121 | 376S1116 | | Q8102 | BLC Inrush FET |
| 740S0145 | 740S0146 | | F8100 | BLC Fuse |

SYNC_MASTER=J16_LINDA SYNC_DATE=01/22/2013

PAGE TITLE
LCD Backlight Driver (LP8561)

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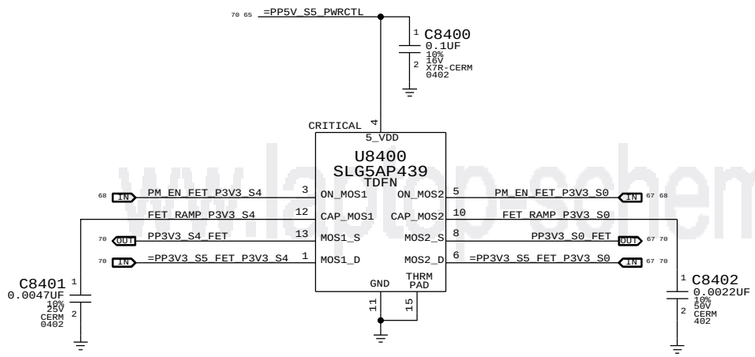
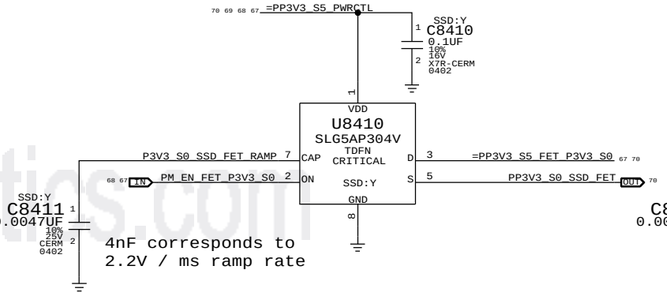
## 3.3V S4 FET



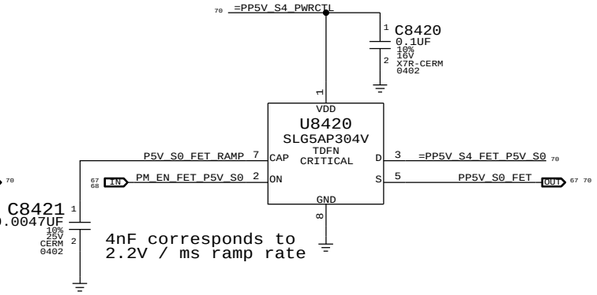

## 3.3V S0 FET



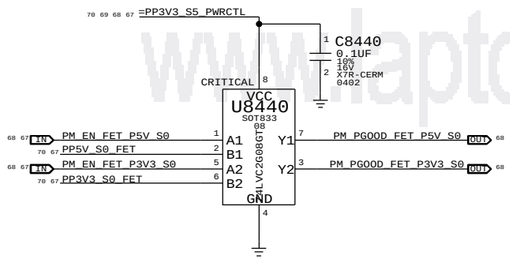

## 3V3 S0 SSD



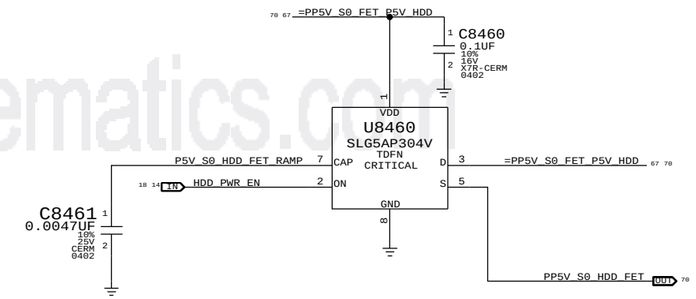

## 5V S0 FET



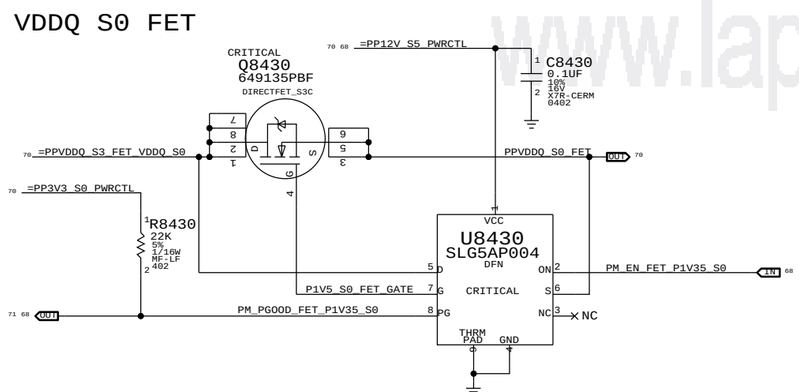

## 5V / 3V3 S0 PGOODs



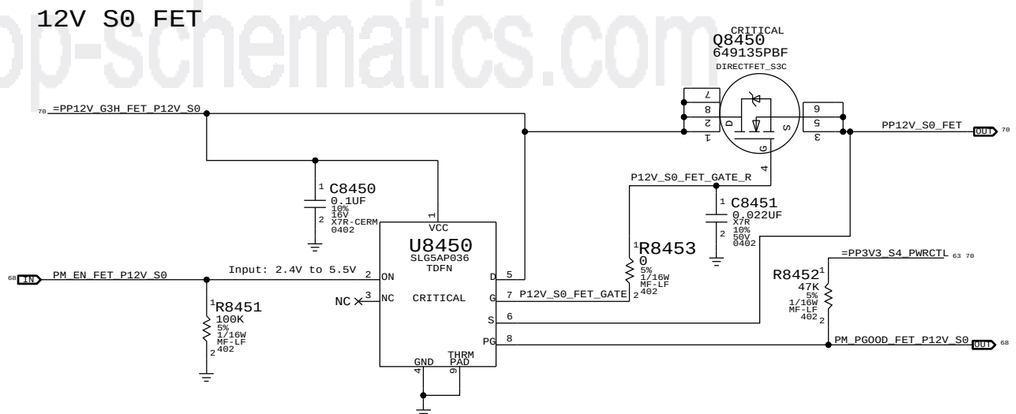

## 5V HDD FET




## VDDQ S0 FET




## 12V S0 FET




SYNC_MASTER=J16_MAX SYNC_DATE=02/11/2013

PAGE TITLE

# FET-Controlled S0 and S4

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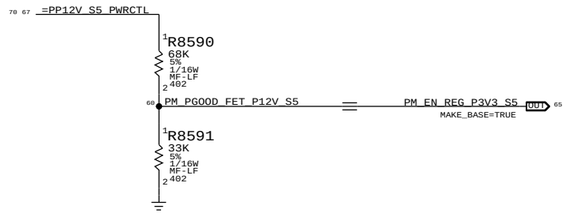
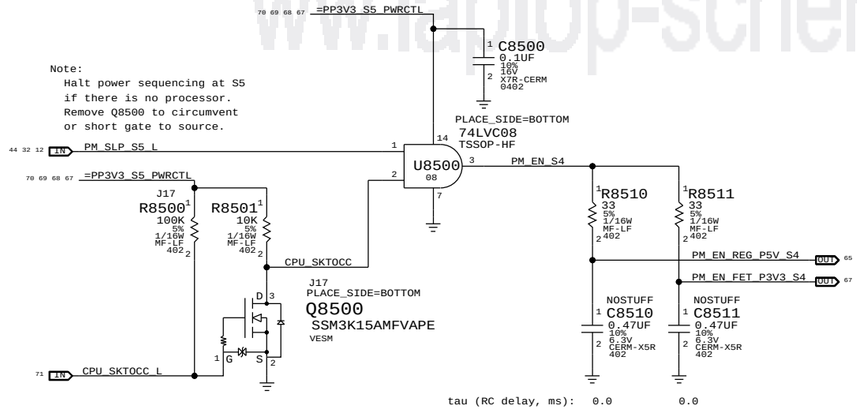
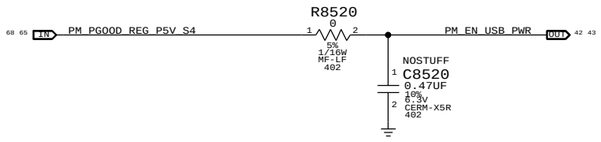
## S5 Enable




## S4 Enables

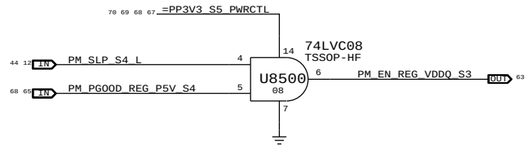



## S4 USB Enable

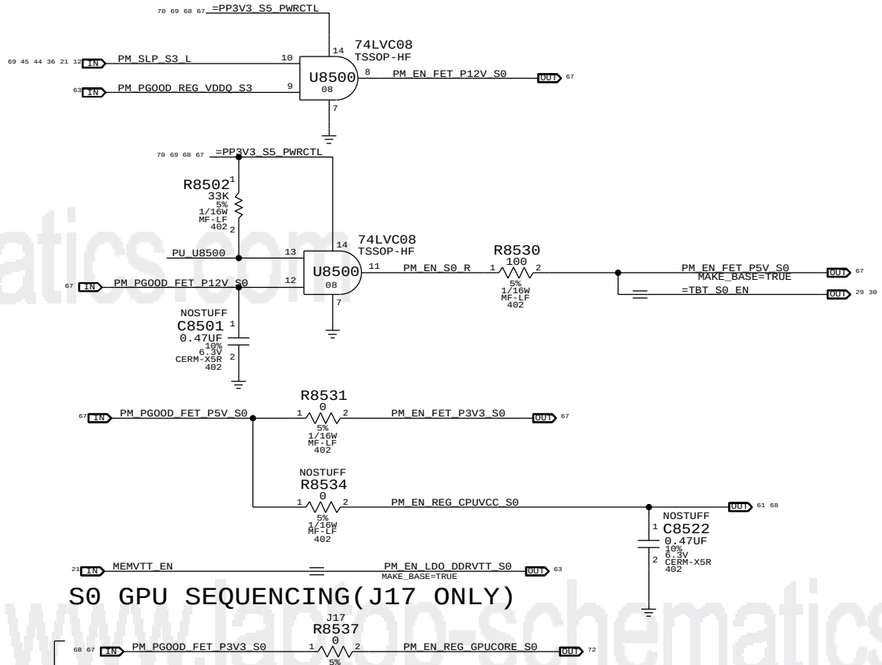



## S4 TBT S4 Port Enable

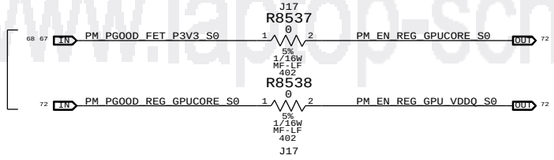
## S3 VDDQ Enable



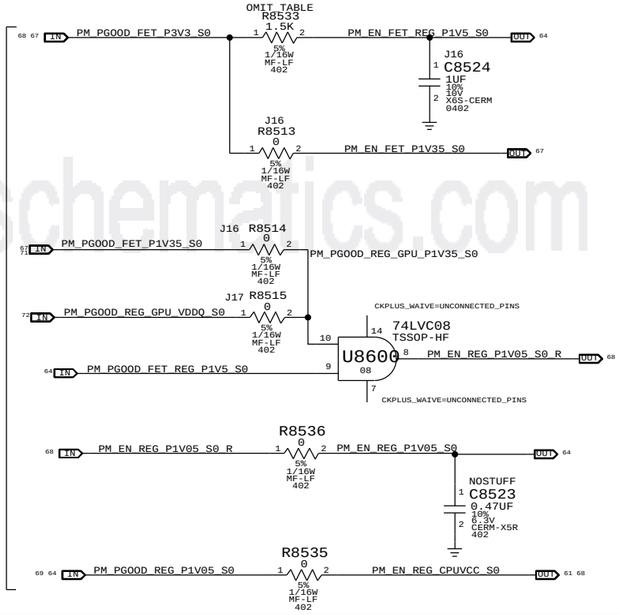

## S0 Enables




## S0 GPU SEQUENCING(J17 ONLY)




## S0 PCH Sequencing




| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 116S0070 | 1 | RES,1.5K,0402,5% | R8533 | J16 |
| 116S0004 | 1 | RES,0OHM,0402,5% | R8533 | J17 |

### Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.5 V, 1.05V for PCH/TBT/GPU)
Uncore: VDDQ

### Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. VCC3_3 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC3V3 ramping to 2.6V
4. VCC1_5 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC1V5 ramping to 1.35V
5. VCC may power down before VCC3_3, VCC3_3 must ramp down to 2.6V within 35ms
6. VCC may power down before VCC1_5, VCC1_5 must ramp down to 1.35V within 35ms

NVIDIA:
1. 3V3_S0 must ramp first
4. VDDQ MUST RAMP AFTER GPU_CORE
5. PEX_VDD with IFPC/D/E/F_IOVDD (1.05V) must ramp after VDDQ
6. All rails must reach their target voltages in more than 40 uS

SYNC_MASTER=J16_AARON SYNC_DATE=02/21/2013

PAGE TITLE
# PM Regulator Enables

Apple Inc.

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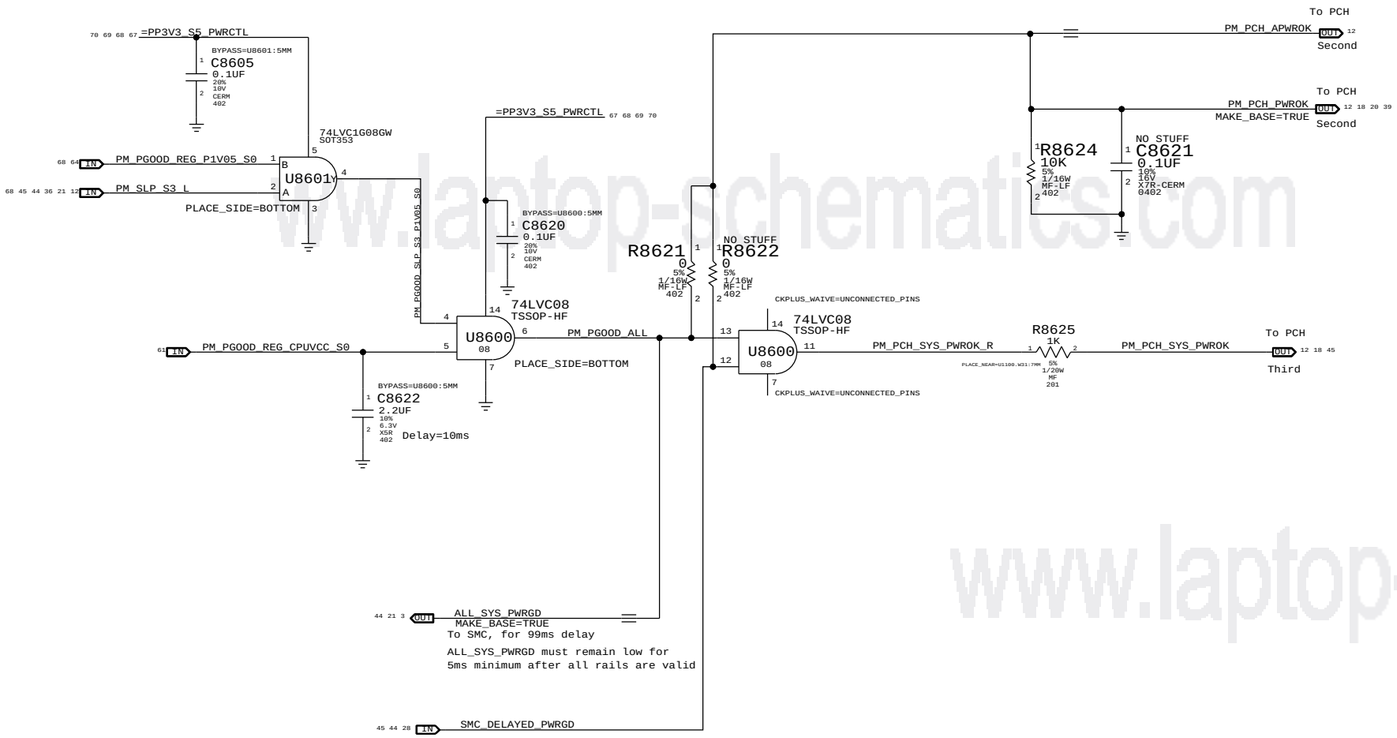
# ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation

## PCH Power Goods




## Resume Reset

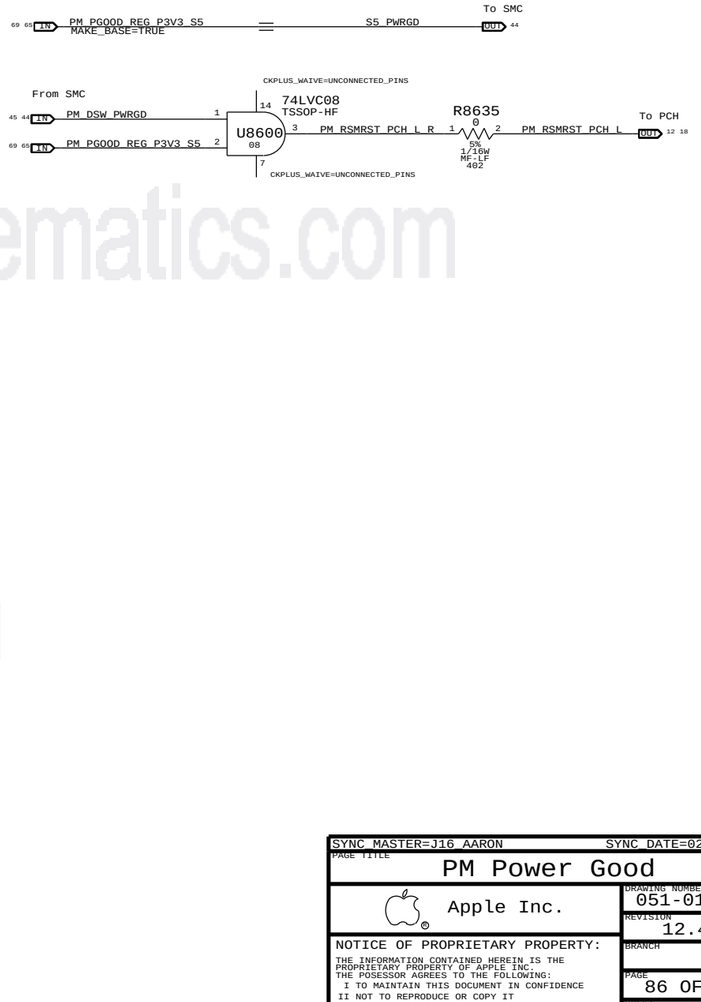
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
The iMac J16/J17 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.

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REVISION: 12.4.0
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## G3 Rails

Always on: Keeps the PCH RTC alive

84 PP3V3_G3 (MAKE_BASE=TRUE)
- PP3V3_G3_RTC — 19
- =PPVRTC_G3_PCH — 11 12 15

## G3H Rails

84 PP12V_ACDC (MAKE_BASE=TRUE)
- PP12V_G3H_ACDC — 60
- =PP12V_G3H_SNS_R — 48

84 PP12V_G3H (MAKE_BASE=TRUE)
- PP12V_G3H_SNS — 48
- =PP12V_G3H_REG_3V42_G3H — 60
- =PP12V_G3H_FET_P12V_S5 — 60
- =PP12V_G3H_FET_P12V_S0 — 67

84 PP3V42_G3H (MAKE_BASE=TRUE)
- PP3V42_G3H_REG — 60
- =PP3V3_G3H_BT — 32
- =PP3V3_G3H_SMC — 44 45 51
- =PP3V3_G3H_RTC_D — 19
- =PPVIN_G3H_SMCVREF — 45
- =PP3V3_G3H_SMC_USBMUX — 42
- =PP3V3_G3H_LPCPLUS — 46

## Ground/Common

GND (MAKE_BASE=TRUE)

## S5 Rails

Enabled when system has AC and is in S5

84 PP12V_S5 (MAKE_BASE=TRUE)
- PP12V_S5_FET — 60
- =PP12V_S5_REG_P3V3P5V_S5 — 65
- =PP12V_S5_REG_VDDQ_S3 — 63
- =PP12V_S5_PWRCTL — 67 68
- =PPHV_SW_TBTAPWRSW — 29
- =PPHV_SW_TBTBPWRSW — 30
- =PP12V_S5_SNS — 48

84 PP5V_S5 (MAKE_BASE=TRUE)
- PP5V_S5_LDO — 65
- =PP5V_S5_PWRCTL — 65 67

84 PP3V3_S5 (MAKE_BASE=TRUE)
- PP3V3_S5_REG — 65
- =PP3V3_S5_FET_P3V3_S4 — 67
- =PP3V3_S5_FET_P3V3_S0 — 67
- =PP3V3_S5_PWRCTL — 67 68 69
- =PP3V3_S5_VRD — 65
- =PP3V3_S5_LED — 3
- =PP3V3_SUS_PCH_VCCSUS_GPIO — 15 17
- =PP3V3_S5_PCH_VCCDSW — 15 17
- =PP3V3_SUS_PCH_VCC_SPI — 15 17
- =PP3V3R1V5_S0_PCH_VCCSUSHDA — 15 17
- =PP3V3_SUS_PCH_VCCSUS_USB — 15 17
- =PP3V3_SUS_PCH_VCCSUS_RTC — 15 17
- =PP3V3_SUS_PCH_VCCSUS_USB3 — 15
- =PP3V3_S5_PCH — 19 20
- =PP3V3_S5_ROM — 46
- =PP3V3_S5_SENSE — 48
- =PP3V3_S5_SMC — 45
- =PP3V3_S5_XDP — 18
- =PP3V3_S4_TBTAPWRSW — 29
- =PP3V3_S4_TBTBPWRSW — 30
- =PP3V3_S5_SNS — 49
- =PP3V3_SUS_PCH_GPIO — 11 12 13 14
- =PP3V3_S5_PCH_GPIO — 12

## S4 Rails

Enabled when system has AC and is in run or sleep

84 PP5V_S4 (MAKE_BASE=TRUE)
- PP5V_S4_REG — 65
- =PP5V_S4_REG_VDDQ_S3 — 63
- =PP5V_S4_FET_P5V_S0 — 67
- =PP5V_S4_MEMRESET — 21
- =PP5V_S4_PWRCTL — 67
- =PP5V_S4_USB — 42 43
- =PP5V_S4_CAMERA — 38

84 PP3V3_S4 (MAKE_BASE=TRUE)
- PP3V3_S4_FET — 67
- =PP3V3_S4_FET_ENET — 36
- =PP3V3_S4_PWRCTL — 63 67
- =PP3V3_S4_ALS — 38
- =PP3V3_S4_LED — 3
- =PP3V3_S4_MEMRESET — 21
- =PP3V3_S3RS4_PCH_GPIO — 13
- =PP3V3_S4_PM — 21
- =PP3V3_S4_SDCARD — 37
- =PP3V3_S4_SMC — 45
- =PP3V3_S4_SMBUS_SMC_2 — 47
- =PP3V3_S4_TBT — 26 27 28 29 30 68
- =PP3V3_S4_CAMERA — 38 39
- =PP3V3_S4_AUDIO_DIG — 56
- =PP3V3_S4_SNS_R — 48
- =PP3V3_S3_VREFMRGN — 22

84 PP3V3_S4_AP (MAKE_BASE=TRUE)
- PP3V3_S4_SNS — 48
- =PP3V3_S4_AP — 32 45

## S3 Rails

Enabled when system is in run or sleep

84 PP3V3_ENET (MAKE_BASE=TRUE)
- PP3V3_ENET_FET — 36
- =PP3V3_ENET_PHY — 35 36
- =PP3V3_ENET_SYSCLK — 19
- =PPVDDIO_ENET_CLK — 19

82 PPVDDQ_S3 (MAKE_BASE=TRUE)
- PPVDDQ_S3_REG — 63
- =PPVDDQ_S3_FET_VDDQ_S0 — 67
- =PPVDDQ_S3_SNS_DDR_R — 49

82 PPVDDQ_S3_DDR (MAKE_BASE=TRUE)
- PPVDDQ_S3_SNS_DDR — 49
- =PPVDDQ_S3_LDO_DDRVTT — 63
- =PPDDR_S3_MEMVREF — 22
- =PPVDDQ_S3_MEM_A — 23
- =PPVDDQ_S3_MEM_B — 24
- =PPVDDQ_S3_MEMRESET — 21

## S0 Rails

Enabled when system is in run

84 PP12V_S0 (MAKE_BASE=TRUE)
- PP12V_S0_FET — 67
- =PP12V_S0_REG_CPUVCC_S0 — 62
- =PP12V_S0_REG_P1V05_S0 — 64
- =PP12V_S0_AUDIO_SPKRAMP — 54 55
- =PP12V_S0_BKLT — 66
- =PP12V_S0_FAN — 51
- =PP12V_S0_LCD — 40

84 PP5V_S0 (MAKE_BASE=TRUE)
- PP5V_S0_FET — 67
- =PP5V_S0_REG_CPUVCC_S0 — 61 62
- =PP5V_S0_REG_P1V05_S0 — 64
- =PP5V_S0_AUDIO — 52 59
- =PP5V_S0_ISENSE — 48
- =PP5V_S0_LPCPLUS — 46
- =PP5V_S0_BKLT — 66
- =PP5V_S0_FET_P5V_HDD — 67

84 PPHDD_S0 (MAKE_BASE=TRUE)
- PP5V_S0_HDD_FET — 67
- =PPHDD_S0_SNS_R — 48

84 PP5V_S0_HDD (MAKE_BASE=TRUE)
- PPHDD_S0_SNS — 48
- =PP5V_S0_SATA — 34

84 PP3V3_S0 (MAKE_BASE=TRUE)
- PP3V3_S0_FET — 67
- =PP3V3_S0_P3V3TBTFET — 28
- =PP3V3_S0_PWRCTL — 67
- =PP3V3_S0_VRD — 60 61 64
- =PP3V3_S0_AUDIO — 38 52 54 55 58
- =PP3V3_S0_AUDIO_DIG — 56
- =PP3V3_S0_DP — 31 40 47
- =PP3V3_S0_ENET — 35
- =PP3V3_S0_FAN — 51
- =PP3V3_S0_INTDPMUX — 41
- =PP3V3_S0_LED — 3
- =PP3V3_S0_LED_SATA — 33
- =PP3V3_S0_PCH — 13 19
- =PP3V3_S0_PCH_VCC3_3_GPIO — 15 17
- =PP3V3_S0_PCH_VCC3_3_THRM — 15 17
- =PP3V3_S0_PCH_VCCCLK3_3 — 15 17
- =PP3V3_S0_PCH_VCC3_3_HVCMOS — 15 17
- =PP3V3_S0_PCH_VCC_FUSE — 15 17
- =PP3V3_S0_PCH_VCC3_3_USB — 15 17
- =PP3V3_S0_RSTBUF — 20
- =PP3V3_S0_SDCARD — 37
- =PP3V3_S0_SENSE — 34 48 49 50
- =PP3V3_S0_SMBUS — 47
- =PP3V3_S0_SMBUS_SMC_0 — 47
- =PP3V3_S0_SMBUS_SMC_1 — 47
- =PP3V3_S0_SMBUS_SMC_3 — 47
- =PP3V3_S0_SMC — 45
- =PP3V3_S0_TBTPWRCTL — 28
- =PP3V3_S0_BKLT_VDDIO — 66
- =PPSPD_S0_MEM_A — 23
- =PPSPD_S0_MEM_B — 24
- =PP3V3_S0_PCH_GPIO — 11 12 14 28
- =PP3V3_S0_REG_P1V5_S0 — 64

84 PP3V3_S0_SSD (MAKE_BASE=TRUE)
- PP3V3_S0_SSD_FET — 67
- =PPSSD_S0_SNS_R — 49

84 PPSSD_S0 (MAKE_BASE=TRUE)
- PPSSD_S0_SNS — 49
- =PP3V3_S0_SSD — 33

82 PPVDDQ_S0 (MAKE_BASE=TRUE)
- PPVDDQ_S0_FET — 67
- =PPVDDQ_S0_SNS_R — 49

82 PPVDDQ_S0_CPU (MAKE_BASE=TRUE)
- PPVDDQ_S0_SNS — 49
- =PP1V5_S3_CPU_VCCDDR — 6
- =PP1V5R1V35_S0_CPU — 8 10

84 PP1V5_S0 (MAKE_BASE=TRUE)
- PP1V5_S0_REG — 64
- =PP1V5_S0_SENSE — 34
- =PP1V5_S0_PCH_VCCVRM — 17
- =PP1V5_S0_PCH_RCOMP — 12 13
- =PP1V5_S0_PCH_SATA — 11
- =PP1V5_S0_PCH_CLK — 11 19
- =PP1V5_S0_AUD_DIG — 52

82 PPDDRVTT_S0 (MAKE_BASE=TRUE)
- PPDDRVTT_S0_LDO — 63
- =PPDDRVTT_S0_CLAMP — 21
- =PPDDRVTT_S0_MEM_A — 23
- =PPDDRVTT_S0_MEM_B — 24

82 PP1V05_S0 (MAKE_BASE=TRUE)
- PP1V05_S0_REG — 64
- =PP1V05_S0_P1V05TBTFET — 28
- =PP1V05_S0_PCH_VCC — 15 17
- =PP1V05_S0_PCH_VCCCLK_CLK100 — 15 17
- =PP1V05_S0M_PCH_VCCASW — 15 17
- =PP1V05_S0_PCH_VCC_CLK — 17
- =PP1V05_S0_PCH_VCCIO_FDI — 15 17
- =PP1V05_S0_PCH_VCCCLK_SSC — 15 17
- =PP1V05_S0_PCH_VCCUSBPLL — 15 17
- =PP1V05_S0_PCH_VCCIO — 15 17
- =PP1V05_S0_PCH_VCCCLK_SSC100 — 15 17
- =PP1V05_S0_PCH_VCCCLK_CLK135 — 15 17
- =PP1V05_S0_PCH_VCCIO_USB2 — 15 17
- =PP1V05_S0_PCH_VCCIO_GPIO — 15
- =PP1V05_S0_PCH_V_PROC_IO — 14 15 17
- =PP1V05_S0_SNS — 48
- =PP1V05_S0_SMC — 45
- =PP1V05_S0_XDP — 18

83 PPCPUVCC_S0_CPU (MAKE_BASE=TRUE)
- PPCPUVCC_S0_REG — 62
- =PPCPUVCC_S0_CPU — 48 61
- =PPVCC_S0_CPU — 6 8 10

## Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

84 PP3V3_TBTLC (MAKE_BASE=TRUE)
- =PP3V3_TBTLC_FET — 28
- =PP3V3_TBT_PCH_GPIO — 20
- =PP3V3_TBTLC_RTR — 26 27 28
- =PPVDDIO_TBT_CLK — 19

82 28 PP1V05_TBTLC (MAKE_BASE=TRUE)
- =PP1V05_TBTLC_FET — 28
- =PP1V05_TBTLC_RTR — 27

82 PP1V05_TBTCIO (MAKE_BASE=TRUE)
- =PP1V05_TBTCIO_FET — 28
- =PP1V05_TBTCIO_RTR — 27

SYNC_MASTER=J16_MAX SYNC_DATE=02/11/2013

PAGE TITLE: Power Aliases

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# Display Aliases

61 REG_ISENVCC_4_NR = AGND_CPU 61 62 83
MAKE_BASE=TRUE

## UNUSED CPU SOCKET

68 CPU_SKTOCC_L = CPU_SKTOCC_L_ALIAS
MAKE_BASE=TRUE

## MEMORY PGOOD

21 =PM_PGOOD_MEM_S0 = PM_PGOOD_FET_P1V35_S0 67 68
MAKE_BASE=TRUE

26 DP_TBTSNK0_HPD = TP_DP_IG_B_HPD 12
MAKE_BASE=TRUE

85 26 DP_TBTSNK0_ML_C_P<3..0> = TP_DP_IG_B_MLP<3..0> 5
MAKE_BASE=TRUE

85 26 DP_TBTSNK0_ML_C_N<3..0> = TP_DP_IG_B_MLN<3..0> 5
MAKE_BASE=TRUE

85 26 DP_TBTSNK0_AUXCH_C_P = TP_DP_IG_B_AUXCHP 12
MAKE_BASE=TRUE

85 26 DP_TBTSNK0_AUXCH_C_N = TP_DP_IG_B_AUXCHN 12
MAKE_BASE=TRUE

31 DP_TBTSNK0_DDC_DATA = TP_DP_IG_B_DDC_DATA 12
MAKE_BASE=TRUE

31 DP_TBTSNK0_DDC_CLK = TP_DP_IG_B_DDC_CLK 12
MAKE_BASE=TRUE

26 DP_TBTSNK1_HPD = TP_DP_IG_C_HPD 12
MAKE_BASE=TRUE

85 26 DP_TBTSNK1_ML_C_P<3..0> = TP_DP_IG_C_MLP<3..0> 5
MAKE_BASE=TRUE

85 26 DP_TBTSNK1_ML_C_N<3..0> = TP_DP_IG_C_MLN<3..0> 5
MAKE_BASE=TRUE

85 26 DP_TBTSNK1_AUXCH_C_P = TP_DP_IG_C_AUXCHP 12
MAKE_BASE=TRUE

85 26 DP_TBTSNK1_AUXCH_C_N = TP_DP_IG_C_AUXCHN 12
MAKE_BASE=TRUE

31 DP_TBTSNK1_DDC_DATA = TP_DP_IG_C_DDC_DATA 12
MAKE_BASE=TRUE

31 DP_TBTSNK1_DDC_CLK = TP_DP_IG_C_DDC_CLK 12
MAKE_BASE=TRUE

41 DP_INT_HPD = TP_DP_IG_D_HPD 12
MAKE_BASE=TRUE

85 41 DP_INT_ML_P<3..0> = TP_DP_IG_D_MLP<3..0> 5
MAKE_BASE=TRUE

85 41 DP_INT_ML_N<3..0> = TP_DP_IG_D_MLN<3..0> 5
MAKE_BASE=TRUE

41 DP_INT_DDC_DATA = TP_DP_IG_D_DDC_DATA 12
MAKE_BASE=TRUE

41 DP_INT_DDC_CLK = TP_DP_IG_D_DDC_CLK 12
MAKE_BASE=TRUE

85 41 DP_INT_AUX_P = TP_DP_IG_D_AUXCHP 12
MAKE_BASE=TRUE

85 41 DP_INT_AUX_N = TP_DP_IG_D_AUXCHN 12
MAKE_BASE=TRUE

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PAGE TITLE
Signal Aliases

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## CPU Reserved

78 18 6 CPU_CFG<15..12> — TP_CPU_CFG<15..12> (MAKE_BASE=TRUE)

## CPU Memory

75 MEM_A_CLK_N<2..3> — NC_MEM_A_CLKN<2..3> (MAKE_BASE=TRUE, NO_TEST=TRUE)
75 MEM_A_CLK_P<2..3> — NC_MEM_A_CLKP<2..3> (MAKE_BASE=TRUE, NO_TEST=TRUE)
75 MEM_A_CS_L<2..3> — NC_MEM_A_CS_L<2..3> (MAKE_BASE=TRUE, NO_TEST=TRUE)
75 MEM_A_CKE<2..3> — NC_MEM_A_CKE<2..3> (MAKE_BASE=TRUE, NO_TEST=TRUE)
75 MEM_B_CLK_N<2..3> — NC_MEM_B_CLKN<2..3> (MAKE_BASE=TRUE, NO_TEST=TRUE)
75 MEM_B_CLK_P<2..3> — NC_MEM_B_CLKP<2..3> (MAKE_BASE=TRUE, NO_TEST=TRUE)
75 MEM_B_CS_L<2..3> — NC_MEM_B_CS_L<2..3> (MAKE_BASE=TRUE, NO_TEST=TRUE)
75 MEM_B_CKE<2..3> — NC_MEM_B_CKE<2..3> (MAKE_BASE=TRUE, NO_TEST=TRUE)
75 MEM_A_ODT<2..3> — NC_MEM_A_ODT<2..3> (MAKE_BASE=TRUE, NO_TEST=TRUE)
75 MEM_B_ODT<2..3> — NC_MEM_B_ODT<2..3> (MAKE_BASE=TRUE, NO_TEST=TRUE)

## PCH GPIO

11 TP_PCH_GPIO64_CLKOUTFLEX0 — NC_PCH_GPIO64_CLKOUTFLEX0 (MAKE_BASE=TRUE, NO_TEST=TRUE)
11 TP_PCH_GPIO65_CLKOUTFLEX1 — NC_PCH_GPIO65_CLKOUTFLEX1 (MAKE_BASE=TRUE, NO_TEST=TRUE)
11 TP_PCH_GPIO66_CLKOUTFLEX2 — NC_PCH_GPIO66_CLKOUTFLEX2 (MAKE_BASE=TRUE, NO_TEST=TRUE)
11 TP_PCH_GPIO67_CLKOUTFLEX3 — NC_PCH_GPIO67_CLKOUTFLEX3 (MAKE_BASE=TRUE, NO_TEST=TRUE)

## UNUSED IG DISPLAY

5 TP_DP_IG_A_MLP<3..0> (MAKE_BASE=TRUE) — NC_DP_IG_A_MLP<3..0> (MAKE_BASE=TRUE, NO_TEST=TRUE)
5 TP_DP_IG_A_MLN<3..0> (MAKE_BASE=TRUE) — NC_DP_IG_A_MLN<3..0> (MAKE_BASE=TRUE, NO_TEST=TRUE)
5 TP_DP_IG_A_AUXCHP (MAKE_BASE=TRUE) — NC_DP_IG_A_AUXCHP (MAKE_BASE=TRUE, NO_TEST=TRUE)
5 TP_DP_IG_A_AUXCHN (MAKE_BASE=TRUE) — NC_DP_IG_A_AUXCHN (MAKE_BASE=TRUE, NO_TEST=TRUE)

## PCH PCI

13 TP_LPC_DREQ0_L — NC_LPC_DREQ0_L (MAKE_BASE=TRUE, NO_TEST=TRUE)

## PCH Miscellaneous

11 TP_HDA_SDIN1 — NC_HDA_SDIN1 (MAKE_BASE=TRUE, NO_TEST=TRUE)
11 TP_HDA_SDIN2 — NC_HDA_SDIN2 (MAKE_BASE=TRUE, NO_TEST=TRUE)
11 TP_HDA_SDIN3 — NC_HDA_SDIN3 (MAKE_BASE=TRUE, NO_TEST=TRUE)
11 TP_PCI_CLK33M_OUT2 — NC_PCI_CLK33M_OUT2 (MAKE_BASE=TRUE, NO_TEST=TRUE)
11 TP_PCI_CLK33M_OUT3 — NC_PCI_CLK33M_OUT3 (MAKE_BASE=TRUE, NO_TEST=TRUE)

## UNUSED GRAPHICS ALIASES

20 TP_GPU_RESET_L — NC_TP_GPU_RESET_L (MAKE_BASE=TRUE, NO_TEST=TRUE)

## UNUSED THUNDERBOLT ALIASES

26 TP_TBT_PCIE_RESET0_L — NC_TBT_PCIE_RESET0_L (MAKE_BASE=TRUE, NO_TEST=TRUE)
26 TP_TBT_PCIE_RESET1_L — NC_TBT_PCIE_RESET1_L (MAKE_BASE=TRUE, NO_TEST=TRUE)
26 TP_TBT_PCIE_RESET2_L — NC_TBT_PCIE_RESET2_L (MAKE_BASE=TRUE, NO_TEST=TRUE)
26 TP_TBT_PCIE_RESET3_L — NC_TBT_PCIE_RESET3_L (MAKE_BASE=TRUE, NO_TEST=TRUE)
26 TP_TBT_THERM_DP — NC_TBT_THERM_DP (MAKE_BASE=TRUE, NO_TEST=TRUE)

## UNUSED VREG ALIASES

61 REG_PWM_CPUVCC_4 — NC_REG_PWM_CPUVCC_4 (MAKE_BASE=TRUE, NO_TEST=TRUE)
61 REG_ISENVCC_4_P — NC_REG_ISENVCC_4P (MAKE_BASE=TRUE, NO_TEST=TRUE)

## UNUSED GPU ALIASES

68 PM_EN_REG_GPUCORE_S0 — NC_PM_EN_REG_GPUCORE_S0 (MAKE_BASE=TRUE, NO_TEST=TRUE)
68 PM_PGOOD_REG_GPUCORE_S0 — NC_PM_PGOOD_REG_GPUCORE_S0 (MAKE_BASE=TRUE, NO_TEST=TRUE)
68 PM_EN_REG_GPU_VDDQ_S0 — NC_PM_EN_REG_GPU_VDDQ_S0 (MAKE_BASE=TRUE, NO_TEST=TRUE)
68 PM_PGOOD_REG_GPU_VDDQ_S0 — NC_PM_PGOOD_REG_GPU_VDDQ_S0 (MAKE_BASE=TRUE, NO_TEST=TRUE)

## UNUSED PEG ALIASES

5 =PEG_D2R_P<0..15> — NC_PEG_D2R_P<0..15> (MAKE_BASE=TRUE, NO_TEST=TRUE)
5 =PEG_D2R_N<0..15> — NC_PEG_D2R_N<0..15> (MAKE_BASE=TRUE, NO_TEST=TRUE)
5 =PEG_R2D_C_P<0..15> — NC_PEG_R2D_C_P<0..15> (MAKE_BASE=TRUE, NO_TEST=TRUE)
5 =PEG_R2D_C_N<0..15> — NC_PEG_R2D_C_N<0..15> (MAKE_BASE=TRUE, NO_TEST=TRUE)

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PAGE TITLE: Unused Signal Aliases

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# J16 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

| BOARD LAYERS | BOARD AREAS | BOARD UNITS (MIL OF MM) | ALLEGRO VERSION |
|---|---|---|---|
| TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM | NO_TYPE,BGA | MM | 16.2 |

## General Physical Rule Definitions

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| DEFAULT | * | Y | 0.1 MM | =50_OHM_SE | 12.7 MM | 0 MM | 0 MM |
| STANDARD | * | Y | =DEFAULT | =DEFAULT | 12.7 MM | =DEFAULT | =DEFAULT |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 34_OHM_SE | * | Y | 0.215 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 34_OHM_SE | TOP,BOTTOM | Y | 0.215 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 39_OHM_SE | * | Y | 0.170 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 39_OHM_SE | TOP,BOTTOM | Y | 0.170 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 42_OHM_SE | * | Y | 0.145 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 42_OHM_SE | TOP,BOTTOM | Y | 0.145 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 45_OHM_SE | * | Y | 0.138 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 45_OHM_SE | TOP,BOTTOM | Y | 0.138 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 50_OHM_SE | * | Y | 0.110 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 50_OHM_SE | TOP,BOTTOM | Y | 0.110 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 55_OHM_SE | * | Y | 0.085 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 55_OHM_SE | TOP,BOTTOM | Y | 0.085 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 68_OHM_DIFF | * | Y | 0.180 MM | 0.085 MM | =STANDARD | 0.140 MM | 0.1 MM |
| 68_OHM_DIFF | TOP,BOTTOM | Y | 0.180 MM | 0.085 MM | =STANDARD | 0.140 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 80_OHM_DIFF | * | Y | 0.135 MM | 0.085 MM | =STANDARD | 0.160 MM | 0.1 MM |
| 80_OHM_DIFF | TOP,BOTTOM | Y | 0.135 MM | 0.085 MM | =STANDARD | 0.160 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 85_OHM_DIFF | * | Y | 0.125 MM | 0.085 MM | =STANDARD | 0.190 MM | 0.1 MM |
| 85_OHM_DIFF | TOP,BOTTOM | Y | 0.125 MM | 0.085 MM | =STANDARD | 0.190 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 90_OHM_DIFF | * | Y | 0.111 MM | 0.085 MM | =STANDARD | 0.200 MM | 0.1 MM |
| 90_OHM_DIFF | TOP,BOTTOM | Y | 0.111 MM | 0.085 MM | =STANDARD | 0.200 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 100_OHM_DIFF | * | Y | 0.089 MM | 0.085 MM | =STANDARD | 0.220 MM | 0.1 MM |
| 100_OHM_DIFF | TOP,BOTTOM | Y | 0.089 MM | 0.085 MM | =STANDARD | 0.220 MM | 0.1 MM |

## General Spacing Definitions

Default

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DEFAULT | * | 0.1 MM | ? |
| STANDARD | * | =DEFAULT | ? |

Fixed and Dielectric

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| 1:1_SPACING | * | 0.1 MM | ? |
| 1X_DIELECTRIC | * | 0.076 MM | ? |
| 1X_DIELECTRIC | TOP,BOTTOM | 0.071 MM | ? |

BGA

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| BGA_P1MM | * | =STANDARD | ? |

Power and Common

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| GND | * | =STANDARD | ? |
| GND_P2MM | * | =2:1_SPACING | 1000 |
| PWR_P2MM | * | =2:1_SPACING | 1100 |

## Board Stack-up

Finished board thickness: 1.58 mm

| | | | |
|---|---|---|---|
| | Top | Signal | 0.5 oz (Cu plated) |
| | | Prepreg | 0.071 mm |
| | 2 | Plane | 1 oz |
| | | Prepreg | 0.076 mm |
| | 3 | Signal | 0.5 oz |
| | | Prepreg | 0.435 mm |
| | 4 | Plane | 1 oz |
| | | Core | 0.127 mm |
| | 5 | Plane | 1 oz |
| | | Prepreg | 0.435 mm |
| | 6 | Signal | 0.5 oz |
| | | Prepreg | 0.076 mm |
| | 2 | Plane | 1 oz |
| | | Prepreg | 0.071 mm |
| | Btm | Signal | 0.5 oz (Cu plated) |

## BGA Area Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| * | * | BGA | BGA_P1MM |

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PAGE TITLE: J16 RULE DEFINITIONS

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# DDR3

## DDR3-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| DDR_34S | * | =34_OHM_SE | =34_OHM_SE | =34_OHM_SE | =34_OHM_SE | =STANDARD | =STANDARD |
| DDR_39S | * | =39_OHM_SE | =39_OHM_SE | =39_OHM_SE | =39_OHM_SE | =STANDARD | =STANDARD |
| DDR_42S | * | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | =STANDARD | =STANDARD |
| DDR_42S_D | * | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | 0.1016 MM | 0.1016 MM |
| DDR_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| DDR_68D | * | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF |
| DDR_COMP | * | Y | 0.305 MM | 0.105 MM | =STANDARD | =STANDARD | =STANDARD |

Minimum diff spacing is 4 mil
Table 4-5, Intel Doc# 486712

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| POWER_DDR_P4MM | * | Y | 0.400 MM | 0.100 MM | 3.0 MM | =STANDARD | =STANDARD |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| POWER_DDR | * | POWER_DDR_P4MM |
| DDR_CLK_PHY | * | DDR_68D |
| DDR_CTRL_PHY | * | DDR_39S |
| DDR_CMD_PHY | * | DDR_34S |
| DDR_DQ_PHY | * | DDR_42S |
| DDR_DQS_PHY | * | DDR_42S_D |
| DDR_COMP_PHY | * | DDR_COMP |

## DDR3 Power-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| POWER_DDR | * | =2:1_SPACING | ? |

## DDR3-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DDR_CLK_ISO | * | =5:1_SPACING | ? |
| DDR_CTRL_ISO | * | =3.5:1_SPACING | ? |
| DDR_CTRL2CTRL | * | =2.5:1_SPACING | ? |
| DDR_CMD_ISO | * | =3.5:1_SPACING | ? |
| DDR_CMD2CMD | * | =2:1_SPACING | ? |
| DDR_DATA_ISO | * | =3:1_SPACING | ? |
| DDR_DQ2DQ | * | =2:1_SPACING | 900 |
| DDR_DQ2DQS | * | =3:1_SPACING | ? |
| DDR_BL2BL | * | =3:1_SPACING | ? |
| DDR_CH2CH | * | =6.5:1_SPACING | ? |
| DDR_COMP_ISO | * | 0.381 MM | ? |

## Main Segment Min Spacing Rules (mils) (Shark Bay PDG, Intel Doc# 486712)

| Table | Trace | Design (diff) | Iso | Design | Comments |
|---|---|---|---|---|---|
| 4-2 | 4 | | 15 | 19.69 | CLK trace spacing controlled by =68_OHM_DIFF |
| 4-3 | 8 | 9.84 | 12 | 13.78 | |
| | | | | | |
| 4-4 | 6 | 7.87 | 12 | 13.78 | |
| | | | | | |
| 4-5 | 8.5 | 7.87 | 12 | 11.81 | DQ or DQS to other signals not in the same bytelane (but not ch) |
| | | | | | DQ to DQ in the same bytelane of the same channel |
| | | | 10 | 11.81 | DQ to DQS in the same bytelane of the same channel |
| | | | 12 | 11.81 | DQ or DQS in different bytelanes of the same channel |
| | | | 25 | 25.59 | DQ or DQS in different channels |
| | | | - | 25.59 | DDR3 to any other signal not DDR3 |

## Constraints

### Clocks: CK[3:0], CK#[3:0]

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| DDR_CLK | * | * | DDR_CLK_ISO |

### Control: CS#[3:0], CKE[3:0], ODT[3:0]

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| DDR_CTRL | * | * | DDR_CTRL_ISO |
| DDR_CTRL | DDR_CTRL | * | DDR_CTRL2CTRL |

### Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| DDR_CMD | * | * | DDR_CMD_ISO |
| DDR_CMD | DDR_CMD | * | DDR_CMD2CMD |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| DDR_COMP | * | * | DDR_COMP_ISO |

### Data: DQS[7:0], DQS#[7:0], DQ[63:0]

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET | |
|---|---|---|---|---|
| DDR_A_DQ_BYTE* | * | * | DDR_DATA_ISO | |
| DDR_A_DQS* | * | * | DDR_DATA_ISO | |
| DDR_B_DQ_BYTE* | * | * | DDR_DATA_ISO | |
| DDR_B_DQS* | * | * | DDR_DATA_ISO | |
| DDR_*_DQ_BYTE* | =SAME | * | DDR_DQ2DQ | See Note (3) |
| DDR_A_DQ_BYTE* | DDR_A_DQS* | * | DDR_DQ2DQS | See Note (1) |
| DDR_A_DQ_BYTE* | DDR_A_DQ_BYTE* | * | DDR_BL2BL | See Note (3) |
| DDR_B_DQ_BYTE* | DDR_B_DQS* | * | DDR_DQ2DQS | See Note (1) |
| DDR_B_DQ_BYTE* | DDR_B_DQ_BYTE* | * | DDR_BL2BL | |
| DDR_A_* | DDR_B_* | * | DDR_CH2CH | See Note (2) |

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

## DDR3

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| Channel A | | | | |
| [117] DDR_A_CLK0 | DDR_CLK_PHY | DDR_CLK | MEM_A_CLK_P<1..0> | 7 23 |
| [117] DDR_A_CLK0 | DDR_CLK_PHY | DDR_CLK | MEM_A_CLK_N<1..0> | 7 23 |
| [125] DDR_A_CLK1 | DDR_CLK_PHY | DDR_CLK | MEM_A_CLK_P<3..2> | 72 |
| [125] DDR_A_CLK1 | DDR_CLK_PHY | DDR_CLK | MEM_A_CLK_N<3..2> | 72 |
| [118] DDR_A_CTRL0 | DDR_CTRL_PHY | DDR_CTRL | MEM_A_CKE<1..0> | 7 23 |
| [118] DDR_A_CTRL0 | DDR_CTRL_PHY | DDR_CTRL | MEM_A_CS_L<1..0> | 7 23 |
| [118] DDR_A_CTRL0 | DDR_CTRL_PHY | DDR_CTRL | MEM_A_ODT<1..0> | 7 23 |
| [124] DDR_A_CTRL1 | DDR_CTRL_PHY | DDR_CTRL | MEM_A_CKE<3..2> | 72 |
| [124] DDR_A_CTRL1 | DDR_CTRL_PHY | DDR_CTRL | MEM_A_CS_L<3..2> | 72 |
| [124] DDR_A_CTRL1 | DDR_CTRL_PHY | DDR_CTRL | MEM_A_ODT<3..2> | 72 |
| [116] DDR_A_CMD | DDR_CMD_PHY | DDR_CMD | MEM_A_A<15..0> | 7 23 |
| [116] DDR_A_CMD | DDR_CMD_PHY | DDR_CMD | MEM_A_BA<2..0> | 7 23 |
| [116] DDR_A_CMD | DDR_CMD_PHY | DDR_CMD | MEM_A_RAS_L | 7 23 |
| [116] DDR_A_CMD | DDR_CMD_PHY | DDR_CMD | MEM_A_CAS_L | 7 23 |
| [116] DDR_A_CMD | DDR_CMD_PHY | DDR_CMD | MEM_A_WE_L | 7 23 |
| [119] DDR_A_DQ_BYTE0 | DDR_DQ_PHY | DDR_A_DQ_BYTE0 | MEM_A_DQ<7..0> | 7 25 |
| [119] DDR_A_DQ_BYTE1 | DDR_DQ_PHY | DDR_A_DQ_BYTE1 | MEM_A_DQ<15..8> | 7 25 |
| [119] DDR_A_DQ_BYTE2 | DDR_DQ_PHY | DDR_A_DQ_BYTE2 | MEM_A_DQ<23..16> | 7 25 |
| [119] DDR_A_DQ_BYTE3 | DDR_DQ_PHY | DDR_A_DQ_BYTE3 | MEM_A_DQ<31..24> | 7 25 |
| [119] DDR_A_DQ_BYTE4 | DDR_DQ_PHY | DDR_A_DQ_BYTE4 | MEM_A_DQ<39..32> | 7 25 |
| [119] DDR_A_DQ_BYTE5 | DDR_DQ_PHY | DDR_A_DQ_BYTE5 | MEM_A_DQ<47..40> | 7 25 |
| [119] DDR_A_DQ_BYTE6 | DDR_DQ_PHY | DDR_A_DQ_BYTE6 | MEM_A_DQ<55..48> | 7 25 |
| [119] DDR_A_DQ_BYTE7 | DDR_DQ_PHY | DDR_A_DQ_BYTE7 | MEM_A_DQ<63..56> | 7 25 |
| [120] DDR_A_DQS0 | DDR_DQS_PHY | DDR_A_DQS0 | MEM_A_DQS_P<0> | 7 25 |
| [120] DDR_A_DQS0 | DDR_DQS_PHY | DDR_A_DQS0 | MEM_A_DQS_N<0> | 7 25 |
| [120] DDR_A_DQS1 | DDR_DQS_PHY | DDR_A_DQS1 | MEM_A_DQS_P<1> | 7 25 |
| [120] DDR_A_DQS1 | DDR_DQS_PHY | DDR_A_DQS1 | MEM_A_DQS_N<1> | 7 25 |
| [120] DDR_A_DQS2 | DDR_DQS_PHY | DDR_A_DQS2 | MEM_A_DQS_P<2> | 7 25 |
| [120] DDR_A_DQS2 | DDR_DQS_PHY | DDR_A_DQS2 | MEM_A_DQS_N<2> | 7 25 |
| [120] DDR_A_DQS3 | DDR_DQS_PHY | DDR_A_DQS3 | MEM_A_DQS_P<3> | 7 25 |
| [120] DDR_A_DQS3 | DDR_DQS_PHY | DDR_A_DQS3 | MEM_A_DQS_N<3> | 7 25 |
| [120] DDR_A_DQS4 | DDR_DQS_PHY | DDR_A_DQS4 | MEM_A_DQS_P<4> | 7 25 |
| [120] DDR_A_DQS4 | DDR_DQS_PHY | DDR_A_DQS4 | MEM_A_DQS_N<4> | 7 25 |
| [120] DDR_A_DQS5 | DDR_DQS_PHY | DDR_A_DQS5 | MEM_A_DQS_P<5> | 7 25 |
| [120] DDR_A_DQS5 | DDR_DQS_PHY | DDR_A_DQS5 | MEM_A_DQS_N<5> | 7 25 |
| [120] DDR_A_DQS6 | DDR_DQS_PHY | DDR_A_DQS6 | MEM_A_DQS_P<6> | 7 25 |
| [120] DDR_A_DQS6 | DDR_DQS_PHY | DDR_A_DQS6 | MEM_A_DQS_N<6> | 7 25 |
| [121] DDR_A_DQS7 | DDR_DQS_PHY | DDR_A_DQS7 | MEM_A_DQS_P<7> | 7 25 |
| [121] DDR_A_DQS7 | DDR_DQS_PHY | DDR_A_DQS7 | MEM_A_DQS_N<7> | 7 25 |
| Channel B | | | | |
| [121] DDR_B_CLK0 | DDR_CLK_PHY | DDR_CLK | MEM_B_CLK_P<1..0> | 7 24 |
| [121] DDR_B_CLK0 | DDR_CLK_PHY | DDR_CLK | MEM_B_CLK_N<1..0> | 7 24 |
| [125] DDR_B_CLK1 | DDR_CLK_PHY | DDR_CLK | MEM_B_CLK_P<3..2> | 72 |
| [125] DDR_B_CLK1 | DDR_CLK_PHY | DDR_CLK | MEM_B_CLK_N<3..2> | 72 |
| [121] DDR_B_CTRL0 | DDR_CTRL_PHY | DDR_CTRL | MEM_B_CKE<1..0> | 7 24 |
| [121] DDR_B_CTRL0 | DDR_CTRL_PHY | DDR_CTRL | MEM_B_CS_L<1..0> | 7 24 |
| [121] DDR_B_CTRL0 | DDR_CTRL_PHY | DDR_CTRL | MEM_B_ODT<1..0> | 7 24 |
| [126] DDR_B_CTRL1 | DDR_CTRL_PHY | DDR_CTRL | MEM_B_CKE<3..2> | 72 |
| [126] DDR_B_CTRL1 | DDR_CTRL_PHY | DDR_CTRL | MEM_B_CS_L<3..2> | 72 |
| [126] DDR_B_CTRL1 | DDR_CTRL_PHY | DDR_CTRL | MEM_B_ODT<3..2> | 72 |
| [121] DDR_B_CMD | DDR_CMD_PHY | DDR_CMD | MEM_B_A<15..0> | 7 24 |
| [121] DDR_B_CMD | DDR_CMD_PHY | DDR_CMD | MEM_B_BA<2..0> | 7 24 |
| [121] DDR_B_CMD | DDR_CMD_PHY | DDR_CMD | MEM_B_RAS_L | 7 24 |
| [122] DDR_B_CMD | DDR_CMD_PHY | DDR_CMD | MEM_B_CAS_L | 7 24 |
| [122] DDR_B_CMD | DDR_CMD_PHY | DDR_CMD | MEM_B_WE_L | 7 24 |
| [122] DDR_B_DQ_BYTE0 | DDR_DQ_PHY | DDR_B_DQ_BYTE0 | MEM_B_DQ<7..0> | 7 25 |
| [122] DDR_B_DQ_BYTE1 | DDR_DQ_PHY | DDR_B_DQ_BYTE1 | MEM_B_DQ<15..8> | 7 25 |
| [122] DDR_B_DQ_BYTE2 | DDR_DQ_PHY | DDR_B_DQ_BYTE2 | MEM_B_DQ<23..16> | 7 25 |
| [122] DDR_B_DQ_BYTE3 | DDR_DQ_PHY | DDR_B_DQ_BYTE3 | MEM_B_DQ<31..24> | 7 25 |
| [122] DDR_B_DQ_BYTE4 | DDR_DQ_PHY | DDR_B_DQ_BYTE4 | MEM_B_DQ<39..32> | 7 25 |
| [122] DDR_B_DQ_BYTE5 | DDR_DQ_PHY | DDR_B_DQ_BYTE5 | MEM_B_DQ<47..40> | 7 25 |
| [122] DDR_B_DQ_BYTE6 | DDR_DQ_PHY | DDR_B_DQ_BYTE6 | MEM_B_DQ<55..48> | 7 25 |
| [122] DDR_B_DQ_BYTE7 | DDR_DQ_PHY | DDR_B_DQ_BYTE7 | MEM_B_DQ<63..56> | 7 25 |
| [123] DDR_B_DQS0 | DDR_DQS_PHY | DDR_B_DQS0 | MEM_B_DQS_P<0> | 7 25 |
| [123] DDR_B_DQS0 | DDR_DQS_PHY | DDR_B_DQS0 | MEM_B_DQS_N<0> | 7 25 |
| [123] DDR_B_DQS1 | DDR_DQS_PHY | DDR_B_DQS1 | MEM_B_DQS_P<1> | 7 25 |
| [123] DDR_B_DQS1 | DDR_DQS_PHY | DDR_B_DQS1 | MEM_B_DQS_N<1> | 7 25 |
| [123] DDR_B_DQS2 | DDR_DQS_PHY | DDR_B_DQS2 | MEM_B_DQS_P<2> | 7 25 |
| [123] DDR_B_DQS2 | DDR_DQS_PHY | DDR_B_DQS2 | MEM_B_DQS_N<2> | 7 25 |
| [123] DDR_B_DQS3 | DDR_DQS_PHY | DDR_B_DQS3 | MEM_B_DQS_P<3> | 7 25 |
| [123] DDR_B_DQS3 | DDR_DQS_PHY | DDR_B_DQS3 | MEM_B_DQS_N<3> | 7 25 |
| [123] DDR_B_DQS4 | DDR_DQS_PHY | DDR_B_DQS4 | MEM_B_DQS_P<4> | 7 25 |
| [123] DDR_B_DQS4 | DDR_DQS_PHY | DDR_B_DQS4 | MEM_B_DQS_N<4> | 7 25 |
| [124] DDR_B_DQS5 | DDR_DQS_PHY | DDR_B_DQS5 | MEM_B_DQS_P<5> | 7 25 |
| [124] DDR_B_DQS5 | DDR_DQS_PHY | DDR_B_DQS5 | MEM_B_DQS_N<5> | 7 25 |
| [124] DDR_B_DQS6 | DDR_DQS_PHY | DDR_B_DQS6 | MEM_B_DQS_P<6> | 7 25 |
| [124] DDR_B_DQS6 | DDR_DQS_PHY | DDR_B_DQS6 | MEM_B_DQS_N<6> | 7 25 |
| [124] DDR_B_DQS7 | DDR_DQS_PHY | DDR_B_DQS7 | MEM_B_DQS_P<7> | 7 25 |
| [124] DDR_B_DQS7 | DDR_DQS_PHY | DDR_B_DQS7 | MEM_B_DQS_N<7> | 7 25 |
| Reset | | | | |
| [124] | DDR_50S | | MEM_RESET_L | 21 23 24 |
| SM COMP | | | | |
| [126] | DDR_COMP_PHY | DDR_COMP | CPU_SM_RCOMP<0..2> | 6 |

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# PCI Express/DMI

## PCIe-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| PCIE_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |
| PCIE_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |
| PCIE_COMP | * | Y | 0.305 MM | 0.105 MM | =STANDARD | =STANDARD | =STANDARD |
| CPU_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| CLK_PCIE_PHY | * | PCIE_90D |
| COMP_PCIE_PHY | * | PCIE_COMP |
| CPU_ASYNC_PHY | * | CPU_50S |

## PCIe and DMI Compensation Rules (mils)

| Table | Imp | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 4-5 | 50 | 50 | 15 | 15.75 | PCIe. Impedance inferred from Table 4-7. |
| 4-7 | 50 | 50 | 8 | 15.75 | DMI. Numbers based on Intel stack-up. |

## PCIe-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CLK_PCIE_ISO | * | =5:1_SPACING | ? |
| COMP_PCIE_ISO | * | =4:1_SPACING | ? |
| CPU_ASYNC_ISO | * | =3:1_SPACING | ? |
| CPU_MS_ISO | TOP,BOTTOM | =4.5:1_SPACING | ? |
| CPU_MS_ISO | * | =3:1_SPACING | ? |

## Spacing Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| CLK_PCIE | * | * | CLK_PCIE_ISO |
| COMP_PCIE | * | * | COMP_PCIE_ISO |
| CPU_ASYNC | * | * | CPU_ASYNC_ISO |
| CPU_ASYNC_MS | * | * | CPU_MS_ISO |

## PEG Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

| Section | Imp | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 4.2.1 | 80 | 80 | 16 | 15.75 | PCIe Gen3. Allow looser spacing for same direction on stripline per Anil |

## CPU ASYNCHRONOUS

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| U67 | CPU_ASYNC_PHY | CPU_ASYNC | CPU_PROCHOT_L | 6 44 45 61 62 |
| U67 | CPU_ASYNC_PHY | CPU_ASYNC | CPU_PROCHOT_R_L | 6 |
| U67 PECI | CPU_ASYNC_PHY | CPU_ASYNC_MS | CPU_PECI | 6 14 44 45 |
| U67 | CPU_ASYNC_PHY | CPU_ASYNC_MS | SMC_PECI_L | 44 45 |
| U67 | CPU_ASYNC_PHY | CPU_ASYNC | CPU_CATERR_L | 6 45 |
| U67 | CPU_ASYNC_PHY | CPU_ASYNC | CPU_PWRGD | 6 14 18 |
| U67 | CPU_ASYNC_PHY | CPU_ASYNC | PM_SYNC | 6 12 |
| U68 | CPU_ASYNC_PHY | CPU_ASYNC | PM_THRMTRIP_L | 6 14 45 |
| U68 | CPU_ASYNC_PHY | CPU_ASYNC | CPU_RESET_L | 6 14 18 |
| U68 XDP_BPM_L | CPU_ASYNC_PHY | CPU_ASYNC | XDP_BPM_L<1..0> | 6 18 |

## PCIe (CPU)

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| CPU PCIe Compensation | | | | |
| U67 | COMP_PCIE_PHY | COMP_PCIE | CPU_PEG_RCOMP | 5 |
| CPU eDP Compensation | | | | |
| U67 | COMP_PCIE_PHY | COMP_PCIE | CPU_EDP_RCOMP | 5 |
| U67 | COMP_PCIE_PHY | COMP_PCIE | CPU_CFG_RCOMP | 6 |

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### Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| PCIE_PHY | * | PCIE_85D |
| COMP_DMI_PHY | * | DMI_COMP |

### PCIe-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| PCIE_SAME_DIR | TOP,BOTTOM | =5X_DIELECTRIC | ? |
| PCIE_SAME_DIR | * | =3.5X_DIELECTRIC | ? |
| PCIE_ALT_DIR | * | =7X_DIELECTRIC | ? |
| PCIE_ISO | * | =4:1_SPACING | ? |

### TBT x4 PCIE Spacing Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| PCIE_TBT_R2D | PCIE_TBT_R2D | * | PCIE_SAME_DIR |
| PCIE_TBT_D2R | PCIE_TBT_D2R | * | PCIE_SAME_DIR |
| PCIE_TBT_D2R | PCIE_TBT_R2D | * | PCIE_ALT_DIR |
| PCIE_TBT_D2R | * | * | PCIE_ISO |
| PCIE_TBT_R2D | * | * | PCIE_ISO |

### PCH x1 PCIE Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| PCIE | * | * | PCIE_ISO |

### DMI-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DMI_SAME_DIR | TOP,BOTTOM | =5X_DIELECTRIC | ? |
| DMI_SAME_DIR | * | =4X_DIELECTRIC | ? |
| DMI_ALT_DIR | * | =5X_DIELECTRIC | ? |
| DMI_ISO | * | =4X_DIELECTRIC | ? |

### DMI x4 PCIE Spacing Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| DMI_N2S | DMI_N2S | * | DMI_SAME_DIR |
| DMI_S2N | DMI_S2N | * | DMI_SAME_DIR |
| DMI_N2S | DMI_S2N | * | DMI_ALT_DIR |
| DMI_N2S | * | * | DMI_ISO |
| DMI_S2N | * | * | DMI_ISO |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| DMI_COMP | * | Y | 0.2032 MM | 0.2032 MM | 3 MM | =STANDARD | =STANDARD |

### PCIe (PCH)

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| x4 Thunderbolt | | | | |
| PCIE_GEN2_R2D | PCIE_PHY | PCIE_TBT_R2D | PCIE_TBT_R2D_P<3..0> | 26 |
| PCIE_GEN2_R2D | PCIE_PHY | PCIE_TBT_R2D | PCIE_TBT_R2D_N<3..0> | 26 |
| | PCIE_PHY | PCIE_TBT_R2D | PCIE_TBT_R2D_C_P<3..0> | 13 26 |
| | PCIE_PHY | PCIE_TBT_R2D | PCIE_TBT_R2D_C_N<3..0> | 13 26 |
| PCIE_GEN2_D2R | PCIE_PHY | PCIE_TBT_D2R | PCIE_TBT_D2R_P<3..0> | 13 26 |
| PCIE_GEN2_D2R | PCIE_PHY | PCIE_TBT_D2R | PCIE_TBT_D2R_N<3..0> | 13 26 |
| | PCIE_PHY | PCIE_TBT_D2R | PCIE_TBT_D2R_C_P<3..0> | 26 |
| | PCIE_PHY | PCIE_TBT_D2R | PCIE_TBT_D2R_C_N<3..0> | 26 |
| PCIE_REF_CLK_CONN | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_TBT_P | 11 26 |
| PCIE_REF_CLK_CONN | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_TBT_N | 11 26 |
| x1 AirPort | | | | |
| PCIE_GEN2_R2D_CONN_AP | PCIE_PHY | PCIE | PCIE_AP_R2D_P | 32 |
| PCIE_GEN2_R2D_CONN_AP | PCIE_PHY | PCIE | PCIE_AP_R2D_N | 32 |
| | PCIE_PHY | PCIE | PCIE_AP_R2D_C_P | 13 32 |
| | PCIE_PHY | PCIE | PCIE_AP_R2D_C_N | 13 32 |
| PCIE_GEN2_D2R_CONN_AP | PCIE_PHY | PCIE | PCIE_AP_D2R_P | 13 32 |
| PCIE_GEN2_D2R_CONN_AP | PCIE_PHY | PCIE | PCIE_AP_D2R_N | 13 32 |
| PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_AP_P | 11 32 |
| PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_AP_N | 11 32 |
| x1 Caesar IV | | | | |
| PCIE_GEN2_R2D | PCIE_PHY | PCIE | PCIE_ENET_R2D_P | 35 |
| PCIE_GEN2_R2D | PCIE_PHY | PCIE | PCIE_ENET_R2D_N | 35 |
| | PCIE_PHY | PCIE | PCIE_ENET_R2D_C_P | 13 35 |
| | PCIE_PHY | PCIE | PCIE_ENET_R2D_C_N | 13 35 |
| PCIE_GEN2_D2R | PCIE_PHY | PCIE | PCIE_ENET_D2R_P | 13 35 |
| PCIE_GEN2_D2R | PCIE_PHY | PCIE | PCIE_ENET_D2R_N | 13 35 |
| | PCIE_PHY | PCIE | PCIE_ENET_D2R_C_P | 35 |
| | PCIE_PHY | PCIE | PCIE_ENET_D2R_C_N | 35 |
| PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_ENET_P | 11 35 |
| PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_ENET_N | 11 35 |
| x2 SSD | | | | |
| PCIE_REF_CLK_CONN | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_SSD_P | 11 33 |
| PCIE_REF_CLK_CONN | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_SSD_N | 11 33 |
| PCH PCIE Compensation | | | | |
| | COMP_DMI_PHY | COMP_PCIE | PCH_PCIE_RCOMP | 13 |

### DMI

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| DMI | | | | |
| DMI_N2S | PCIE_PHY | DMI_N2S | DMI_N2S_P<3..0> | 5 12 |
| DMI_N2S | PCIE_PHY | DMI_N2S | DMI_N2S_N<3..0> | 5 12 |
| DMI_S2N | PCIE_PHY | DMI_S2N | DMI_S2N_P<3..0> | 5 12 |
| DMI_S2N | PCIE_PHY | DMI_S2N | DMI_S2N_N<3..0> | 5 12 |
| PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | DMI_CLK100M_CPU_P | 6 11 |
| PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | DMI_CLK100M_CPU_N | 6 11 |
| DMI Compensation | | | | |
| | COMP_DMI_PHY | COMP_PCIE | PCH_DMI_RCOMP | 12 |

### CPU DP REF CLK

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| CPU DP REF CLK | | | | |
| CPU_CLK135_PLL | PCIE_PHY | CLK_PCIE | CPU_CLK135M_DPLLREF_N | 6 11 |
| CPU_CLK135_PLL | PCIE_PHY | CLK_PCIE | CPU_CLK135M_DPLLREF_P | 6 11 |
| CPU_CLK135_PLL | PCIE_PHY | CLK_PCIE | CPU_CLK135M_DPLLSS_N | 6 11 |
| CPU_CLK135_PLL | PCIE_PHY | CLK_PCIE | CPU_CLK135M_DPLLSS_P | 6 11 |

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## SATA

### SATA-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SATA_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| SATA_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |
| SATA_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

### Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| SATA_PHY | * | SATA_85D |
| COMP_SATA_PHY | * | SATA_50S |
| SATA_PHY_90 | * | SATA_90D |

### SATA-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SATA_ISO | * | =6:1_SPACING | ? |
| COMP_SATA_ISO | * | =4:1_SPACING | ? |

### Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SATA | * | * | SATA_ISO |
| COMP_SATA | * | * | COMP_SATA_ISO |

### SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

| Section | Imp | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 15.2.1 | 90 | 95 | 20 | 23.62 | SATA Gen2, SATA Gen3 |

### SATA Compensation Rules (mils)

| Table | Imp | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 15-3 | 50 | 50 | 15 | 15.75 | SATA Gen2, SATA Gen3 |

## FDI

### FDI-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| FDI_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| COMP_FDI | * | Y | 0.25 MM | 0.25 MM | 3 MM | =STANDARD | =STANDARD |

### Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| FDI_SE_PHY | * | FDI_50S |
| COMP_FDI_PHY | * | COMP_FDI |

### FDI-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| FDI_ISO | * | =3:1_SPACING | ? |
| COMP_FDI_ISO | * | =4:1_SPACING | ? |

### Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| FDI | * | * | FDI_ISO |
| COMP_FDI | * | * | COMP_FDI_ISO |

### FDI Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

| Table | Imp | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 6-1/6-2 | 85 | 85 | 12 | 11.81 | FDI main length |

### FDI Compensation Rules (mils)

| Table | Trace | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 6-4 | 10 | 11.81 | - | 15.75 | Using PCIe guidelines |

## XDP

### XDP-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| XDP_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

### Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| XDP_PHY | * | XDP_55S |

### XDP-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| XDP_ISO | * | =2:1_SPACING | ? |
| CLK_JTAG_ISO | * | =4:1_SPACING | ? |

### Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| XDP | * | * | XDP_ISO |
| CLK_JTAG | * | * | CLK_JTAG_ISO |

### Desktop Debug Design Guide (Intel Doc# 430883)

| Section | Imp | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 1.5 | 45-65 | 55 | - | 15.75 | Isolation is for JTAG clocks.<br>All signals default are 50 Ohm SE. |

## SATA

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| PCH SATA Port 0 (HDD) | | | | |
| T90 SATA_R2D | SATA_PHY_90 | SATA | SATA_HDD_R2D_P | 33 |
| T92 SATA_R2D | SATA_PHY_90 | SATA | SATA_HDD_R2D_N | 33 |
| T89 | SATA_PHY_90 | SATA | SATA_HDD_R2D_C_P | 11 33 |
| T99 | SATA_PHY_90 | SATA | SATA_HDD_R2D_C_N | 11 33 |
| T94 SATA_D2R | SATA_PHY_90 | SATA | SATA_HDD_D2R_P | 11 33 |
| T95 SATA_D2R | SATA_PHY_90 | SATA | SATA_HDD_D2R_N | 11 33 |
| T91 | SATA_PHY_90 | SATA | SATA_HDD_D2R_C_P | 33 |
| T93 | SATA_PHY_90 | SATA | SATA_HDD_D2R_C_N | 33 |
| PCH SATA Port 1 (SSD) | | | | |
| T96 SATA_SSD_R2D | SATA_PHY | SATA | SSD_R2D_P<0..1> | 11 33 |
| T98 SATA_SSD_R2D | SATA_PHY | SATA | SSD_R2D_N<0..1> | 11 33 |
| T115 SATA_SSD_R2D | SATA_PHY | SATA | SSD_R2D_C_P<0..1> | 33 |
| T114 SATA_SSD_R2D | SATA_PHY | SATA | SSD_R2D_C_N<0..1> | 33 |
| T103 SATA_SSD_D2R | SATA_PHY | SATA | SSD_D2R_P<0..1> | 11 33 |
| T102 SATA_SSD_D2R | SATA_PHY | SATA | SSD_D2R_N<0..1> | 11 33 |
| PCH SATA Compensation | | | | |
| T104 | COMP_SATA_PHY | COMP_SATA | PCH_SATA_RCOMP | 11 |

## XDP

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| CPU XDP | | | | |
| T37 XDP_BPM_L | XDP_PHY | XDP | XDP_BPM_L<7..2> | 6 18 |
| T38 XDP_CPU_CFG | XDP_PHY | XDP | CPU_CFG<17..4> | 6 18 72 |
| T142 XDP_CPU_CFG_3 | XDP_PHY | XDP | CPU_CFG<3> | 6 18 |
| T143 XDP_CPU_CFG | XDP_PHY | XDP | CPU_CFG<2..0> | 6 18 |
| T45 | XDP_PHY | CLK_JTAG | XDP_CPU_TCK | 6 18 |
| T46 | XDP_PHY | XDP | XDP_CPU_TMS | 6 18 |
| T47 | XDP_PHY | XDP | XDP_CPU_TDI | 6 18 |
| T48 | XDP_PHY | XDP | XDP_CPU_TDO | 6 18 |
| PCH XDP | | | | |
| T49 | XDP_PHY | CLK_JTAG | XDP_PCH_TCK | 11 18 |
| T50 | XDP_PHY | XDP | XDP_PCH_TMS | 11 18 |
| T51 | XDP_PHY | XDP | XDP_PCH_TDI | 11 18 |
| T52 | XDP_PHY | XDP | XDP_PCH_TDO | 11 18 |

## FDI

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| FDI | | | | |
| T112 | FDI_SE_PHY | FDI | FDI_CSYNC | 5 12 |
| T113 | FDI_SE_PHY | FDI | FDI_INT | 5 12 |
| FDI Compensation | | | | |
| T116 | COMP_FDI_PHY | COMP_FDI | PCH_FDI_RCOMP | 12 |

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## PCH

### PCH-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| PCH_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| CLK_PCH_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

### PCH-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CLK_PCH | * | =4:1_SPACING | ? |
| COMP_PCH | * | =2:1_SPACING | ? |

## PCI

### PCI-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| CLK_PCI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

### PCI-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CLK_PCI | * | =2:1_SPACING | ? |

## LPC

### LPC-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| LPC_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| CLK_LPC_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

### LPC-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| LPC | * | =1.5:1_SPACING | ? |
| CLK_LPC | * | =2:1_SPACING | ? |

## HDA

### HDA-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| HDA_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

### HDA-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| HDA | * | =2x_DIELECTRIC | ? |

## Crystal

### Crystal-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| CLK_XTAL | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

### Crystal-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| XTAL | * | =4X_DIELECTRIC | ? |

## SPI

### SPI-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SPI_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| SPI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

### SPI-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SPI | * | =2:1_SPACING | ? |

## PCI

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| PCI Clock | | | | |
| H33 | CLK_PCI_55S | CLK_PCI | PCH_CLK33M_PCIIN | 11 19 |
| H32 | CLK_PCI_55S | CLK_PCI | PCH_CLK33M_PCIOUT | 11 19 |

## LPC

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| LPC | | | | |
| H38 | LPC_55S | LPC | LPC_AD<3..0> | 13 44 46 |
| H39 | LPC_55S | LPC | LPC_AD_R<3..0> | 13 |
| H33 | LPC_55S | LPC | LPC_FRAME_L | 13 44 46 |
| H37 | LPC_55S | LPC | LPC_FRAME_R_L | 13 |
| LPC Clocks | | | | |
| H36 | CLK_LPC_55S | CLK_LPC | LPC_CLK33M_LPCPLUS | 19 46 |
| H34 | CLK_LPC_55S | CLK_LPC | LPC_CLK33M_LPCPLUS_R | 11 19 |
| H41 | CLK_LPC_55S | CLK_LPC | LPC_CLK33M_SMC | 19 44 |
| H42 | CLK_LPC_55S | CLK_LPC | LPC_CLK33M_SMC_R | 11 19 |

## PCH Clocks

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| PCH Reference Clock | | | | |
| H48 | CLK_PCH_55S | CLK_PCH | SYSCLK_CLK25M_SB | 11 19 |
| H60 | CLK_PCH_55S | CLK_PCH | SYSCLK_CLK25M_SB_R | 11 |
| PCH RTC 32K | | | | |
| H44 | CLK_XTAL | XTAL | PCH_CLK32K_RTCX1 | 11 19 |
| H43 | CLK_XTAL | XTAL | PCH_CLK32K_RTCX2 | 11 19 |
| H52 | CLK_XTAL | XTAL | PCH_CLK32K_RTCX2_R | 19 |
| SMC 32K | | | | |
| H26 | CLK_PCH_55S | CLK_PCH | PM_CLK32K_SUSCLK_R | 12 45 |
| H58 | CLK_PCH_55S | CLK_PCH | SMC_CLK32K | 44 45 |

## 25 MHz Reference Clocks

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| 25M Reference Crystal | | | | |
| H27 | CLK_XTAL | XTAL | SYSCLK_CLK25M_X1 | 19 |
| H28 | CLK_XTAL | XTAL | SYSCLK_CLK25M_X2 | 19 |
| H29 | CLK_XTAL | XTAL | SYSCLK_CLK25M_X2_R | 19 |
| 25M Reference Clocks | | | | |
| H46 | CLK_PCH_55S | CLK_PCH | SYSCLK_CLK25M_ENET | 19 35 |
| H45 | CLK_PCH_55S | CLK_PCH | SYSCLK_CLK25M_ENET_R | 19 |
| H30 | CLK_PCH_55S | CLK_PCH | SYSCLK_CLK25M_TBT | 19 26 |
| H31 | CLK_PCH_55S | CLK_PCH | SYSCLK_CLK25M_TBT_R | 26 |

## HDA

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| HDA | | | | |
| H35 | HDA_55S | HDA | HDA_BIT_CLK | 11 52 |
| H40 | HDA_55S | HDA | HDA_BIT_CLK_R | 11 |
| H36 | HDA_55S | HDA | HDA_RST_L | 11 52 |
| H40 | HDA_55S | HDA | HDA_RST_R_L | 11 |
| H46 | HDA_55S | HDA | HDA_SDOUT | 11 52 |
| H67 | HDA_55S | HDA | HDA_SDOUT_R | 11 19 |
| H66 | HDA_55S | HDA | HDA_SYNC | 11 52 |
| H68 | HDA_55S | HDA | HDA_SYNC_R | 11 |
| H65 | HDA_55S | HDA | HDA_SDIN0 | 11 52 |
| H69 | HDA_55S | HDA | AUD_SDI_R | 52 |
| SPDIF | | | | |
| H27 | | HDA | AUD_SPDIF_CHIP | 52 |
| H71 | | HDA | AUD_SPDIF_OUT | 52 56 |

## SPI Bootrom

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| SPI ROM | | | | |
| H91 | SPI_50S | SPI | SPI_CLK_R | 13 46 |
| H92 | SPI_50S | SPI | SPI_CLK | 46 |
| H93 | SPI_50S | SPI | SPI_ALT_CLK | 46 |
| H40 | SPI_50S | SPI | SPI_SMC_CLK | 44 46 |
| H47 | SPI_50S | SPI | SPI_MLB_CLK | 46 |
| H95 | SPI_50S | SPI | SPI_CS0_R_L | 13 46 |
| H90 | SPI_50S | SPI | SPI_CS0_L | 46 |
| H96 | SPI_50S | SPI | SPI_ALT_CS_L | 46 |
| H40 | SPI_50S | SPI | SPI_SMC_CS_L | 44 46 |
| H97 | SPI_50S | SPI | SPI_MLB_CS_L | 46 |
| H98 | SPI_50S | SPI | SPI_MOSI_R | 13 46 |
| H46 | SPI_50S | SPI | SPI_MOSI | 46 |
| H41 | SPI_50S | SPI | SPI_ALT_MOSI | 46 |
| H43 | SPI_50S | SPI | SPI_SMC_MOSI | 44 46 |
| H44 | SPI_50S | SPI | SPI_MLB_MOSI | 46 |
| H40 | SPI_50S | SPI | SPI_MISO | 13 46 |
| H40 | SPI_50S | SPI | SPI_ALT_MISO | 46 |
| H42 | SPI_50S | SPI | SPI_SMC_MISO | 44 46 |
| H45 | SPI_50S | SPI | SPI_MLB_MISO | 46 |
| H40 | SPI_50S | SPI | SPIROM_USE_MLB | 14 46 |

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## USB

### USB-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| USB_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |
| USB_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

### Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| USB2_PHY | * | USB_90D |
| USB3_PHY | * | USB_85D |

### USB-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| USB2_ISO | * | =3:1_SPACING | ? |
| USB2_ISO | TOP,BOTTOM | =3:1_SPACING | ? |
| USB3_ISO | * | =5.5:1_SPACING | ? |
| USB3_ISO | TOP,BOTTOM | =5.5:1_SPACING | ? |

### USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

| Section | Imp | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 12.2.1 | 90 | 90 | 12 | 11.81 | USB 2.0 |
| 13.3.1 | 85 | 85 | 20 | 21.65 | USB 3.0 |

### Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| USB2 | * | * | USB2_ISO |
| USB3 | * | * | USB3_ISO |

## Caesar IV (Ethernet/SD)

### CIV-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| ENET_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| ENET_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |
| SD_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

### Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| ENET_COMP_PHY | * | ENET_50S |
| ENET_DIFF_PHY | * | ENET_100D |
| SD_PHY | * | SD_50S |
| CIV_SPI | * | SPI_55S |

### CIV-specific Spacing Definitions
Ethernet

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| ENET_DIFF_ISO | * | =6:1_SPACING | ? |
| ENET_DIFF2DIFF | * | =3:1_SPACING | ? |
| ENET_TRANS_ISO | * | 1.27 MM | ? |
| COMP_ENET_ISO | * | =4:1_SPACING | ? |

SD

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SD_ISO | * | =3:1_SPACING | ? |

### Constraints
Ethernet

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| ENET_DIFF | * | * | ENET_DIFF_ISO |
| ENET_DIFF | ENET_DIFF | * | ENET_DIFF2DIFF |
| ENET_TRANS | * | * | ENET_TRANS_ISO |
| COMP_ENET | * | * | COMP_ENET_ISO |
| ENET_TRANS | ENET_TRANS | * | ENET_DIFF2DIFF |

2 kV isolation

SD

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SD | * | * | SD_ISO |

## Camera Processor-to-Camera Sensor I/F (SMIA/MIPI)

### Camera Processor's SMIA Interface Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SMIA_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| SMIA_DIFF_PHY | * | SMIA_100D |

### Camera Processor's SMIA Interface Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SMIA_DIFF_ISO | * | =6:1_SPACING | ? |
| SMIA_DIFF2DIFF | * | =3:1_SPACING | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SMIA_DIFF | * | * | SMIA_DIFF_ISO |
| SMIA_DIFF | SMIA_DIFF | * | SMIA_DIFF2DIFF |

## USB 3.0 and USB 2.0 Trixies Muxing

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| **External Port A (J4600)** | | | | |
| J42 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTA_RX_P | 42 |
| J42 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTA_RX_N | 42 |
| J42 | USB3_PHY | USB3 | USB3_EXTA_RX_F_P | 13 42 |
| J42 | USB3_PHY | USB3 | USB3_EXTA_RX_F_N | 13 42 |
| J41 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTA_TX_P | 13 42 |
| J41 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTA_TX_N | 13 42 |
| J41 | USB3_PHY | USB3 | USB3_EXTA_TX_F_P | 42 |
| J41 | USB3_PHY | USB3 | USB3_EXTA_TX_F_N | 42 |
| J48 | USB3_PHY | USB3 | USB3_EXTA_TX_C_P | 42 |
| J48 | USB3_PHY | USB3 | USB3_EXTA_TX_C_N | 42 |
| J41 USB2_MUXED_MOJO_CONN | USB2_PHY | USB2 | USB_EXTA_0_P | 13 42 |
| J41 USB2_MUXED_MOJO_CONN | USB2_PHY | USB2 | USB_EXTA_0_N | 13 42 |
| J41 | USB2_PHY | USB2 | USB2_EXTA_MUXED_P | 42 |
| J42 | USB2_PHY | USB2 | USB2_EXTA_MUXED_N | 42 |
| J39 | USB2_PHY | USB2 | USB2_EXTA_P | 42 |
| J39 | USB2_PHY | USB2 | USB2_EXTA_N | 42 |
| **External Port B (J4610)** | | | | |
| J42 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTB_RX_P | 42 |
| J42 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTB_RX_N | 42 |
| J42 | USB3_PHY | USB3 | USB3_EXTB_RX_F_P | 13 42 |
| J42 | USB3_PHY | USB3 | USB3_EXTB_RX_F_N | 13 42 |
| J42 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTB_TX_P | 13 42 |
| J42 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTB_TX_N | 13 42 |
| J42 | USB3_PHY | USB3 | USB3_EXTB_TX_F_P | 42 |
| J42 | USB3_PHY | USB3 | USB3_EXTB_TX_F_N | 42 |
| J49 | USB3_PHY | USB3 | USB3_EXTB_TX_C_P | 42 |
| J49 | USB3_PHY | USB3 | USB3_EXTB_TX_C_N | 42 |
| J43 USB2_CONN | USB2_PHY | USB2 | USB_EXTB_8_P | 13 42 |
| J43 USB2_CONN | USB2_PHY | USB2 | USB_EXTB_8_N | 13 42 |
| J43 | USB2_PHY | USB2 | USB2_EXTB_P | 42 |
| J43 | USB2_PHY | USB2 | USB2_EXTB_N | 42 |
| **External Port C (J4700)** | | | | |
| J43 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTC_RX_P | 43 |
| J43 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTC_RX_N | 43 |
| J43 | USB3_PHY | USB3 | USB3_EXTC_RX_F_P | 13 43 |
| J44 | USB3_PHY | USB3 | USB3_EXTC_RX_F_N | 13 43 |
| J44 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTC_TX_P | 13 43 |
| J44 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTC_TX_N | 13 43 |
| J44 | USB3_PHY | USB3 | USB3_EXTC_TX_F_P | 43 |
| J44 | USB3_PHY | USB3 | USB3_EXTC_TX_F_N | 43 |
| J49 | USB3_PHY | USB3 | USB3_EXTC_TX_C_P | 43 |
| J49 | USB3_PHY | USB3 | USB3_EXTC_TX_C_N | 43 |
| J44 USB2_CONN | USB2_PHY | USB2 | USB_EXTC_1_P | 13 43 |
| J44 USB2_CONN | USB2_PHY | USB2 | USB_EXTC_1_N | 13 43 |
| J49 | USB2_PHY | USB2 | USB2_EXTC_P | 43 |
| J49 | USB2_PHY | USB2 | USB2_EXTC_N | 43 |
| **External Port D (J4710)** | | | | |
| J45 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTD_RX_P | 43 |
| J45 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTD_RX_N | 43 |
| J45 | USB3_PHY | USB3 | USB3_EXTD_RX_F_P | 13 43 |
| J45 | USB3_PHY | USB3 | USB3_EXTD_RX_F_N | 13 43 |
| J45 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTD_TX_P | 13 43 |
| J45 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTD_TX_N | 13 43 |
| J46 | USB3_PHY | USB3 | USB3_EXTD_TX_F_P | 43 |
| J46 | USB3_PHY | USB3 | USB3_EXTD_TX_F_N | 43 |
| J49 | USB3_PHY | USB3 | USB3_EXTD_TX_C_P | 43 |
| J49 | USB3_PHY | USB3 | USB3_EXTD_TX_C_N | 43 |
| J46 USB2_CONN | USB2_PHY | USB2 | USB_EXTD_9_P | 13 43 |
| J46 USB2_CONN | USB2_PHY | USB2 | USB_EXTD_9_N | 13 43 |
| J46 | USB2_PHY | USB2 | USB2_EXTD_P | 43 |
| J46 | USB2_PHY | USB2 | USB2_EXTD_N | 43 |
| **Camera (J3510)** | | | | |
| J42 USB2_CONN_TNT | USB2_PHY | USB2 | USB_CAMERA_P | 13 38 |
| J52 USB2_CONN_TNT | USB2_PHY | USB2 | USB_CAMERA_N | 13 38 |
| **PCH USB Compensation** | | | | |
| J48 | PCH_55S | COMP_PCH | PCH_USB_RBIAS | 13 |

## RMH Love

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| J49 USB2_MUXED_BT | USB2_PHY | USB2 | USB_BT_P | 13 32 |
| J41 USB2_MUXED_BT | USB2_PHY | USB2 | USB_BT_N | 13 32 |
| J50 USB2_MUXED_BT | USB2_PHY | USB2 | USB_BT_MUX_P | 32 |
| J50 USB2_MUXED_BT | USB2_PHY | USB2 | USB_BT_MUX_N | 32 |

## Et tu Brute?

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| **Ethernet** | | | | |
| J47 ENET_MDI | ENET_DIFF_PHY | ENET_DIFF | ENETCONN_MDI_P<3..0> | 35 36 |
| J47 ENET_MDI | ENET_DIFF_PHY | ENET_DIFF | ENETCONN_MDI_N<3..0> | 35 36 |
| J47 | ENET_DIFF_PHY | ENET_TRANS | ENETCONN_MDI_T_P<3..0> | 36 |
| J47 | ENET_DIFF_PHY | ENET_TRANS | ENETCONN_MDI_T_N<3..0> | 36 |
| J51 | | ENET_TRANS | ENETCONN_MCT0 | 36 |
| J52 | | ENET_TRANS | ENETCONN_MCT1 | 36 |
| J52 | | ENET_TRANS | ENETCONN_MCT2 | 36 |
| J52 | | ENET_TRANS | ENETCONN_MCT3 | 36 |
| J52 | | ENET_TRANS | ENETCONN_MCT_BS | 36 |
| J47 | ENET_COMP_PHY | COMP_ENET | ENET_RDAC | 35 |
| **SD** | | | | |
| J47 SD_DATA | SD_PHY | SD | ENET_CR_DATA<7..0> | 35 |
| J48 | SD_PHY | SD | SDCONN_DATA<7..0> | 35 37 |
| J48 SD_CMD | SD_PHY | SD | ENET_SD_CMD | 35 |
| J48 | SD_PHY | SD | SDCONN_CMD | 35 37 |
| J51 | SD_PHY | SD | SDCONN_CMD_R | |
| J48 SD_CLK | SD_PHY | SD | ENET_SD_CLK | 35 |
| J48 | SD_PHY | SD | SDCONN_CLK | 35 37 |
| J48 | SD_PHY | SD | SDCONN_CLK_R | 37 |
| J48 | SD_PHY | SD | ENET_MEDIA_SENSE | 11 35 |
| J48 | SD_PHY | SD | ENET_SD_DETECT_L | 35 37 |
| **CIV SPI** | | | | |
| J49 | CIV_SPI | SPI | ENET_SCLK | 35 |
| J48 | CIV_SPI | SPI | ENET_MISO | 35 |
| J49 | CIV_SPI | SPI | ENET_MOSI | 35 |
| J49 | CIV_SPI | SPI | ENET_CS_L | 35 |

## Camera Processor-Camera Sensor I/F

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| J50 SMIA_DP | SMIA_DIFF_PHY | SMIA_DIFF | SMIA_DATA_P | 38 |
| J50 SMIA_DP | SMIA_DIFF_PHY | SMIA_DIFF | SMIA_DATA_N | 38 |
| J50 SMIA_DP | SMIA_DIFF_PHY | SMIA_DIFF | SMIA_CLK_P | 38 |
| J50 SMIA_DP | SMIA_DIFF_PHY | SMIA_DIFF | SMIA_CLK_N | 38 |
| J50 | SPI_50S | SPI | CAM_SF_CLK | 38 |
| J50 | SPI_50S | SPI | CAM_SF_CLK_R | 38 |
| J50 | SPI_50S | SPI | CAM_SF_DIN | 38 |
| J51 | SPI_50S | SPI | CAM_SF_DIN_R | 38 |
| J51 | SPI_50S | SPI | CAM_SF_CS_L | 38 |
| J51 | SPI_50S | SPI | CAM_SF_WP_L | 38 |
| J51 | SPI_50S | SPI | CAM_SF_DOUT | 38 |
| J51 | SPI_50S | SPI | CAM_SF_DOUT_R | 38 |
| J51 | SMB_PHY | SMB | I2C_CAMSENSOR_SDA | 38 |
| J51 | SMB_PHY | SMB | I2C_CAMSENSOR_SCL | 38 |

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## SMBus

### SMBus-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SMB_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

### Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| SMB_PHY | * | SMB_55S |

### SMBus-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SMB_ISO | * | =2x_DIELECTRIC | ? |

### Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SMB | * | * | SMB_ISO |

## Sensor

### Sensor-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 1:1_DIFFPAIR | * | Y | =STANDARD | =STANDARD | =STANDARD | 0.1 MM | 0.085 MM |

### Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| SNS_DIFF_PHY | * | 1:1_DIFFPAIR |

### Sensor-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SENSE_ISO | * | =1.5:1_SPACING | ? |

### Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SENSE | * | * | SENSE_ISO |
| SENSE | POWER | * | PWR_P2MM |
| SENSE | GND | * | GND_P2MM |

## SMC Generic Control Line Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SMC_ISO | * | =1:1_SPACING | ? |

### Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SMC_CTRL | * | * | SMC_ISO |

## SMC Generic Control Line Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SMC_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

### Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| SMC_GEN | * | SMC_50S |

## Current/Voltage Sense

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| **Common** | | | | |
| I3 | | SENSE | GND_SMC_AVSS | 44 45 48 49 |
| **12V S5 (System Total)** | | | | |
| I4 SNS_CURRENT | SNS_DIFF_PHY | SENSE | SNS_P12VG3H_P | 48 |
| I5 SNS_CURRENT | SNS_DIFF_PHY | SENSE | SNS_P12VG3H_N | 48 |
| I6 | | SENSE | ISNS_P12VG3H_R | 48 |
| I7 | | SENSE | ISNS_P12VG3H | 45 48 |
| I8 | | SENSE | VSNS_P12VG3H | 45 48 |
| **HDD** | | | | |
| I80 SNS_CURRENT | SNS_DIFF_PHY | SENSE | SNS_HDD_P | 48 |
| I82 SNS_CURRENT | SNS_DIFF_PHY | SENSE | SNS_HDD_N | 48 |
| I81 | | SENSE | ISNS_HDDS0_R | 48 |
| I83 | | SENSE | ISNS_HDDS0 | 45 48 |
| I84 | | SENSE | VSNS_HDDS0 | 45 48 |
| **SSD** | | | | |
| I85 SNS_CURRENT | SNS_DIFF_PHY | SENSE | SNS_SSD_P | 49 |
| I87 SNS_CURRENT | SNS_DIFF_PHY | SENSE | SNS_SSD_N | 49 |
| I86 | | SENSE | ISNS_SSDS0_R | 49 |
| I88 | | SENSE | ISNS_SSDS0 | 45 49 |
| I89 | | SENSE | VSNS_P3V3S5 | 45 49 |
| **VDDQ S3 (DDR)** | | | | |
| I33 SNS_CURRENT | SNS_DIFF_PHY | SENSE | SNS_VDDQS3_DDR_P | 49 |
| I32 SNS_CURRENT | SNS_DIFF_PHY | SENSE | SNS_VDDQS3_DDR_N | 49 |
| I35 | | SENSE | ISNS_VDDQS3_DDR_R | 49 |
| I34 | | SENSE | ISNS_VDDQS3_DDR | 45 49 |
| I36 | | SENSE | VSNS_VDDQS3_DDR | 45 49 |
| **CPU Core** | | | | |
| I42 SNS_CURRENT | SNS_DIFF_PHY | SENSE | REG_CPUVCC_IMON_R | 48 |
| I43 SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNS_CPUVCC_FB_R | 48 |
| I44 | | SENSE | ISNS_CPUVCC_FB | 48 |
| I45 | | SENSE | ISNS_CPUVCC | 45 48 |
| I46 | | SENSE | VSNS_CPUVCC | 45 48 |
| **PP1V05_S0_PCH** | | | | |
| I510 | | SENSE | VSNS_P1V05S0_PCH | 45 48 |
| **PP1V5_S0** | | | | |
| I511 SNS_CURRENT | SNS_DIFF_PHY | SENSE | SNS_PVDDQS0_P | 49 |
| I512 SNS_CURRENT | SNS_DIFF_PHY | SENSE | SNS_PVDDQS0_N | 49 |
| I513 | | SENSE | ISNS_PVDDQS0_R | 49 |
| I514 | | SENSE | ISNS_PVDDQS0 | 45 49 |
| I515 | | SENSE | VSNS_PVDDQS0 | 45 49 |
| **Airport** | | | | |
| I105 SNS_CURRENT | SNS_DIFF_PHY | SENSE | SNS_P3V3S4_AP_P | 48 |
| I107 SNS_CURRENT | SNS_DIFF_PHY | SENSE | SNS_P3V3S4_AP_N | 48 |
| I106 | | SENSE | ISNS_P3V3S4_AP_R | 48 |
| I108 | | SENSE | ISNS_P3V3S4_AP | 45 48 |

## SMC

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| **SMC** | | | | |
| I1 | CLK_XTAL | XTAL | SMC_XTAL | 44 45 |
| I2 | CLK_XTAL | XTAL | SMC_EXTAL | 44 45 |
| I91 | SMC_GEN | SMC_CTRL | SMC_LRESET_L | 20 44 |
| I90 | SMC_GEN | SMC_CTRL | SMC_RUNTIME_SCI_L | 14 44 |
| I92 | SMC_GEN | SMC_CTRL | SMC_WAKE_SCI_L | 14 44 |
| I93 | SMC_GEN | SMC_CTRL | SMC_FAN_0_CTL | 44 51 |
| I94 | SMC_GEN | SMC_CTRL | SMC_FAN_0_TACH | 44 51 |

## SMBus

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| **SMC** | | | | |
| I10 | SMB_PHY | SMB | SMBUS_SMC_0_S0_SCL | 44 47 |
| I9 | SMB_PHY | SMB | SMBUS_SMC_0_S0_SDA | 44 47 |
| I11 | SMB_PHY | SMB | SMBUS_SMC_1_S0_SCL | 44 47 |
| I12 | SMB_PHY | SMB | SMBUS_SMC_1_S0_SDA | 44 47 |
| I13 | SMB_PHY | SMB | SMBUS_SMC_2_S4_SCL | 44 47 |
| I14 | SMB_PHY | SMB | SMBUS_SMC_2_S4_SDA | 44 47 |
| I15 | SMB_PHY | SMB | SMBUS_SMC_3_SCL | 44 47 |
| I16 | SMB_PHY | SMB | SMBUS_SMC_3_SDA | 44 47 |
| I19 | SMB_PHY | SMB | SMBUS_SMC_5_G3H_SCL | 44 45 |
| I20 | SMB_PHY | SMB | SMBUS_SMC_5_G3H_SDA | 44 45 |
| **PCH** | | | | |
| I21 | TBT_I2C_5SS | TBT_I2C | SMBUS_PCH_CLK | 13 47 |
| I52 | TBT_I2C_5SS | TBT_I2C | SMBUS_PCH_DATA | 13 47 |
| I53 | SMB_PHY | SMB | SML_PCH_0_CLK | 13 47 |
| I54 | SMB_PHY | SMB | SML_PCH_0_DATA | 13 47 |
| **Display TCon** | | | | |
| I55 | SMB_PHY | SMB | SMB_DP_TCON_SCL | 40 47 |
| I56 | SMB_PHY | SMB | SMB_DP_TCON_SDA | 40 47 |

## Temperature Sense

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| **EMC1414-1 (Production)** | | | | |
| I67 SNS_TEMP | SNS_DIFF_PHY | SENSE | SNS_T1_1_P | 50 |
| I68 SNS_TEMP | SNS_DIFF_PHY | SENSE | SNS_T1_1_N | 50 |
| I69 SNS_TEMP | SNS_DIFF_PHY | SENSE | SNS_T1_3_P | 50 |
| I60 SNS_TEMP | SNS_DIFF_PHY | SENSE | SNS_T1_3_N | 50 |
| I65 SNS_TEMP | SNS_DIFF_PHY | SENSE | SNS_ACDC_P | 50 60 |
| I66 SNS_TEMP | SNS_DIFF_PHY | SENSE | SNS_ACDC_N | 50 60 |
| I42 | SNS_DIFF_PHY | SENSE | SNS_T1_2_P | 50 |
| I43 | SNS_DIFF_PHY | SENSE | SNS_T1_2_N | 50 |
| **TMP423 (Development)** | | | | |
| I67 SNS_TEMP | SNS_DIFF_PHY | SENSE | SNS_T2_1_P | 50 |
| I68 SNS_TEMP | SNS_DIFF_PHY | SENSE | SNS_T2_1_N | 50 |
| I69 SNS_TEMP | SNS_DIFF_PHY | SENSE | SNS_T2_2_P | 50 |
| I70 SNS_TEMP | SNS_DIFF_PHY | SENSE | SNS_T2_2_N | 50 |
| I71 SNS_TEMP | SNS_DIFF_PHY | SENSE | SNS_T2_3_P | 50 |
| I72 SNS_TEMP | SNS_DIFF_PHY | SENSE | SNS_T2_3_N | 50 |
| **HDD Out-of-Band** | | | | |
| I73 | | SENSE | HDD_OOB1_D2R_L | 34 |
| I74 | | SENSE | HDD_OOB1_D2R_F_L | 34 |
| I75 | | SENSE | HDD_OOB1_D2R_R_L | 34 |
| I11 | | SENSE | SMC_OOB1_D2R_L | 34 44 |
| I76 | | SENSE | SMC_OOB1_R2D_L | 34 44 |
| I110 | | SENSE | SMC_OOB1_R2D_R_L | 34 |
| **SSD Out-of-Band** | | | | |
| I77 | | SENSE | SMC_OOB2_R2D_L | 33 45 |
| I78 | | SENSE | SMC_OOB2_D2R_L | 33 45 |

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# DC-DC

## Power-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| GND_P3MM | * | Y | 0.300 MM | 0.150 MM | 12.7 MM | =STANDARD | =STANDARD |
| GND_P5MM | * | Y | 0.500 MM | 0.150 MM | 12.7 MM | =STANDARD | =STANDARD |
| POWER_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| POWER_P3MM | * | Y | 0.300 MM | 0.150 MM | 12.7 MM | =STANDARD | =STANDARD |
| POWER_P6MM | * | Y | 0.600 MM | 0.150 MM | 12.7 MM | =STANDARD | =STANDARD |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| GND | * | GND_P5MM |
| GND | BGA | GND_P3MM |
| POWER | * | POWER_P6MM |
| POWER | BGA | POWER_P3MM |
| VR_CTL_PHY | * | POWER_P3MM |
| VR_CTL_PHY | BGA | STANDARD |
| VR_VID_PHY | * | POWER_50S |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| VR_DIDT_PHY | * | POWER_P6MM |
| VR_DIDT_PHY | BGA | STANDARD |

## Power-specific Spacing Definitions
## Power and Common

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| POWER_ISO | * | =STANDARD | ? |
| GND_ISO | * | =STANDARD | ? |

## Constraints
## Power and Common

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| POWER | * | * | POWER_ISO |
| GND | * | * | GND_ISO |

## DC-DC Baddies

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SWNODE_ISO | * | =8:1_SPACING | 1000 |
| SWNODE_SW2SW | * | =1:1_SPACING | ? |
| SWNODE_SW2PWR | * | =2:1_SPACING | ? |
| SWNODE_SW2GND | * | =2:1_SPACING | ? |

## DC-DC Baddies

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| VR_SWITCH | * | * | SWNODE_ISO |
| VR_SWITCH | * | BGA | BGA_P1MM |
| VR_SWITCH | VR_SWITCH | * | SWNODE_SW2SW |
| VR_SWITCH | POWER | * | SWNODE_SW2PWR |
| VR_SWITCH | GND | * | SWNODE_SW2GND |

## DC-DC Control

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| VR_CTL_ISO | * | =3:1_SPACING | ? |
| VR_VID_ISO | * | =4X_DIELECTRIC | ? |

## DC-DC Control

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| VR_CTL | * | * | VR_CTL_ISO |
| VR_VID | * | * | VR_VID_ISO |

## VDDQ S3 (1.35V)/VTT S0

| | Physical | Spacing | Voltage | DIDT | NO_TEST | |
|---|---|---|---|---|---|---|
| **Input Bus** | | | | | | |
| J47 | POWER | POWER | 5V | | | REG_V5IN_U7300 63 |
| **Local Ground** | | | | | | |
| J44 | GND | GND | 0V | | | AGND_VDDQS3 63 |
| **VDDQ S3** | | | | | | |
| J45 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_VDDQS3 63 |
| J43 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_VDDQS3_L 63 |
| J46 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_VDDQS3 63 |
| J48 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_VDDQS3_RC 63 |
| J49 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_VDDQS3 63 |
| J50 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_VDDQS3_R 63 |
| J52 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_LGATE_VDDQS3 63 |
| J51 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_SNUBBER_VDDQS3 63 |
| J53 | VR_CTL_PHY | VR_CTL | | | | REG_VDDQS3_VDDQSNS 63 |
| J55 | VR_CTL_PHY | VR_CTL | | | | REG_VDDQS3_VREF 63 |
| J56 | VR_CTL_PHY | VR_CTL | | | | REG_VDDQS3_REFIN 63 |
| J57 | VR_CTL_PHY | VR_CTL | | | | REG_VDDQS3_MODE 63 |
| J58 | VR_CTL_PHY | VR_CTL | | | | REG_VDDQS3_TRIP 63 |
| J59 | VR_CTL_PHY | VR_CTL | | | | LDO_DDRVTTS0_SNS 63 |
| J61 | VR_CTL_PHY | VR_CTL | | | | REG_VDDQS3_VTTREF 63 |
| **Output Bus** | | | | | | |
| J60 | POWER | POWER | 1.35V | | | PPVDDQ_S3 70 |
| J62 | POWER_DDR | POWER_DDR | 0.675V | | | PPDDRVTT_S0 70 |
| **FET Switched** | | | | | | |
| J63 | POWER | POWER | 1.35V | | | PPVDDQ_S0 70 |
| **Sensed** | | | | | | |
| J64 | POWER | POWER | 1.35V | | | PPVDDQ_S3_DDR 70 |
| J67 | POWER | POWER | 1.35V | | | PPVDDQ_S0_CPU 70 |

## PCH/GPU/TBT 1.05V S0

| | Electrical Contraint Set | Physical | Spacing | Voltage | DIDT | NO_TEST | |
|---|---|---|---|---|---|---|---|
| **Input Bus** | | | | | | | |
| J1 | | POWER | POWER | 5V | | | REG_VCC_U7400 64 |
| J2 | | POWER | POWER | 5V | | | REG_PVCC_U7400 64 |
| **Local Ground** | | | | | | | |
| J3 | | GND | GND | 0V | | | AGND_P1V05S0 64 |
| **1.05V S0** | | | | | | | |
| J5 | | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_P1V05S0 64 |
| J4 | | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_P1V05S0_L 64 |
| J7 | | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_P1V05S0 64 |
| J6 | | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_P1V05S0_RC 64 |
| J8 | | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_P1V05S0 64 |
| J9 | | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_P1V05S0_R 64 |
| J10 | | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_LGATE_P1V05S0 64 |
| J12 | | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_SNUBBER_P1V05S0 64 |
| J11 | | VR_CTL_PHY | VR_CTL | | | | REG_P1V05S0_OCSET 64 |
| J14 | | VR_CTL_PHY | VR_CTL | | | | REG_P1V05S0_VO 64 |
| J16 | | | SENSE | | | | REG_P1V05S0_FB 64 |
| J18 | | | SENSE | | | | REG_P1V05S0_RTN 64 |
| J21 | | VR_CTL_PHY | VR_CTL | | | | REG_P1V05S0_SREF 64 |
| J20 | | VR_CTL_PHY | VR_CTL | | | | REG_P1V05S0_FSEL 64 |
| **Output Bus** | | | | | | | |
| J22 | | POWER | POWER | 1.05V | | | PP1V05_S0 70 |
| **FET Switched** | | | | | | | |
| J23 | | POWER | POWER | 1.05V | | | PP1V05_TBTLC 28 70 |
| J66 | | POWER | POWER | 1.05V | | | PP1V05_TBTCIO 70 |

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## CPU VCC Phases

| Electrical Contraint Set | Physical | Spacing | Voltage | DIDT | NO_TEST | |
|---|---|---|---|---|---|---|
| **Input Bus** | | | | | | |
| H102 | POWER | POWER | 12V | | | PP12V_S0_CPUVCC_FLT 61 62 |
| H103 | POWER | POWER | 5V | | | REG_VCC_U7000 61 |
| **Local Ground** | | | | | | |
| H104 | GND | GND | 0V | | | AGND_CPU 61 62 71 |
| **Phase 1** | | | | | | |
| H105 | VR_CTL_PHY | VR_CTL | | | | REG_THWN_1 62 |
| H106 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUVCC_1 61 62 |
| H107 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUVCC_1_R 61 |
| H108 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_CPUVCC_1 62 |
| H109 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_CPUVCC1 62 |
| H110 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_CPUVCC_1 62 |
| H111 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_CPUVCC_1_RC 62 |
| H112 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_SNUBBER_CPUVCC_1 62 |
| H113 | POWER | POWER | 1.8V | | | PPCPUVCC_S0_SENSE_1 62 |
| H114 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENVCC_1_P 61 62 |
| H115 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENVCC_1_N 62 |
| H116 | | SENSE | | | | REG_ISENVCC_1_NR 61 62 |
| **Phase 2** | | | | | | |
| H117 | VR_CTL_PHY | VR_CTL | | | | REG_THWN_2 62 |
| H118 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUVCC_2 61 62 |
| H119 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUVCC_2_R 61 |
| H120 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_CPUVCC_2 62 |
| H121 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_CPUVCC2 62 |
| H122 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_CPUVCC_2 62 |
| H123 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_CPUVCC_2_RC 62 |
| H124 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_SNUBBER_CPUVCC_2 62 |
| H125 | POWER | POWER | 1.8V | | | PPCPUVCC_S0_SENSE_2 62 |
| H126 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENVCC_2_P 61 62 |
| H127 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENVCC_2_N 62 |
| H128 | | SENSE | | | | REG_ISENVCC_2_NR 61 62 |
| **Phase 3** | | | | | | |
| H135 | VR_CTL_PHY | VR_CTL | | | | REG_THWN_3 62 |
| H136 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUVCC_3 61 62 |
| H137 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUVCC_3_R 61 |
| H138 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_CPUVCC_3 62 |
| H139 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_CPUVCC3 62 |
| H140 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_CPUVCC_3 62 |
| H141 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_CPUVCC_3_RC 62 |
| H142 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_SNUBBER_CPUVCC_3 62 |
| H143 | POWER | POWER | 1.8V | | | PPCPUVCC_S0_SENSE_3 62 |
| H144 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENVCC_3_P 61 62 |
| H145 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENVCC_3_N 62 |
| H146 | | SENSE | | | | REG_ISENVCC_3_NR 61 62 |

## CPU VCC Controller

| Electrical Contraint Set | Physical | Spacing | Voltage | DIDT | NO_TEST | |
|---|---|---|---|---|---|---|
| **ISL6372** | | | | | | |
| H152 | VR_CTL_PHY | VR_CTL | | | | REG_CPUVCC_DVC 61 |
| H153 | VR_CTL_PHY | VR_CTL | | | | CPUVCC_DVC_RC 61 |
| H154 | VR_CTL_PHY | VR_CTL | | | | CPUVCC_FB_RC_2 61 |
| H155 | VR_CTL_PHY | VR_CTL | | | | REG_CPUVCC_COMP 61 |
| H156 | VR_CTL_PHY | VR_CTL | | | | CPUVCC_COMP_RC 61 |
| H157 | VR_CTL_PHY | VR_CTL | | | | REG_CPUVCC_FB 61 |
| H158 | VR_CTL_PHY | VR_CTL | | | | CPUVCC_FB_RC 61 |
| H159 | VR_CTL_PHY | VR_CTL | | | | CPUVCC_FB_R_1 61 |
| H160 | VR_CTL_PHY | VR_CTL | | | | CPUVCC_FB_R_2 61 |
| H161 | VR_CTL_PHY | VR_CTL | | | | CPUVCC_PSICOMP_RC 61 |
| H162 | VR_CTL_PHY | VR_CTL | | | | REG_CPUVCC_PSICOMP 61 |
| H163 | VR_CTL_PHY | VR_CTL | | | | REG_CPUVCC_HFCOMP 61 |
| H164 VSNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | CPU_VCCSENSE_P 8 61 |
| H165 VSNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | CPU_VCCSENSE_N 9 61 |
| H166 | SNS_DIFF_PHY | SENSE | | | | CPU_VCCSENSE_R_P 61 |
| H167 | SNS_DIFF_PHY | SENSE | | | | CPU_VCCSENSE_R_N 61 |
| H168 | SNS_DIFF_PHY | SENSE | 1.8V | | | SNS_VCC_XW_P 61 |
| H169 | SNS_DIFF_PHY | SENSE | 0V | | | SNS_VCC_XW_N 61 |
| H170 | | SENSE | | | | REG_CPUVCC_VSEN 61 |
| H171 | | SENSE | | | | REG_CPUVCC_RGND 61 |
| H172 | | SENSE | | | | REG_CPUVCC_VIN 61 |
| H173 | VR_CTL_PHY | VR_CTL | | | | REG_CPUVCC_IMON 48 61 |
| H174 | VR_CTL_PHY | VR_CTL | | | | CPUVCC_IMON_R 61 |
| H175 | VR_CTL_PHY | VR_CTL | | | | REG_CPUVCC_TM 61 |
| H176 | VR_CTL_PHY | VR_CTL | | | | REG_CPUVCC_IMX 61 |
| H177 | VR_CTL_PHY | VR_CTL | | | | REG_CPUVCC_NPSI 61 |
| H178 | VR_CTL_PHY | VR_CTL | | | | REG_CPUVCC_FDVID 61 |
| H179 | VR_CTL_PHY | VR_CTL | | | | REG_CPUVCC_TMX 61 |
| H180 | VR_CTL_PHY | VR_CTL | | | | REG_CPUVCC_MEMVRSEL 61 |
| H181 | VR_CTL_PHY | VR_CTL | | | | REG_CPUVCC_RSET 61 |
| H182 CPU_VIDSCLK | VR_VID_PHY | VR_VID | | | | CPU_VIDSCLK 8 61 |
| H183 | VR_VID_PHY | VR_VID | | | | CPU_VIDSCLK_R 8 |
| H184 CPU_VIDALERT_L | VR_VID_PHY | VR_VID | | | | CPU_VIDALERT_L 8 61 |
| H185 | VR_VID_PHY | VR_VID | | | | CPU_VIDALERT_R_L 8 |
| H186 CPU_VIDSOUT | VR_VID_PHY | VR_VID | | | | CPU_VIDSOUT 8 61 |
| H187 | VR_VID_PHY | VR_VID | | | | CPU_VIDSOUT_R 8 |
| **Output Bus** | | | | | | |
| H188 | POWER | POWER | 1.8V | | | PPCPUVCC_S0_CPU 70 |

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### 12V

| | Physical | Spacing | Voltage | DIDT | NO_TEST | |
|---|---|---|---|---|---|---|
| Input Bus | | | | | | |
| H45 | POWER | POWER | 12V | | | PP12V_ACDC 70 |
| FET Switched | | | | | | |
| H46 | POWER | POWER | 12V | | | PP12V_S5 70 |
| H48 | POWER | POWER | 12V | | | PP12V_S0 70 |
| Sensed | | | | | | |
| H49 | POWER | POWER | 12V | | | PP12V_G3H 70 |

### 3.42V G3H

| | Physical | Spacing | Voltage | DIDT | NO_TEST | |
|---|---|---|---|---|---|---|
| 3.42V G3H | | | | | | |
| H54 | POWER | VR_SWITCH | 12V | TRUE | | P3V42G3H_BOOST 60 |
| H56 | POWER | VR_SWITCH | 12V | TRUE | | P3V42G3H_SW 60 |
| H55 | VR_CTL_PHY | VR_CTL | | | | P3V42G3H_FB 60 |
| H58 | VR_CTL_PHY | VR_CTL | | | | P3V42G3H_SHDN_L 60 |
| Output Bus | | | | | | |
| H46 | POWER | POWER | 3.425V | | | PP3V42_G3H 70 |

### 3.3V G3

| | Physical | Spacing | Voltage | DIDT | NO_TEST | |
|---|---|---|---|---|---|---|
| H57 | POWER | POWER | 3.3V | | | PP3V3_G3 70 |

### 3.3V S5/5V S4

| | Physical | Spacing | Voltage | DIDT | NO_TEST | |
|---|---|---|---|---|---|---|
| Input Bus | | | | | | |
| H44 | POWER | POWER | 12V | | | REG_VIN_U7600 65 |
| H42 | POWER | POWER | 5V | | | REG_VCC1_U7600 65 |
| H43 | POWER | POWER | 5V | | | REG_VCC2_U7600 65 |
| 3.3V S5 | | | | | | |
| H40 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_P3V3S5 65 |
| H47 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_P3V3S5 65 |
| H84 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_P3V3S5_RC 65 |
| H41 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_P3V3S5 65 |
| H86 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_LGATE_P3V3S5 65 |
| H85 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_SNUBBER_P3V3S5 65 |
| H107 | VR_CTL_PHY | VR_CTL | | | | REG_P3V3S5_ISEN 65 |
| H108 | VR_CTL_PHY | VR_CTL | | | | REG_P3V3S5_OCSET 65 |
| H110 | VR_CTL_PHY | VR_CTL | | | | REG_P3V3S5_FSET 65 |
| H106 | VR_CTL_PHY | VR_CTL | | | | REG_P3V3S5_VOUT 65 |
| H109 | VR_CTL_PHY | VR_CTL | | | | REG_P3V3S5_VOUT_R 65 |
| H105 | VR_CTL_PHY | VR_CTL | | | | REG_P3V3S5_FB 65 |
| 5V S3 | | | | | | |
| H113 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_P5VS4 65 |
| H111 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_P5VS4 65 |
| H115 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_P5VS4_RC 65 |
| H112 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_P5VS4 65 |
| H114 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_LGATE_P5VS4 65 |
| H116 | VR_DIDT_PHY | VR_SWITCH | 12V | TRUE | | REG_SNUBBER_P5VS4 65 |
| H117 | VR_CTL_PHY | VR_CTL | | | | REG_P5VS4_ISEN 65 |
| H118 | VR_CTL_PHY | VR_CTL | | | | REG_P5VS4_OCSET 65 |
| H119 | VR_CTL_PHY | VR_CTL | | | | REG_P5VS4_FSET 65 |
| H115 | VR_CTL_PHY | VR_CTL | | | | REG_P5VS4_VOUT 65 |
| H113 | VR_CTL_PHY | VR_CTL | | | | REG_P5VS4_VOUT_R 65 |
| H117 | VR_CTL_PHY | VR_CTL | | | | REG_P5VS4_FB 65 |
| Output Bus | | | | | | |
| H116 | POWER | POWER | 5V | | | PP5V_S5 70 |
| H111 | POWER | POWER | 5V | | | PP5V_S4 70 |
| H114 | POWER | POWER | 3.3V | | | PP3V3_S5 70 |
| FET Switched | | | | | | |
| H120 | POWER | POWER | 5V | | | PP5V_S0 70 |
| H121 | POWER | POWER | 3.3V | | | PP3V3_S4 70 |
| H122 | POWER | POWER | 3.3V | | | PP3V3_S0 70 |
| H145 | POWER | POWER | 3.3V | | | PP3V3_S0_SSD 70 |
| H121 | POWER | POWER | 3.3V | | | PP3V3_ENET 70 |
| H138 | POWER | POWER | 3.3V | | | PP3V3_TBTLC 70 |
| Sensed | | | | | | |
| H146 | POWER | POWER | 3.3V | | | PPSSD_S0 70 |
| H147 | POWER | POWER | 3.3V | | | PP3V3_S4_AP 70 |

### HDD S0

| | Physical | Spacing | Voltage | DIDT | NO_TEST | |
|---|---|---|---|---|---|---|
| FET Switched | | | | | | |
| H139 | POWER | POWER | 5V | | | PPHDD_S0 70 |
| Sensed | | | | | | |
| H140 | POWER | POWER | 5V | | | PP5V_S0_HDD 70 |

### 1V5 S0

| | Physical | Spacing | Voltage | DIDT | NO_TEST | |
|---|---|---|---|---|---|---|
| OUTPUT BUS | | | | | | |
| H137 | POWER | POWER | 1.5V | | | PP1V5_S0 70 |
| H135 | VR_CTL_PHY | VR_CTL | | | | REG_P1V5S0_SS 64 |
| H136 | VR_CTL_PHY | VR_CTL | | | | REG_P1V5S0_ISET 64 |
| H134 | VR_CTL_PHY | VR_CTL | | | | REG_P1V5S0_ADJ 64 |

### Ground/Common

| | Physical | Spacing | Voltage | DIDT | NO_TEST | |
|---|---|---|---|---|---|---|
| Common | | | | | | |
| H138 | GND | GND | 0V | | | GND |

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PAGE TITLE
# Platform VReg Constraints

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## Thunderbolt

### Thunderbolt-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| TBT_I2C_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| TBT_SPI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| TBTDP_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

### Thunderbolt-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| TBT_I2C | * | =2x_DIELECTRIC | ? |
| TBT_SPI | * | =2x_DIELECTRIC | ? |
| TBTDP | * | =5x_DIELECTRIC | ? |
| TBTDP | TOP,BOTTOM | =7x_DIELECTRIC | ? |

SOURCE: Bill Cornelius's T29 Routing Notes

## DisplayPort

### DP-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| DP_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | 0.08MM | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |

### DP-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DISPLAYPORT | * | =3:1_SPACING | ? |

Pairs should be within 100 mils of clock length.
Max length of DisplayPort traces: 12 inches

DisplayPort intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX channel intra-pair matching should be 5 ps. No relationship to other signals.

## TBT IC Net Properties

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| H51 | DP_85D | DISPLAYPORT | DP_TBTSNK0_ML_C_P<3..0> | 26 71 |
| H53 | DP_85D | DISPLAYPORT | DP_TBTSNK0_ML_C_N<3..0> | 26 71 |
| H52 DP_TBTSNK0_ML | DP_85D | DISPLAYPORT | DP_TBTSNK0_ML_P<3..0> | 26 |
| H54 DP_TBTSNK0_ML | DP_85D | DISPLAYPORT | DP_TBTSNK0_ML_N<3..0> | 26 |
| H56 | DP_85D | DISPLAYPORT | DP_TBTSNK0_AUXCH_C_P | 26 71 |
| H55 | DP_85D | DISPLAYPORT | DP_TBTSNK0_AUXCH_C_N | 26 71 |
| H57 DP_TBTSNK0_AUX | DP_85D | DISPLAYPORT | DP_TBTSNK0_AUXCH_P | 26 |
| H58 DP_TBTSNK0_AUX | DP_85D | DISPLAYPORT | DP_TBTSNK0_AUXCH_N | 26 |
| H91 | DP_85D | DISPLAYPORT | DP_TBTSNK1_ML_C_P<3..0> | 26 71 |
| H92 | DP_85D | DISPLAYPORT | DP_TBTSNK1_ML_C_N<3..0> | 26 71 |
| H90 DP_TBTSNK1_ML | DP_85D | DISPLAYPORT | DP_TBTSNK1_ML_P<3..0> | 26 |
| H93 DP_TBTSNK1_ML | DP_85D | DISPLAYPORT | DP_TBTSNK1_ML_N<3..0> | 26 |
| H95 | DP_85D | DISPLAYPORT | DP_TBTSNK1_AUXCH_C_P | 26 71 |
| H94 | DP_85D | DISPLAYPORT | DP_TBTSNK1_AUXCH_C_N | 26 71 |
| H96 DP_TBTSNK1_AUX | DP_85D | DISPLAYPORT | DP_TBTSNK1_AUXCH_P | 26 |
| H97 DP_TBTSNK1_AUX | DP_85D | DISPLAYPORT | DP_TBTSNK1_AUXCH_N | 26 |
| H60 DP_INTPNL_TBT_ML_MUX | DP_85D | DISPLAYPORT | DP_TBTSRC_ML_P<3..0> | 41 |
| H62 DP_INTPNL_TBT_ML_MUX | DP_85D | DISPLAYPORT | DP_TBTSRC_ML_N<3..0> | 41 |
| H61 DP_INTPNL_TBT_ML_MUX | DP_85D | DISPLAYPORT | DP_TBTSRC_ML_C_P<3..0> | 41 |
| H63 DP_INTPNL_TBT_ML_MUX | DP_85D | DISPLAYPORT | DP_TBTSRC_ML_C_N<3..0> | 41 |
| H64 DP_INTPNL_TBT_AUX_MUX | DP_85D | DISPLAYPORT | DP_TBTSRC_AUXCH_P | 41 |
| H65 DP_INTPNL_TBT_AUX_MUX | DP_85D | DISPLAYPORT | DP_TBTSRC_AUXCH_N | 41 |
| H66 | DP_85D | DISPLAYPORT | DP_TBTSRC_AUX_C_P | 41 |
| H67 | DP_85D | DISPLAYPORT | DP_TBTSRC_AUX_C_N | 41 |
| H31 | TBT_I2C_55S | TBT_I2C | I2C_TBTRTR_SCL | 26 |
| H32 | TBT_I2C_55S | TBT_I2C | I2C_TBTRTR_SDA | 26 |
| H33 TBT_SPI_CLK | TBT_SPI_55S | TBT_SPI | TBT_SPI_CLK | 26 |
| H34 TBT_SPI_MOSI | TBT_SPI_55S | TBT_SPI | TBT_SPI_MOSI | 26 |
| H35 TBT_SPI_MISO | TBT_SPI_55S | TBT_SPI | TBT_SPI_MISO | 26 |
| H36 TBT_SPI_CS_L | TBT_SPI_55S | TBT_SPI | TBT_SPI_CS_L | 26 |

*: Only used on hosts supporting T29 video-in

## DisplayPort

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| Graphics Source | | | | |
| H42 DP_INTPNL_EG_ML_MUX | DP_85D | DISPLAYPORT | DP_INT_ML_P<1..0> | 41 71 |
| H43 DP_INTPNL_EG_ML_MUX | DP_85D | DISPLAYPORT | DP_INT_ML_N<1..0> | 41 71 |
| H44 DP_INTPNL_EG_AUX_MUX | DP_85D | DISPLAYPORT | DP_INT_AUX_P | 41 71 |
| H45 DP_INTPNL_EG_AUX_MUX | DP_85D | DISPLAYPORT | DP_INT_AUX_N | 41 71 |
| H46 | DP_85D | DISPLAYPORT | DP_INT_AUX_C_P | 41 |
| H47 | DP_85D | DISPLAYPORT | DP_INT_AUX_C_N | 41 |
| Internal Panel | | | | |
| H68 | DP_85D | DISPLAYPORT | DP_INTPNL_ML_C_P<3..0> | 41 |
| H69 | DP_85D | DISPLAYPORT | DP_INTPNL_ML_C_N<3..0> | 41 |
| H87 DP_INTPNL_ML_CONN | DP_85D | DISPLAYPORT | DP_INTPNL_ML_P<3..0> | 40 41 |
| H88 DP_INTPNL_ML_CONN | DP_85D | DISPLAYPORT | DP_INTPNL_ML_N<3..0> | 40 41 |
| H89 DP_INTPNL_AUX_CONN | DP_85D | DISPLAYPORT | DP_INTPNL_AUX_P | 40 41 |
| H91 DP_INTPNL_AUX_CONN | DP_85D | DISPLAYPORT | DP_INTPNL_AUX_N | 40 41 |
| Internal DP SPDIF | | | | |
| H51 | | HDA | DP_INT_SPDIF_AUDIO | 40 52 |

## TBT/DP Net Properties

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| Port A | | | | |
| T64 TBT_A_R2D1 | TBTDP_90D | TBTDP | TBT_A_R2D_C_P<1> | 26 29 |
| T65 TBT_A_R2D1 | TBTDP_90D | TBTDP | TBT_A_R2D_C_N<1> | 26 29 |
| T66 TBT_A_R2D0 | TBTDP_90D | TBTDP | TBT_A_R2D_C_P<0> | 26 29 |
| T68 TBT_A_R2D0 | TBTDP_90D | TBTDP | TBT_A_R2D_C_N<0> | 26 29 |
| T63 | TBTDP_90D | TBTDP | TBT_A_R2D_P<1..0> | 29 |
| T67 | TBTDP_90D | TBTDP | TBT_A_R2D_N<1..0> | 29 |
| T59 DP_TBTPA_ML1 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_C_P<1> | 26 29 |
| T58 DP_TBTPA_ML1 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_C_N<1> | 26 29 |
| T60 DP_TBTPA_ML3 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_C_P<3> | 26 29 |
| T61 DP_TBTPA_ML3 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_C_N<3> | 26 29 |
| T45 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_P<1> | 29 |
| T47 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_N<1> | 29 |
| T70 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_P<3> | 29 |
| T72 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_N<3> | 29 |
| T50 DP_A_LSX | DP_85D | DISPLAYPORT | DP_A_LSX_ML_P<1> | 29 |
| T49 DP_A_LSX | DP_85D | DISPLAYPORT | DP_A_LSX_ML_N<1> | 29 |
| T48 | TBTDP_90D | TBTDP | TBT_A_D2R_C_P<1..0> | 29 |
| T52 | TBTDP_90D | TBTDP | TBT_A_D2R_C_N<1..0> | 29 |
| T54 TBT_A_D2R1 | TBTDP_90D | TBTDP | TBT_A_D2R_P<1> | 26 29 |
| T55 TBT_A_D2R1 | TBTDP_90D | TBTDP | TBT_A_D2R_N<1> | 26 29 |
| T57 TBT_A_D2R0 | TBTDP_90D | TBTDP | TBT_A_D2R_P<0> | 26 29 |
| T74 TBT_A_D2R0 | TBTDP_90D | TBTDP | TBT_A_D2R_N<0> | 26 29 |
| T56 TBT_A_AUXCH | DP_85D | DISPLAYPORT | DP_TBTPA_AUXCH_C_P | 26 29 |
| T69 TBT_A_AUXCH | DP_85D | DISPLAYPORT | DP_TBTPA_AUXCH_C_N | 26 29 |
| T46 | DP_85D | DISPLAYPORT | DP_TBTPA_AUXCH_P | 29 |
| T53 | DP_85D | DISPLAYPORT | DP_TBTPA_AUXCH_N | 29 |
| T51 DP_A_AUXCH_DDC | DP_85D | DISPLAYPORT | DP_A_AUXCH_DDC_P | 29 |
| T62 DP_A_AUXCH_DDC | DP_85D | DISPLAYPORT | DP_A_AUXCH_DDC_N | 29 |
| T73 | TBTDP_90D | TBTDP | TBT_A_D2R1_AUXDDC_P | 29 |
| T81 | TBTDP_90D | TBTDP | TBT_A_D2R1_AUXDDC_N | 29 |
| Port B | | | | |
| T85 TBT_B_R2D1 | TBTDP_90D | TBTDP | TBT_B_R2D_C_P<1> | 26 30 |
| T84 TBT_B_R2D1 | TBTDP_90D | TBTDP | TBT_B_R2D_C_N<1> | 26 30 |
| T86 TBT_B_R2D0 | TBTDP_90D | TBTDP | TBT_B_R2D_C_P<0> | 26 30 |
| T91 TBT_B_R2D0 | TBTDP_90D | TBTDP | TBT_B_R2D_C_N<0> | 26 30 |
| T83 | TBTDP_90D | TBTDP | TBT_B_R2D_P<1..0> | 30 |
| T94 | TBTDP_90D | TBTDP | TBT_B_R2D_N<1..0> | 30 |
| T87 DP_TBTPB_ML1 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_C_P<1> | 26 30 |
| T89 DP_TBTPB_ML1 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_C_N<1> | 26 30 |
| T88 DP_TBTPB_ML3 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_C_P<3> | 26 30 |
| T90 DP_TBTPB_ML3 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_C_N<3> | 26 30 |
| T80 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_P<1> | 30 |
| T82 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_N<1> | 30 |
| T76 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_P<3> | 30 |
| T78 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_N<3> | 30 |
| T95 DP_B_LSX | DP_85D | DISPLAYPORT | DP_B_LSX_ML_P<1> | 30 |
| T92 DP_B_LSX | DP_85D | DISPLAYPORT | DP_B_LSX_ML_N<1> | 30 |
| T81 | TBTDP_90D | TBTDP | TBT_B_D2R_C_P<1..0> | 30 |
| T96 | TBTDP_90D | TBTDP | TBT_B_D2R_C_N<1..0> | 30 |
| T98 TBT_B_D2R1 | TBTDP_90D | TBTDP | TBT_B_D2R_P<1> | 26 30 |
| T99 TBT_B_D2R1 | TBTDP_90D | TBTDP | TBT_B_D2R_N<1> | 26 30 |
| T97 TBT_B_D2R0 | TBTDP_90D | TBTDP | TBT_B_D2R_P<0> | 26 30 |
| T77 TBT_B_D2R0 | TBTDP_90D | TBTDP | TBT_B_D2R_N<0> | 26 30 |
| T100 TBT_B_AUXCH | DP_85D | DISPLAYPORT | DP_TBTPB_AUXCH_C_P | 26 30 |
| T97 TBT_B_AUXCH | DP_85D | DISPLAYPORT | DP_TBTPB_AUXCH_C_N | 26 30 |
| T93 | DP_85D | DISPLAYPORT | DP_TBTPB_AUXCH_P | 30 |
| T79 | DP_85D | DISPLAYPORT | DP_TBTPB_AUXCH_N | 30 |
| T100 DP_B_AUXCH_DDC | DP_85D | DISPLAYPORT | DP_B_AUXCH_DDC_P | 30 |
| T75 DP_B_AUXCH_DDC | DP_85D | DISPLAYPORT | DP_B_AUXCH_DDC_N | 30 |
| T74 | TBTDP_90D | TBTDP | TBT_B_D2R1_AUXDDC_P | 30 |
| T71 | TBTDP_90D | TBTDP | TBT_B_D2R1_AUXDDC_N | 30 |

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# Backlight Controller

## BLC-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| BLC_P6MM | * | Y | 0.600 MM | 0.100 MM | 3.0 MM | =STANDARD | =STANDARD |
| BLC_P3MM | * | Y | 0.300 MM | 0.100 MM | 3.0 MM | =STANDARD | =STANDARD |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| POWER_BLC | * | BLC_P6MM |
| POWER_BLC_RET | * | BLC_P3MM |
| BLC_CTL_PHY | * | BLC_P3MM |

## BLC-specific Spacing Definitions
## BLC High Voltage Output

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| BLC_HV_ISO | * | 0.45mm | 1000 |

## Constraints
## BLC High Voltage Output

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| BLC_HV | BLC_CTL | * | BLC_CTL_ISO |
| BLC_HV | BLC_HV | * | BLC_CTL_ISO |
| BLC_HV | * | * | BLC_HV_ISO |

## BLC Baddies

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| PHASE_ISO | * | =8:1_SPACING | 2000 |
| PHASE_SW2SW | * | =1:1_SPACING | ? |
| PHASE_SW2PWR | * | =2:1_SPACING | ? |
| PHASE_SW2GND | * | =2:1_SPACING | ? |

## BLC Baddies

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| BLC_PHASE | * | * | PHASE_ISO |
| BLC_PHASE | BLC_PHASE | * | PHASE_SW2SW |
| BLC_PHASE | POWER | * | PHASE_SW2PWR |
| BLC_PHASE | GND | * | PHASE_SW2GND |

## BLC Control

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| BLC_CTL_ISO | * | =3:1_SPACING | ? |

## BLC Control

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| BLC_CTL | * | * | BLC_CTL_ISO |

## Is it chel'oh or sel'oh?

| | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| Input Bus | | | | | | | |
| H38 | POWER | POWER | 12V | | | PP12V_BKLT_SNS | 66 |
| H40 | POWER | POWER | 12V | | | PP12V_BKLT_FUSED | 66 |
| H46 | POWER | POWER | 12V | | | PP12V_S0_BKLT_FILT | 66 |
| H72 | POWER | POWER | 12V | | | PP12V_S0_BKLT_PWR | 66 |
| H94 | POWER | POWER | 12V | | | PP12V_S0_BKLT_PWR_R | 66 |
| H96 | POWER | POWER | 5V | | | PP5V_S0_BKLT_R | 66 |
| H62 | POWER | POWER | 3.3V | | | PP3V3_S0_BKLT_VDDIO_R | 66 |
| Local Ground | | | | | | | |
| H34 | BLC_CTL_PHY | BLC_PHASE | 0V | | | PGND_BKLT | 66 |
| H70 | BLC_CTL_PHY | BLC_PHASE | 0V | | | DGND_BKLT | 66 |
| H88 | BLC_CTL_PHY | BLC_PHASE | 0V | | | LGND_BKLT | 66 |
| Backlight | | | | | | | |
| H52 | POWER_BLC | BLC_PHASE | 80V | TRUE | | BKLT_PHASE | 66 |
| H56 | BLC_CTL_PHY | BLC_PHASE | 80V | TRUE | | BKLT_GATE | 66 |
| H54 | BLC_CTL_PHY | BLC_PHASE | 80V | TRUE | | BKLT_GATE_R | 66 |
| H58 | BLC_CTL_PHY | BLC_PHASE | 80V | TRUE | | BKLT_SNUBBER | 66 |
| H60 | BLC_CTL_PHY | BLC_PHASE | 12V | TRUE | | BKLT_SW_R | 66 |
| H50 | BLC_CTL_PHY | BLC_CTL | | | | BKLT_ISET | 66 |
| H48 | BLC_CTL_PHY | BLC_CTL | | | | BKLT_FLT | 66 |
| H68 | BLC_CTL_PHY | BLC_CTL | | | | BKLT_FLT_RC | 66 |
| H78 | SNS_DIFF_PHY | SENSE | | | | BKLT_SW_P | 66 |
| H80 | SNS_DIFF_PHY | SENSE | | | | BKLT_SW_N | 66 |
| H42 | | SENSE | | | | BKLT_FB | 66 |
| H90 | | BLC_HV | 67V | | | BKLT_FB_XW | 66 |
| H76 | | BLC_HV | 67V | | | BKLT_FB_R | 66 |
| H74 | POWER_BLC_RET | BLC_CTL | | | | BKLT_ISEN1 | 66 |
| H82 | POWER_BLC_RET | BLC_CTL | | | | BKLT_ISEN2 | 66 |
| H84 | POWER_BLC_RET | BLC_CTL | | | | BKLT_ISEN3 | 66 |
| H86 | POWER_BLC_RET | BLC_CTL | | | | BKLT_ISEN4 | 66 |
| H92 | POWER_BLC_RET | BLC_CTL | | | | BKLT_ISEN5 | 66 |
| H44 | POWER_BLC_RET | BLC_CTL | | | | BKLT_ISEN6 | 66 |
| H36 | POWER_BLC_RET | BLC_HV | | | | BKLT_ISEN1_R | 66 |
| H38 | POWER_BLC_RET | BLC_HV | | | | BKLT_ISEN2_R | 66 |
| H98 | POWER_BLC_RET | BLC_HV | | | | BKLT_ISEN3_R | 66 |
| H32 | POWER_BLC_RET | BLC_HV | | | | BKLT_ISEN4_R | 66 |
| H64 | POWER_BLC_RET | BLC_HV | | | | BKLT_ISEN5_R | 66 |
| H66 | POWER_BLC_RET | BLC_HV | | | | BKLT_ISEN6_R | 66 |
| H30 | POWER_BLC_RET | BLC_HV | | | | LED_RETURN_1 | 66 |
| H28 | POWER_BLC_RET | BLC_HV | | | | LED_RETURN_2 | 66 |
| H26 | POWER_BLC_RET | BLC_HV | | | | LED_RETURN_3 | 66 |
| H24 | POWER_BLC_RET | BLC_HV | | | | LED_RETURN_4 | 66 |
| H22 | POWER_BLC_RET | BLC_HV | | | | LED_RETURN_5 | 66 |
| H20 | POWER_BLC_RET | BLC_HV | | | | LED_RETURN_6 | 66 |
| Output Bus | | | | | | | |
| H18 | POWER_BLC | BLC_HV | 67V | | | BKLT_BOOST | 66 |
| H16 | POWER_BLC | BLC_HV | 67V | | | BKLT_BOOST_1 | 66 |
| H14 | POWER_BLC | BLC_HV | 67V | | | BKLT_BOOST_2 | 66 |

## Cello Miscellaneous

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| SPI | | | | |
| H66 | SMB_PHY | SMB | BKLT_SCL | 66 |
| H68 | SMB_PHY | SMB | BKLT_SDA | 66 |

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