

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
A	0001052699	PRODUCTION RELEASED		2011-01-10

J72 MLB

PVT REV.A

LAST MODIFIED=Mon Apr 23 11:04:38 2013

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	Table of Contents	N/A	N/A
2	2	BLOCK DIAGRAM: SYSTEM	N/A	N/A
3	4	BOM TABLES	N/A	N/A
4	6	SOC: MAIN	N/A	N/A
5	7	SOC: I/OS	N/A	N/A
6	8	SOC: NAND	N/A	N/A
7	9	SOC: DP,MIPI	N/A	N/A
8	10	SOC: DDR	N/A	N/A
9	11	SOC: IO POWER	N/A	N/A
10	12	SOC: SRAM POWER	N/A	N/A
11	13	SOC: CPU POWER	N/A	N/A
12	14	DDR: CHANNEL 0 AND 1	N/A	N/A
13	15	SOC: MISC & ALIASES	N/A	N/A
14	16	NAND: NAND	N/A	N/A
15	17	AUDIO: L81 CODEC	N/A	N/A
16	18	AUDIO: HP/DMIC FLEX CONNS	N/A	N/A
17	19	AUDIO: SPEAKER AMPS RIGHT	N/A	N/A
18	20	AUDIO: SPEAKER AMPS LEFT	N/A	N/A
19	24	SENSOR: OSCAR, GYRO, ACCEL	N/A	N/A
20	25	SENSOR: HALL EFFECT	N/A	N/A
21	26	IO: BUTTON FLEX CONN	N/A	N/A
22	27	CAMERA: FF AND ALS CONN	N/A	N/A
23	28	CAMERA: REAR CONN	N/A	N/A
24	29	SENSOR: COMPASS	N/A	N/A
25	30	CELL: SYSTEM & DEBUG CONNECTORS	RADIO_MLB_72_B7	06/03/2013

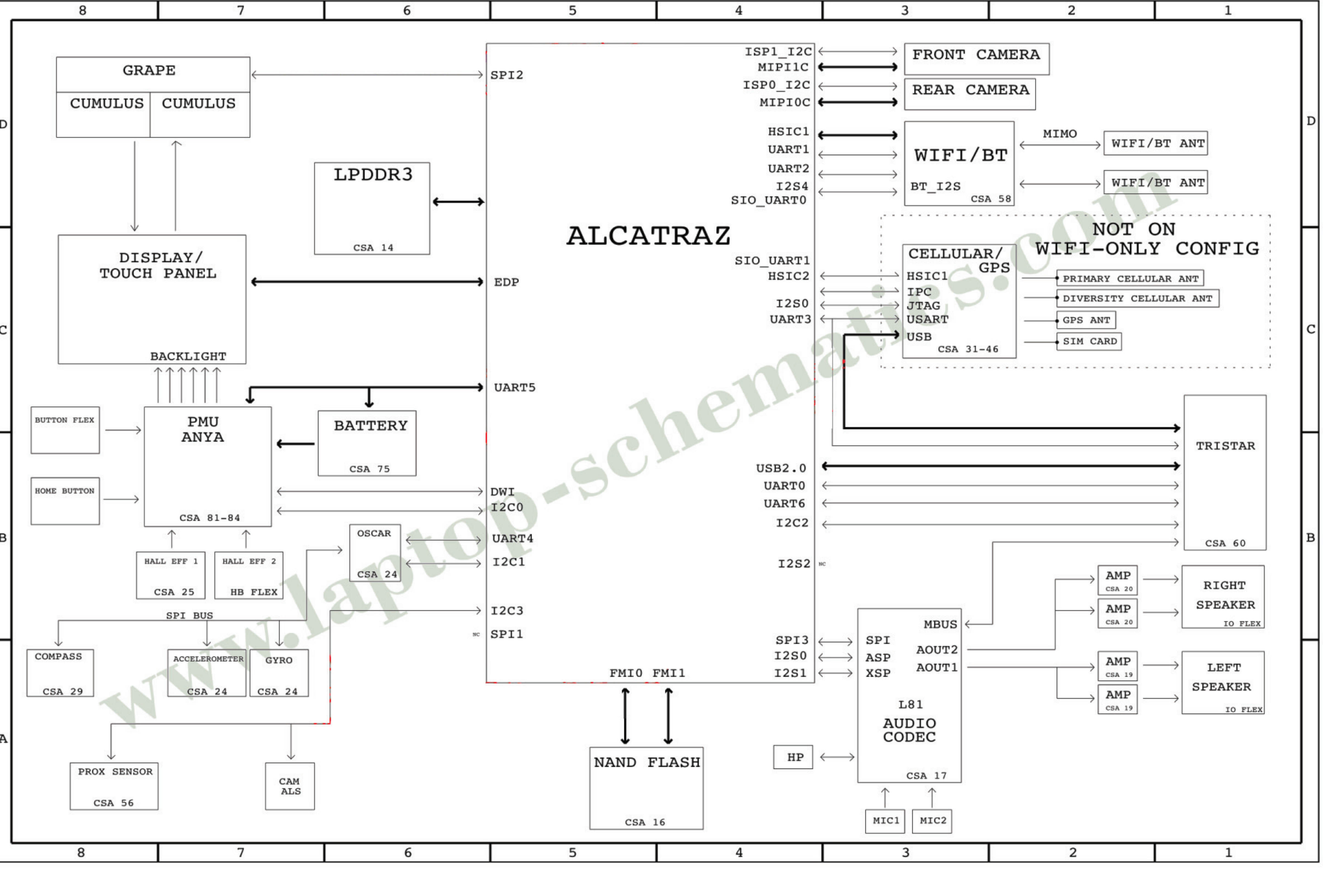
PDF	CSA	CONTENTS	SYNC MASTER	DATE
26	32	CELL: BASEBAND PMU (1 OF 2)	RADIO_MLB_72_B7	06/03/2013
27	33	CELL: BASEBAND PMU (2 OF 2)	RADIO_MLB_72_B7	06/03/2013
28	34	CELL: BASEBAND (1 OF 2)	RADIO_MLB_72_B7	06/03/2013
29	35	CELL: BASEBAND(2 OF 2)	RADIO_MLB_72_B7	06/03/2013
30	36	CELL: TRANSCEIVER (1 OF 2)	RADIO_MLB_72_B7	06/03/2013
31	37	CELL: TRANSCEIVER (2 OF 2)	RADIO_MLB_72_B7	06/03/2013
32	38	CELL: TRANSCEIVER MATCHING	RADIO_MLB_72_B7	06/03/2013
33	39	CELL: SAW BANK	RADIO_MLB_72_B7	06/03/2013
34	40	CELL: BAND 1/4 PAT	RADIO_MLB_72_B7	06/03/2013
35	41	CELL: BAND 2/3 PAD	RADIO_MLB_72_B7	06/03/2013
36	42	CELL: BAND 20 PAD	RADIO_MLB_72_B7	06/03/2013
37	43	CELL: BAND 5/8 PAD	RADIO_MLB_72_B7	06/03/2013
38	44	CELL: BAND 13/17 PAD	RADIO_MLB_72_B7	06/03/2013
39	45	CELL: PA DC/DC CONVERTER	RADIO_MLB_72_B7	06/03/2013
40	46	CELL: 2G FEM	RADIO_MLB_72_B7	06/03/2013
41	47	CELL: RX DIVERSITY	RADIO_MLB_72_B7	06/03/2013
42	48	CELL: GPS	RADIO_MLB_72_B7	06/03/2013
43	49	CELL: ANTENNA FEEDS	RADIO_MLB_72_B7	06/03/2013
44	51	CELL: SIM FLEX CONN	N/A	N/A
45	56	SENSOR: PROX AD7149	N/A	N/A
46	58	WIFI/BT: MODULE	WIFI_DEV	05/21/2013
47	60	IO: TRISTAR	N/A	N/A
48	61	IO: FILTERING	N/A	N/A
49	62	IO: FLEX HOTBAR PADS	N/A	N/A
50	63	IO: HOME BUTTON FILTERS	N/A	N/A

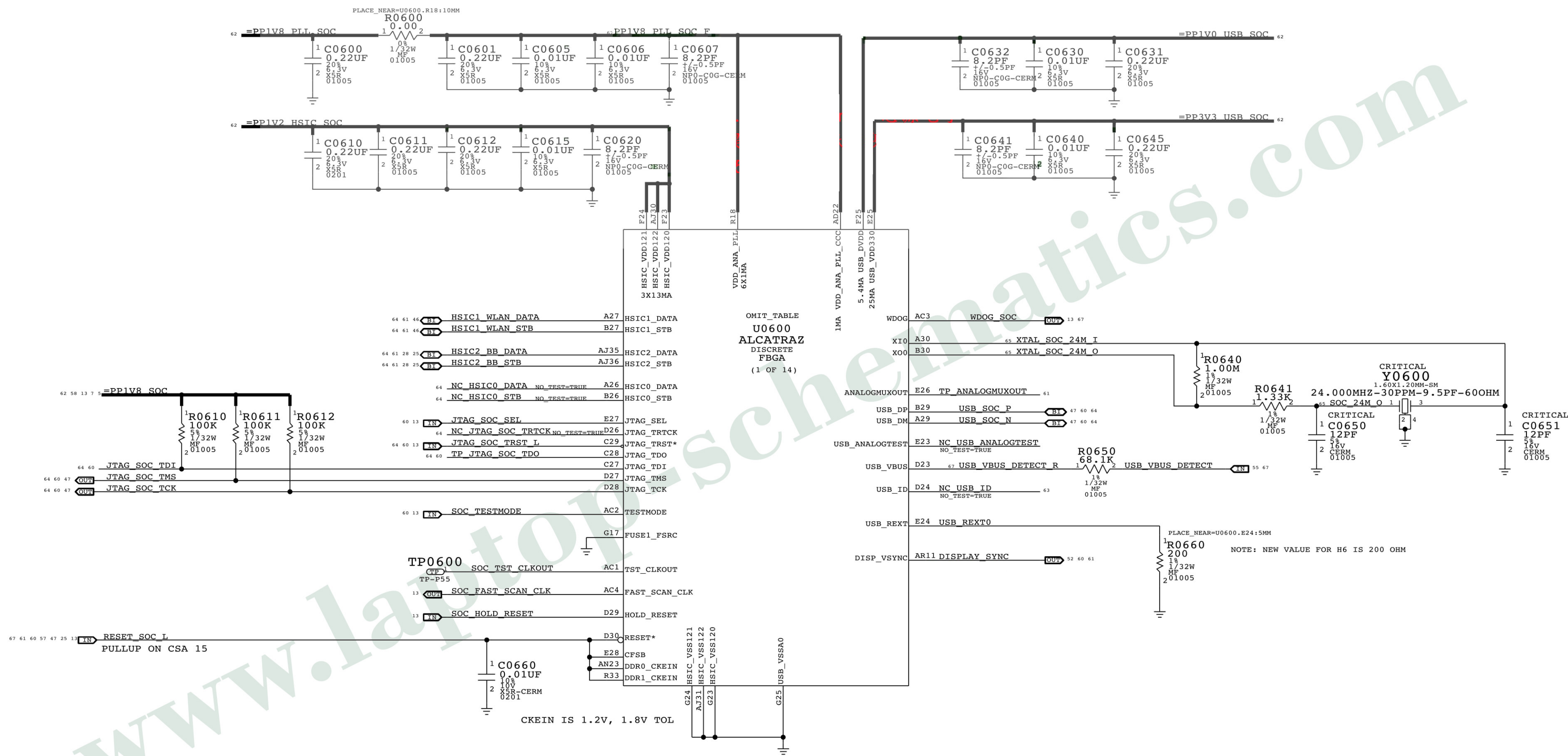
PDF	CSA	CONTENTS	SYNC MASTER	DATE
51	65	GRAPE: 1V8 POWER SWITCH	N/A	N/A
52	66	GRAPE: CUMULUS	N/A	N/A
53	70	DISPLAY: EDP CONN	N/A	N/A
54	75	POWER: BATTERY CONNECTOR	N/A	N/A
55	81	PMU: ANYA PAGE 1	N/A	N/A
56	82	PMU: ANYA PAGE 2	N/A	N/A
57	83	PMU: ANYA PAGE 3	N/A	N/A
58	84	PMU: ANYA PAGE 4	N/A	N/A
59	90	SOC: DEBUG	N/A	N/A
60	93	TEST: TP/HOLES/FIDUCUALS	N/A	N/A
61	94	TEST: EE TP/PP	N/A	N/A
62	121	POWER: ALIASES	N/A	N/A
63	150	CONSTRAINTS: MLB RULES	N/A	N/A
64	151	CONSTRAINTS: LOW SPEED BUS	N/A	N/A
65	152	CONSTRAINTS: DISPLAY/AUDIO	N/A	N/A
66	153	CONSTRAINTS: DDR/FMI	N/A	N/A
67	154	CONSTRAINTS: POWER / GND	N/A	N/A
68	157	CONSTRAINTS: RF	N/A	N/A
69	158	CONSTRAINTS: WIFI/BT	WIFI_DEV	05/21/2013

MLB# 820-3508 rev.A

DRAWING
TITLE=BACH
ABBREV=DRAWING

DRAWING TITLE		J72 MLB	
DRAWING NUMBER		SIDE D	
REVISION		A	
BRANCH			
PAGE		1 OF 68	
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DRAWING

I2S0 AND I2S2 ARE OPTIMIZED FOR LOW MCK JITTER

R0700
33.2
1/32W
MF
01005

OMIT_TABLE

U0600
ALCATRAZ
DISCRETE
FBGA
(3 OF 14)

SEP_7816UART0_RST

SEP_7816UART0_SCL

SEP_7816UART0_SDA

SEP_7816UART1_RST

SEP_7816UART1_SCL

SEP_7816UART1_SDA

SIO_7816UART0_RST

SIO_7816UART0_SCL

SIO_7816UART0_SDA

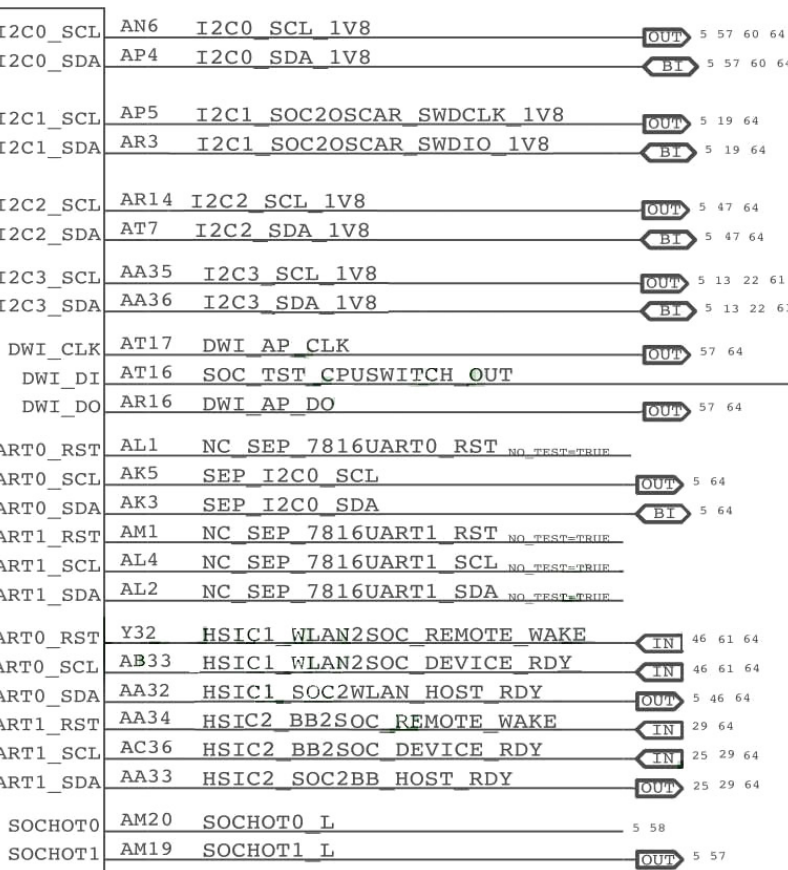
SIO_7816UART1_RST

SIO_7816UART1_SCL

SIO_7816UART1_SDA

SOCHOT0_L

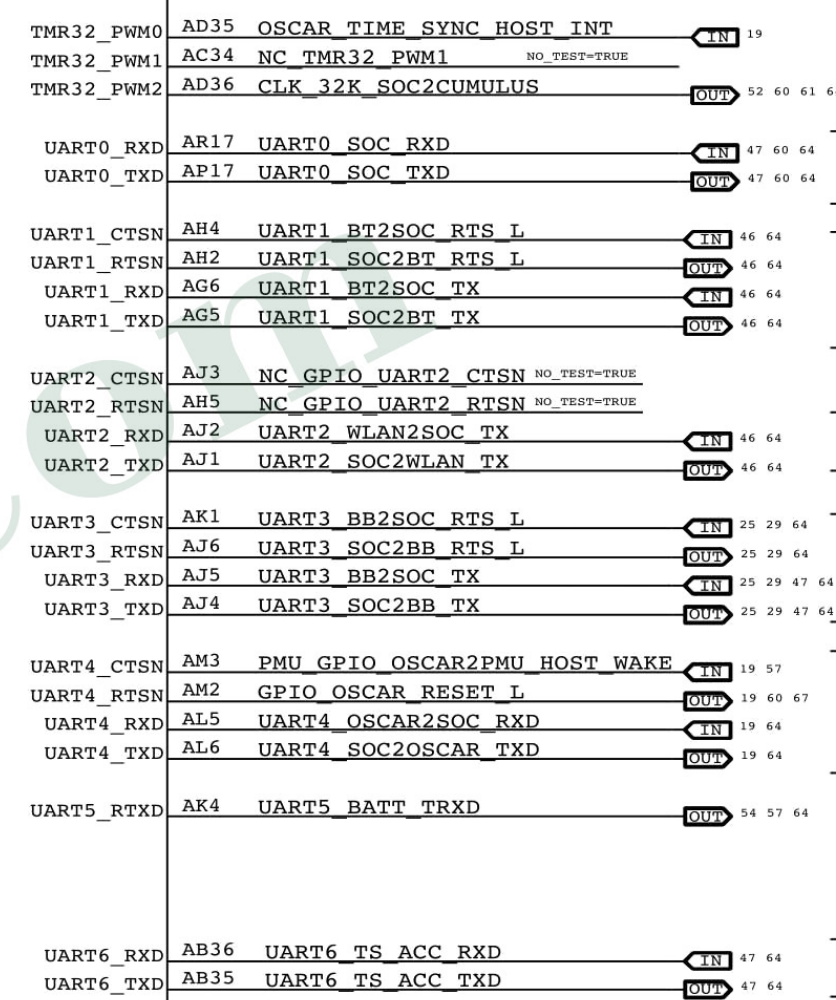
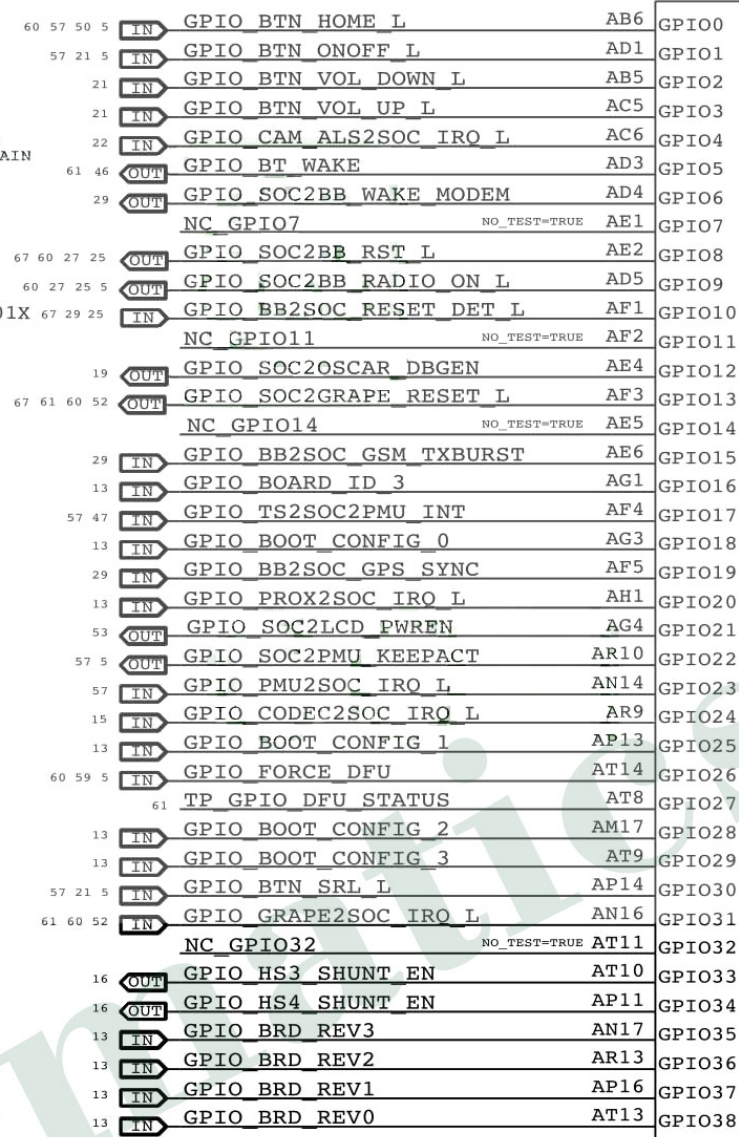
SOCHOT1_L



TP0700
A
TP-P55

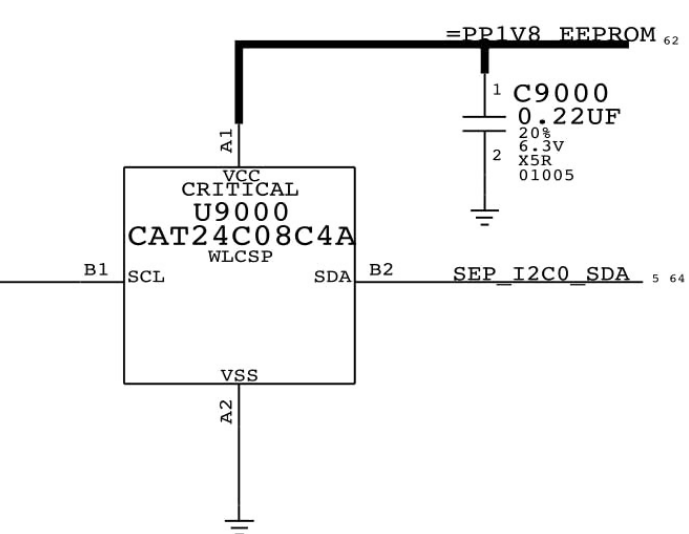
OMIT_TABLE

U0600
ALCATRAZ
DISCRETE
FBGA
(2 OF 14)

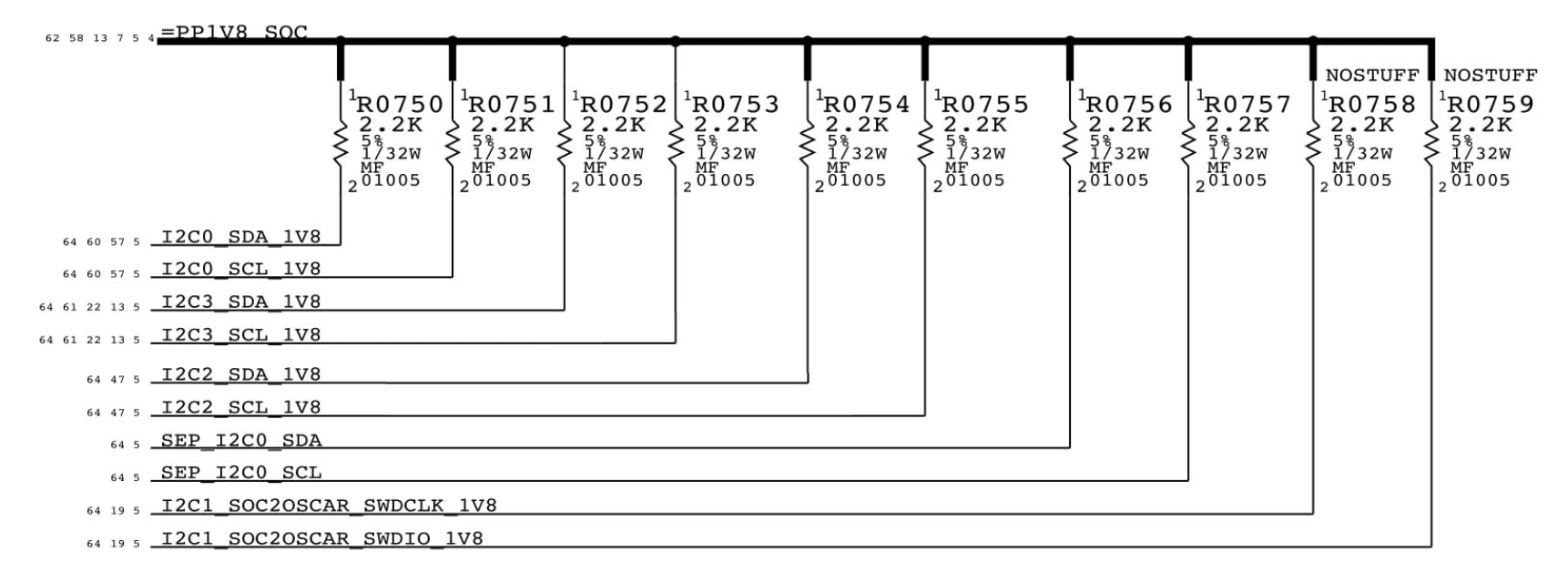


SEP EEPROM

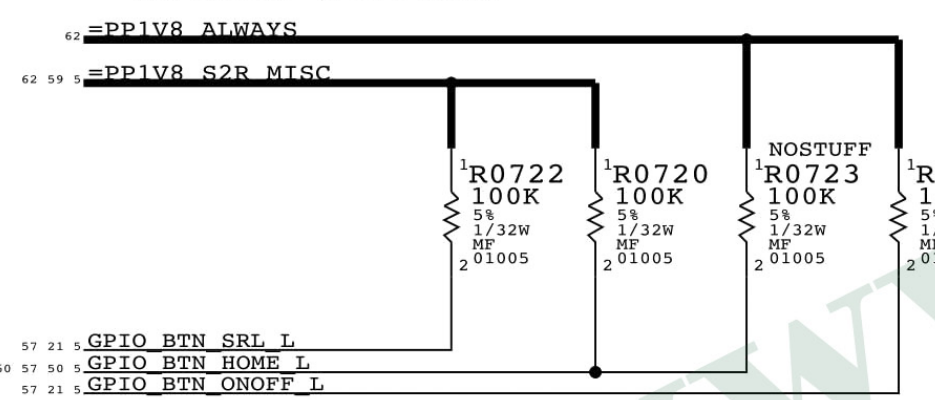
UNPROGRAMMED P/N: 335S0894



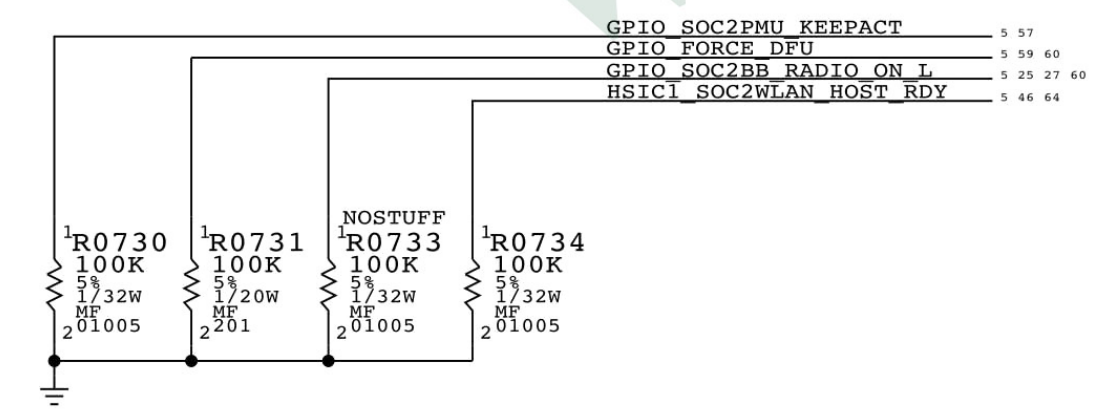
I2C PULL-UPS



BUTTON PULLUPS



GPIO_SOC2PMU_KEEPACT
GPIO_FORCE_DFU
GPIO_SOC2BB_RADIO_ON_L
HSIC1_SOC2WLAN_HOST_RDY



DRAWING

D

D

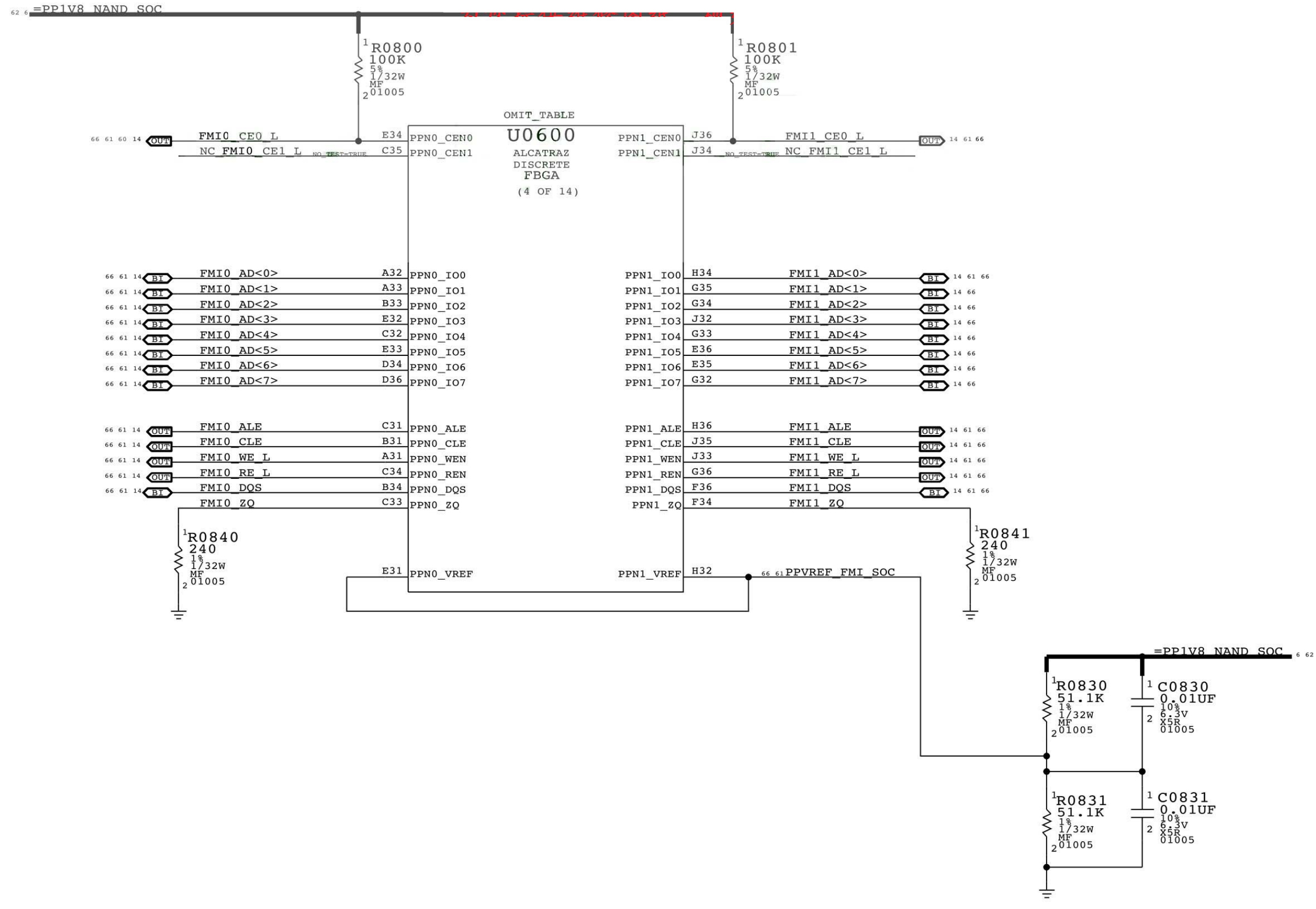
C

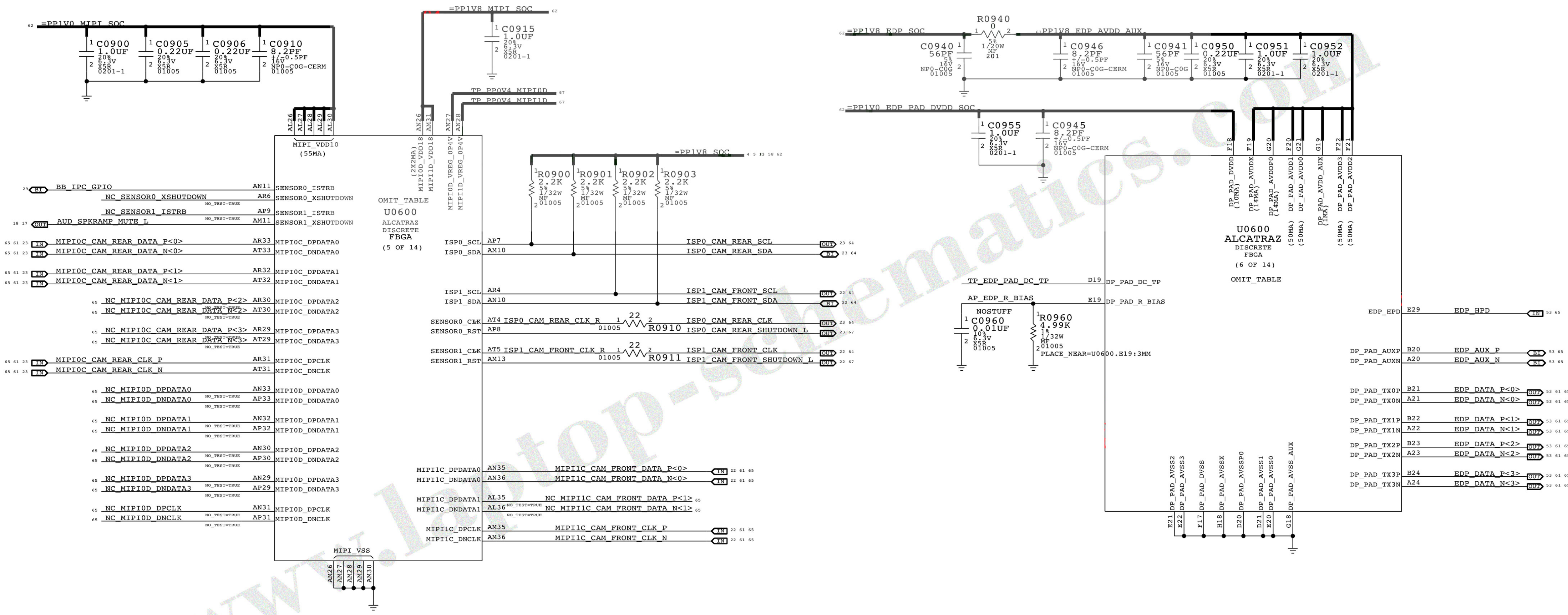
C

B

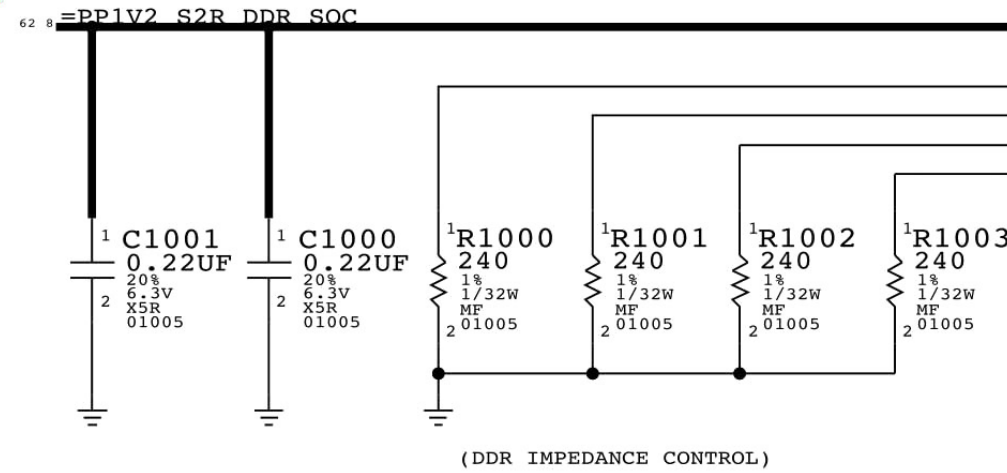
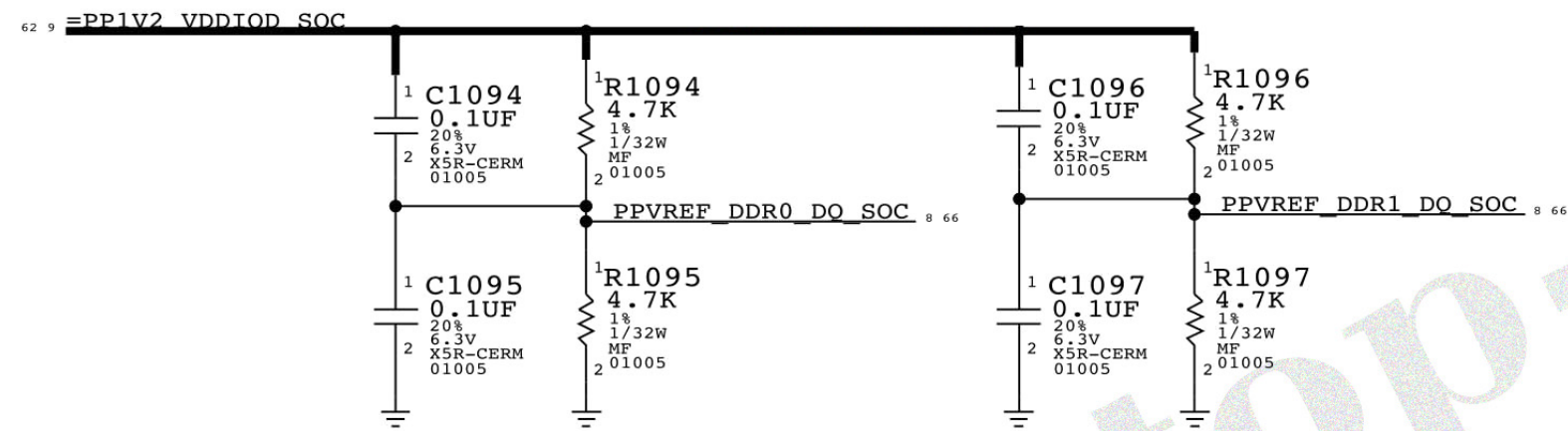
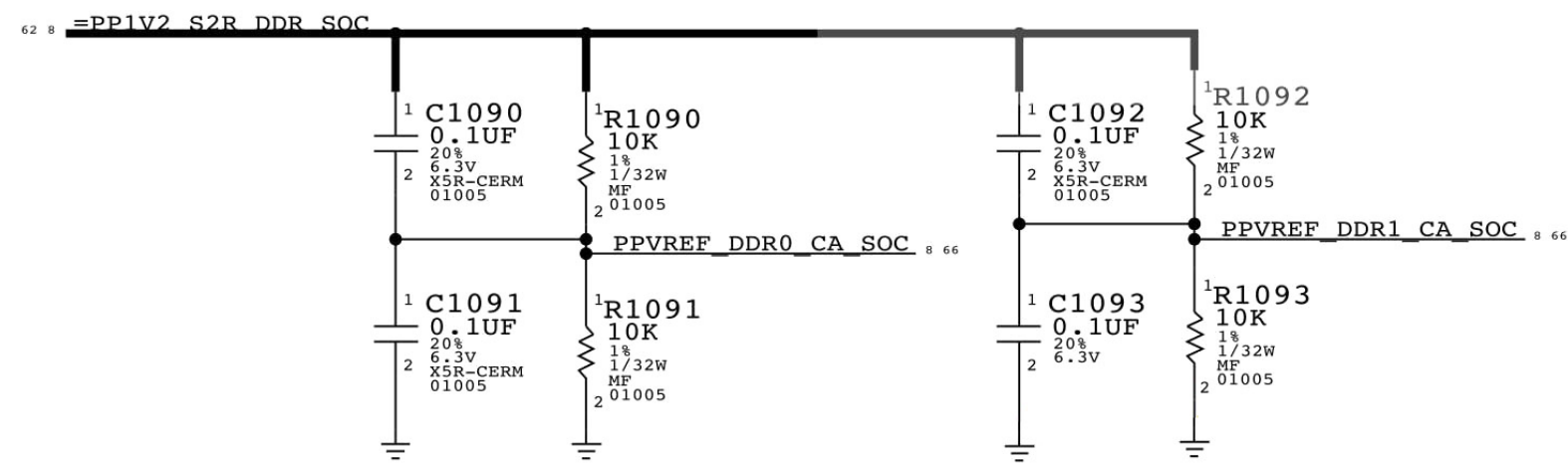
B

A





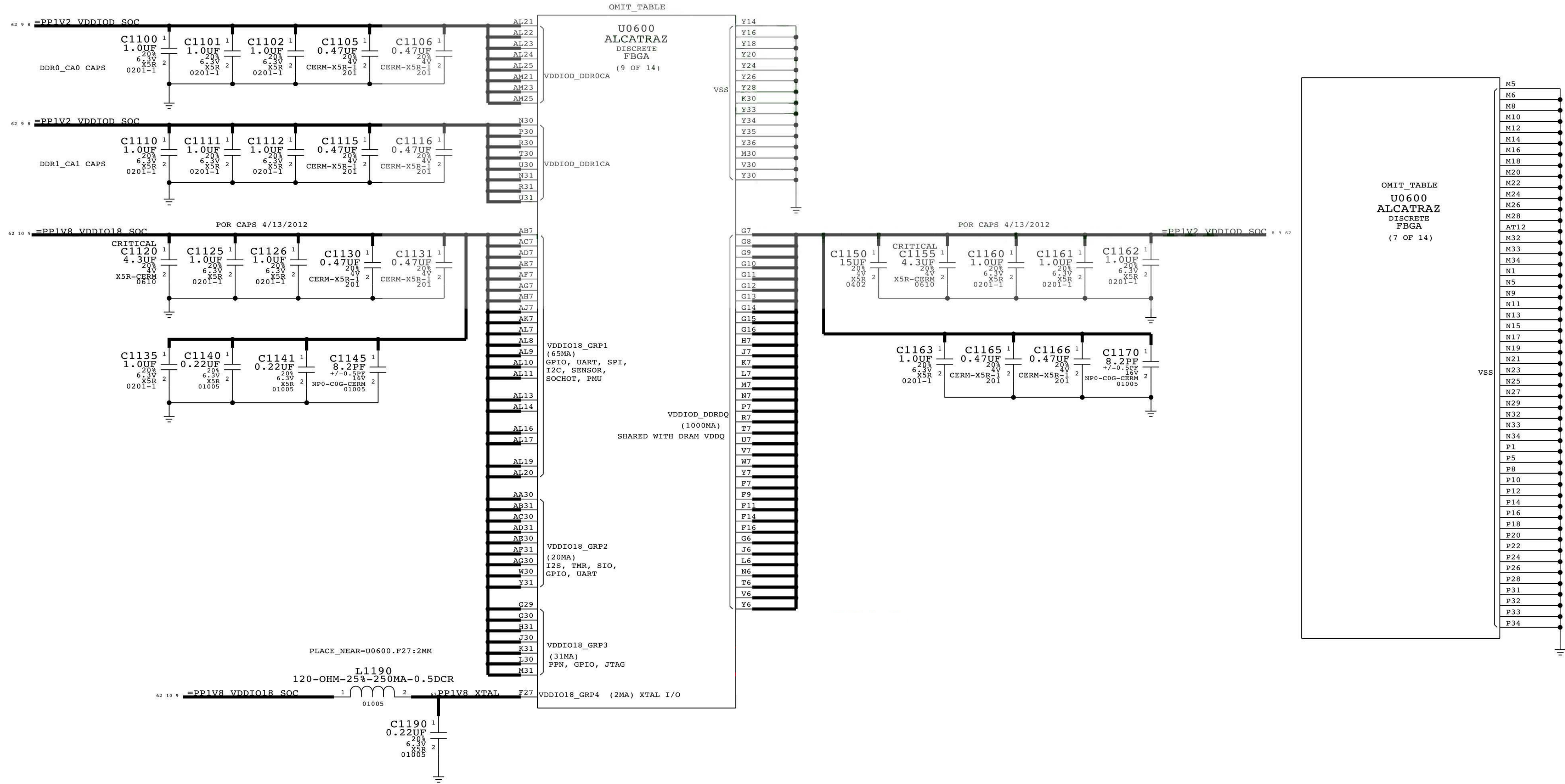
DRAWING

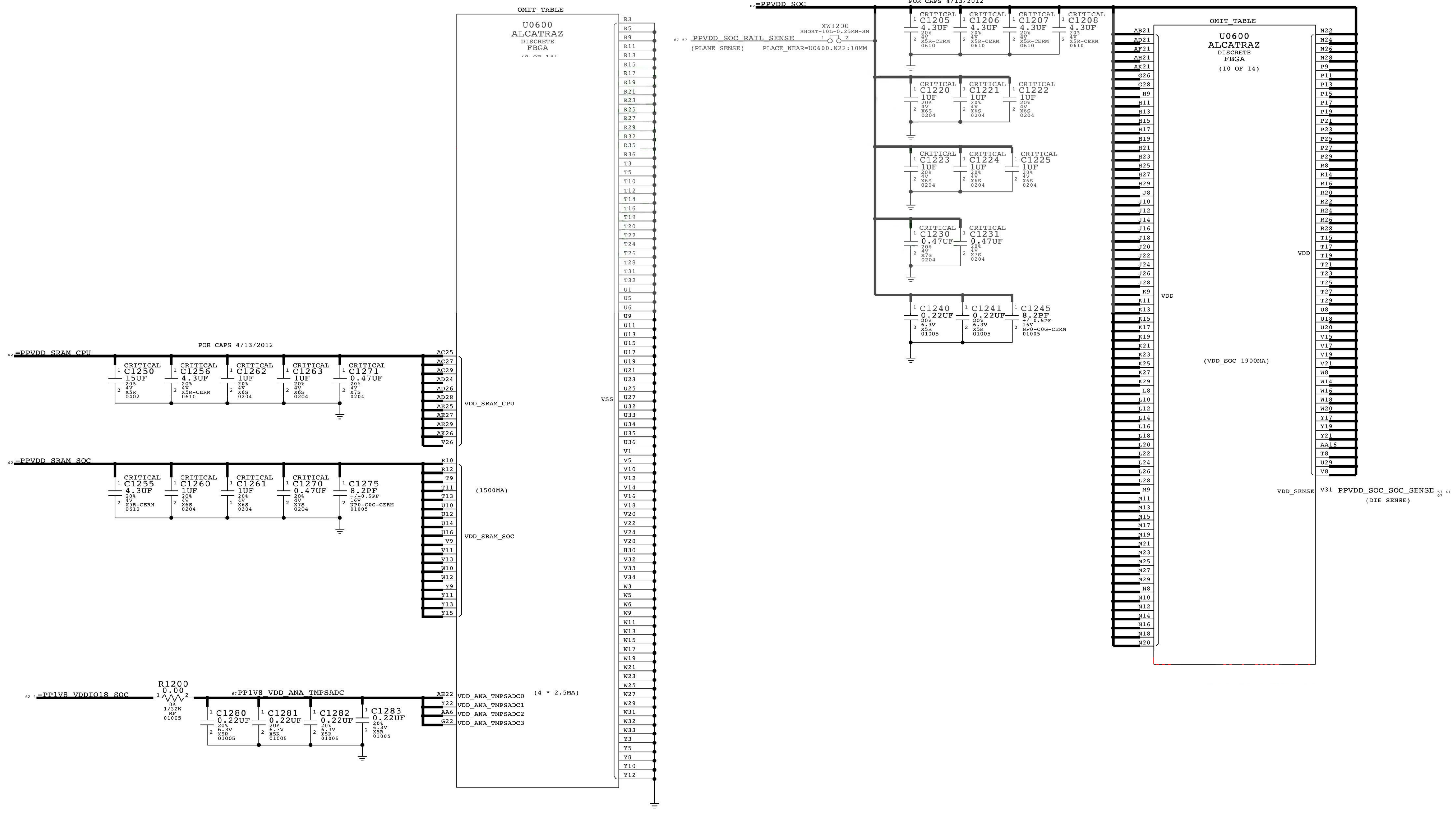


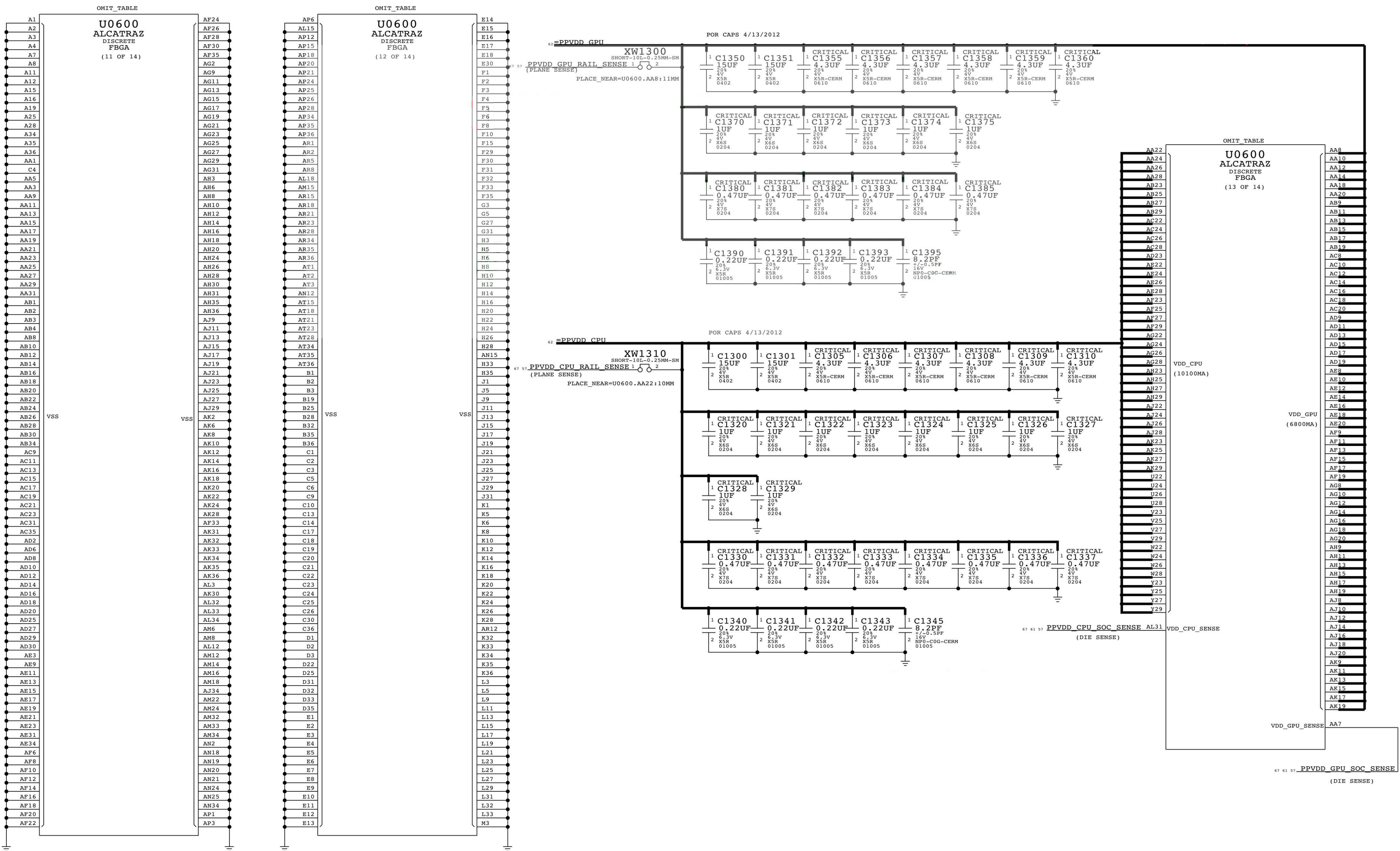
OMIT TABLE
U0600
ALCATRAZ
DISCRETE
FBGA
(14 OF 14)

66 61 12	DDRO_CA<0>	AP27	DDR0_CA0	DDR1_CA0	L34	DDR1_CA<0>	12 61 66
66 61 12	DDRO_CA<1>	AR27	DDR0_CA1	DDR1_CA1	L35	DDR1_CA<1>	12 61 66
66 61 12	DDRO_CA<2>	AT27	DDR0_CA2	DDR1_CA2	L36	DDR1_CA<2>	12 61 66
66 61 12	DDRO_CA<3>	AR26	DDR0_CA3	DDR1_CA3	M35	DDR1_CA<3>	12 61 66
66 61 12	DDRO_CA<4>	AT26	DDR0_CA4	DDR1_CA4	M36	DDR1_CA<4>	12 61 66
66 61 12	DDRO_CA<5>	AR20	DDR0_CA5	DDR1_CA5	V35	DDR1_CA<5>	12 61 66
66 61 12	DDRO_CA<6>	AT20	DDR0_CA6	DDR1_CA6	V36	DDR1_CA<6>	12 61 66
66 61 12	DDRO_CA<7>	AT19	DDR0_CA7	DDR1_CA7	W36	DDR1_CA<7>	12 61 66
66 61 12	DDRO_CA<8>	AR19	DDR0_CA8	DDR1_CA8	W35	DDR1_CA<8>	12 61 66
66 61 12	DDRO_CA<9>	AP19	DDR0_CA9	DDR1_CA9	W34	DDR1_CA<9>	12 61 66
66 61 12	DDRO_CKE<0>	AR24	DDR0_CKEU	DDR1_CKE0	P35	DDR1_CKE<0>	12 61 66
66 61 12	DDRO_CKE<1>	AT24	DDR0_CKE1	DDR1_CKE1	P36	DDR1_CKE<1>	12 61 66
66 61 12	DDRO_CSN<0>	AR25	DDR0_CSN0	DDR1_CSN0	N35	DDR1_CSN<0>	12 61 66
66 61 12	DDRO_CSN<1>	AT25	DDR0_CSN1	DDR1_CSN1	N36	DDR1_CSN<1>	12 61 66
66 61 12	DDRO_DM<0>	D11	DDR0_DM0	DDR1_DM0	P4	DDR1_DM<0>	12 61 66
66 61 12	DDRO_DM<1>	D9	DDR0_DM1	DDR1_DM1	T4	DDR1_DM<1>	12 61 66
66 61 12	DDRO_DM<2>	C15	DDR0_DM2	DDR1_DM2	K3	DDR1_DM<2>	12 61 66
66 61 12	DDRO_DM<3>	D7	DDR0_DM3	DDR1_DM3	V4	DDR1_DM<3>	12 61 66
66 61 12	DDRO_DQ<0>	B15	DDR0_DQ0	DDR1_DQ0	K2	DDR1_DQ<0>	12 61 66
66 61 12	DDRO_DQ<1>	B14	DDR0_DQ1	DDR1_DQ1	L4	DDR1_DQ<1>	12 61 66
66 61 12	DDRO_DQ<2>	B14	DDR0_DQ2	DDR1_DQ2	L2	DDR1_DQ<2>	12 61 66
66 61 12	DDRO_DQ<3>	B13	DDR0_DQ3	DDR1_DQ3	M4	DDR1_DQ<3>	12 61 66
66 61 12	DDRO_DQ<4>	B13	DDR0_DQ4	DDR1_DQ4	M2	DDR1_DQ<4>	12 61 66
66 61 12	DDRO_DQ<5>	D12	DDR0_DQ5	DDR1_DQ5	N4	DDR1_DQ<5>	12 61 66
66 61 12	DDRO_DQ<6>	C12	DDR0_DQ6	DDR1_DQ6	N3	DDR1_DQ<6>	12 61 66
66 61 12	DDRO_DQ<7>	B12	DDR0_DQ7	DDR1_DQ7	N2	DDR1_DQ<7>	12 61 66
66 61 12	DDRO_DQ<8>	C11	DDR0_DQ8	DDR1_DQ8	P3	DDR1_DQ<8>	12 61 66
66 61 12	DDRO_DQ<9>	B11	DDR0_DQ9	DDR1_DQ9	P2	DDR1_DQ<9>	12 61 66
66 61 12	DDRO_DQ<10>	D10	DDR0_DQ10	DDR1_DQ10	R4	DDR1_DQ<10>	12 61 66
66 61 12	DDRO_DQ<11>	B10	DDR0_DQ11	DDR1_DQ11	R2	DDR1_DQ<11>	12 61 66
66 61 12	DDRO_DQ<12>	B9	DDR0_DQ12	DDR1_DQ12	T2	DDR1_DQ<12>	12 61 66
66 61 12	DDRO_DQ<13>	D8	DDR0_DQ13	DDR1_DQ13	U4	DDR1_DQ<13>	12 61 66
66 61 12	DDRO_DQ<14>	C8	DDR0_DQ14	DDR1_DQ14	U3	DDR1_DQ<14>	12 61 66
66 61 12	DDRO_DQ<15>	B8	DDR0_DQ15	DDR1_DQ15	U2	DDR1_DQ<15>	12 61 66
66 61 12	DDRO_DQ<16>	D18	DDR0_DQ16	DDR1_DQ16	G4	DDR1_DQ<16>	12 61 66
66 61 12	DDRO_DQ<17>	B18	DDR0_DQ17	DDR1_DQ17	G2	DDR1_DQ<17>	12 61 66
66 61 12	DDRO_DQ<18>	D17	DDR0_DQ18	DDR1_DQ18	H4	DDR1_DQ<18>	12 61 66
66 61 12	DDRO_DQ<19>	B17	DDR0_DQ19	DDR1_DQ19	H2	DDR1_DQ<19>	12 61 66
66 61 12	DDRO_DQ<20>	D16	DDR0_DQ20	DDR1_DQ20	J4	DDR1_DQ<20>	12 61 66
66 61 12	DDRO_DQ<21>	C16	DDR0_DQ21	DDR1_DQ21	J3	DDR1_DQ<21>	12 61 66
66 61 12	DDRO_DQ<22>	B16	DDR0_DQ22	DDR1_DQ22	J2	DDR1_DQ<22>	12 61 66
66 61 12	DDRO_DQ<23>	D15	DDR0_DQ23	DDR1_DQ23	K4	DDR1_DQ<23>	12 61 66
66 61 12	DDRO_DQ<24>	C7	DDR0_DQ24	DDR1_DQ24	V3	DDR1_DQ<24>	12 61 66
66 61 12	DDRO_DQ<25>	B7	DDR0_DQ25	DDR1_DQ25	V2	DDR1_DQ<25>	12 61 66
66 61 12	DDRO_DQ<26>	D6	DDR0_DQ26	DDR1_DQ26	W4	DDR1_DQ<26>	12 61 66
66 61 12	DDRO_DQ<27>	B6	DDR0_DQ27	DDR1_DQ27	W2	DDR1_DQ<27>	12 61 66
66 61 12	DDRO_DQ<28>	D5	DDR0_DQ28	DDR1_DQ28	Y4	DDR1_DQ<28>	12 61 66
66 61 12	DDRO_DQ<29>	B5	DDR0_DQ29	DDR1_DQ29	Y2	DDR1_DQ<29>	12 61 66
66 61 12	DDRO_DQ<30>	D4	DDR0_DQ30	DDR1_DQ30	AA4	DDR1_DQ<30>	12 61 66
66 61 12	DDRO_DQ<31>	B4	DDR0_DQ31	DDR1_DQ31	AA2	DDR1_DQ<31>	12 61 66
66 61 12	DDRO_DQS_P<0>	A14	DDR0_PDQS0	DDR1_PDQS0	L1	DDR1_DQS_P<0>	12 61 66
66 61 12	DDRO_DQS_P<1>	A9	DDR0_PDQS1	DDR1_PDQS1	T1	DDR1_DQS_P<1>	12 61 66
66 61 12	DDRO_DQS_P<2>	A18	DDR0_PDQS2	DDR1_PDQS2	G1	DDR1_DQS_P<2>	12 61 66
66 61 12	DDRO_DQS_P<3>	A5	DDR0_PDQS3	DDR1_PDQS3	Y1	DDR1_DQS_P<3>	12 61 66
66 61 12	DDRO_DQS_N<0>	A13	DDR0_NDQS0	DDR1_NDQS0	M1	DDR1_DQS_N<0>	12 61 66
66 61 12	DDRO_DQS_N<1>	A10	DDR0_NDQS1	DDR1_NDQS1	R1	DDR1_DQS_N<1>	12 61 66
66 61 12	DDRO_DQS_N<2>	A17	DDR0_NDQS2	DDR1_NDQS2	H1	DDR1_DQS_N<2>	12 61 66
66 61 12	DDRO_DQS_N<3>	A6	DDR0_NDQS3	DDR1_NDQS3	W1	DDR1_DQS_N<3>	12 61 66
66 61 12	DDRO_CK_P	AT22	DDR0_CK	DDR1_CK	T36	DDR1_CK_P	12 61 66
66 61 12	DDRO_CK_N	AR22	DDR0_CKB	DDR1_CKB	T35	DDR1_CK_N	12 61 66

AP23	DDRO_VDD_CKE	DDR0_VDD_CKE	(<1MA EACH)
R34	DDR1_VDD_CKE		
AN22	DDRO_RREF_CA	DDR0_RREF_CA	
T33	DDR1_RREF_CA	DDR1_RREF_CA	
F12	DDRO_RREF_DQ	DDR0_RREF_DQ	
R6	DDR1_RREF_DQ	DDR1_RREF_DQ	
AP22	PPVREF_DDR0_CA_SOC	DDR0_VREF_CA	
T34	PPVREF_DDR1_CA_SOC	DDR1_VREF_CA	
F13	PPVREF_DDR0_DO_SOC	DDR0_VREF_DQ	
P6	PPVREF_DDR1_DO_SOC	DDR1_VREF_DQ	







OMIT_TABLE
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 FBGA
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OMIT_TABLE
U0600
 ALCATRAZ
 DISCRETE
 FBGA
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D

D

C

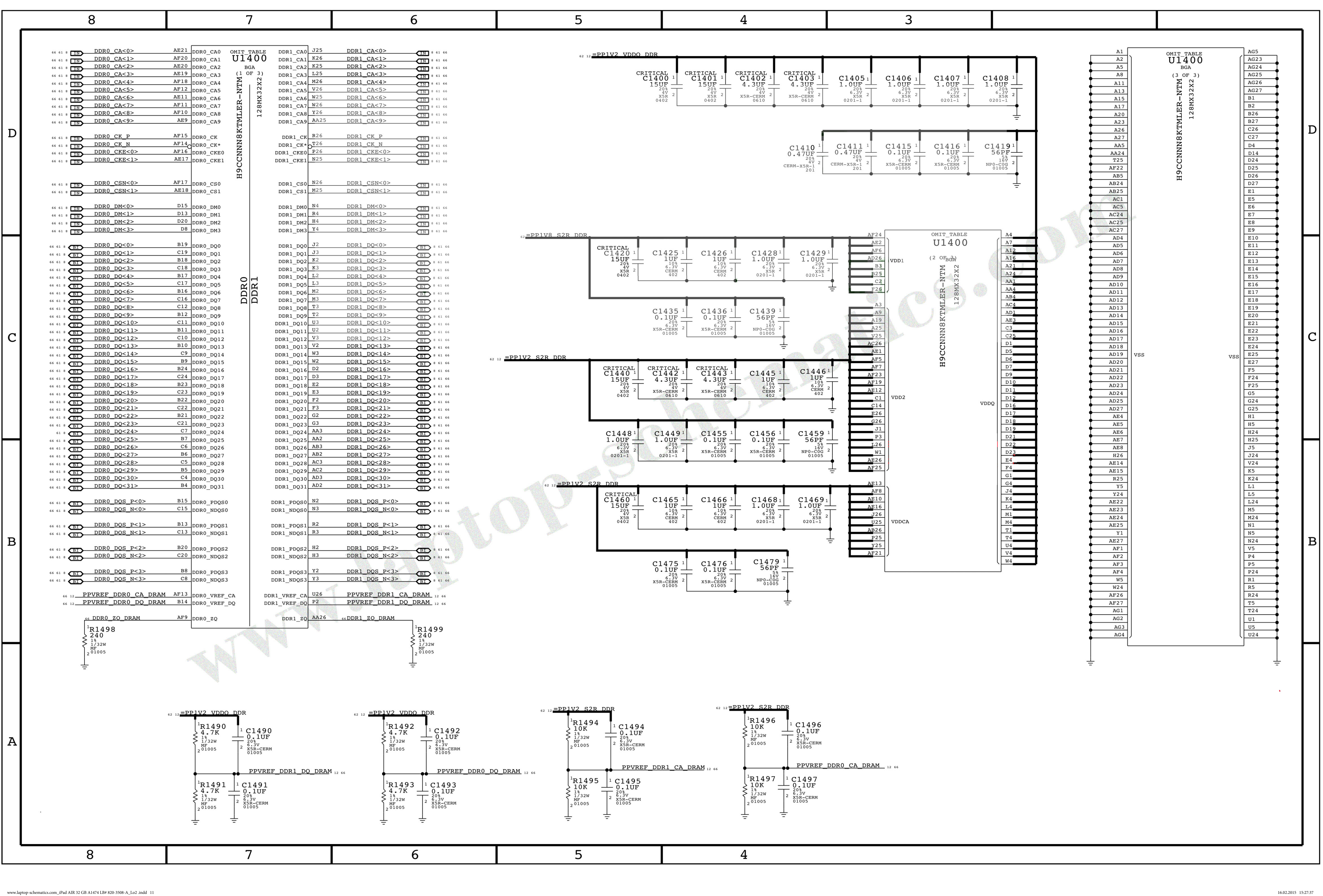
C

B

B

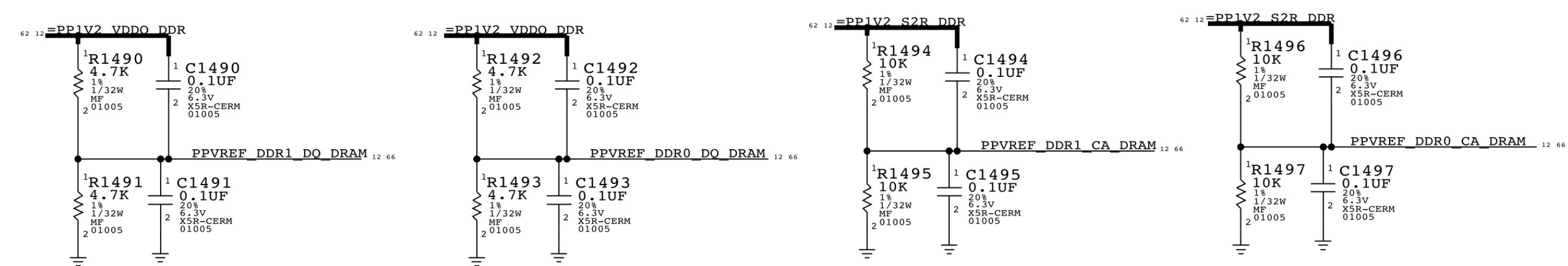
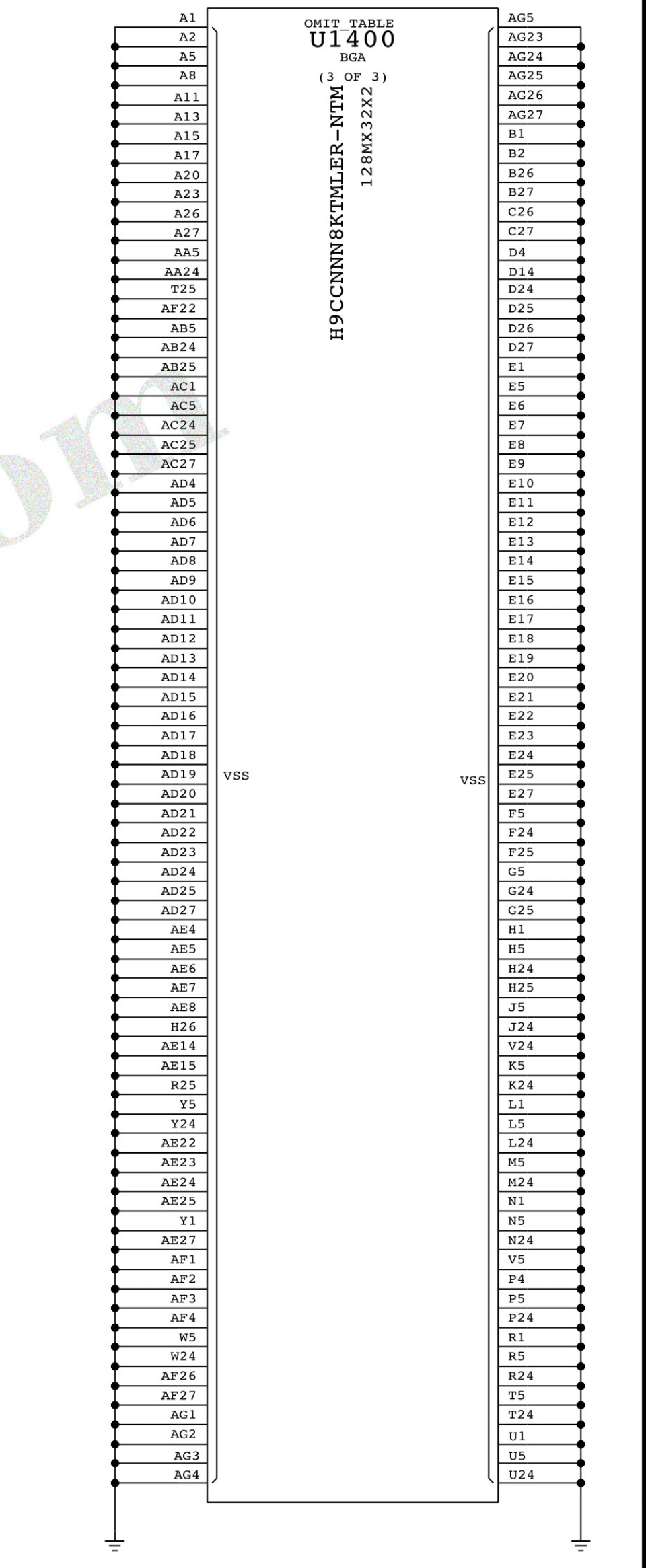
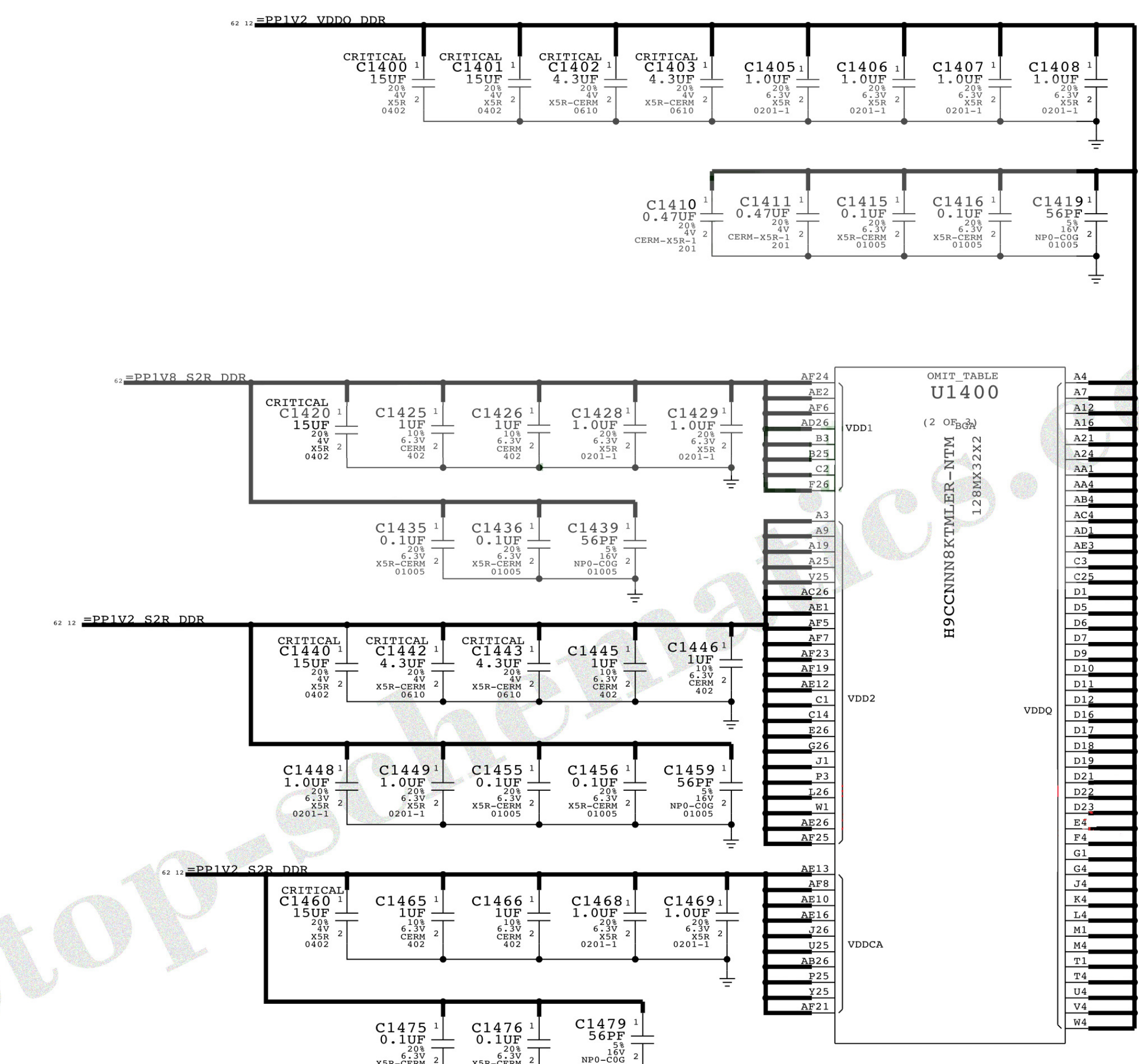
A

A



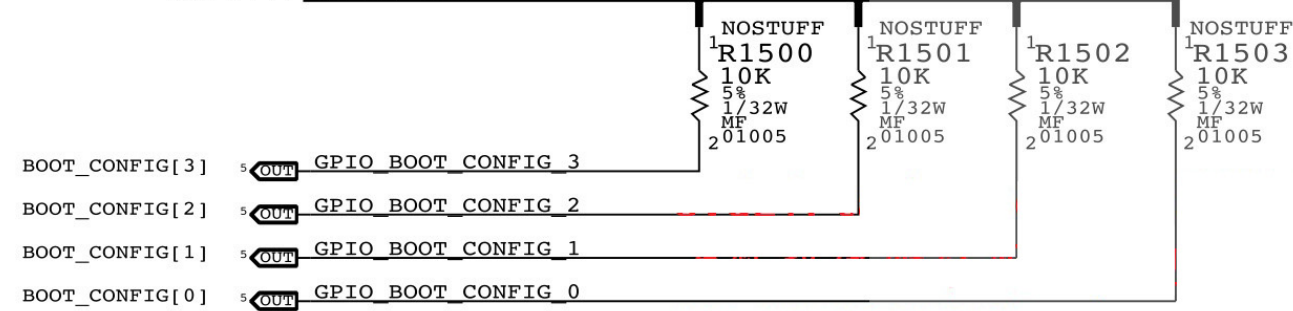
66 61 8	DDR0_CA<0>	AE21	DDR0_CA0
66 61 8	DDR0_CA<1>	AF20	DDR0_CA1
66 61 8	DDR0_CA<2>	AE20	DDR0_CA2
66 61 8	DDR0_CA<3>	AE19	DDR0_CA3
66 61 8	DDR0_CA<4>	AF18	DDR0_CA4
66 61 8	DDR0_CA<5>	AF12	DDR0_CA5
66 61 8	DDR0_CA<6>	AE11	DDR0_CA6
66 61 8	DDR0_CA<7>	AF11	DDR0_CA7
66 61 8	DDR0_CA<8>	AF10	DDR0_CA8
66 61 8	DDR0_CA<9>	AE9	DDR0_CA9
66 61 8	DDR0_CK_P	AF15	DDR0_CK
66 61 8	DDR0_CK_N	AF14	DDR0_CK*
66 61 8	DDR0_CKE<0>	AF16	DDR0_CKE0
66 61 8	DDR0_CKE<1>	AE17	DDR0_CKE1
66 61 8	DDR0_CSN<0>	AF17	DDR0_CS0
66 61 8	DDR0_CSN<1>	AE18	DDR0_CS1
66 61 8	DDR0_DM<0>	D15	DDR0_DM0
66 61 8	DDR0_DM<1>	D13	DDR0_DM1
66 61 8	DDR0_DM<2>	D20	DDR0_DM2
66 61 8	DDR0_DM<3>	D8	DDR0_DM3
66 61 8	DDR0_DQ<0>	B19	DDR0_DQ0
66 61 8	DDR0_DQ<1>	C19	DDR0_DQ1
66 61 8	DDR0_DQ<2>	B18	DDR0_DQ2
66 61 8	DDR0_DQ<3>	C18	DDR0_DQ3
66 61 8	DDR0_DQ<4>	B17	DDR0_DQ4
66 61 8	DDR0_DQ<5>	C17	DDR0_DQ5
66 61 8	DDR0_DQ<6>	B16	DDR0_DQ6
66 61 8	DDR0_DQ<7>	C16	DDR0_DQ7
66 61 8	DDR0_DQ<8>	C12	DDR0_DQ8
66 61 8	DDR0_DQ<9>	B12	DDR0_DQ9
66 61 8	DDR0_DQ<10>	C11	DDR0_DQ10
66 61 8	DDR0_DQ<11>	B11	DDR0_DQ11
66 61 8	DDR0_DQ<12>	C10	DDR0_DQ12
66 61 8	DDR0_DQ<13>	B10	DDR0_DQ13
66 61 8	DDR0_DQ<14>	C9	DDR0_DQ14
66 61 8	DDR0_DQ<15>	B9	DDR0_DQ15
66 61 8	DDR0_DQ<16>	B24	DDR0_DQ16
66 61 8	DDR0_DQ<17>	C24	DDR0_DQ17
66 61 8	DDR0_DQ<18>	B23	DDR0_DQ18
66 61 8	DDR0_DQ<19>	C23	DDR0_DQ19
66 61 8	DDR0_DQ<20>	B22	DDR0_DQ20
66 61 8	DDR0_DQ<21>	C22	DDR0_DQ21
66 61 8	DDR0_DQ<22>	B21	DDR0_DQ22
66 61 8	DDR0_DQ<23>	C21	DDR0_DQ23
66 61 8	DDR0_DQ<24>	C7	DDR0_DQ24
66 61 8	DDR0_DQ<25>	B7	DDR0_DQ25
66 61 8	DDR0_DQ<26>	C6	DDR0_DQ26
66 61 8	DDR0_DQ<27>	B6	DDR0_DQ27
66 61 8	DDR0_DQ<28>	C5	DDR0_DQ28
66 61 8	DDR0_DQ<29>	B5	DDR0_DQ29
66 61 8	DDR0_DQ<30>	C4	DDR0_DQ30
66 61 8	DDR0_DQ<31>	B4	DDR0_DQ31
66 61 8	DDR0_DQS_P<0>	B15	DDR0_PDQS0
66 61 8	DDR0_DQS_N<0>	C15	DDR0_NDQS0
66 61 8	DDR0_DQS_P<1>	B13	DDR0_PDQS1
66 61 8	DDR0_DQS_N<1>	C13	DDR0_NDQS1
66 61 8	DDR0_DQS_P<2>	B20	DDR0_PDQS2
66 61 8	DDR0_DQS_N<2>	C20	DDR0_NDQS2
66 61 8	DDR0_DQS_P<3>	B8	DDR0_PDQS3
66 61 8	DDR0_DQS_N<3>	C8	DDR0_NDQS3
66 12	PPVREF_DDR0_CA_DRAM	AF13	DDR0_VREF_CA
66 12	PPVREF_DDR0_DO_DRAM	B14	DDR0_VREF_DO
66 12	PPVREF_DDR1_CA_DRAM	U26	DDR1_VREF_CA
66 12	PPVREF_DDR1_DO_DRAM	F2	DDR1_VREF_DO
66 12	PPVREF_DDR1_QO_DRAM	AA26	DDR1_VREF_QO

DDR1_CA0	J25	DDR1_CA<0>	66 61 66
DDR1_CA1	K26	DDR1_CA<1>	66 61 66
DDR1_CA2	K25	DDR1_CA<2>	66 61 66
DDR1_CA3	L25	DDR1_CA<3>	66 61 66
DDR1_CA4	M26	DDR1_CA<4>	66 61 66
DDR1_CA5	V26	DDR1_CA<5>	66 61 66
DDR1_CA6	W25	DDR1_CA<6>	66 61 66
DDR1_CA7	W26	DDR1_CA<7>	66 61 66
DDR1_CA8	Y26	DDR1_CA<8>	66 61 66
DDR1_CA9	AA25	DDR1_CA<9>	66 61 66
DDR1_CK	R26	DDR1_CK_P	66 61 66
DDR1_CK*	T26	DDR1_CK_N	66 61 66
DDR1_CKE0	F26	DDR1_CKE<0>	66 61 66
DDR1_CKE1	N25	DDR1_CKE<1>	66 61 66
DDR1_CS0	N26	DDR1_CSN<0>	66 61 66
DDR1_CS1	M25	DDR1_CSN<1>	66 61 66
DDR1_DM0	N4	DDR1_DM<0>	66 61 66
DDR1_DM1	R4	DDR1_DM<1>	66 61 66
DDR1_DM2	H4	DDR1_DM<2>	66 61 66
DDR1_DM3	Y4	DDR1_DM<3>	66 61 66
DDR1_DQ0	J2	DDR1_DQ<0>	66 61 66
DDR1_DQ1	J3	DDR1_DQ<1>	66 61 66
DDR1_DQ2	K2	DDR1_DQ<2>	66 61 66
DDR1_DQ3	K3	DDR1_DQ<3>	66 61 66
DDR1_DQ4	L2	DDR1_DQ<4>	66 61 66
DDR1_DQ5	L3	DDR1_DQ<5>	66 61 66
DDR1_DQ6	M2	DDR1_DQ<6>	66 61 66
DDR1_DQ7	M3	DDR1_DQ<7>	66 61 66
DDR1_DQ8	T3	DDR1_DQ<8>	66 61 66
DDR1_DQ9	T2	DDR1_DQ<9>	66 61 66
DDR1_DQ10	U3	DDR1_DQ<10>	66 61 66
DDR1_DQ11	U2	DDR1_DQ<11>	66 61 66
DDR1_DQ12	V3	DDR1_DQ<12>	66 61 66
DDR1_DQ13	V2	DDR1_DQ<13>	66 61 66
DDR1_DQ14	W3	DDR1_DQ<14>	66 61 66
DDR1_DQ15	W2	DDR1_DQ<15>	66 61 66
DDR1_DQ16	D2	DDR1_DQ<16>	66 61 66
DDR1_DQ17	D3	DDR1_DQ<17>	66 61 66
DDR1_DQ18	E2	DDR1_DQ<18>	66 61 66
DDR1_DQ19	E3	DDR1_DQ<19>	66 61 66
DDR1_DQ20	F2	DDR1_DQ<20>	66 61 66
DDR1_DQ21	F3	DDR1_DQ<21>	66 61 66
DDR1_DQ22	G2	DDR1_DQ<22>	66 61 66
DDR1_DQ23	G3	DDR1_DQ<23>	66 61 66
DDR1_DQ24	AA3	DDR1_DQ<24>	66 61 66
DDR1_DQ25	AA2	DDR1_DQ<25>	66 61 66
DDR1_DQ26	AB3	DDR1_DQ<26>	66 61 66
DDR1_DQ27	AB2	DDR1_DQ<27>	66 61 66
DDR1_DQ28	AC3	DDR1_DQ<28>	66 61 66
DDR1_DQ29	AC2	DDR1_DQ<29>	66 61 66
DDR1_DQ30	AD3	DDR1_DQ<30>	66 61 66
DDR1_DQ31	AD2	DDR1_DQ<31>	66 61 66



BOOT CONFIG ID

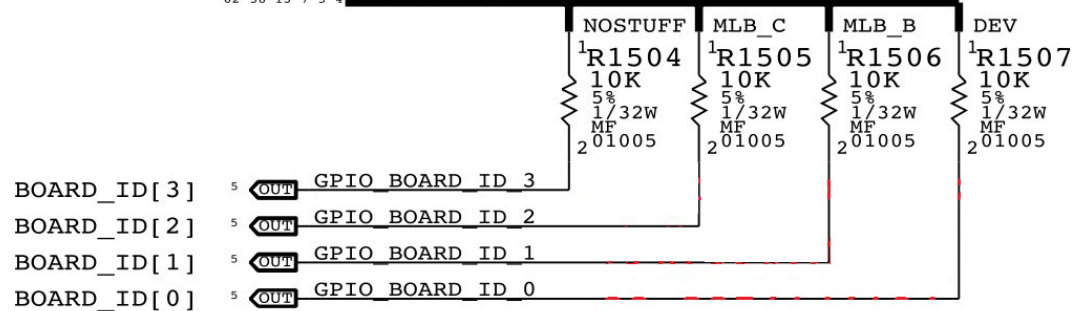
62 58 13 7 5 4 =PP1V8 SOC



BOOT_CONFIG[3:0]	MODE	S/W READ FLOW
0000	SPI	1. SET GPIO AS INPUT
0001	SPI W/TEST	2. DISABLE PU AND ENABLE PD
0010	NAND <-- CURRENT SETTING	3. READ
0011	NAND W/TEST	

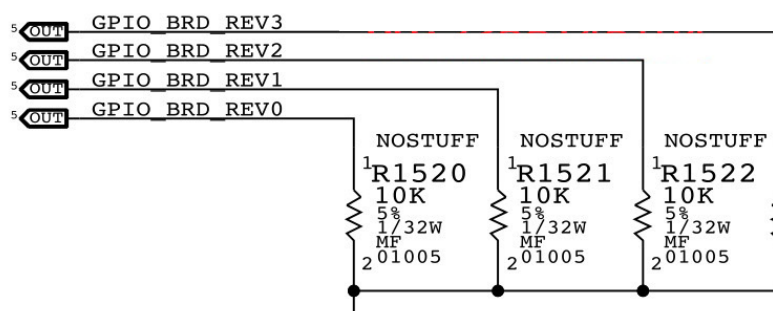
BOARD ID

62 58 13 7 5 4 =PP1V8 SOC



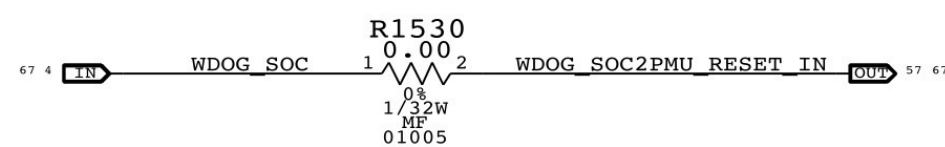
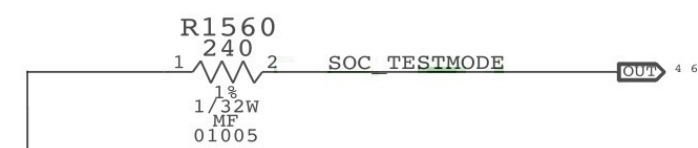
BOARD_ID[3-0]	S/W READ FLOW
0000	MLB_A AP
0001	MLB_A DEV
0010	MLB_B AP
0011	MLB_B DEV
0100	MLB_C AP
0101	MLB_C DEV

BOARD REVISION

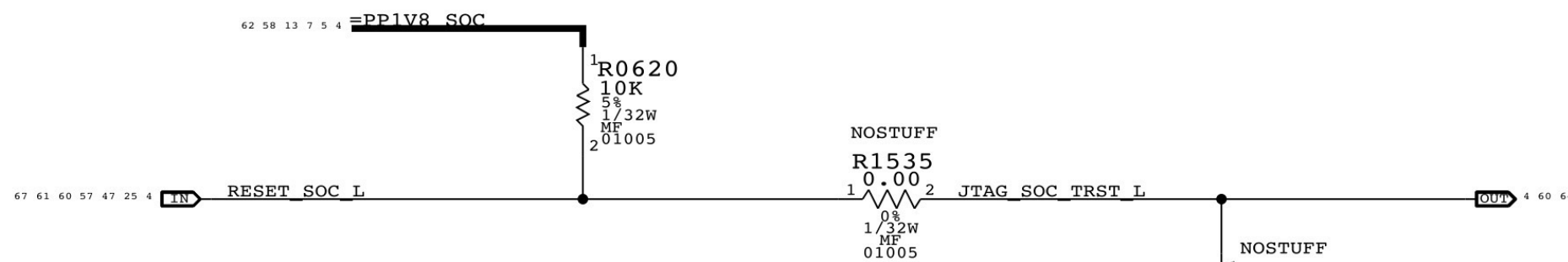
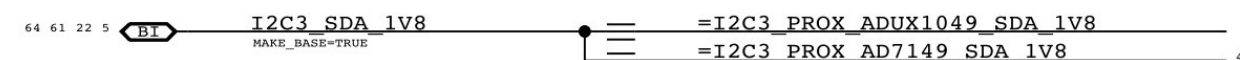
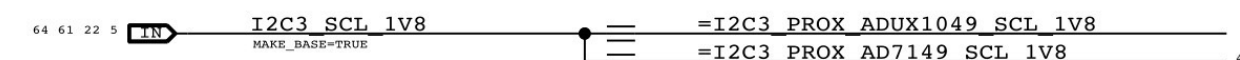


BRD_REV[3-0]	S/W READ FLOW
0000	PROTO 0
0001	PROTO 0 + T2
0010	PROTO 1 + T2
0011	PROTO 1 + T1
0100	PROTO 1 + T1 + B0
0101	PROTO 2 + T2 + B0
0110	EVT + T2 + B0
0111	DVT + T2 + B1

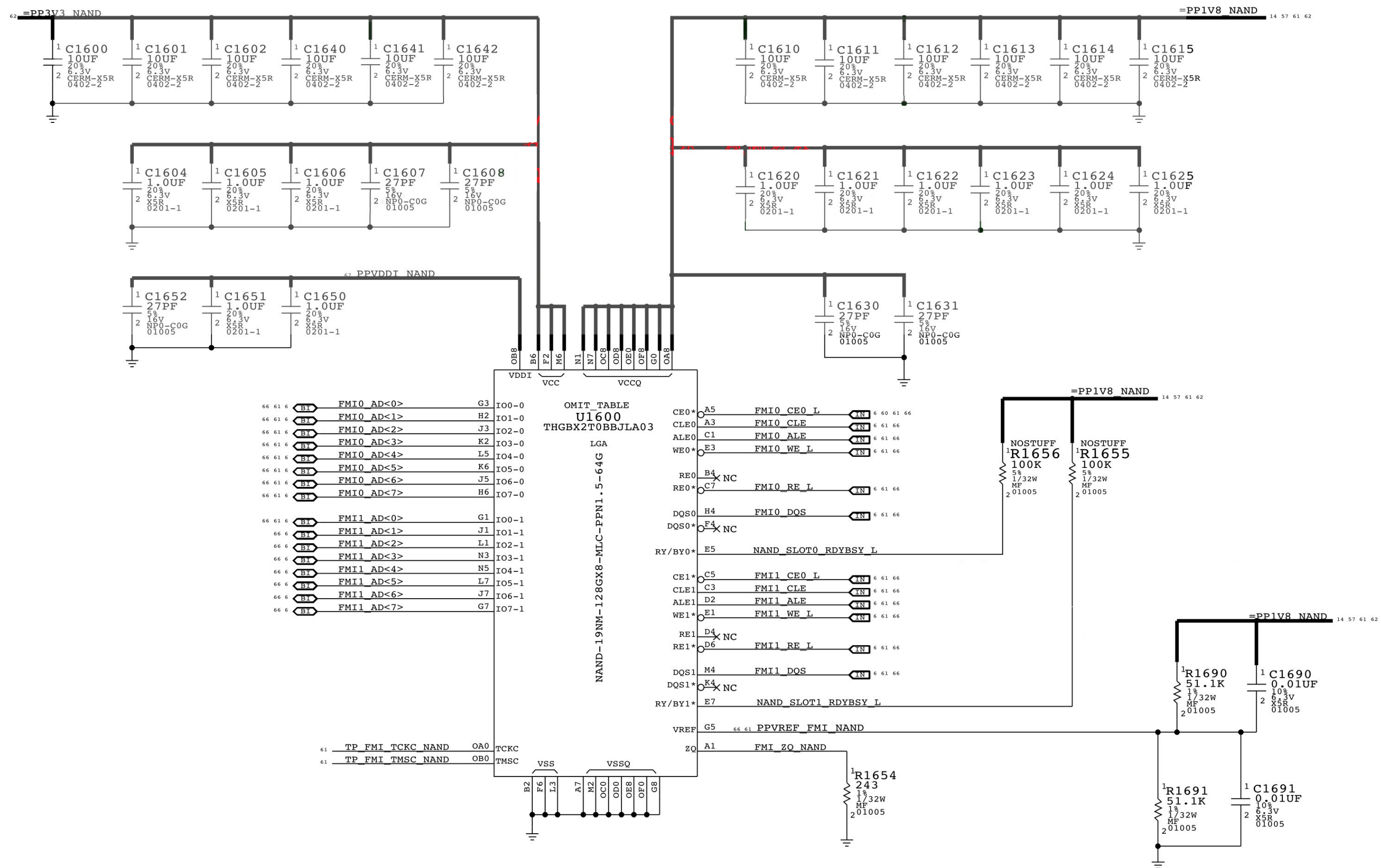
JTAG



ALIASED NETS TO ALLOW BREAKING ON DEV BOARD



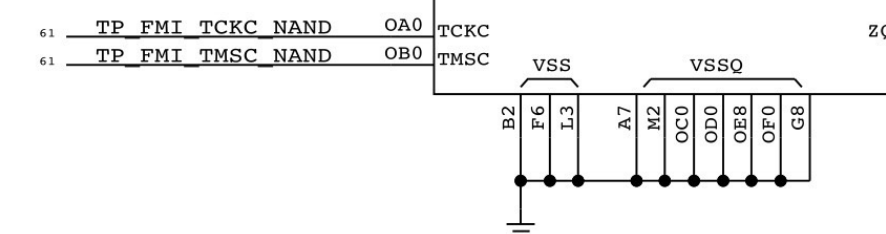
NOTE: WHEN USING A0 SOC
 STUFF R1535
 NOSTUFF R1536
 CHANGE R0620 TO 4.7K



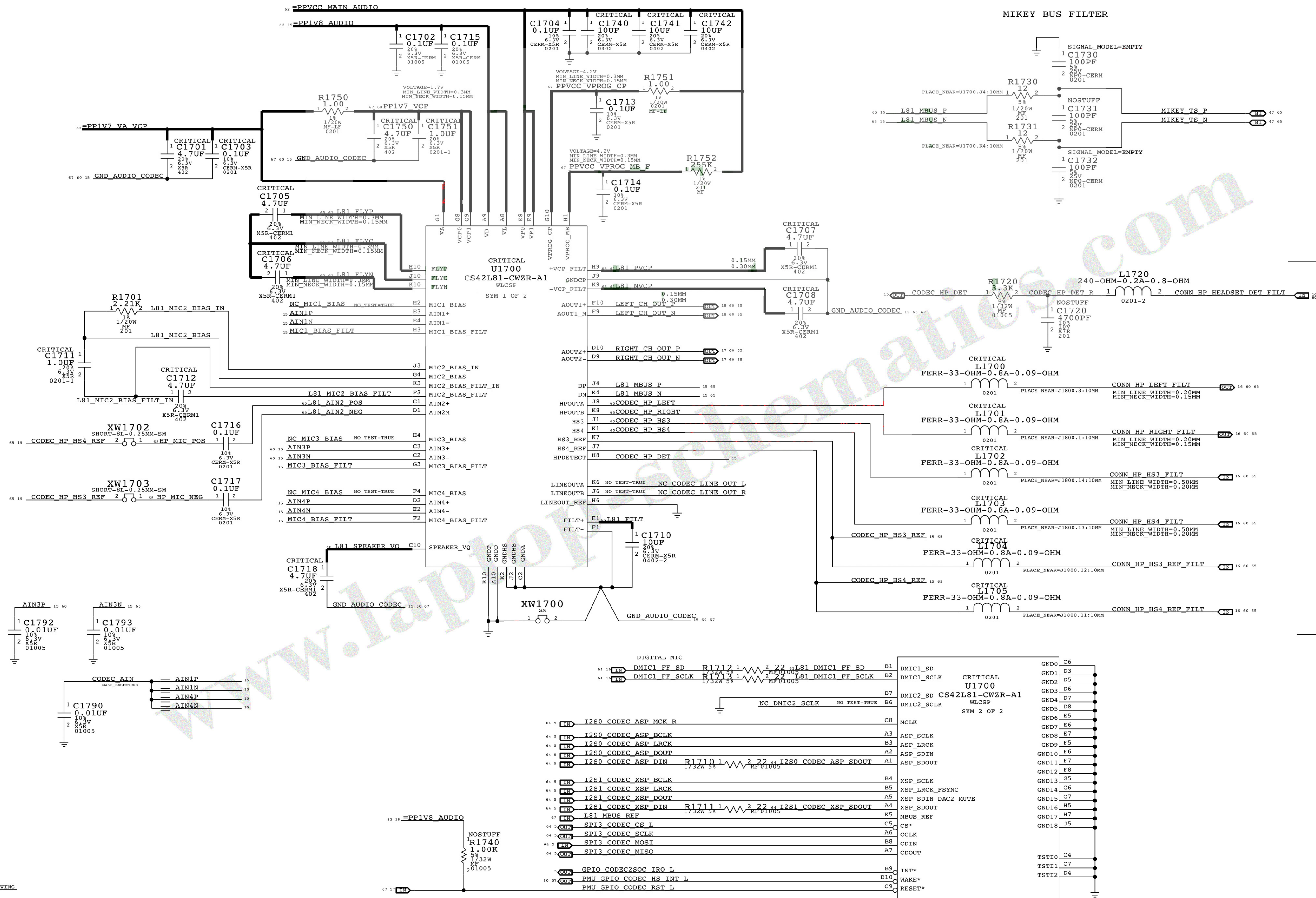
OMIT_TABLE
U1600
THGBX2T0BBJLA03

LGA
NAND-19NM-128GX8-MLC-PPN1.5-64G

66 61	B	FMI0_AD<0>	G3	I00-0
66 61	B	FMI0_AD<1>	H2	I01-0
66 61	B	FMI0_AD<2>	J3	I02-0
66 61	B	FMI0_AD<3>	K2	I03-0
66 61	B	FMI0_AD<4>	L5	I04-0
66 61	B	FMI0_AD<5>	K6	I05-0
66 61	B	FMI0_AD<6>	J5	I06-0
66 61	B	FMI0_AD<7>	H6	I07-0
66 61	B	FMI1_AD<0>	G1	I00-1
66 61	B	FMI1_AD<1>	J1	I01-1
66 61	B	FMI1_AD<2>	L1	I02-1
66 61	B	FMI1_AD<3>	N3	I03-1
66 61	B	FMI1_AD<4>	N5	I04-1
66 61	B	FMI1_AD<5>	L7	I05-1
66 61	B	FMI1_AD<6>	J7	I06-1
66 61	B	FMI1_AD<7>	G7	I07-1



NOTE: U1900 DECAPS CHANGED ON 5/24/12 PER RDAR://PROBLEM/11485846

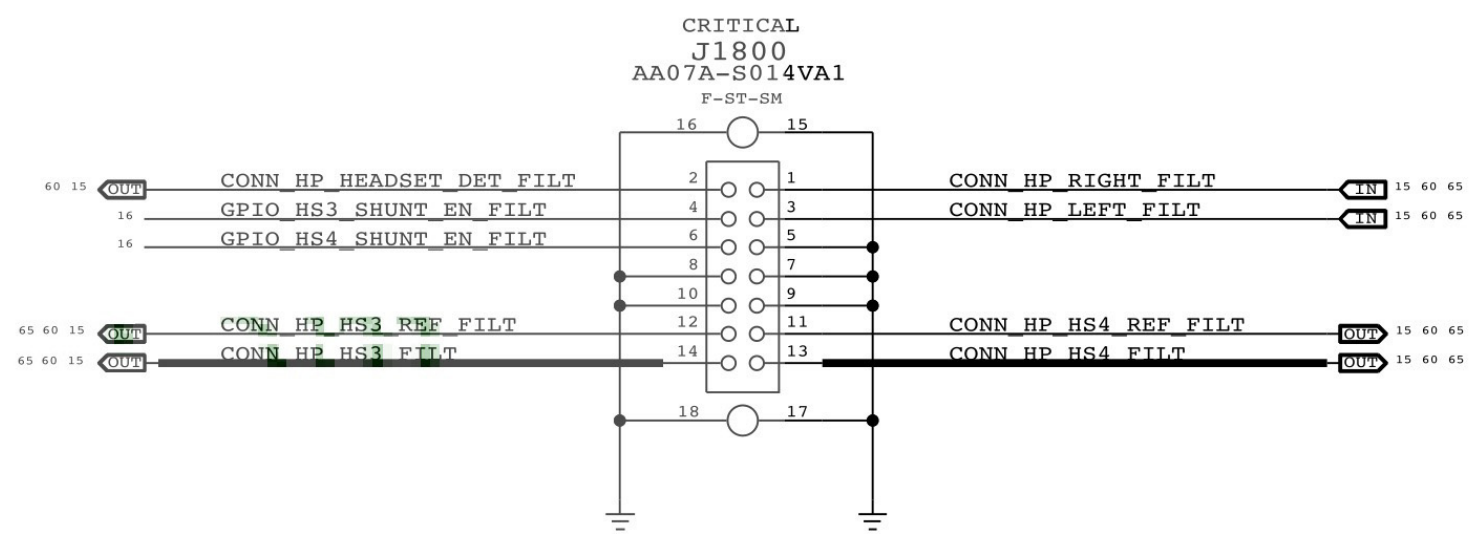


TO HEADPHONE JACK

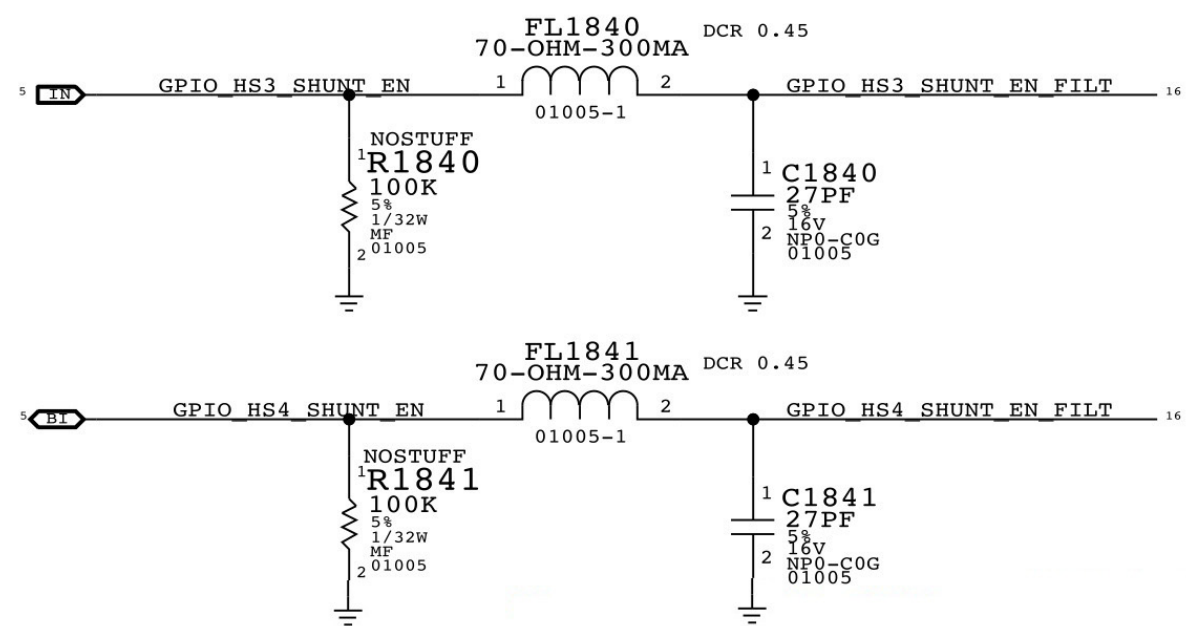
DRAWING

HP JACK B2B CONNECTOR

J1800 MATCHES AUDIO_JACK_FLEX_3.0.0 1/9/13
MLB: 516S1084
FLEX: 516S1085



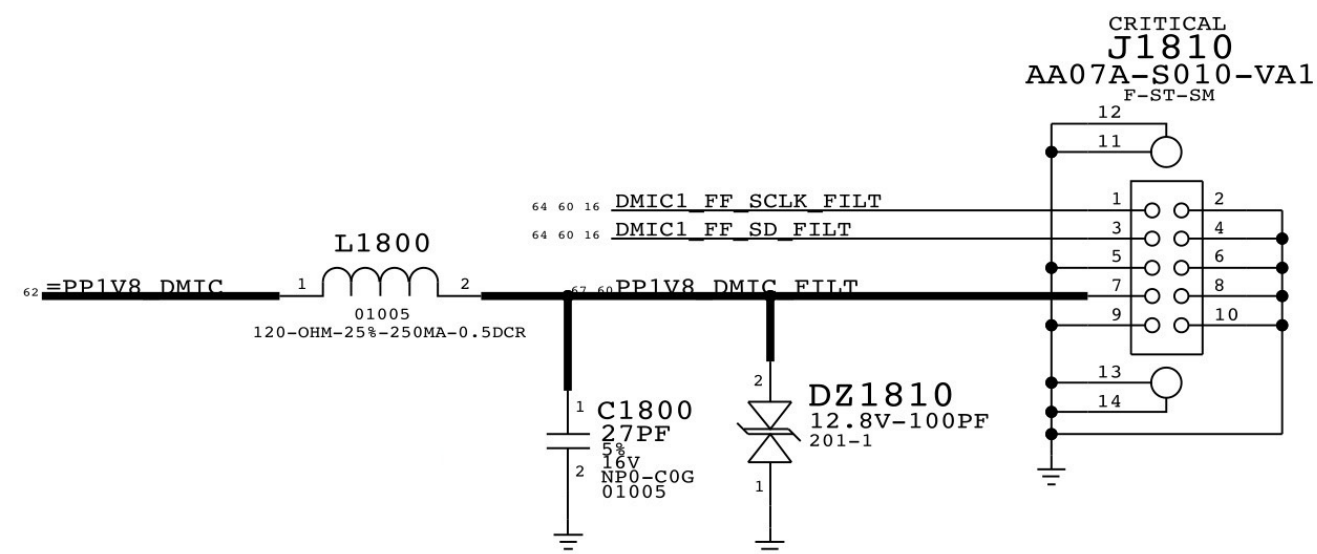
SHUNT FILTERS



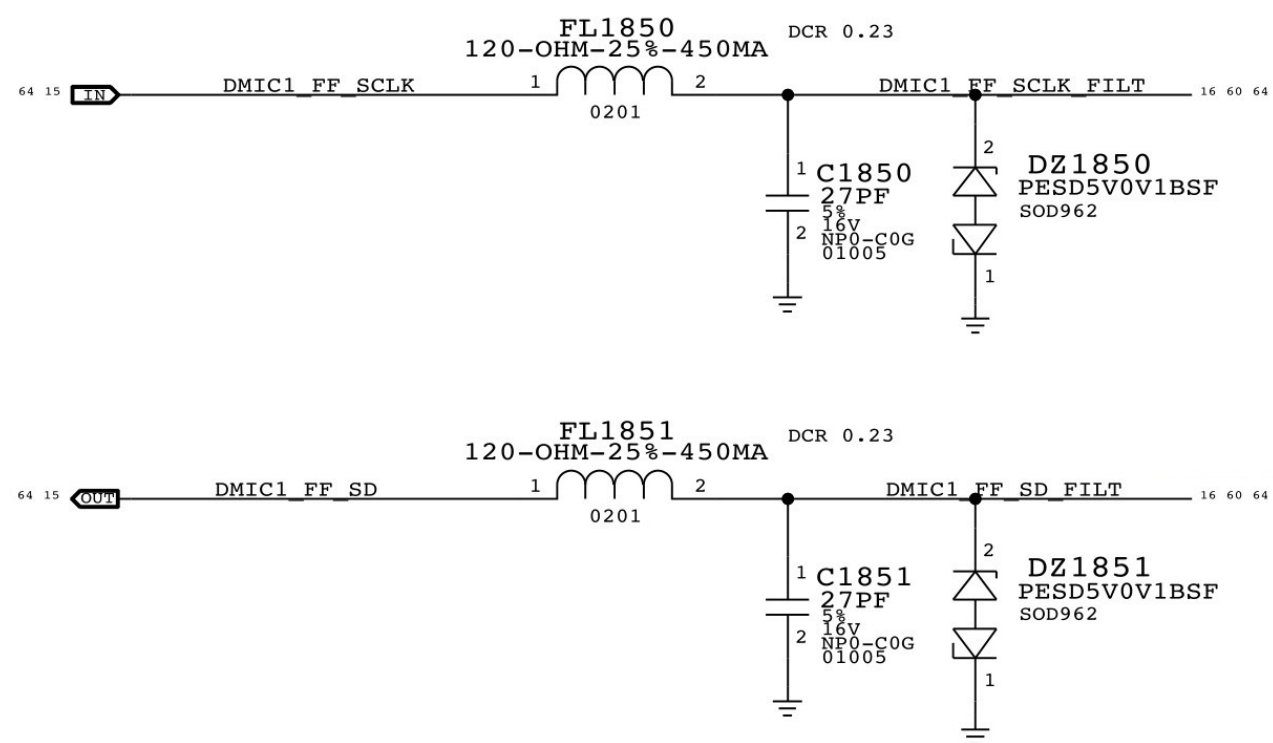
MICROPHONE FLEX B2B CONNECTOR

J1810 MATCHES MIC_FLEX_2.0.0 1/7/13

MLB APN: 516S0899
FLEX APN: 516S0900



DMIC FILTERS



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37780077	37780111	?		?

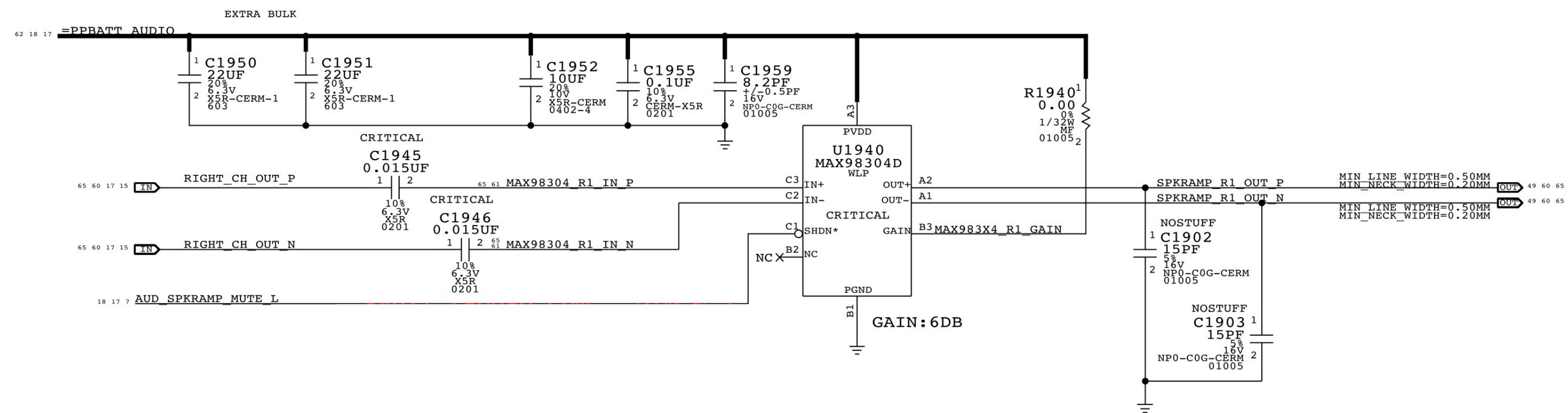
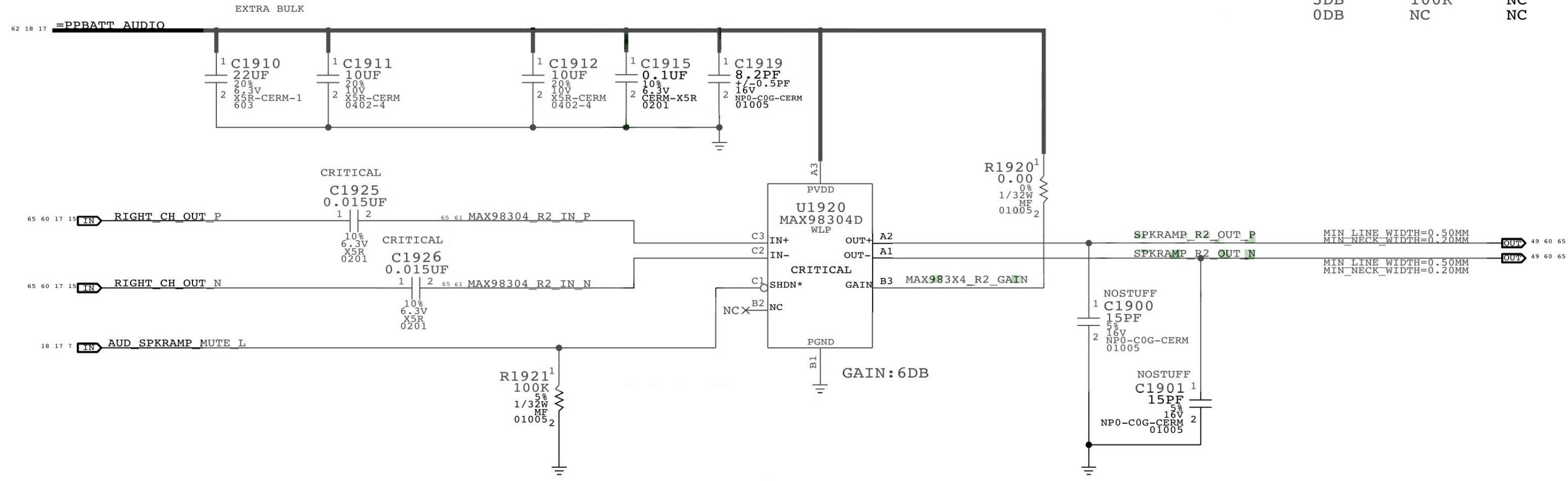
DZ1850, DZ1851

SPEAKER AMPLIFIER

APN:353S3445
 TURN ON TIME: 3.5MS
 TURN ON DELAY: ?MS

75HZ +/- XXX%

GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC

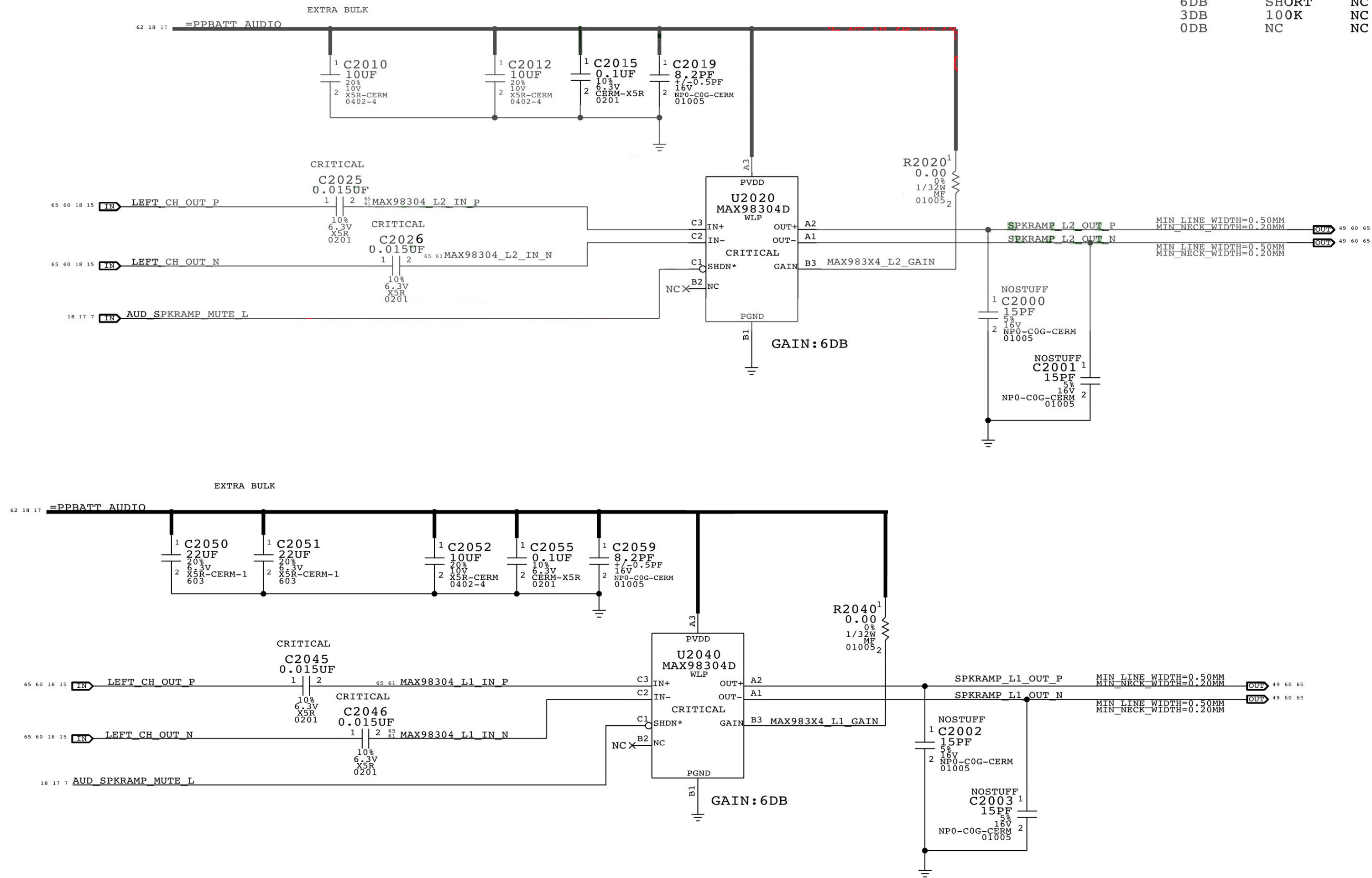


SPEAKER AMPLIFIER

APN:353S3445
TURN ON TIME: 3.5MS
TURN ON DELAY: ?MS

75HZ +/- XXX%

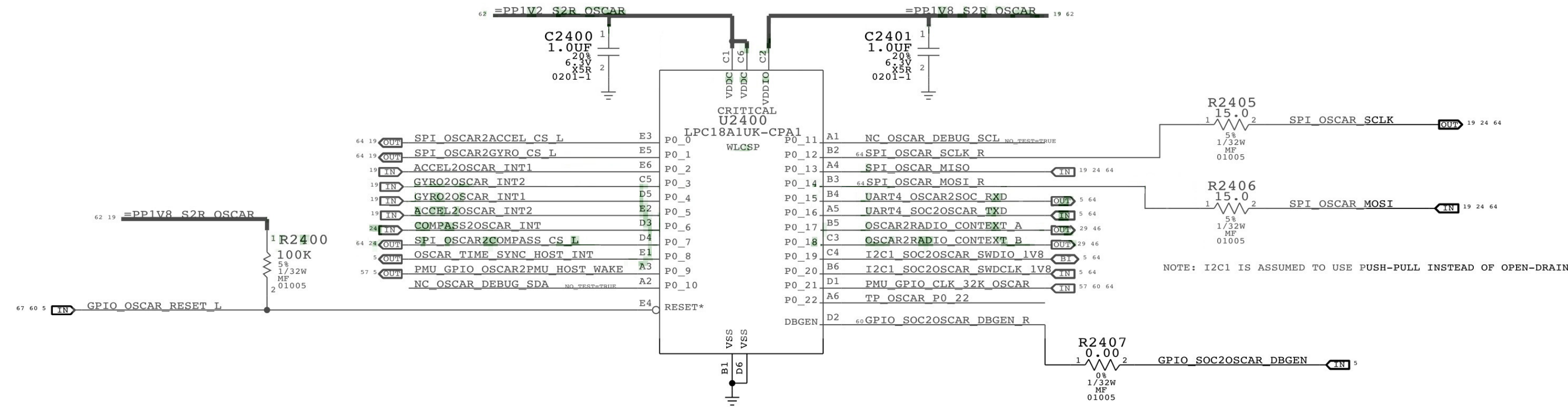
GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC



OSCAR

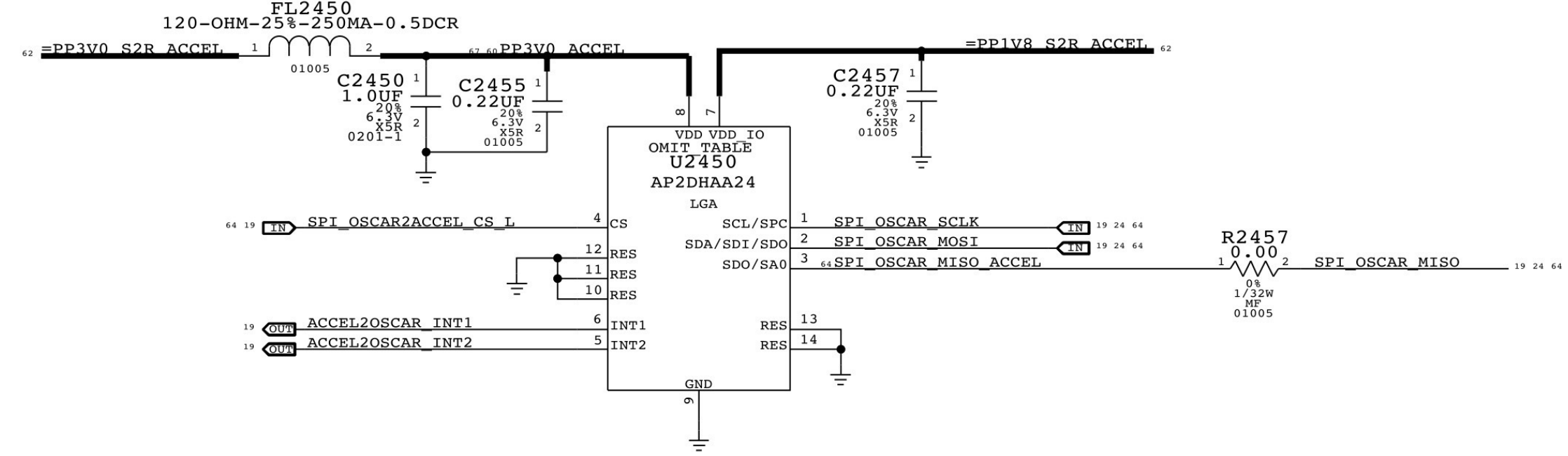
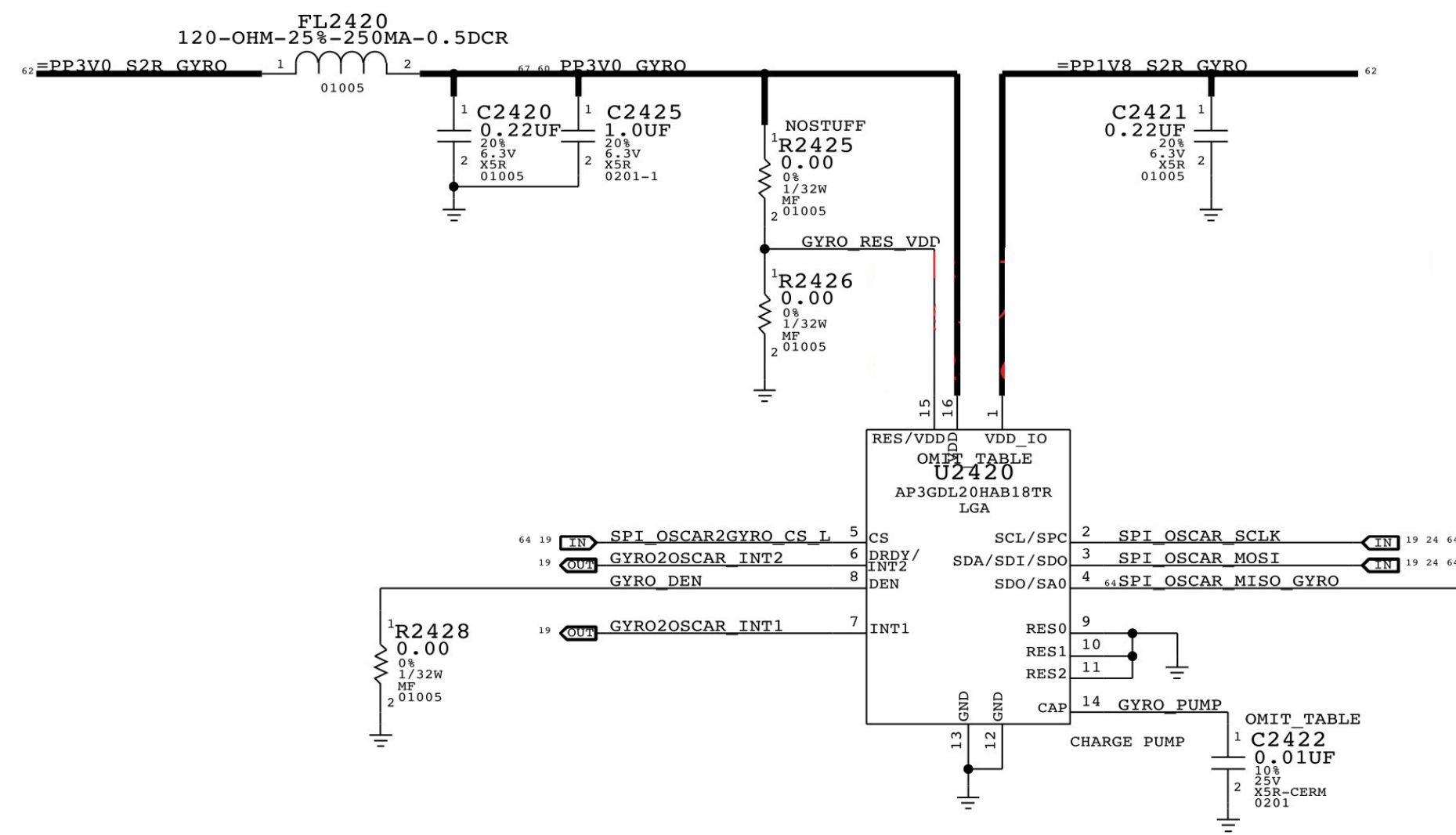
APN 337S4416 (A1)

OSCAR VDDIO = 1.8V HIBERNATE (NEED TO WAKE HOST)
OSCAR CORE = 1.2V HIBERNATE (NEED TO RUN IN S2R)



GYRO

ACCELEROMETER



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D

D

C

C

B

B

A

8

7

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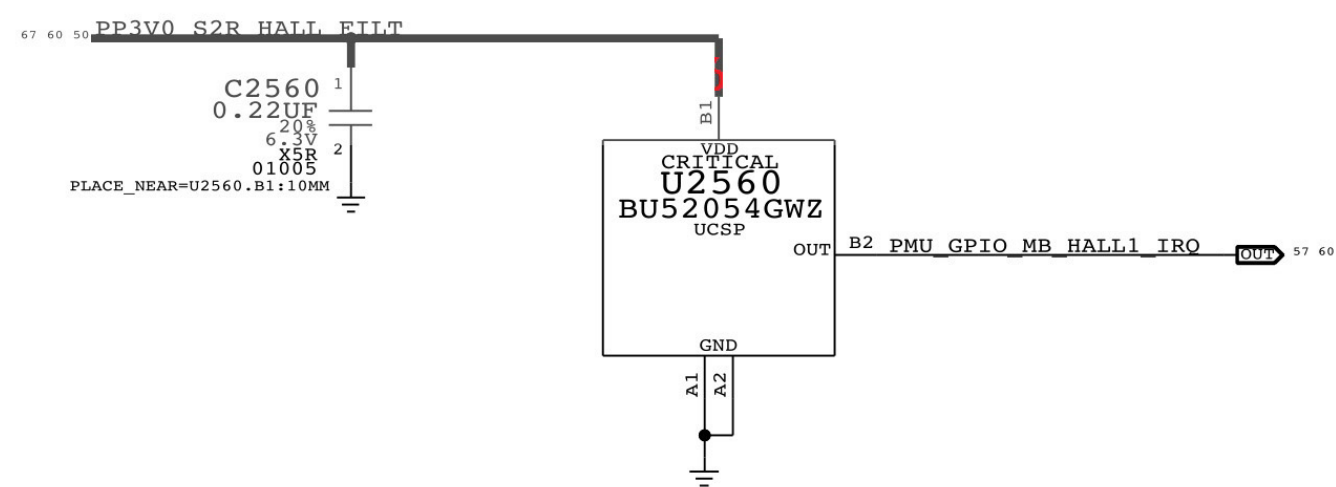
5

4

HALL EFFECT

BIPOLAR ONE OUTPUT APN 353S3687

C=PANEL HALL EFFECT SENSOR
(B=PANEL HALL EFFECT SENSOR ON HB)



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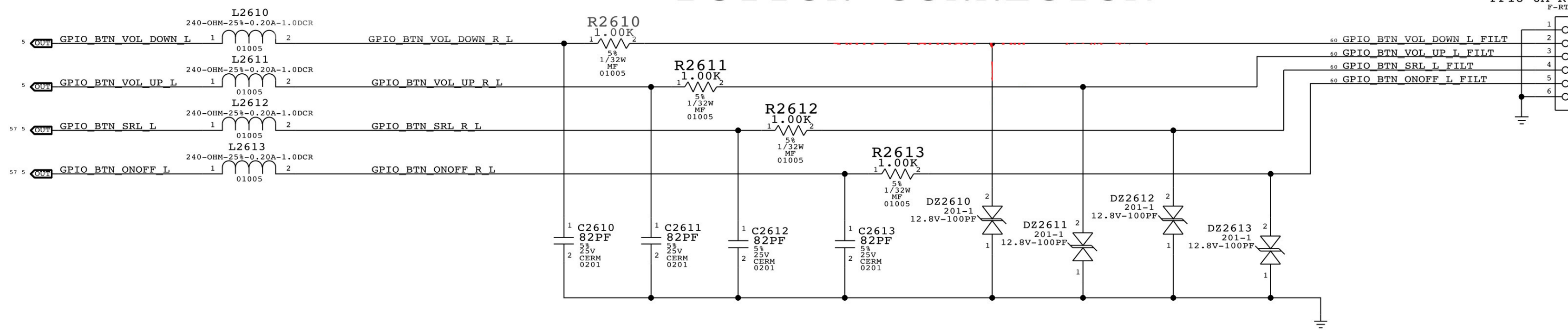
5

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BUTTON CONNECTOR

APN: 518S0692
 CRITICAL
J2610
 FF18-6A-R11AD-B-3H
 F-RT-SM



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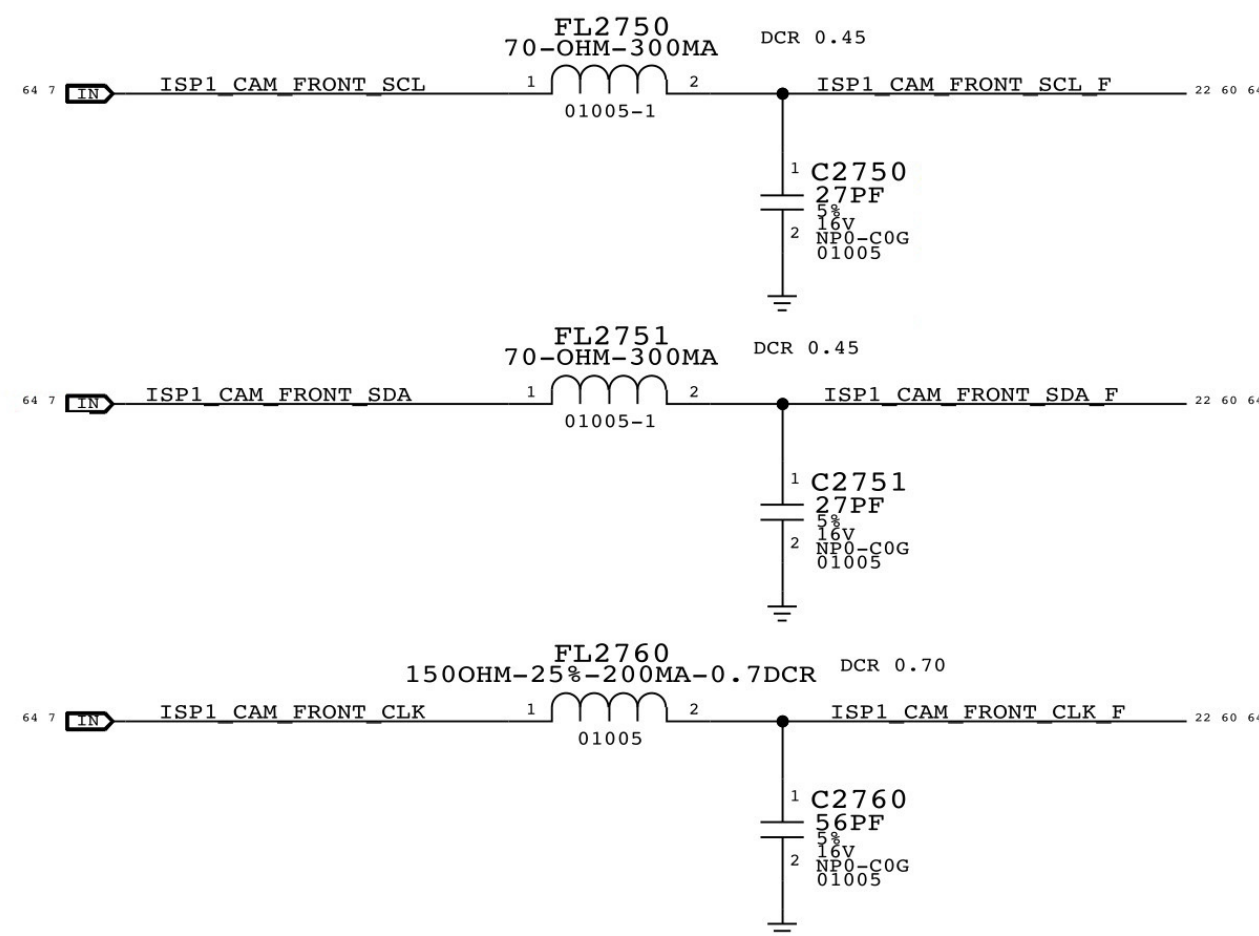
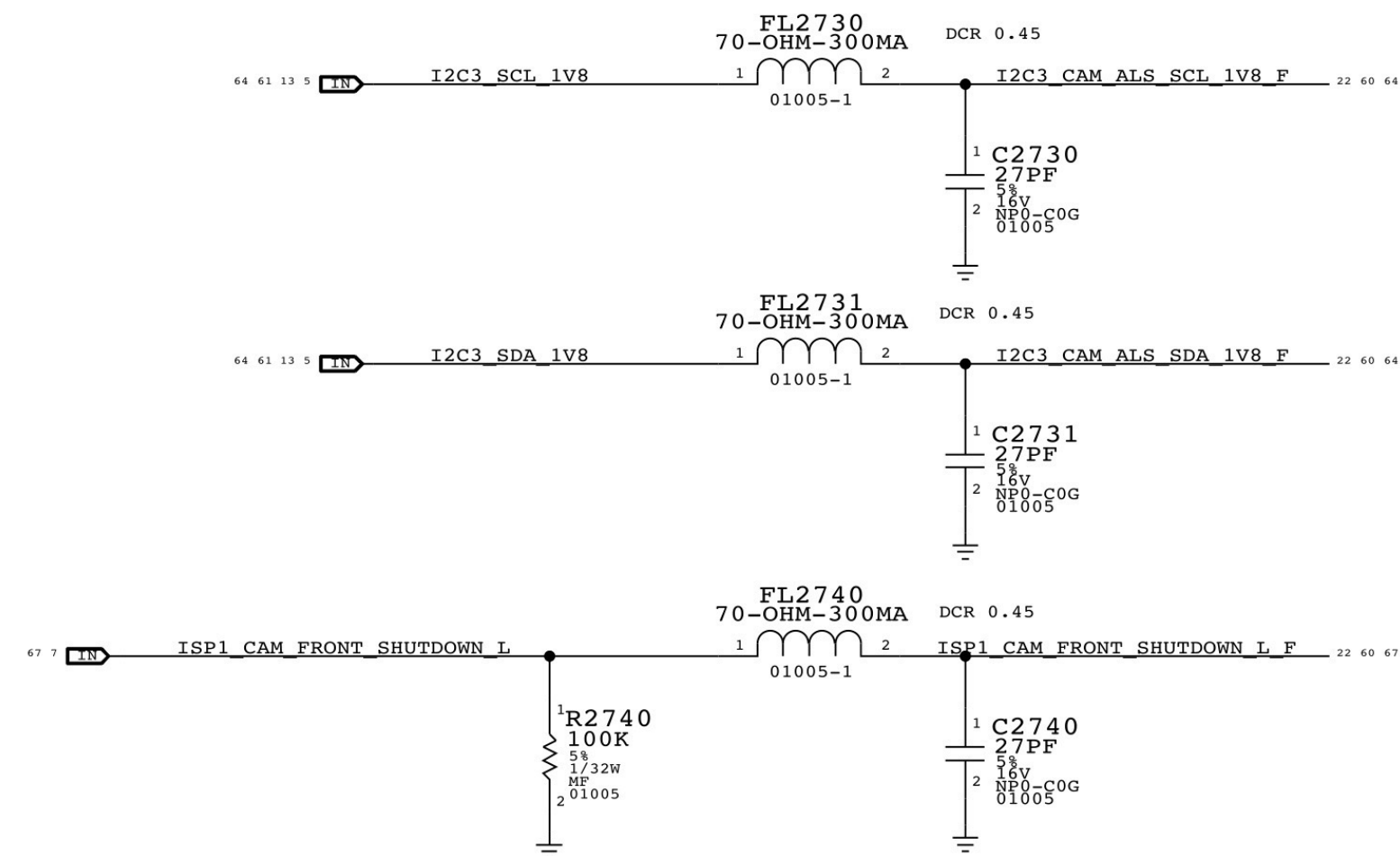
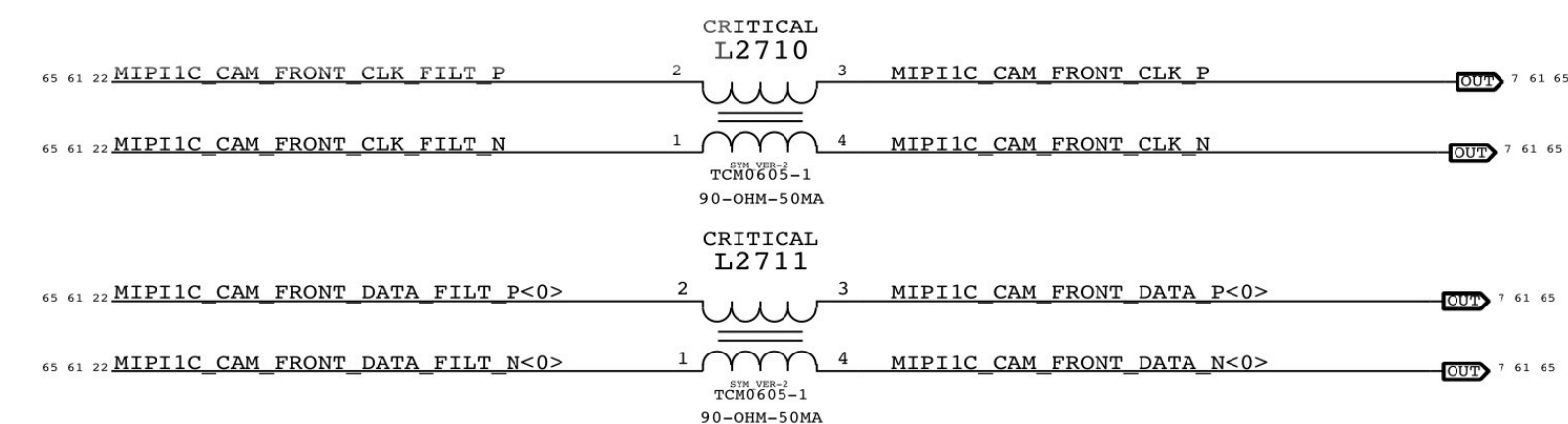
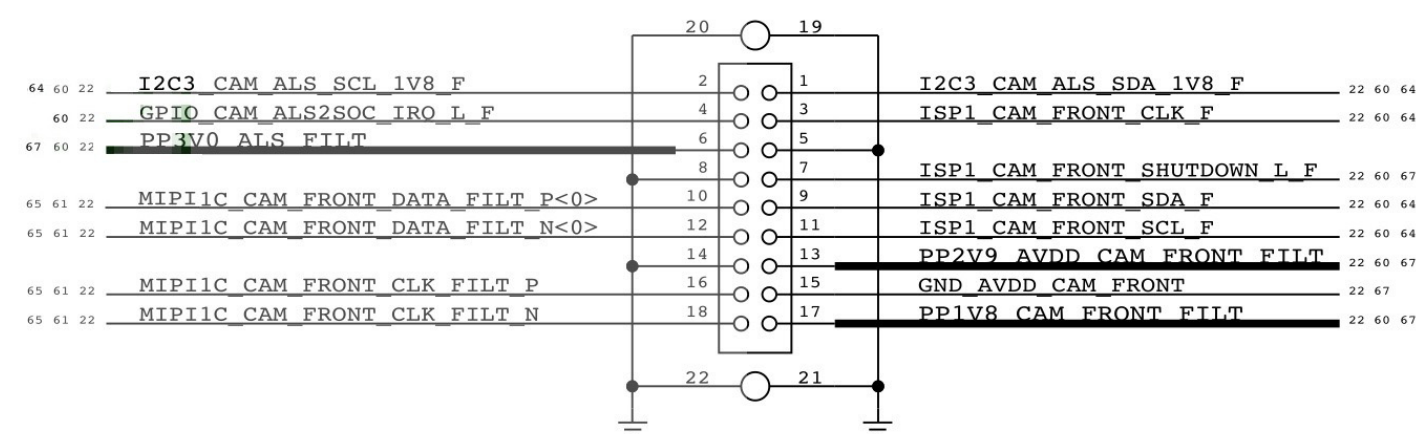
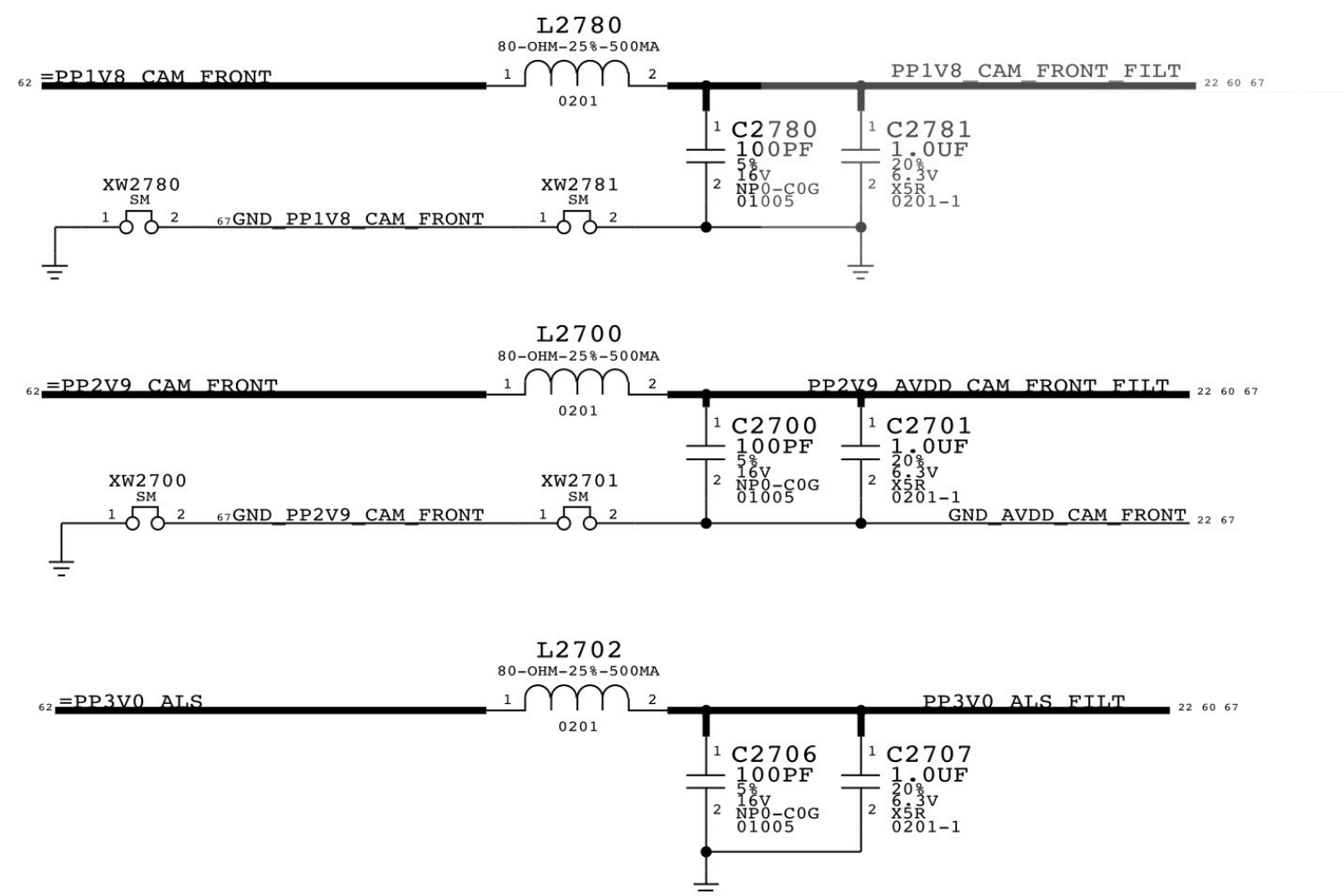
4

FRONT CAMERA CONNECTOR

J65 CAMERA CONNECTOR

APN:MLB 516S0876
APN:FLEX 516S0869

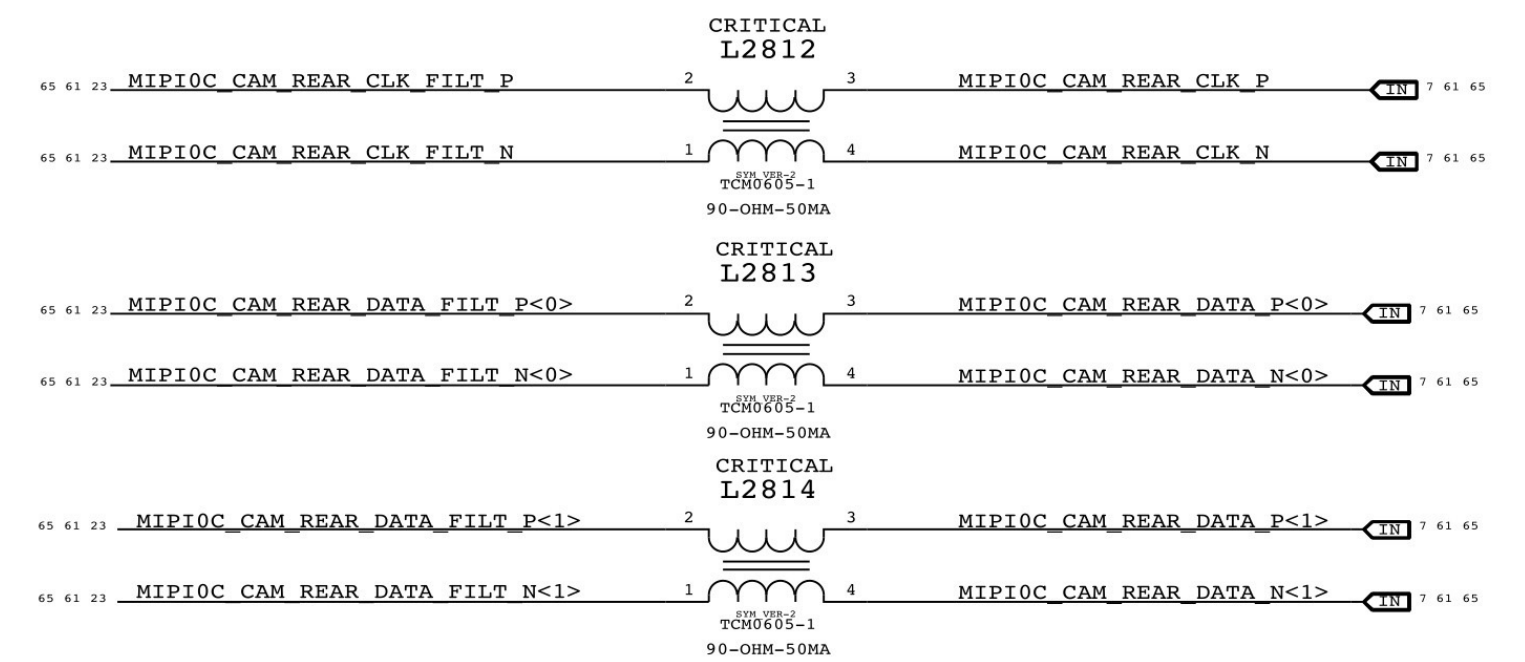
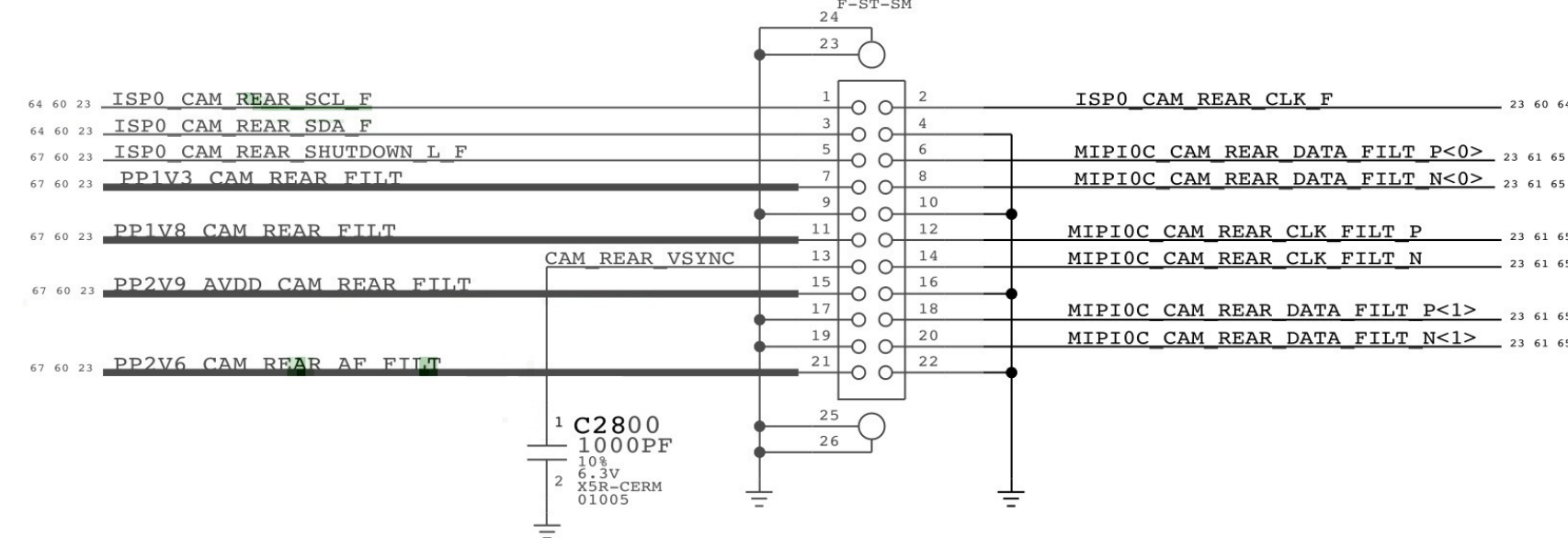
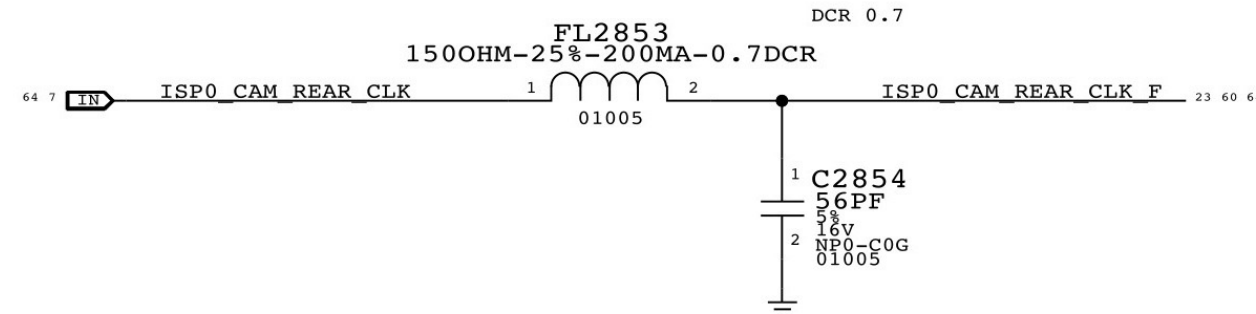
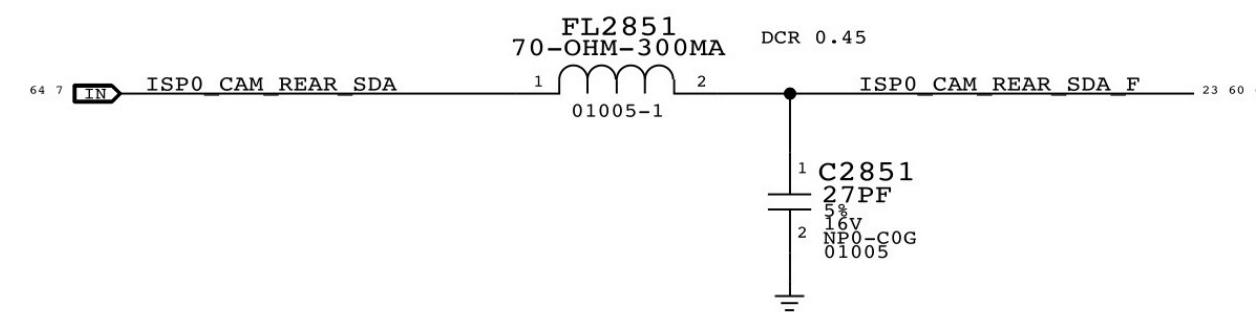
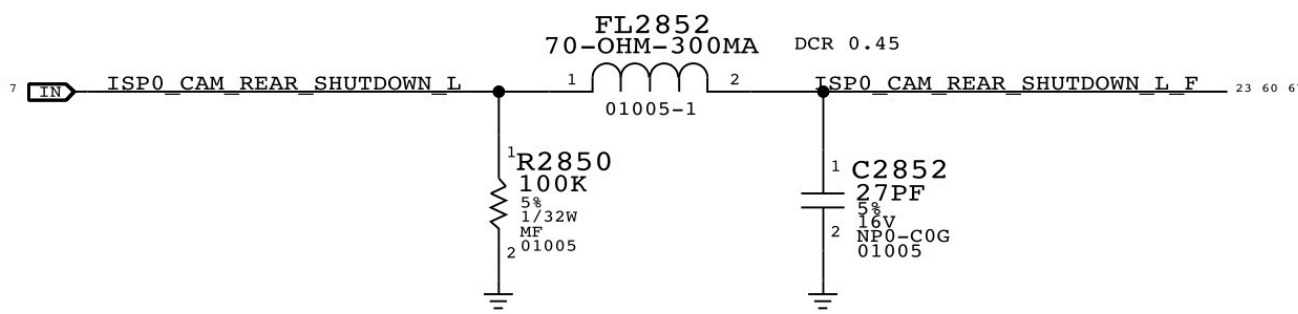
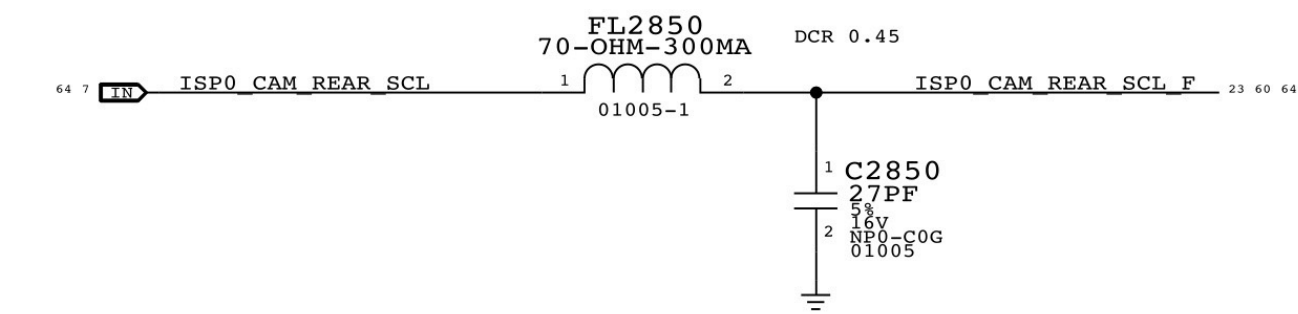
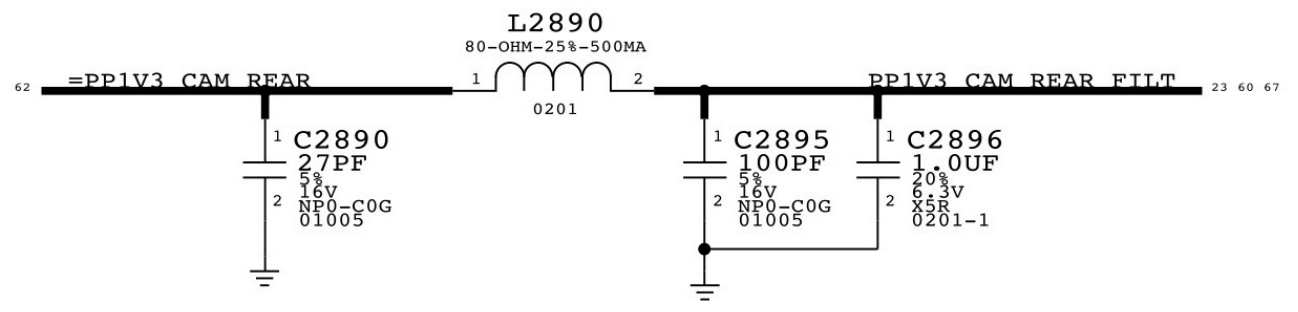
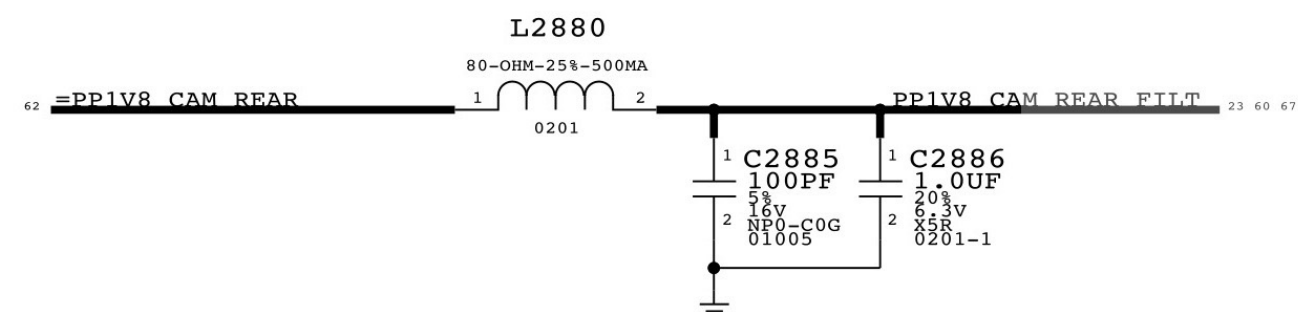
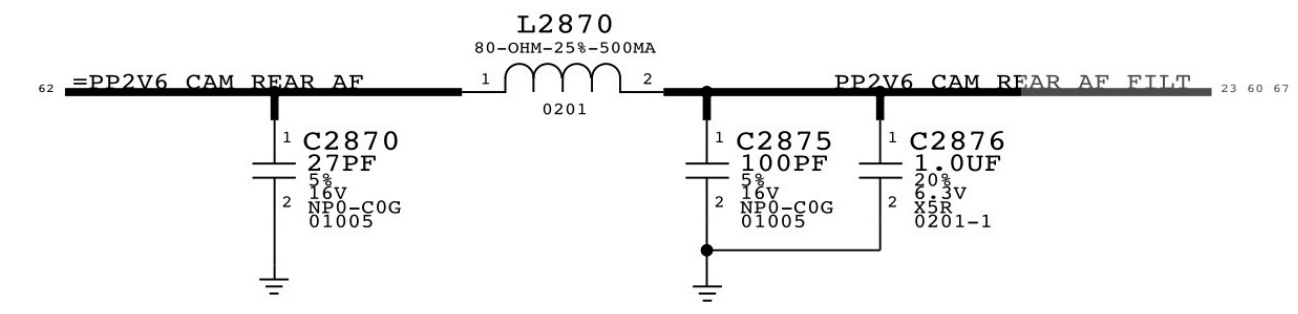
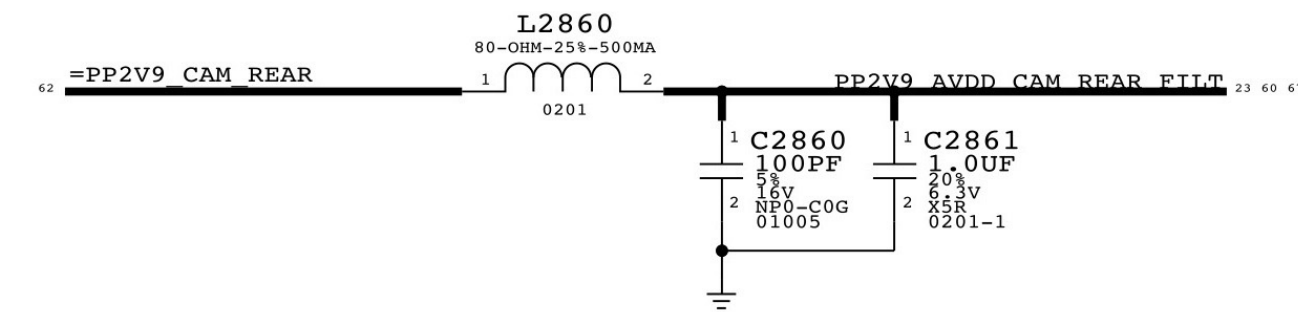
CRITICAL
J2700
503548-1820
F-ST-SM



REAR CAMERA CONNECTOR

FLEX: 516S0974
MLB: 516S0973

CRITICAL
J2800
AA07-S022VA1
F-ST-SM



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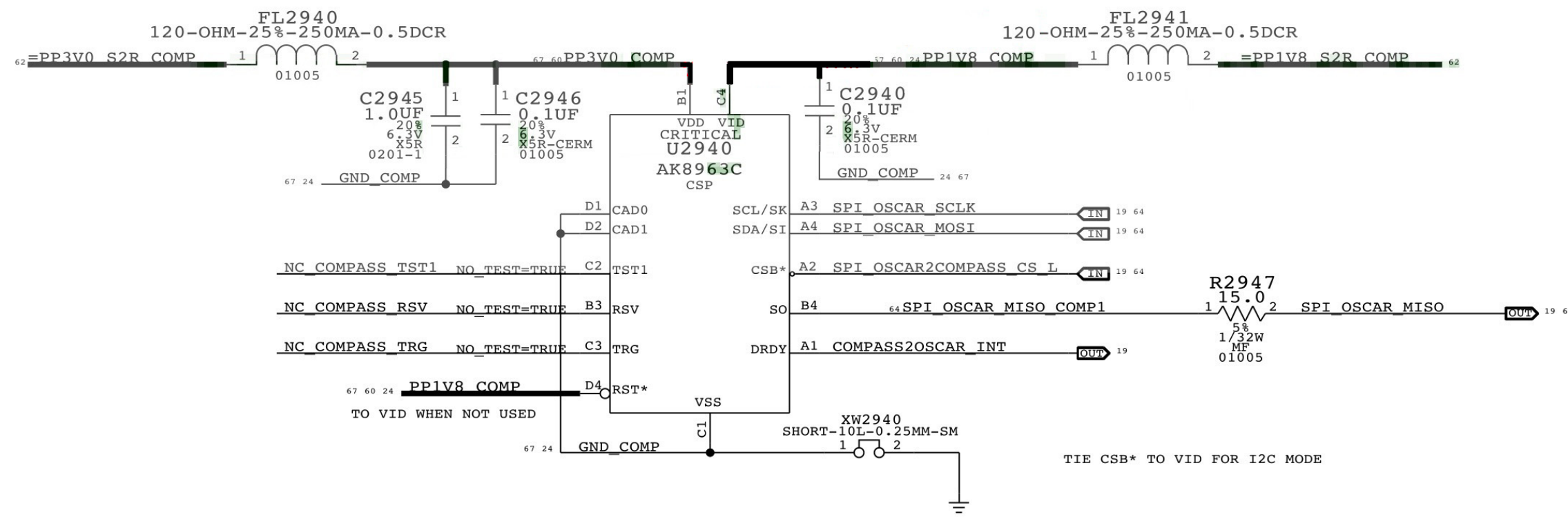
5

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COMPASS

APN 338S1014



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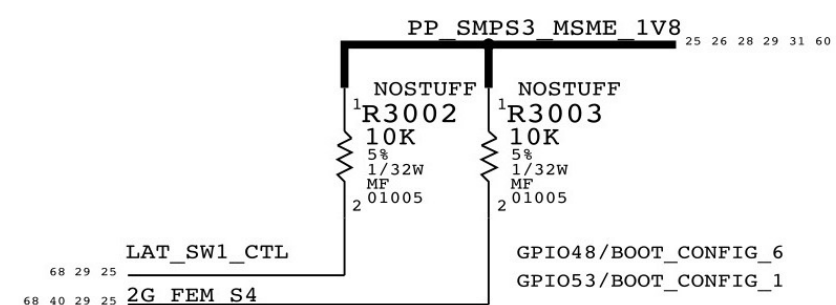
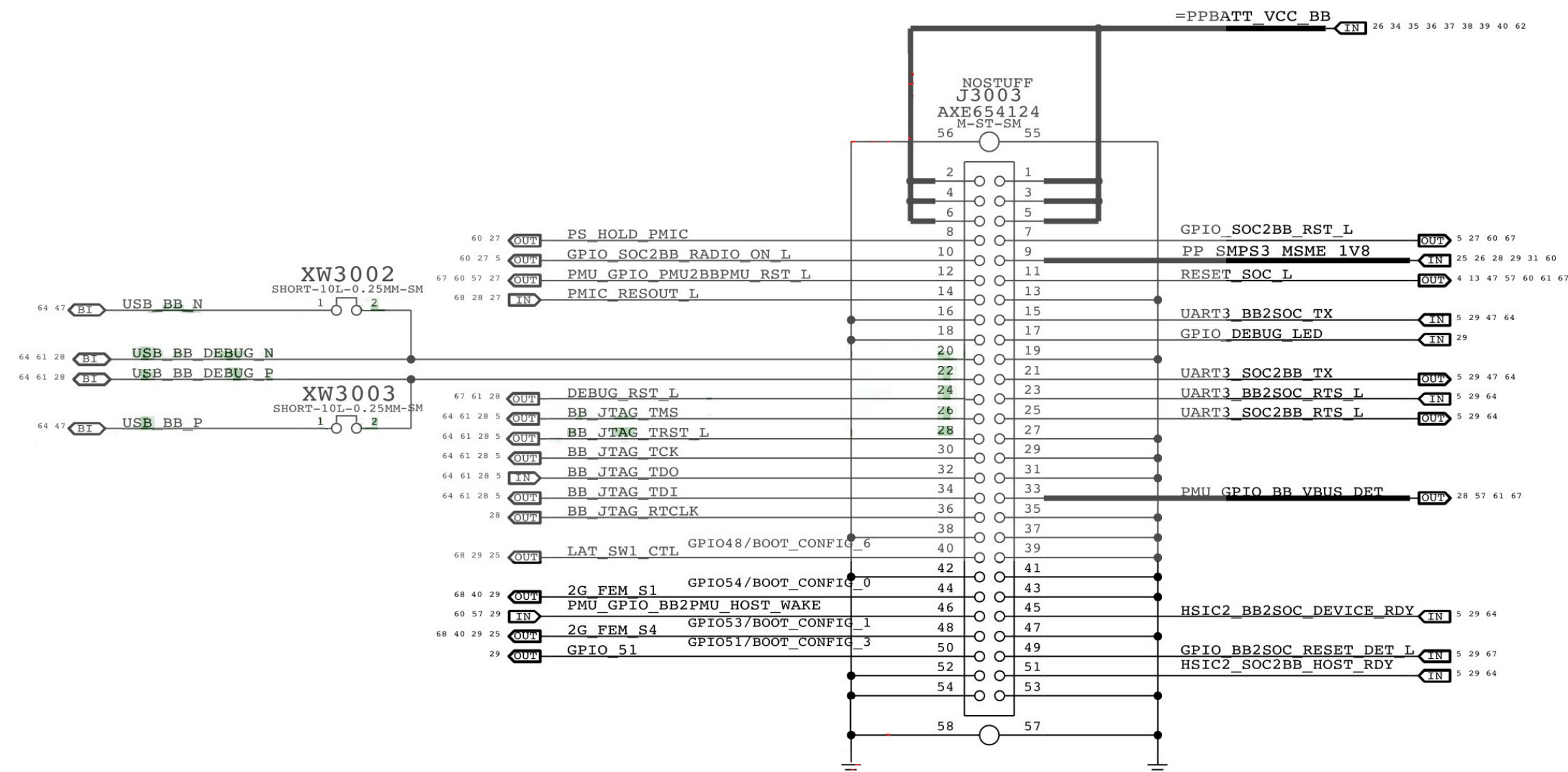
AP INTERFACE & DEBUG CONNECTOR

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

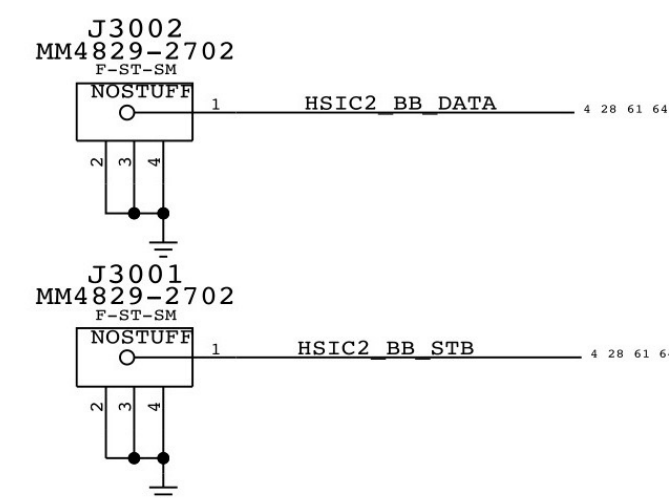
PROBE POINTS

- PP3000 P4MM SR 1 BB ERROR FLAG 29 68
- PP3001 P4MM SR 1 SLEEP CLK 32K 27 28 68
- PP3002 P4MM SR 1 PMIC_SSBI 27 28 68
- PP3003 P4MM SR 1 19P2M_MDM 27 28 68
- PP3008 P4MM SR 1 WTR_SSBI_TX_GPS 29 30
- PP3009 P4MM SR 1 WTR_SSBI_PRX_DRX 29 30
- PP3010 P4MM SR 1 WTR_RX_ON 29 30 68
- PP3011 P4MM SR 1 WTR_RF_ON 29 30 68
- PP3012 P4MM SR 1 UART_WLAN2BB_LTE_COEX 29 46
- PP3013 P4MM SR 1 UART_BB2WLAN_LTE_COEX 29 46

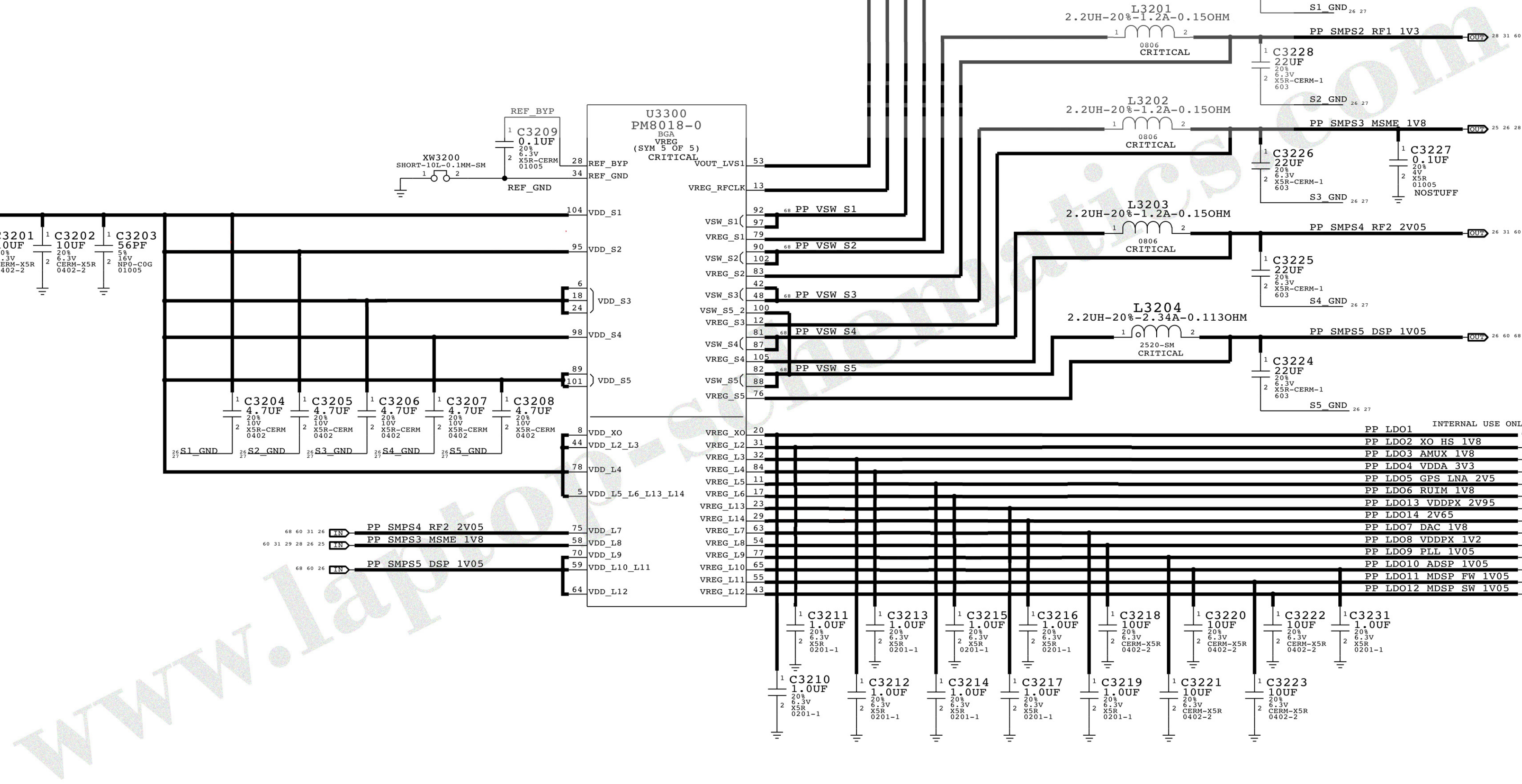
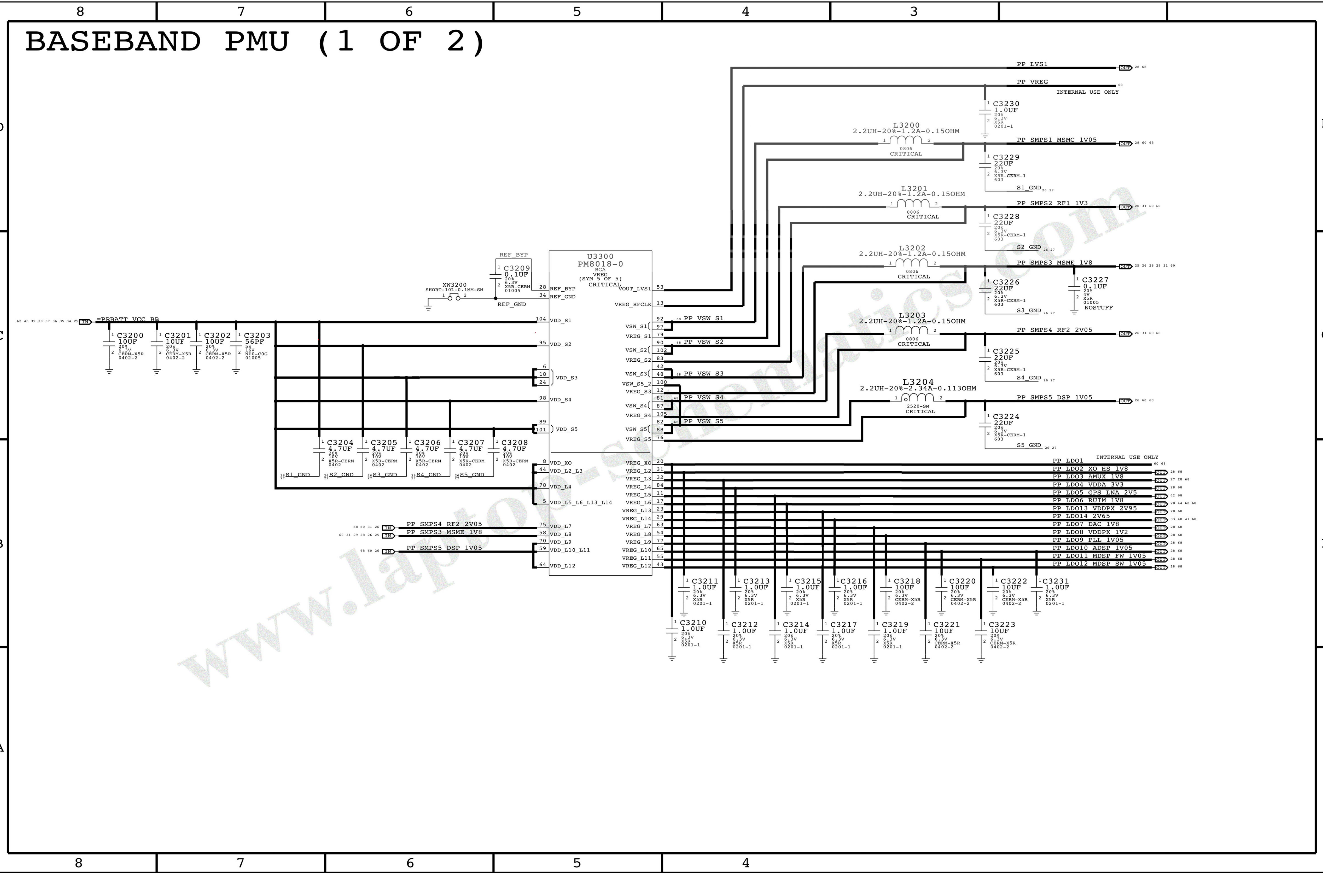
DEBUG CONNECTOR



BOOT OPTIONS	BOOT CONFIG SW REGISTER VALUE	GPIO/BOOT_CONFIG CONFIGURATION								
		6	5	4	3	2	1	0		
BOOT_DEFAULT_OPTION	0X00	X	0	0	0	0	0	0	0	X
BOOT_NAND_OPTION	0X01	X	1	0	0	0	0	0	1	X
BOOT_HSIC_OPTION	0X02	X	1	0	0	0	0	1	0	X
BOOT_USB_OPTION	0X03	X	1	0	0	0	0	1	1	X
ENABLE_SAHARA_PROTOCOL	0X08	X	1	0	0	1	0	X	X	X

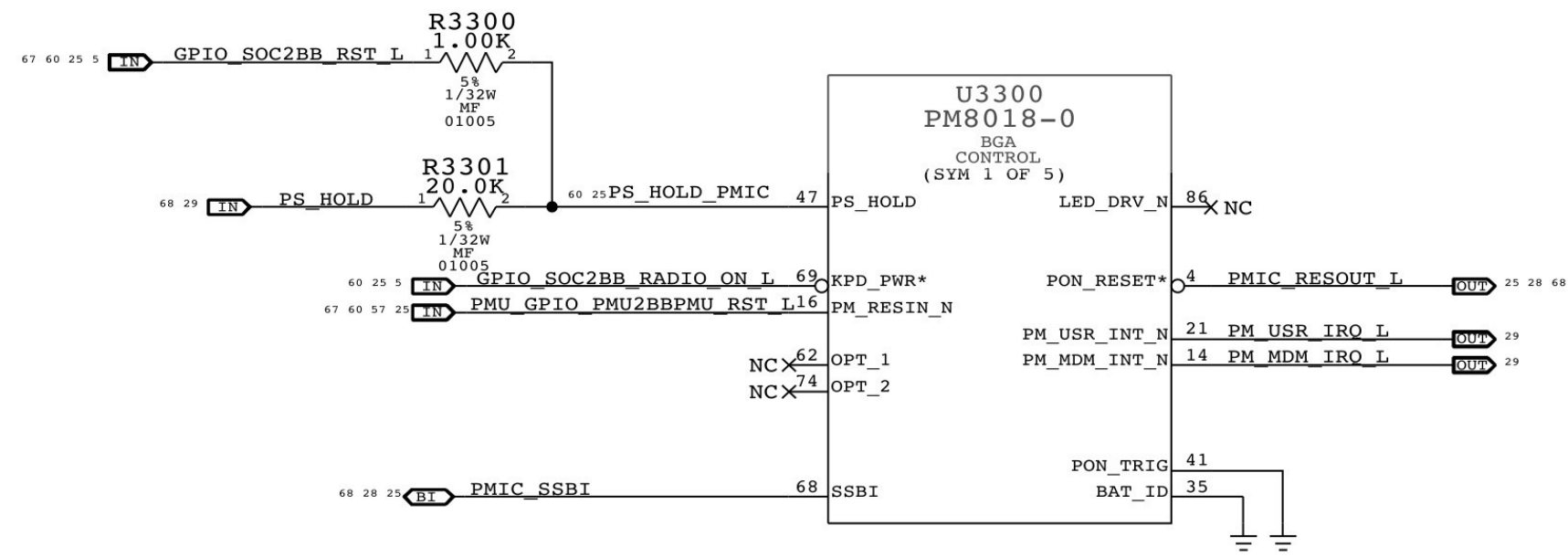


BASEBAND PMU (1 OF 2)



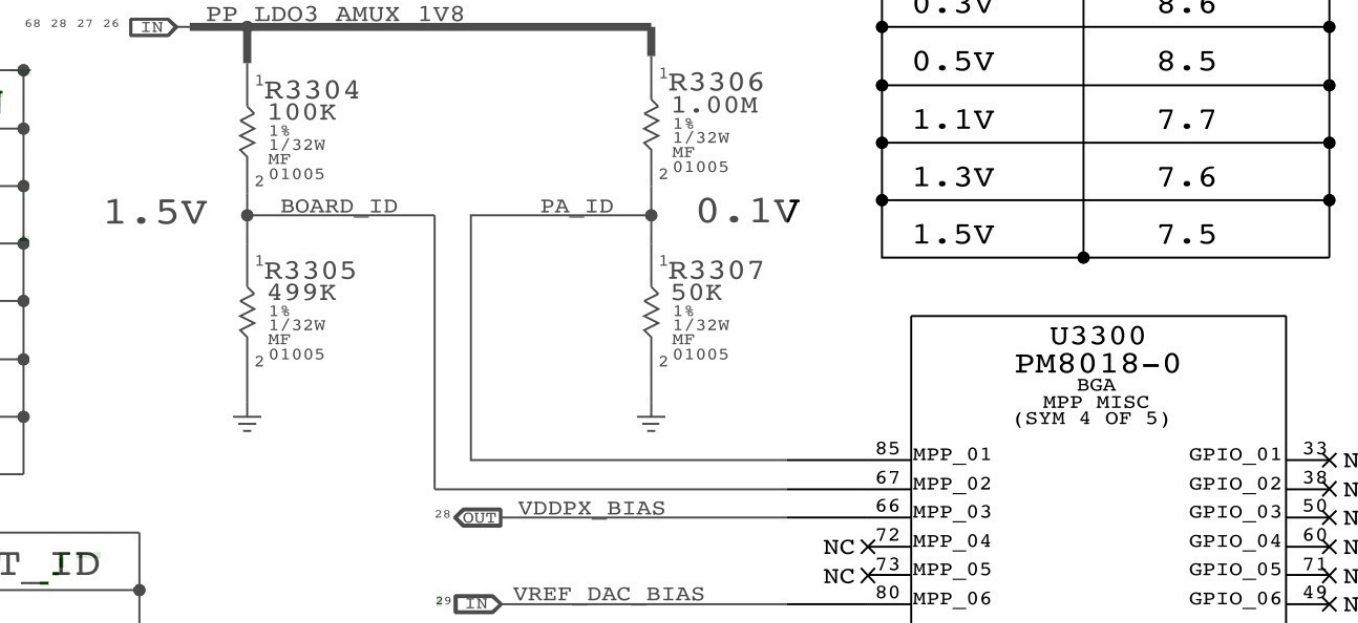
BASEBAND PMU (2 OF 2)

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

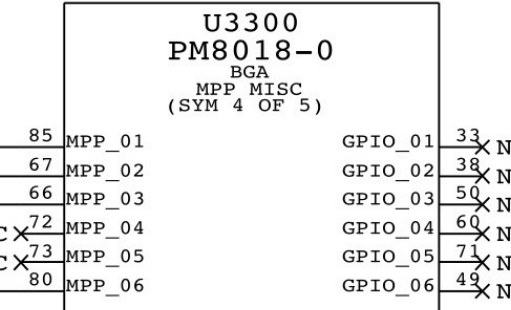


BOARD_ID	REVISION
0.7V	PROTO1
0.9V	PROTO2
1.1V	EVT1
1.3V	EVT2
1.5V	DVT
1.7V	PVT

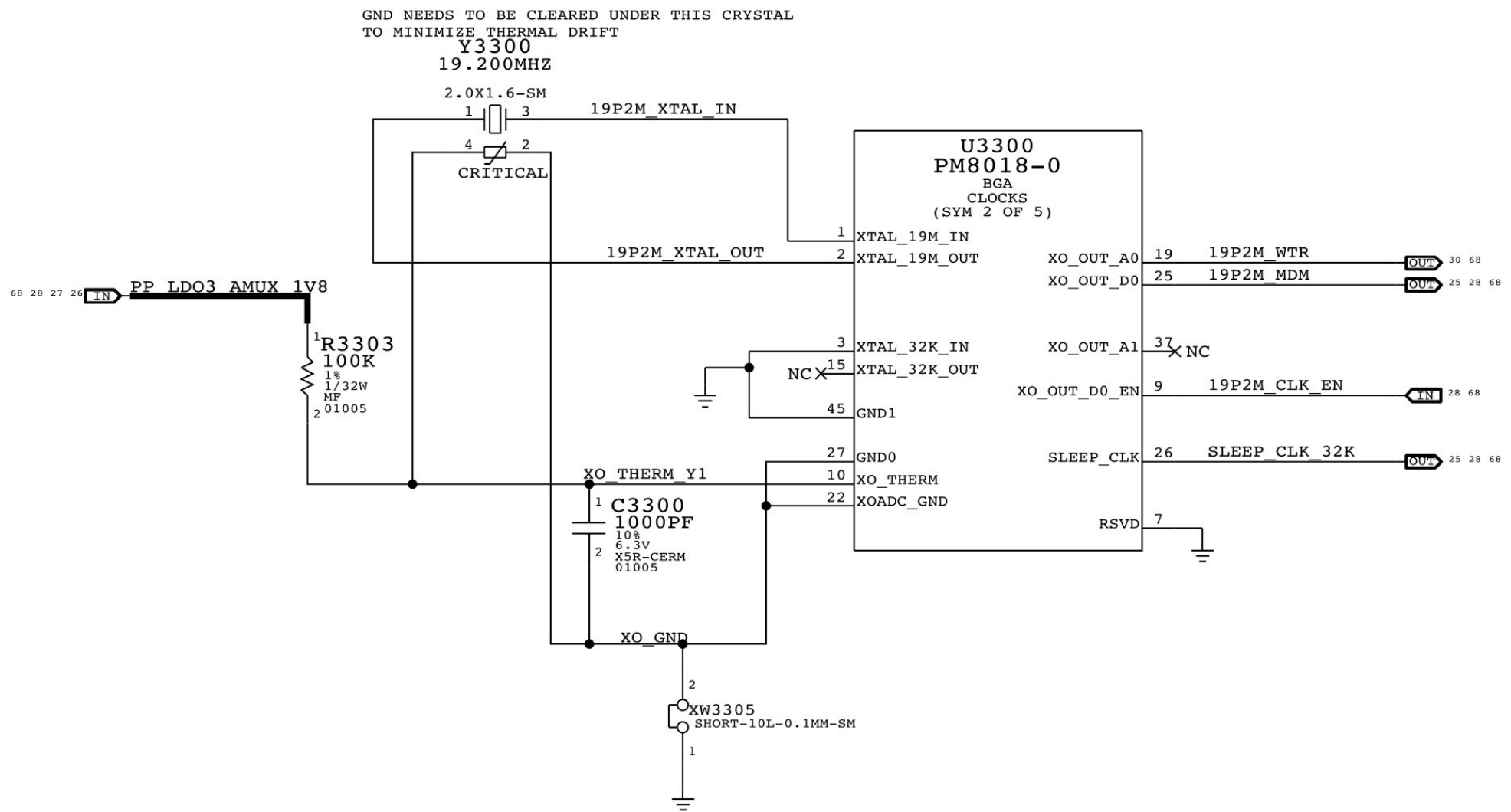
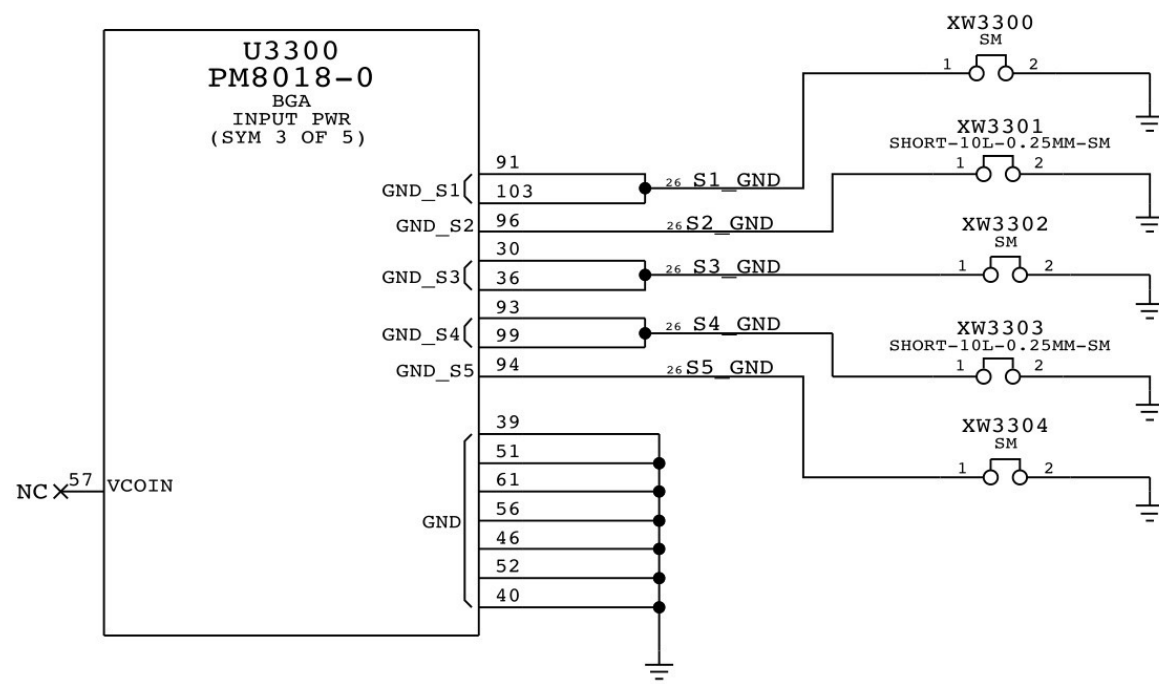
BB GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX



PA_ID	MAV VER
0.1V	8.7
0.3V	8.6
0.5V	8.5
1.1V	7.7
1.3V	7.6
1.5V	7.5



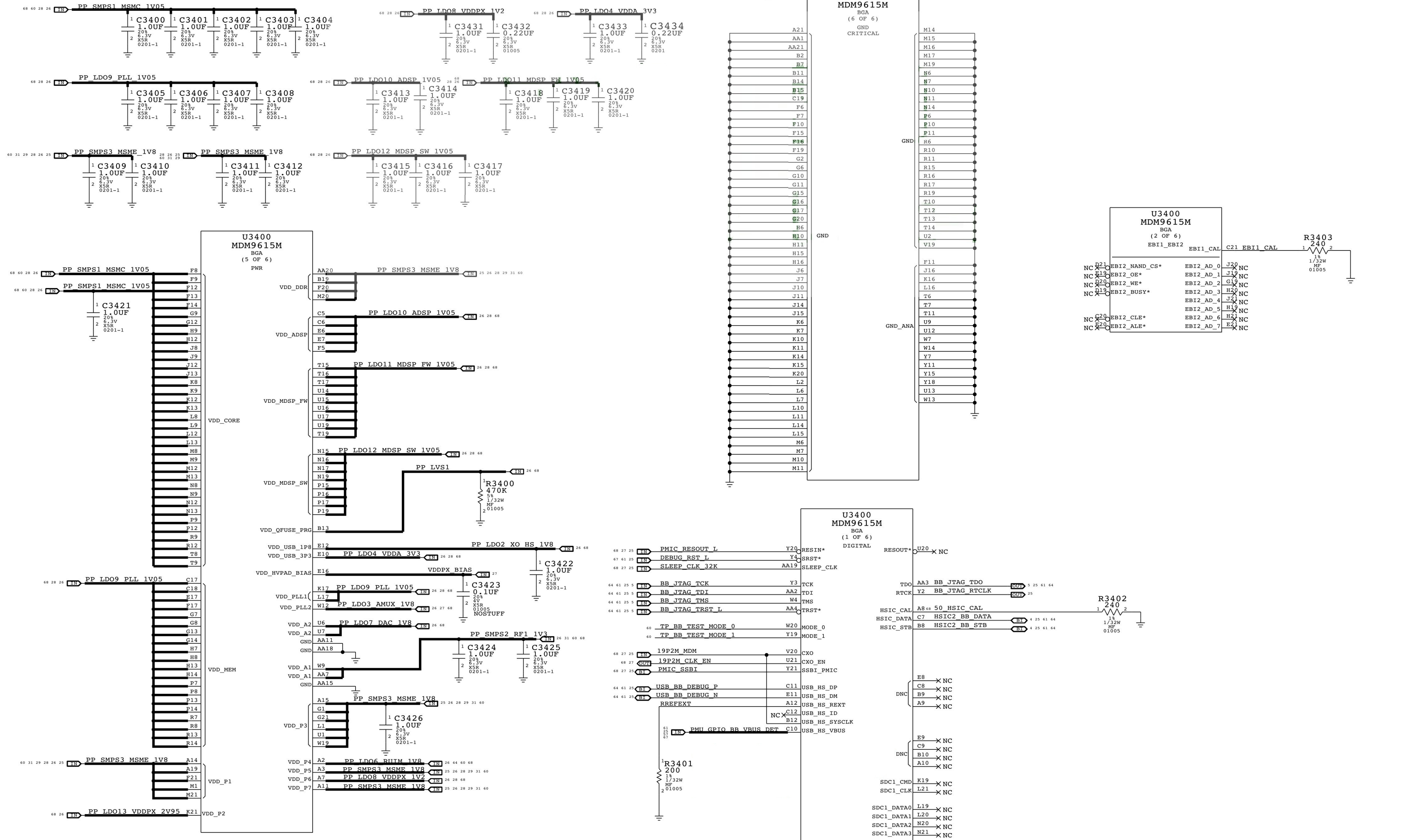
PA THERMISTOR REMOVED TO MATCH N41, AP SECTION NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.



GND NEEDS TO BE CLEARED UNDER THIS CRYSTAL TO MINIMIZE THERMAL DRIFT

BASEBAND (1 OF 2)

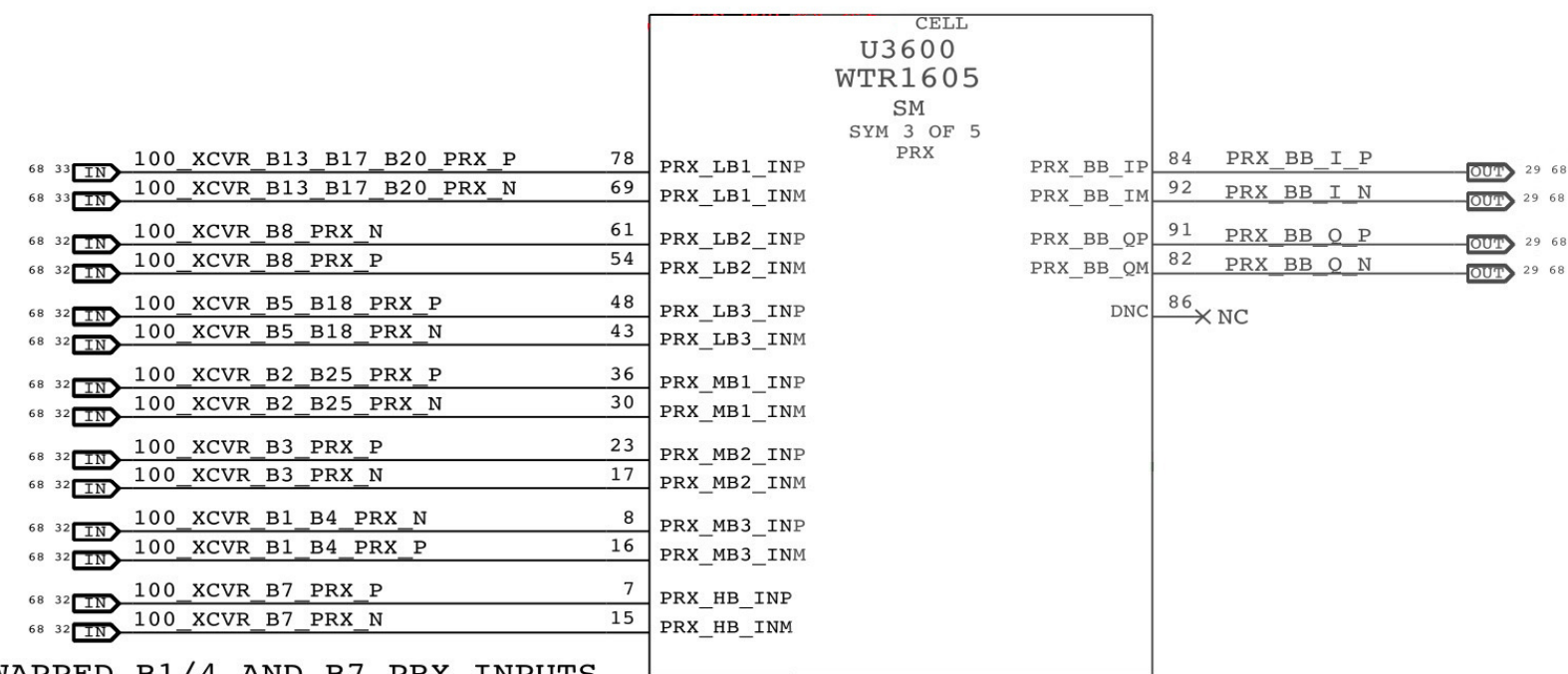
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST



RF TRANSCEIVER (1 OF 2)

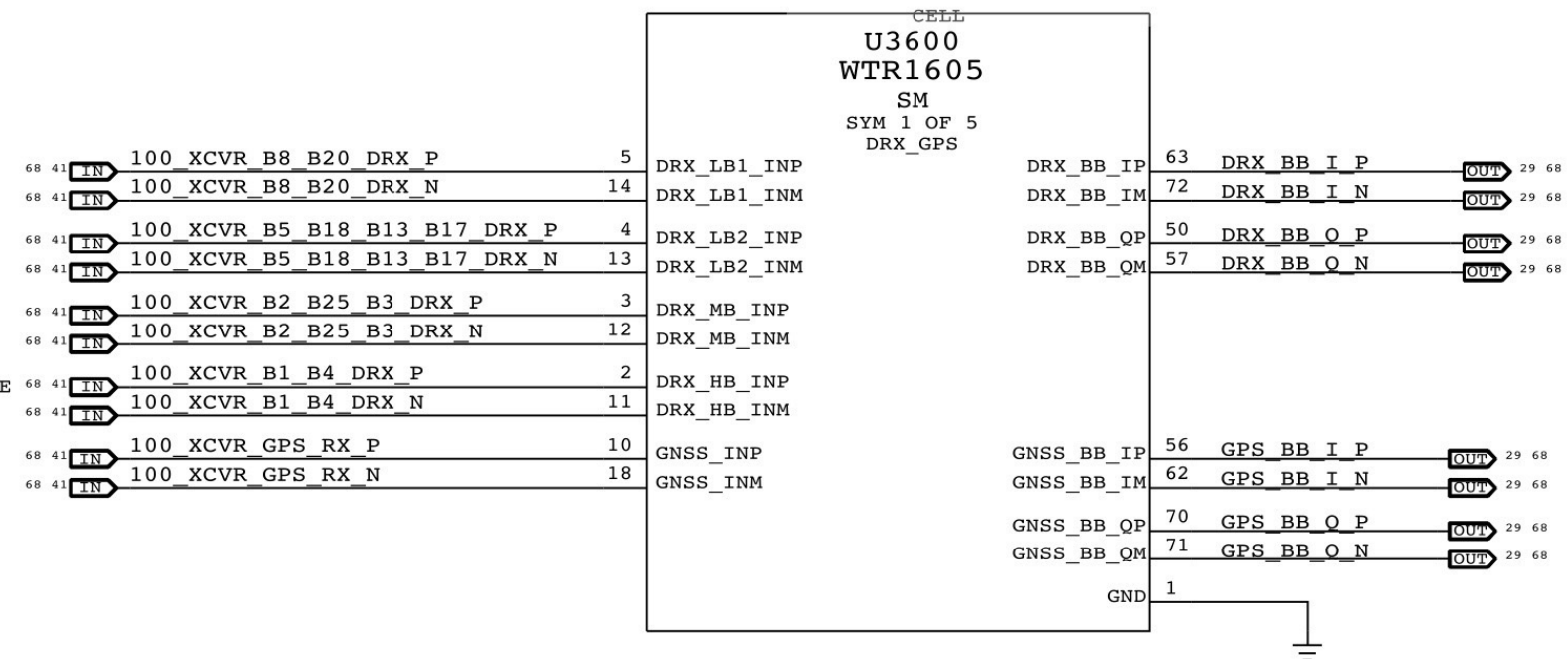
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

PRX TRANSCEIVER RF AND IQ PORTS



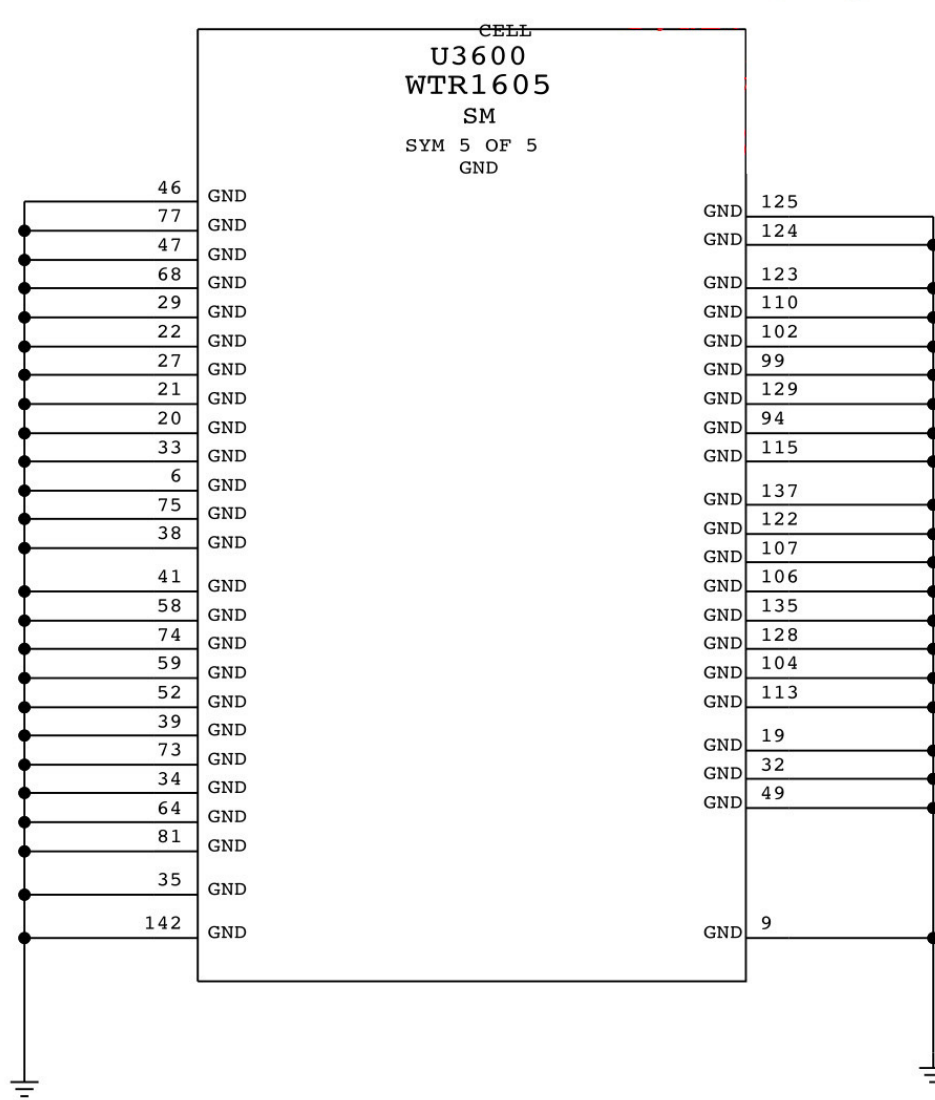
SWAPPED B1/4 AND B7 PRX INPUTS

DRX TRANSCEIVER RF AND IQ PORTS

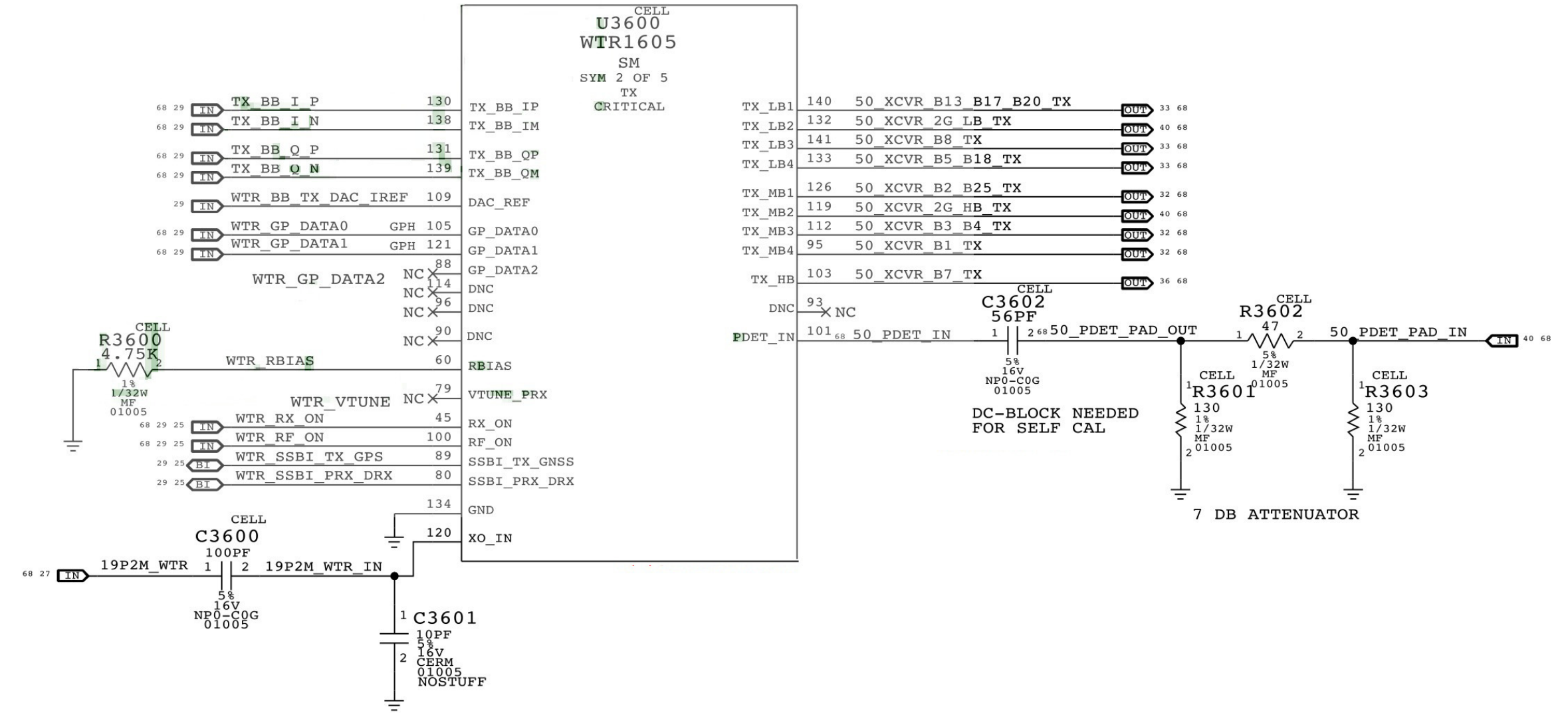


B7 DIFF PAIR NET NAME TO BE UPDATED

TRANSCEIVER GROUND CONNECTIONS



TRANSCEIVER PHASE CONTROL, TX RF & IQ PORTS



D

C

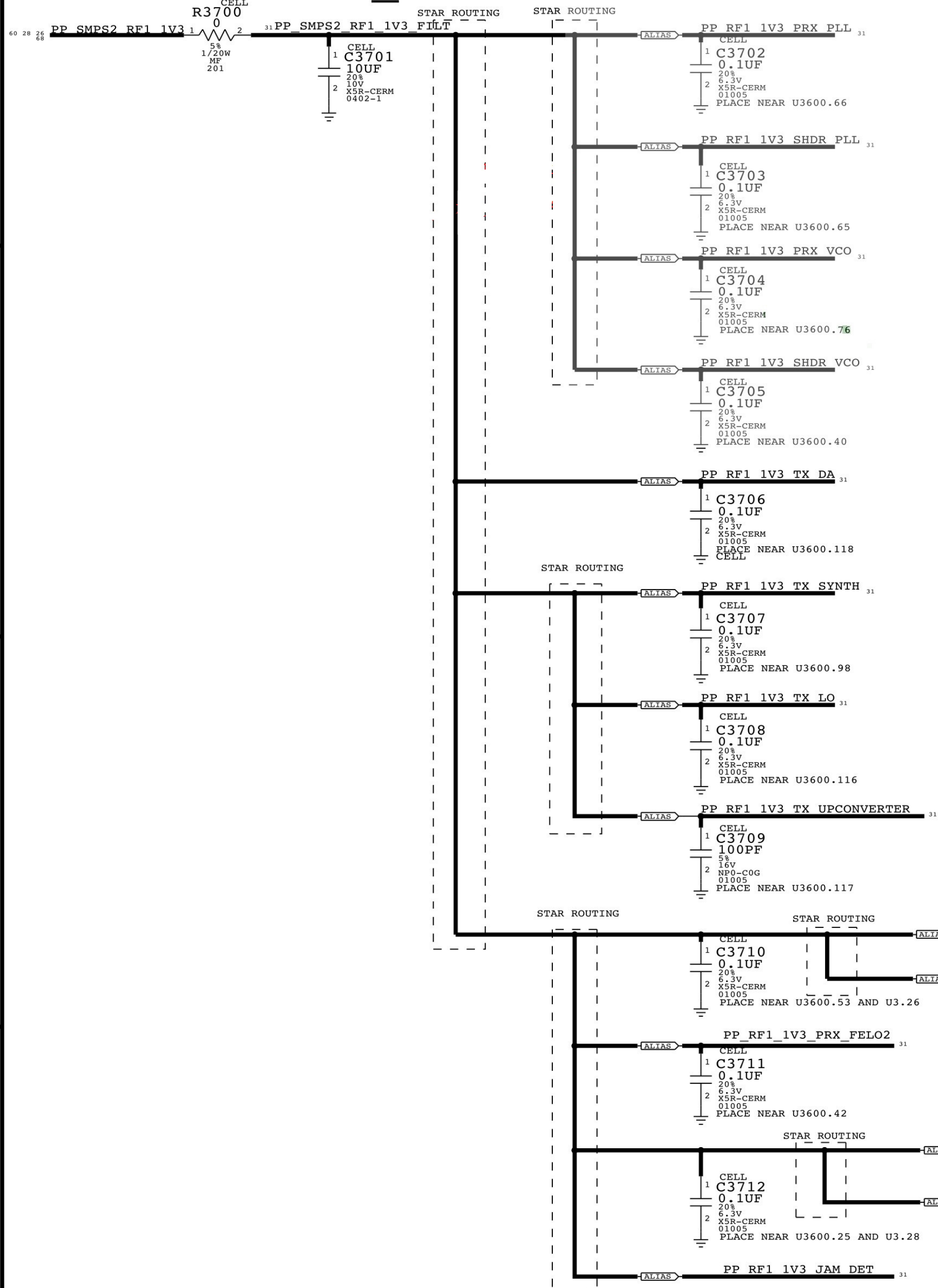
B

A

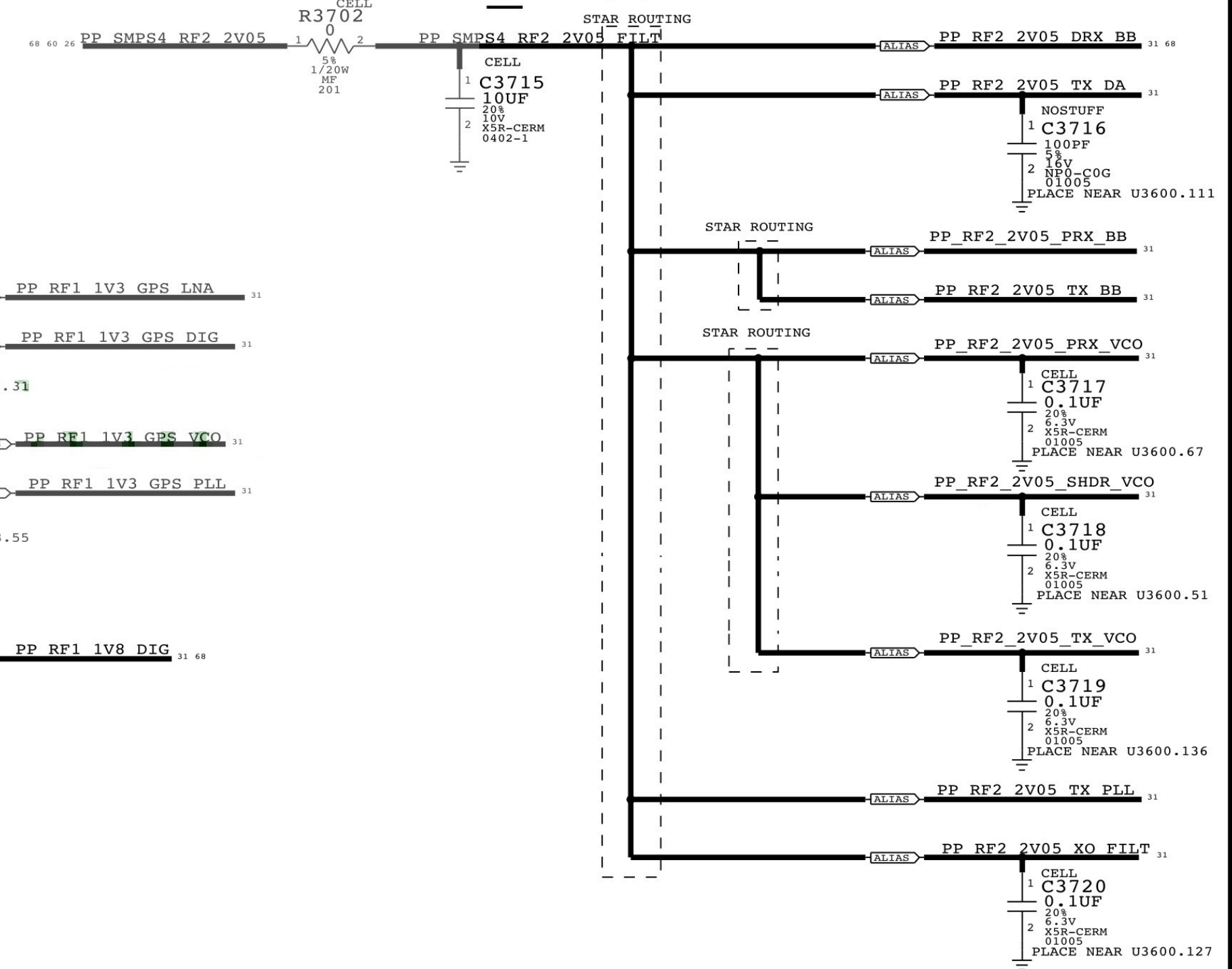
RF TRANSCEIVER (2 OF 2)

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

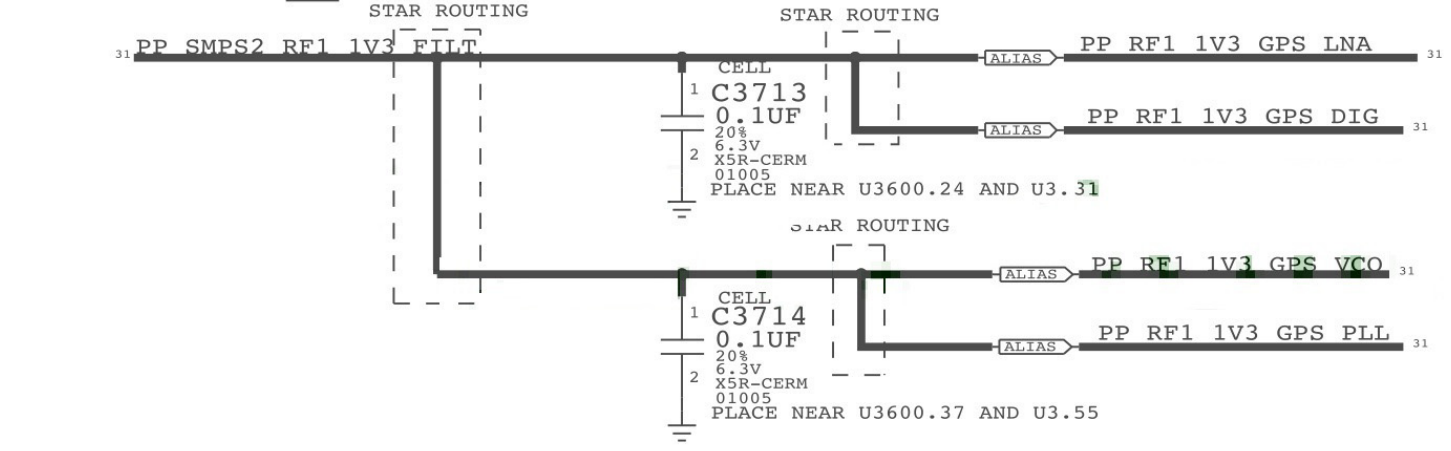
RF1_1V3



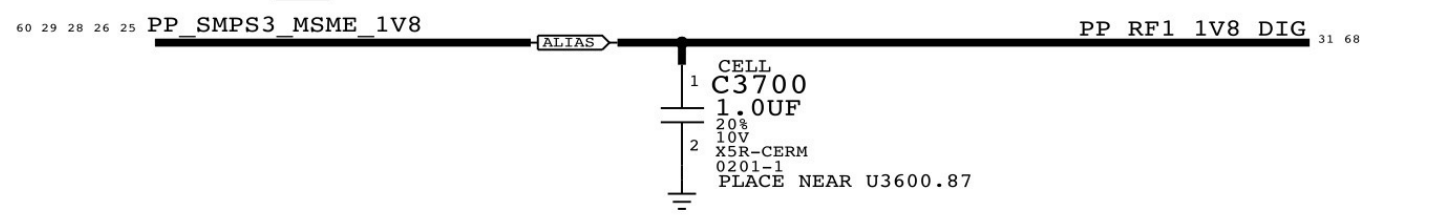
RF2_2V05



RF1_1V3



RF1_1V8



TRANSCEIVER POWER CONNECTIONS

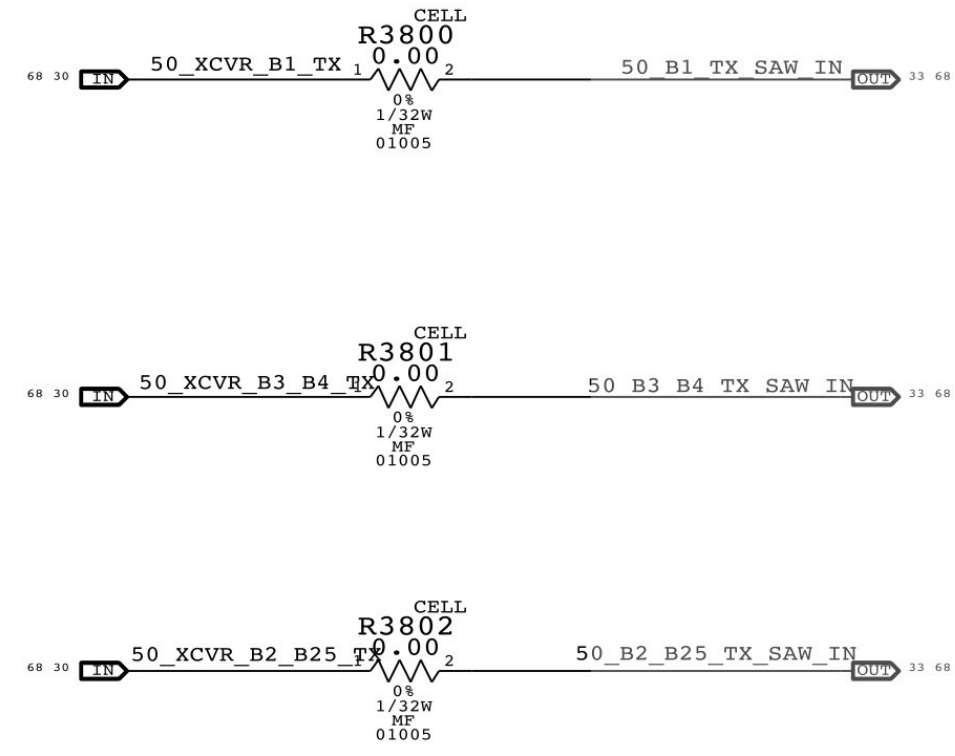
U3600		WTR1605	
SM		SRM 4 OF 5	
PWR			
VDD_RF1_P_FELO	53	VDD_RF2_T_DA	111
VDD_RF1_P_FELO	42	VDD_RF1_T_DA	118
VDD_RF1_D_LBLO	28	VDD_RF1_T_UPC	117
VDD_RF1_D_FE	26	VDD_RF1_T_LO	116
VDD_RF1_D_MBLO	25	VDD_RF2_T_BB	108
VDD_RF1_JDET	85	VDD_RF2_T_VCO	136
VDD_RF2_P_BB	83	VDD_RF2_XO	127
VDD_RF2_D_BB	44	VDD_RF1_T_SYN	98
VDD_RF2_P_VCO	67	VDD_RF2_T_PLL	97
VDD_RF1_P_VCO	76	VDD_RF1_G_LNA	24
VDD_RF1_P_PLL	66	VDD_RF1_G_VCO	37
VDD_RF2_S_VCO	51	VDD_RF1_G_PLL	55
VDD_RF1_S_VCO	40	VDD_RF1_G_BB	31
VDD_RF1_S_PLL	65	VDD_DIO	87

PP RF1 1V3 PRX FELO1	53
PP RF1 1V3 PRX FELO2	42
PP RF1 1V3 DRX LBLO	28
PP RF1 1V3 DRX FE	26
PP RF1 1V3 DRX MBLO	25
PP RF1 1V3 JAM DET	85
PP RF2 2V05 PRX BB	83
PP RF2 2V05 DRX BB	44
PP RF2 2V05 PRX VCO	67
PP RF1 1V3 PRX VCO	76
PP RF1 1V3 PRX PLL	66
PP RF2 2V05 SHDR VCO	51
PP RF1 1V3 SHDR VCO	40
PP RF1 1V3 SHDR PLL	65

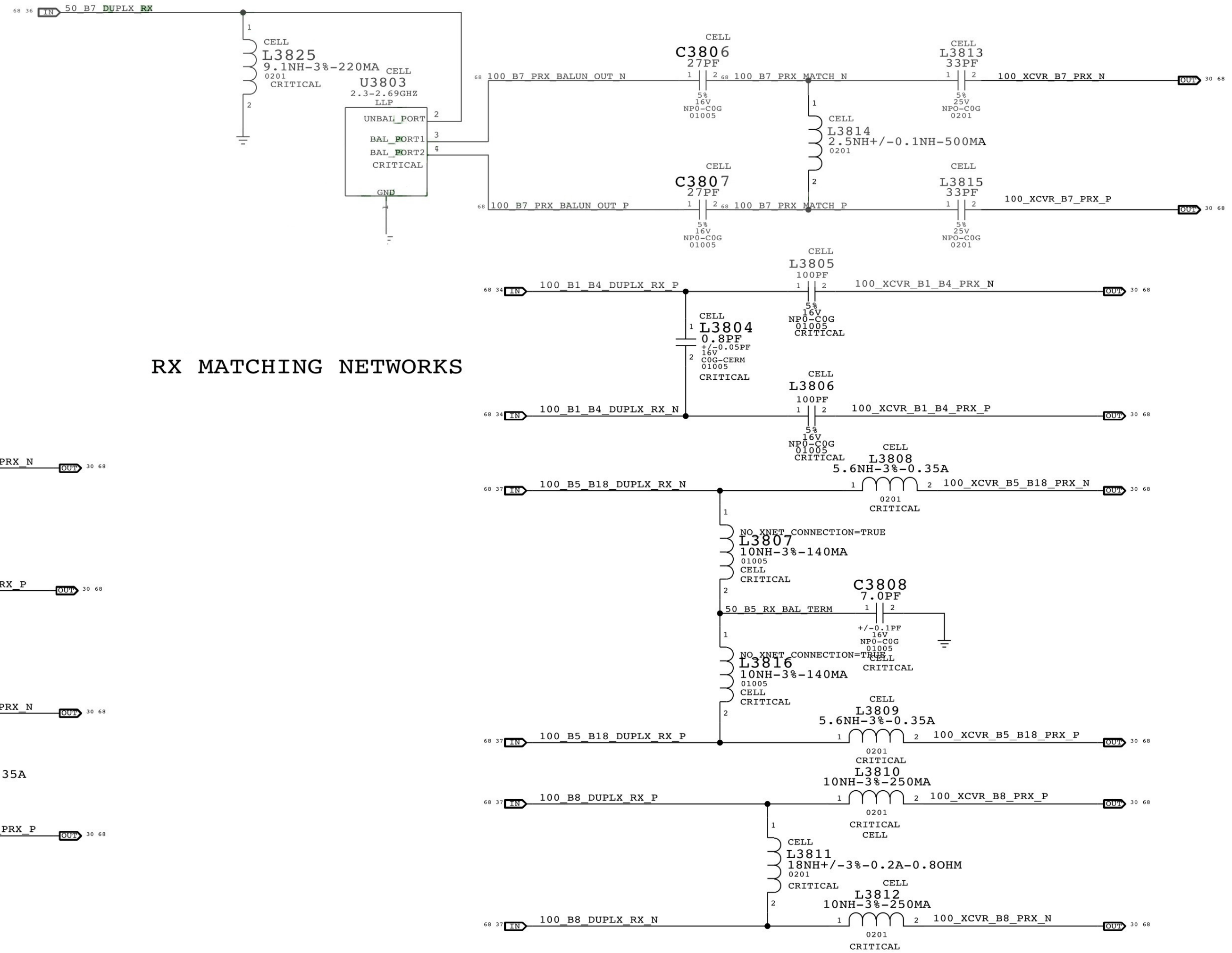
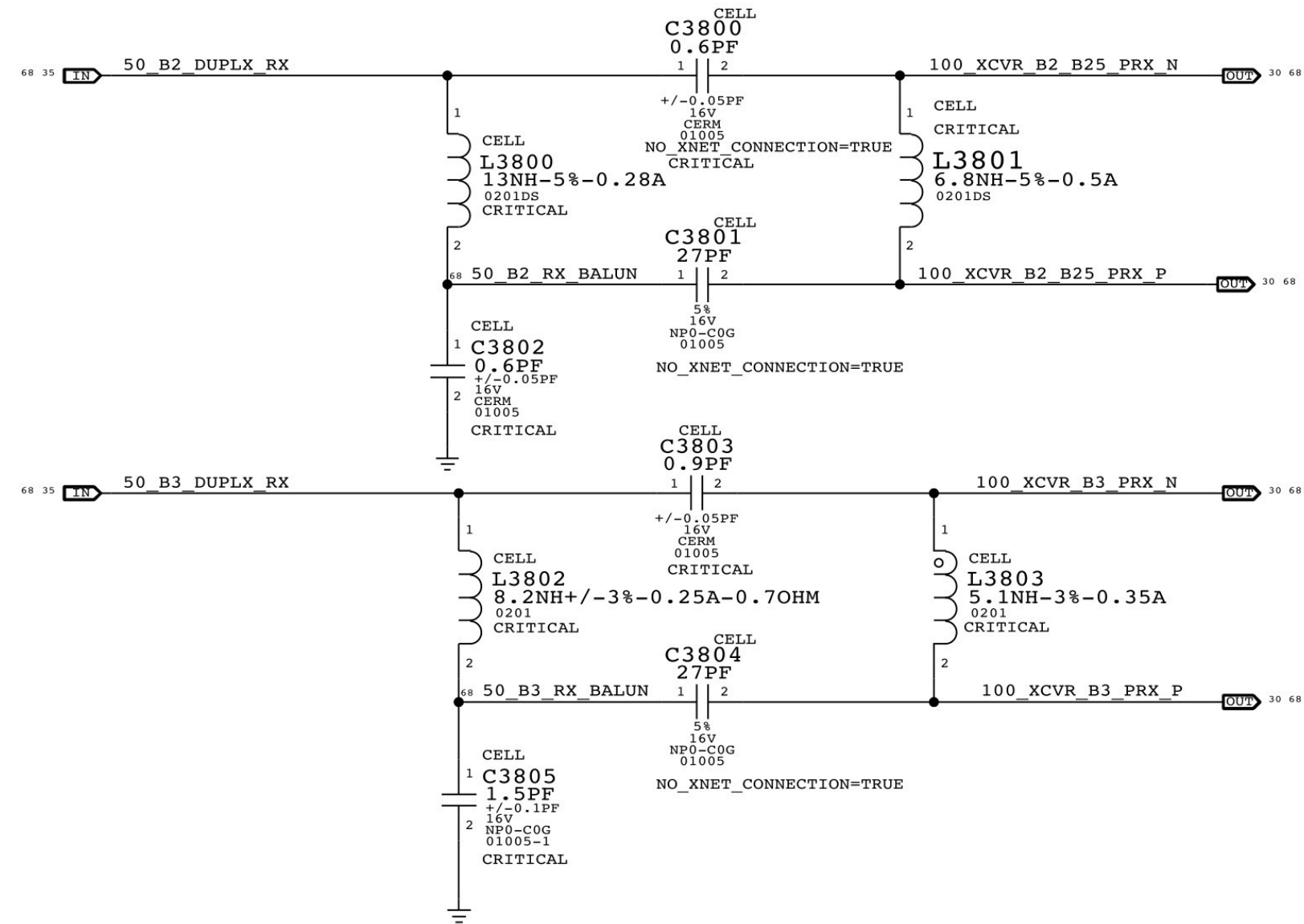
PP RF2 2V05 TX DA	31
PP RF1 1V3 TX DA	31
PP RF1 1V3 TX UPCONVERTER	31
PP RF1 1V3 TX LO	31
PP RF2 2V05 TX BB	31
PP RF2 2V05 TX VCO	31
PP RF2 2V05 XO FILT	31
PP RF1 1V3 TX SYNTH	31
PP RF2 2V05 TX PLL	31
PP RF1 1V3 GPS LNA	31
PP RF1 1V3 GPS VCO	31
PP RF1 1V3 GPS PLL	31
PP RF1 1V3 GPS DIG	31
PP RF1 1V8 DIG	31

TRANSCEIVER TX AND RX MATCHING NETWORKS

TX MATCHING NETWORKS



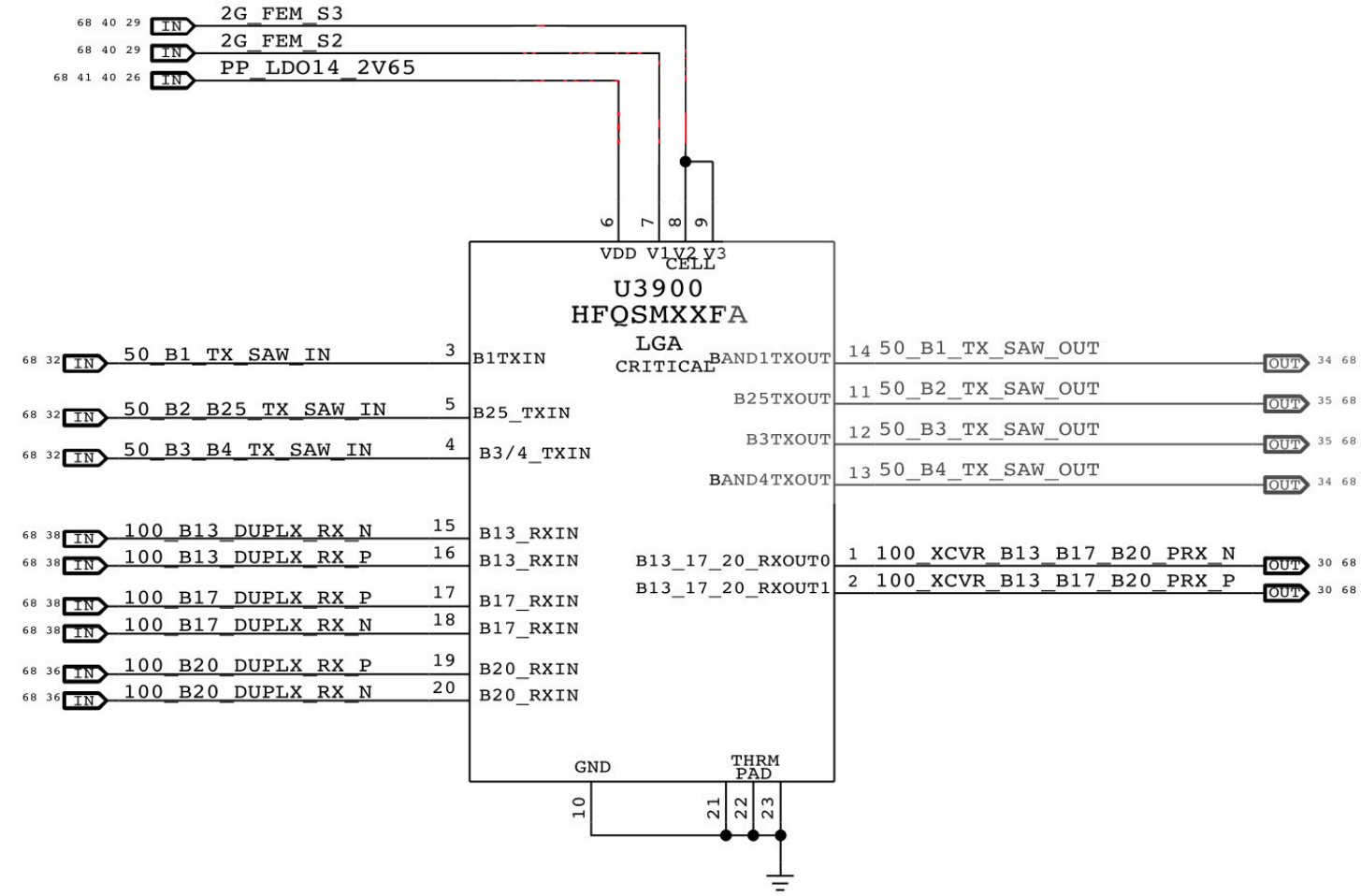
RX MATCHING NETWORKS



SAW BANK

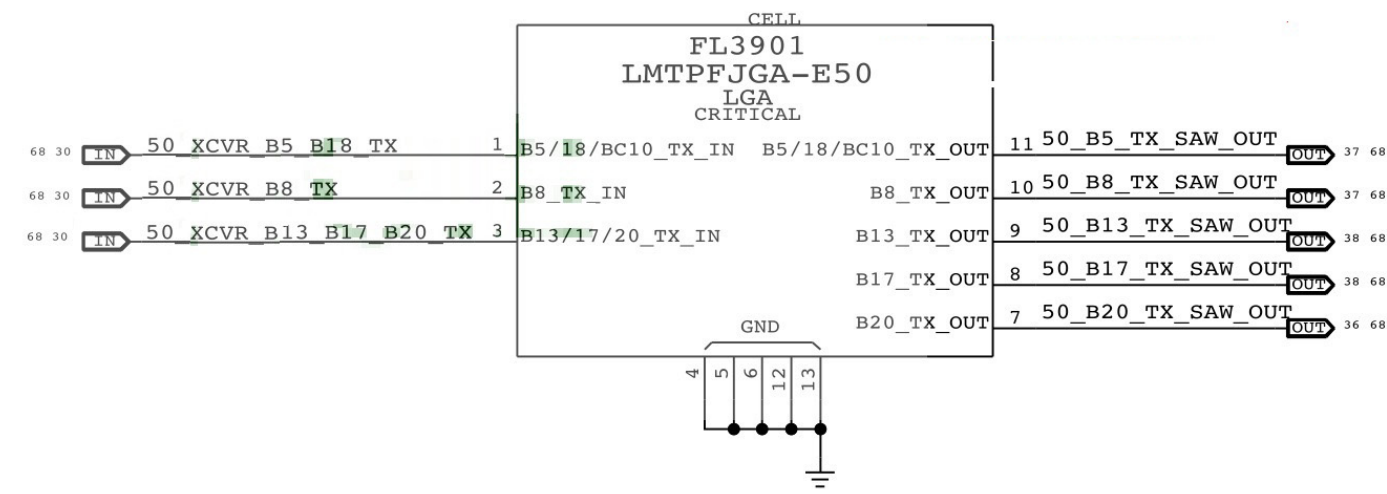
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

HB TX SAW BANK + B13/B17/B20 DP6T SWITCH AND MATCHING



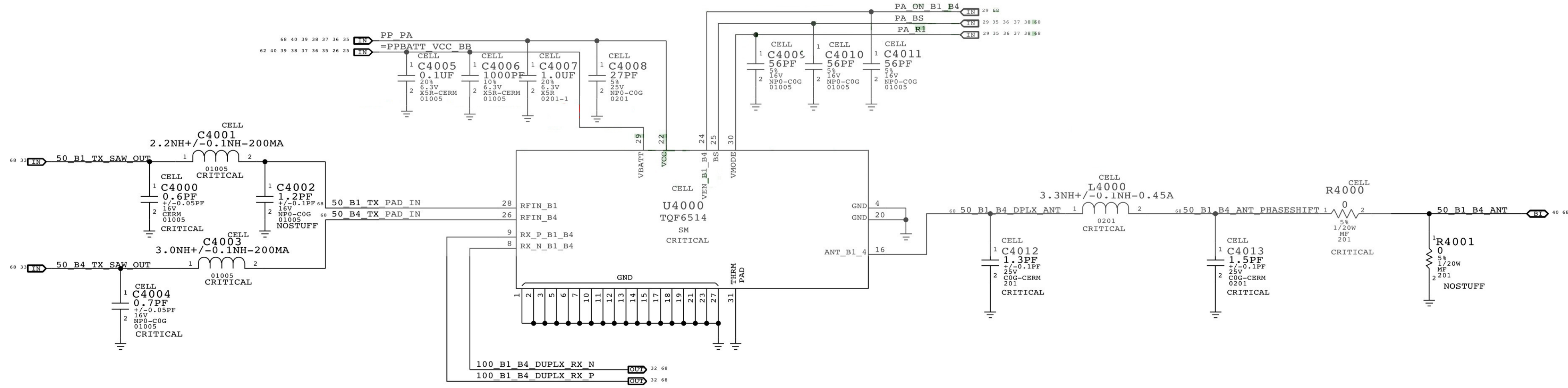
BAND	V3=V2	V1
B3 TX	HIGH	X
B4 TX	LOW	X
B13 RX	HIGH	HIGH
B17 RX	HIGH	LOW
B20 RX	LOW	HIGH

LB TX SAW BANK



BAND 1/4 PAD

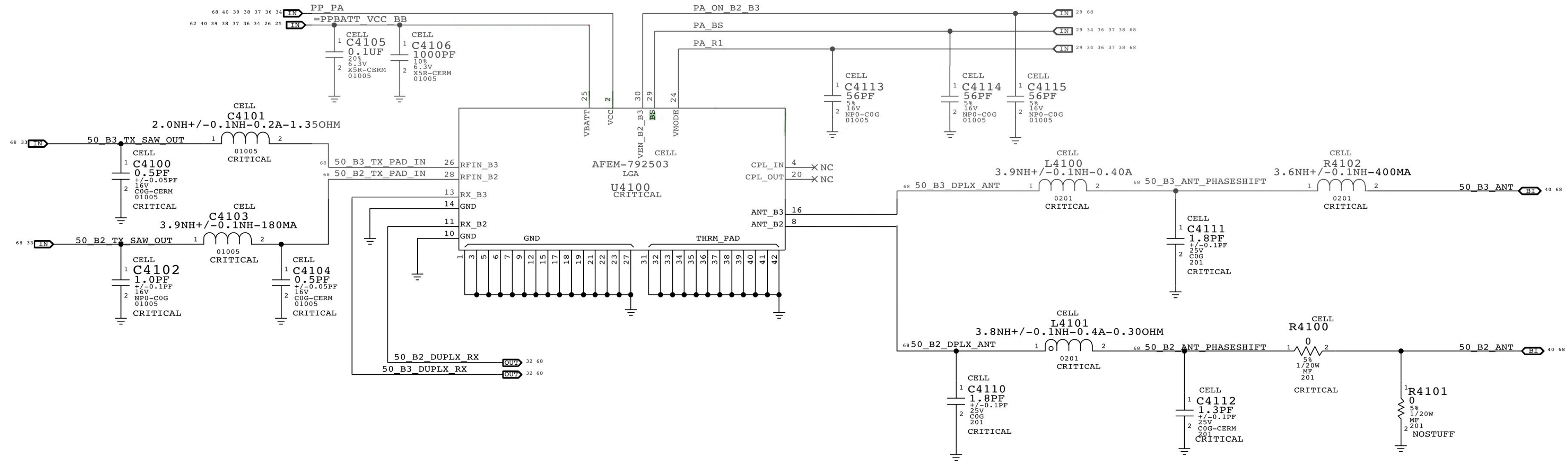
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA POWER MODE	PA_BS	PA_ON_B1_B4	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B4	HPM	0	1	0
B4	LPM	0	1	1
B1	HPM	1	1	0
B1	LPM	1	1	1

BAND 2/3 PAD

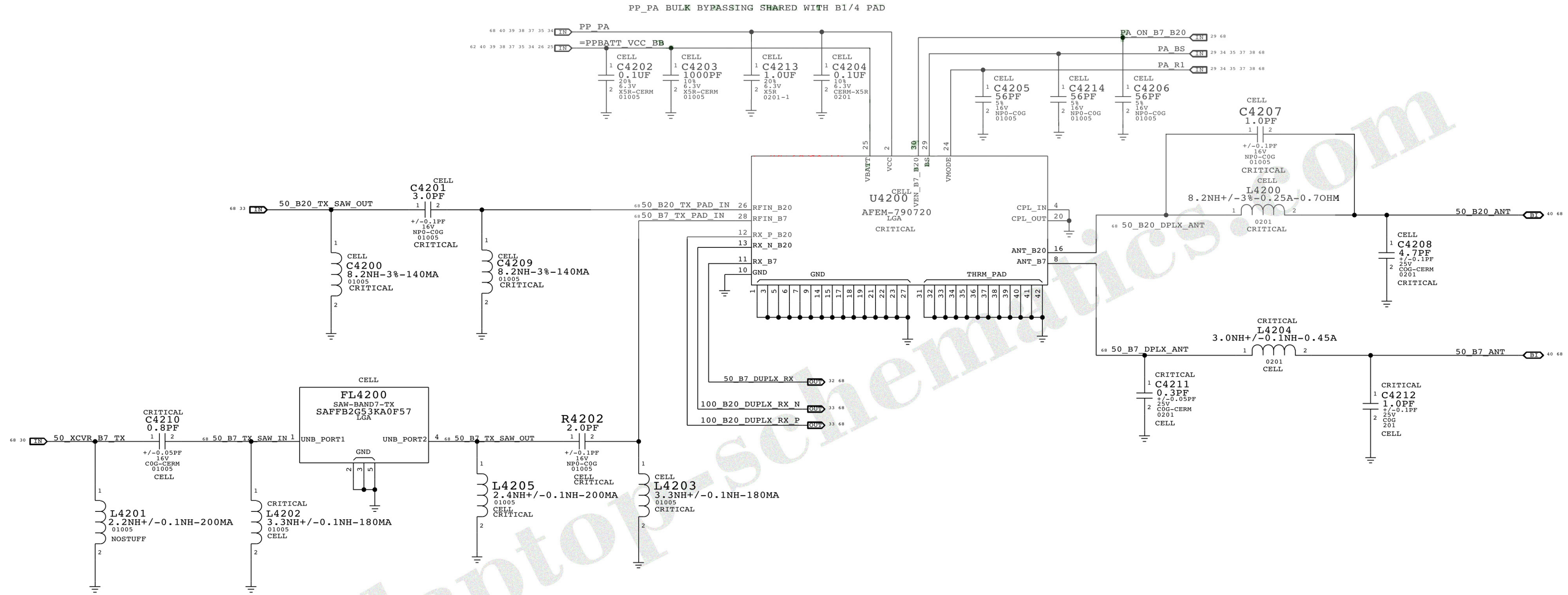
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA POWER MODE	PA_BS	PA_ON_B2_B3	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B3	HPM	0	1	0
B3	LPM	0	1	1
B2	HPM	1	1	0
B2	LPM	1	1	1

BAND 20/7 PAD

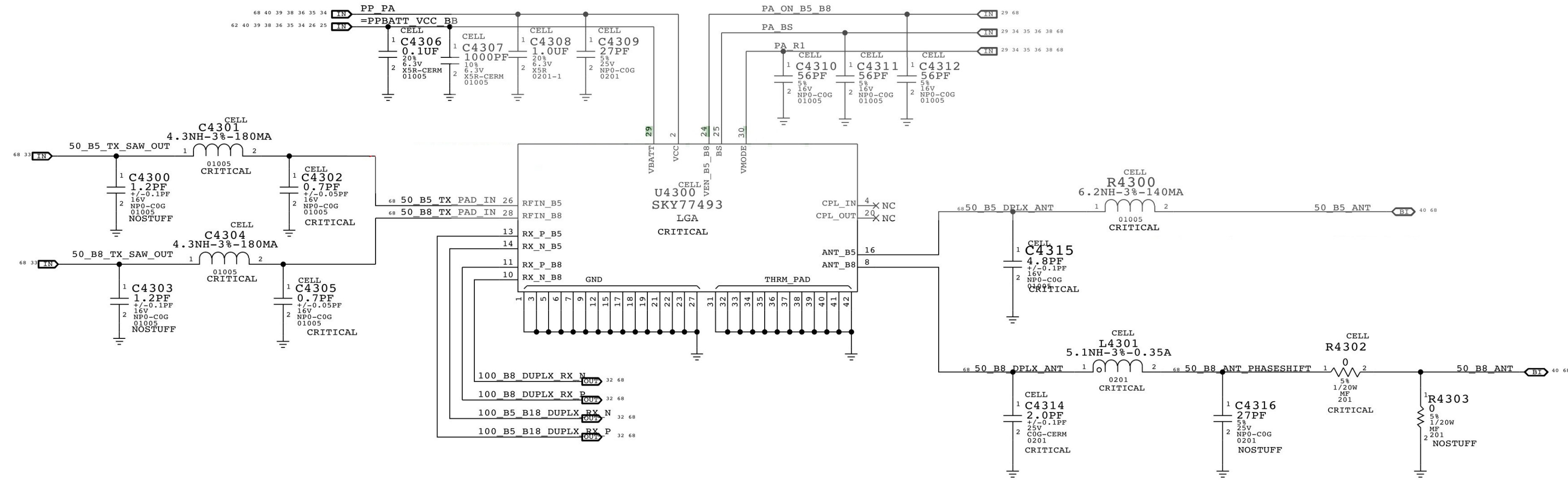
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA POWER MODE	PA_ON_B20	PA_R1
POWER DOWN	LPM	0	0
STANDBY	X	0	X
B20	HPM	1	0
B20	LPM	1	1

BAND 5/8 PAD

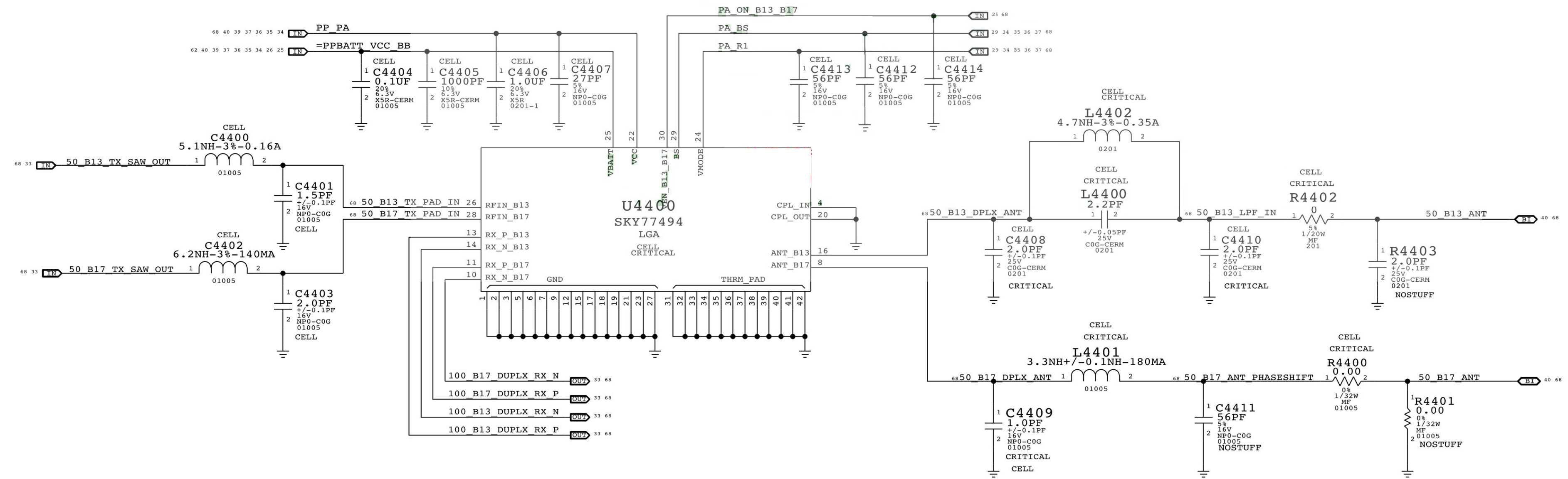
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA POWER MODE	PA_BS	PA_ON_B5_B8	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B5	HPM	0	1	0
B5	LPM	0	1	1
B8	HPM	1	1	0
B8	LPM	1	1	1

BAND 13/17 PAD

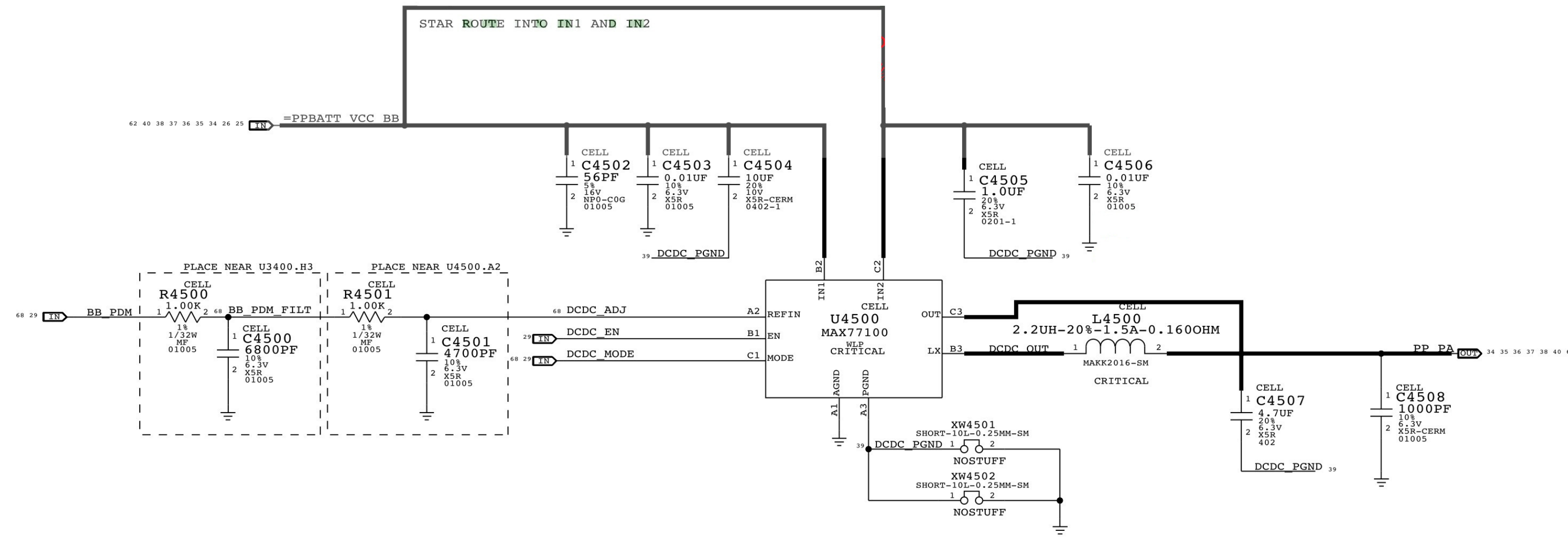
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



BAND	PA POWER MODE	PA_BS	PA_ON_B13_B17	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B17	HPM	0	1	0
B17	LPM	0	1	1
B13	HPM	1	1	0
B13	LPM	1	1	1

PA DC/DC CONVERTER

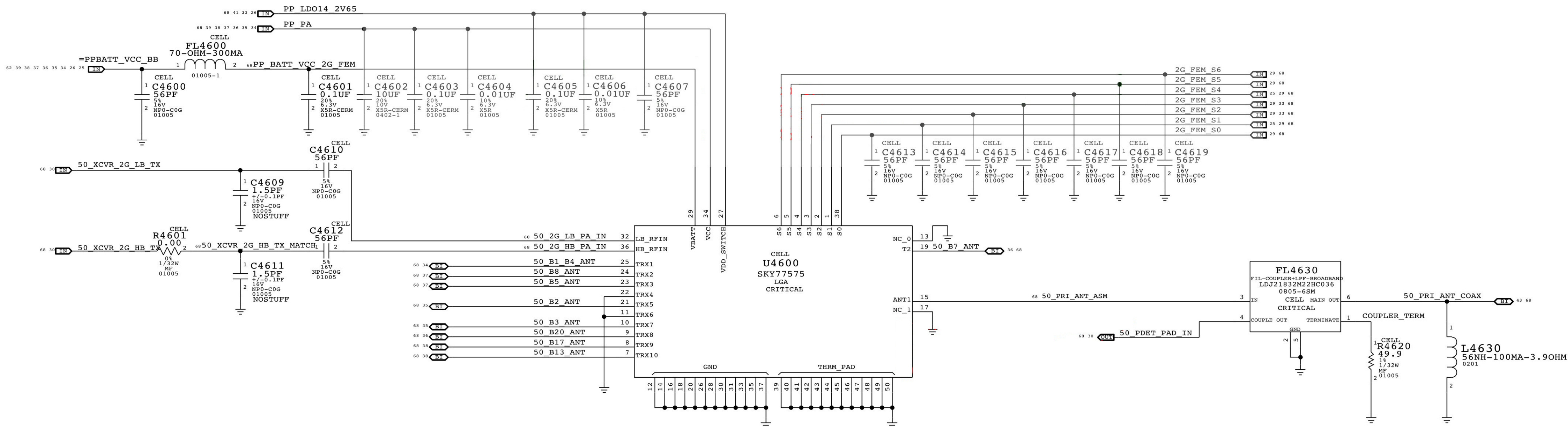
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.



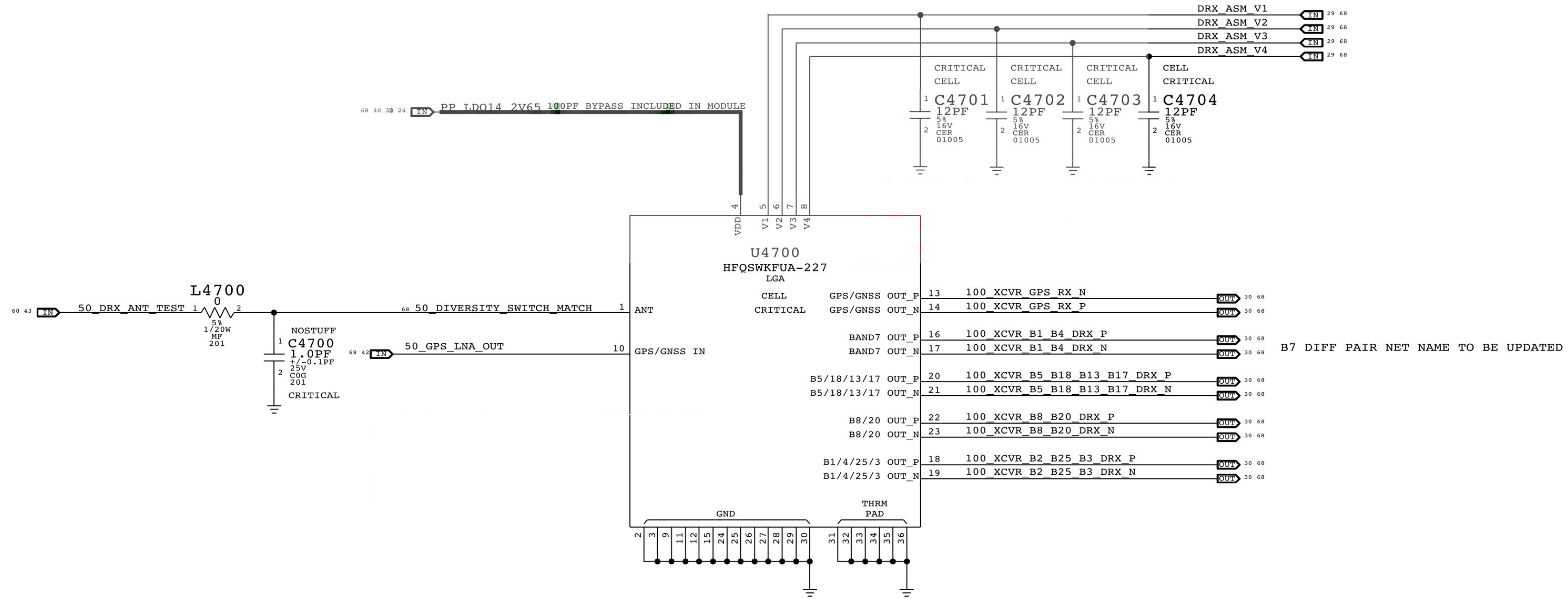
2G FEM

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

2G FEM



RX DIVERSITY

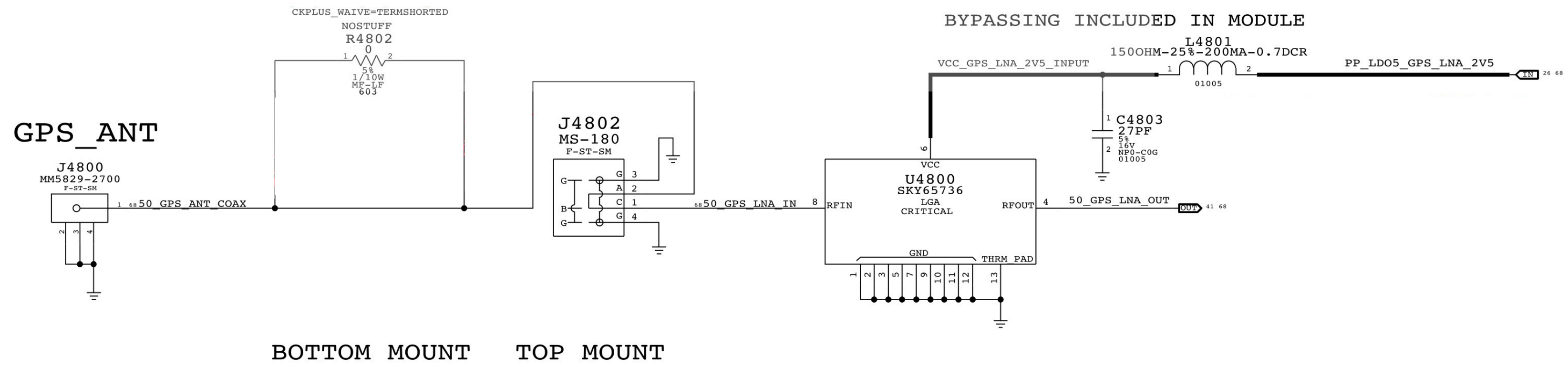


NEED TO UPDATE

BAND	DRX_ASM_V4	DRX_ASM_V3	DRX_ASM_V2	DRX_ASM_V1
B1/B4	LOW	LOW	LOW	LOW
B2/25	LOW	HIGH	LOW	LOW
B3	HIGH	LOW	LOW	LOW
B5/6/18	LOW	LOW	HIGH	LOW
B8	LOW	LOW	LOW	HIGH
B13/17	LOW	HIGH	HIGH	HIGH
B20	LOW	HIGH	HIGH	LOW
OFF	LOW	LOW	HIGH	HIGH
SWITCH IS TERMINATED IN ALL OTHER POSSIBLE STATES				

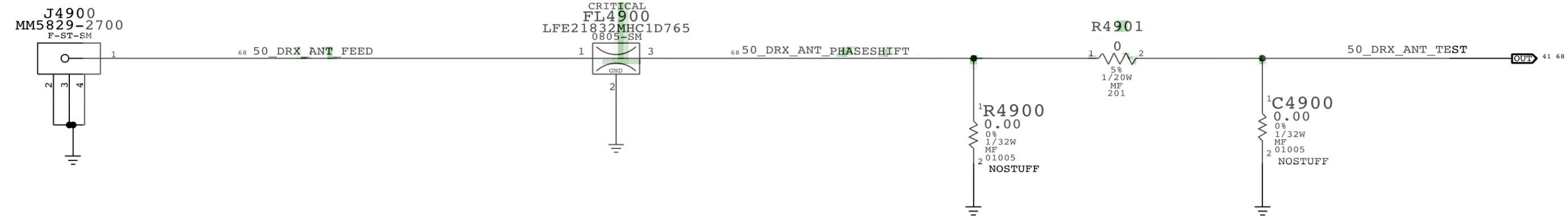
B7 DIFF PAIR NET NAME TO BE UPDATED

GPS

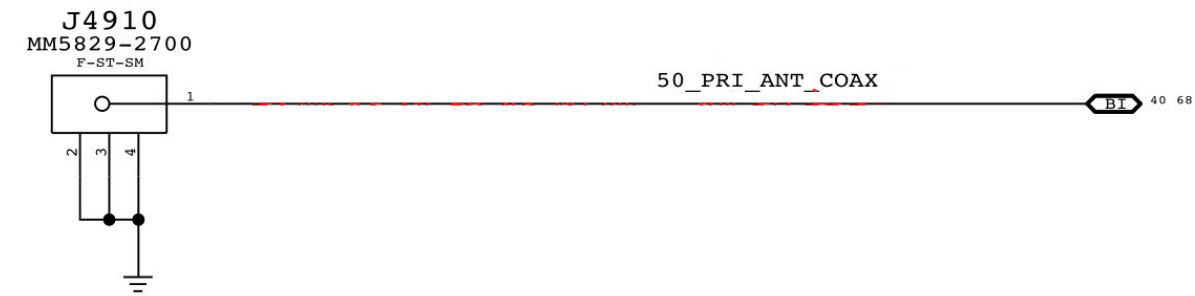


ANTENNA FEEDS

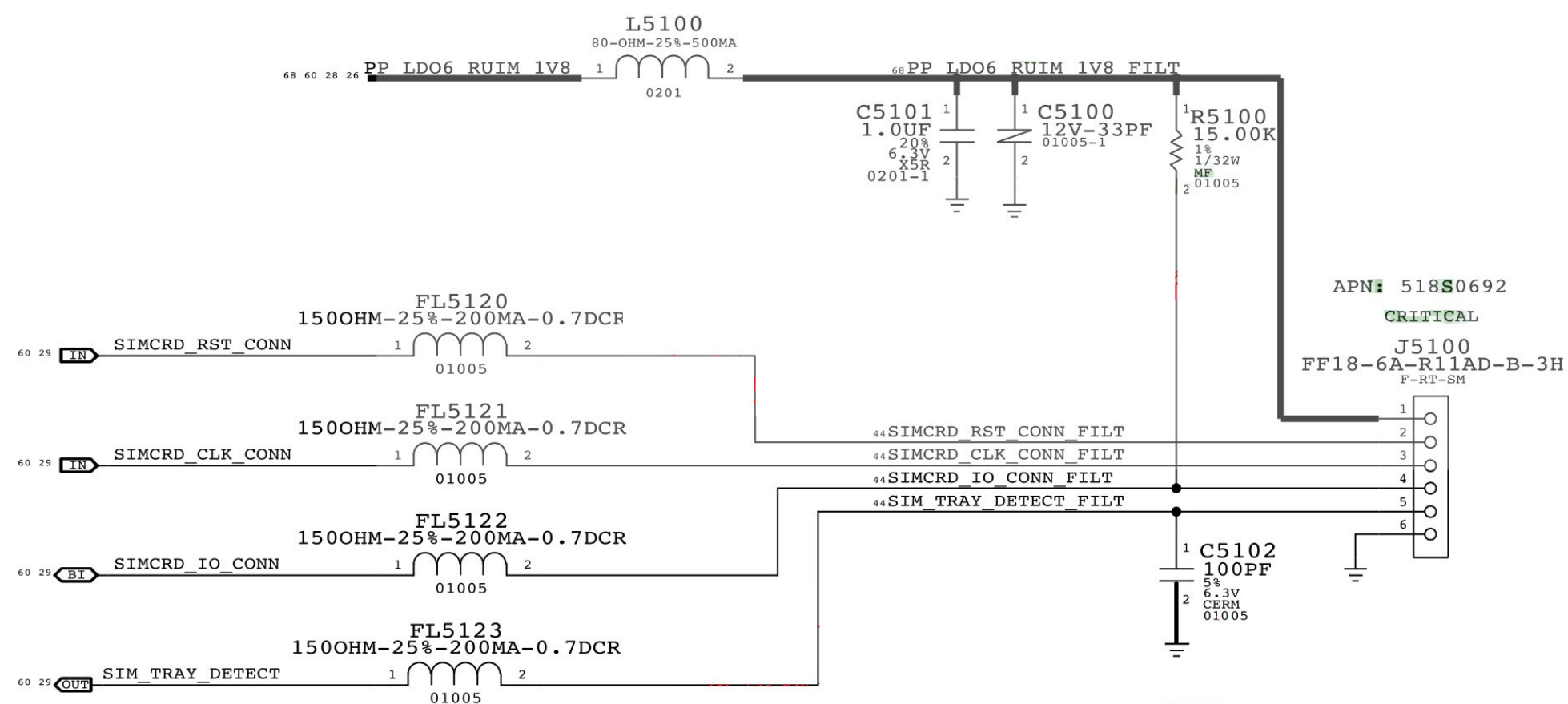
DRX_ANT COAX



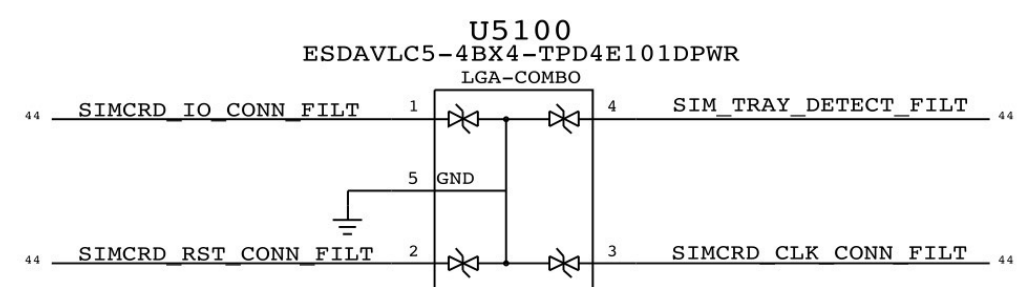
PRI_ANT COAX



SIM CARD FLEX CONN

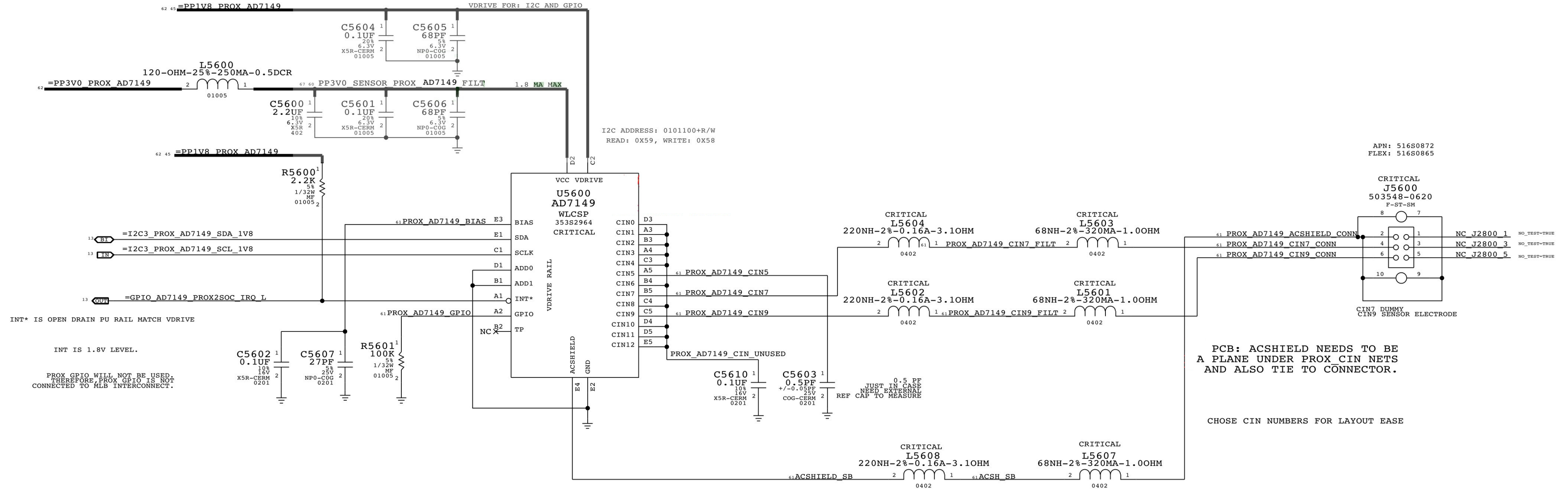


SIM CARD ESD PROTECTION



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37780130	37780159	?	U5100	RDAR://PROBLEM/12840016

PROX SENSOR



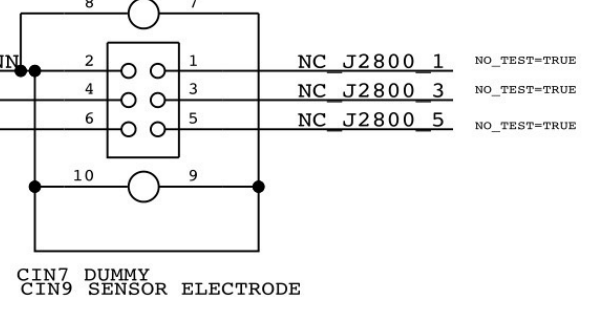
PCB: ENSURE ACSHIELD PLANE UNDER U3200, NO GND PLANE NEAR PROX_CIN NETS..

PCB: ACSHIELD NEEDS TO BE A PLANE UNDER PROX_CIN NETS AND ALSO TIE TO CONNECTOR.

CHOOSE CIN NUMBERS FOR LAYOUT EASE

APN: 516S0872
FLEX: 516S0865

CRITICAL
J5600
503548-0620
F-ST-SM



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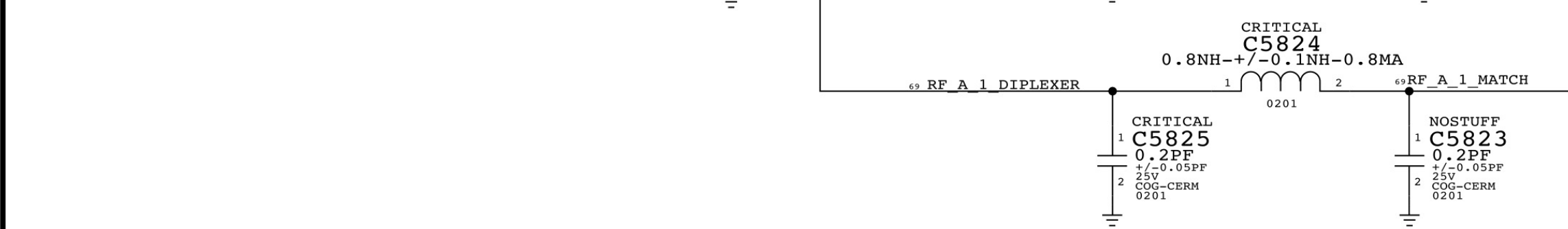
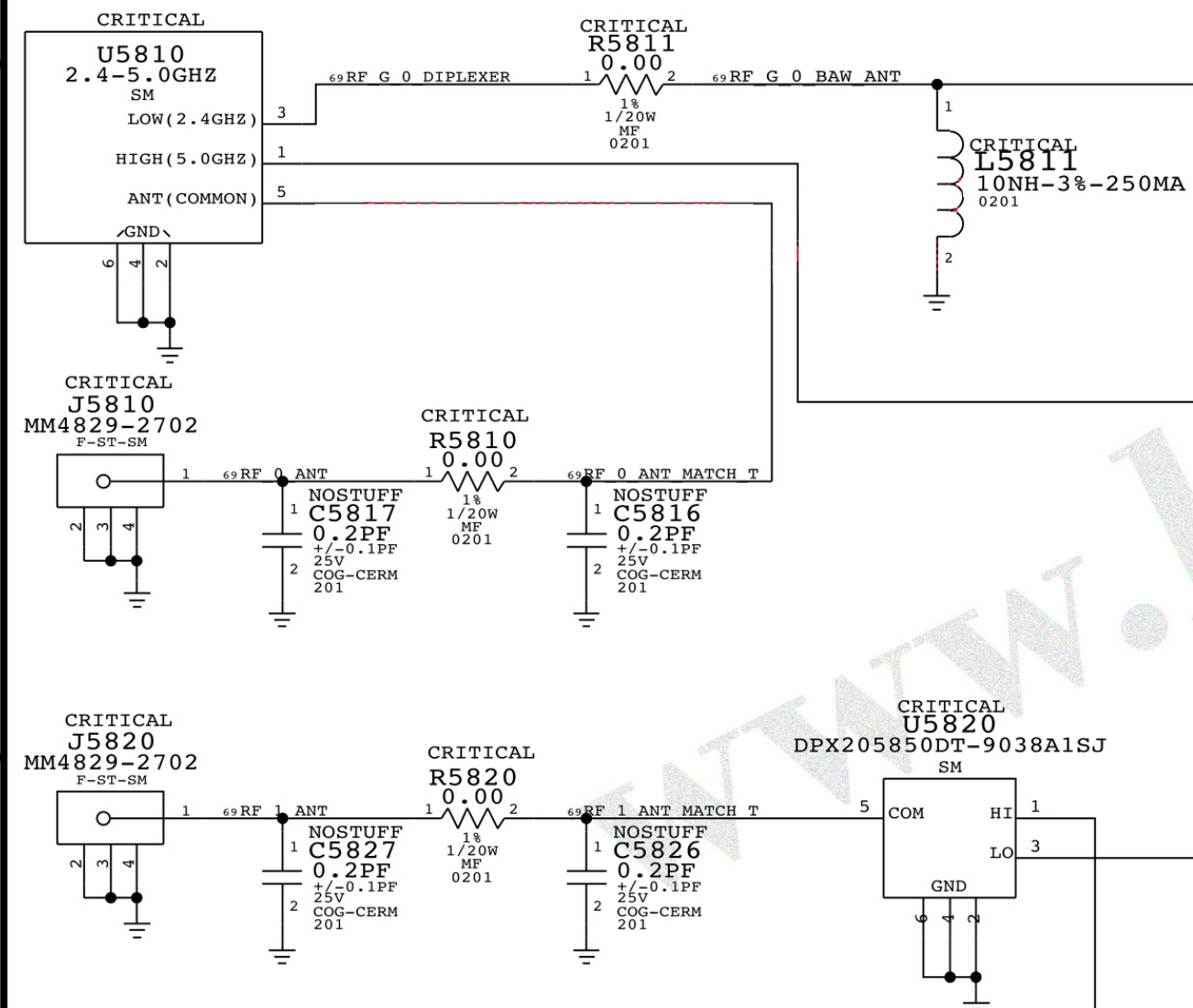
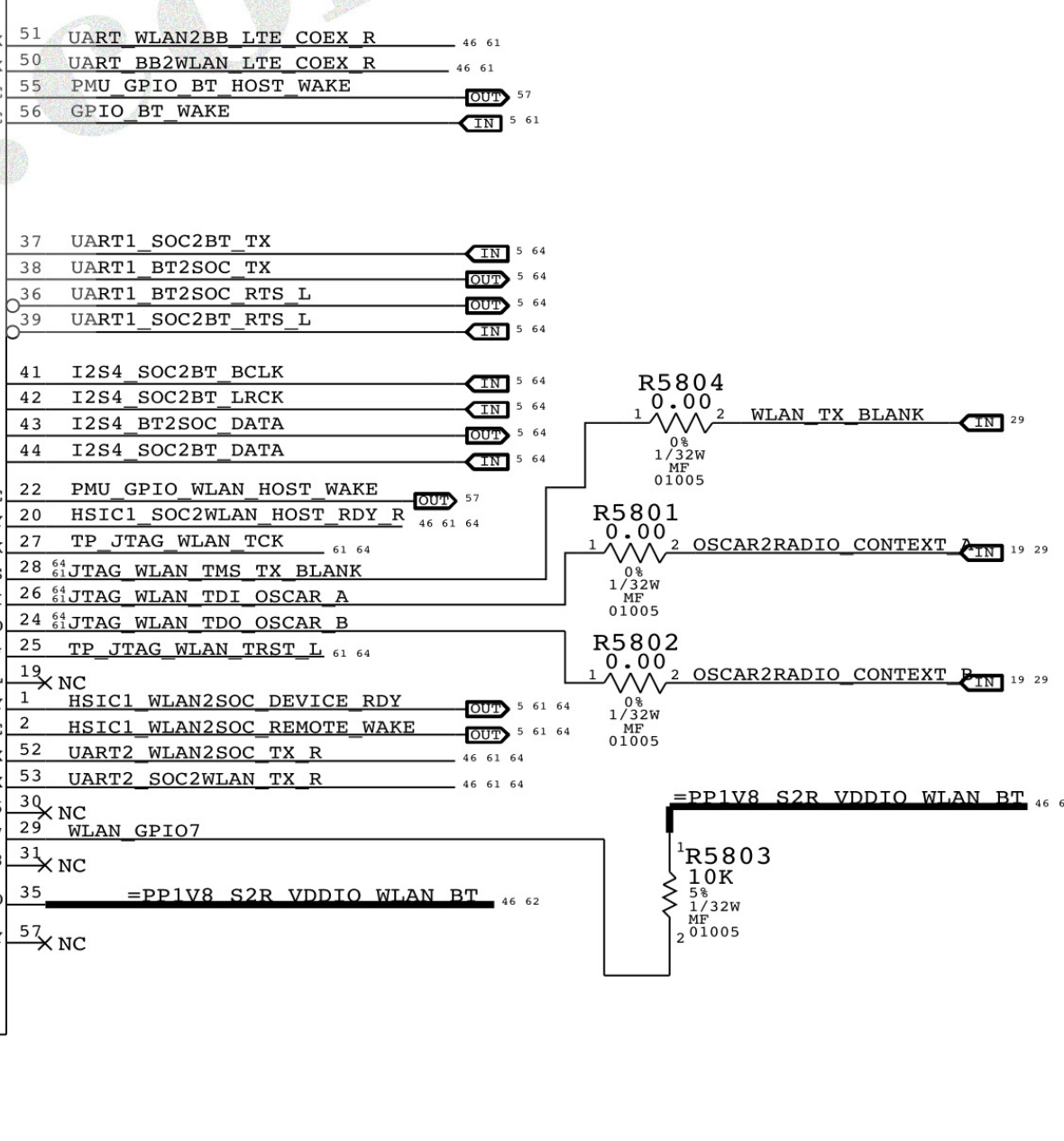
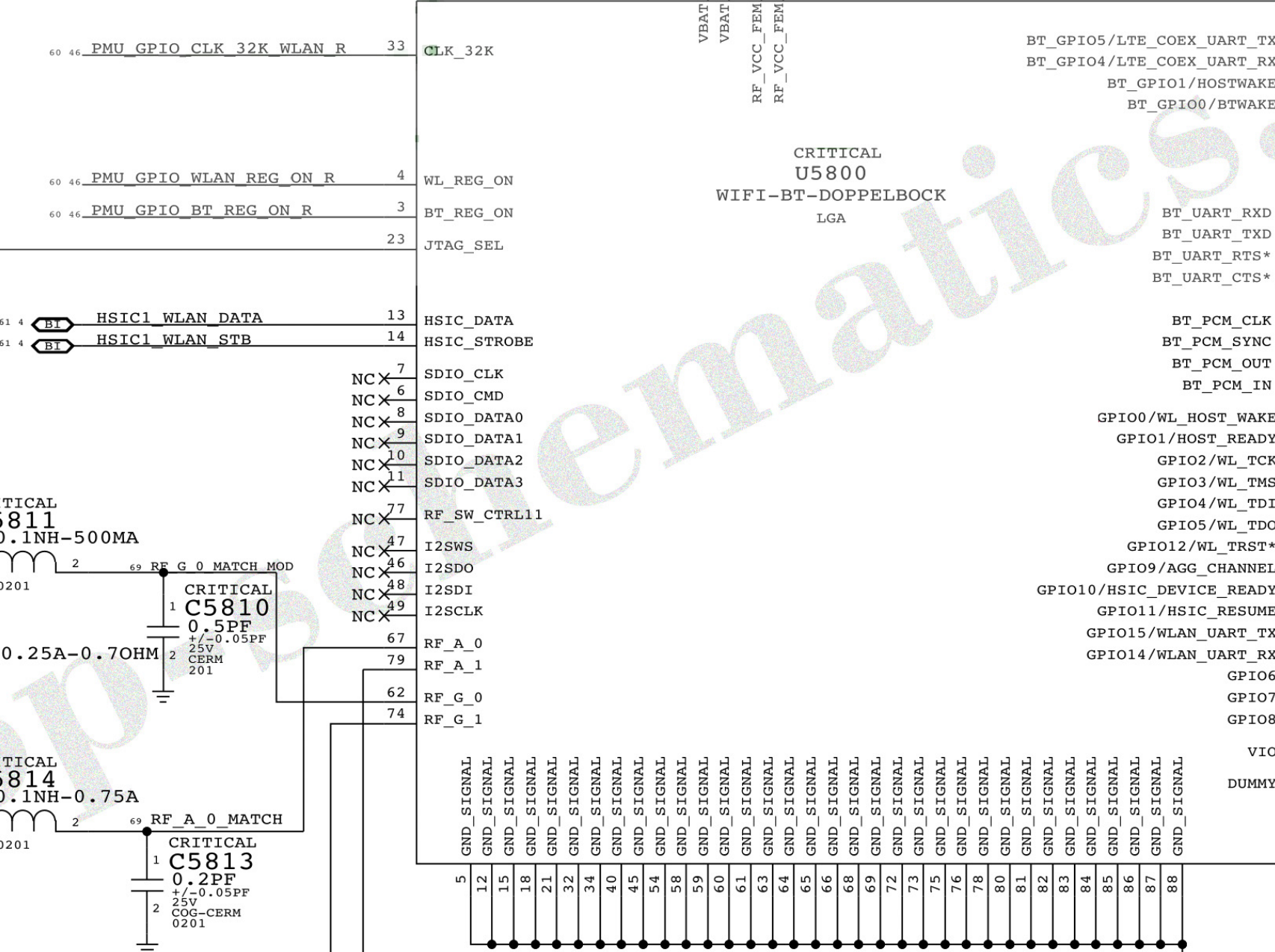
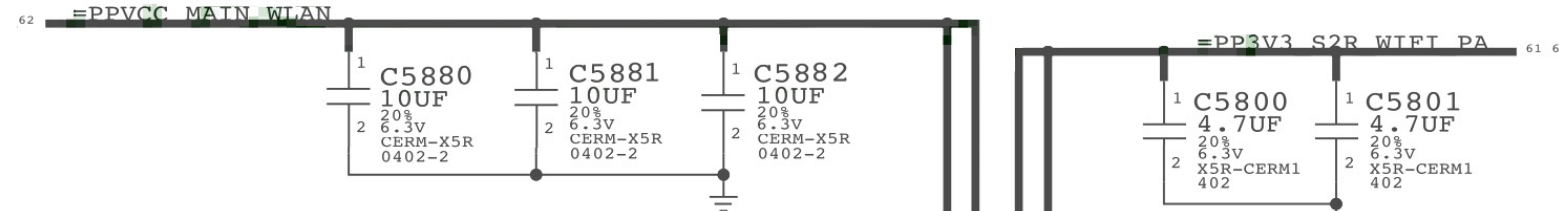
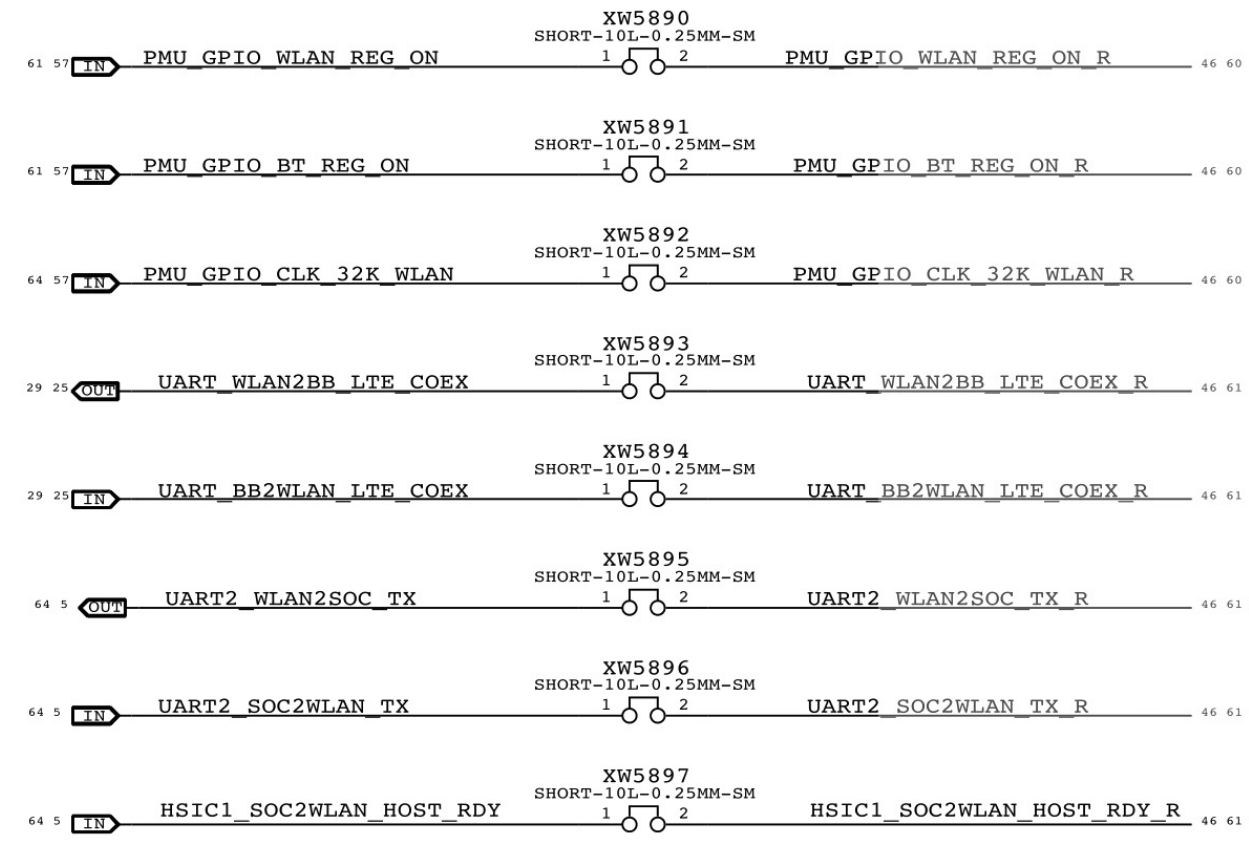
6

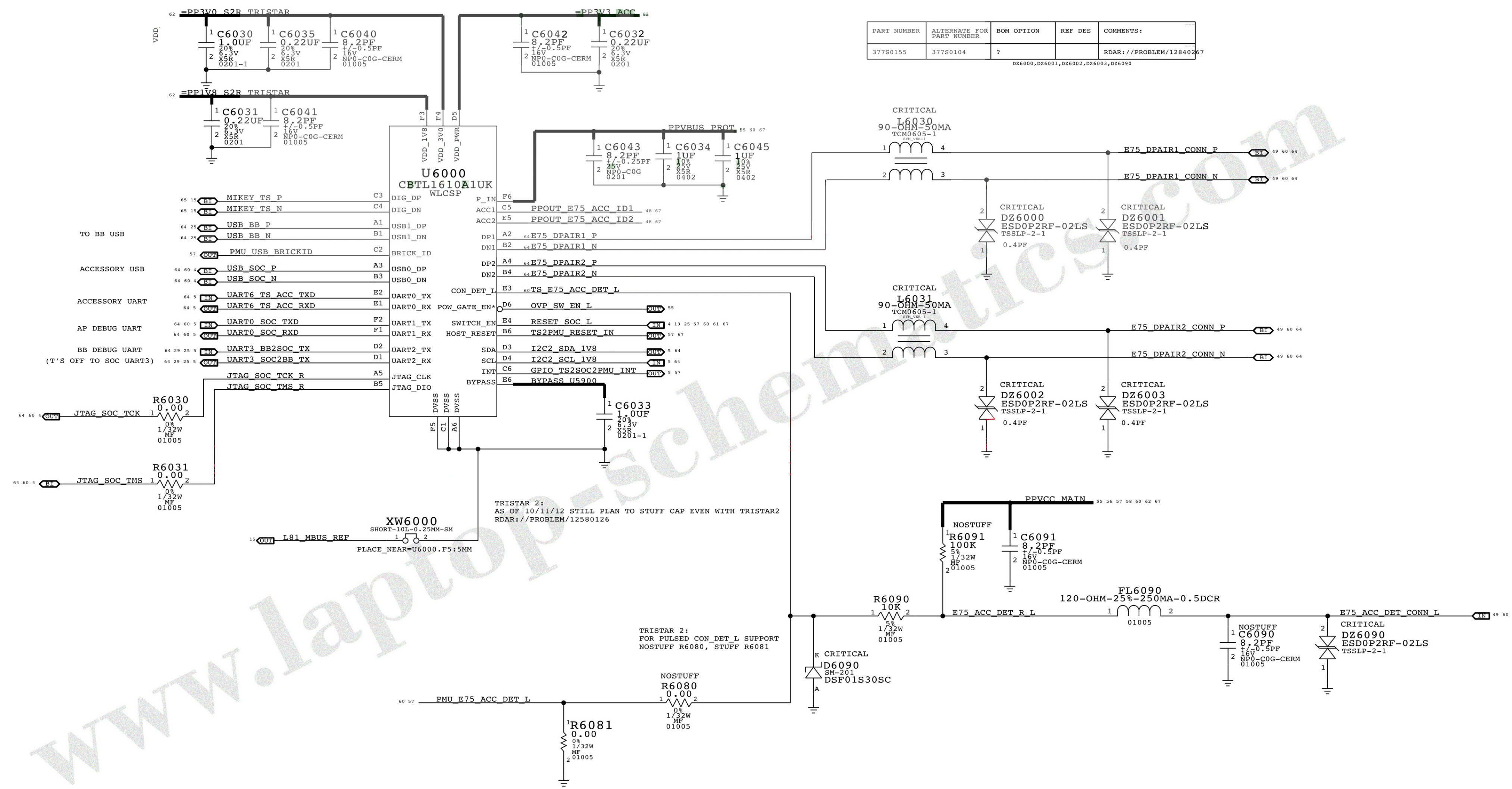
5

4

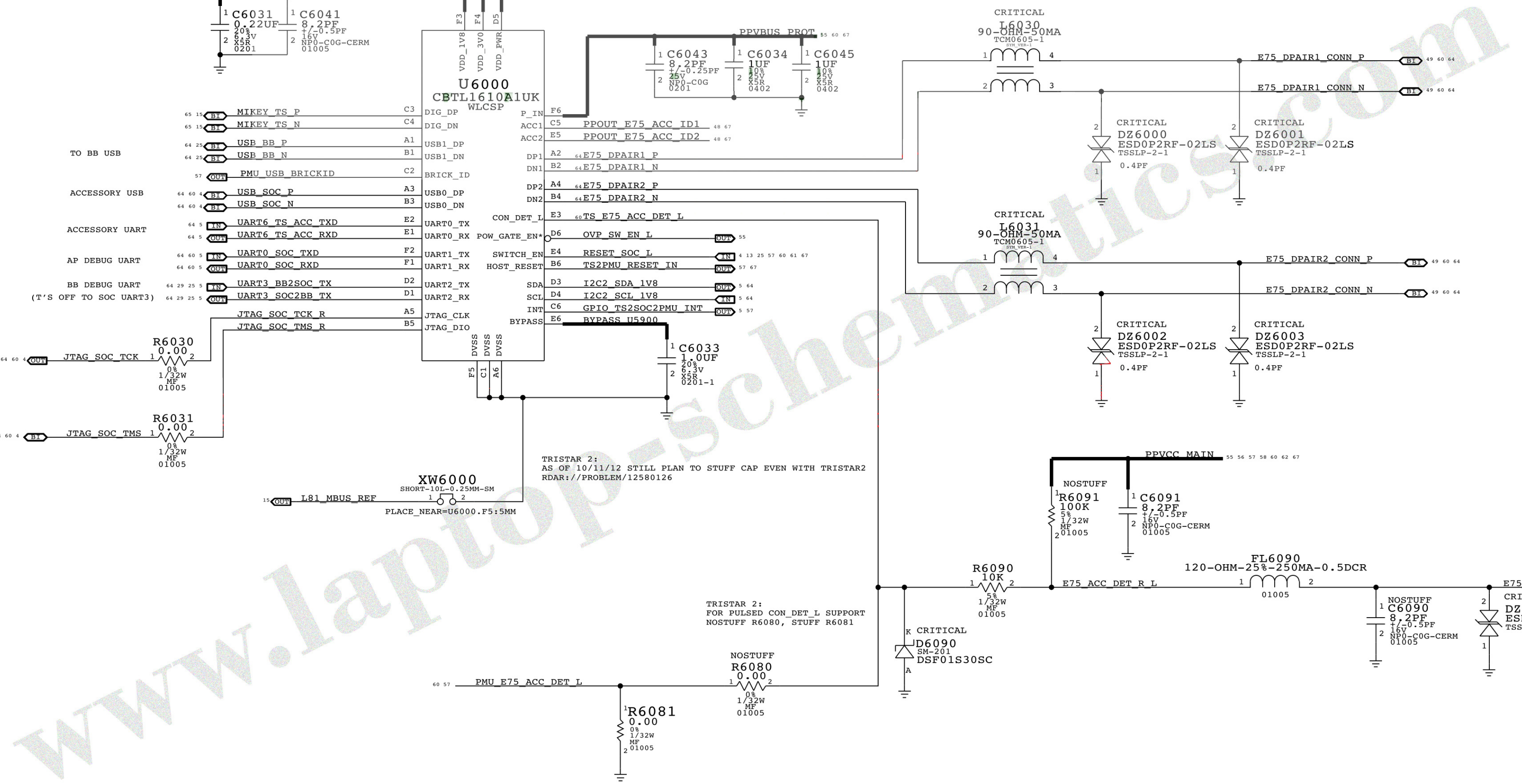
WIFI/BT: MODULE

MODULE ISOLATION





PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
377S0155	377S0104	?		RDAR://PROBLEM/12840267
DZ6000, DZ6001, DZ6002, DZ6003, DZ6090				



8

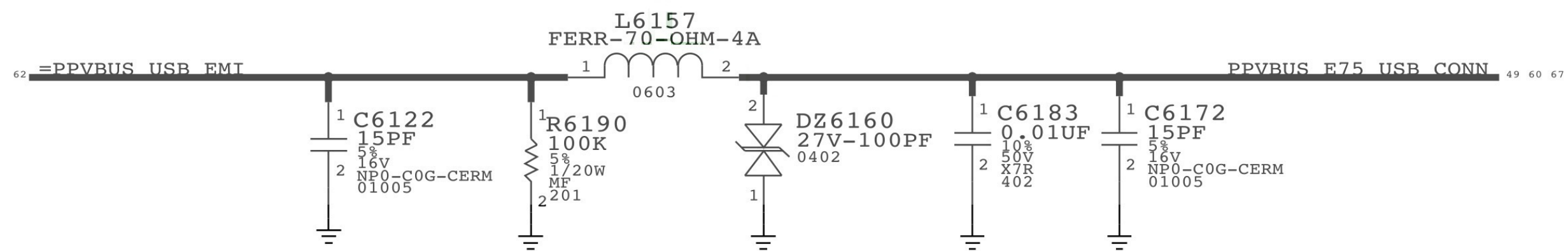
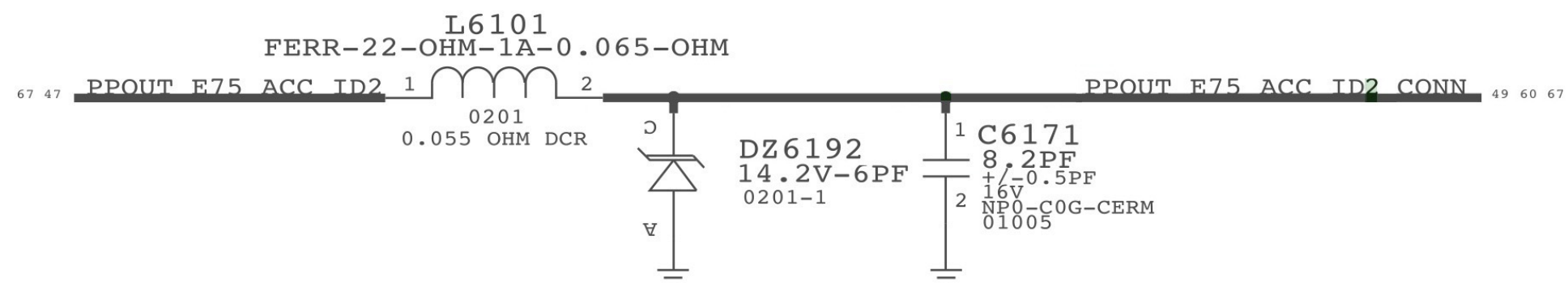
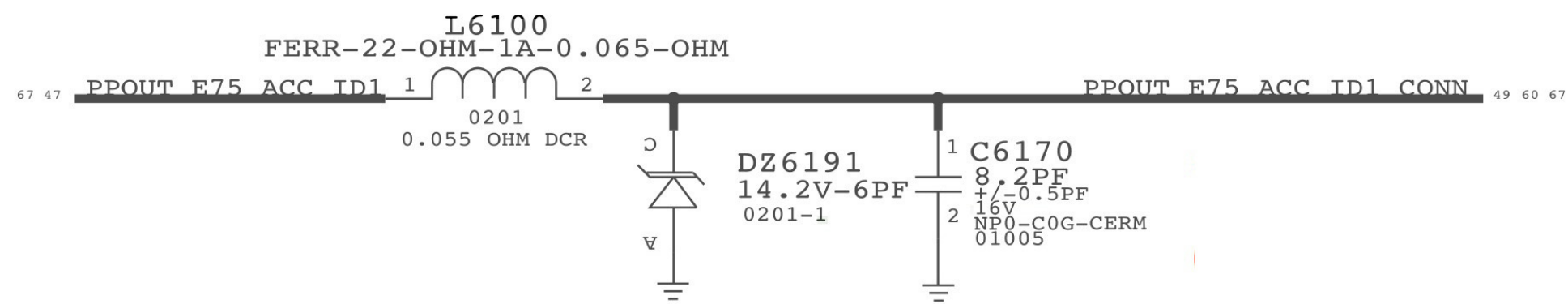
7

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3



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0116	377S0108		DZ6160	RDAR:8370432
155S0320	155S0513		L6100,L6101	RDAR://PROBLEM/9625601
155S0741	155S0397		L6157	RDAR://PROBLEM/11238851

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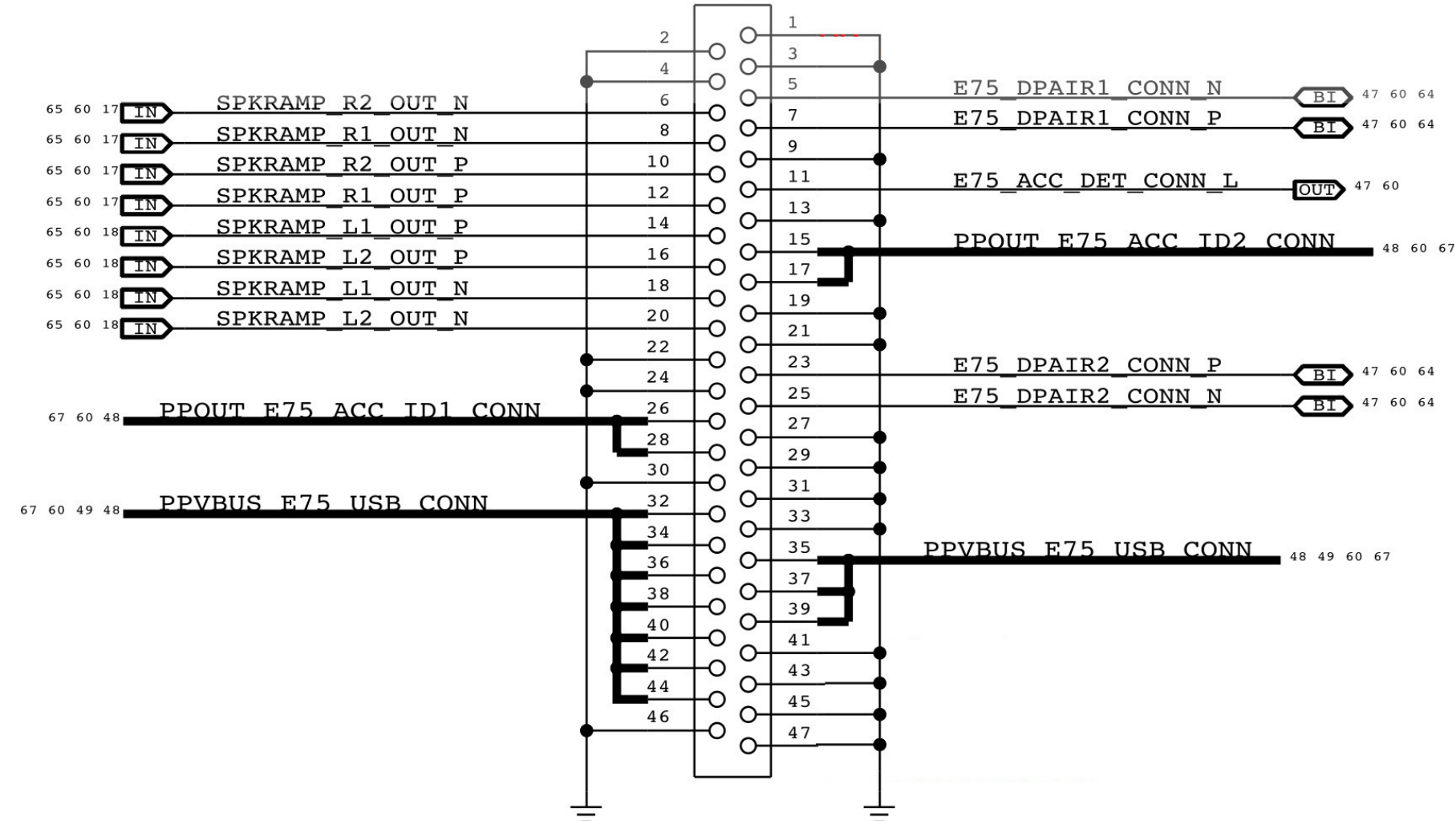
4

3

IO FLEX HOTBAR PADS

MLB 998-5877
FLEX 998-5876

OMIT
J6200
PCB-X110
HB-SM



PINOUT MATCHES IO_FLEX 4.2.0 3/12/13

8

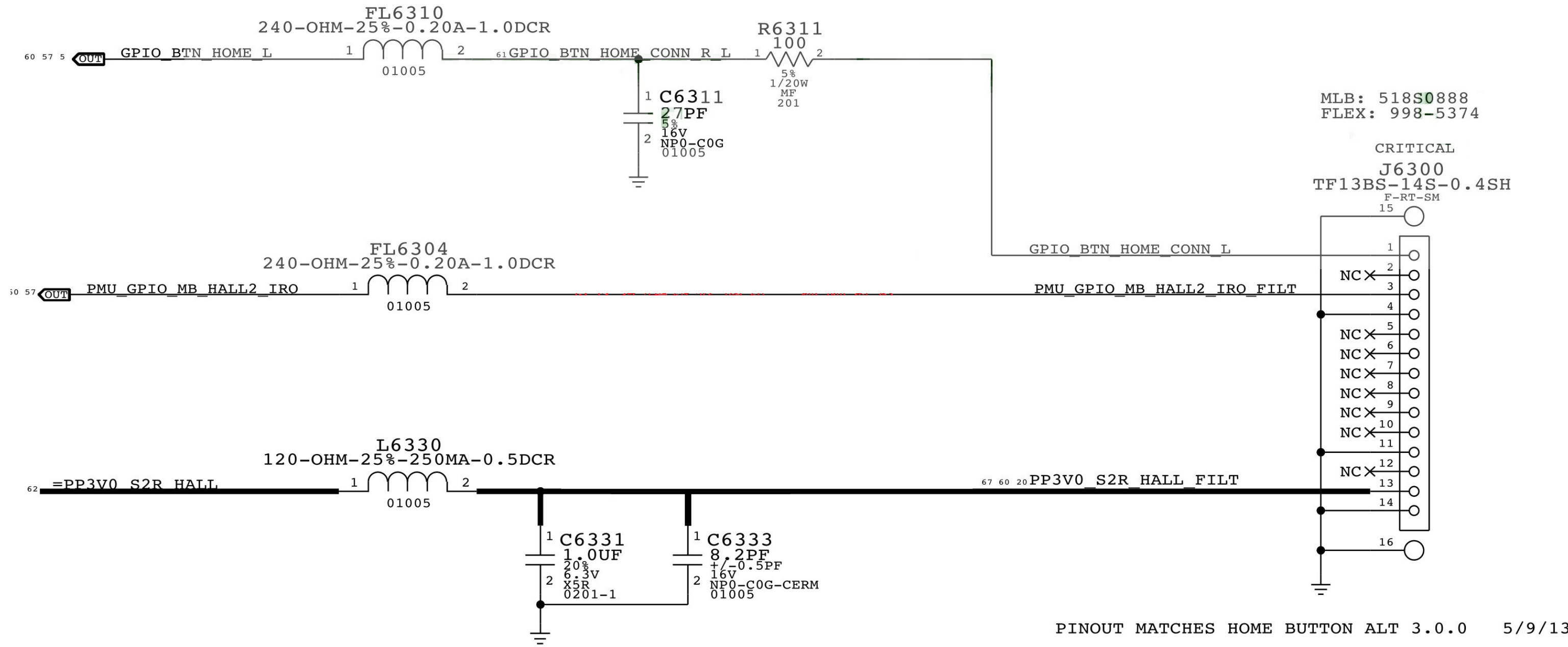
7

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HOME BUTTON FILTERS



D

D

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C

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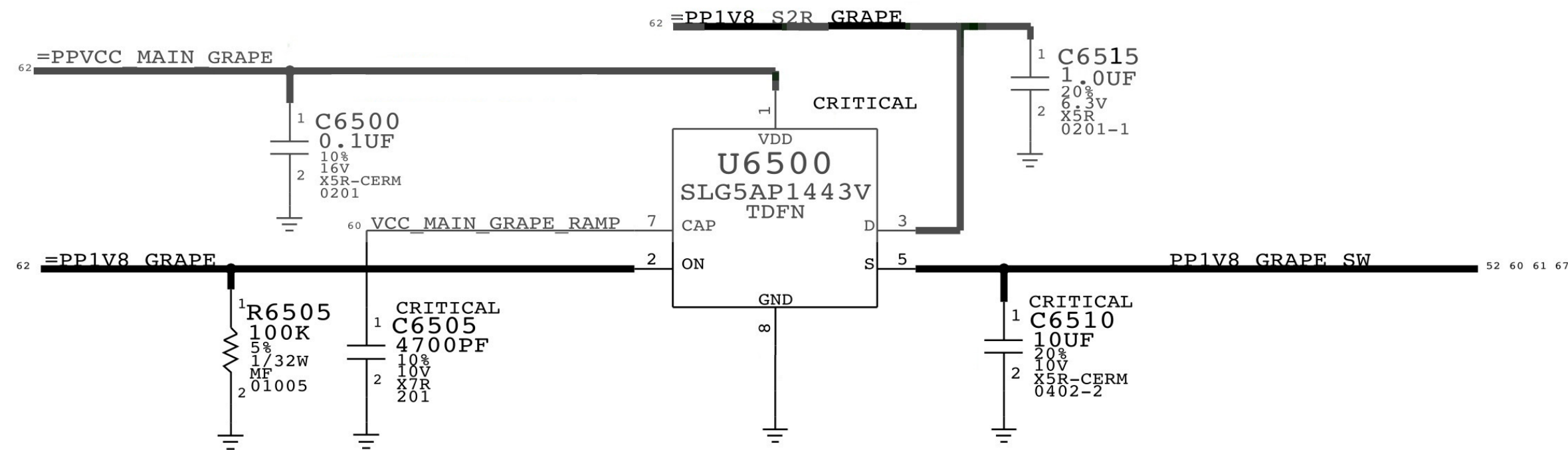
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GRAPE CONNECTOR SUPPORT



LAYOUT NOTE:
 PUT THERMAL VIAS AROUND U2300 IN CASE OF SHORTED CONDITION

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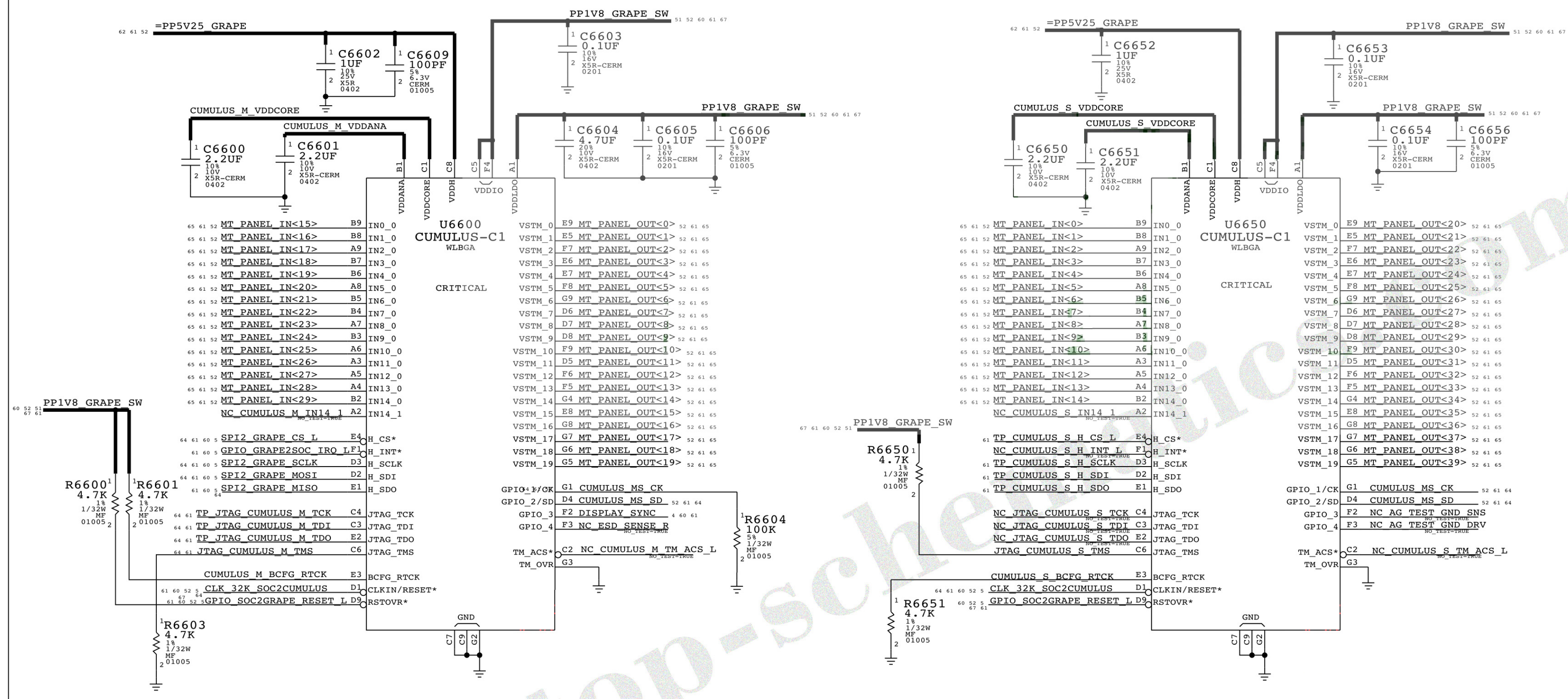
5

4

CUMULUS C1 (CSP) IN MASTER-SLAVE CONFIG

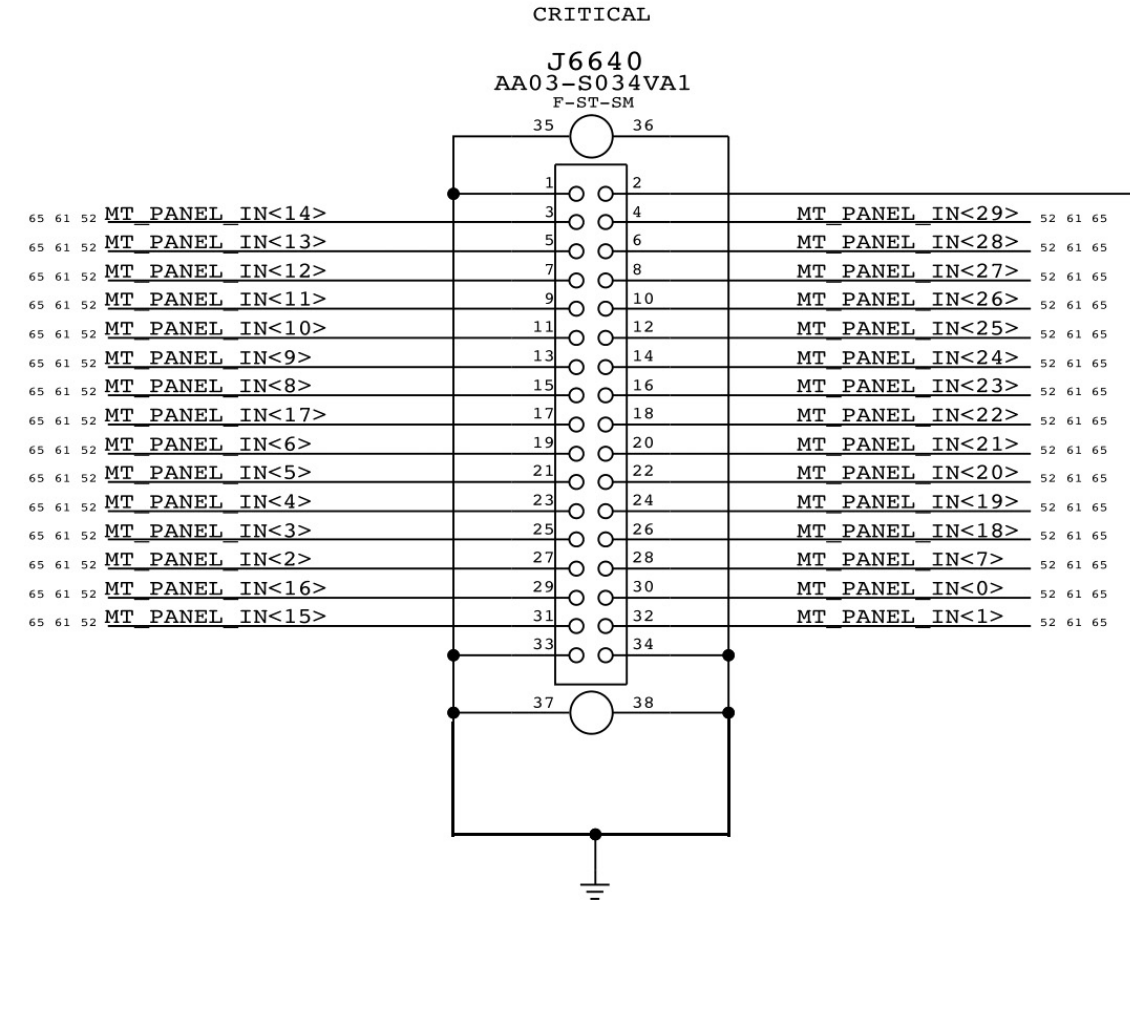
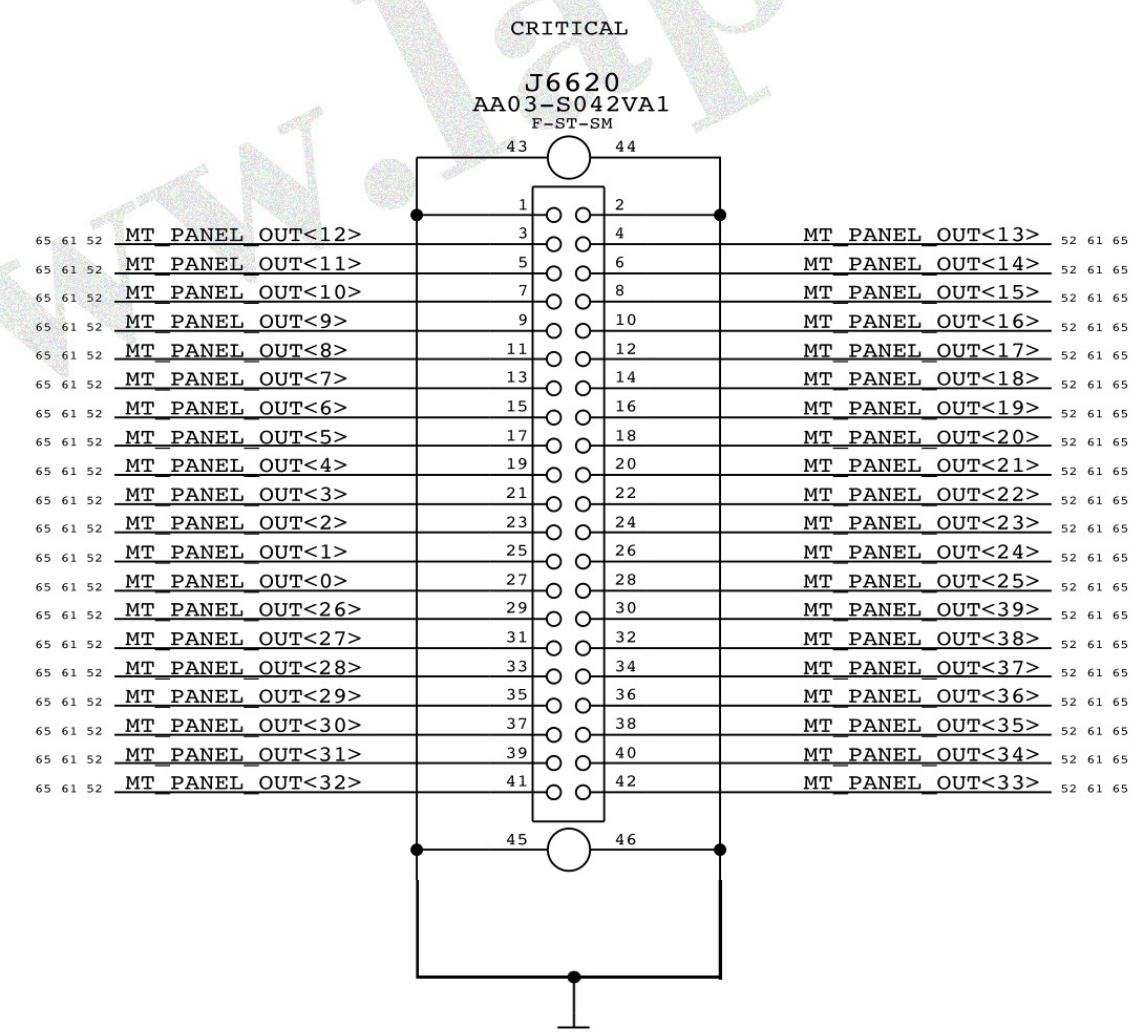
MASTER CUMULUS

SLAVE CUMULUS

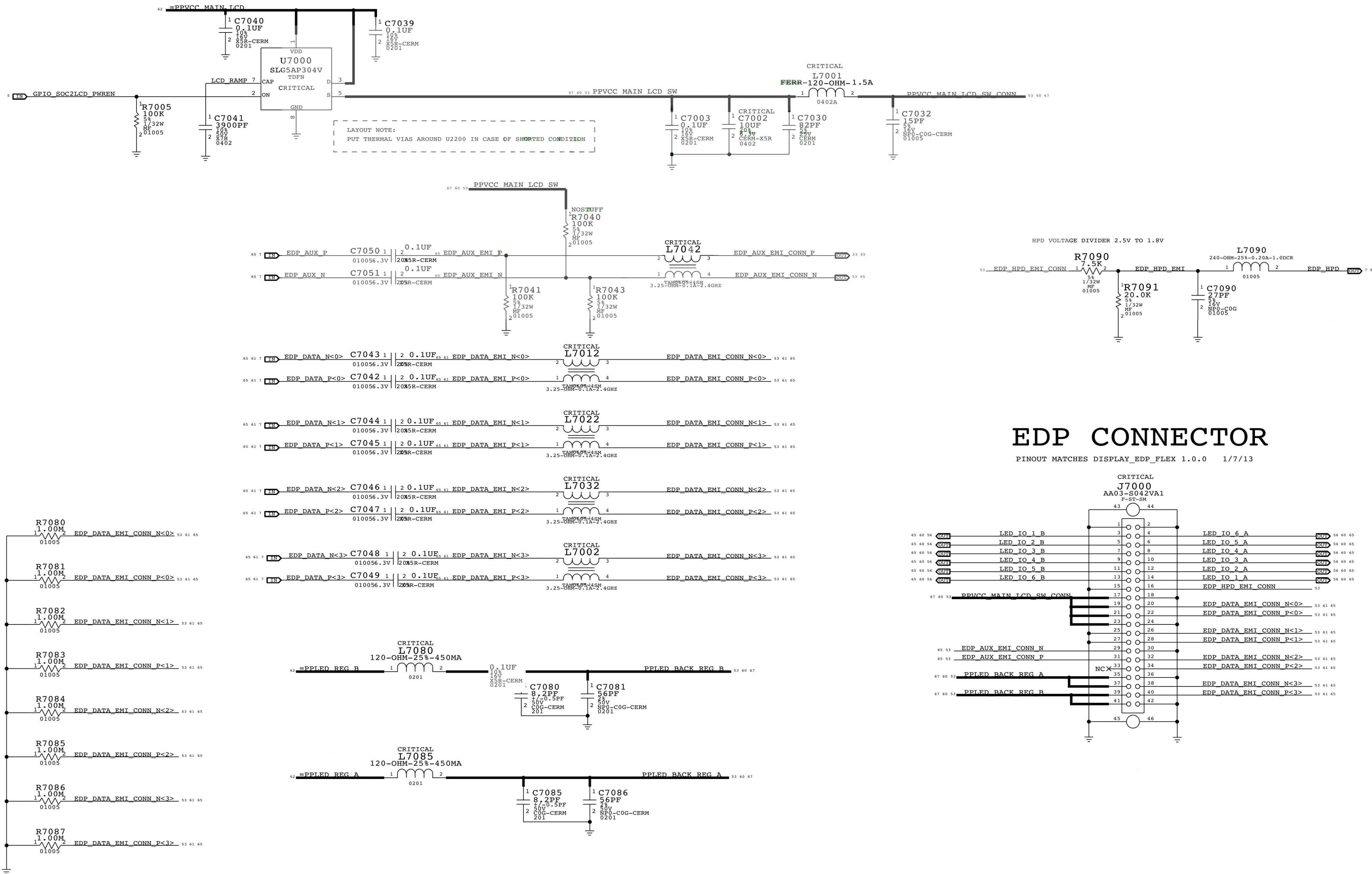


PINOUT MATCHES GRAPE_FLEX_DRIVE_ALT 0.1.0 1/8/13

PINOUT MATCHES GRAPE_FLEX_SENSE_ALT 0.1.0 1/8/13

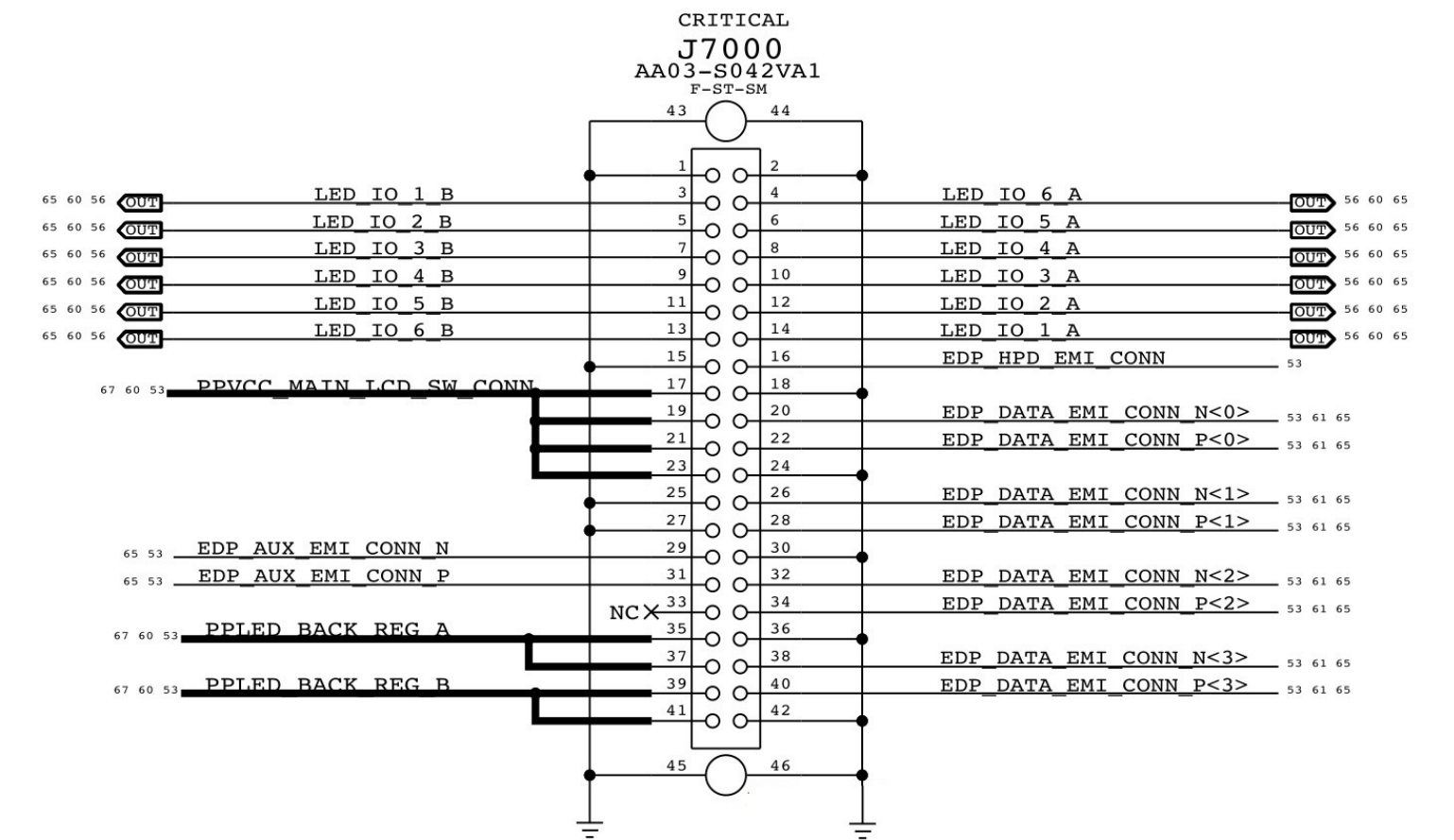


EDP CONNECTOR SUPPORT



EDP CONNECTOR

PINOUT MATCHES DISPLAY_EDP_FLEX 1.0.0 1/7/13



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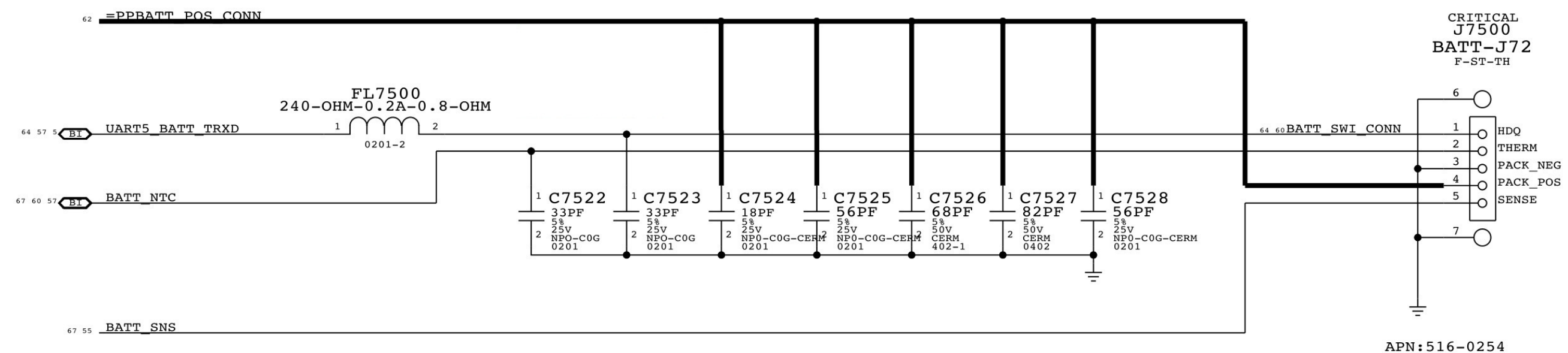
C

B

A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0823	?		RDAR://PROBLEM/11282371

FL7500,LI920



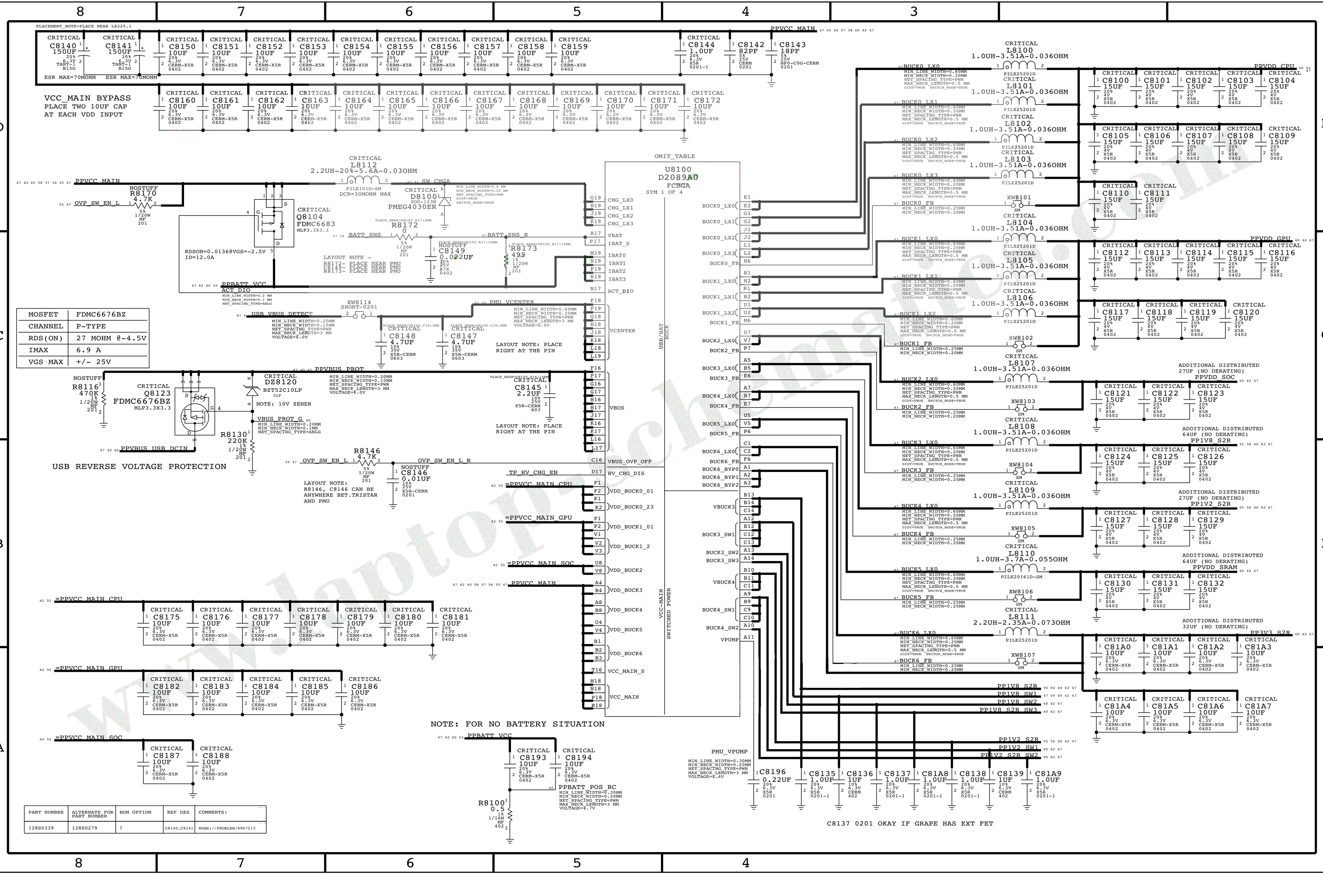
8

7

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4



MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
128S0339	128S0279	7	C8140, C8141	RDAR://PROBLEM/8967213

NOTE: FOR NO BATTERY SITUATION

C8137 0201 OKAY IF GRAPE HAS EXT FET

LDO INPUTS

OMIT_TABLE

U8100
D2089A0
FCB66
SYM 2
OP 4

LDO OUTPUTS

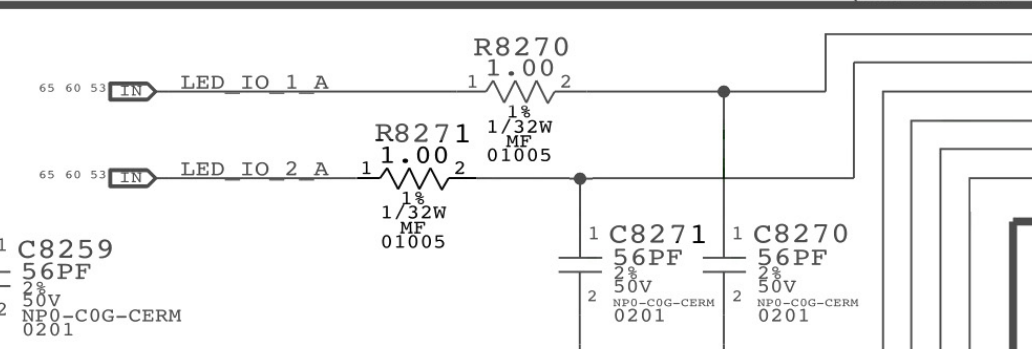
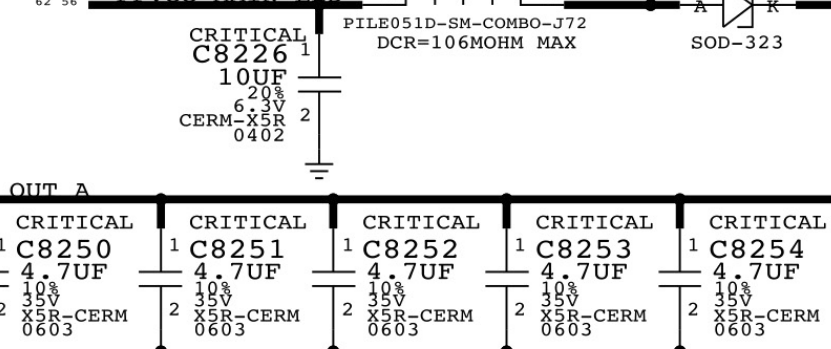
VLD01	U19 (50MA; 2.5-3.3V)	PP3V0 SPARE1	56 60 62 67
VLD02	A16 (100MA; 1.65-1.805V; BUCK3)	PP1V7 VA VCP	56 60 62 67
VLD03	U18 (50MA; 2.5-3.3V)	PP3V0 S2R SENSOR	56 60 62 67
VLD04	T19 (50MA; 2.5-3.3V)	PP3V0 ALS	56 60 62 67
VLD05	V9 (1000MA; 2.5-3.6V)	PP3V0 UVLO	56 60 62 67
VLD06	U15 (50MA; 2.5-3.6V)	PP3V3 ACC	56 60 62 67
VLD07	V14 (300MA; 1.7-3.0V)	PP3V0 S2R TRISTAR	56 60 62 67
VLD08	V15 (300MA; 1.7-3.0V)	PP3V0 S2R HALL	56 60 62 67
VLD09	A15 (300MA; 1.2-3.0V)	PP1V3 CAM	56 60 62 67
VLD010	A17 (150MA; 0.6-1.3V)	PP1V0 SOC	56 60 62 67
VLD011	V16 (300MA; 1.7-3.0V)	PP2V6 CAM AF	56 60 62 67
VLD013	U17 (300MA; 1.7-3.0V)	PP2V9 CAM	56 60 62 67
ON_BUF	T10 (5MA; 1.8V; ON_BUFF)	PP1V8 ALWAYS	56 60 62 67

CRITICAL
L8229
2.2UH-1.05A-0.195OHM
MIN LINE WIDTH=0.4MM
MIN NECK WIDTH=0.2MM
NET SPACING TYPE=PWR

CRITICAL
D8230
PMEG2005AEL
SOD882
VOLTAGE=6.0V
MIN LINE WIDTH=0.4MM
MIN NECK WIDTH=0.2MM
NET SPACING TYPE=PWR

CRITICAL
L8225
4.7UH-3.4A-0.075OHM
MIN LINE WIDTH=0.6MM
MIN NECK WIDTH=0.20MM

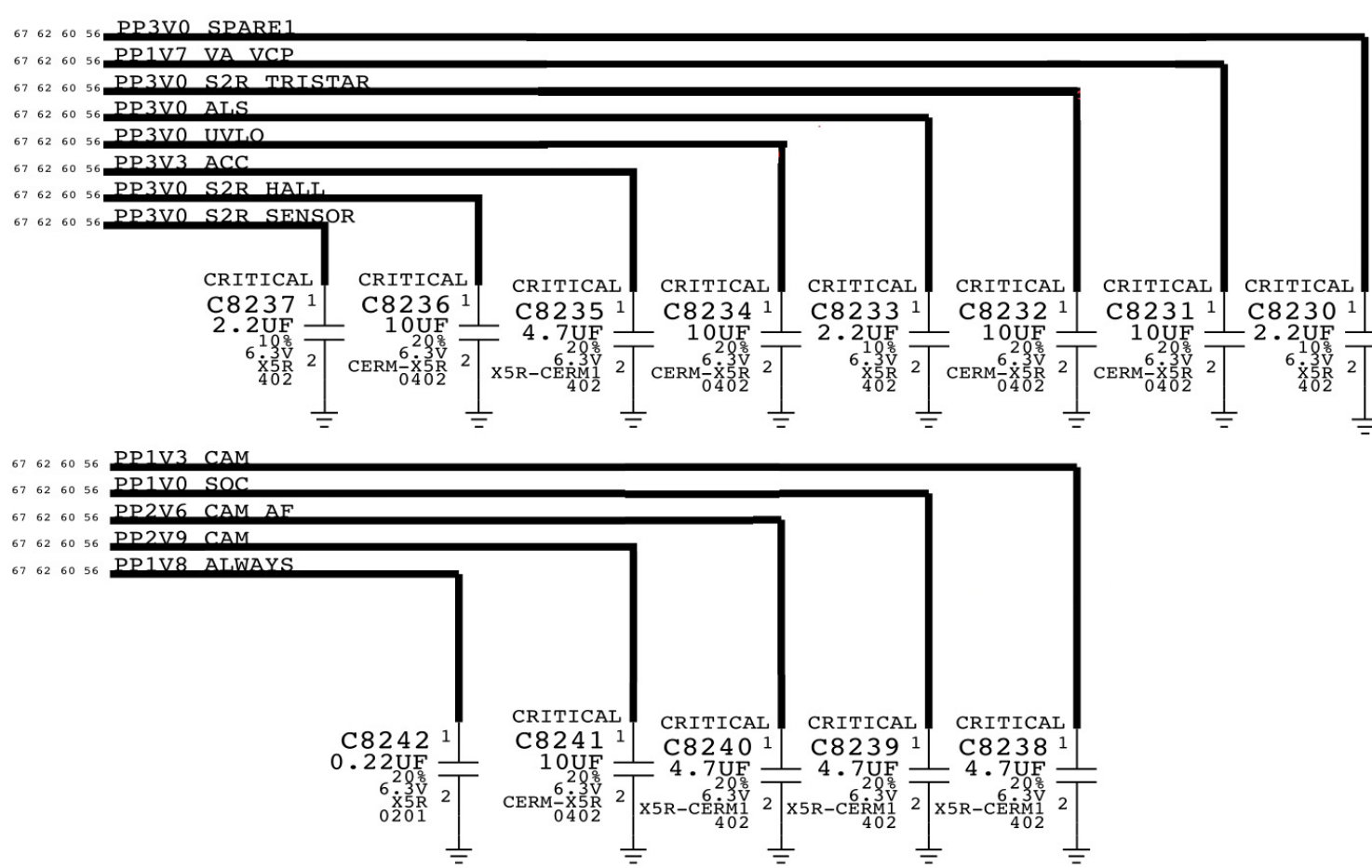
CRITICAL
D8228
PMEG4010BEA
SOD-323



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1837	152S1789	?	L8225, L8255	RDAR://PROBLEM/13487208

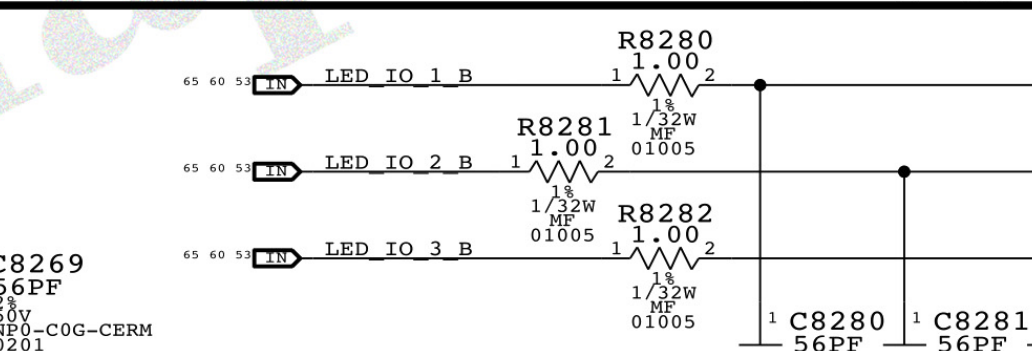
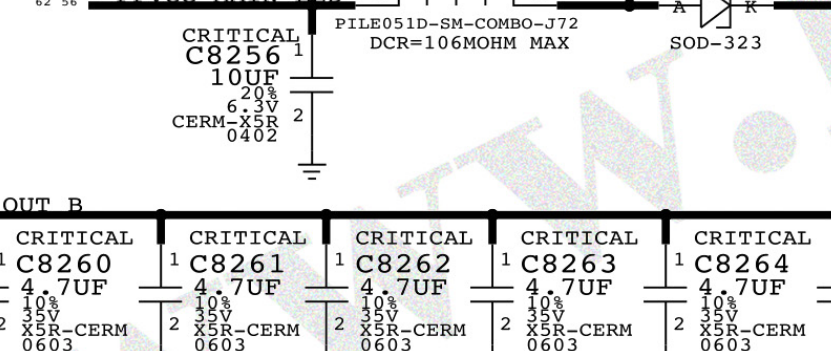
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392	?	Y8200	RDAR://PROBLEM/9936684

LDO BYPASS



CRITICAL
L8255
4.7UH-3.4A-0.075OHM
MIN LINE WIDTH=0.6MM
MIN NECK WIDTH=0.20MM

CRITICAL
D8258
PMEG4010BEA
SOD-323



D

D

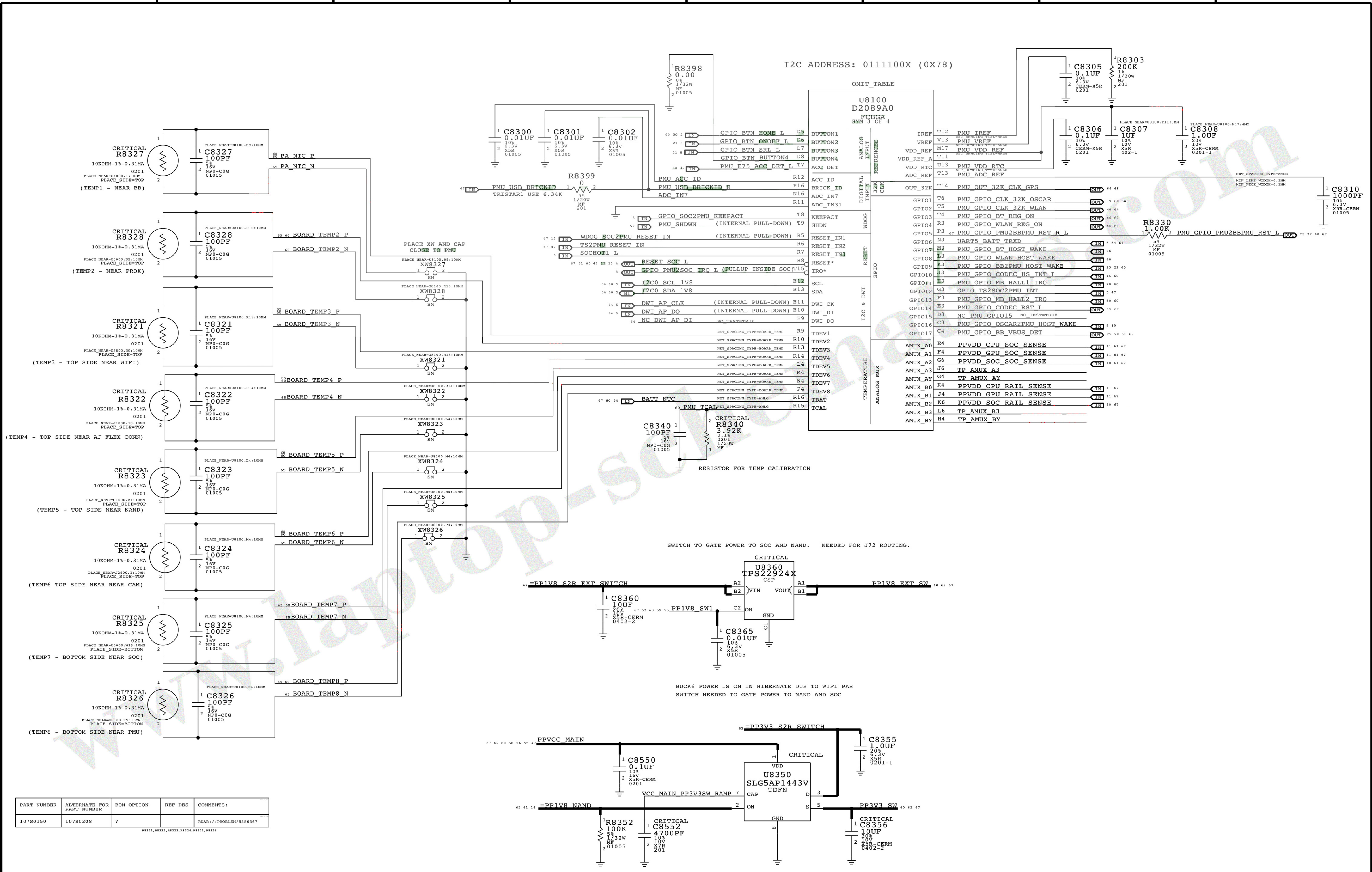
C

C

B

B

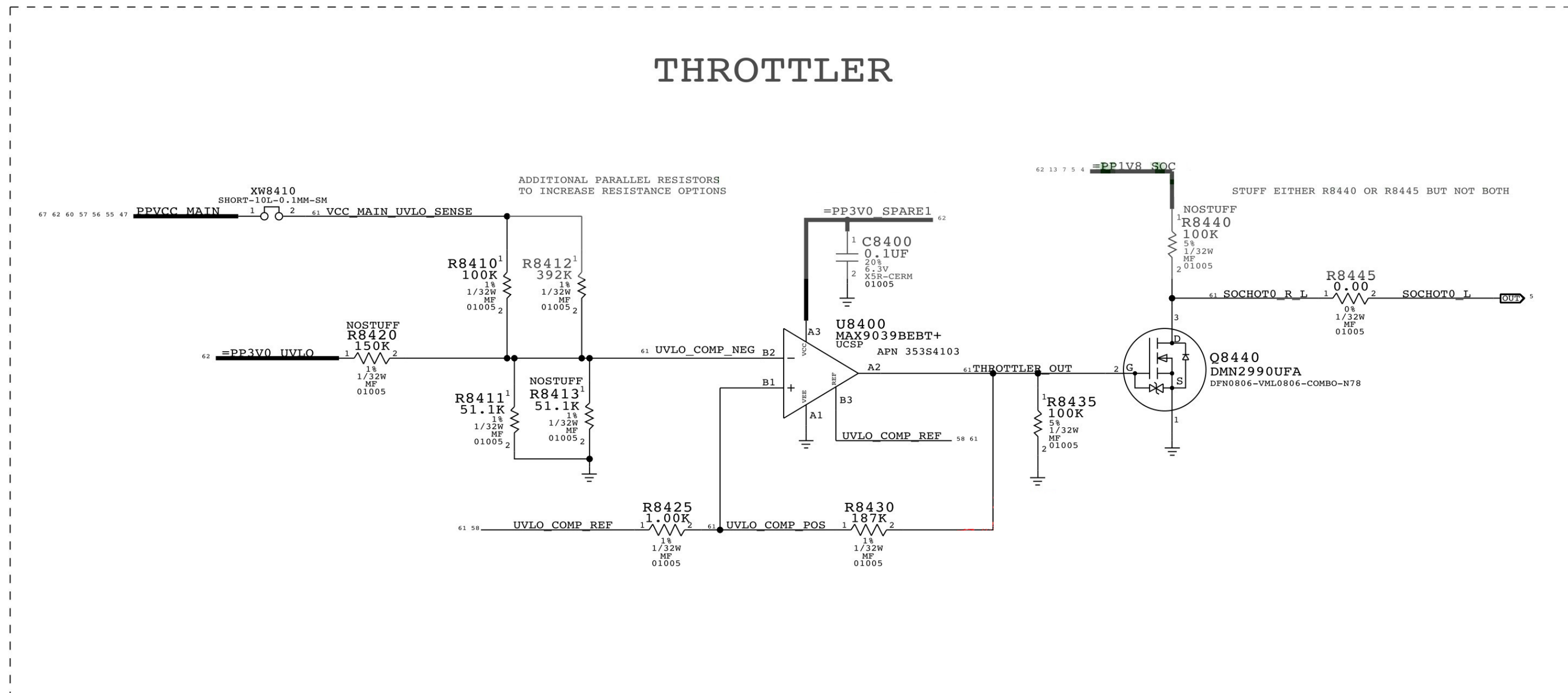
A



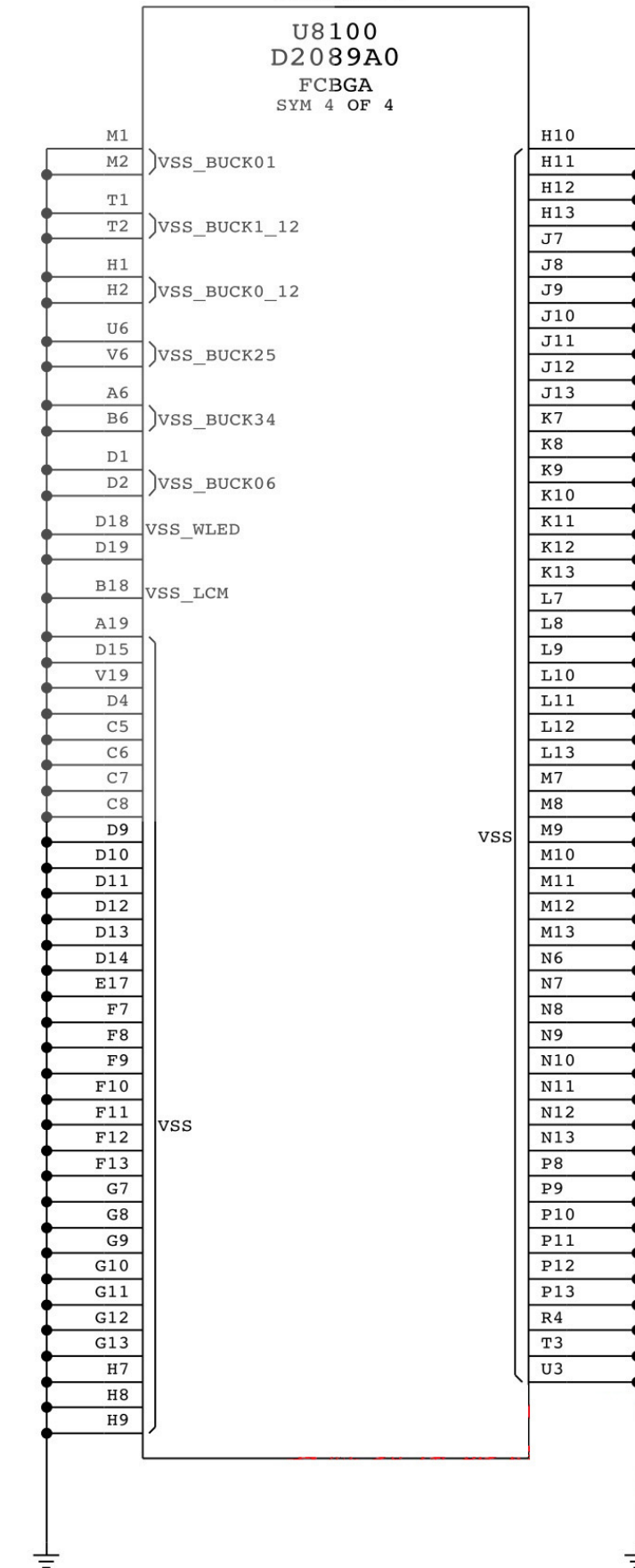
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
107S0150	107S0208	?		RDAR://PROBLEM/8380367

R8321, R8322, R8323, R8324, R8325, R8326

THROTTLER



OMIT_TABLE



ADD A VIA PER PIN FOR ALL VSS_* AND VSSA_* PINS

8

7

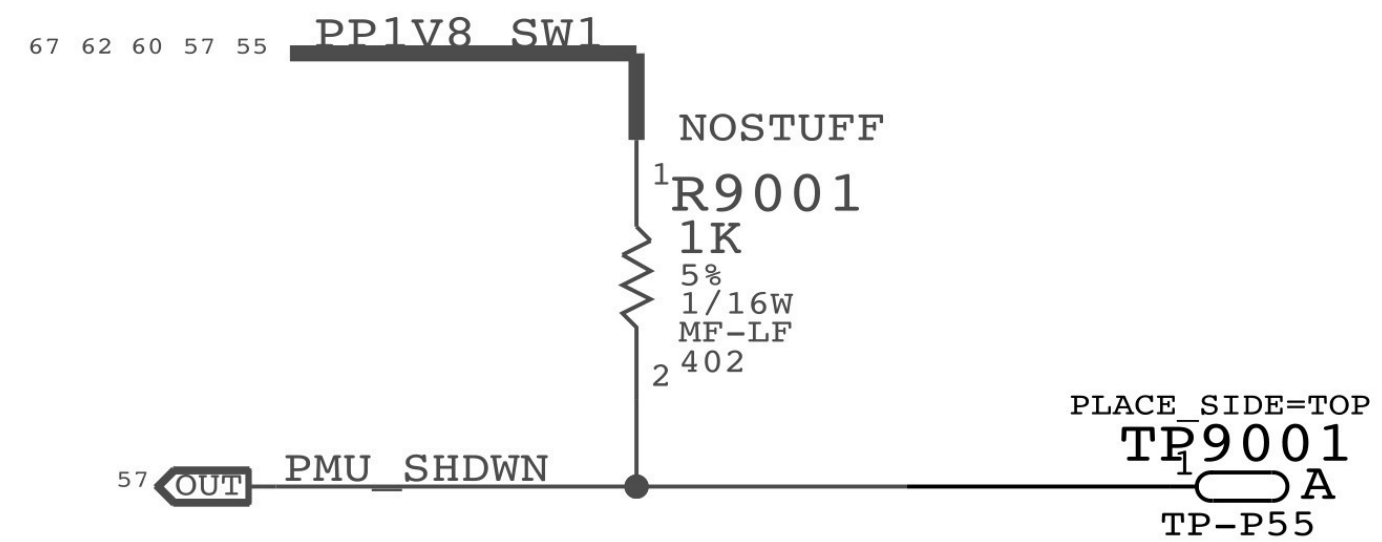
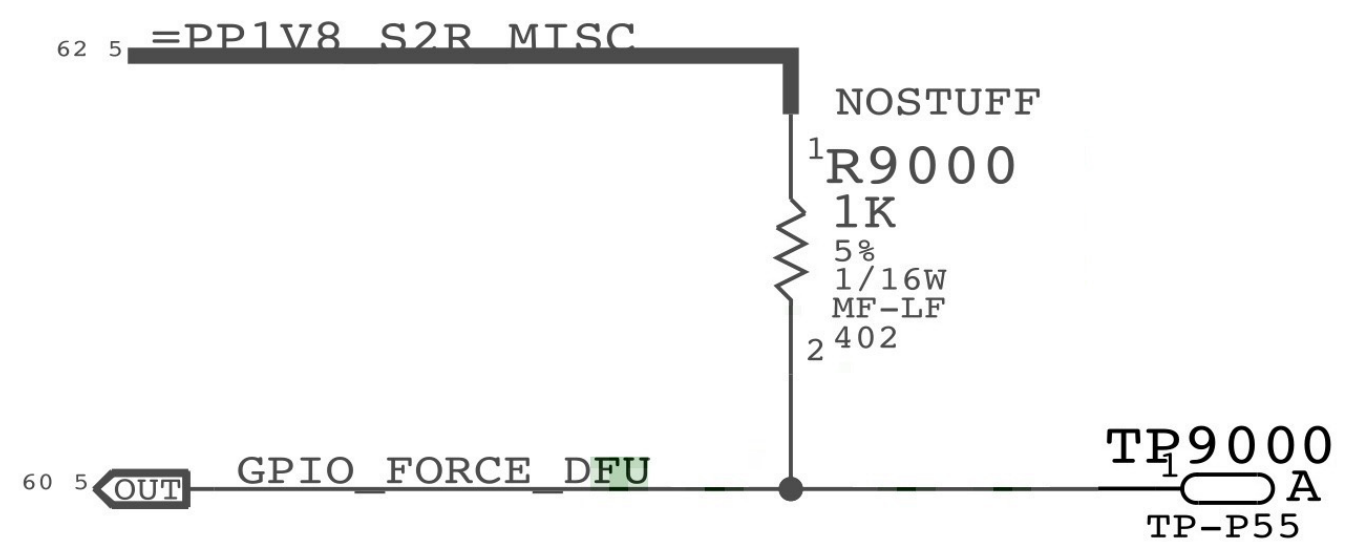
6

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3

DEBUG RESET ACCESS



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POWER

SMT TEST FIXTURE TP

Table of power test points including PPVDD CPU, PPVDD GPU, PPVDD SOC, PPIV8 S2R, PPIV8 SW1, PPIV8 SW1 FOREHEAD, PPIV8 SW2, PPIV8 SW2, PPIV8 S2R SW3, PPIV8 S2R SW3 COMP, PPIV2 S2R, PPIV2 SW1, PPIV2 S2R SW2, PPVDD SRAM, PP3V3 S2R, PP3V3 SW, PP3V0 SPARE1, PPIV7 VA VCP, PP3V0 S2R SENSOR, PP3V0 ALS, PP3V3 ACC, PP3V0 S2R TRISTAR, PP3V0 S2R HALL, PPIV3 CAM, PPIV3 CAM, PPIV0 SOC, PP2V6 CAM AF, PP2V9 CAM, PP2V5 GRAPE, PPVCC MAIN, PPBATT VCC, PPVBUS USB DCIN, PPIV8 ALWAYS, PPLED OUT A, PPLED OUT B, PP6V0 LCM VBOOST.

Table of power test points including PPBATT POS RC, PMU VCENTER, PPVBUS PROT, VBUS PROT G.

Table of power test points including PPIV2 CAM FRONT FILT, PPIV3 CAM REAR FILT, PPIV7 VCP, PPIV8 CAM FRONT FILT, PPIV8 CAM REAR FILT, PPIV8 DMIC FILT, PPIV8 GRAPE SW.

Table of power test points including PPIV8 COMP, PP2V6 CAM REAR AF FILT, PP2V9 AVDD CAM FRONT FILT, PP2V9 AVDD CAM REAR FILT, PP3V0 ALS FILT, PP3V0 HP ALS FILT, PP3V0 IO ALS FILT, PP3V0 S2R HALL FILT.

Table of power test points including PP3V0 GYRO, PP3V0 ACCEL, PP3V0 COMP, PP3V0 SENSOR PROX FILT, PP3V0 SENSOR PROX ADUX1049, PP3V0 SENSOR PROX AD7149, PP2V5 GRAPE, PPVCC MAIN LCD SW CONN, PPVCC MAIN LCD SW.

Table of power test points including PP SMPS1 MSMC 1V05, PP SMPS2 RF1 1V3, PP SMPS3 MSME 1V8, PP SMPS4 RF2 2V05, PP SMPS5 DSP 1V05.

Table of power test points including PP LDO1, PP3V0 UVLO.

Table of power test points including TP BB TEST MODE 0, TP BB TEST MODE 1.

Table of power test points including GPIO SOC2OSCAR DBGEN.

Table of power test points including TP9300 PPBATT VCC.

Table of power test points including TP9301 PPBATT VCC.

Table of power test points including TP9302 PPBATT VCC.

Table of power test points including TP9305.

Table of power test points including TP9306.

Table of power test points including TP9307.

Table of power test points including TP9310 PPVBUS E75 USB CONN.

Table of power test points including TP9311 PPVBUS E75 USB CONN.

Table of power test points including TP9312 PPVBUS E75 USB CONN.

Table of power test points including TP9315.

Table of power test points including TP9316.

Table of power test points including TP9317.

Table of power test points including TP9317.

Table of power test points including TP9317.

Table of power test points including TP9317.

Table of power test points including TP9317.

Table of power test points including TP9317.

Table of power test points including TP9317.

Table of power test points including TP9317.

Table of power test points including TP9317.

Table of GPIO test points including GPIO CAM ALS2SOC IRO L F, GPIO FORCE DPU, GPIO GRAPE2SOC IRO FILT L, GPIO SOC2BB RADIO ON L, GPIO SOC2BB RST L, GPIO SOC2GRAPE RESET FILT L, GPIO OSCAR RESET L, CLK 32K SOC2CUMULUS FILT, HP ALS IRO L CONN FILT.

Table of PMU GPIO test points including PMU GPIO BB2PMU HOST WAKE, PMU GPIO BT REG ON R, PMU GPIO CLK 32K OSCAR, PMU GPIO CLK 32K WLAN R, PMU GPIO CODEC HS INT L, PMU GPIO PMU2BBPMU RST L, PMU GPIO WLAN REG ON R, PMU TCAL, PMU E75 ACC DET L, TS E75 ACC DET L, PMU GPIO MB HALL1 IRO, PMU GPIO MB HALL2 IRO.

Table of audio test points including CONN HP HEADSET DET FILT, CONN HP HS3 FILT, CONN HP HS3 REF FILT, CONN HP HS3 FILT, CONN HP HS3 REF FILT, CONN HP HS4 FILT, CONN HP HS4 REF FILT, CONN HP LEFT FILT, CONN HP RIGHT FILT, SPRAMP L1 OUT N, SPRAMP L1 OUT P, SPRAMP R1 OUT N, SPRAMP R1 OUT P, SPRAMP L2 OUT N, SPRAMP L2 OUT P, SPRAMP R2 OUT N, SPRAMP R2 OUT P.

Table of audio test points including LEFT CH OUT P, LEFT CH OUT N, RIGHT CH OUT P, RIGHT CH OUT N, AIN3P, AIN3N, GND AUDIO CODEC, DMIC1 PF SCLK FILT, DMIC1 PF SD FILT, L81 SPEAKER VO.

Table of audio test points including LEFT CH OUT P, LEFT CH OUT N, RIGHT CH OUT P, RIGHT CH OUT N, AIN3P, AIN3N, GND AUDIO CODEC, DMIC1 PF SCLK FILT, DMIC1 PF SD FILT, L81 SPEAKER VO.

Table of GRAPE test points including GPIO GRAPE2SOC IRO L, GPIO SOC2GRAPE RESET L, CLK 32K SOC2CUMULUS, DISPLAY SYNC, SPI2 GRAPE SCLK, SPI2 GRAPE MISO, SPI2 GRAPE MOSI, SPI2 GRAPE CS L, VCC MAIN GRAPE RAMP.

Table of UART test points including UART0 SOC RXD, UART0 SOC TXD.

Table of NAND test points including FMIO_CE0 L.

Table of DISPLAY test points including DISPLAY SYNC FILT.

Table of I2C test points including I2C3 CAM ALS SCL 1V8 F, I2C3 CAM ALS SDA 1V8 F, I2C0 HP ALS SCL 1V8 FILT, I2C0 HP ALS SDA 1V8 FILT, I2C0 SCL 1V8, I2C0 SDA 1V8.

Table of SIM test points including SIMCRD_RST CONN, SIMCRD_CLK CONN, SIMCRD_IO CONN, SIM TRAY DETECT, PP LDO6 RUM 1V8.

TEST POINT RULES: CENTER TO CENTER SPACING >= 1MM, DIAMETER >= 0.5MM, EDGE TO SHIELD >= 0.55MM

BACKLIGHT

Table of backlight test points including PPLED BACK REG A, LED IO 1 A, LED IO 2 A, LED IO 3 A, LED IO 4 A, LED IO 5 A, LED IO 6 A, PPLED BACK REG B, LED IO 1 B, LED IO 2 B, LED IO 3 B, LED IO 4 B, LED IO 5 B, LED IO 6 B.

BATTERY

Table of battery test points including BATT SWI CONN, BATT NTC, E75 ACC DET CONN L, PPOUT E75 ACC ID1 CONN, PPOUT E75 ACC ID2 CONN, E75 DPAIR1 CONN P, E75 DPAIR1 CONN N, E75 DPAIR2 CONN P, E75 DPAIR2 CONN N, PPVBUS E75 USB CONN.

REEST JTAG/CONFIG

Table of reest test points including JTAG SOC SEL, JTAG SOC ACK, JTAG SOC TD1, TP JTAG SOC TDO, JTAG SOC TMS, JTAG SOC TRST L, SOC TESTMODE, RESET SOC L, PS HOLD PMIC.

BUTTONS

Table of buttons test points including GPIO BTN ONOFF L FILT, GPIO BTN HOME L, GPIO BTN VOL UP L FILT, GPIO BTN VOL DOWN L FILT, GPIO BTN SRL L FILT.

BOARD TEMP

Table of board temp test points including PA NTC P, BOARD TEMP2 P, BOARD TEMP3 P, BOARD TEMP4 P, BOARD TEMP5 P, BOARD TEMP6 P, BOARD TEMP7 P, BOARD TEMP8 P.

USB

Table of USB test points including USB SOC N, USB SOC P.

CAMERA

Table of camera test points including ISPO CAM REAR CLK F, ISPO CAM REAR SCL F, ISPO CAM REAR SDA F, ISPO CAM REAR SHUTDOWN L F, ISP1 CAM FRONT CLK F, ISP1 CAM FRONT SCL F, ISP1 CAM FRONT SDA F, ISP1 CAM FRONT SHUTDOWN L F.

NAND

Table of NAND test points including FMIO_CE0 L.

DISPLAY

Table of display test points including DISPLAY SYNC FILT.

I2C

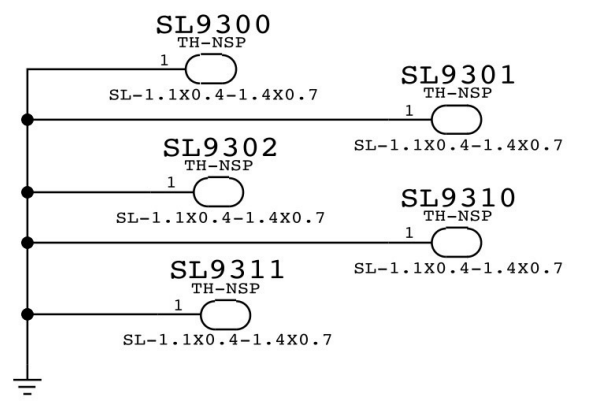
Table of I2C test points including I2C3 CAM ALS SCL 1V8 F, I2C3 CAM ALS SDA 1V8 F, I2C0 HP ALS SCL 1V8 FILT, I2C0 HP ALS SDA 1V8 FILT, I2C0 SCL 1V8, I2C0 SDA 1V8.

SIM

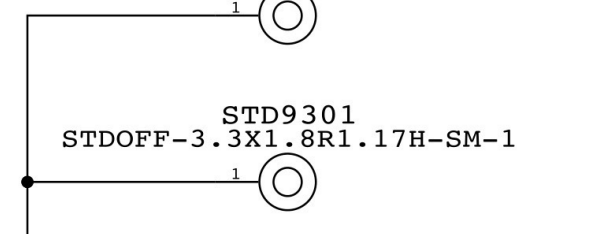
Table of SIM test points including SIMCRD_RST CONN, SIMCRD_CLK CONN, SIMCRD_IO CONN, SIM TRAY DETECT, PP LDO6 RUM 1V8.

PLATED THROUGH HOLES

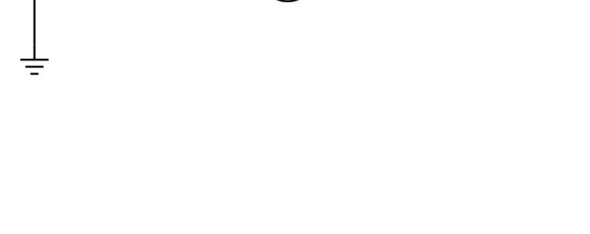
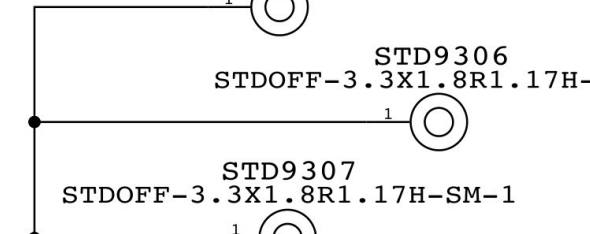
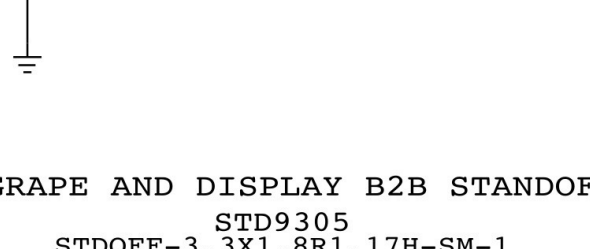
DRILL SIZE: 1.1MM X 0.4MM, PLATING SIZE: 1.4MM X 0.7MM



FOREHEAD B2B STANDOFFS



GRAPE AND DISPLAY B2B STANDOFFS



RF FIXTURE

Table of RF fixture test points including E75 DPAIR1 CONN N, E75 DPAIR1 CONN P, E75 DPAIR2 CONN N, E75 DPAIR2 CONN P, PPVBUS E75 USB CONN, PPOUT E75 ACC ID1 CONN, PPOUT E75 ACC ID2 CONN, E75 ACC DET CONN L, BATT NTC.

EE CHARACTERIZATION TP

FOR FRANK (SEG)

NAND

BOTTOM SIDE	PP9460	F4MM SH	FMIO_AD<0>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.A321:2MM	6 14 61 66
BOTTOM SIDE	PP9461	F4MM SH	FMIO_DOS	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.B34:2MM	6 14 61 66
			FMIO_AD<0..7>	EE_TEST=TRUE	FUNC_TEST=TRUE	6 14 61 66
			FMIO_CE0_L	FUNC_TEST=TRUE		6 14 61 66
			FMIO_ALE	FUNC_TEST=TRUE		6 14 66
			FMIO_CLE	FUNC_TEST=TRUE		6 14 66
			FMIO_WE_L	FUNC_TEST=TRUE		6 14 66
			FMIO_RE_L	FUNC_TEST=TRUE		6 14 66
			FMIO_DOS	FUNC_TEST=TRUE		6 14 61 66
			FM11_CE0_L	FUNC_TEST=TRUE		6 14 66
			FM11_ALE	FUNC_TEST=TRUE		6 14 66
			FM11_CLE	FUNC_TEST=TRUE		6 14 66
			FM11_WE_L	FUNC_TEST=TRUE		6 14 66
			FM11_RE_L	FUNC_TEST=TRUE		6 14 66
			FM11_DOS	FUNC_TEST=TRUE		6 14 66
			PPVREF_FMI_SOC	FUNC_TEST=TRUE		6 66
			PPVREF_FMI_NAND	FUNC_TEST=TRUE		14 66
TOP SIDE	PP9440	F4MM SH	TP_FMI_TCKC_NAND		PLACE_SIDE=TOP	14
TOP SIDE	PP9441	F4MM SH	TP_FMI_TMSC_NAND		PLACE_SIDE=TOP	14
TOP SIDE	PP9442	F4MM SH	=PP1V8_NAND		PLACE_SIDE=TOP	14 57 62
TOP SIDE	PP9443	F4MM SH	GND		PLACE_SIDE=TOP	
TOP SIDE	PP9450	F4MM SH	RESET_SOC_L	EE		4 13 25 47 57 60 67
			TP_ANALOGMUXOUT			4
TOP SIDE	PP9452	F4MM SH	SOCHOTO_R_L			58
			TP_GPIO_DFU_STATUS	FUNC_TEST=TRUE		5

CAMERA

PP9470	F4MM SH	MIPIC_CAM_FRONT_CLK_P	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.AN35:3MM	7 22 61 65
PP9471	F4MM SH	MIPIC_CAM_FRONT_CLK_N	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.AN36:3MM	7 22 61 65
PP9472	F4MM SH	MIPIC_CAM_FRONT_DATA_P<0>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.AN35:3MM	7 22 61 65
PP9473	F4MM SH	MIPIC_CAM_FRONT_DATA_N<0>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.AN36:3MM	7 22 61 65
PP9474	F4MM SH	MIPIC_CAM_REAR_CLK_P	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.AR31:3MM	7 23 61 65
PP9475	F4MM SH	MIPIC_CAM_REAR_CLK_N	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.AR31:3MM	7 23 61 65
PP9476	F4MM SH	MIPIC_CAM_REAR_DATA_P<0>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.AR33:3MM	7 23 61 65
PP9477	F4MM SH	MIPIC_CAM_REAR_DATA_N<0>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.AT33:3MM	7 23 61 65

HIGH SPEED, NO TEST

DDRO_CA<0..9>	NO_TEST=TRUE	8 12 61 66
DDRO_CK_P	NO_TEST=TRUE	8 12 61 66
DDRO_CK_N	NO_TEST=TRUE	8 12 61 66
DDRO_CA<0..9>	NO_TEST=TRUE	8 12 61 66
DDRO_CKE<0..1>	NO_TEST=TRUE	8 12 61 66
DDRO_CSN<0..1>	NO_TEST=TRUE	8 12 66
DDRO_DM<0..3>	NO_TEST=TRUE	8 12 66
DDRO_DQ<0..31>	NO_TEST=TRUE	8 12 61 66
DDRO_DQS_P<0..3>	NO_TEST=TRUE	8 12 61 66
DDRO_DQS_N<0..3>	NO_TEST=TRUE	8 12 61 66
DDR1_CA<0..9>	NO_TEST=TRUE	12 61 66
DDR1_CK_P	NO_TEST=TRUE	12 61 66
DDR1_CK_N	NO_TEST=TRUE	12 61 66
DDR1_CA<0..9>	NO_TEST=TRUE	12 61 66
DDR1_CKE<0..1>	NO_TEST=TRUE	12 61 66
DDR1_CSN<0..1>	NO_TEST=TRUE	12 61 66
DDR1_DM<0..3>	NO_TEST=TRUE	12 66
DDR1_DQ<0..31>	NO_TEST=TRUE	12 66
DDR1_DQS_P<0..3>	NO_TEST=TRUE	12 66
DDR1_DQS_N<0..3>	NO_TEST=TRUE	12 66
MIPIC_CAM_REAR_CLK_P	NO_TEST=TRUE	7 23 61 65
MIPIC_CAM_REAR_CLK_N	NO_TEST=TRUE	7 23 61 65
MIPIC_CAM_REAR_DATA_P<0..1>	NO_TEST=TRUE	7 23 61 65
MIPIC_CAM_REAR_DATA_N<0..1>	NO_TEST=TRUE	7 23 61 65
MIPIC_CAM_REAR_CLK_FILT_P	NO_TEST=TRUE	23 65
MIPIC_CAM_REAR_CLK_FILT_N	NO_TEST=TRUE	23 65
MIPIC_CAM_REAR_DATA_FILT_P<0..3>	NO_TEST=TRUE	23 65
MIPIC_CAM_REAR_DATA_FILT_N<0..3>	NO_TEST=TRUE	23 65
MIPIC_CAM_FRONT_CLK_P	NO_TEST=TRUE	7 22 61 65
MIPIC_CAM_FRONT_CLK_N	NO_TEST=TRUE	7 22 61 65
MIPIC_CAM_FRONT_DATA_P<0>	NO_TEST=TRUE	7 22 61 65
MIPIC_CAM_FRONT_DATA_N<0>	NO_TEST=TRUE	7 22 61 65
MIPIC_CAM_FRONT_CLK_FILT_P	NO_TEST=TRUE	22 65
MIPIC_CAM_FRONT_CLK_FILT_N	NO_TEST=TRUE	22 65
MIPIC_CAM_FRONT_DATA_FILT_P<0>	NO_TEST=TRUE	22 65
MIPIC_CAM_FRONT_DATA_FILT_N<0>	NO_TEST=TRUE	22 65
EDP_DATA_P<0..3>	NO_TEST=TRUE	7 53 65
EDP_DATA_N<0..3>	NO_TEST=TRUE	7 53 65
EDP_DATA_EMI_P<0..3>	NO_TEST=TRUE	53 65
EDP_DATA_EMI_N<0..3>	NO_TEST=TRUE	53 65
EDP_DATA_EMI_CONN_P<0..3>	NO_TEST=TRUE	53 65
EDP_DATA_EMI_CONN_N<0..3>	NO_TEST=TRUE	53 65

PP9400	F4MM SH	PPVDD_SOC_SOC_SENSE		PLACE_NEAR=U0600.V31:1MM	10 57 67
PP9401	F4MM SH	PPVDD_CPU_SOC_SENSE		PLACE_NEAR=U0600.AL31:1MM	11 57 67
PP9402	F4MM SH	PPVDD_GPU_SOC_SENSE		PLACE_NEAR=U0600.AA7:1MM	11 57 67

DRAM

NEAR DRAM

PP9410	F4MM SH	DDR0_CK_N	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.AE14:1MM	8 12 61 66
PP9411	F4MM SH	DDR0_CK_P	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.AE15:1MM	8 12 61 66
PP9412	F4MM SH	DDR0_CKE<0>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.AE16:1MM	8 12 61 66
PP9413	F4MM SH	DDR0_CKE<1>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.AE17:1MM	8 12 61 66
PP9414	F4MM SH	DDR0_CA<0>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.AE21:1MM	8 12 61 66
PP9415	F4MM SH	DDR0_DQ<2>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.B18:1MM	8 12 61 66
PP9416	F4MM SH	DDR0_DQS_N<3>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.C8:1MM	8 12 61 66
PP9417	F4MM SH	DDR0_DQS_P<3>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.B8:1MM	8 12 61 66
PP9418	F4MM SH	DDR0_DOS_N<0>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.C15:1MM	8 12 61 66
PP9419	F4MM SH	DDR0_DOS_P<0>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.B15:1MM	8 12 61 66
PP9420	F4MM SH	DDR1_CK_N	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.T26:1MM	8 12 61 66
PP9421	F4MM SH	DDR1_CK_P	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.R26:1MM	8 12 61 66
PP9422	F4MM SH	DDR1_CKE<0>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.P26:1MM	8 12 61 66
PP9423	F4MM SH	DDR1_CKE<1>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.N25:1MM	8 12 61 66
PP9424	F4MM SH	DDR1_CA<0>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.J25:1MM	8 12 61 66
PP9425	F4MM SH	DDR1_CA<1>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.K26:1MM	8 12 61 66
PP9426	F4MM SH	DDR1_CA<2>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.K25:1MM	8 12 61 66
PP9427	F4MM SH	DDR1_CA<3>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.L25:1MM	8 12 61 66
PP9428	F4MM SH	DDR1_CSN<0>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U1400.N35:1MM	8 12 61 66
PP9435	F4MM SH	DDR0_DQ<28>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.D5:1MM	8 12 61 66
PP9436	F4MM SH	DDR0_DOS_N<3>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.A6:1MM	8 12 61 66
PP9437	F4MM SH	DDR0_DQS_P<3>	NO_XNET_CONNECTION=TRUE	PLACE_NEAR=U0600.A5:1MM	8 12 61 66

NEAR SOC

POWER, NO TEST

PP6V0_LCM_HI	NO_TEST=TRUE	56 67
SW_CHGA	NO_TEST=TRUE	56 67
WLED_LX_A	NO_TEST=TRUE	56 67
WLED_LX_B	NO_TEST=TRUE	56 67
L81_PVCP	NO_TEST=TRUE	15 65
L81_NVCP	NO_TEST=TRUE	15 65
CHARGE_PUMP_OUTPUTS	NO_TEST=TRUE	15 65
L81_FLYC	NO_TEST=TRUE	15 65
L81_FLYN	NO_TEST=TRUE	15 65
L81_FLYP	NO_TEST=TRUE	15 65
THROTTLE_OUT	NO_TEST=TRUE	58
UVLO_COMP_NEG	NO_TEST=TRUE	58
UVLO_COMP_POS	NO_TEST=TRUE	58
UVLO_COMP_REF	NO_TEST=TRUE	58
VCC_MAIN_UVLO_SENSE	NO_TEST=TRUE	58

GRAPE

CONVERT TO PROBE POINTS IF NOT ABLE TO PLACE TESTPOINT

TP_JTAG_CUMULUS_M_TCK	52 64
TP_JTAG_CUMULUS_M_TDI	52 64
JTAG_CUMULUS_M_TMS	52 64
TP_JTAG_CUMULUS_M_TDO	52 64
DISPLAY_SYNC	52 64 60
CUMULUS_MS_CK	52 64
CUMULUS_MS_SD	52 64
GPIO_GRAPE2SOC_IRO_L	5 52 60
GPIO_SOC2GRAPE_RESET_L	5 52 60 67
CLK_32K_SOC2CUMULUS	5 52 60 64
SPI2_GRAPE_MOSI	5 52 60 64
SPI2_GRAPE_MISO	5 52 60 64
SPI2_GRAPE_SCLK	5 52 60 67
SPI2_GRAPE_CS_L	5 52 60 64
TP_CUMULUS_S_H_CS_L	52
TP_CUMULUS_S_H_SCLK	52
TP_CUMULUS_S_H_SDI	52
TP_CUMULUS_S_H_SDO	52
=PP5V25_GRAPE	52 62
PP1V8_GRAPE_SW	51 52 60 67

AUDIO

L81_DMIC1_FF_SD	FUNC_TEST=TRUE	15
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NO TEST DUE TO LAYOUT

I2C3 TP AT ALS FILTER SIDE

I2C3_SCL_IV8	NO_TEST=TRUE	5 13 22 64
I2C3_SDA_IV8	NO_TEST=TRUE	5 13 22 64
MAX98304_L1_IN_N	NO_TEST=TRUE	18 65
MAX98304_L1_IN_P	NO_TEST=TRUE	18 65
MAX98304_R1_IN_N	NO_TEST=TRUE	17 65
MAX98304_R1_IN_P	NO_TEST=TRUE	17 65
MAX98304_L2_IN_N	NO_TEST=TRUE	18 65
MAX98304_L2_IN_P	NO_TEST=TRUE	18 65
MAX98304_R2_IN_N	NO_TEST=TRUE	17 65
MAX98304_R2_IN_P	NO_TEST=TRUE	17 65
GPIO_BTN_HOME_CONN_R_L	NO_TEST=TRUE	50

NO TEST ON PROX

PROX_AD7149_CIN5	NO_TEST=TRUE	45
PROX_AD7149_CIN7	NO_TEST=TRUE	45
PROX_AD7149_CIN9	NO_TEST=TRUE	45
PROX_AD7149_CIN7_FILT	NO_TEST=TRUE	45
PROX_AD7149_CIN9_FILT	NO_TEST=TRUE	45
PROX_AD7149_CIN7_CONN	NO_TEST=TRUE	45
PROX_AD7149_CIN9_CONN	NO_TEST=TRUE	45
PROX_AD7149_ACSHIELD_CONN	NO_TEST=TRUE	45
PROX_AD7149_BIAS	NO_TEST=TRUE	45
ACSHIELD_SB	NO_TEST=TRUE	45
ACSH_SB	NO_TEST=TRUE	45
PROX_AD7149_GPIO	NO_TEST=TRUE	45

WIFI

JTAG_WLAN_TMS_TX_BLANK	FUNC_TEST=TRUE	46 64
TP_JTAG_WLAN_TCK	FUNC_TEST=TRUE	46 64
JTAG_WLAN_TDI_OSCAR_A	FUNC_TEST=TRUE	46 64
JTAG_WLAN_TDO_OSCAR_B	FUNC_TEST=TRUE	46 64
TP_JTAG_WLAN_TRST_L	FUNC_TEST=TRUE	46 64
JTAG_WLAN_SEL	FUNC_TEST=TRUE	46
UART2_SOC2WLAN_TX_R	FUNC_TEST=TRUE	46 64
UART2_WLAN2SOC_TX_R	FUNC_TEST=TRUE	46
UART_BB2WLAN_LTE_COEX_R	FUNC_TEST=TRUE	46 64
UART_WLAN2BB_LTE_COEX_R	FUNC_TEST=TRUE	46
=PP3V3_S2R_WIFI_PA	FUNC_TEST=TRUE	46 62

HSIC1_SOC2WLAN_HOST_RDY_R	FUNC_TEST=TRUE	46 64
HSIC1_WLAN2SOC_DEVICE_RDY	FUNC_TEST=TRUE	5 46 64
HSIC1_WLAN2SOC_REMOTE_WAKE	FUNC_TEST=TRUE	5 46 64

FOR HSIC CHARACTERIZATION

PP9480	F4MM SH	HSIC1_WLAN_DATA	PLACE_NEAR=U0600.A27:3MM	4 46 61 64
PP9481	F4MM SH	HSIC1_WLAN_STB	PLACE_NEAR=U0600.B27:3MM	4 46 61 64
PP9482	F4MM SH	HSIC1_WLAN_DATA	PLACE_NEAR=U5800.13:3MM	4 46 61 64
PP9483	F4MM SH	HSIC1_WLAN_STB	PLACE_NEAR=U5800.14:3MM	4 46 61 64

PMU_GPIO_WLAN_REG_ON	FUNC_TEST=TRUE	46 57
PMU_GPIO_BT_REG_ON	FUNC_TEST=TRUE	46 57
GPIO_BT_WAKE	FUNC_TEST=TRUE	5 46

BASEBAND

BB_JTAG_TMS	FUNC_TEST=TRUE	5 25 28 64
BB_JTAG_TCK	FUNC_TEST=TRUE	5 25 28 64
BB_JTAG_TDI	FUNC_TEST=TRUE	5 25 28 64
BB_JTAG_TDO	FUNC_TEST=TRUE	5 25 28 64
BB_JTAG_TRST_L	FUNC_TEST=TRUE	5 25 28 64
USB_BB_DEBUG_P	FUNC_TEST=TRUE	25 28 64
USB_BB_DEBUG_N	FUNC_TEST=TRUE	25 28 64
DEBUG_RST_L	FUNC_TEST=TRUE	25 28 67
PMU_GPIO_BB_VBUS_DET	FUNC_TEST=TRUE	25 28 57 67

FOR HSIC CHARACTERIZATION

PP9485	F4MM SH	HSIC2_BB_DATA	PLACE_NEAR=U0600.AJ35:3MM	4 25 28 61 64
PP9486	F4MM SH	HSIC2_BB_STB	PLACE_NEAR=U0600.AJ36:3MM	4 25 28 61 64
PP9487	F4MM SH	HSIC2_BB_DATA	PLACE_NEAR=U3400.C7:3MM	4 25 28 61 64
PP9488	F4MM SH	HSIC2_BB_STB	PLACE_NEAR=U3400.B8:3MM	4 25 28 61 64

POWER CONNECTIONS

BUCK0

67 60 55 PPVDD_CPU == =PPVDD_CPU 11
MAKE_BASE=TRUE

BUCK1

67 60 55 PPVDD_GPU == =PPVDD_GPU 13
MAKE_BASE=TRUE

BUCK2

67 60 55 PPVDD_SOC == =PPVDD_SOC 10
MAKE_BASE=TRUE

BUCK3

67 60 56 55 PP1V8_S2R == =PP1V8_S2R_MISC 5 59
MAKE_BASE=TRUE
== =PP1V8_S2R_VDDIO_WLAN_BT 46
== =PP1V8_S2R_TRISTAR 47
== =PP1V8_S2R_DDR 12
== =PP1V8_S2R_GRAPE 51
== =PP1V8_S2R_EXT_SWITCH 57

BUCK3_SW

67 60 59 57 55 PP1V8_SW1 == =PP1V8_AUDIO 15
MAKE_BASE=TRUE
XWC130
SM
1 2 PP1V8_SW1_FOREHEAD 40 42 47
67 62 60 PP1V8_SW1_FOREHEAD == =PP1V8_DMIC 16
== =PP1V8_CAM_FRONT 22
== =PP1V8_CAM_REAR 23
== =PP1V8_PROX_AD7149 45

PP1V8_EXT_SW

67 60 57 PP1V8_EXT_SW == =PP1V8_VDDIO18_SOC 9 10
MAKE_BASE=TRUE
== =PP1V8_SOC 4 5 7 13 58
== =PP1V8_MIPI_SOC 7
== =PP1V8_EDP_SOC 7
== =PP1V8_NAND_SOC 6
== =PP1V8_NAND 14 57 61
== =PP1V8_PLL_SOC 4
== =PP1V8_EEPROM 5

PP1V8_SW2

67 60 55 PP1V8_SW2 == =PP1V8_GRAPE 51
MAKE_BASE=TRUE
67 60 55 PP1V8_S2R_SW3 == =PP1V8_S2R_GYRO 19
MAKE_BASE=TRUE
== =PP1V8_S2R_ACCEL 19
== =PP1V8_S2R_OSCAR 19
XWC133
SM
1 2 PP1V8_S2R_SW3_COMP 60 62 67
67 62 60 PP1V8_S2R_SW3_COMP == =PP1V8_S2R_COMP 24
MAKE_BASE=TRUE

BUCK4

67 60 56 55 PP1V2_S2R == =PP1V2_S2R_DDR 12
MAKE_BASE=TRUE
== =PP1V2_S2R_DDR_SOC 8

BUCK4_SW

67 60 55 PP1V2_SW1 == =PP1V2_VDDO_DDR 12
MAKE_BASE=TRUE
== =PP1V2_VDDIOD_SOC 8 9
== =PP1V2_HSIC_SOC 4
67 60 55 PP1V2_S2R_SW2 == =PP1V2_S2R_OSCAR 19
MAKE_BASE=TRUE

BUCK5

67 60 55 PPVDD_SRAM == =PPVDD_SRAM_CPU 10
MAKE_BASE=TRUE
== =PPVDD_SRAM_SOC 10

BUCK6

67 60 55 PP3V3_S2R == =PP3V3_S2R_SWITCH 57
MAKE_BASE=TRUE
== =PP3V3_S2R_WIFI_PA 46 61

PP3V3_SW

67 60 57 PP3V3_SW == =PP3V3_EDP_PU 14
MAKE_BASE=TRUE
== =PP3V3_NAND 14
== =PP3V3_USB_SOC 4

LDO1

67 60 56 PP3V0_SPARE1 == =PP3V0_SPARE1 58
MAKE_BASE=TRUE

LDO2

67 60 56 PP1V7_VA_VCP == =PP1V7_VA_VCP 15
MAKE_BASE=TRUE

LDO3

67 60 56 PP3V0_S2R_SENSOR == =PP3V0_S2R_GYRO 19
MAKE_BASE=TRUE
== =PP3V0_S2R_ACCEL 19
== =PP3V0_S2R_COMP 24

LDO4

67 60 56 PP3V0_ALS == =PP3V0_ALS 22
MAKE_BASE=TRUE
== =PP3V0_PROX_AD7149 45

LDO5

67 60 56 PP3V0_UVLO == =PP3V0_UVLO 58
MAKE_BASE=TRUE

LDO6

67 60 56 PP3V3_ACC == =PP3V3_ACC 47
MAKE_BASE=TRUE

LDO7

67 60 56 PP3V0_S2R_TRISTAR == =PP3V0_S2R_TRISTAR 47
MAKE_BASE=TRUE

LDO8

67 60 56 PP3V0_S2R_HALL == =PP3V0_S2R_HALL 50
MAKE_BASE=TRUE

LDO9

67 60 56 PP1V3_CAM == =PP1V3_CAM_REAR 23
MAKE_BASE=TRUE
BACKUP RAIL. CAN BE BOOSTED TO MEET
1.1V MIN ON CAMERA IF NEEDED.

LDO10

67 60 56 PP1V0_SOC == =PP1V0_USB_SOC 4
MAKE_BASE=TRUE
== =PP1V0_MIPI_SOC 7
== =PP1V0_EDP_PAD_DVDD_SOC 7

LDO11

67 60 56 PP2V6_CAM_AF == =PP2V6_CAM_REAR_AF 23
MAKE_BASE=TRUE

LDO13

67 60 56 PP2V9_CAM == =PP2V9_CAM_FRONT 22
MAKE_BASE=TRUE
== =PP2V9_CAM_REAR 23

VLCM1

67 60 56 PP5V25_GRAPE == =PP5V25_GRAPE 52 61
MAKE_BASE=TRUE

CHARGER MAIN

67 60 58 57 56 55 47 PPVCC_MAIN == =PPVCC_MAIN_AUDIO 15
MAKE_BASE=TRUE
== =PPVCC_MAIN_LED 56
== =PPVCC_MAIN_CPU 55
== =PPVCC_MAIN_GPU 55
== =PPVCC_MAIN_SOC 55
== =PPVCC_MAIN_GRAPE 51
== =PPVCC_MAIN_LCD 53
== =PPVCC_MAIN_VDD_LCM 56
== =PPVCC_MAIN_WLAN 46

BATTERY

67 60 55 PPBATT_VCC == =PPBATT_POS_CONN 54
MAKE_BASE=TRUE
== =PPBATT_VCC_BB 25 26 34 35 36 37 38 39 40
== =PPBATT_AUDIO 17 18

USB POWER INPUT

67 60 55 PPVBUS_USB_DCIN == =PPVBUS_USB_EMI 48
MAKE_BASE=TRUE

ON_BUF

67 60 56 PP1V8_ALWAYS == =PP1V8_ALWAYS 5
MAKE_BASE=TRUE

BACKLIGHT BOOST

67 60 56 PPLED_OUT_A == =PPLED_REG_A 53
MAKE_BASE=TRUE

67 60 56 PPLED_OUT_B == =PPLED_REG_B 53
MAKE_BASE=TRUE

8

7

6

5

4

3

2

1

MLB CONSTRAINTS

Table with columns: BOARD LAYERS, BOARD AREAS, BOARD UNITS (MIL OR MM), ALLEGRO VERSION. Rows: TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, BOTTOM; NO_TYPE, BGA; MM; 16.5

PHYSICAL CONSTRAINTS

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows: DEFAULT TOP,BOTTOM; DEFAULT ISL2-9

45 OHM SINGLE-ENDED PHYSICAL RULES

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows: 45_OHM_SE TOP,BOTTOM; 45_OHM_SE ISL5; 45_OHM_SE ISL7; 45_OHM_SE ISL9; 45_OHM_SE *

90 OHM DIFFERENTIAL PAIR PHYSICAL RULES

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows: 90_OHM_DIFF TOP,BOTTOM; 90_OHM_DIFF ISL5; 90_OHM_DIFF ISL7; 90_OHM_DIFF ISL9; 90_OHM_DIFF *

50 OHM RF SINGLE-ENDED PHYSICAL RULES

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows: 50_OHM_RF TOP; 50_OHM_RF ISL3; 50_OHM_RF ISL4; 50_OHM_RF ISL7; 50_OHM_RF BOTTOM; 50_OHM_RF *

100 OHM RF DIFFERENTIAL PAIR PHYSICAL RULES

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows: 100_OHM_RF TOP; 100_OHM_RF ISL4; 100_OHM_RF ISL7; 100_OHM_RF *

DRAM SINGLE-ENDED PHYSICAL RULES

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows: DRAM_SE ISL5, ISL7, ISL9; DRAM_SE *

DRAM DIFFERENTIAL PAIR PHYSICAL RULES

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows: DRAM_DIFF ISL5, ISL7, ISL9; DRAM_DIFF *

GRAPE PHYSICAL CONSTRAINTS

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows: GRAPE_SE TOP,BOTTOM; GRAPE_SE ISL2-9

TCF VERSION (USING SPACING RULE)

Table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows: TCF_VERSION * 0.020 MM ? 0.020 - 12/17/2012

TCF_VERSION NC_USB_ID ASSIGNING RULE TO NC NET

SPACING CONSTRAINTS

DEFAULT SPACING RULES

Table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows: DEFAULT * 0.08 MM ?

REGULAR SPACING RULES

Table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows: 1.2:1_SPACING, 1.5:1_SPACING, 2:1_SPACING, 2.4:1_SPACING, 3:1_SPACING, 4:1_SPACING, 5:1_SPACING

POWER/GND SPACING RULES

Table with columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows: GND, PWR

Table with columns: NET_PHYSICAL_TYPE, AREA_TYPE, PHYSICAL_RULE_SET. Rows: GND, PP_PWR

POWER

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows: GND, PWR_OP1MM, PWR_OP2MM, PWR_OP25MM, PWR_OP3MM, PWR_OP4MM, PWR_OP5MM, PWR_PMU, PWR_OP75MM, PWR_1MM, PWR_1P2MM, PWR_2MM, PWR_10MM, PWR_15MM, PWR_RF

MISC PHYSICAL RULES

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows: SPEAKER, AUDIO_DIFF, LED, TEMP_SENSE, PWR_SENSE, RF_DIFF

MISC

Table with columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows: CLK, ANLG

MAX_LINE_WIDTH=1 MM GND GND GND

NOTES:

- 0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

(NOTE: TOP LAYER REF L3, CLEAR L2, NECK REF ADJACENT)
(NOTE: L3 LAYER REF L1 AND L4, CLEAR L2)
(NOTE: L4 LAYER REF L2 AND L5, CLEAR L3, NECK REF ADJACENT)
(NOTE: L7 LAYER REF L5 AND L8, CLEAR L6, NECK REF ADJACENT)
(NOTE: BOT LAYER REF L8, CLEAR L9, NECK REF ADJACENT)

(NOTE: REF ADJACENT)
(NOTE: L4 LAYER REF L3 AND L6, CLEAR L5, NECK REF ADJACENT)
(NOTE: L7 LAYER REF L5 AND L8, CLEAR L6, NECK REF ADJACENT)

(NOTE: L5 46 OHMS. L7 48 OHMS, L9 45 OHMS)

(NOTE: L5 89 OHMS. L7 91 OHMS, L9 86 OHMS)

Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_50S	*	45_OHM_SE	CLK	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
U000	CLK_50S	CLK	CLK 32K SOC2CUMULUS	5 52 60 61
U001	CLK_50S	CLK	CLK 32K SOC2CUMULUS FILT	60
U002	CLK_50S	CLK	CUMULUS MS CK	52 61
U003	CLK_50S	CLK	CUMULUS MS SD	52 61
U004	CLK_50S	CLK	PMU GPIO CLK 32K WLAN	46 57
U005	CLK_50S	CLK	PMU GPIO CLK 32K OSCAR	19 57 60
U006	CLK_50S	CLK	PMU_OUT_32K_CLK_GPS	57 68
U007	CLK_50S	CLK	ISP1_CAM_FRONT_CLK_R	7
U008	CLK_50S	CLK	ISP1_CAM_FRONT_CLK	7 22
U009	CLK_50S	CLK	ISP1_CAM_FRONT_CLK_F	7 22 60
U010	CLK_50S	CLK	ISP0_CAM_REAR_CLK_R	7
U011	CLK_50S	CLK	ISP0_CAM_REAR_CLK	7 23
U012	CLK_50S	CLK	ISP0_CAM_REAR_CLK_F	23 60

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART_50S	*	45_OHM_SE	UART	*	*	3:1_SPACING
			UART	UART	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
U013	UART_50S	UART	UART0 SOC RXD	5 47 60
U014	UART_50S	UART	UART0 SOC TXD	5 47 60
U015	UART_50S	UART	UART3 SOC2BB RTS L	5 25 29
U016	UART_50S	UART	UART3 BB2SOC RTS L	5 25 29
U017	UART_50S	UART	UART3 SOC2BB TX	5 25 29 47
U018	UART_50S	UART	UART3 BB2SOC TX	5 25 29 47
U019	UART_50S	UART	UART4 OSCAR2SOC_RXD	5 19
U020	UART_50S	UART	UART4 SOC2OSCAR_TXD	5 19
U021	UART_50S	UART	UART1 SOC2BT RTS L	5 46
U022	UART_50S	UART	UART1 BT2SOC RTS L	5 46
U023	UART_50S	UART	UART1 SOC2BT TX	5 46
U024	UART_50S	UART	UART1 BT2SOC TX	5 46
U025	UART_50S	UART	UART2 SOC2WLAN_TX	5 46
U026	UART_50S	UART	UART2 WLAN2SOC_TX	5 46
U027	UART_50S	UART	UART2 SOC2WLAN_TX_R	46 61
U028	UART_50S	UART	UART2 WLAN2SOC_TX_R	46 61
U029	UART_50S	UART	UART6 TS_ACC_RXD	5 47
U030	UART_50S	UART	UART6 TS_ACC_TXD	5 47
U031	UART_50S	UART	UART5 BATT_TRXD	5 54 57
U032		UART	BATT_SWI_CONN	54 60

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S_50S	*	45_OHM_SE	I2S	*	*	3:1_SPACING
			I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
U033	I2S_50S	CLK	I2S0 CODEC ASP_MCK_R	5 15
U034	I2S_50S	CLK	I2S0 CODEC ASP_MCK	5
U035	I2S_50S	I2S	I2S0 CODEC ASP_BCLK	5 15
U036	I2S_50S	I2S	I2S0 CODEC ASP_LRCK	5 15
U037	I2S_50S	I2S	I2S0 CODEC ASP_DIN	5 15
U038	I2S_50S	I2S	I2S0 CODEC ASP_DOUT	5 15
U039	I2S_50S	I2S	I2S0 CODEC ASP_SDOUT	15
U040	I2S_50S	I2S	NC_I2S1_MCK	5
U041	I2S_50S	I2S	I2S1 CODEC_XSP_BCLK	5 15
U042	I2S_50S	I2S	I2S1 CODEC_XSP_LRCK	5 15
U043	I2S_50S	I2S	I2S1 CODEC_XSP_DIN	5 15
U044	I2S_50S	I2S	I2S1 CODEC_XSP_DOUT	5 15
U045	I2S_50S	I2S	I2S1 CODEC_XSP_SDOUT	15
U046	I2S_50S	CLK	NC_I2S2_MCK_R	5
U047	I2S_50S	CLK	NC_I2S2_MCK	5
U048	I2S_50S	I2S	NC_I2S2_BCLK	5
U049	I2S_50S	I2S	NC_I2S2_LRCK	5
U050	I2S_50S	I2S	NC_I2S2_DIN	5
U051	I2S_50S	I2S	NC_I2S2_DOUT	5
U052	I2S_50S	I2S	NC_I2S4_MCK	5
U053	I2S_50S	I2S	I2S4 SOC2BT_BCLK	5 46
U054	I2S_50S	I2S	I2S4 SOC2BT_LRCK	5 46
U055	I2S_50S	I2S	I2S4 SOC2BT_DATA	5 46
U056	I2S_50S	I2S	I2S4 BT2SOC_DATA	5 46

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
U057		DWI	DWI_AP_CLK	5 57
U058		DWI	NC_DWI_AP_DI	57
U059		DWI	DWI_AP_DO	5 57

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
U060	I2C_50S	I2C	I2C0_SDA_I1V8	5 57 60
U061	I2C_50S	I2C	I2C0_SCL_I1V8	5 57 60
U062	I2C_50S	I2C	I2C3_CAM_ALS_SDA_I1V8_F	22 60
U063	I2C_50S	I2C	I2C3_CAM_ALS_SCL_I1V8_F	22 60
U064	I2C_50S	I2C	I2C0_HP_ALS_SDA_I1V8_FILT	60
U065	I2C_50S	I2C	I2C0_HP_ALS_SCL_I1V8_FILT	60
U066	I2C_50S	I2C	I2C1_SOC2OSCAR_SWDCCLK_I1V8	5 19
U067	I2C_50S	I2C	I2C1_SOC2OSCAR_SWDIO_I1V8	5 19
U068	I2C_50S	I2C	I2C2_SDA_I1V8	5 47
U069	I2C_50S	I2C	I2C2_SCL_I1V8	5 47
U070	I2C_50S	I2C	I2C3_SDA_I1V8	5 13 22 61
U071	I2C_50S	I2C	I2C3_SCL_I1V8	5 13 22 61
U072	I2C_50S	I2C	DMIC1_FF_SD_FILT	16 60
U073	I2C_50S	I2C	DMIC1_FF_SCLK_FILT	16 60
U074	I2C_50S	I2C	DMIC1_FF_SD	15 14
U075	I2C_50S	I2C	DMIC1_FF_SCLK	15 14
U076	I2C_50S	I2C	SEP_I2C0_SCL	5
U077	I2C_50S	I2C	SEP_I2C0_SDA	5
U078	I2C_50S	I2C	ISP0_CAM_REAR_SCL	7 23
U079	I2C_50S	I2C	ISP0_CAM_REAR_SDA	7 23
U080	I2C_50S	I2C	ISP0_CAM_REAR_SCL_F	23 60
U081	I2C_50S	I2C	ISP0_CAM_REAR_SDA_F	23 60
U082	I2C_50S	I2C	ISP1_CAM_FRONT_SCL	7 22
U083	I2C_50S	I2C	ISP1_CAM_FRONT_SDA	7 22
U084	I2C_50S	I2C	ISP1_CAM_FRONT_SCL_F	22 60
U085	I2C_50S	I2C	ISP1_CAM_FRONT_SDA_F	22 60

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
U086	SPI_50S	SPI	SPI3_CODEC_MISO	5 15
U087	SPI_50S	SPI	SPI3_CODEC_MOSI	5 15
U088	SPI_50S	SPI	SPI3_CODEC_SCLK	5 15
U089	SPI_50S	SPI	SPI3_CODEC_CS_L	5 15
U090	SPI_50S	SPI	SPI2_GRAPE_MISO	5 52 60 61 64
U091	SPI_50S	SPI	SPI2_GRAPE_MOSI	5 52 60 61 64
U092	SPI_50S	SPI	SPI2_GRAPE_SCLK	5 52 60 61 64
U093	SPI_50S	SPI	SPI2_GRAPE_CS_L	5 52 60 61 64
U094	SPI_50S	SPI	SPI2_GRAPE_MISO	5 52 60 61 64
U095	SPI_50S	SPI	SPI2_GRAPE_MOSI	5 52 60 61 64
U096	SPI_50S	SPI	SPI2_GRAPE_SCLK	5 52 60 61 64
U097	SPI_50S	SPI	SPI2_GRAPE_CS_L	5 52 60 61 64
U098	SPI_50S	SPI	SPI_OSCAR_MISO	19 24
U099	SPI_50S	SPI	SPI_OSCAR_MOSI	19 24
U100	SPI_50S	SPI	SPI_OSCAR_SCLK	19 24
U101	SPI_50S	SPI	SPI_OSCAR_MISO_GYRO	19
U102	SPI_50S	SPI	SPI_OSCAR_MISO_ACCEL	19
U103	SPI_50S	SPI	SPI_OSCAR_MISO_COMP1	24
U104	SPI_50S	SPI	SPI_OSCAR_MOSI_R	19
U105	SPI_50S	SPI	SPI_OSCAR_SCLK_R	19
U106	SPI_50S	SPI	SPI_OSCAR2ACCEL_CS_L	19
U107	SPI_50S	SPI	SPI_OSCAR2GYRO_CS_L	19
U108	SPI_50S	SPI	SPI_OSCAR2COMPASS_CS_L	19 24

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
U109	JTAG	JTAG	JTAG_SOC_TCK	4 47 60
U110	JTAG	JTAG	JTAG_SOC_TMS	4 47 60
U111	JTAG	JTAG	JTAG_SOC_TDI	4 60
U112	JTAG	JTAG	TP_JTAG_SOC_TDO	4 60
U113	RST	JTAG	JTAG_SOC_TRST_L	4 13 60
U114	JTAG	JTAG	NC_JTAG_SOC_TRTCK	4
U115	JTAG	JTAG	BB_JTAG_TMS	5 25 28 61
U116	JTAG	JTAG	BB_JTAG_TCK	5 25 28 61
U117	JTAG	JTAG	BB_JTAG_TDO	5 25 28 61
U118	JTAG	JTAG	BB_JTAG_TDI	5 25 28 61
U119	RST	JTAG	BB_JTAG_TRST_L	5 25 28 61
U120	JTAG	JTAG	JTAG_WLAN_TMS_TX_BLANK	46 61
U121	JTAG	JTAG	TP_JTAG_WLAN_TCK	46 61
U122	JTAG	JTAG	JTAG_WLAN_TDO_OSCAR_B	46 61
U123	JTAG	JTAG	JTAG_WLAN_TDI_OSCAR_A	46 61
U124	RST	JTAG	TP_JTAG_WLAN_TRST_L	46 61
U125	JTAG	JTAG	TP_JTAG_CUMULUS_M_TCK	52 61
U126	JTAG	JTAG	TP_JTAG_CUMULUS_M_TDI	52 61
U127	JTAG	JTAG	JTAG_CUMULUS_M_TMS	52 61
U128	JTAG	JTAG	TP_JTAG_CUMULUS_M_TDO	52 61

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB_90D	*	90_OHM_DIFF	USB	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
U129	USB	USB	USB_SOC_P	4 47 60
U130	USB	USB	USB_SOC_N	4 47 60
U131	USB	USB	USB_BB_P	25 47
U132	USB	USB	USB_BB_N	25 47
U133	USB	USB	USB_BB_DEBUG_P	25 28 61
U134	USB	USB	USB_BB_DEBUG_N	25 28 61
U135	USB	USB	E75_DPAIR1_CONN_P	47 49 60
U136	USB	USB	E75_DPAIR1_CONN_N	47 49 60
U137	USB	USB	E75_DPAIR2_CONN_P	47 49 60
U138	USB	USB	E75_DPAIR2_CONN_N	47 49 60
U139	USB	USB	E75_DPAIR1_P	47
U140	USB	USB	E75_DPAIR1_N	47
U141	USB	USB	E75_DPAIR2_P	47
U142	USB	USB	E75_DPAIR2_N	47

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	4:1_SPACING
HSIC	GND	*	1.5:1_SPACING
HSIC_RDY	*	*	2:1_SPACING
HSIC_RDY	GND	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
U143	HSIC	HSIC	HSIC1_WLAN_DATA	4 46 61
U144	HSIC	HSIC	HSIC1_WLAN_STB	4 46 61
U145	HSIC	HSIC	HSIC2_BB_DATA	4 25 28 61
U146	HSIC	HSIC	HSIC2_BB_STB	4 25 28 61
U147	HSIC	HSIC	NC_HSIC0_DATA	4
U148	HSIC	HSIC	NC_HSIC0_STB	4
U149	HSIC	HSIC_RDY	HSIC1_WLAN2SOC_REMOTE_WAKE	5 46 61
U150	HSIC			

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPIOC	*	*	4:1_SPACING
MIPIIC	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PHYSICAL	SPACING	NET_TYPE	PART_NUMBER
	PHYSICAL	SPACING				
M100	MIPT_90D	MIPTOC			MIPIOC_CAM_REAR_CLK_P	7 23 61
M101	MIPT_90D	MIPTOC			MIPIOC_CAM_REAR_CLK_N	7 23 61
M102	MIPT_90D	MIPTOC			MIPIOC_CAM_REAR_DATA_P<0>	7 23 61
M103	MIPT_90D	MIPTOC			MIPIOC_CAM_REAR_DATA_N<0>	7 23 61
M104	MIPT_90D	MIPTOC			MIPIOC_CAM_REAR_DATA_P<1>	7 23 61
M105	MIPT_90D	MIPTOC			MIPIOC_CAM_REAR_DATA_N<1>	7 23 61
M106	MIPT_90D	MIPTOC			NC_MIPIOC_CAM_REAR_DATA_P<2>	7
M107	MIPT_90D	MIPTOC			NC_MIPIOC_CAM_REAR_DATA_N<2>	7
M108	MIPT_90D	MIPTOC			NC_MIPIOC_CAM_REAR_DATA_P<3>	7
M109	MIPT_90D	MIPTOC			NC_MIPIOC_CAM_REAR_DATA_N<3>	7
M110	MIPT_90D	MIPTOC			MIPIOC_CAM_REAR_CLK_FILT_P	23 61
M111	MIPT_90D	MIPTOC			MIPIOC_CAM_REAR_CLK_FILT_N	23 61
M112	MIPT_90D	MIPTOC			MIPIOC_CAM_REAR_DATA_FILT_P<0>	23 61
M113	MIPT_90D	MIPTOC			MIPIOC_CAM_REAR_DATA_FILT_N<0>	23 61
M114	MIPT_90D	MIPTOC			MIPIOC_CAM_REAR_DATA_FILT_P<1>	23 61
M115	MIPT_90D	MIPTOC			MIPIOC_CAM_REAR_DATA_FILT_N<1>	23 61
M116	MIPT_90D	MIPTOC			NC_MIPIOC_CAM_REAR_DATA_FILT_P<2>	7
M117	MIPT_90D	MIPTOC			NC_MIPIOC_CAM_REAR_DATA_FILT_N<2>	7
M118	MIPT_90D	MIPTOC			NC_MIPIOC_CAM_REAR_DATA_FILT_P<3>	7
M119	MIPT_90D	MIPTOC			NC_MIPIOC_CAM_REAR_DATA_FILT_N<3>	7
M120	MIPT_90D	MIPTIC			MIPIIC_CAM_FRONT_CLK_P	7 22 61
M121	MIPT_90D	MIPTIC			MIPIIC_CAM_FRONT_CLK_N	7 22 61
M122	MIPT_90D	MIPTIC			MIPIIC_CAM_FRONT_DATA_P<0>	7 22 61
M123	MIPT_90D	MIPTIC			MIPIIC_CAM_FRONT_DATA_N<0>	7 22 61
M124	MIPT_90D	MIPTIC			NC_MIPIIC_CAM_FRONT_DATA_P<1>	7
M125	MIPT_90D	MIPTIC			NC_MIPIIC_CAM_FRONT_DATA_N<1>	7
M126	MIPT_90D	MIPTIC			MIPIIC_CAM_FRONT_CLK_FILT_P	23 61
M127	MIPT_90D	MIPTIC			MIPIIC_CAM_FRONT_CLK_FILT_N	23 61
M128	MIPT_90D	MIPTIC			MIPIIC_CAM_FRONT_DATA_FILT_P<0>	23 61
M129	MIPT_90D	MIPTIC			MIPIIC_CAM_FRONT_DATA_FILT_N<0>	23 61
M130	MIPT_90D	MIPTIC			NC_MIPIOD_DPCLK	7
M131	MIPT_90D	MIPTIC			NC_MIPIOD_DNCLK	7
M132	MIPT_90D	MIPTIC			NC_MIPIOD_DPDATA0	7
M133	MIPT_90D	MIPTIC			NC_MIPIOD_DNDATA0	7
M134	MIPT_90D	MIPTIC			NC_MIPIOD_DPDATA1	7
M135	MIPT_90D	MIPTIC			NC_MIPIOD_DNDATA1	7
M136	MIPT_90D	MIPTIC			NC_MIPIOD_DPDATA2	7
M137	MIPT_90D	MIPTIC			NC_MIPIOD_DNDATA2	7
M138	MIPT_90D	MIPTIC			NC_MIPIOD_DPDATA3	7
M139	MIPT_90D	MIPTIC			NC_MIPIOD_DNDATA3	7
M140	MIPT_90D	MIPTOC			MIPI_CAM0_CLKCON_P	7
M141	MIPT_90D	MIPTOC			MIPI_CAM0_CLKCON_N	7
M142	MIPT_90D	MIPTOC			MIPI_CAM0_D0CON_P	7
M143	MIPT_90D	MIPTOC			MIPI_CAM0_D0CON_N	7
M144	MIPT_90D	MIPTOC			MIPI_CAM0_D1CON_P	7
M145	MIPT_90D	MIPTOC			MIPI_CAM0_D1CON_N	7
M146	MIPT_90D	MIPTOC			MIPI_CAM0_D2CON_P	7
M147	MIPT_90D	MIPTOC			MIPI_CAM0_D2CON_N	7
M148	MIPT_90D	MIPTOC			MIPI_CAM0_D3CON_P	7
M149	MIPT_90D	MIPTOC			MIPI_CAM0_D3CON_N	7
M150	MIPT_90D	MIPTIC			MIPI_CAM1_CLKCON_P	7
M151	MIPT_90D	MIPTIC			MIPI_CAM1_CLKCON_N	7
M152	MIPT_90D	MIPTIC			MIPI_CAM1_D0CON_P	7
M153	MIPT_90D	MIPTIC			MIPI_CAM1_D0CON_N	7
M154	MIPT_90D	MIPTIC			MIPI_CAM1_D1CON_P	7
M155	MIPT_90D	MIPTIC			MIPI_CAM1_D1CON_N	7
M156	MIPT_90D	MIPTIC			MIPI_CAM1_D2CON_P	7
M157	MIPT_90D	MIPTIC			MIPI_CAM1_D2CON_N	7
M158	MIPT_90D	MIPTIC			MIPI_CAM1_D3CON_P	7
M159	MIPT_90D	MIPTIC			MIPI_CAM1_D3CON_N	7

DEV

BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LED	*	LED

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LEDA	*	*	2.4:1_SPACING
LEDB	*	*	2.4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PHYSICAL	SPACING	NET_TYPE	PART_NUMBER
	PHYSICAL	SPACING				
M160	LEDA	LEDA			LED_IO1_A_R	56
M161	LEDB	LEDB			LED_IO1_B_R	56
M162	LEDA	LEDA			LED_IO2_A_R	56
M163	LEDB	LEDB			LED_IO2_B_R	56
M164	LEDA	LEDA			LED_IO3_A_R	56
M165	LEDB	LEDB			LED_IO3_B_R	56
M166	LEDA	LEDA			LED_IO4_A_R	56
M167	LEDB	LEDB			LED_IO4_B_R	56
M168	LEDA	LEDA			LED_IO5_A_R	56
M169	LEDB	LEDB			LED_IO5_B_R	56
M170	LEDA	LEDA			LED_IO6_A_R	56
M171	LEDB	LEDB			LED_IO6_B_R	56
M172	LEDA	LEDA			LED_IO_1_A	53 56 60
M173	LEDB	LEDB			LED_IO_1_B	53 56 60
M174	LEDA	LEDA			LED_IO_2_A	53 56 60
M175	LEDB	LEDB			LED_IO_2_B	53 56 60
M176	LEDA	LEDA			LED_IO_3_A	53 56 60
M177	LEDB	LEDB			LED_IO_3_B	53 56 60
M178	LEDA	LEDA			LED_IO_4_A	53 56 60
M179	LEDB	LEDB			LED_IO_4_B	53 56 60
M180	LEDA	LEDA			LED_IO_5_A	53 56 60
M181	LEDB	LEDB			LED_IO_5_B	53 56 60
M182	LEDA	LEDA			LED_IO_6_A	53 56 60
M183	LEDB	LEDB			LED_IO_6_B	53 56 60

AUDIO/SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING
AUDIO	AUDIO	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PHYSICAL	SPACING	NET_TYPE	PART_NUMBER
	PHYSICAL	SPACING				
M190	SPKR_DIFF	SPEAKER	AUDIO		SPKRAMP_L1_OUT_P	18 49 60
M191	SPKR_DIFF	SPEAKER	AUDIO		SPKRAMP_L1_OUT_N	18 49 60
M192	SPKR_DIFF	SPEAKER	AUDIO		SPKRAMP_L2_OUT_P	18 49 60
M193	SPKR_DIFF	SPEAKER	AUDIO		SPKRAMP_L2_OUT_N	18 49 60
M194	SPKR_DIFF	SPEAKER	AUDIO		SPKRAMP_R1_OUT_P	17 49 60
M195	SPKR_DIFF	SPEAKER	AUDIO		SPKRAMP_R1_OUT_N	17 49 60
M196	SPKR_DIFF	SPEAKER	AUDIO		SPKRAMP_R2_OUT_P	17 49 60
M197	SPKR_DIFF	SPEAKER	AUDIO		SPKRAMP_R2_OUT_N	17 49 60
M198	USB_90D	USB			MIKEY_TS_P	15 47
M199	USB_90D	USB			MIKEY_TS_N	15 47
M200	USB_90D	USB			L81_MBUS_P	15
M201	USB_90D	USB			L81_MBUS_N	15
M202	SPKR_DIFF	AUDIO_DIFF	AUDIO		LEFT_CH_OUT_P	15 18 60
M203	SPKR_DIFF	AUDIO_DIFF	AUDIO		LEFT_CH_OUT_N	15 18 60
M204	SPKR_DIFF	AUDIO_DIFF	AUDIO		RIGHT_CH_OUT_P	15 17 60
M205	SPKR_DIFF	AUDIO_DIFF	AUDIO		RIGHT_CH_OUT_N	15 17 60
M206	SPKR_DIFF	AUDIO_DIFF	AUDIO		MAX98304_L1_IN_P	18 61
M207	SPKR_DIFF	AUDIO_DIFF	AUDIO		MAX98304_L1_IN_N	18 61
M208	SPKR_DIFF	AUDIO_DIFF	AUDIO		MAX98304_R1_IN_P	17 61
M209	SPKR_DIFF	AUDIO_DIFF	AUDIO		MAX98304_R1_IN_N	17 61
M210	SPKR_DIFF	AUDIO_DIFF	AUDIO		MAX98304_L2_IN_P	18 61
M211	SPKR_DIFF	AUDIO_DIFF	AUDIO		MAX98304_L2_IN_N	18 61
M212	SPKR_DIFF	AUDIO_DIFF	AUDIO		MAX98304_R2_IN_P	17 61
M213	SPKR_DIFF	AUDIO_DIFF	AUDIO		MAX98304_R2_IN_N	17 61
M214	AUDIO_DIFF	AUDIO			SPKR_L1_VSNS_P	
M215	AUDIO_DIFF	AUDIO			SPKR_L1_VSNS_N	
M216	AUDIO_DIFF	AUDIO			SPKR_R1_VSNS_P	
M217	AUDIO_DIFF	AUDIO			SPKR_R1_VSNS_N	
M218	PWR_OP5MM	AUDIO			CODEC_HP_HS3	15
M219	PWR_OP5MM	AUDIO			CODEC_HP_HS4	15
M220	PWR_OP5MM	AUDIO			CONN_HP_HS3_FILT	15 16 60
M221	PWR_OP5MM	AUDIO			CONN_HP_HS4_FILT	15 16 60
M222	PWR_OP2MM	AUDIO			CODEC_HP_LEFT	15
M223	PWR_OP2MM	AUDIO			CODEC_HP_RIGHT	15
M224	PWR_OP2MM	AUDIO			CONN_HP_LEFT_FILT	15 16 60
M225	PWR_OP2MM	AUDIO			CONN_HP_RIGHT_FILT	15 16 60
M226	PP_PWR	PWR			L81_NVCP	15 61
M227	PP_PWR	PWR			L81_PVCP	15 61
M228	PP_PWR	PWR			L81_FLYP	15 61
M229	PP_PWR	PWR			L81_FLYN	15 61
M230	PP_PWR	PWR			L81_FLYC	15 61
M231	PP_PWR	PWR			SPEAKER_VO	
M232	PP_PWR	PWR			L81_FILT	15
M233	PWR_OP1MM	AUDIO			HP_MIC_POS	15
M234	PWR_OP1MM	AUDIO			HP_MIC_NEG	15
M235	PWR_OP1MM	AUDIO			L81_AIN2_POS	15
M236	PWR_OP1MM	AUDIO			L81_AIN2_NEG	15
M237	PWR_OP1MM	AUDIO			CODEC_HP_HS3_REF	15
M238	PWR_OP1MM	AUDIO			CODEC_HP_HS4_REF	15
M239	PWR_OP1MM	AUDIO			CONN_HP_HS3_REF_FILT	15 16 60
M240	PWR_OP1MM	AUDIO			CONN_HP_HS4_REF_FILT	15 16 60
M241	CRYSTAL	*	*	*	5:1_SPACING	
M242	CRYSTAL				XTAL_SOC_24M_I	4
M243	CRYSTAL				XTAL_SOC_24M_O	4
M244	CRYSTAL				SOC_24M_O	4
M245	CRYSTAL				PMU_XTAL	56
M246	CRYSTAL				PMU_EXTAL	56

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PHYSICAL	SPACING	NET_TYPE	PART_NUMBER
	PHYSICAL	SPACING				
M247	CRYSTAL				XTAL_SOC_24M_I	4
M248	CRYSTAL				XTAL_SOC_24M_O	4
M249	CRYSTAL				SOC_24M_O	4
M250	CRYSTAL				PMU_XTAL	56
M251	CRYSTAL				PMU_EXTAL	56

EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP_50S	*	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PHYSICAL	SPACING	NET_TYPE	PART_NUMBER
	PHYSICAL	SPACING				
M252	EDP_90D	EDP			EDP_AUX_P	7 53
M253	EDP_90D	EDP			EDP_AUX_N	7 53 61
M254	EDP_50S	EDP			EDP_HPD	7 53
M255	EDP_90D	EDP			EDP_DATA_P<0>	7 53 61
M256	EDP_90D	EDP			EDP_DATA_N<0>	7 53 61
M257	EDP_90D	EDP			EDP_DATA_P<1>	7 53 61
M258	EDP_90D	EDP			EDP_DATA_N<1>	7 53 61
M259	EDP_90D	EDP			EDP_DATA_P<2>	7 53 61
M260	EDP_90D	EDP			EDP_DATA_N<2>	7 53 61
M261	EDP_90D	EDP			EDP_DATA_P<3>	7 53 61
M262	EDP_90D	EDP			EDP_DATA_N<3>	7 53 61
M263	EDP_90D	EDP			EDP_AUX_EMI_P	53
M264	EDP_90D	EDP			EDP_AUX_EMI_N	53
M265	EDP_90D	EDP			EDP_DATA_EMI_P<0>	53 61
M266	EDP_90D	EDP			EDP_DATA_EMI_N<0>	53 61
M267	EDP_90D	EDP			EDP_DATA_EMI_P<1>	53 61
M268	EDP_90D	EDP			EDP_DATA_EMI_N<1>	53 61
M269	EDP_90D	EDP			EDP_DATA_EMI_P<2>	53 61
M270	EDP_90D	EDP			EDP_DATA_EMI_N<2>	53 61
M271	EDP_90D	EDP			EDP_DATA_EMI_P<3>	53 61
M272						

DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	DRAM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	DRAM_DIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
R100	DDR_50S	DDR	DDR0_CA<0>	8 12 61
R101	DDR_50S	DDR	DDR0_CA<9..1>	8 12 61
R102	DDR_50S	DDR	DDR0_DM<3..0>	8 12 61
R103	DDR_90D	DDR	DDR0_CK_P	8 12 61
R104	DDR_90D	DDR	DDR0_CK_N	8 12 61
R105	DDR_50S	DDR	DDR0_CKE<1..0>	8 12 61
R106	DDR_50S	DDR	DDR0_CSN<1..0>	8 12 61
R107		DDR	DDR0_CA_ZO_SOC	8
R108		DDR	DDR0_DO_ZO_SOC	8
R109		DDR	DDR0_ZO_DRAM	12
R110	DDR_50S	DDR	DDR0_DQ<1..0>	8 12 61
R111	DDR_50S	DDR	DDR0_DQ<2>	8 12 61
R112	DDR_50S	DDR	DDR0_DQ<7..3>	8 12 61
R113	DDR_90D	DDR	DDR0_DQS_P<0>	8 12 61
R114	DDR_90D	DDR	DDR0_DQS_N<0>	8 12 61
R115	DDR_50S	DDR	DDR0_DQ<15..8>	8 12 61
R116	DDR_90D	DDR	DDR0_DQS_P<1>	8 12 61
R117	DDR_90D	DDR	DDR0_DQS_N<1>	8 12 61
R118	DDR_50S	DDR	DDR0_DQ<23..16>	8 12 61
R119	DDR_90D	DDR	DDR0_DQS_P<2>	8 12 61
R120	DDR_90D	DDR	DDR0_DQS_N<2>	8 12 61
R121	DDR_50S	DDR	DDR0_DQ<27..25>	8 12 61
R122	DDR_50S	DDR	DDR0_DQ<28>	8 12 61
R123	DDR_50S	DDR	DDR0_DQ<31..29>	8 12 61
R124	DDR_90D	DDR	DDR0_DQS_P<3>	8 12 61
R125	DDR_90D	DDR	DDR0_DQS_N<3>	8 12 61
R126	DDR_50S	DDR	DDR1_CA<3..0>	8 12 61
R127	DDR_50S	DDR	DDR1_CA<9..4>	8 12 61
R128	DDR_50S	DDR	DDR1_DM<3..0>	8 12 61
R129	DDR_90D	DDR	DDR1_CK_P	8 12 61
R130	DDR_90D	DDR	DDR1_CK_N	8 12 61
R131	DDR_50S	DDR	DDR1_CKE<1..0>	8 12 61
R132	DDR_50S	DDR	DDR1_CSN<0>	8 12 61
R133	DDR_50S	DDR	DDR1_CSN<1>	8 12 61
R134		DDR	DDR1_CA_ZO_SOC	8
R135		DDR	DDR1_DO_ZO_SOC	8
R136		DDR	DDR1_ZO_DRAM	12
R137	DDR_50S	DDR	DDR1_DQ<7..0>	8 12 61
R138	DDR_90D	DDR	DDR1_DQS_P<0>	8 12 61
R139	DDR_90D	DDR	DDR1_DQS_N<0>	8 12 61
R140	DDR_50S	DDR	DDR1_DQ<15..8>	8 12 61
R141	DDR_90D	DDR	DDR1_DQS_P<1>	8 12 61
R142	DDR_90D	DDR	DDR1_DQS_N<1>	8 12 61
R143	DDR_50S	DDR	DDR1_DQ<23..16>	8 12 61
R144	DDR_90D	DDR	DDR1_DQS_P<2>	8 12 61
R145	DDR_90D	DDR	DDR1_DQS_N<2>	8 12 61
R146	DDR_50S	DDR	DDR1_DQ<31..24>	8 12 61
R147	DDR_90D	DDR	DDR1_DQS_P<3>	8 12 61
R148	DDR_90D	DDR	DDR1_DQS_N<3>	8 12 61

VREF (DDR/FMI)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

VOLTAGE	NET_TYPE			
	PHYSICAL	SPACING		
0.6V	MIN_NECK_WIDTH=0.15 MM PP_PWR	PWR	PPVREF_DDR0_CA_SOC	8
0.6V	PP_PWR	PWR	PPVREF_DDR0_DO_SOC	8
0.6V	PP_PWR	PWR	PPVREF_DDR1_CA_SOC	8
0.6V	PP_PWR	PWR	PPVREF_DDR1_DO_SOC	8
0.6V	PP_PWR	PWR	PPVREF_DDR0_CA_DRAM	12
0.6V	PP_PWR	PWR	PPVREF_DDR0_DO_DRAM	12
0.6V	PP_PWR	PWR	PPVREF_DDR1_CA_DRAM	12
0.6V	PP_PWR	PWR	PPVREF_DDR1_DO_DRAM	12
0.9V	PP_PWR	VREF	PPVREF_FMI_SOC	6 61
0.9V	PP_PWR	VREF	PPVREF_FMI_NAND	14 61

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE				
	PHYSICAL	SPACING			
R149	FMI0_AD_CTRL_PP	NAND_50S	NAND	FMI0_AD<0>	6 14 61
R150	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<1>	6 14 61
R151	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<2>	6 14 61
R152	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<3>	6 14 61
R153	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<4>	6 14 61
R154	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<5>	6 14 61
R155	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<6>	6 14 61
R156	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_AD<7>	6 14 61
R157	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_ALE	6 14 61
R158	FMI0_CE	NAND_50S	NAND	FMI0_CE0_L	6 14 60 61
R159	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_CLE	6 14 61
R160	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_DOS	6 14 61
R161	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_RE_L	6 14 61
R162	FMI0_AD_CTRL	NAND_50S	NAND	FMI0_WE_L	6 14 61
R163	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<0>	6 14 61
R164	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<1>	6 14
R165	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<2>	6 14
R166	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<3>	6 14
R167	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<4>	6 14
R168	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<5>	6 14
R169	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<6>	6 14
R170	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_AD<7>	6 14
R171	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_ALE	6 14 61
R172	FMI1_CE	NAND_50S	NAND	FMI1_CE0_L	6 14 61
R173	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_CLE	6 14 61
R174	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_DOS	6 14 61
R175	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_RE_L	6 14 61
R176	FMI1_AD_CTRL	NAND_50S	NAND	FMI1_WE_L	6 14 61

NAND DEV

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
R177	NAND_50S	NAND	FMI0_AD_BUF<0>	
R178	NAND_50S	NAND	FMI0_AD_BUF<1>	
R179	NAND_50S	NAND	FMI0_AD_BUF<2>	
R180	NAND_50S	NAND	FMI0_AD_BUF<3>	
R181	NAND_50S	NAND	FMI0_AD_BUF<4>	
R182	NAND_50S	NAND	FMI0_AD_BUF<5>	
R183	NAND_50S	NAND	FMI0_AD_BUF<6>	
R184	NAND_50S	NAND	FMI0_AD_BUF<7>	
R185	NAND_50S	NAND	FMI0_ALE_BUF	
R186	NAND_50S	NAND	FMI0_CE0_BUF_L	
R187	NAND_50S	NAND	FMI0_CLE_BUF	
R188	NAND_50S	NAND	FMI0_DQS_BUF	
R189	NAND_50S	NAND	FMI0_DQSN_BUF	
R190	NAND_50S	NAND	FMI0_REP_BUF	
R191	NAND_50S	NAND	FMI0_RE_BUF_L	
R192	NAND_50S	NAND	FMI0_WE_BUF_L	
R193	NAND_50S	NAND	FMI1_AD_BUF<0>	
R194	NAND_50S	NAND	FMI1_AD_BUF<1>	
R195	NAND_50S	NAND	FMI1_AD_BUF<2>	
R196	NAND_50S	NAND	FMI1_AD_BUF<3>	
R197	NAND_50S	NAND	FMI1_AD_BUF<4>	
R198	NAND_50S	NAND	FMI1_AD_BUF<5>	
R199	NAND_50S	NAND	FMI1_AD_BUF<6>	
R200	NAND_50S	NAND	FMI1_AD_BUF<7>	
R201	NAND_50S	NAND	FMI1_ALE_BUF	
R202	NAND_50S	NAND	FMI1_CE0_BUF_L	
R203	NAND_50S	NAND	FMI1_CLE_BUF	
R204	NAND_50S	NAND	FMI1_DQS_BUF	
R205	NAND_50S	NAND	FMI1_DQSN_BUF	
R206	NAND_50S	NAND	FMI1_REP_BUF	
R207	NAND_50S	NAND	FMI1_RE_BUF_L	
R208	NAND_50S	NAND	FMI1_WE_BUF_L	

PWR

NET_TYPE			VOLTAGE	PHYSICAL	SPACING	
PHYSICAL	SPACING					
BUCKS						
PP_PWR	PP_PWR	EWR	4.7V			BUCK0 LX0 55
PP_PWR	PP_PWR	EWR	4.7V			BUCK0 LX1 55
PP_PWR	PP_PWR	EWR	4.7V			BUCK0 LX2 55
PP_PWR	PP_PWR	EWR	4.7V			BUCK0 LX3 55
PP_PWR	PP_PWR	EWR	1.1V			BUCK0 FB 55
PP_PWR	PP_PWR	EWR	4.7V			BUCK1 LX0 55
PP_PWR	PP_PWR	EWR	4.7V			BUCK1 LX1 55
PP_PWR	PP_PWR	EWR	4.7V			BUCK1 LX2 55
PP_PWR	PP_PWR	EWR	1.1V			BUCK1 FB 55
PP_PWR	PP_PWR	EWR	4.7V			BUCK2 LX0 55
PP_PWR	PP_PWR	EWR	1.0V			BUCK2 FB 55
PP_PWR	PP_PWR	EWR	4.7V			BUCK3 LX0 55
PP_PWR	PP_PWR	EWR	1.8V			BUCK3 FB 55
PP_PWR	PP_PWR	EWR	4.7V			BUCK4 LX0 55
PP_PWR	PP_PWR	EWR	1.2V			BUCK4 FB 55
PP_PWR	PP_PWR	EWR	4.7V			BUCK5 LX0 55
PP_PWR	PP_PWR	EWR	1.0V			BUCK5 FB 55
PP_PWR	PP_PWR	EWR	4.7V			BUCK6 LX0 55
PP_PWR	PP_PWR	EWR	3.3V			BUCK6 FB 55
RAILS						
PP_PWR	PP_PWR	EWR	1.1V	MIN_NECK_WIDTH=0.15 MM		PPVDD_CPU 55 60 62
PP_PWR	PP_PWR	EWR	1.1V	MIN_NECK_WIDTH=0.15 MM		PPVDD_GPU 55 60 62
PP_PWR	PP_PWR	EWR	1.0V	MIN_NECK_WIDTH=0.15 MM		PPVDD_SOC 55 60 62
PP_PWR	PP_PWR	EWR	1.8V	MAXIMUM_NECK_LENGTH=5 MM		PP1V8_S2R 55 56 60 62
PP_PWR	PP_PWR	EWR	1.8V	MAX_LINE_WIDTH=0.6 MM		PP1V8_SW1 55 57 59 60 62
PP_PWR	PP_PWR	EWR	1.8V	MAXIMUM_NECK_LENGTH=10 MM		PP1V8_SW1_FOREHEAD 55 62
PP_PWR	PP_PWR	EWR	1.8V	MIN_NECK_WIDTH=0.15 MM		PP1V8_EXT_SW 55 60 62
PP_PWR	PP_PWR	EWR	1.8V	PWR_0P1MM		PP1V8_SW2 55 60 62
PP_PWR	PP_PWR	EWR	1.8V	PWR_0P1MM		PP1V8_S2R_SW3 55 60 62
PP_PWR	PP_PWR	EWR	1.8V	MAX_LINE_WIDTH=0.5 MM		PP1V8_S2R_SW3_COMP 60 62
PP_PWR	PP_PWR	EWR	1.8V	MAXIMUM_NECK_LENGTH=10 MM		
PP_PWR	PP_PWR	EWR	1.2V	MAXIMUM_NECK_LENGTH=5 MM		PP1V2_S2R 55 56 60 62
PP_PWR	PP_PWR	EWR	1.2V	PWR_1MM		PP1V2_SW1 55 60 62
PP_PWR	PP_PWR	EWR	1.2V	MAXIMUM_NECK_LENGTH=15 MM		PP1V2_S2R_SW2 55 60 62
PP_PWR	PP_PWR	EWR	3.3V	MIN_NECK_WIDTH=0.1 MM		PPVDD_SRAM 55 60 62
PP_PWR	PP_PWR	EWR	3.3V	PWR_1MM		PP3V3_S2R 55 60 62
PP_PWR	PP_PWR	EWR	3.3V	MAXIMUM_NECK_LENGTH=15 MM		PP3V3_SW 57 60 62
LDOS						
PP_PWR	PP_PWR	EWR	3.0V	MAXIMUM_NECK_LENGTH=20 MM		PP3V0_SPARE1 56 60 62
PP_PWR	PP_PWR	EWR	1.7V	PP_PWR		PP1V7_VA_VCP 56 60 62
PP_PWR	PP_PWR	EWR	3.0V	MAX_LINE_WIDTH=0.5 MM		PP3V0_S2R_SENSOR 56 60 62
PP_PWR	PP_PWR	EWR	3.0V	MAXIMUM_NECK_LENGTH=10 MM		PP3V0_ALS 56 60 62
PP_PWR	PP_PWR	EWR	3.0V	PWR_0P4MM		PP3V0_UVLO 56 60 62
PP_PWR	PP_PWR	EWR	3.3V	PP_PWR		PP3V3_ACC 56 60 62
PP_PWR	PP_PWR	EWR	3.0V	PWR_0P3MM		PP3V0_S2R_TRISTAR 56 60 62
PP_PWR	PP_PWR	EWR	3.0V	PWR_0P3MM		PP3V0_S2R_HALL 56 60 62
PP_PWR	PP_PWR	EWR	1.3V	MAXIMUM_NECK_LENGTH=7 MM		PP1V3_CAM 56 60 62
PP_PWR	PP_PWR	EWR	1.0V	MAXIMUM_NECK_LENGTH=15 MM		PP1V0_SOC 56 60 62
PP_PWR	PP_PWR	EWR	2.6V	MAXIMUM_NECK_LENGTH=45 MM		PP2V6_CAM_AF 56 60 62
PP_PWR	PP_PWR	EWR	2.9V	MAXIMUM_NECK_LENGTH=40 MM		PP2V9_CAM 56 60 62
PP_PWR	PP_PWR	EWR	5.25V	MAXIMUM_NECK_LENGTH=5 MM		PP5V25_GRAPE 56 60 62
INPUT/MAIN/ALWAYS						
PP_PWR	PP_PWR	EWR	4.7V	MIN_NECK_WIDTH=0.15 MM		PPVCC_MAIN 47 55 56 57 58 60 62
PP_PWR	PP_PWR	EWR	4.7V	MAXIMUM_NECK_LENGTH=15 MM		PPBATT_VCC 55 60 62
PP_PWR	PP_PWR	EWR	6.0V	PWR_2MM		PPVBUS_USB_DCIN 55 60 62
PP_PWR	PP_PWR	EWR	1.8V	MAX_LINE_WIDTH=0.6 MM		PP1V8_ALWAYS 56 60 62
PP_PWR	PP_PWR	EWR	4.7V	PWR_10MM		PPBATT_AUDIO_AMP 56 60 62
PMU						
PP_PWR	PP_PWR	EWR	20.4V	PP_PWR		WLED_LX_B 56 61
PP_PWR	PP_PWR	EWR	20.4V	PP_PWR		WLED_LX_A 56 61
PP_PWR	PP_PWR	EWR	20.4V	MAX_LINE_WIDTH=0.6 MM		PPLLED_OUT_A 56 60 62
PP_PWR	PP_PWR	EWR	20.4V	MAX_LINE_WIDTH=0.6 MM		PPLLED_OUT_B 56 60 62
PP_PWR	PP_PWR	EWR	20.4V	PWR_PMU		PPLLED_BACK_REG_A 53 60
PP_PWR	PP_PWR	EWR	20.4V	PWR_PMU		PPLLED_BACK_REG_B 53 60
PP_PWR	PP_PWR	EWR	6.0V	PP_PWR		PP6V0_LCM_VBOOST 56 60
PP_PWR	PP_PWR	EWR	6.0V	PWR_0P2MM		PPVBUS_PROT 47 55 60
PP_PWR	PP_PWR	EWR	6.0V	PP_PWR		PMU_VCENTER 55 60
PP_PWR	PP_PWR	EWR	6.0V	PP_PWR		PP6V0_LCM_HI 56 61
PP_PWR	PP_PWR	EWR	20.4V	PP_PWR		LCM_LX 56
PP_PWR	PP_PWR	EWR	4.7V	PP_PWR		SW_CHGA 55 61
PP_PWR	PP_PWR	EWR	6.0V	PWR_0P2MM		USB_VBUS_DETECT 4 55
PP_PWR	PP_PWR	EWR	6.0V	PWR_0P2MM		USB_VBUS_DETECT_R 4
PP_PWR	PP_PWR	EWR	6.0V			PMU_GPIO_BB_VBUS_DET 25 28 57 61

NET_TYPE			VOLTAGE	PHYSICAL	SPACING	
PHYSICAL	SPACING					
PP_PWR	PP_PWR	EWR	1.8V			PP1V8_PLL_SOC_F 4
PP_PWR	PP_PWR	EWR	1.8V			PP1V8_EDP_AVDD_AUX 7
PP_PWR	PP_PWR	EWR	0.4V			TP_PP0V4_MIPI1D 7
PP_PWR	PP_PWR	EWR	0.4V			TP_PP0V4_MIPI1D 7
PP_PWR	PWR_0P2MM	EWR	1.8V			PP1V8_XTAL 9
PP_PWR	PP_PWR	EWR	1.8V			PP1V8_VDD_ANA_TMPSADC 10
PP_PWR	PP_PWR	EWR	1.2V			PPVDDI_NAND 14
PP_PWR	PP_PWR	EWR	1.8V			PP1V8_DMIC_FILTER 14 60
PP_PWR	PP_PWR	EWR	3.0V			PP3V0_HP_ALS_FILTER 60
PP_PWR	PP_PWR	EWR	8.75V			SPKR_L1_SWITCH
PP_PWR	PP_PWR	EWR	8.75V			SPKR_R1_SWITCH
PP_PWR	PP_PWR	EWR	1.8V			PPVDD_SPKRAMP
PP_PWR	PP_PWR	EWR	1.7V			PP1V7_VCP 15 60
PP_PWR	PP_PWR	EWR	4.2V			PPVCC_VPROG_CP 15
PP_PWR	PP_PWR	EWR	4.2V			PPVCC_VPROG_MB 15
PP_PWR	PP_PWR	EWR	4.2V			PPVCC_VPROG_MB_F 15
PP_PWR	PWR_1MM	EWR	4.7V			PPVCC_MAIN_LCD_SW 53 60
PP_PWR	PWR_1MM	EWR	4.7V			PPVCC_MAIN_LCD_SW_CONN 53 60
PP_PWR	PWR_1MM	EWR	4.7V			PPVCC_MAIN_GRAPE_FILTER 53 60
PP_PWR	PP_PWR	EWR	5.25V			PP5V25_GRAPE_FILTER 51 52 60 61
PP_PWR	PP_PWR	EWR	1.8V			PP1V8_GRAPE_SW 51 52 60 61
PP_PWR	PP_PWR	EWR	1.8V			PP1V8_GRAPE_FILTER 51 52 60 61
PP_PWR	PP_PWR	EWR	3.0V			PP3V0_GYRO 19 60
PP_PWR	PP_PWR	EWR	3.0V			PP3V0_ACCEL 19 60
PP_PWR	PWR_0P3MM	EWR	3.0V			PP3V0_S2R_HALL_FILTER 20 50 60
PP_PWR	PWR_0P3MM	EWR	1.2V			PP1V2_CAM_FRONT_FILTER 60
PP_PWR	PP_PWR	EWR	1.8V			PP1V8_CAM_FRONT_FILTER 22 60
PP_PWR	PP_PWR	EWR	2.9V			PP2V9_AVDD_CAM_FRONT_FILTER 22 60
PP_PWR	PWR_0P3MM	EWR	3.0V			PP3V0_ALS_FILTER 22 60
PP_PWR	PP_PWR	EWR	2.6V			PP2V6_CAM_REAR_AF_FILTER 23 60
PP_PWR	PP_PWR	EWR	1.28V			PP1V3_CAM_REAR_FILTER 23 60
PP_PWR	PP_PWR	EWR	1.8V			PP1V8_CAM_REAR_FILTER 23 60
PP_PWR	PP_PWR	EWR	1.28V			PP1V3_CAM_REAR 23 60
PP_PWR	PP_PWR	EWR	2.8V			PP2V9_AVDD_CAM_REAR_FILTER 23 60
PP_PWR	PP_PWR	EWR	3.0V			PP3V0_COMP 24 60
PP_PWR	PP_PWR	EWR	1.8V			PP1V8_COMP 24 60
PP_PWR	PP_PWR	EWR	3.0V			PP3V0_SENSOR_PROX_FILTER 60
PP_PWR	PP_PWR	EWR	3.0V			PP3V0_SENSOR_PROX_ADUX1049_FILTER 60
PP_PWR	PP_PWR	EWR	3.0V			PPAVDD_SENSOR_PROX_ADUX1049 45 60
PP_PWR	PP_PWR	EWR	3.0V			PP3V0_SENSOR_PROX_AD7149_FILTER 45 60
PP_PWR	PWR_2MM	EWR	6.0V			PPVBUS_E75_USB_CONN 48 49 60
PP_PWR	PP_PWR	EWR	3.3V			PPOUT_E75_ACC_ID1_CONN 48 49 60
PP_PWR	PP_PWR	EWR	3.3V			PPOUT_E75_ACC_ID2_CONN 48 49 60
PP_PWR	PP_PWR	EWR	3.3V			PPOUT_E75_ACC_ID1 47 48
PP_PWR	PP_PWR	EWR	3.3V			PPOUT_E75_ACC_ID2 47 48
PP_PWR	PP_PWR	EWR	3.0V			PP3V0_IO_ALS_FILTER 60
PP_PWR		ANLG				BATT_NTC 54 57 60
PP_PWR		ANLG				BATT_SNS 54 55
PP_PWR		ANLG				BATT_SNS_R 55

GND

NET	VOLTAGE	NET_TYPE		
		PHYSICAL	SPACING	
PP_PWR	GND			GND_AUDIO_CODEC 15 60
PP_PWR	GND			GND_AVDD_CAM_FRONT 22
PP_PWR	GND			GND_PP1V8_CAM_FRONT 22
PP_PWR	GND			GND_PP2V9_CAM_FRONT 22
PP_PWR	GND			GND_COMP 24
PP_PWR	GND			GND_PMU
PP_PWR	GND			GND_SPKR_AMP_L1
PP_PWR	GND			GND_SPKR_AMP_L2
PP_PWR	GND			GND_SPKR_AMP_R1
PP_PWR	GND			GND_SPKR_AMP_R2

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	3:1_SPACING

NET_TYPE			ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
PHYSICAL	SPACING					
PP_PWR	RST	RST				BB_TRST_L
PP_PWR	RST	RST				DBG_RST
PP_PWR	RST	RST				DEBUG_RST_L 25 28 61
PP_PWR	RST	RST				GSM_TXBURST_IND
PP_PWR	RST	RST				RST_AP_1V8_L
PP_PWR	RST	RST				RESET_SOC_L 4 13 25 47 57 60 61
PP_PWR	RST	RST				GPIO_SOC2BB_RST_L 5 25 27 60
PP_PWR	RST	RST				RST_BB_PMU_L
PP_PWR	RST	RST				RST_BT_L
PP_PWR	RST	RST				RST_DET_L
PP_PWR	RST	RST				GPIO_SOC2GRAPE_RESET_L 5 52 60 61
PP_PWR	RST	RST				PMU_GPIO_CODEC_RST_L 15 57
PP_PWR	RST	RST				TS2PMU_RESET_IN 47 57
PP_PWR	RST	RST				GPIO_BB2SOC_RESET_DET_L 5 25 29
PP_PWR	RST	RST				SIMCRD_RST
PP_PWR	RST	RST				WDOG_SOC 4 13
PP_PWR	RST	RST				WDOG_SOC2PMU_RESET_IN 13 57
PP_PWR	RST	RST				GPIO_OSCAR_RESET_L 5 29 60
PP_PWR	RST	RST				ISP1_CAM_FRONT_SHUTDOWN_L 7 22
PP_PWR	RST	RST				ISP1_CAM_REAR_SHUTDOWN_L 7 23
PP_PWR	RST	RST				ISP1_CAM_FRONT_SHUTDOWN_L_F 22 60
PP_PWR	RST	RST				ISP0_CAM_REAR_SHUTDOWN_L_F 22 60
PP_PWR	RST	RST				PMU_GPIO_PMU2BBPMU_RST_L 25 27 57 60
PP_PWR	RST	RST				PMU_GPIO_PMU2BBPMU_RST_R_L 57
PP_PWR	RST	RST				JTAG_AP_TRST_L
PP_PWR	RST	RST				GPIO_BB_RST_L
PP_PWR	RST	RST				RST_PMU_IN
PP_PWR	RST	RST				UD881_RST
PP_PWR	RST	RST				UD882_RST

PMU SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PMU_SENSE	*	*	3:1_SPACING
PMU_SENSE	GND	*	1.5:1_SPACING

NET	VOLTAGE	NET_TYPE		
		PHYSICAL	SPACING	
PP_PWR	1.1V	PWR_SENSE	PMU_SENSE	PPVDD_CPU_SOC_SENSE 11 57 61
PP_PWR	1.1V	PWR_SENSE	PMU_SENSE	PPVDD_GPU_SOC_SENSE 11 57 61
PP_PWR	1.0V	PWR_SENSE	PMU_SENSE	PPVDD_SOC_SOC_SENSE 11 57 61
PP_PWR	1.1V	PWR_SENSE	PMU_SENSE	PPVDD_CPU_RAIL_SENSE 11 57
PP_PWR	1.1V	PWR_SENSE	PMU_SENSE	PPVDD_GPU_RAIL_SENSE 11 57
PP_PWR	1.0V	PWR_SENSE	PMU_SENSE	PPVDD_SOC_RAIL_SENSE 10 57
PP_PWR	1.05V	MIN_NECK_WIDTH=0.05 MM	PMU_SENSE	ADC_SMPS1_MSMC_1V05
PP_PWR	1.8V	MIN_NECK_WIDTH=0.05 MM	PMU_SENSE	ADC_SMPS3_MSME_1V8

RF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
WIFI_50S	*	50_OHM_RF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
WIFI	*	*	4:1_SPACING

	NET_TYPE			
	PHYSICAL	SPACING		
142	WIFI_50S	WIFI	RF_G_0_MATCH_MOD	46
152	WIFI_50S	WIFI	RF_G_0_MATCH_ANT	
153	WIFI_50S	WIFI	RF_G_0_BAW_MOD	46
154	WIFI_50S	WIFI	RF_G_0_BAW_ANT	46
141	WIFI_50S	WIFI	RF_G_0_DIPLEXER	46
142	WIFI_50S	WIFI	RF_A_0_MATCH	46
143	WIFI_50S	WIFI	RF_A_0_DIPLEXER	46
144	WIFI_50S	WIFI	RF_G_1_MATCH_MOD	46
155	WIFI_50S	WIFI	RF_G_1_MATCH_ANT	
156	WIFI_50S	WIFI	RF_G_1_BAW_MOD	
157	WIFI_50S	WIFI	RF_G_1_BAW_ANT	
145	WIFI_50S	WIFI	RF_G_1_DIPLEXER	46
146	WIFI_50S	WIFI	RF_A_1_MATCH	46
147	WIFI_50S	WIFI	RF_A_1_DIPLEXER	46
148	WIFI_50S	WIFI	RF_0_ANT_MATCH_T	46
150	WIFI_50S	WIFI	RF_0_ANT	46
151	WIFI_50S	WIFI	RF_1_ANT_MATCH_T	46
149	WIFI_50S	WIFI	RF_1_ANT	46