1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,D1

9/8/12

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9216	1	SCHEM,MLB,D1	SCH	CRITICAL	
820-3462	1	PCBF,MLB(NEW),D1	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST MODIFIED=Thu Aug 9 12 34 09 2012

DRAWING TITLE: SCHEM,MLB,D1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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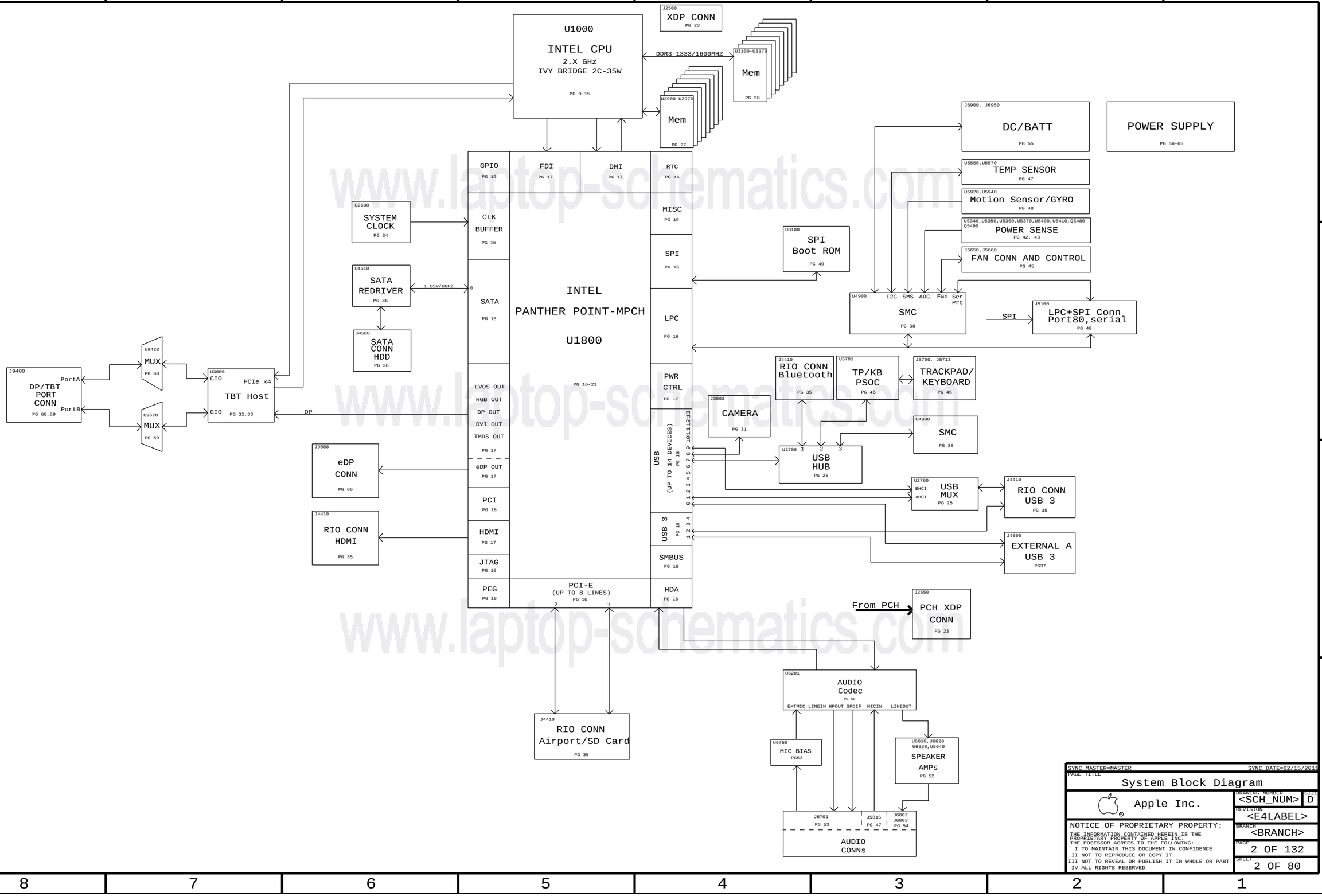
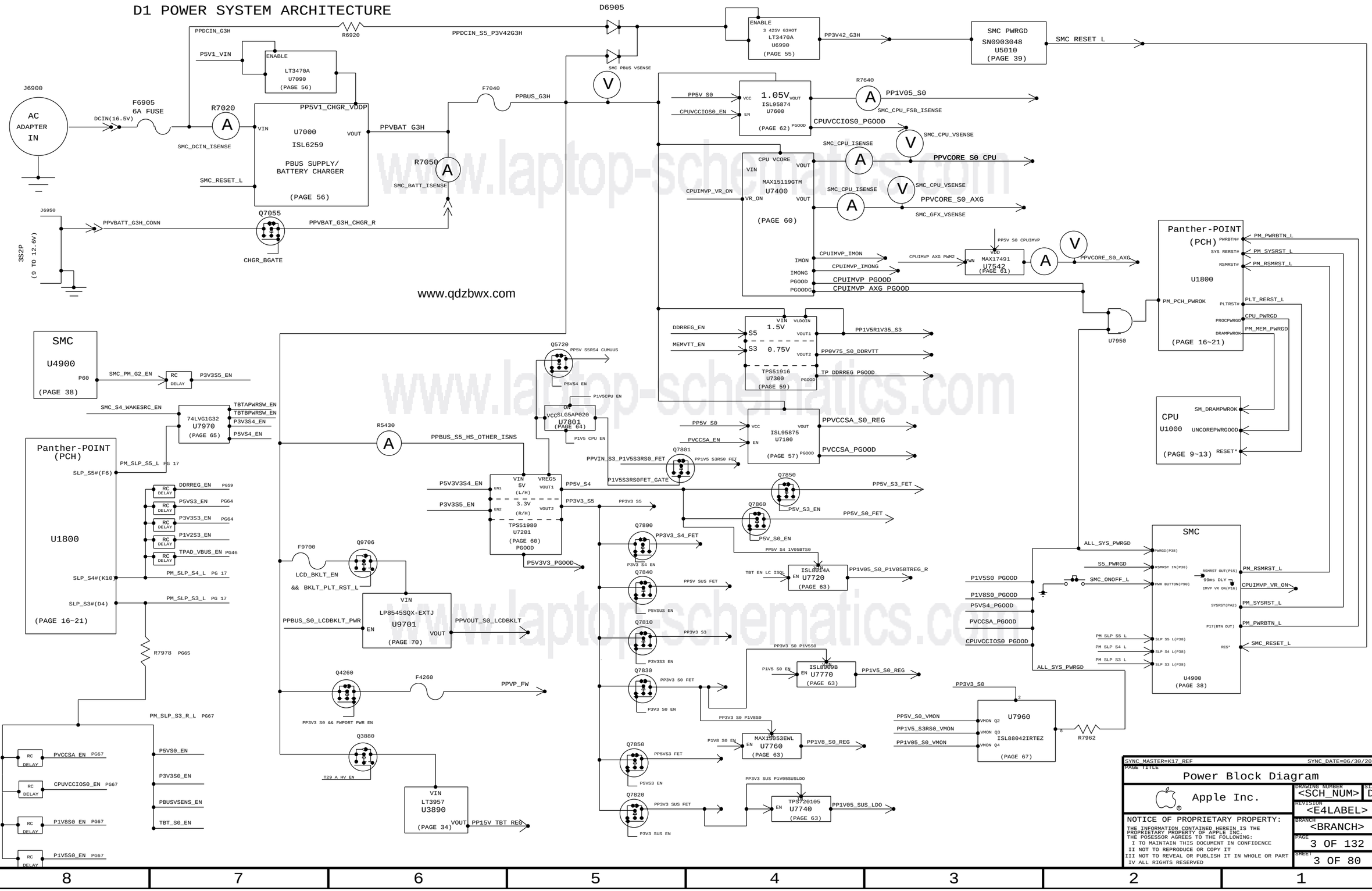


D1 POWER SYSTEM ARCHITECTURE



SYNC_MASTER=K17_REF	SYNC_DATE=06/30/2009
PAGE TITLE	Power Block Diagram
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-4094	DEV BOM,MLB,D1	D1_DEVEL:PVB
607-9189	CMN PTS,PCBA,MLB,D1	D1_COMMON
639-3288	PCBA,2.5G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:DWP2,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3289	PCBA,2.9G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:DWNY,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3290	PCBA,2.5G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:DWP0,RAM_6G_HYNIX_CH0_1600_S
639-3291	PCBA,2.9G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:DWNW,RAM_6G_HYNIX_CH0_1600_S
639-3694	PCBA,2.5G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F16P,RAM_4G_SAMSUNG_35NM_1600_S
639-3695	PCBA,2.9G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F16M,RAM_4G_SAMSUNG_35NM_1600_S
639-3696	PCBA,2.9G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F16N,RAM_4G_HYNIX_1600_S
639-3697	PCBA,2.5G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F16V,RAM_4G_HYNIX_1600_S
639-3773	PCBA,2.5G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F26M,RAM_6G_ELPIDA_CH0_1600_S
639-3772	PCBA,2.9G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F26J,RAM_6G_ELPIDA_CH0_1600_S
639-3770	PCBA,2.5G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F26L,RAM_4G_ELPIDA_1600_S
639-3771	PCBA,2.9G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F26H,RAM_4G_ELPIDA_1600_S
639-3849	PCBA,2.5G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F2WT,RAM_6G_MICRON_CH0_1600_S
639-3848	PCBA,2.9G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F2WR,RAM_6G_MICRON_CH0_1600_S
639-3873	PCBA,2.6G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33H,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3874	PCBA,2.8G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33P,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3875	PCBA,2.6G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33L,RAM_6G_HYNIX_CH0_1600_S
639-3876	PCBA,2.8G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F339,RAM_6G_HYNIX_CH0_1600_S
639-3881	PCBA,2.6G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33G,RAM_4G_SAMSUNG_35NM_1600_S
639-3882	PCBA,2.8G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33C,RAM_4G_SAMSUNG_35NM_1600_S
639-3884	PCBA,2.8G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F337,RAM_4G_HYNIX_1600_S
639-3883	PCBA,2.6G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33D,RAM_4G_HYNIX_1600_S
639-3877	PCBA,2.6G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33Q,RAM_6G_ELPIDA_CH0_1600_S
639-3878	PCBA,2.8G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F338,RAM_6G_ELPIDA_CH0_1600_S
639-3885	PCBA,2.6G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33J,RAM_4G_ELPIDA_1600_S
639-3886	PCBA,2.8G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33N,RAM_4G_ELPIDA_1600_S
639-3879	PCBA,2.6G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33M,RAM_6G_MICRON_CH0_1600_S
639-3880	PCBA,2.8G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F336,RAM_6G_MICRON_CH0_1600_S
639-3846	PCBA,2.5G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F2WV,RAM_4G_MICRON_1600_S
639-3847	PCBA,2.9G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F2WQ,RAM_4G_MICRON_1600_S
639-3887	PCBA,2.6G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33K,RAM_4G_MICRON_1600_S
639-3888	PCBA,2.8G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33F,RAM_4G_MICRON_1600_S

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DV7Q]	CRITICAL	EEEE:DV7Q
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWNY]	CRITICAL	EEEE:DWNY
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWNW]	CRITICAL	EEEE:DWNW
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWP0]	CRITICAL	EEEE:DWP0
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWP2]	CRITICAL	EEEE:DWP2
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16M]	CRITICAL	EEEE:F16M
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16N]	CRITICAL	EEEE:F16N
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16P]	CRITICAL	EEEE:F16P
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16V]	CRITICAL	EEEE:F16V
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26H]	CRITICAL	EEEE:F26H
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26J]	CRITICAL	EEEE:F26J
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26L]	CRITICAL	EEEE:F26L
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26M]	CRITICAL	EEEE:F26M
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WQ]	CRITICAL	EEEE:F2WQ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WR]	CRITICAL	EEEE:F2WR
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WT]	CRITICAL	EEEE:F2WT
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WV]	CRITICAL	EEEE:F2WV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F336]	CRITICAL	EEEE:F336
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F337]	CRITICAL	EEEE:F337
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F338]	CRITICAL	EEEE:F338
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F339]	CRITICAL	EEEE:F339
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33C]	CRITICAL	EEEE:F33C
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33D]	CRITICAL	EEEE:F33D
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33F]	CRITICAL	EEEE:F33F
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33G]	CRITICAL	EEEE:F33G
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33H]	CRITICAL	EEEE:F33H
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33J]	CRITICAL	EEEE:F33J
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33K]	CRITICAL	EEEE:F33K
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33L]	CRITICAL	EEEE:F33L
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33M]	CRITICAL	EEEE:F33M
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33N]	CRITICAL	EEEE:F33N
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33P]	CRITICAL	EEEE:F33P
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33Q]	CRITICAL	EEEE:F33Q

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0364	128S0264		ALL	Kemet alt to Sanyo
128S0303	128S0353		ALL	Panasonic alt to Sanyo
376S0953	376S0958		ALL	RENESAS ALT TO FAIRCHILD
128S0311	128S0329		ALL	NEC ALT TO SANYO
353S3237	353S2192		ALL	TI ALT TO INTERSIL
376S0977	376S0859		ALL	Diodes alt to Toshiba
138S0722	138S0691		ALL	Multi alt to Samsung
197S0487	197S0485		ALL	Epson alt to TXC
197S0484	197S0485		ALL	NDK alt to TXC
197S0479	197S0486		ALL	Epson alt to TXC
197S0478	197S0486		ALL	NDK alt to TXC
197S0481	197S0480		ALL	Epson alt to NDK
376S0972	376S0612		ALL	ROHM alt to Toshiba
376S1053	376S0604		ALL	Diodes alt to Fairchild
376S1017	376S0612		ALL	ROHM alt to Toshiba
138S0624	138S0677		ALL	Murata alt to Taiyo Yuden
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung
152S1703	152S1701		ALL	Sumida alt to Cyntec
371S0730	371S0490		ALL	Diodes alt to NXP
138S0725	138S0724		ALL	Samsung alt to Murata
138S0727	138S0709		ALL	Samsung alt to Murata
376S1080	376S0820		ALL	Diodes alt to ON Semi
372S0186	372S0185		ALL	NXP alt to Diodes
128S0363	128S0296		ALL	NEC alt to Sanyo
376S0903	376S0796		ALL	Fairchild alt to Siliconix
740S0144	740S0118		ALL	Littlefuse alt to Polytronic
152S1539	152S1598		ALL	Cyntec alt to Toko
152S1645	152S0461		ALL	Cyntec alt to Vishay
155S0667	155S0583		ALL	MAG LAYERS ALT TO MURATA
103S0305	103S0266		ALL	Yageo alt to Cyntec
112S0274	112S0254		ALL	Yageo alt to Cyntec
376S1113	376S1110		ALL	Diodes to AOS
155S0588	155S0367		ALL	murata ALT TO MURATA

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4181	1	IVB QBP0 ES2 K0 2 3 35W 2+2 1 0 3M BGA	U1000	CRITICAL	CPU IVB 2C 2 3G ES2
337S4182	1	IVB QBP0 ES2 K0 2 6 35W 2+2 1 0S 4M BGA	U1000	CRITICAL	CPU IVB 2C 2 6G ES2
337S4292	1	IVB Q4CT Q5 L1 2 5 35W 2+2 1 1 3M BGA	U1000	CRITICAL	CPU IVB 2C 2 5G Q5
337S4300	1	IVB QC36 Q5 L1 2 6 35W 2+2 1 2 3M BGA	U1000	CRITICAL	CPU IVB 2C 2 6G Q5
337S4302	1	IVB QC34 Q5 L1 2 8 35W 2+2 1 2 3M BGA	U1000	CRITICAL	CPU IVB 2C 2 8G Q5
337S4294	1	IVB QC4M Q5 L1 2 9 35W 2+2 1 2S 4M BGA	U1000	CRITICAL	CPU IVB 2C 2 9G Q5
337S4264	1	IVB S R0N0 PRQ L1 2 5 35W 2+2 1 1 3M BGA	U1000	CRITICAL	CPU IVB 2C 2 5G
337S4338	1	IVB S R0MY PRQ L1 2 6 35W 2+2 1 2 3M BGA	U1000	CRITICAL	CPU IVB 2C 2 6G
337S4339	1	IVB S R0MU PRQ L1 2 8 35W 2+2 1 2 3M BGA	U1000	CRITICAL	CPU IVB 2C 2 8G
337S4265	1	IVB S R0MU PRQ L1 2 9 35W 2+2 1 2S 4M BGA	U1000	CRITICAL	CPU IVB 2C 2 9G
337S4180	1	IC PCH PPT MB SFF ES2 B0	U1800	CRITICAL	PCH ES2
337S4235	1	IC PCH PPT MB SFF P Q5 C0	U1800	CRITICAL	PCH C0
337S4283	1	IC PCH PPT MB SFF PRQ C1	U1800	CRITICAL	PCH C1
338S1113	1	IC TBT CR-4C B1 PRQ 288FCBGA 12X12MM	U3600	CRITICAL	TBTNTR B1
333S0623	16	IC SDRAM 2GBIT 256MX8 DDR3-1600 78FBGA	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070 U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	2G SAMSUNG 35NM 1600 S
333S0622	16	IC SDRAM 2GBIT 256MX8 DDR3-1600 78FBGA	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070 U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	2G HYNIX 1600 S
333S0628	16	IC SDRAM DDR3-1600 256MX8 78FBGA D-DIE ELPIDA	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070 U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	2G ELPIDA 1600 S
333S0649	16	IC SDRAM DDR3-1600 256MX8 78FBGA MICRON	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070 U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	2G MICRON 1600 S
333S0625	16	IC SDRAM DDR3-1600 512MX8 78FBGA HYNIX	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070 U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	4G HYNIX 1600 S
333S0629	16	IC SDRAM DDR3-1600 512MX8 78FBGA B-DIE ELPIDA	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070 U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	4G ELPIDA 1600 S
333S0624	16	IC SDRAM DDR3-1600 512MX8 78FBGA 035 SAMSUNG	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070 U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	4G SAMSUNG 35NM 1600 S
333S0623	8	IC SDRAM 2GBIT 256MX8 DDR3-1600 78FBGA	U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	6G SAMSUNG 35NM CH0 1600 S
333S0624	8	IC SDRAM DDR3-1600 512MX8 78FBGA 035 SAMSUNG	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070	CRITICAL	6G SAMSUNG 35NM CH0 1600 S
333S0622	8	IC SDRAM 2GBIT 256MX8 DDR3-1600 78FBGA	U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	6G HYNIX CH0 1600 S
333S0625	8	IC SDRAM DDR3-1600 512MX8 78FBGA HYNIX	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070	CRITICAL	6G HYNIX CH0 1600 S
333S0628	8	IC SDRAM DDR3-1600 256MX8 78FBGA D-DIE ELPIDA	U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	6G ELPIDA CH0 1600 S
333S0629	8	IC SDRAM DDR3-1600 512MX8 78FBGA B-DIE ELPIDA	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070	CRITICAL	6G ELPIDA CH0 1600 S
333S0660	16	IC SDRAM DDR3-1600 512MX8 78FBGA MICRON	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070 U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	4G MICRON 1600 S
333S0649	8	IC SDRAM DDR3-1600 256MX8 78FBGA MICRON	U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	6G MICRON CH0 1600 S
333S0660	8	IC SDRAM DDR3-1600 512MX8 78FBGA MICRON	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070	CRITICAL	6G MICRON CH0 1600 S

D1 BOM GROUPS

BOM GROUP	BOM OPTIONS
D1_COMMON	ALTERNATE,COMMON,D1_COMMON1,D1_COMMON2,D1_PROGPARTS,D1_PVB
D1_COMMON1	CPUMEM:S0,SMC_DEBUG_YES,TBTBST:Y,TBTRTR:B1,TBTHV:P15V,HUB_2NONREM,USBHUB:2512B,AXG_PHASE2,TBTISNS:YES
D1_COMMON2	EDP:YES,PPDDR:1V35,LPCPLUS_CONN:YES,LPCPLUS_R:YES,CAPS:INT,BTPWR:S4,SKIP_5V3V3:AUDIBLE,TPAD_5V_LDO:S5,SMS
D1_PVB	LOADISNS:NO,LCDBKLT:PROD,KBDBKLT:PROD
D1_PROGPARTS	SMC_PROG:PVB,TBTROM:PROG,BOOTROM_PROG:PVB,TPAD_PSOC:PROG
D1_BLANK	
D1_DEVEL:ENG	ALTERNATE,IVB_PPT_XDP,LOADISNS:YES,S0PGOOD_ISL,DDRVREF_DAC,VREFDQ:M1_M3,VREFCA:LDO_DAC
D1_DEVEL:PVB	ALTERNATE IVB PPT XDP VREFDQ M1 M3 VREFCA LDO
IVB_PPT_XDP	XDP XDP CONN XDP CPU BPM XDP PCH

DDR3 SPD STRAPPINGS

BOM GROUP	BOM OPTIONS
RAM_4G_HYNIX_1600_S	4G_HYNIX_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_2G_ELPIDA_1600_S	2G_ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_4G_SAMSUNG_28NM_1600_S	4G_SAMSUNG_28NM_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_2G_MICRON_1600_S	2G_MICRON_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_ELPIDA_1600_S	4G_ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_4G_SAMSUNG_35NM_1600_S	4G_SAMSUNG_35NM_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_6G_SAMSUNG_35NM_CH0_1600_S	6G_SAMSUNG_35NM_CH0_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM_4G_MICRON_1600_S	4G_MICRON_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM_6G_MICRON_CH0_1600_S	6G_MICRON_CH0_1600_S,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_6G_ELPIDA_CH0_1600_S	6G_ELPIDA_CH0_1600_S,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_6G_SAMSUNG_28NM_CH0_1600_S	6G_SAMSUNG_28NM_CH0_1600_S,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_6G_HYNIX_CH0_1600_S	6G_HYNIX_CH0_1600_S,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_2G_SAMSUNG_1600_S	2G_SAMSUNG_35NM_1600_S,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_2G_HYNIX_1600_S	2G_HYNIX_1600_S,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0642	16	IC SDRAM DDR3-1600 512MX8 78FBGA C-DIE SAMSUNG	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070 U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	4G SAMSUNG 28NM 1600 S
333S0623	8	IC SDRAM 2GBIT 256MX8 DDR3-1600 78FBGA	U2100 U2110 U2120 U2130 U2140 U2150 U2160 U2170	CRITICAL	6G SAMSUNG 28NM CH0 1600 S
333S0642	8	IC SDRAM DDR3-1600 512MX8 78FBGA C-DIE SAMSUNG	U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070	CRITICAL	6G SAMSUNG 28NM CH0 1600 S

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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PD Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-1533	1	STDOFF,BMU,TOPSIDE,D1,SM	J6950_63	CRITICAL	
860-1530	1	STDOFF-1.9D2.93H-TH-0.85-1.2	J6950_64	CRITICAL	
860-1529	1	STDOFF-1.80D1.53H-SM	J6950_65	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	
946-4350	1	D1 MLB LOCTITE UV GLUE 190024/S 0.24G	EDGE_BOND	CRITICAL	

DEVELOPMENT/BASE BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-4094	1	D1 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-9189	1	D1 MLB BASE BOM	BASE	CRITICAL	BASE_BOM

SMC

341S3528	1	IC SMC12 PROTO1 D1	U4900	CRITICAL	SMC PROG PROTO
341S3404	1	IC SMC DEVELOPMENT-PIB D1	U4900	CRITICAL	SMC PROG PIB
341S3405	1	IC SMC DEVELOPMENT-FSB D1	U4900	CRITICAL	SMC PROG FSB
341S3406	1	IC SMC DEVELOPMENT-PVB D1	U4900	CRITICAL	SMC PROG PVB

EFI ROM

341S3571	1	IC EF ROM PROTO1 D1	U6100	CRITICAL	BOOTROM PROG PROTO
341S3603	1	IC EFI ROM PIB D1	U6100	CRITICAL	BOOTROM PROG PIB
341S3636	1	IC EFI ROM PIB2 D1	U6100	CRITICAL	BOOTROM PROG PIB2
341S3650	1	IC EFI ROM FSB D1	U6100	CRITICAL	BOOTROM PROG FSB
341SXXXX	1	IC EFI ROM FSB2 D1	U6100	CRITICAL	BOOTROM PROG FSB2
341S3667	1	IC EFI ROM PVB D1	U6100	CRITICAL	BOOTROM PROG PVB

Programmables - All builds

335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH Macronix	U6100	CRITICAL	BOOTROM BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH Numonyx	U6100	CRITICAL	BOOTROM BLANK
341S3670	1	IC TP PSOC V224 PVB D1	U5701	CRITICAL	TPAD PSOC PROG
337S2983	1	IC TP PSOC QFN BLANK	U5701	CRITICAL	TPAD PSOC BLANK
341S3668	1	IC EEPROM CR V14 1 D1 PVB	U3690	CRITICAL	TBTROM PROG
335S0865	1	IC EEPROM SERIAL 8KB SOIC	U3690	CRITICAL	TBTROM BLANK
338S1098	1	IC SMC12 A3 LX4FS1AH58BC1GA3	U4900	CRITICAL	SMC BLANK
998 3919	1	SOCKET SMC12	J4900	CRITICAL	SMC SOCKET

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST
PP5V_S0 — 3 TPs per Fan
FAN_LT_PWM
FAN_LT_TACH

J5660 (RIGHT FAN CONN)

FAN_RT_PWM
FAN_RT_TACH
GND — 5 TPs per Fan

J3502 (ALS/CAMERA CONN)

SMBUS_SMC_2_S3_SDA
SMBUS_SMC_2_S3_SCL
PP5V_S3_ALSCAMERA_F

J4400 (RIO CABLE CONN)

PP3V3_S4
PP3V3_S3
PP3V3_WLAN_F
PP5V_S4
PP1V5_S0

J4410 (RIO FLEX CONN)

USB_EXTB_OC_L
HDMI_IG_DDC_CLK
HDMI_IG_DDC_DATA
HDMI_HPD_L
PM_SLP_S3_L
PM_SLP_S4_L
AP_CLKREQ_Q_L
ENET_RESET_L
ENET_CLKREQ_L
SD_PWR_EN
SDCONN_STATE_CHANGE_SMC
PCIE_WAKE_L
AP_CLKREQ_Q_L
AP_RESET_CONN_L
WIFI_EVENT_L
USB_EXTB_P
USB_EXTB_N
USB_BT_CONN_P
USB_BT_CONN_N

AP_RESET_CONN_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA

SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA

J5815 (KBD BACKLIGHT CONN)

PP_KBD_BOOST_VOUT
KBDLED_CATHODE1
KBDLED_CATHODE2
SMC_KBDLED_PRESENT_L

J6950 (MAIN BATT CONN)

PPVBAT_G3H_CONN
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
SYS_DETECT_L_R

SYSDET1
SYSDET_3_4

J6801 (2 MIC CONN)

CON_DMIC_PWR
CON_DMIC_SDA1
CON_DMIC_CLK

PCH_VSS_NCTF<19>
PCH_VSS_NCTF<19>

J4600 (LEFT USB CONN)

PP5V_S3_LTUSB_A_F
USB_LT1_N
USB_LT1_P

FUNC_TEST
GND
GND
GND — 6 TPs

U1000 CHARZ TPS

PCIE_TBT_D2R_P<0> — PP0700
PCIE_TBT_D2R_N<0> — PP0701
DMI_S2N_P<0> — PP0702
DMI_S2N_N<0> — PP0703
DMI_CLK100M_CPU_P — PP0721
DMI_CLK100M_CPU_N — PP0722

U1800 CHARZ TPS

DMI_N2S_P<0> — PP0704
DMI_N2S_N<0> — PP0705
FDI_DATA_P<0> — PP0706
FDI_DATA_N<0> — PP0707
FDI_DATA_P<4> — PP0708
FDI_DATA_N<4> — PP0709
PCIE_AP_D2R_P — PP0710
PCIE_AP_D2R_N — PP0711
PCIE_ENET_D2R_P — PP0712
PCIE_ENET_D2R_N — PP0713
PCIE_CLK100M_TBT_P — PP0723
PCIE_CLK100M_TBT_N — PP0724

U4900 CHARZ TPS

LPC_AD<0> — PP0714
LPC_AD<1> — PP0715
LPC_AD<2> — PP0716
LPC_AD<3> — PP0717
LPC_FRAME_L — PP0718
LPC_CLK33M_SMC — PP0719

AUD_DMIC_SDA1 — PP0720

J6701 (AUDIO JACK CONN)

AUD_CONN_SLEEVE
AUD_CONN_MIC_XW
AUD_CONN_SLEEVE_XW
AUD_CONN_HP_LEFT
AUD_CONN_TIPDET_INV
PP3V3_S0
AUD_SPDIF_OUT_JACK
AUD_CONN_HP_RIGHT
AUD_CONN_TYPEDET
AUD_CONN_MIC

J6802 (AUDIO LEFT SPEAKER CONN)

SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
SPKRCONN_L_ID
SPKRCONN_SL_OUT_P
SPKRCONN_SL_OUT_N

J6803 (AUDIO RIGHT SPEAKER CONN)

SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
SPKRCONN_R_ID
SPKRCONN_SR_OUT_P
SPKRCONN_SR_OUT_N
GND

J9000 (EDP CONN)

PP5VR3V3_SW_LCD
PPVOUT_S0_LCDBKLT — 2 TP needed
LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1
LCD_HPD_CONN
DP_INT_AUX_P
DP_INT_AUX_N

J3401 & J3402 (AIRPORT/BT/CAMERA CONN)

PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_CONN_N
AP_CLKREQ_Q_L
PCIE_WAKE_L
AP_RESET_CONN_L
PP3V3_WLAN_F
PP5V_S3_ALSCAMERA_F
SMBUS_SMC_2_S3_SDA
SMBUS_SMC_2_S3_SCL
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N

J5713 (KEY BOARD CONN)

PP3V3_S4
PP3V42_G3H
WS_KBD1
WS_KBD2
WS_KBD3
WS_KBD4
WS_KBD5
WS_KBD6
WS_KBD7
WS_KBD8
WS_KBD9
WS_KBD10
WS_KBD11
WS_KBD12
WS_KBD13
WS_KBD14
WS_KBD15_CAP
WS_KBD16_NUM
WS_KBD17
WS_KBD18
WS_KBD19
WS_KBD20
WS_KBD21
WS_KBD22
WS_KBD23
WS_KBD_ONOFF_L
WS_LEFT_SHIFT_KBD
WS_LEFT_OPTION_KBD
WS_CONTROL_KBD

J5700 (IPD FLEX CONN)

PP3V3_S4
Z2_CS_L
Z2_MOSI
Z2_MISO
Z2_SCLK
Z2_HOST_INTN
PP5V_S4_CUMULUS
Z2_CLKIN
SMBUS_SMC_2_S3_SCL
SMBUS_SMC_2_S3_SDA
PSOC_SCLK
PSOC_MOSI
PSOC_MISO
PICKB_L
PSOC_F_CS_L
Z2_KEY_ACT_L

J6900 (DC POWER CONN)

TDM_ONEWIRE_MPM
ADAPTER_SENSE
PP18V5_DCIN_FUSE
GND

J4500 (SSD/HDD FLEX CONN)

PP3V3_S0_SSD_FLT
SMC_OOB1_TX_L
SMC_OOB1_RX_L
PP5V_S0_HDD_FLT
GND

FUNC_TEST
BKLT_EN
LCD_BKLT_PWM
PM_CLKRUN_L
PM_SYSRST_L
SMC_ONOFF_L

J5100 (LPC + SPI CONN)

PP3V42_G3H
PP5V_S0
LPC_CLK33M_LPCPLUS
LPC_AD<0>
LPC_AD<2>
LPC_AD<1>
LPC_AD<3>
SPI_ALT_MOSI
LPCPLUS_GPIO
LPCPLUS_RESET_L
SMC_TDO
TP_SMC_TRST_L
TP_SMC_MD1
SMC_TX_L
SPI_ALT_MISO
LPC_FRAME_L
SPIROM_USE_MLB
PM_CLKRUN_L
SPI_ALT_CLK
SPI_ALT_CS_L
LPC_SERIRQ
LPC_PWRDWN_L
SMC_TDI
SMC_TCK
SMC_RESET_L
SMC_ROMBOOT
SMC_RX_L
SMC_TMS

POWER RAILS

FUNC_TEST

PM_SLP_S3_L
PP0V75_S0_DDRVTT
PP1V05_S0
LED_RETURN_2
LED_RETURN_3
LED_RETURN_4
LED_RETURN_5
LED_RETURN_6
GND — 4 TPs
PP3V3_S0
PP3V3_S3
PP3V3_S5
PP3V3_S5_AVREF_SMC
PP3V42_G3H
PP5V_S0
PP5V_S3
PP5V_S5
PPBUS_G3H
PPDCIN_G3H
PPVCORE_S0_CPU
PPVTTDDR_S3
DMI_S2N_P<3..1>
DMI_S2N_N<3..1>
DMI_N2S_P<3..1>
DMI_N2S_N<3..1>

TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0_R
TBTBPWRSW_ISET_S3
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTAPWRSW_ISET_S3_R

TBT_A_R2D_C_P<1..0>
TBT_A_R2D_C_N<1..0>
TBT_A_R2D_P<1..0>
TBT_A_R2D_N<1..0>
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_B_R2D_C_P<1..0>
TBT_B_R2D_C_N<1..0>
TBT_B_R2D_P<1..0>
TBT_B_R2D_N<1..0>
TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>
TBT_B_D2R_C_P<1>
TBT_B_D2R_C_N<1>
TBT_B_D2R_P<0>
TBT_B_D2R_N<0>
TBT_B_D2R_P<1>
TBT_B_D2R_N<1>

PCIE_AP_D2R_P
PCIE_AP_D2R_N
PCIE_AP_R2D_P
PCIE_AP_R2D_N

ICT Test Points

CPU NO_TESTs

TP_TBT_MONDC0 — NC_TBT_MONDC0
TP_TBT_MONDC1 — NC_TBT_MONDC1
TP_TBT_PCIE_RESET0_L — NC_TBT_PCIE_RESET0_L
TP_TBT_PCIE_RESET1_L — NC_TBT_PCIE_RESET1_L
TP_TBT_PCIE_RESET2_L — NC_TBT_PCIE_RESET2_L
TP_TBT_PCIE_RESET3_L — NC_TBT_PCIE_RESET3_L
TP_TBT_XTAL25OUT — NC_TBT_XTAL25OUT

TP_DP_TBTSRC_ML_CP<3> — NC_DP_TBTSRC_ML_CP<3>
TP_DP_TBTSRC_ML_CN<3> — NC_DP_TBTSRC_ML_CN<3>
TP_DP_TBTSRC_ML_CP<2> — NC_DP_TBTSRC_ML_CP<2>
TP_DP_TBTSRC_ML_CN<2> — NC_DP_TBTSRC_ML_CN<2>
TP_DP_TBTSRC_ML_CP<1> — NC_DP_TBTSRC_ML_CP<1>
TP_DP_TBTSRC_ML_CN<1> — NC_DP_TBTSRC_ML_CN<1>
TP_DP_TBTSRC_ML_CP<0> — NC_DP_TBTSRC_ML_CP<0>
TP_DP_TBTSRC_ML_CN<0> — NC_DP_TBTSRC_ML_CN<0>
TP_DP_TBTSRC_AUXCH_CP — NC_DP_TBTSRC_AUXCH_CP
TP_DP_TBTSRC_AUXCH_CN — NC_DP_TBTSRC_AUXCH_CN

TP_SPI_CS1_L — NC_SPI_CS1_L
TP_PCH_GPIO8 — NC_PCH_GPIO8
TP_PCH_STRP_BBS1 — NC_PCH_STRP_BBS1
TP_PCH_STRP_ESI_L — NC_PCH_STRP_ESI_L
TP_PCH_TP23 — NC_PCH_TP23
TP_PCI_CLK33M_OUT2 — NC_PCI_CLK33M_OUT2
TP_PCIE_CLK100M_PEGAN — NC_PCIE_CLK100M_PEGAN
TP_PCIE_CLK100M_PEGAP — NC_PCIE_CLK100M_PEGAP
TP_PM_SLP_A_L — NC_PM_SLP_A_L
TP_PPVOUT_PCH_DCPSUSBYP — NC_PPVOUT_PCH_DCPSUSBYP
TP_SMC_MPM5_LED_PWR — NC_SMC_MPM5_LED_PWR
TP_SMC_MPM5_LED_CHG — NC_SMC_MPM5_LED_CHG
TP_SMS_INT2 — NC_SMS_INT2

PCIE_TBT_R2D_C_P<3..0>
PCIE_TBT_R2D_C_N<3..0>
PCIE_TBT_R2D_P<3..0>
PCIE_TBT_R2D_N<3..0>
PCIE_TBT_D2R_P<3..1>
PCIE_TBT_D2R_N<3..1>
PCIE_TBT_D2R_C_P<3..1>
PCIE_TBT_D2R_C_N<3..1>

MEM_A_DQ<0>
MEM_A_DQ<12..2>
MEM_A_DQ<19..14>
MEM_A_DQ<24..21>
MEM_A_DQ<32..26>
MEM_A_DQ<42..34>
MEM_A_DQ<54..44>
MEM_A_DQ<56>
MEM_A_DQ<63..58>
MEM_B_DQ<2..0>
MEM_B_DQ<13..4>
MEM_B_DQ<19..15>
MEM_B_DQ<25..21>
MEM_B_DQ<35..27>
MEM_B_DQ<40..37>
MEM_B_DQ<47..42>
MEM_B_DQ<57..49>
MEM_B_DQ<63..59>
NC_MEM_EVENT_L

HDMI_IG_CLK_C_P
HDMI_IG_CLK_C_N
HDMI_IG_DATA_C_P<2..0>
HDMI_IG_DATA_C_N<2..0>

PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
USB3_EXTB_TX_C_P
USB3_EXTB_TX_C_N

TP_XDP_PCH_HOOK4 — NC_XDP_PCH_HOOK4
TP_XDP_PCH_HOOK5 — NC_XDP_PCH_HOOK5
TP_XDP_PCH_OBSFN_B<0> — NC_XDP_PCH_OBSFN_B<0>
TP_XDP_PCH_OBSFN_B<1> — NC_XDP_PCH_OBSFN_B<1>
TP_XDP_PCH_OBSFN_A<0> — NC_XDP_PCH_OBSFN_A<0>
TP_XDP_PCH_OBSFN_A<1> — NC_XDP_PCH_OBSFN_A<1>
TP_XDP_PCH_OBSFN_D<0> — NC_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_D<1> — NC_XDP_PCH_OBSFN_D<1>
TP_XDP_PCH_TRST_L — NC_XDP_PCH_TRST_L

TP_1V05_S0_PCH_VCCAPLLEXP — NC_1V05_S0_PCH_VCCAPLLEXP
TP_AUD_CODEC_MICBIAS — NC_AUD_CODEC_MICBIAS
TP_AUD_MIC_INRP — NC_AUD_MIC_INRP
TP_AUD_MIC_INRN — NC_AUD_MIC_INRN
AUD_SPDIF_IN — AUD_SPDIF_IN
TP_BKL_FAULT — NC_BKL_FAULT
TP_LPC_DREQ0_L — NC_LPC_DREQ0_L

S2 CAMERA PCIE SIGNALS

NC_PCIE_CAMERA_D2RP — PCIE_EXCARD_D2R_N
NC_PCIE_CAMERA_D2RN — PCIE_EXCARD_D2R_P
NC_PCIE_CAMERA_R2D_CN — PCIE_EXCARD_R2D_C_N
NC_PCIE_CAMERA_R2D_CP — PCIE_EXCARD_R2D_C_P
NC_PCIE_CLK100M_CAMERAN — PCIE_CLK100M_EXCARD_N
NC_PCIE_CLK100M_CAMERAP — PCIE_CLK100M_EXCARD_P

NO_TEST NC NO_TESTs

NC_PCIE_5_D2RN
NC_PCIE_5_D2RP
NC_PCIE_5_R2D_CN
NC_PCIE_5_R2D_CP
NC_PCIE_6_D2RN
NC_PCIE_6_D2RP
NC_PCIE_6_R2D_CN
NC_PCIE_6_R2D_CP
NC_PCIE_7_D2RN
NC_PCIE_7_D2RP
NC_PCIE_7_R2D_CN
NC_PCIE_7_R2D_CP
NC_PCIE_8_D2RN
NC_PCIE_8_D2RP
NC_PCIE_8_R2D_CN
NC_PCIE_8_R2D_CP

TP_PCIE_CLK100M_PE4N — NC_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P — NC_PCIE_CLK100M_PE4P
TP_PCIE_CLK100M_PEBN — NC_PCIE_CLK100M_PEBN
TP_PCIE_CLK100M_PEBP — NC_PCIE_CLK100M_PEBP

TP_SATA_C_D2RN — NC_SATA_C_D2RN
TP_SATA_C_D2RP — NC_SATA_C_D2RP
TP_SATA_C_R2D_CN — NC_SATA_C_R2D_CN
TP_SATA_C_R2D_CP — NC_SATA_C_R2D_CP
TP_SATA_D_D2RN — NC_SATA_D_D2RN
TP_SATA_D_D2RP — NC_SATA_D_D2RP
TP_SATA_D_R2D_CN — NC_SATA_D_R2D_CN
TP_SATA_D_R2D_CP — NC_SATA_D_R2D_CP
TP_SATA_E_D2RN — NC_SATA_E_D2RN
TP_SATA_E_D2RP — NC_SATA_E_D2RP
TP_SATA_E_R2D_CN — NC_SATA_E_R2D_CN
TP_SATA_E_R2D_CP — NC_SATA_E_R2D_CP
TP_SATA_F_D2RN — NC_SATA_F_D2RN
TP_SATA_F_D2RP — NC_SATA_F_D2RP
TP_SATA_F_R2D_CN — NC_SATA_F_R2D_CN
TP_SATA_F_R2D_CP — NC_SATA_F_R2D_CP

TP_CRT_IG_BLUE — NC_CRT_IG_BLUE
TP_CRT_IG_GREEN — NC_CRT_IG_GREEN
TP_CRT_IG_RED — NC_CRT_IG_RED
TP_CRT_IG_DDC_CLK — NC_CRT_IG_DDC_CLK
TP_CRT_IG_DDC_DATA — NC_CRT_IG_DDC_DATA
TP_CRT_IG_HSYNC — NC_CRT_IG_HSYNC
TP_CRT_IG_VSYNC — NC_CRT_IG_VSYNC

TP_HDA_SDIN1 — NC_HDA_SDIN1
TP_HDA_SDIN2 — NC_HDA_SDIN2
TP_HDA_SDIN3 — NC_HDA_SDIN3

TP_SDVO_TVCLKINN — NC_SDVO_TVCLKINN
TP_SDVO_TVCLKINP — NC_SDVO_TVCLKINP
TP_SDVO_STALLN — NC_SDVO_STALLN
TP_SDVO_STALLP — NC_SDVO_STALLP
TP_SDVO_INTN — NC_SDVO_INTN
TP_SDVO_INTP — NC_SDVO_INTP

TP_PCI_PME_L — NC_PCI_PME_L
TP_PCI_CLK33M_OUT3 — NC_PCI_CLK33M_OUT3

NC_ISNS_LCDBKLTN
NC_ISNS_LCDBKLTP
NC_ISNS_WLANN
NC_ISNS_WLANP
NC_ISNS_LCD_PANELN
NC_ISNS_LCD_PANELP

PCH ALIASES

NC_LPC_DREQ0_L — TP_LPC_DREQ0_L
NC_LPC_DREQ1_L — TP_LPC_DREQ1_L
TP_CLINK_CLK — NC_CLINK_CLK
TP_CLINK_DATA — NC_CLINK_DATA
TP_CLINK_RESET_L — NC_CLINK_RESET_L

PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N

PCIE_AP_R2D_C_P
PCIE_AP_R2D_C_N
PCIE_AP_D2R_P
PCIE_AP_D2R_N
PCIE_AP_D2R_PI_P
PCIE_AP_D2R_PI_N
PCIE_AP_R2D_PI_P
PCIE_AP_R2D_PI_N

PCIE_CLK100M_PCH_P
PCIE_CLK100M_PCH_N
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N

PCH_CLK100M_SATA_P

PCH_CLK33M_PCIIN

PCIE_CLK100M_SSD_P
PCIE_CLK100M_SSD_N
PEG_CLK100M_P
PEG_CLK100M_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_FW_P
PCIE_CLK100M_FW_N
PCIE_CLK100M_EXCARD_P
PCIE_CLK100M_EXCARD_N

SATA_HDD_R2D_RDRIN_P
SATA_HDD_R2D_RDRIN_N
SATA_HDD_D2R_RDROUT_P
SATA_HDD_D2R_RDROUT_N
SATA_HDD_D2R_RDRIN_P
SATA_HDD_D2R_RDRIN_N
SATA_HDD_R2D_RDROUT_P
SATA_HDD_R2D_RDROUT_N
SATA_HDD_D2R_RC_P
SATA_HDD_D2R_RC_N
SATA_HDD_R2D_RC_P

SATA_HDD_R2D_C_P
SATA_HDD_R2D_C_N
SATA_HDD_D2R_P
SATA_HDD_D2R_N

SATA_SSDRHDD_D2R_P
SATA_SSDRHDD_D2R_N
SATA_SSDRHDD_R2D_P
SATA_SSDRHDD_R2D_N

USB3_EXTA_RX_F_P
USB3_EXTA_RX_F_N
USB3_EXTA_RX_P
USB3_EXTA_RX_N

USB3_EXTA_TX_C_P
USB3_EXTA_TX_C_N
USB3_EXTA_TX_N
USB3_EXTA_RX_N

USB3_EXTB_RX_RC_P
USB3_EXTB_RX_RC_N
USB3_EXTB_RX_P
USB3_EXTB_RX_N

SYNC_MASTER=MASTER — SYNC_DATE=MASTER

PAGE TITLE: Functional / ICT Test

Apple Inc.

DRAWING NUMBER: <SCH_NUM> — SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 7 OF 132
SHEET: 7 OF 80

G3H Rails

=PPBUS_G3H → PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE

- =PPBUS_S0_LCDBKLT
- =PPVIN_S5_HS_OTHER_ISNS_R
- =PPVIN_S5_HS_COMPUTING_ISNS_R
- =PPVIN_SW_TBTBST
- =PPBUS_S0_VSENSE
- =PPBUS_G3H_T25_R

=PPVIN_S5_HS_COMPUTING_ISNS → PPVIN_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE

- =PPVIN_S0_CPUIMVP
- =PPVIN_S3_DDRREG
- =PPVIN_S0_CPUVCCIOS0
- =PPVIN_S0_CPUAXG
- =PPVIN_S0_VCCSAS0

=PPVIN_S5_HS_OTHER_ISNS → PPVIN_S5_HS_OTHER_ISNS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 mm MAKE_BASE=TRUE

- =PPVIN_S5_P5VP3V3

=PP18V5_DCIN_CONN → PPDCIN_G3H
MIN_LINE_WIDTH=0.6 mm VOLTAGE=18.5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE

- =PPDCIN_S5_CHGR

=PP3V42_G3H_REG → PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE

- =PP3V3_S5_LPCPLUS
- =PP3V3_S5_SMC
- =PP3V42_G3H_CHGR
- =PP3V42_G3H_ONEWIREPROT
- =PP3V42_G3H_PWRCTL
- =PP3V42_G3H_SMBUS_SMC_5
- =PP3V42_G3H_SMCUSBMUX
- =PP3V42_G3H_TPAD
- =PPVIN_S5_SMCVREF
- =PPVBAT_G3_SYSCLK

=PP3V42_G3H_BMU
=PP3V42_G3H_AUDIO
=PP3V42_G3H_TDM
=PP3V42_S3_HALL

For PCH RTC Power

=PPVRTC_G3_OUT → PPVRTC_G3H
MIN_LINE_WIDTH=0.3 mm VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE

- =PPVRTC_G3_PCH

5V Rails

=PP5V_S5_LDO → PP5V_S5
MIN_LINE_WIDTH=0.5 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.1 mm MAKE_BASE=TRUE

- =PP5V_S5_P1V5S3RS0FET
- =PP5V_S5_P5VSUSFET
- =PP5V_S5_TPAD

=PP5V_SUS_FET → PP5V_SUS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE

- =PP5V_SUS_PCH

=PP5V_S4_REG → PP5V_S4
MIN_LINE_WIDTH=0.5 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE

- =PP5V_S0_LCD
- =PP5V_S3_LTUSB
- =PP5V_S4_P5VS0FET
- =PP5V_S4_P5VS3FET
- =PP5V_S4_AUDIO
- =PP5V_S4_RIO
- =PP5V_S4_P1V05TBTS0
- =PP5V_S4_TPAD

=PP5V_S3_FET → PP5V_S3
MIN_LINE_WIDTH=0.5 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE

- =PP5V_S3_ISNS
- =PP5V_S3_ALSCAMERA
- =PP5V_S3_DDRREG
- =PP5V_S3_DEBUG_ADC_AVDD
- =PP5V_S3_DEBUG_ADC_DVDD
- =PP5V_S3_DEBUG_ISNS
- =PP5V_S3_MEMRESET

=PP5V_S0_FET → PP5V_S0
MIN_LINE_WIDTH=0.4 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE

- =PP5V_S0_AUDIO_XW

=PP5V_S0_AUDIO

- =PP5V_S0_BKL
- =PP5V_S0_CPUIMVP
- =PP5V_S0_CPUVCCIOS0
- =PP5V_S0_FAN_LT
- =PP5V_S0_FAN_RT
- =PP5V_S0_KBDLED
- =PP5V_S0_LPCPLUS
- =PP5V_S0_PCH
- =PP5V_S0_HDD
- =PP5V_S0_RMC
- =PP5V_S0_VCCSAS0
- =PP5V_S0_VMON

3.3V Rails

=PP3V3_S4_FET → PP3V3_S4
MIN_LINE_WIDTH=0.6 mm VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1 mm MAKE_BASE=TRUE

=PP3V3_S4_TBT
=PP3V3_S4_RIO

- =PP3V3_S4_TPAD
- =PP3V3_S4_SMC
- =PP3V3_S4_BT

=PP3V3_SUS_FET → PP3V3_SUS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE

- =PP3V3_SUS_P1V05SUSLDO
- =PP3V3_SUS_PCH_VCCSUS
- =PP3V3_SUS_PCH_VCCSUS_GPIO
- =PP3V3_SUS_PCH_GPIO
- =PP3V3_SUS_PCH_VCCSUS_USB
- =PP3V3_SUS_CNTRL
- =PP3V3_SUS_SMC

=PP3V3_SUS_PCH
=PP3V3_SUS_ROM
=PP3V3_SUS_PCH_VCC_SPI

=PP3V3_S5_REG → PP3V3_S5
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

- =PP3V3_S0_P3V3S0FET
- =PP3V3_S3_P3V3S3FET
- =PP3V3_S4_TBTAPWRSW
- =PP3V3_S4_TBTBPWRSW
- =PP3V3_S4_P3V3S4FET
- =PP3V3_S5_CPU_VCCDDR
- =PP3V3_S5_P3V3SUSFET
- =PP3V3_S5_PCH
- =PP3V3_S5_PCHPWRGD
- =PP3V3_S5_PCH_GPIO
- =PP3V3_S5_PCH_VCCDSW
- =PP3V3_S5_PWRCTL
- =PP3V3_S5_SMCBATLOW
- =PP3V3_S5_SYSCLK
- =PP3V3_S5_VMON
- =PP3V3_S5_XDP
- =PP3V3_S5_P1V5S0

=PP3V3_S3_FET → PP3V3_S3
MIN_LINE_WIDTH=0.508MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE

- =PP3V3_S3_ISNS
- =PP3V3_S3_MEMRESET
- =PP3V3_S3_PCH_GPIO
- =PP3V3_S3_RIO
- =PP3V3_S3_SMBUS_SMC_2_S3
- =PP3V3_S3_SMBUS_SMC_3
- =PP3V3_S3_USBMUX
- =PP3V3_S3_USB_HUB
- =PP3V3_S3_USB_RESET
- =PP3V3_S3_VREFMRGN
- =PP3V3_S3_WLAN
- =PP3V3_S3_GYRO
- =PP3V3_S3_SMS
- =PP3V3_S3_SDBUF
- =PP3V3_S3_CAMERA
- =PP3V3_S3_P1V2S3
- =PP3V3_S3_P1V8S3
- =PP3V3_S3_BT

=PP3V3_S0_FET → PP3V3_S0
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.075 mm MAKE_BASE=TRUE

- =PP3V3_S0_AUDIO
- =PP3V3_S0_AUDIO_DIG
- =PP3V3_S0_BKL_VDDIO
- =PP3V3_S0_CPUTHMSNS
- =PP3V3_S0_P1V5S0
- =PP3V3_S0_P1V8S0
- =PP3V3_S0_BKLI2C
- =PP3V3_S0_DDCMUX
- =PP3V3_S0_FAN_LT
- =PP3V3_S0_FAN_RT
- =PP3V3_S0_GPUTHMSNS
- =PP3V3_S0_HS_ISNS
- =PP3V3_S0_IMVPISNS
- =PP3V3_S0_ISNS
- =PP3V3_S0_CPU_VCCIO_SEL
- =PP3V3_S0_LCD
- =PP3V3_S0_P3V3TBTFET
- =PP3V3_S0_PCH
- =PP3V3_S0_PCH_GPIO
- =PP3V3_S0_PCH_VCC3_3_CLK
- =PP3V3_S0_PCH_VCC3_3_GPIO
- =PP3V3_S0_PCH_VCC3_3_HVCMOS
- =PP3V3_S0_PCH_VCC3_3_PCI
- =PP3V3_S0_PCH_VCC3_3_SATA
- =PP3V3_S0_PCH_VCCADCAC
- =PP3V3_S0_PCH_VCC3_3
- =PP3V3_S0_PWRCTL
- =PP3V3_S0_RSTBUF
- =PP3V3_S0_SATAMUX
- =PP3V3_S0_SB_PM
- =PP3V3_S0_SMBUS_PCH
- =PP3V3_S0_SMBUS_SMC_0_S0
- =PP3V3_S0_SMBUS_SMC_1_S0
- =PP3V3_S0_SSD
- =PP3V3_S0_SYSCLK
- =PP3V3_S0_TBTI2C
- =PP3V3_S0_TBTPWRCTL
- =PP3V3_S0_HDMI
- =PP3V3_S0_TPAD
- =PP3V3_S0_VMON
- =PP3V3_S0_XDP
- =PP3V3_S0_DDR3THMSNS
- =PP3V3_S0_SPKRTHMSNS
- =PP3V3_S0_HS_COMPUTING_ISNS
- =PP3V3_S0_HS_OTHER_ISNS
- =PP3V3_S0_PCH_STRAPS

1.8V/1.5V/1.2V/1.05V Rails

=PP1V8_S0_REG → PP1V8_S0
2A max supply
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

- =PP1V8R1V5_S0_PCH_VCCVRM
- =PP1V8_S0_AUDIO
- =PP1V8_S0_CPU_VCCPLL
- =PP1V8_S0_PCH_VCC_DFTERM
- =PPVDDIO_S0_SBCLK

=PP1V8_S0_CPU_VCCPLL_R → PP1V8_S0_CPU_VCCPLL_R
MIN_LINE_WIDTH=0.5 MM VOLTAGE=1.8V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

=PPDDR_S3_REG → PP1V5R1V35_S3
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.35V
MAKE_BASE=TRUE

- =PPDDR_S3_MEMVREF
- =PPVIN_S3_P1V5S3RS0_FET
- =PPVIN_S0_DDRREG_LDO
- =PPVIN_S3_MEM_ISNS_R

=PPVIN_S3_MEM_ISNS → PP1V5R1V35_MEM
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.35V
MAKE_BASE=TRUE

- =PP1V5R1V35_S3_MEM_A
- =PP1V5R1V35_S3_MEM_B
- =PP1V5_S3_MEMRESET

=PP1V5_S3RS0_FET → PP1V5_S3RS0_CPUDDR
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

- =PP1V5_S3RS0_VMON
- =PP1V5R1V35_S3_CPU_VCCDDR

=PP1V5_S0_REG → PP1V5_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

- =PP1V5_S0_AUDIO
- =PP3V3R1V5_S0_PCH_VCCSUSHDA
- =PP1V5_S0_RDRVR

=PPVTT_S3_DDR_BUF → PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.675V
MAKE_BASE=TRUE

=PPVTT_S0_DDR_LDO → PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.675V
MAKE_BASE=TRUE

- =PP0V75_S0_MEM_VTT_A
- =PP0V75_S0_MEM_VTT_B
- =PPVTT_S0_VTTCLAMP

=PP1V05_SUS_LDO → PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

- =PP1V05_SUS_PCH_JTAG

=PPCPUVCCIO_S0_REG → PP1V05_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

- =PP1V05_S0_CPU_VCCIO
- =PPVCCIO_S0_XDP
- =PPVCCIO_S0_CPUIMVP
- =PPVCCIO_S0_SMC
- =PP1V05_S0_VMON
- =PP1V05_S0_RMC
- =PP1V05_S0_PCH_VCCIO_PLLPCIE
- =PP1V05_S0_PCH_VCCADPLL
- =PP1V05_S0_PCH_VCCIO
- =PP1V05_S0_PCH_VCCIO_PCIE
- =PP1V05_S0_PCH_VCCIO_SATA
- =PP1V05_S0_PCH_VCCIO_CLK
- =PP1V05_S0_PCH_VCCIO_USB
- =PP1V05_S0_PCH_VCC_CORE
- =PP1V05_S0_PCH_VCCASW
- =PP1V05_S0_PCH_VCCIO_CLK
- =PP1V05_S0_PCH_VCCDIFFCLK
- =PP1V05_S0_PCH
- =PP1V05_S0_PCH_VCCSSC
- =PP1V05_S0_PCH_V_PROC_IO
- =PP1V05_S0_PCH_VCCIO_PLLUSB
- =PP1V05_S0_PCH_VCC_DMI
- =PP1V05_S0_PCH_VCCIO_PLLFDI
- =PP1V05_S0_PCH_VCCDMI_FDI

=PPBUS_G3H_T25 → PPBUS_G3H_T25_PWR
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

Backlight Rails

=PPBUS_SW_BKL → PPBUS_SW_BKL
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

- =PPBUS_S0_LCDBKLT_PWR

=PP18V5_DCIN_ISOL → PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.3 MM VOLTAGE=18.5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

- =PPDCIN_S5_CHGR_ISOL
- =PPDCIN_S5_VSENSE

TBT Rails (off when no cable)

=PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.25 mm
VOLTAGE=12.8V

=PP15V_TBT_REG → PP15V_TBT
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

- =PPHV_SW_TBTAPWRSW
- =PPHV_SW_TBTBPWRSW

=PP3V3_TBTLC_FET → PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_TBT_PCH_GPIO
- =PP3V3_TBTLC_RTR
- =PPVDDIO_TBT_CLK
- =PP3V3_TBT_PCH_GPIO

=PP1V05_S0_P1V05TBTREG_R → PP1V05_S0_P1V05TBTREG_R
MIN_LINE_WIDTH=0.4 mm VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE

=PP1V05_S0_P1V05TBTREG → PP1V05_S0_P1V05TBTREG
MIN_LINE_WIDTH=0.4 mm VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE

- =PP1V05_TBTLC_RTR
- =PP1V05_TBTLC

=PP1V05_TBTCIO_FET → PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

- =PP1V05_TBTCIO_RTR

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG → PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.25V

- =PPVCORE_S0_CPU

=PPVCORE_S0_AXG_REG → PPVCORE_S0_AXG
MIN_LINE_WIDTH=0.6 mm MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.05V

- =PPVCORE_S0_CPU_VCCAXG

=PP1V5_S3_CPU_VCCDQ → PP1V5_S3_CPU_VCCDQ
MIN_LINE_WIDTH=0.6 mm MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.5V

=PP1V05_S0_CPU_VCCPQE → PP1V05_S0_CPU_VCCPQE
MIN_LINE_WIDTH=0.6 mm VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE

=PPVCCSA_S0_REG → PPVCCSA_S0_REG
MIN_LINE_WIDTH=0.6 mm VOLTAGE=0.9V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE

- =PPVCCSA_S0_CPU

SYNC_MASTER=MASTER SYNC_DATE=MASTER
PAGE TITLE: Power Aliases

Apple Inc.

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Frame Holes

ZT0940
4P5R2P3-3P5B

ZT0960
4P5R2P3-3P5B

Bosses for limiting deflection

SH0910
2.8OD1.2ID-2.25H-SM-D1 APN:860-1557

SH0911
2.8OD1.2ID-2.25H-SM-D1

SH0912
2.8OD1.2ID-2.25H-SM-D1

SH0913
2.8OD1.2ID-2.25H-SM-D1

SH0950
SM
SHLD-D1-USB

SH0951
SM
SHLD-D1-MLB-T29

D1 THERMAL MODULE STANDOFF (860-1439)

SH0920
STDOFF-4.50D2.15H-SM

SH0921
STDOFF-4.50D2.15H-SM

SH0926
STDOFF-4.50D2.15H-SM

SH0927
STDOFF-4.50D2.15H-SM

D1 BMU MODULE STANDOFFS

SH0928
STDOFF-4.50D1.73H-SM
APN: 860-1490

SH0963
STDOFF-4.50D2.33H-SM

SH0963 is BMU standoff with flange. 860-1534

TH0900 for upper TBT can gnd slot

TH0903 for lower TBT can gnd slot

TH0904,5 for USB can gnd slot

FAN BOSSES (4X 860-1327)

SH0922
STDOFF-4.50D1.8H-SM

SH0923
STDOFF-4.50D1.8H-SM

SH0924
STDOFF-4.50D1.8H-SM

SH0925
STDOFF-4.50D1.8H-SM

D1 POGO PINS (870-2451)

SH0932
POGO-2.3OD-5.5H-SM-LOW-FORCE

SH0933
POGO-2.3OD-4.1H-SM-LOW-FORCE

SH0934
POGO-2.3OD-5.5H-SM-LOW-FORCE

SH0935
POGO-2.3OD-5.5H-SM-LOW-FORCE

SH0936
POGO-2.3OD-5.5H-SM-LOW-FORCE

SH0937
POGO-2.3OD-5.5H-SM-LOW-FORCE

D1 ELIPTICAL SLOT HOLES

ZT0930
SL-3.9X2.3-4.2x2.6

ZT0920
SL-2.8X1.8-3.1x2.1

ZT0931
SL-3.9X2.3-4.2x2.6

TH0900
SL-1.1X0.5-1.4x0.8

TH0903
SL-1.1X0.5-1.4x0.8

TH0904
SL-1.1X0.45-1.4x0.75

TH0905
SL-1.1X0.45-1.4x0.75

APN:862-0118

APN:998-3975

MLB_RAMCFG0 — RAMCFG0:L R0910 1K 5% 1/20W MF 2012
MLB_RAMCFG1 — RAMCFG1:L R0911 1K 5% 1/20W MF 2012
MLB_RAMCFG2 — RAMCFG2:L R0912 1K 5% 1/20W MF 2012
MLB_RAMCFG3 — RAMCFG3:L R0913 1K 5% 1/20W MF 2012

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

Digital Ground

=PP5V_S0_AUDIO_XW

XW0902 SM — PP5V_S0_AUDIO_AMP_L
XW0903 SM — PP5V_S0_AUDIO_AMP_R
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

eDP signals

DP_INT_AUX_C_P	MAKE_BASE=TRUE	TP_EDP_AUX_P
DP_INT_AUX_C_N	MAKE_BASE=TRUE	TP_EDP_AUX_N
DP_INT_ML_C_P<3..0>	MAKE_BASE=TRUE	TP_EDP_TX_P<3..0>
DP_INT_ML_C_N<3..0>	MAKE_BASE=TRUE	TP_EDP_TX_N<3..0>

LCD_BKLT_PWM	MAKE_BASE=TRUE	LVDS_IG_BKL_PWM
LCD_BKLT_EN	MAKE_BASE=TRUE	LVDS_IG_BKL_ON
LCD_PWR_EN	MAKE_BASE=TRUE	LVDS_IG_PANEL_PWR

CR SFF DG v1p0 Table 3-56 mapping for HDMI

HDMI_IG_CLK_C_P	MAKE_BASE=TRUE	TP_DP_IG_B_MLP<3>
HDMI_IG_CLK_C_N	MAKE_BASE=TRUE	TP_DP_IG_B_MLN<3>
HDMI_IG_DATA_C_P<2..0>	MAKE_BASE=TRUE	TP_DP_IG_B_MLP<0..2>
HDMI_IG_DATA_C_N<2..0>	MAKE_BASE=TRUE	TP_DP_IG_B_MLN<0..2>
HDMI_IG_DDC_CLK	MAKE_BASE=TRUE	DPA_IG_DDC_CLK
HDMI_IG_DDC_DATA	MAKE_BASE=TRUE	DPA_IG_DDC_DATA
HDMI_HPD	MAKE_BASE=TRUE	DPA_IG_HPD

DP_TBTSNK0_AUXCH_C_P	MAKE_BASE=TRUE	DPB_IG_AUX_CH_P
DP_TBTSNK0_AUXCH_C_N	MAKE_BASE=TRUE	DPB_IG_AUX_CH_N
DP_TBTSNK0_ML_C_P<3..0>	MAKE_BASE=TRUE	TP_DP_IG_C_MLP<3..0>
DP_TBTSNK0_ML_C_N<3..0>	MAKE_BASE=TRUE	TP_DP_IG_C_MLN<3..0>
DP_TBTSNK0_DDC_CLK	MAKE_BASE=TRUE	DPB_IG_DDC_CLK
DP_TBTSNK0_DDC_DATA	MAKE_BASE=TRUE	DPB_IG_DDC_DATA
DP_TBTSNK0_HPD	MAKE_BASE=TRUE	DPB_IG_HPD
DP_TBTSNK1_AUXCH_C_P	MAKE_BASE=TRUE	TP_DP_IG_D_AUXP
DP_TBTSNK1_AUXCH_C_N	MAKE_BASE=TRUE	TP_DP_IG_D_AUXN
DP_TBTSNK1_ML_C_P<3..0>	MAKE_BASE=TRUE	TP_DP_IG_D_MLP<3..0>
DP_TBTSNK1_ML_C_N<3..0>	MAKE_BASE=TRUE	TP_DP_IG_D_MLN<3..0>
DP_TBTSNK1_DDC_CLK	MAKE_BASE=TRUE	TP_DP_IG_D_CTRL_CLK
DP_TBTSNK1_DDC_DATA	MAKE_BASE=TRUE	TP_DP_IG_D_CTRL_DATA
DP_TBTSNK1_HPD	MAKE_BASE=TRUE	TP_DP_IG_D_HPD

NC_PCH_GPIO64_CLKOUTFLEX0	TRUE MAKE_BASE=TRUE	TP_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1	TRUE MAKE_BASE=TRUE	TP_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2	TRUE MAKE_BASE=TRUE	TP_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3	TRUE MAKE_BASE=TRUE	TP_PCH_GPIO67_CLKOUTFLEX3

CPU signals

MEMVTT_EN	MAKE_BASE=TRUE	=DDRVTT_EN

T29 Signals Through PEG

PCIE_TBT_D2R_P<3..0>	MAKE_BASE=TRUE	=PEG_D2R_P<11..8>
PCIE_TBT_D2R_N<3..0>	MAKE_BASE=TRUE	=PEG_D2R_N<11..8>
PCIE_TBT_R2D_C_P<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<11..8>
PCIE_TBT_R2D_C_N<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<11..8>

SD_PWR_EN_PCH	MAKE_BASE=TRUE	ENET_LOW_PWR_PCH
SD_PWR_EN	MAKE_BASE=TRUE	ENET_LOW_PWR
TP_FW_PWR_EN	MAKE_BASE=TRUE	FW_PWR_EN

Unused PEG signals

NC_PEG_D2RP<15..12>	MAKE_BASE=TRUE NO_TEST=TRUE	=PEG_D2R_P<15..12>
NC_PEG_D2RN<15..12>	MAKE_BASE=TRUE NO_TEST=TRUE	=PEG_D2R_N<15..12>
NC_PEG_R2D_CP<15..12>	MAKE_BASE=TRUE NO_TEST=TRUE	=PEG_R2D_C_P<15..12>
NC_PEG_R2D_CN<15..12>	MAKE_BASE=TRUE NO_TEST=TRUE	=PEG_R2D_C_N<15..12>

Unused GPU signals

NC_PEG_D2RP<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE	=PEG_D2R_P<7..0>
NC_PEG_D2RN<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE	=PEG_D2R_N<7..0>
NC_PEG_R2D_CP<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE	=PEG_R2D_C_P<7..0>
NC_PEG_R2D_CN<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE	=PEG_R2D_C_N<7..0>

NC_DPA_IG_AUX_CHP	MAKE_BASE=TRUE NO_TEST=TRUE	DPA_IG_AUX_CH_P
NC_DPA_IG_AUX_CHN	MAKE_BASE=TRUE NO_TEST=TRUE	DPA_IG_AUX_CH_N

NC_PEG_CLK100MN	MAKE_BASE=TRUE NO_TEST=TRUE	PEG_CLK100M_N
NC_PEG_CLK100MP	MAKE_BASE=TRUE NO_TEST=TRUE	PEG_CLK100M_P

UNUSED USB SIGNALS

NC_USB3_EXTC_TXP	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTC_TX_P
NC_USB3_EXTC_TXN	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTC_TX_N
NC_USB3_EXTC_RXP	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTC_RX_P
NC_USB3_EXTC_RXN	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTC_RX_N
NC_USB_EXTCP	MAKE_BASE=TRUE NO_TEST=TRUE	USB_EXTC_P
NC_USB_EXTCN	MAKE_BASE=TRUE NO_TEST=TRUE	USB_EXTC_N
NC_USB3_EXTD_TXP	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTD_TX_P
NC_USB3_EXTD_TXN	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTD_TX_N
NC_USB3_EXTD_RXP	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTD_RX_P
NC_USB3_EXTD_RXN	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTD_RX_N
NC_USB_EXTD_EHCIP	MAKE_BASE=TRUE NO_TEST=TRUE	USB_EXTD_EHCI_P
NC_USB_EXTD_EHCIN	MAKE_BASE=TRUE NO_TEST=TRUE	USB_EXTD_EHCI_N
NC_USB_4N	MAKE_BASE=TRUE NO_TEST=TRUE	TP_USB_4N
NC_USB_4P	MAKE_BASE=TRUE NO_TEST=TRUE	TP_USB_4P
NC_USB_SDN	MAKE_BASE=TRUE NO_TEST=TRUE	TP_USB_SDN
NC_USB_SDP	MAKE_BASE=TRUE NO_TEST=TRUE	TP_USB_SDP
NC_USB_WLANN	MAKE_BASE=TRUE NO_TEST=TRUE	TP_USB_WLANN
NC_USB_WLANP	MAKE_BASE=TRUE NO_TEST=TRUE	TP_USB_WLANP
NC_USB_BT_HSN	MAKE_BASE=TRUE NO_TEST=TRUE	TP_USB_BT_HSN
NC_USB_BT_HSP	MAKE_BASE=TRUE NO_TEST=TRUE	TP_USB_BT_HSP
NC_USB_12N	MAKE_BASE=TRUE NO_TEST=TRUE	TP_USB_12N
NC_USB_12P	MAKE_BASE=TRUE NO_TEST=TRUE	TP_USB_12P
NC_USB_13N	MAKE_BASE=TRUE NO_TEST=TRUE	TP_USB_13N
NC_USB_13P	MAKE_BASE=TRUE NO_TEST=TRUE	TP_USB_13P

USB SIGNALS

USB_BT_P	MAKE_BASE=TRUE	USBHUB_DN1_P
USB_BT_N	MAKE_BASE=TRUE	USBHUB_DN1_N
USB_TPAD_P	MAKE_BASE=TRUE	USBHUB_DN2_P
USB_TPAD_N	MAKE_BASE=TRUE	USBHUB_DN2_N
USB_SMC_P	MAKE_BASE=TRUE	USBHUB_DN3_P
USB_SMC_N	MAKE_BASE=TRUE	USBHUB_DN3_N
PU_USBHUB_DN4_P	MAKE_BASE=TRUE	USBHUB_DN4_P
PU_USBHUB_DN4_N	MAKE_BASE=TRUE	USBHUB_DN4_N

NC_CPU_THERMDN	MAKE_BASE=TRUE NO_TEST=TRUE	CPU_THERMD_N
NC_CPU_THERMDP	MAKE_BASE=TRUE NO_TEST=TRUE	CPU_THERMD_P
NC_LCD_FSS	MAKE_BASE=TRUE NO_TEST=TRUE	LCD_FSS

NC_PCIE_CLK100M_SSDN	MAKE_BASE=TRUE	PCIE_CLK100M_SSD_N
NC_PCIE_CLK100M_SSDP	MAKE_BASE=TRUE	PCIE_CLK100M_SSD_P
NC_PCIE_CLK100M_FWN	MAKE_BASE=TRUE	PCIE_CLK100M_FW_N
NC_PCIE_CLK100M_FWP	MAKE_BASE=TRUE	PCIE_CLK100M_FW_P

NC_PCIE_FW_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE	PCIE_FW_D2R_N
NC_PCIE_FW_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE	PCIE_FW_D2R_P
NC_PCIE_FW_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE	PCIE_FW_R2D_C_N
NC_PCIE_FW_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE	PCIE_FW_R2D_C_P

Unused SATA ODD Signals

NC_SATA_ODD_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE	SATA_ODD_D2R_N
NC_SATA_ODD_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE	SATA_ODD_D2R_P
NC_SATA_ODD_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE	SATA_ODD_R2D_C_N
NC_SATA_ODD_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE	SATA_ODD_R2D_C_P

Unused Memory Signals

NC_MEM_A_CLKP<1>	MAKE_BASE=TRUE NO_TEST=TRUE	MEM_A_CLK_P<1>
NC_MEM_A_CLKN<1>	MAKE_BASE=TRUE NO_TEST=TRUE	MEM_A_CLK_N<1>
NC_MEM_B_CLKP<1>	MAKE_BASE=TRUE NO_TEST=TRUE	MEM_B_CLK_P<1>
NC_MEM_B_CLKN<1>	MAKE_BASE=TRUE NO_TEST=TRUE	MEM_B_CLK_N<1>

=PP3V3_S0_PWRCTL

R0991 10K 5% 1/20W MF 201

Unused PGOOD signal

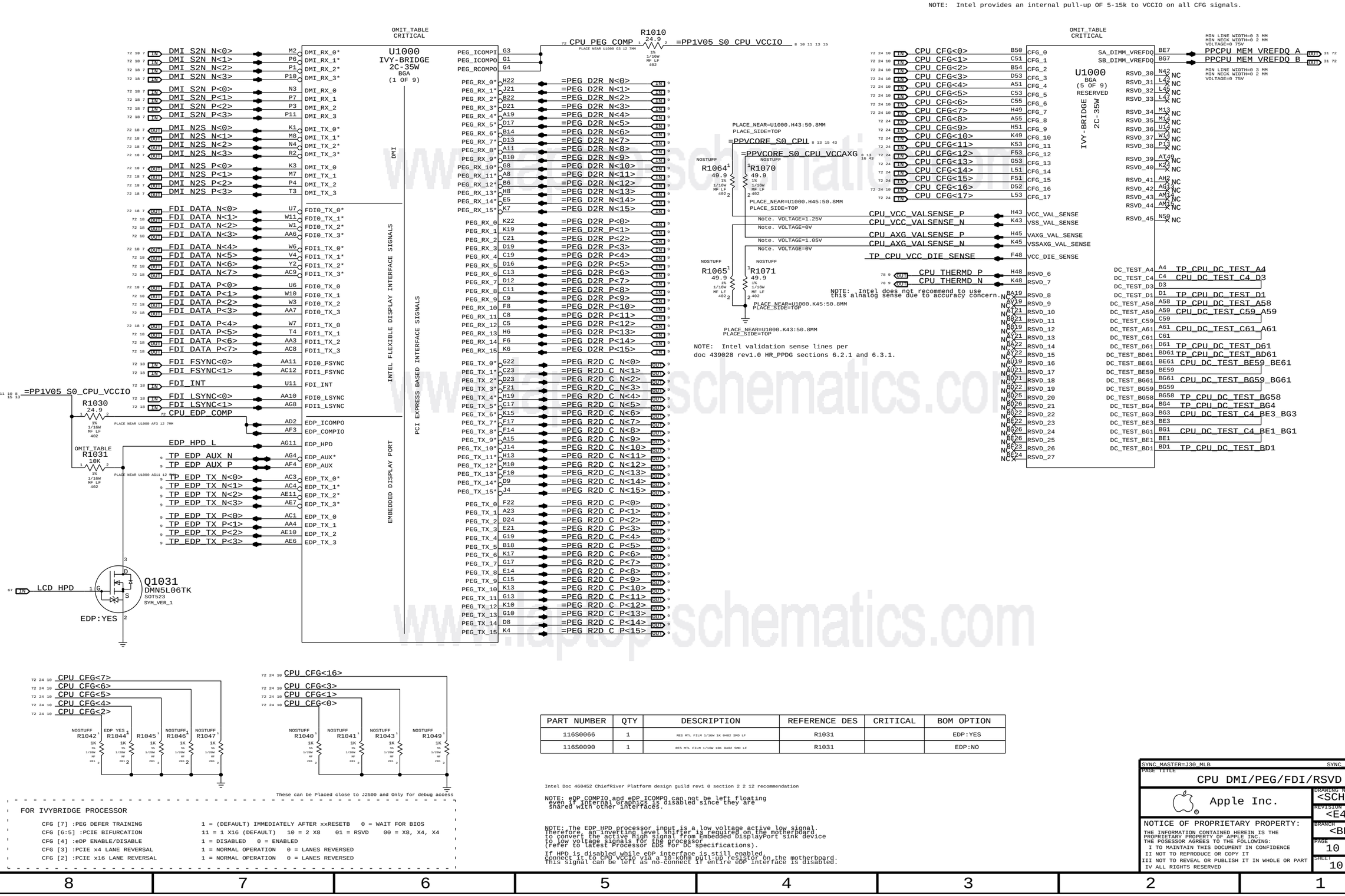
CPUIMVP_AXG_PGOOD

TP_P1V5S3RS0_RAMP_DONE	MAKE_BASE=TRUE	P1V5S3RS0_RAMP_DONE
TP_DDRREG_PGOOD	MAKE_BASE=TRUE	DDRREG_PGOOD

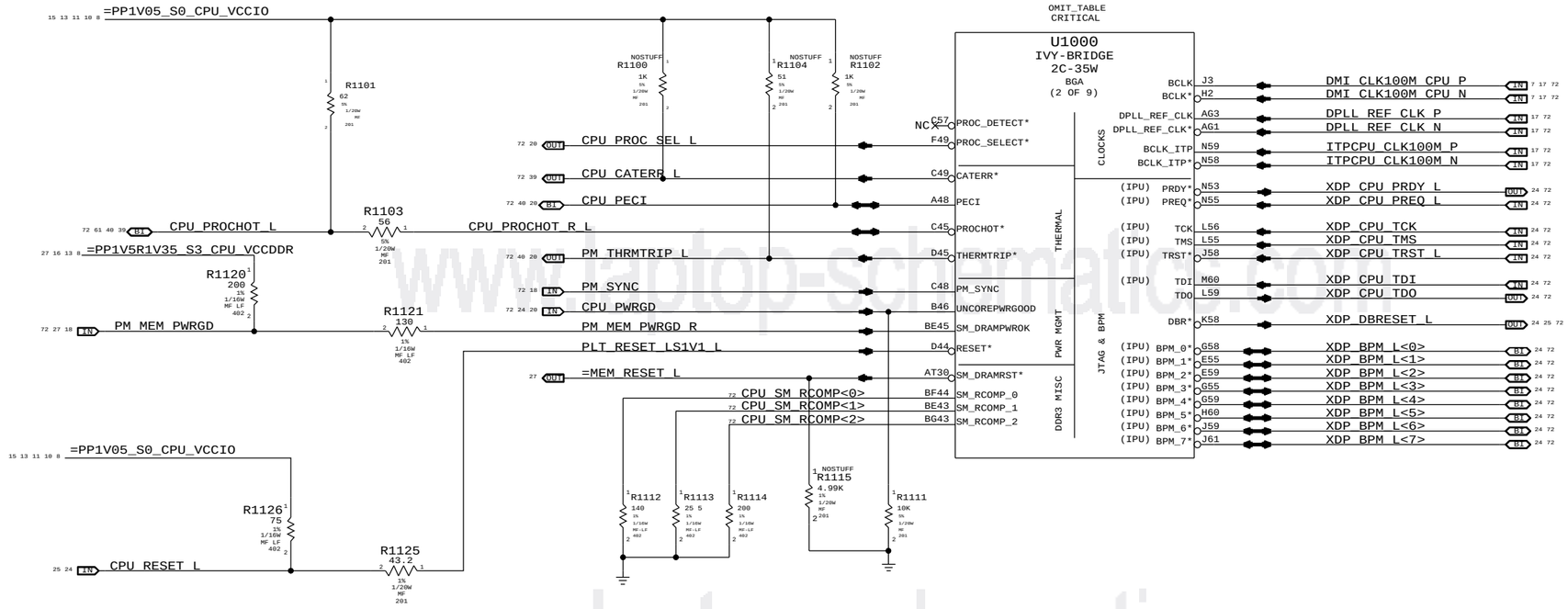
SYNC_MASTER=D1_MLB_TEST
SYNC_DATE=01/27/2012
PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 9 OF 132
SHEET: 9 OF 80



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0066	1	RES MTL FILM 1/16W 1K 0402 SMD LF	R1031		EDP:YES
116S0090	1	RES MTL FILM 1/16W 10K 0402 SMD LF	R1031		EDP:NO



SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2013

PAGE TITLE: CPU CLOCK/MISC/JTAG

Apple Inc.

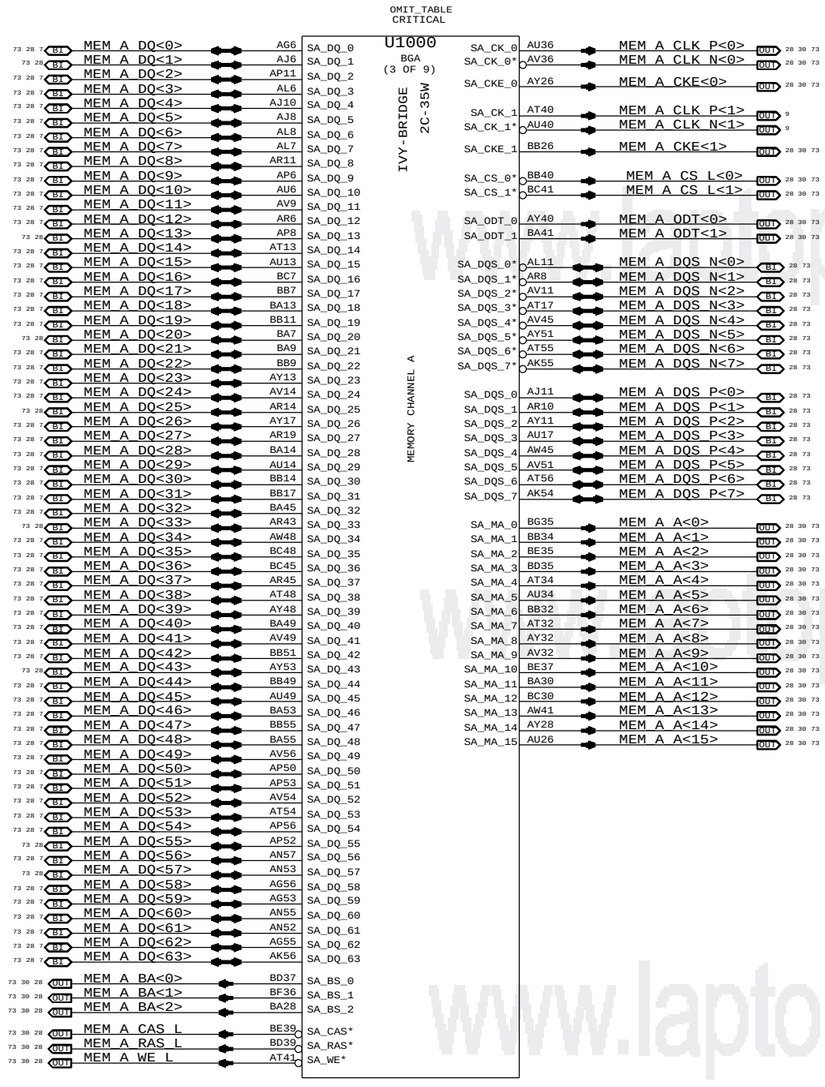
DRAWING NUMBER: <SCH_NUM> SIZE: D

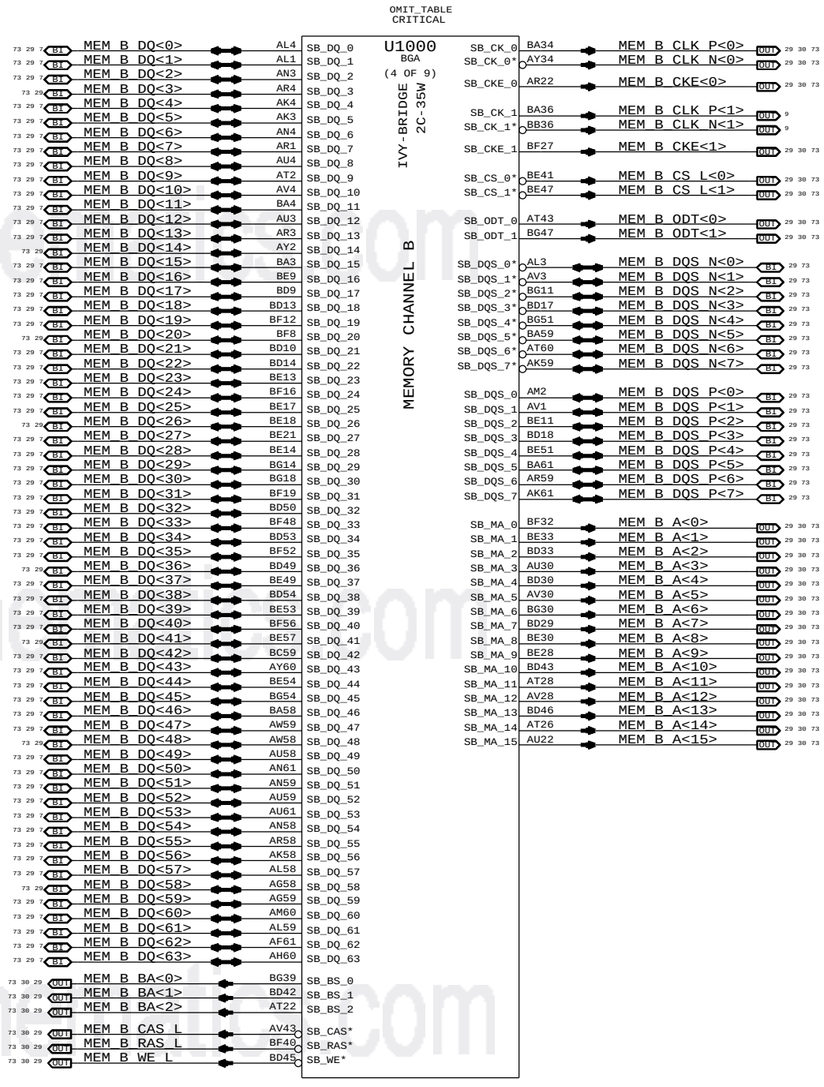
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 11 OF 132

SHEET: 11 OF 80





SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2011

PAGE TITLE

CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 12 OF 132

SHEET 12 OF 80

=PPVCORE_S0_CPU
15 13 10 8 43

OMIT_TABLE
CRITICAL

U1000
BGA
(6 OF 9)
IVY-BRIDGE
2C-35W
CORE SUPLLY
PEG AND DDR

A26	VCC_1	VCCIO_1	AF46
A29	VCC_2	VCCIO_3	AG48
A31	VCC_3	VCCIO_4	AG50
A34	VCC_4	VCCIO_5	AG51
A35	VCC_5	VCCIO_6	AJ17
A38	VCC_6	VCCIO_7	AJ21
A39	VCC_7	VCCIO_8	AJ25
A42	VCC_8	VCCIO_9	AJ43
C26	VCC_9	VCCIO_10	AJ47
C27	VCC_10	VCCIO_11	AK50
C32	VCC_11	VCCIO_12	AK51
C34	VCC_12	VCCIO_13	AL14
C37	VCC_13	VCCIO_14	AL15
C39	VCC_14	VCCIO_15	AL16
C42	VCC_15	VCCIO_16	AL20
D27	VCC_16	VCCIO_17	AL22
D32	VCC_17	VCCIO_18	AL26
D34	VCC_18	VCCIO_19	AL45
D37	VCC_19	VCCIO_20	AL48
D39	VCC_20	VCCIO_21	AM16
D42	VCC_21	VCCIO_22	AM17
E26	VCC_22	VCCIO_23	AM21
E28	VCC_23	VCCIO_24	AM43
E32	VCC_24	VCCIO_25	AM47
E34	VCC_25	VCCIO_26	AN20
E37	VCC_26	VCCIO_27	AN42
E38	VCC_27	VCCIO_28	AN45
F25	VCC_28	VCCIO_29	AN48
F26	VCC_29	VCCIO_30	AA14
F28	VCC_30	VCCIO_31	AA15
F32	VCC_31	VCCIO_32	AB17
F34	VCC_32	VCCIO_33	AB20
F37	VCC_33	VCCIO_34	AC13
F38	VCC_34	VCCIO_35	AD16
F42	VCC_35	VCCIO_36	AD18
G42	VCC_36	VCCIO_37	AD21
H25	VCC_37	VCCIO_38	AE14
H26	VCC_38	VCCIO_39	AE15
H28	VCC_39	VCCIO_40	AF16
H29	VCC_40	VCCIO_41	AF18
H32	VCC_41	VCCIO_42	AF20
H34	VCC_42	VCCIO_43	AG15
H35	VCC_43	VCCIO_44	AG16
H37	VCC_44	VCCIO_45	AG17
H38	VCC_45	VCCIO_46	AG20
H40	VCC_46	VCCIO_47	AG21
J25	VCC_47	VCCIO_48	AJ14
J26	VCC_48	VCCIO_49	AJ15
J28	VCC_49	VCCIO_50	W16
J29	VCC_50	VCCIO_51	W17
J32	VCC_51		
J34	VCC_52	VCCIO_SEL	BC22
J35	VCC_53		
J37	VCC_54	VCCPQE_1	AM25
J38	VCC_55	VCCPQE_2	AN22
J40	VCC_56		
J42	VCC_57	VIDALERT*	A44
K26	VCC_58	VIDSCLK	B43
K27	VCC_59	VIDSOUT	C44
K29	VCC_60		
K32	VCC_61	VCC_SENSE	F43
K34	VCC_62	VSS_SENSE	G43
K35	VCC_63		
K37	VCC_64	VCCIO_SENSE	AN16
K39	VCC_66	VSS_SENSE_VCCIO	AN17
K42	VCC_67		
L25	VCC_68		
L28	VCC_69		
L33	VCC_70		
L36	VCC_71		
L40	VCC_72		
N26	VCC_73		
N30	VCC_74		
N34	VCC_75		
N38	VCC_76		

QUIET RAIL
SVID
SENSE LINES

=PP1V05_S0_CPU_VCCIO
8 10 11 13 15
(NOT controlled by VCCIO SEL)
Fixed at 1 05V

=PP3V3_S0_CPU_VCCIO_SEL
8
NOSTUFF
R1320 10K 5% 1/20W MF 201
IVB supports 1.05V VCCIO.
VCCIO_SEL can be NC.
CPU_VCCIO_SEL

=PP1V05_S0_CPU_VCCPQE
8 15
CPU_VIDALERT_L_R
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_VCCSENSE_P
CPU_VCCSENSE_N
CPU_VCCIOSENSE_P
CPU_VCCIOSENSE_N

R1302 130 1% 1/16W MF LF 402
PLACE_NEAR=U1000.C44:2.54mm
R1300 75 1% 1/20W MF 201
PLACE_NEAR=R1310.2:2.54mm
R1310 43 1/20W 1 2 5% MF
CPU_VIDALERT_L
PLACE_NEAR=U1000.A44:38mm
R1311 0 1/20W 1 2 5% MF
CPU_VIDSCLK
R1312 0 1/20W 1 2 5% MF
CPU_VIDSOUT
61 72

=PPVCORE_S0_CPU
8 10 13 15 43
=PP1V05_S0_CPU_VCCIO
8 10 11 13 15
R1360 100 1% 1/16W MF LF 402
PLACE_NEAR=U1000.F43:50.8mm
PLACE_SIDE=TOP
R1362 100 1% 1/16W MF LF 402
PLACE_NEAR=U1000.AN16:50.8mm
PLACE_SIDE=TOP
Note. VOLTAGE=1.25V
Note. VOLTAGE=0V
Note. VOLTAGE=1.05V
Note. VOLTAGE=0V
61 72
63 72
R1361 100 1% 1/16W MF LF 402
PLACE_NEAR=U1000.G43:50.8mm
PLACE_SIDE=TOP
R1363 100 1% 1/16W MF LF 402
PLACE_NEAR=U1000.AN17:50.8mm
PLACE_SIDE=TOP

PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.

=PPVCORE_S0_CPU_VCCAXG
43 16 13 10 8

OMIT_TABLE
CRITICAL

U1000
BGA
(7 OF 9)
IVY-BRIDGE
2C-35W
GRPHICS
DDR3-1.5V RAILS

AA46	VAXG_1	VDDQ_1	AJ28
AB47	VAXG_2	VDDQ_2	AJ33
AB50	VAXG_3	VDDQ_3	AJ36
AB51	VAXG_4	VDDQ_4	AJ40
AB52	VAXG_5	VDDQ_5	AL30
AB53	VAXG_6	VDDQ_6	AL34
AB55	VAXG_7	VDDQ_7	AL38
AB56	VAXG_8	VDDQ_8	AL42
AB58	VAXG_9	VDDQ_9	AM33
AB59	VAXG_10	VDDQ_10	AM36
AC61	VAXG_11	VDDQ_11	AM40
AD47	VAXG_12	VDDQ_12	AN30
AD48	VAXG_13	VDDQ_13	AN34
AD50	VAXG_14	VDDQ_14	AN38
AD51	VAXG_15	VDDQ_15	AR26
AD52	VAXG_16	VDDQ_16	AR28
AD53	VAXG_17	VDDQ_17	AR30
AD55	VAXG_18	VDDQ_18	AR32
AD56	VAXG_19	VDDQ_19	AR34
AD58	VAXG_20	VDDQ_20	AR36
AD59	VAXG_21	VDDQ_21	AR40
AE46	VAXG_22	VDDQ_22	AV41
N45	VAXG_23	VDDQ_23	AW26
P47	VAXG_24	VDDQ_24	BA40
P48	VAXG_25	VDDQ_25	BB28
P50	VAXG_26	VDDQ_26	BG33
P51	VAXG_27		
P52	VAXG_28	VCCDQ_1	AM28
P53	VAXG_29	VCCDQ_2	AN26
P55	VAXG_30		
P56	VAXG_31	VDDQ_SENSE	BC43
P61	VAXG_32	VSS_SENSE_VDDQ	BA43
T48	VAXG_33		
T58	VAXG_34	VCCSA_SENSE	U10
T59	VAXG_35		
T61	VAXG_36	VCCSA_VID_0	D48
U46	VAXG_37	VCCSA_VID_1	D49
V47	VAXG_38		
V48	VAXG_39	SM_VREF	AY43
V50	VAXG_40		
V51	VAXG_41		
V52	VAXG_42		
V53	VAXG_43		
V55	VAXG_44		
V56	VAXG_45		
V58	VAXG_46		
V59	VAXG_47		
W50	VAXG_48		
W51	VAXG_49		
W52	VAXG_50		
W53	VAXG_51		
W55	VAXG_52		
W56	VAXG_53		
W61	VAXG_54		
Y48	VAXG_55		
Y61	VAXG_56		
		F45	VAXG_SENSE
		G45	VSSAXG_SENSE
		BB3	VCCPLL_1
		BC1	VCCPLL_2
		BC4	VCCPLL_3
		L17	VCCSA_1
		L21	VCCSA_2
		N16	VCCSA_3
		N20	VCCSA_4
		N22	VCCSA_5
		P17	VCCSA_6
		P20	VCCSA_7
		R16	VCCSA_8
		R18	VCCSA_9
		R21	VCCSA_10
		U15	VCCSA_11
		V16	VCCSA_12
		V17	VCCSA_13
		V18	VCCSA_14
		V21	VCCSA_15
		W20	VCCSA_16

QUIET RAIL
SENSE LINE
1.8V RAIL
SA RAIL

=PP1V5R1V35_S3_CPU_VCCDDR
8 11 13 16 27
=PP1V5_S3_CPU_VCCDQ
8 16
CPU_VDDQ_SENSE_P
Note. VOLTAGE=1.05V
CPU_VDDQ_SENSE_N
Note. VOLTAGE=0V
CPU_VCCSASENSE
CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>
58 72
CPU_SM_VREF
13
VOLTAGE=0.75V

=PPVCORE_S0_CPU_VCCAXG
43 16 13 10 8
R1370 100 1% 1/16W MF LF 402
PLACE_NEAR=U1000.F45:50.8mm
PLACE_SIDE=TOP
CPU_AXG_SENSE_P
CPU_AXG_SENSE_N
Note. VOLTAGE=1.05V
Note. VOLTAGE=0V
72 61

=PP1V8_S0_CPU_VCCPLL_R
15 8
=PPVCCSA_S0_CPU
16 13 8
R1371 100 1% 1/16W MF LF 402
PLACE_NEAR=U1000.G45:50.8mm
PLACE_SIDE=TOP

PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.

=PPVCCSA_S0_CPU
16 13 8
=PP1V5R1V35_S3_CPU_VCCDDR
27 16 13 11 8
R1382 100 1% 1/16W MF LF 402
PLACE_NEAR=U1000.U10:50.8mm
R1380 100 1% 1/16W MF LF 402
PLACE_NEAR=U1000.BC43:50.8mm
PLACE_SIDE=TOP
R1381 100 1% 1/16W MF LF 402
PLACE_NEAR=U1000.BA43:50.8mm
PLACE_SIDE=TOP
R1314 10K 5% 1/20W MF 201
R1313 10K 5% 1/20W MF 201

PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.

=PP1V5R1V35_S3_CPU_VCCDDR
27 16 13 11 8
R1330 1K 1% 1/16W MF LF 402
PLACE_NEAR=U1000.BJ44:2.54mm
CPU_SM_VREF
13
R1331 1K 1% 1/16W MF LF 402
PLACE_NEAR=U1000.BJ44:2.54mm
C1330 0.1UF 10% 16V X7R_CERM 0402
PLACE_NEAR=U1000.BJ44:2.54mm

SYNC_MASTER=J30_MLB
SYNC_DATE=07/14/2011
PAGE TITLE
CPU POWER

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REVISION <E4LABEL>
BRANCH <BRANCH>
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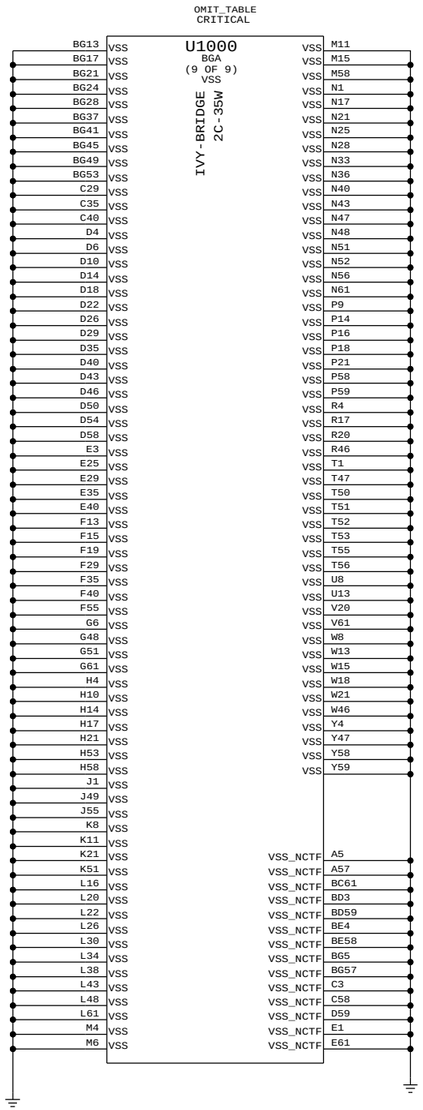

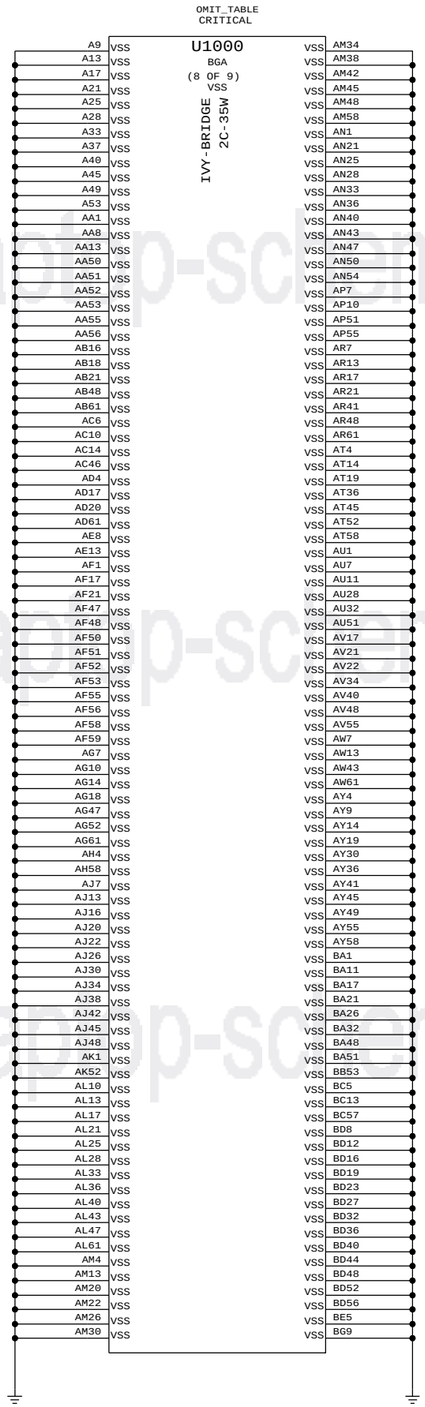

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Apple Inc.

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All INTEL recommendations from Intel doc #458544 Chief River Platform Power Design Guide v0p9

CPU VCORE DECOUPLING

Intel recommendation (Table 7-2): Option 2: 35x 2.2uF, 12x 22uF, 4x 470uF, or Option 3: 35x 2.2uF, 6x 22uF, 6x 330 uF

43 13 10 8 =PPVCORE_S0_CPU

CRITICAL C1600 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1604 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1606 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1607 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1608 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1609 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1610 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1612 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1613 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1615 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1617 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1623 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1624 2.2UF 20% 6.3V CERM 402-2

CRITICAL C1625 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1627 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1628 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1631 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1632 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1635 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1637 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1638 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1639 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1640 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1641 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1642 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1643 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1644 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1645 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1647 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1648 2.2UF 20% 6.3V CERM 402-2

CRITICAL C1650 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1651 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1652 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1653 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1654 2.2UF 20% 6.3V CERM 402-2

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

CRITICAL C1646 20UF 20% 2V X6T-CERM 0402
CRITICAL C168F 20UF 20% 2V X6T-CERM 0402
NO STUFF C16A0 20UF 20% 2V X6T-CERM 0402

CRITICAL C1655 20UF 20% 2V X6T-CERM 0402
NO STUFF C1656 20UF 20% 2V X6T-CERM 0402
CRITICAL C1657 20UF 20% 2V X6T-CERM 0402
CRITICAL C1658 20UF 20% 2V X6T-CERM 0402
NO STUFF C1659 20UF 20% 2V X6T-CERM 0402
NO STUFF C1660 20UF 20% 2V X6T-CERM 0402
CRITICAL C1661 20UF 20% 2V X6T-CERM 0402
NO STUFF C1662 20UF 20% 2V X6T-CERM 0402
NO STUFF C1663 20UF 20% 2V X6T-CERM 0402
NO STUFF C1664 20UF 20% 2V X6T-CERM 0402
NO STUFF C1665 20UF 20% 2V X6T-CERM 0402
NO STUFF C1666 20UF 20% 2V X6T-CERM 0402
NO STUFF C166A 20UF 20% 2V X6T-CERM 0402
NO STUFF C166B 20UF 20% 2V X6T-CERM 0402
CRITICAL C166C 20UF 20% 2V X6T-CERM 0402
NO STUFF C166D 20UF 20% 2V X6T-CERM 0402
NO STUFF C166E 20UF 20% 2V X6T-CERM 0402
CRITICAL C166F 20UF 20% 2V X6T-CERM 0402
CRITICAL C165A 20UF 20% 2V X6T-CERM 0402
NO STUFF C165B 20UF 20% 2V X6T-CERM 0402
NO STUFF C1667 20UF 20% 2V X6T-CERM 0402
CRITICAL C1674 20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1667-C1679):
Place close to U1000 on bottom side.

CRITICAL C16A1 20UF 20% 2V X6T-CERM 0402
NO STUFF C16A2 20UF 20% 2V X6T-CERM 0402
CRITICAL C16A3 20UF 20% 2V X6T-CERM 0402

NO STUFF C1675 20UF 20% 2V X6T-CERM 0402
NO STUFF C1668 20UF 20% 2V X6T-CERM 0402
CRITICAL C1669 20UF 20% 2V X6T-CERM 0402
NO STUFF C1670 20UF 20% 2V X6T-CERM 0402
CRITICAL C1671 20UF 20% 2V X6T-CERM 0402
NO STUFF C1672 20UF 20% 2V X6T-CERM 0402
NO STUFF C1673 20UF 20% 2V X6T-CERM 0402
CRITICAL C1649 20UF 20% 2V X6T-CERM 0402
NO STUFF C164A 20UF 20% 2V X6T-CERM 0402
NO STUFF C1676 20UF 20% 2V X6T-CERM 0402
CRITICAL C1677 20UF 20% 2V X6T-CERM 0402
NO STUFF C1678 20UF 20% 2V X6T-CERM 0402
CRITICAL C1679 20UF 20% 2V X6T-CERM 0402
CRITICAL C165C 20UF 20% 2V X6T-CERM 0402
NO STUFF C165D 20UF 20% 2V X6T-CERM 0402
CRITICAL C165E 20UF 20% 2V X6T-CERM 0402
NO STUFF C165F 20UF 20% 2V X6T-CERM 0402
NO STUFF C164E 20UF 20% 2V X6T-CERM 0402
NO STUFF C164B 20UF 20% 2V X6T-CERM 0402
NO STUFF C164C 20UF 20% 2V X6T-CERM 0402
CRITICAL C164D 20UF 20% 2V X6T-CERM 0402
CRITICAL C164F 20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

C1680 470UF-4MOHM 20% 2 0V POLY TANT D2T SM1
C1681 470UF-4MOHM 20% 2 0V POLY TANT D2T SM1
C1682 470UF-4MOHM 20% 2 0V POLY TANT D2T SM1
C1683 470UF-4MOHM 20% 2 0V POLY TANT D2T SM1
C168D 270UF 20% 2V TANT CASE-B2-SM
C168E 270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Table 7-7): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000

13 11 10 8 =PP1V05_S0_CPU_VCCIO

C1684 1UF 10% 10V X5R CERM 0402
C1685 1UF 10% 10V X5R CERM 0402
C1686 1UF 10% 10V X5R CERM 0402
C1687 1UF 10% 10V X5R CERM 0402
C1688 1UF 10% 10V X5R CERM 0402
C1689 1UF 10% 10V X5R CERM 0402
C1690 1UF 10% 10V X5R CERM 0402
C1691 1UF 10% 10V X5R CERM 0402
C1692 1UF 10% 10V X5R CERM 0402
C1693 1UF 10% 10V X5R CERM 0402
C1694 1UF 10% 10V X5R CERM 0402
C1695 1UF 10% 10V X5R CERM 0402
C1696 1UF 10% 10V X5R CERM 0402

C1697 1UF 10% 10V X5R CERM 0402
C1698 1UF 10% 10V X5R CERM 0402
C1699 1UF 10% 10V X5R CERM 0402
C169A 1UF 10% 10V X5R CERM 0402
C169B 1UF 10% 10V X5R CERM 0402
C169C 1UF 10% 10V X5R CERM 0402
C169D 1UF 10% 10V X5R CERM 0402
C169E 1UF 10% 10V X5R CERM 0402
C169F 1UF 10% 10V X5R CERM 0402
C161A 1UF 10% 10V X5R CERM 0402
C161B 1UF 10% 10V X5R CERM 0402
C161C 1UF 10% 10V X5R CERM 0402
C161D 1UF 10% 10V X5R CERM 0402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C161E 10UF 20% 6.3V CERM X5R 0402 1
C161F 10UF 20% 6.3V CERM X5R 0402 1
C162A 10UF 20% 6.3V CERM X5R 0402 1
C162B 10UF 20% 6.3V CERM X5R 0402 1
C162C 10UF 20% 6.3V CERM X5R 0402 1
C162D 10UF 20% 6.3V CERM X5R 0402 1
C162E 10UF 20% 6.3V CERM X5R 0402 1
C167A 10UF 20% 6.3V CERM X5R 0402 1
C167B 10UF 20% 6.3V CERM X5R 0402 1
C167C 10UF 20% 6.3V CERM X5R 0402 1

C167D 270UF 20% 2V TANT CASE-B2-SM
C167E 270UF 20% 2V TANT CASE-B2-SM
C168A 270UF 20% 2V TANT CASE-B2-SM
C168B 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603
=PP1V05_S0_CPU_VCCPQE 8 13
C167F 1UF 10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (table 7-5): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

8 PP1V8_S0_CPU_VCCPLL
R1600 0 5% 1/10W MF LF 402
PP1V8_S0_CPU_VCCPLL_R 8 13
PLACE NEAR=U1000 AK61 5mm PLACE NEAR=U1000 AK61 5mm
PLACE NEAR U1000 AK63 2 54 mm NO VIA
C160X 1UF 10% 10V X5R 402
C160Y 1UF 10% 10V X5R 402
C160Z 270UF 20% 2V TANT CASE-B2-SM
C168C 270UF 20% 2V TANT CASE-B2-SM
PLACE NEAR U1000 AK65 2 54 mm NO VIA

CPU VCCPLL Low pass filter

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VAXG DECOUPLING

Intel recommendation (Table 7-4) for GT2 3.9mOhm LL: 11x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

43 13 10 8 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL C1700 1UF 10% 10V X5R CERM 0402
CRITICAL C1701 1UF 10% 10V X5R CERM 0402
CRITICAL C1702 1UF 10% 10V X5R CERM 0402
CRITICAL C1703 1UF 10% 10V X5R CERM 0402
CRITICAL C1704 1UF 10% 10V X5R CERM 0402
CRITICAL C1705 1UF 10% 10V X5R CERM 0402
CRITICAL C1706 1UF 10% 10V X5R CERM 0402
CRITICAL C1707 1UF 10% 10V X5R CERM 0402
CRITICAL C1708 1UF 10% 10V X5R CERM 0402
CRITICAL C1709 1UF 10% 10V X5R CERM 0402
CRITICAL C1710 1UF 10% 10V X5R CERM 0402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL C1711 10UF 20% 6.3V CERM X5R 0402 1
CRITICAL C1712 10UF 20% 6.3V CERM X5R 0402 1
CRITICAL C1713 10UF 20% 6.3V CERM X5R 0402 1
CRITICAL C1714 10UF 20% 6.3V CERM X5R 0402 1
CRITICAL C1715 10UF 20% 6.3V CERM X5R 0402 1
CRITICAL C1716 10UF 20% 6.3V CERM X5R 0402 1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL C1717 20UF 20% 2V X6T-CERM 0402
CRITICAL C1718 20UF 20% 2V X6T-CERM 0402
CRITICAL C1719 20UF 20% 2V X6T-CERM 0402
CRITICAL C1720 20UF 20% 2V X6T-CERM 0402
CRITICAL C1721 20UF 20% 2V X6T-CERM 0402
CRITICAL C1722 20UF 20% 2V X6T-CERM 0402
NO STUFF C1725 20UF 20% 2V X6T-CERM 0402
NO STUFF C1726 20UF 20% 2V X6T-CERM 0402
NO STUFF C1727 20UF 20% 2V X6T-CERM 0402
NO STUFF C1728 20UF 20% 2V X6T-CERM 0402
NO STUFF C1729 20UF 20% 2V X6T-CERM 0402
NO STUFF C172A 20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1723-C1724):

Place near inductors on bottom side.

C1723 470UF-4MOHM 20% 2.0V POLY TANT D2T SM1
C1724 470UF-4MOHM 20% 2.0V POLY TANT D2T SM1

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Table 7-11): 10x 1uF, 8x 10uF, 1x 330uF

27 13 11 8 =PP1V5R1V35_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):

Place on bottom side of U1000

C1738 1UF 10% 10V X5R CERM 0402
C1739 1UF 10% 10V X5R CERM 0402
C1740 1UF 10% 10V X5R CERM 0402
C1741 1UF 10% 10V X5R CERM 0402
C1742 1UF 10% 10V X5R CERM 0402
C1743 1UF 10% 10V X5R CERM 0402
C1744 1UF 10% 10V X5R CERM 0402
C1745 1UF 10% 10V X5R CERM 0402
C1746 1UF 10% 10V X5R CERM 0402
C1747 1UF 10% 10V X5R CERM 0402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM X5R 0402 1
C1749 10UF 20% 6.3V CERM X5R 0402 1
C1750 10UF 20% 6.3V CERM X5R 0402 1
C1751 10UF 20% 6.3V CERM X5R 0402 1
C1752 10UF 20% 6.3V CERM X5R 0402 1
C1753 10UF 20% 6.3V CERM X5R 0402 1
C1754 10UF 20% 6.3V CERM X5R 0402 1
C1755 10UF 20% 6.3V CERM X5R 0402 1

C1756 270UF 20% 2V TANT CASE-B2-SM
C1770 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702 0.010 1% 1/4W MF 0603
=PP1V5_S3_CPU_VCCDQ 8 13
C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Table 7-9): 5x 1uf, 5x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

13 8 =PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 1UF 10% 10V X5R CERM 0402
C1759 1UF 10% 10V X5R CERM 0402
C1760 1UF 10% 10V X5R CERM 0402
C1761 1UF 10% 10V X5R CERM 0402
C1762 1UF 10% 10V X5R CERM 0402

C1763 10UF 20% 6.3V CERM X5R 0402 1
C1764 10UF 20% 6.3V CERM X5R 0402 1
C1765 10UF 20% 6.3V CERM X5R 0402 1
C1766 10UF 20% 6.3V CERM X5R 0402 1
C1767 10UF 20% 6.3V CERM X5R 0402 1

C1768 270UF 20% 2V TANT CASE-B2-SM
C1769 270UF 20% 2V TANT CASE-B2-SM

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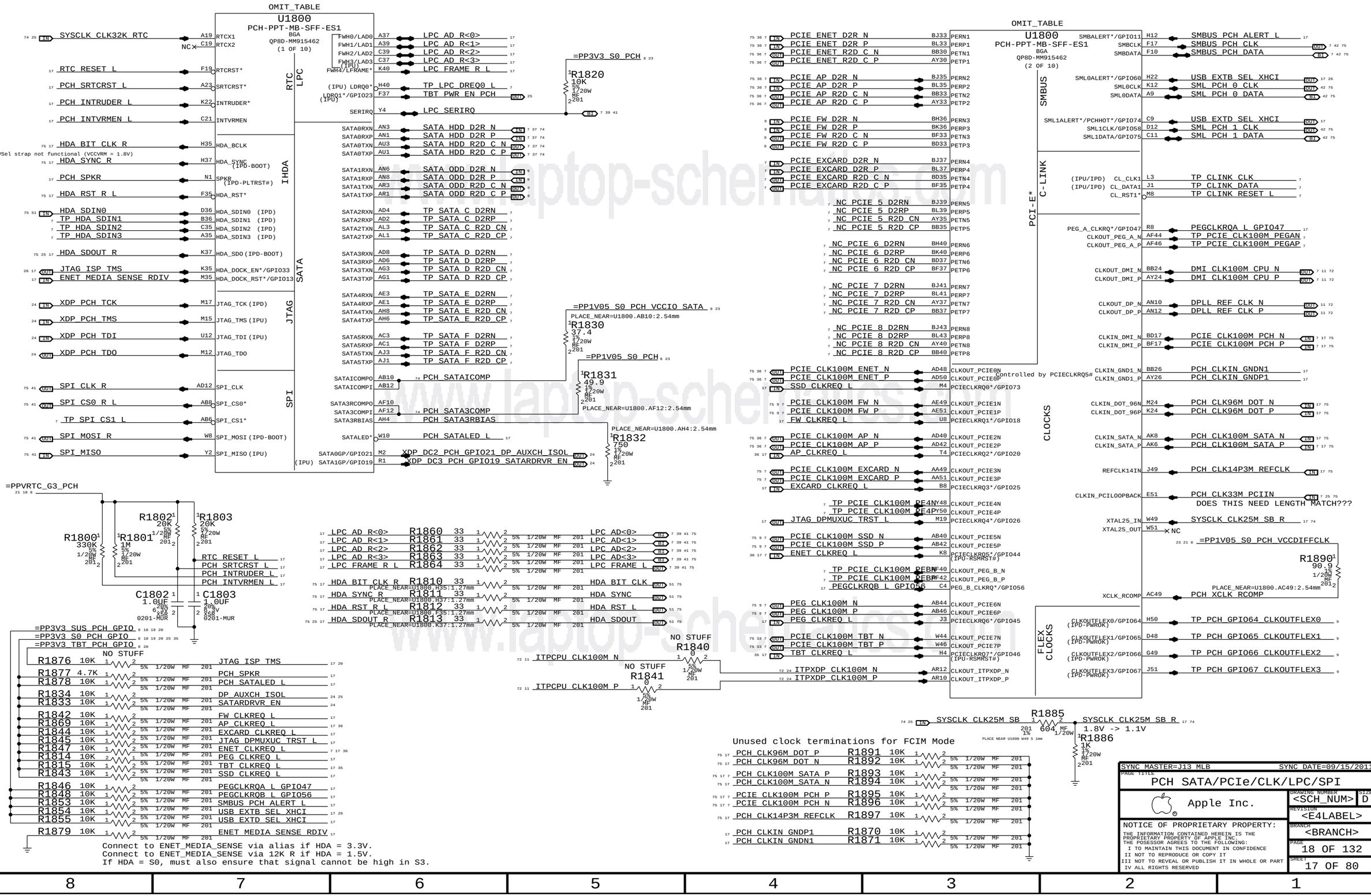

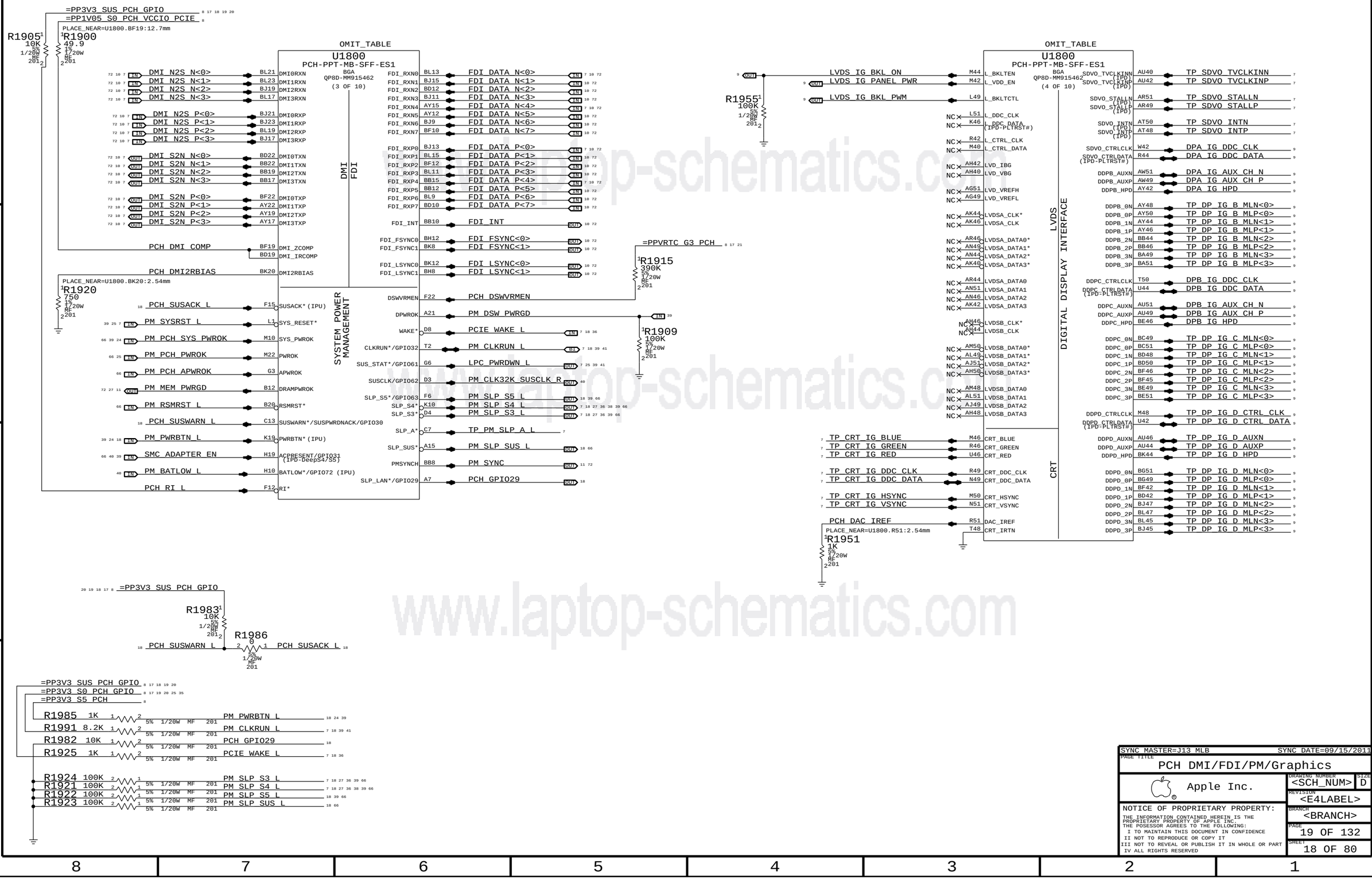

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
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NC	BH24	TP1	
NC	BK24	TP2	
NC	BH20	TP3	
NC	BK16	TP4	
NC	BH16	TP5	
NC	AN42	TP6	
NC	AN40	TP7	
NC	AR40	TP8	
NC	AR42	TP9	
NC	D20	TP10	
NC	M30	TP11	
NC	E3	TP12	
NC	AM4	TP13	
NC	AT4	TP14	
NC	AT2	TP15	
NC	AD10	TP16	
NC	B24	TP17	
NC	D24	TP18	
NC	AD44	TP19	
NC	AD46	TP20	
NC	BJ48	TP21	
NC	BL7	TP22	
7 TP_PCH_TP23	W40	TP23	
NC	K30	TP24	
NC	BH49	TP41	
NC	BB42	TP42	

	AU6	NC	
	AU8	NC	
	AW1	NC	
	AW3	NC	
	AY2	NC	
	AY4	NC	
	AY6	NC	
	AY8	NC	
	BA1	NC	
	BA3	NC	
	BB6	NC	
	BC1	NC	
RSVD	BC3		
	BD2	NC	
	BD4	NC	
	BE1	NC	
	BE3	NC	
	BE6	NC	
	BF6	NC	
	BF7	NC	
	BG1	NC	
	BG3	NC	
	BH3	NC	
	BH4	NC	
	BJ4	NC	
	BJ5	NC	
	BJ7	NC	
	BK6	NC	
	BL5	NC	

USB

74 38 7 IN	USB3_EXTA_RX_N	BJ25	USB3RN1
9 IN	USB3_EXTC_RX_N	BJ27	USB3RN2
74 36 7 IN	USB3_EXTB_RX_N	BJ31	USB3RN3
9 IN	USB3_EXTD_RX_N	BJ29	USB3RN4
74 38 7 IN	USB3_EXTA_RX_P	BL25	USB3RP1
9 IN	USB3_EXTC_RX_P	BL27	USB3RP2
74 36 7 IN	USB3_EXTB_RX_P	BL31	USB3RP3
9 IN	USB3_EXTD_RX_P	BL29	USB3RP4
74 38 7 OUT1	USB3_EXTA_TX_N	BF26	USB3TN1
9 OUT1	USB3_EXTC_TX_N	BB28	USB3TN2
74 36 OUT1	USB3_EXTB_TX_N	BF28	USB3TN3
9 OUT1	USB3_EXTD_TX_N	BF30	USB3TN4
74 38 OUT1	USB3_EXTA_TX_P	BD26	USB3TP1
9 OUT1	USB3_EXTC_TX_P	AY28	USB3TP2
74 36 OUT1	USB3_EXTB_TX_P	BD28	USB3TP3
9 OUT1	USB3_EXTD_TX_P	BD30	USB3TP4

USBP0N	F24	USB_EXTA_N	BI 38 74
USBP0P	H24	USB_EXTA_P	BI 38 74
USBP1N	C25	USB_EXTC_N	BI 9
USBP1P	A25	USB_EXTC_P	BI 9
USBP2N	C27	USB_EXTB_XHCI_N	BI 26 74
USBP2P	A27	USB_EXTB_XHCI_P	BI 26 74
USBP3N	H28	USB_EXTD_XHCI_N	BI 26 74
USBP3P	F28	USB_EXTD_XHCI_P	BI 26 74
USBP4N	M26	TP_USB_4N	9
USBP4P	K26	TP_USB_4P	9
USBP5N	D28	TP_USB_SDN	9
USBP5P	B28	TP_USB_SDP	9
USBP6N	H26	TP_USB_WLANN	9
USBP6P	F26	TP_USB_WLANP	9
USBP7N	D32	USB_HUB_UP_N	BI 26 74
USBP7P	B32	USB_HUB_UP_P	BI 26 74
USBP8N	M28	USB_CAMERA_N	BI 32 74
USBP8P	K28	USB_CAMERA_P	BI 32 74
USBP9N	C29	USB_EXTB_EHCI_N	BI 26 74
USBP9P	A29	USB_EXTB_EHCI_P	BI 26 74
USBP10N	C31	USB_EXTD_EHCI_N	BI 9
USBP10P	A31	USB_EXTD_EHCI_P	BI 9
USBP11N	H33	TP_USB_BT_HSN	9
USBP11P	F33	TP_USB_BT_HSP	9
USBP12N	H30	TP_USB_12N	9
USBP12P	F30	TP_USB_12P	9
USBP13N	M33	TP_USB_13N	9
USBP13P (IPD)	K33	TP_USB_13P	9

Ext A (XHCI/EHCI)

Ext C (XHCI/EHCI)

Ext B (XHCI)

Ext D (XHCI) (Mobiles: Trackpad)

Unused

RSVD: SD

RSVD: WiFi

USB Hub (All LS/FS Devices)

Camera

Ext B (EHCI)

Ext D (EHCI)

RSVD: BT (HS)

Unused

Unused

PCI

19 OUT1	JTAG_GMUX_TMS	G46	REQ1*/GPIO50
19 OUT1	BLC_I2C_MUX_SEL	K44	REQ2*/GPIO52
19 OUT1	USE_HDD_OOB_L	F46	REQ3*/GPIO54
7	TP_PCH_STRP_BBS1	F42	GNT1*/GPIO51
7	TP_PCH_STRP_ESI_L	H42	GNT2*/GPIO53
	PCH_STRP_TOPBLK_SWP_L	D44	GNT3*/GPIO55 (IPU-PCIERST#)
19 IN	BLC_GPIO	A47	PIRQE*/GPIO2
55 19 IN	AUD_IP_PERIPHERAL_DET	C41	PIRQF*/GPIO3
33 19 IN	TBT_PWR_REQ_L	F45	PIRQG*/GPIO4
54 19 IN	AUD_I2C_INT_L	F40	PIRQH*/GPIO5
7	TP_PCI_PME_L	H2	PME* (IPU)
27 25 OUT1	PLT_RESET_L	F7	PLTRSTB*
75 25 OUT1	LPC_CLK33M_SMC_R	G51	CLKOUT_PCI0
25 OUT1	LPC_CLK33M_LPCPLUS_R	E49	CLKOUT_PCI1
7	TP_PCI_CLK33M_OUT2	H48	CLKOUT_PCI2
7	TP_PCI_CLK33M_OUT3	J43	CLKOUT_PCI3
25 OUT1	PCH_CLK33M_PCIOUT	G45	CLKOUT_PCI4 (IPD)

35 25 20 19 18 17 8 =PP3V3_S0_PCH_GPIO

R2010	10K	1	2	5%	1/20W	MF	201	PCI_INTA_L
R2011	10K	1	2	5%	1/20W	MF	201	PCI_INTB_L
R2012	10K	1	2	5%	1/20W	MF	201	PCI_INTC_L
R2013	10K	1	2	5%	1/20W	MF	201	PCI_INTD_L

R2054 10K 2 1 5% 1/20W MF 201 — NO STUFF

USBRBIAS* C33 — 74 PCH_USB_RBIAS
USBRBIAS A33

PLACE_NEAR=U1800.A33:2.54mm
R2070 22.6 1% 1/20W MF 201

OC0*/GPIO59	C17	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	IN 19 24
OC1*/GPIO40	A17	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	IN 19 24
OC2*/GPIO41	A13	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L	IN 19 24
OC3*/GPIO42	D16	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L	IN 19 24
OC4*/GPIO43	A11	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L	IN 24
OC5*/GPIO9	B16	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L	IN 24
OC6*/GPIO10	C23	XDP_DB2_PCH_GPIO10_AP_PWR_EN	OUT 24
OC7*/GPIO14	H15	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	IN 19 24

=PP3V3_SUS_PCH_GPIO 8 17 18 20
=PP3V3_S3_PCH_GPIO 8 25
=PP3V3_S0_PCH_GPIO 8 17 18 19 20 25 35

R2016	10K	1	2	5%	1/20W	MF	201	JTAG_GMUX_TMS 19
R2017	10K	1	2	5%	1/20W	MF	201	BLC_I2C_MUX_SEL 19
R2018	10K	1	2	5%	1/20W	MF	201	USE_HDD_OOB_L 19
R2030	10K	1	2	5%	1/20W	MF	201	BLC_GPIO 19

NO STUFF Redundant to pull-up on audio page

R2014	10K	1	2	5%	1/20W	MF	201	AUD_IP_PERIPHERAL_DET 19 55
R2031	10K	1	2	5%	1/20W	MF	201	TBT_PWR_REQ_L 19 33

NO STUFF Redundant to pull-up on audio page

R2033	10K	1	2	5%	1/20W	MF	201	AUD_I2C_INT_L 19 54
R2069	10K	1	2	5%	1/20W	MF	201	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE 19 24
R2060	10K	1	2	5%	1/20W	MF	201	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L 19 24
R2061	10K	1	2	5%	1/20W	MF	201	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L 19 24
R2062	10K	1	2	5%	1/20W	MF	201	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L 19 24
R2068	10K	1	2	5%	1/20W	MF	201	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L 19 24
R2067	10K	2	1	5%	1/20W	MF	201	AP_PWR_EN 24 36 66

SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE
PCH PCI/USB/TP/RSVD

Apple Inc.

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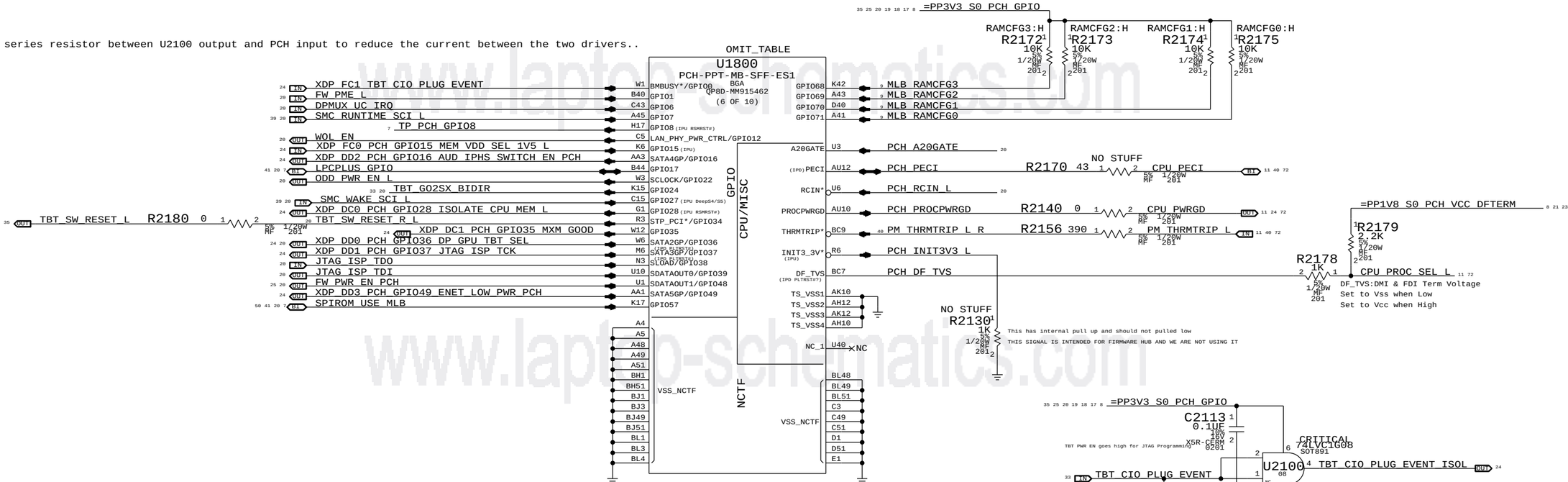
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

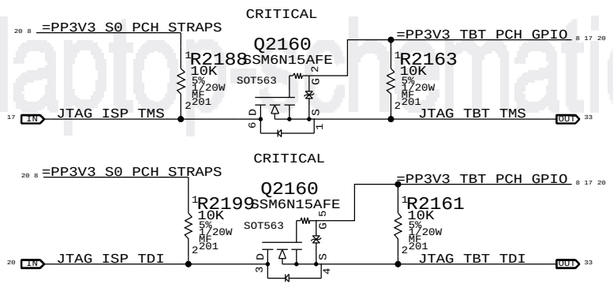
Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

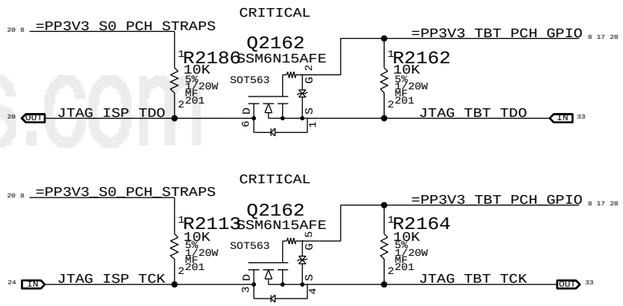
R2574 is 1K series resistor between U2100 output and PCH input to reduce the current between the two drivers..

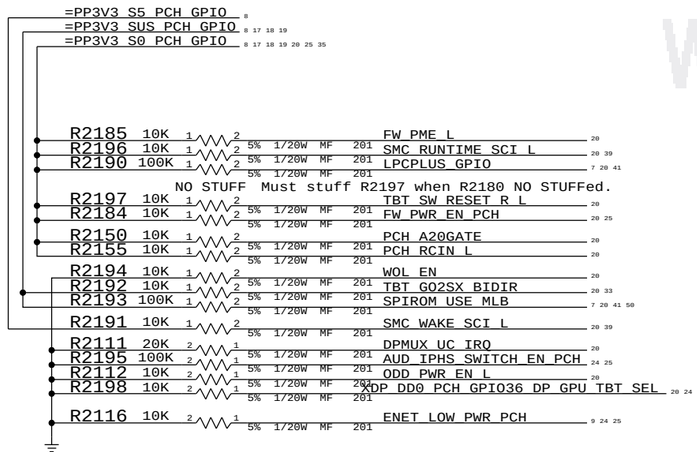


JTAG Isolation due to glitch in and out of sleep

NOTE TCK from PCH is Push Pull CMOS
NOTE TMS/TDI from PCH is Open Drain
NOTE TDO from CR is Push Pull CMOS







SYNC_MASTER=J13_MLB	SYNC_DATE=09/15/2011
PAGE TITLE	PCH GPIO/MISC/NCTF
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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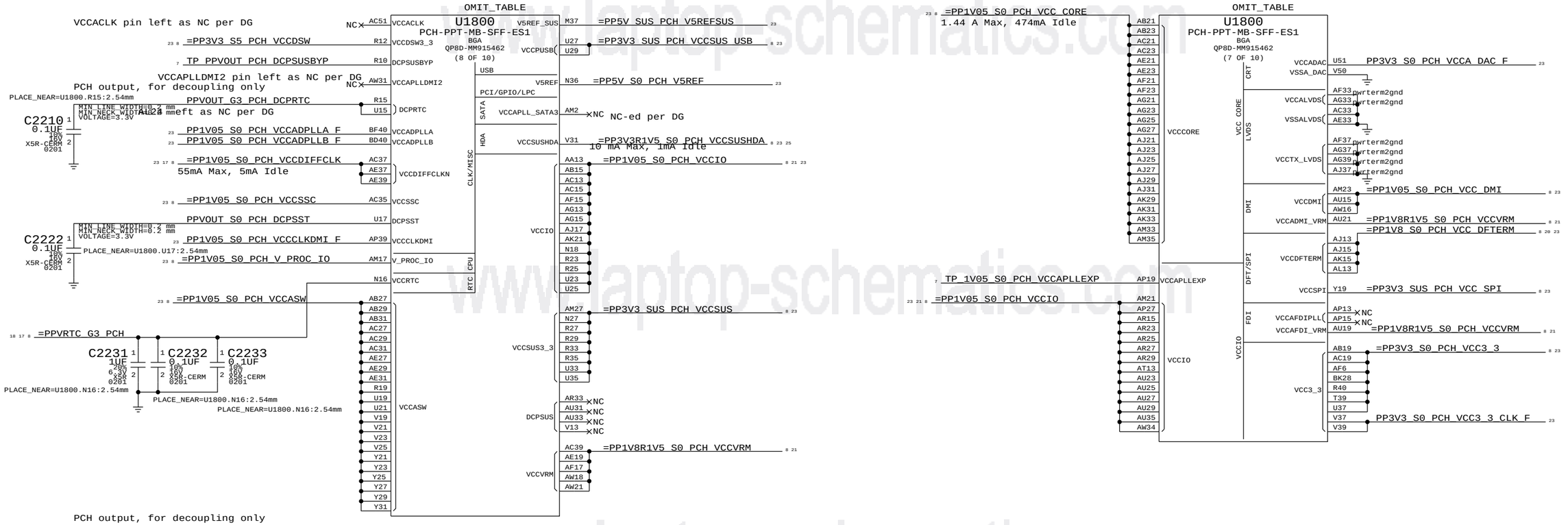

SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE: PCH POWER

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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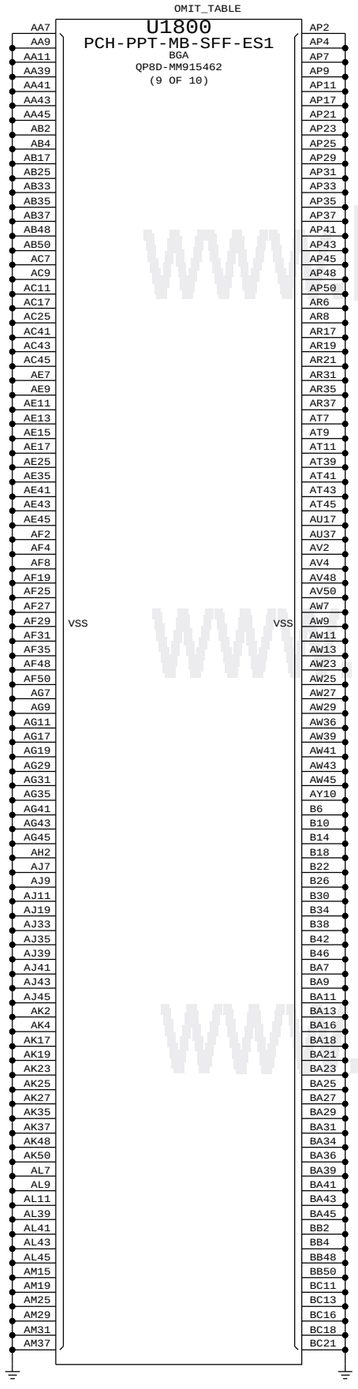

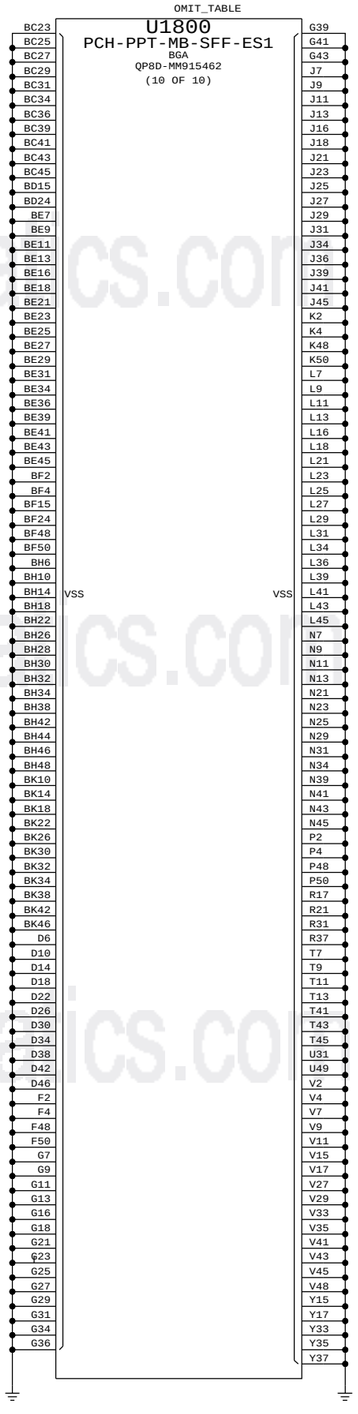

SYNC MASTER=J13 MLB SYNC DATE=09/15/2011

PAGE TITLE

PCH GROUNDS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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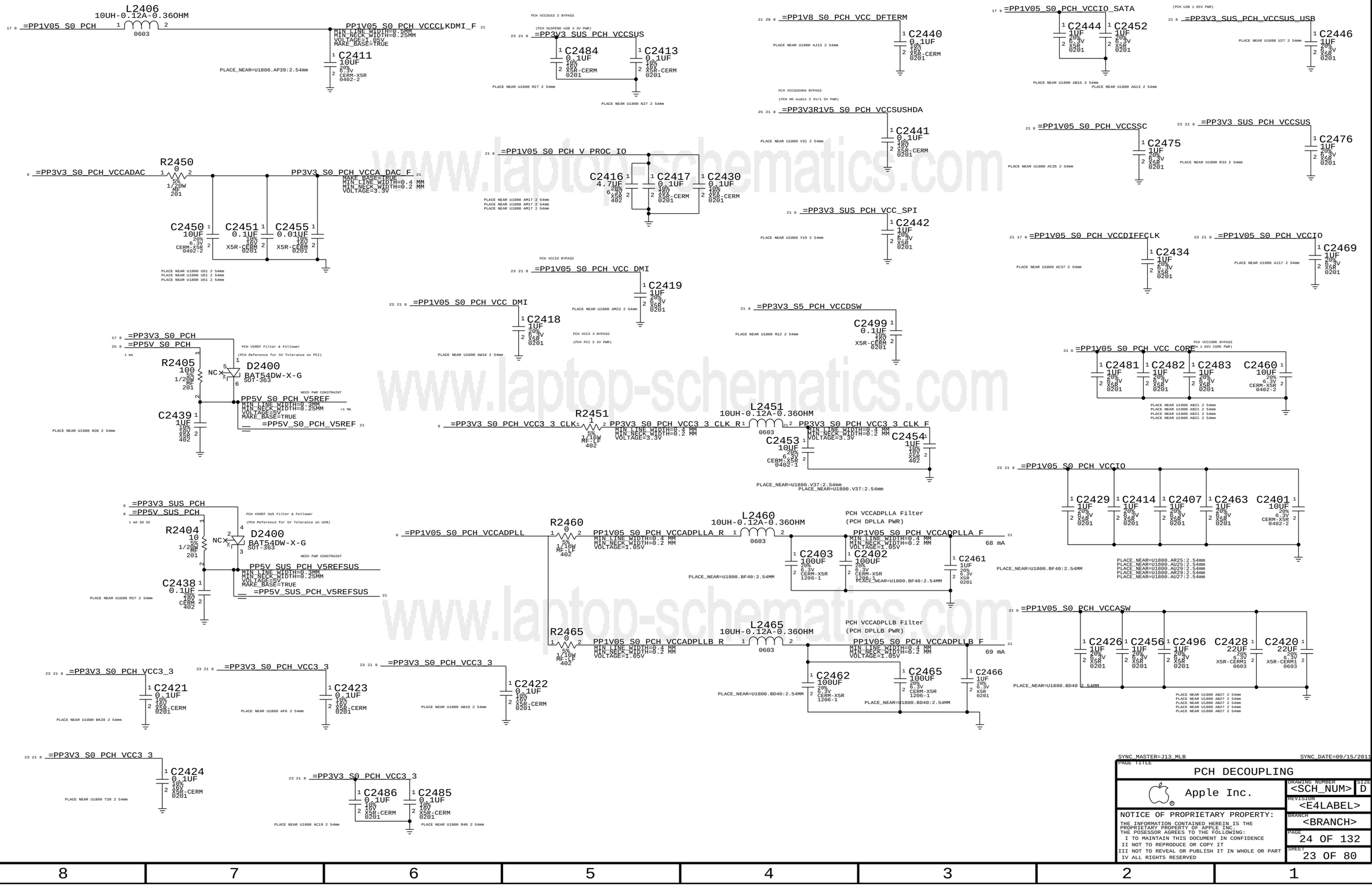

CPU Micro2-XDP

=PPVCCIO_S0_XDP

=PP3V3_S0_XDP
NO STUFF
R2540 1K 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J2500
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<16>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<17>
XDP_BPM_L<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<0>
XDP_BPM_L<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<1>
XDP_BPM_L<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<2>
XDP_BPM_L<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<3>
CPU_CFG<10>	OBSEN_B0	OBSEN_D0	CPU_CFG<8>
CPU_CFG<11>	OBSEN_B1	OBSEN_D1	CPU_CFG<9>
XDP_OBSDATA_B<0>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<4>
XDP_OBSDATA_B<1>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<5>
XDP_OBSDATA_B<2>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<6>
XDP_OBSDATA_B<3>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<7>
XDP_CPU_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	XDP_CPU_CLK100M_P
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	XDP_CPU_CLK100M_N
	VCC_OBS_AB	VCC_OBS_CD	
XDP_CPU_CFG<0>	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_VR_READY	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_CPU_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_CPU_TRST_L
	TCK1	TDI	XDP_CPU_TDI
XDP_CPU_TCK	TCK0	TMS	XDP_CPU_TMS
		XDP_PRESENT#	

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C2500 0.1UF 10% 10V X7R-CERM 0402
XDP C2501 0.1UF 10% 10V X7R-CERM 0402
518S0847

=PP1V05_SUS_PCH_JTAG

XDP_PCH_TDO	R2550 51	XDP PLACE_NEAR=J2550.52:2.54mm
XDP_PCH_TDI	R2551 51	XDP PLACE_NEAR=U1800.K5:2.54mm
XDP_PCH_TMS	R2552 51	XDP PLACE_NEAR=U1800.H7:2.54mm
XDP_PCH_TCK	R2556 51	XDP PLACE_NEAR=U1800.J3:2.54mm

1K series R on PCH Support Page

=PPVCCIO_S0_XDP

XDP_CPU_TDO	R2510 51	XDP PLACE_NEAR=J2500.52:2.54mm
XDP_CPU_TDI	R2511 51	XDP PLACE_NEAR=U1000.K61:2.54mm
XDP_CPU_TMS	R2512 51	XDP PLACE_NEAR=U1000.H59:2.54mm
XDP_CPU_TCK	R2513 51	XDP PLACE_NEAR=U1000.J58:2.54mm
XDP_CPU_TRST_L	R2514 51	XDP PLACE_NEAR=U1000.H63:2.54mm

(R2560-R2563)
XDP_CPU:BPM

XDP_BPM_L<4>	R2560 0	5% 1/20W MF 201
XDP_BPM_L<5>	R2561 0	5% 1/20W MF 201
XDP_BPM_L<6>	R2562 0	5% 1/20W MF 201
XDP_BPM_L<7>	R2563 0	5% 1/20W MF 201

(R2564-R2567)
XDP_CPU:CFG

CPU_CFG<12>	R2564 0	5% 1/20W MF 201
CPU_CFG<13>	R2565 0	5% 1/20W MF 201
CPU_CFG<14>	R2566 0	5% 1/20W MF 201
CPU_CFG<15>	R2567 0	5% 1/20W MF 201

CPU_PWRGD	R2500 1K	XDP PLACE_NEAR=U1000.C60:2.54mm 5% 1/20W MF 201
PM_PWRBTN_L	R2502 0	XDP PLACE_NEAR=U4900.P17:2.54mm 5% 1/20W MF 201
CPU_CFG<0>	R2501 1K	XDP PLACE_NEAR=U1000.B57:2.54mm 5% 1/20W MF 201
PM_PCH_SYS_PWROK	R2504 330	XDP 5% 1/20W MF 201

R2581 1K 1/20W 5% MF 201
R2580 1K 1/20W 5% MF 201

XDP SIGNALS

(R2520-R2537)

XDP_DA0_USB_EXTA_OC_L	R2520 33	XDP 5% 1/20W MF 201
XDP_DA1_USB_EXTB_OC_L	R2521 33	5% 1/20W MF 201
XDP_DA2_USB_EXTC_OC_L	R2522 33	5% 1/20W MF 201
XDP_DA3_USB_EXTD_OC_L	R2523 33	5% 1/20W MF 201
XDP_DB0_USB_EXTB_OC_EHCI_L	R2524 33	5% 1/20W MF 201
XDP_DB1_USB_EXTD_OC_EHCI_L	R2525 33	5% 1/20W MF 201
XDP_DB2_AP_PWR_EN	R2526 33	5% 1/20W MF 201
XDP_DB3_SDCONN_STATE_CHANGE	R2527 33	5% 1/20W MF 201
XDP_FC0_MEM_VDD_SEL_1V5_L	R2528 33	5% 1/20W MF 201
XDP_FC1	R2529 33	5% 1/20W MF 201
XDP_DC0_ISOLATE_CPU_MEM_L	R2530 33	5% 1/20W MF 201
XDP_DC1_MXM_GOOD	R2531 33	5% 1/20W MF 201
XDP_DC2_DP_AUXCH_ISOL	R2532 33	5% 1/20W MF 201
XDP_DC3_SATARDRVR_EN	R2533 33	5% 1/20W MF 201
XDP_DD0_DP_GPU_TBT_SEL	R2534 33	5% 1/20W MF 201
XDP_DD1_JTAG_ISP_TCK	R2535 33	5% 1/20W MF 201
XDP_DD2_AUD_IPHS_SWITCH_EN	R2536 33	5% 1/20W MF 201
XDP_DD3_ENET_LOW_PWR	R2537 33	5% 1/20W MF 201

PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	XDP_DA0_USB_EXTA_OC_L
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	XDP_DA1_USB_EXTB_OC_L
XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L	XDP_DA2_USB_EXTC_OC_L
XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L	XDP_DA3_USB_EXTD_OC_L
XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI	XDP_DB0_USB_EXTB_OC_EHCI_L
XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L	XDP_DB1_USB_EXTD_OC_EHCI_L
XDP_DB2_PCH_GPIO10_AP_PWR_EN	XDP_DB2_AP_PWR_EN
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	XDP_DB3_SDCONN_STATE_CHANGE
XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L	XDP_FC0_MEM_VDD_SEL_1V5_L
XDP_FC1_TBT_CIO_PLUG_EVENT	XDP_FC1
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	XDP_DC0_ISOLATE_CPU_MEM_L
XDP_DC1_PCH_GPIO35_MXM_GOOD	XDP_DC1_MXM_GOOD
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	XDP_DC2_DP_AUXCH_ISOL
XDP_DC3_PCH_GPIO19_SATARDRVR_EN	XDP_DC3_SATARDRVR_EN
XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL	XDP_DD0_DP_GPU_TBT_SEL
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	XDP_DD1_JTAG_ISP_TCK
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	XDP_DD2_AUD_IPHS_SWITCH_EN
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	XDP_DD3_ENET_LOW_PWR

PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	R2590 0	USB_EXTA_OC_L
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	R2591 0	USB_EXTB_OC_L
XDP_DB2_PCH_GPIO10_AP_PWR_EN	R2596 0	AP_PWR_EN
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	R2597 0	SDCONN_STATE_CHANGE
XDP_DC3_PCH_GPIO19_SATARDRVR_EN	R2573 0	SATARDRVR_EN
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	R2570 0	ISOLATE_CPU_MEM_L
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	R2572 0	DP_AUXCH_ISOL
XDP_FC1_TBT_CIO_PLUG_EVENT	R2574 1K	TBT_CIO_PLUG_EVENT_ISOL

Non-XDP Signals

PPDDR:1V5

XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L	R2595 0	MEM_VDD_SEL_1V5_L
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	R2575 0	JTAG_ISP_TCK
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	R2576 0	AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	R2577 0	ENET_LOW_PWR_PCH

PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needes to split between route from PCH to J2550 and path to non-XDP signal destination.

PCH Micro2-XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J2550
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

TP_XDP_PCH_OBSFN_A<0>	OBSEN_A0	OBSEN_C0	XDP_FC0_MEM_VDD_SEL_1V5_L
TP_XDP_PCH_OBSFN_A<1>	OBSEN_A1	OBSEN_C1	XDP_FC1
XDP_DA0_USB_EXTA_OC_L	OBSDATA_A0	OBSDATA_C0	XDP_DC0_ISOLATE_CPU_MEM_L
XDP_DA1_USB_EXTB_OC_L	OBSDATA_A1	OBSDATA_C1	XDP_DC1_MXM_GOOD
XDP_DA2_USB_EXTC_OC_L	OBSDATA_A2	OBSDATA_C2	XDP_DC2_DP_AUXCH_ISOL
XDP_DA3_USB_EXTD_OC_L	OBSDATA_A3	OBSDATA_C3	XDP_DC3_SATARDRVR_EN
TP_XDP_PCH_OBSFN_B<0>	OBSEN_B0	OBSEN_D0	TP_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_B<1>	OBSEN_B1	OBSEN_D1	TP_XDP_PCH_OBSFN_D<1>
XDP_DB0_USB_EXTB_OC_EHCI_L	OBSDATA_B0	OBSDATA_D0	XDP_DD0_DP_GPU_TBT_SEL
XDP_DB1_USB_EXTD_OC_EHCI_L	OBSDATA_B1	OBSDATA_D1	XDP_DD1_JTAG_ISP_TCK
XDP_DB2_AP_PWR_EN	OBSDATA_B2	OBSDATA_D2	XDP_DD2_AUD_IPHS_SWITCH_EN
XDP_DB3_SDCONN_STATE_CHANGE	OBSDATA_B3	OBSDATA_D3	XDP_DD3_ENET_LOW_PWR
XDP_PCH_S5_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	TP_XDP_PCH_HOOK4
XDP_PCH_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	TP_XDP_PCH_HOOK5
	VCC_OBS_AB	VCC_OBS_CD	
TP_XDPPCH_HOOK2	HOOK2	RESET#/HOOK6	XDPPCH_PLTRST_L
TP_XDPPCH_HOOK3	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_PCH_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	TP_XDP_PCH_TRST_L
	TCK1	TDI	XDP_PCH_TDI
XDP_PCH_TCK	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C2580 0.1UF 10% 10V X7R-CERM 0402
XDP C2581 0.1UF 10% 10V X7R-CERM 0402
518S0847

ALL_SYS_PWRGD	R2584 1K	XDP PLACE_NEAR=J2550.39:2.54mm 5% 1/20W MF 201
PM_PWRBTN_L	R2585 0	XDP PLACE_NEAR=U4900.P17:2.54mm 5% 1/20W MF 201

SYNC_MASTER=J30_MLB	SYNC_DATE=07/14/2011	
PAGE TITLE	CPU & PCH XDP	
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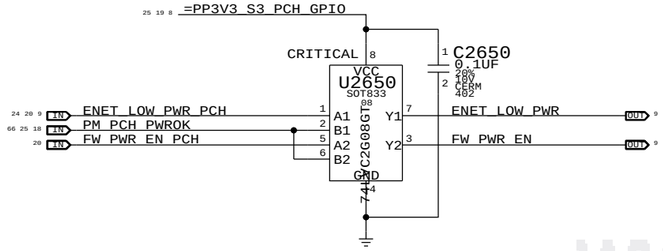
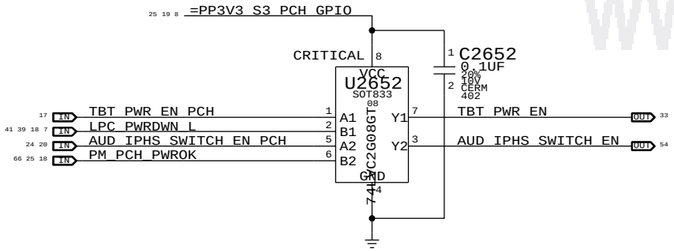
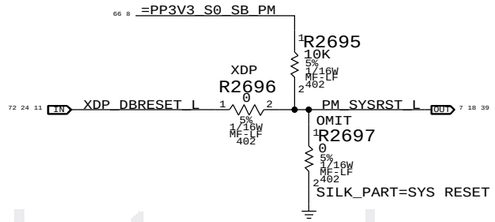
GPIO Glitch Prevention

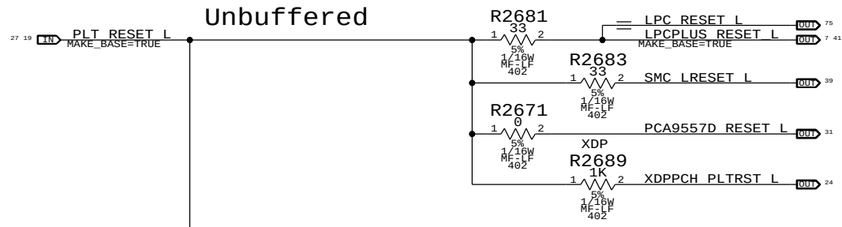




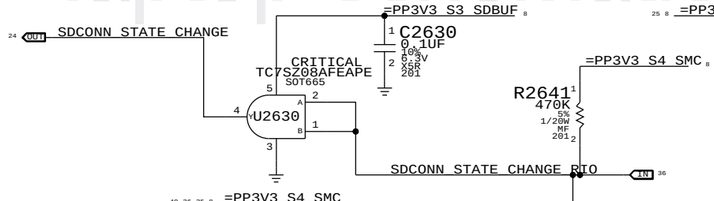
PCH Reset Button



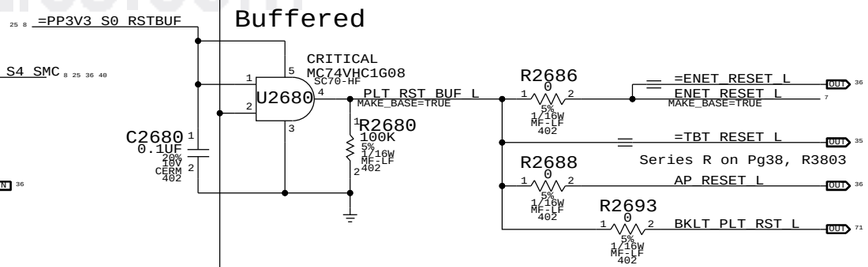
Platform Reset Connections



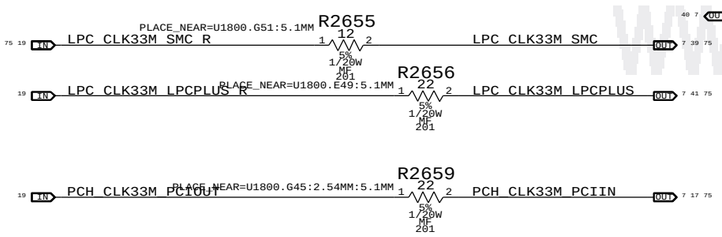
SDCONN_STATE_CHANGE ISOLATION



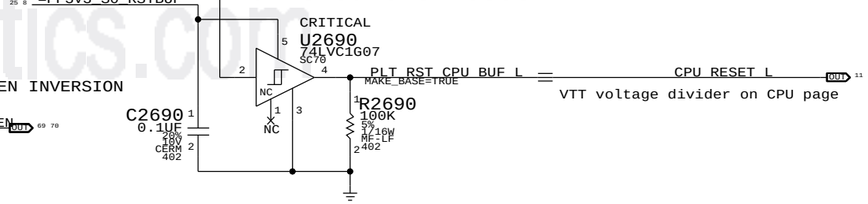
Buffered



33 MHz Clock Series Termination



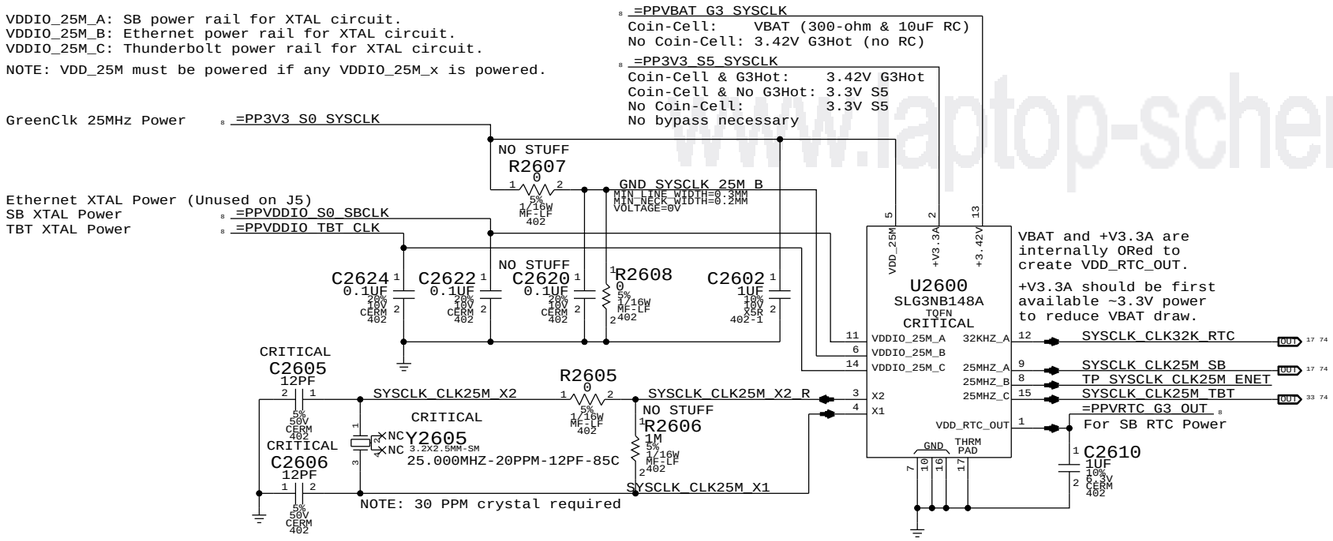
Buffered CPU reset



System RTC Power Source & 32kHz / 25MHz Clock Generator

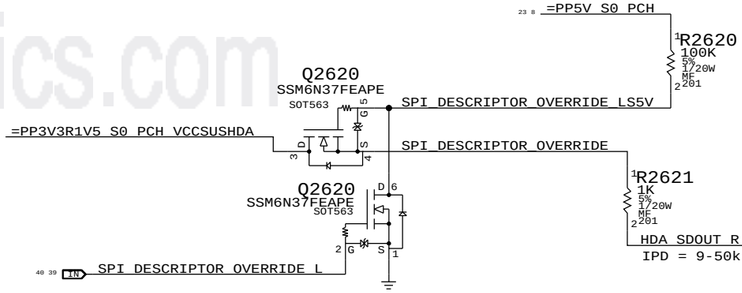
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Chipset Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

USB MUX FOR LS/FS INTERNAL DEVICES

NON_REM 1 : NON_REM 0 — STRAP PIN CFG

NON_REM 1	NON_REM 0	STRAP PIN CFG
0	0	ALL PORTS ARE REMOVABLE
0	1	PORT 1 IS NON REMOVABLE
1	0	PORT 1&2 ARE NON REMOVABLE
1	1	PORT 1&2&3 ARE NON REMOVABLE

CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STRAPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0485	1	XTAL,24MHZ,60PPM,16PF,2.5X2X0.55MM,90C	Y2700	CRITICAL	

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB:2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB:2513B
338S0983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB:2512B

D1,D2 ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
J3X ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B

=PP3V3_S3_USB_HUB — BYPASS=U27000.5::5MM — BYPASS=U2700.5::2MM

C2700 4.7UF 20% 6.3V X5R 603 — C2701 0.1UF 10% 10V X7R-CERM 0402 — C2702 0.1UF 10% 10V X7R-CERM 0402 — C2703 0.1UF 10% 10V X7R-CERM 0402

BYPASS=U2700.15::2MM — BYPASS=U2700.10::2MM — BYPASS=U2700.23::5MM — BYPASS=U2700.23::2MM

C2704 4.7UF 20% 6.3V X5R 603 — C2705 0.1UF 10% 10V X7R-CERM 0402 — C2706 0.1UF 10% 10V X7R-CERM 0402 — C2708 0.1UF 10% 10V X7R-CERM 0402

CRITICAL
Y2700 SM-2 OMIT_TABLE
24.000MHZ-16PF
BYPASS=U2700.36::2MM — BYPASS=U2650.29::2MM

CRITICAL C2709 18PF 5% 50V CERM 402 — R2700 1M 5% 1/10W MF-LF 402 — CRITICAL C2710 18PF 5% 50V CERM 402 — R2701 100 5% 1/16W MF-LF 402

HUB_NONREM1_1 — R2702 10K 5% 1/16W MF-LF 402 — R2703 10K 5% 1/16W MF-LF 402 — HUB_NONREM0_1

HUB_NONREM1_0 — R2704 10K 5% 1/16W MF-LF 402 — R2705 10K 5% 1/16W MF-LF 402 — HUB_NONREM0_0

R2706 10K 5% 1/16W MF-LF 402 — R2707 10K 5% 1/16W MF-LF 402

J5 USES 197S0181 FOR Y2700 DUE TO HEIGHT LIMITATION
J3X USE 197S0284 FOR Y2700 TO SAVE COST

PPUSB_HUB2_VDD1V8 MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM VOLTAGE=1.8V
PPUSB_HUB2_VDD1V8PLL MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM VOLTAGE=1.8V

C2711 0.1UF 10% 10V X7R-CERM 0402 — C2712 1UF 10% 10V X5R 402 — C2713 0.1UF 10% 10V X7R-CERM 0402 — C2714 1UF 10% 10V X5R 402

VDD33 — CRFILT — PLLFILT

SYM VER 1
U2700 USB2513B QFN OMIT_TABLE

TEST		USBDM_DN1/PRT_DIS_M1	1 USBHUB_DN1_N
RESET*		USBDP_DN1/PRT_DIS_P1	2 USBHUB_DN1_P
XTALIN/CLKIN		USBDM_DN2/PRT_DIS_M2	3 USBHUB_DN2_N
XTALOUT		USBDP_DN2/PRT_DIS_P2	4 USBHUB_DN2_P
SUSP_IND/LOCAL_PWR/NON_REM0		USBDM_DN3/PRT_DIS_M3	6 USBHUB_DN3_N
SDA/SMBDATA/NON_REM1		USBDP_DN3/PRT_DIS_P3	7 USBHUB_DN3_P
SCL/SMBCLK/CFG_SEL0		NC	8 USBHUB_DN4_N
HS_IND/CFG_SEL1		NC	9 USBHUB_DN4_P
		PRTPWR1/BC_EN1*	12 TP_USB_HUB_PRTPWR1
		PRTPWR2/BC_EN2*	16 TP_USB_HUB_PRTPWR2
		PRTPWR3/BC_EN3*	18 TP_USB_HUB_PRTPWR3
		NC	20 TP_USB_HUB_PRTPWR4
	IPU	OCS1*	13 TP_USB_HUB_OCS1
	IPU	OCS2*	17 TP_USB_HUB_OCS2
	IPU	OCS3*	19 TP_USB_HUB_OCS3
	IPU	NC	21 TP_USB_HUB_OCS4
		RBIAS	35 USB_HUB_RBIAS
		VBUS_DET	27 USB_HUB_VBUS_DET
		USBDM_UP	30 USB_HUB_UP_N
		USBDP_UP	31 USB_HUB_UP_P
THRM_PAD			37

CKPLUS_WAIVE=ndifpr_badterm
CRITICAL R2709 12K 1% 1/16W MF 402

PCH PORT 7 (EHCI1)

USB_HUB_TEST — USB_HUB_RESET_L — USB_HUB_XTAL1 — USB_HUB_XTAL2 — USB_HUB_NONREM0 — USB_HUB_NONREM1 — USB_HUB_CFG_SEL0 — USB_HUB_CFG_SEL1

BLUETOOTH FOR D1/D2 & J3X
TRACKPAD/KEYBOARD FOR D1/D2, IR FOR J3X
SMC DEBUG PORT FOR D1/D2, TPAD/KBD FOR J3X
NC FOR D1/D2, SMC DEBUG PORT FOR J3X

=PP3V3_S3_USB_HUB
NOSTUFF R2716 10K 5% 1/16W MF-LF 402 — NOSTUFF R2717 10K 5% 1/16W MF-LF 402 — NOSTUFF R2718 10K 5% 1/16W MF-LF 402 — NOSTUFF R2719 10K 5% 1/16W MF-LF 402 — NOSTUFF R2722 10K 5% 1/16W MF-LF 402 — NOSTUFF R2723 10K 5% 1/16W MF-LF 402

USBHUB_DN3_N — USBHUB_DN3_P — USBHUB_DN4_N — USBHUB_DN4_P — USBHUB_DN2_N — USBHUB_DN2_P

=PP3V3_S3_USB_HUB
R2708 10K 5% 1/16W MF-LF 402

TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R5701 & R5702, STUFF R2720 & R2721

NOSTUFF R2720 27 5% 1/16W MF-LF 402 — USB_EXTD_XHCI_N — USB_TPAD_R_N
NOSTUFF R2721 27 5% 1/16W MF-LF 402 — USB_EXTD_XHCI_P — USB_TPAD_R_P

TO PCH XHCI — TO TP/KB

=PP3V3_S3_USB_RESET
R2712 10K 5% 1/16W MF-LF 402 — USB_HUB_RESET_L
C2715 0.1UF 10% 10V X7R-CERM 0402
BYPASS=U2700.26::2MM

USB XHCI/EHCI2 PORT MUX FOR EXT B

=PP3V3_S3_USBMUX
C2760 0.1UF 20% 10V CERM 402

U2760 PI3USB102ZLE TQFN CRITICAL

PCH PORT 9 (EHCI2)	USB_EXTB_EHCI_P	M+	Y+ USB_EXTB_P
	USB_EXTB_EHCI_N	M-	Y- USB_EXTB_N
PCH PORT 1 (XHCI)	USB_EXTB_XHCI_P	D+	
	USB_EXTB_XHCI_N	D-	
		OE*	SEL USB_EXTB_SEL_XHCI
		VCC	
		GND	

TO CONNECTOR

PULL-UP TO 3.3V SUS ON PCH PAGE, SEL PIN IS LEAKAGE-SAFE
PCH GPIO60
SEL=0 CHOOSE USB EHCI2 PORT
SEL=1 CHOOSE USB XHCI PORT

SYNC_MASTER=J5 AMD SYNC_DATE=08/17/2011
PAGE TITLE: USB HUB & MUX
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 27 OF 132
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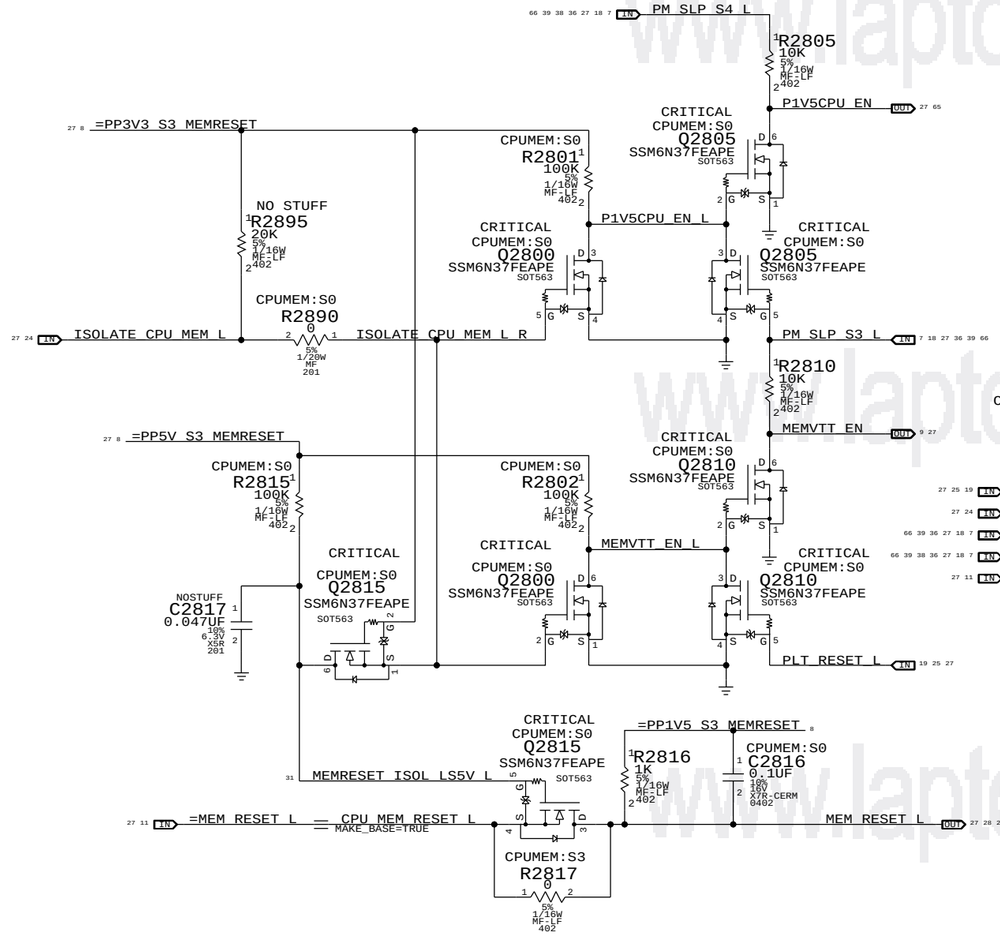
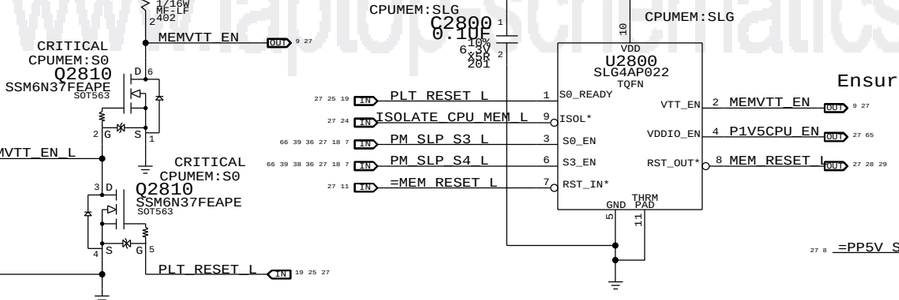
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

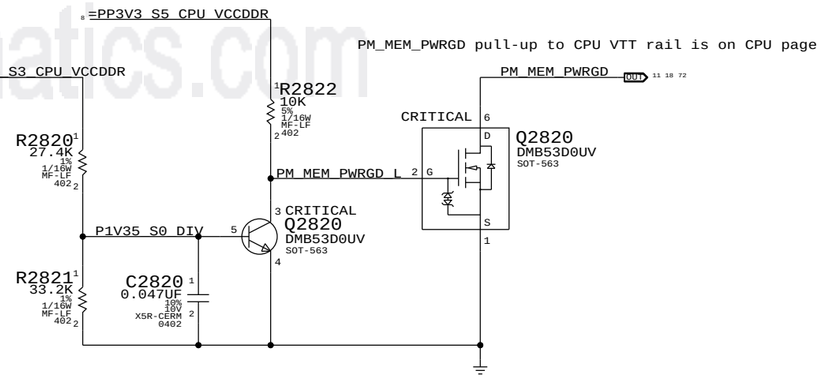
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



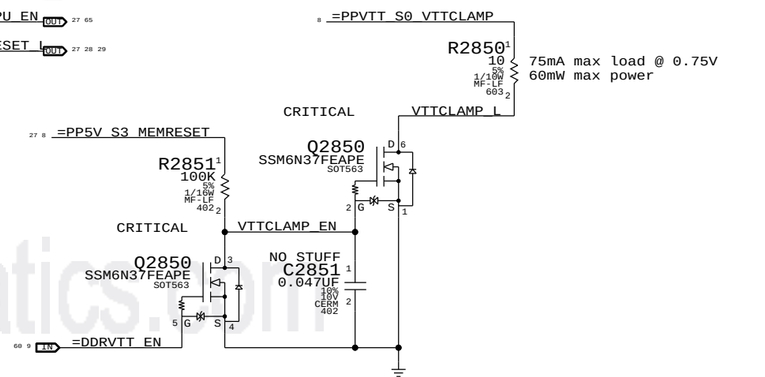


1V35 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
S3	5	0	1	1	1	0 (*)	1	1	1
to	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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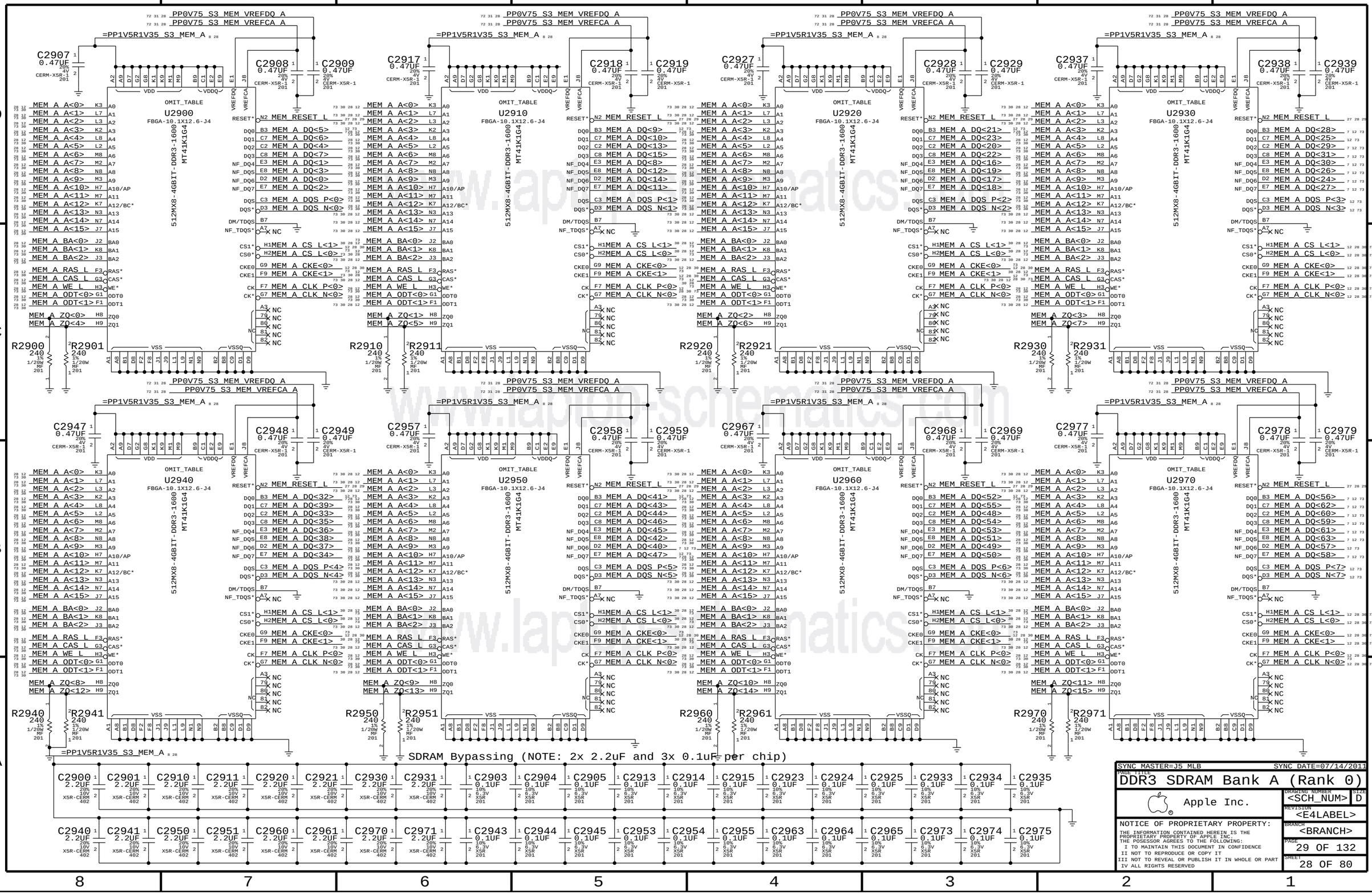

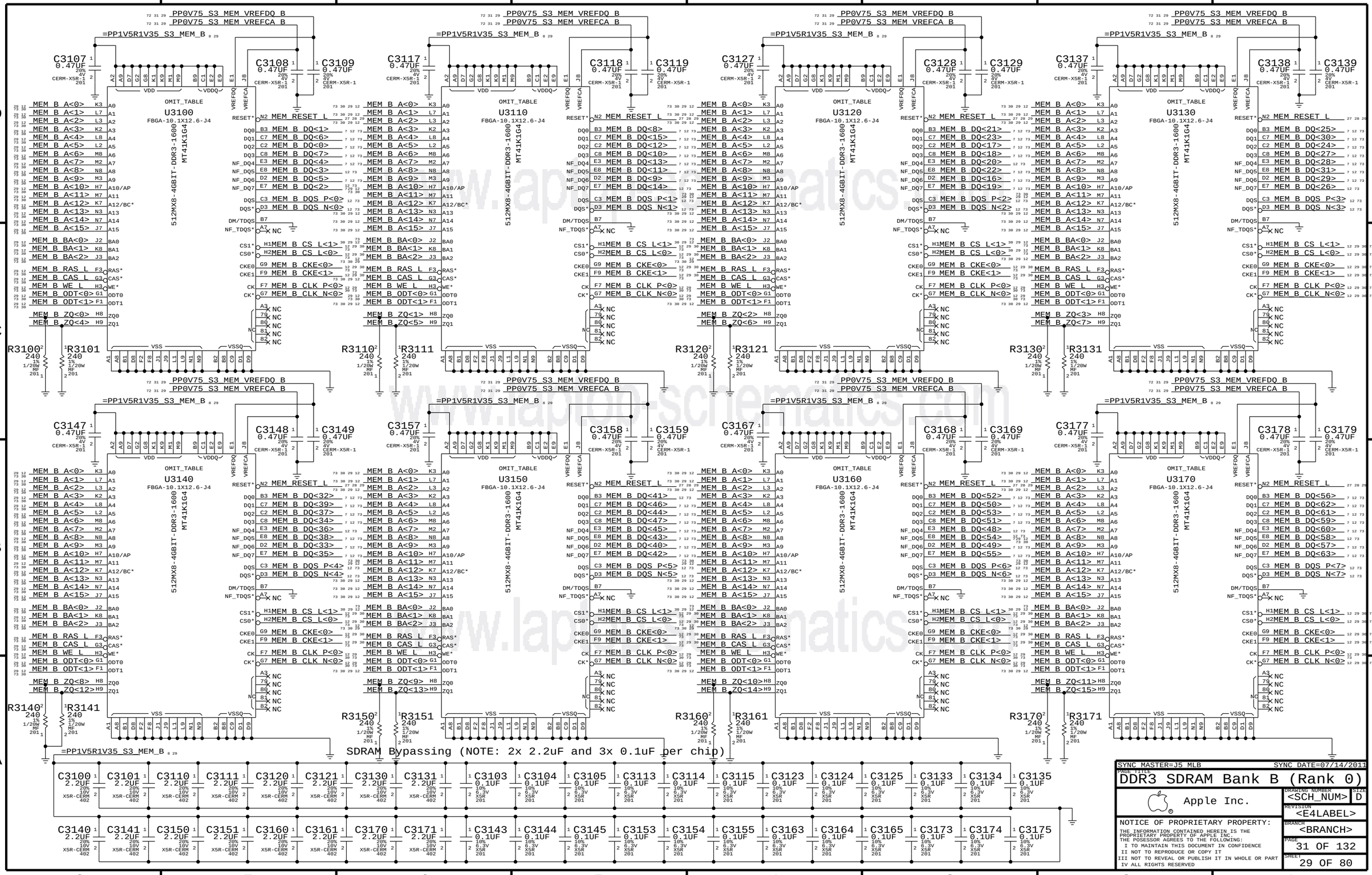
U3100
U3110
U3120
U3130
U3140
U3150
U3160
U3170
FBGA-10.1X12.6-J4
512MX8-4GBIT-DDR3-1600
MT41K1G4
OMIT_TABLE
=PP1V5R1V35_S3_MEM_B
PP0V75_S3_MEM_VREFDQ_B
PP0V75_S3_MEM_VREFCA_B
MEM_RESET_L
MEM_B_BA<0>
MEM_B_BA<1>
MEM_B_BA<2>
MEM_B_RAS_L
MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ODT<1>
MEM_B_CS_L<1>
MEM_B_CS_L<0>
MEM_B_CKE<0>
MEM_B_CKE<1>
MEM_B_CLK_P<0>
MEM_B_CLK_N<0>
MEM_B_DQS_P<0>
MEM_B_DQS_N<0>
MEM_B_ZQ<0>
MEM_B_ZQ<4>
MEM_B_ZQ<8>
MEM_B_ZQ<12>
SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)
SYNC_MASTER=J5_MLB
SYNC_DATE=07/14/2011
PAGE TITLE
DDR3 SDRAM Bank B (Rank 0)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
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29 OF 80
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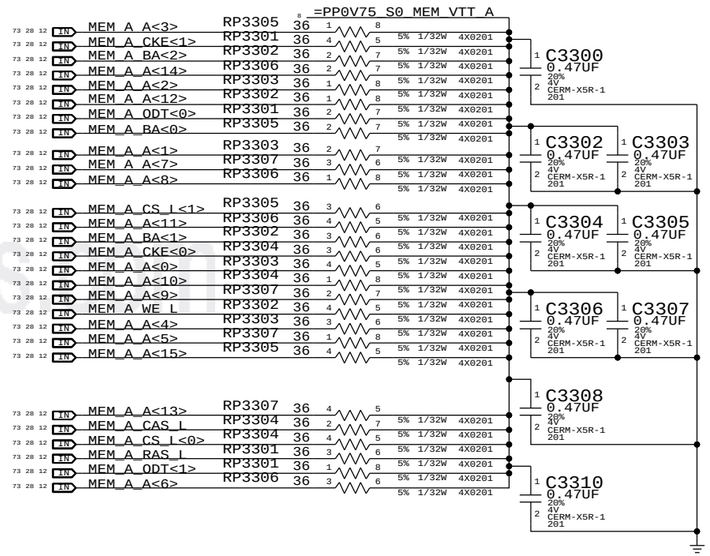
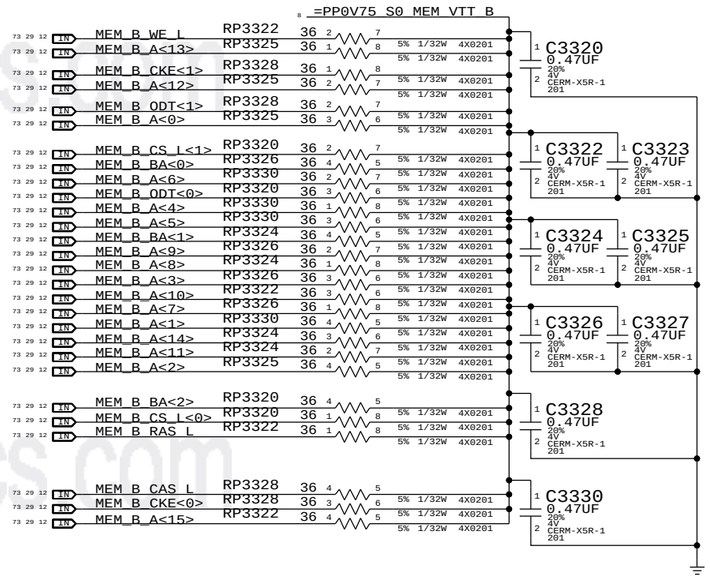
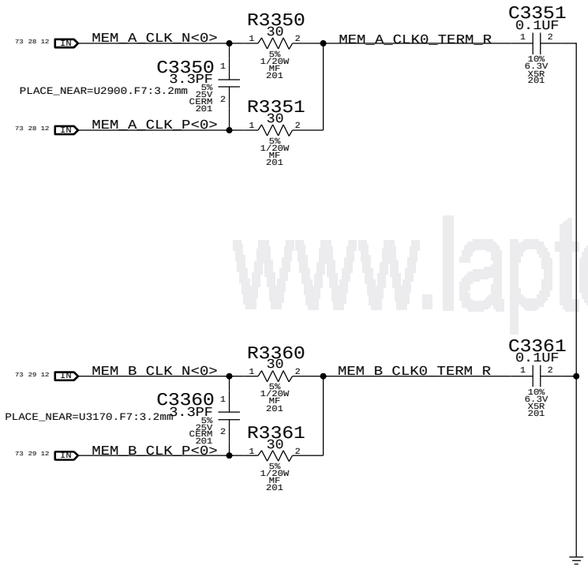
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE: DDR3 Termination

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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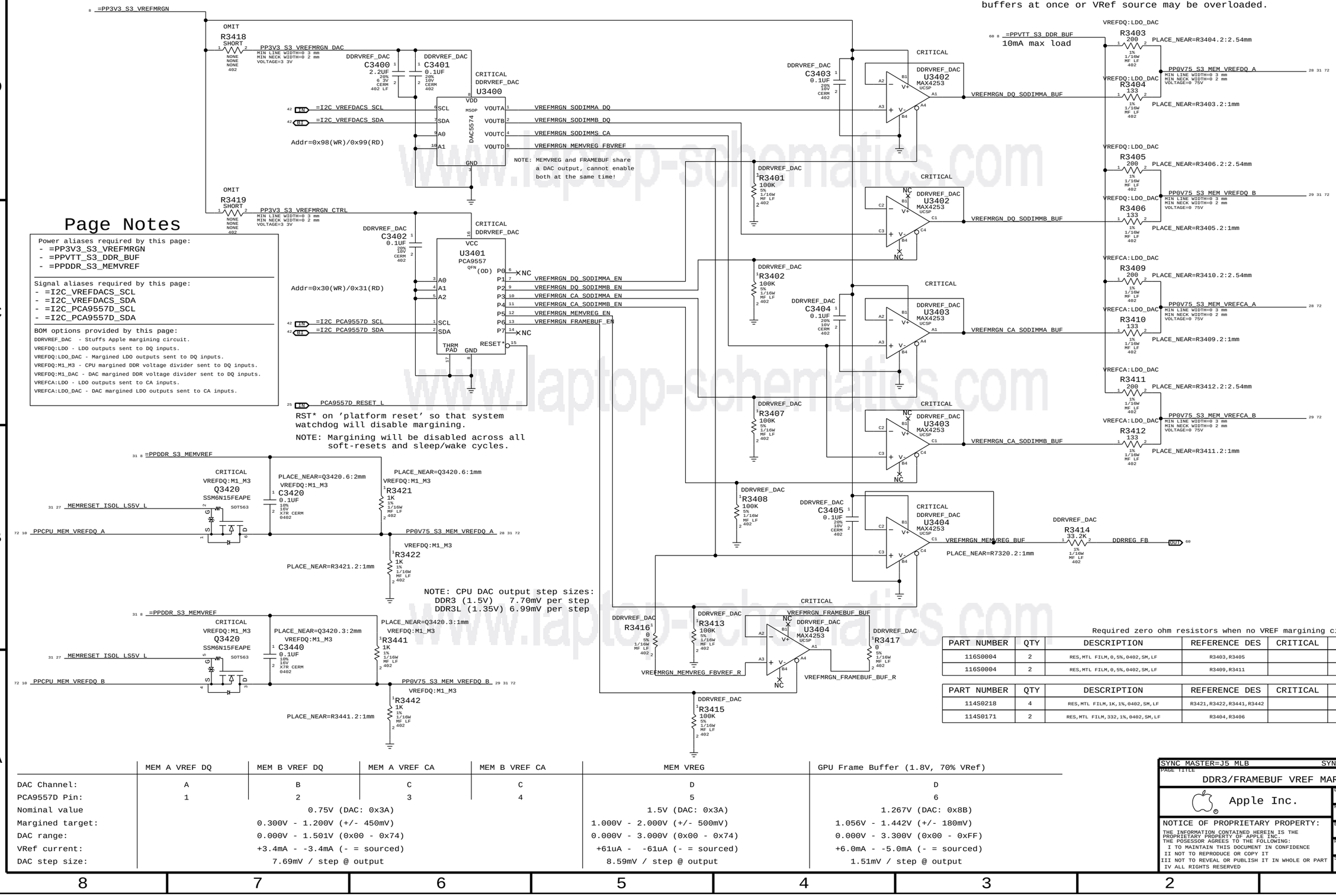

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs Apple margining circuit.
- VREFDQ:LDO - LDO outputs sent to DQ inputs.
- VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
- VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
- VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
- VREFCA:LDO - LDO outputs sent to CA inputs.
- VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=J5 MLB SYNC DATE=07/29/2011

PAGE TITLE: DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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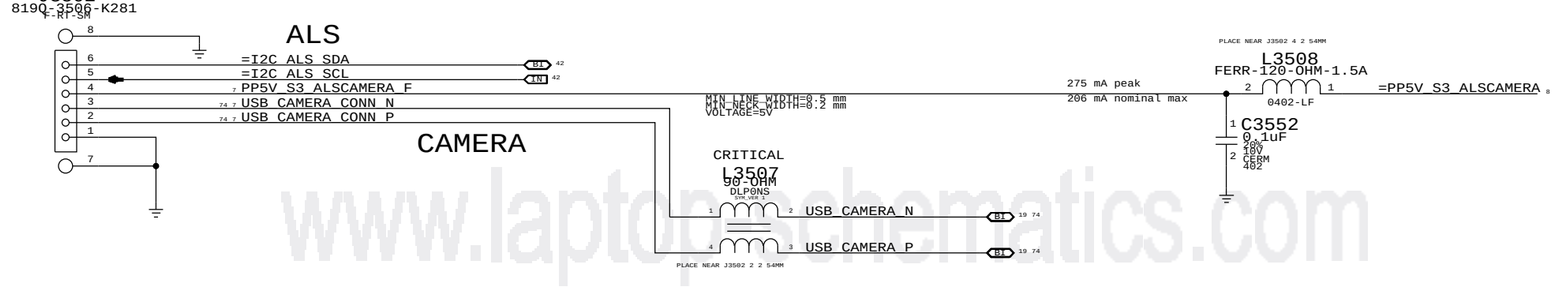
518S0767

CRITICAL
J3502
819Q-3506-K281
F-RT-SM



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
ALS/CAMERA CONNECTOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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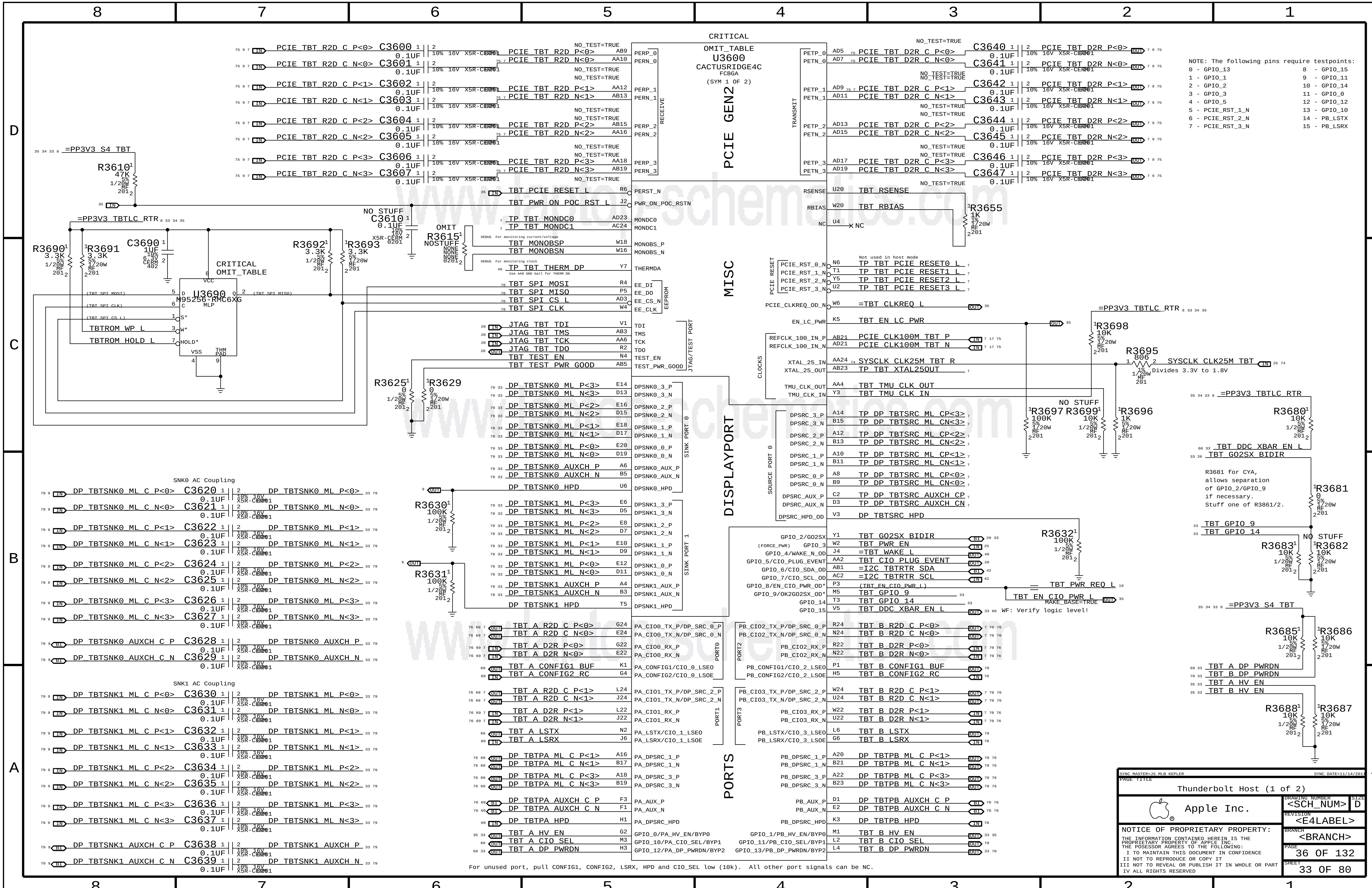
SHEET 32 OF 80


CRITICAL
OMIT_TABLE
U3600
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)
PCIE GEN2
MISC
DISPLAYPORT
PORTS
RECEIVE
TRANSMIT
EEPROM
JTAG/TEST PORT
PCIE RESET
CLOCKS
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_10
13 - PCIE_RST_0_N
14 - PB_LSTX
15 - PB_LSRX
=PP3V3_S4_TBT
=PP3V3_TBTLC_RTR
CRITICAL
OMIT_TABLE
U3690
M95256-RMC6XG
MLP
TBTROM_WP_L
TBTROM_HOLD_L
TBT_PCIE_RESET_L
TBT_PWR_ON_POC_RST_L
TBT_SPI_MOSI
TBT_SPI_MISO
TBT_SPI_CS_L
TBT_SPI_CLK
TBT_RSENSE
TBT_RBIAS
TBT_EN_LC_PWR
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
SYSCLK_CLK25M_TBT
Divides 3.3V to 1.8V
Not used in host mode
SNK0 AC Coupling
SNK1 AC Coupling
R3681 for CYA, allows separation of GPIO_2/GPIO_9 if necessary. Stuff one of R3861/2.
WF: Verify logic level!
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=J5_MLB_KEPLER
SYNC_DATE=11/14/2011
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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SHEET 33 OF 80
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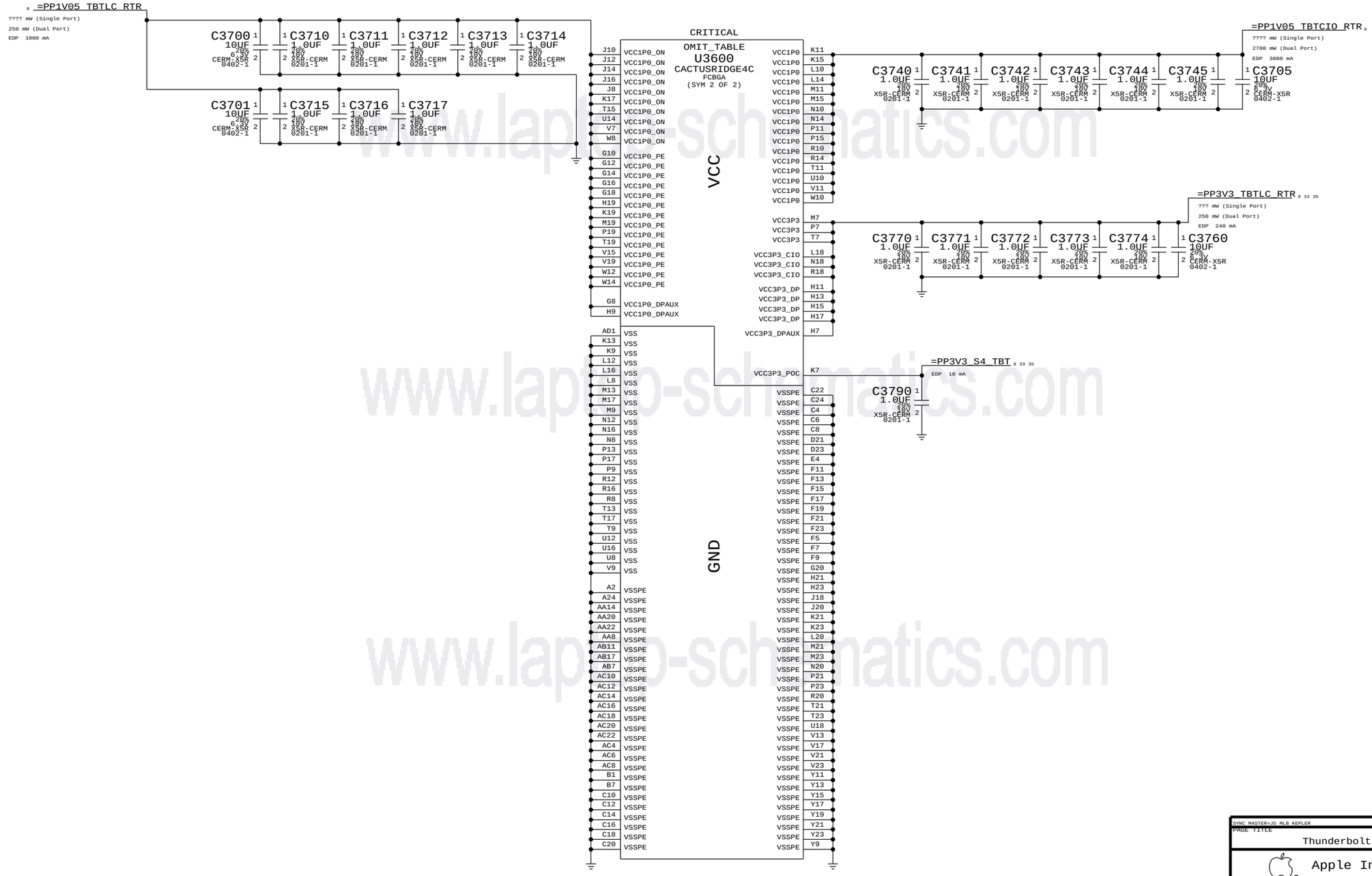

SYNC MASTER=J5 MLB KEPLER SYNC DATE=11/14/2011

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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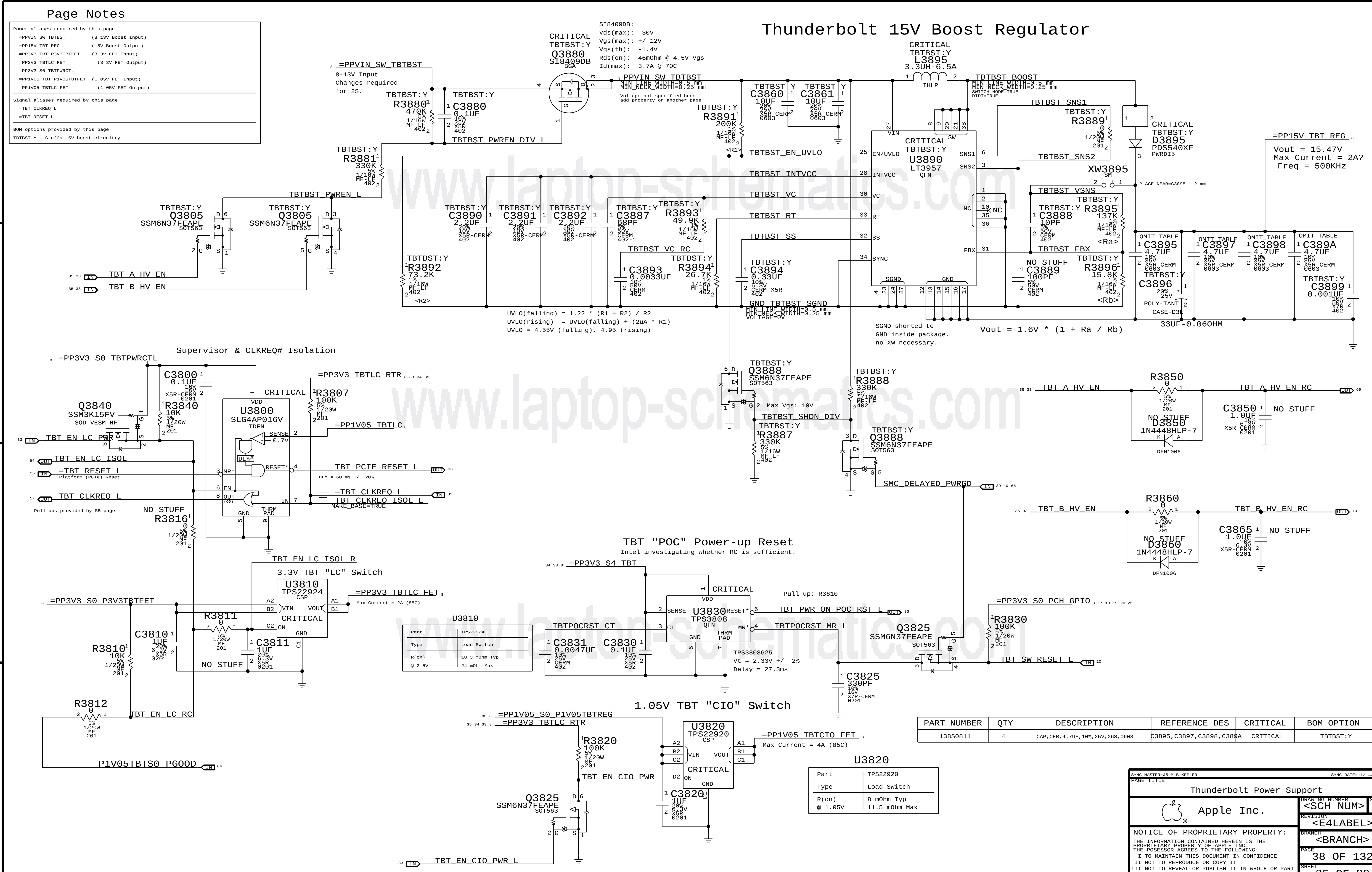
Thunderbolt 15V Boost Regulator



U3810	
Part	TPS22924C
Type	Load Switch
R(on) @ 2 5V	18 3 mOhm Typ 24 mOhm Max

U3820	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	4	CAP,CER,4.7UF,10%,25V,X6S,0603	C3895,C3897,C3898,C389A	CRITICAL	TBTBST:Y

SYNC MASTER=J5 MLB KEPLER SYNC DATE=11/14/2011

PAGE TITLE: Thunderbolt Power Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0OHM, 0201	L4470,L4471,L4473,L4474		

3V S3 WLAN FET

DEBUG CURRENT SENSE RD135 connects to PP3V3_WLAN_F

AIRPORT

U4450 TPS22924 CSP CRITICAL

Max Current = 2A (85C)

Part	TPS22924C
Type	Load Switch
R(on)	18 3 mOhm Typ
@ 2 5V	24 mOhm Max

RIO POWER CONNECTOR

CRITICAL J4400 504050-0691 M-RT-SM

518s0862

RIO FLEX CONNECTOR

CRITICAL J4410 DF40CG3.0-70DS-0.4V F-ST-SM

516S1058

*NOTE: This connector is shielded 70P Hirose Receptacle.

Note: This receptacle mates with the plug with APN 998-4708.

Supervisor & CLKFREG # Isolation

Delay = 130 ms +/- 20%

SIGNAL_MODEL=MOJO_MUX

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

APN:311S0302

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: RIO CONNECTORS

Apple Inc.

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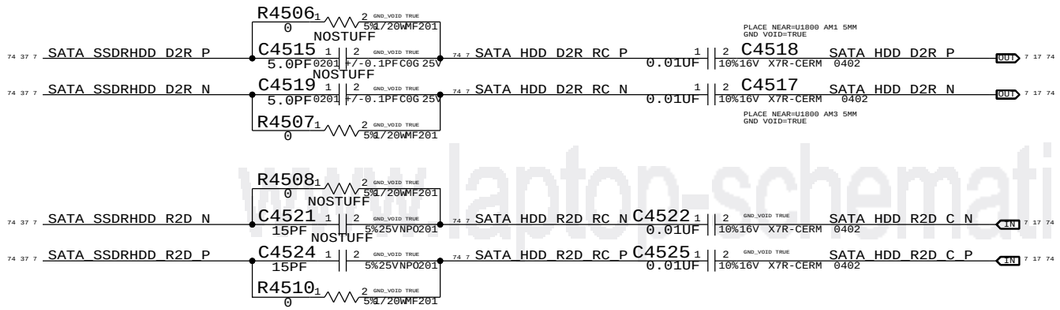
C4518 & C4517 Placement Note:
It is critical that these two should be near
to U1800 pin AM1 and AM3.

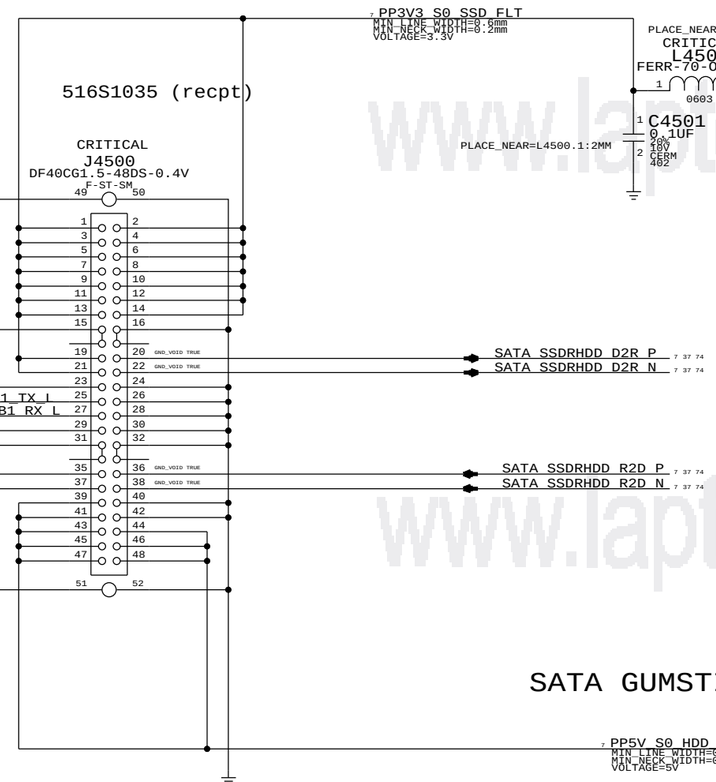
D2R Passive DeEmphasis

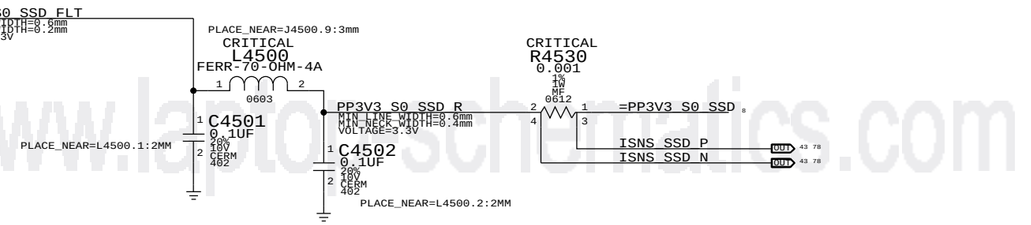
VALUE: 0.0 DB



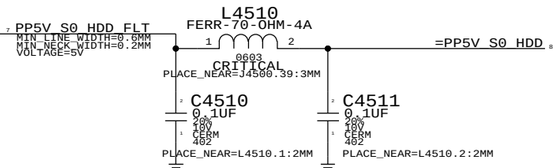
R2D Passive DeEmphasis

VALUE: 0.0 DB





SATA GUMSTICK2 CONNECTOR



SYNC_MASTER=MASTER	SYNC_DATE=MASTER
PAGE TITLE	SSD/HDD Connectors
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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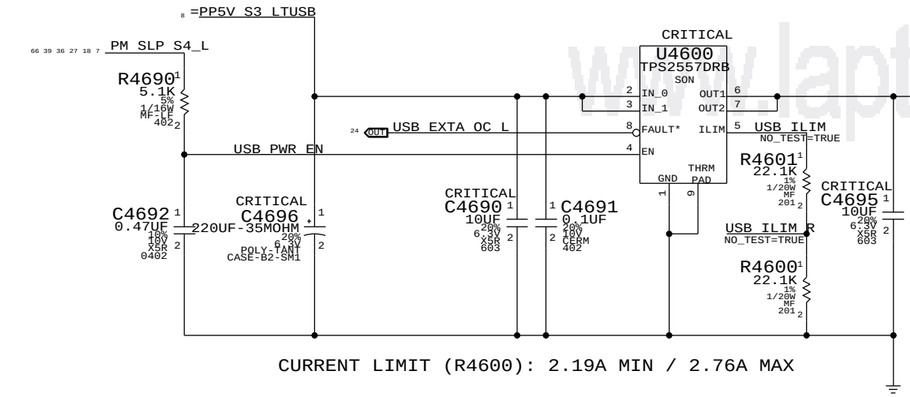
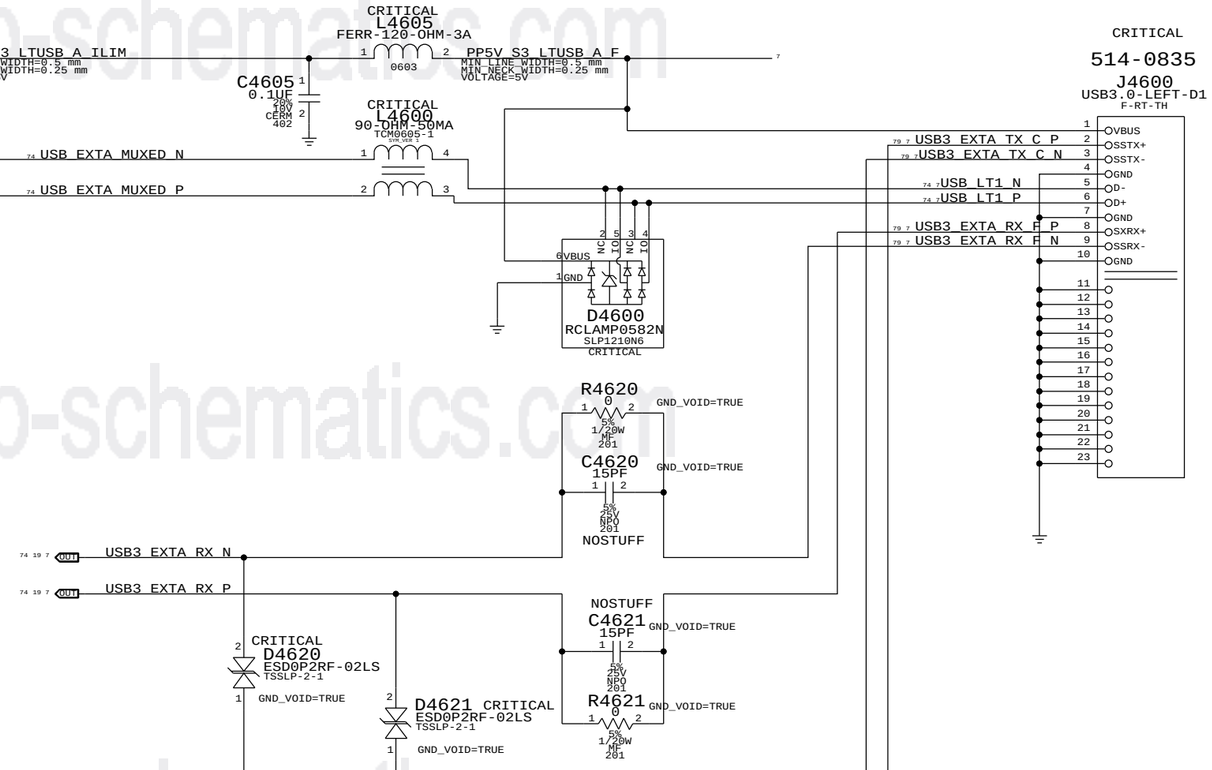
USB Port Power Switch

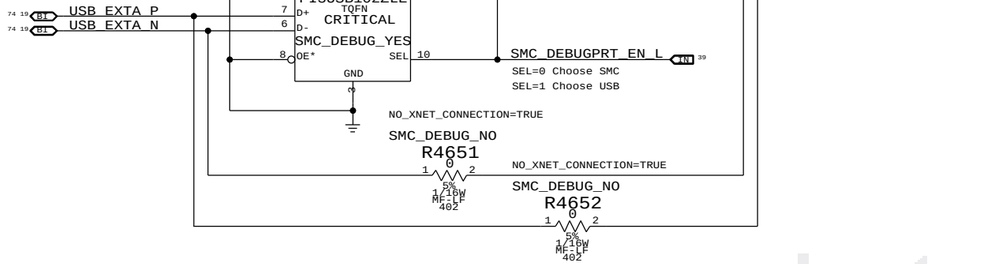


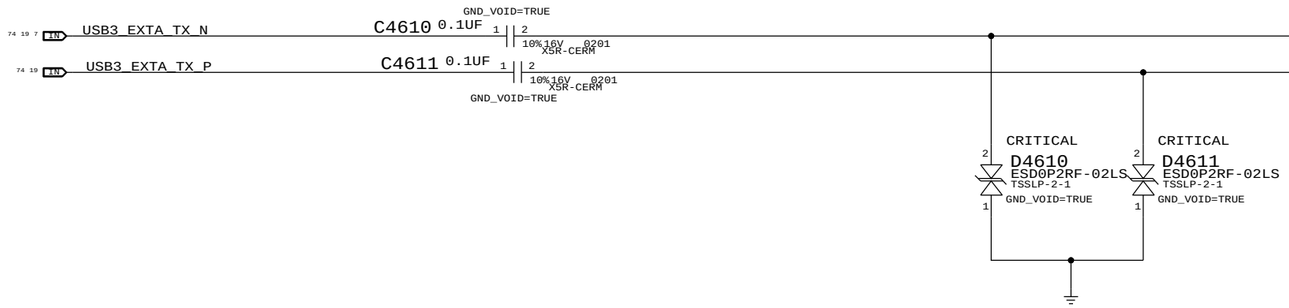
CURRENT LIMIT (R4600): 2.19A MIN / 2.76A MAX

Left USB Port A



USB/SMC Debug Mux





SYNC_MASTER=J5_AMD SYNC_DATE=08/24/2011

PAGE TITLE: USB 3.0 CONNECTORS

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 46 OF 132
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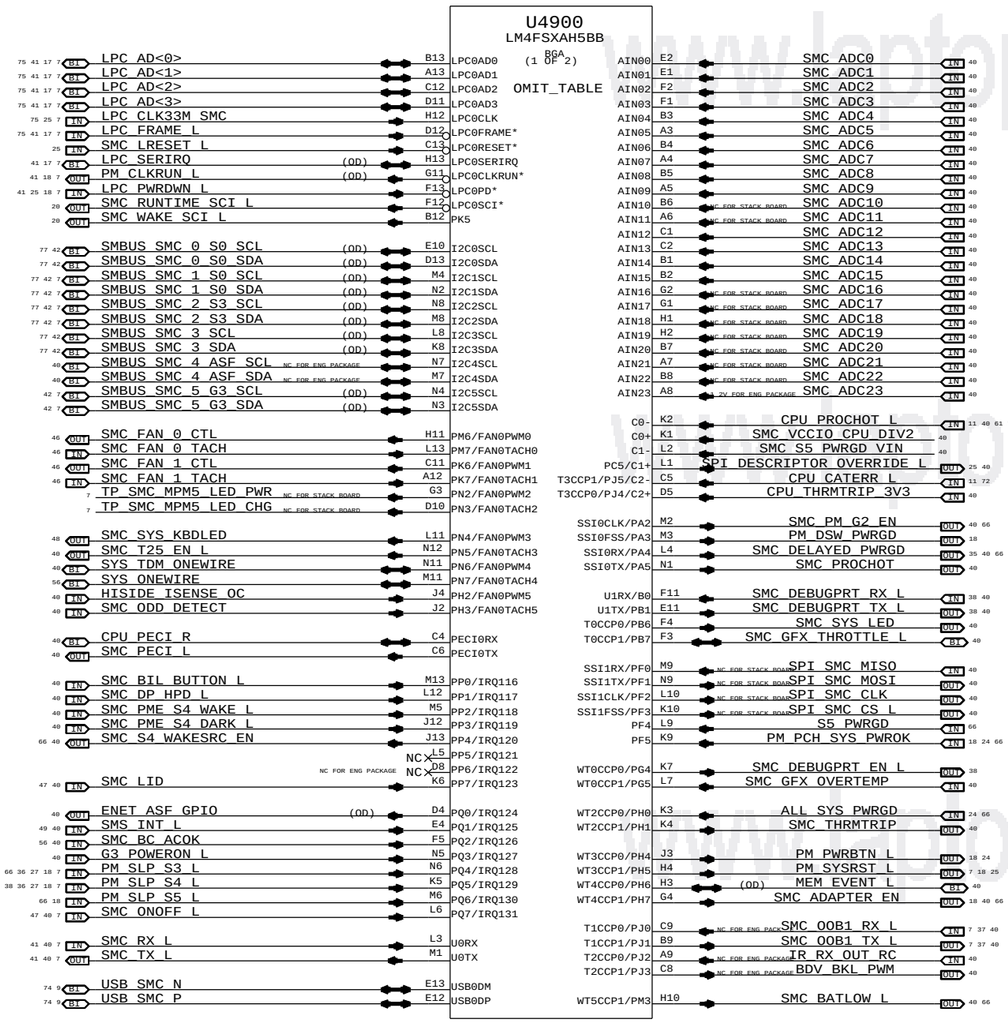
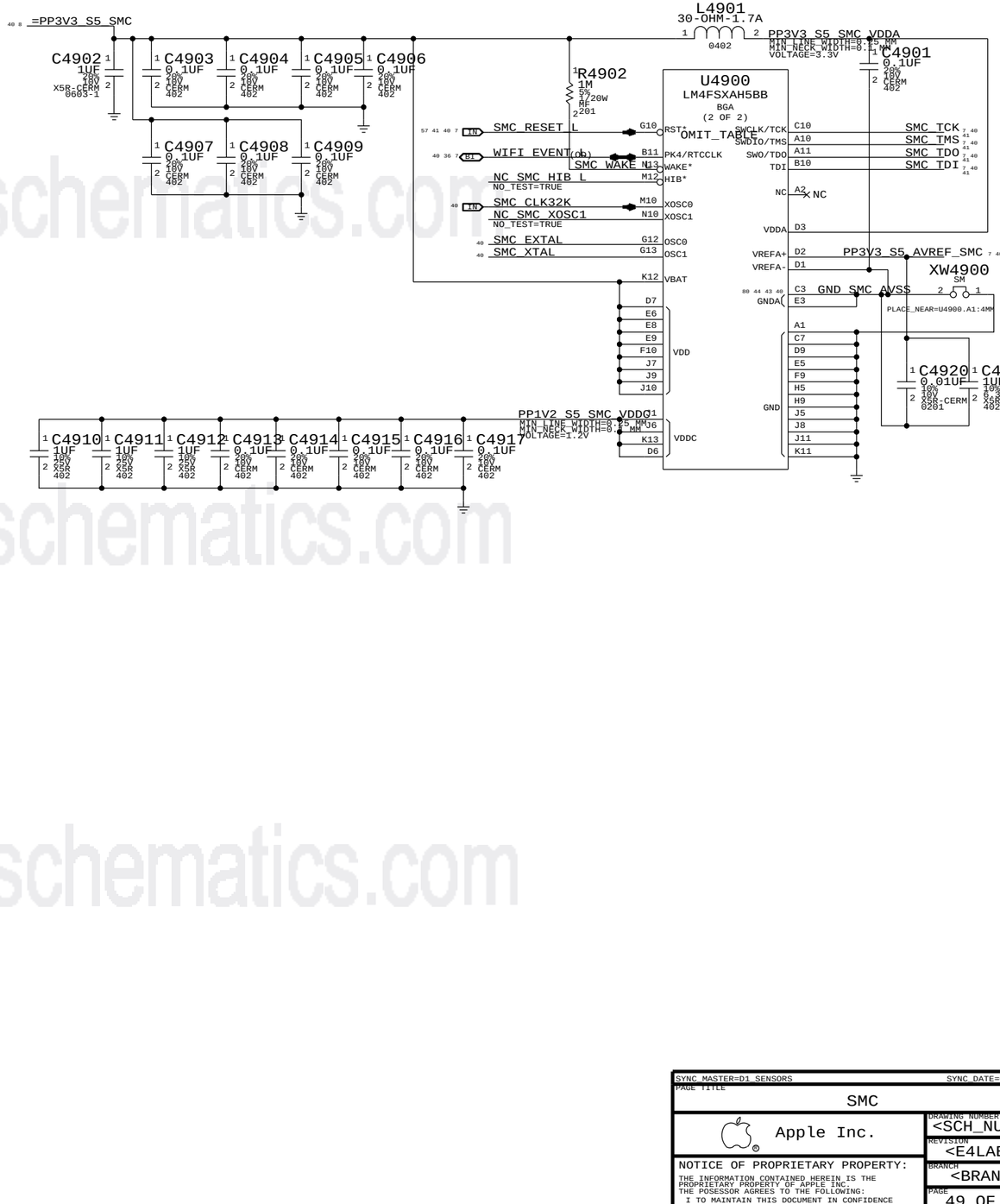
NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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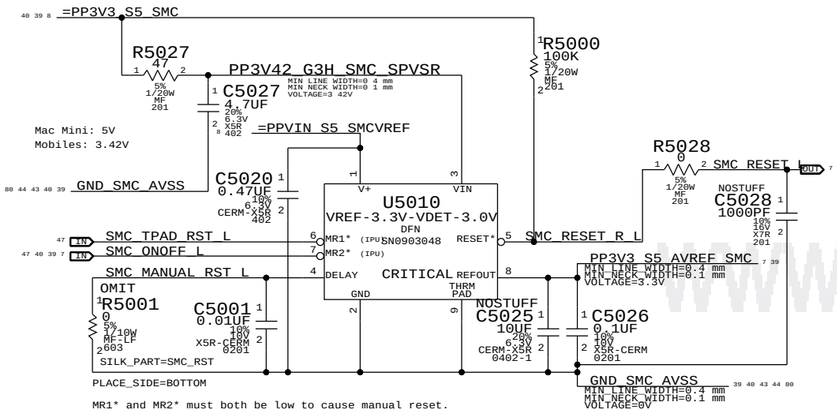
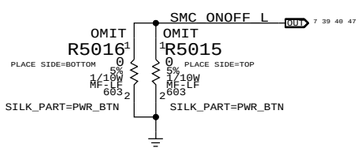
SMC Reset "Button", Supervisor & AVREF Supply



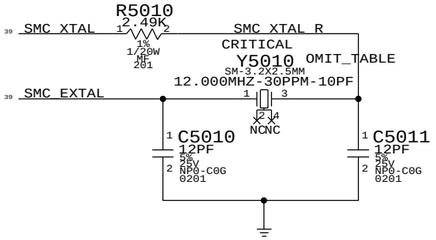
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



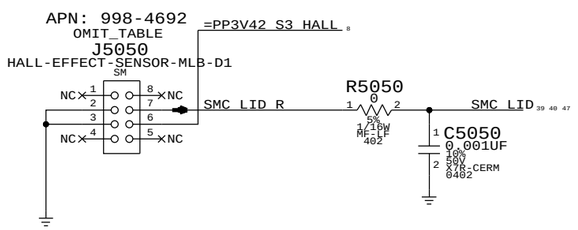
SMC Crystal Circuit



SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0486	1	XTAL,12MHZ,30PPM,10PF,3.2X2.5X0.7MM,90C	Y5010	CRITICAL	

Hall Effect pads



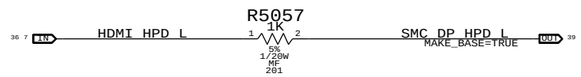
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-9320	1	SUBASSY,PCBA HALL EFFECT,J4	J5050	CRITICAL	

639-3261 (J4 Hall effect board) reports to 607-9320

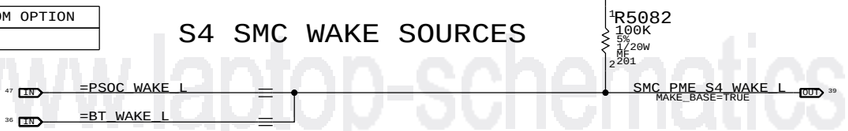
SMC_BC_ACOK / SMC_ADC* / SMC_PME_S4_DARK_L

=CHGR_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE
HISIDE_ISENSE_OC	NC_HISIDE_ISENSE_OC	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC0	SMC_CPU_VSENSE	MAKE_BASE=TRUE
SMC_ADC1	SMC_CPU_ISENSE	MAKE_BASE=TRUE
SMC_ADC2	NC_SMC_GPU_HI_ISENSE	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC3	SMC_DCIN_VSENSE	MAKE_BASE=TRUE
SMC_ADC4	SMC_DCIN_ISENSE	MAKE_BASE=TRUE
SMC_ADC5	SMC_PBUS_VSENSE	MAKE_BASE=TRUE
SMC_ADC6	SMC_SSD_ISENSE	MAKE_BASE=TRUE
SMC_ADC7	SMC_BMON_ISENSE	MAKE_BASE=TRUE
SMC_ADC8	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE
SMC_ADC9	SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE
SMC_ADC10	SMC_MEM_ISENSE	MAKE_BASE=TRUE
SMC_ADC11	SMC_VCCIO_ISENSE	MAKE_BASE=TRUE
SMC_ADC12	SMC_AXG_VSENSE	MAKE_BASE=TRUE
SMC_ADC13	SMC_CPU_SA_ISENSE	MAKE_BASE=TRUE
SMC_ADC14	SMC_CPU_SA_VSENSE	MAKE_BASE=TRUE
SMC_ADC15	SMC_LCD_PANEL_ISENSE	MAKE_BASE=TRUE
SMC_ADC16	SMC_LCDBKLT_VSENSE	MAKE_BASE=TRUE
SMC_ADC17	SMC_LCDBKLT_ISENSE	MAKE_BASE=TRUE
SMC_ADC18	SMC_AXG_ISENSE	MAKE_BASE=TRUE
SMC_ADC19	NC_SMC_GPU_P1V35_ISENSE	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC20	NC_SMC_T25_ISENSE	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC21	NC_SMC_PCH_CORE_ISENSE	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC22	SMC_X29_ISENSE	MAKE_BASE=TRUE
SMC_ADC23	SMC_TBT_ISENSE	MAKE_BASE=TRUE
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
BDV_BKL_PWM	NC_BDV_BKL_PWM	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PME_S4_DARK_L	SDCONN_STATE_CHANGE_SMC	MAKE_BASE=TRUE
	=TBT_WAKE_L	

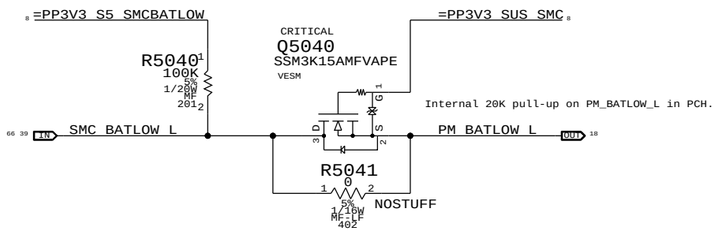
HDMI HPD ESD PROTECTION



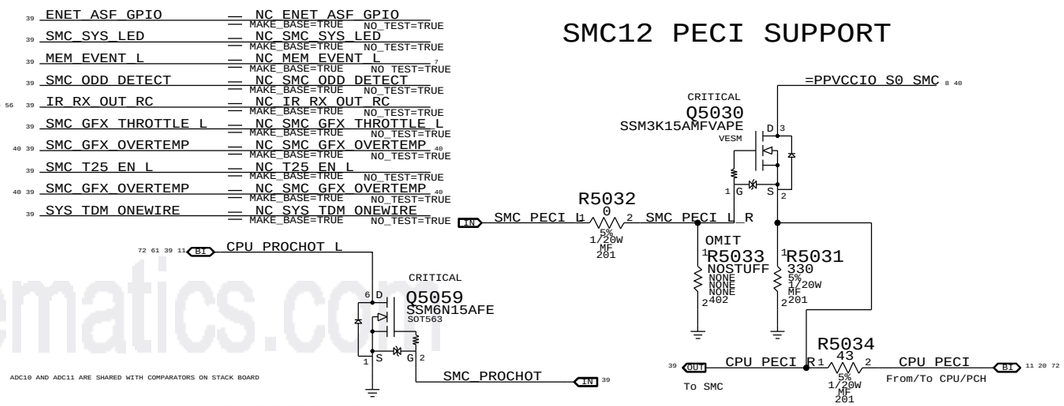
S4 SMC WAKE SOURCES



BATLOW# ISOLATION

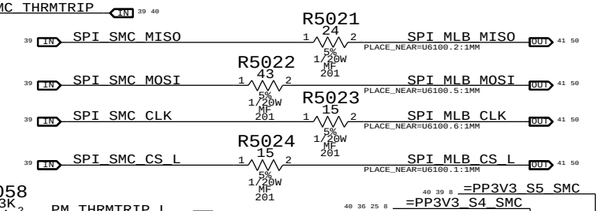


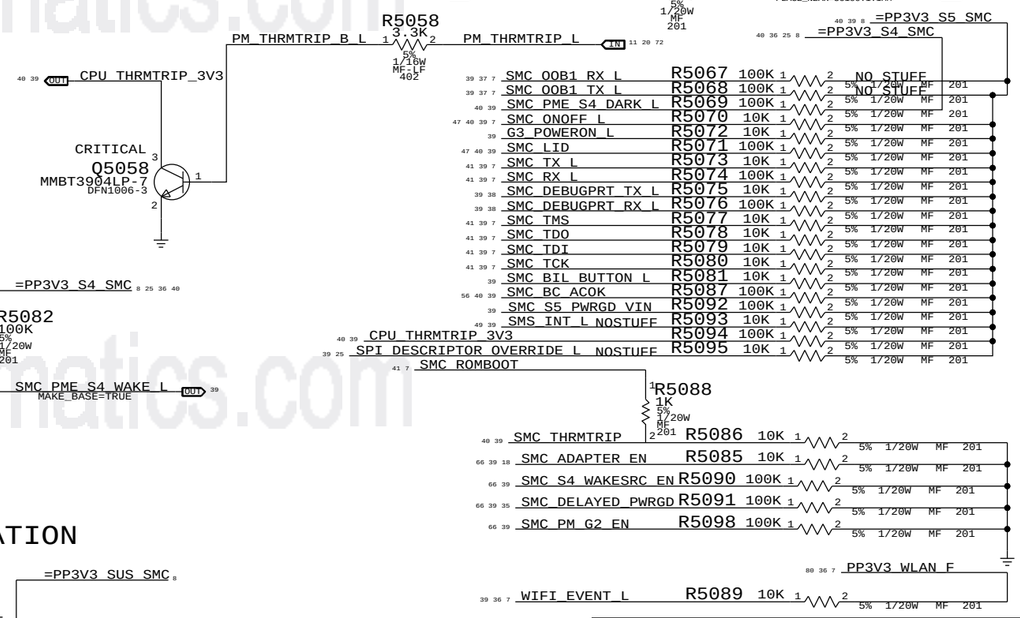
SMC12 PECI SUPPORT



SMC12 SPI SUPPORT

SERIES RESISTORS ARE NO STUFFED UNTIL THE TOPOLOGY OF 2 SPI MASTERS IS VERIFIED





SYNC_MASTER=D1_SENSORS	SYNC_DATE=02/20/2012
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
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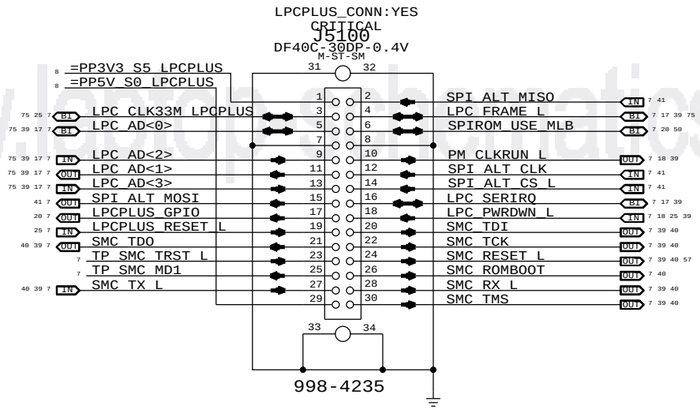
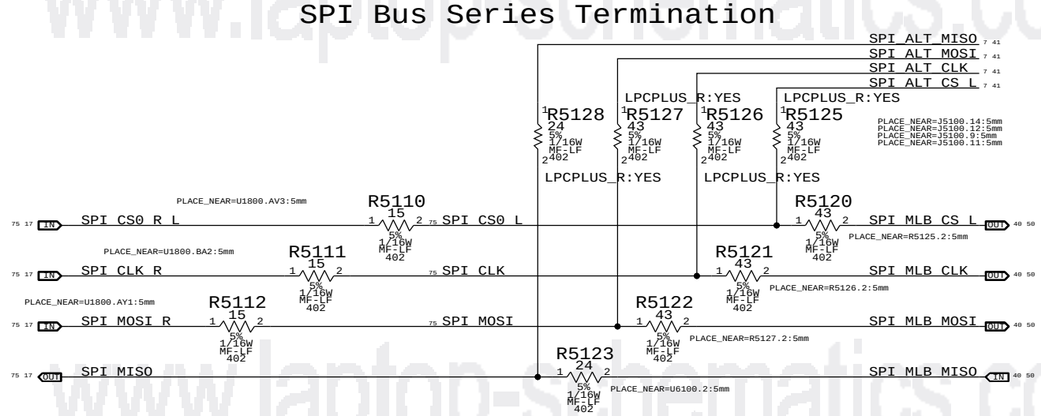
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 51 OF 132
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PCH SMBus "0" Connections

=PP3V3_S0_SMBUS_PCH

Panther Point
U1800
(MASTER)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

R5200 1K 5% 1/20W MF 201
R5201 1K 5% 1/20W MF 201

TBT
U3600
(WRITE: 0XX READ: 0XX)
=I2C_TBTRTR_SCL
=I2C_TBTRTR_SDA

VRef DACs
U3300
(Write: 0x98 Read: 0x99)
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA

AUDIO
U6411
(WRITE: 0X34 READ: 0X35)

Margin Control
U3301
(Write: 0x30 Read: 0x31)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA

AUDIO
U6410
(WRITE: 0X32 READ: 0X33)

MIKEY
U6751
(WRITE: 0X72 READ: 0X73)
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA

AUDIO
U6400
(WRITE: 0XE0 READ: 0XE1)

XDP Connectors
J2500 & J2550
(MASTER)
=SMBUS_XDP_SCL
=SMBUS_XDP_SDA

AUDIO
U6750
(WRITE: 0X76 READ: 0X77)

HDMI Redriver (on RIO)
J4410
(WRITE: 0xCC READ: 0xCD)
=I2C_HDMIRDRV_SCL
=I2C_HDMIRDRV_SDA

LED BACKLIGHT
U9700
(WRITE: 0X58 READ: 0X59)
=I2C_BKL_1_SCL
=I2C_BKL_1_SDA

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

SMC
U4900
(MASTER)
SMB_0_S0_CLK
SMB_0_S0_DATA

R5250 4.7K 5% 1/20W MF 201
R5251 4.7K 5% 1/20W MF 201

SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE

GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)
=SMBUS_GPUTHMSNS_SCL
=SMBUS_GPUTHMSNS_SDA

SMC "5" SMBUS CONNECTIONS

=PP3V42_G3H_SMBUS_SMC_5

SMC
U4900
(MASTER)
SMB_5_CLK
SMB_5_DATA

R5280 2.0K 5% 1/20W MF 201
R5281 2.0K 5% 1/20W MF 201

SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
MAKE_BASE=TRUE

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA

Battery
J6955
(See Table)
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA

Battery
Battery Manager - (Write: 0x16 Read: 0x17)

SMC "2" SMBUS CONNECTIONS

NOTE SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_2_S3

SMC
U4900
(MASTER)
SMB_2_S3_CLK
SMB_2_S3_DATA

R5270 1K 5% 1/20W MF 201
R5271 1K 5% 1/20W MF 201

SMBUS_SMC_2_S3_SCL
SMBUS_SMC_2_S3_SDA
MAKE_BASE=TRUE

Trackpad
J5800
(Write: 0x90 Read: 0x91)
=I2C_TPAD_SCL
=I2C_TPAD_SDA

ALS
J3502
(Write: 0x72 Read: 0x73)
=I2C_ALS_SCL
=I2C_ALS_SDA

SMS
U5920
(WRITE: 0X30/31 READ: 0X32/33)
=I2C_SMC_SMS_SCL
=I2C_SMC_SMS_SDA

GYRO
U5940
(WRITE: 0XD0 READ: 0XD1)
=I2C_SMC_GYRO_SCL
=I2C_SMC_GYRO_SDA

SMC "3" SMBUS CONNECTIONS

=PP3V3_S3_SMBUS_SMC_3

SMC
U4900
(MASTER)
SMB_3_CLK
SMB_3_DATA

DEBUG_ADC
R5290 4.7K 5% 1/20W MF 201
DEBUG_ADC
R5291 4.7K 5% 1/20W MF 201

SMBUS_SMC_3_SCL
SMBUS_SMC_3_SDA
MAKE_BASE=TRUE

DEBUG SENSOR ADC A
UD000
(Write: 0x10 Read: 0x11)
=I2C_SMC_ADCS_SCL
=I2C_SMC_ADCS_SDA

PCH "SMLink 0" Connections

=PP3V3_S0_SMBUS_PCH

Panther Point
U1800
(MASTER)
SML_PCH_0_CLK
SML_PCH_0_DATA
MAKE_BASE=TRUE

R5210 8.2K 5% 1/20W MF 201
R5211 8.2K 5% 1/20W MF 201

SMC "1" SMBUS CONNECTIONS

=PP3V3_S0_SMBUS_SMC_1_S0

SMC
U4900
(MASTER)
SMB_1_S0_CLK
SMB_1_S0_DATA

R5260 1K 5% 1/20W MF 201
R5261 1K 5% 1/20W MF 201

SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA
MAKE_BASE=TRUE

CPU/DDR3/PCH/AIRFLOW TEMP
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)
=I2C_CPUTHMSNS_SCL
=I2C_CPUTHMSNS_SDA

PCH "SMLink 1" Connections

Panther Point
U1800
(Write: 0x88 Read: 0x89)
SML_PCH_1_CLK
SML_PCH_1_DATA

SMLink 1 is slave port to access PCH & CPU via PECI.

X29 TEMP
TMP105: U5523
(WRITE: 0X92 READ: 0X93)
=I2C_X29THMSNS_SCL
=I2C_X29THMSNS_SDA

SPKR TEMP
U6420
(WRITE: 0XD8 READ: 0XD9)
U6421
(WRITE: 0X38 READ: 0X39)
=I2C_SPKRTHMSNS_SCL
=I2C_SPKRTHMSNS_SDA

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
SMBus Connections

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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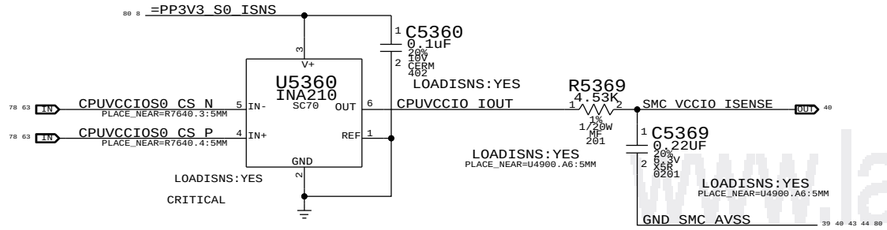
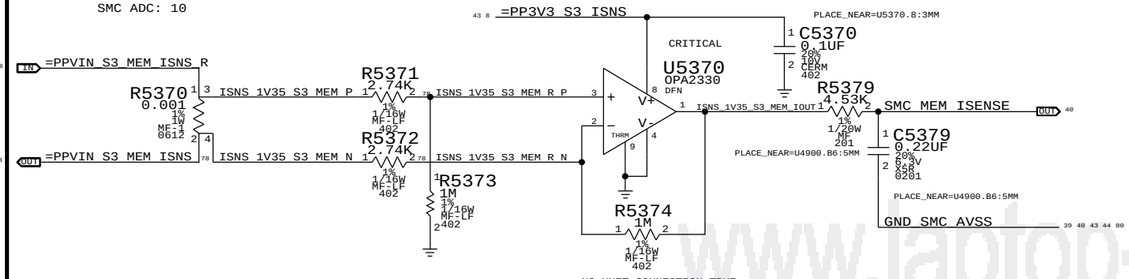
CPU/PCH VCCIO & TBT 1.05V Load Side Current Sense (IC1C)

Gain: 200x, EDP: 20 A
Rsense: 0.001 (R7640)
V across Rsense: 15 mV
SMC ADC: 11



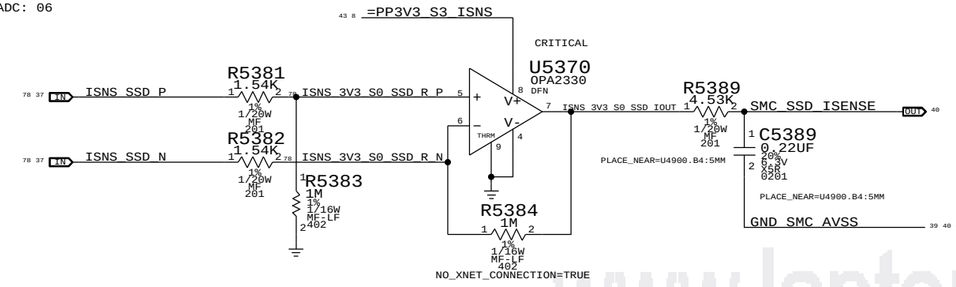
DDR 1.35V S3 (Memory) Current Sense (IM0C)

Gain: 364.9x, EDP: 9 A
Rsense: 0.001 (R5370)
V across Rsense: 9 mV
SMC ADC: 10



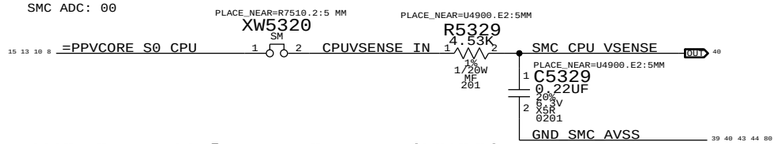
SSD Current Sense (ISDC)

Gain: 649.35x, EDP: 5 A (16.5 W)
Rsense: 0.001 (R5370)
V across Rsense: 5 mV
SMC ADC: 06



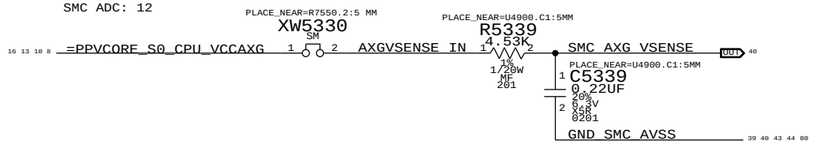
CPU Core Voltage Sense (VC0C)

Gain: 1x
SMC ADC: 00



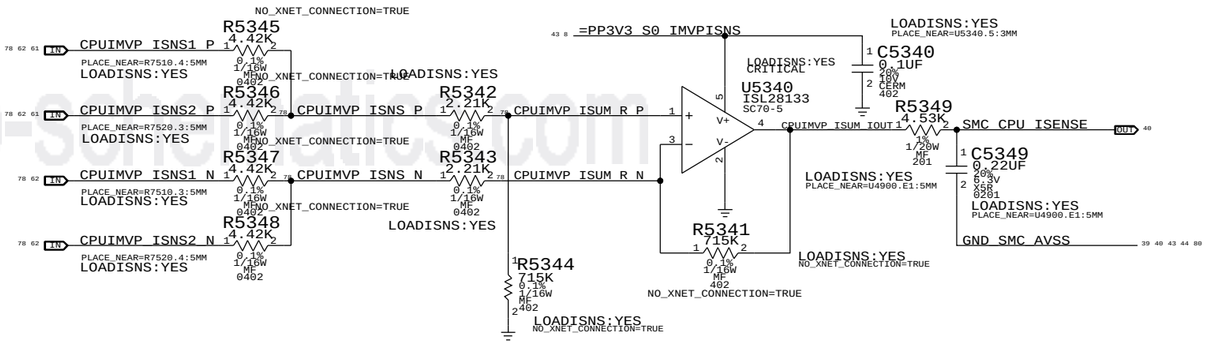
AXG Core Voltage Sense (VN0C)

Gain: 1x
SMC ADC: 12



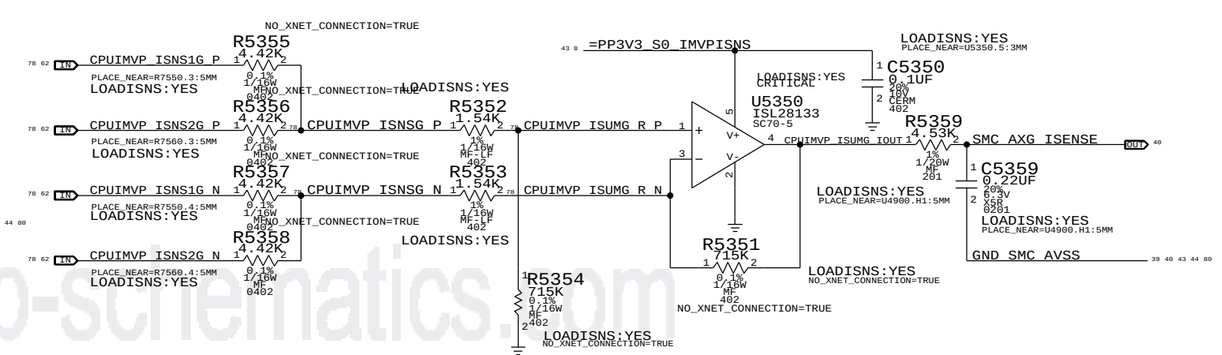
CPU Core Load Side Current Sense (IC0C)

Gain: 161.7x, EDP: 53 A
Rsense: 2x of 0.00075 (R7510, R7520), Rsum: 0.000375
V across Rsense: 19.8 mV
SMC ADC: 01



AXG Core Load Side Current Sense (IN0C)

Gain: 190.6x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375
V across Rsense: 17.25 mV
SMC ADC: 18



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5349,C5359,C5369		LOADISNS:NO

SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE
Power Sensor: Load Side

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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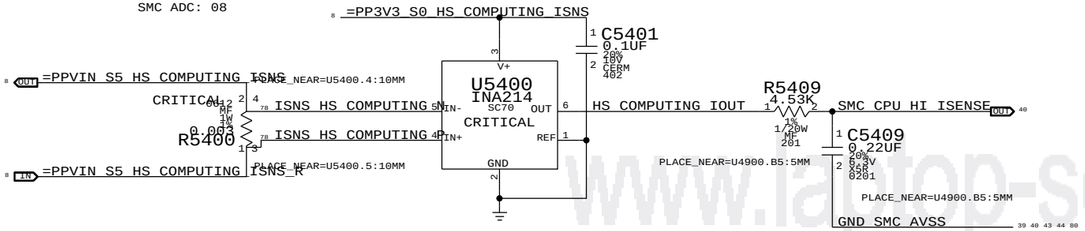
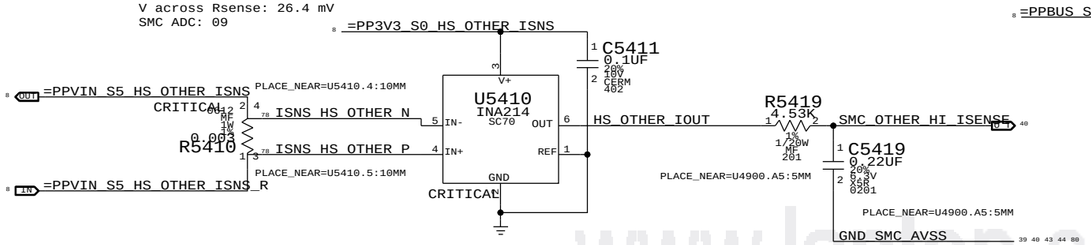
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A
Rsense: 0.003 (R5400)
V across Rsense: 52.2 mV
SMC ADC: 08



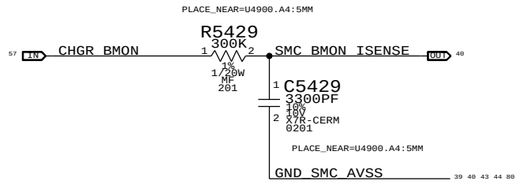
OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A
Rsense: 0.003 (R5410)
V across Rsense: 26.4 mV
SMC ADC: 09



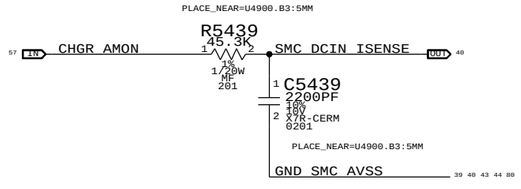
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x, EDP: 6.6 A
Rsense: 0.010 (R7050)
SMC ADC: 07



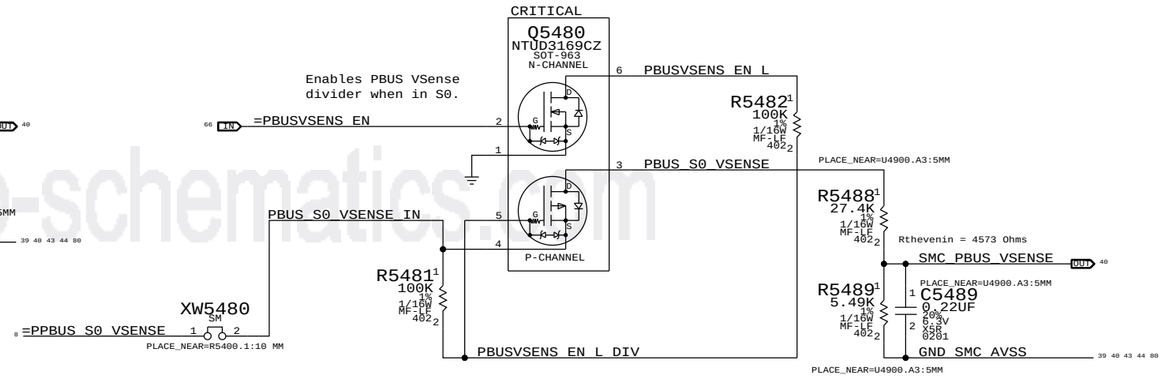
DC-In (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7020)
SMC ADC: 04



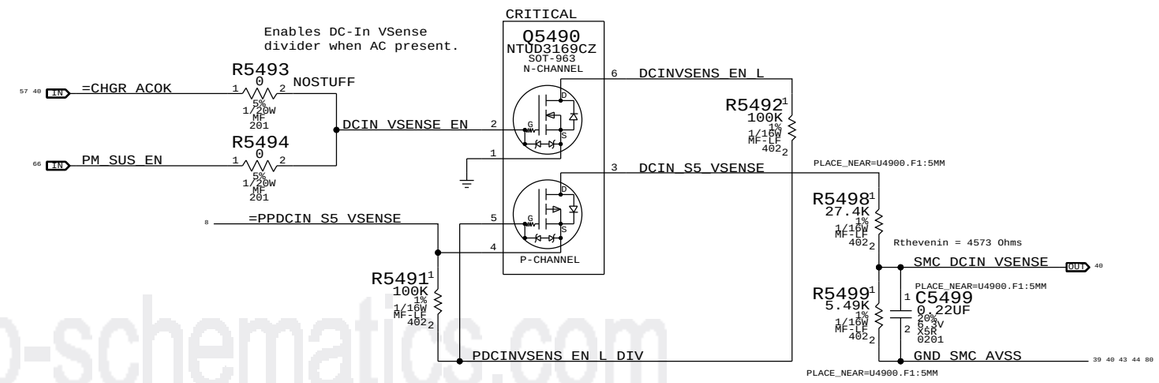
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
SMC ADC: 05



DC In Voltage Sense & Enable (VD0R)

Gain: 0.167x
SMC ADC: 03



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

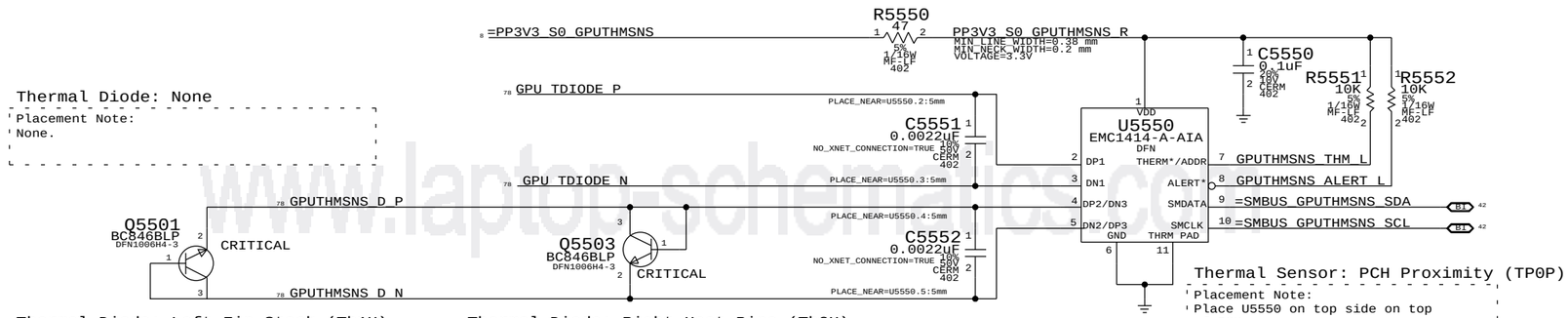
PAGE TITLE: Power Sensor: High Side

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 54 OF 132
SHEET: 44 OF 80

Thermal Sensor A:
PCH Proximity, Left Fin Pipe, Right Fin Stack

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: None

Placement Note:
None.

Thermal Sensor: PCH Proximity (TP0P)

Placement Note:
Place U5550 on top side on top of PCH.

Thermal Diode: Left Fin Stack (Th1H)

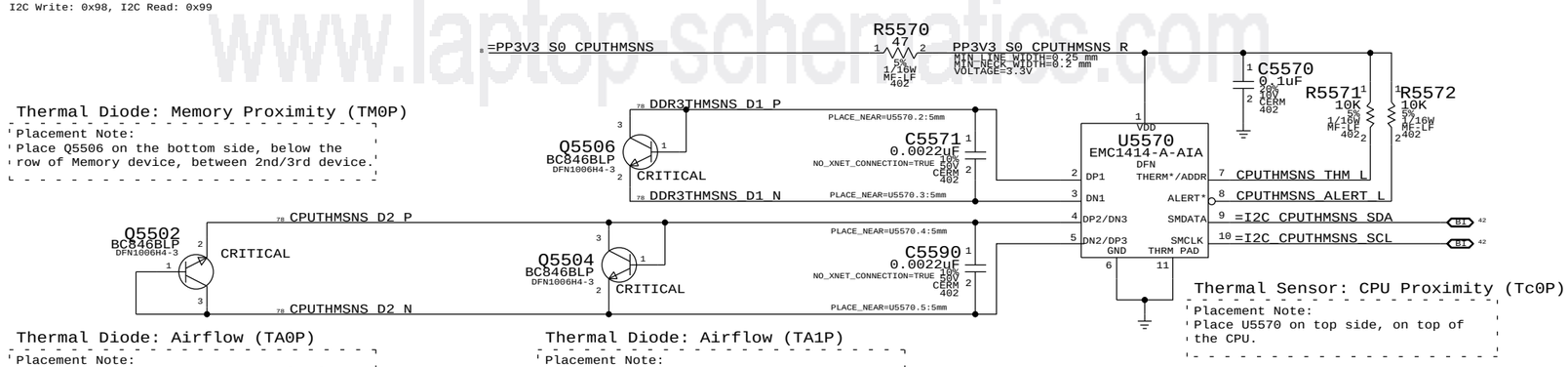
Placement Note:
Place Q5501 on the top side on the corner close to the Left Fin Stack.

Thermal Diode: Right Heat Pipe (Th2H)

Placement Note:
Place Q5503 under the top side on the corner close to the Right Fin Stack.

Thermal Sensor B:
CPU Proximity, Memory Proximity, Airflow

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: Memory Proximity (TM0P)

Placement Note:
Place Q5506 on the bottom side, below the row of Memory device, between 2nd/3rd device.

Thermal Sensor: CPU Proximity (Tc0P)

Placement Note:
Place U5570 on top side, on top of the CPU.

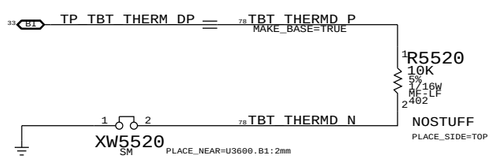
Thermal Diode: Airflow (TA0P)

Placement Note:
Place Q5502 on the bottom side, below left underneath the left fan well in the neck.

Thermal Diode: Airflow (TA1P)

Placement Note:
Place Q5504 on the either side, near LCD connector and DCIN connector.

Thermal Sensor: T29 Die



Note: Use GND pin B1 on U3600 for N leg.

SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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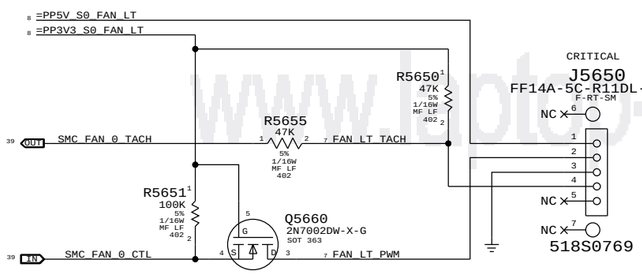
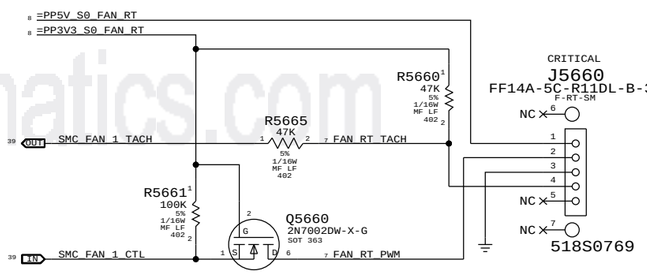
Left Fan



Right Fan



SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE

Fan Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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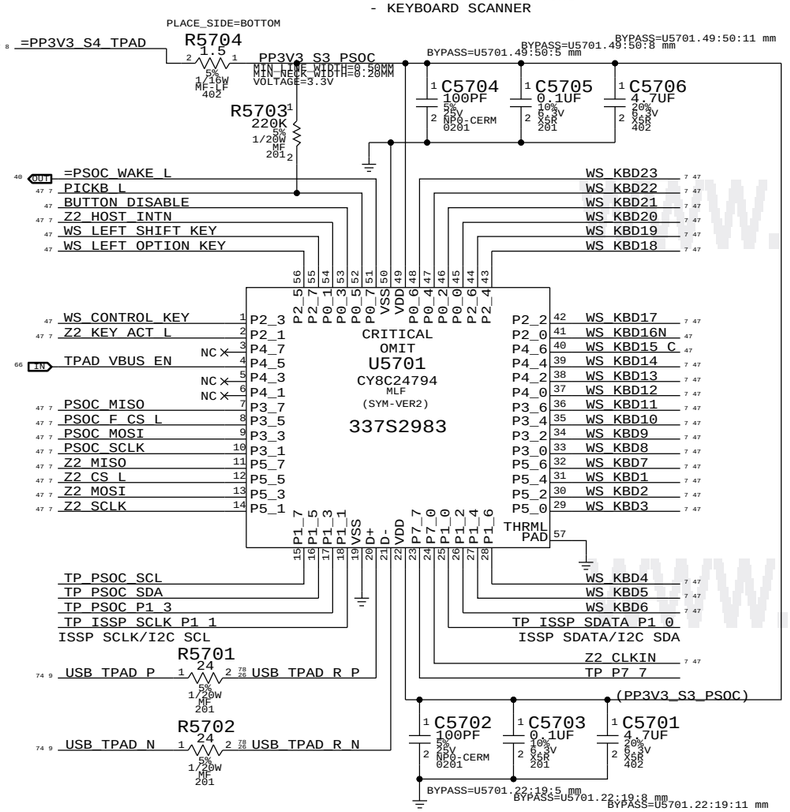
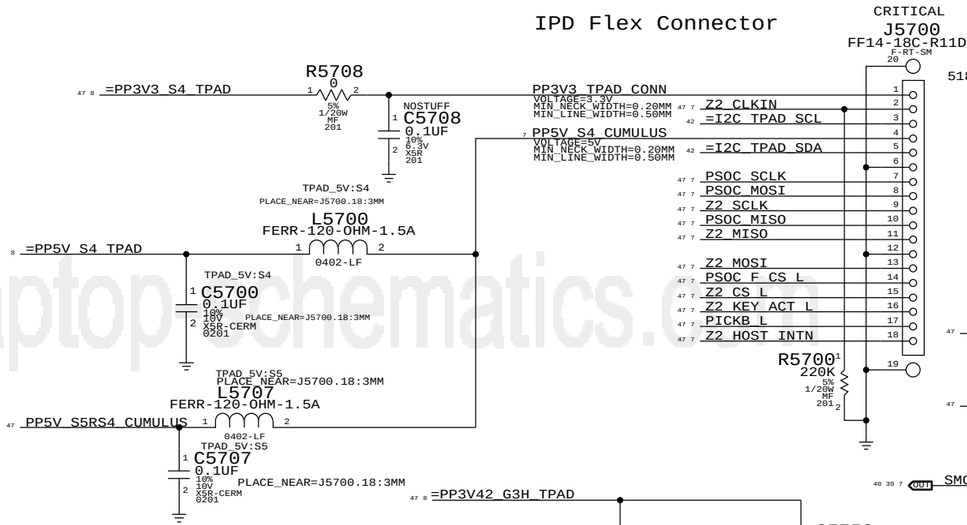
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

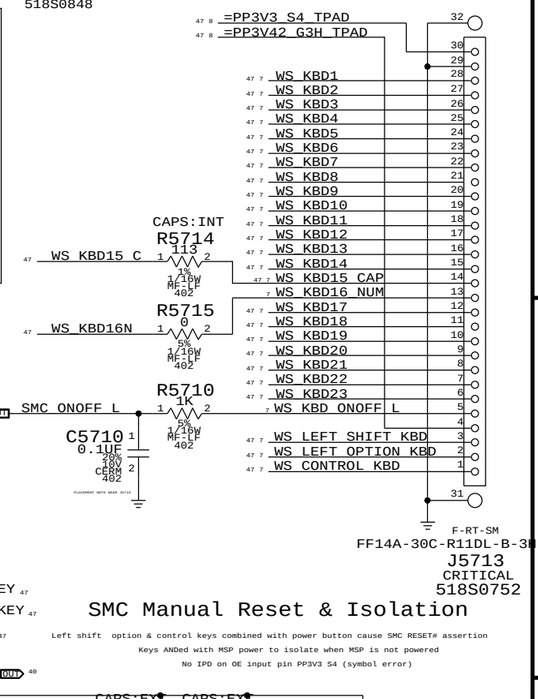


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

IPD Flex Connector



Keyboard Connector



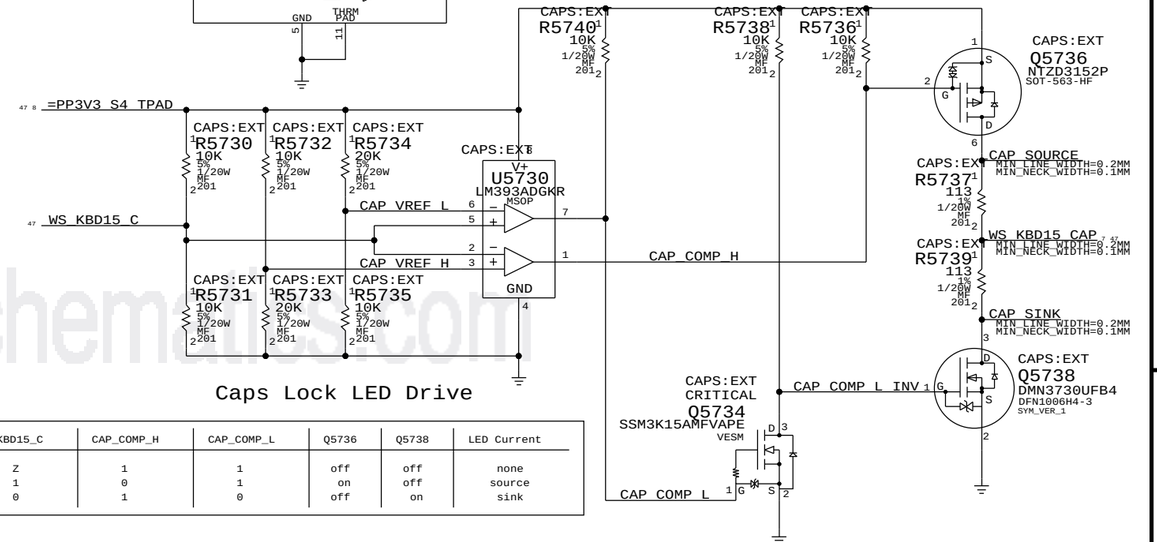
SMC Manual Reset & Isolation

Left shift option & control keys combined with power button cause SMC RESET# assertion

Keys ANDed with MSP power to isolate when MSP is not powered

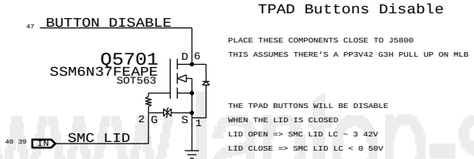
No IPD on OE input pin PP3V3 S4 (symbol error)

Caps Lock LED Drive



WS_KBD15_C	CAP_COMP_H	CAP_COMP_L	Q5736	Q5738	LED Current
Z	1	1	off	off	none
1	0	1	on	off	source
0	1	0	off	on	sink

TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800

THIS ASSUMES THERE'S A PP3V42 G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE WHEN THE LID IS CLOSED

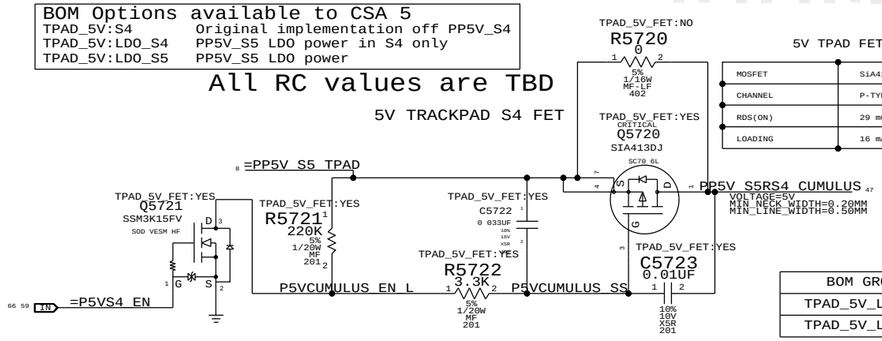
LID OPEN => SMC LID LC ~ 3 42V

LID CLOSE => SMC LID LC < 0 50V

BOM Options available to CSA 5	
TPAD_5V:S4	Original implementation off PP5V_S4
TPAD_5V:LDO_S4	PP5V_S5 LDO power in S4 only
TPAD_5V:LDO_S5	PP5V_S5 LDO power

All RC values are TBD

5V TRACKPAD S4 FET



5V TPAD FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	16 mA (EDP)

BOM GROUP	BOM OPTIONS
TPAD_5V_LDO:S4	TPAD_5V_FET:YES,TPAD_5V:S5
TPAD_5V_LDO:S5	TPAD_5V_FET:NO,TPAD_5V:S5

SYNC_MASTER=D2 MLB KEPLER SYNC_DATE=12/08/2011

PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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8 =PP3V3_S0_TPAD

R5858 470K 5% 1/16W MF-LF 402

48 39 SMC_SYS_KBDLED

R5859 4.7K 5% 1/16W MF-LF 402

CRITICAL
J5815
AA07A-S010-VA1
F-ST-SM

48 7 KBDLED_CATHODE2
48 7 PP_KBD_BOOST_VOUT
7 SMC_KBDLED_PRESENT_L

KBDLED_CATHODE1 7 48
PP_KBD_BOOST_VOUT 7 48

J5815 PIN 5 IS GROUNDED ON KEYBOARD BACKLIGHT FLEX

Keyboard Backlight Driver & Detection

To detect Keyboard backlight SMC will tristate and read SMC_SYS_KBDLED

If LOW keyboard backlight present

If HIGH keyboard backlight not present

516S0899
Keyboard Backlight Connector

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	2	CAP,CER,4.7UF,10%,25V,X6S,0603	C5810,C5811	CRITICAL	

152S1701 COMBO
CRITICAL
L5850
10UH-20%-1.4A-0.17OHM
PST041H-CDH46D14-SM

371S0490
CRITICAL
D5850
SOD-323
PMEG4010BEA

XW5810 SM

8 =PP5V_S0_KBDLED

PPVIN_S0_KBDLED_L
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V

OMIT_TABLE
C5810 4.7UF 10% 25V X5R-CERM 0603

OMIT_TABLE
C5811 4.7UF 10% 25V X5R-CERM 0603

C5812 0.1UF 10% 25V X5R 402

R5810 0 5% 1/16W MF-LF 402

KBDLED_SW1
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
SWITCH_NODE=TRUE

PP_KBD_BOOST_VOUT 7 48
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=30V

XW5850 SM

C5860 1.0UF 10% 50V X5R 0603
C5861 1.0UF 10% 50V X5R 0603
C5862 1.0UF 10% 50V X5R 0603
C5863 1.0UF 10% 50V X5R 0603
C5864 220PF 10% 50V X7R-CERM 0402

PP_KBDBOOST_XW
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=30V

R5870 237K 1% 1/16W MF-LF 402
NOSTUFF C5870 33PF 5% 50V CERM 402

R5871 10K 1% 1/16W MF-LF 402
NOSTUFF C5871 33PF 5% 50V CERM 402

GND_KBDLED_AGND 48

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,1/16W,0.5,0402,SMD,LF	R5852,R5853	CRITICAL	KBDBKLT:PROD

PPVIN_S0_KBDLED_C
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V

C5850 1UF 10% 25V X5R 603-1
C5851 0.01UF 10% 16V X7R-CERM 0402

R5802 0 5% 1/16W MF-LF 402

48 GND_KBDLED_AGND
PVDC_KBDLED

C5852 1UF 10% 25V X5R 603-1

R5850 100K 5% 1/16W MF-LF 402

48 GND_KBDLED_AGND

U5850
TQFN
ISL97682

11	VDC	VIN	7
6	EN	LX	9
5	PWMI	OVP	12
3	RSET		
8	FPW/DIRECTPWM		
4	FSW	CH1	13
2	COMP	CH2	15
		NC	14
		NC	16
1	AGND	PGND	10
		THRM PAD	17

KBDLED_EN
SMC_SYS_KBDLED_FILTER
KBDLED_RSET
KBDLED_FPW
KBDLED_FSW
KBDLED_COMP

KBDLED_OVP

KBDBKLT:ENG
R5852 10.2 0.1% 1/16W TF 402

KBDLED_CATHODE1_R
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=35V

KBDLED_CATHODE1
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=35V

KBDBKLT:ENG
R5853 10.2 0.1% 1/16W TF 402

KBDLED_CATHODE2_R
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=35V

KBDLED_CATHODE2
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=35V

R5851 0 5% 1/16W MF-LF 402

48 39 SMC_SYS_KBDLED

I_LED= 804/RSET

NOSTUFF C5854 33PF 5% 50V CERM 402

R5855 40.2K 1% 1/16W MF-LF 402

R5856 137K 1% 1/16W MF-LF 402

C5853 33PF 5% 50V CERM 402

R5854 10K 5% 1/16W MF-LF 402

KBDLEDCOMP_RC

C5855 0.0082UF 10% 25V X7R 402

FSW =1 MHZ
SEE SPEC FOR OTHERS

NOSTUFF R5857 100K 5% 1/16W MF-LF 402

XW5800 SM

48 GND_KBDLED_AGND

MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V

SYNC_MASTER=D2_MLB_KEPLER SYNC_DATE=12/08/2011

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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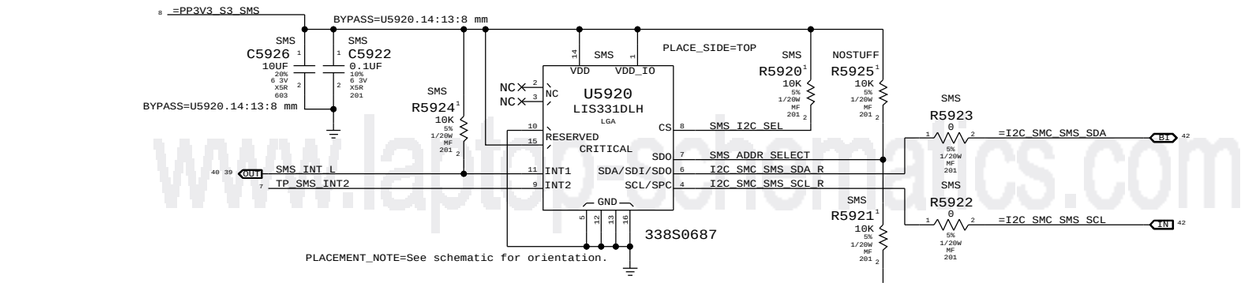
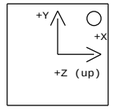


SMS_ADDR_SELECT=0 Addr: 0x30(Wr)/0x31(Rd)
SMS_ADDR_SELECT=1 Addr: 0x32(Wr)/0x33(Rd)

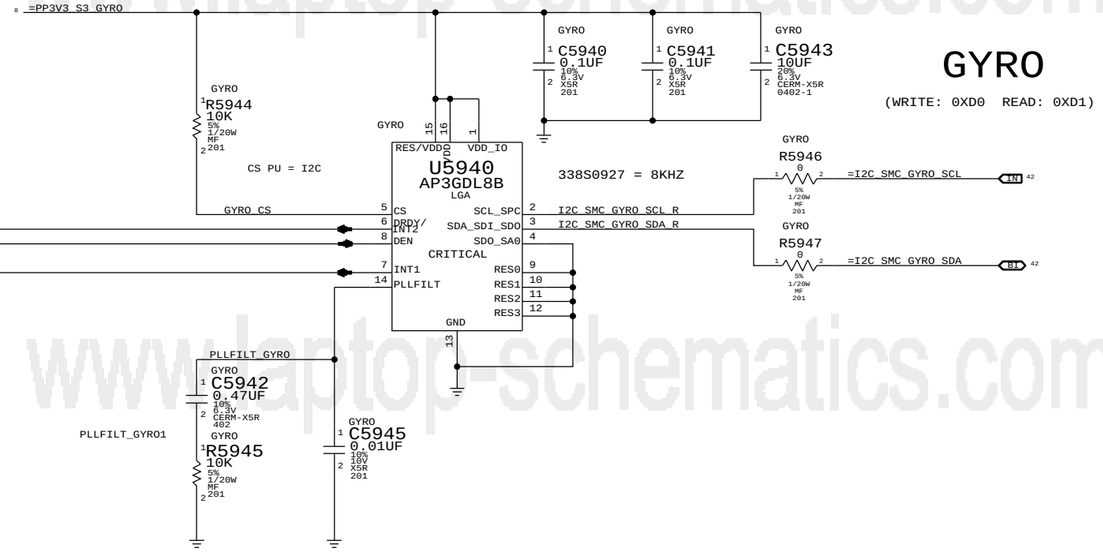
NOTE: SDA and SCL have internal pull-ups to VDD_IO.

Desired orientation when placed on top-side (view top):



Front of system

Circle indicates pin 1 location when placed in correct orientation



GYRO

(WRITE: 0XD0 READ: 0XD1)

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE: DIGITAL ACCELEROMETER & GYRO

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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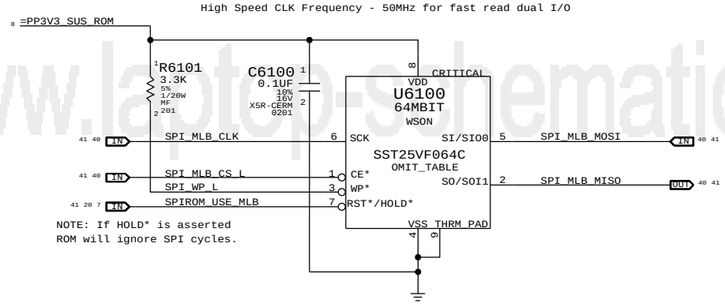
DUAL I/O MODE (MODE 0 & 3) SUPPORTED
High Speed CLK Frequency - 50MHz for fast read dual I/O



SYNC_MASTER=J13_MLB SYNC_DATE=01/20/2012

PAGE TITLE
SPI ROM

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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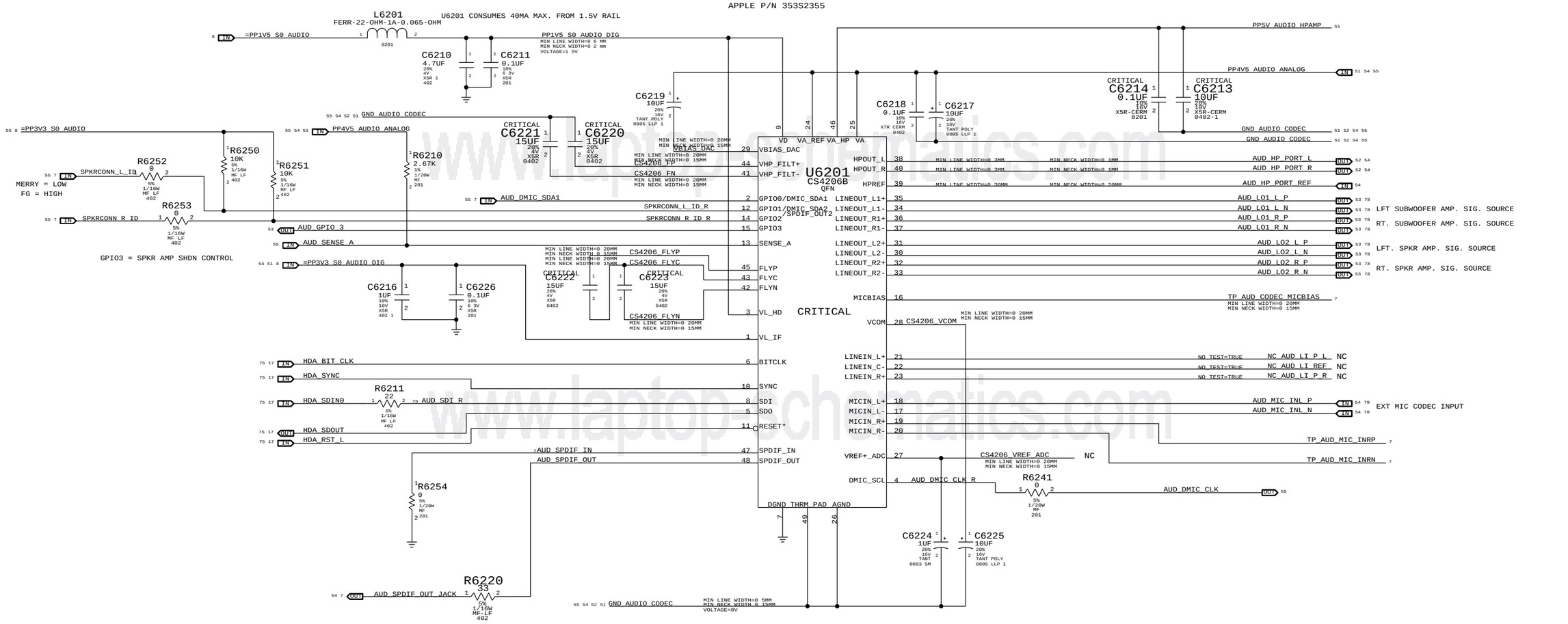
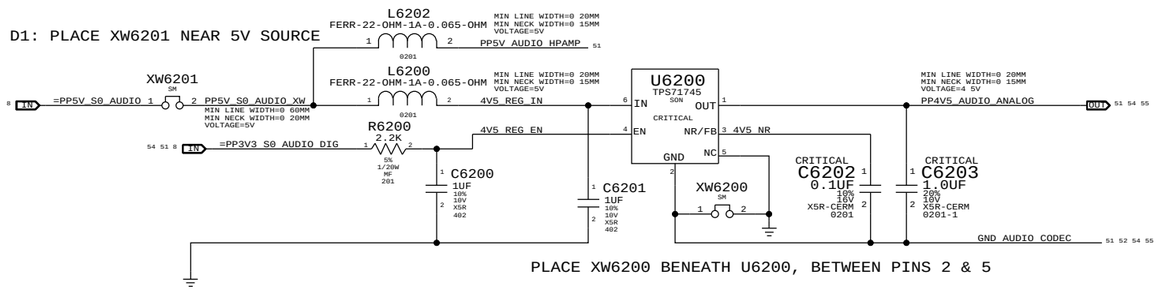
AUDIO CODEC

APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012
PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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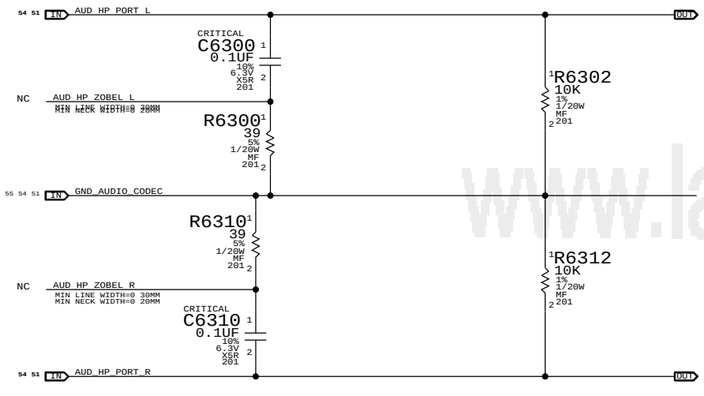
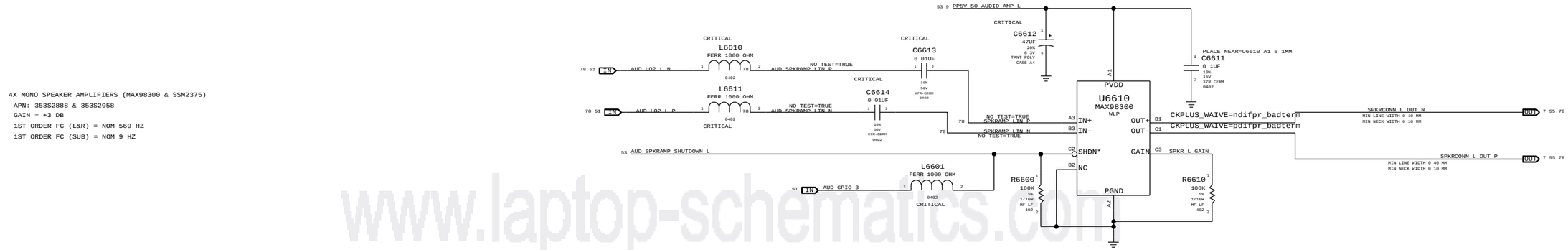
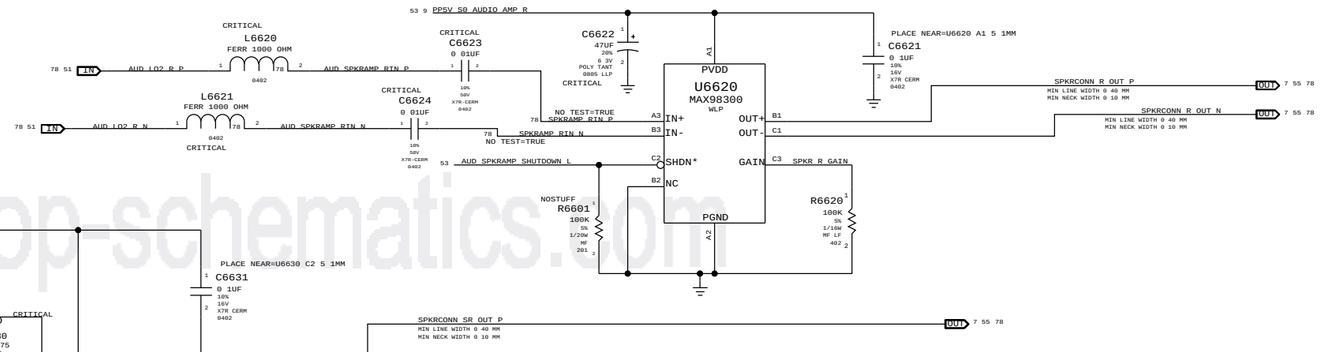
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

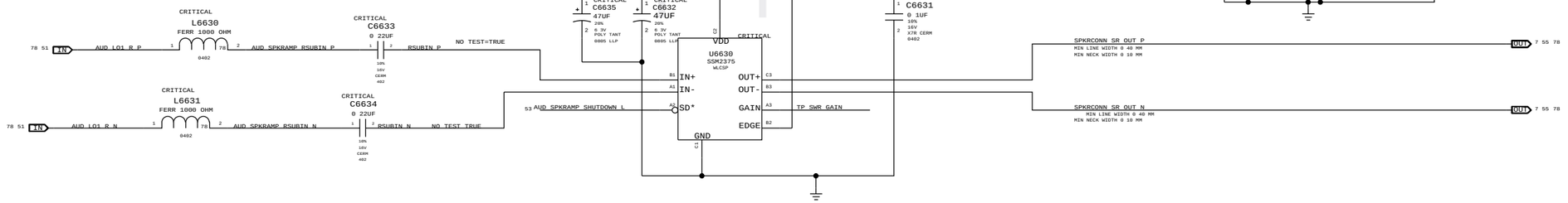


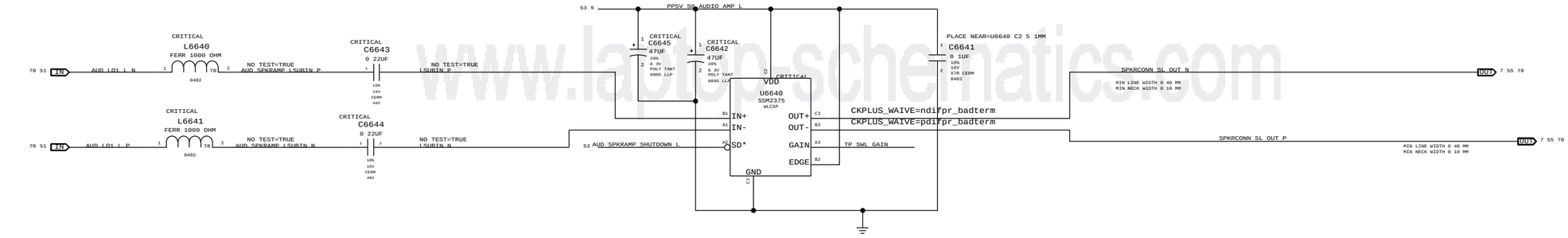
SYNC_MASTER=D1_AUDIO	SYNC_DATE=06/06/2012
PAGE TITLE: AUDIO: HEADPHONE FILTER	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
NOTICE OF PROPRIETARY PROPERTY:	BRANCH: <BRANCH>
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	PAGE: 63 OF 132
	SHEET: 52 OF 80

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









SYNC MASTER=D1 AUDIO
SYNC DATE=06/06/2013

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM>
SIZE D
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AUDIO JACK: HP CONNECTOR WITH MIKEY & CHS

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=10.63KHZ

MIKEY 1A
APN:353S2640
MIKEY ADDRESS: WRITE=72H, READ=73H

I2C PULLUPS ON SOUTHBRIDGE PAGE

PP4V5_AUDIO_ANALOG
=PP3V3_S0_AUDIO_DIG
R6762 10K 5% 1/20W MF 201
C6755 4.7UF 20% 6.3V X5R-CERM1 402
R6757 33 5% 1/20W MF 201
=I2C_MIKEY_SCL
R6758 33 5% 1/20W MF 201
=I2C_MIKEY_SDA
AUDIO_SCL
AUDIO_SDA
AUD_I2C_INT_L
AUD_IPHS_SWITCH_EN
HS_HDET
NOSTUFF R6761 47K 5% 1/20W MF 201
AUD_PORTA_DET_L
R6755 100K 5% 1/20W MF 201
GND_AUDIO_CODEC

U6751 CD3282A1 WCSP
AVDD
SCL MICBIAS HS_MIC_BIAS
SDA DETECT HS_SW_DET
INT* BYPASS HS_RX_BP
ENABLE
HDET
CS
DGND AGND

NO_XNET_CONNECTION=TRUE
R6754 1K 5% 1/20W MF 201
C6756 0.01UF 10% 16V X5R-CERM 0201

L6754 FERR-22-OHM-1A-0.065-OHM 0201
=PP3V42_G3H_AUDIO
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM VOLTAGE=3.42V
PP3V42_G3H_AUDIO_LC
C6790 1UF 10% 10V X5R 402
C6754 0.1UF 10% 16V X5R-CERM 0201
GND_AUDIO_CODEC

U6750 TS3A8235YFP WCSP CRITICAL
VDD
RAMPI CHS_CLAMPI
RAMPO
CLAMPI CHS_CLAMPO
CLAMPO
MIC HS_MIC_HI
REF HS_MIC_LO
SCL AUDIO_SCL
SDA AUDIO_SDA
ADDR
GND1 GND2 GND
MIC1 MIC2

R6751 1K 5% 1/20W MF 201
R6752 2.2K 1% 1/20W MF 201
R6753 2.2K 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE

C6752 0.1UF 10% 6.3V X5R 201
C6753 0.1UF 10% 6.3V X5R 201
AUD_MIC_INL_P
AUD_MIC_INL_N
R6756 100K 5% 1/20W MF 201
C6750 6800PF 10% 10V X5R-X7R-CERM 0201
R6750 2.2K 5% 1/20W MF 201
R6759 0 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
C6758 27PF 5% 25V NPO-C0G 0201
C6751 10UF 20% 6.3V X5R-CERM 0402-1
C6791 10UF 20% 6.3V X5R-CERM 0402-1
GND_AUDIO_CODEC

XW6751
AUD_HP_PORT_REF
PLACE_NEAR=U6750.D1:5.1MM
NO_XNET_CONNECTION=TRUE
R6760 47K 5% 1/20W MF 201
NOSTUFF
GND_AUDIO_CODEC

R/C6750 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210119)

US_HS_GND
CH_HS_GND
GND_AUDIO_CODEC

L6701 FERR-33-OHM-0.8A-0.09-OHM 0201
US_HS_MIC
AUD_CONN_MIC

L6700 120-OHM-25%-1.3A 0402
US_HS_GND
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.06MM
AUD_CONN_SLEEVE_XW
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM

L6702 120-OHM-25%-1.3A 0402
CH_HS_GND
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.06MM
AUD_CONN_MIC_XW
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM

=PP3V3_S0_AUDIO_DIG
AUD_SPDIF_OUT_JACK
AUD_TIPDET_INV

APN:510S0009
J6701 51138-0274 F-ST-SM

L6704 120-OHM-25%-1.3A 0402
AUD_HP_PORT_L
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.1MM
AUD_CONN_HP_LEFT
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.1MM

L6703 FERR-33-OHM-0.8A-0.09-OHM 0201
CH_HS_MIC
AUD_CONN_SLEEVE

L6705 120-OHM-25%-1.3A 0402
AUD_HP_PORT_R
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.1MM
AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.1MM

L6706 FERR-470-OHM 0201
AUD_TYPEDET
AUD_CONN_TYPEDET

I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012
PAGE TITLE: AUDIO: JACK
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 2)	0X02 (2)	0X09 (9 A)	N/A	0X09 (B)
TWEETERS	0X04 4)	0X04 (4)	0X0B (11)	GPIO 3	N/A
SUB	0X03 3)	0X03 (03)	0X0A (10)	GPIO 3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (A)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
DMIC 1	0X06 (6)	0X0E (D E)	3V3	N/A
DMIC2	0X05 (5)	0X12 (12 C)	3V3	0X0C (12 C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13 V22 B LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

2-MIC CONNECTOR

MIN LINE WIDTH=0 40MM
MIN NECK WIDTH=0 15MM
VOLTAGE=3 3V

=PP3V3_S0_AUDIO → R6885 0 5% 1/16W MF-LF 402 → CON_DMIC_PWR
AUD_DMIC_SDA1 → R6884 0 5% 1/16W MF-LF 402 → CON_DMIC_SDA1
AUD_DMIC_CLK → R6883 0 5% 1/16W MF-LF 402 → CON_DMIC_CLK

CRITICAL J6801 FF14A-6C-R11DL-B-3H F-RT-SM
NC, 1, 2, 3, 4, 5, 6, NC

SPEAKER CONNECTOR HP=80HZ

APN: 518S0627

CRITICAL J6802 78171-6006 M-RT-SM

SPKRCONN_L_OUT_P	IN	1
SPKRCONN_L_OUT_N	IN	2
SPKRCONN_L_ID	OUT	3
		4
SPKRCONN_SL_OUT_P	IN	5
SPKRCONN_SL_OUT_N	IN	6
		7, 8

CRITICAL J6803 78171-6006 M-RT-SM

SPKRCONN_R_OUT_P	IN	1
SPKRCONN_R_OUT_N	IN	2
SPKRCONN_R_ID	OUT	3
		4
SPKRCONN_SR_OUT_P	IN	5
SPKRCONN_SR_OUT_N	IN	6
		7, 8

PORT B DETECT(SPDIF DELEGATE)

AUD_SENSE_A → R6896 20.0K 1% 1/16W MF-LF 402 → AUD_PORTA_DET_L
Q6897 SSM6N15AFE SOT563 (D 6, G 2, S 1)

PORT A DETECT (HEADPHONES)

R6895 39.2K 1% 1/16W MF-LF 402 → AUD_PORTB_DET_L
Q6897 SSM6N15AFE SOT563 (D 3, G 5, S 4)

AUD_OUTJACK_INSERT_L

GND_AUDIO_CODEC → R6802 100K 5% 1/20W MF 201 → AUD_TYPEDET_OD

Q6800 DMC2400UV SOT563 (P-CHN)
PP4V5_AUDIO_ANALOG → R6801 150K 1% 1/20W MF 201 → AUD_TYPEDET

PP4V5_AUDIO_ANALOG → R6803 100K 5% 1/20W MF 201 → AUD_TYPEDET_OD_INV

C6800 0.1UF 10% 6.3V X5R 201 — PLACE_NEAR=Q6800.4:5.1MM

Q6800 DMC2400UV SOT563 (N-CHN)
AUD_TYPEDET_OD → GND_AUDIO_CODEC

=PP3V3_S0_AUDIO → R6867 0 5% 1/16W MF-LF 402 → AUD_IP_PERIPHERAL_DET (OUT 19)
EXTRACTION NOTIFICATION

=PP3V3_S0_AUDIO → R6865 47K 5% 1/20W MF 201 → AUD_TIPDET_FET1
=PP3V3_S0_AUDIO → R6866 475K 1% 1/20W MF 201 → AUD_TIPDET_INV_R
APN:376S0613

Q6803 SSM6N15AFE SOT563 (D 6, G 2, S 1)
AUD_TIPDET_INV → R6892 1.5K 1% 1/16W MF-LF 402 → AUD_TIPDET_INV_R
C6860 1UF 10% 25V X5R 402

CRITICAL L6801 FERR-33-OHM-0.8A-0.09-OHM 0201
AUD_TIPDET_FET1 → AUD_TIPDET_FET2
C6891 1UF 10% 25V X5R 402

Q6803 SSM6N15AFE SOT563 (D 3, G 5, S 4)
AUD_OUTJACK_INSERT_L → GND_AUDIO_CODEC

NOM R6892-C6860 FC = 106Hz
SSM6N15FE Vth = 0.8V to 1.5V
SSM6N15FE IGSS = +/-1uA
FLEX-SIDE RPULLDOWN = 100k (TB 49.9k in REV 3)

=PP5V_S4_AUDIO → SPEAKERID R6810 100K 1% 1/16W MF-LF 402 → SPKRCONN_L_ID
=PP5V_S4_AUDIO → SPEAKERID R6811 100K 1% 1/16W MF-LF 402 → SPKRCONN_R_ID
SPEAKERID R6812 100K 1% 1/16W MF-LF 402
SPEAKERID R6813 100K 1% 1/16W MF-LF 402
SPEAKERID R6816 100K 1% 1/16W MF-LF 402

=PP5V_S4_AUDIO → SPEAKERID C6810 0.1UF 10% 6.3V X5R 201

SPEAKERID CRITICAL U6800 MCP6541T SC70-5
MCP6514_POS, MCP6514_NEG, MCP6514_OUT

SPEAKERID L6802 FERR-1000-OHM 0402
SPEAKERID R6820 33 5% 1/16W MF-LF 402 → SPKR_MATCH_DRV_R → SPKR_MATCH_DRV

=PP5V_S4_AUDIO → SPEAKERID R6814 274K 1% 1/16W MF-LF 402
SPEAKERID R6815 90.9K 1% 1/16W MF-LF 402
SPEAKERID R6817 45.3K 1% 1/16W MF-LF 402
SPEAKERID C6811 4.7UF 20% 10V X5R-CERM 0402

PORT C DETECT(SPEAKER MISMATCH)

AUD_SENSE_A → SPEAKERID R6894 10K 1% 1/16W MF-LF 402 → AUD_PORTC_DET_L
SPEAKERID Q6896 SSM6N15AFE SOT563 (D 6, G 2, S 1)
GND_AUDIO_CODEC

AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S3452	353S1286		U6800	MAXIM ALT TO MICROCHIP
376S0975	376S1081		Q6800	TOSHIBA ALT TO DIODES

SYNC MASTER=D1 AUDIO
SYNC DATE=06/06/2012
PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

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MagSafe DC Power Jack

CRITICAL
F6905
6AMP-32V-0.0095OHM
0603

=PP18V5_DCIN_CONN

CRITICAL
J6900
53780-8608
F-RT-SM

PP18V5_DCIN_FUSE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=18.5V

NC

NO STUFF
C6905
0.1UF
10%
50V
X7R
603-1

518S0543

=PP3V42_G3H_ONEWIREPROT

C6908
0.1UF
10%
10V
CERM
402
PLACEMENT NOTE PLACE NEAR U6900 and U6901

CRITICAL
U6901
TC7SZ08FEAPE
SOT665

SMC_BC_ACOK
ENI 39 40

SMC_BC_ACOK_VCC

C6900
0.1UF
20%
10V
CERM
402

U6900
MAX9940
SC70-5
VCC
EXT
INT
CRITICAL
NC GND
NC

R6929
2.0K
5%
1/10W
MF-LF
402

ADAPTER_SENSE

SYS_ONEWIRE
BI 39

1-Wire OverVoltage Protection

The chassis ground will otherwise float and can send transients onto ADAPTER SENSE when AC is connected

=PP18V5_DCIN_ISOL

BLEEDER
CRITICAL
D6920
SBR0330CW
SOT-323

DCIN_ISOL_BLEEDER_PSRC
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.20MM

C6920
0.1UF
10%
50V
X7R
603-1

BLEEDER

R6930
1K
5%
1/16W
MF-LF
402

BLEEDER
Q6920
AO3407A
SOT23

DCIN_ISOL_BLEEDER_R
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.20MM

BLEEDER
Q6930
2N7002
SOT23-HF1

DCIN_ISOL_BLEEDER_NGATE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.20MM

BLEEDER
R6921
10K
5%
1/16W
MF-LF
402

Q6910
SI5419DU
POWERPAK

5A

C6912
0.047UF
10%
25V
X5R
0402

R6911
10K
1%
1/20W
MF
201

DCIN_ISOL_GATE_R

R6912
68K
1%
1/20W
MF
201

Input impedance of 68K meets sparkitecture requirements for both MPM4 and MPM5.

R6910
100K
5%
1/20W
MF
201

When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.

When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg

DCIN_ISOL_GATE

D6910
GDZT2R6.8
GDZ-0201

6.8V Zener

PLACE COMPONENTS NEAR BATTERY CONNECTOR AREA

PPVBAT_G3H_CONN 7 57

C6950
0.1UF
10%
25V
X5R
402

C6960
1UF
10%
25V
X5R
603-1

SYSDET 3 4

OMIT
998-4777
CRITICAL
J6950
INTERPOSER-D1-TOP
COMBO-SM

STIFF 63
TALL 64
SHRT 65

R6920
47
1%
1/32W
MF
805

PP18V5_DCIN_CONN_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V

CRITICAL
D6905
SBR0330CW
SOT-323

R6905
10
5%
1/16W
MF-LF
805

=PPBUS_G3H 57 8

PPBUS_G3H_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V

PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V

=SMBUS_BATT_SCL
BI 42

=SMBUS_BATT_SDA
BI 42

CRITICAL
D6950
RCLAMP2402B
SC-75

SH6950
4.0OD2.7ID-1.8H

Pin 63 (SH0962) is Neoconix stiffener, 860-1533
Pin 64 (SH0961) is Neoconix tall locator pin. 860-1530
Pin 65 (SH0960) is Neoconix short clocking pin. 860-1529

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	3	CAP,CER,4.7UF,10%,25V,X6S,0603	C6990,C6991,C6992	CRITICAL	

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

OMIT_TABLE
C6992
4.7UF
10%
25V
X5R-CERM
0603

OMIT_TABLE
C6991
4.7UF
10%
25V
X5R-CERM
0603

OMIT_TABLE
C6990
4.7UF
10%
25V
X5R-CERM
0603

U6990
LT3470AED
DFN
VIN
BOOST
SHDN*
NC
SW
BIAS
FB
GND
THRM PAD

P3V42G3H_BOOST
DIDT TRUE
NO_TEST=TRUE

C6994
0.22UF
10%
10V
CERM
402

CRITICAL
L6995
10UH-30%-0.85A-460MOHM
2520

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE TRUE
DIDT TRUE

P3V42G3H_FB

C6995
22PF
5%
50V
CERM
201

R6995
348K
1%
1/20W
MF
201

R6996
200K
1%
1/20W
MF
201

CRITICAL
C6999
22UF
20%
6.3V
X5R
0603

=PP3V42_G3H_REG 8

Vout = 3.425V
100MA MAX OUTPUT
(Switcher limit)

Vout = 1.25V * (1 + Ra / Rb)

SYNC_MASTER=MASTER
SYNC_DATE=MASTER

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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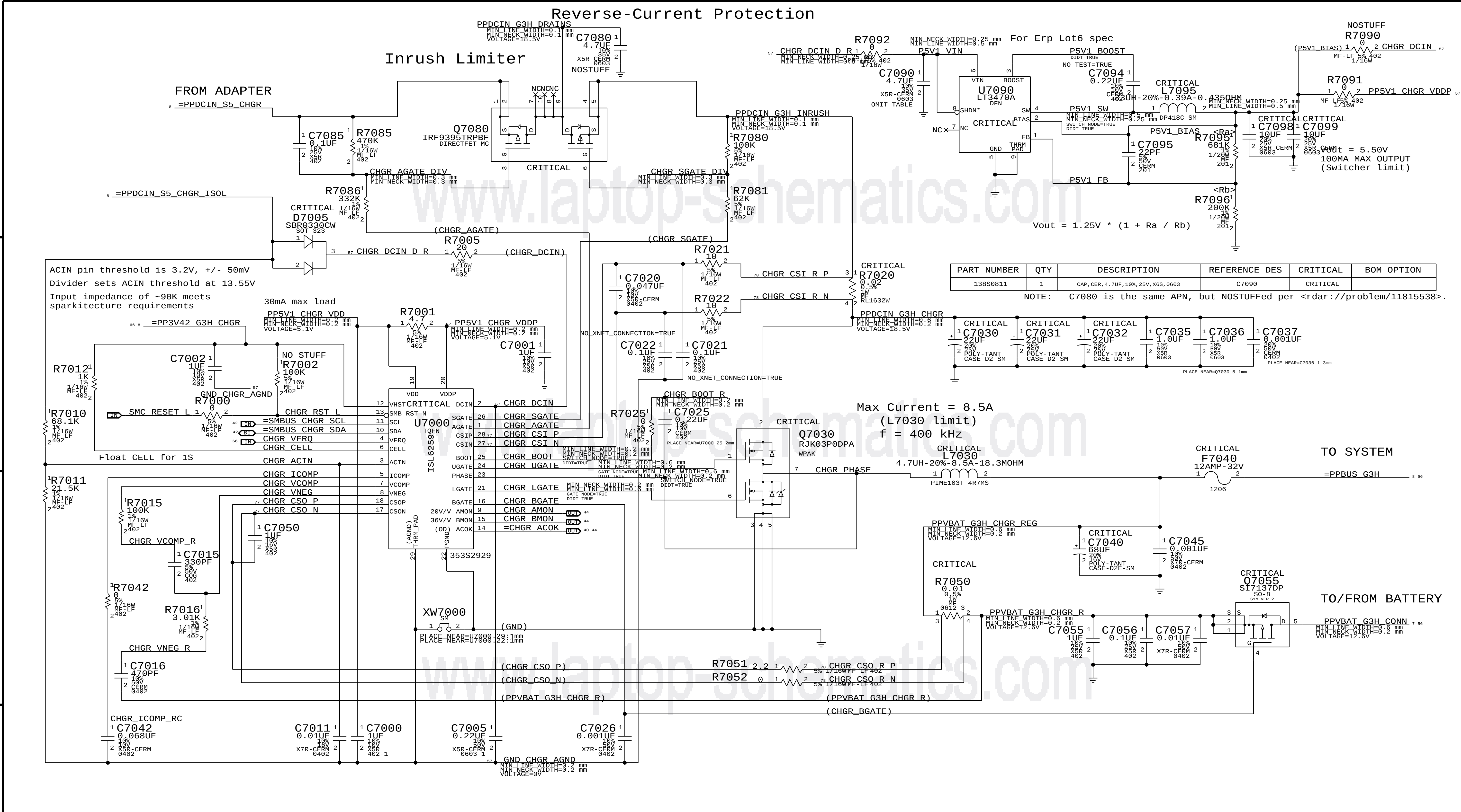
SHEET 56 OF 80



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X6S,0603	C7090	CRITICAL	

NOTE: C7080 is the same APN, but NOSTUFFed per <rdar://problem/11815538>.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

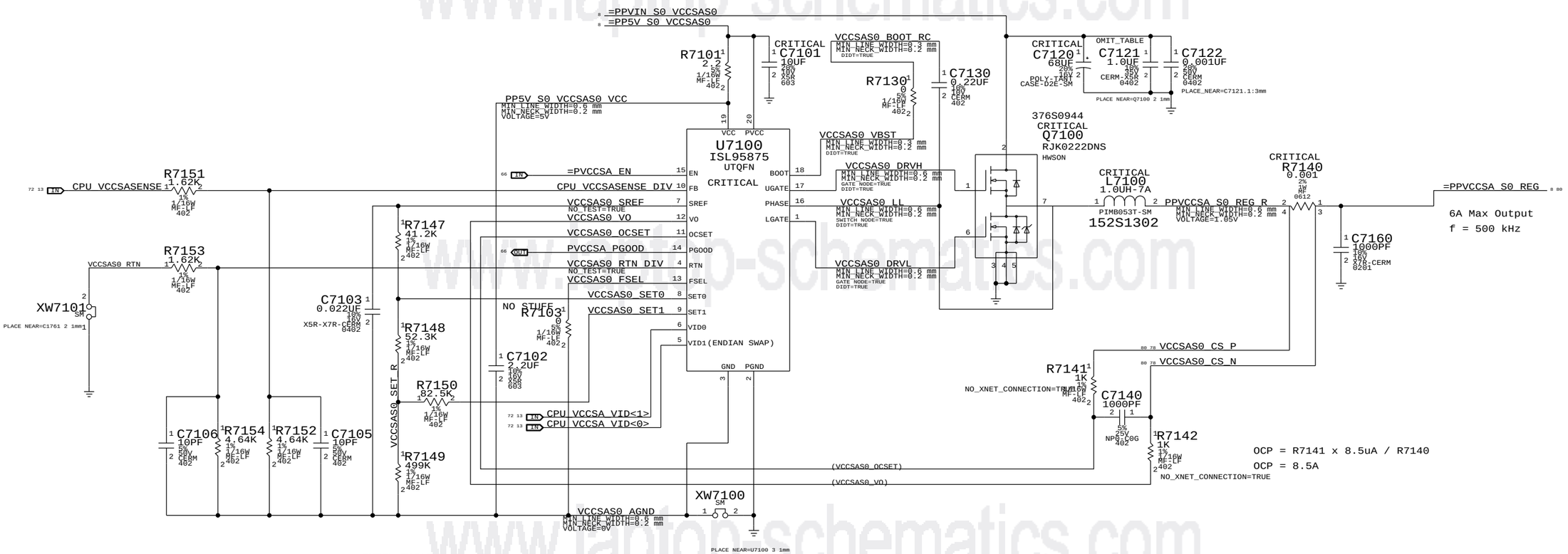
DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

System Agent Power Supply

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	1	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7121	CRITICAL	



INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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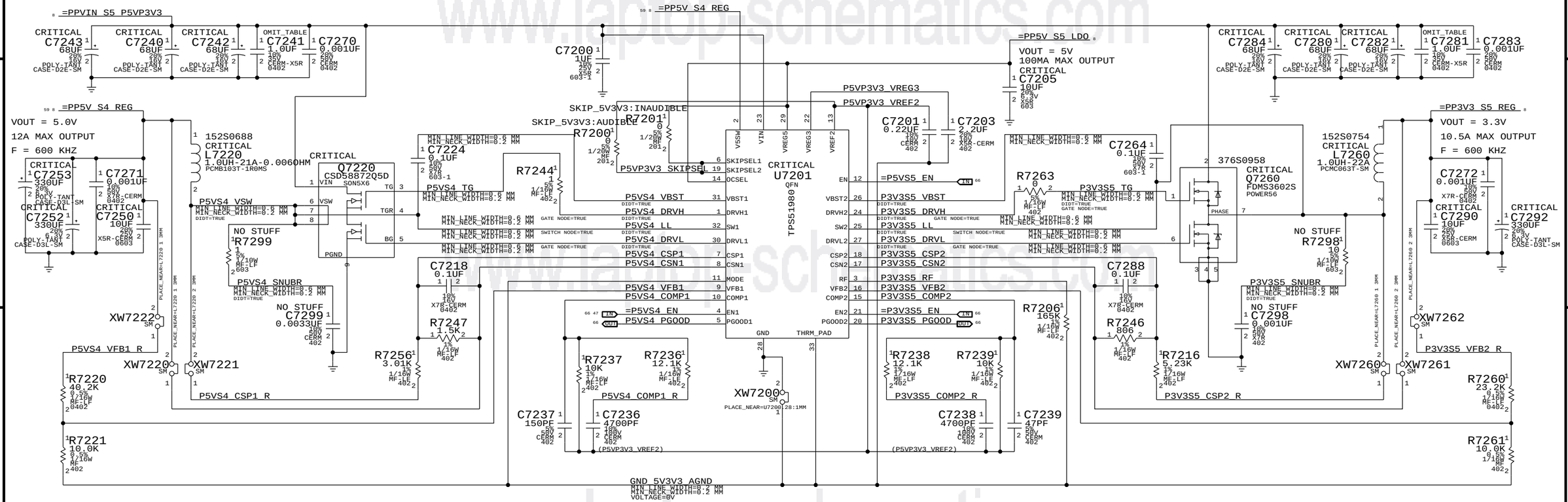
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	2	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7241,C7281	CRITICAL	



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: 5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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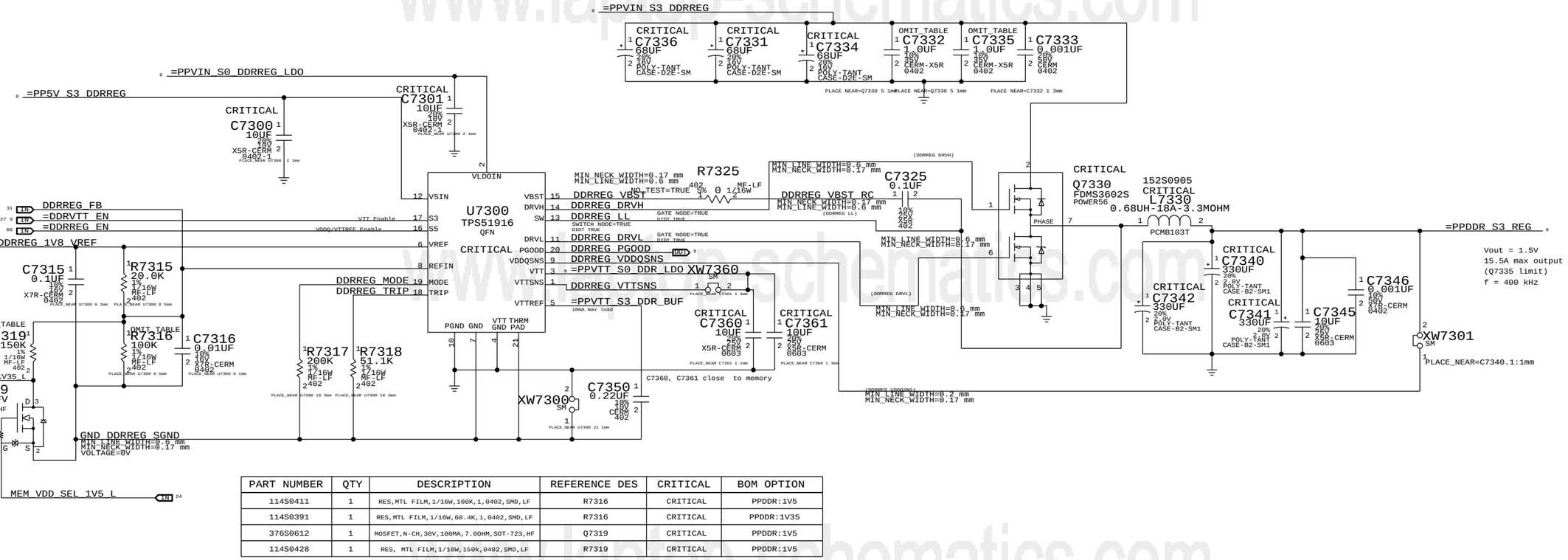
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	2	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7332,C7335	CRITICAL	

DDR3 (1V5R1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7316	CRITICAL	PPDDR:1V5
114S0391	1	RES,MTL FILM,1/16W,60.4K,1,0402,SMD,LF	R7316	CRITICAL	PPDDR:1V35
376S0612	1	MOSFET,N-CH,30V,100MA,7.0OHM,SOT-723,HF	Q7319	CRITICAL	PPDDR:1V5
114S0428	1	RES, MTL FILM,1/16W,150k,0402,SMD,LF	R7319	CRITICAL	PPDDR:1V5

SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE: 1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 73 OF 132

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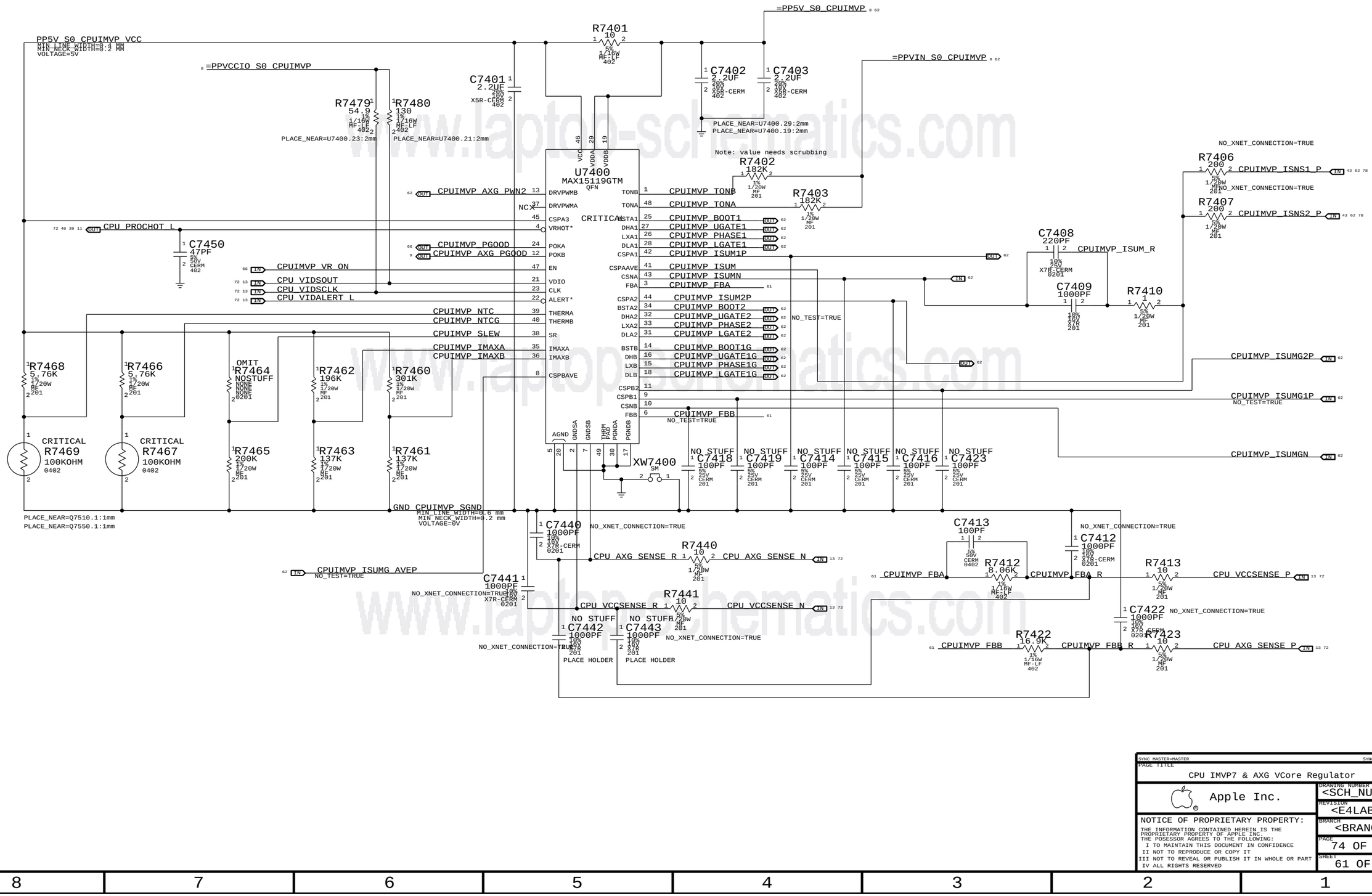

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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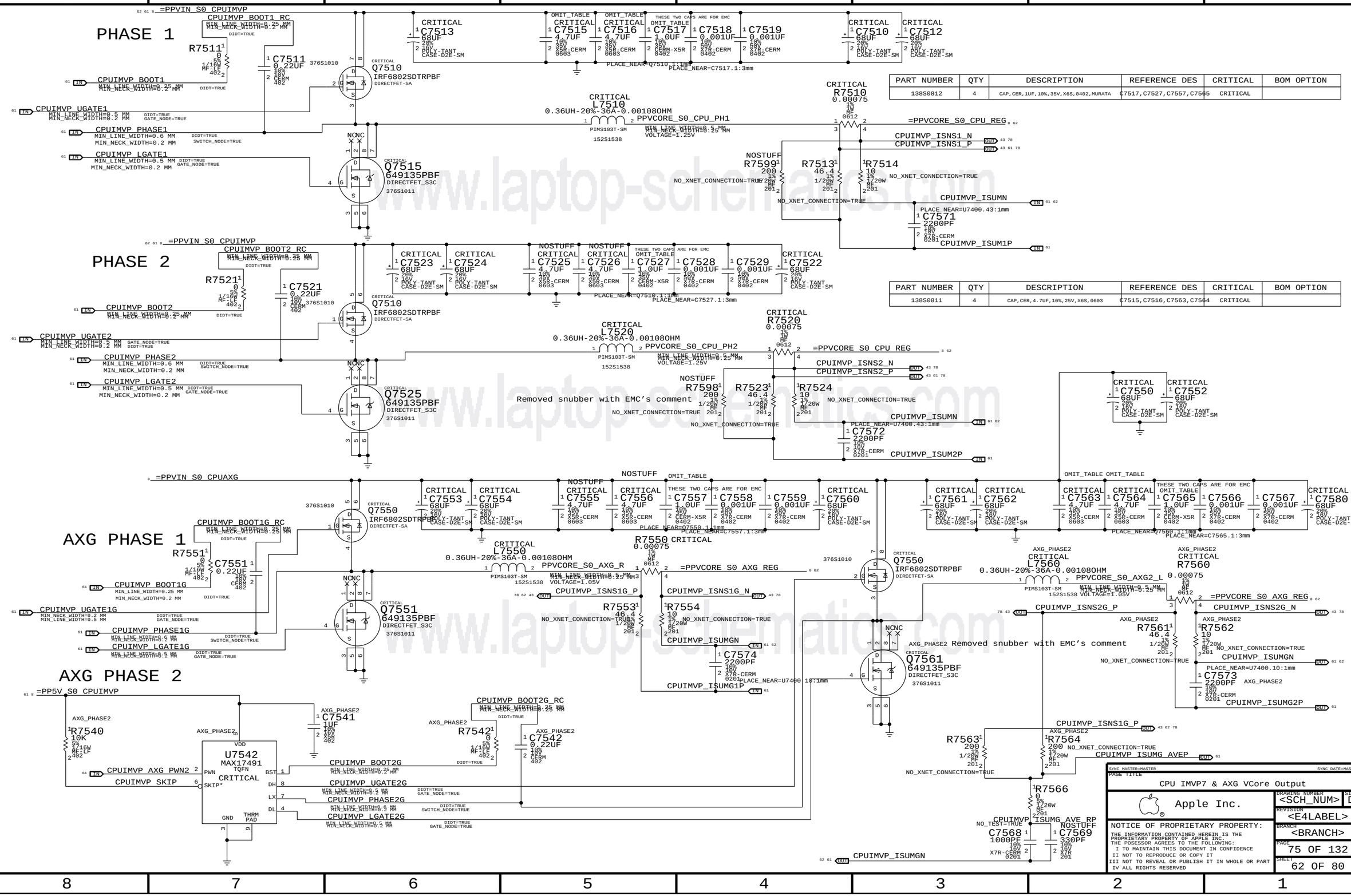
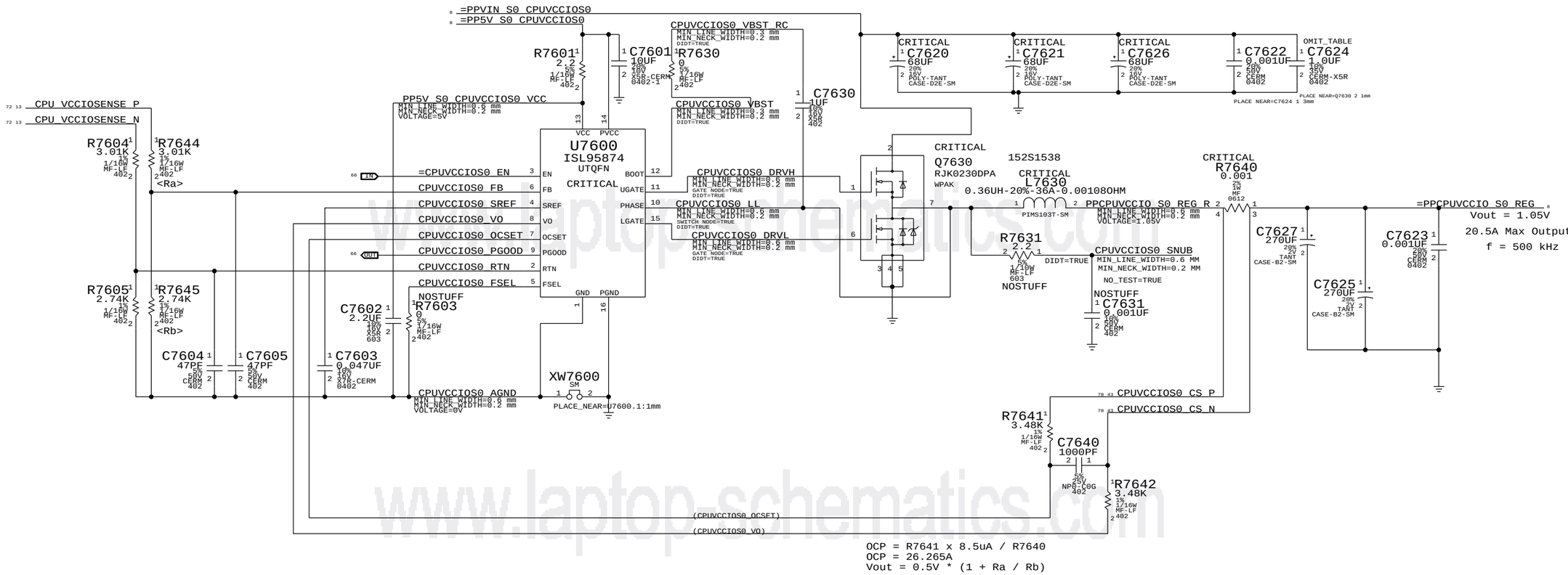


CPU VCCIO (1.05V S0) Regulator

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	1	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7624	CRITICAL	



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: CPUVCCIO (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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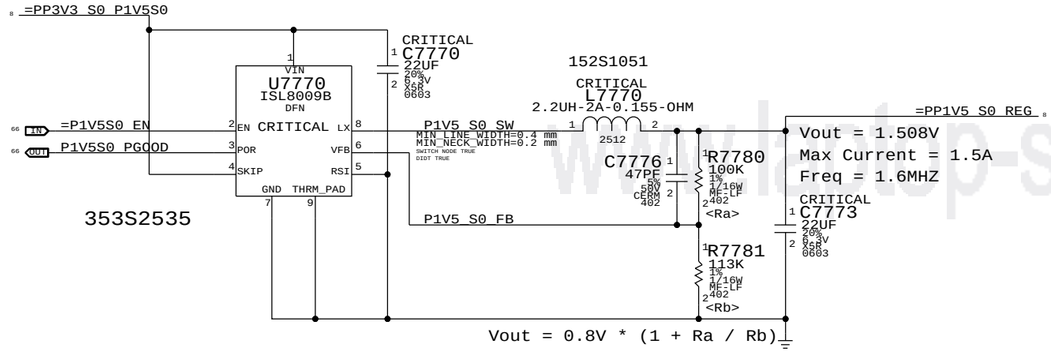
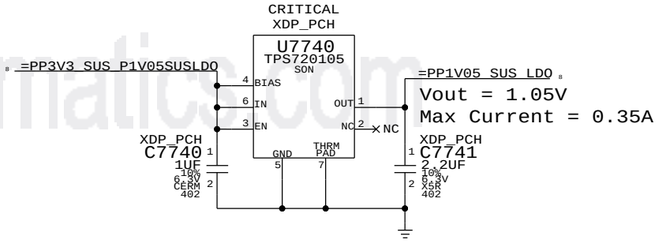
1.5V S0 Switcher



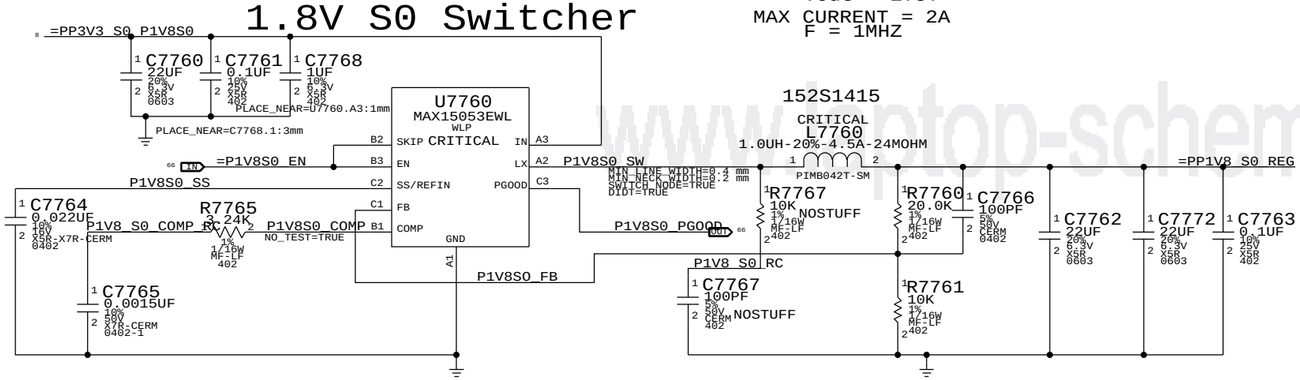
1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

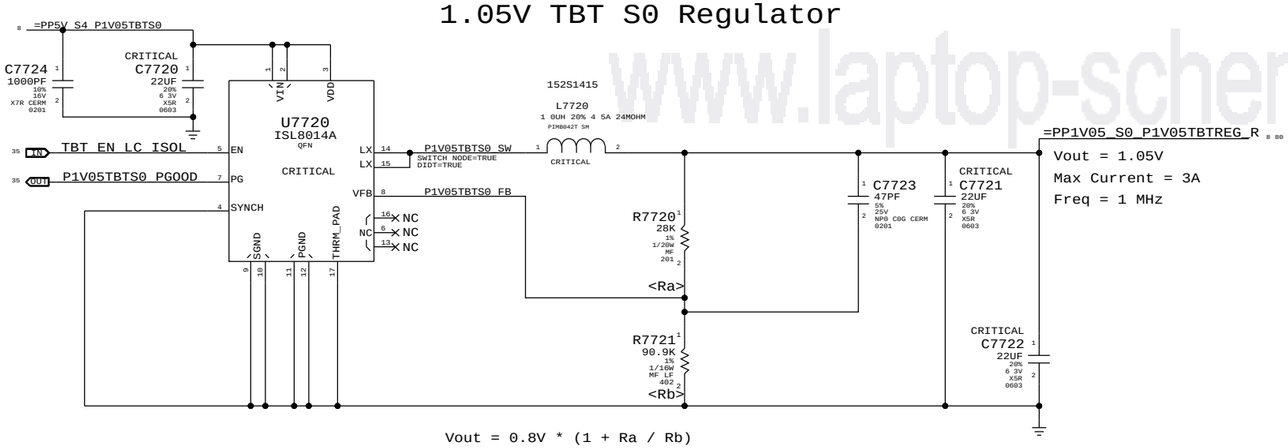


1.8V S0 Switcher

Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



1.05V TBT S0 Regulator



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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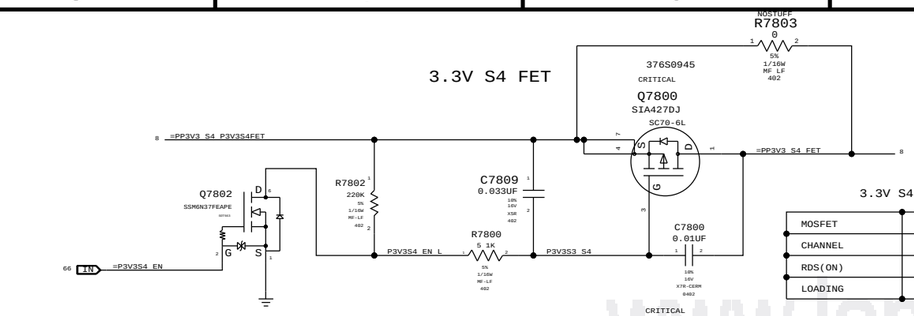
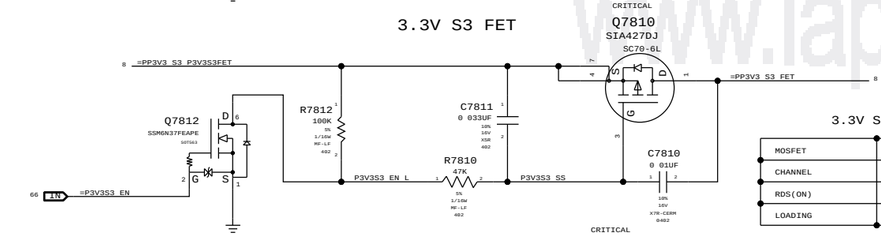
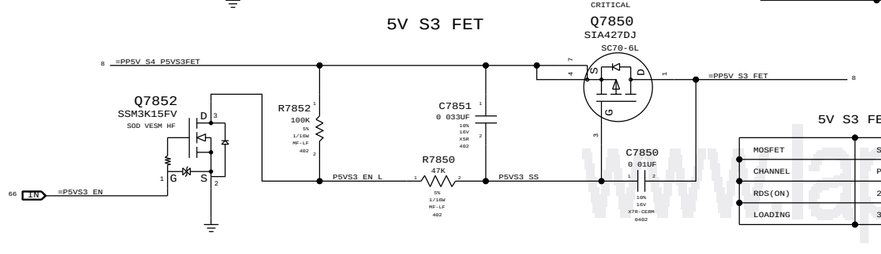


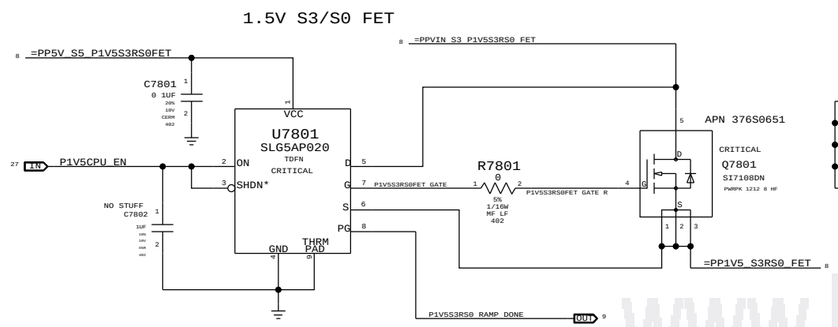
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)



3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

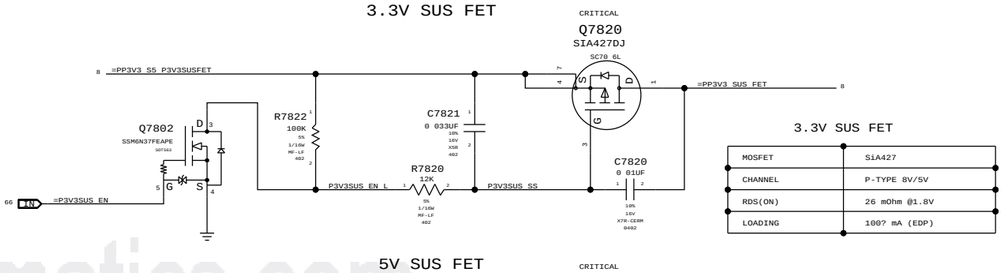


5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

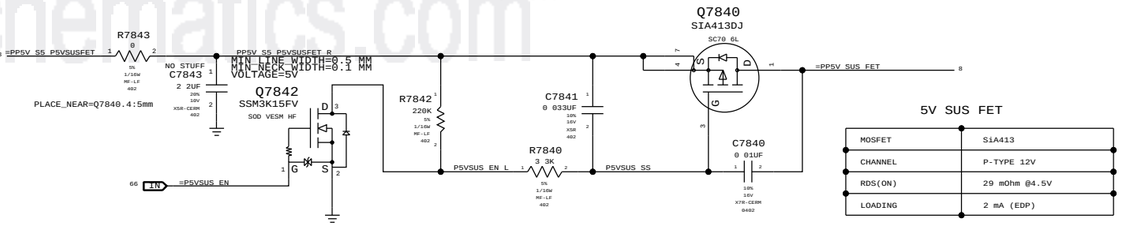


1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

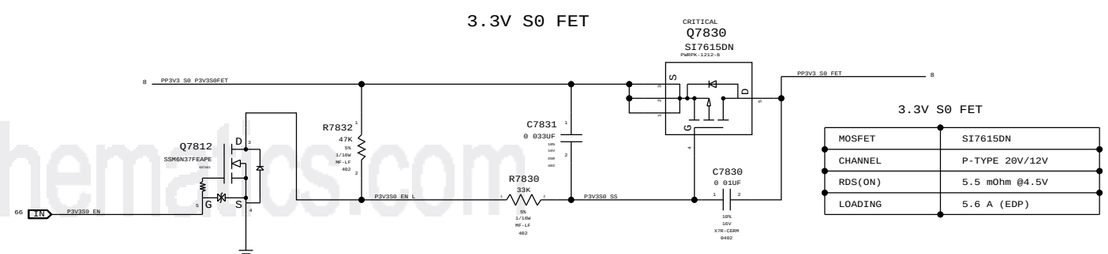
5V_SUS FET INPUT FILTER



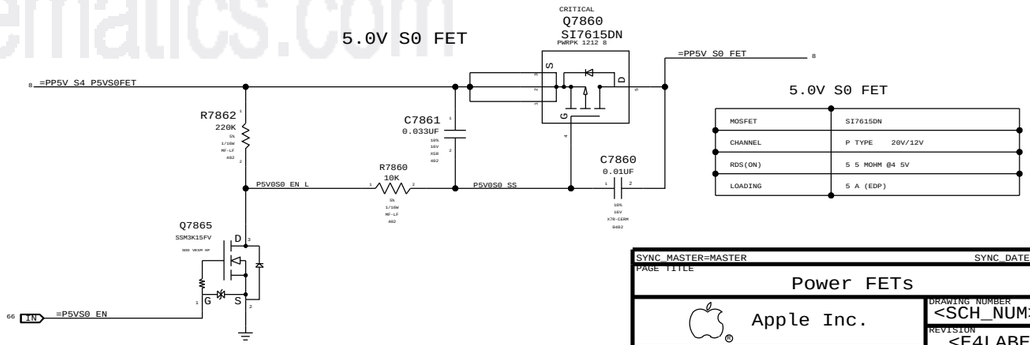
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)



5V SUS FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)



3.3V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P TYPE 20V/12V
RDS(ON)	5 5 MOHM @4 5V
LOADING	5 A (EDP)

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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BRANCH <BRANCH>

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S5 Rail Enables & PGOOD

=P5VS5_EN → SMC_PM_G2_EN (MAKE_BASE=TRUE) → R7940 100 5% 1/16W MF-LF 402 (PLACE NEAR U7201 21 7mm) → P3V3S5_EN (MAKE_BASE=TRUE) → =P3V3S5_EN

C7942 0.0033UF 10% 16V X5R 402 — NO STUFF

=PP3V42_G3H_PWRCTL → R7941 100K 5% 1/16W MF-LF 402 (PLACE NEAR U7201 20 7mm)

P3V3S5_PGOOD → S5_PWRGD (MAKE_BASE=TRUE)

S5_PWRGD (old name RSMRST_PWRGD)-->SMC

SMC-->PM_DSW_PWRGD

Mobile System Power State Table

State	SMC ADAPTER EN	SMC PM G2 ENABLE	SMC S4 WAKESRC EN	PM SUS EN	PM SLP S5 L	PM SLP S4 L	PM SLP S3 L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

1.2V, 5V, 3.3V, DDR S3 ENABLE

PM_SLP_S4_L → PM_SLP_S4_L:100K pull down in PCH page

R7911 5.1K 1% 1/16W MF-LF 402 (PLACE NEAR U7300 10 6mm)
R7912 0 5% 1/16W MF-LF 402 (PLACE NEAR Q7812 2 6mm)
R7913 0 5% 1/16W MF-LF 402 (PLACE NEAR Q7842 2 6mm)
R7914 0 5% 1/16W MF-LF 402 (PLACE NEAR U4900 K5 6mm)
R7916 3.3K 1% 1/16W MF-LF 402 (PLACE NEAR U4900 K5 6mM)

C7910 0.47UF 10% 6.3V X5R 402
NO STUFF C7912 0.47UF 10% 6.3V X5R 402
NO STUFF C7913 0.47UF 10% 6.3V X5R 402
NO STUFF C7914 0.47UF 10% 6.3V X5R 402
NO STUFF C7916 0.47UF 10% 6.3V X5R 402

TPAD_VBUS_EN
P1V2S3_EN
P5VS3_EN → =P5VS3_EN (MAKE_BASE=TRUE)
P3V3S3_EN → =P3V3S3_EN (MAKE_BASE=TRUE)
DDRREG_EN → =DDRREG_EN (MAKE_BASE=TRUE)

3.3V S4 ENABLE

=PP3V3_S5_PWRCTL → C7970 0.1UF 20% 10V X5R 402 (PLACE NEAR U7940 1 2 3mm)

PM_SLP_S5_L:100K pull down on PCH page → PM_SLP_S5_L

U7970 74LVC1G32 SOT891

SMC_S4_WAKESRC_EN (MAKE_BASE=TRUE)

P5V3V3_S4_EN (MAKE_BASE=TRUE) → =P3V3S4_EN

NOSTUFF R7915 0 5% 1/16W MF-LF 402

=TBTAPWRSW_EN
=TBTBPWRSW_EN
=P5VS4_EN

CPUVCORE ENABLE

ALL_SYS_PWRGD → R7974 0 5% 1/16W MF-LF 402 (PLACE NEAR U7400 7 5mm) → CPUIMVP_VR_ON

3.3V/5.0V Sus ENABLE

=PP3V3_S5_PWRCTL → C7940 0.1UF 20% 10V CERM 402 (PLACE NEAR U7940 1 2 3mm)

SMC_BATLOW_L:100K pull up on SMC page → SMC_BATLOW_L

PM_SLP_SUS_L:100K pull down on PCH page → PM_SLP_SUS_L

U7940 74AUP1G3208 SOT891 (VCC, GND)

PM_SUS_EN (MAKE_BASE=TRUE) → =P5VSUS_EN, =P3V3SUS_EN

NO STUFF R7917 0 5% 1/16W MF-LF 402

S0 ENABLE

PM_SLP_S3_L → R7978 100 5% 1/16W MF-LF 402

PM_SLP_S3_L:100K pull down in PCH page

CHGR VFRQ Generation

=PP3V42_G3H_CHGR → R7931 100K 5% 1/16W MF-LF 402 → CHGR_VFRQ

Q7931 SSM3K15FV SOD-VESM-HF

VFRQ Low Fix Frequency
VFRQ High Variable Frequency

S0 Rail PGOOD (BJT Version)

=PP3V3_S0_VMON → R7951 15.0K 1% 1/16W MF-LF 402
=PP3V3_S5_VMON → R7956 150K 1% 1/16W MF-LF 402

R7953 1K 5% 1/16W MF-LF 402 (VMON_3V3_DIV)
R7952 7.15K 1% 1/16W MF-LF 402
R7954 1K 5% 1/16W MF-LF 402 (VMON_Q3_BASE)
=PP1V5_S3RS0_VMON
R7955 1K 5% 1/16W MF-LF 402 (VMON_Q4_BASE)
=PP1V05_S0_VMON

Q7950 ASMCC0179 DFN2015H4-8 (Q1, Q2, Q3, Q4) — CRITICAL

S0PGD_C
ALL_SYS_PWRGD
353S2809
S0PGD_BJT_GND_R

Worst-Case Thresholds:
Q2: 0.XXXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V

R7957 100 5% 1/16W MF-LF 402

3.3V SUS Detect

=PP3V3_S5_PWRCTL → C7930 0.1UF 20% 10V CERM 402 (PLACE NEAR U7930 6 2 3mm)

No stuff C7931, 12ms Min delay time
U7930 Sense input threhold is 3.07V

CRITICAL

U7930 TPS3808G33DBVRG4 SOT23-6 (SENSE, RESET*, MR*, VDD, GND)

=PP3V3_SUS_CNTRL → R7933 100K 5% 1/16W MF-LF 402
=PP3V3_SUS_CNTRL → PM_RSMRST_L

PM_RSMRST_L goes to U1800.C21

Sus_PGOOD_4CT

C7931 0.001UF 20% 25V CERM 402 — NO STUFF

PCH S0 PWRGD

=PP3V3_S5_PCHPWRGD
=PP3V3_S0_SB_PM

R7950 1K 5% 1/16W MF-LF 402
C7950 0.1UF 20% 10V CERM 402

ALL_SYS_PWRGD
CPUIMVP_PGOOD

U7950 74LVC2G08GT SOT833 (PLACE NEAR U1800 P12 7mm)

PM_S0_PGOOD → R7949 1K 5% 1/16W MF-LF 402 → SYS_PWROK_R → PM_PCH_SYS_PWROK

PM_PCH_APWROK

SMC_DELAYED_PWRGD → R7948 0 5% 1/16W MF-LF 402 → PM_PCH_PWROK (MAKE_BASE=TRUE)

S0 Rail PGOOD Circuitry (ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

=PP5V_S0_VMON
=PP1V5_S3RS0_VMON
=PP1V05_S0_VMON
=PP3V3_S0_VMON

R7960 6.04K 1% 1/16W MF-LF 402
R7970 10K 1% 1/16W MF-LF 402
R7972 6.04K 1% 1/16W MF-LF 402
R7961 15.0K 1% 1/16W MF-LF 402
R7971 12.4K 1% 1/16W MF-LF 402
R7973 15.0K 1% 1/16W MF-LF 402

C7960 0.1UF 20% 10V CERM 402

U7960 ISL88042IRTEZ TDFN (V2MON, V3MON, VMON, VDD, RST*, GND, THRM_PAD) — CRITICAL

S0PGOOD_ISL
P5V_DIV_VMON
P1V5_DIV_VMON
P1V05_VID_VMON
353S2310

=PP3V3_S0_PWRCTL → R7967 10K 1% 1/16W MF-LF 402

R7968 100 5% 1/16W MF-LF 402 ← P1V5S0_PGOOD
R7966 100 5% 1/16W MF-LF 402 ← P1V8S0_PGOOD
R7965 100 5% 1/16W MF-LF 402 ← P5VS4_PGOOD
R7969 100 5% 1/16W MF-LF 402 ← CPUVCCIOS0_PGOOD
R7963 100 5% 1/16W MF-LF 402 ← PVCCSA_PGOOD

S0PGOOD_ISL → R7962 330 5% 1/16W MF-LF 402 → ALL_SYS_PWRGD

"WLAN" = ("S3" && "AP_PWR_EN")

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

SMC_ADAPTER_EN → Q7920 SSM6N37FEAPE SOT563 (NO STUFF R7929 0 5% 1/16W MF-LF 402)
PM_SLP_S3_L → Q7920 SSM6N37FEAPE SOT563
AC_EN_L

Q7925 SSM6N15AFE SOT563
PM_WLAN_EN_L
=PP3V3_S3_WLAN → R7926 10K 5% 1/16W MF-LF 402
PM_WLAN_EN
R7925 10K 5% 1/16W MF-LF 402
Q7925 SSM6N15AFE SOT563
AP_PWR_EN

1.2V, 5V, 3.3V, DDR S3 ENABLE (PM_SLP_S3_R_L)

PM_SLP_S3_R_L (MAKE_BASE=TRUE)

R7987 33K 5% 1/16W MF-LF 402 (PLACE NEAR U7100 15 6mm)
R7981 20K 5% 1/16W MF-LF 402 (PLACE NEAR U7600 3 6mm)
R7985 20K 5% 1/16W MF-LF 402
R7988 10K 5% 1/16W MF-LF 402 (PLACE NEAR U7770 3 6mm)
R7986 5.1K 5% 1/16W MF-LF 402 (PLACE NEAR U7760 B3 6mm)

C7987 0.47UF 10% 6.3V X5R 402 (PLACE NEAR U7100 15 6mm)
C7981 0.47UF 10% 6.3V X5R 402 (PLACE NEAR U7600 3 6mm)
C7984 0.47UF 10% 6.3V X5R 402 (PLACE NEAR U7770 3 6mm)
C7988 0.47UF 10% 6.3V X5R 402 (PLACE NEAR U7770 3 6mm)
C7986 0.47UF 10% 6.3V X5R 402 (PLACE NEAR U7760 B3 6mm)

=P5VS0_EN
=P3V3S0_EN
=PBUSVSENS_EN
=TBT_S0_EN
P1V8S0_EN → =P1V8S0_EN (MAKE_BASE=TRUE)
P1V5S0_EN → =P1V5S0_EN (MAKE_BASE=TRUE)
P1V05S0_EN (Replaced by TBT EN LC ISOL)
CPUVCCIOS0_EN → =CPUVCCIOS0_EN (MAKE_BASE=TRUE)
PVCCSA_EN → =PVCCSA_EN (MAKE_BASE=TRUE)

SYNC_MASTER=MASTER
SYNC_DATE=MASTER
PAGE TITLE: Power Control 1/ENABLE

Apple Inc.

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LCD PANEL INTERFACE (eDP)

LCD Panel HPD & AUX strapping

LCD Panel Current XW Short

EDP: 1 A, Refdes: XW9020

LCD_HPD	R9000 0 5% 1/20W MF 201
DP_INT_AUX_C_P	C9028 0.1UF 10% 10V X5R-CERM 0201
DP_INT_AUX_C_N	C9029 0.1UF 10% 10V X5R-CERM 0201
DP_INT_ML_C_P<0>	C9020 0.1UF 10% 10V X5R-CERM 0201
DP_INT_ML_C_N<0>	C9021 0.1UF 10% 10V X5R-CERM 0201
DP_INT_ML_C_P<1>	C9022 0.1UF 10% 10V X5R-CERM 0201
DP_INT_ML_C_N<1>	C9023 0.1UF 10% 10V X5R-CERM 0201
DP_INT_ML_C_P<2>	C9024 0.1UF 10% 10V X5R-CERM 0201
DP_INT_ML_C_N<2>	C9025 0.1UF 10% 10V X5R-CERM 0201
DP_INT_ML_C_P<3>	C9026 0.1UF 10% 10V X5R-CERM 0201
DP_INT_ML_C_N<3>	C9027 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
J9000
20525-130E-01
F-RT-SM

PPVOUT_S0_LCDBKLT	31
NC	1
LED_RETURN_6	2
LED_RETURN_5	3
LED_RETURN_4	4
LED_RETURN_3	5
LED_RETURN_2	6
LED_RETURN_1	7
LCD_HPD_CONN	8
LCD_FSS	9
DP_INT_AUX_P	10
DP_INT_AUX_N	11
DP_INT_ML_P<0>	12
DP_INT_ML_N<0>	13
DP_INT_ML_P<1>	14
DP_INT_ML_N<1>	15
DP_INT_ML_P<2>	16
DP_INT_ML_N<2>	17
DP_INT_ML_P<3>	18
DP_INT_ML_N<3>	19
	20
	21
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	32

518S0829

CRITICAL
U9000
FPF1009
MFET-2X2-8IN

=PP5V_S0_LCD	1 ON, 2 VIN_1, 3 VIN_2, 4 VOUT_1, 5 VOUT_2, 6 GND, 7 THRM PAD
C9009	0.1UF 10% 16V X7R-CERM 0402
C9011	0.1UF 10% 16V X7R-CERM 0402
C9012	10UF 20% 6.3V X5R 603
PP5VR3V3_SW_LCD_ISNS	MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V
XW9020	SM
PP5VR3V3_SW_LCD_UF	MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V
L9000	CRITICAL, FERR-220-OHM, 0805
PP5VR3V3_SW_LCD	MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V
C9001	0.1UF 10% 16V X5R-CERM 0201
C9002	0.1UF 10% 16V X5R-CERM 0201
C9003	1000PF 10% 100V X7R-CERM 0603
C9000	1000PF 10% 100V X7R-CERM 0603
NC_ISNS_LCD_PANELN	
NC_ISNS_LCD_PANELP	

=PP3V3_S0_LCD

R9003	1M 5% 1/20W MF 201, NO_XNET_CONNECTION=TRUE
DP_INT_AUX_N	
LCD_HPD_CONN	
DP_INT_AUX_P	
R9001	1M 5% 1/20W MF 201
R9002	1M 5% 1/20W MF 201, NO_XNET_CONNECTION=TRUE

LCD_PWR_EN

R9010 1K 5% 1/10W MF 402

BP9000	BEAD-PROBE SM, NO_XNET_CONNECTION=TRUE
BP9001	BEAD-PROBE SM, NO_XNET_CONNECTION=TRUE
BP9002	BEAD-PROBE SM, NO_XNET_CONNECTION=TRUE
BP9003	BEAD-PROBE SM, NO_XNET_CONNECTION=TRUE
BP9004	BEAD-PROBE SM, NO_XNET_CONNECTION=TRUE
BP9005	BEAD-PROBE SM, NO_XNET_CONNECTION=TRUE
BP9006	BEAD-PROBE SM, NO_XNET_CONNECTION=TRUE
BP9007	BEAD-PROBE SM, NO_XNET_CONNECTION=TRUE
R9011	1M 5% 1/20W MF 201, NO_XNET_CONNECTION=TRUE
R9012	1M 5% 1/20W MF 201, NO_XNET_CONNECTION=TRUE
R9013	1M 5% 1/20W MF 201, NO_XNET_CONNECTION=TRUE
R9014	1M 5% 1/20W MF 201, NO_XNET_CONNECTION=TRUE
R9015	1M 5% 1/20W MF 201, NO_XNET_CONNECTION=TRUE
R9016	1M 5% 1/20W MF 201, NO_XNET_CONNECTION=TRUE
R9017	1M 5% 1/20W MF 201, NO_XNET_CONNECTION=TRUE
R9018	1M 5% 1/20W MF 201, NO_XNET_CONNECTION=TRUE

BEAD_PROBE=TRUE
DP_INT_ML_P<0>
DP_INT_ML_N<0>
DP_INT_ML_P<1>
DP_INT_ML_N<1>
DP_INT_ML_P<2>
DP_INT_ML_N<2>
DP_INT_ML_P<3>
DP_INT_ML_N<3>

SYNC_MASTER=D1_SENSORS
SYNC_DATE=07/11/2012

PAGE TITLE
eDP Display Connector

Apple Inc.

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DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!

8 =PP3V3_S0_DDCMUX

R9251 R9252 R9253 R9254
2.2K 1% 1/20W MF 201

C9280 0.1UF 20% 10V CERM 402

U9200
TS3DS10224
QFN
CRITICAL

69 OUT DP_TBTPA_DDC_CLK	1	INA+	
69 BI DP_TBTPA_DDC_DATA	2	INA-	
	16	ENA	
	14	SAI	
	10	ENB	
70 OUT DP_TBTPB_DDC_CLK	3	INB+	
70 BI DP_TBTPB_DDC_DATA	4	INB-	
33 IN TBT_DDC_XBAR_EN_L	12	SBI	
	13	VCC	
	5	GND	
	21	THRM PAD	
	20	OUTA1+	
	19	OUTA1-	
	18	OUTA0+	DP_TBTSNK0_DDC_CLK IN 9
	17	OUTA0-	DP_TBTSNK0_DDC_DATA BI 9
	15	SAO	
	6	OUTB1+	
	7	OUTB1-	
	8	OUTB0+	DP_TBTSNK1_DDC_CLK IN 9
	9	OUTB0-	DP_TBTSNK1_DDC_DATA BI 9
	11	SBO	

SAI/SBI = 1: INA == OUTA0, INB == OUTB0
SAI/SBI = 0: INA == OUTB0, INB == OUTA0

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: DDC Crossbar

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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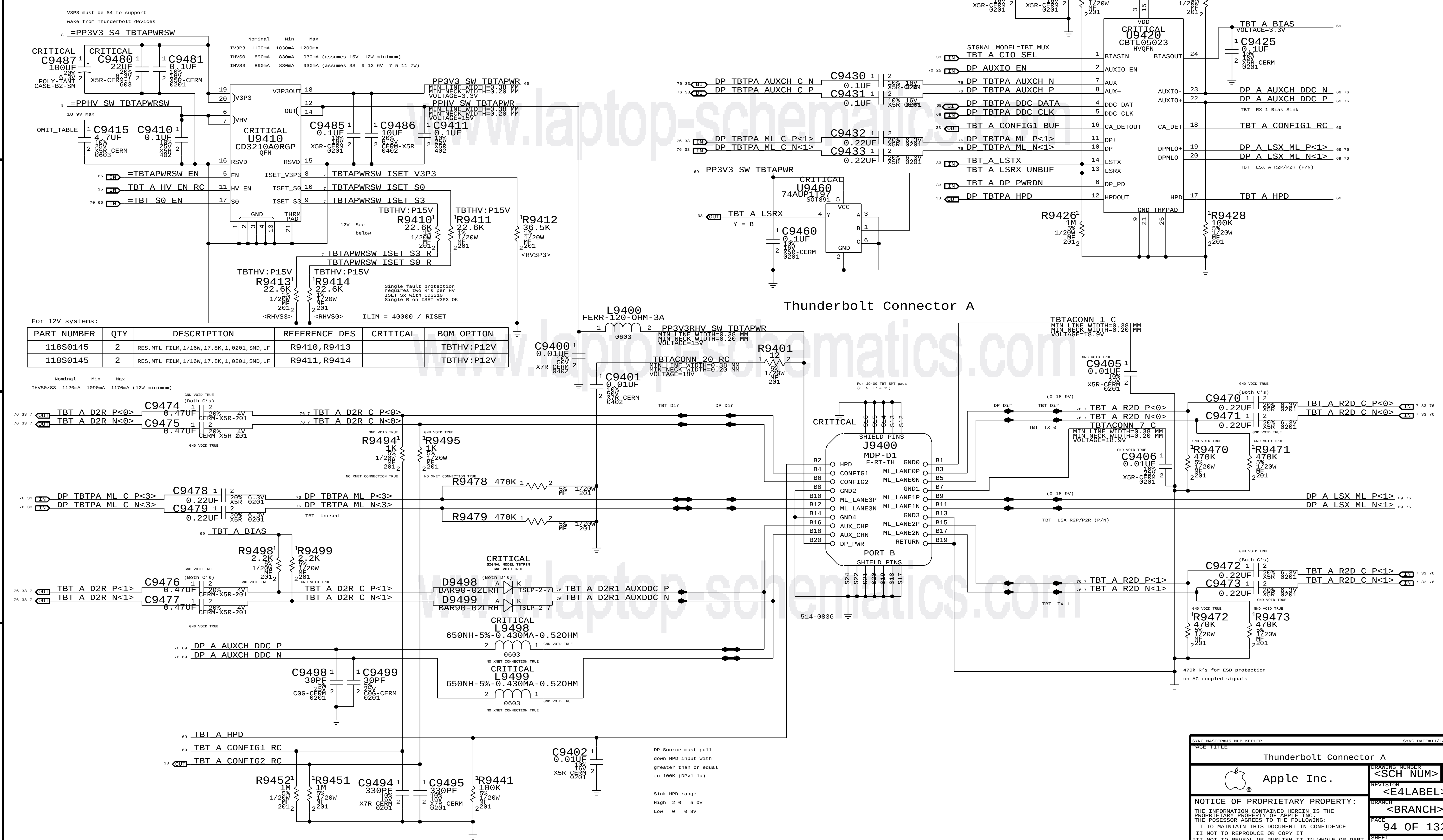
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X5R,0603,MURATA	C9415	CRITICAL	

3.3V/HV Power MUX

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9411,R9414		TBTHV:P12V

Thunderbolt Connector A



SYNC MASTER=J5 MLB KEPLER SYNC DATE=11/14/2011

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

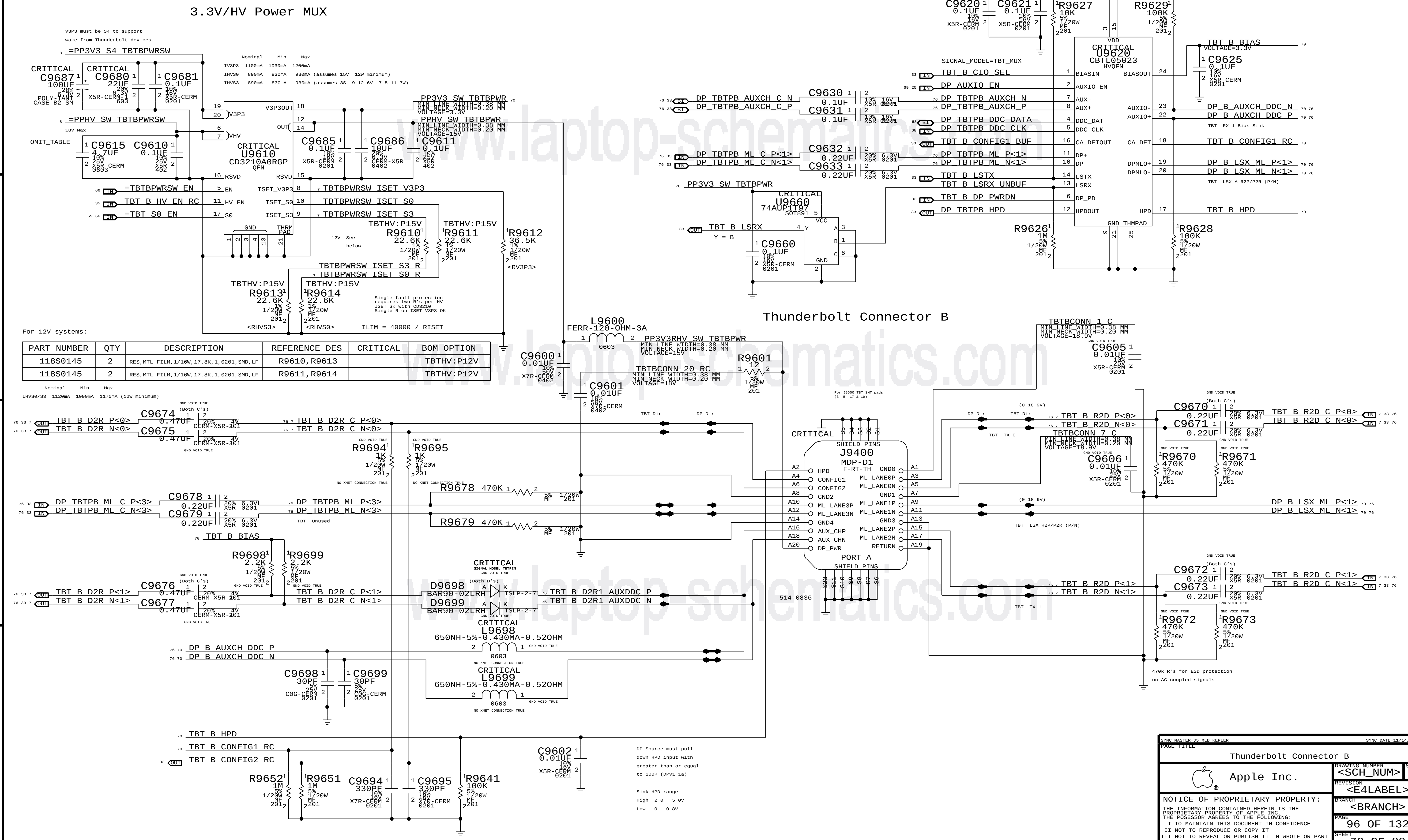
DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X5R,0603,MURATA	C9615	CRITICAL	

3.3V/HV Power MUX



For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9610,R9613		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9611,R9614		TBTHV:P12V

SYNC MASTER=J5_MLB_KEPLER SYNC DATE=11/14/2011

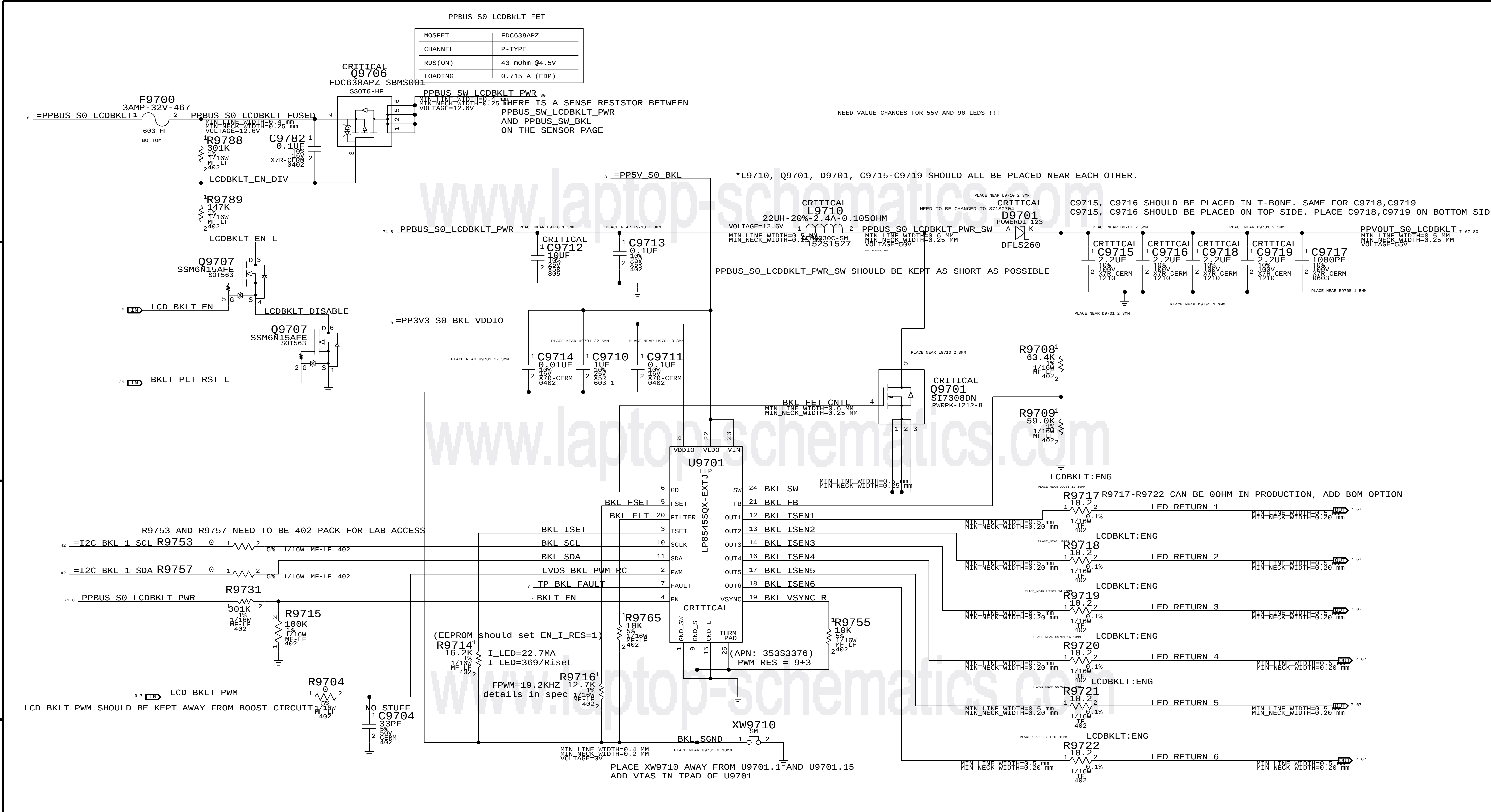
PAGE TITLE: Thunderbolt Connector B

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>


PPBUS S0 LCDBKLT FET
MOSFET FDC638APZ
CHANNEL P-TYPE
RDS(ON) 43 mOhm @4.5V
LOADING 0.715 A (EDP)
CRITICAL Q9706 FDC638APZ_SBMS001 SSOT6-HF
F9700 3AMP-32V-467 603-HF BOTTOM
=PPBUS_S0_LCDBKLT
PPBUS_S0_LCDBKLT_FUSED
PPBUS_SW_LCDBKLT_PWR
THERE IS A SENSE RESISTOR BETWEEN
PPBUS_SW_LCDBKLT_PWR
AND PPBUS_SW_BKL
ON THE SENSOR PAGE
NEED VALUE CHANGES FOR 55V AND 96 LEDS !!!
R9788 301K 1% 1/16W MF-LF 402
C9782 0.1UF 10% 16V X7R-CERM 0402
LCDBKLT_EN_DIV
R9789 147K 1% 1/16W MF-LF 402
LCDBKLT_EN_L
Q9707 SSM6N15AFE SOT563
LCD_BKLT_EN
LCDBKLT_DISABLE
BKLT_PLT_RST_L
=PP5V_S0_BKL
*L9710, Q9701, D9701, C9715-C9719 SHOULD ALL BE PLACED NEAR EACH OTHER.
C9715, C9716 SHOULD BE PLACED IN T-BONE. SAME FOR C9718,C9719
C9715, C9716 SHOULD BE PLACED ON TOP SIDE. PLACE C9718,C9719 ON BOTTOM SIDE
PPBUS_S0_LCDBKLT_PWR
CRITICAL C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
CRITICAL L9710 22UH-20%-2.4A-0.105OHM 152S1527
PPBUS_S0_LCDBKLT_PWR_SW
CRITICAL D9701 POWERDI-123 DFLS260
PPVOUT_S0_LCDBKLT
VOLTAGE=55V
CRITICAL C9715 2.2UF 10% 100V X7R-CERM 1210
CRITICAL C9716 2.2UF 10% 100V X7R-CERM 1210
CRITICAL C9718 2.2UF 10% 100V X7R-CERM 1210
CRITICAL C9719 2.2UF 10% 100V X7R-CERM 1210
C9717 1000PF 10% 100V X7R-CERM 0603
PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE
=PP3V3_S0_BKL_VDDIO
C9714 0.01UF 10% 16V X7R-CERM 0402
C9710 1UF 10% 25V X5R 603-1
C9711 0.1UF 10% 16V X7R-CERM 0402
BKL_FET_CNTL
CRITICAL Q9701 SI7308DN PWRPK-1212-8
R9708 63.4K 1% 1/16W MF-LF 402
R9709 59.0K 1% 1/16W MF-LF 402
LCDBKLT:ENG
U9701 LP8545SQX-EXTJ LLP
VDDIO VLDO VIN GD FSET FILTER ISET SCLK SDA PWM FAULT EN SW FB OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 VSYNC GND_SW GND_S GND_L THRM PAD
BKL_FSET BKL_FLT BKL_ISET BKL_SCL BKL_SDA LVDS_BKL_PWM_RC TP_BKL_FAULT BKLT_EN
BKL_SW BKL_FB BKL_ISEN1 BKL_ISEN2 BKL_ISEN3 BKL_ISEN4 BKL_ISEN5 BKL_ISEN6 BKL_VSYNC_R
R9717-R9722 CAN BE 0OHM IN PRODUCTION, ADD BOM OPTION
R9717 10.2 0.1% 1/16W TF 402 LED_RETURN_1
R9718 10.2 0.1% 1/16W TF 402 LED_RETURN_2
R9719 10.2 0.1% 1/16W TF 402 LED_RETURN_3
R9720 10.2 0.1% 1/16W TF 402 LED_RETURN_4
R9721 10.2 0.1% 1/16W TF 402 LED_RETURN_5
R9722 10.2 0.1% 1/16W TF 402 LED_RETURN_6
R9753 AND R9757 NEED TO BE 402 PACK FOR LAB ACCESS
=I2C_BKL_1_SCL R9753 0 5% 1/16W MF-LF 402
=I2C_BKL_1_SDA R9757 0 5% 1/16W MF-LF 402
R9731 301K 1% 1/16W MF-LF 402
R9715 100K 1% 1/16W MF-LF 402
R9765 10K 5% 1/16W MF-LF 402
R9755 10K 5% 1/16W MF-LF 402
(EEPROM should set EN_I_RES=1)
R9714 16.2K 1% 1/16W MF-LF 402
I_LED=22.7MA
I_LED=369/Riset
R9716 12.7K 1% 1/16W MF-LF 402
FPWM=19.2KHZ
details in spec
(APN: 353S3376)
PWM RES = 9+3
LCD_BKLT_PWM
R9704 0 5% 1/16W MF-LF 402
LCD_BKLT_PWM SHOULD BE KEPT AWAY FROM BOOST CIRCUIT
NO STUFF C9704 33PF 5% 50V CERM 402
BKL_SGND
XW9710 SM
PLACE XW9710 AWAY FROM U9701.1 AND U9701.15
ADD VIAS IN TPAD OF U9701

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	6	RES,MTL FILM,1/16W,0,5,0402,SMD,LF	R9717,R9718,R9719,R9720,R9721,R9722	CRITICAL	LCDBKLT:PROD

SYNC MASTER=J5 MLB KEPLER SYNC DATE=09/21/2011

PAGE TITLE: LCD Backlight Driver (LP8545)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.1MM	0.1MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	=4X_DIELECTRIC	?
CPU_ITP	*	=4x_DIELECTRIC	?
CPU_VCCSENSE	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=6X_DIELECTRIC	?
CLK_PCIE	*	=5X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	7 10 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	7 10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	7 10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	7 10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	7 10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	7 10 18
FDI_FSYNC	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	10 18
FDI_LSYNC	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	10 18
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	10 18
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	7 11 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	7 11 17
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_COMP	10
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 24
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 17
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 17
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	17 24
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	17 24
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLK_P	11 17
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLK_N	11 17
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 24
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 24
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 24
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 24
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 24
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	11 24
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	11 24
XDP_BRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	11 24 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	11 24
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	11 24
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	11 39
CPU_PROC_SEL_L	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	11 20
CPU_PECI	CPU_50S	CPU_VID	CPU_PECI	11 20 40
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 39 40 61
XDP_CPU_PWRGD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	24
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	11 20 40
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	11 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	11 18 27
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	11 20 24
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	11
	CPU_50S	CPU_VID	CPU_VIDSOUT	13 61
	CPU_50S	CPU_VID	CPU_VIDSCLK	13 61
	CPU_50S	CPU_VID	CPU_VIDALERT_L	13 61
	CPU_55S	CPU_VID	CPU_VCCSA_VID<1..0>	13 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	13 63
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	13 63
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	10
CPU_VCCSASENSE	CPU_50S	CPU_AGTL	CPU_VCCSASENSE	13 58
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_A	10 31
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_B	10 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_A	28 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	29 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_A	28 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	29 31
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	24
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	24

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	72 OHM DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	85 OHM DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4X_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3X_DIELECTRIC	?
MEM_CTRL2MEM	*	=3X_DIELECTRIC	?
MEM_CMD2CMD	*	=2X_DIELECTRIC	?
MEM_CMD2MEM	*	=3X_DIELECTRIC	?
MEM_DATA2DATA	*	=2X_DIELECTRIC	?
MEM_DATA2MEM	*	=3X_DIELECTRIC	?
MEM_DQS2MEM	*	=4X_DIELECTRIC	?
MEM_2OTHER	*	=6X_DIELECTRIC	?
MEM_DQBL2BL	*	=4X_DIELECTRIC	?
MEM_DQCH2CH	*	=6X_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_*	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_*	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_*	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_*	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQ_BYTE*	MEM_*	*	MEM_DATA2MEM
MEM_*_DQ_BYTE*	=SAME	*	MEM_DATA2DATA
MEM_A_DQ_BYTE*	MEM_A_DQ_BYTE*	*	MEM_DQBL2BL
MEM_B_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQBL2BL
MEM_A_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQCH2CH

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<0>	12 28 30
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<0>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<1..0>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<1>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<0>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<1>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	12 28 30
MEM_A_DQ_BYTE0	MEM_50S	MEM_A_DQ_BYTE0	MEM_A_DQ<7..0>	7 12 28
MEM_A_DQ_BYTE1	MEM_50S	MEM_A_DQ_BYTE1	MEM_A_DQ<15..8>	7 12 28
MEM_A_DQ_BYTE2	MEM_50S	MEM_A_DQ_BYTE2	MEM_A_DQ<23..16>	7 12 28
MEM_A_DQ_BYTE3	MEM_50S	MEM_A_DQ_BYTE3	MEM_A_DQ<31..24>	7 12 28
MEM_A_DQ_BYTE4	MEM_50S	MEM_A_DQ_BYTE4	MEM_A_DQ<39..32>	7 12 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_A_DQ_BYTE5	MEM_A_DQ<47..40>	7 12 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_A_DQ_BYTE6	MEM_A_DQ<55..48>	7 12 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_A_DQ_BYTE7	MEM_A_DQ<63..56>	7 12 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	12 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	12 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	12 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	12 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	12 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	12 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	12 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	12 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	12 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	12 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	12 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	12 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	12 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	12 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	12 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	12 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<0>	12 29 30
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<0>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<1>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<0>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<1..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	12 29 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_B_DQ_BYTE0	MEM_B_DQ<7..0>	7 12 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_B_DQ_BYTE1	MEM_B_DQ<15..8>	7 12 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_B_DQ_BYTE2	MEM_B_DQ<23..16>	7 12 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_B_DQ_BYTE3	MEM_B_DQ<31..24>	7 12 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_B_DQ_BYTE4	MEM_B_DQ<39..32>	7 12 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_B_DQ_BYTE5	MEM_B_DQ<47..40>	7 12 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_B_DQ_BYTE6	MEM_B_DQ<55..48>	7 12 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_B_DQ_BYTE7	MEM_B_DQ<63..56>	7 12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	12 29

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Chief River SFF Platform DG, Rev 0.7 (#460452), Section 2.6.3

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Digital Video Signal Constraints

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA 90D	*	90_OHM_DIFF	90 OHM DIFF	90 OHM DIFF	90 OHM DIFF	90 OHM DIFF	90 OHM DIFF
SATA 37SE	*	37_OHM_SE	37 OHM SE	37 OHM SE	37 OHM SE	37 OHM SE	37 OHM SE
SATA 50SE	*	50_OHM_SE	50 OHM SE	50 OHM SE	50 OHM SE	50 OHM SE	50 OHM SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	5 1 SPACING	?
SATA ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP BOTTOM	5 1 SPACING	?

SOURCE HR PLATFORM DESIGN GUIDE TABLES 191 193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH USB RBIAS	*	STANDARD	STANDARD	STANDARD	STANDARD	STANDARD	STANDARD
USB 85D	*	85_OHM_DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	4 1 SPACING	?
USB RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP BOTTOM	4 1 SPACING	?

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USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3 85D	*	85_OHM_DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	*	5 1 SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	TOP BOTTOM	5 1 SPACING	?

SOURCE CR SFF PLATFORM DESIGN GUIDE V0 7 TABLE 4 211 1X1+

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	SPACING	
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRIN_P 7
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRIN_N 7
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDROUT_P 7
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDROUT_N 7
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRIN_P 7
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRIN_N 7
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDROUT_N 7
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDROUT_P 7
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RC_P 7 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RC_N 7 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_N 7 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_P 7 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P 7 17 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_N 7 17 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P 7 17 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_N 7 17 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_SSDRHDD_D2R_P 7 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_SSDRHDD_D2R_N 7 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_SSDRHDD_R2D_P 7 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_SSDRHDD_R2D_N 7 37
PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP 17
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP 17
USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_P 19 26
USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_N 19 26
USB_EXTB	USB_85D	USB	USB_EXTB_EHCI_P 19 26
USB_EXTB	USB_85D	USB	USB_EXTB_EHCI_N 19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_P 19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_N 19 26
USB_EXTA	USB_85D	USB	USB_EXTA_P 19 38
USB_EXTA	USB_85D	USB	USB_EXTA_N 19 38
USB_EXTB	USB_85D	USB	USB_EXTB_P 7 26 36
USB_EXTB	USB_85D	USB	USB_EXTB_N 7 26 36
USB_EXTC	USB_85D	USB	USB_EXTD_P
USB_EXTC	USB_85D	USB	USB_EXTD_N
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P 7 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_N 7 32
USB_BT	USB_85D	USB	USB_BT_P 7 9 36
USB_BT	USB_85D	USB	USB_BT_N 7 9 36
USB_TPAD	USB_85D	USB	USB_TPAD_P 9 47
USB_TPAD	USB_85D	USB	USB_TPAD_N 9 47
USB_SMC	USB_85D	USB	USB_SMC_P 9 39
USB_SMC	USB_85D	USB	USB_SMC_N 9 39
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS 19
USB_EXTD	USB_85D	USB	USB_EXTD_XHCI_P 19 26
USB_EXTD	USB_85D	USB	USB_EXTD_XHCI_N 19 26
USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P 38
USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_N 38
USB_CAMERA	USB_85D	USB	USB_CAMERA_P 19 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_N 19 32
USB_EXTA	USB_85D	USB	USB_LT1_P 7 38
USB_EXTA	USB_85D	USB	USB_LT1_N 7 38
USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_P 19 36
USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_N 19 36
USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_P 7 19 36
USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_N 7 19 36
USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_P 19 38
USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_N 7 19 38
USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_P 7 19 38
USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_N 7 19 38

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	SPACING	
SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC 17 25
SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB 17 25
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R 17
SYSCLK_CLK25M_ENET	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R
SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT 25 33
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT_R 33

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
LPC_AD	LPC_50S	LPC	LPC AD<3..0>	7 17 39 41
LPC_FRAME_L	LPC_50S	LPC	LPC FRAME L	7 17 39 41
LPC_RESET_L	LPC_50S	LPC	LPC RESET L	25
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC R	19 25
	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC	7 25 39
	CLK_LPC_50S	CLK_LPC	LPC CLK33M LPCPLUS	7 25 41
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS PCH CLK	7 17 42
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS PCH DATA	7 17 42
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML PCH 0 CLK	17 42
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML PCH 0 DATA	17 42
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SML PCH 1 CLK	17 42
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SML PCH 1 DATA	17 42
HDA_BIT_CLK	HDA_50S	HDA	HDA BIT CLK	17 51
	HDA_50S	HDA	HDA BIT CLK R	17
HDA_SYNC	HDA_50S	HDA	HDA SYNC	17 51
	HDA_50S	HDA	HDA SYNC R	17
HDA_RST_L	HDA_50S	HDA	HDA RST R L	17
	HDA_50S	HDA	HDA RST L	17 51
HDA_SDIN0	HDA_50S	HDA	HDA SDIN0	17 51
	HDA_50S	HDA	AUD SDI R	51
HDA_SDOUT	HDA_50S	HDA	HDA SDOUT	17 51
	HDA_50S	HDA	HDA SDOUT R	17 25
SPI_CLK	SPI_55S	SPI	SPI CLK R	17 41
	SPI_55S	SPI	SPI CLK	41
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	17 41
	SPI_55S	SPI	SPI MOSI	41
SPI_MISO	SPI_55S	SPI	SPI MISO	17 41
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	17 41
	SPI_55S	SPI	SPI CS0 L	41
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D C P	7 17 36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D C N	7 17 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R P	7 17 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R N	7 17 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D P	7 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D N	7 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D C P	7 17 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D C N	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R P	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R N	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R PI P	7 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R PI N	7 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP R2D PI P	7 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP R2D PI N	7 36
PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M PCH P	7 17
PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M PCH N	7 17
PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M TBT P	7 17 33
PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M TBT N	7 17 33
PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH CLK96M DOT P	17
PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH CLK96M DOT N	17
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M SATA P	7 17
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M SATA N	17
	CPU_50S	CLK_PCIE	PCH CLK14P3M REFCLK	17
	CPU_50S	CLK_PCIE	PCH CLK33M PCIIN	7 17 25
PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M SSD P	7 9 17
PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M SSD N	7 9 17
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG CLK100M P	7 9 17
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG CLK100M N	7 9 17
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET P	7 17 36
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET N	7 17 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP P	7 17 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP N	7 17 36
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW P	7 9 17
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW N	7 9 17
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M EXCARD P	7 17
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M EXCARD N	7 17
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE TBT R2D C P<3..0>	7 9 33
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE TBT R2D C N<3..0>	7 9 33
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE TBT R2D P<3..0>	7 33
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE TBT R2D N<3..0>	7 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE TBT D2R P<3..0>	7 9 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE TBT D2R N<3..0>	7 9 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE TBT D2R C P<3..0>	7 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE TBT D2R C N<3..0>	7 33

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2013

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

NOTE: Thunderbolt high-speed nets are NOT directly assigned to TBTDP_*D physical rules.
TABLE_PHYSICAL_ASSIGNMENT symbols must be used to create the assignments.
Proper differential impedance depends on mDP connector used.
For 514-0637: R2D nets (SMT pins) = 80D, D2R nets (TH pins) = 100D

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
HDMI	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMI	TOP,BOTTOM	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_P<1..0>	7 33 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_N<1..0>	7 33 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_P<1..0>	7 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_N<1..0>	7 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3..1:2>	33 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3..1:2>	33 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3..1:2>	69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3..1:2>	69
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	69
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<1>	7 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<1>	7 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<0>	7 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<0>	7 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_P<1>	7 33 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_N<1>	7 33 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_P<0>	7 33 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_N<0>	7 33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	69
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	69
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_P	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_N	69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_P<1..0>	7 33 70
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_N<1..0>	7 33 70
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_P<1..0>	7 70
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_N<1..0>	7 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3..1:2>	33 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3..1:2>	33 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3..1:2>	70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3..1:2>	70
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	70
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<0>	7 70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<0>	7 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<1>	7 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<1>	7 70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_P<0>	7 33 70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_N<0>	7 33 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_P<1>	7 33 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_N<1>	7 33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	70
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	70
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_P	70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_N	70

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	33
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	33
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	33
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	33

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=T29_CR SYNC_DATE=08/31/2011

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	NET TYPE SPACING		
SMBUS_SMC_2_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL	7 39 42
SMBUS_SMC_2_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA	7 39 42
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL	7 39 42
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA	7 39 42
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	39 42
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	39 42
SMBUS_SMC_5_SCL	SMB_50S	SMB	SMBUS_SMC_5_SCL	
SMBUS_SMC_5_SDA	SMB_50S	SMB	SMBUS_SMC_5_SDA	
SMBUS_SMC_3_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL	39 42
SMBUS_SMC_3_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA	39 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	NET TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	57
CHGR_CST	1TO1_DIFFPAIR		CHGR_CSI_N	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_N	57

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_CLK	*	GND_P2MM
GND	MEM_CMD	*	GND_P2MM
GND	MEM_CTRL	*	GND_P2MM
GND	MEM_*_DQ_BYTE*	*	GND_P2MM
GND	MEM_DQS	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB3	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB3	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DDR3 Loaded Segment Constraint Relaxations
Alternate single ended and differential impedances between devices.

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_37S	BGA_MEM	MEM_50S
MEM_40S	BGA_MEM	MEM_50S
MEM_72D	BGA_MEM	MEM_85D

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
1TO1_DIFFPAIR	*	1:1_DIFFPAIR
SENSE_1TO1_55S	*	SENSE_1TO1_55S
THERM_1TO1_55S	*	THERM_1TO1_55S
DIFFPAIR	*	DIFFPAIR

Graphics, SATA Constraint Relaxations
Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

D1 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	NET TYPE SPACING	
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P 45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N 45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P 9 10
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_N 9 10
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P 45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N 45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P 45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_N 45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	TBT_THERMD_P 45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	TBT_THERMD_N 45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_P 45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_N 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P 43 63
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N 43 63
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VDDQ_SENSE_P 13
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VDDQ_SENSE_N 13
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCD_PANEL_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCD_PANEL_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_P 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_N 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_SSD_P 37 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_SSD_N 37 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_3V3_S0_SSD_R_P 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_3V3_S0_SSD_R_N 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_WLAN_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_WLAN_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_P 80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_N 80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_R_P 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_R_N 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P 58 80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N 58 80
HDMI_CLK	HDMI_90D	HDMI	HDMI_IG_CLK_C_P 7 9 36
HDMI_CLK	HDMI_90D	HDMI	HDMI_IG_CLK_C_N 7 9 36
HDMI_DATA	HDMI_90D	HDMI	HDMI_IG_DATA_C_P<2..0> 7 9 36
HDMI_DATA	HDMI_90D	HDMI	HDMI_IG_DATA_C_N<2..0> 7 9 36

D1 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	NET TYPE SPACING	
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P 7 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N 7 36
	1TO1_DIFFPAIR		CHGR_CSI_R_P 57
	1TO1_DIFFPAIR		CHGR_CSI_R_N 57
	1TO1_DIFFPAIR		CHGR_CSO_R_P 57
	1TO1_DIFFPAIR		CHGR_CSO_R_N 57
USB_BT	USB_85D	USB	USB_BT_CONN_P 36
USB_BT	USB_85D	USB	USB_BT_CONN_N 36
USB_BT	USB_85D	USB	USB_BT_WAKE_P 36
USB_BT	USB_85D	USB	USB_BT_WAKE_N 36
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P 7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N 7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P 7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N 7 53 55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_P 7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_N 7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_P 7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_N 7 53 55 78
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_P 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_N 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P 43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N 43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_P 43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_N 43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P 44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N 44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P 44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N 44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P 43 61 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N 43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P 43 61 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N 43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N 43
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P 51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N 51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P 51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N 51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P 51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N 51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P 51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N 51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P 51 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N 51 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN_P 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN_N 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN_P 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN_N 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_P 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_N 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_P 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_N 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_HI_RC 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_LO_RC 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_HI 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_LO 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_P 7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_N 7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_P 7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_N 7 53 55 78
USB_TPAD	USB_85D	USB	USB_TPAD_R_P 26 47
USB_TPAD	USB_85D	USB	USB_TPAD_R_N 26 47
USB_HUB	USB_85D	USB	PU_USBHUB_DN4_P 9
USB_HUB	USB_85D	USB	PU_USBHUB_DN4_N 9
		SB_POWER	PP3V3_S5 7 8
		SB_POWER	PP3V3_S0 7 8
		SB_POWER	PP1V5_S3RS0_CPUDDR 8
		GND	GND

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Project Specific Constraints

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D1 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_MEM	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
50_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.105 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.120 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.079 MM	0.079 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

Stackup-Defined Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP BOTTOM	0.1 MM	?
1:1_SPACING	ISL3 ISL4 ISL9 ISL10	0.1 MM	?
1:1_SPACING	ISL ISL5 ISL6 ISL7 ISL8 I L11	0.101 MM	?

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3 ISL4 ISL9 ISL10	0.053 MM	?
1X_DIELECTRIC	ISL ISL5 ISL6 ISL7 ISL8 I L11	0.101 MM	?

J4 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET TYPE)	SPACING (NET TYPE)		
I68 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	9 33
I69 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	9 33
I66 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	9 33
I67 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	9 33
I68 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	9 33
I69 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	9 33
I66 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	9 33
I70 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	9 33
I72 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	33
I73 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	33
I74 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	33
I75 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	33
I75 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	33
I77 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	33
I76 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	33
I78 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	33
I62 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	9 67
I63 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	9 67
I59 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_C_P	9 67
I60 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_C_N	9 67
I57 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	7 67
I58 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	7 67
I56 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67
I55 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67
I54 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	
I53 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	
I41 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_RC_P	7 36
I42 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_RC_N	7 36
I43 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_F_P	7 38
I44 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_F_N	7 38
I45 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_C_P	7 38
I46 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_C_N	7 38
I47 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
I48 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_N	7 36

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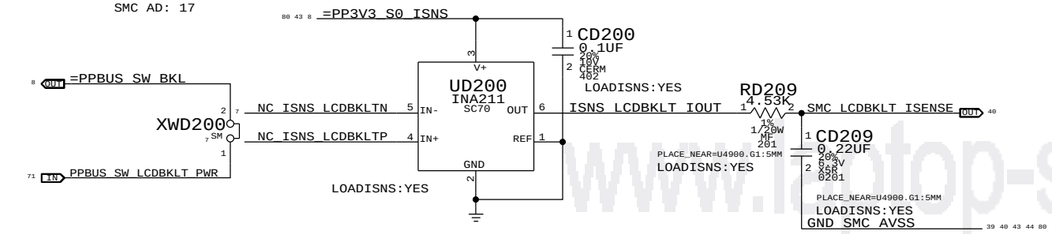
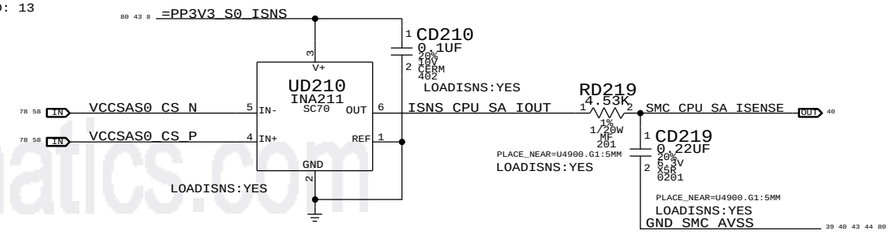
LCD Backlight Current Sense (IBLC)

Gain: 500x. EDP: 0.9 A
Rsense: 0.005 (RD200 / XWD200)
V across Rsense: 4.5 mV
SMC AD: 17



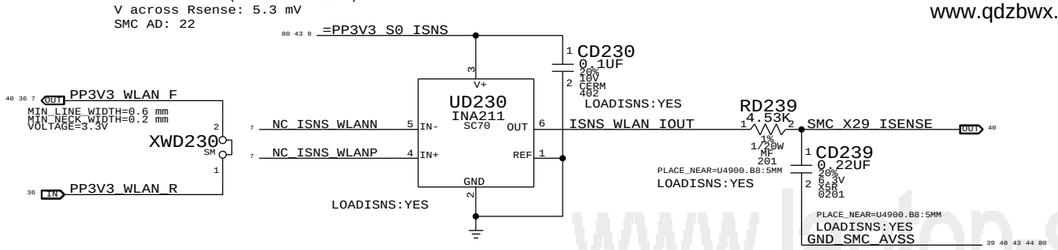
CPU SA Current Sense (IC2C)

Gain: 500x. EDP: 6 A
Rsense: 0.001 (R7140)
V across Rsense: 6 mV
SMC AD: 13



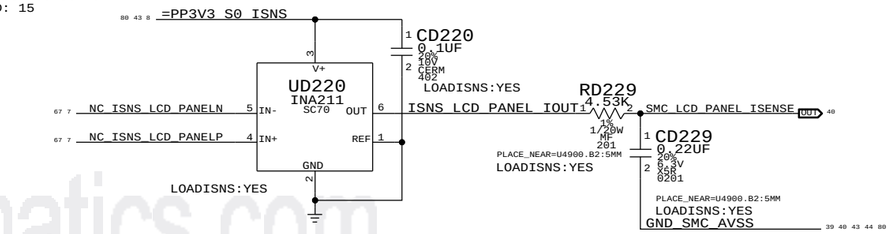
Airport X29 Current Sense (IAPC)

Gain: 500x. EDP: 1.06 A
Rsense: 0.005 (RD230 / XWD230)
V across Rsense: 5.3 mV
SMC AD: 22



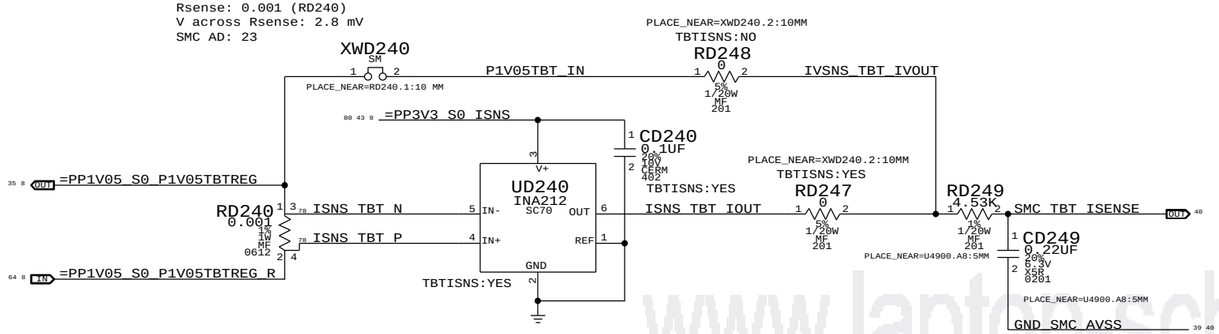
LCD Panel Current Sense (ILDC)

Gain: 500x. EDP: 1 A
Rsense: 0.005 (R9020, XW9020)
V across Rsense: 5 mV
SMC AD: 15



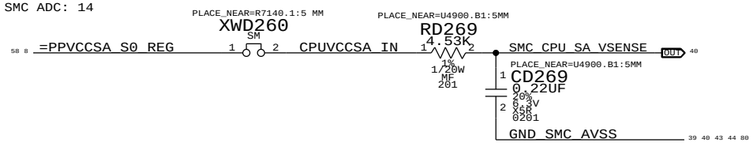
Thunderbolt TBT Current/Voltage Sense (IHSP/VHSP)

Gain: 1000x. EDP: 2.8 A
Rsense: 0.001 (RD240)
V across Rsense: 2.8 mV
SMC AD: 23



CPU SA Voltage Sense (VC2C)

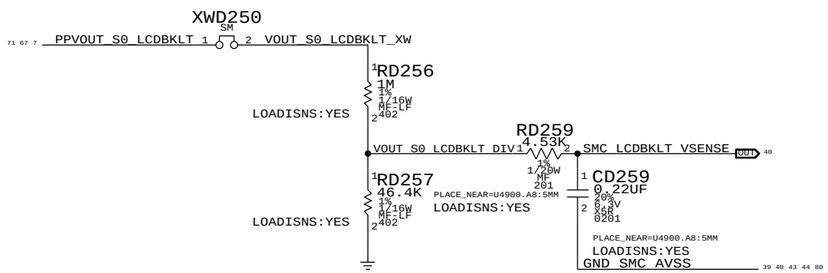
Gain: 1x
SMC ADC: 14



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD209,CD219,CD229		LOADISNS:NO
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD239,CD259		LOADISNS:NO

LCD Backlight Voltage Sense (VBLC)

Gain: 0.04434



SYNC MASTER=D1 SENSORS
SYNC DATE=07/11/2012

PAGE TITLE
Power Sensors: Extended

Apple Inc.

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