1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J41 MLB SCHEMATIC 6.6.0
DVT
4/09/13

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9795	1	SCHEM,MLB,J41	SCH	CRITICAL	
820-3435	1	PCBF,MLB,J41	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Apr 9 19:41:45 2013

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE: <PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 1 OF 120
SHEET: 1 OF 73

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,MLB_MISC,MLB_DEBUG:ENG,MLB_PROGPARTS
MLB_MISC	PP5V5_DCIN:NO,TBTHV:P15V,EDP,CAM_XTAL:NO,CAM_WAKE:NO,APCLKRQ:ISOL,TPAD_INTWAKE:SHARED,USB_PWR:S3,SD_ON_MLB,VCORE_FETS
MLB_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,DDRVREF_DAC,S0PGOOD_ISL,DBGLED,ISNS:ENG
MLB_DEVEL:PVT	XDP_CONN
MLB_DEBUG:ENG	DEVEL_BOM,XDP,LPCPLUS
MLB_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,XDP,LPCPLUS,ISNS:PROD
MLB_DEBUG:PROD	BKLT:PROD,LPCPLUS,XDP,ISNS:PROD

Current Sensor Configuration

BOM GROUP	BOM OPTIONS
ISNS:ENG	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,P1V05_ISNS:YES,AIRPORT_ISNS:YES,SSD_ISNS:YES,LCDBKLT_ISNS:YES,P3V3SS_ISNS:YES,3V3S0_ISNS:YES,OTHER_HS_ISNS:YES,CAM_ISNS:YES,CPUDDR_ISNS:YES,PANEL_ISNS:YES
ISNS:PROD	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,P1V05_ISNS:NO,AIRPORT_ISNS:NO,SSD_ISNS:YES,LCDBKLT_ISNS:NO,P3V3SS_ISNS:NO,3V3S0_ISNS:NO,OTHER_HS_ISNS:NO,CAM_ISNS:NO,CPUDDR_ISNS:NO,PANEL_ISNS:NO

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB
DDR3:MICRON_4GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:MICRON_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	EEPROM,256KBIT,SPI,5MHZ,1.8V,2X3QFN	U2890	CRITICAL	TBTROM:BLANK
341S3802	1	IC,EEPROM,C/R (V23.4) EVT,J41/J41	U2890	CRITICAL	TBTROM:PROG
338S1159	1	IC,SMC12-A3,40MHZ/50DMIPS MCU,9X9,157BGA	U5000	CRITICAL	SMC:BLANK
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_NUM:BLANK
341S3809	1	IC,EFI ROM (V0071) DVT,J41/J43	U6100	CRITICAL	BOOTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4525	1	HSW,SR16M,PRQ,C0,1.3,15W,2+3,1.0,3M,BGA	U0500	CRITICAL	CPU:1.3GHZ
337S4526	1	HSW,SR16L,PRQ,C0,1.4,15W,2+3,1.1,3M,BGA	U0500	CRITICAL	CPU:1.4GHZ
337S4528	1	HSW,SR16H,PRQ,C0,1.7,15W,2+3,1.1,4M,BGA	U0500	CRITICAL	CPU:1.7GHZ
338S1113	1	IC,TBT,CR-4C,B1,PRQ,CIO,288,12X12 FC-CSP	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CAMERA PROCESSOR	U3900	CRITICAL	
607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	J41_MLB
946-3892	1	J11/J13 MLB DYMAX ADHESIVE 29993-SC 0.4G	GLUE	CRITICAL	
825-7670	1	LABEL,TEXT,MLB,K21/K78	LABEL		
376S0964	2	MOSFET,N-CH,25V,30A,9.6M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S1104	2	MOSFET,N-CH,25V,30A,6.1M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN
376S1173	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1174	2	MOSFET,N-CH,30V,22A,6.6M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
900-0090	1		SOLDERPASTE	CRITICAL	

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0677	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0681	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0676	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0680	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0678	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0666	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0679	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:MICRON_4GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1032	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S0586	152S1301		ALL	Dale/Vishay alt to Cyntec
372S0186	372S0185		ALL	NXP alt to Diodes
197S0479	197S0478		ALL	200uW Epson alt to NDK
376S1053	376S0604		ALL	Diodes alt to Fairchild
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0371	128S0376		ALL	Kemet alt to Sanyo
128S0394	128S0415		ALL	NEC alt to Sanyo
152S1821	152S1757		ALL	Cyntec alt to NEC
197S0480	197S0343		ALL	NDK crystal alt to TXC
197S0481	197S0343		ALL	Epson crystal alt to TXC
107S0254	107S0241		ALL	Cyntec sense R alt to TFT
353S3452	353S1286		ALL	Maxim alt to Microchip
128S0386	128S0284		ALL	Kemet alt to Sanyo
128S0397	128S0325		ALL	Kemet alt to Sanyo
377S0155	377S0104		ALL	OnSemi alt to Infineon
128S0398	128S0220		ALL	Kemet alt to Sanyo
197S0542	197S0544		ALL	NDK alt to TXC
197S0545	197S0544		ALL	Epson alt to TXC
138S0681	138S0638		ALL	Taiyo alt to Samsung
138S0841	138S0638		ALL	Murata alt to Samsung
376S1180	376S0761		ALL	Renesas alt to Vishay
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cyntec alt to TFT
107S0250	107S0248		ALL	Cyntec alt to TFT

SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-4118	PCBA,MLB,BEST,HY 4GB,J41:	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_4GB
639-4274	PCBA,MLB,BEST,HY 8GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_8GB
639-4275	PCBA,MLB,BEST,EL 4GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_4GB
639-4276	PCBA,MLB,BEST,EL 8GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_8GB
639-4702	PCBA,MLB,BEST,MI 4GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:MICRON_4GB
639-4434	PCBA,MLB,BETTER,HY 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_4GB
639-4435	PCBA,MLB,BETTER,HY 8GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_8GB
639-4436	PCBA,MLB,BETTER,EL 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_4GB
639-4437	PCBA,MLB,BETTER,EL 8GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_8GB
639-4703	PCBA,MLB,BETTER,MI 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:MICRON_4GB
685-0024	CMN PTS,PCBA,MLB,J41	MLB_COMMON,J41_MLB
985-0017	J41 MLB DEVELOPMENT BOM	MLB_DEVEL:ENG
685-0062	VCORE FET,REN,J41	VCORE_FET:REN
685-0063	VCORE FET,VSHY,J41	VCORE_FET:VSHY

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,SMC:PROG,TBTROM:PROG

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S3757	1	IC,SMC-A3 SCPL,EXT,V22.12A18,PROTO 1,J41	U5000	CRITICAL	SMC:PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-0062	685-0063		ALL	Renesas alt to Vishay
333S0704	333S0700		ALL	Elpida CAM DRAM alt to Hynix

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
985-0017	1	J41 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
685-0024	1	CMN PTS,PCBA,MLB,J41	CMNPTS	CRITICAL	MLB_CMNPTS
685-0063	1	VCORE FET,VSHY,J41	VCOREFETS	CRITICAL	VCORE_FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: BOM Variants

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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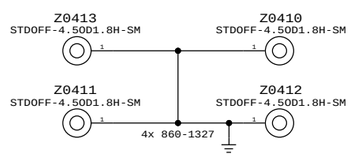
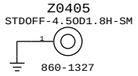
PD Module Parts

806-5107	1	CAN,TOPSIDE,ALT,J41/J43	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-5108	1	CAN,TOPSIDE,COVER,ALT,J41/J43	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3142	1	CAN,TBT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,TBT,J11/J13	TBTCOVER	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
725-1792	1	INSULATOR,CPU,J41/J43	CPU_INSULATOR	CRITICAL	

CPU Heat Sink Mounting Bosses

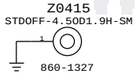


Fan Boss



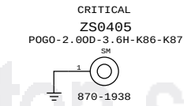
X21 Boss

SSD Boss

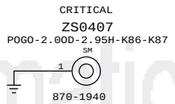


EMI I/O Pogo Pins

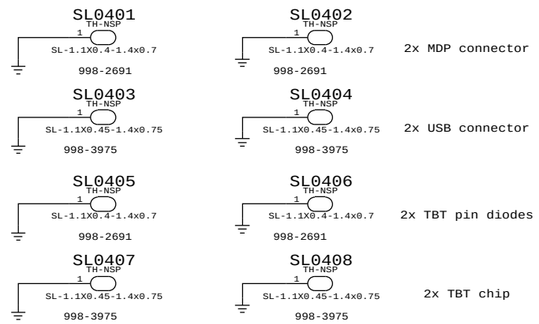
DisplayPort Pogo



USB/SD Card Pogo



Can Slots



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PAGE TITLE: PD Parts

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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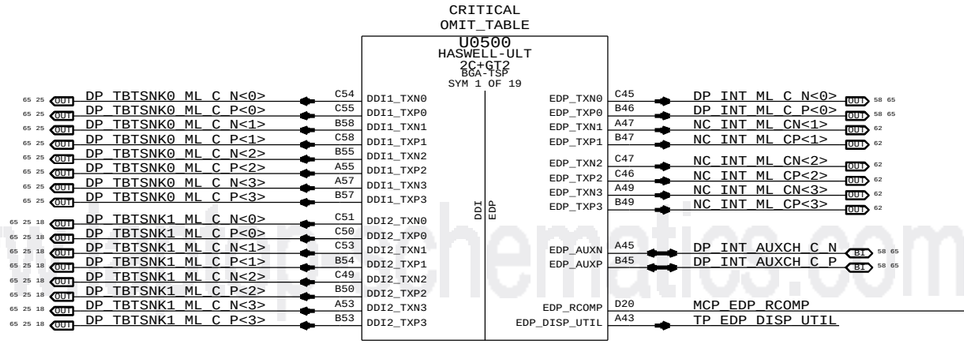
DDI Port Assignments:

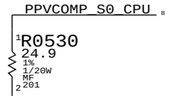
TBT Sink 0

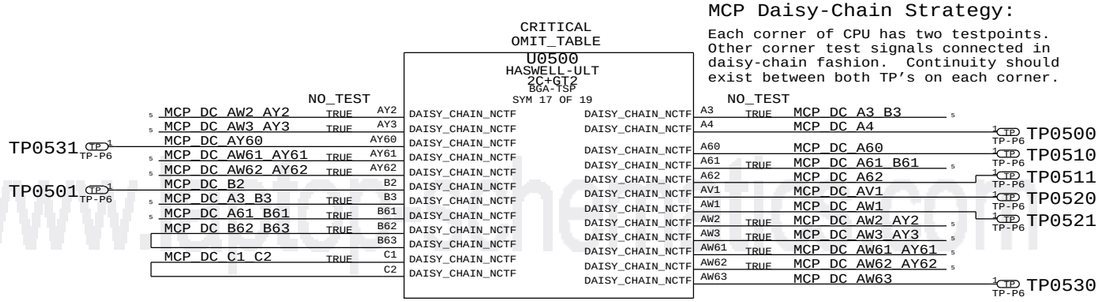
TBT Sink 1
(MUXed with HDMI
 if necessary)



eDP Port Assignment:

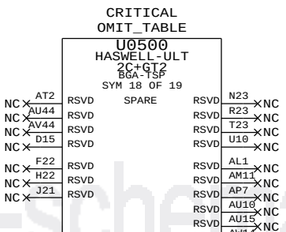
Internal panel





MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.



SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE: CPU GFX/NCTF/RSVD

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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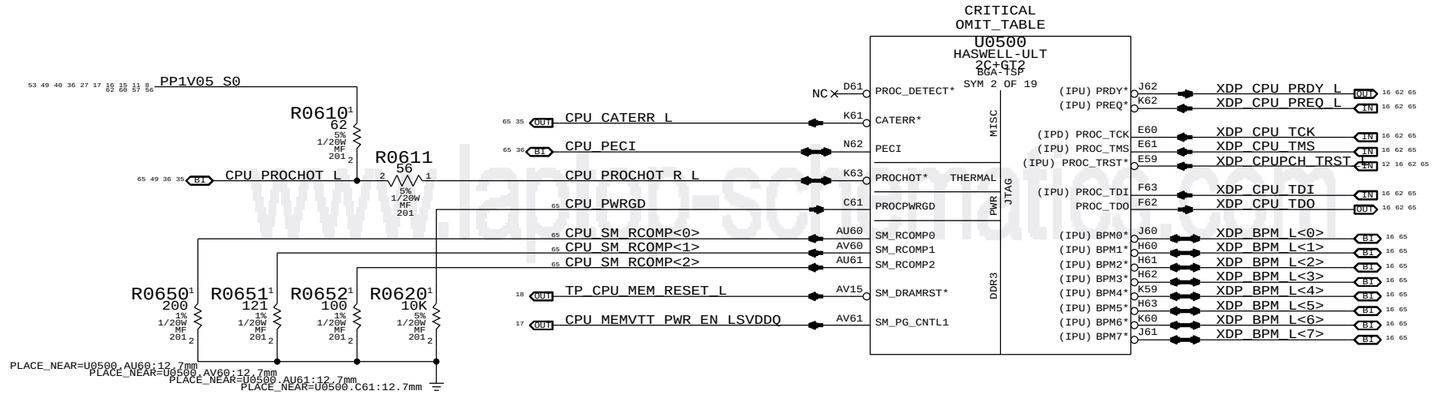
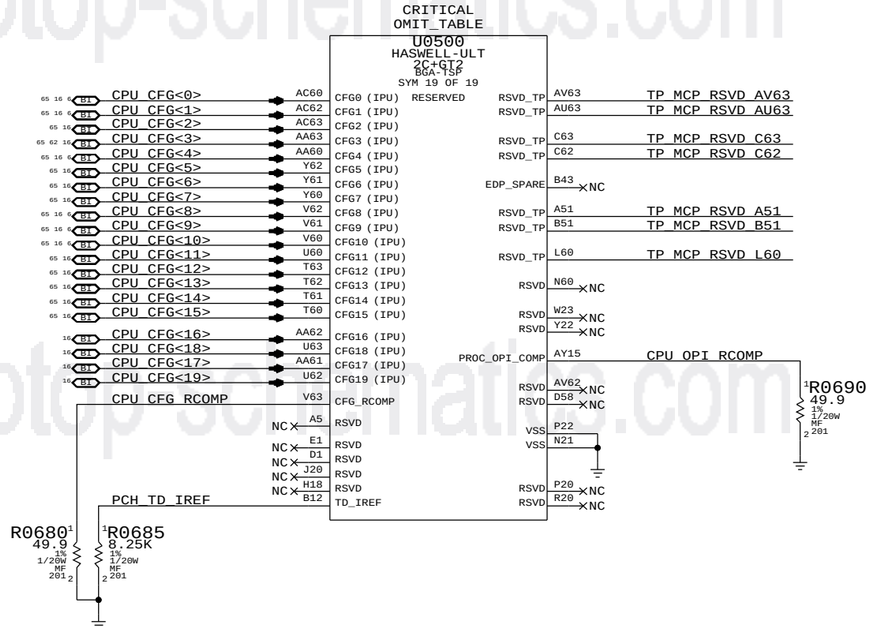
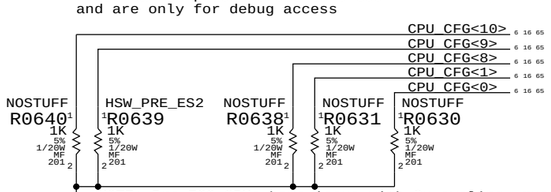


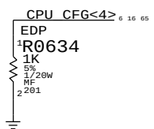


CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE: CPU Misc/JTAG/CFG/RSVD

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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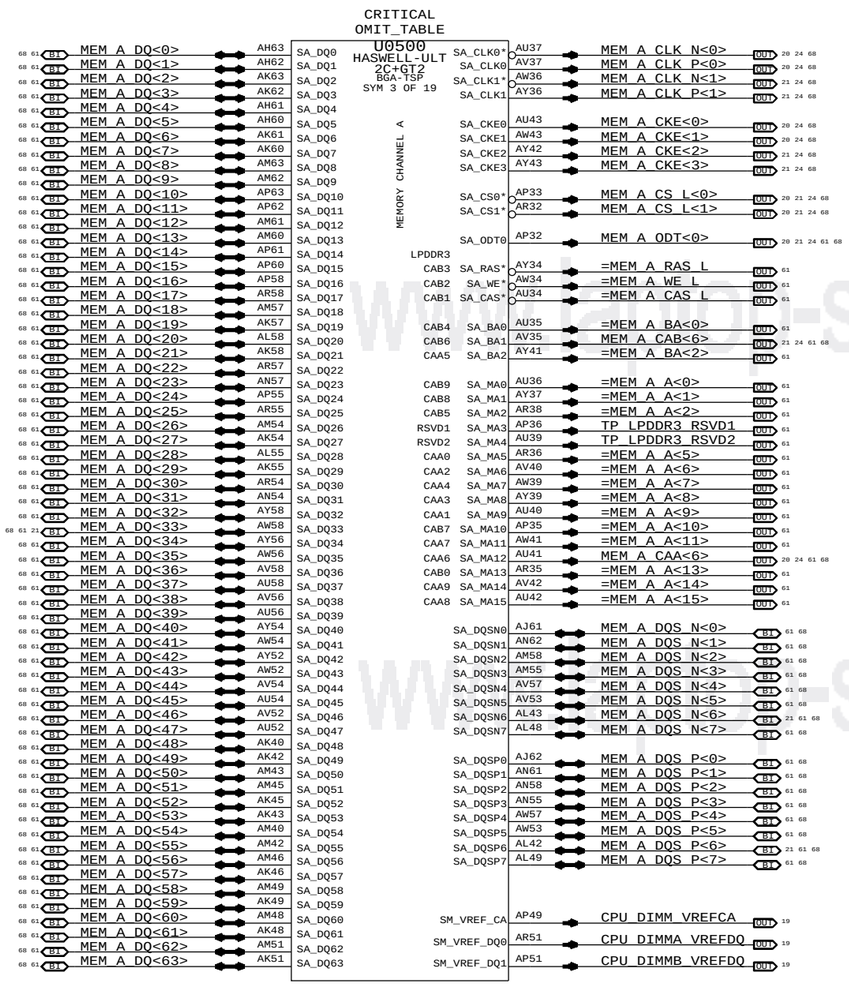

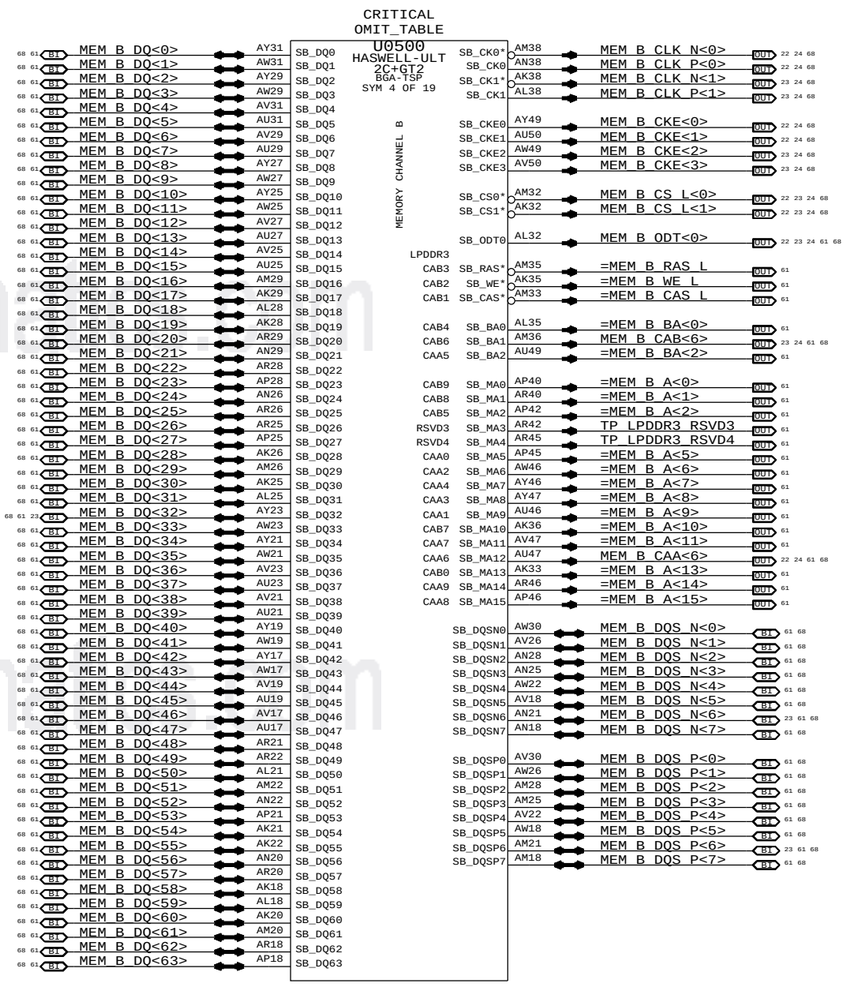

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE
CPU DDR3/LPDDR3 Interfaces

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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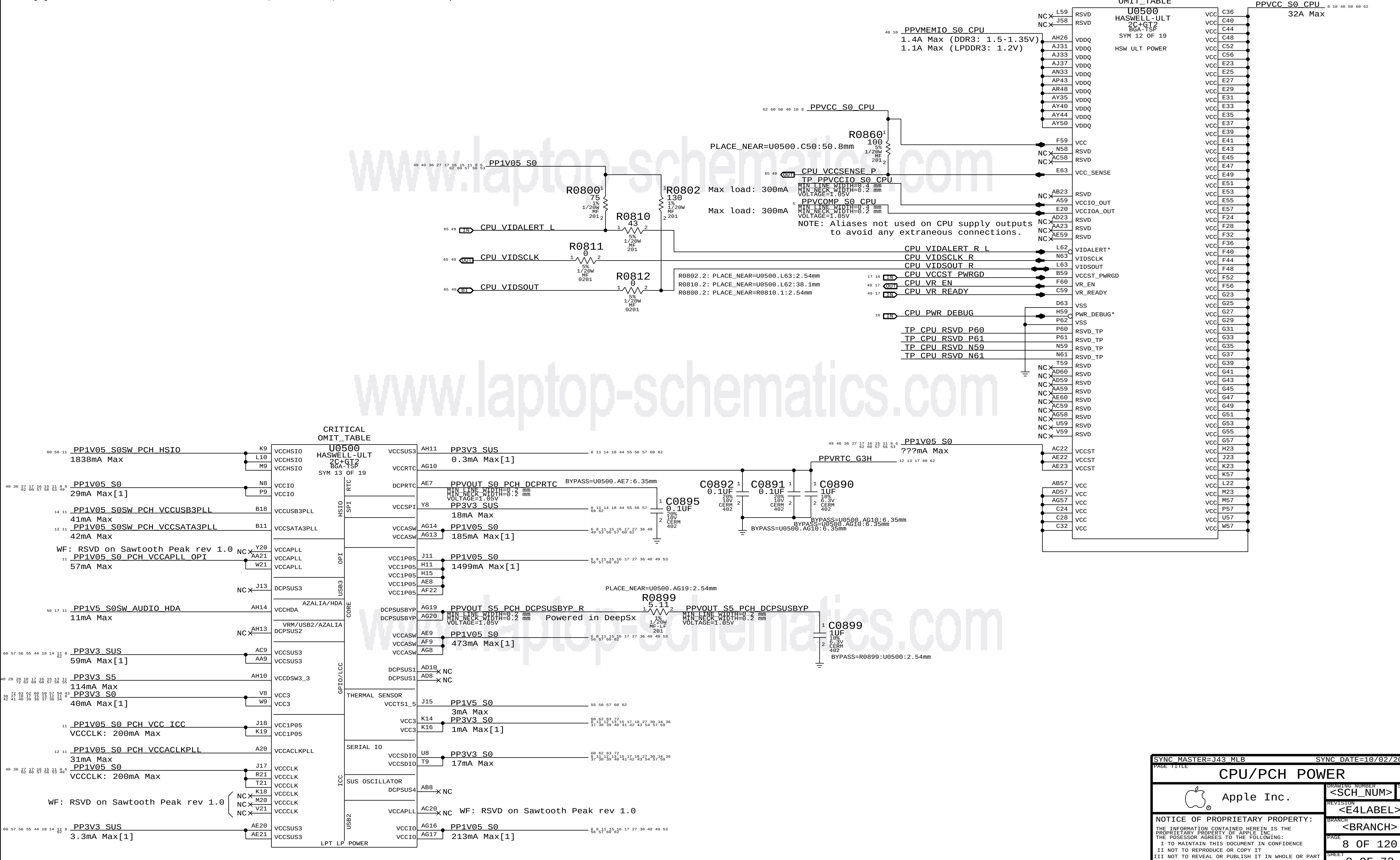
HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 12 OF 19
HSW ULT POWER
PPVCC_S0_CPU
32A Max
PPVMEMIO_S0_CPU
1.4A Max (DDR3: 1.5-1.35V)
1.1A Max (LPDDR3: 1.2V)
PPVCC_S0_CPU
R0860
100
PLACE_NEAR=U0500.C50:50.8mm
PP1V05_S0
R0800
75
R0802
130
Max load: 300mA
Max load: 300mA
CPU_VCCSENSE_P
TP_PPVCCIO_S0_CPU
PPVCOMP_S0_CPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.
R0810
43
CPU_VIDALERT_L
CPU_VIDSCLK
R0811
0
CPU_VIDSOUT
R0812
0
R0802.2: PLACE_NEAR=U0500.L63:2.54mm
R0810.2: PLACE_NEAR=U0500.L62:38.1mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_VCCST_PWRGD
CPU_VR_EN
CPU_VR_READY
CPU_PWR_DEBUG
TP_CPU_RSVD_P60
TP_CPU_RSVD_P61
TP_CPU_RSVD_N59
TP_CPU_RSVD_N61
PP1V05_S0
???mA Max
PPVRTC_G3H
C0892
0.1UF
C0891
0.1UF
C0890
1UF
C0895
0.1UF
BYPASS=U0500.AG10:6.35mm
BYPASS=U0500.AE7:6.35mm
CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 13 OF 19
LPT LP POWER
PP1V05_S0SW_PCH_HSIO
1838mA Max
PP1V05_S0
29mA Max[1]
PP1V05_S0SW_PCH_VCCUSB3PLL
41mA Max
PP1V05_S0SW_PCH_VCCSATA3PLL
42mA Max
WF: RSVD on Sawtooth Peak rev 1.0
PP1V05_S0_PCH_VCCAPLL_OPI
57mA Max
PP1V5_S0SW_AUDIO_HDA
11mA Max
PP3V3_SUS
59mA Max[1]
PP3V3_S5
114mA Max
PP3V3_S0
40mA Max[1]
PP1V05_S0_PCH_VCC_ICC
VCCCLK: 200mA Max
PP1V05_S0_PCH_VCCACLKPLL
31mA Max
PP1V05_S0
VCCCLK: 200mA Max
WF: RSVD on Sawtooth Peak rev 1.0
PP3V3_SUS
3.3mA Max[1]
PP3V3_SUS
0.3mA Max[1]
PPVOUT_S0_PCH_DCPRTC
PP3V3_SUS
18mA Max
PP1V05_S0
185mA Max[1]
PP1V05_S0
1499mA Max[1]
PLACE_NEAR=U0500.AG19:2.54mm
R0899
5.11
PPVOUT_S5_PCH_DCPSUSBYP_R
Powered in DeepSx
PPVOUT_S5_PCH_DCPSUSBYP
C0899
1UF
BYPASS=R0899:U0500:2.54mm
PP1V05_S0
473mA Max[1]
PP1V5_S0
3mA Max
PP3V3_S0
1mA Max[1]
PP3V3_S0
17mA Max
WF: RSVD on Sawtooth Peak rev 1.0
PP1V05_S0
213mA Max[1]

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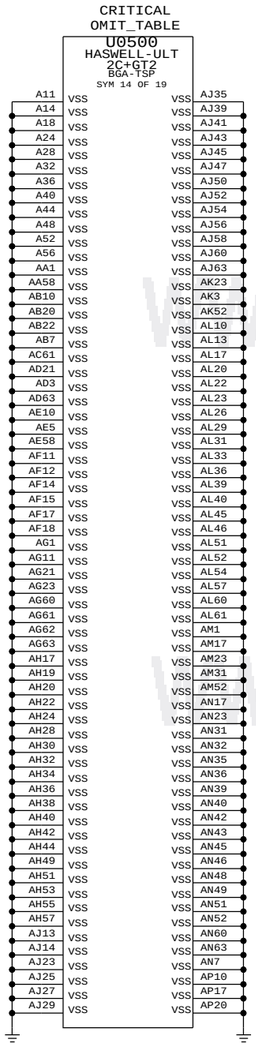

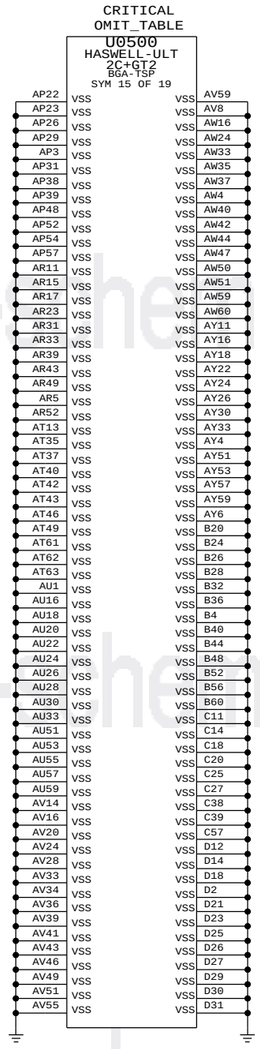

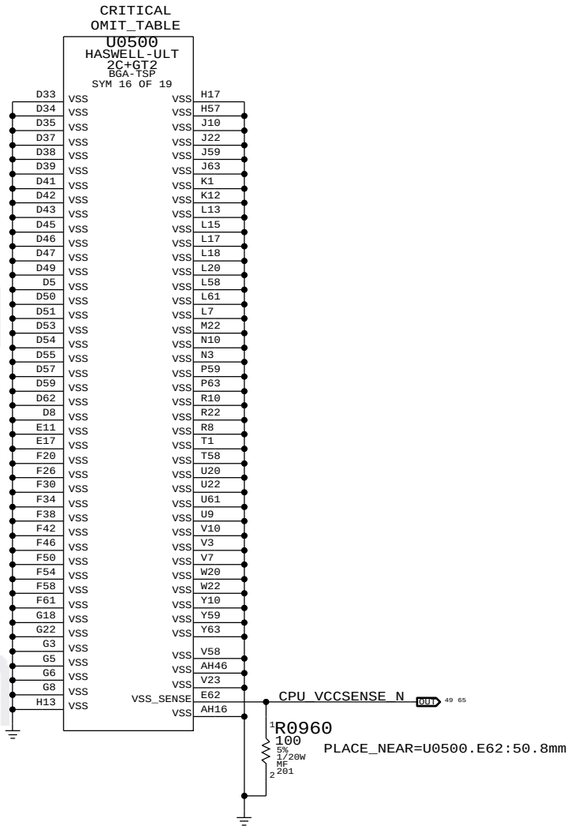

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All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 1.0 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 10uF 0402 mirrored stuff, 1x 470uF stuff, 50x 10uF mirrored no stuff, 50x 10uF single sided no stuff

62 60 50 40 8 PPVCC_S0_CPU

NO STUFF C1000 10UF 20% 4V X6S 0402 | NO STUFF C1001 10UF 20% 4V X6S 0402 | NO STUFF C1002 10UF 20% 4V X6S 0402 | NO STUFF C1003 10UF 20% 4V X6S 0402 | NO STUFF C1004 10UF 20% 4V X6S 0402 | NO STUFF C1005 10UF 20% 4V X6S 0402 | NO STUFF C1006 10UF 20% 4V X6S 0402 | NO STUFF C1007 10UF 20% 4V X6S 0402 | NO STUFF C1008 10UF 20% 4V X6S 0402 | NO STUFF C1009 10UF 20% 4V X6S 0402 | NO STUFF C1010 10UF 20% 4V X6S 0402 | NO STUFF C1011 10UF 20% 4V X6S 0402 | NO STUFF C1012 10UF 20% 4V X6S 0402 | NO STUFF C1013 10UF 20% 4V X6S 0402 | NO STUFF C1014 10UF 20% 4V X6S 0402 | NO STUFF C105A 10UF 20% 4V X6S 0402 | CRITICAL C105B 10UF 20% 4V X6S 0402 | CRITICAL C105C 10UF 20% 4V X6S 0402 | NO STUFF C105D 10UF 20% 4V X6S 0402 | NO STUFF C105E 10UF 20% 4V X6S 0402 | CRITICAL C105F 10UF 20% 4V X6S 0402

NO STUFF C1015 10UF 20% 4V X6S 0402 | NO STUFF C1016 10UF 20% 4V X6S 0402 | NO STUFF C1017 10UF 20% 4V X6S 0402 | NO STUFF C1018 10UF 20% 4V X6S 0402 | NO STUFF C1019 10UF 20% 4V X6S 0402 | NO STUFF C1020 10UF 20% 4V X6S 0402 | NO STUFF C1021 10UF 20% 4V X6S 0402 | NO STUFF C1030 10UF 20% 4V X6S 0402 | NO STUFF C104A 10UF 20% 4V X6S 0402 | NO STUFF C104B 10UF 20% 4V X6S 0402 | NO STUFF C104C 10UF 20% 4V X6S 0402 | CRITICAL C104D 10UF 20% 4V X6S 0402 | NO STUFF C104E 10UF 20% 4V X6S 0402 | CRITICAL C104F 10UF 20% 4V X6S 0402 | CRITICAL C106A 10UF 20% 4V X6S 0402 | NO STUFF C106B 10UF 20% 4V X6S 0402 | NO STUFF C106C 10UF 20% 4V X6S 0402 | NO STUFF C106D 10UF 20% 4V X6S 0402 | NO STUFF C106E 10UF 20% 4V X6S 0402

CRITICAL C1070 10UF 20% 4V X6S 0402 | CRITICAL C1071 10UF 20% 4V X6S 0402 | NO STUFF C1072 10UF 20% 4V X6S 0402 | NO STUFF C1073 10UF 20% 4V X6S 0402 | NO STUFF C1074 10UF 20% 4V X6S 0402 | NO STUFF C1075 10UF 20% 4V X6S 0402 | CRITICAL C1076 10UF 20% 4V X6S 0402 | CRITICAL C1077 10UF 20% 4V X6S 0402 | NO STUFF C1078 10UF 20% 4V X6S 0402 | NO STUFF C1079 10UF 20% 4V X6S 0402 | NO STUFF C1080 10UF 20% 4V X6S 0402 | NO STUFF C1081 10UF 20% 4V X6S 0402 | NO STUFF C1082 10UF 20% 4V X6S 0402 | CRITICAL C1083 10UF 20% 4V X6S 0402 | CRITICAL C1084 10UF 20% 4V X6S 0402

CRITICAL C1085 10UF 20% 4V X6S 0402 | CRITICAL C1086 10UF 20% 4V X6S 0402 | CRITICAL C1087 10UF 20% 4V X6S 0402 | NO STUFF C1088 10UF 20% 4V X6S 0402 | NO STUFF C1089 10UF 20% 4V X6S 0402 | NO STUFF C1090 10UF 20% 4V X6S 0402 | CRITICAL C1091 10UF 20% 4V X6S 0402 | CRITICAL C1092 10UF 20% 4V X6S 0402 | NO STUFF C1093 10UF 20% 4V X6S 0402 | NO STUFF C1094 10UF 20% 4V X6S 0402 | NO STUFF C1095 10UF 20% 4V X6S 0402 | NO STUFF C1096 10UF 20% 4V X6S 0402 | CRITICAL C1097 10UF 20% 4V X6S 0402

NO STUFF C1022 10UF 20% 4V X6S 0402 | NO STUFF C1023 10UF 20% 4V X6S 0402 | NO STUFF C1024 10UF 20% 4V X6S 0402 | NO STUFF C1025 10UF 20% 4V X6S 0402 | NO STUFF C1026 10UF 20% 4V X6S 0402 | NO STUFF C1027 10UF 20% 4V X6S 0402 | NO STUFF C1028 10UF 20% 4V X6S 0402 | NO STUFF C1029 10UF 20% 4V X6S 0402 | NO STUFF C1032 10UF 20% 4V X6S 0402 | NO STUFF C1033 10UF 20% 4V X6S 0402 | NO STUFF C1034 10UF 20% 4V X6S 0402 | NO STUFF C1035 10UF 20% 4V X6S 0402 | NO STUFF C1036 10UF 20% 4V X6S 0402 | NO STUFF C1037 10UF 20% 4V X6S 0402 | NO STUFF C1038 10UF 20% 4V X6S 0402

NO STUFF C1039 10UF 20% 4V X6S 0402 | NO STUFF C1044 10UF 20% 4V X6S 0402 | NO STUFF C1045 10UF 20% 4V X6S 0402 | NO STUFF C1046 10UF 20% 4V X6S 0402 | NO STUFF C1047 10UF 20% 4V X6S 0402 | NO STUFF C1048 10UF 20% 4V X6S 0402 | NO STUFF C1049 10UF 20% 4V X6S 0402

NO STUFF C1056 10UF 20% 4V X6S 0402 | NO STUFF C1057 10UF 20% 4V X6S 0402 | NO STUFF C1058 10UF 20% 4V X6S 0402 | NO STUFF C1059 10UF 20% 4V X6S 0402 | NO STUFF C1062 10UF 20% 4V X6S 0402 | NO STUFF C1063 10UF 20% 4V X6S 0402 | NO STUFF C1064 10UF 20% 4V X6S 0402 | NO STUFF C1065 10UF 20% 4V X6S 0402 | NO STUFF C1066 10UF 20% 4V X6S 0402 | NO STUFF C1067 10UF 20% 4V X6S 0402 | NO STUFF C1068 10UF 20% 4V X6S 0402 | NO STUFF C1069 10UF 20% 4V X6S 0402 | NO STUFF C1098 10UF 20% 4V X6S 0402 | NO STUFF C1099 10UF 20% 4V X6S 0402 | NO STUFF C109A 10UF 20% 4V X6S 0402

NO STUFF C109B 10UF 20% 4V X6S 0402 | NO STUFF C109C 10UF 20% 4V X6S 0402 | NO STUFF C109D 10UF 20% 4V X6S 0402 | NO STUFF C109E 10UF 20% 4V X6S 0402 | NO STUFF C109F 10UF 20% 4V X6S 0402 | NO STUFF C108A 10UF 20% 4V X6S 0402 | NO STUFF C108B 10UF 20% 4V X6S 0402 | NO STUFF C108C 10UF 20% 4V X6S 0402 | NO STUFF C108D 10UF 20% 4V X6S 0402 | NO STUFF C108E 10UF 20% 4V X6S 0402 | NO STUFF C108F 10UF 20% 4V X6S 0402 | NO STUFF C107A 10UF 20% 4V X6S 0402 | NO STUFF C107B 10UF 20% 4V X6S 0402

CRITICAL C1031 470UF-0.0045OHM 20% 2.5V POLY-TANT SM

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 4x 2.2uF 0402, 6x 10uF 0402, 2x 270uF B2 no stuff

40 8 PPVMEMIO_S0_CPU

C1040 2.2UF 20% 6.3V CERM 402-LF | C1041 2.2UF 20% 6.3V CERM 402-LF | C1042 2.2UF 20% 6.3V CERM 402-LF | C1043 2.2UF 20% 6.3V CERM 402-LF

C1050 10UF 20% 6.3V CERM-X5R 0402-1 | C1051 10UF 20% 6.3V CERM-X5R 0402-1 | C1052 10UF 20% 6.3V CERM-X5R 0402-1 | C1053 10UF 20% 6.3V CERM-X5R 0402-1 | C1054 10UF 20% 6.3V CERM-X5R 0402-1 | C1055 10UF 20% 6.3V CERM-X5R 0402-1

C1060 270UF 20% 2V TANT CASE-B2-SM | NO STUFF C1061 270UF 20% 2V TANT CASE-B2-SM

2x Bulk nostuff per Harris Beach v1.0 schematic

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Apple Inc.

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
NO STUFF
C1200 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH10:6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS
NO STUFF
C1202 0.1UF 20% 25V CERM 402
BYPASS=U0500.Y8:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS
C1204 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.AC9:12.7mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS
C1206 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH11:6.35mm

PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
PP3V3_S0
C1208 1UF 10% 6.3V CERM 402
BYPASS=U0500.U8:6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0SW_AUDIO_HDA
C1210 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH14:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0
C1212 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.V8:12.7mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0
C1214 0.1UF 20% 25V CERM 402
BYPASS=U0500.K14:6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
NO STUFF
C1250 22UF 20% 6.3V X5R-CERM-1 603
C1251 1UF 10% 6.3V CERM 402
BYPASS=U0500.AE9:12.7mm
BYPASS=U0500.AE9:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0
C1264 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG16:6.35mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C1255 10UF 20% 6.3V X5R 603
C1256 1UF 10% 6.3V CERM 402
C1257 1UF 10% 6.3V CERM 402
BYPASS=U0500.J11:12.7mm
BYPASS=U0500.J11:6.35mm
BYPASS=U0500.AE8:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
PP1V05_S0
C1266 1UF 10% 6.3V CERM 402
C1267 1UF 10% 6.3V CERM 402
BYPASS=U0500.J17:6.35mm
BYPASS=U0500.R21:6.35mm

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
PP1V05_S0SW_PCH_HSIO
C1260 1UF 10% 6.3V CERM 402
C1261 1UF 10% 6.3V CERM 402
C1262 10UF 20% 6.3V CERM-X5R 0402-1
BYPASS=U0500.K9:6.35mm
BYPASS=U0500.L10:6.35mm
BYPASS=U0500.M9:6.35mm

PP1V05_S0
??mA Max
R1270 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603

PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max

C1270 47UF 20% 4V CERM-X5R 0805-1
C1271 47UF 20% 4V CERM-X5R 0805-1
C1272 1UF 10% 10V X5R 402
BYPASS=U0500.A20:12.7mm
BYPASS=U0500.A20:12.7mm
BYPASS=U0500.A20:6.35mm

R1275 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603

PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max

C1275 47UF 20% 4V CERM-X5R 0805-1
C1276 47UF 20% 4V CERM-X5R 0805-1
C1277 1UF 10% 10V X5R 402
BYPASS=U0500.J18:12.7mm
BYPASS=U0500.J18:12.7mm
BYPASS=U0500.J18:6.35mm

R1280 0 5% 1/16W MF-LF 402

CRITICAL
NO STUFF
L1280 2.2UH-240MA-0.221OHM 0603

PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max

NO STUFF C1280 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1281 47UF 20% 4V CERM-X5R 0805-1
C1282 1UF 10% 10V X5R 402
BYPASS=U0500.AA21:12.7mm
BYPASS=U0500.AA21:12.7mm
BYPASS=U0500.AA21:6.35mm

PP1V05_S0SW_PCH_HSIO
83mA Max

CRITICAL
L1290 2.2UH-240MA-0.221OHM 0603

PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max

NO STUFF C1290 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1291 47UF 20% 4V CERM-X5R 0805-1
C1292 1UF 10% 10V X5R 402
BYPASS=U0500.B11:12.7mm
BYPASS=U0500.B11:12.7mm
BYPASS=U0500.B11:6.35mm

CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603

PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max

NO STUFF C1295 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1296 47UF 20% 4V CERM-X5R 0805-1
C1297 1UF 10% 10V X5R 402
BYPASS=U0500.B18:12.7mm
BYPASS=U0500.B18:12.7mm
BYPASS=U0500.B18:6.35mm

LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

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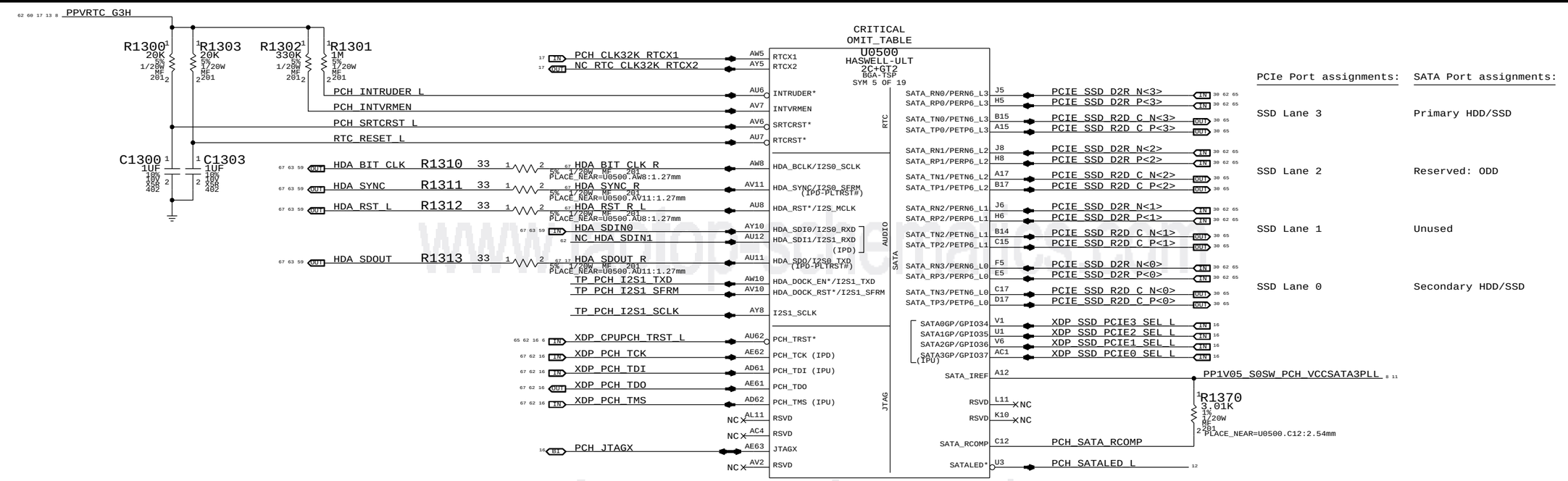

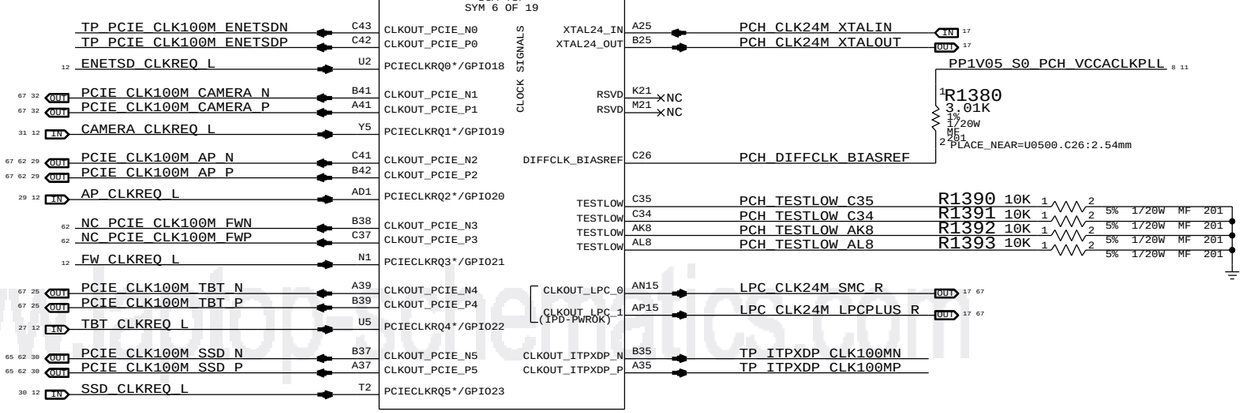

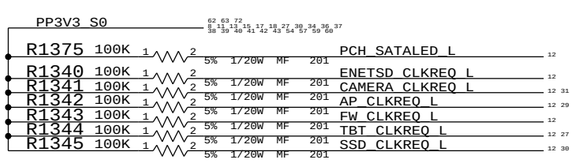

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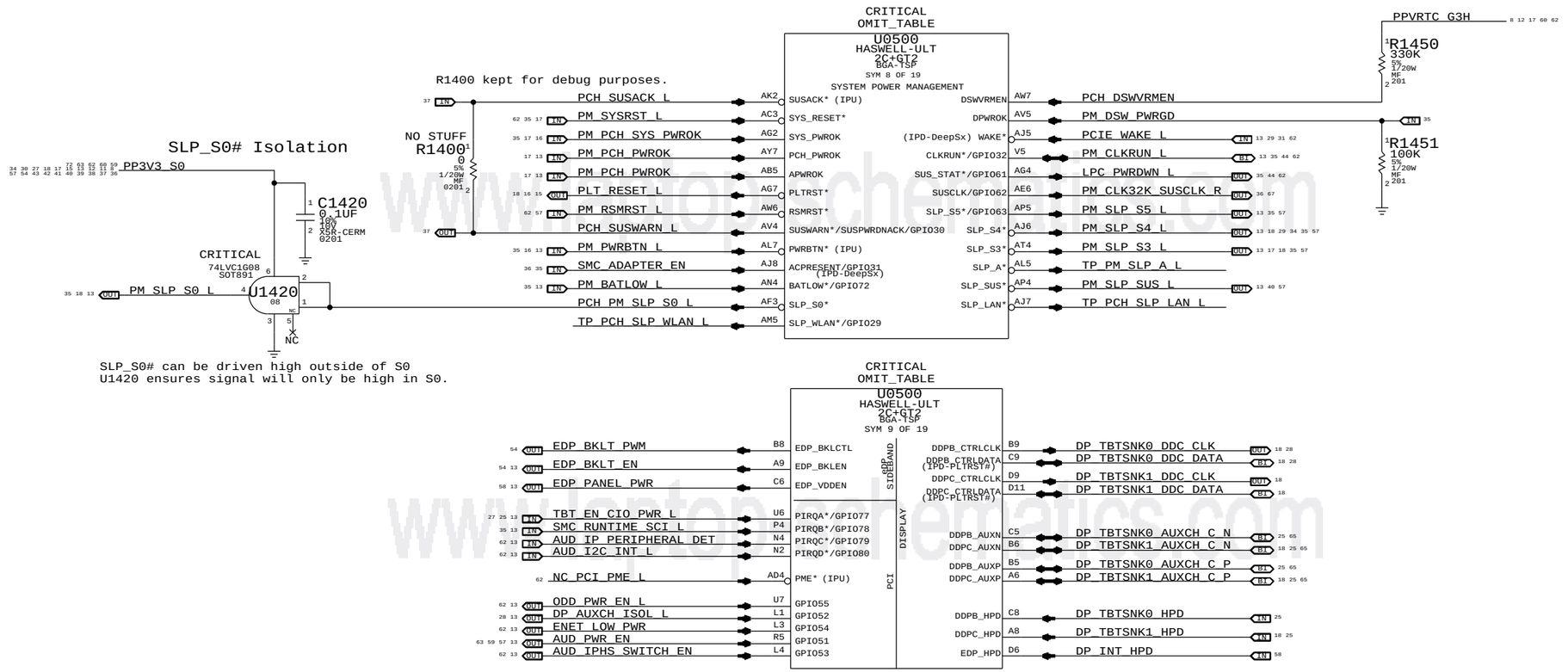

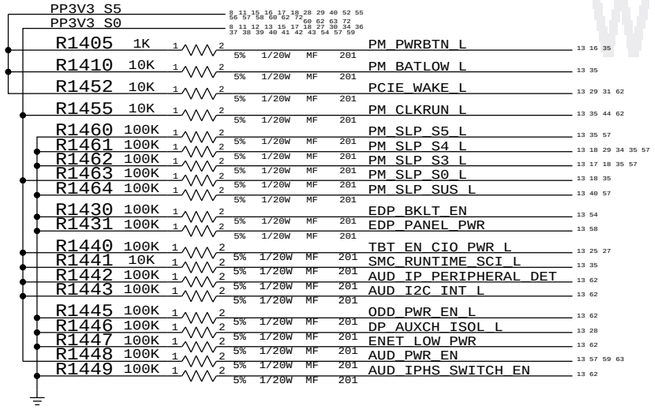

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PCIe Port Assignments:

Thunderbolt lane 0

Thunderbolt lane 1

Thunderbolt lane 2

Thunderbolt lane 3

AirPort

Reserved: FireWire

SD Card Reader
(& Ethernet if combo)

Camera

CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 11 OF 19

PCIE_TBT_D2R_N<0> F10 PERN5_L0
PCIE_TBT_D2R_P<0> E10 PERP5_L0
PCIE_TBT_R2D_C_N<0> C23 PETN5_L0
PCIE_TBT_R2D_C_P<0> C22 PETP5_L0
PCIE_TBT_D2R_N<1> F8 PERN5_L1
PCIE_TBT_D2R_P<1> E8 PERP5_L1
PCIE_TBT_R2D_C_N<1> B23 PETN5_L1
PCIE_TBT_R2D_C_P<1> A23 PETP5_L1
PCIE_TBT_D2R_N<2> H10 PERN5_L2
PCIE_TBT_D2R_P<2> G10 PERP5_L2
PCIE_TBT_R2D_C_N<2> B21 PETN5_L2
PCIE_TBT_R2D_C_P<2> C21 PETP5_L2
PCIE_TBT_D2R_N<3> E6 PERN5_L3
PCIE_TBT_D2R_P<3> F6 PERP5_L3
PCIE_TBT_R2D_C_N<3> B22 PETN5_L3
PCIE_TBT_R2D_C_P<3> A21 PETP5_L3
PCIE_AP_D2R_N G11 PERN3
PCIE_AP_D2R_P F11 PERP3
PCIE_AP_R2D_C_N C29 PETN3
PCIE_AP_R2D_C_P B30 PETP3
NC_PCIE_FW_D2RN F13 PERN4
NC_PCIE_FW_D2RP G13 PERP4
NC_PCIE_FW_R2D_CN B29 PETN4
NC_PCIE_FW_R2D_CP A29 PETP4
NC_USB3RPCIE_SD_D2RN G17 PERN1/USB3RN2
NC_USB3RPCIE_SD_D2RP F17 PERP1/USB3RP2
NC_USB3RPCIE_SD_R2D_CN C30 PETN1/USB3TN2
NC_USB3RPCIE_SD_R2D_CP C31 PETP1/USB3TP2
PCIE_CAMERA_D2R_N F15 PERN2/USB3RN3
PCIE_CAMERA_D2R_P G15 PERP2/USB3RP3
PCIE_CAMERA_R2D_C_N B31 PETN2/USB3TN3
PCIE_CAMERA_R2D_C_P A31 PETP2/USB3TP3
NC E15 RSVD
NC E13 RSVD
PCIE_RCOMP A27
PCIE_IREF B27

PCI-E
USB

USB2N0 AN8 USB_EXTA_N
USB2P0 AM8 USB_EXTA_P
USB2N1 AR7 USB_EXTB_N
USB2P1 AT7 USB_EXTB_P
USB2N2 AR8 USB_BT_N
USB2P2 AP8 USB_BT_P
USB2N3 AR10 NC_USB_IRN
USB2P3 AT10 NC_USB_IRP
USB2N4 AM15 USB_TPAD_N
USB2P4 AL15 USB_TPAD_P
USB2N5 AM13 TP_USB_5N
USB2P5 AN13 TP_USB_5P
USB2N6 AP11 NC_USB_CAMERAN
USB2P6 AN11 NC_USB_CAMERAP
USB2N7 AR13 NC_USB_SDN
USB2P7 AP13 NC_USB_SDP
(IPD)

USB3RN0 G20 USB3_EXTA_D2R_N
USB3RP0 H20 USB3_EXTA_D2R_P
USB3TN0 C33 USB3_EXTA_R2D_C_N
USB3TP0 B34 USB3_EXTA_R2D_C_P
USB3RN1 E18 USB3_EXTB_D2R_N
USB3RP1 F18 USB3_EXTB_D2R_P
USB3TN1 B33 USB3_EXTB_R2D_C_N
USB3TP1 A33 USB3_EXTB_R2D_C_P

USBRBIAS* AJ10 PCH_USB_RBIAS
USBRBIAS AJ11
PLACE_NEAR=U0500.AJ10:2.54mm
R1570 22.6 1% 1/20W MF 201

RSVD AN10 NC
RSVD AM10 NC

OC0*/GPIO40 AL3 XDP_USB_EXTA_OC_L
OC1*/GPIO41 AT1 XDP_USB_EXTB_OC_L
OC2*/GPIO42 AH2 XDP_USB_EXTC_OC_L
OC3*/GPIO43 AV3 XDP_USB_EXTD_OC_L

PP1V05_S0SW_PCH_VCCUSB3PLL
R1500 3.01K 1% 1/20W MF 201
PLACE_NEAR=U0500.A27:2.54mm
PCH_PCIE_RCOMP

USB Port Assignments:

Ext A (LS/FS/HS)

Ext B (LS/FS/HS)

BT

IR

Trackpad

Unused

Reserved: Camera

Reserved: SD (HS)

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 7 OF 19

LPC_AD<0> R1540 33 LPC_AD_R<0>
LPC_AD<1> R1541 33 LPC_AD_R<1>
LPC_AD<2> R1542 33 LPC_AD_R<2>
LPC_AD<3> R1543 33 LPC_AD_R<3>
LPC_FRAME_L R1544 33 LPC_FRAME_R_L
5% 1/20W MF 201

(IPU)
LAD0 AU14
LAD1 AW12
LAD2 AY12
LAD3 AW11
LFRAME* AV12

LPC
SMBUS

SPI_CLK_R AA3
SPI_CS0_R_L Y7
TP_SPI_CS1_L Y4
TP_SPI_CS2_L AC2
SPI_MOSI_R AA2
SPI_MISO AA4
SPI_IO<2> Y6
SPI_IO<3> AF1

SPI_CLK (IPU)
SPI_CS0* (IPU)
SPI_CS1* (IPU)
SPI_CS2* (IPU)
SPI_MOSI (IPU/IPD)
SPI_MISO (IPU)
SPI_IO2 (IPU)
SPI_IO3 (IPU)

SPI

C-LINK

SMBALERT*/GPIO11 AN2 PCH_SMBALERT_L
SMBCLK AP2 SMBUS_PCH_CLK
SMBDATA AH1 SMBUS_PCH_DATA
SML0ALERT*/GPIO60 AL2 WOL_EN
SML0CLK AN1 SML_PCH_0_CLK
SML0DATA AK1 SML_PCH_0_DATA
SML1ALERT*/PCHHOT*/GPIO73 AU4 PCH_SML1ALERT_L
SML1CLK_GPIO75 AU3 SMBUS_SMC_1_S0_SCL
SML1DATA/GPIO74 AH3 SMBUS_SMC_1_S0_SDA
(IPU/IPD) CL_CLK AF2 NC_CLINK_CLK
(IPU/IPD) CL_DATA AD2 NC_CLINK_DATA
CL_RST* AF4 NC_CLINK_RESET_L

SML1ALERT# pull-up not provided on this page, may be wire-ORed into other signals. Otherwise, 100k pull-up to 3.3V SUS required.

PP3V3_SUS
PP3V3_SUS

R1580 100K XDP_USB_EXTA_OC_L
R1581 100K XDP_USB_EXTB_OC_L
R1582 100K XDP_USB_EXTC_OC_L
R1583 100K XDP_USB_EXTD_OC_L
R1548 1K SPI_IO<2>
R1549 1K SPI_IO<3>
R1590 100K PCH_SMBALERT_L
R1591 100K WOL_EN
5% 1/20W MF 201

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012
PAGE TITLE: PCH PCIe/USB/LPC/SPI/SMBus
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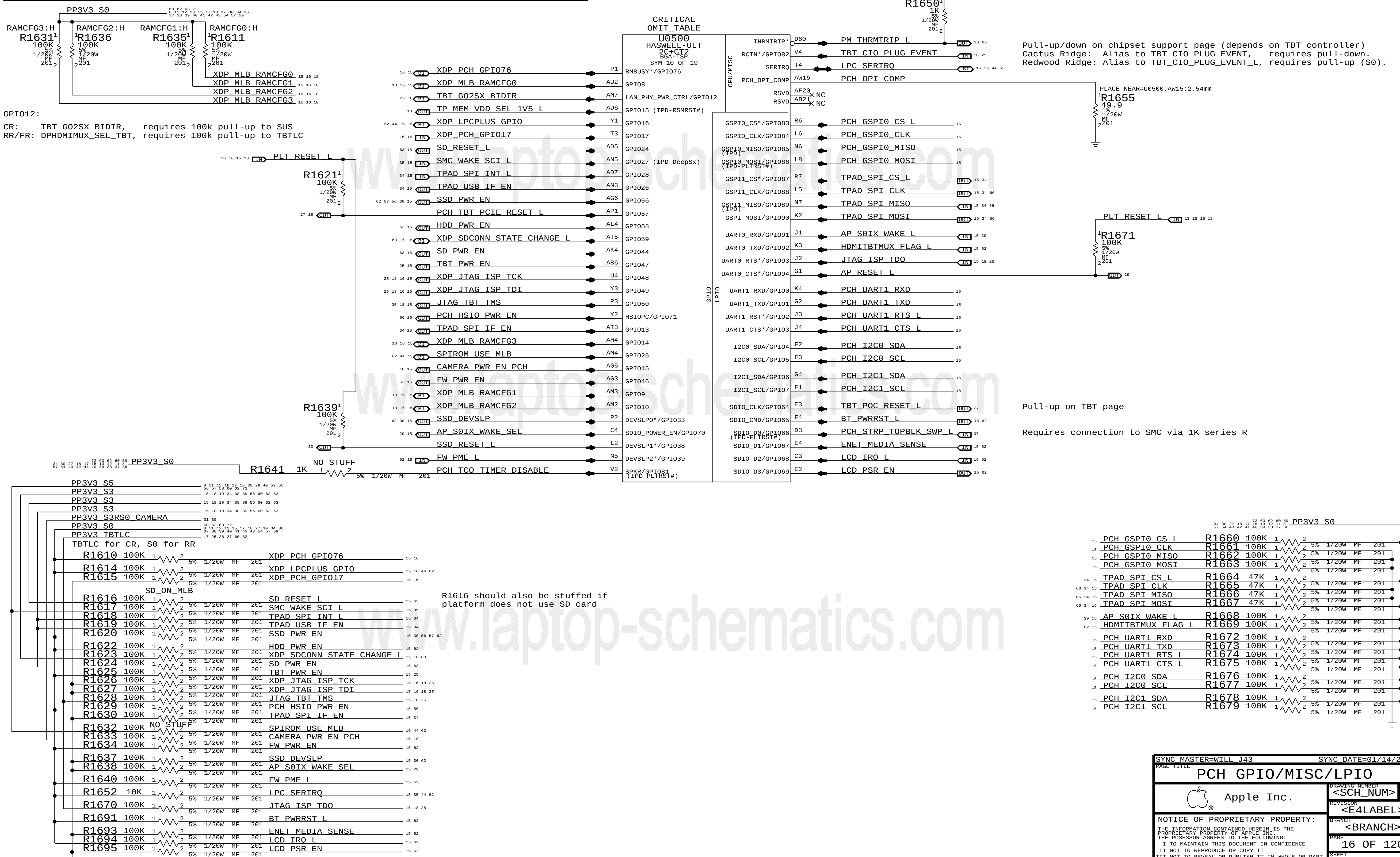
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H



SYNC_MASTER=WILL_J43 SYNC_DATE=01/14/2013

PAGE TITLE: PCH GPIO/MISC/LPIO

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

Merged (CPU/PCH) Micro2-XDP

PP1V05_S0

CRITICAL XDP_CONN J1800 DF40RC-60DP-0.4V M-ST-SM1

R1830 150 5% 1/16W MF-LF 402 PP1V05_S0

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

518S0847

XDP_CPU_PRESENT_L

CPU_VCCST_PWRGD → R1800 1K XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.C61:2.54mm

PM_PWRBTN_L → R1802 0 XDP 5% 1/20W MF 0201 PLACE_NEAR=U5000.J3:2.54mm

PM_PCH_SYS_PWROK → R1804 0 XDP 5% 1/16W MF-LF 402

XDP_CPU_TCK

PCH_JTAGX → R1835 0 XDP 5% 1/20W MF 0201 PLACE_NEAR=J1800.58:28mm

XDP_PCH_TDO → R1810 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.F62:28mm

XDP_CPU_TCK → R1813 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.E60:28mm

TDI and TMS are terminated in CPU.

C1804 0.1UF 10V X5R-CERM 0201 XDP

R1831 1K 5% 1/16W MF-LF 402 XDP

C1800 0.1UF 10V X5R-CERM 0201 XDP

C1801 0.1UF 10V X5R-CERM-X5R 0201 XDP

C1806 0.1UF 10V X5R-CERM-X5R 0201 XDP

XDP_PRESENT# → R1805 1K XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.AG7:2.54mm → PLT_RESET_L

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563 PLACE_NEAR=J1800.51:28mm → XDP_CPU_TDO

CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563 MAKE_BASE=TRUE → XDP_CPUPCH_TRST_L

CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563 PLACE_NEAR=J1800.53:28mm → XDP_CPUPCH_TRST_L

CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563 PLACE_NEAR=J1800.55:28mm → XDP_CPU_TDI

CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563 PLACE_NEAR=J1800.57:28mm → XDP_CPU_TMS

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
ALL_SYS_PWRGD

C1845 0.1UF 10V X5R-CERM 0201

U1845 74LVC1G07GF SOT891 VCC GND

R1845 330K 5% 1/20W MF 201

XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

PCH_JTAGX	R1899 1K	NO STUFF	
XDP_PCH_TDO	R1890 51	XDP	
XDP_PCH_TDI	R1891 51	XDP	
XDP_PCH_TMS	R1892 51	XDP	
XDP_PCH_TCK	R1896 51	NO STUFF	
XDP_CPUPCH_TRST_L	R1897 51	NO STUFF	

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals		Non-XDP Signals
XDP_MLB_RAMCFG0	TP1870	
XDP_USB_EXTA_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	TP1873	
XDP_USB_EXTD_OC_L	TP1874	
XDP_SDCONN_STATE_CHANGE_L	MAKE_BASE=TRUE	XDP_SDCONN_STATE_CHANGE_L
XDP_MLB_RAMCFG1	TP1876	
XDP_MLB_RAMCFG2	TP1877	
XDP_MLB_RAMCFG3	TP1878	
XDP_JTAG_ISP_TCK	MAKE_BASE=TRUE	XDP_JTAG_ISP_TCK
XDP_SSD_PCIE3_SEL_L	R1881 1K	
XDP_SSD_PCIE2_SEL_L	R1882 1K	NOTE: Must not short XDP pins together!
XDP_SSD_PCIE1_SEL_L	R1883 1K	
XDP_SSD_PCIE0_SEL_L	R1884 1K	SSD_PCIE_SEL_L
XDP_LPCPLUS_GPIO	MAKE_BASE=TRUE	XDP_LPCPLUS_GPIO
XDP_PCH_GPIO17	TP1886	
XDP_PCH_GPIO76	TP1887	
XDP_JTAG_ISP_TDI	MAKE_BASE=TRUE	XDP_JTAG_ISP_TDI

Unused & MLB_RAMCFGx GPIOs have TPs.
USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.
JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.
NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.
SSD_PCIEx_SEL_L straps are connected via 1K to common net.
LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: CPU/PCH Merged XDP

Apple Inc.

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System RTC Power Source & 32kHz / 25MHz Clock Generator

Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5

This looks a little ugly to support new and old parts. With GreenCLK Rev C pin 5 must receive S5 power (Stuff R2042)

No bypass necessary

GreenCLK 25MHz Power Must be powered if any VDDIO is powered. — PP3V3_S5RS3RS0_SYSCLKGEN

CAM XTAL Power — PP1V2_CAM_XTALPCIEVDD

TBT XTAL Power — PP3V3_TBTLC

C1924 0.1UF 10% 16V X5R-CERM 0201
C1922 0.1UF 10% 16V X5R-CERM 0201
C1902 1UF 20% 6.3V X5R 0201

U1900 SLG3NB148CV TOFN CRITICAL

NC, VDD, VG3HOT

VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.

CKPLUS_WAIVE=PwrTerm2Gnd

VIOE_25M_A, VIOE_25M_B, VIOE_25M_C

32.768K — PCH_CLK32K_RTCX1

25M_A NC
25M_B SYSCLK_CLK25M_CAMERA
25M_C SYSCLK_CLK25M_TBT
VOUT — PPVRTC_G3H
8 12 13 60 62

For SB RTC Power

C1910 1UF 20% 6.3V X5R 0201

GND, THRM PAD

C1905 12PF 5% 25V NP0-C0G-CERM 0201
C1906 12PF 5% 25V NP0-C0G-CERM 0201

SYSCLK_CLK25M_X2 — R1905 0 5% 1/20W MF 0201 — SYSCLK_CLK25M_X2_R

NO STUFF
R1906 1M 5% 1/20W MF 201

CRITICAL
Y1905 25.000MHZ-12PF-20PPM
SM-3.2X2.5MM

SYSCLK_CLK25M_X1

NOTE: 30 PPM or better required for RTC accuracy

NC_RTC_CLK32K_RTCX2 — NC_RTC_CLK32K_RTCX2
MAKE_BASE=TRUE NO_TEST=TRUE

PCH Reset Button

PP3V3_S0

R1995 10K 5% 1/20W MF 0201

XDP
R1996 0 5% 1/20W MF 0201

XDP_DBRESET_L — PM_SYSRST_L

NO STUFF
R1997 0 5% 1/16W MF-LF 402

SILK_PART=SYS_RESET

Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

PP1V2_S3

C1970 0.1UF 10% 16V X5R-CERM 0201

U1970 74AUP1G07GF SOT891 (VCC, A, Y, NC, NC, NC, GND)

PP3V3_S0

R1970 330K 5% 1/20W MF 201

TPS51916 I(leak) = +/- 1uA, Vih(min) = 1.8V
33uW when driven-low

CPU_MEMVTT_PWR_EN_LSVDDQ

MEMVTT_PWR_EN
MAKE_BASE=TRUE
MEMVTT_PWR_EN

PCH ME Disable Strap

PP5V_S0

R1920 100K 5% 1/20W MF 201

Q1920 DMN5L06VK-7 SOT-563

PP1V5_S0SW_AUDIO_HDA

SPI_DESCRIPTOR_OVERRIDE_LS5V

SPI_DESCRIPTOR_OVERRIDE

R1921 1K 5% 1/20W MF 201

HDA_SDOUT_R
IPD = 9-50k

SPI_DESCRIPTOR_OVERRIDE_L

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

PCH 24MHz Crystal

C1915 6.8PF +/-0.1PF 25V C0G 0201
C1916 6.8PF +/-0.1PF 25V C0G 0201

PCH_CLK24M_XTALOUT_R — R1915 0 5% 1/20W ME 0201 — PCH_CLK24M_XTALOUT

CRITICAL
Y1915 24.000MHZ-20PPM-6PF
3.20X2.50MM-SM1

R1916 1M 5% 1/20W ME 201

PCH_CLK24M_XTALIN

PCH 24MHz Outputs

LPC_CLK24M_SMC_R — PLACE_NEAR=U0500.AN15:5.1mm — R1927 22 5% 1/20W MF 201 — LPC_CLK24M_SMC
MAKE_BASE=TRUE
LPC_CLK24M_SMC

LPC_CLK24M_LPCPLUS_R — PLACE_NEAR=U0500.AP15:5.1mm — R1926 22 5% 1/20W MF 201 — LPC_CLK24M_LPCPLUS

VCCST (1.05V S0) PWRGD

PP3V3_S5

C1930 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
U1930 74AUP1G09 SOT891 (VCC, A, B, Y, NC, NC, GND)

PP1V05_S0

R1931 10K 5% 1/20W MF 201

ALL_SYS_PWRGD

PM_SLP_S3_L

CPU_VCCST_PWRGD

PCH PWROK Generation

PP3V42_G3H
PP3V3_S0

BYPASS=U1950:5MM
C1950 0.1UF 10% 16V X5R-CERM 0201

R1950 10K 5% 1/20W MF 201

CPU_VR_EN

R1955 10K 5% 1/20W MF 201

NO STUFF
R1951 0 5% 1/20W MF 0201

CPU_VR_READY
MAKE_BASE=TRUE
CPU_VR_READY

ALL_SYS_PWRGD — CPUVR_PGOOD_R

U1950 74LVC2G08GT SOT833

PM_S0_PGOOD

NO STUFF
R1961 100K 5% 1/20W MF 201

R1963 0 5% 1/20W MF 0201

NO STUFF WF: Do we need this?
R1960 0 5% 1/20W MF 0201

CKPLUS_WAIVE=UNCONNECTED_PINS

U1950 74LVC2G08GT SOT833

SYS_PWROK_R

R1962 1K 5% 1/20W MF 201

PM_PCH_SYS_PWROK

PM_PCH_PWROK
PM_PCH_PWROK
MAKE_BASE=TRUE

SMC_DELAYED_PWRGD

SYNC_MASTER=J43_MLB1	SYNC_DATE=01/09/2013
PAGE TITLE	Chipset Support
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Platform Reset Connections

Unbuffered

PLT_RESET_L → R2081 33 1/10W MF-LF 402 → LPCPLUS_RESET_L

R2071 0 1/20W MF 0201 → PCA9557D_RESET_L

Scrub for Layout Optimization

Buffered

PP3V3_S0 → CRITICAL U2071 MC74VHC1G08 SC70-HF

C2071 0.1UF 10% 16V X5R-CERM 0201

R2070 100K 5% 1/20W MF 201

PLT_RST_BUF_L → R2072 0 1/20W MF 0201 → SMC_LRESET_L

R2088 0 1/20W MF 0201 → BKLT_PLT_RST_L

R2089 0 1/20W MF 0201 → CAM_PCIE_RESET_L

PCH_TBT_PCIE_RESET_L (IN) = PCH_TBT_PCIE_RESET_L (OUT)
MAKE_BASE=TRUE

GreenCLK 25MHz Power

PP3V3_S3 → NO STUFF R2040 0 1/20W MF 0201 → PP3V3_S5RS3RS0_SYSCLKGEN

PP3V3_S5RS3RS0_SYSCLKGEN
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0 → NO STUFF R2041 0 1/20W MF 0201

R2041/2 should be stuffed for GreekCLK A or B depending on S2 rail

R2042 should be stuffed for GreenCLK C

PP3V3_S5 → R2042 0 1/20W MF 0201

DDC Pull-Ups

2.2k pull-ups are required by PCH to indicate active display interface.

DP++ spec violation, should remove!

PP3V3_S0

NO STUFF R2020 2.2K 5% 1/20W MF 201

R2021 2.2K 5% 1/20W MF 201

NO STUFF R2022 2.2K 5% 1/20W MF 201

R2023 2.2K 5% 1/20W MF 201

DP_TBTSNK0_DDC_CLK
DP_TBTSNK0_DDC_DATA
DP_TBTSNK1_DDC_CLK
DP_TBTSNK1_DDC_DATA

TBTSNK1_DDC is pulled-up just to indicate that DP port is used. No DDC on this port, AUX-only.

NOTE: Only DDC_DATA is sensed by PCH, so DDC_CLK pull-ups are unstuffed.

Thunderbolt Pull-up/downs

Cactus Ridge GO2SX signal pulled-up to SUS rail

PP3V3_SUS

R2013 10K 5% 1/20W MF 201

TBT_GO2SX_BIDIR (BI) = TBT_GO2SX_BIDIR (BI) MAKE_BASE TRUE

Cactus Ridge PLUG_EVENT is active-high, always driven (pull-down)

TBT_CIO_PLUG_EVENT (OUT) = TBT_CIO_PLUG_EVENT (IN) TRUE

Required for unused second TBT port

TBT_B_CIO_SEL (IN)
DP_TBTPB_HPD (OUT)
TBT_B_CONFIG2_RC (OUT)
TBT_B_CONFIG1_BUF (OUT)
TBT_B_LSRX (IN)

R2015 100K 5% 1/20W MF 201

R2016 10K 5% 1/20W MF 201

R2017 10K 5% 1/20W MF 201

R2018 10K 5% 1/20W MF 201

R2019 10K 5% 1/20W MF 201

R2014 10K 5% 1/20W MF 201

PP3V3_S5 → NOSTUFF C2030 0.1UF 10% 16V X5R-CERM 0201
BYPASS=U2030:3mm

NOSTUFF CRITICAL U2030 74LVC1G08 SOT891

PM_SLP_S4_L (IN)
CAMERA_PWR_EN_PCH (IN)
CAMERA_PWR_EN (OUT)
NC

R2030 0 1/20W MF 0201

Power State Debug LEDs

(For development only)

PP3V3_S5 → DBGLED R2094 0 1/10W MF-LF 402 → PP3V3_S5_DBGLED
PLACE_SIDE=BOTTOM
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=3.3V

DBGLED R2090 20K	DBGLED R2091 20K	DBGLED R2092 20K	DBGLED R2093 20K	DBGLED R2095 20K
DBGLED_S5	DBGLED_S4	DBGLED_S3	DBGLED_S0I3	DBGLED_S0
DBGLED D2090 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S5_ON	DBGLED D2091 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S4_ON	DBGLED D2092 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S3_ON	DBGLED D2093 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S0I3_ON	DBGLED D2095 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S0_ON
DBGLED_S4_D	DBGLED_S3_D	DBGLED_S0I3_D	DBGLED_S0_D	
DBGLED Q2090 DMN5L06VK-7 SOT-563	DBGLED Q2090 DMN5L06VK-7 SOT-563	DBGLED Q2091 DMN5L06VK-7 SOT-563	DBGLED Q2091 DMN5L06VK-7 SOT-563	

S4_PWR_EN (IN)
PM_SLP_S4_L (IN)
PM_SLP_S3_L (IN)
PM_SLP_S0_L (IN)

TBT Aliases

MAKE_BASE

DP_TBTSNK0_DDC_CLK (IN) = DP_TBTSNK0_DDC_CLK (OUT) TRUE
DP_TBTSNK0_DDC_DATA (BI) = DP_TBTSNK0_DDC_DATA (BI) TRUE

MAKE_BASE

DP_TBTSNK1_HPD (OUT) = DP_TBTSNK1_HPD (IN) TRUE
=DP_TBTSNK1_ML_C_P<3..0> (IN) = DP_TBTSNK1_ML_C_P<3..0> (OUT) TRUE
=DP_TBTSNK1_ML_C_N<3..0> (IN) = DP_TBTSNK1_ML_C_N<3..0> (OUT) TRUE
DP_TBTSNK1_AUXCH_C_P (BI) = DP_TBTSNK1_AUXCH_C_P (BI) TRUE
DP_TBTSNK1_AUXCH_C_N (BI) = DP_TBTSNK1_AUXCH_C_N (BI) TRUE
DP_TBTSNK1_DDC_CLK (IN) = DP_TBTSNK1_DDC_CLK TRUE
DP_TBTSNK1_DDC_DATA (BI) = DP_TBTSNK1_DDC_DATA TRUE

Single-port TBT implementation does not require DDC Crossbar

MAKE_BASE MAKE_BASE

JTAG_ISP_TDO (OUT) = JTAG_ISP_TDO (IN) TRUE
XDP_JTAG_ISP_TCK (IN) = XDP_JTAG_ISP_TCK (OUT)
XDP_JTAG_ISP_TDI (IN) = XDP_JTAG_ISP_TDI (OUT)
JTAG_TBT_TMS (IN) = JTAG_TBT_TMS (OUT) TRUE

No MAKE_BASE on TCK/TDI as these are provided on XDP page.

RAM Configuration Straps

Pull-downs for chip-down RAM systems

XDP_MLB_RAMCFG0 (OUT)
XDP_MLB_RAMCFG1 (OUT)
XDP_MLB_RAMCFG2 (OUT)
XDP_MLB_RAMCFG3 (OUT)

RAMCFG3:L	RAMCFG2:L	RAMCFG1:L	RAMCFG0:L
R2050 10K 5% 1/20W MF 201	R2051 10K 5% 1/20W MF 201	R2052 10K 5% 1/20W MF 201	R2053 10K 5% 1/20W MF 201

LPDDR3 Alias Support

TP_CPU_MEM_RESET_L (IN) = TP_CPU_MEM_RESET_L MAKE_BASE=TRUE
TP_MEM_VDD_SEL_1V5_L (IN) = TP_MEM_VDD_SEL_1V5_L MAKE_BASE=TRUE
PP0V6_S3_MEM_VREFDQ_A = PP0V6_S3_MEM_VREFDQ_A MAKE_BASE=TRUE VOLTAGE=0.6V
PP0V6_S3_MEM_VREFCA_A = PP0V6_S3_MEM_VREFCA_A MAKE_BASE=TRUE VOLTAGE=0.6V
PP0V6_S3_MEM_VREFDQ_B = PP0V6_S3_MEM_VREFDQ_B MAKE_BASE=TRUE VOLTAGE=0.6V
PP0V6_S3_MEM_VREFCA_B = PP0V6_S3_MEM_VREFCA_B MAKE_BASE=TRUE VOLTAGE=0.6V

SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013

PAGE TITLE: Project Chipset Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during DAC margining

CPU_DIMMA_VREFDQ
CPU_DIMMB_VREFDQ
CPU_DIMM_VREFCA

CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563
CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.

CPU_MEM_VREFDQ_A_ISOL
CPU_MEM_VREFDQ_B_ISOL
CPU_MEM_VREFCA_A_ISOL
CPU_MEM_VREFCA_B_ISOL

DDRVREF_DAC R2225 100K 5% 1/20W MF 201 — VREFMRGN_DQ_A_EN_RC — DDRVREF_DAC C2225 0.1UF 10% 6.3V CERM-X5R 0201
DDRVREF_DAC R2201 100K 5% 1/20W MF 201
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
Q2225 pin 6: PLACE_NEAR=Q2220.6:2.54mm

DDRVREF_DAC R2245 100K 5% 1/20W MF 201 — VREFMRGN_DQ_B_EN_RC — DDRVREF_DAC C2245 0.1UF 10% 6.3V CERM-X5R 0201
DDRVREF_DAC R2202 100K 5% 1/20W MF 201
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
Q2265 pin 6: PLACE_NEAR=Q2260.6:2.54mm

DDRVREF_DAC R2265 100K 5% 1/20W MF 201 — VREFMRGN_CA_A_EN_RC — DDRVREF_DAC C2265 0.1UF 10% 6.3V CERM-X5R 0201
DDRVREF_DAC R2215 100K 5% 1/20W MF 201
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563

DDRVREF_DAC R2285 100K 5% 1/20W MF 201 — VREFMRGN_CA_B_EN_RC — DDRVREF_DAC C2285 0.1UF 10% 6.3V CERM-X5R 0201
DDRVREF_DAC R2207 100K 5% 1/20W MF 201
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
R22x6 pin 2: PLACE_NEAR=Q2225.1:2.54mm, PLACE_NEAR=Q2265.1:2.54mm, PLACE_NEAR=Q2225.4:2.54mm, PLACE_NEAR=Q2265.4:2.54mm

VRef Dividers

Always used, regardless of margining option.

PP1V2_S3

R2223 10 1% 1/20W MF 201 — PLACE_NEAR=Q2221.2:1mm — R2222 8.2K 1% 1/20W MF 201
C2220 0.022UF 10% 6.3V X5R-CERM 0201 — PLACE_NEAR=Q2220.6:2mm
R2220 24.9 1% 1/20W MF 201 — PLACE_NEAR=Q2220.6:3mm — PP0V6_S3_MEM_VREFDQ_A (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm)
MEM_VREFDQ_A_RC

R2243 10 1% 1/20W MF 201 — PLACE_NEAR=Q2241.2:1mm — R2242 8.2K 1% 1/20W MF 201
C2240 0.022UF 10% 6.3V X5R-CERM 0201 — PLACE_NEAR=Q2260.6:2mm
R2240 24.9 1% 1/20W MF 201 — PLACE_NEAR=Q2260.6:3mm — PP0V6_S3_MEM_VREFDQ_B (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm)
MEM_VREFDQ_B_RC

R2263 10 1% 1/20W MF 201 — PLACE_NEAR=Q2261.2:1mm — R2262 8.2K 1% 1/20W MF 201
C2260 0.022UF 10% 6.3V X5R-CERM 0201 — PLACE_NEAR=Q2220.3:2mm
R2260 24.9 1% 1/20W MF 201 — PLACE_NEAR=Q2220.3:3mm — PP0V6_S3_MEM_VREFCA_A (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm)
MEM_VREFCA_A_RC

R2283 10 1% 1/20W MF 201 — PLACE_NEAR=R2281.2:1mm — R2282 8.2K 1% 1/20W MF 201
C2280 0.022UF 10% 6.3V X5R-CERM 0201 — PLACE_NEAR=Q2260.3:2mm
R2280 24.9 1% 1/20W MF 201 — PLACE_NEAR=Q2260.3:3mm — PP0V6_S3_MEM_VREFCA_B (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm)
MEM_VREFCA_B_RC

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

PP3V3_S3
OMIT R2218 SHORT 402
PP3V3_S3_VREFMRGN_DAC (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)
DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC

U2200 DAC5574 MSOP
SMBUS_PCH_CLK (SCL)
SMBUS_PCH_DATA (SDA)
Addr=0x98(WR)/0x99(RD)
VOUTA — VREFMRGN_DQ_A
VOUTB — VREFMRGN_DQ_B
VOUTC — VREFMRGN_CA_AB
VOUTD — VREFMRGN_MEMVREG

NOTE: MEMVREG and SPARE share a DAC output, cannot enable both at the same time!

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC
R2200 100K 5% 1/20W MF 201

U2201 PCA9557 QFN (OD)
Addr=0x30(WR)/0x31(RD)
SMBUS_PCH_CLK
SMBUS_PCH_DATA
P0 — VREFMRGN_CPU_EN
P1 — VREFMRGN_DQ_A_EN
P2 — VREFMRGN_DQ_B_EN
P3 — VREFMRGN_CA_A_EN
P4 — VREFMRGN_CA_B_EN
P5 — VREFMRGN_MEMVREG_EN
P6 — VREFMRGN_SPARE_EN
P7 — NC
RESET* — PCA9557D_RESET_L
THRM PAD, GND

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

(All 4 R's) DDRVREF_DAC
R2226 4.02K 1% 1/20W MF 201 — VREFMRGN_DQ_A_RDIV
R2246 4.02K 1% 1/20W MF 201 — VREFMRGN_DQ_B_RDIV
R2266 4.02K 1% 1/20W MF 201 — VREFMRGN_CA_A_RDIV
R2286 4.02K 1% 1/20W MF 201 — VREFMRGN_CA_B_RDIV

PP3V3_S3
DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_MEMVREG_BUF
DDRVREF_DAC R2214 38.3K 1% 1/20W MF 201 — DDRREG_FB (OUT) — PLACE_NEAR=R7415.2:1mm

DDRVREF_DAC R2213 100K 5% 1/20W MF 201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_SPARE_BUF
DDRVREF_DAC R2217 1M 5% 1/20W MF 201
Pins B1 & B4: CKPLUS_WAIVE=unconnected_pins

DDRVREF_DAC R2212 100K 5% 1/20W MF 201

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output	3.53mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC_MASTER=WILL_J43 SYNC_DATE=02/04/2013

PAGE TITLE: DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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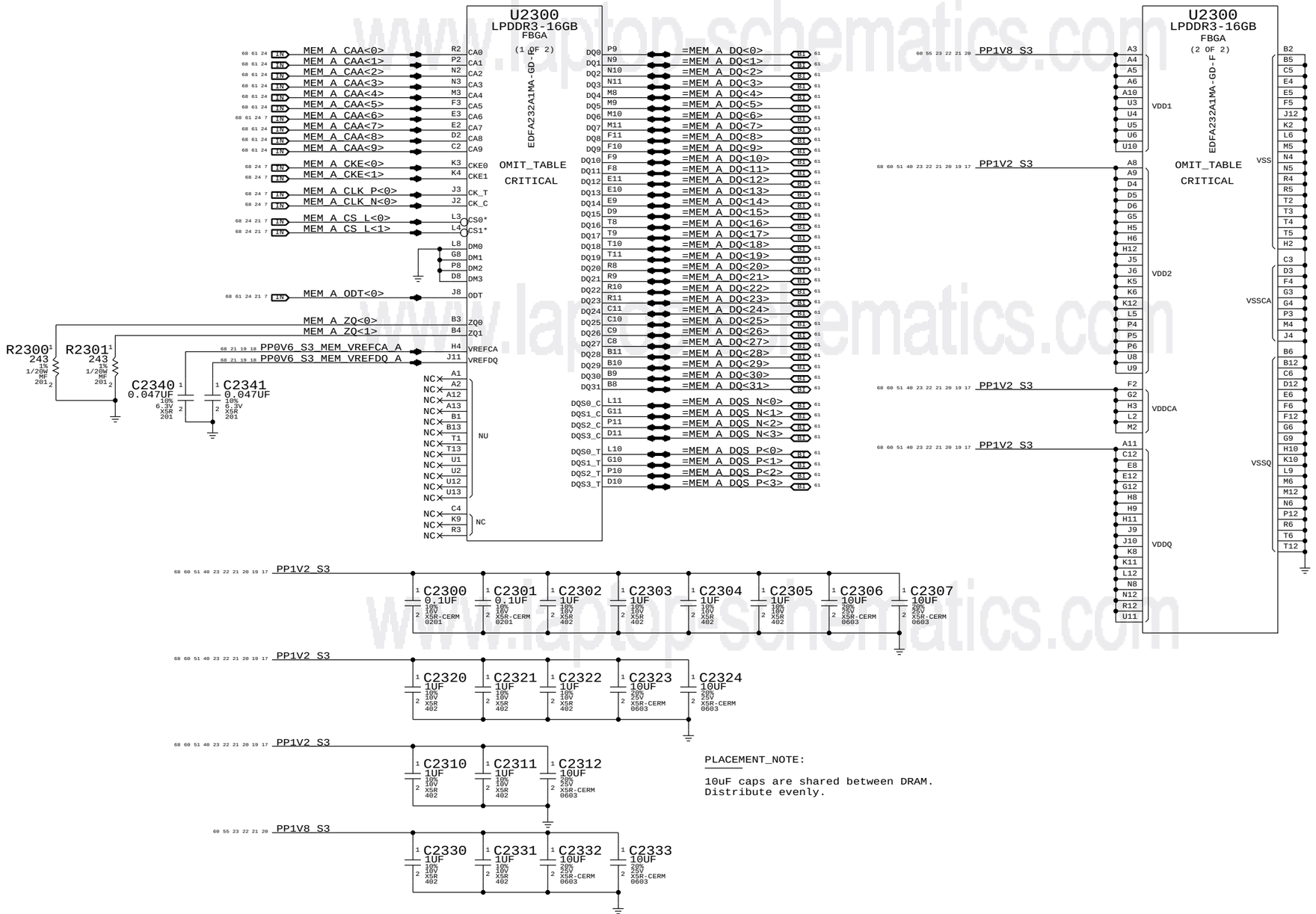
LPDDR3 CHANNEL A (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
LPDDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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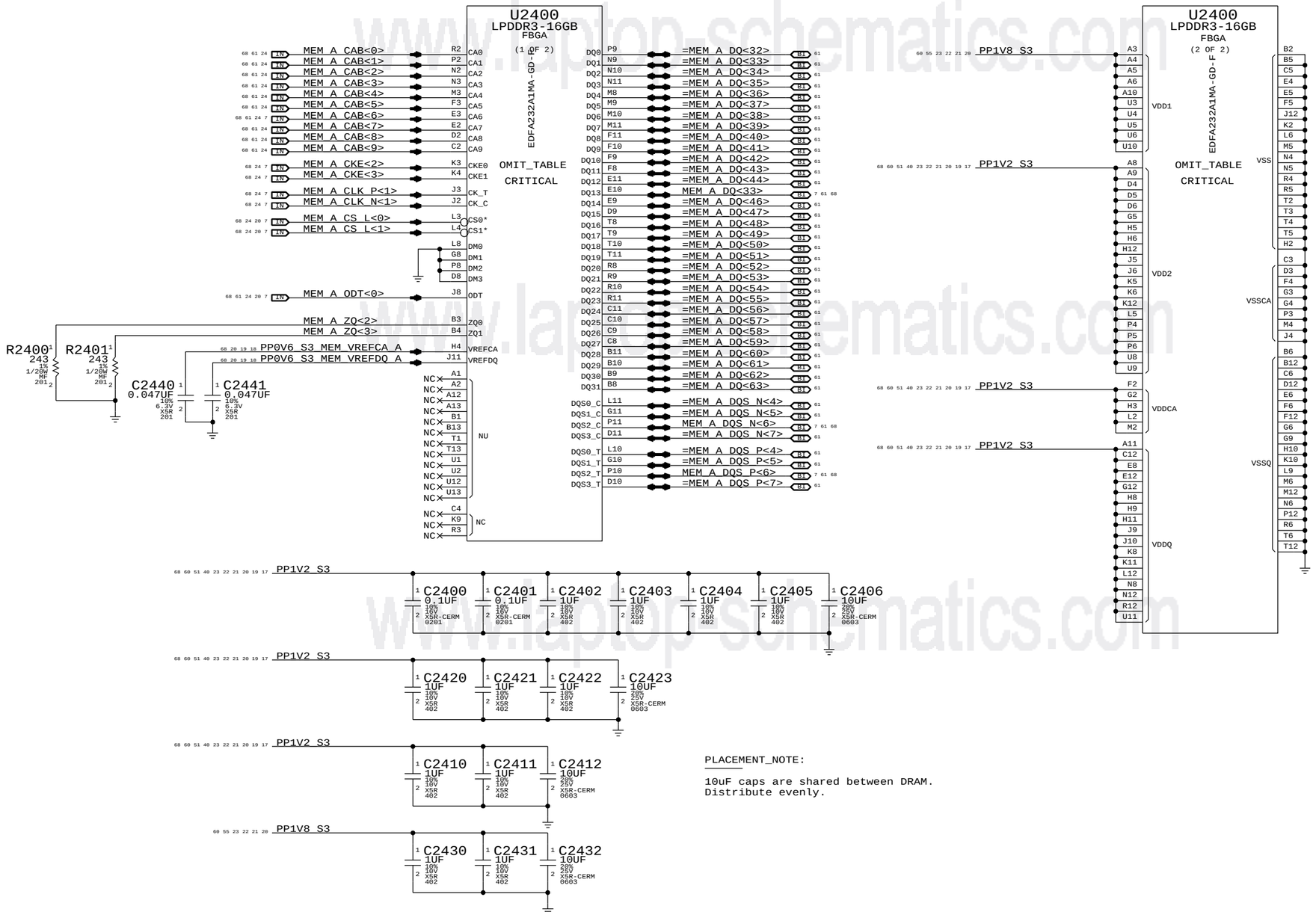
LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
LPDDR3 DRAM Channel A (32-63)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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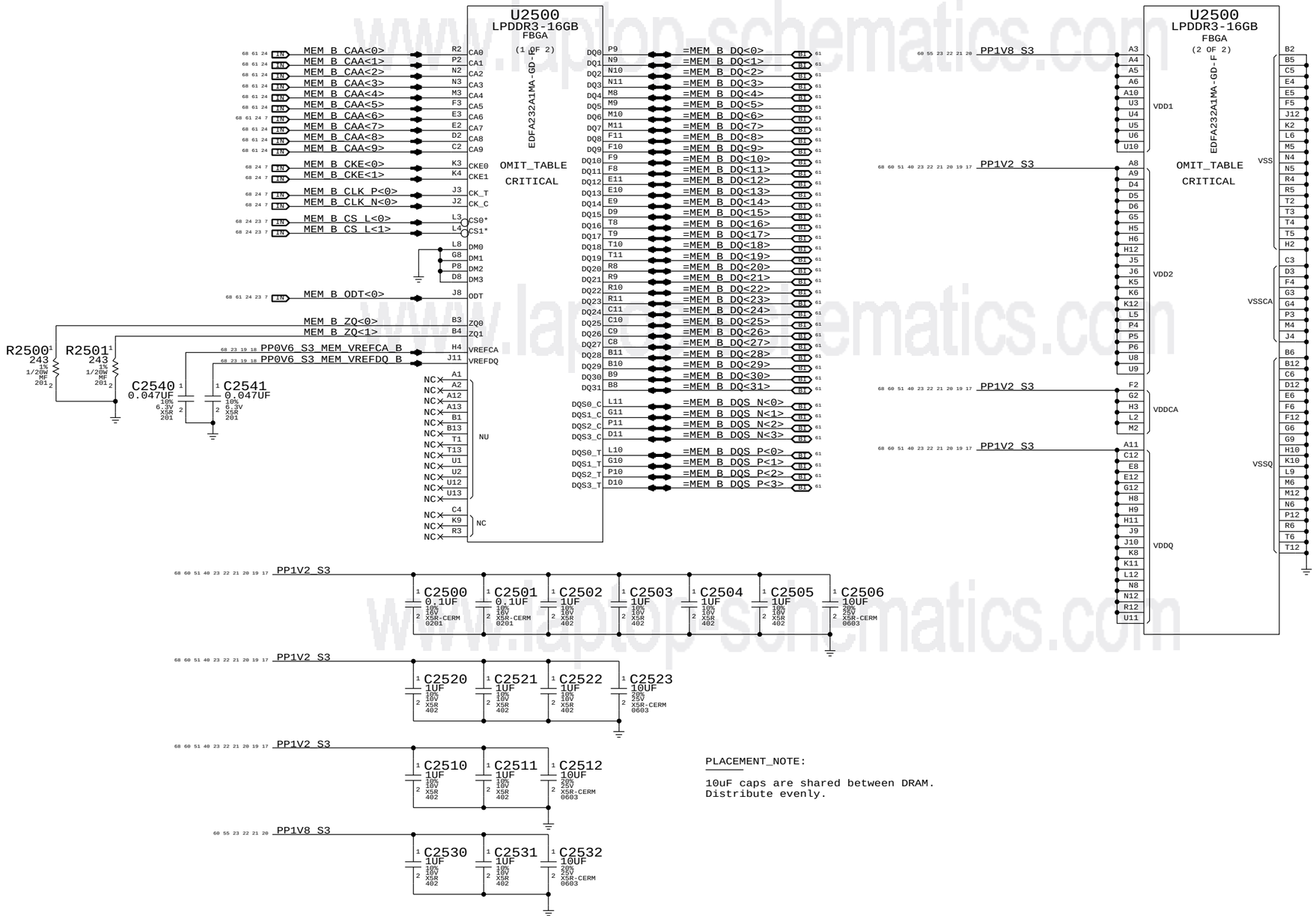
LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
LPDDR3 DRAM Channel B (0-31)

Apple Inc.

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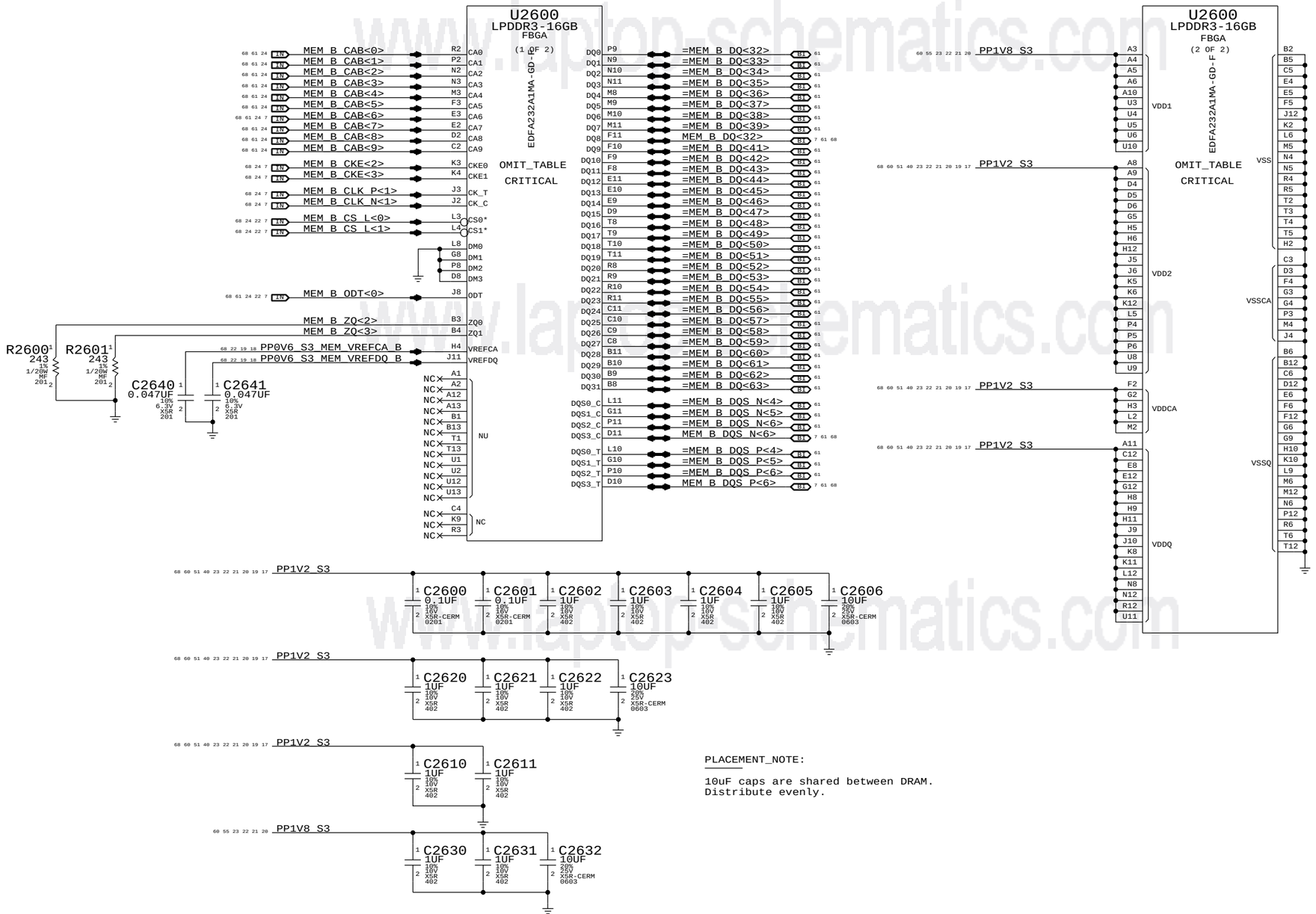
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
LPDDR3 DRAM Channel B (32-63)

Apple Inc.

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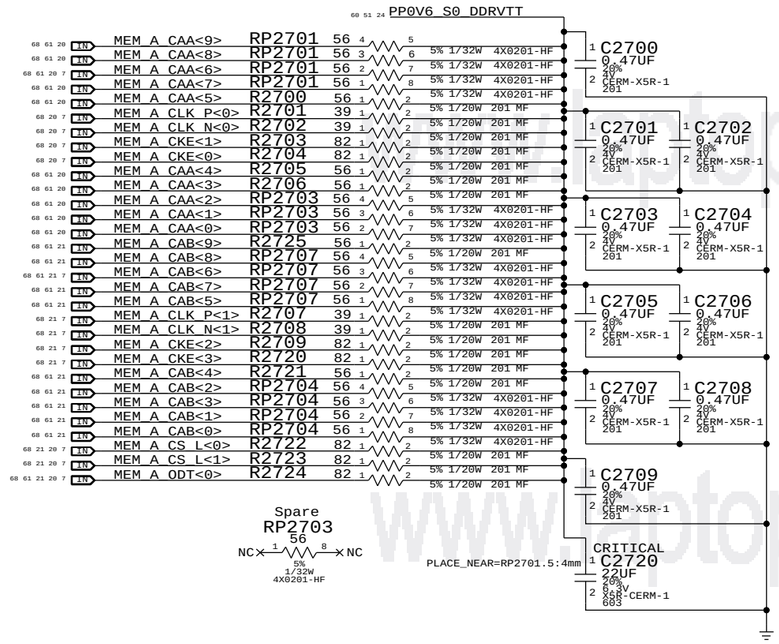
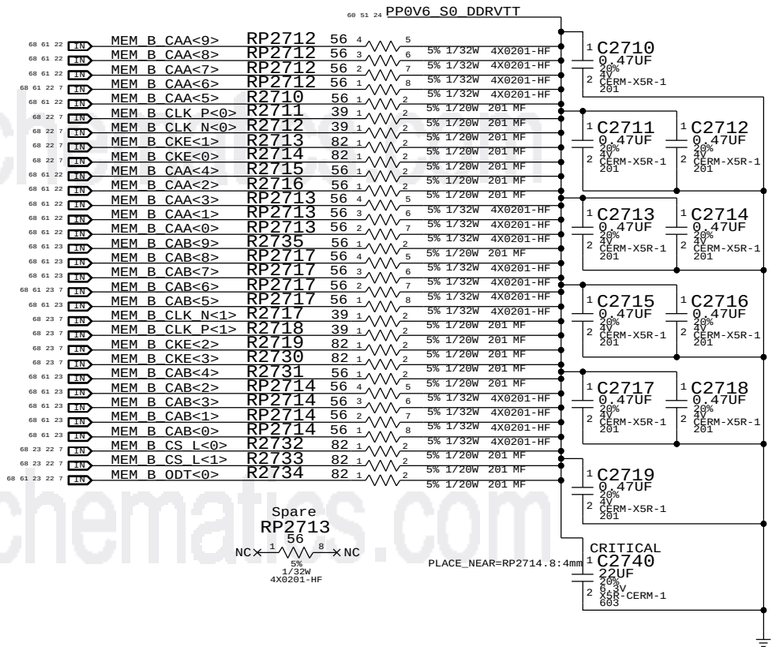
Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





SYNC_MASTER=J43_MLB SYNC_DATE=09/21/2012

PAGE TITLE: LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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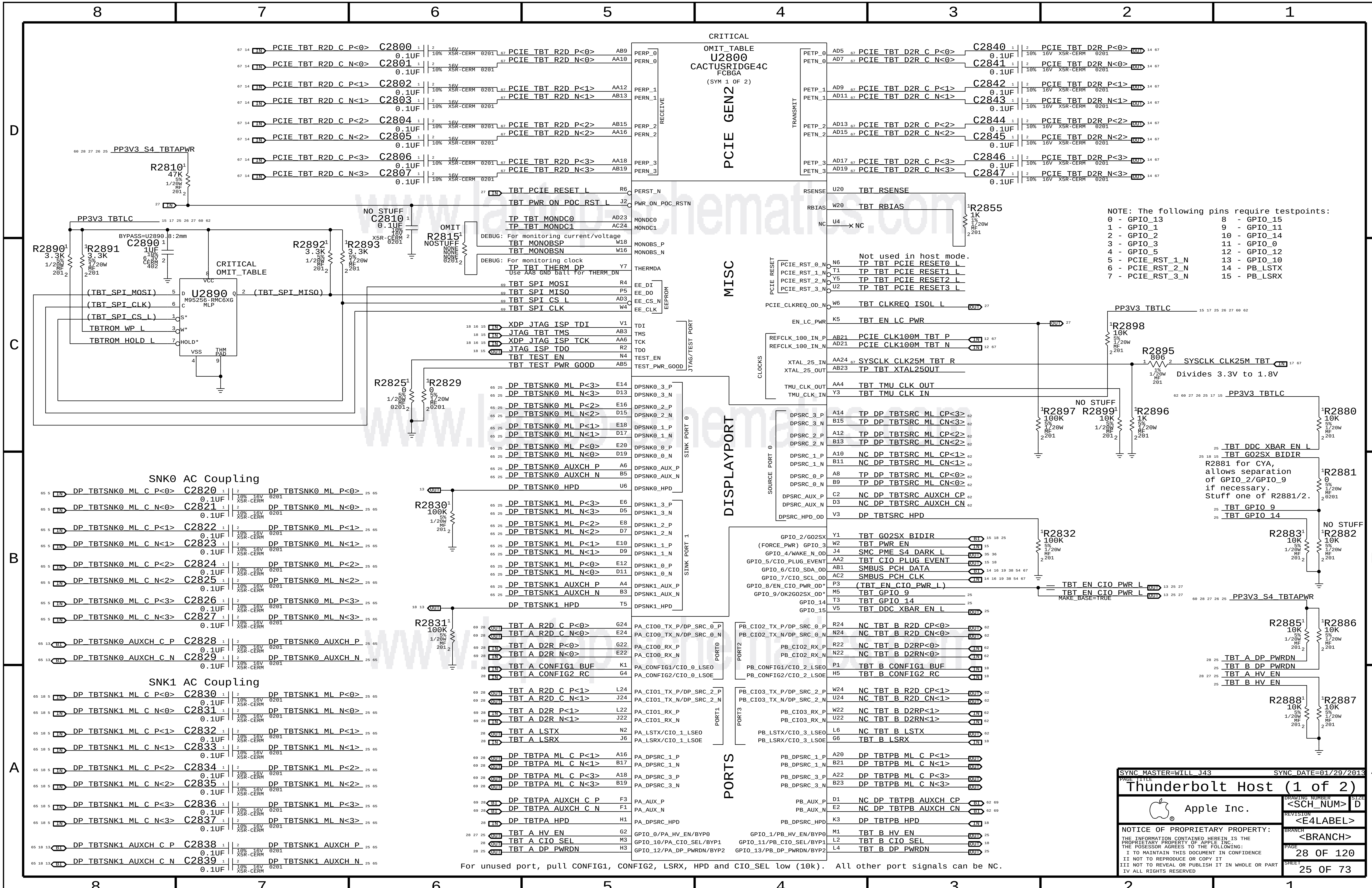
CRITICAL
OMIT_TABLE
U2800
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)
PCIE GEN2
MISC
DISPLAYPORT
PORTS
SNK0 AC Coupling
SNK1 AC Coupling
CRITICAL
OMIT_TABLE
U2890
M95256-RMC6XG
MLP
BYPASS=U2890.8:2mm
NO STUFF
OMIT
NOSTUFF
DEBUG: For monitoring current/voltage
DEBUG: For monitoring clock
Use AA8 GND ball for THERM_DN
Not used in host mode.
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
Divides 3.3V to 1.8V
R2881 for CYA, allows separation of GPIO_2/GPIO_9 if necessary. Stuff one of R2881/2.
MAKE_BASE=TRUE
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=WILL_J43
SYNC_DATE=01/29/2013
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
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<BRANCH>
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25 OF 73
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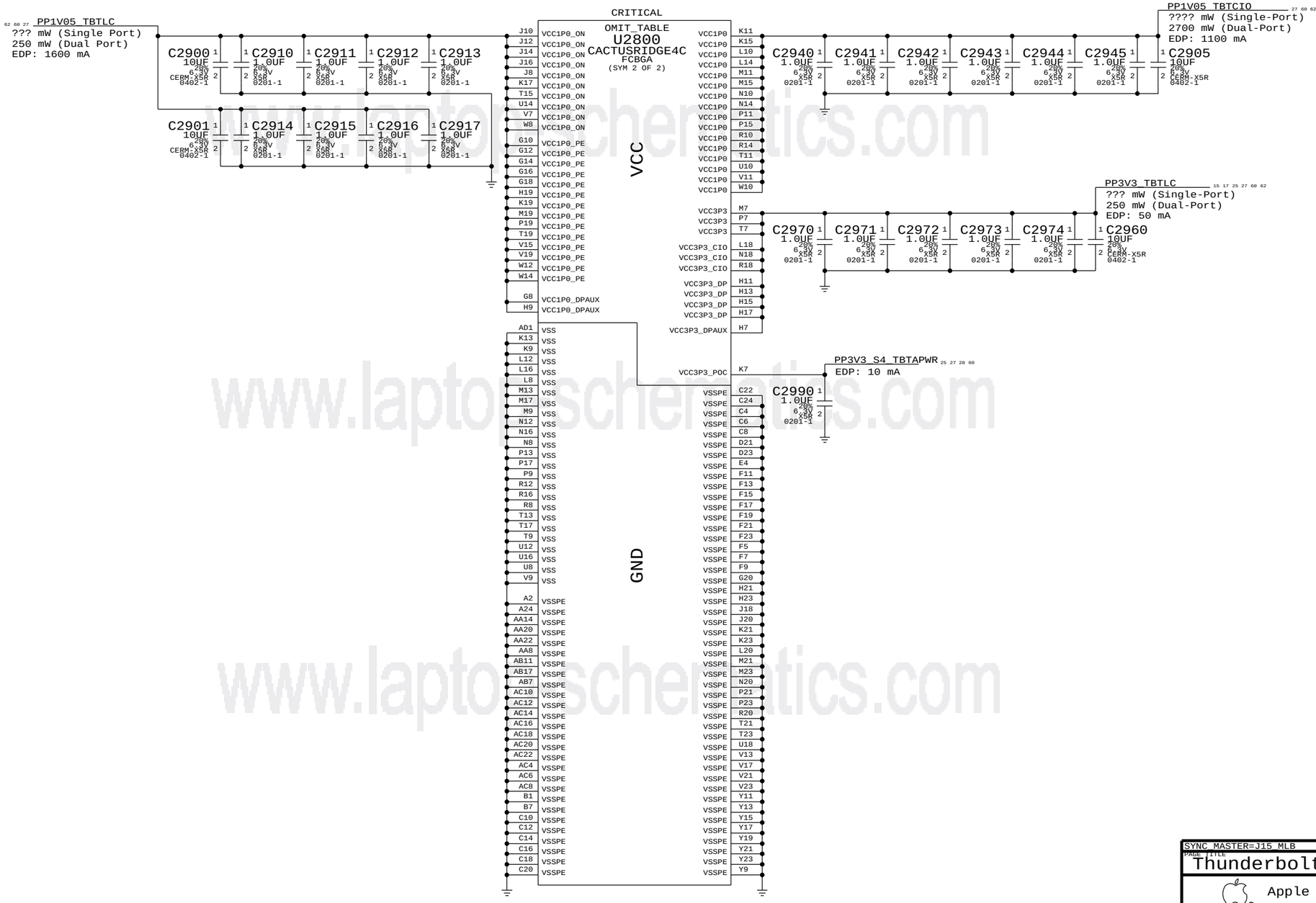

EDP numbers are from 12/22/2011 email from Haim Lustig (Intel) to Paul Baker (Apple)
Power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC_MASTER=J15_MLB SYNC_DATE=07/16/2012

PAGE TITLE
Thunderbolt Host (2 of 2)

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
(NONE)

TBT 15V Boost Regulator

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPBUS_G3H
8-13V Input
Changes required for 2S.

PPVIN_S4SW_TBTBST_FET
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_MODE=TRUE
DIOT=TRUE

TBTBST_SNS1
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

TBTBST_SNS2
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

TBTBST_VSNS
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

PP15V_TBT
Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

PLACE_NEAR=C3095.1:2 mm

TBTBST_EN_UVLO
TBTBST_INTVCC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
TBTBST_VC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
TBTBST_FBX
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
TBTBST_VSNS_RC
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

SGND shorted to GND inside package, no XW necessary.

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

Vout = 1.6V * (1 + Ra / Rb)

TBT_A_HV_EN

Supervisor & CLKREQ# Isolation

PP3V3_S0
PP3V3_TBTLC
PP1V05_TBTLC
TBT_EN_LC_PWR
PCH_TBT_PCIE_RESET_L
Platform (PCIe) Reset
TBT_CLKREQ_L
Pull-up provided by SB page.
TBT_PCIE_RESET_L
DLY = 60 ms +/- 20%
TBT_CLKREQ_ISOL_L
MAKE_BASE=TRUE
TBT_EN_LC_ISOL
TBT_EN_LC_RC3V3
TBT_EN_LC_RC1V05

3.3V TBT "LC" Switch

Max Current = 2A (85C)

U3010	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ / 25.8 mOhm Max

1.05V TBT "LC" Switch

Max Current = 4A (85C)

U3015	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	6.1 mOhm Typ / 10.4 mOhm Max

TBT "POC" Power-up Reset

PP3V3_S4_TBTAPWR
Pull-up: R2810
TBT_PWR_ON_POC_RST_L
TBTPOCRST_CT
TBTPOCRST_MR_L
TPS3808G25
Vt = 2.33V +/- 2%
Delay = 27.3ms
PP3V3_S0
TBT_POC_RESET_L

1.05V TBT "CIO" Switch

PP1V05_S0
PP3V3_TBTLC
TBT_EN_CIO_PWR
TBT_EN_CIO_PWR_L
Max Current = 4A (85C)

U3020	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	6.1 mOhm Typ / 10.4 mOhm Max

SMC_DELAYED_PWRGD

SYNC_MASTER=WILL_J43	SYNC_DATE=12/17/2012
PAGE TITLE	TBT Power Support
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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	BRANCH <BRANCH>
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3.3V/HV Power MUX

V3P3 must be S4 to support wake
from Thunderbolt device attach.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
CRITICAL C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3280 22UF 20% 6.3V X5R-CERM 0603
C3281 0.1UF 10% 16V X5R-CERM 0201
PP15V_TBT 18.9V Max
C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 16V X5R 402
CRITICAL U3210 CD3211A0RGPR QFN
V3P3 V3P3OUT VHV OUT ENHVU FAULTZ EN ISET_V3P3 HV_EN ISET_S0 S0 ISET_S3 GND THRM PAD
C3285 0.1UF 10% 16V X5R-CERM 0201
C3286 10UF 20% 6.3V CERM-X5R 0402-1
C3211 0.1UF 10% 25V X5R 402
PP3V3_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
PP3V3RHV_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
S4_PWR_EN
TBT_A_HV_EN
PM_SLP_S3_BUF_L
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTHV:P15V
12V: See below
R3210 22.6K 1% 1/20W MF 201
R3211 22.6K 1% 1/20W MF 201
R3212 36.5K 1% 1/20W MF 201 <RV3P3>
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R3213 22.6K 1% 1/20W MF 201 <RHVS3>
R3214 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

PP3V3_S4_TBTAPWR
C3220 0.1UF 10% 16V X5R-CERM 0201
CRITICAL U3220 CBTL05024 HVQFN24-COMBO
SIGNAL_MODEL=TBT_MUX
VDD GND_THMPAD
TBT_A_D2R_N<1> TBT_A_D2R_P<1> C3277 0.47UF 20% 4V_201 CERM-X5R-1 C3276 0.47UF 20% 4V_201 CERM-X5R-1
GND_VOID=TRUE (Both C's)
TBT_A_D2R_C_N<1> TBT_A_D2R_C_P<1>
DP_TBTPA_AUXCH_C_N DP_TBTPA_AUXCH_C_P C3230 0.1UF 10% 16V X5R-CERM 0201 C3231 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPA_AUXCH_N DP_TBTPA_AUXCH_P
DP_TBTSNK0_DDC_DATA DP_TBTSNK0_DDC_CLK
DDC_DAT DDC_CLK
DP_TBTPA_ML_C_P<1> DP_TBTPA_ML_C_N<1> C3232 0.22UF 20% 6.3V X5R 0201 C3233 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_P<1> DP_TBTPA_ML_N<1>
TBT_A_LSTX TBT_A_LSRX
LSTX (IPU) LSRX (IPD)
DP_TBTPA_HPD
HPDOUT
TBT_A_CONFIG1_BUF
CA_DETOUT
TBT_A_CIO_SEL
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R1_AUXDDC_P
TBT: RX_1
TBT_A_CONFIG1_RC
TBT_A_HPD
TBT: LSX_A_R2P/P2R (P/N)

Thunderbolt Connector A

CRITICAL L3200 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTAPWR_F
C3200 0.01UF 10% 16V X7R-CERM 0402
R3201 12 5% 1/20W MF 201
C3201 0.01UF 10% 50V X7R-CERM 0402
TBTACONN_20_RC
TBTACONN_1_C
TBTACONN_7_C
GND_VOID=TRUE (0-18.9V)
C3205 0.01UF 10% 25V X5R-CERM 0201
C3206 0.01UF 10% 25V X5R-CERM 0201
TBT Dir DP Dir
TBT: TX_0
TBT: TX_1
TBT: RX_0
TBT: Unused
TBT: RX_1
J3200 MDP-J11 F-RT-TH
CRITICAL 514-0818
HOT_PLUG_DETECT CONFIG1 CONFIG2 GND ML_LANE3P ML_LANE3N GND AUX_CHP AUX_CHN DP_PWR
GND ML_LANE0P ML_LANE0N GND ML_LANE1P ML_LANE1N GND ML_LANE2P ML_LANE2N RETURN
SHIELD PINS
TBT_A_D2R_C_N<0> TBT_A_D2R_C_P<0> C3274 0.47UF 20% 4V_201 CERM-X5R-1 C3275 0.47UF 20% 4V_201 CERM-X5R-1
TBT_A_D2R_N<0> TBT_A_D2R_P<0>
R3294 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3295 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
DP_TBTPA_ML_C_N<3> DP_TBTPA_ML_C_P<3> C3278 0.22UF 20% 6.3V X5R 0201 C3279 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_N<3> DP_TBTPA_ML_P<3>
R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201
TBT_A_D2R1_AUXDDC_P TBT_A_D2R1_AUXDDC_N
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R-CERM 0201
C3295 330PF 10% 16V X7R-CERM 0201
R3241 100K 5% 1/20W MF 201
C3202 0.01UF 10% 16V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
C3270 0.22UF 20% 6.3V X5R 0201 C3271 0.22UF 20% 6.3V X5R 0201
C3272 0.22UF 20% 6.3V X5R 0201 C3273 0.22UF 20% 6.3V X5R 0201
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201
470K R's for ESD protection on AC-coupled signals.

SYNC_MASTER=J43_MLB SYNC_DATE=09/04/2012

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

Sense resistor on sensor page

PP3V3_WLAN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

PP3V3_WLAN_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
Max Current = 2A (85C)

U3550
TPS22924
CSP
CRITICAL
A1 VOUT
B1
A2 VIN
B2 PP3V3_S5
C2 ON SMC_WIFI_PWR_EN
GND
C1

C3550
1.0UF
10%
6.3V
X6S
0201-1

C3521
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=J3501:5mm

514S0335
CRITICAL
J3501
SSD-K99
F-RT-SM1

AIRPORT

PCIE_AP_R2D_N → C3531 0.1UF → PCIE_AP_R2D_C_N
PCIE_AP_R2D_P → C3530 0.1UF → PCIE_AP_R2D_C_P
WIFI_EVENT_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_P
PCIE_AP_D2R_N

C3531, C3530: 0.1UF 10% 16V X5R-CERM 0201

C3532
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=J3501:1.5mm

Supervisor & CLKREQ# Isolation

Delay = 130 ms +/- 20%

APCLKRQ:ISOL
R3553 100K 5% 1/20W MF 201
R3554 232K 1% 1/20W MF 201

U3540
SLG4AP041V
TDFN
CRITICAL
VDD
SENSE
VREF
DLY
RESET*
MR*
EN
OUT (OD)
THRM PAD
GND

P3V3WLAN_VMON
AP_RESET_CONN_L → R3558 0 → AP_RESET_CONN_R_L
AP_CLKREQ_Q_L
R3555 100K 5% 1/20W MF 201

C3540
0.1UF
10%
6.3V
CERM-X5R
0201

SMC_WIFI_PWR_EN
AP_CLKREQ_R_L
AP_RESET_L

APCLKRQ:ISOL
R3556 0 5% 1/20W MF 0201

APCLKRQ:BIDIR
R3557 0 5% 1/20W MF 0201
AP_CLKREQ_L

NOSTUFF
R3559 0 5% 1/20W MF 0201

PCIe Wake Muxing

PP3V3_S5
R3561 100K 5% 1/20W MF 201
C3560 0.1UF 10% 6.3V CERM-X5R 0201
AP_PCIE_WAKE_L

U3560
NC7SB3157P6XG
SC70
VER-3
VCC
GND
S
B0
B1
A

SEL	OUTPUT
L	PCIE_WAKE_L (B0)
H	AP_S0IX_WAKE_L (B1)

AP_S0IX_WAKE_SEL
PCIE_WAKE_L
AP_S0IX_WAKE_L

NOSTUFF
R3560 0 5% 1/20W MF 0201

BLUETOOTH

PP3V3_S4

U3510
USB3740
DFN
CRITICAL
VDD
DP_2
DM_2
DP_1
DM_1
OE*
S
GND
DP
DM

C3510
0.1UF
10%
6.3V
CERM-X5R
0201

USB_BT_P
USB_BT_N
NC
BT_WAKE
PM_SLP_S4_L

SEL	OUTPUT
L	BT_WAKE (1)
H	USB_BT (2)

USB_BT_CONN_P
USB_BT_CONN_N
SIGNAL_MODEL=BT_MUX

NO_XNET_CONNECTION=TRUE
Q3510
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2

SMC_PME_S4_WAKE_L

R3512 15K 1% 1/20W MF 201

SYNC_MASTER=J43_MLB
SYNC_DATE=10/02/2012

PAGE TITLE
Wireless Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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OOB Isolation

PP3V3_S0SW_SSD

BYPASS=U3710:5 mm
C3718 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
74LVC1G08 SOT891
U3710 08
SMC_OOB1_R2D_L (IN)

NC

PP3V3_S0

BYPASS=U3711:5 mm
C3719 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
74LVC1G08 SOT891
U3711 08
SMC_OOB1_D2R_L (OUT)

NC

PLACE_NEAR=J3700.1:3mm
CRITICAL
L3700 FERR-26-OHM-6A 0603

PP3V3_S0SW_SSD
PP3V3_S0SW_SSD_FLT
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.15mm
VOLTAGE=3.3V

C3701 0.1UF 10% 10V X5R-CERM 0201
PLACE_NEAR=L3700.1:1mm

C3702 0.1UF 10% 10V X5R-CERM 0201
PLACE_NEAR=L3700.1:1mm

PP3V3_S0

R3710 100K 5% 1/20W MF 201
R3700 100K 5% 1/20W MF 201

514S0449
CRITICAL
J3700 SSD-GS3
F-RT-SM

GND_VOID	1	53	GND_VOID		
	2	52	SMC_OOB1_R2D_CONN_L		
	3	51	SMC_OOB1_D2R_CONN_L		
	4				
	5	50	SSD_PCIE_SEL_L	OUT	16 62
	6	49	SSD_DEVSLP	IN	15 62
PP3V3_S0	7	48	SMC_PWRFAIL_WARN_L	IN	35
SSD_RESET_CONN_L	8	47	SSD_PWR_EN	IN	15 30 56 57 62
NC_SSD_MFG_RSVD	9				
	10	46	SMC_PWRFAIL_WARN_L Signal has PU on SSD module		
PCIE_SSD_R2D_C_N<3> C3710 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE	11	45	PCIE_SSD_D2R_N<3>	OUT	12 62 65
PCIE_SSD_R2D_C_P<3> C3711 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE	12	44	PCIE_SSD_D2R_P<3>	OUT	12 62 65
PCIE_SSD_R2D_C_N<2> C3712 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE	14	42	PCIE_SSD_D2R_N<2>	OUT	12 62 65
PCIE_SSD_R2D_C_P<2> C3713 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE	15	41	PCIE_SSD_D2R_P<2>	OUT	12 62 65
PCIE_SSD_R2D_C_N<1> C3714 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE	18	38	PCIE_SSD_D2R_N<1>	OUT	12 62 65
PCIE_SSD_R2D_C_P<1> C3715 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE	19	37	PCIE_SSD_D2R_P<1>	OUT	12 62 65
PCIE_SSD_R2D_C_N<0> C3716 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE	21	35	PCIE_SSD_D2R_N<0>	OUT	12 62 65
PCIE_SSD_R2D_C_P<0> C3717 0.1UF 10% 16V X5R-CERM 0201 GND_VOID=TRUE	22	34	PCIE_SSD_D2R_P<0>	OUT	12 62 65
SSD_CLKREQ_CONN_L	24	33			
	25	32			
	26	31	PCIE_CLK100M_SSD_N	IN	12 62 65
	27	30	PCIE_CLK100M_SSD_P	IN	12 62 65
	28	29			
	54	59			
	55	60			
	56	61			
	57	62			
	58	63			

Per Intel PDG, use PCIe style decoupling, when muxing PCIe & SATA

PCIe polarity inversion and lane reversal are only permitted on the device side, provided the device PHY supports it.

Gumstick3 Connector

Supervisor & CLKREQ# Isolation

Delay = ~55ms

PP3V3_S0SW_SSD
PP3V42_G3H

R3740 100K 5% 1/20W MF 201
R3741 232K 1% 1/20W MF 201
R3742 100K 1% 1/20W MF 201

CRITICAL
C3740 0.1UF 10% 6.3V CERM-X5R 0201

U3740 SLG4AP016V TDFN

P3V3SSD_VMON
SENSE 0.7V
DLY
RESET*
MR*
EN
IN
OUT (OD)
THRM PAD
GND

SSD_RESET_L (IN 15)
SSD_PWR_EN (IN 15 30 56 57 62)
SSD_CLKREQ_L (OUT 12)

SYNC_MASTER=J43_MLB	SYNC_DATE=02/20/2013
PAGE TITLE	SSD Connector
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U3900 BCM15700 FBGA SYM 3 OF 3 CRITICAL OMIT_TABLE

U3900 BCM15700 FBGA SYM 2 OF 3 CRITICAL OMIT_TABLE

U3900 BCM15700 FBGA SYM 1 OF 3 CRITICAL OMIT_TABLE

SYNC_MASTER=J43_MLB1	SYNC_DATE=01/09/2013
PAGE TITLE	Camera 1 of 2
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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PP1V35_CAM

PP0V675_CAM_VREF

R4000 0 0201 5% 1/20W MF

PP0V675_MEM_CAM_VREFDQ
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.675V

PP0V675_MEM_CAM_VREFCA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.675V

R4022 1K 1% 1/20W MF 201
R4023 1K 1% 1/20W MF 201
R4002 1K 5% 1/20W MF 201
NOSTUFF R4003 1K 5% 1/20W MF 201

BYPASS=U4000.A1:4mm
C4002 10UF 20% 6.3V CERM-X5R 0402-1
C4003 10UF 20% 6.3V CERM-X5R 0402-1
BYPASS=U4000.B2:4mm
C4004 0.47UF 20% 6.3V CERM-X5R-1 201
C4005 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U4000.D2:4mm
C4006 2.2UF 20% 6.3V X5R-CERM 402
C4007 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U4000.K2:4mm
C4008 2.2UF 20% 6.3V X5R-CERM 402
C4009 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U4000.H9:4mm

C4010 0.1UF 10% 6.3V CERM-X5R 0201
C4011 0.1UF 10% 6.3V CERM-X5R 0201

U4000
4GB-DDR3-256MX16
FBGA
H5TC4G63AFR
CRITICAL

MEM_CAM_A<0>	N3	A0	
MEM_CAM_A<1>	P7	A1	
MEM_CAM_A<2>	P3	A2	
MEM_CAM_A<3>	N2	A3	
MEM_CAM_A<4>	P8	A4	
MEM_CAM_A<5>	P2	A5	
MEM_CAM_A<6>	R8	A6	
MEM_CAM_A<7>	R2	A7	
MEM_CAM_A<8>	T8	A8	
MEM_CAM_A<9>	R3	A9	
MEM_CAM_A<10>	L7	A10/AP	
MEM_CAM_A<11>	R7	A11	
MEM_CAM_A<12>	N7	A12/BC*	
MEM_CAM_A<13>	T3	A13	
MEM_CAM_A<14>	T7	A14	
MEM_CAM_BA<0>	M2	BA0	
MEM_CAM_BA<1>	N8	BA1	
MEM_CAM_BA<2>	M3	BA2	
MEM_CAM_RAS_L	J3	RAS*	
MEM_CAM_CAS_L	K3	CAS*	
MEM_CAM_WE_L	L3	WE*	
MEM_CAM_CLK_P	J7	CK	
MEM_CAM_CLK_N	K7	CK*	
MEM_CAM_CKE	K9	CKE	
MEM_CAM_CS_L	L2	CS*	
MEM_CAM_ODT	K1	ODT	
MEM_CAM_ZQ_DDR	L8	ZQ	
MEM_CAM_RESET_L	T2	RESET*	

MEM_CAM_DQ<0>	E3	DQL0	
MEM_CAM_DQ<1>	F7	DQL1	
MEM_CAM_DQ<2>	F2	DQL2	
MEM_CAM_DQ<3>	F8	DQL3	
MEM_CAM_DQ<4>	H3	DQL4	
MEM_CAM_DQ<5>	H8	DQL5	
MEM_CAM_DQ<6>	G2	DQL6	
MEM_CAM_DQ<7>	H7	DQL7	
MEM_CAM_DQS_P<0>	F3	DQSL	
MEM_CAM_DQS_N<0>	G3	DQSL*	
MEM_CAM_DQS_P<1>	C7	DQSU	
MEM_CAM_DQS_N<1>	B7	DQSU*	
MEM_CAM_DQ<8>	D7	DQU0	
MEM_CAM_DQ<9>	C3	DQU1	
MEM_CAM_DQ<10>	C8	DQU2	
MEM_CAM_DQ<11>	C2	DQU3	
MEM_CAM_DQ<12>	A7	DQU4	
MEM_CAM_DQ<13>	A2	DQU5	
MEM_CAM_DQ<14>	B8	DQU6	
MEM_CAM_DQ<15>	A3	DQU7	
MEM_CAM_DM<0>	E7	DML	
MEM_CAM_DM<1>	D3	DMU	

VDDQ A1 A8 C1 C9 D2 D9 E1 E9 F1 H2 H9
VDD B2 D9 G7 K2 K8 M1 N1 N9 R1 R9 M8
VREFCA H1
VREFDQ J1
NC J9 L1 L9 M7
VSSQ B1 B9 D1 D8 E2 E8 F9 G1 G9
VSS A9 B3 E1 G8 J2 J8 M1 M9 P1 P9 T1 T9

R4020 84.5 1% 1/20W MF 201
R4021 82 1% 1/20W MF 201 NO STUFF
MEM_CAM_CKE_R
R4006 100PF 5% 25V NP0-CERM 0201 NO STUFF
R4004 240 1% 1/20W MF 201

PCIE_CAMERA_R2D_C_P C4033 0.1UF 10% 10V X5R-CERM 0201 PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D_C_N C4032 0.1UF 10% 10V X5R-CERM 0201 PCIE_CAMERA_R2D_N
PCIE_CAMERA_D2R_C_P C4031 0.1UF 10% 10V X5R-CERM 0201 PCIE_CAMERA_D2R_P
PCIE_CAMERA_D2R_C_N C4030 0.1UF 10% 10V X5R-CERM 0201 PCIE_CAMERA_D2R_N
PCIE_CLK100M_CAMERA_P C4061 0.1UF 10% 10V X5R-CERM 0201 PCIE_CLK100M_CAMERA_C_P
PCIE_CLK100M_CAMERA_N C4062 0.1UF 10% 10V X5R-CERM 0201 PCIE_CLK100M_CAMERA_C_N

SYSCLK_CLK25M_CAMERA
R4008 0 0201 5% 1/20W MF CAM_XTAL:NO
CLK25M_CAM_CLKP

C4015 12PF 5% 25V NP0-C0G-CERM 0201 CAM_XTAL:YES
CLK25M_CAM_XTALP
CRITICAL
Y4000 SM-3.2X2.5MM 25.000MHZ-12PF-20PPM CAM_XTAL:YES
CLK25M_CAM_XTALN
C4014 12PF 5% 25V NP0-C0G-CERM 0201 CAM_XTAL:YES
R4007 0 0201 5% 1/20W MF CAM_XTAL:YES
R4012 1M 1% 1/20W MF 201 NOSTUFF
R4009 0 0201 5% 1/20W MF CAM_XTAL:YES
CLK25M_CAM_XTALP_R
R4010 0 0201 5% 1/20W MF CAM_XTAL:YES
CLK25M_CAM_CLKN
C4016 100PF 5% 25V NP0-CERM 0201 CAM_XTAL:NO

NOTE: TBD PPM crystal required

PP1V8_CAM
R4005 100K 5% 1/20W MF 201
CAM_WAKE:YES
R4030 0 0201 5% 1/20W MF
CAM_SENSOR_WAKE_L_CONN
CAM_SENSOR_WAKE_L
CAM_WAKE:NO
R4031 0 5% 1/20W MF 0201

CAMERA SENSOR

CRITICAL
J4002
CCR20-AK7100-1
F-RT-SM

1		
2	MIPI_CLK_CONN_N	
3	MIPI_CLK_CONN_P	
4	CAM_SENSOR_WAKE_L_CONN	
5	MIPI_DATA_CONN_N	
6	MIPI_DATA_CONN_P	
7		
8	SMBUS_SMC_1_S0_SDA	
9	SMBUS_SMC_1_S0_SCL	
10	I2C_CAM_SCK	
11	I2C_CAM_SDA	
12	PP5V_S3RS0_ALSCAM_F	MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=5V
13		
14		

518S0892

ALS

L4009 90-OHM-50MA TCM0605-1
MIPI_CLK_N
MIPI_CLK_P
PLACE_NEAR=J4002.2:2.54MM
CRITICAL

L4007 90-OHM-50MA TCM0605-1
MIPI_DATA_N
MIPI_DATA_P
PLACE_NEAR=J4002.5:2.54MM
CRITICAL

L4010 FERR-120-OHM-1.5A 0402-LF
PP5V_S0
C4013 0.1UF 10% 10V CERM 402
NOSTUFF
L4011 FERR-120-OHM-1.5A 0402-LF
PP5V_S4RS3

77.2 mA nominal max
96.2 mA peak

SYNC_MASTER=J43_MLB
SYNC_DATE=09/14/2012
PAGE TITLE: Camera 2 of 2
Apple Inc.
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SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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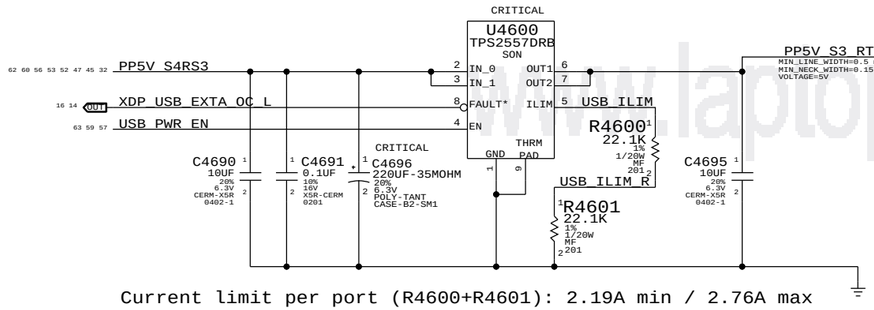
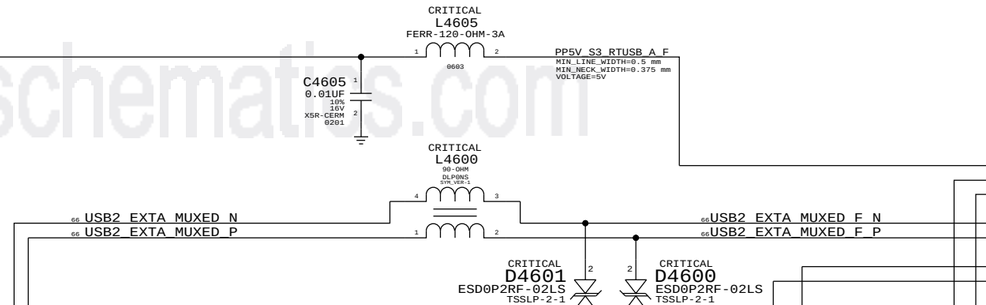
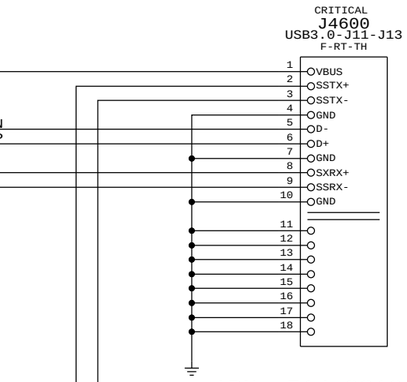
Right USB Port A

USB Port Power Switch



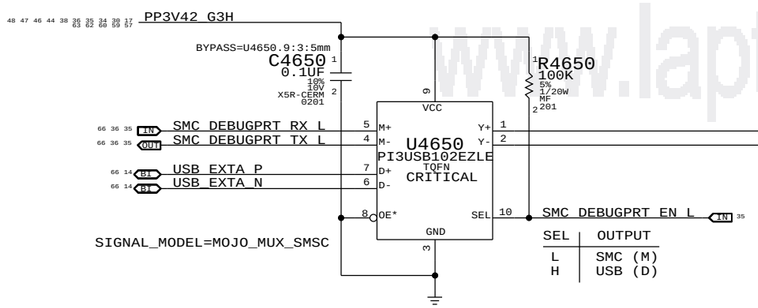
Current limit per port (R4600+R4601): 2.19A min / 2.76A max



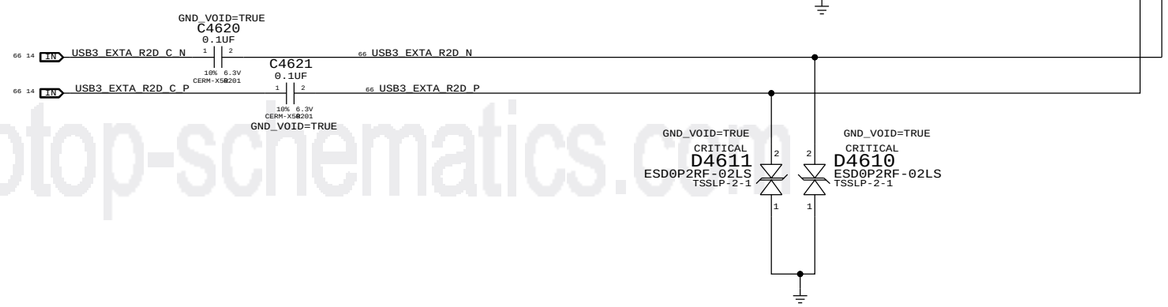


APN: 514-0819

Mojo SMC Debug Mux



SEL	OUTPUT
L	SMC (M)
H	USB (D)



SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE: External A USB3 Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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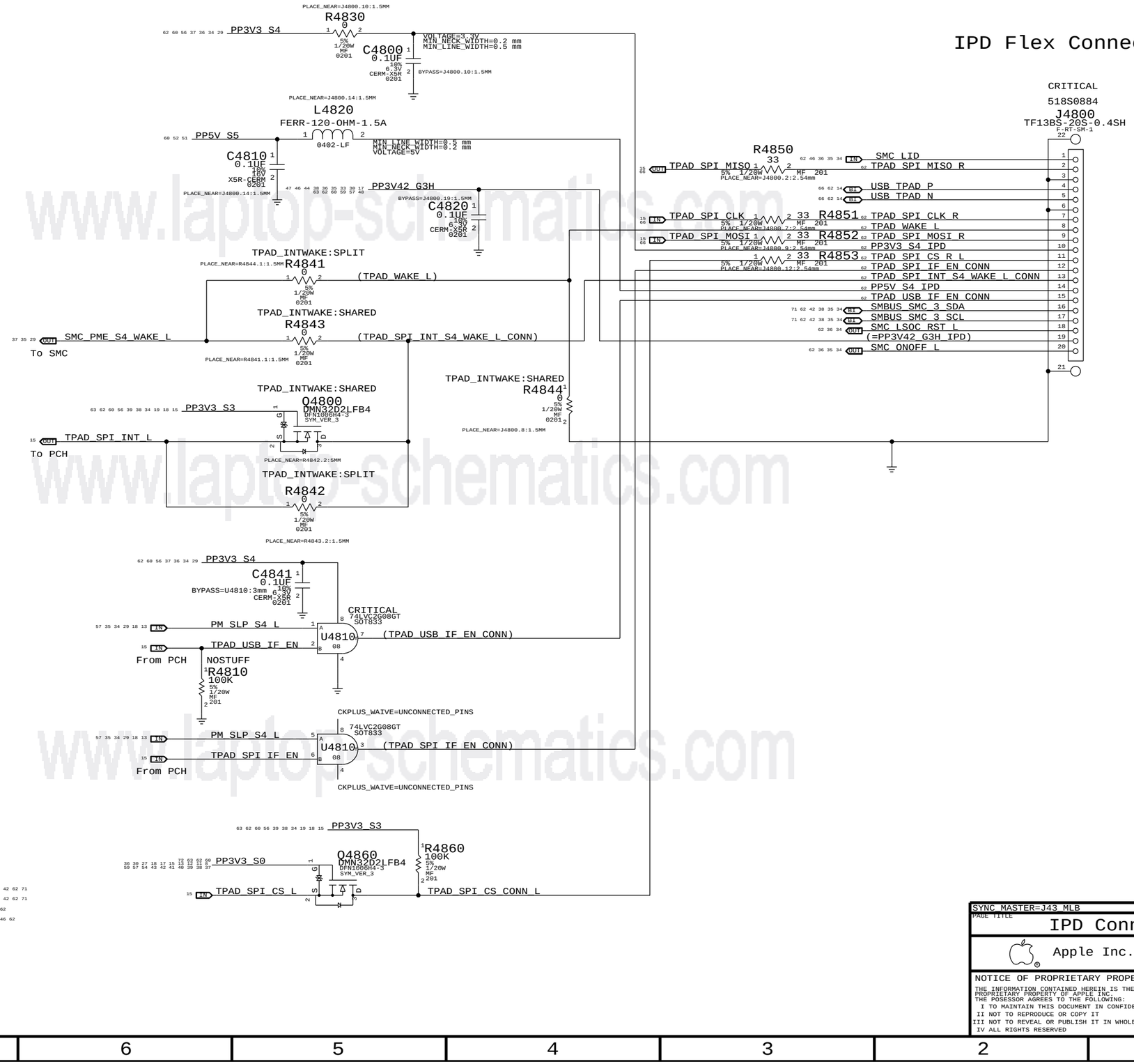
IPD Flex Connector



SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013

PAGE TITLE: IPD Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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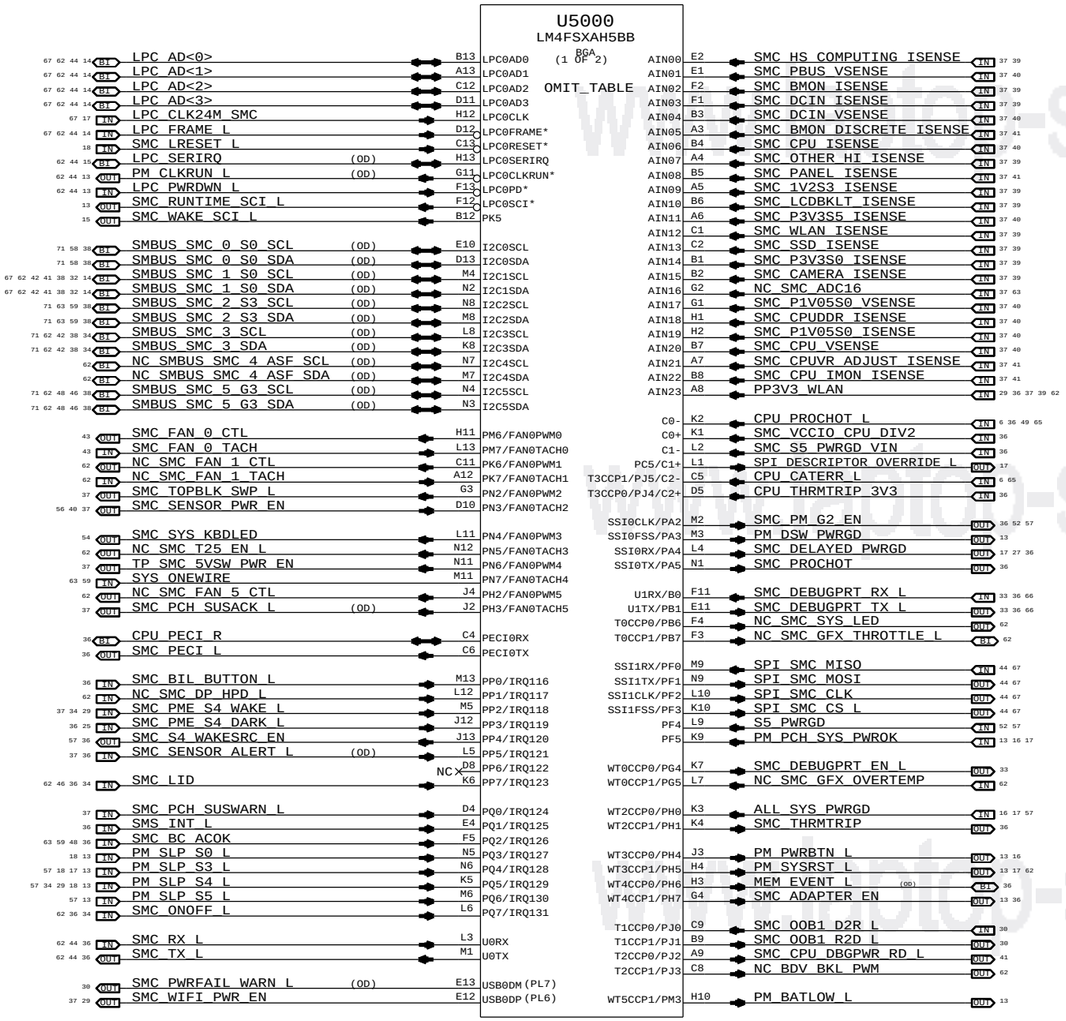

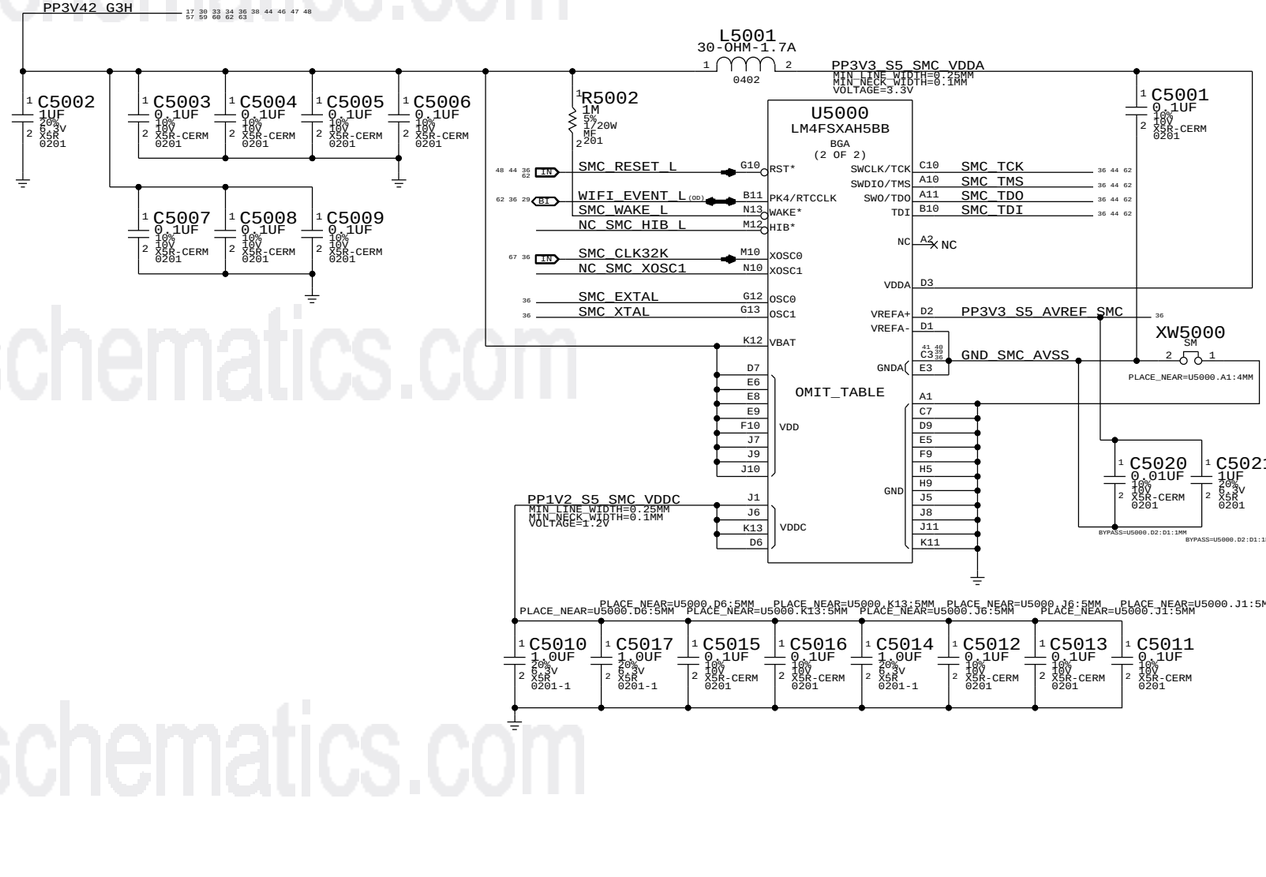

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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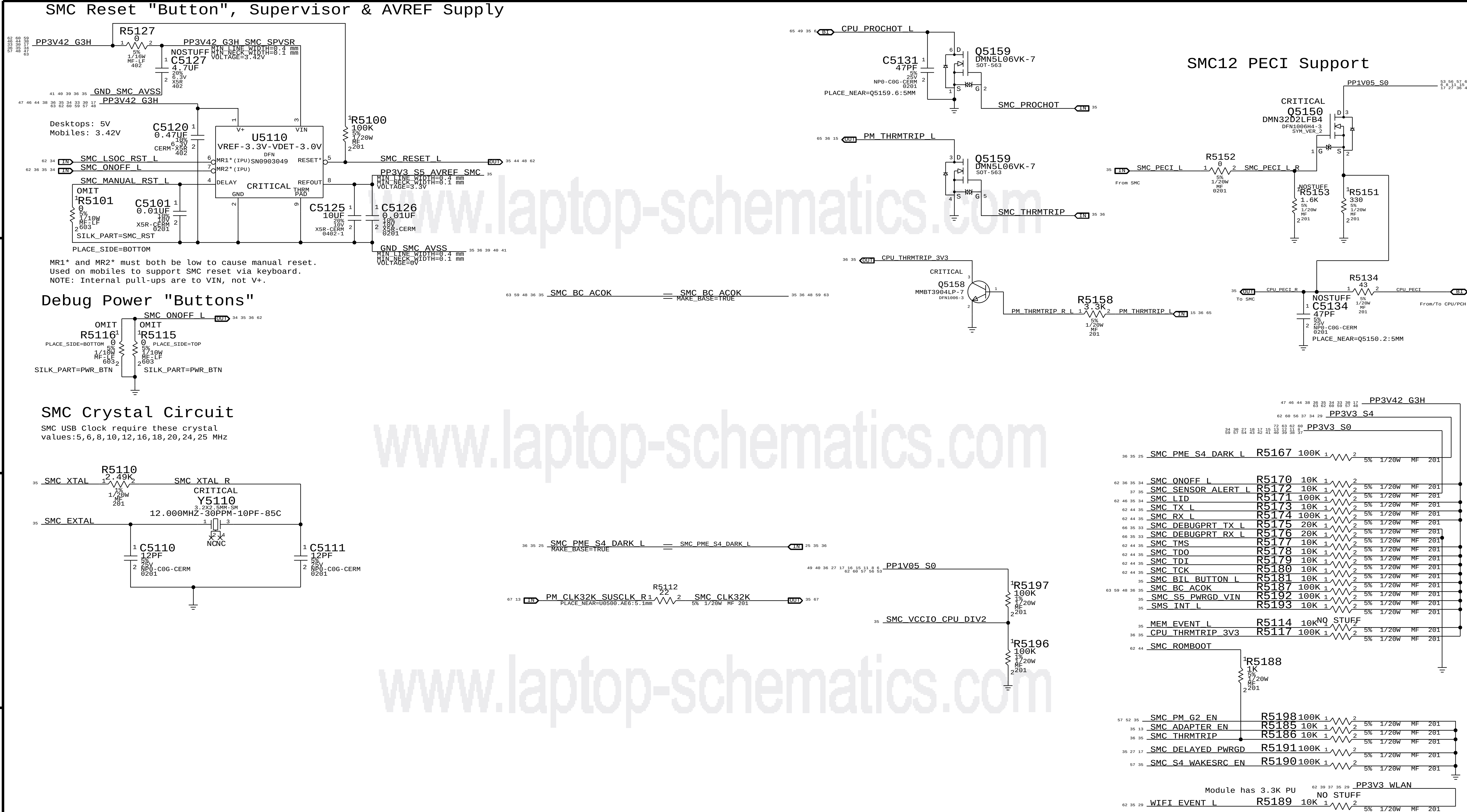
SMC Reset "Button", Supervisor & AVREF Supply
PP3V42_G3H
R5127
PP3V42_G3H_SMC_SPVSR
NOSTUFF
C5127
4.7UF
GND_SMC_AVSS
Desktops: 5V
Mobiles: 3.42V
C5120
0.47UF
U5110
VREF-3.3V-VDET-3.0V
SN0903049
CRITICAL
R5100
100K
SMC_LSOC_RST_L
SMC_ONOFF_L
SMC_MANUAL_RST_L
SMC_RESET_L
PP3V3_S5_AVREF_SMC
OMIT
R5101
C5101
0.01UF
SILK_PART=SMC_RST
PLACE_SIDE=BOTTOM
C5125
10UF
C5126
0.01UF
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.
Debug Power "Buttons"
R5116
R5115
SILK_PART=PWR_BTN
SMC Crystal Circuit
SMC USB Clock require these crystal
values:5,6,8,10,12,16,18,20,24,25 MHz
SMC_XTAL
R5110
2.49K
SMC_XTAL_R
CRITICAL
Y5110
12.000MHZ-30PPM-10PF-85C
SMC_EXTAL
C5110
12PF
C5111
12PF
SMC_BC_ACOK
SMC_PME_S4_DARK_L
PM_CLK32K_SUSCLK_R
R5112
22
SMC_CLK32K
CPU_PROCHOT_L
C5131
47PF
Q5159
DMN5L06VK-7
SMC_PROCHOT
PM_THRMTRIP_L
SMC_THRMTRIP
CPU_THRMTRIP_3V3
Q5158
MMBT3904LP-7
R5158
3.3K
PM_THRMTRIP_R_L
PP1V05_S0
R5197
100K
SMC_VCCIO_CPU_DIV2
R5196
100K
SMC12 PECI Support
PP1V05_S0
CRITICAL
Q5150
DMN32D2LFB4
SMC_PECI_L
R5152
SMC_PECI_L_R
R5153
1.6K
R5151
330
CPU_PECI_R
R5134
43
CPU_PECI
C5134
47PF
PLACE_NEAR=Q5150.2:5MM
PP3V42_G3H
PP3V3_S4
PP3V3_S0
SMC_PME_S4_DARK_L R5167 100K
SMC_ONOFF_L R5170 10K
SMC_SENSOR_ALERT_L R5172 10K
SMC_LID R5171 100K
SMC_TX_L R5173 10K
SMC_RX_L R5174 100K
SMC_DEBUGPRT_TX_L R5175 20K
SMC_DEBUGPRT_RX_L R5176 20K
SMC_TMS R5177 10K
SMC_TDO R5178 10K
SMC_TDI R5179 10K
SMC_TCK R5180 10K
SMC_BIL_BUTTON_L R5181 10K
SMC_BC_ACOK R5187 100K
SMC_S5_PWRGD_VIN R5192 100K
SMS_INT_L R5193 10K
MEM_EVENT_L R5114 10K NO STUFF
CPU_THRMTRIP_3V3 R5117 100K
SMC_ROMBOOT
R5188
1K
SMC_PM_G2_EN R5198 100K
SMC_ADAPTER_EN R5185 10K
SMC_THRMTRIP R5186 10K
SMC_DELAYED_PWRGD R5191 100K
SMC_S4_WAKESRC_EN R5190 100K
Module has 3.3K PU
PP3V3_WLAN
NO STUFF
WIFI_EVENT_L R5189 10K

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE

SMC Shared Support

Apple Inc.

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BRANCH <BRANCH>

39 37 35 SMC_HS_COMPUTING_ISENSE — SMC_HS_COMPUTING_ISENSE 35 37 39
40 37 35 SMC_PBUS_VSENSE — SMC_PBUS_VSENSE 35 37 40
39 37 35 SMC_BMON_ISENSE — SMC_BMON_ISENSE 35 37 39
39 37 35 SMC_DCIN_ISENSE — SMC_DCIN_ISENSE 35 37 39
40 37 35 SMC_DCIN_VSENSE — SMC_DCIN_VSENSE 35 37 40
41 37 35 SMC_BMON_DISCRETE_ISENSE — SMC_BMON_DISCRETE_ISENSE 35 37 41
40 37 35 SMC_CPU_ISENSE — SMC_CPU_ISENSE 35 37 40
39 37 35 SMC_OTHER_HI_ISENSE — SMC_OTHER_HI_ISENSE 35 37 39
41 37 35 SMC_PANEL_ISENSE — SMC_PANEL_ISENSE 35 37 41
39 37 35 SMC_1V2S3_ISENSE — SMC_1V2S3_ISENSE 35 37 39
39 37 35 SMC_LCDBKLT_ISENSE — SMC_LCDBKLT_ISENSE 35 37 39
40 37 35 SMC_P3V3S5_ISENSE — SMC_P3V3S5_ISENSE 35 37 40
39 37 35 SMC_WLAN_ISENSE — SMC_WLAN_ISENSE 35 37 39
39 37 35 SMC_SSD_ISENSE — SMC_SSD_ISENSE 35 37 39
39 37 35 SMC_P3V3S0_ISENSE — SMC_P3V3S0_ISENSE 35 37 39
39 37 35 SMC_CAMERA_ISENSE — SMC_CAMERA_ISENSE 35 37 39
NC_SMC_ADC16 OUT 35 63 SD alias on page 103
40 37 35 SMC_P1V05S0_VSENSE — SMC_P1V05S0_VSENSE 35 37 40
40 37 35 SMC_CPUDDR_ISENSE — SMC_CPUDDR_ISENSE 35 37 40
40 37 35 SMC_P1V05S0_ISENSE — SMC_P1V05S0_ISENSE 35 37 40
40 37 35 SMC_CPU_VSENSE — SMC_CPU_VSENSE 35 37 40
41 37 35 SMC_CPUVR_ADJUST_ISENSE — SMC_CPUVR_ADJUST_ISENSE 35 37 41
41 37 35 SMC_CPU_IMON_ISENSE — SMC_CPU_IMON_ISENSE 35 37 41
62 39 37 36 35 29 PP3V3_WLAN — PP3V3_WLAN 29 35 36 37 39 62

MAKE_BASE=TRUE

56 40 37 35 SMC_SENSOR_PWR_EN — SMC_SENSOR_PWR_EN 35 37 40 56
37 35 29 SMC_WIFI_PWR_EN — SMC_WIFI_PWR_EN 29 35 37
37 35 TP_SMC_5VSW_PWR_EN — TP_SMC_5VSW_PWR_EN 35 37

R5230 0 5% 1/20W MF 0201

35 IN SMC_PCH_SUSWARN_L — PCH_SUSWARN_L OUT 13

R5231 0 5% 1/20W MF 0201

35 OUT SMC_PCH_SUSACK_L — PCH_SUSACK_L IN 13

Top-Block Swap

PP3V3_S0 62 63 72 8 11 12 13 15 17 18 27 30 34 36 38 39 40 41 42 43 54 57 59 60

R5296 1K 5% 1/20W MF 201

R5283 1K 5% 1/20W MF 201

35 IN SMC_TOPBLK_SWP_L — PCH_STRP_TOPBLK_SWP_L OUT 15

62 60 56 37 36 34 29 PP3V3_S4

37 35 29 SMC_WIFI_PWR_EN — R5295 10K 5% 1/20W MF 201 — NOSTUFF

56 40 37 35 SMC_SENSOR_PWR_EN — R5294 10K 5% 1/20W MF 201 — NOSTUFF

PP3V3_S4 29 34 36 37 56 60 62

R5282 100K 5% 1/20W MF 201

35 34 29 37 IN SMC_PME_S4_WAKE_L

35 34 29 37 IN SMC_PME_S4_WAKE_L — SMC_PME_S4_WAKE_L OUT 29 34 35 37

MAKE_BASE=TRUE

41 IN SMC_HS_COMP_ALERT_L — R5216 100 5% 1/20W MF 201

14 IN PCH_SML1ALERT_L — R5215 100 5% 1/20W MF 201 — NOSTUFF

41 IN SMC_BMON_COMP_ALERT_L — R5213 100 5% 1/20W MF 201

63 59 IN FINSTACKSNS_ALERT_L — R5210 100 5% 1/20W MF 201 — NOSTUFF

42 IN CPUTHMSNS_ALERT_L — R5214 100 5% 1/20W MF 201

42 IN CPUBMONSNS_ALERT_L — R5211 100 5% 1/20W MF 201 — NOSTUFF

42 IN TBTMLBSNS_ALERT_L — R5212 100 5% 1/20W MF 201 — SMC_SENSOR_ALERT_L OUT 35 36

SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE

SMC Project Support

Apple Inc.

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REVISION <E4LABEL>

BRANCH <BRANCH>

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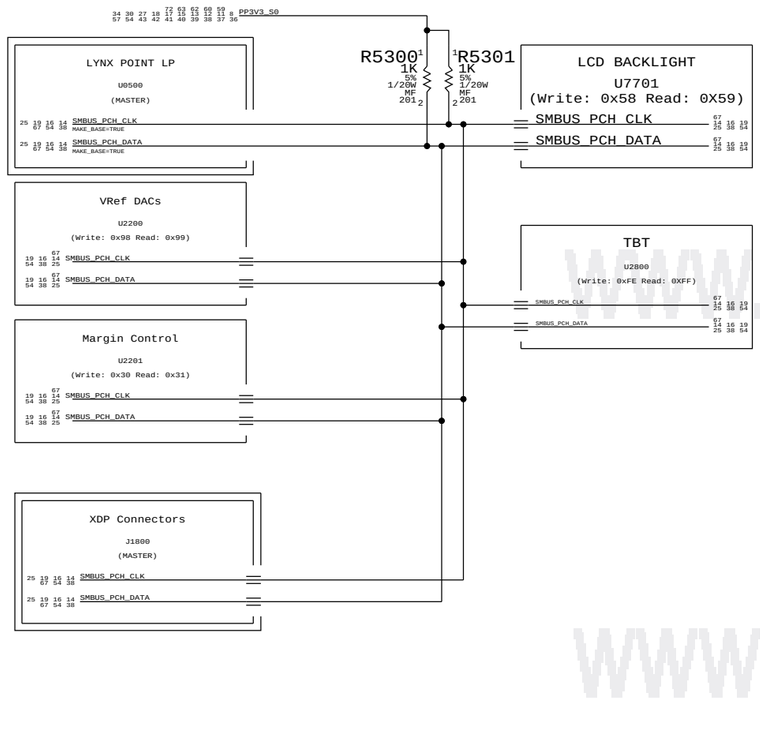
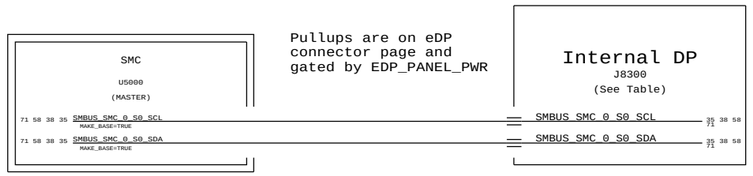
LYNX POINT LP S0 SMBus "0" Connections



SMC "0" SMBus S0 Connections

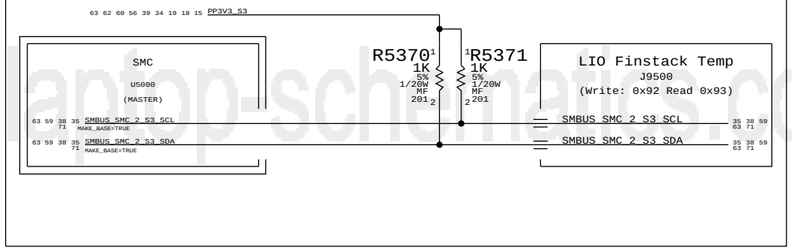


(* = Multiple options)

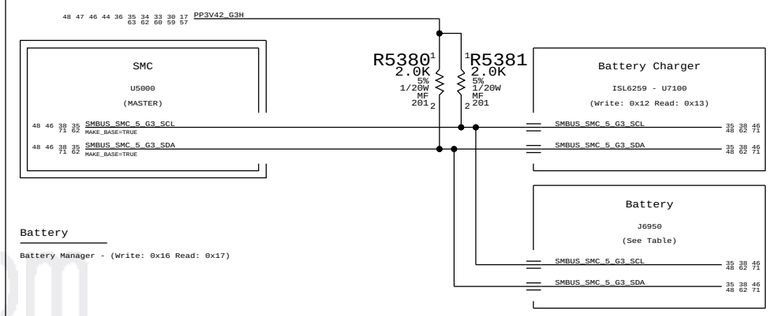
Internal DP

	J43		J41		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

SMC "2" SMBus S3 Connections



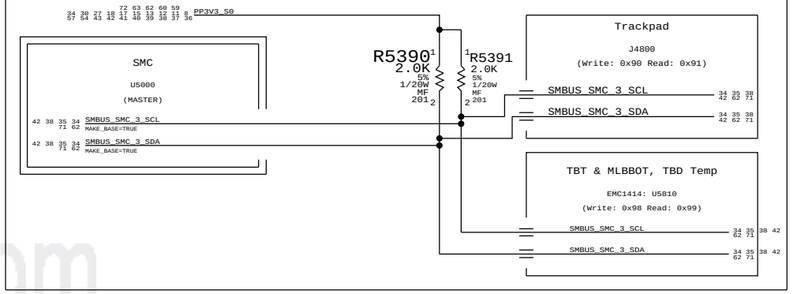
SMC "5" SMBus G3H Connections



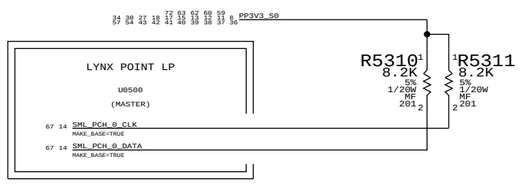
Battery

Battery Manager - (Write: 0x16 Read: 0x17)

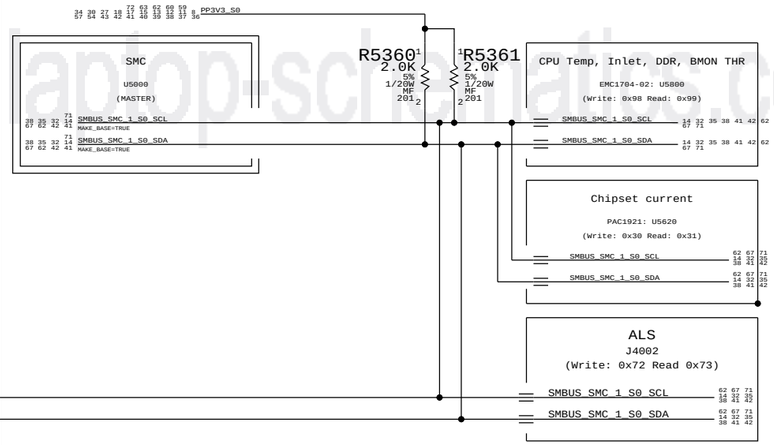
SMC "3" SMBus S0 Connections



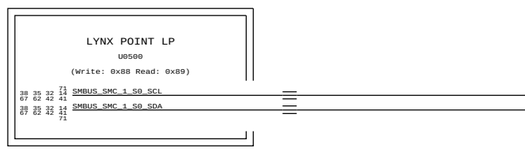
LYNX POINT LP S0 "SMLink 0" Connections



SMC S0 "1" SMBus Connections



LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to
access PCH

SYNC_MASTER=J43_MLB SYNC_DATE=09/28/2012

PAGE TITLE: SMBus Connections

Apple Inc.

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REVISION: <E4LABEL>
BRANCH: <BRANCH>
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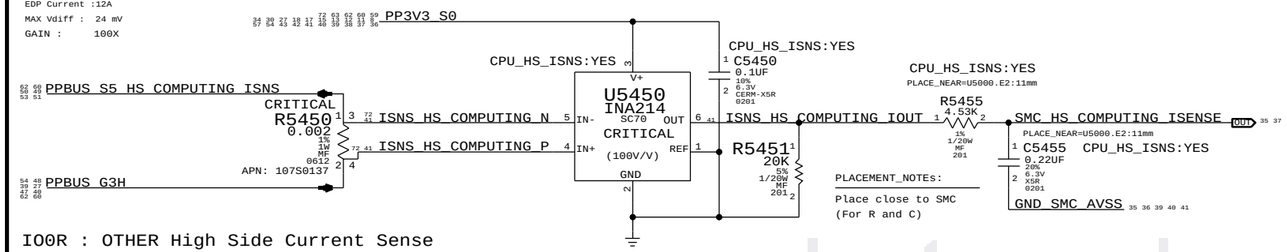
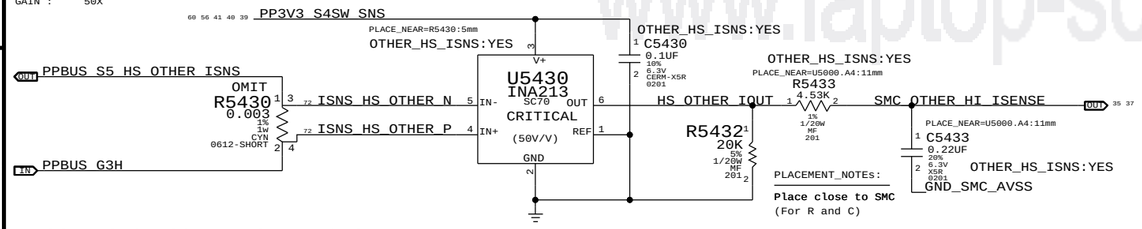
IC0R : COMPUTING High Side Current Sense

EDP Current :12A
MAX Vdiff : 24 mV
GAIN : 100X



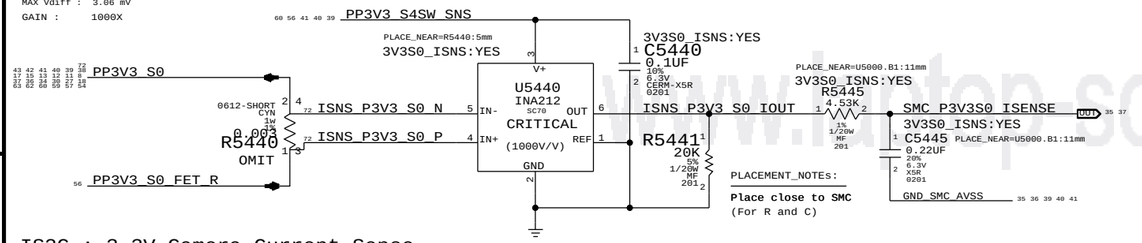
IO0R : OTHER High Side Current Sense

EDP Current :10.75A
MAX Vdiff : 53.75 mV
GAIN : 50X



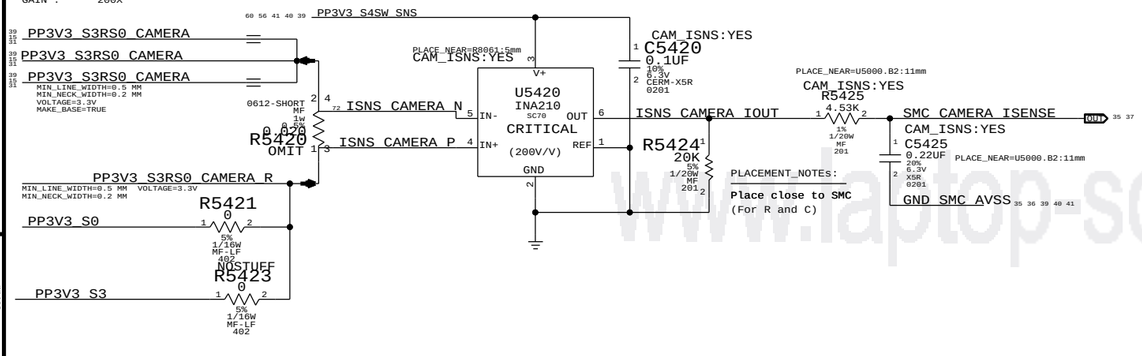
IR0C : 3.3V S0 FET Current Sense

EDP Current :1.02A
MAX Vdiff : 3.06 mV
GAIN : 1000X

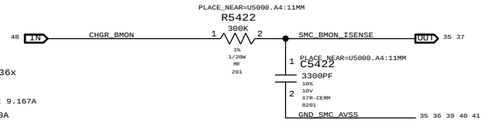


IS2C : 3.3V Camera Current Sense

EDP Current : 0.82A
MAX Vdiff : 16.36 mV
GAIN : 200X

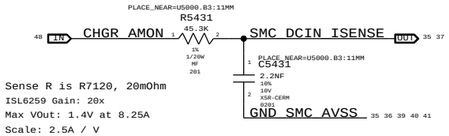


CHARGER BMON High Side Current Sense



ISL6259 Gain: 36x
Scale: 2.78A / V
Max VOut: 3.3V at 9.167A
EDP Current: 310A

DC-IN (AMON) Current Sense

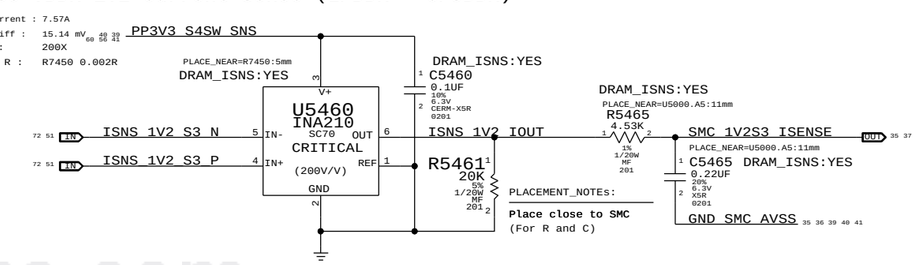


Sense R is R7120, 20mOhm
ISL6259 Gain: 20x
Max VOut: 1.4V at 8.25A
Scale: 2.5A / V
EDP Current: 3.5A

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES,SENSE,0.003OHM,1W,4-TERM,1%,0612,TFT	R5480	CRITICAL	

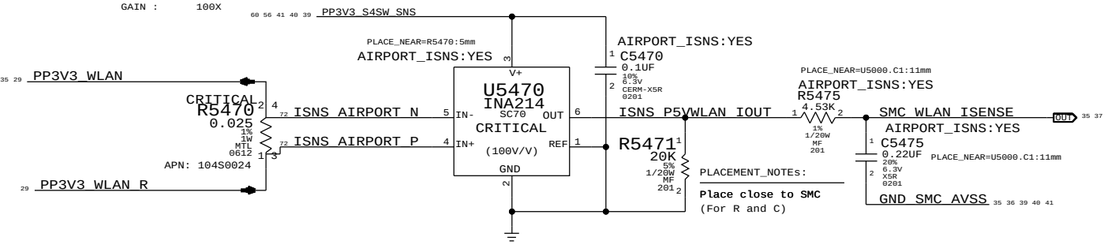
IM3C :DDR 1V2 Current Sense (LPDDR + CPUDDR)

EDP Current : 7.57A
MAX Vdiff : 15.14 mV
GAIN : 200X
SENSE R : R7450 0.002R



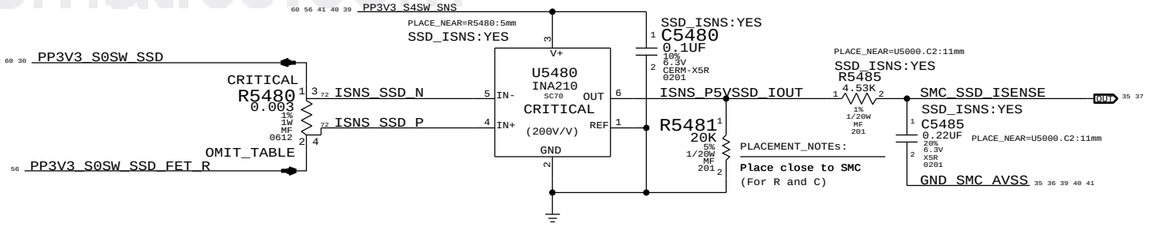
IAPC :AirPort Current Sense

EDP Current : 1.00A
MAX Vdiff : 25 mV
GAIN : 100X



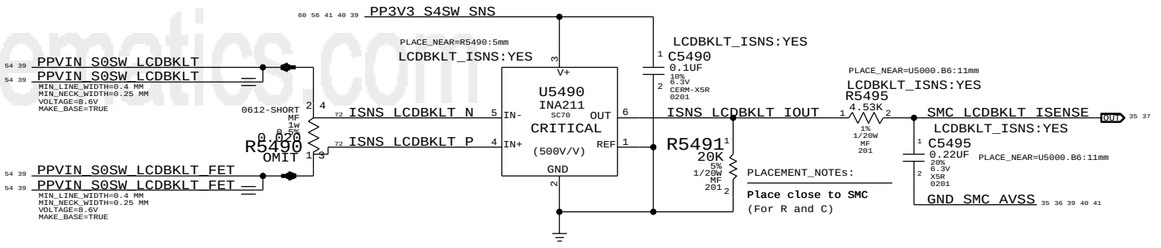
ISDC : SSD Current Sense

EDP Current : 3.00A
MAX Vdiff : 15 mV
GAIN : 200X



IBLC : LCD Backlight Driver Input Current Sense

EDP Current : 0.67A
MAX Vdiff : 0.06 mV
GAIN : 500X



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		SSD_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5433		OTHER_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5425		CAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

SYNC_MASTER=SID J41 SYNC_DATE=02/26/2013
PAGE TITLE
High Side Current Sensing

Apple Inc.

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BRANCH <BRANCH>
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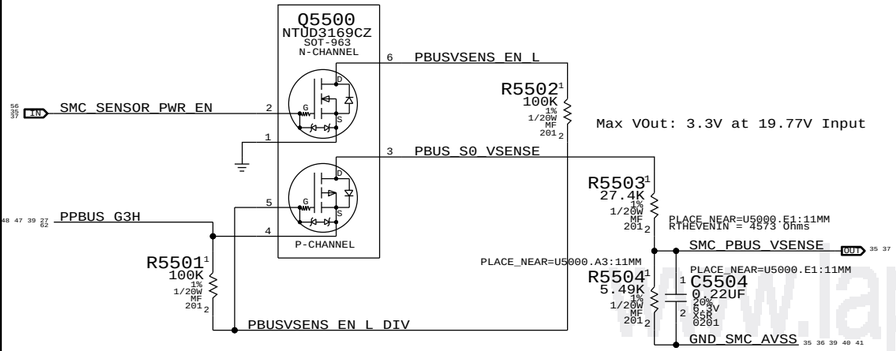
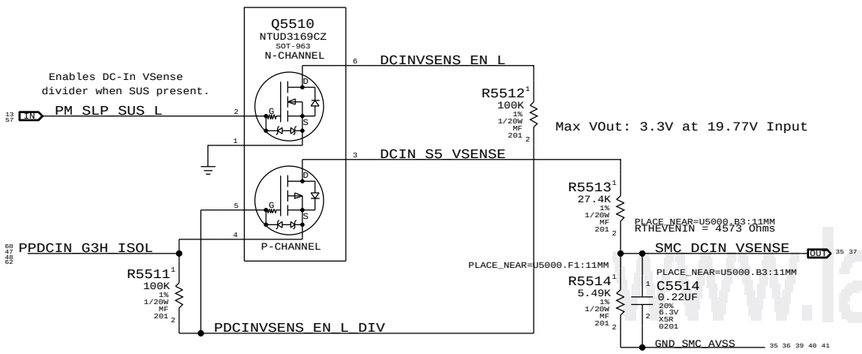
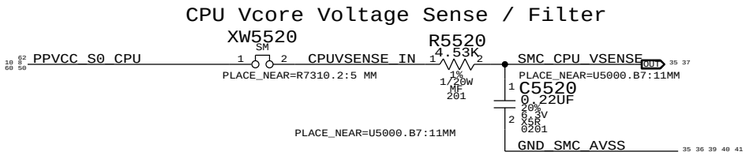
VP0R: PBUS Voltage Sense Enable & Filter



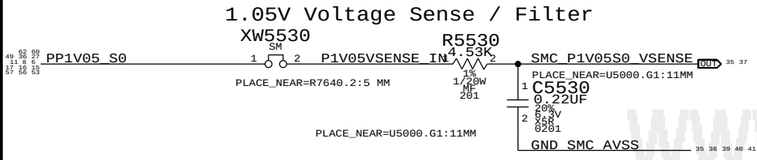
VD0R: DC-In Voltage Sense Enable & Filter



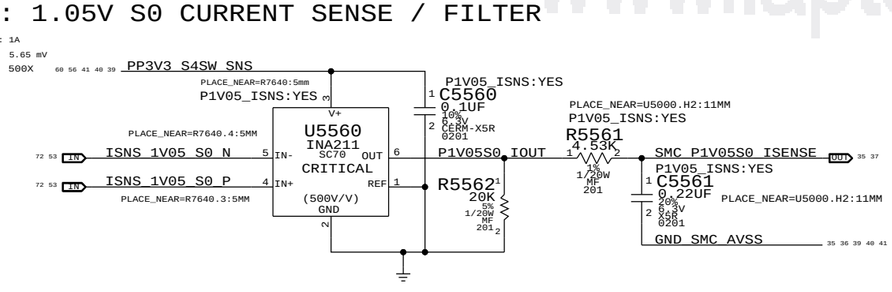
CPU Vcore Voltage Sense / Filter



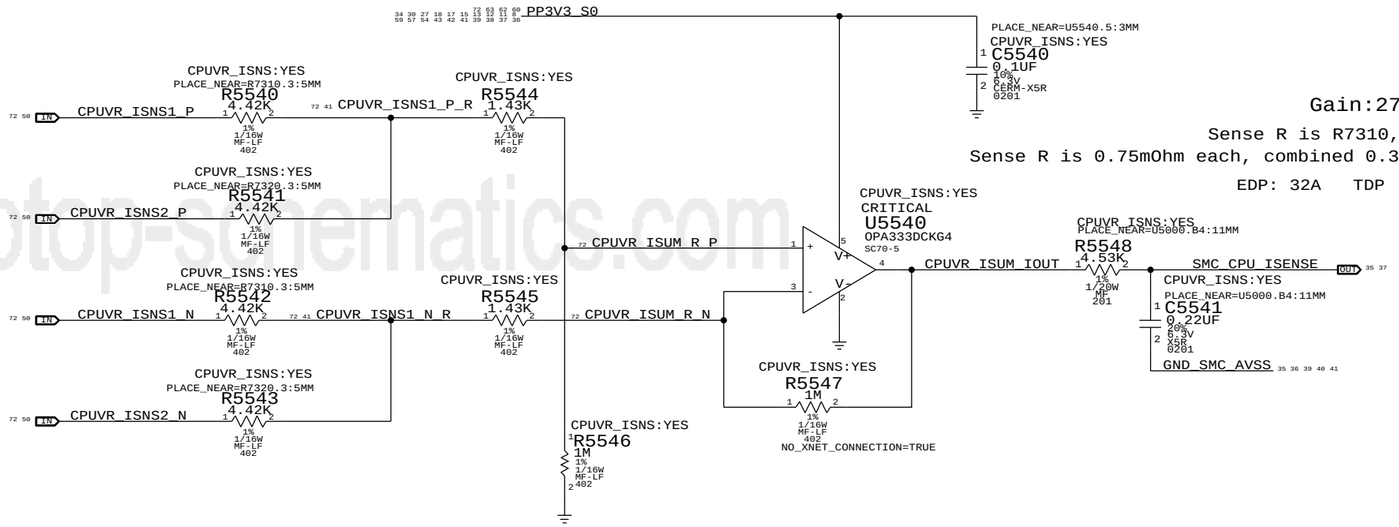
1.05V Voltage Sense / Filter



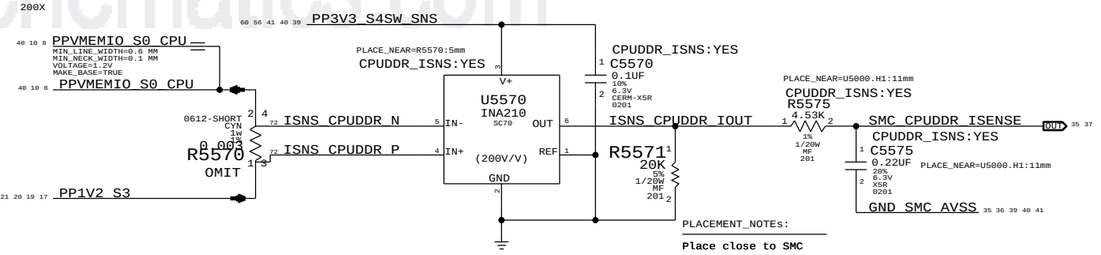
IC1C: 1.05V S0 CURRENT SENSE / FILTER



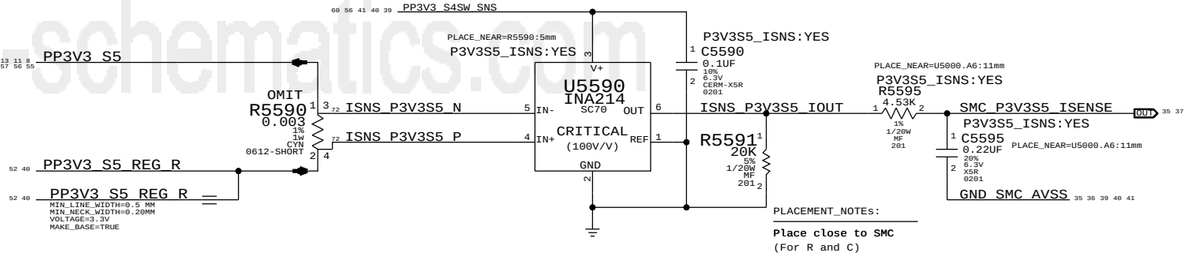
ICS0 : CPU VCore Load Side Current Sense



IM0C : CPU DDR Current Sense



IR5C :3.3 S5 REG Current Sense



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5541		CPUVR_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5561		P1V05_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5595		P3V3S5_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5575		CPUDDR_ISNS:NO

SYNC_MASTER=SID_J41 SYNC_DATE=02/26/2013

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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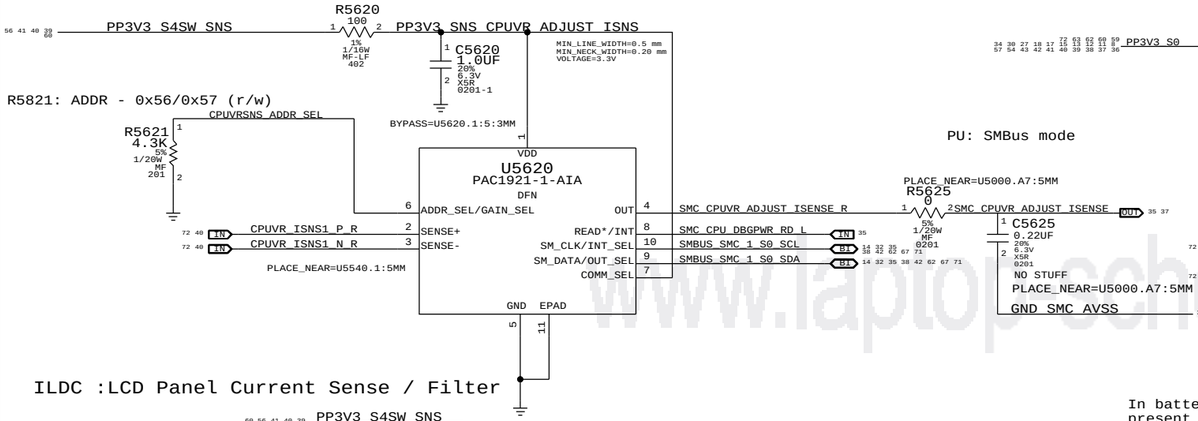
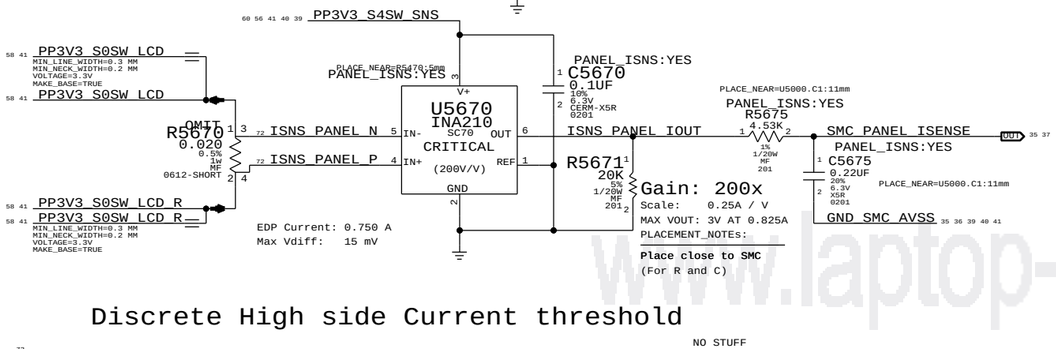
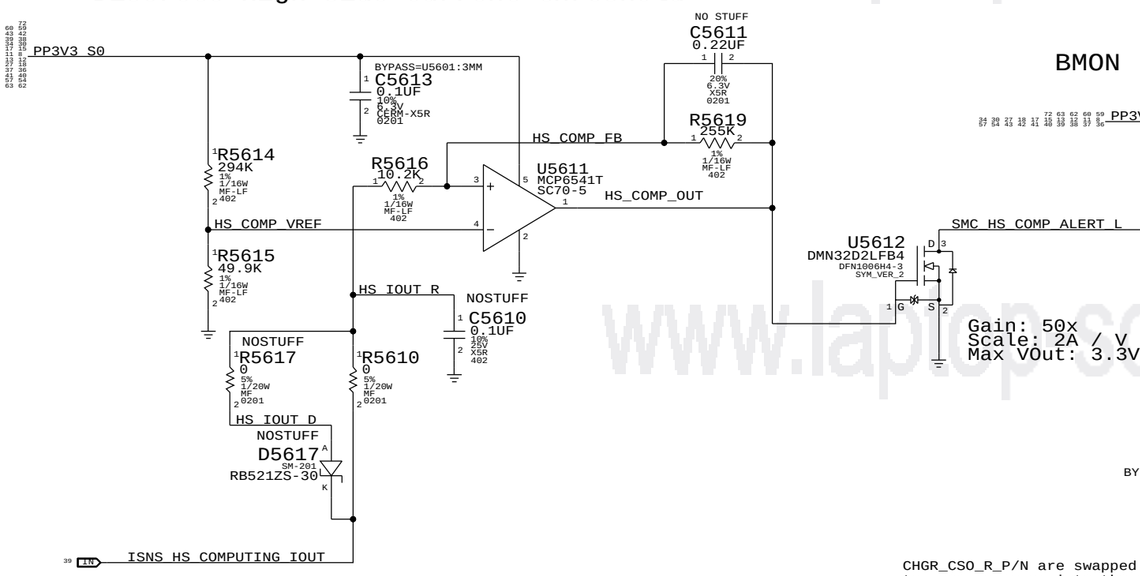
ICS3 : Adjustable Gain CPU VR Current



ILDC :LCD Panel Current Sense / Filter



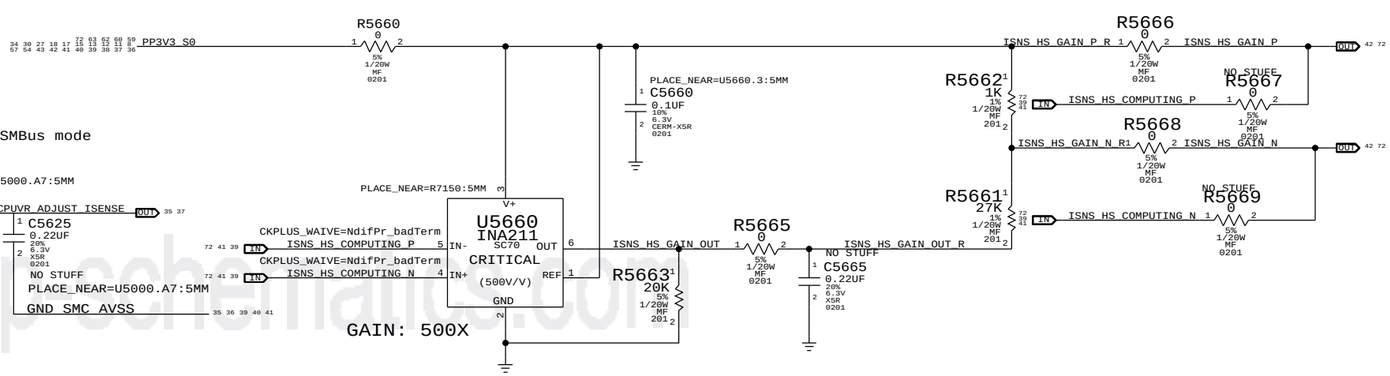
Discrete High side Current threshold



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5675		PANEL_ISNS:NO

Sense Pins gain stage for U5800 (EMC1704)

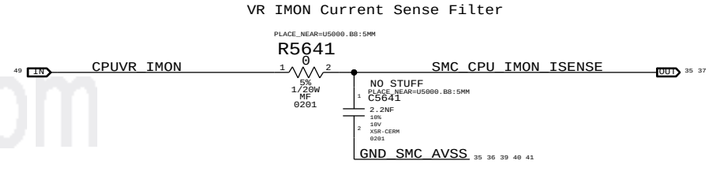


GAIN: 500X

In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

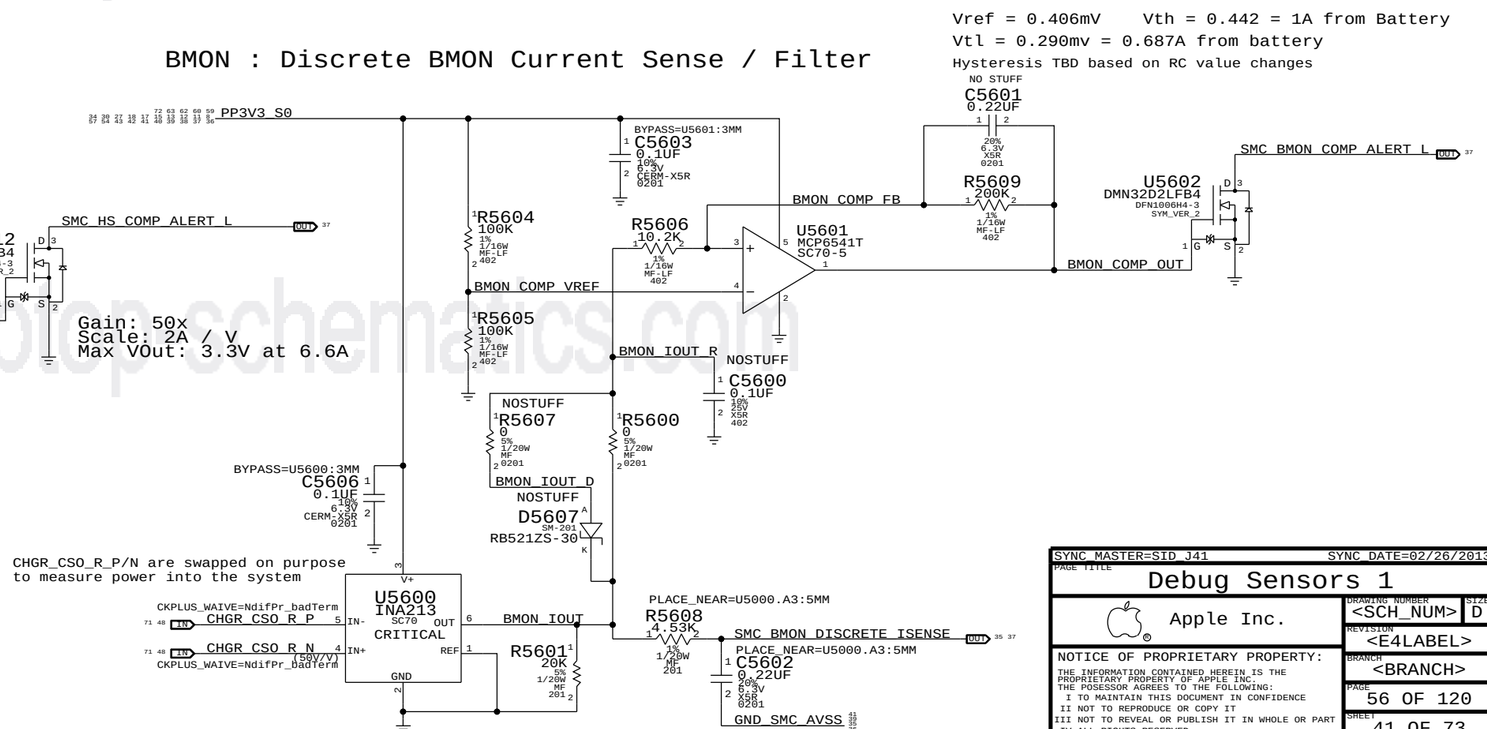
With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800.
This will set the minumum current threshold at 0.100mA

VR IMON Current Sense Filter



Vref = 0.406mV Vth = 0.442 = 1A from Battery
Vtl = 0.290mv = 0.687A from battery
Hysteresis TBD based on RC value changes

BMON : Discrete BMON Current Sense / Filter



Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

CHGR_CSO_R_P/N are swapped on purpose to measure power into the system

SYNC_MASTER=SID_J41 SYNC_DATE=02/26/2013

PAGE TITLE: Debug Sensors 1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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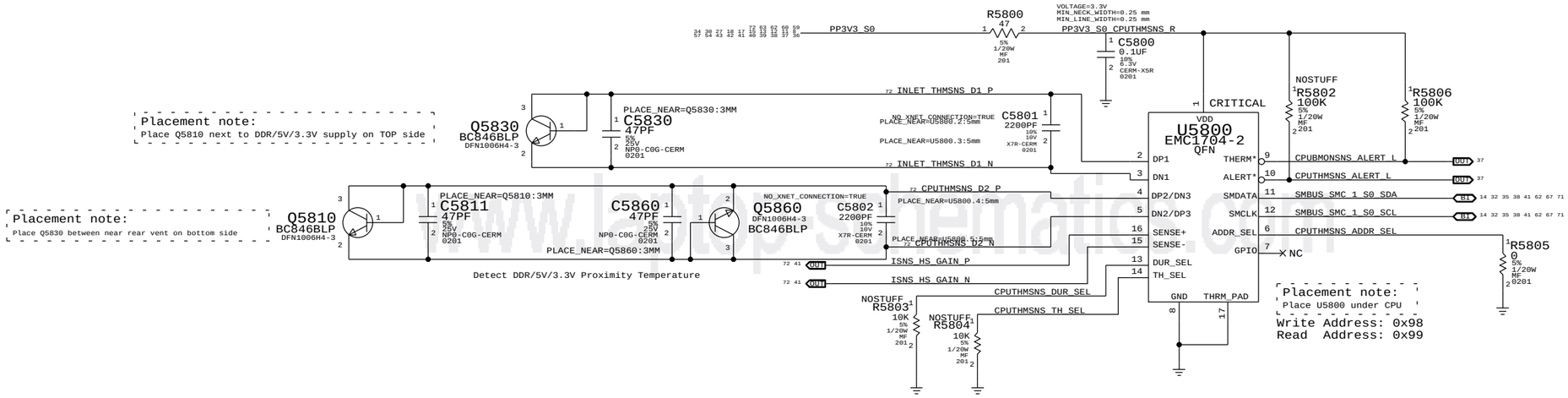
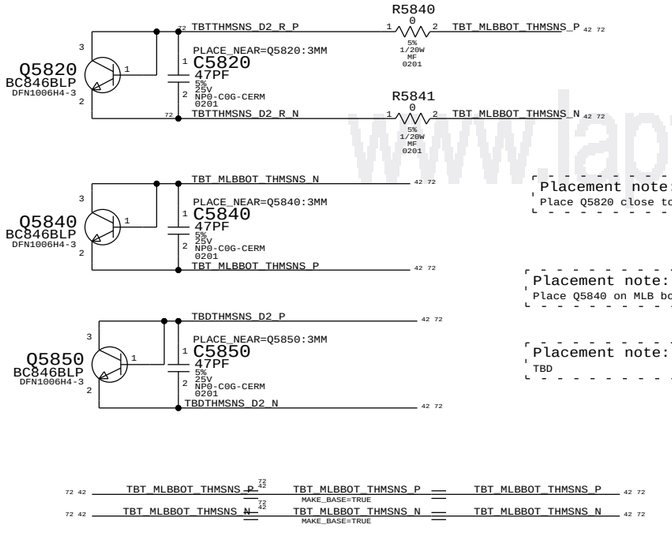
CPU Proximity, Inlet ,DDR and BMON THR Sensor



TBT,MLB Bottom Proximity Sensors



Placement note:
Place Q5820 close to TBT on TOP side

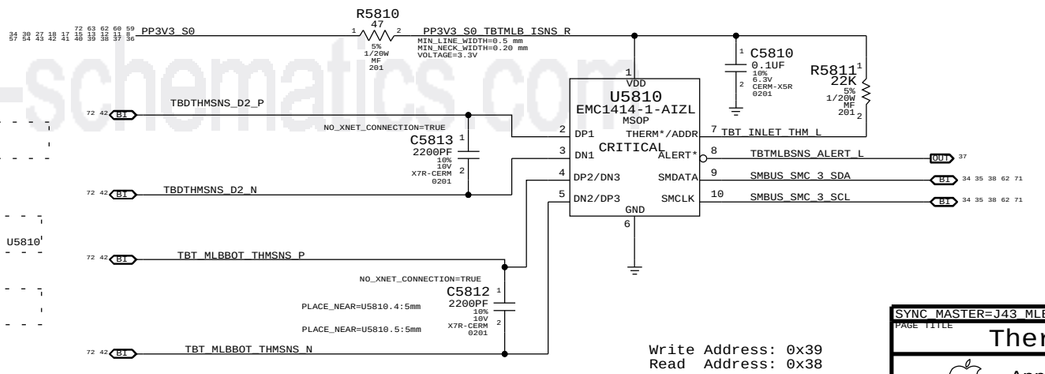
Placement note:
Place Q5840 on MLB bottom side opposite U5810

Placement note:
TBD

TBT_MLBBOT_THMSNS_P —MAKE_BASE=TRUE— TBT_MLBBOT_THMSNS_P

TBT_MLBBOT_THMSNS_N —MAKE_BASE=TRUE— TBT_MLBBOT_THMSNS_N

TBT, MLBBOT and TBD Temp Sensor



Write Address: 0x39
Read Address: 0x38

SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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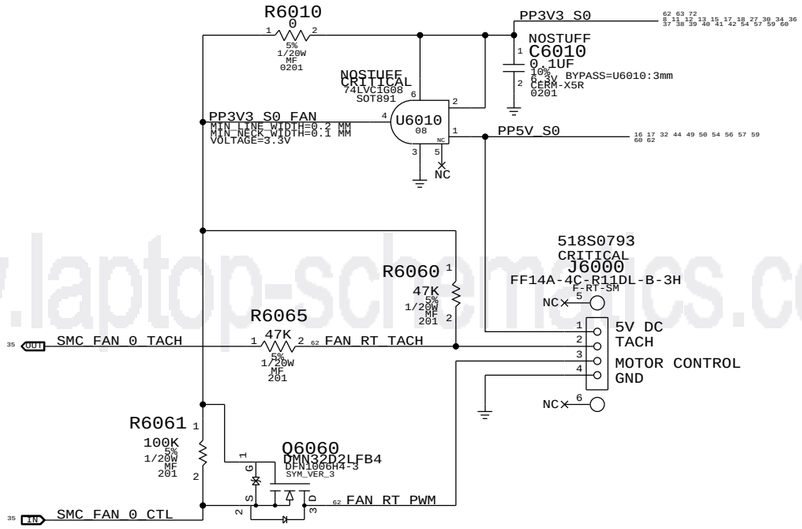
FAN CONNECTOR



SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE

Fan

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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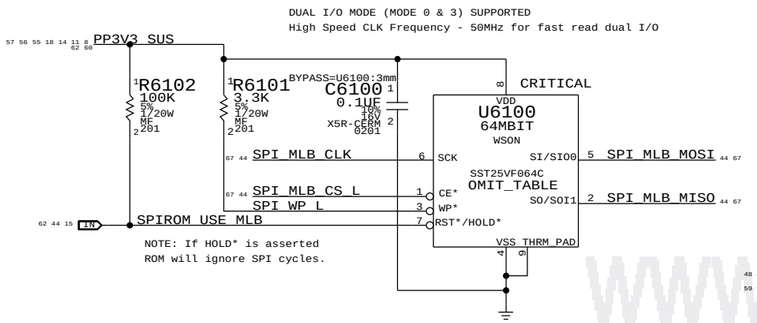
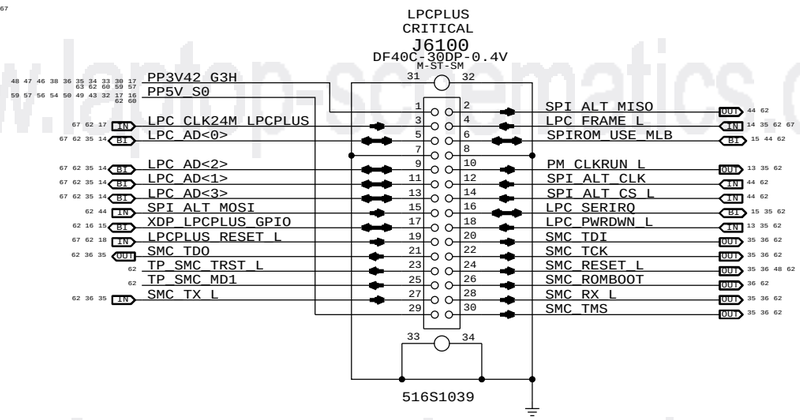
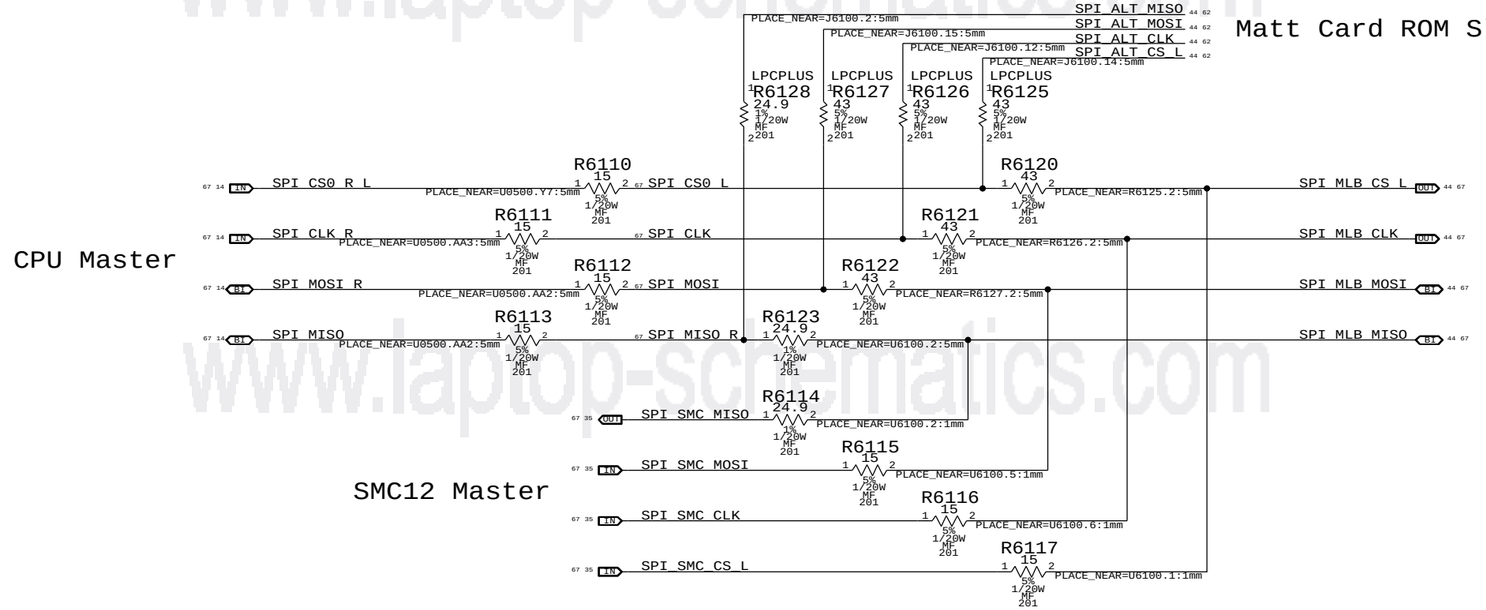


LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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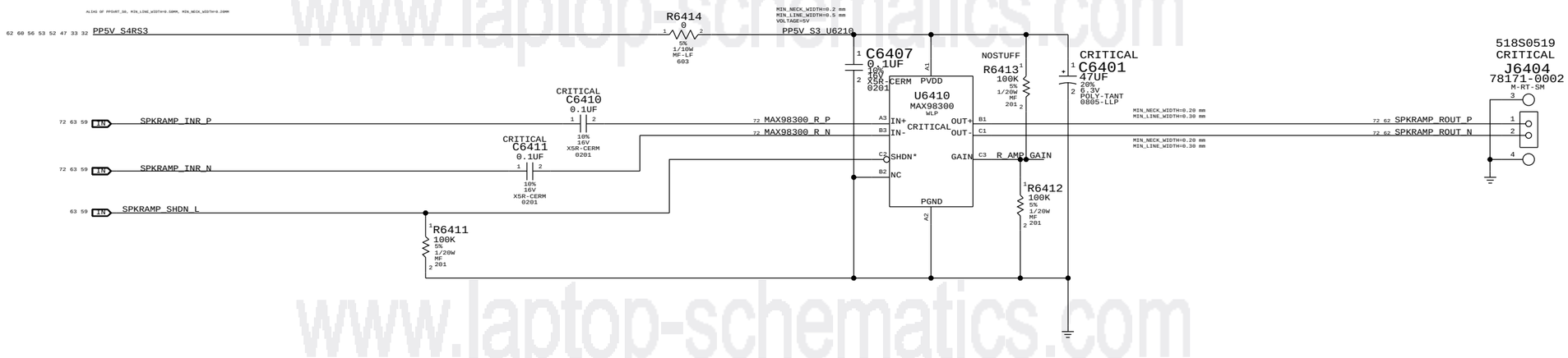
SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC_MASTER=J43_MLB SYNC_DATE=09/04/2012

PAGE TITLE: Audio: Speaker Amp

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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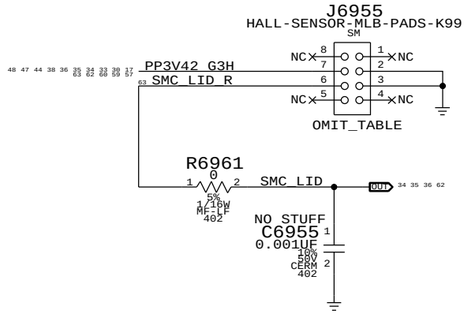
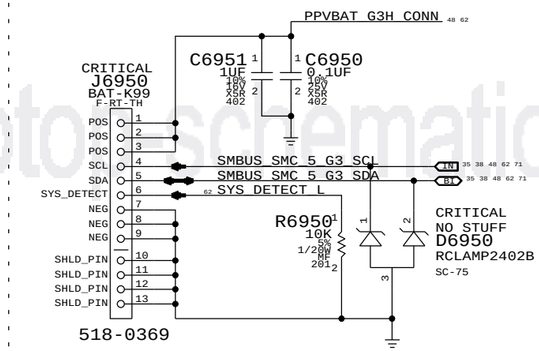
Hall Effect Sensor



11"-Specific Battery Connector



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Battery Connector & Hall Effect

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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MLB to LIO Power Cable Connector

CRITICAL
J7000
WTB-PWR-M82
M-RT-SM

518S0508

PPDCIN G3H
PP5V S4RS3

C7006 0.1UF 10% 16V X5R-CERM 0201
NO STUFF CRITICAL C7007 1UF 10% 35V X5R 603
NO STUFF CRITICAL C7008 1UF 10% 35V X5R 603
NO STUFF C7005 0.1UF 10% 50V X7R 603-1

R7012 68K 1% 1/20W MF 201

Input impedance of 68K meets sparkitecture requirements for detection of B121 (16.5V)

CRITICAL
Q7010
SI5419DU
POWERPAK

R7010 100K 5% 1/20W MF 201

CRITICAL C7012 0.047UF 10% 25V X5R 0402

R7011 10K 5% 1/20W MF 201

DCIN ISOL GATE

PPDCIN G3H ISOL

CRITICAL
D7012
GDZT2R6.8
GDZ-0201
6.8V Zener

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

PPBUS G3H

R7006 4.7 5% 1/8W MF-LF 805

CRITICAL
D7005
BAT30CWFILM
SOT-323

PPBUS G3H R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=8.6V

R7005 10 5% 1/8W MF-LF 805

PP18V5 DCIN ISOL R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=18.5V

PPVIN G3H P3V42G3H
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V

U7090
LT3470AEDD
DFN
VIN BOOST SW SHDN* BIAS NC FB GND THRM PAD

P3V42G3H BOOST
DIDT=TRUE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm

C7094 0.22UF 10% 16V CERM 402

CRITICAL L7095 10UH-20%-0.85A-0.46OHM 2520

P3V42G3H SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE

PP3V42_G3H
Vout = 3.425V
300mA Max Output
(Switcher limit)

P3V42G3H SHDN L

R7080 0 5% 1/20W MF 0201

C7095 22PF 5% 50V NP0-C0G-CERM 0201

<Ra>
R7095 348K 1% 1/20W MF 201

<Rb>
R7096 200K 1% 1/20W MF 201

CRITICAL C7099 10UF 20% 16V X5R-CERM 0402-1

CRITICAL C7098 10UF 20% 16V X5R-CERM 0402-1

CRITICAL C7091 1UF 10% 25V X5R 402

CRITICAL C7090 1UF 10% 25V X5R 402

CRITICAL C7092 5.6UF 20% 25V POLY-TANT CASE-B2-SM

NO STUFF R7081 49.9K 1% 1/20W MF 201

NO STUFF C7080 1000PF 10% 25V CERM 0402

P3V42G3H FB
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

Vout = 1.25V * (1 + Ra / Rb)

SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE: DC-In & G3H Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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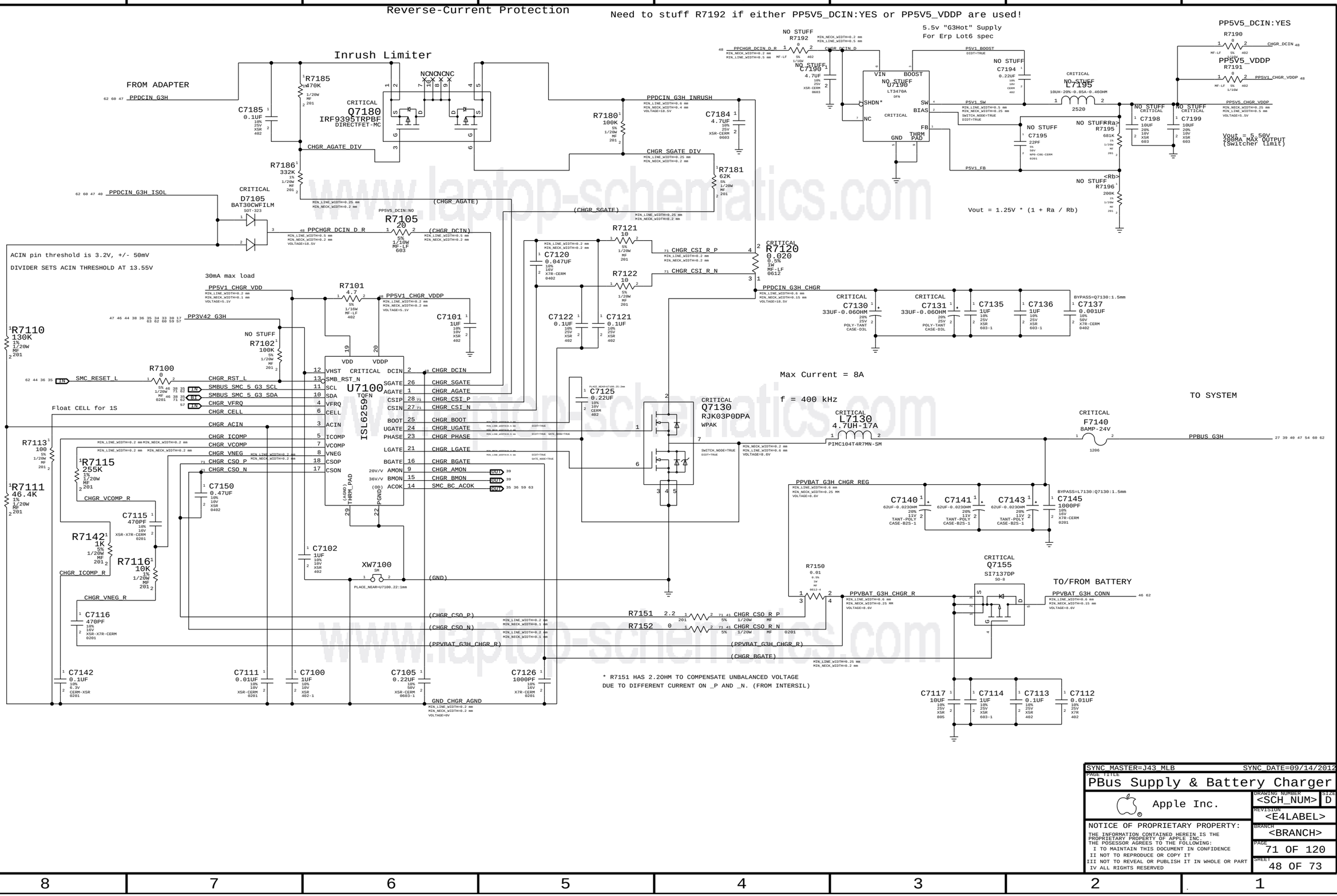

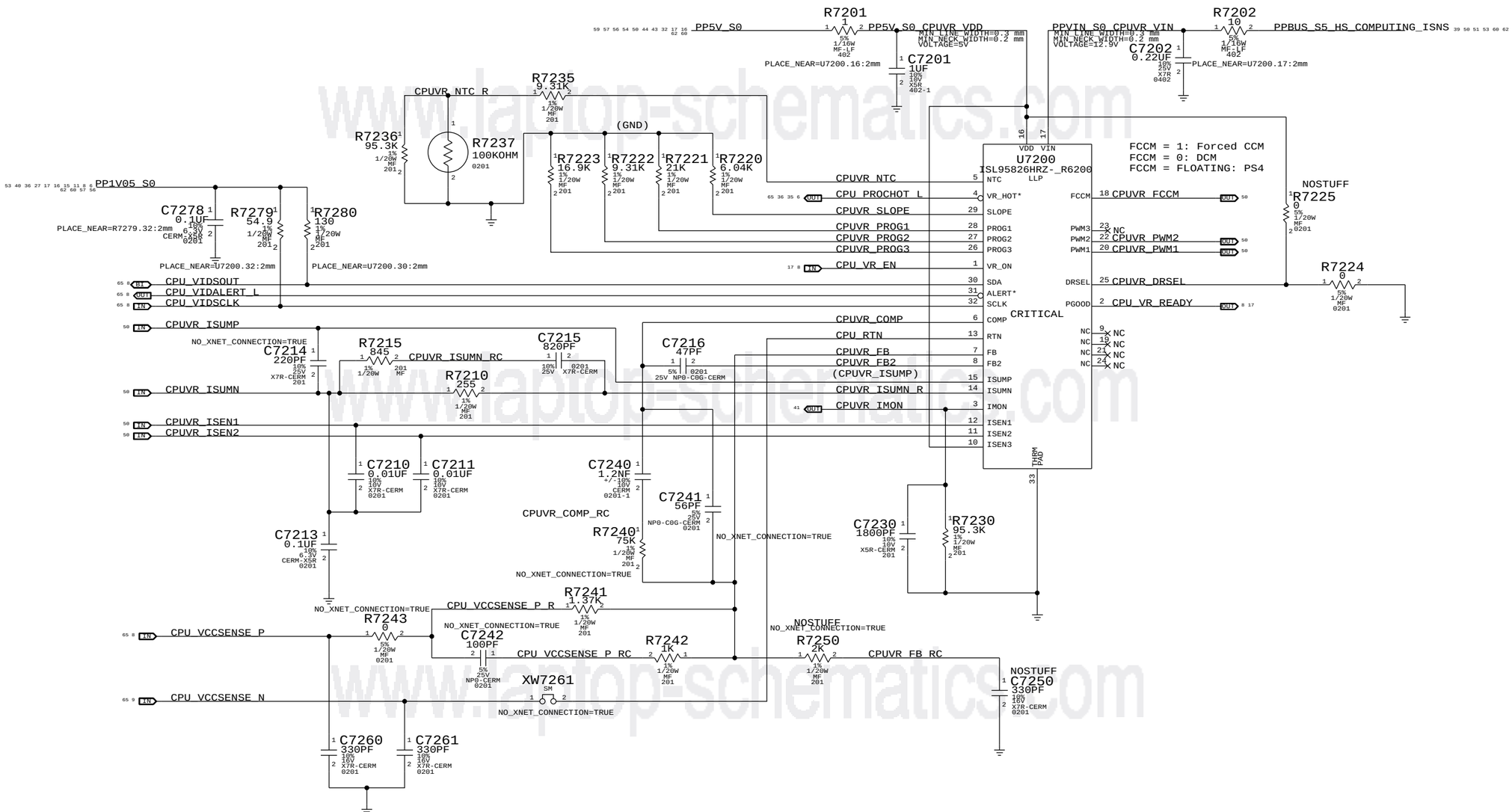

SYNC_MASTER=J43_MLB SYNC_DATE=10/09/2012

PAGE TITLE
CPU VR12.6 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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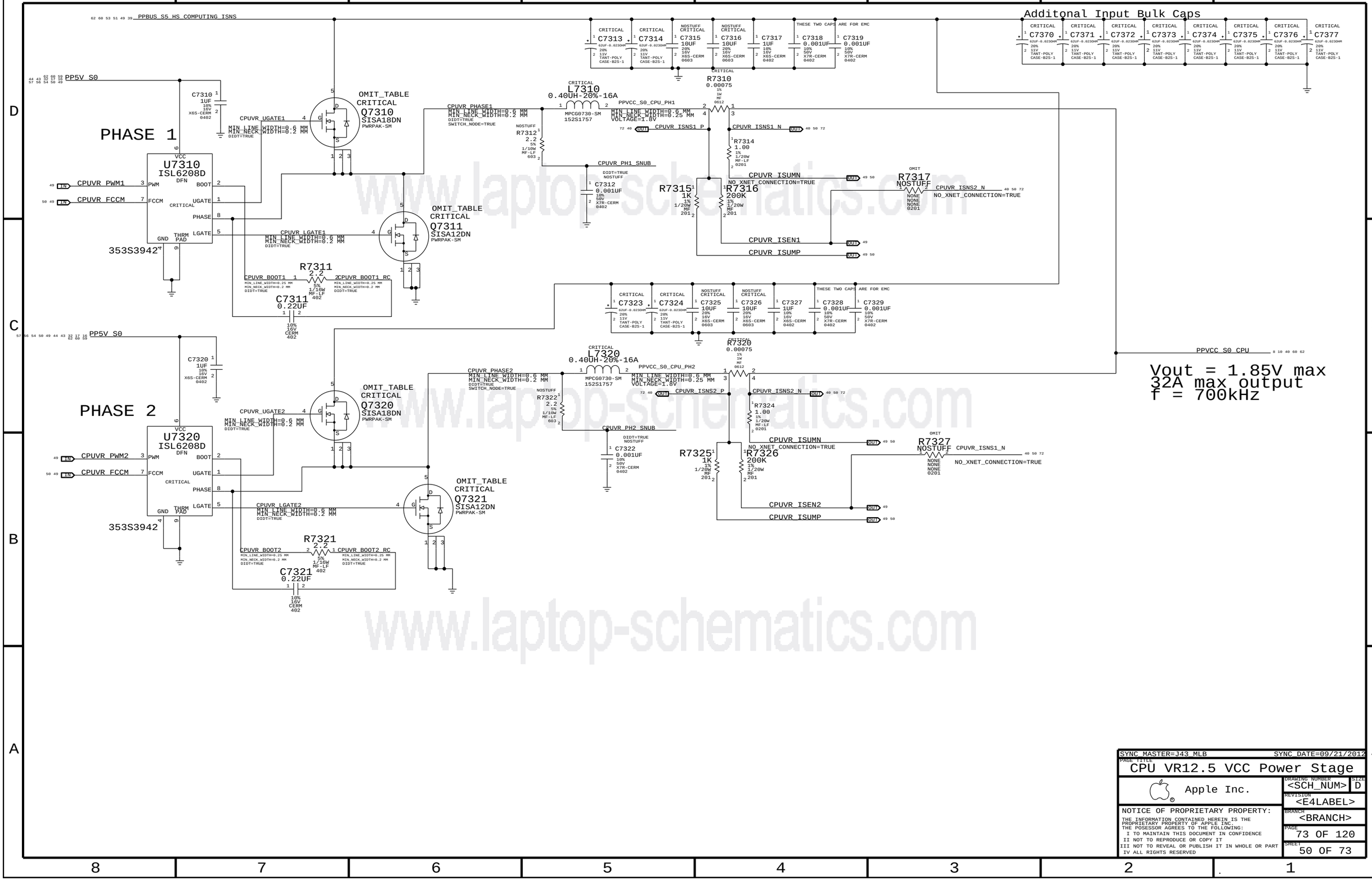
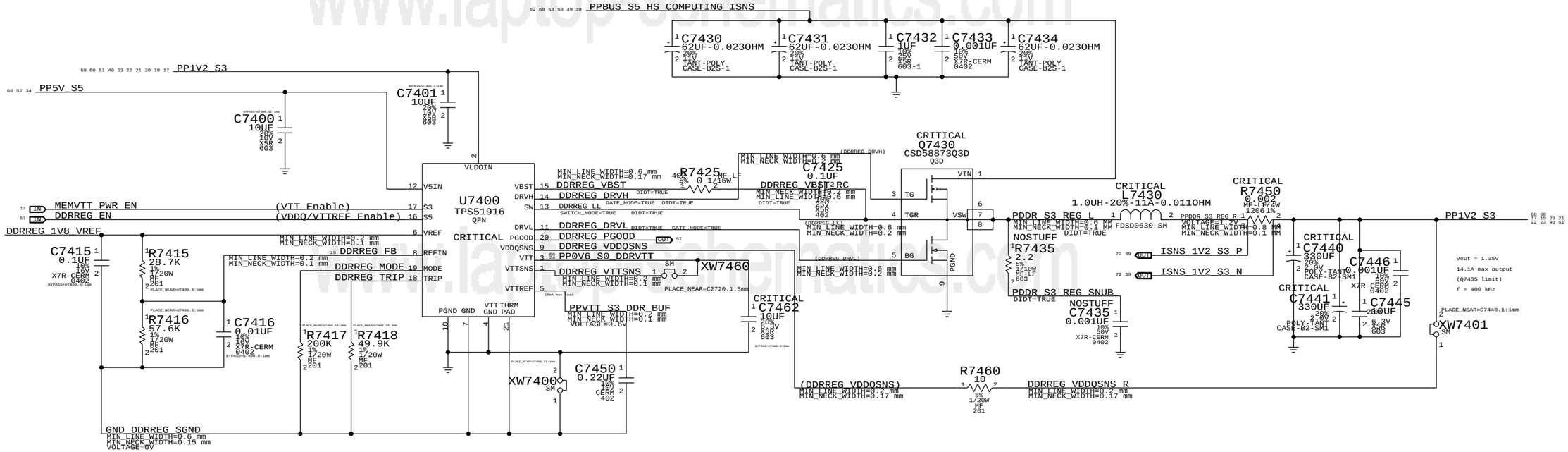
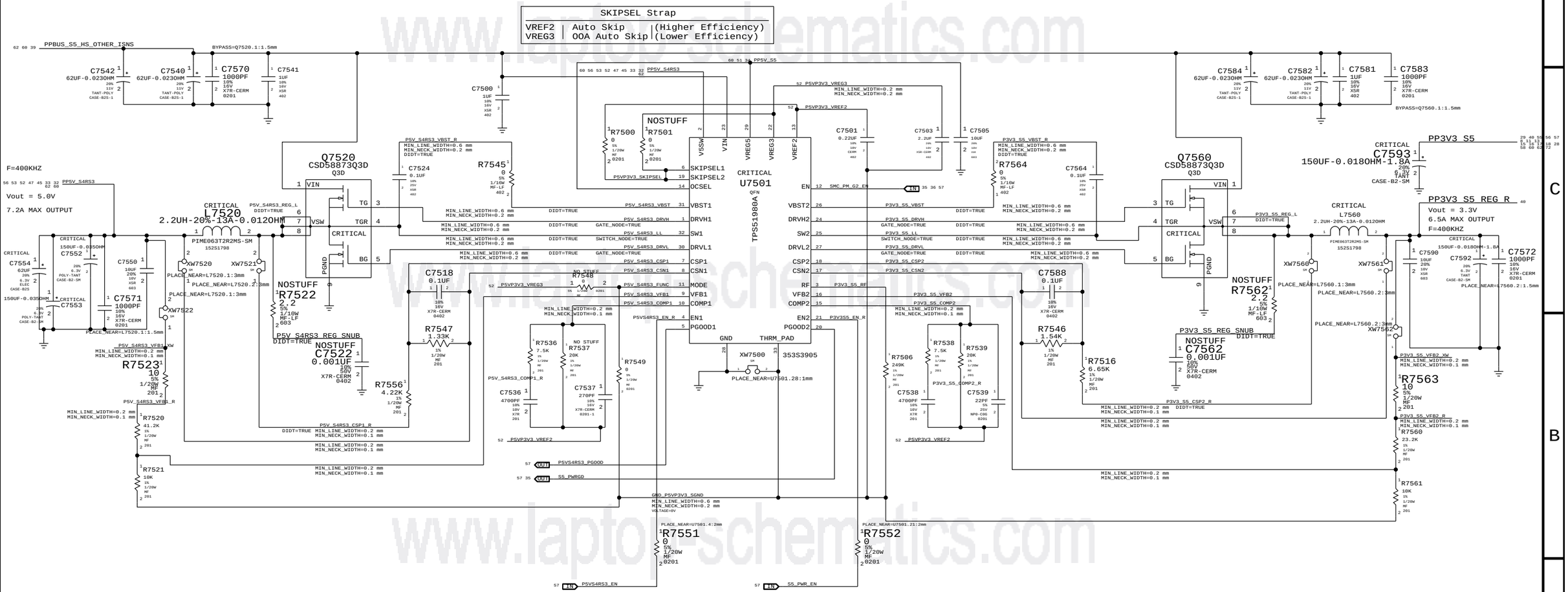
SHEET 49 OF 73

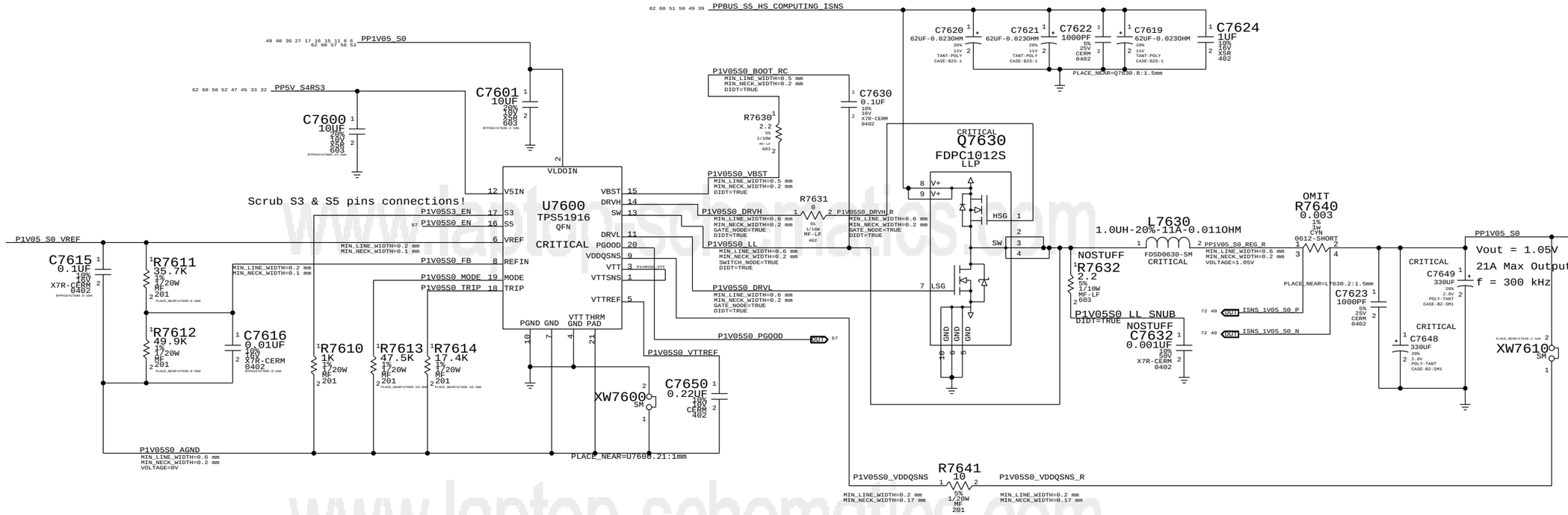




SYNC_MASTER=J43_MLB	SYNC_DATE=09/17/2012
PAGE TITLE	LPDDR3 Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 74 OF 120
	SHEET 51 OF 73



1.05V S0 Regulator



SYNC_MASTER=J43_MLB SYNC_DATE=09/10/2012

PAGE TITLE: 1.05V S0 Power Supply

Apple Inc.

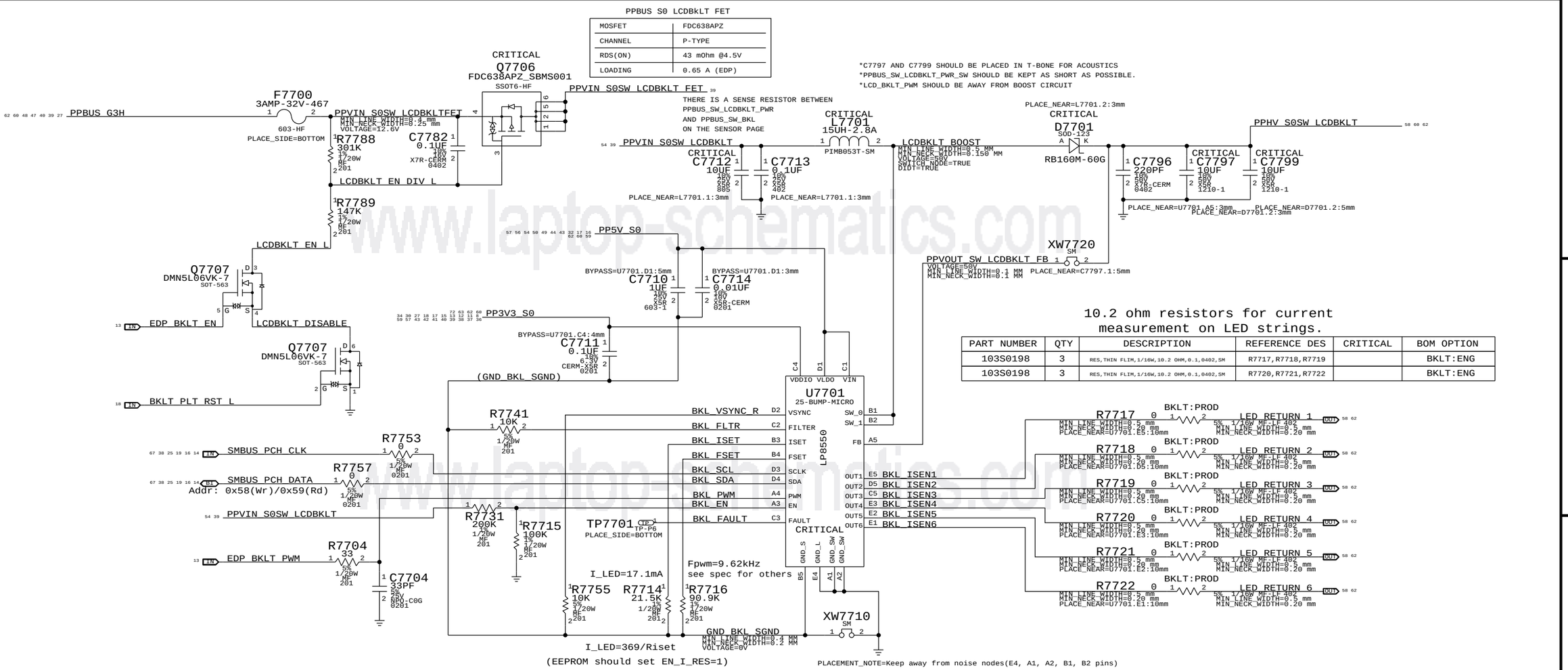
DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 76 OF 120

SHEET: 53 OF 73



SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE: LCD/KBD Backlight Driver

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

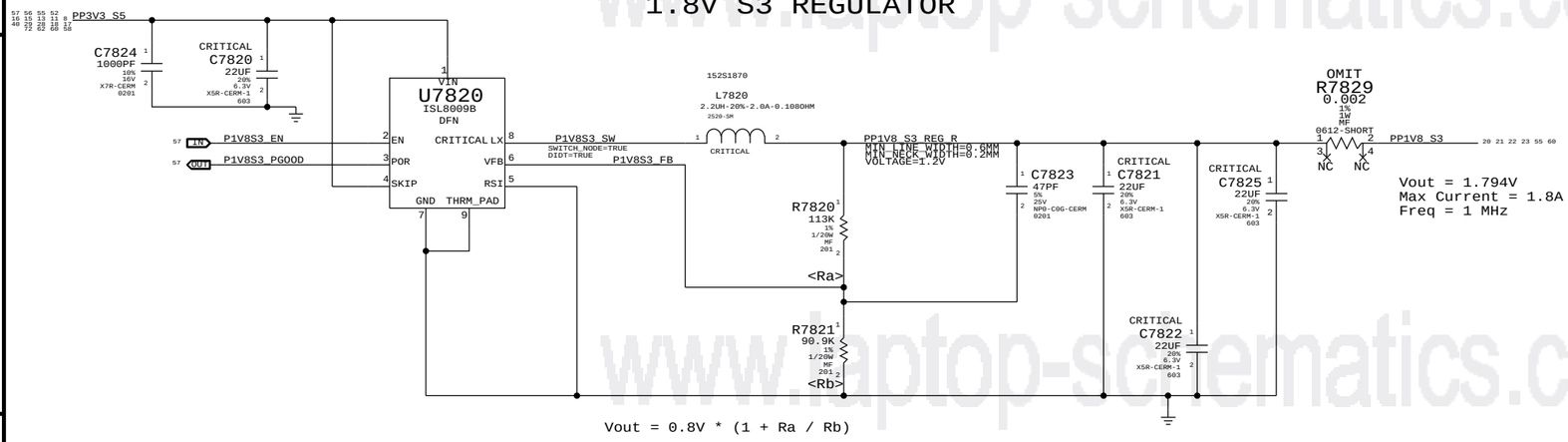
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 77 OF 120

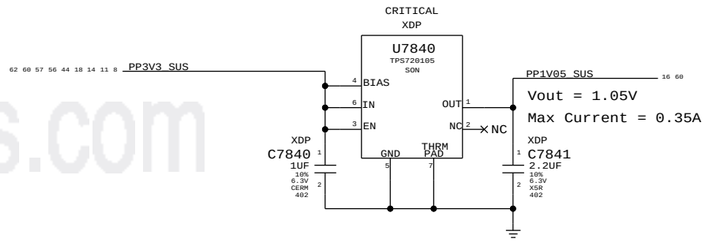
SHEET: 54 OF 73

1.8V S3 REGULATOR

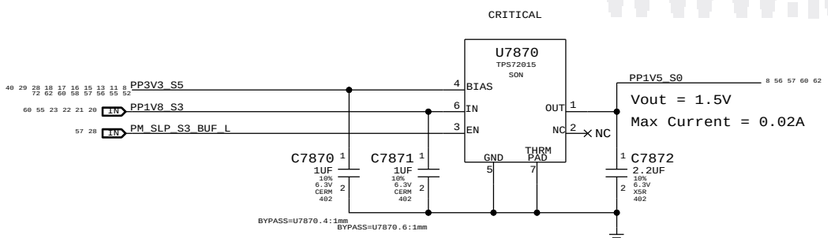


1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



SYNC_MASTER=J43_MLB SYNC_DATE=10/04/2012

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

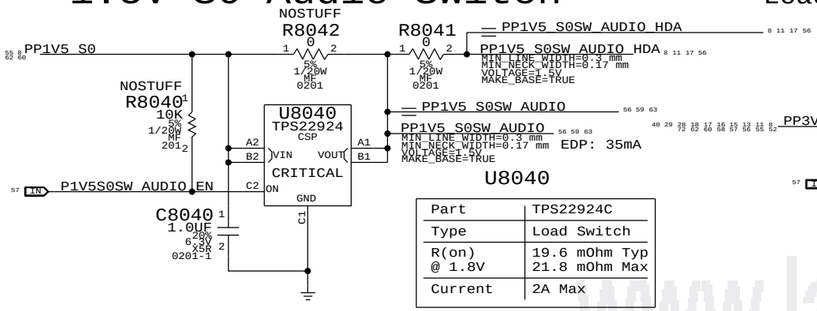
BRANCH: <BRANCH>

PAGE: 78 OF 120

SHEET: 55 OF 73

1.5V S0 Audio Switch

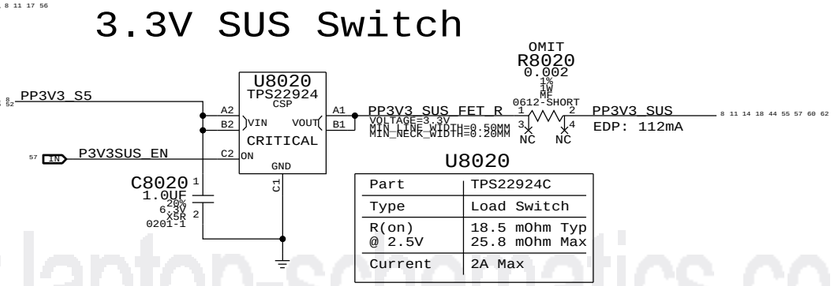
Loading specs per J41/43_PowerBudget_Riviera_rev0.99e



U8040

Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

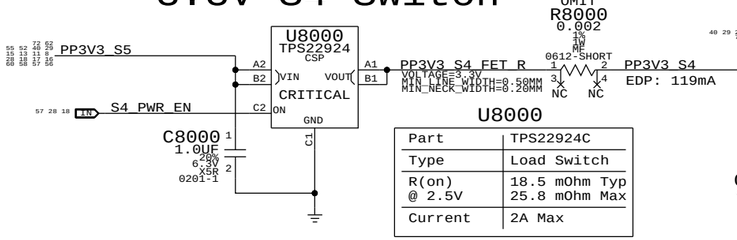
3.3V SUS Switch



U8020

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

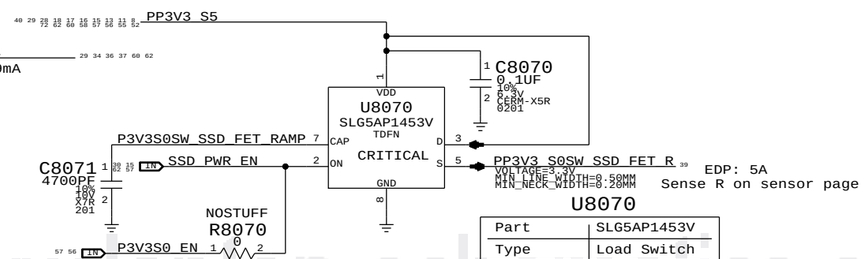
3.3V S4 Switch



U8000

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

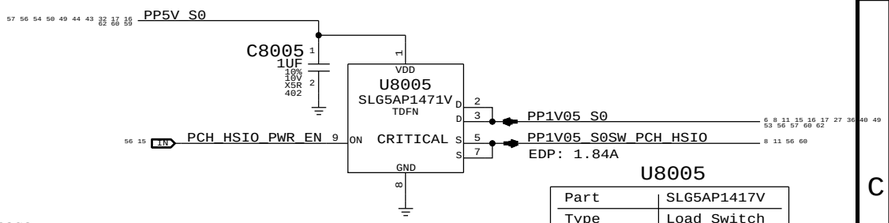
3.3V SSD Switch



U8070

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

1.05V PCH HSIO Switch

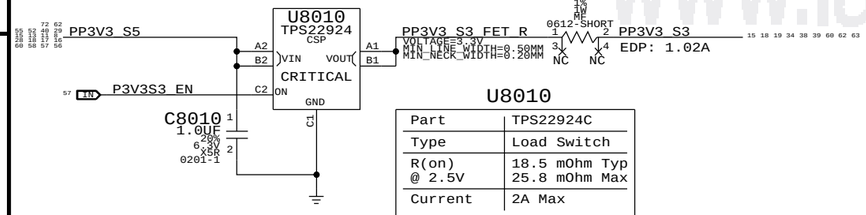


HSIO has turn-on requirement of <0.1V/uS ramp rate and <65uS from EN to 95% (1.05V)

U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

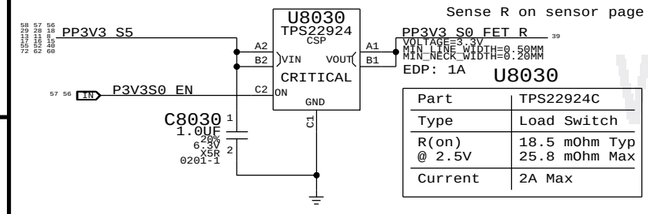
3.3V S3 Switch



U8010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

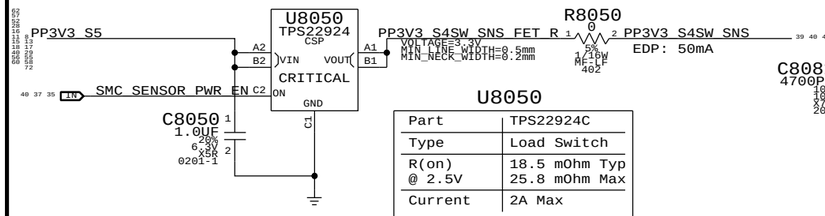
3.3V S0 Switch



U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

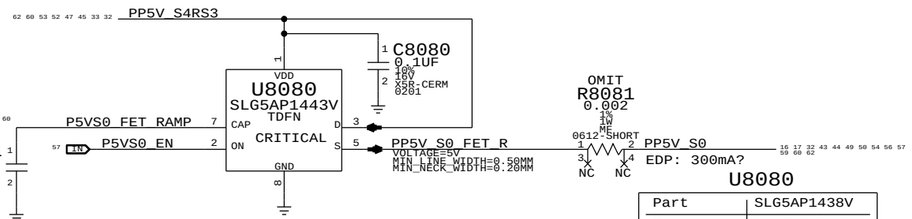
3.3V Sensor Switch



U8050

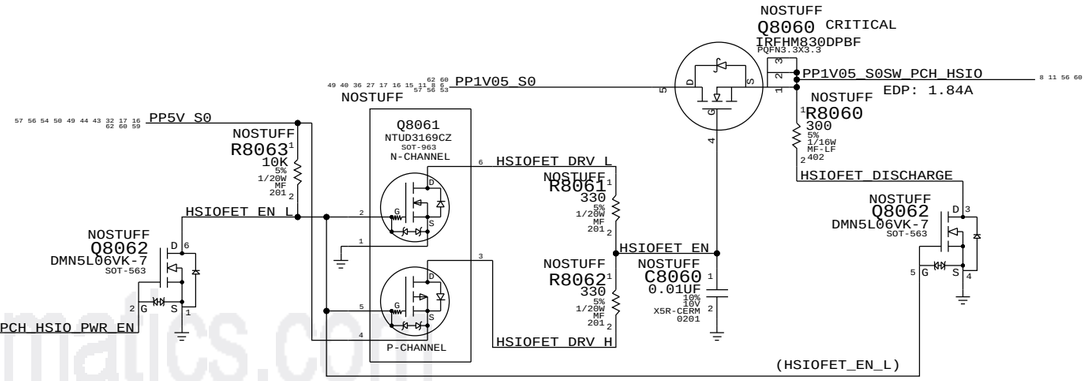
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

5V S0 Switch



U8080

Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A



SYNC_MASTER=J43_MLB SYNC_DATE=10/04/2012

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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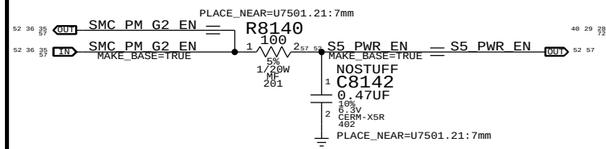
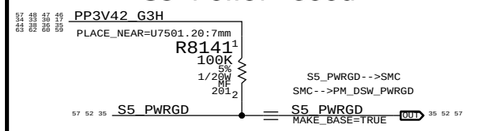
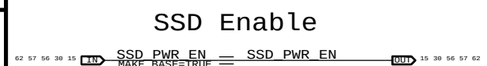
S5 Enables



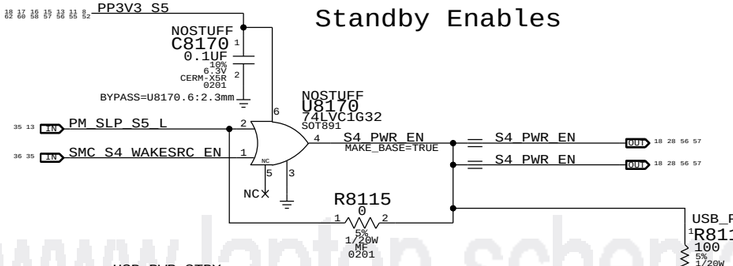
S5 Power Good

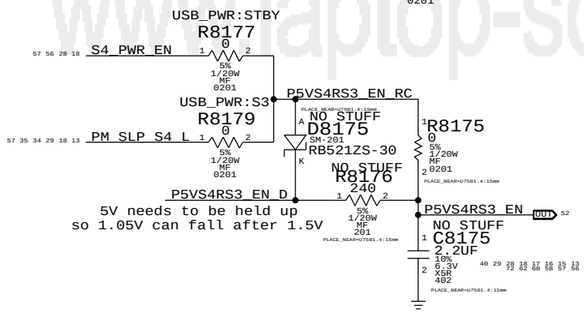


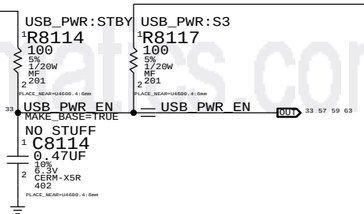
SSD Enable



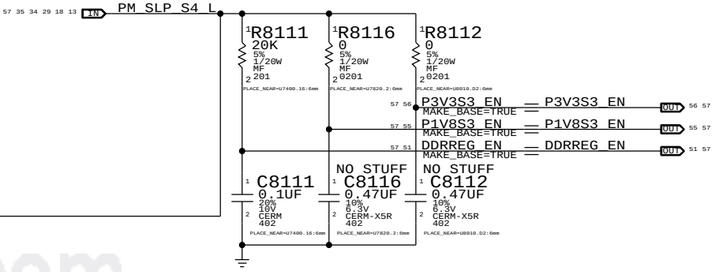
Standby Enables







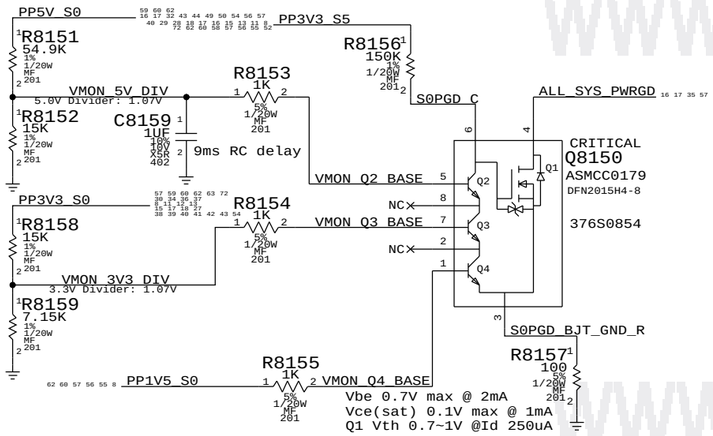
S3 Enables



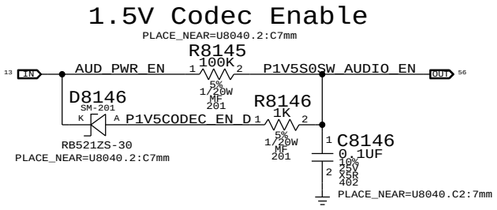
Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

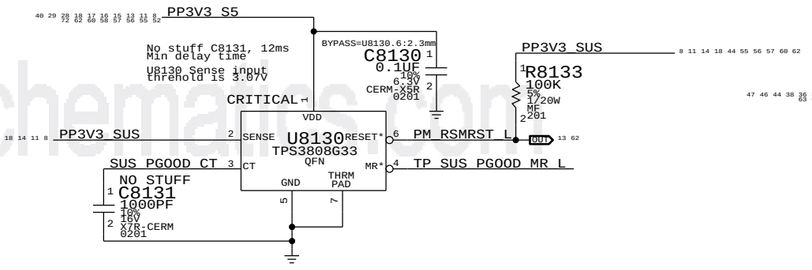
S0 Rail PGOOD (BJT Version)



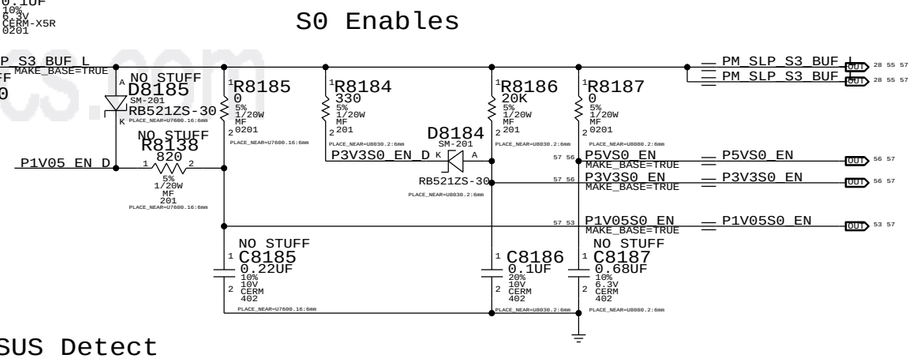
1.5V Codec Enable



3.3V SUS Detect



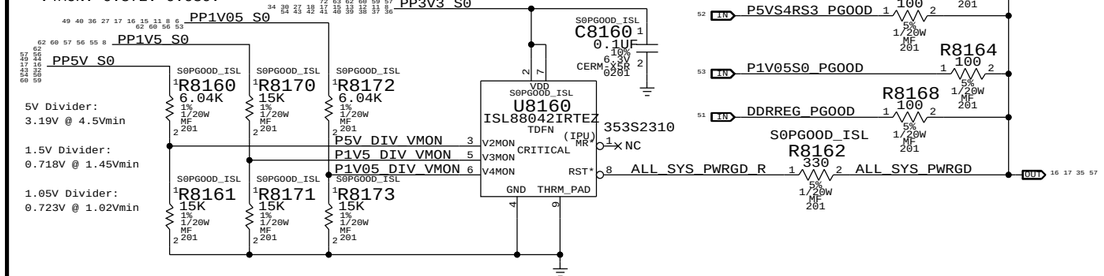
S0 Enables



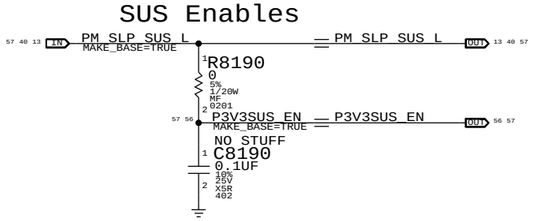
S0 Rail PGOOD Circuitry

(ISL version used for development)

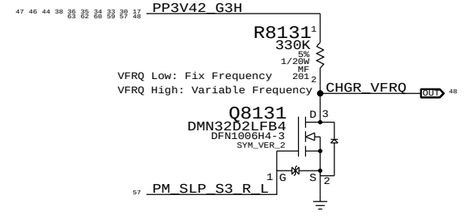
Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V



SUS Enables



CHGR VFRQ Generation



SYNC_MASTER=J43_MLB SYNC_DATE=09/16/2012

PAGE TITLE: Power Control

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 81 OF 120
SHEET: 57 OF 73

LCD Connector

Internal DP Connector: 518S0829

CRITICAL
J8300
20525-130E-01
F-RT-SM

PP3V3_S5
EDP_PANEL_PWR
CRITICAL
U8300
FPF1009
MFET-2X2-8IN
ON
VIN_1
VIN_2
VOUT_1
VOUT_2
GND
THRM PAD
PP3V3_S0SW_LCD_R
Sense resistor on sensor page
PP3V3_S0SW_LCD
C8309 0.1UF 10% 6.3V CERM-X5R 0201
C8311 0.1UF 10% 6.3V CERM-X5R 0201
C8312 10UF 20% 6.3V X5R 603

R8363 4.7K 5% 1/20W MF 201
R8364 4.7K 5% 1/20W MF 201
Pull-ups on panel side, 4.7 kOhm to 3.3V
SMBUS_SMC_0_S0_SDA
R8361 0 5% 1/20W MF 0201
I2C_TCON_SDA_R
SMBUS_SMC_0_S0_SCL
R8362 0 5% 1/20W MF 0201
I2C_TCON_SCL_R
PPHV_S0SW_LCDBKLT
LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1
LED Backlight I/F
DP_INT_HPD
R8360 0 5% 1/20W MF 0201
DP_INT_HPD_CONN
L8304 FERR-120-OHM-1.5A 0402-LF
C8315 1000PF 10% 16V X7R-CERM 0201
PP3V3_S0SW_LCD_UF
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
DisplayPort I/F
DP_INT_AUXCH_C_N
C8324 0.1UF 10% 16V X5R-CERM 0201
(DP_INT_AUX_CH_C_N)
DP_INT_AUXCH_C_P
C8325 0.1UF 10% 16V X5R-CERM 0201
(DP_INT_AUX_CH_C_P)
DP_INT_ML_C_P<0>
C8320 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_C_N<0>
C8321 0.1UF 10% 16V X5R-CERM 0201
DP_INT_AUX_CH_C_N
DP_INT_AUX_CH_C_P
DP_INT_ML_P<0>
DP_INT_ML_N<0>
PLACE_NEAR=J8300.24:1mm
PLACE_NEAR=J8300.25:1mm
R8318 1M 5% 1/20W MF 201
R8317 1M 5% 1/20W MF 201
PLACE_NEAR=J8300.14:2mm
R8350 100K 5% 1/20W MF 201
R8380 1M 5% 1/20W MF 201
R8370 1M 5% 1/20W MF 201
PLACE_NEAR=J8300.3:2mm
C8317 1000PF 5% 50V C0G-CERM 603

NC
NC
NC

SYNC_MASTER=J43_MLB
SYNC_DATE=09/11/2012

PAGE TITLE
Internal DisplayPort Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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LIO Connector

516S1036 (HIROSE 3.0mm RCPT)

CRITICAL

J9500

DF40CG3.0-48DS-0.4V

F-ST-SM

PP5V_S0 — NOSTUFF R9500 0 5% 1/20W MF 0201 — VOLTAGE=5V, MIN_LINE_WIDTH=0.1MM, MIN_NECK_WIDTH=0.1MM

C9510 0.1UF 10% 16V X5R-CERM 0201 BYPASS=J9500:1.5mm

C9520 0.1UF 10% 16V X5R-CERM 0201 BYPASS=J9500:1.5mm

C9500 0.1UF 10% 16V X5R-CERM 0201 BYPASS=J9500:1.5mm

J9500	Net	Direction
2	AUD_PWR_EN	IN
4	PP5V_S0_ALT_AUD_LDO_EN	
6	SPKRAMP_SHDN_L	OUT
8		
10		
12	PP1V5_S0SW_AUDIO	
14	PP3V3_S0	
16		
20	SPKRAMP_INR_N	OUT
22	SPKRAMP_INR_P	OUT
24		
26		
28	USB3_EXTB_D2R_RC_N	
30	USB3_EXTB_D2R_RC_P	
32		
36		
38	USB_EXTB_N	BI
40	USB_EXTB_P	BI
42		
44	USB3_EXTB_R2D_N	
46	USB3_EXTB_R2D_P	
48		
52		
3	SMBUS_SMC_2_S3_SCL	IN
5	SMBUS_SMC_2_S3_SDA	BI
7		
9	SYS_ONEWIRE	BI
11	SMC_BC_ACOK	OUT
13	XDP_USB_EXTB_OC_L	OUT
15		
19	USB_PWR_EN	IN
21	FINSTACKSNS_ALERT_L	OUT
23		
25		
27	HDA_SYNC	IN
29	HDA_RST_L	IN
31		
35		
37		
39	HDA_SDOUT	IN
41	HDA_SDIN0	OUT
43	HDA_BIT_CLK	IN
45		
47		
51		
1, 49, 50	PP3V42_G3H	

NOSTUFF C9550 10PF 5% 25V C0G-CERM 0402

USB3_EXTB_D2R_N — GND_VOID=TRUE — R9510 0 5% 1/20W MF 0201 — NOSTUFF C9531 15PF 5% 25V NP0-CERM 0201

USB3_EXTB_D2R_P — GND_VOID=TRUE — R9520 0 5% 1/20W MF 0201 — NOSTUFF C9532 15PF 5% 25V NP0-CERM 0201

USB3_EXTB_R2D_C_N — C9521 0.1UF 10% 16V X5R-CERM 0201

USB3_EXTB_R2D_C_P — C9522 0.1UF 10% 16V X5R-CERM 0201

Diode	Net	Part
D9511	USB3_EXTB_D2R_N	ESD0P2RF-02LS TSSLP-2-1
D9510	USB3_EXTB_D2R_P	ESD0P2RF-02LS TSSLP-2-1
D9520	USB3_EXTB_R2D_C_N	ESD0P2RF-02LS TSSLP-2-1
D9521	USB3_EXTB_R2D_C_P	ESD0P2RF-02LS TSSLP-2-1

SYNC_MASTER=CLEAN_J41 SYNC_DATE=11/13/2012

PAGE TITLE: LIO Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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SHEET: 59 OF 73

"G3Hot" (Always-Present) Rails

PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_S5_HS_OTHER_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

PP3V42_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE

PPVRTC_G3H
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE

5V Rails

PP5V_S5
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S4RS3
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.175 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE

3.3V Rails

PP3V3_S5
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4
MIN_LINE_WIDTH=0.60MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_SUS
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S3
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4SW_SNS
MIN_LINE_WIDTH=0.60MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0SW_SSD
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

1.8V/1.5V/1.2V/1.05V Rails

PP1V8_S3
2A max supply
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V5_S0
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP0V6_S0_DDRVTT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

PP1V05_S0
? mA
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.175 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_S0SW_PCH_HSIO
1.84A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

LCDBKLT Rail

PPHV_S0SW_LCDBKLT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=50V
MAKE_BASE=TRUE

TBT Rails (off when no cable)

PP15V_TBT
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=17.8V
MAKE_BASE=TRUE

PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP1V05_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PPVIN_S4SW_TBTBST_FET
VOLTAGE=8.6V

CPU "VCORE" RAILS

PPVCC_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE
Power Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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SHEET 60 OF 73

Memory Bit/Byte Swizzle

LPDDR3 Command/Address

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	=MEM_A_BA<2>	TRUE	MEM_A_CAA<5>		
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	=MEM_A_A<11>	TRUE	MEM_A_CAA<7>		
	=MEM_A_A<15>	TRUE	MEM_A_CAA<8>		
	=MEM_A_A<14>	TRUE	MEM_A_CAA<9>		
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	=MEM_A_WE_L	TRUE	MEM_A_CAB<2>		
	=MEM_A_RAS_L	TRUE	MEM_A_CAB<3>		
	=MEM_A_BA<0>	TRUE	MEM_A_CAB<4>		
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68 61 24 21 7	MEM_A_CAB<6>	TRUE	MEM_A_CAB<6>	7 21 24 61 68	
	=MEM_A_A<10>	TRUE	MEM_A_CAB<7>		
	=MEM_A_A<1>	TRUE	MEM_A_CAB<8>		
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68 61 24 21 20 7	MEM_A_ODT<0>	TRUE	MEM_A_ODT<0>	7 20 21 24 61 68	
61 7	TP_LPDDR3_RSVD1	TRUE	TP_LPDDR3_RSVD1	7 61	
61 7	TP_LPDDR3_RSVD2	TRUE	TP_LPDDR3_RSVD2	7 61	
	=MEM_B_A<5>	TRUE	MEM_B_CAA<0>		
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68 61 24 23 22 7	MEM_B_CAB<6>	TRUE	MEM_B_CAB<6>	7 23 24 61 68	
	=MEM_B_A<10>	TRUE	MEM_B_CAB<7>		
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68 61 24 23 22 7	MEM_B_ODT<0>	TRUE	MEM_B_ODT<0>	7 22 23 24 61 68	
61 7	TP_LPDDR3_RSVD3	TRUE	TP_LPDDR3_RSVD3	7 61	
61 7	TP_LPDDR3_RSVD4	TRUE	TP_LPDDR3_RSVD4	7 61	

MAKE_BASE

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68 61 21 7	MEM_A_DQ<33>	TRUE	MEM_A_DQ<33>	7 21 61 68	
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MAKE_BASE

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SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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Functional Test Points

J3501: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN	(Need 6 TPs)	29 35 36 37 39
TRUE	WIFI_EVENT_L		29 35 36
TRUE	PCIE_AP_R2D_N		29 67
TRUE	PCIE_AP_R2D_P		29 67
TRUE	PCIE_CLK100M_AP_N		12 29 67
TRUE	PCIE_CLK100M_AP_P		12 29 67
TRUE	PCIE_AP_D2R_P		14 29 67
TRUE	PCIE_AP_D2R_N		14 29 67
TRUE	PCIE_WAKE_L		13 29 31
TRUE	AP_RESET_CONN_L		29
TRUE	AP_CLKREQ_O_L		29
TRUE	USB_BT_CONN_P		29 66
TRUE	USB_BT_CONN_N		29 66
TRUE	PP3V3_S4		29 34 36 37 56 60 62

(Need to add 8 GND TPs)

J3700: SSD Connector

FUNC_TEST

TRUE	PP3V3_S0SW_SSD_FLT	(Need 5 TPs)	30
TRUE	PCIE_SSD_R2D_N<3..0>		30 65
TRUE	PCIE_SSD_R2D_P<3..0>		30 65
TRUE	PP3V3_S0		40 41 42 43 54 57 59 60 62 63 72
TRUE	SSD_RESET_CONN_L		30
TRUE	SSD_CLKREQ_CONN_L		30
TRUE	SMC_OOB1_R2D_CONN_L		30
TRUE	SMC_OOB1_D2R_CONN_L		30
TRUE	SSD_PCIE_SEL_L		16 30
TRUE	SSD_DEVSLP		15 30
TRUE	SSD_PWRFAIL_WARN_L		
TRUE	SSD_PWR_EN		15 30 56 57
TRUE	PCIE_SSD_D2R_N<3..0>		12 30 65
TRUE	PCIE_SSD_D2R_P<3..0>		12 30 65
TRUE	PCIE_CLK100M_SSD_N		12 30 65
TRUE	PCIE_CLK100M_SSD_P		12 30 65

(Need to add 6 GND TPs)

J4002: Camera Connector

FUNC_TEST

TRUE	MIPI_CLK_CONN_N		32 70
TRUE	MIPI_CLK_CONN_P		32 70
TRUE	CAM_SENSOR_WAKE_L_CONN		32
TRUE	MIPI_DATA_CONN_N		32 70
TRUE	MIPI_DATA_CONN_P		32 70
TRUE	SMBUS_SMC_1_S0_SDA		14 32 35 38 41 42 67 71
TRUE	SMBUS_SMC_1_S0_SCL		14 32 35 38 41 42 67 71
TRUE	I2C_CAM_SCK		31 32
TRUE	I2C_CAM_SDA		31 32
TRUE	PP5V_S3RS0_ALSCAM_F	(Need TBD TPs)	32

(Need to add TBD GND TPs)

J6000: Fan Connector

FUNC_TEST

TRUE	PP5V_S0		16 17 32 43 44 49 50 54 56 57 59 60 62
TRUE	FAN_RT_TACH		43
TRUE	FAN_RT_PWM		43

(Need to add 1 GND TP)

J4800: IPD Flex Connector

FUNC_TEST

TRUE	SMC_LID		34 35 36 46
TRUE	TPAD_SPI_MISO_R		34
TRUE	USB_TPAD_P		14 34 66
TRUE	USB_TPAD_N		14 34 66
TRUE	TPAD_SPI_CLK_R		34
TRUE	TPAD_WAKE_L		34
TRUE	TPAD_SPI_MOSI_R		34
TRUE	PP3V3_S4_IPD		34
TRUE	TPAD_SPI_CS_R_L		34
TRUE	TPAD_SPI_IF_EN_CONN		34
TRUE	TPAD_SPI_INT_S4_WAKE_L_CONN		34
TRUE	PP5V_S4_IPD		34
TRUE	TPAD_USB_IF_EN_CONN		34
TRUE	SMBUS_SMC_3_SDA		34 35 38 42 71
TRUE	SMBUS_SMC_3_SCL		34 35 38 42 71
TRUE	SMC_LSOC_RST_L		34 36
TRUE	PP3V42_G3H		17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	SMC_ONOFF_L		34 35 36

(Need to add 5 GND TPs)

J7000: DC-In Connector

FUNC_TEST

TRUE	PPDCIN_G3H	(Need 4 TPs)	4 48 60 62
TRUE	PP5V_S4RS3	(Need 3 TPs)	32 33 45 47 52 53 56 60

(Need to add 5 GND TPs)

J6404: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_ROUT_P		45 72
TRUE	SPKRAMP_ROUT_N		45 72

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	(Need 4 TPs)	46 48
TRUE	SMBUS_SMC_5_G3_SCL		35 38 46 48 71
TRUE	SMBUS_SMC_5_G3_SDA		35 38 46 48 71
TRUE	SYS_DETECT_L		46

(Need to add 4 GND TPs near J7050 and 1 for shield)

J8300: Internal DP Connector

FUNC_TEST

TRUE	PPHV_S0SW_LCDBKLT	(Need 2 TPs)	54 58 60
TRUE	LED_RETURN_6		54 58
TRUE	LED_RETURN_5		54 58
TRUE	LED_RETURN_4		54 58
TRUE	LED_RETURN_3		54 58
TRUE	LED_RETURN_2		54 58
TRUE	LED_RETURN_1		54 58
TRUE	DP_INT_HPD_CONN		58
TRUE	I2C_TCON_SDA_R		58
TRUE	I2C_TCON_SCL_R		58
TRUE	PP3V3_S0SW_LCD_UF	(Need 2 TPs)	58
TRUE	DP_INT_AUX_CH_C_N		58 65
TRUE	DP_INT_AUX_CH_C_P		58 65
TRUE	DP_INT_ML_P<0>		58 65
TRUE	DP_INT_ML_N<0>		58 65

(Need to add 5 GND TPs)

J7715: KB BKLT Connector

FUNC_TEST

TRUE	KBDLED_ANODE		54
TRUE	KBDLED_FB		54

(Need to add 2 GND TPs)

J1800: XDP Connector

(Only a subset are needed for FCT HVM test fixture)

FUNC_TEST

TRUE	XDP_CPU_TCK		6 16 65
TRUE	XDP_PCH_TCK		12 16 67
TRUE	XDP_CPU_TDI		6 16 65
TRUE	XDP_CPU_TDO		6 16 65
TRUE	XDP_CPUPCH_TRST_L		6 12 16 65
TRUE	XDP_CPU_TMS		6 16 65
TRUE	XDP_PCH_TMS		12 16 67
TRUE	XDP_PCH_TDI		12 16 67
TRUE	XDP_PCH_TDO		12 16 67
TRUE	XDP_CPU_PREQ_L		6 16 65
TRUE	XDP_CPU_PRDY_L		6 16 65
TRUE	XDP_CPU_VCCST_PWRGD		16
TRUE	PM_RSMRST_L		13 57
TRUE	XDP_SYS_PWROK		16
TRUE	PM_SYSRST_L		13 17 35
TRUE	CPU_CFG<3>		6 16 65
TRUE	PP1V05_S0		6 8 11 15 16 17 27 36 40 49 53 56 57 60 62

(Need to add 2 GND TPs)

J6100: LPC+SPI Connector

FUNC_TEST

TRUE	PP3V42_G3H		62 63
TRUE	PP5V_S0		17 30 33 34 35 36 38 44 46 47 48 59 60 62
TRUE	LPC_CLK24M_LPCPLUS		16 17 32 43 44 49 50 54 56 57 59 60 62
TRUE	LPC_AD<3..0>		17 44 67
TRUE	SPI_ALT_MOSI		14 35 44 67
TRUE	XDP_LPCPLUS_GPIO		44
TRUE	LPCPLUS_RESET_L		15 16 44
TRUE	SMC_TDO		18 44 67
TRUE	TP_SMC_TRST_L		35 36 44
TRUE	TP_SMC_MD1		44
TRUE	SMC_TX_L		44
TRUE	SPI_ALT_MISO		35 36 44
TRUE	LPC_FRAME_L		44
TRUE	SPIROM_USE_MLB		14 35 44 67
TRUE	PM_CLKRUN_L		15 44
TRUE	SPI_ALT_CLK		13 35 44
TRUE	SPI_ALT_CS_L		44
TRUE	LPC_SERIRQ		15 35 44
TRUE	LPC_PWRDWN_L		13 35 44
TRUE	SMC_TDI		35 36 44
TRUE	SMC_TCK		35 36 44
TRUE	SMC_RESET_L		35 36 44 48
TRUE	SMC_ROMBOOT		36 44
TRUE	SMC_RX_L		35 36 44
TRUE	SMC_TMS		35 36 44

(Need to add 6 GND TPs)

TRUE	GND	

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H	27 39 40 47 48 54 60
TRUE	PPVIN_S4SW_TBTBST_FET	27 60
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	39 49 50 51 53 60
TRUE	PPDCIN_G3H	47 48 60 62
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	PPVRTC_G3H	8 12 13 17 60
TRUE	PP3V3_S5	8 11 13 15 16 17 18 28 29 40 52 56 59 60 62 72
TRUE	PP3V3_SUS	8 11 14 18 44 55 56 57 60
TRUE	PP3V3_S3	15 18 19 34 38 39 56 60 63
TRUE	PP3V3_S0	60 62 63 72
TRUE	PP3V3_S0SW_SSD	8 11 12 13 15 16 17 18 27 30 34 36 37 38 39 40 41 42 43 54 57 59
TRUE	PP1V5_S0	8 55 56 57 60
TRUE	PP1V05_S0	6 8 11 15 16 17 27 36 40 49 53 56 57 60 62
TRUE	PP15V_TBT	27 28 60
TRUE	PP3V3_TBTLC	15 17 25 26 27 60
TRUE	PP1V05_TBTLC	26 27 60
TRUE	PPVCC_S0_CPU	8 10 40 50 60
TRUE	PP1V05_TBTCIO	26 27 60
TRUE	PPBUS_S5_HS_OTHER_ISNS	39 52 60
TRUE	PPDCIN_G3H_ISOL	40 47 48 60
TRUE	PP3V3_S4	29 34 36 37 56 60 62

(Need to add 27 GND TPs)

NO_TEST Nets

	NO_TEST	MAKE_BASE			
62	NC_PCIE_CLK100M_SDP	TRUE	TRUE	NC_PCIE_CLK100M_SDP	62
62	NC_PCIE_CLK100M_SDN	TRUE	TRUE	NC_PCIE_CLK100M_SDN	62
62 12	NC_PCIE_CLK100M_FWP	TRUE	TRUE	NC_PCIE_CLK100M_FWP	12 62
62 12	NC_PCIE_CLK100M_FWN	TRUE	TRUE	NC_PCIE_CLK100M_FWN	12 62
62 14	NC_PCIE_FW_D2RP	TRUE	TRUE	NC_PCIE_FW_D2RP	14 62
62 14	NC_PCIE_FW_D2RN	TRUE	TRUE	NC_PCIE_FW_D2RN	14 62
62 14	NC_PCIE_FW_R2D_CP	TRUE	TRUE	NC_PCIE_FW_R2D_CP	14 62
62 14	NC_PCIE_FW_R2D_CN	TRUE	TRUE	NC_PCIE_FW_R2D_CN	14 62
62 14	NC_USB_IRP	TRUE	TRUE	NC_USB_IRP	14 62
62 14	NC_USB_IRN	TRUE	TRUE	NC_USB_IRN	14 62
62 14	NC_USB_CAMERAP	TRUE	TRUE	NC_USB_CAMERAP	14 62
62 14	NC_USB_CAMERAN	TRUE	TRUE	NC_USB_CAMERAN	14 62
62 14	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	14 62
62 14	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	14 62
65	DP_INT_ML_C_P<3..1>	TRUE	TRUE	NC_INT_ML_CP<3..1>	5
65	DP_INT_ML_C_N<3..1>	TRUE	TRUE	NC_INT_ML_CN<3..1>	5
62 12	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1	12 62
62 13	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	13 62
62 14	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	14 62
62 14	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	14 62
62 14	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	14 62

CPU/PCH

62 35	NC_SMC_SYS_LED	TRUE	TRUE	NC_SMC_SYS_LED	35 62
62	NC_IR_RX_OUT_RC	TRUE	TRUE	NC_IR_RX_OUT_RC	62
62	NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP	62
62	NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN	62
62 35	NC_SMC_GFX_OVERTEMP	TRUE	TRUE	NC_SMC_GFX_OVERTEMP	35 62
62 35	NC_SMC_GFX_THROTTLE_L	TRUE	TRUE	NC_SMC_GFX_THROTTLE_L	35 62
62 35	NC_SMC_FAN_1_CTL	TRUE	TRUE	NC_SMC_FAN_1_CTL	35 62
62 35	NC_SMC_FAN_1_TACH	TRUE	TRUE	NC_SMC_FAN_1_TACH	35 62
62 35	NC_SMC_FAN_5_CTL	TRUE	TRUE	NC_SMC_FAN_5_CTL	35 62
62	NC_ENET_ASF_GPIO	TRUE	TRUE	NC_ENET_ASF_GPIO	62
62	NC_SMC_MPM5_LED_PWR	TRUE	TRUE	NC_SMC_MPM5_LED_PWR	62
62	NC_SMC_MPM5_LED_CHG	TRUE	TRUE	NC_SMC_MPM5_LED_CHG	62
62 35	NC_SMC_T25_EN_L	TRUE	TRUE	NC_SMC_T25_EN_L	35 62
62 35	NC_SMC_DP_HPD_L	TRUE	TRUE	NC_SMC_DP_HPD_L	35 62
62 35	NC_SMBUS_SMC_4_ASF_SCL	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SCL	35 62
62 35	NC_SMBUS_SMC_4_ASF_SDA	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SDA	35 62
62 35	NC_BDV_BKL_PWM	TRUE	TRUE	NC_BDV_BKL_PWM	35 62

SMC

69	TBT_B_R2D_C_P<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CP<1..0>	25
69	TBT_B_R2D_C_N<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CN<1..0>	25
69	TBT_B_D2R_P<1..0>	TRUE	TRUE	NC_TBT_B_D2RP<1..0>	25
69	TBT_B_D2R_N<1..0>	TRUE	TRUE	NC_TBT_B_D2RN<1..0>	25
62 25	NC_TBT_B_LSTX	TRUE	TRUE	NC_TBT_B_LSTX	25 62
69 62	NC_DP_TBTPB_ML_CP<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CP<3..1:2>	62 69
69 62	NC_DP_TBTPB_ML_CN<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CN<3..1:2>	62 69
69 62 25	NC_DP_TBTPB_AUXCH_CP	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CP	25 62 69
69 62 25	NC_DP_TBTPB_AUXCH_CN	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CN	25 62 69
25	TP_DP_TBTSRC_ML_CP<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3>	
25	TP_DP_TBTSRC_ML_CN<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3>	
25	TP_DP_TBTSRC_ML_CP<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<2>	
25	TP_DP_TBTSRC_ML_CN<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<2>	
62 25	NC_DP_TBTSRC_ML_CP<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<1>	25 62
62 25	NC_DP_TBTSRC_ML_CN<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<1>	25 62
25	TP_DP_TBTSRC_ML_CP<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<0>	
25	TP_DP_TBTSRC_ML_CN<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<0>	
62 25	NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP	25 62
62 25	NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN	25 62

TBT

Unused nets with offpage

(Nets with offpages not used on this project)

HDD_PWR_EN	15
WOL_EN	14
BT_PWRRST_L	15
HDMITBTMUX_FLAG_L	15
FW_PWR_EN	15
FW_PME_L	15
ENET_MEDIA_SENSE	15
LCD_PSR_EN	15
LCD_IRQ_L	15
ODD_PWR_EN_L	13
ENET_LOW_PWR	13
AUD_IP_PERIPHERAL_DET	13
AUD_I2C_INT_L	13
AUD_IPHS_SWITCH_EN	13

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: Func Test / No Test

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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NO_TEST Nets

		NO_TEST	MAKE_BASE			
66 63 14	NC_USB3RPCIE_SD_D2RP	=	TRUE	TRUE	NC_USB3RPCIE_SD_D2RP	14 63 66
66 63 14	NC_USB3RPCIE_SD_D2RN	=	TRUE	TRUE	NC_USB3RPCIE_SD_D2RN	14 63 66
66 63 14	NC_USB3RPCIE_SD_R2D_CP	=	TRUE	TRUE	NC_USB3RPCIE_SD_R2D_CP	14 63 66 — CPU/PCH
66 63 14	NC_USB3RPCIE_SD_R2D_CN	=	TRUE	TRUE	NC_USB3RPCIE_SD_R2D_CN	14 63 66
63 37 35	NC_SMC_ADC16	=	TRUE	TRUE	NC_SMC_ADC16	35 37 63 — SMC

Power Aliases

63 62 60 56 39 38 34 19 18 15	PP3V3_S3	=	PP3V3_S3 15 18 19 34 38 39 56 60 62 63

Functional Test Points

J9500: LIO Connector

FUNC_TEST		
TRUE	AUD_PWR_EN	13 57 59
TRUE	PP5V_S0_ALT_AUD_LDO_EN	59
TRUE	SPKRAMP_SHDN_L	45 59
TRUE	PP1V5_S0SW_AUDIO	56 59
TRUE	PP3V3_S0	60 62 72
TRUE	SPKRAMP_INR_N	5 11 12 13 15 17 18 27 30 34 36 37 38 39 40 41 42 43 54 57 59
TRUE	SPKRAMP_INR_P	45 59 72
TRUE	USB3_EXTB_D2R_RC_N	45 59 72
TRUE	USB3_EXTB_D2R_RC_P	59 63 66
TRUE	USB_EXTB_N	59 63 66
TRUE	USB_EXTB_P	14 59 66
TRUE	USB3_EXTB_R2D_N	14 59 66
TRUE	USB3_EXTB_R2D_P	59 63 66
TRUE	PP3V42_G3H	59 63 66
TRUE	SMBUS_SMC_2_S3_SCL	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	SMBUS_SMC_2_S3_SDA	35 38 59 71
TRUE	SYS_ONEWIRE	35 38 59 71
TRUE	SMC_BC_ACOK	35 59
TRUE	XDP_USB_EXTB_OC_L	35 36 48 59
TRUE	USB_PWR_EN	14 16 59
TRUE	FINSTACKSNS_ALERT_L	33 57 59
TRUE		37 59
TRUE	HDA_SYNC	12 59 67
TRUE	HDA_RST_L	12 59 67
TRUE	HDA_SDOUT	12 59 67
TRUE	HDA_SDIN0	12 59 67
TRUE	HDA_BIT_CLK	12 59 67

(Need to add 5 GND TPs)

J6955: HALL EFFECT Connector

FUNC_TEST		
TRUE	SMC_LID_R	46
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63

Bead Probes

66 59 14	USB3_EXTB_D2R_N	1	TP_SM	BEAD-PROBE	BPA511
66 59 14	USB3_EXTB_D2R_P	1	TP_SM	BEAD-PROBE	BPA510
66 63 59	USB3_EXTB_D2R_RC_N	1	TP_SM	BEAD-PROBE	BPA520
66 63 59	USB3_EXTB_D2R_RC_P	1	TP_SM	BEAD-PROBE	BPA521
66 59 14	USB3_EXTB_R2D_C_N	1	TP_SM	BEAD-PROBE	BPA513
66 59 14	USB3_EXTB_R2D_C_P	1	TP_SM	BEAD-PROBE	BPA512
66 63 59	USB3_EXTB_R2D_N	1	TP_SM	BEAD-PROBE	BPA523
66 63 59	USB3_EXTB_R2D_P	1	TP_SM	BEAD-PROBE	BPA522

Unused nets with offpage

(Nets with offpages not used on this project)

SD_RESET_L	15
XDP_SDCONN_STATE_CHANGE_L	15 16
SD_PWR_EN	15

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Project FCT/NC/Aliases

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J41/J43 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,MEM_TERM	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2,ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4,ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.110 MM	0.110 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110MM		0.095 MM	0.095 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL2,ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL3,ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL3,ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL4,ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

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PCB Rule Definitions

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

Note: DisplayPort tables are on Page 113

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	6 36
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	
	CPU_45S	CPU_TTP	XDP_DBRESET_L	16 17
	CPU_45S	CPU_TTP	XDP_CPU_PRDY_L	6 16 62
	CPU_45S	CPU_TTP	XDP_CPU_PREQ_L	6 16 62
	CPU_27P4S	CPU_COMP	EDP_COMP	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	6
	CPU_45S	CPU_TTP	CPU_CFG<11..0>	6 16 62
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 35
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 35 36 49
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	15 36
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
XDP_TDI	CPU_45S	CPU_TTP	XDP_CPU_TDI	6 16 62
XDP_TDO	CPU_45S	CPU_TTP	XDP_CPU_TDO	6 16 62
XDP_TMS	CPU_45S	CPU_TTP	XDP_CPU_TMS	6 16 62
XDP_TCK	CPU_45S	CPU_TTP	XDP_CPU_TCK	6 16 62
XDP_TRST_L	CPU_45S	CPU_TTP	XDP_CPUPCH_TRST_L	6 12 16 62
XDP_BPM_L	CPU_45S	CPU_TTP	XDP_BPM_L<1..0>	6 16
	CPU_45S	CPU_TTP	XDP_BPM_L<7..2>	6 16
	CPU_45S	CPU_TTP	XDP_OBSDATA_B<3..0>	
	CPU_45S	CPU_TTP	CPU_CFG<15..12>	6 16
(FSB_CPURST_L)	CPU_45S	CPU_TTP	XDP_CPURST_L	16
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 49
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 49
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	8 49
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	8 49
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	8 49
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	12 30
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	12 30
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	30 62
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	30 62
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	12 30 62
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 30 62
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	5 25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	5 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	13 25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	13 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	5 18 25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	5 18 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	13 18 25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	13 18 25
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	58 62
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	58 62
	DP_80D	DP_TX	DP_INT_ML_C_P<3..0>	5 58 62
	DP_80D	DP_TX	DP_INT_ML_C_N<3..0>	5 58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 58
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 58
	DP_80D	DP_AUX	DP_INT_AUXCH_P	
	DP_80D	DP_AUX	DP_INT_AUXCH_N	

PCIe SSD

DP

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CPU Constraints

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	
USB_BT	USB_80D	USB	USB_BT_P	14 29
USB_BT	USB_80D	USB	USB_BT_N	14 29
	USB_80D	USB	USB_BT_CONN_P	29 62
	USB_80D	USB	USB_BT_CONN_N	29 62
	USB_80D	USB	USB_BT_WAKE_P	
	USB_80D	USB	USB_BT_WAKE_N	
USB_TPAD	USB_80D	USB	USB_TPAD_P	14 34 62
USB_TPAD	USB_80D	USB	USB_TPAD_N	14 34 62
	USB_80D	USB	USB_TPAD_CONN_P	
	USB_80D	USB	USB_TPAD_CONN_N	
	USB_80D	USB	TPAD_SPI_MOSI_USB_P	
	USB_80D	USB	TPAD_SPI_MISO_USB_N	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	
	SPI_45S	SPI	TPAD_SPI_MOSI	15 34
	SPI_45S	SPI	TPAD_SPI_MISO	15 34
	SPI_45S	SPI	TPAD_SPI_CLK	15 34
USB_EXTA	USB_80D	USB	USB_EXTA_P	14 33
USB_EXTA	USB_80D	USB	USB_EXTA_N	14 33
	UART_45S	UART	SMC_DEBUGPRT_TX_L	33 35 36
	UART_45S	UART	SMC_DEBUGPRT_RX_L	33 35 36
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_P	33
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_N	33
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_P	33
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_N	33
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_P	14 33
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_N	14 33
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_P	33
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_N	33
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_P	
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_P	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_P	14 33
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_N	14 33
USB_EXTB	USB_80D	USB	USB_EXTB_P	14 59 63
USB_EXTB	USB_80D	USB	USB_EXTB_N	14 59 63
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_P	14 59 63
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_N	14 59 63
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_P	59 63
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_N	59 63
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P	59 63
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N	59 63
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_P	14 59 63
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_N	14 59 63
USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RP	14 63
USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RN	14 63
USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CP	14 63
USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CN	14 63
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P	
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N	
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P	
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	14
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	

USB Hucopyb nets

TP SPI nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

SYNC_MASTER=CLEAN_J41 SYNC_DATE=11/13/2012

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 35 44 62
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	14 35 44 62
	LPC_45S	LPC	LPCPLUS_RESET_L	18 44 62
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 35
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	17 44 62
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS_R	12 17
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	14 16 19 25 38 54
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	14 16 19 25 38 54
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	14 38
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	14 38
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 35 38 41 42 62
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 35 38 41 42 62
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 59 63
	HDA_45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 59 63
	HDA_45S	HDA	HDA_SYNC_R	12
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	12
	HDA_45S	HDA	HDA_RST_L	12 59 63
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	12 59 63
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 59 63
	HDA_45S	HDA	HDA_SDOUT_R	12 17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	13 36
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	35 36
SPI_CLK	SPI_45S	SPI	SPI_CLK_R	14 44
	SPI_45S	SPI	SPI_CLK	44
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R	14 44
	SPI_45S	SPI	SPI_MOSI	44
SPI_MISO	SPI_45S	SPI	SPI_MISO	14 44
	SPI_45S	SPI	SPI_MISO_R	44
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L	14 44
	SPI_45S	SPI	SPI_CS0_L	44
	SPI_45S	SPI	SPI_SMC_CLK	35 44
	SPI_45S	SPI	SPI_SMC_MOSI	35 44
	SPI_45S	SPI	SPI_SMC_MISO	35 44
	SPI_45S	SPI	SPI_SMC_CS_L	35 44
	SPI_45S	SPI	SPI_MLB_CLK	44
	SPI_45S	SPI	SPI_MLB_MOSI	44
	SPI_45S	SPI	SPI_MLB_MISO	44
	SPI_45S	SPI	SPI_MLB_CS_L	44
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	29 62
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	29 62
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	14 29
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	14 29
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	14 29 62
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	14 29 62
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	12 29 62
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	12 29 62
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	25
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	14 25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	14 25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	12 25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	12 25
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P	
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N	
XDP_TDI	PCH_45S	PCH_TTP	XDP_PCH_TDI	12 16 62
XDP_TDO	PCH_45S	PCH_TTP	XDP_PCH_TDO	12 16 62
XDP_TMS	PCH_45S	PCH_TTP	XDP_PCH_TMS	12 16 62
XDP_TCK	PCH_45S	PCH_TTP	XDP_PCH_TCK	12 16 62
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P	31 32
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N	31 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P	14 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N	14 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P	31 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N	31 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	12 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	12 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	31 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	31 32

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1	
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	17 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP	31 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	31 32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	17 25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	25
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	17
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2	
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R	
	CLK_25M_45S	CLK_25M	SDSCLK_CLK25M_X1	

SYNC_MASTER=J43_MLB SYNC_DATE=09/14/2012

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_CS_L<1..0>
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_ODT<0>
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_CS_L<1..0>
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_ODT<0>
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DQ<7..0>
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DQ<15..8>
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DQ<23..16>
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DQ<31..24>
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DQ<39..32>
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DQ<47..40>
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DQ<55..48>
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DQ<63..56>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_N<7>
		MEM_PWR	PP1V2_S3
		MEM_PWR	PP0V6_S3_MEM_VREFCA_A
		MEM_PWR	PP0V6_S3_MEM_VREFDQ_A
		MEM_PWR	PP0V6_S3_MEM_VREFCA_B
		MEM_PWR	PP0V6_S3_MEM_VREFDQ_B

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0> 25 28
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0> 25 28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0> 28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0> 28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1> 25 28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1> 25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3> 25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3> 25 28
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2> 28
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2> 28
	DP_80D	DP_TX	DP_A_LSX_ML_P<1> 28
	DP_80D	DP_TX	DP_A_LSX_ML_N<1> 28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0> 28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0> 28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1> 25 28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1> 25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0> 25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0> 25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P 25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N 25 28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P 28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N 28
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P 28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N 28
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0> 62
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0> 62
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CP<3..1:2> 62
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CN<3..1:2> 62
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0> 62
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0> 62
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CP 25 62
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CN 25 62
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 25
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 25
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 25
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 25

Only used on hosts supporting Thunderbolt video-in

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 31 32
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 31 32
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 31 32
	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 31 32
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 32 62
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 32 62
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 31 32
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 32 62
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 32 62
		S2_MEM_PWR	PP1V35_CAM 31 32
		S2_MEM_PWR	PP0V675_CAM_VREF 31 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ 32

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
2TO1_DIFFPAIR	*	=STANDARD	0.2 MM	0.1 MM	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL 35 38 58
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA 35 38 58
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL 14 32 35 38 41 42 62 67
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA 14 32 35 38 41 42 62 67
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL 35 38 59 63
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA 35 38 59 63
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL 34 35 38 42 62
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA 34 35 38 42 62
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL 35 38 46 48 62
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA 35 38 46 48 62

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SENSE_DIFFPAIR			CHGR_CSI_P 48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSI_N 48
	2TO1_DIFFPAIR		CHGR_CSI_R_P 48
	2TO1_DIFFPAIR		CHGR_CSI_R_N 48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_P 48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_N 48
	2TO1_DIFFPAIR		CHGR_CSO_R_P 41 48
	2TO1_DIFFPAIR		CHGR_CSO_R_N 41 48

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1TO1_DIFFPAIR	0.200 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
THERM_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SPKR_DIFFPAIR	*	=1TO1_DIFFPAIR	0.300 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_N	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_P	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_N	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N	42
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P	40 50
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N	40 50
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_P	40 50
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_N	40 50
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P_R	40 41
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N_R	40 41
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_P	40
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_N	40
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_P	40
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_N	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_N	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_P	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_P	39
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_P	40 53
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_N	40 53
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	39 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	39 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_N	39 51
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_P	39 51
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_P	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_N	41 42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_P	41 42
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	45 59 63
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	45 59 63
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_P	45
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_N	45
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	45 62
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	45 62
		SB_POWER	PP3V3_S5	8 11 13 15 16 17 18 28 29 40 52 55 56 57 58 60 62
		SB_POWER	PP3V3_S0	8 11 12 13 15 17 18 27 30 34 36 37 38 39 40 41 42 43 54 57 59
	GND		GND	

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