

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

| REV | ECN | DESCRIPTION OF REVISION | CK APPD | DATE |
|-----|------------|-------------------------|---------|------------|
| 2 | 0001669557 | ENGINEERING RELEASED | | 2012-10-14 |

X155 PROTO1 SINGLE_BRD

Mon Oct 8 11:06:07 2012

| PDF PAGE | CSA PAGE | CONTENTS | SYNC MASTER | DATE |
|----------|----------|------------------------------|-------------|------|
| 2 | 2 | H5P JTAG, USB ,PLL | N/A | N/A |
| 3 | 3 | H5P GPIO & CONTROL | N/A | N/A |
| 4 | 4 | H5P IO POWER | N/A | N/A |
| 5 | 5 | H5P SOC/CPU/SRAM PWR | N/A | N/A |
| 6 | 6 | H5P W/ NAND | N/A | N/A |
| 7 | 7 | H5P VIDEO | N/A | N/A |
| 8 | 8 | BUTTON FLEX B2B | N/A | N/A |
| 9 | 9 | L67 AUDIO CODEC (1/2) | N/A | N/A |
| 10 | 10 | L67 AUDIO CODEC (2/2) | N/A | N/A |
| 11 | 11 | CG FLEX B2B | N/A | N/A |
| 12 | 12 | AGATHA PMU(1/2) | N/A | N/A |
| 13 | 13 | AGATHA PMU(2/2) | N/A | N/A |
| 14 | 14 | CHESTNUT + BACKLIGHT DRIVER | N/A | N/A |
| 15 | 15 | SPKR AMP + LED DRIVER | N/A | N/A |
| 16 | 16 | TRISTAR | N/A | N/A |
| 17 | 17 | DOCKFLEX B2B | N/A | N/A |
| 18 | 18 | D404 (TOUCH B2B, DRIVER ICS) | N/A | N/A |
| 19 | 19 | LCM CONNECTOR | N/A | N/A |
| 20 | 20 | SENSORS | N/A | N/A |
| 21 | 21 | CAM0 CONNECTOR | N/A | N/A |
| 22 | 22 | BATT B2B, TPS, PD FEATURES | N/A | N/A |
| 23 | 23 | RADIO_MLB HIERARCH. SYMBOL | N/A | N/A |

TO DO: CLEANUP ALTERNATES FOR X155

ALTERNATES

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|-------------|---------------------------|------------|---------|----------------------|
| 138S0648 | 138S0652 | ALTERNATE | ? | 4.7UF CERM 0402 6.3V |
| 339S0177 | 339S0176 | ALTERNATE | ? | H5P ALTERNATE |
| 339S0178 | 339S0176 | ALTERNATE | ? | H5P ALTERNATE |

X155 BOM CALLOUTS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|-------------------------|-------------------------|----------|------------|
| 051-9584 | 1 | SCH, SINGLE_BRD, X155 | SCH | Y | ? |
| 820-3329 | 1 | PCB, SINGLE_BRD, X155 | PCB | Y | ? |
| 825-6838 | 1 | LABEL FOR X155 639-3796 | EEEE_F284 | Y | EEEE_16G |

COMPASS BOM OPTIONS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|-----------------------|-------------------------|----------|-------------|
| 639-4024 | 1 | ST GYRO - COMPASS POP | U16 | Y | COMPASS_POP |

NAND BOM OPTIONS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|--------------------------------|-------------------------|----------|------------|
| 335S0878 | 1 | NAND, 19NM, 16GX8, MLC, PPN1.5 | U4 | Y | NAND_16G |

HORIZONTAL CAP BOM OPTIONS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|----------------------------|--------------------------|----------|----------------|
| 138S0801 | 5 | HRZN CAPS_1:10UF,0402,6.3V | C422,C74,C92,C250,C265 | Y | HRZN_CAP_GRP1 |
| 138S0801 | 5 | HRZN CAPS_1:10UF,0402,6.3V | C293,C294,C257,C299,C262 | Y | HRZN_CAP_GRP2 |
| 138S0801 | 5 | HRZN CAPS_1:10UF,0402,6.3V | C264,C378,C189,C203,C245 | Y | HRZN_CAP_GRP3 |
| 138S0801 | 5 | HRZN CAPS_1:10UF,0402,6.3V | C190,C204,C239,C246,C195 | Y | HRZN_CAP_GRP4 |
| 138S0801 | 5 | HRZN CAPS_1:10UF,0402,6.3V | C205,C243,C247,C252,C297 | Y | HRZN_CAP_GRP5 |
| 138S0801 | 5 | HRZN CAPS_1:10UF,0402,6.3V | C386,C387,C333,C332,C335 | Y | HRZN_CAP_GRP6 |
| 138S0801 | 3 | HRZN CAPS_1:10UF,0402,6.3V | C42_RF,C43_RF,C44_RF | Y | HRZN_CAP_GRP7 |
| 138S0801 | 1 | HRZN CAPS_1:10UF,0402,6.3V | C1201_RF | Y | HRZN_CAP_GRP8 |
| 138S0801 | 4 | HRZN CAPS_1:10UF,0402,6.3V | C182,C307,C209,C187 | Y | HRZN_CAP_GRP10 |
| 138S0794 | 2 | HRZN CAPS_1:10UF,0402,10V | C52,C156 | Y | HRZN_CAP_GRP11 |
| 138S0582 | 1 | 4.7UF 0.55MM HEIGHT | C193 | Y | LOW_Z_CAP |

BOARD ID RADIO BOM OPTIONS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|----------------|-------------------------|----------|------------|
| 118S0621 | 1 | 1.00M 1% 01005 | R25_RF | Y | N51_CFG_A |
| 118S0732 | 1 | 50K 1% 01005 | R26_RF | Y | N51_CFG_A |
| 117S0159 | 1 | 470K 5% 01005 | R25_RF | Y | N51_CFG_B |
| 118S0626 | 1 | 100K 1% 01005 | R26_RF | Y | N51_CFG_B |
| 118S0626 | 1 | 100K 1% 01005 | R25_RF | Y | N53_CFG_A |
| 118S0726 | 1 | 162K 1% 01005 | R26_RF | Y | N53_CFG_A |
| 118S0626 | 1 | 100K 1% 01005 | R25_RF | Y | N53_CFG_B |
| 118S0623 | 1 | 267K 1% 01005 | R26_RF | Y | N53_CFG_B |
| 118S0659 | 1 | 255K 1% 01005 | R25_RF | Y | N48_CFG_A |
| 118S0626 | 1 | 100K 1% 01005 | R26_RF | Y | N48_CFG_A |
| 118S0689 | 1 | 147K 1% 01005 | R25_RF | Y | N48_CFG_B |
| 118S0626 | 1 | 100K 1% 01005 | R26_RF | Y | N48_CFG_B |
| 118S0626 | 1 | 100K 1% 01005 | R25_RF | Y | N49_CFG_A |
| 118S0650 | 1 | 499K 1% 01005 | R26_RF | Y | N49_CFG_A |
| 118S0732 | 1 | 50K 1% 01005 | R25_RF | Y | N49_CFG_B |
| 118S0621 | 1 | 1.00M 1% 01005 | R26_RF | Y | N49_CFG_B |

GYRO BOM OPTIONS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|------------------|-------------------------|----------|------------|
| 338S1158 | 1 | ST GYRO | U8 | Y | GYRO_ST |
| 132S0391 | 1 | ST GYRO - CP CAP | C11 | Y | GYRO_ST |

CHESTNUT BOM OPTIONS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|-------------------------------|-------------------------|----------|-------------------|
| 338S1172 | 1 | TI CHESTNUT | U3 | Y | CHESTNUT_TI |
| 152S1649 | 1 | TI CHESTNUT - 1.5 UH IND | L19 | Y | CHESTNUT_TI |
| 338S1168 | 1 | INTERSIL CHESTNUT | U3 | Y | CHESTNUT_INTERSIL |
| 152S1611 | 1 | INTERSIL CHESTNUT -2.2 UH IND | L19 | Y | CHESTNUT_INTERSIL |

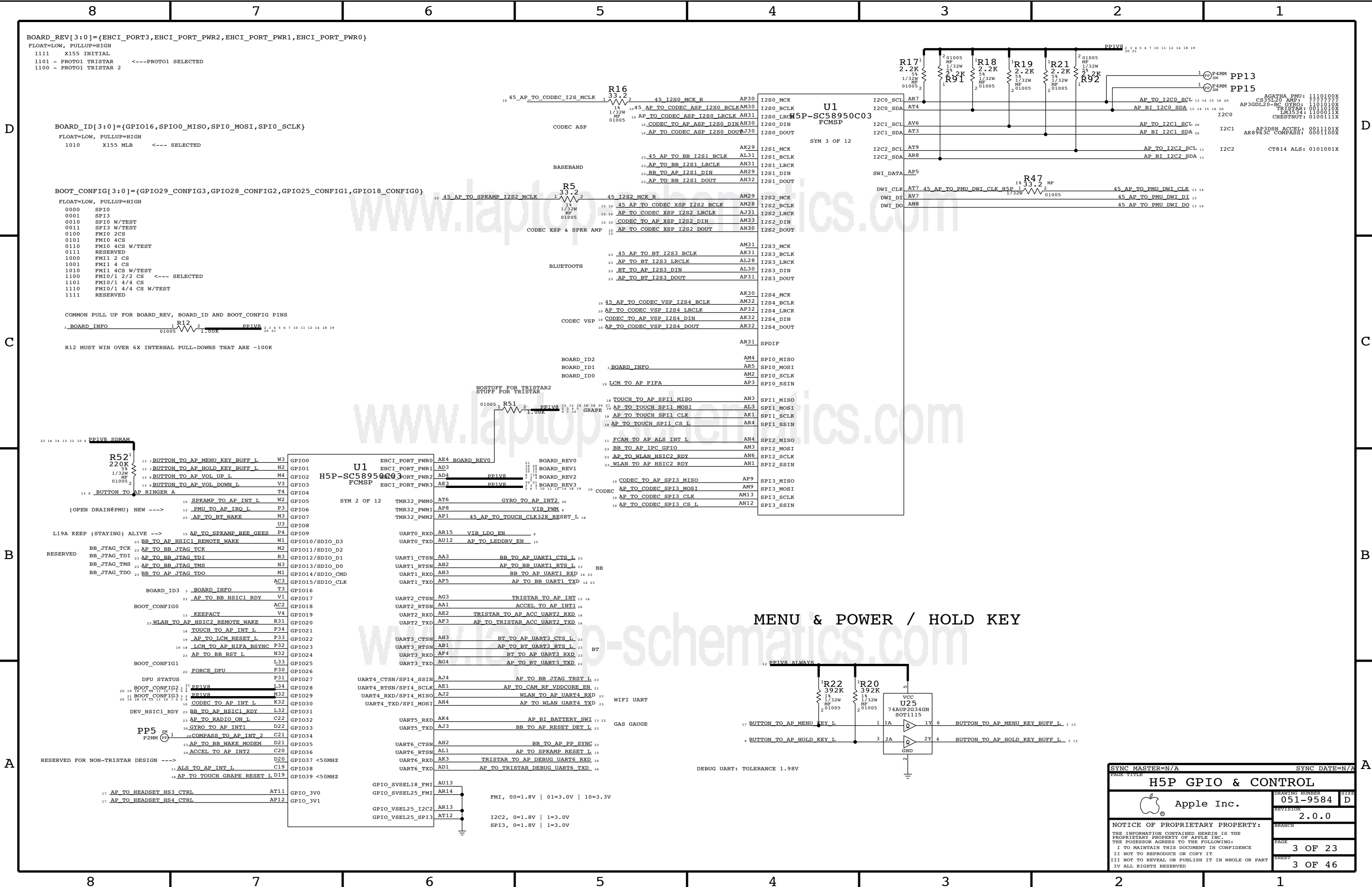
TRISTAR BOM OPTIONS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|----------------------------|-------------------------|----------|------------|
| 343S0614 | 1 | CBTL1608A1UK,WCSF,TRISTAR | U2 | Y | TRISTAR |
| 343S0639 | 1 | CBTL1610A0UK,WCSF,TRISTAR2 | U2 | Y | TRISTAR2 |
| 118S0671 | 2 | RES 150HM 01005 5% | R102,R103 | Y | TRISTAR |
| 117S0202 | 2 | RES 200HM 01005 5% | R102,R103 | Y | TRISTAR2 |

SCH 051-9584
BRD 820-3329

BOM 639-3796 X155

| | | | |
|---|--|-----------------------|----------|
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BOARD_REV[3:0]={EHCI_PORT3,EHCI_PORT_PWR2,EHCI_PORT_PWR1,EHCI_PORT_PWR0}
 FLOAT=LOW, PULLUP=HIGH
 1111 X155 INITIAL
 1101 - PROTO1 TRISTAR <---PROTO1 SELECTED
 1100 - PROTO1 TRISTAR 2

BOARD_ID[3:0]={GPIO16,SPIO0_MISO,SPIO0_MOSI,SPIO0_SCLK}
 FLOAT=LOW, PULLUP=HIGH
 1010 X155 MLB <--- SELECTED

BOOT_CONFIG[3:0]={GPIO29_CONFIG3,GPIO28_CONFIG2,GPIO25_CONFIG1,GPIO18_CONFIG0}
 FLOAT=LOW, PULLUP=HIGH
 0000 SPIO
 0001 SPI3
 0010 SPIO W/TEST
 0011 SPI3 W/TEST
 1000 FMIO 2 CS
 1001 FMIO 4 CS
 1010 FMIO 4CS W/TEST
 1100 FMIO/1 2/2 CS <--- SELECTED
 1101 FMIO/1 4/4 CS
 1110 FMIO/1 4/4 CS W/TEST
 1111 RESERVED

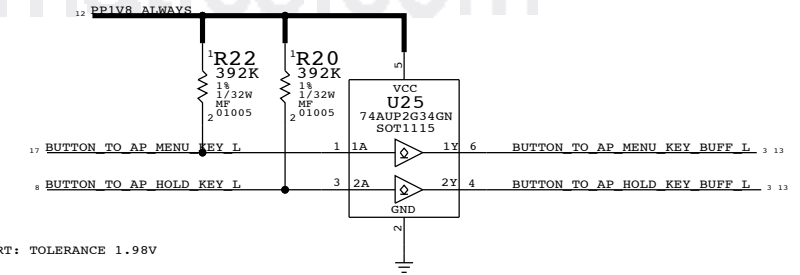
COMMON PULL UP FOR BOARD_REV, BOARD_ID AND BOOT_CONFIG PINS
 BOARD_INFO 1 R12 2 PPIVR 2,3,4,5,6,7,10,11,12,14,18,19
 R12 MUST WIN OVER 6X INTERNAL PULL-DOWNS THAT ARE ~100K

NOSTUFF FOR TRISTAR2 STUFF FOR TRISTAR
 R51 1 2 PPIVR 11,12,14,18,19,20,21 GRAPE
 R52 1 2 PPIVR SDRAM

GPIO0 EHCI_PORT_PWR0 AE4 BOARD_REV0
 GPIO1 EHCI_PORT_PWR1 AD3 BOARD_REV1
 GPIO2 EHCI_PORT_PWR2 AD4 BOARD_REV2
 GPIO3 EHCI_PORT_PWR3 AE3 BOARD_REV3
 GPIO4
 GPIO5 TMR32_PWM0 AT6 GYRO_TO_AP_INT2 20
 GPIO6 TMR32_PWM1 AP8 VIB_PWM 8
 GPIO7 TMR32_PWM2 AP1 45 AP_TO_TOUCH_CLK32K_RESET_L 18
 GPIO8
 GPIO9
 GPIO10/SDIO_D3 UART0_RXD AR15 VIB_LDO_EN 8
 GPIO11/SDIO_D2 UART0_TXD AU12 AP_TO_LEDDRVR_EN 15
 GPIO12/SDIO_D1
 GPIO13/SDIO_D0 UART1_CTSN AA3 BB_TO_AP_UART1_CTS_L 23
 GPIO14/SDIO_CMD UART1_RTSN AB2 AP_TO_BB_UART1_RTS_L 23
 GPIO15/SDIO_CLK UART1_RXD AB3 BB_TO_AP_UART1_RXD 16 23
 UART1_TXD AF5 AP_TO_BB_UART1_TXD 16 23
 GPIO16
 GPIO17 UART2_CTSN AG3 TRISTAR_TO_AP_INT1 13 16
 GPIO18 UART2_RTSN AA1 ACCEL_TO_AP_INT1 20
 GPIO19 UART2_RXD AE2 TRISTAR_TO_AP_ACC_UART2_RXD 16
 GPIO20 UART2_TXD AF3 AP_TO_TRISTAR_ACC_UART2_TXD 16
 GPIO21
 GPIO22 UART3_CTSN AH3 BT_TO_AP_UART3_CTS_L 23
 GPIO23 UART3_RTSN AB1 AP_TO_BT_UART3_RTS_L 23
 GPIO24 UART3_RXD AF4 BT_TO_AP_UART3_RXD 23
 GPIO25 UART3_TXD AG4 AP_TO_BT_UART3_TXD 23
 GPIO26
 GPIO27 UART4_CTSN/SPI4_SSN AJ4 AP_TO_BB_JTAG_TRST_L 23
 GPIO28 UART4_RTSN/SPI4_SCLK AE1 AP_TO_CAM_RF_VDDCORE_EN 21
 GPIO29 UART4_RXD/SPI4_MISO AJ2 WLAN_TO_AP_UART4_RXD 23
 GPIO30 UART4_TXD/SPI_MOSI AH4 AP_TO_WLAN_UART4_TXD 23
 GPIO31
 GPIO32 UART5_RXD AK4 AP_BI_BATTERY_SWI 13 22
 GPIO33 UART5_TXD AJ3 BB_TO_AP_RESET_DET_L 23
 GPIO34
 GPIO35 UART6_CTSN AH2 BB_TO_AP_PP_SYNC 23
 GPIO36 UART6_RTSN AL1 AP_TO_SPKAMP_RESET_L 15
 GPIO37 UART6_RXD AK3 TRISTAR_TO_AP_DEBUG_UART6_RXD 16
 GPIO38 UART6_TXD AD1 AP_TO_TRISTAR_DEBUG_UART6_TXD 16
 GPIO39 <50MHZ
 GPIO_SVSEL18_FMI AU13
 GPIO_SVSEL25_FMI AR14
 GPIO_VSEL25_I2C2 AR13
 GPIO_VSEL25_SPI3 AT12

| | | | | | |
|----------------------------------|-----|------|--------------------------|------|------------|
| 10 45 AP TO CODEC I2S MCLK | R16 | 33 2 | 45 I2S0 MCK R | AP30 | I2S0_MCK |
| 10 45 AP TO CODEC ASP I2S0 BCLK | | | 45 I2S0 BCLK | AM30 | I2S0_BCLK |
| 10 45 AP TO CODEC ASP I2S0 LRCLK | | | 45 I2S0 LRCLK | AM31 | I2S0_LRCLK |
| 10 45 AP TO CODEC ASP I2S0 DIN | | | 45 I2S0 DIN | AM32 | I2S0_DIN |
| 10 45 AP TO CODEC ASP I2S0 DOUT | | | 45 I2S0 DOUT | AM33 | I2S0_DOUT |
| 23 45 AP TO BB I2S1 BCLK | | | 45 I2S1 BCLK | AL31 | I2S1_BCLK |
| 23 45 AP TO BB I2S1 LRCLK | | | 45 I2S1 LRCLK | AL32 | I2S1_LRCLK |
| 23 45 AP TO BB I2S1 DIN | | | 45 I2S1 DIN | AL33 | I2S1_DIN |
| 23 45 AP TO BB I2S1 DOUT | | | 45 I2S1 DOUT | AL34 | I2S1_DOUT |
| 15 45 AP TO CODEC XSP I2S2 BCLK | | | 45 I2S2 BCLK | AM28 | I2S2_BCLK |
| 15 45 AP TO CODEC XSP I2S2 LRCLK | | | 45 I2S2 LRCLK | AJ31 | I2S2_LRCLK |
| 15 45 AP TO CODEC XSP I2S2 DIN | | | 45 I2S2 DIN | AM33 | I2S2_DIN |
| 15 45 AP TO CODEC XSP I2S2 DOUT | | | 45 I2S2 DOUT | AM30 | I2S2_DOUT |
| 23 45 AP TO BT I2S3 BCLK | | | 45 I2S3 BCLK | AM31 | I2S3_BCLK |
| 23 45 AP TO BT I2S3 LRCLK | | | 45 I2S3 LRCLK | AL28 | I2S3_LRCLK |
| 23 45 AP TO BT I2S3 DIN | | | 45 I2S3 DIN | AL30 | I2S3_DIN |
| 23 45 AP TO BT I2S3 DOUT | | | 45 I2S3 DOUT | AP31 | I2S3_DOUT |
| 10 45 AP TO CODEC VSP I2S4 BCLK | | | 45 I2S4 BCLK | AM32 | I2S4_BCLK |
| 10 45 AP TO CODEC VSP I2S4 LRCLK | | | 45 I2S4 LRCLK | AP32 | I2S4_LRCLK |
| 10 45 AP TO CODEC VSP I2S4 DIN | | | 45 I2S4 DIN | AK32 | I2S4_DIN |
| 10 45 AP TO CODEC VSP I2S4 DOUT | | | 45 I2S4 DOUT | AR32 | I2S4_DOUT |
| 10 LCM TO AP PIFA | | | 10 LCM TO AP PIFA | AP3 | SPIO_SSN |
| 18 TOUCH TO AP SPI1 MISO | | | 18 TOUCH TO AP SPI1 MISO | AN3 | SPI1_MISO |
| 21 AP TO TOUCH SPI1 MOSI | | | 21 AP TO TOUCH SPI1 MOSI | AL3 | SPI1_MOSI |
| 18 AP TO TOUCH SPI1 CLK | | | 18 AP TO TOUCH SPI1 CLK | AK1 | SPI1_SCLK |
| 18 AP TO TOUCH SPI1 CS L | | | 18 AP TO TOUCH SPI1 CS L | AR4 | SPI1_SSN |
| 11 FCAM TO AP ALS INT L | | | 11 FCAM TO AP ALS INT L | AN4 | SPI2_MISO |
| 23 BB TO AP IPC GPIO | | | 23 BB TO AP IPC GPIO | AM3 | SPI2_MOSI |
| 23 AP TO WLAN HSIC2 RDY | | | 23 AP TO WLAN HSIC2 RDY | AN6 | SPI2_SCLK |
| 23 WLAN TO AP HSIC2 RDY | | | 23 WLAN TO AP HSIC2 RDY | AN1 | SPI2_SSN |
| 10 CODEC TO AP SPI3 MISO | | | 10 CODEC TO AP SPI3 MISO | AP9 | SPI3_MISO |
| 10 AP TO CODEC SPI3 MOSI | | | 10 AP TO CODEC SPI3 MOSI | AM9 | SPI3_MOSI |
| 10 AP TO CODEC SPI3 CLK | | | 10 AP TO CODEC SPI3 CLK | AM13 | SPI3_SCLK |
| 10 AP TO CODEC SPI3 CS L | | | 10 AP TO CODEC SPI3 CS L | AN12 | SPI3_SSN |

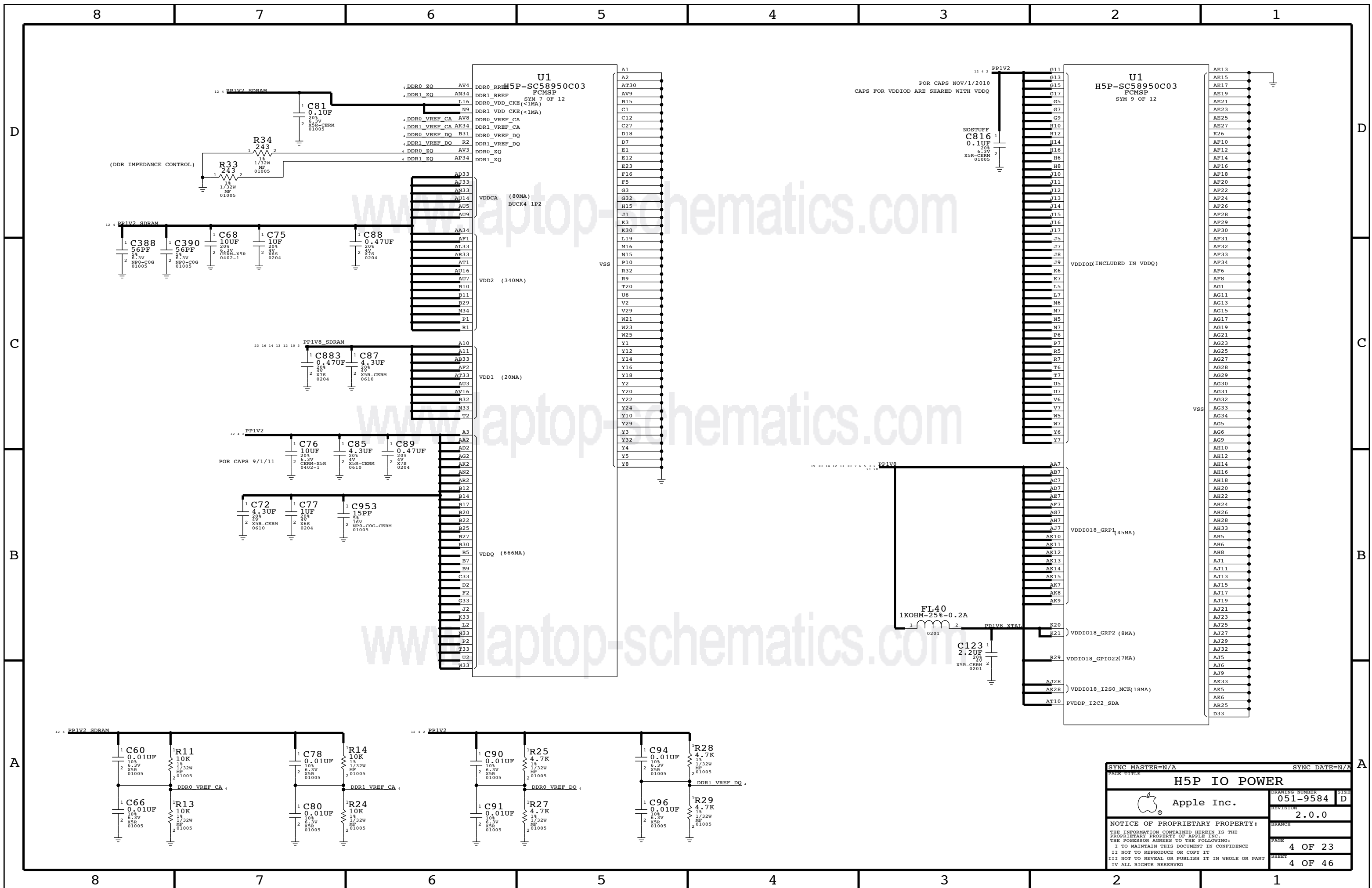
MENU & POWER / HOLD KEY



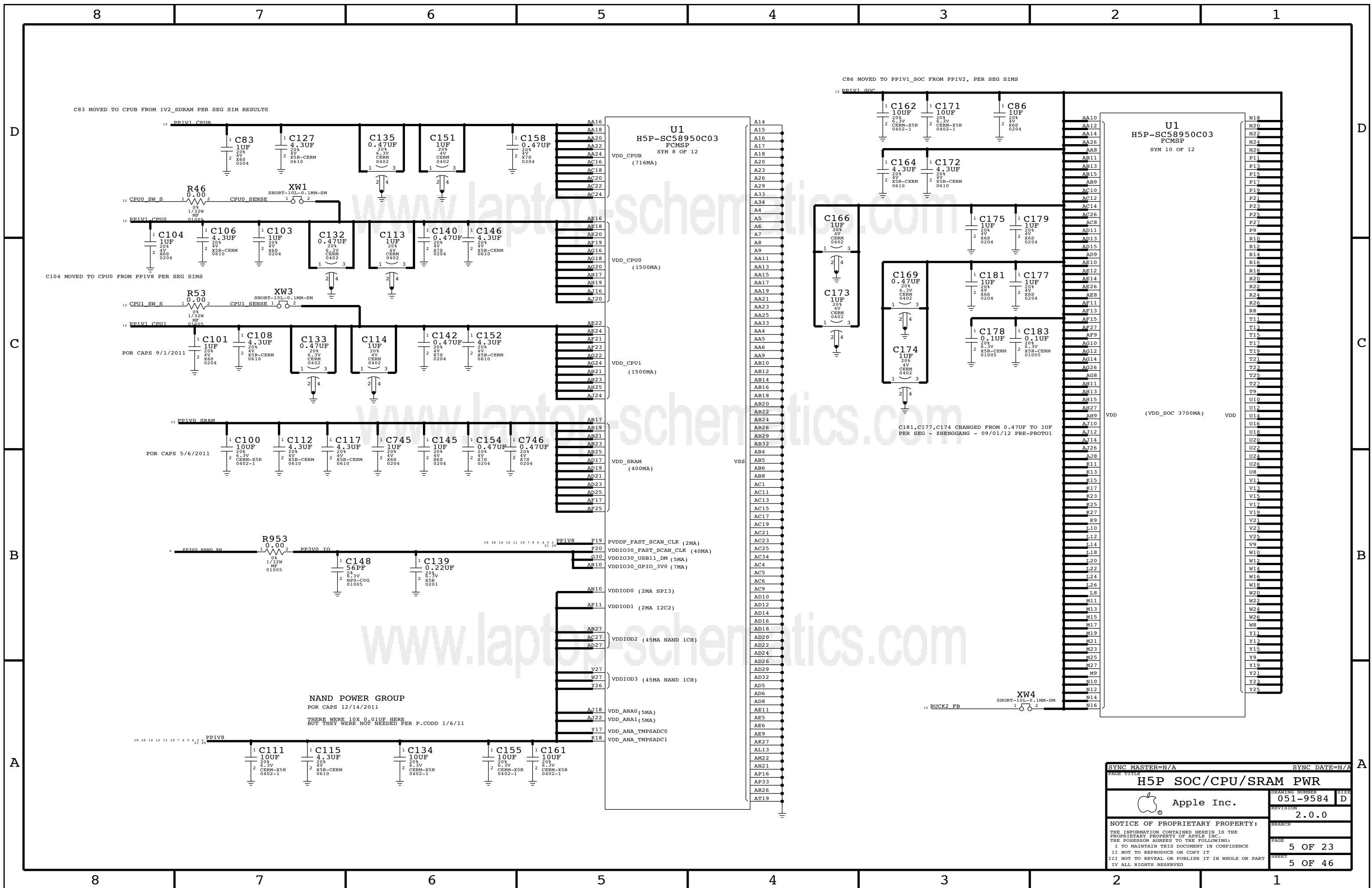
DEBUG UART: TOLERANCE 1.98V

FMI, 00=1.8V | 01=3.0V | 10=3.3V
 I2C2, 0=1.8V | 1=3.0V
 SPI3, 0=1.8V | 1=3.0V

| | | | | | |
|---|--|-----------------|--|----------------|------|
| PAGE TITLE | | SYNC MASTER=N/A | | SYNC DATE=N/A | |
| H5P GPIO & CONTROL | | | | DRAWING NUMBER | SIZE |
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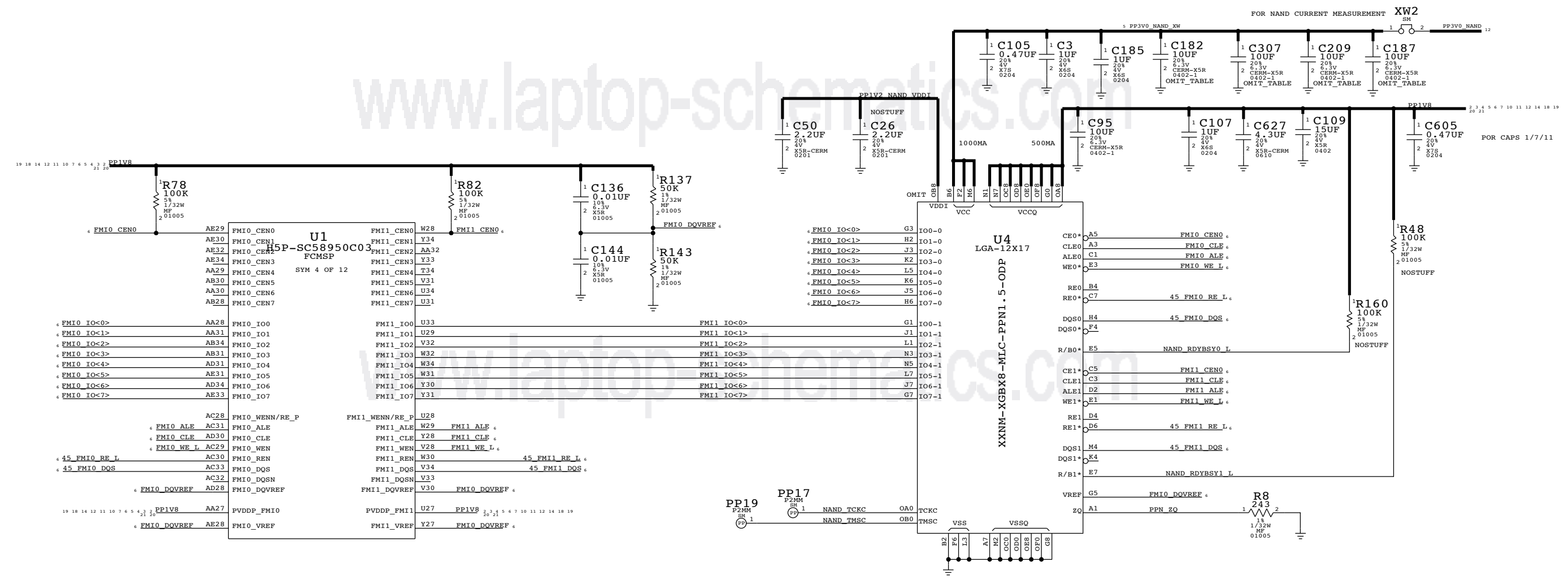


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| H5P IO POWER | | | |
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| | | 4 OF 46 | |



| | | | |
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| H5P SOC/CPU/SRAM PWR | | | |
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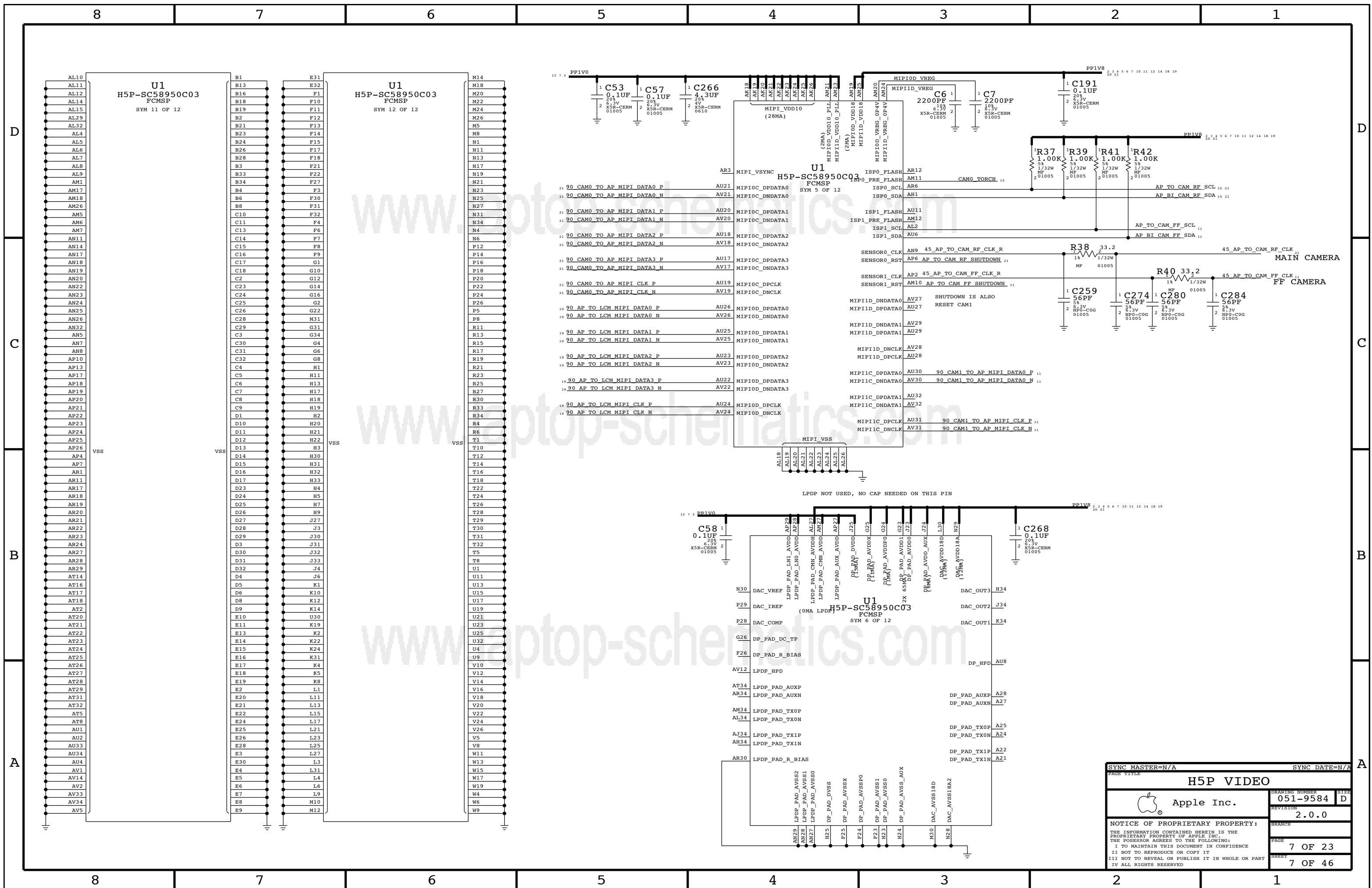
NAND



- PP2 P4MM SH 1 FMIO IO<0>
- PP3 P4MM SH 1 45 FMIO RE L
- PP14 P4MM SH 1 45 FMIO DQS

NOTE: NAND PADS SHOULD BE SHIELDED FROM TRACES WITH A GROUND PLANE

| | | | |
|---|--|----------------|----------|
| SYNC MASTER=N/A | | SYNC DATE=N/A | |
| H5P W/ NAND | | | |
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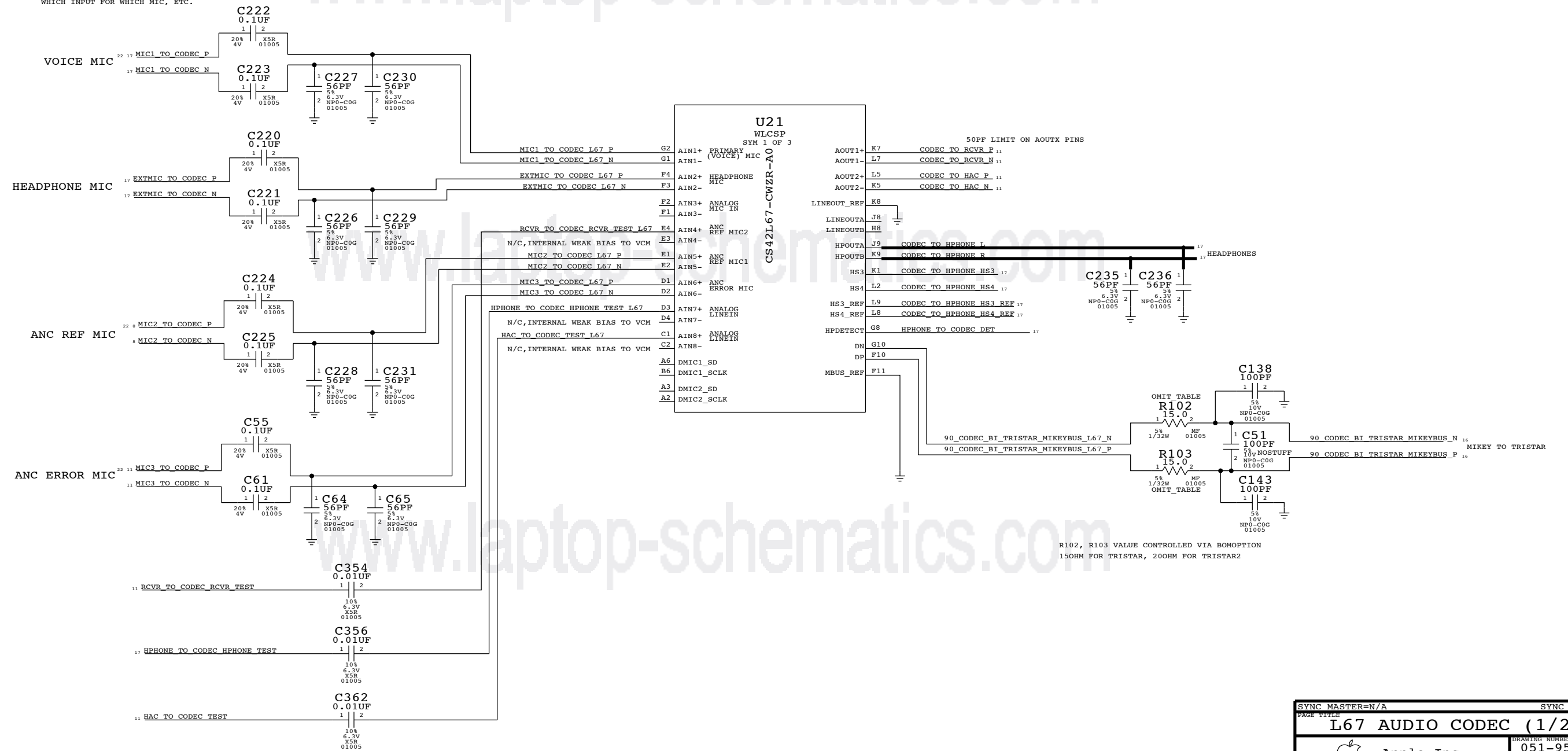
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| | | PAGE | 7 OF 23 |
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L67 AUDIO CODEC

AUDIO I/O

(ANALOG MIC IN, DIG MIC IN, HPOUT, LINEOUT, RECEIVER OUT, MIKEYBUS)

TO DO: REVIEW AUDIO MIC PATHS,
WHICH BIAS OUTPUT USED FOR WHICH MIC,
WHICH INPUT FOR WHICH MIC, ETC.



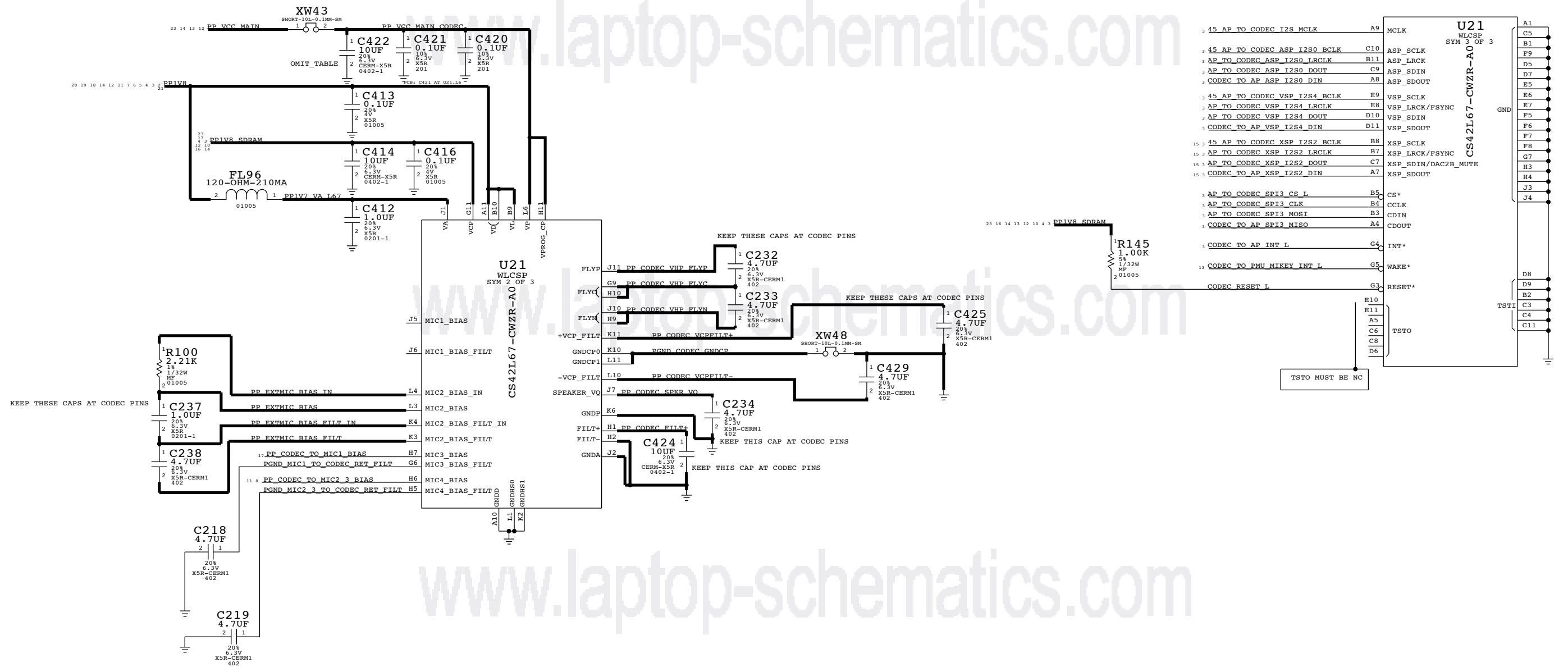
R102, R103 VALUE CONTROLLED VIA BMOPTION
150HM FOR TRISTAR, 200HM FOR TRISTAR2

| | | | |
|---|--|----------------------------|------------------|
| SYNC MASTER=N/A | | SYNC DATE=N/A | |
| PAGE TITLE L67 AUDIO CODEC (1/2) | | | |
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L67 AUDIO CODEC

POWER, MICBIAS

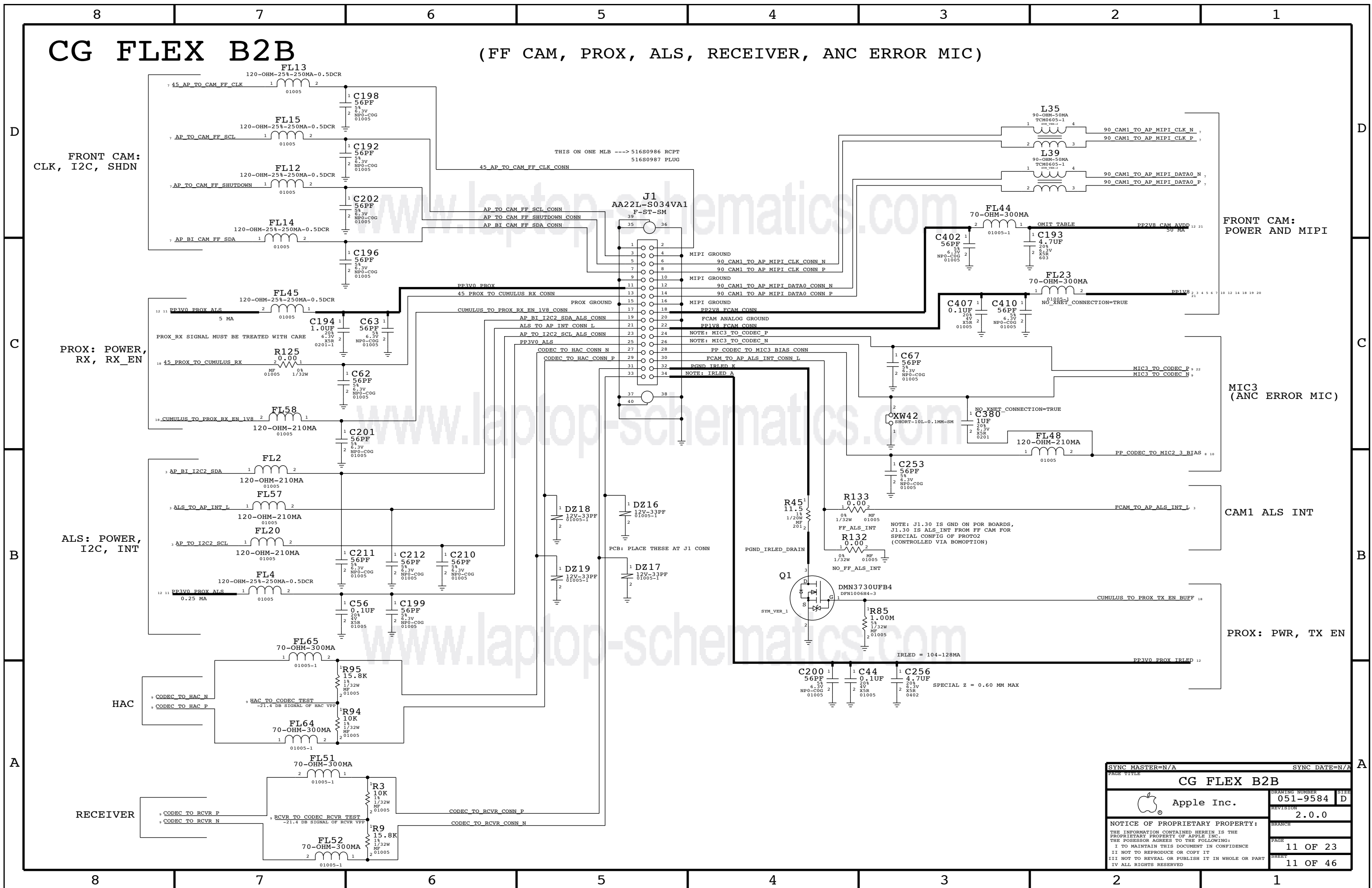
DIGITAL SYSTEM I/O



| | | | |
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| SYNC MASTER=N/A | | SYNC DATE=N/A | |
| PAGE TITLE L67 AUDIO CODEC (2/2) | | | |
| DRAWING NUMBER 051-9584 | | SIZE D | |
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CG FLEX B2B

(FF CAM, PROX, ALS, RECEIVER, ANC ERROR MIC)



FRONT CAM:
CLK, I2C, SHDN

FRONT CAM:
POWER AND MIPI

PROX: POWER,
RX, RX_EN

MIC3
(ANC ERROR MIC)

ALS: POWER,
I2C, INT

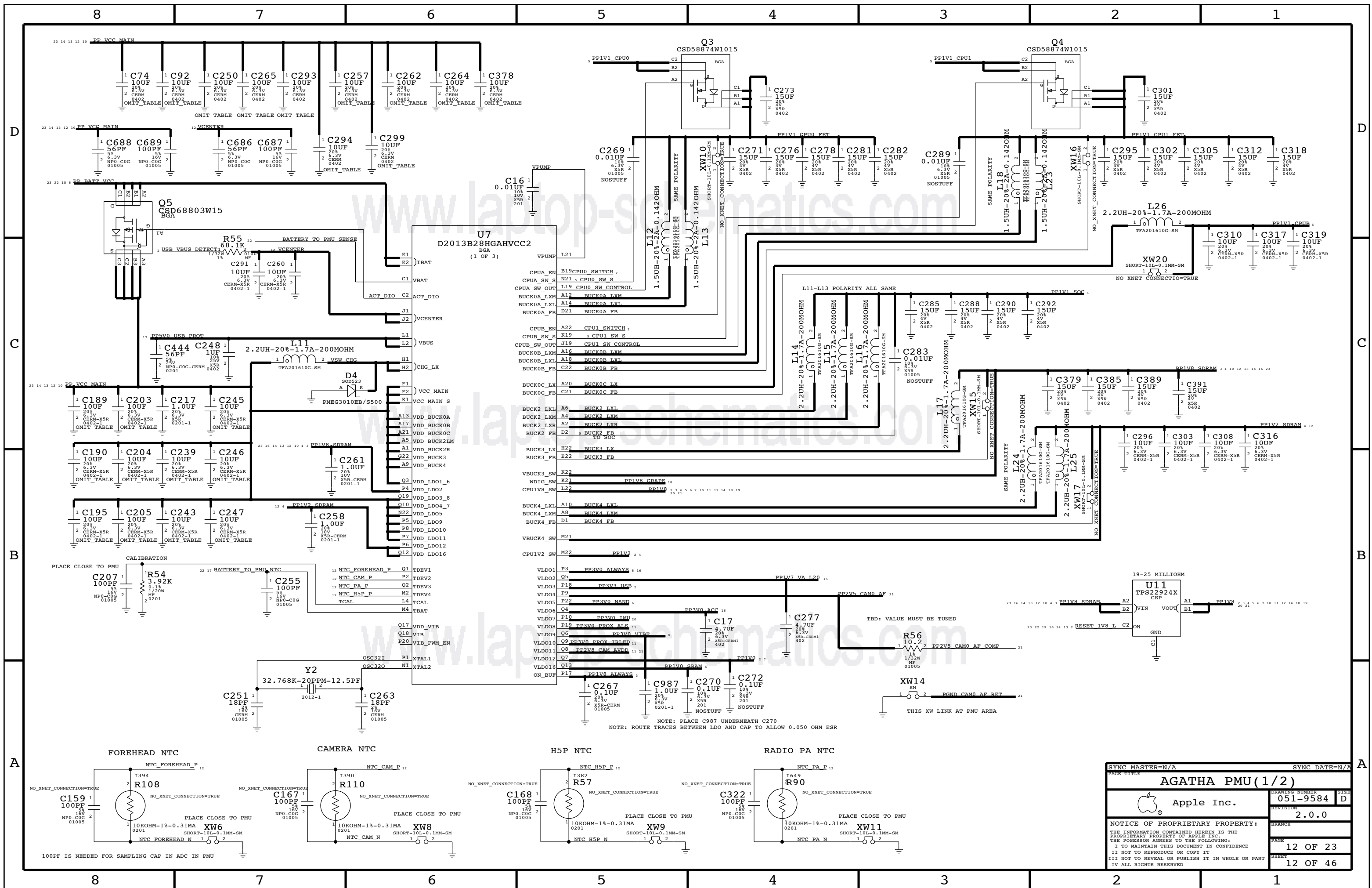
CAM1 ALS INT

PROX: PWR, TX EN

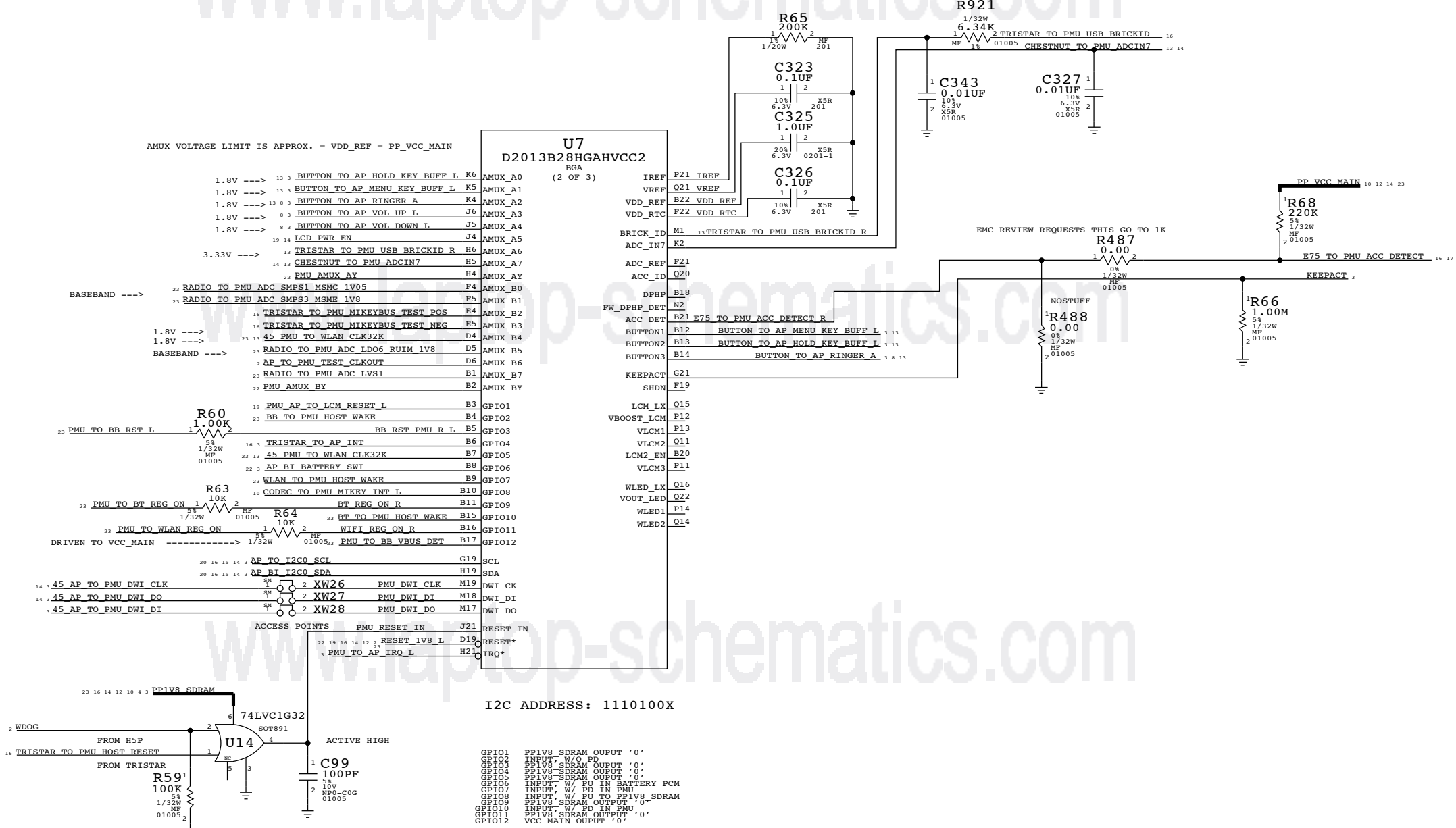
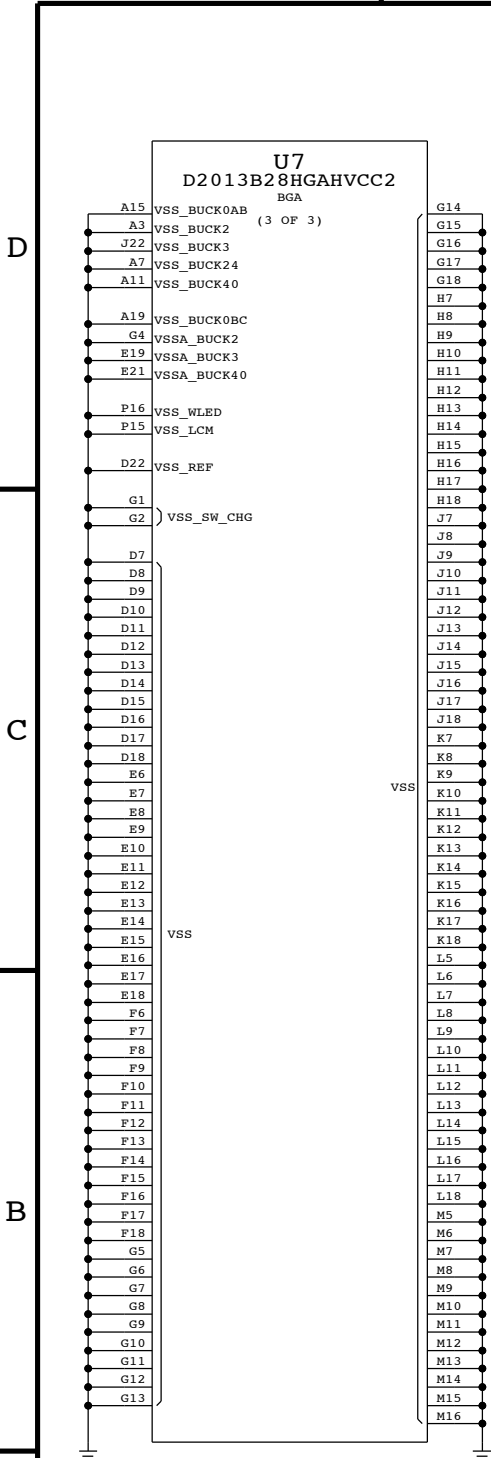
HAC

RECEIVER

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| PAGE TITLE | | SYNC DATE=N/A | |
| AGATHA PMU (1/2) | | | |
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AMUX VOLTAGE LIMIT IS APPROX. = VDD_REF = PP_VCC_MAIN

| | | | | | | | |
|------------|----|----------------------------------|-----|---------|----------------|---------|------------------------------|
| 1.8V ---> | 13 | BUTTON TO AP HOLD KEY BUFF L | K6 | AMUX_A0 | IREF | F21 | IREF |
| 1.8V ---> | 13 | BUTTON TO AP MENU KEY BUFF L | K5 | AMUX_A1 | VREF | Q21 | VREF |
| 1.8V ---> | 13 | BUTTON TO AP RINGER A | K4 | AMUX_A2 | VDD_REF | B22 | VDD_REF |
| 1.8V ---> | 8 | BUTTON TO AP VOL UP L | J6 | AMUX_A3 | VDD_RTC | F22 | VDD_RTC |
| 1.8V ---> | 8 | BUTTON TO AP VOL DOWN L | J5 | AMUX_A4 | BRICK_ID | M1 | TRISTAR TO PMU USB BRICKID R |
| 1.8V ---> | 8 | LCD_PWR_EN | J4 | AMUX_A5 | ADC_IN7 | K2 | ADC_REF |
| 3.33V ---> | 12 | TRISTAR TO PMU USB BRICKID R | H6 | AMUX_A6 | ADC_REF | F21 | ADC_REF |
| | 14 | CHESTNUT TO PMU ADCIN7 | H5 | AMUX_A7 | ACC_ID | Q20 | ACC_ID |
| | | PMU AMUX AY | H4 | AMUX_AY | DPHP | B18 | DPHP |
| | 23 | RADIO TO PMU ADC SMP31 MSMC 1V05 | F4 | AMUX_B0 | FW_DPHP_DET | N2 | FW_DPHP_DET |
| | 23 | RADIO TO PMU ADC SMP33 MSME 1V8 | F5 | AMUX_B1 | ACC_DET | B21 | E75 TO PMU ACC DETECT R |
| | 16 | TRISTAR TO PMU MIKEYBUS TEST POS | E4 | AMUX_B2 | BUTTON1 | B12 | BUTTON TO AP MENU KEY BUFF L |
| | 16 | TRISTAR TO PMU MIKEYBUS TEST NEG | E5 | AMUX_B3 | BUTTON2 | B13 | BUTTON TO AP HOLD KEY BUFF L |
| 1.8V ---> | 23 | 45 PMU TO WLAN CLK32K | D4 | AMUX_B4 | BUTTON3 | B14 | BUTTON TO AP RINGER A |
| 1.8V ---> | 23 | RADIO TO PMU ADC LD06 RUIM 1V8 | D5 | AMUX_B5 | KEEPACT | G21 | KEEPACT |
| | 2 | AP TO PMU TEST_CLKOUT | D6 | AMUX_B6 | SHDN | F19 | SHDN |
| | 2 | RADIO TO PMU ADC LVS1 | B1 | AMUX_B7 | LCM_LX | Q15 | LCM_LX |
| | 2 | PMU AMUX BY | B2 | AMUX_BY | VBOOST_LCM | P12 | VBOOST_LCM |
| | 19 | PMU AP TO LCM RESET L | B3 | GPI01 | VLCM1 | P13 | VLCM1 |
| | 23 | BB TO PMU HOST WAKE | B4 | GPI02 | VLCM2 | Q11 | VLCM2 |
| | | BB_RST PMU R L | B5 | GPI03 | LCM2_EN | B20 | LCM2_EN |
| | 16 | TRISTAR TO AP INT | B6 | GPI04 | VLCM3 | P11 | VLCM3 |
| | 23 | 45 PMU TO WLAN CLK32K | B7 | GPI05 | WLED_LX | Q16 | WLED_LX |
| | 23 | AP BI BATTERY_SHI | B8 | GPI06 | VOUT_LED | Q22 | VOUT_LED |
| | 23 | WLAN TO PMU HOST WAKE | B9 | GPI07 | WLED1 | P14 | WLED1 |
| | 10 | CODEC TO PMU MIKEY INT L | B10 | GPI08 | WLED2 | Q14 | WLED2 |
| | 5 | BT REG ON R | B11 | GPI09 | | | |
| | 23 | BT TO PMU HOST WAKE | B15 | GPI010 | | | |
| | 5 | WIFI REG ON R | B16 | GPI011 | | | |
| | 5 | PMU TO BB VBUS_DET | B17 | GPI012 | | | |
| | 20 | 15 | 14 | 3 | AP TO I2CO_SCL | G19 | SCL |
| | 20 | 15 | 14 | 3 | AP BI I2CO_SDA | H19 | SDA |
| 14 | 45 | AP TO PMU DWI_CLK | M19 | DWI_CLK | M19 | DWI_CLK | |
| 14 | 45 | AP TO PMU DWI_DO | M18 | DWI_DI | M18 | DWI_DI | |
| 14 | 45 | AP TO PMU DWI_DI | M17 | DWI_DO | M17 | DWI_DO | |

ACCESS POINTS

| | | |
|-----|----------|----------|
| J21 | RESET_IN | RESET_IN |
| D19 | RESET* | RESET* |
| H21 | IRQ* | IRQ* |

I2C ADDRESS: 1110100X

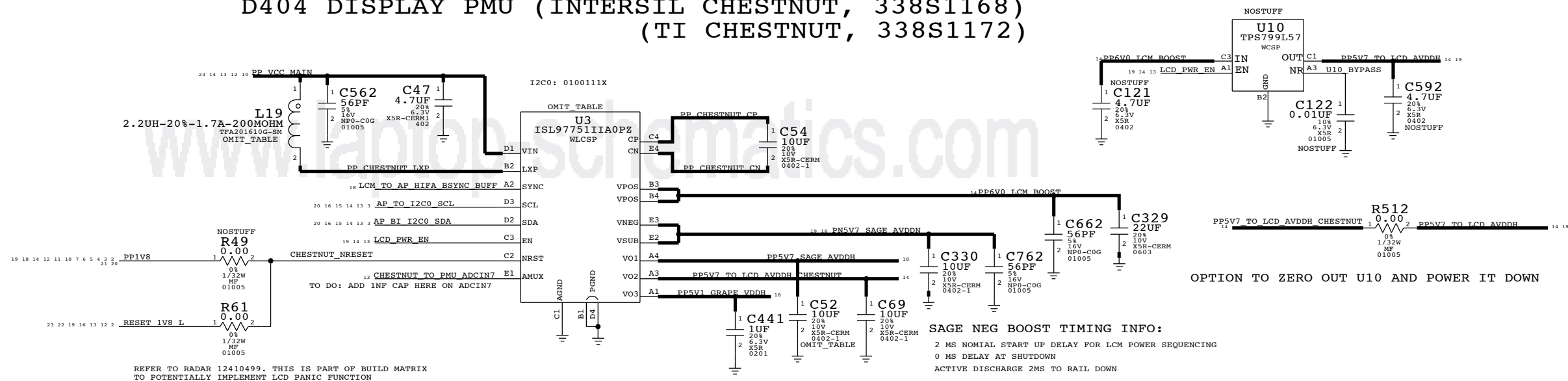
| | |
|-------|-----------------------------|
| GPI01 | PP1V8_SDRAM_OUTPUT '0' |
| GPI02 | INPUT* W/O PD |
| GPI03 | PP1V8_SDRAM_OUTPUT '0' |
| GPI04 | PP1V8_SDRAM_OUTPUT '0' |
| GPI05 | PP1V8_SDRAM_OUTPUT '0' |
| GPI06 | INPUT* W/ PU IN BATTERY PCM |
| GPI07 | INPUT* W/ PD IN PMU |
| GPI08 | INPUT* W/ PU TO PP1V8_SDRAM |
| GPI09 | PP1V8_SDRAM_OUTPUT '0' |
| GPI10 | INPUT* W/ PD IN PMU |
| GPI11 | PP1V8_SDRAM_OUTPUT '0' |
| GPI12 | VCC_MAIN_OUTPUT '0' |

RESET_IN ACTIVE HIGH INPUT W/ INTERNAL 200K PD
RESET* OPEN DRAIN OUTPUT
IRQ* OPEN DRAIN OUTPUT

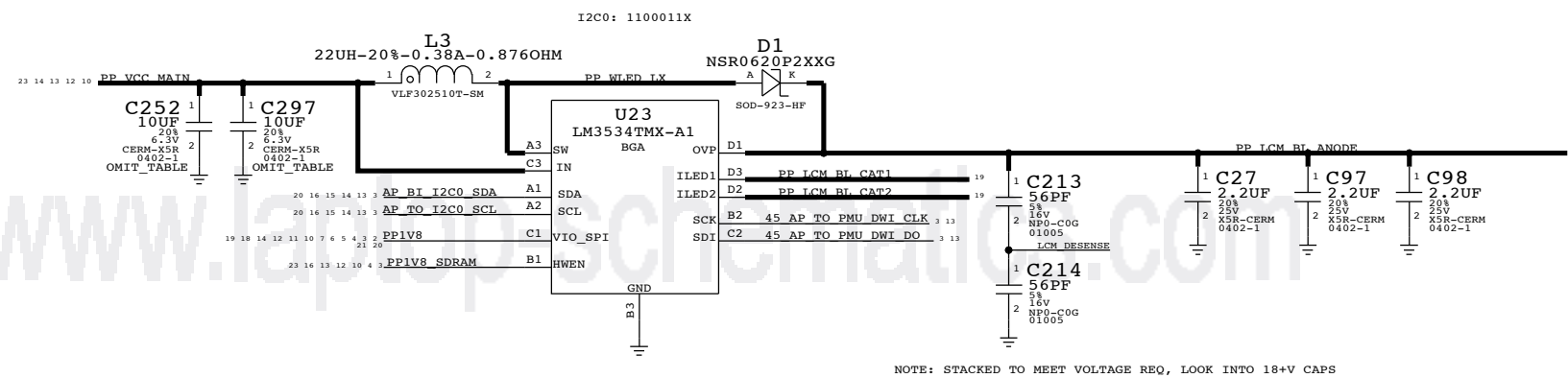
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CHESTNUT, BACKLIGHT DRIVER

D404 DISPLAY PMU (INTERSIL CHESTNUT, 338S1168) (TI CHESTNUT, 338S1172)



D404 BACKLIGHT DRIVER

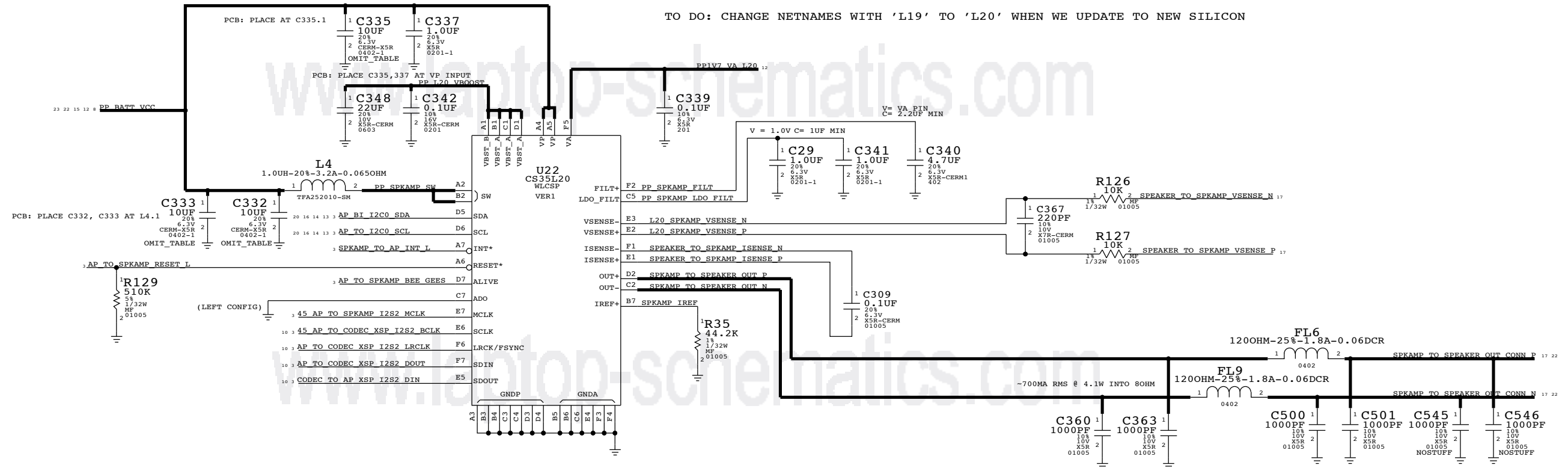


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| CHESTNUT + BACKLIGHT DRIVER | | | | | |
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SPEAKER AMP, LED DRIVER

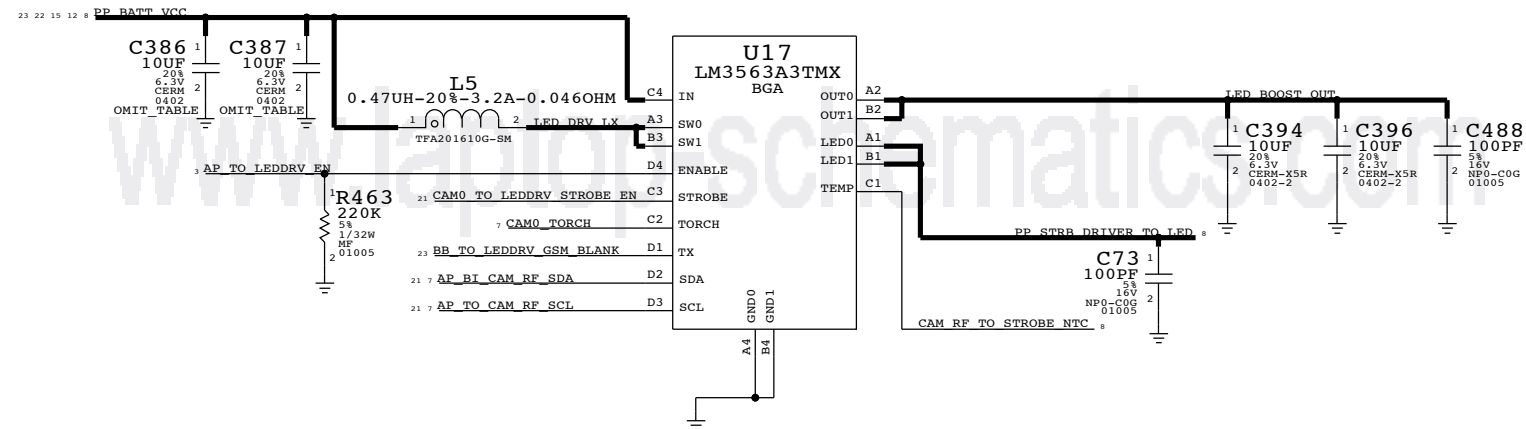
SPEAKER AMP (REPLACED WITH L20)

I2C ADDRESS: 1000000X



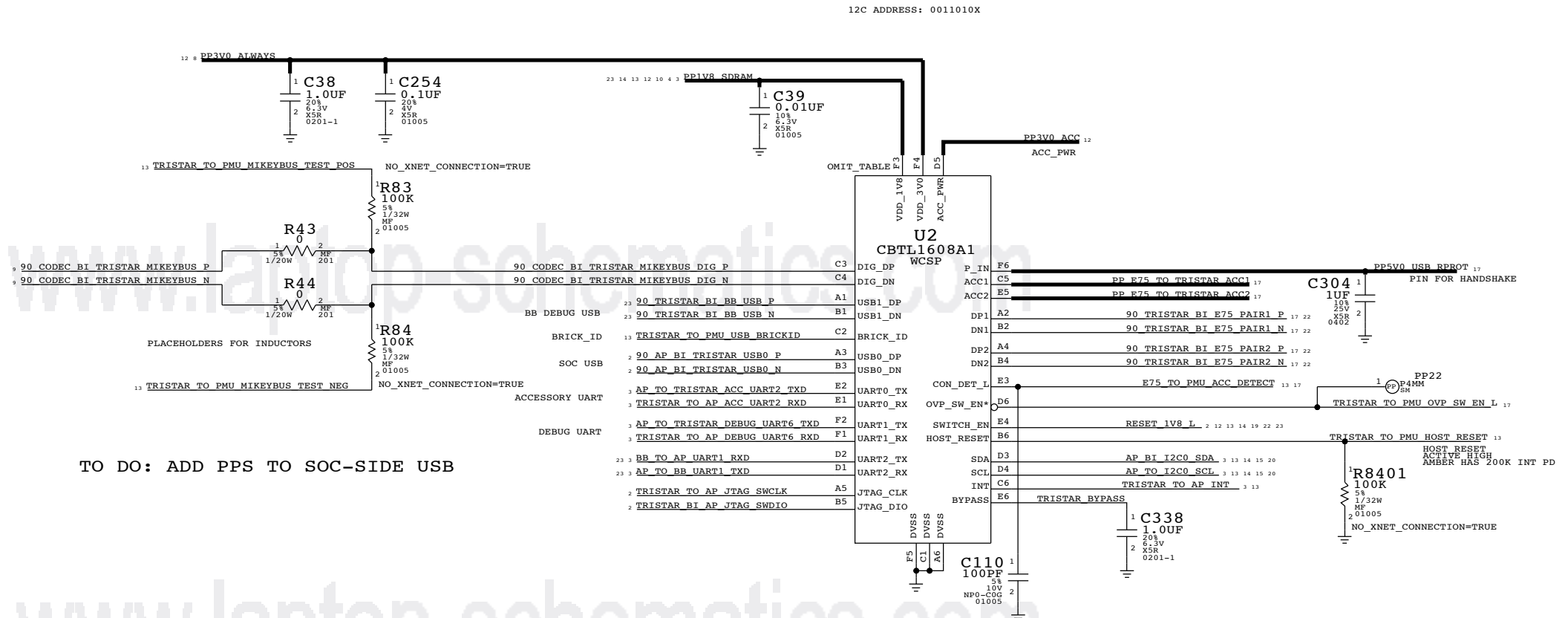
LED DRIVER

I2C ADDRESS: 1100011X



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| SYNC MASTER=N/A | | SYNC DATE=N/A | |
| PAGE TITLE SPKR AMP + LED DRIVER | | | |
| DRAWING NUMBER 051-9584 | | SIZE D | |
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TRISTAR

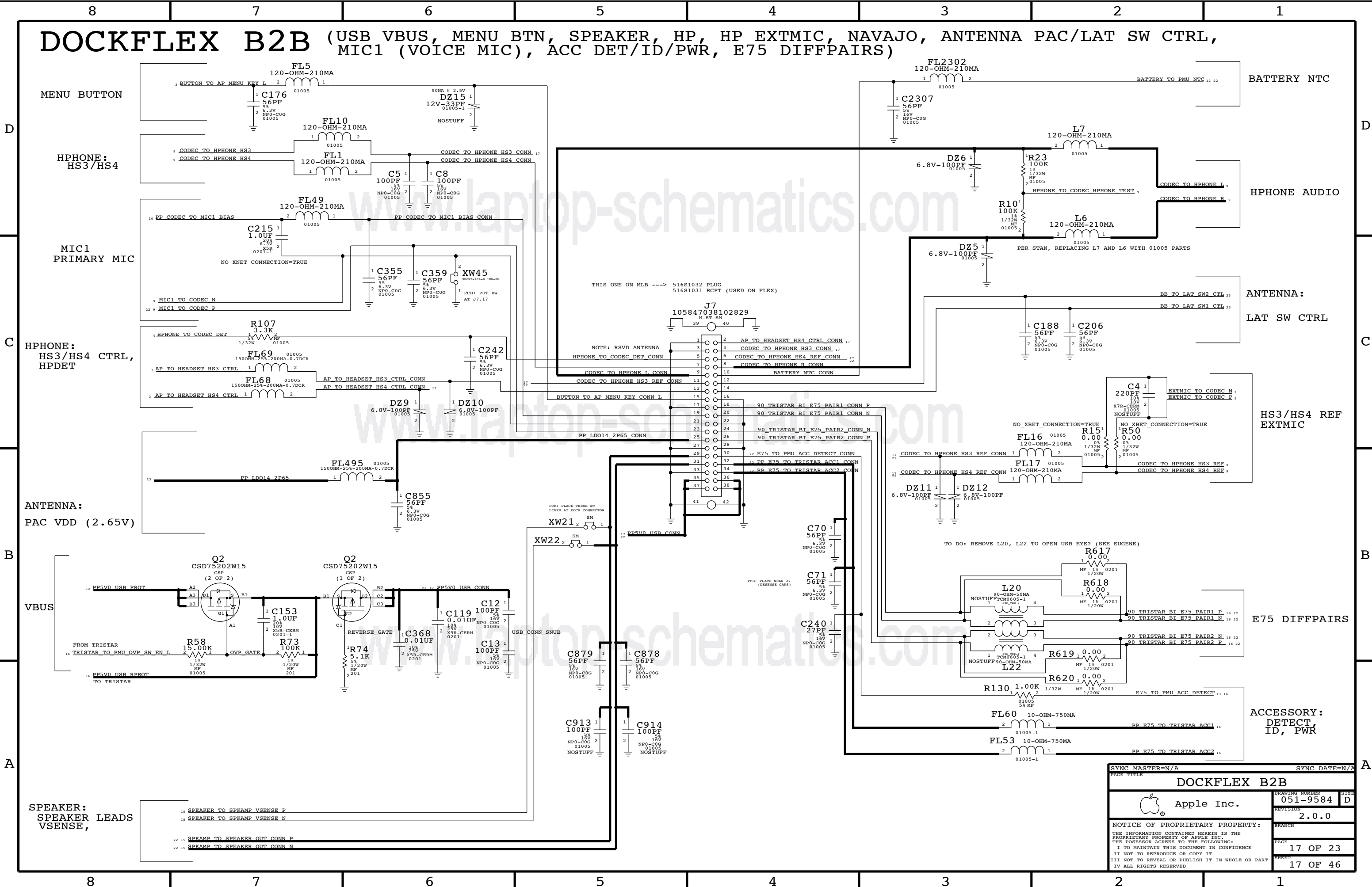


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| TRISTAR | | | |
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DOCKFLEX B2B (USB VBUS, MENU BTN, SPEAKER, HP, HP EXTMIC, NAVAJO, ANTENNA PAC/LAT SW CTRL, MIC1 (VOICE MIC), ACC DET/ID/PWR, E75 DIFFPAIRS)



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| DOCKFLEX B2B | | | |
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| | | SHEET | |
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D404 (B2B, DRIVER ICS)

SAGE2 C0

343S0628: B0 APN FOR PROTO1
343S0645: C0 APN FOR EVT1

CUMULUS C0

343S0574

(TURN ON LATER THAN PPIV8_GRAPE)
(TURN OFF SAME TIME AS PPIV8_GRAPE)

PP5V1 GRAPE VDDH

PP CUMULUS VDDCORE

PP CUMULUS VDDANA

PP CUMULUS VDDIO

PP CUMULUS VDDIO

PP CUMULUS VDDIO

PP CUMULUS VDDIO

PP CUMULUS VDDIO

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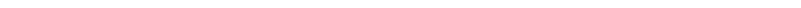
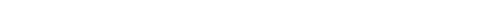
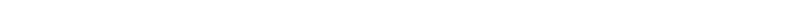
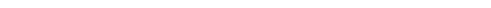
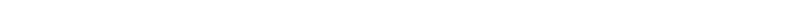
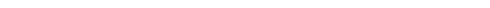
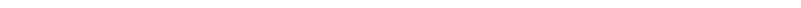
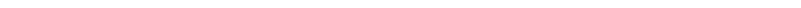
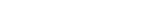
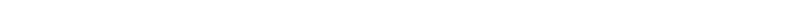
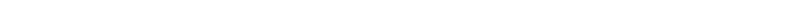
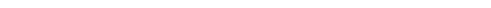
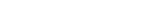
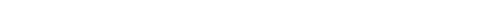
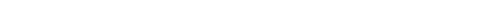
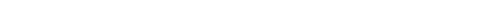
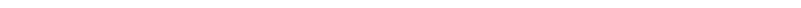
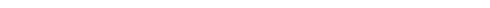
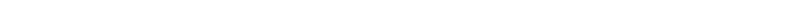
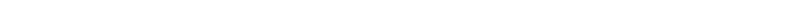
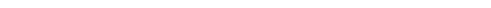
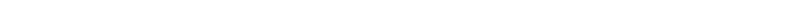
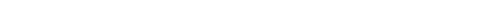
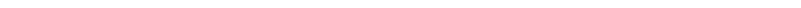
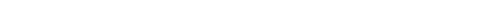
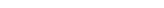
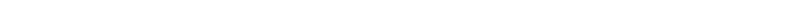
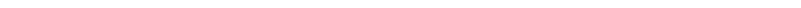
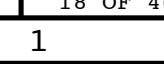
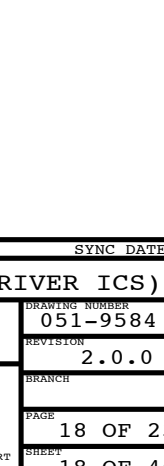
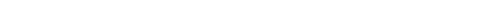
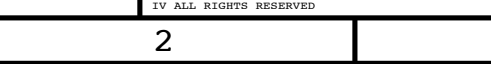
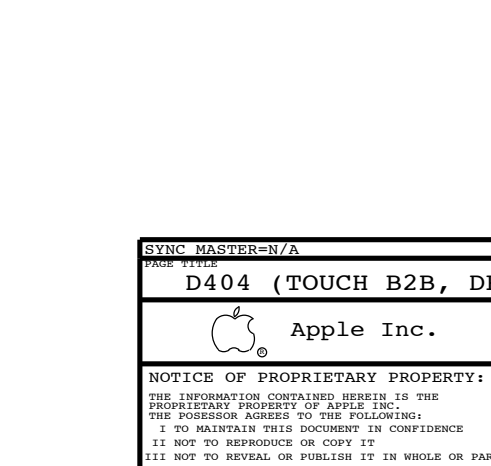
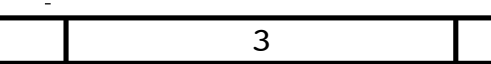
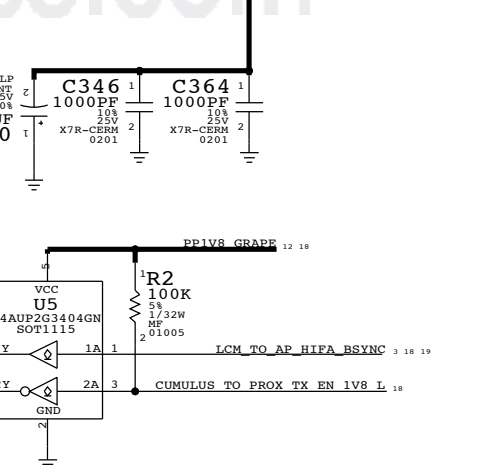
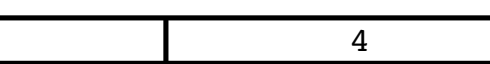
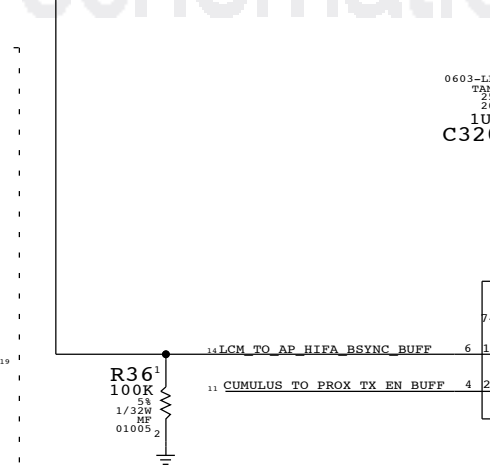
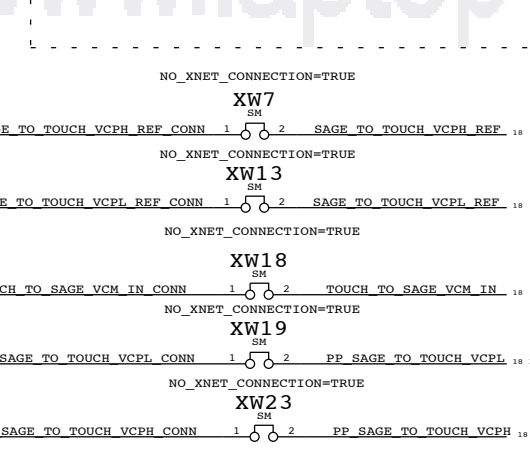
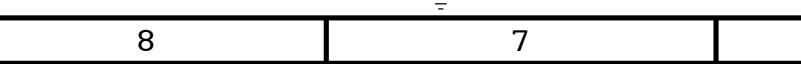
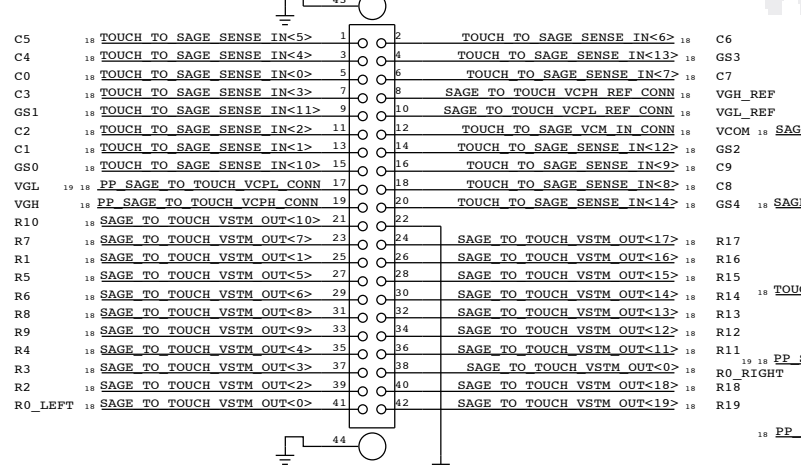
PP CUMULUS VDDIO

PP CUMULUS VDDIO

PP CUMULUS VDDIO

TOUCH B2B

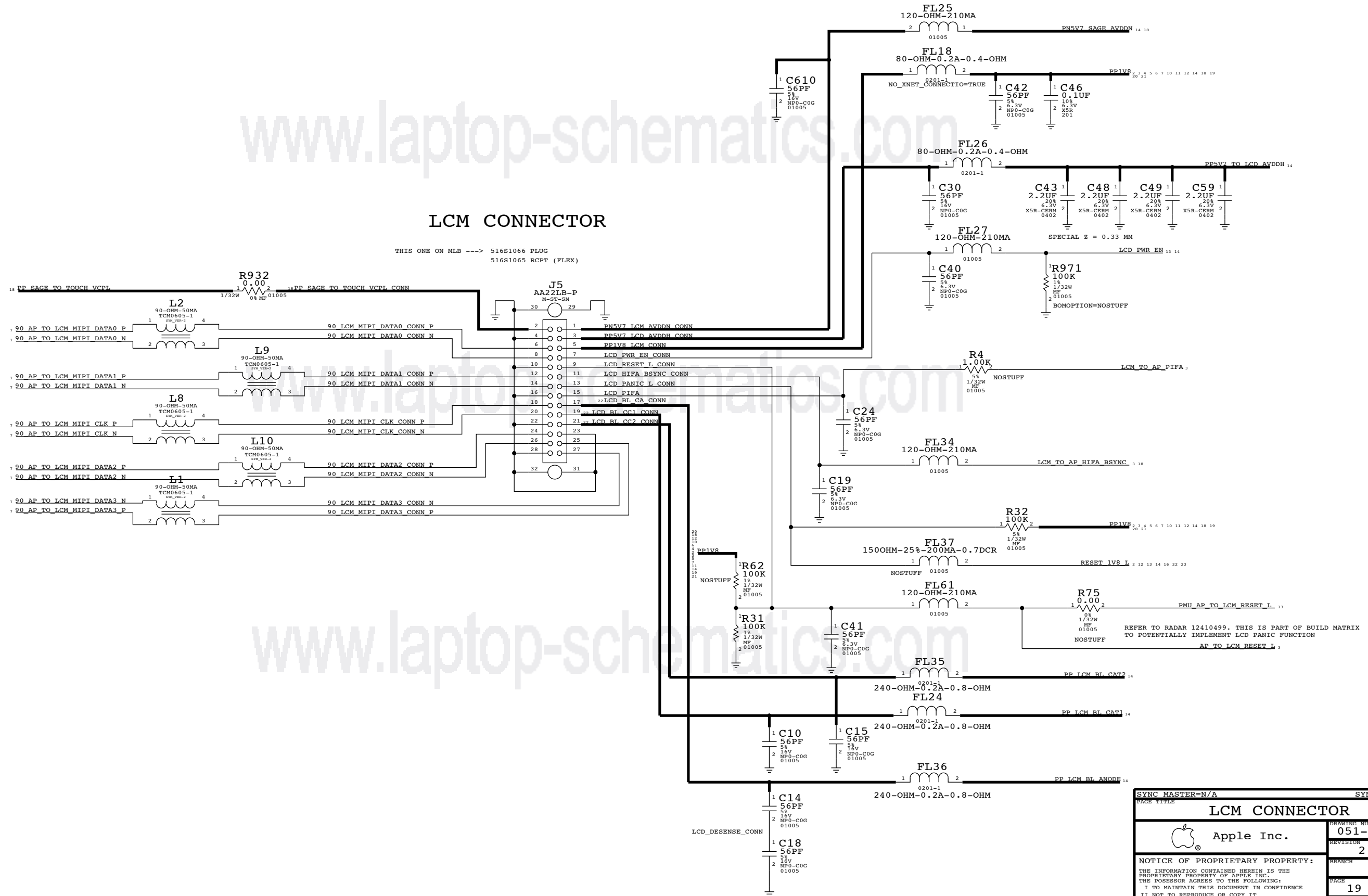
504459-4210



LCM B2B

LCM CONNECTOR

THIS ONE ON MLB ----> 516S1066 PLUG
516S1065 RCPT (FLEX)



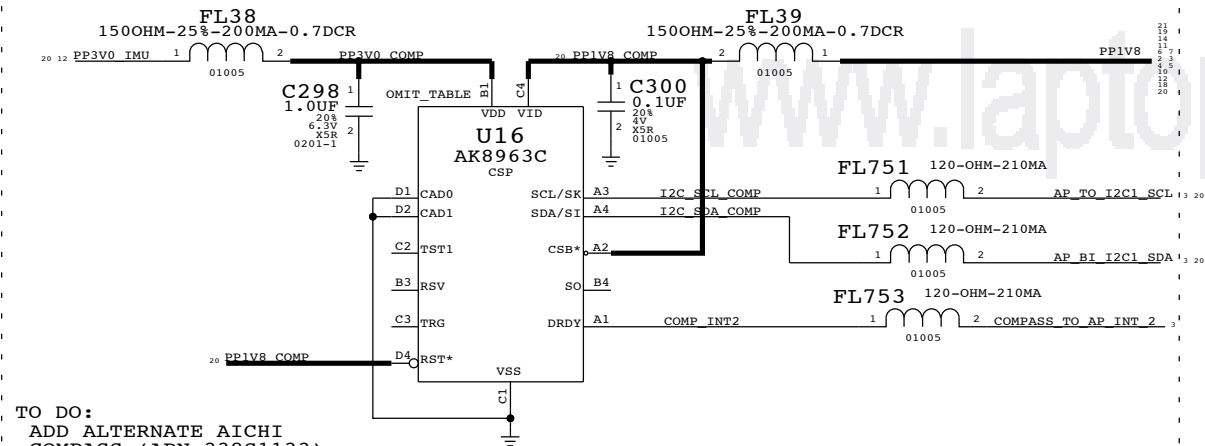
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| | DRAWING NUMBER | | SIZE |
| | 051-9584 | | D |
| REVISION | | BRANCH | |
| 2.0.0 | | | |
| PAGE | | SHEET | |
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SENSORS

THIS PART OUTSIDE OF SHIELD

COMPASS

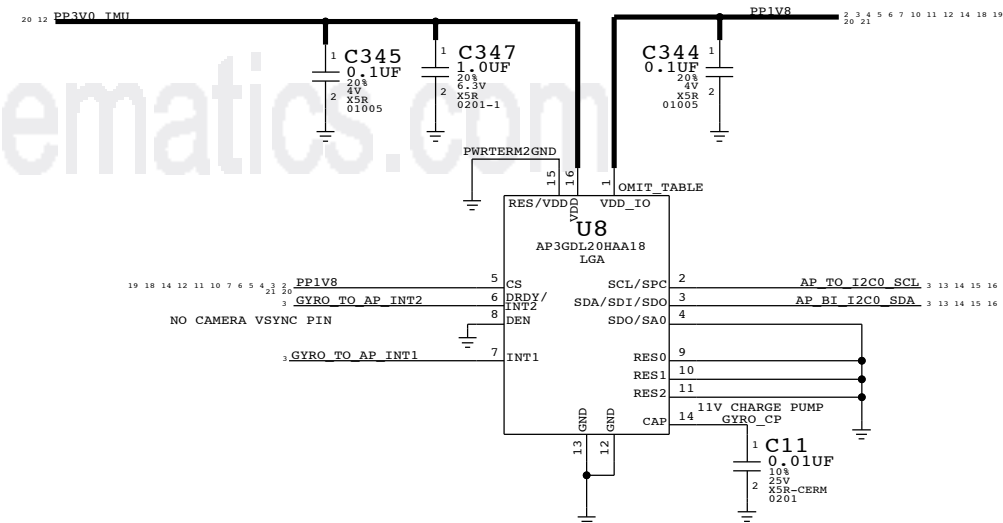
COMPASS DEVICE: 338S1014
COMPASS INTERPOSER: 998-5120



THESE PARTS INSIDE OF SHIELD

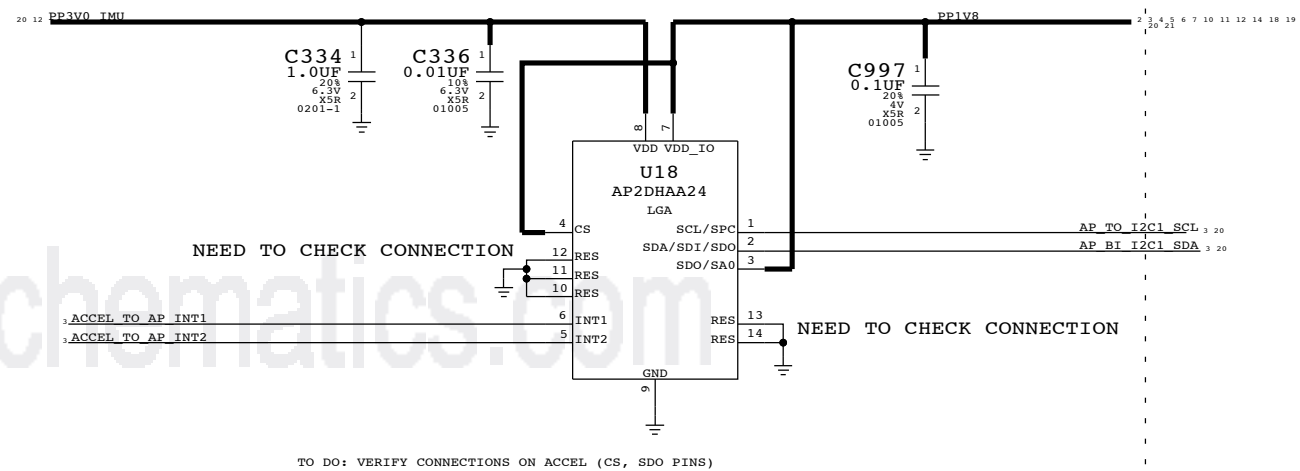
GYRO

AP3GDL20H, APN 338S1158



ACCELEROMETER

AP2DHAA, APN 338S1114



| | | | |
|---|--|----------------|----------|
| SYNC MASTER=N/A | | SYNC DATE=N/A | |
| OSCAR + SENSORS | | | |
| Apple Inc. | | DRAWING NUMBER | 051-9584 |
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| | | PAGE | 20 OF 23 |
| | | SHEET | 20 OF 46 |

CAM0: MAIN CAMERA CONNECTOR

8

7

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D

D

C

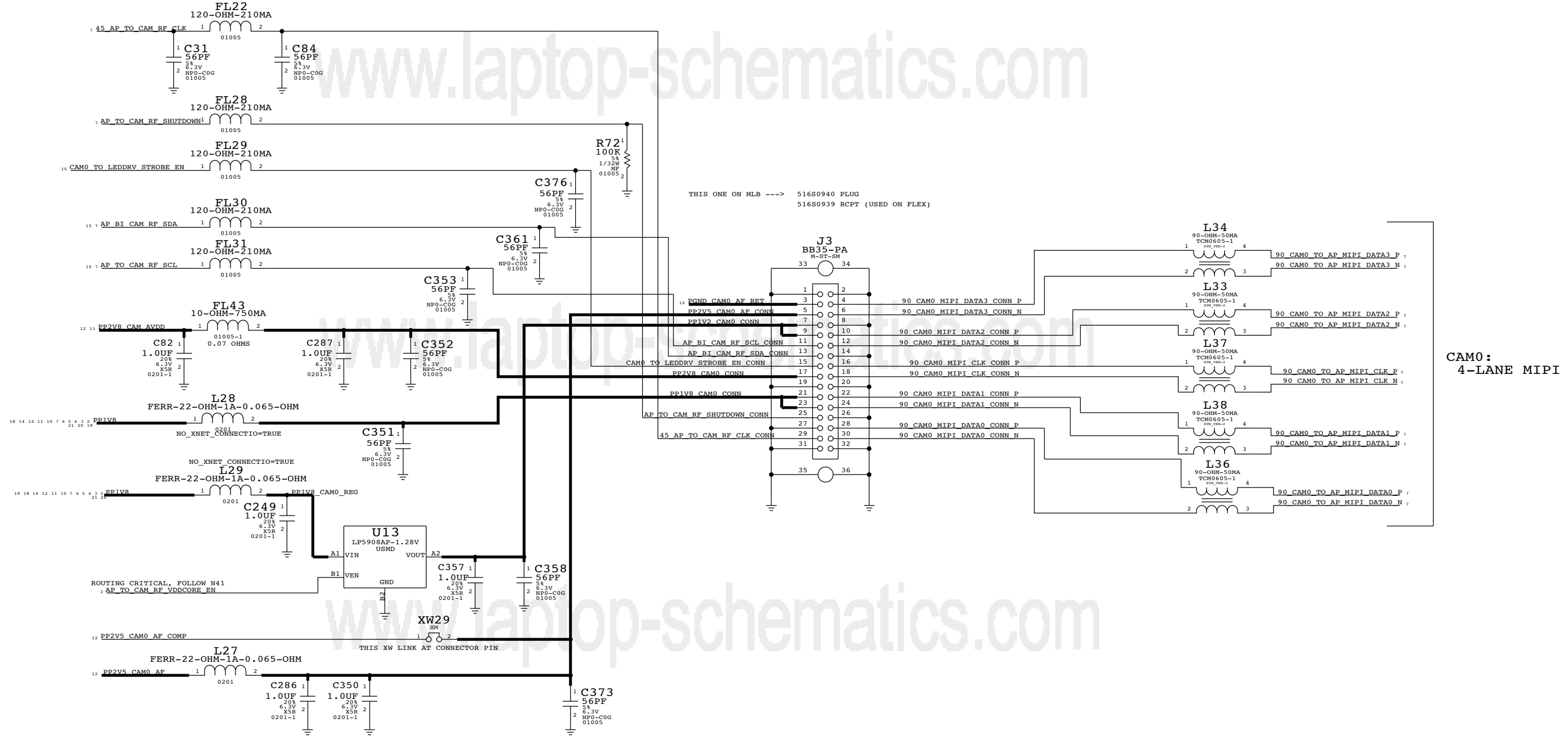
C

B

B

A

A



CAM0:
4-LANE MIPI

| | | | |
|---|----------------|---------------|-------------------|
| SYNC MASTER=N/A | | SYNC DATE=N/A | |
| PAGE TITLE CAM0 CONNECTOR | | | |
| Apple Inc. | DRAWING NUMBER | 051-9584 | SIZE D |
| | REVISION | 2.0.0 | BRANCH |
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| | | | SHEET 21 OF 46 |

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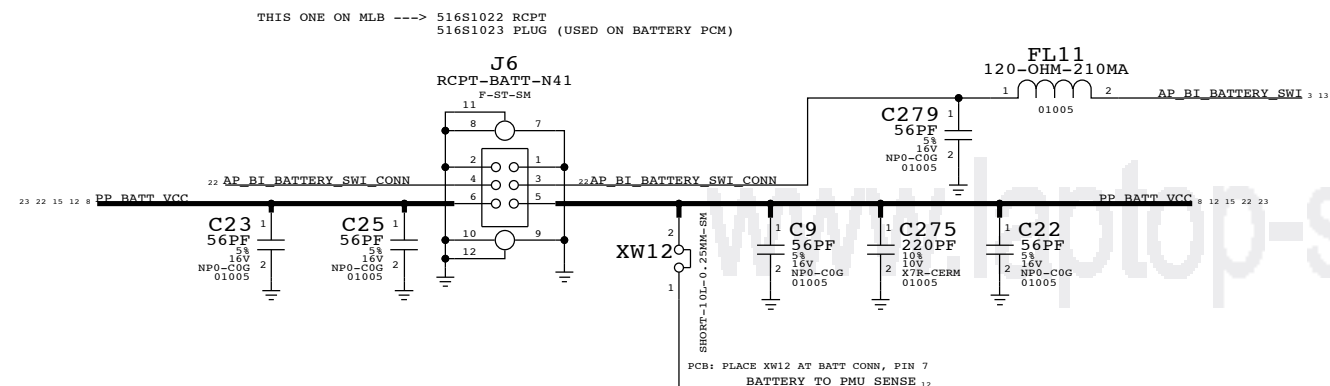
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2

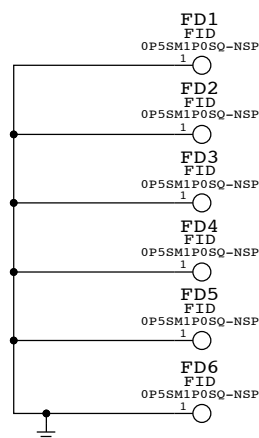
1

BATT CONN, TPS, STANDOFFS/SHIELDS/FIDUCIALS

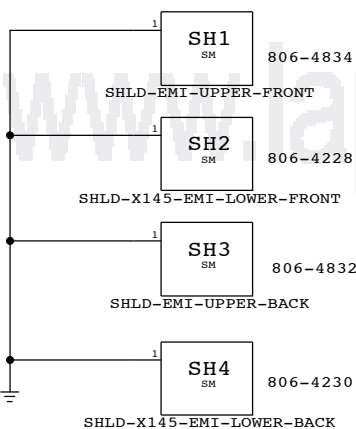
BATTERY CONN



FIDUCIALS

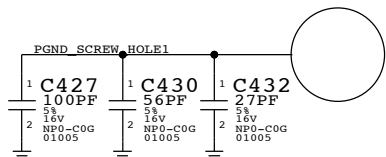


SHIELDS

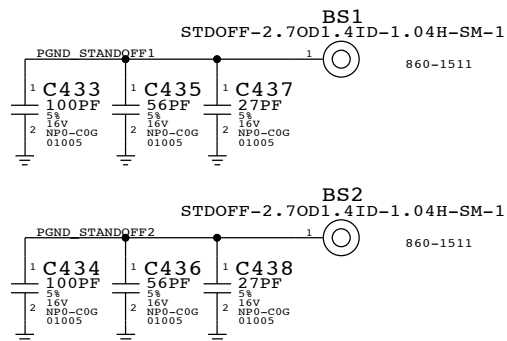


AC COUPLED SCREW HOLES + STANDOFFS (ON NORTH END OF SINGLE_BRD, TO MITIGATE COMPASS RETURN CURRENTS)

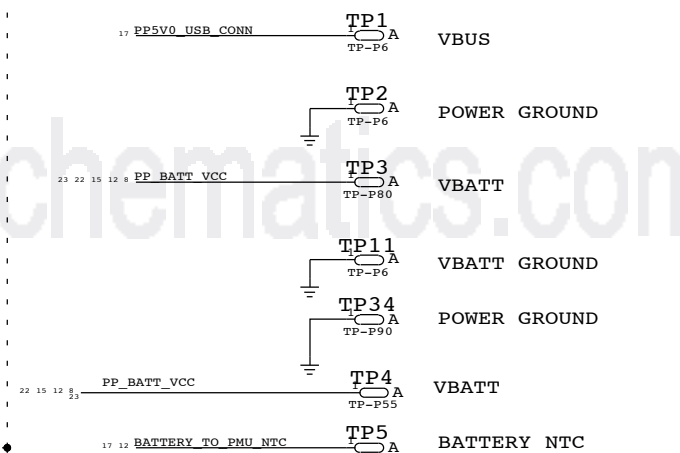
SCREW HOLES



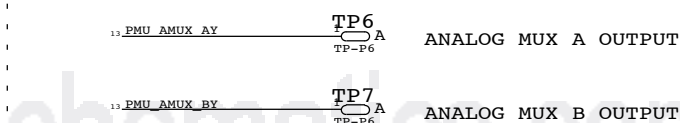
STANDOFFS



POWER TP



SUPER TP



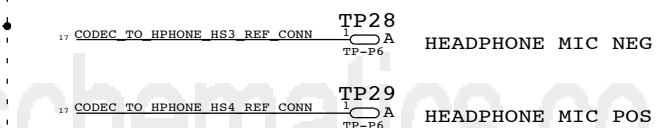
RESET



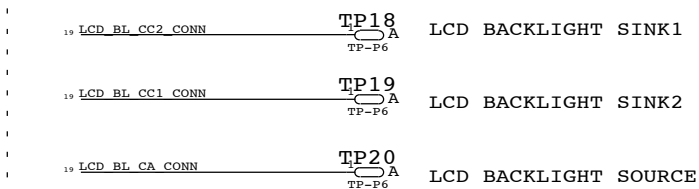
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HEADPHONE MIC

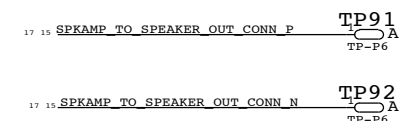


LCM BACKLIGHT

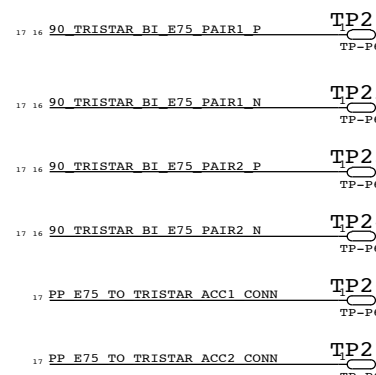


TESTPOINTS

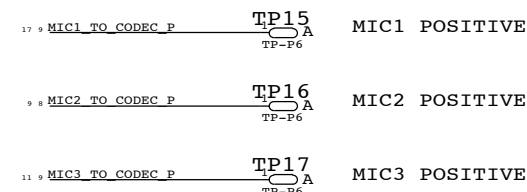
SPKAMP OUTPUT TP



E75 - USB/UART/ID/POWER



MIC AUDIO



DRIVE MIC WRT NEAREST GROUND TEST POINT

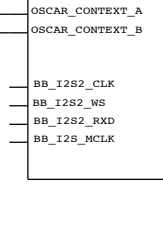
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|---|--|----------------------------|-------------------|
| SYNC MASTER=N/A | | SYNC DATE=N/A | |
| BATT B2B, TPS, PD FEATURES | | | |
| Apple Inc. | | DRAWING NUMBER 051-9584 | SIZE D |
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| | | BRANCH | SHEET 22 OF 46 |

RADIO_MLB HIERARCHICAL SYMBOL

AP/RADIO INTERFACE

RF
I612

| | | | | | |
|-----------------------|-----|----------------------------------|----------------|-------------------------|---|
| 25 22 15 12 8 | IN | PP_BATT_VCC | MAKE BASE=TRUE | PP_BATT_VCC_CONN | |
| 46 14 13 10 | IN | PP_VCC_MAIN | MAKE BASE=TRUE | PP_VCC_MAIN_WLAN | |
| 46 16 14 13 12 10 4 3 | IN | PPIV8_SDRAM | MAKE BASE=TRUE | PP_WL_BT_VDDIO_AP | |
| 26 17 | OUT | PP_LDO14_2P65 | MAKE BASE=TRUE | PP_LDO14_2V65 | |
| 25 3 | IN | AP TO RADIO ON L | MAKE BASE=TRUE | RADIO_ON_L | BB_JTAG_TCK MAKE BASE=TRUE AP TO BB_JTAG_TCK 25 |
| 25 3 | IN | BB TO AP RESET DET L | MAKE BASE=TRUE | RESET_DET_L | BB_JTAG_TDI MAKE BASE=TRUE AP TO BB_JTAG_TDI 25 |
| 25 13 | IN | PMU TO BB_RST_L | MAKE BASE=TRUE | RESET_PMU_L | BB_JTAG_TMS MAKE BASE=TRUE AP TO BB_JTAG_TMS 25 |
| 25 3 | IN | AP TO BB_RST_L | MAKE BASE=TRUE | BB_RST_L | BB_JTAG_TRST_L MAKE BASE=TRUE AP TO BB_JTAG_TRST_L 25 |
| 25 22 19 16 14 13 12 | OUT | RESET_1V8_L | MAKE BASE=TRUE | RF_RESET_L | BB_JTAG_TDO MAKE BASE=TRUE BB TO AP_JTAG_TDO 25 |
| 25 13 | IN | 45 PMU TO WLAN_CLK32K | MAKE BASE=TRUE | CLK32K_AP | |
| 29 15 | OUT | BB TO LEDDRV_GSM_BLANK | MAKE BASE=TRUE | TX_GTR_THRESH | |
| 25 16 | IN | 90 TRISTAR_BI_BB_USB_N | MAKE BASE=TRUE | 90_BB_USB_D_N | |
| 25 16 | IN | 90 TRISTAR_BI_BB_USB_P | MAKE BASE=TRUE | 90_BB_USB_D_P | |
| 25 13 | IN | PMU TO BB_VBUS_DET | MAKE BASE=TRUE | BB_USB_VBUS | |
| 25 3 | IN | AP TO BB_UART1_RTS_L | MAKE BASE=TRUE | BB_UART_CTS_L | |
| 25 3 | OUT | BB TO AP_UART1_CTS_L | MAKE BASE=TRUE | BB_UART_RTS_L | |
| 25 16 3 | IN | AP TO BB_UART1_TXD | MAKE BASE=TRUE | BB_UART_RXD | |
| 25 16 3 | IN | BB TO AP_UART1_RXD | MAKE BASE=TRUE | BB_UART_TXD | |
| 25 13 | OUT | BB TO PMU_HOST_WAKE | MAKE BASE=TRUE | HOST_WAKE_BB | |
| 29 3 | OUT | BB TO AP_PP_SYNC | MAKE BASE=TRUE | PP_SYNC | |
| 25 3 | IN | 45 AP TO BB_I2S1_BCLK | MAKE BASE=TRUE | BB_I2S_CLKRADIO_MLB | |
| 25 3 | IN | AP TO BB_I2S1_DOUT | MAKE BASE=TRUE | BB_I2S_RXD | |
| 25 3 | OUT | BB TO AP_I2S1_DIN | MAKE BASE=TRUE | BB_I2S_TXD | |
| 25 3 | IN | AP TO BB_I2S1_LRCLK | MAKE BASE=TRUE | BB_I2S_WS | |
| 25 13 | OUT | RADIO TO PMU_ADC_SMP31_MSMC_1V05 | MAKE BASE=TRUE | ADC_SMP31_MSMC_1V05 | |
| 25 13 | OUT | RADIO TO PMU_ADC_SMP33_MSME_1V8 | MAKE BASE=TRUE | ADC_SMP33_MSME_1V8 | |
| 25 13 | OUT | RADIO TO PMU_ADC_LDO6_RUIM_1V8 | MAKE BASE=TRUE | ADC_LDO6_RUIM_1V8 | |
| 25 13 | OUT | RADIO TO PMU_ADC_LVS1 | MAKE BASE=TRUE | ADC_LVS1 | |
| 25 13 | IN | PMU TO WLAN_REG_ON | MAKE BASE=TRUE | WLAN_REG_ON | |
| 46 3 | IN | AP TO WLAN_UART4_TXD | MAKE BASE=TRUE | WLAN_UART_RXD | |
| 46 3 | OUT | WLAN TO AP_UART4_RXD | MAKE BASE=TRUE | WLAN_UART_TXD | |
| 46 13 | OUT | WLAN TO PMU_HOST_WAKE | MAKE BASE=TRUE | HOST_WAKE_WLAN | |
| 25 13 | IN | PMU TO BT_REG_ON | MAKE BASE=TRUE | BT_REG_ON | |
| 46 3 | IN | AP TO BT_UART3_RTS_L | MAKE BASE=TRUE | BT_UART_CTS_L | |
| 46 3 | OUT | BT TO AP_UART3_CTS_L | MAKE BASE=TRUE | BT_UART_RTS_L | |
| 25 3 | IN | AP TO BT_UART3_TXD | MAKE BASE=TRUE | BT_UART_RXD | |
| 25 3 | OUT | BT TO AP_UART3_RXD | MAKE BASE=TRUE | BT_UART_TXD | |
| 25 3 | IN | AP TO BT_WAKE | MAKE BASE=TRUE | BT_WAKE | |
| 46 13 | OUT | BT TO PMU_HOST_WAKE | MAKE BASE=TRUE | HOST_WAKE_BT | |
| 46 3 | IN | 45 AP TO BT_I2S3_BCLK | MAKE BASE=TRUE | BT_PCM_CLK | |
| 46 3 | IN | AP TO BT_I2S3_DOUT | MAKE BASE=TRUE | BT_PCM_IN | |
| 46 3 | OUT | BT TO AP_I2S3_DIN | MAKE BASE=TRUE | BT_PCM_OUT | |
| 46 3 | IN | AP TO BT_I2S3_LRCLK | MAKE BASE=TRUE | BT_PCM_SYNC | |
| 25 2 | IN | 50 AP_BI_BB_HSIC1_DATA | MAKE BASE=TRUE | 50_HSIC_BB_DATA | |
| 25 3 | IN | 50 AP_BI_BB_HSIC1_STB | MAKE BASE=TRUE | 50_HSIC_BB_STROBE | |
| 25 3 | IN | AP TO BB_HSIC1_RDY | MAKE BASE=TRUE | AP_HSIC1_RDY | |
| 25 3 | IN | BB TO AP_HSIC1_RDY | MAKE BASE=TRUE | PBL_RUN_BB_HSIC1_RDY | |
| 25 3 | IN | BB TO AP_HSIC1_REMOTE_WAKE | MAKE BASE=TRUE | BB_HSIC1_REMOTE_WAKE | |
| 25 3 | IN | AP TO BB_WAKE_MODEM | MAKE BASE=TRUE | AP_WAKE_MODEM | |
| 25 2 | IN | 50 AP_BI_WLAN_HSIC3_DATA | MAKE BASE=TRUE | 50_HSIC_WLAN_DATA | |
| 25 2 | IN | 50 AP_BI_WLAN_HSIC3_STB | MAKE BASE=TRUE | 50_HSIC_WLAN_STROBE | |
| 25 3 | IN | AP TO WLAN_HSIC2_RDY | MAKE BASE=TRUE | AP_HSIC3_RDY | |
| 25 3 | IN | WLAN TO AP_HSIC2_RDY | MAKE BASE=TRUE | WLAN_HSIC3_DEVICE_RDY | |
| 25 3 | IN | WLAN TO AP_HSIC2_REMOTE_WAKE | MAKE BASE=TRUE | WLAN_HSIC3_RESUME | |
| 25 17 | OUT | BB TO LAT_SW1_CTL | MAKE BASE=TRUE | LAT_SW1_CTL | |
| 29 17 | OUT | BB TO LAT_SW2_CTL | MAKE BASE=TRUE | LAT_SW2_CTL | |
| | | <OUT> BB TO LAT_SW3_CTL | | | |
| 29 8 | OUT | BB TO ANTENNA_PAC_SPT_CS_L | MAKE BASE=TRUE | BB_SPT_TO_PAC_CS | |
| 29 8 | OUT | BB TO ANTENNA_PAC_SPT_SCLK | MAKE BASE=TRUE | BB_SPT_TO_PAC_CLK | |
| 29 8 | OUT | BB TO ANTENNA_PAC_SPT_MOSI | MAKE BASE=TRUE | BB_SPT_TO_PAC_DATA_MOSI | |
| 29 8 | IN | ANTENNA_PAC TO BB_SPT_MISO | MAKE BASE=TRUE | PAC_TO_BB_SPT_DATA_MISO | |
| 29 3 | IN | BB TO AP_IPC_GPIO | MAKE BASE=TRUE | BB_IPC_GPIO | |



| | | | |
|---|--|----------------|----------|
| SYNC MASTER=N/A | | SYNC DATE=N/A | |
| RADIO_MLB HIERARCH. SYMBOL | | | |
| Apple Inc. | | DRAWING NUMBER | 051-9584 |
| | | REVISION | 2.0.0 |
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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

| REV | ECN | DESCRIPTION OF REVISION | CK APPD | DATE |
|-----|------------|-------------------------|---------|------------|
| 2 | 0001669557 | ENGINEERING RELEASED | | 2012-10-14 |

X155 RADIO_MLB SUBDESIGN - PROTO1

10/3/2012


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| 3 | CELLULAR PMU: (1 OF 2) |
| 4 | CELLULAR PMU: (2 OF 2) |
| 5 | CELLULAR BASEBAND: (1 OF 2) |
| 6 | CELLULAR BASEBAND: (2 OF 2) |
| 7 | CELLULAR RF TRANSCEIVER: (1 OF 2) |
| 8 | CELLULAR RF TRANSCEIVER: (2 OF 2) |
| 9 | CELLULAR FRONT END: TX AND RX MATCHING |
| 10 | CELLULAR FRONT END: SAW BANKS |
| 11 | CELLULAR FRONT END: BAND 1/4 PAT |
| 12 | CELLULAR FRONT END: BAND 2/3 PAD |
| 13 | CELLULAR FRONT END: BAND 20 PAD |
| 14 | CELLULAR FRONT END: BAND 5/8 PAD |
| 15 | CELLULAR FRONT END: BAND 13/17 PAD |
| 16 | CELLULAR FRONT END: PA DCDC CONVERTER |
| 17 | CELLULAR FRONT END: 2G FEM |
| 18 | CELLULAR FRONT END: RX DIVERSITY |
| 19 | CELLULAR FRONT END: GPS LNA |
| 20 | CELLULAR FRONT END: ANTENNA FEEDS |
| 21 | FRONT END LOGIC TABLE (1 OF 2) |
| 22 | FRONT END LOGIC TABLE (2 OF 2) |
| 23 | WIFI/BT: MODULE AND FRONT END |

BOARD ID BOM OPTIONS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|----------------|-------------------------|----------|------------|
| 118S0621 | 1 | 1.00M 1% 01005 | R25_RF | Y | N51_CFG_A |
| 118S0732 | 1 | 50K 1% 01005 | R26_RF | Y | N51_CFG_A |
| 117S0159 | 1 | 470K 5% 01005 | R25_RF | Y | N51_CFG_B |
| 118S0626 | 1 | 100K 1% 01005 | R26_RF | Y | N51_CFG_B |
| 118S0626 | 1 | 100K 1% 01005 | R25_RF | Y | N53_CFG_A |
| 118S0726 | 1 | 162K 1% 01005 | R26_RF | Y | N53_CFG_A |
| 118S0626 | 1 | 100K 1% 01005 | R25_RF | Y | N53_CFG_B |
| 118S0623 | 1 | 267K 1% 01005 | R26_RF | Y | N53_CFG_B |
| 118S0659 | 1 | 255K 1% 01005 | R25_RF | Y | N48_CFG_A |
| 118S0626 | 1 | 100K 1% 01005 | R26_RF | Y | N48_CFG_A |
| 118S0689 | 1 | 147K 1% 01005 | R25_RF | Y | N48_CFG_B |
| 118S0626 | 1 | 100K 1% 01005 | R26_RF | Y | N48_CFG_B |
| 118S0626 | 1 | 100K 1% 01005 | R25_RF | Y | N49_CFG_A |
| 118S0650 | 1 | 499K 1% 01005 | R26_RF | Y | N49_CFG_A |
| 118S0732 | 1 | 50K 1% 01005 | R25_RF | Y | N49_CFG_B |
| 118S0621 | 1 | 1.00M 1% 01005 | R26_RF | Y | N49_CFG_B |

SCH : 951-2446
 BOM : 939-0308
 BOARD : 920-2148

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|------------------|-------------------------|----------|------------|
| 951-2446 | 1 | X145_RADIO_MLB | SCH | Y | |
| 825-2029 | 1 | EEE FOR 939-0308 | EEEE_???? | Y | NA |

| | | | |
|--|----------------|--------------------------|----------|
| DRAWING TITLE | | X155 RADIO_MLB SCHEMATIC | |
|  Apple Inc. | DRAWING NUMBER | 051-9584 | SIZE |
| | REVISION | 2.0.0 | D |
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AP INTERFACE & DEBUG CONNECTORS

AP CONNECTIONS

IN = FROM AP
OUT = TO AP

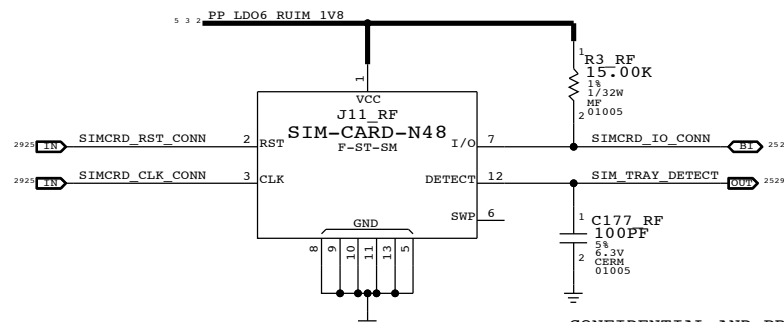
- 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
- 17 PP BATT VCC CONN
- 16 PP VCC MAIN WLAN
- 15 TX GTR THRESH
- 14 BB_RST_L
- 13 RESET_DET_L
- 12 RADIO_ON_L
- 11 RESET_PMU_L
- 10 HOST_WAKE_BB
- 9 RF_RESET_L
- 8 PBL_RUN_BB_HSI_C1_RDY
- 7 WLAN_HSI_C3_RESUME
- 6 AP_WAKE_MODEM
- 5 AP_HSI_C1_RDY
- 4 50_HSI_C1_BB_DATA
- 3 50_HSI_C1_BB_STROBE
- 2 BB_HSI_C1_REMOTE_WAKE
- 1 BB_UART_TXD
- BB_UART_RXD
- BB_UART_RTS_L
- BB_UART_CTS_L
- 90_BB_USB_D_P
- 90_BB_USB_D_N
- BB_I2S_CLK
- BB_I2S_WS
- BB_I2S_TXD
- BB_I2S_RXD
- PP_SYNC
- PP_WL_BT_VDDIO_AP
- CLK32K_AP
- WLAN_REG_ON
- WLAN_UART_TXD
- WLAN_UART_RXD
- WLAN_UART_RTS_L
- WLAN_UART_CTS_L
- BT_REG_ON
- BT_PCM_CLK
- BT_PCM_SYNC
- BT_PCM_OUT
- BT_PCM_IN
- LAT_SW1_CTL
- LAT_SW2_CTL
- BB_SPT_TO_PAC_CS
- BB_SPT_TO_PAC_DATA_MOST
- BB_SPT_TO_PAC_CLK
- PAC_TO_BB_SPT_DATA_MISO
- PP_LDO14_2V65
- BB_JTAG_TCK
- BB_JTAG_TDI
- BB_JTAG_TMS
- BB_JTAG_TRST_L
- BB_JTAG_TDO
- ADC_SMPS1_MSMC_1V05
- ADC_SMPS3_MSME_1V8
- ADC_LDO6_RUIM_1V8
- ADC_LVS1
- BB_IPC_GPIO
- OSCAR_CONTEXT_A
- OSCAR_CONTEXT_B
- BB_I2S2_CLK
- BB_I2S2_WS
- BB_I2S2_MCLK
- BB_I2S2_RXD

PROBE POINTS

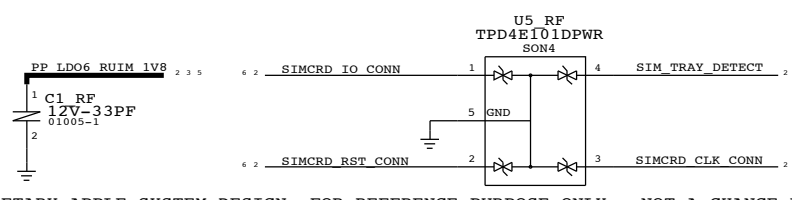
- PP1 RF P4MM 1 BB_ERROR_FLAG
- PP2 RF P4MM 1 SLEEP_CLK_32K
- PP3 RF P4MM 1 PMIC_SSB1
- PP10 RF P4MM-NSM 1 19F2M_MDM
- PP11 RF P4MM 1 CLK32K_AP
- PP14 RF P4MM 1 AP_HSI_C1_RDY
- PP15 RF P4MM 1 WLAN_HSI_C3_DEVICE_RDY
- PP16 RF P4MM 1 WLAN_HSI_C3_RESUME
- PP19 RF P4MM-NSM 1 WTR_SSB1_TX_GPS
- PP20 RF P4MM-NSM 1 WTR_SSB1_PRX_DRX
- PP21 RF P4MM 1 WTR_RX_ON
- PP22 RF P4MM 1 WTR_RF_ON
- PP40 RF P4MM 1 WLAN_COEX_TXD
- PP41 RF P4MM 1 LTE_COEX_TXD
- PP42 RF P4MM 1 50_HSI_C1_BB_STROBE
- PP43 RF P4MM 1 50_HSI_C1_BB_DATA
- PP44 RF P4MM 1 50_HSI_C1_WLAN_STROBE
- PP45 RF P4MM 1 50_HSI_C1_WLAN_DATA
- PP46 RF P4MM 1 BT_UART_TXD
- PP47 RF P4MM 1 BT_UART_RXD
- PP4 RF P4MM 1 BB_I2S_CLK
- PP5 RF P4MM 1 BB_I2S_WS
- PP6 RF P4MM 1 BB_I2S_RXD
- PP7 RF P4MM 1 BB_I2S_TXD

- PP4 RF P4MM 1 BB_I2S_CLK
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- PP6 RF P4MM 1 BB_I2S_RXD
- PP7 RF P4MM 1 BB_I2S_TXD

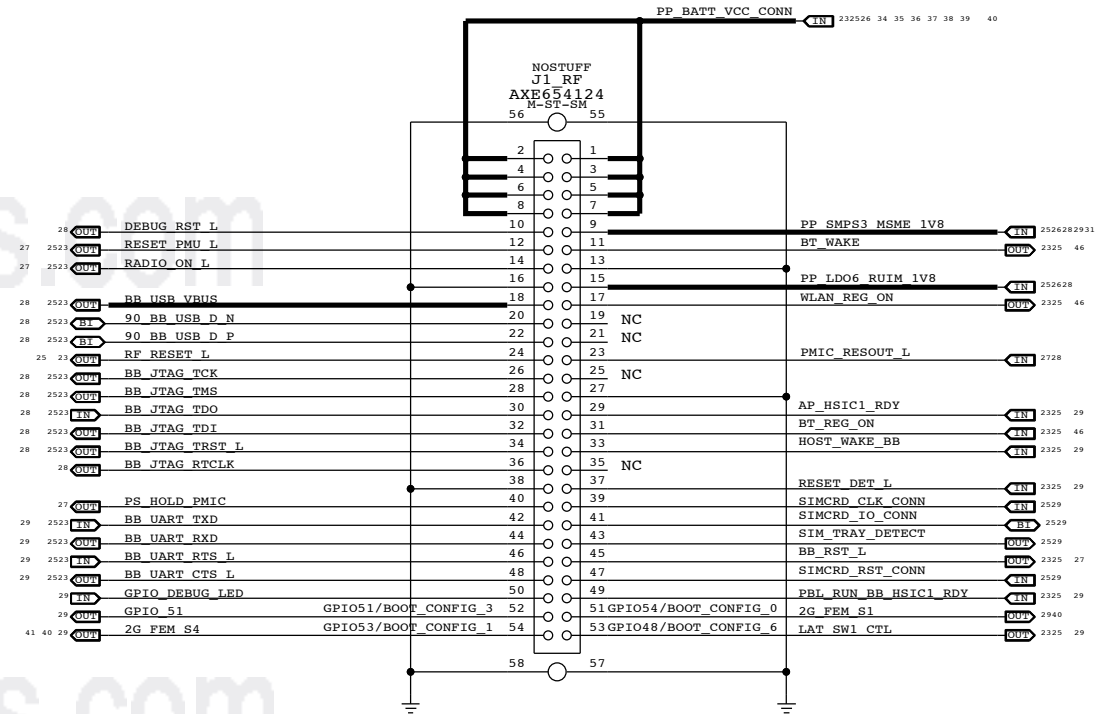
SIM CARD CONNECTOR



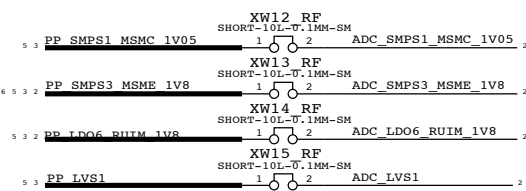
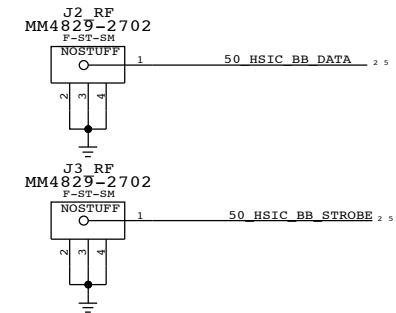
SIM CARD ESD PROTECTION



DEBUG CONNECTOR



| BOOT OPTIONS | BOOT CONFIG SW REGISTER VALUE | GPIO/BOOT_CONFIG CONFIGURATION | | | | | | | | |
|------------------------|-------------------------------|--------------------------------|---|---|---|---|---|---|---|---|
| | | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| BOOT_DEFAULT_OPTION | 0X00 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X |
| BOOT_NAND_OPTION | 0X01 | X | 1 | 0 | 0 | 0 | 0 | 0 | 1 | X |
| BOOT_HSI_C1_OPTION | 0X02 | X | 1 | 0 | 0 | 0 | 0 | 1 | 0 | X |
| BOOT_USB_OPTION | 0X03 | X | 1 | 0 | 0 | 0 | 0 | 1 | 1 | X |
| ENABLE_SAHARA_PROTOCOL | 0X08 | X | 1 | 0 | 0 | 1 | 0 | X | X | X |

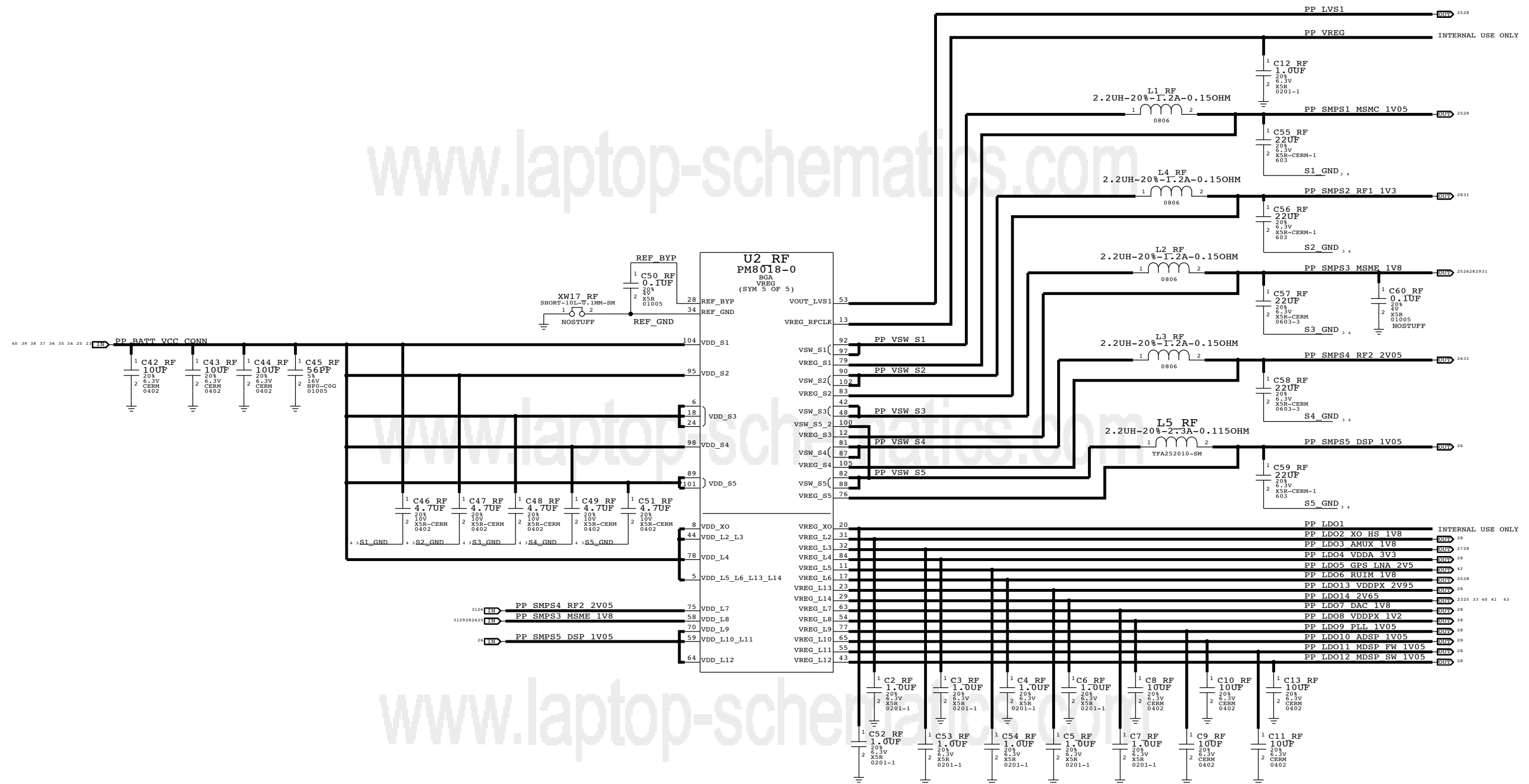


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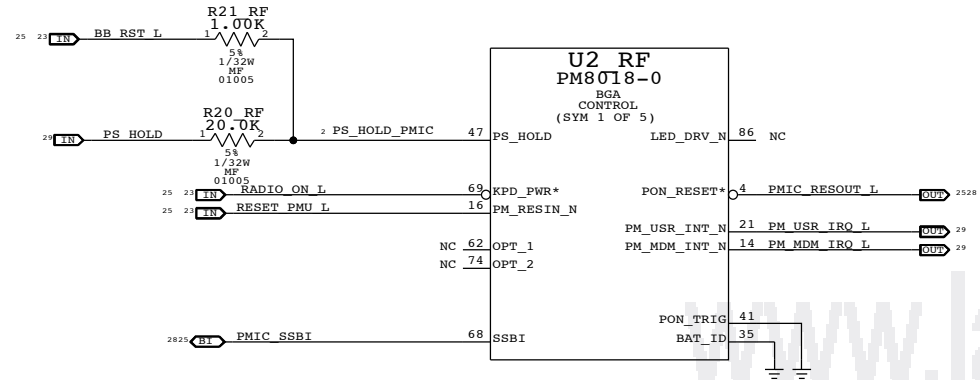
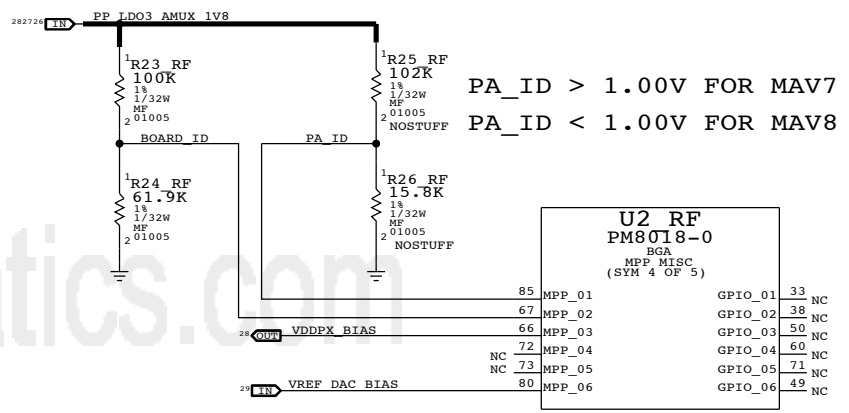
PMU (1 OF 2)



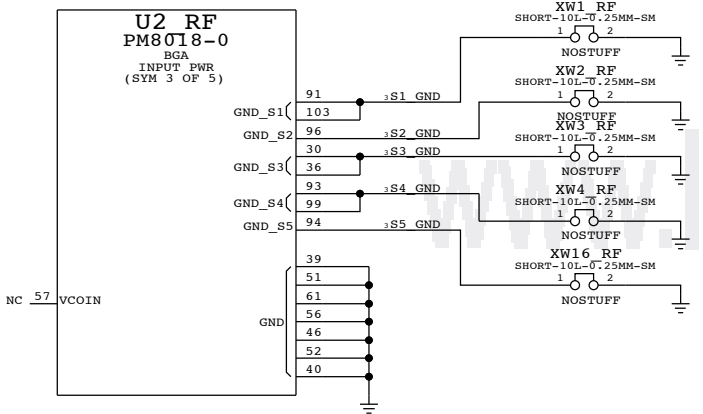
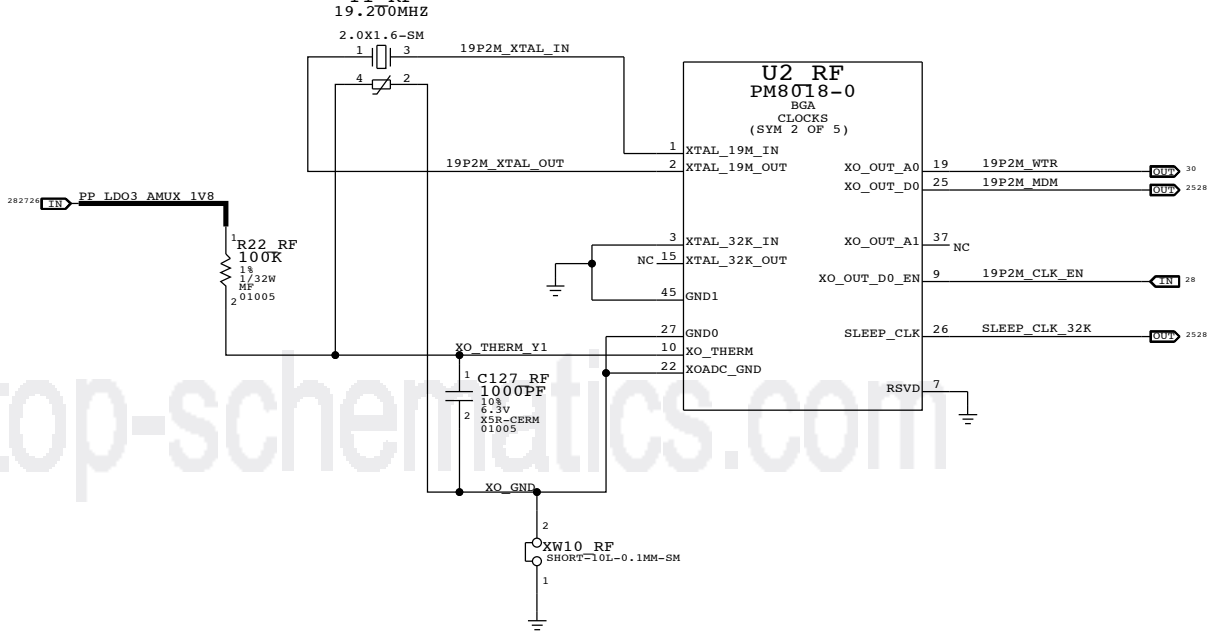
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| | SIZE | D |

PMU (2 OF 2)

| BOARD_ID | REVISION |
|----------|----------|
| 0.7V | PROTO1 |
| 0.9V | PROTO2 |
| 1.1V | EVT1 |
| 1.3V | EVT2 |
| 1.5V | DVT |
| 1.7V | PVT |



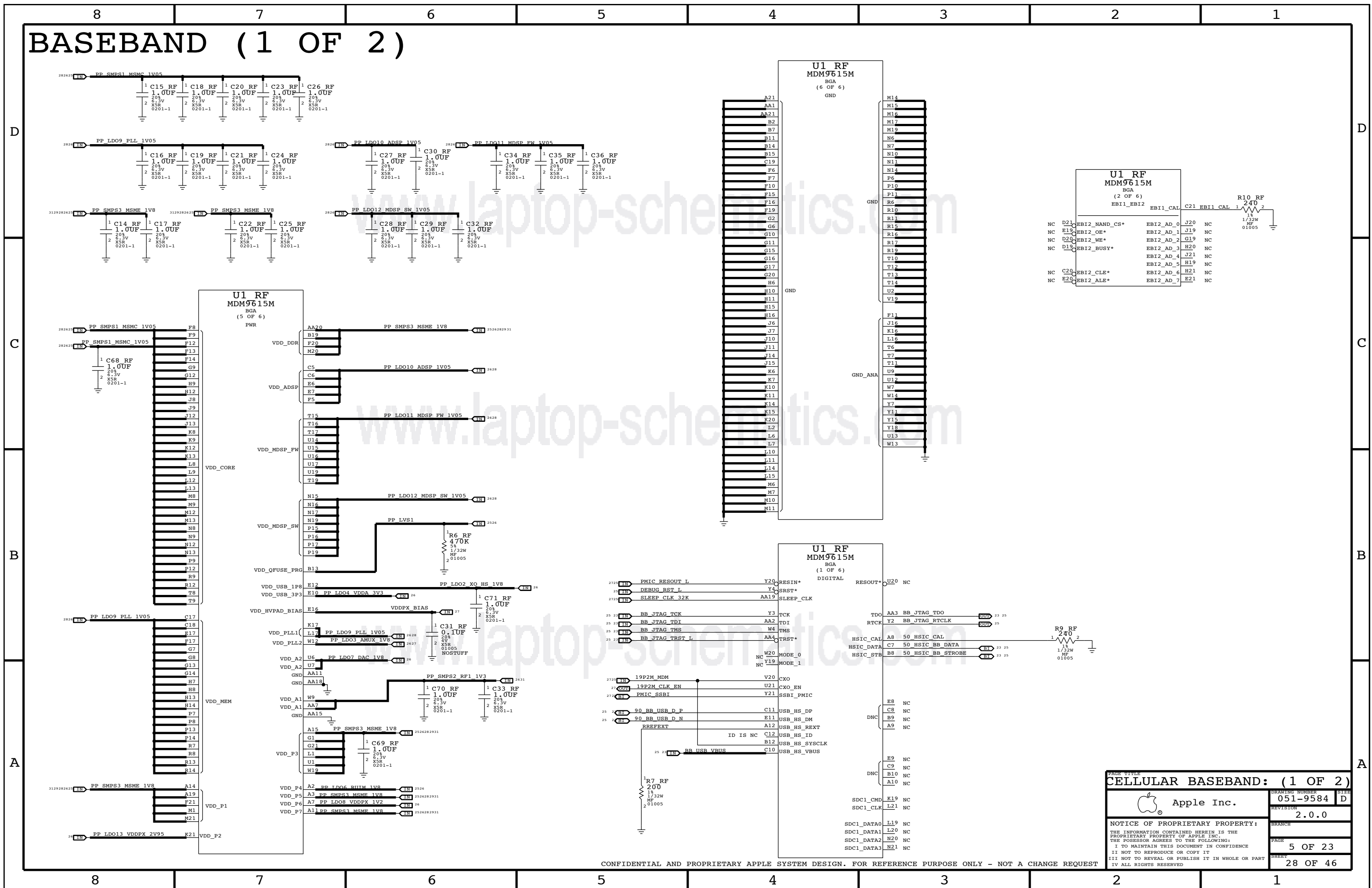
GND NEEDS TO BE CLEARED UNDER THIS CRYSTAL TO MINIMIZE THERMAL DRIFT



PA THERMISTOR REMOVED TO MATCH N41, AP SECTION NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.

| | | |
|--|----------------------------|-------------------|
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BASEBAND (1 OF 2)



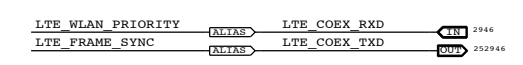
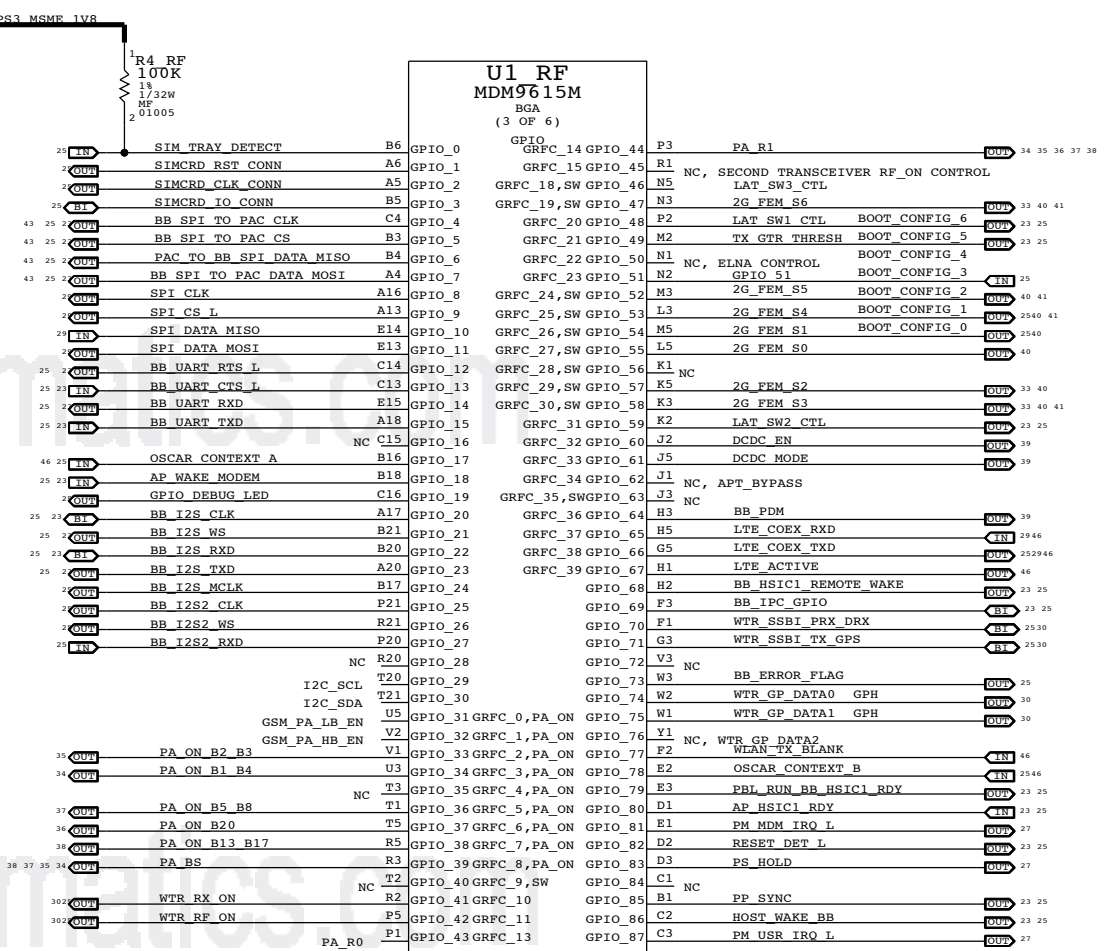
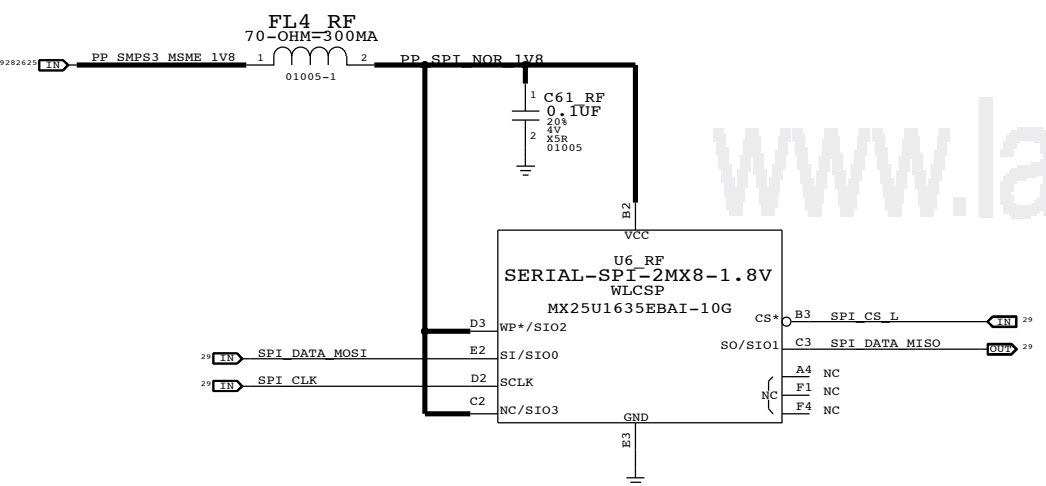
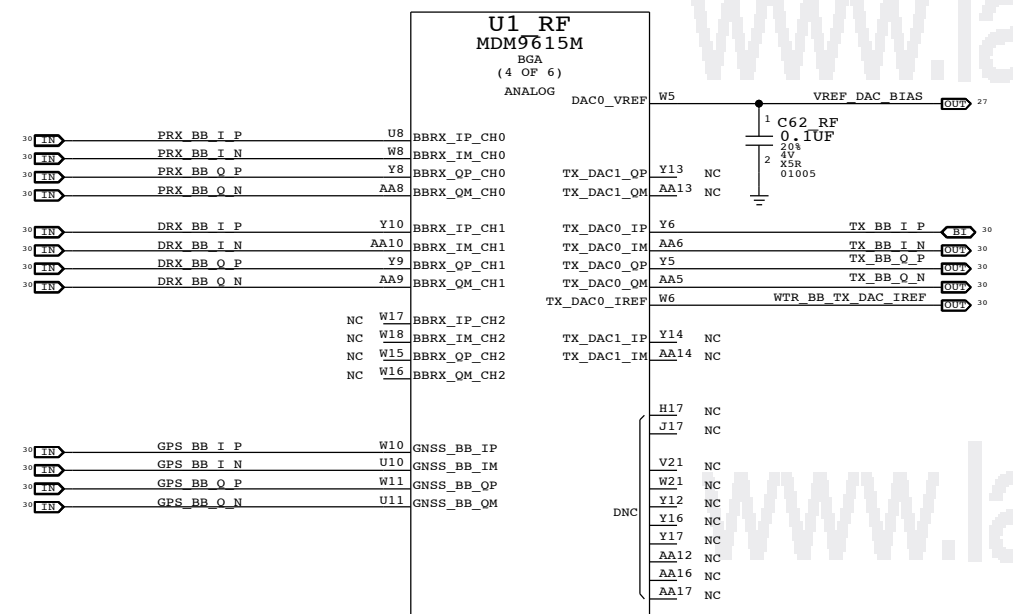
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CELLULAR BASEBAND: (2 OF 2)

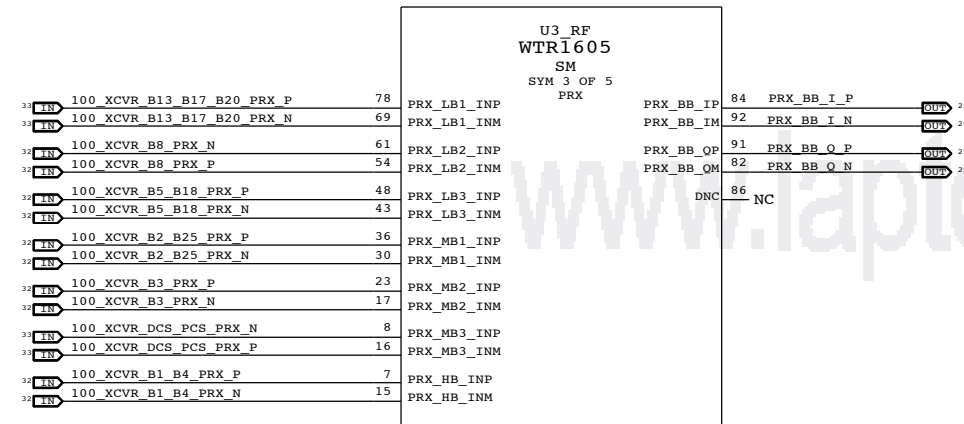
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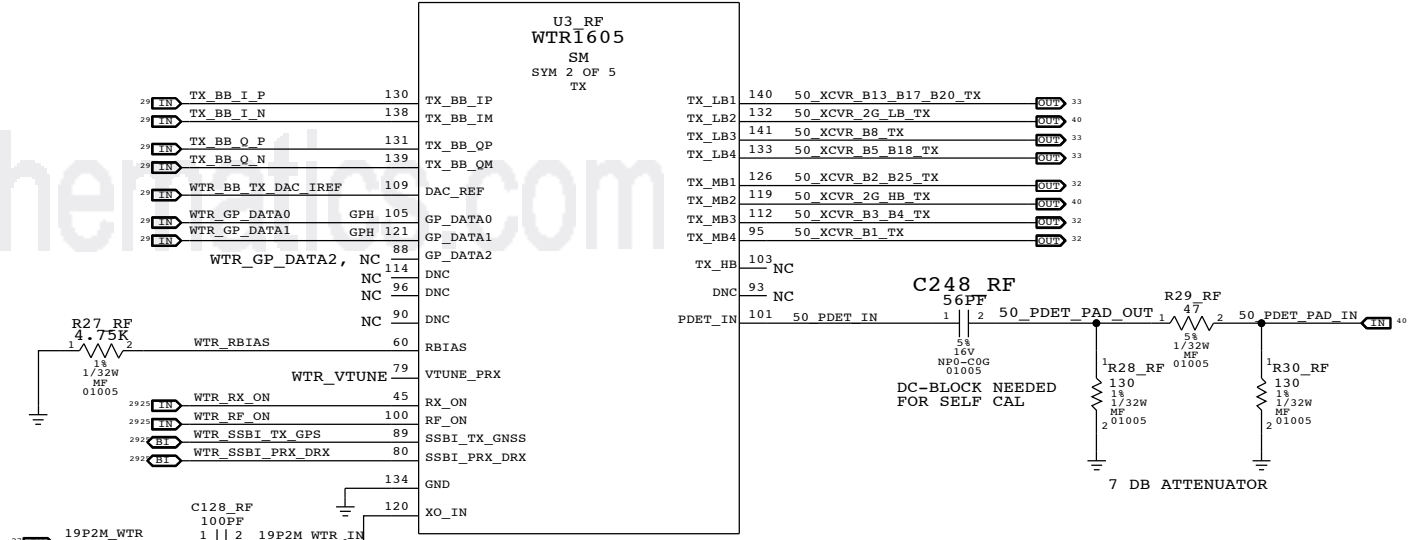
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SHEET: 29 OF 46

RF TRANSCEIVER (1 OF 4)

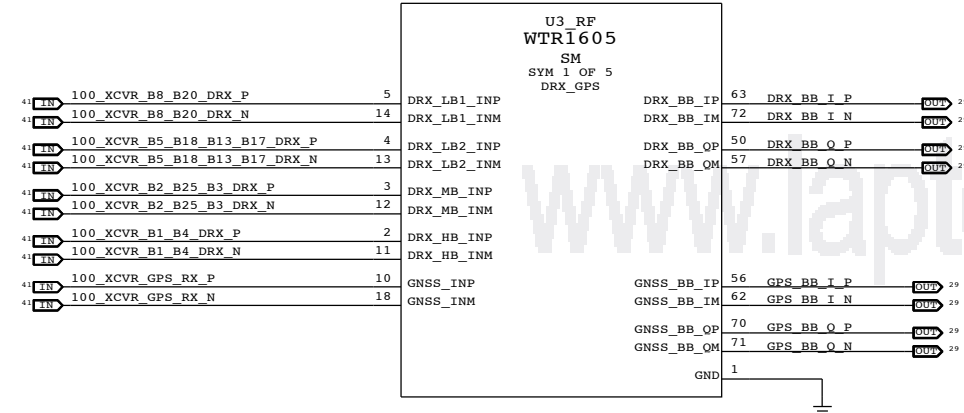
PRX TRANSCEIVER RF AND IQ PORTS



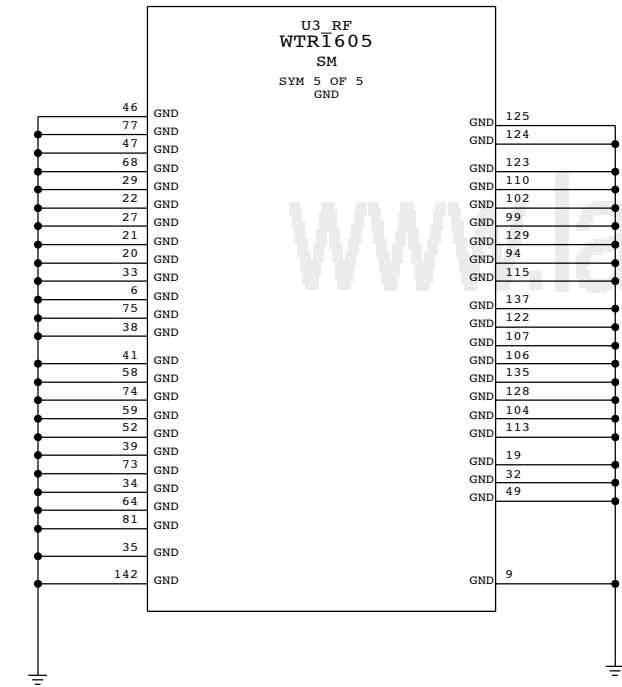
TRANSCEIVER PHASE CONTROL, TX RF & IQ PORTS



DRX TRANSCEIVER RF AND IQ PORTS



TRANSCEIVER GROUND CONNECTIONS



CELLULAR RF TRANSCEIVER: (1 OF 2)

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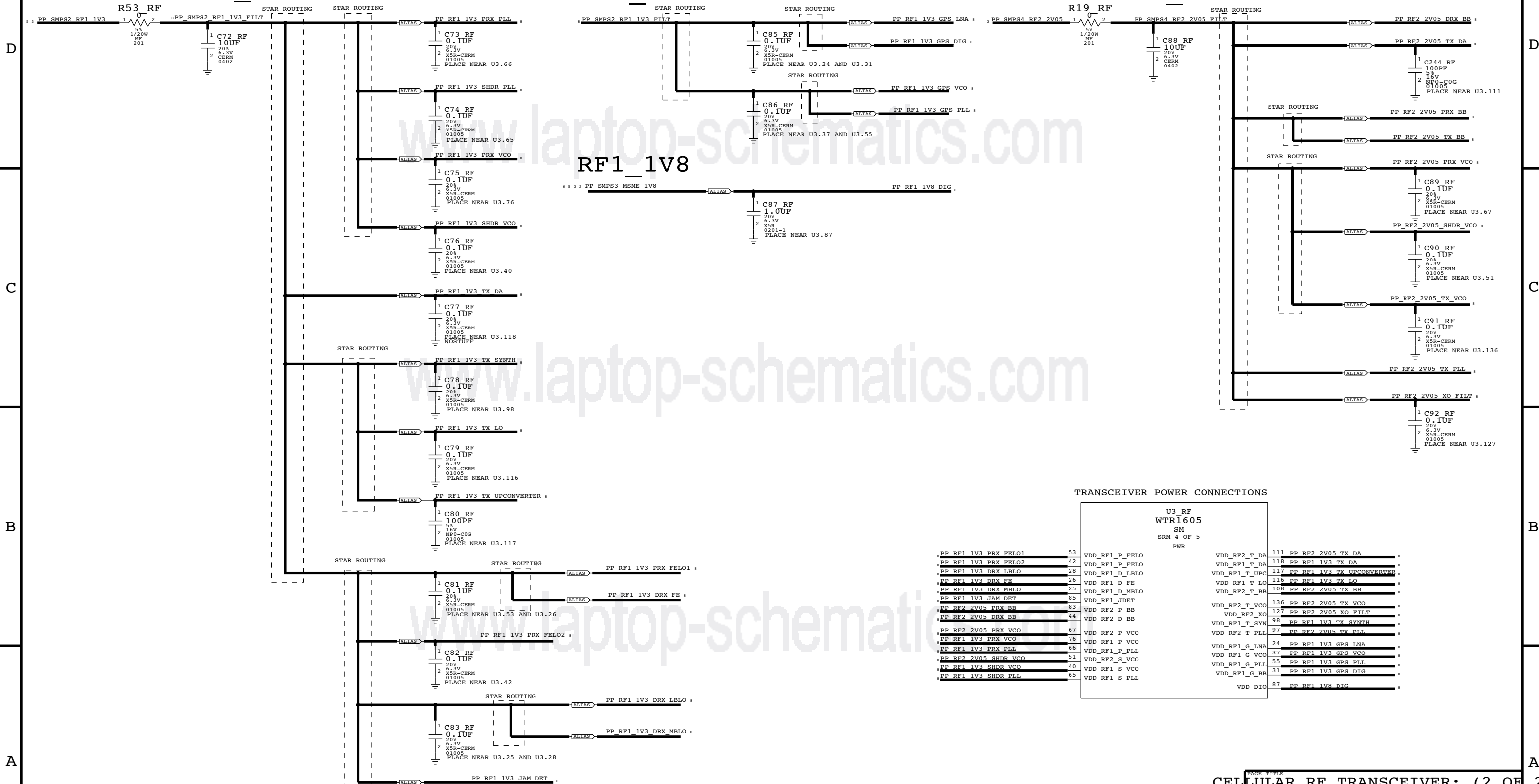
RF TRANSCEIVER (2 OF 2)

RF1_1V3

RF1_1V3

RF2_2V05

RF1_1V8



TRANSCEIVER POWER CONNECTIONS

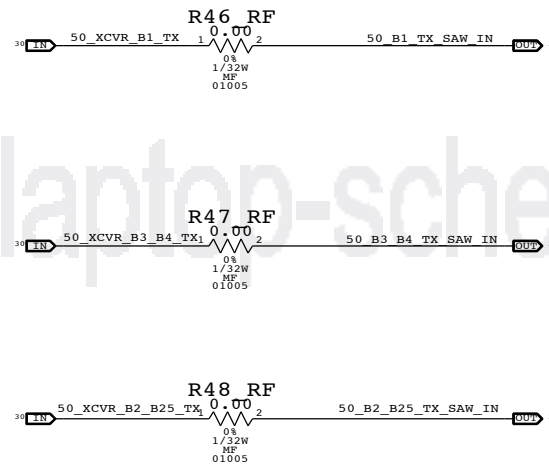
| U3_RF | | WTR1605 | | SM | | SRM 4 OF 5 | | PWR | |
|----------------------|----|----------------|--|---------------|-----|---------------------------|--|-----|--|
| PP RF1 1V3 PRX FELO1 | 53 | VDD_RF1_P_FELO | | VDD_RF2_T_DA | 111 | PP RF2 2V05 TX DA | | | |
| PP RF1 1V3 PRX FELO2 | 42 | VDD_RF1_P_FELO | | VDD_RF1_T_DA | 118 | PP RF1 1V3 TX DA | | | |
| PP RF1 1V3 DRX LBLO | 28 | VDD_RF1_D_LBLO | | VDD_RF1_T_UPC | 117 | PP RF1 1V3 TX UPCONVERTER | | | |
| PP RF1 1V3 DRX FE | 26 | VDD_RF1_D_FE | | VDD_RF1_T_LO | 116 | PP RF1 1V3 TX LO | | | |
| PP RF1 1V3 DRX MBLO | 25 | VDD_RF1_D_MBLO | | VDD_RF2_T_BB | 108 | PP RF2 2V05 TX BB | | | |
| PP RF1 1V3 JAM DET | 85 | VDD_RF1_JDET | | VDD_RF2_T_VCO | 136 | PP RF2 2V05 TX VCO | | | |
| PP RF2 2V05 PRX BB | 83 | VDD_RF2_P_BB | | VDD_RF2_XO | 127 | PP RF2 2V05 XO FILT | | | |
| PP RF2 2V05 DRX BB | 44 | VDD_RF2_D_BB | | VDD_RF1_T_SYN | 98 | PP RF1 1V3 TX SYNTH | | | |
| PP RF2 2V05 PRX VCO | 67 | VDD_RF2_P_VCO | | VDD_RF2_T_PLL | 97 | PP RF2 2V05 TX PLL | | | |
| PP RF1 1V3 PRX VCO | 76 | VDD_RF1_P_VCO | | VDD_RF1_G_LNA | 24 | PP RF1 1V3 GPS LNA | | | |
| PP RF1 1V3 PRX PLL | 66 | VDD_RF1_P_PLL | | VDD_RF1_G_VCO | 37 | PP RF1 1V3 GPS VCO | | | |
| PP RF2 2V05 SHDR VCO | 51 | VDD_RF2_S_VCO | | VDD_RF1_G_PLL | 55 | PP RF1 1V3 GPS PLL | | | |
| PP RF1 1V3 SHDR VCO | 40 | VDD_RF1_S_VCO | | VDD_RF1_G_BB | 31 | PP RF1 1V3 GPS DIG | | | |
| PP RF1 1V3 SHDR PLL | 55 | VDD_RF1_S_PLL | | VDD_DIO | 87 | PP RF1 1V8 DIG | | | |

CELLULAR RF TRANSCEIVER: (2 OF 2)

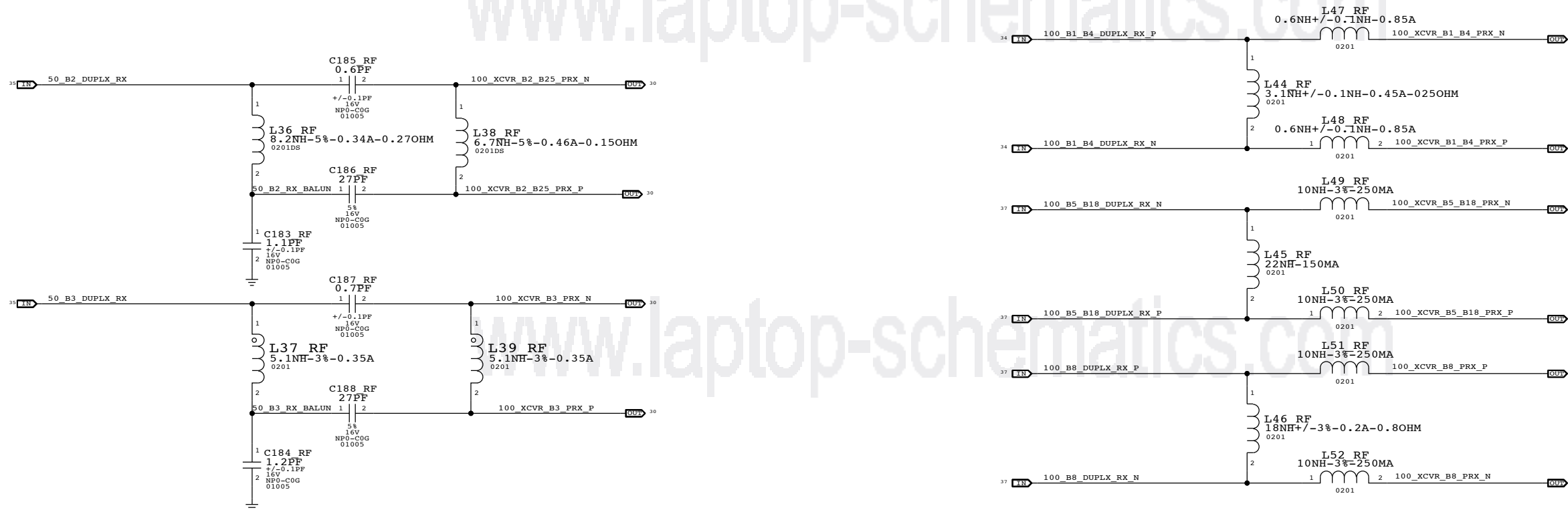
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TRANSCEIVER TX AND RX MATCHING

TX MATCHING NETWORKS



RX MATCHING NETWORKS



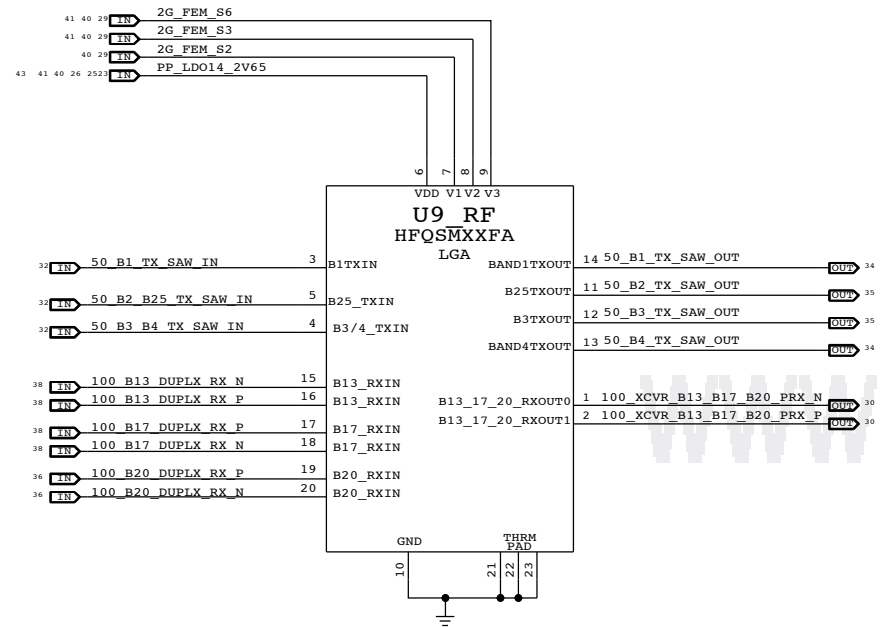
CELLULAR FRONT END: TX AND RX MATCHING

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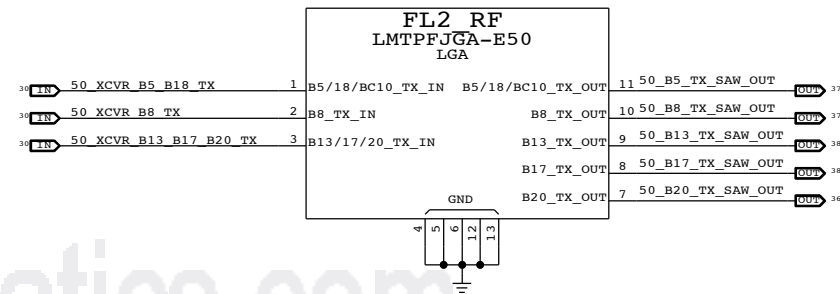
SAW BANKS

HB TX SAW BANK + B13/B17/B20 DP6T SWITCH AND MATCHING

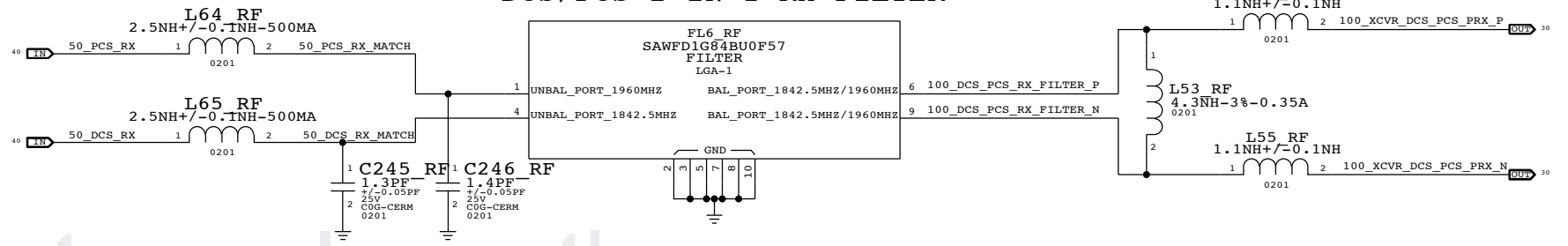


| BAND | S6 | S3 | S2 |
|--------|------|------|------|
| B3 TX | HIGH | X | X |
| B4 TX | LOW | X | X |
| B13 RX | X | HIGH | HIGH |
| B17 RX | X | HIGH | LOW |
| B20 RX | X | LOW | HIGH |

LB TX SAW BANK



DCS/PCS 2-IN-1 RX FILTER

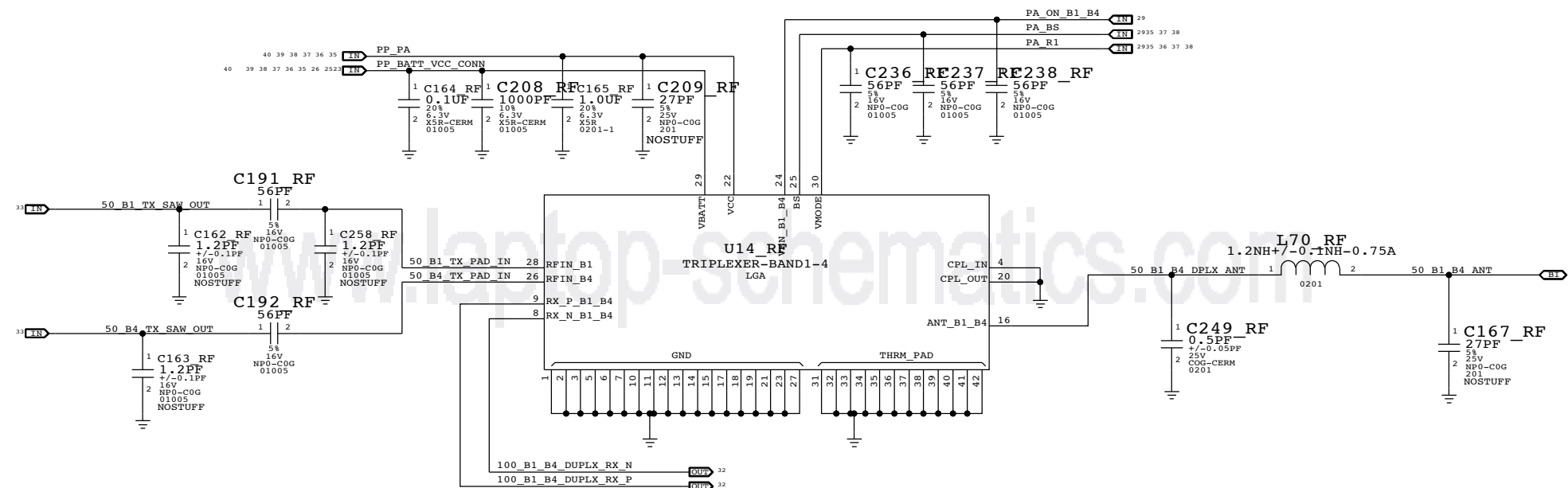


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BAND 1/4 PAT

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| BAND | PA POWER MODE | PA_BS | PA_ON_B1_B4 | PA_R1 |
|------------|---------------|-------|-------------|-------|
| POWER DOWN | X | 0 | 0 | 0 |
| STANDBY | X | X | 0 | X |
| B4 | HPM | 0 | 1 | 0 |
| B4 | LPM | 0 | 1 | 1 |
| B1 | HPM | 1 | 1 | 0 |
| B1 | LPM | 1 | 1 | 1 |

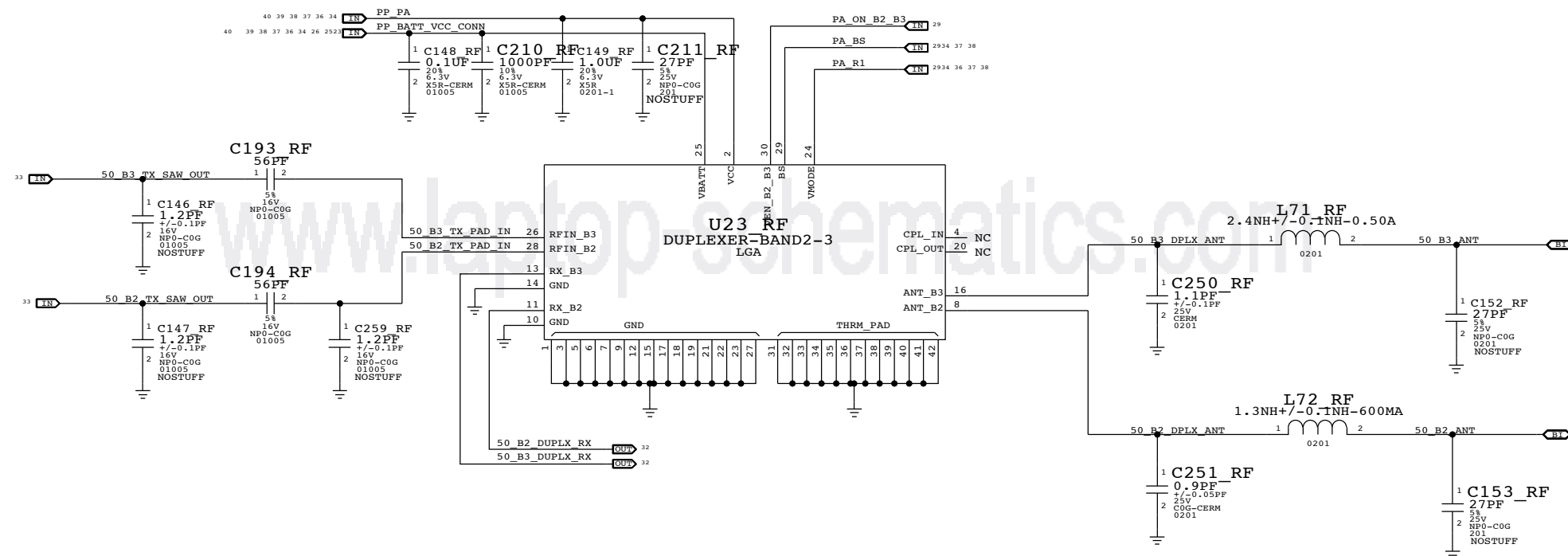
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BAND 2/3 PAD

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| BAND | PA POWER MODE | PA BS | PA_ON B2 B3 | PA R1 |
|------------|---------------|-------|-------------|-------|
| POWER DOWN | X | 0 | 0 | 0 |
| STANDBY | X | X | 0 | X |
| B3 | HPM | 0 | 1 | 0 |
| B3 | LPM | 0 | 1 | 1 |
| B2 | HPM | 1 | 1 | 0 |
| B2 | LPM | 1 | 1 | 1 |

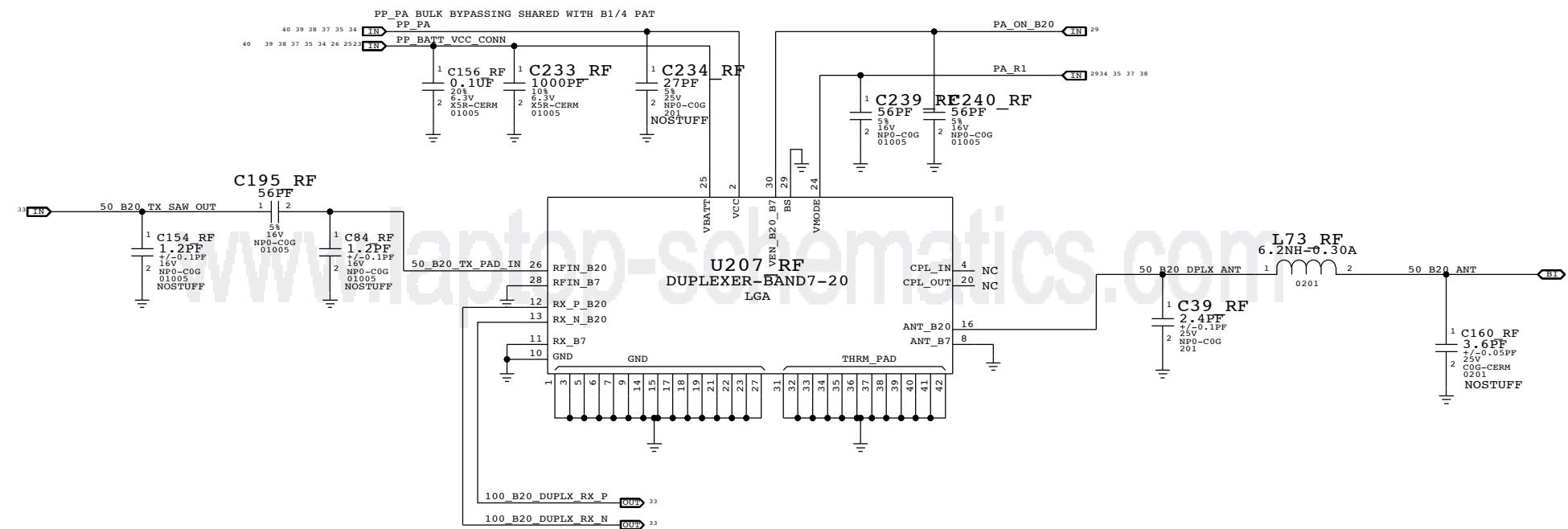
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BAND 20 PAD

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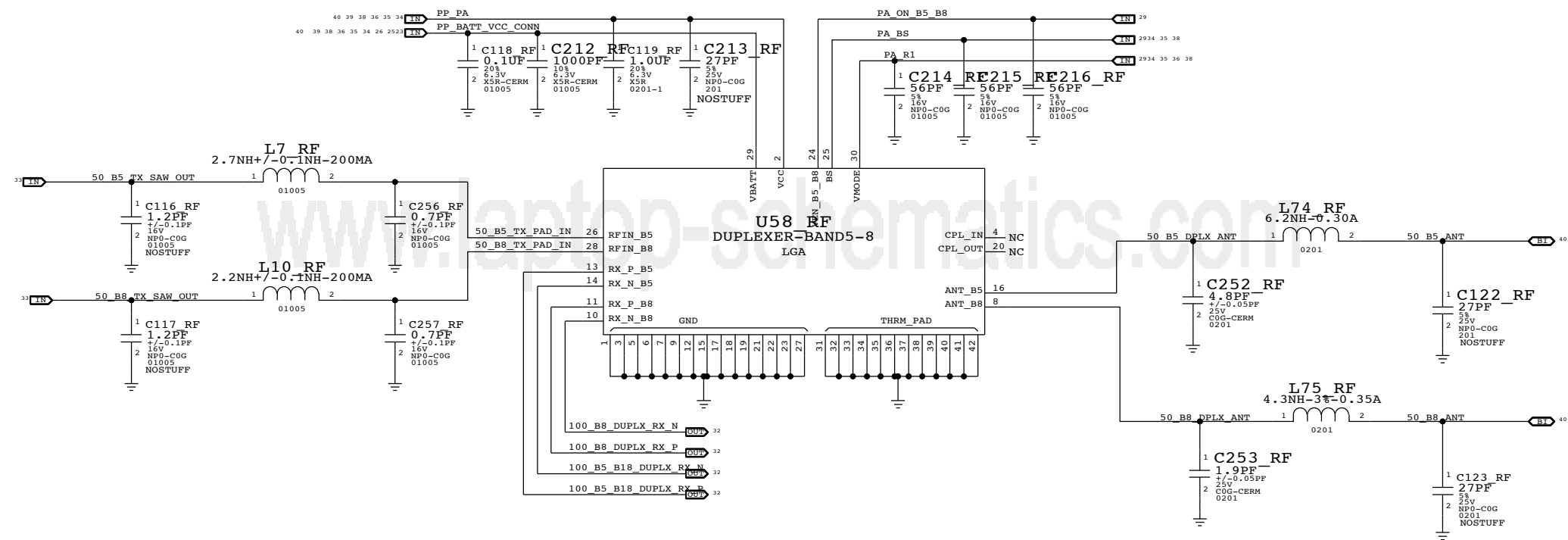
| BAND | PA POWER MODE | PA_ON_B20 | PA_R1 |
|------------|---------------|-----------|-------|
| POWER DOWN | LPM | 0 | 0 |
| STANDBY | X | 0 | X |
| B20 | HPM | 1 | 0 |
| B20 | LPM | 1 | 1 |

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| | | | | | |
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BAND 5/8 PAD

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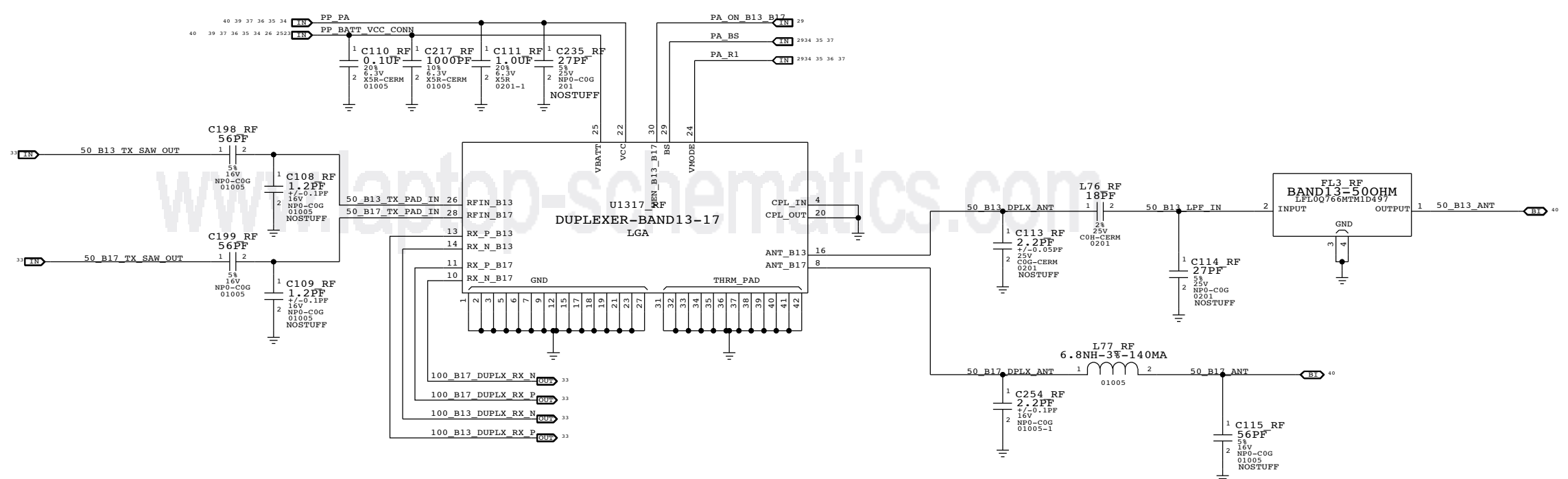
| BAND | PA POWER MODE | PA_BS | PA_ON_B5_B8 | PA_R1 |
|------------|---------------|-------|-------------|-------|
| POWER DOWN | X | 0 | 0 | 0 |
| STANDBY | X | X | 0 | X |
| B5 | HPM | 0 | 1 | 0 |
| B5 | LPM | 0 | 1 | 1 |
| B8 | HPM | 1 | 1 | 0 |
| B8 | LPM | 1 | 1 | 1 |

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| | | SHEET 37 OF 46 | |

BAND 13/17 PAD

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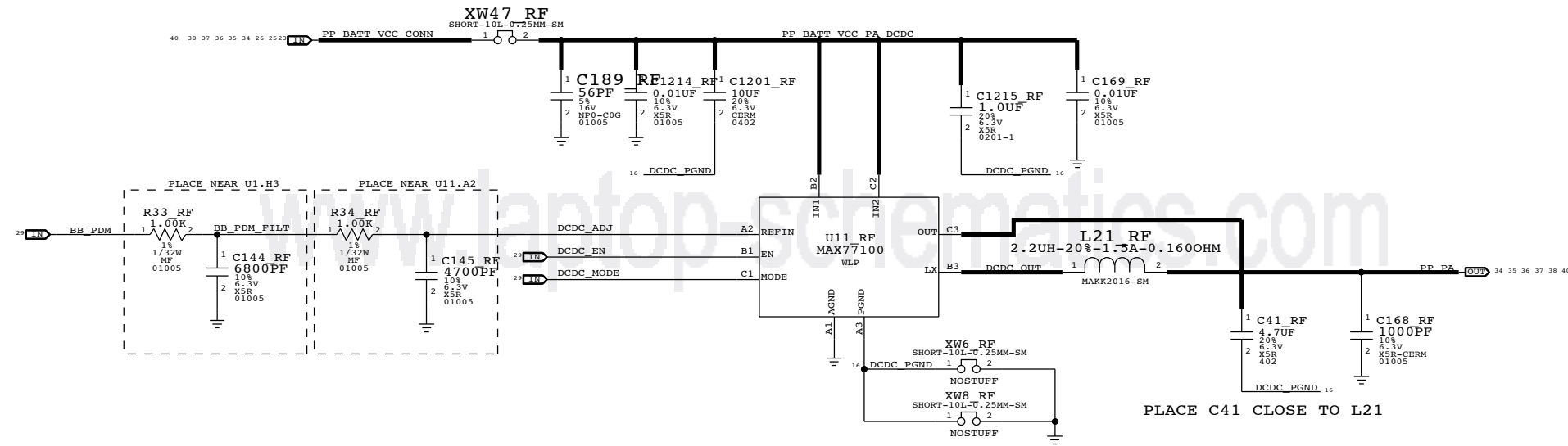
| BAND | PA POWER MODE | PA_BS | PA_ON_B13_B17 | PA_R1 |
|------------|---------------|-------|---------------|-------|
| POWER DOWN | X | 0 | 0 | 0 |
| STANDBY | X | X | 0 | X |
| B17 | HPM | 0 | 1 | 0 |
| B17 | LPM | 0 | 1 | 1 |
| B13 | HPM | 1 | 1 | 0 |
| B13 | LPM | 1 | 1 | 1 |

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PA DC/DC CONVERTER

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CELLULAR FRONT END: PA DCDC CONVERTER

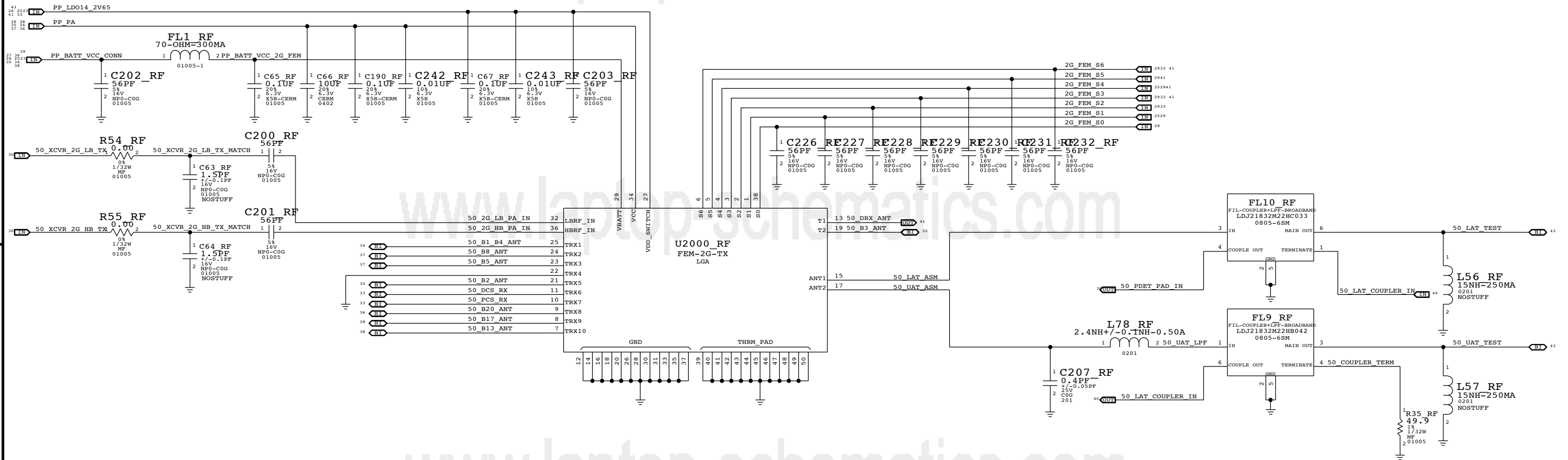
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2G FEM

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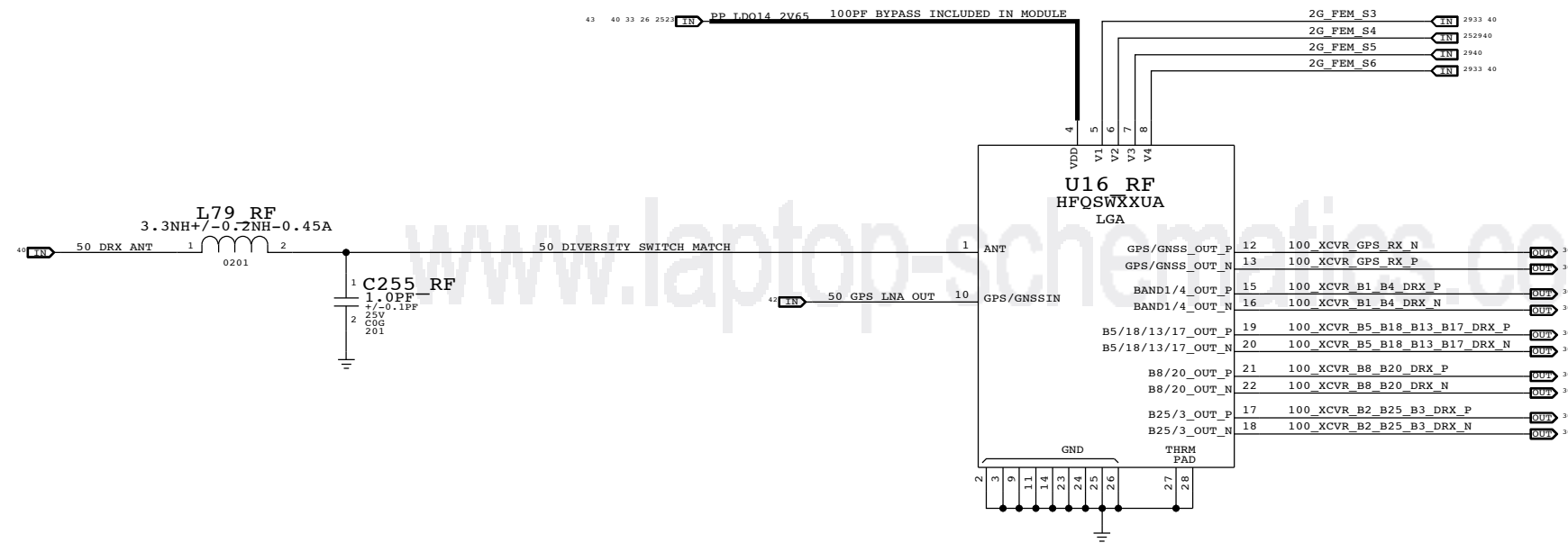


SEE PGS. 21-22 FOR 2G FEM LOGIC TABLE

| | | |
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| SHEET | 40 OF 46 | |

RX DIVERSITY

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| BAND | S6 | S5 | S4 | S3 |
|---------|------|------|------|------|
| B1/B4 | LOW | LOW | LOW | LOW |
| B2/25 | LOW | HIGH | LOW | LOW |
| B3 | HIGH | LOW | LOW | LOW |
| B5/6/18 | LOW | LOW | HIGH | LOW |
| B8 | LOW | LOW | LOW | HIGH |
| B13/17 | LOW | HIGH | HIGH | HIGH |
| B20 | LOW | HIGH | HIGH | LOW |
| OFF | LOW | LOW | HIGH | HIGH |

SWITCH IS TERMINATED IN ALL OTHER POSSIBLE STATES

CELLULAR FRONT END: RX DIVERSITY

Apple Inc.

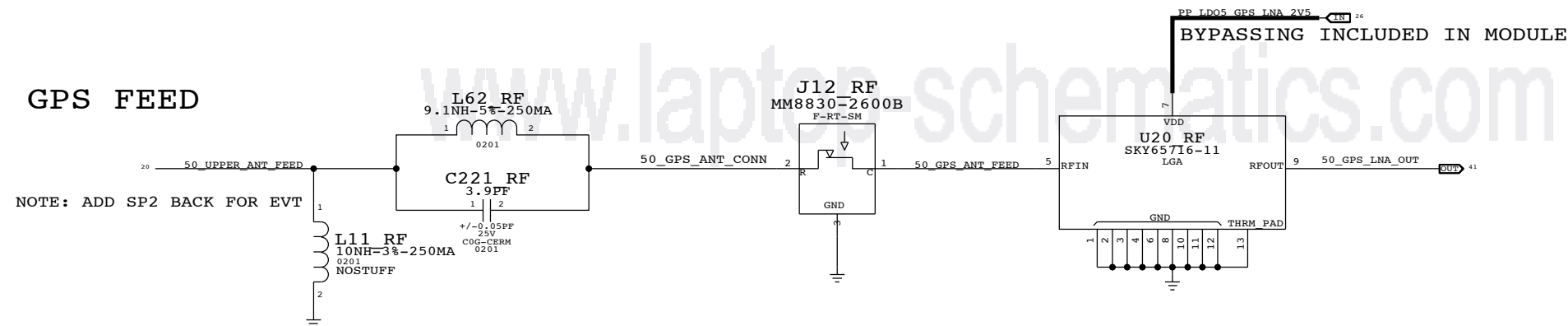
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GPS

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GPS FEED

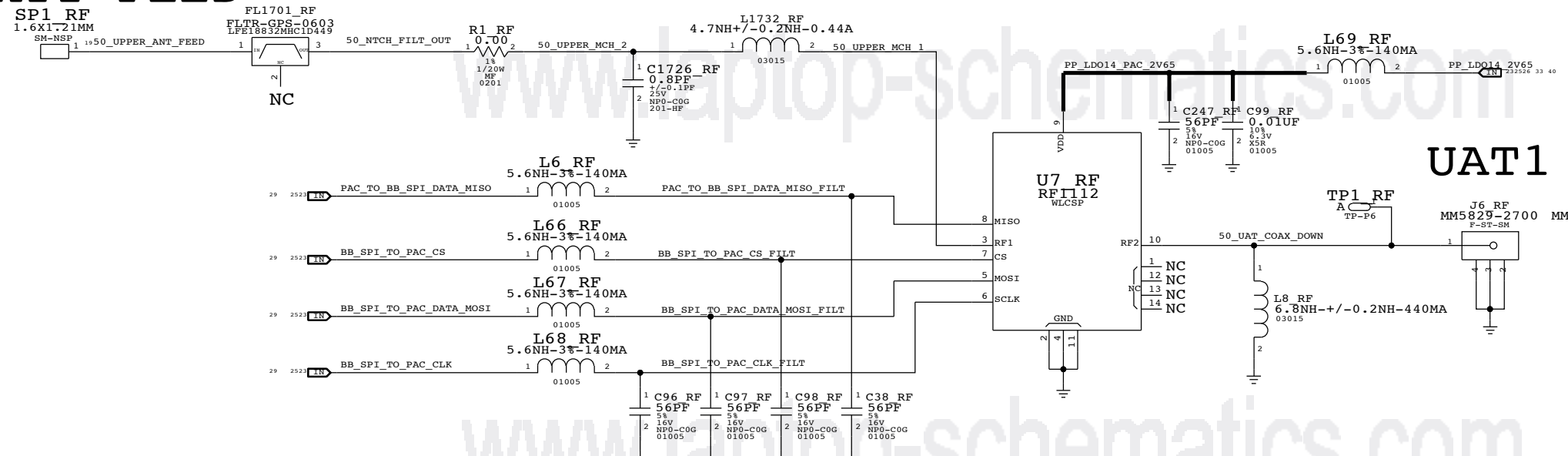


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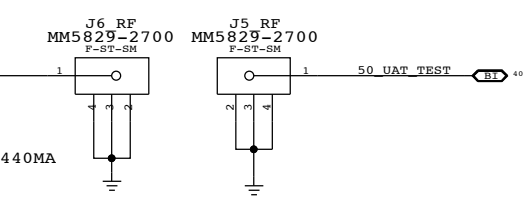
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| | | |

ANTENNA FEEDS

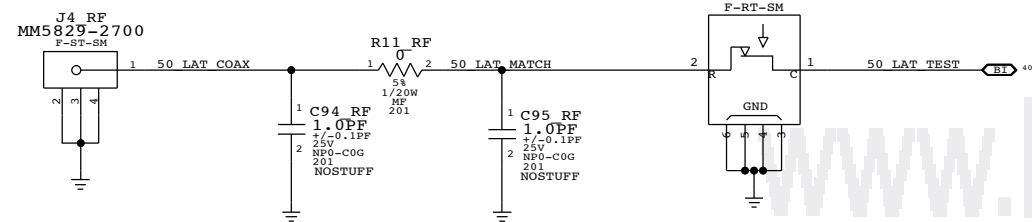
UAT1 FEED



UAT1 COAX



LAT



CELLULAR FRONT END: ANTENNA FEEDS


| | | | |
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| | | PAGE 20 OF 23 | SHEET 43 OF 46 |

FRONT END LOGIC TABLE (1 OF 2)

| BAND | S6 | S5 | S4 | S3 | S2 | S1 | S0 | TX/PRX PATH | DRX PATH |
|-------------------------|------|------|------|------|------|------|------|-------------|----------|
| LB TX, IDLE, LAT | HIGH | HIGH | HIGH | LOW | LOW | HIGH | HIGH | LAT | UAT |
| LB TX, IDLE, UAT | HIGH | HIGH | HIGH | LOW | LOW | LOW | HIGH | UAT | LAT |
| LB TX, LAT, HPM | HIGH | HIGH | HIGH | LOW | HIGH | HIGH | HIGH | LAT | UAT |
| LB TX, UAT, HPM | HIGH | HIGH | HIGH | LOW | HIGH | LOW | HIGH | UAT | LAT |
| LB TX, LAT, LPM | HIGH | HIGH | HIGH | LOW | HIGH | HIGH | LOW | LAT | UAT |
| LB TX, UAT, LPM | HIGH | HIGH | HIGH | LOW | HIGH | LOW | LOW | UAT | LAT |
| LB TX, HIGH Z, LAT, HPM | HIGH | HIGH | LOW | LOW | HIGH | HIGH | HIGH | LAT | UAT |
| LB TX, HIGH Z, UAT, HPM | HIGH | HIGH | LOW | LOW | HIGH | LOW | HIGH | UAT | LAT |
| LB TX, HIGH Z, LAT, LPM | HIGH | HIGH | LOW | LOW | HIGH | HIGH | LOW | LAT | UAT |
| LB TX, HIGH Z, UAT, LPM | HIGH | HIGH | LOW | LOW | HIGH | LOW | LOW | UAT | LAT |
| HB TX, IDLE, LAT | HIGH | HIGH | HIGH | HIGH | LOW | HIGH | HIGH | LAT | UAT |
| HB TX, IDLE, UAT | HIGH | HIGH | HIGH | HIGH | LOW | LOW | HIGH | UAT | LAT |
| HB TX, LAT, HPM | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | LAT | UAT |
| HB TX, UAT, HPM | HIGH | HIGH | HIGH | HIGH | HIGH | LOW | HIGH | UAT | LAT |
| HB TX, LAT, LPM | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | LOW | LAT | UAT |
| HB TX, UAT, LPM | HIGH | HIGH | HIGH | HIGH | HIGH | LOW | LOW | UAT | LAT |
| HB TX, HIGH Z, LAT, HPM | HIGH | HIGH | LOW | HIGH | HIGH | HIGH | HIGH | LAT | UAT |
| HB TX, HIGH Z, UAT, HPM | HIGH | HIGH | LOW | HIGH | HIGH | LOW | HIGH | UAT | LAT |
| HB TX, HIGH Z, LAT, LPM | HIGH | HIGH | LOW | HIGH | HIGH | HIGH | LOW | LAT | UAT |
| HB TX, HIGH Z, UAT, LPM | HIGH | HIGH | LOW | HIGH | HIGH | LOW | LOW | UAT | LAT |
| GSM850 RX, LAT | HIGH | LOW | HIGH | HIGH | LOW | HIGH | HIGH | LAT | UAT |
| GSM850 RX, UAT | HIGH | LOW | HIGH | HIGH | LOW | LOW | HIGH | UAT | LAT |
| GSM900 RX, LAT | HIGH | LOW | HIGH | HIGH | HIGH | HIGH | HIGH | LAT | UAT |
| GSM900 RX, UAT | HIGH | LOW | HIGH | HIGH | HIGH | LOW | HIGH | UAT | LAT |
| GSM1900 RX, LAT | LOW | HIGH | LOW | HIGH | HIGH | HIGH | HIGH | LAT | UAT |
| GSM1900 RX, UAT | LOW | HIGH | LOW | HIGH | HIGH | LOW | HIGH | UAT | LAT |
| GSM1800 RX, LAT | HIGH | LOW | LOW | HIGH | HIGH | HIGH | HIGH | LAT | UAT |
| GSM1800 RX, UAT | HIGH | LOW | LOW | HIGH | HIGH | LOW | HIGH | UAT | LAT |
| TERMINATED, UAT | HIGH | LOW | HIGH | LOW | HIGH | HIGH | HIGH | UAT | LAT |
| TERMINATED, LAT | HIGH | LOW | HIGH | LOW | HIGH | LOW | HIGH | LAT | UAT |

LAT = LOWER ANTENNA
 UAT = UPPER ANTENNA

FRONT END LOGIC TABLE (1 OF 2)

| | | |
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| | | SHEET 44 OF 46 |

FRONT END LOGIC TABLE - DEV2 (2 OF 2)

| BAND | S6 | S5 | S4 | S3 | S2 | S1 | S0 | TX/PRX PATH | DRX PATH |
|-------------------------|------|------|------|------|------|------|------|-------------|----------|
| B1/BC6, LAT | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH | LAT | UAT |
| B1/BC6, UAT | LOW | LOW | LOW | LOW | HIGH | LOW | HIGH | UAT | LAT |
| B2/B25/BC1, LAT | LOW | HIGH | LOW | LOW | HIGH | HIGH | HIGH | LAT | UAT |
| B2/B25/BC1, UAT | LOW | HIGH | LOW | LOW | HIGH | LOW | HIGH | UAT | LAT |
| B3, LAT | HIGH | LOW | LOW | LOW | HIGH | HIGH | HIGH | LAT | UAT |
| B3, UAT | HIGH | LOW | LOW | LOW | HIGH | LOW | HIGH | UAT | LAT |
| B4/BC15, LAT | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH | LAT | UAT |
| B4/BC15, UAT | LOW | LOW | LOW | LOW | HIGH | LOW | HIGH | UAT | LAT |
| B5/B6/B18/BC0/BC10, LAT | LOW | LOW | HIGH | LOW | HIGH | HIGH | HIGH | LAT | UAT |
| B5/B6/B18/BC0/BC10, UAT | LOW | LOW | HIGH | LOW | HIGH | LOW | HIGH | UAT | LAT |
| B8, LAT | LOW | LOW | LOW | HIGH | HIGH | HIGH | HIGH | LAT | UAT |
| B8, UAT | LOW | LOW | LOW | HIGH | HIGH | LOW | HIGH | UAT | LAT |
| B13, LAT | LOW | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | LAT | UAT |
| B13, UAT | LOW | HIGH | HIGH | HIGH | HIGH | LOW | HIGH | UAT | LAT |
| B17, LAT | LOW | HIGH | HIGH | HIGH | LOW | HIGH | HIGH | LAT | UAT |
| B17, UAT | LOW | HIGH | HIGH | HIGH | LOW | LOW | HIGH | UAT | LAT |
| B20, LAT | LOW | HIGH | HIGH | LOW | HIGH | HIGH | HIGH | LAT | UAT |
| B20, UAT | LOW | HIGH | HIGH | LOW | HIGH | LOW | HIGH | UAT | LAT |
| OFF | LOW | LOW | HIGH | HIGH | X | X | X | X | X |
| STANDBY | LOW | LOW | LOW | LOW | LOW | LOW | LOW | X | X |

LAT = LOWER ANTENNA

UAT = UPPER ANTENNA

OFF = LOWEST POWER STATE WITHOUT REMOVING LDO14_2V65 POWER

STANDBY = ADDED TO SUPPORT EXISTING SW ARCHITECTURE. NOT TO BE USED AS A LOW POWER STATE.

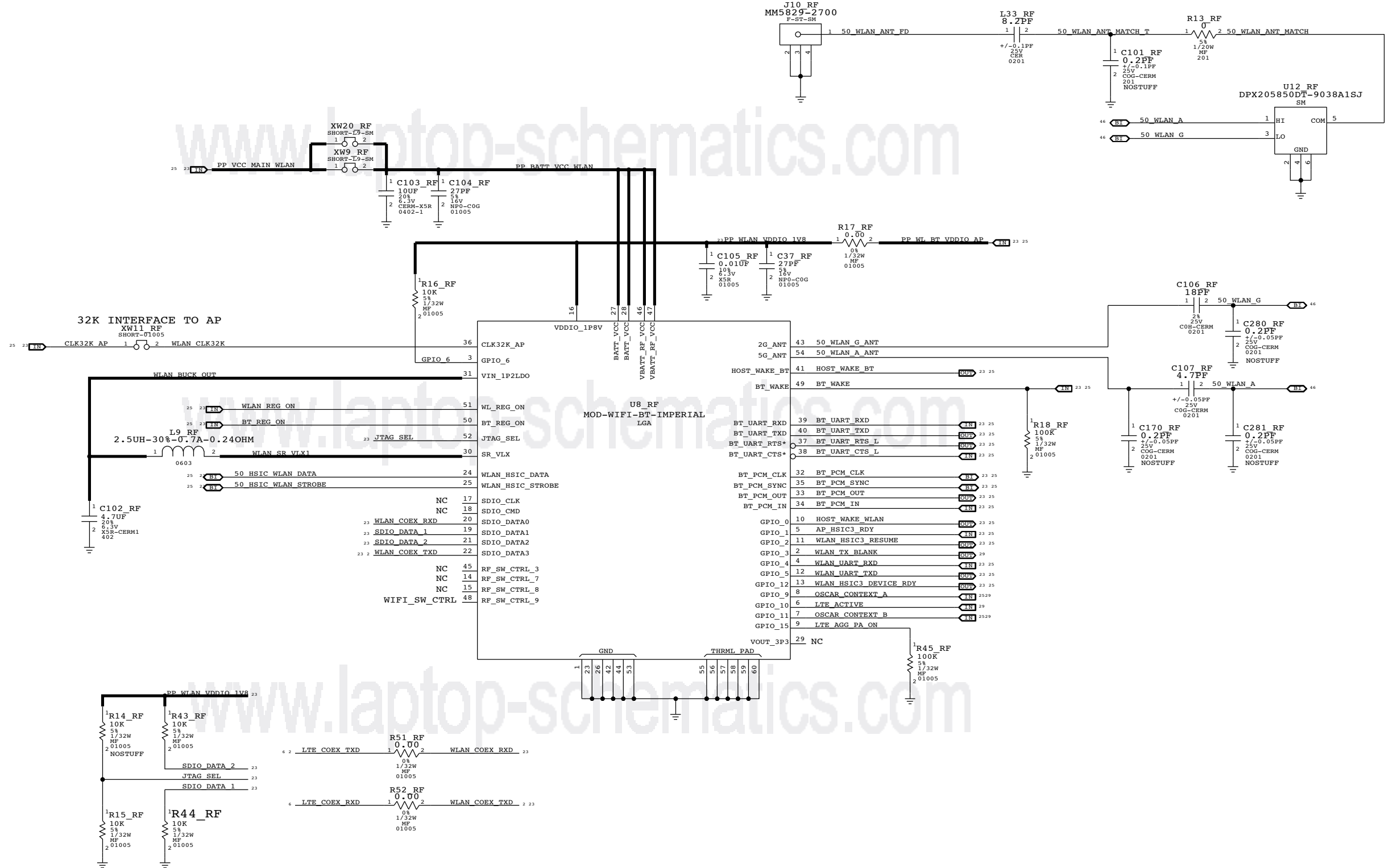
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WLAN/BT

UAT2



PULL-UP ON GPIO6, SDIO_DATA_2 & PULL-DOWN ON SDIO_DATA_1 REQUIRED FOR HSIC BOOTSTRAPPING

| PAGE TITLE | | DRAWING NUMBER | | SIZE |
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